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PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL.

7B90P
PROGRAMMABLE TIME BASE

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

070-2309-00
Product Group 42

Serial Number ____________

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INSTRUMENT SERIAL NUMBERS

Each instrument has a serial number on a panel insert, tag, or stamped on the chassis. The first number or letter designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

B000000	Tektronix, Inc., Beaverton, Oregon, USA
100000	Tektronix Guernsey, Ltd., Channel Islands
200000	Tektronix United Kingdom, Ltd., London
300000	Sony/Tektronix, Japan
700000	Tektronix Holland, NV, Heerenveen, The Netherlands

TABLE OF CONTENTS

WARNING

The remaining portion of this table of contents lists the Servicing instructions. These Servicing instructions are for use by qualified personnel only. To avoid electrical shock, do not perform any servicing other than that called out in the Operating instructions unless qualified to do so.

SECTION 4 - MAINTENANCE

REV A JULY 1979

SECTION 6 - CALIBRATION

SAFETY SUMMARY

This manual contains safety information which the user must follow to ensure safe operation of this instrument. WARNING information is intended to protect the operator; CAUTION information is intended to protect the instrument. The following are general safety precautions that must be observed during all phases of operation and maintenance.

WARNING

Ground the Instrument

To reduce electrical-shock hazard, the mainframe (oscilloscope) chassis must be properly grounded. Refer to the mainframe manual for grounding information.

Do Not Operate in Explosive Atmosphere

Do not operate this instrument in an area where flammable gases or fumes are present. Such operation could cause an explosion.

Avoid Live Circuits

Electrical-shock hazards are present in this instrument. The protective instrument covers must not be removed by operating personnel. Component replacement and internal adjustments must be referred to qualified service personnel.

Do Not Service or Adjust Alone

Do not service or make internal adjustments to this instrument unless another person, capable of giving first aid and resuscitation, is present.

WARNING

Warning Statements

Warning statements accompany potentially dangerous procedures in this manual. The following warnings appear in this manual and are listed here for additional emphasis.

To avoid electrical shock, disconnect the instrument from the power source before soldering.

To avoid electrical shock, disconnect the instrument from the power source before replacing components.

PREFACE

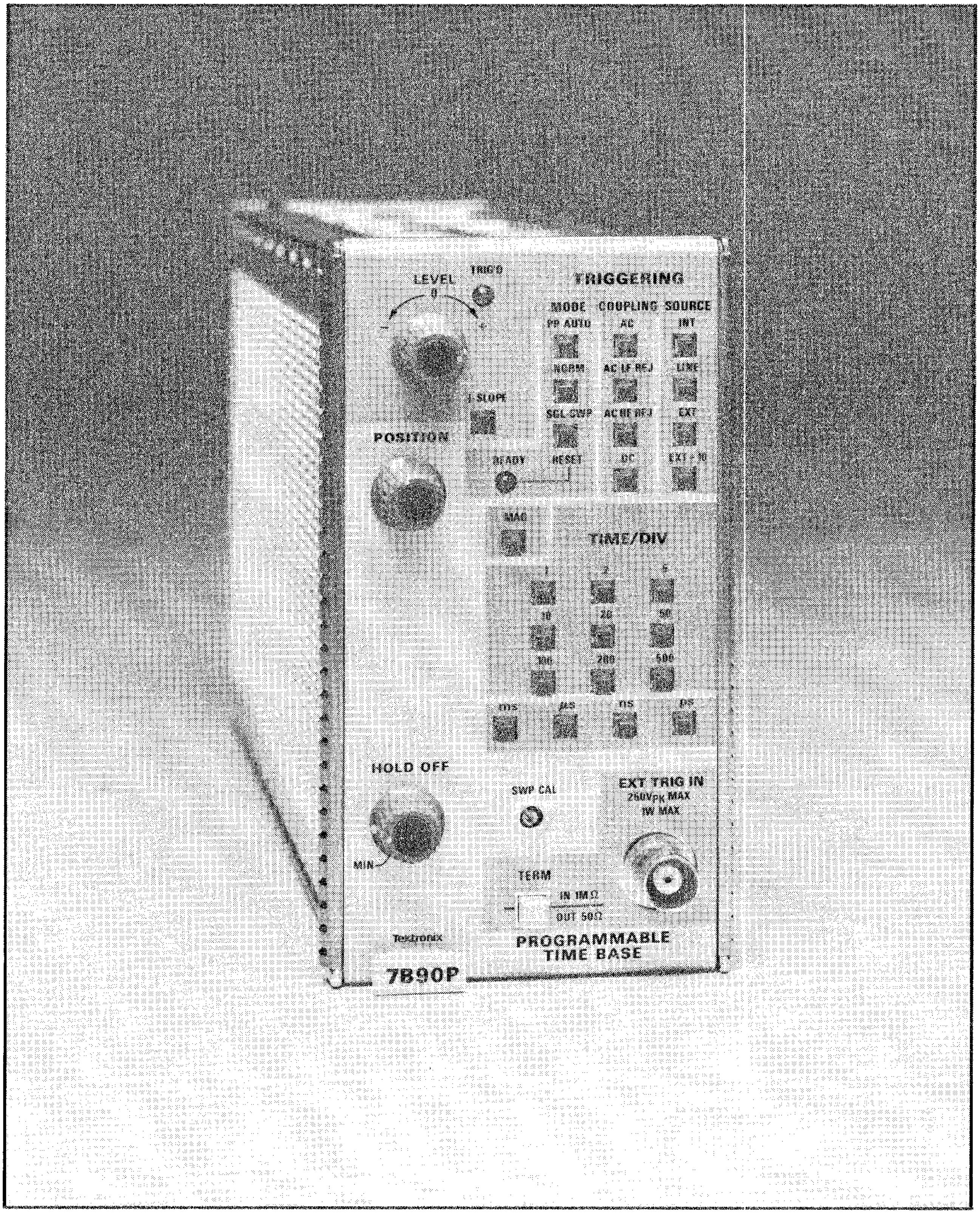
This manual contains two main divisions: operation and service. These divisions are separated by a heavy divider page. Information following this divider sheet is intended for qualified service personnel only.

The first division (operator's portion) begins with an introductory section that briefly describes the 7B90P Programmable Time Base. Specifications and programmable features of the plug-in are also listed. Section 2 describes each of the front-panel controls and connectors, and gives complete instructions for manual operation of the plug-in. Measuring techniques and applications are also discussed in Section 2. The last section of the operator's portion describes programmable operation of the 7B90P via the IEEE 488 Interface Bus, also known as the General Purpose Interface Bus (GPIB).* A complete list of device mnemonics is provided in this section.

The second division of the manual (service portion) begins with a section on preventive and corrective maintenance. Included in this section are some general troubleshooting procedures. Section 5 then provides a detailed circuit description of both the analog and digital portions of the 7B90P. Section 6 is a calibration procedure; it lists the equipment needed, and the steps required, for calibrating the instrument within specified limits. The remaining three sections provide electrical parts lists, schematic diagrams, and mechanical parts lists.

At the back of the manual is a removable sheet which serves as a pocket programming aid. It lists all of the high-level mnemonic codes and low-level hexadecimal codes for exercising programmable control of the 7B90P Programmable Time Base.

*Detailed information on the IEEE 488 bus is provided in IEEE Standard 488-1975, published by the Institute of Electrical & Electronics Engineers--345 E. 47 Street, New York, NY 10017.



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The 7B90P Programmable Time Base

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SECTION 1

INTRODUCTION

The TEKTRONIX 7B90P Programmable Time Base provides calibrated sweep rates for TEKTRONIX 7000-Series programmable mainframes. The 7B90P may be inserted in any 7000-Series mainframe without damage, but is recommended for use only in a programmable mainframe.

The 7B90P has calibrated sweep rates ranging from 500 picoseconds/division to 500 milliseconds/division. Other operating features that can be selected are: normal or automatic triggering, high or low frequency roll-off (attenuation) of the triggering signal, variable trigger hold-off, internal or external triggering, 1X or 10X sweep magnification, and repetitive or single-sweep mode.

The 7B90P has readout encoding capability. Thus, horizontal scale factors can be displayed on a programmable mainframe having readout display capability.

All functions of the 7B90P can be remotely programmed except for the Sweep Calibration (SWP CAL) adjustment and the External Trigger Input Termination (TERM) switch. The status of each programmable function can be set or read by commands sent over the IEEE 488 bus. These commands can be sent in either a high-level or low-level language, both of which are decoded by a microprocessor in the 7B90P.

Specifications

The following tables describe the electrical, programming, environmental, and physical specifications of the 7B90P. Characteristics whose specifications are checked in the calibration procedure are listed under a column entitled PERFORMANCE REQUIREMENTS. Specifications for all other characteristics are listed under SUPPLEMENTAL INFORMATION. Information in the SUPPLEMENTAL INFORMATION column is of a general nature and should not be considered as performance requirements. In cases where a particular plug-in specification is mainframe dependent, a note has been included referencing the manual for the mainframe.

TABLE 1-1

ELECTRICAL SPECIFICATIONS

Sweep Generator

<table>
<tr><th>CHARACTERISTICS</th><th colspan="4">PERFORMANCE REQUIREMENTS</th><th>SUPPLEMENTAL</th></tr>
<tr><td>Sweep Speeds</td><td colspan="4">500 ms/div to 10 ns/div, 24 calibrated steps in a 1-2-5 sequence. Magnifier switch extends fastest sweep speed to 500 ps/div. Fastest sweep speed can not be faster than that of the mainframe.</td><td>See mainframe-manual specifications for usable ranges.</td></tr>
<tr><td>Sweep Accuracy (in 7000-Series programmable mainframe)</td><td colspan="4">Following measurements are made with SWP CAL adjusted at 1 ms/div within temperature range of +20 to +30°C to a timing reference of 0.25% or better.</td><td>See mainframe-manual specifications for usable ranges.</td></tr>
<tr><td rowspan="2">Over Center 8 Divisions</td><td colspan="2">+15 to +35°C</td><td colspan="2">0 to +50°C</td><td rowspan="2"></td></tr>
<tr><td>Unmag</td><td>Mag</td><td>Unmag</td><td>Mag</td></tr>
<tr><td>500 ms/div to 100 ns/div</td><td>2.0%</td><td>3.0%</td><td>3.0%</td><td>4.0%</td><td></td></tr>
<tr><td>50 ns/div to 10 ns/div</td><td>3.0%</td><td>4.0%</td><td>4.0%</td><td>5.0%</td><td></td></tr>
<tr><td>500 ps/div</td><td>----</td><td>5.0%</td><td>----</td><td>6.0%</td><td></td></tr>
<tr><td>Excluded Part of Sweep</td><td colspan="4"></td><td></td></tr>
<tr><td>Start of Sweep</td><td colspan="4">First 10 nanoseconds in 7900-Series programmable mainframe.</td><td></td></tr>
<tr><td rowspan="2">End of Sweep</td><td colspan="4">Beyond 10th division, unmagnified.</td><td rowspan="2"></td></tr>
<tr><td colspan="4">Beyond 100th division, magnified.</td></tr>
</table>

TABLE 1-1 (cont.)

CHARACTERISTICS	PERFORMANCE REQUIREMENTS		SUPPLEMENTAL
Sweep Length (unmagnified)	At least 10.2 divisions at all sweep speeds.		
Position Range (at 1 ms/div)			
Programmed POS Ø (high-level mnemonic) or POSITION control at midrange.			Sweep starts 5 divisions to left of graticule center ±1.0 divisions.
Programmed POS 6.4 or POSITION control fully clockwise.			Sweep starts 1.4 divisions to right of graticule center ±1.0 divisions.
Programmed POS -6.39 or POSITION control fully counterclockwise.			Sweep starts 11.39 divisions to left of graticule center ±1.0 divisions.
Programmed Step Size			0.0125 div (80 steps/div) unmagnified; 0.125 div (8 steps/div) magnified.
Trigger Hold-off Time	Min (ccw)	Max (cw)	When operated in 7912AD, Hold-off is disabled at some sweep speeds.
500 ps/div to 2 μs/div	≤3.5 μs	≥90 μs	
5 μs/div to 20 μs/div	≤3.5 μs	≥900 μs	
50 μs/div to 200 μs/div	≤350 μs	≥9.0 ms	
500 μs/div to 2 ms/div	≤3.5 ms	≥90 ms	
5 ms/div to 500 ms/div	≤35 ms	≥900 ms	
Programmed Range			Min. = programmed HOL Ø Max. = programmed HOL 63
Programmed Resolution			62 steps between min. and max.

TABLE 1-1 (cont.)

Triggering

CHARACTERISTICS	PERFORMANCE REQUIREMENTS			SUPPLEMENTAL
Triggering Sensitivity (from repetitive signal)	Triggering Freq. Range	Min. Triggering Signal Required		External signals are increased 10 times for EXT÷10 operation.
		Int.	Ext.	
PP AUTO Mode (AC or DC coupling)	200 Hz to 50 MHz	0.5 div	125 mV	
	50 MHz to 400 MHz	1.5 div	375 mV	
	at least 50 Hz	2.0 div	500 mV	
NORM or SGL SWP Mode				
AC coupling	30 Hz to 50 MHz	0.3 div	100 mV	
	50 MHz to 400 MHz	1.5 div	250 mV	
AC LF REJ coupling	30 kHz to 50 MHz	0.3 div	100 mV	Does not trigger on sine wave at or below 60 Hz with amplitudes less than 8 divisions INT or 3 V EXT.
	50 MHz to 400 MHz	1.5 div	250 mV	
AC HF REJ coupling	30 Hz to 50 KHz	0.3 div	100 mV	Does not trigger on 50 MHz sine wave with amplitude 1.5 divisions or less INT or 0.15 V or less EXT.
DC coupling	DC to 50 MHz	0.3 div	100 mV	
	50 MHz to 400 MHz	1.5 div	250 mV	

TABLE 1-1 (cont.)

CHARACTERISTICS		PERFORMANCE REQUIREMENTS	SUPPLEMENTAL		
LEVEL Range		Amplitude trigger point referenced to a 5 division, 1 kHz sine-wave display.			
PP AUTO mode					
LEVEL*	**SLOPE**	**Start of Trace**			
Fully - (ccw)	+	0.65 to 1.2 div from bottom.			
Fully + (cw)	+	0.3 to 0.7 div from top.			
Fully - (ccw)	-	0.3 to 0.7 div from bottom.			
Fully + (cw)	-	0.65 to 1.2 div from top.			
NORM or SGL SWP mode INT source:					
Fully - (ccw)*			Triggers 6.4 divisions below trigger signal mean (AC), or center screen (DC).		
Fully + (cw)*			Triggers 6.35 divisions above trigger signal mean (AC), or center screen (DC).		
EXT Source:					
EXT		at least ±3.0 volts			
EXT ÷10		At least ±30 volts			
Minimum Required Trigger Pulse (NORM or SGL SWP modes for 7900-Series programmable mainframe)			Duration as Displayed	Amplitude INT	Amplitude EXT
			1 ns	0.5 div	0.5 div
			0.5 ns	---	150 mV

* ccw = LEV -6.4 (high-level code)
cw = LEV 6.39 (high-level code)

TABLE 1-1 (cont.)

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL
Internal Trigger Jitter	0.1 nanosecond or less at 400 MHz.	
External Trigger Input		
Maximum Input Voltage 1 megohm		250 volts DC plus peak AC.
50 ohms		1 watt
Input R and C 1 megohm		1 megohm in parallel with 20 picofarads ±10%.
50 ohms		50 ohms ±5%
VSWR with 50 ohm termination		1.22 maximum at 400 MHz.

TABLE 1-2

PROGRAMMING SPECIFICATIONS

CHARACTERISTICS	PERFORMANCE REQUIREMENTS	SUPPLEMENTAL
Set-up Time (Full front panel)		Front-panel set-up time is: (decode time)+(byte count)X(time/byte) +(overhead).
High-level		Decode time ≃ 14 ms Byte count ≃ 75 Overhead ≃ 0.4 ms
Low-level		Decode time ≃ 1.5 ms Byte count = 15 Overhead ≃ 0.1 ms

TABLE 1-3

ENVIRONMENTAL SPECIFICATIONS

For temperature, altitude, vibration, shock, and humidity specifications, refer to the manual for the associated mainframe.

TABLE 1-4

PHYSICAL SPECIFICATIONS

Weight	1.2 Kg. (2.6 lbs.)
Dimensions	Fits 7000-Series mainframe plug-in compartment.

Summary of Programmable Features

The TEKTRONIX 7B90P Programmable Time Base can be operated in either Local or Remote mode. In Local mode, it operates like a non-programmable plug-in, such as the TEKTRONIX 7B80. That is, its functions are controllable only from the front panel.

When the 7B90P is set to Remote mode, however, the front panel is rendered inoperative except for two non-programmable functions; the Sweep Calibration adjustment (SWP CAL) and the External Trigger Input Terminator switch (TERM). Under remote control, functions can be controlled only by commands sent over the IEEE 488 bus. However, as control settings are effected remotely, the front panel lights will indicate accordingly.

The Remote/Local state of the 7B90P is slaved to the Remote/Local state of the mainframe in which it is installed. Thus the mainframe must be set to Remote mode for programmed control of the plug-in, and must be set to Local mode for front-panel control of the plug-in.

Front-Panel Buttons

Each pushbutton on the 7B90P front panel (except TERM) serves as both a switch and an indicator. A Light Emitting Diode (LED) mounted behind each button indicates the present state of the function controlled by that button, regardless of whether the corresponding function was set manually or under program control. The switches themselves are a momentary-contact type; it is only necessary to tap a particular button to set that function.

The operation of the front-panel buttons generally falls into one of two categories. The first category includes the +SLOPE and MAG buttons. Since there are just two settings for each of these funtions, buttons in this category are essentially toggle switches. The lighting of each button indicates the current state of the function controlled by that button. For example, repeatedly pressing the MAG button alternately illuminates and extinguishes the MAG button. When MAG is lit, the sweep is magnified; when MAG is not lit, the sweep is not magnified. (Incidentally, pressing the MAG button causes the sweep speed to change and this is indicated by the TIME/DIV buttons; thus the TIME/DIV buttons indicate the correct sweep speed, regardless of the setting of the MAG button.)

The second category of buttons includes the following functions:

TRIGGERING-MODE (PP AUTO, NORM, or SGL SWP/RESET)
TRIGGERING-COUPLING (AC, AC LF REJ, AC HF REJ, or DC)
TRIGGERING-SOURCE (INT, LIN, EXT, or EXT÷10)
TIME/DIV (1,2,5,10,20,50,100,200, or 500; and ms, µs, ns, or ps)

Since there are more than two switch settings for each of these functions, pushbuttons in this category are part of a ganged-switch arrangement. Pressing a particular button cancels the setting of the previously pressed button and selects the new setting. For example, if EXT (Triggering Source) has been pressed or remotely set as indicated by the lighting of the EXT button, pressing INT will extinguish the EXT light and switch the triggering source to internal; the INT button will then be lit to indicate the new setting.

Front-Panel Controls

There are three 7B90P front-panel rotary controls: POSTION, HOLD OFF, and LEVEL (TRIGGERING). Each of these is fully programmable. When the 7B90P is in Local mode, these controls operate as though they were part of a non-programmable plug-in. That is, the trace position, hold-off period, and triggering level are controlled by the current position of each respective knob. When the 7B90P is set to Remote mode, however, each control is disabled and the corresponding functions are now set by commands which set a Digital-to-Analog Converter (DAC). There is one DAC for each of the three controls. Since the 7B90P front panel is disabled during remote operation, the current knob settings may not accurately reflect the true trace position, hold-off period, and triggering level. However, when the 7B90P is again set to Local mode, the trace position, hold-off period, and triggering level will again revert to the settings currently indicated by their respective knobs.

Table 1-5 provides a list of all the 7B90P functions and indicates which functions can be set or read (queried) under manual and remote operation. Setting a function manually refers to pressing a given button or turning a control; reading a function manually refers to looking at the illumination of a particular button or noting the position of a control. Setting and reading functions under remote control refers to setting a function or interrogating the status of a function by sending and receiving messages over the IEEE 488 bus. Information on how this is done is contained in Section 3.

For more information on each of the functions and how they are used, refer to Section 2.

TABLE 1-5

LIST OF 7B90P FUNCTIONS

FUNCTION	MANUAL OPERATION		REMOTE OPERATION	
	SET	READ	SET	READ
TRIGGERING				
MODE	X	X	X	X
COUPLING	X	X	X	X
SOURCE	X	X	X	X
SLOPE	X	X	X	X
LEVEL Control	X	X	X	X
POSITION Control	X	X	X	X
TIME/DIV	X	X	X	X
MAGnified Sweep	X	X	X	X
HOLD OFF Control	X	X	X	X
SWP CAL Adjustment	X			
TERMination (input)	X	X		
Plug-in type[1]		X		X
Trigger Light		X		X
End-of-Sweep SRQ Enable			X	X
Single Sweep Ready Light		X		X

NOTE

An "X" in the above chart denotes that a particular function can be set or read.

[1] The plug-in type (7B90P) is inscribed on the front panel and can be read under program control with the ID command.

Block Diagram

The following is a simplified block diagram of the 7B90P (Fig. 1-1) and a brief description of the blocks. It is included here to provide background information for the sections that follow.

The trigger generator provides a stable display by starting the sweep generator at a controlled point for each sweep. The trigger signal is taken from the internal or line trigger signals from the mainframe or the EXT TRIG IN connector on the front panel. The sweep logic sets up the control signals for PP AUTO (Peak-to-Peak AUTOmatic), NORM (NORMal) or SGL SWP (SinGLe SWeeP) modes. This circuit also generates the hold-off timing for the sweep generator. The sweep generator provides a precise ramp voltage for the sweep outputs. The sweep time is variable in calibrated steps from 500 picoseconds to 500 milliseconds per division. When TIME/DIV is set for 100 ms or slower, the sweep generator asserts a mainframe control line that limits the intensity to protect the CRT from burns due to high intensity at slow sweep speeds. The horizontal preamp provides differential sweep signals to the mainframe and adds DC current for sweep positioning. If the MAGnifier is selected, the gain of the horizontal preamp is increased to magnify the sweep.

The 7B90P sweep speed, triggering, front panel LED's, and IEEE 488 circuit are controlled by a microprocessor system in the plug-in. The heart of this system is a Motorola M6800 Microprocessing Unit (MPU). A control program, resident in 4K (1K=1024) bytes of Read Only Memory (ROM) directs the MPU activity. The MPU also uses 128 bytes of Random Access Memory (RAM) as a "scratch pad".

Five Peripheral Interface Adapters (PIA's) handle internal communication between the MPU and other circuits in the plug-in. The IEEE 488 interface handles the handshaking and communication on the IEEE 488 bus. The clock circuit generates the 2-phase clock signals required by the MPU. When power-up occurs, the power-up circuit initializes the MPU and PIA's, and starts the clock circuit.

A detailed circuit description of these blocks is included in Section 5.

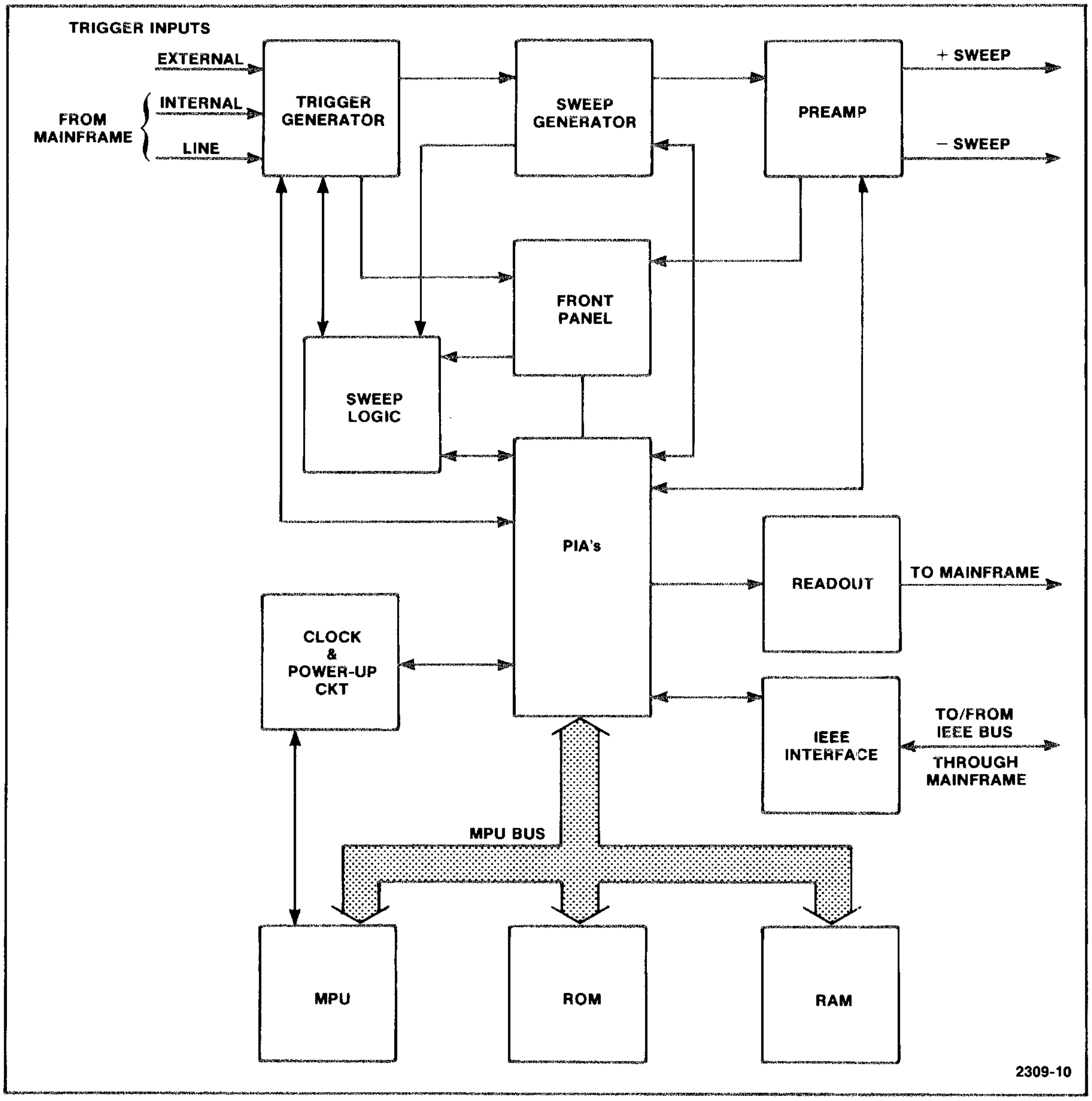

Fig. 1-1. Block diagram of the 7B90P.

SECTION 2

MANUAL OPERATION

This section contains a description of the 7B90P controls, connector, and indicators, and includes instructions for manual (non-programmable) operation of the plug-in. This is followed by a "functional check" section which provides a quick verification of instrument performance. Also included are instructions for installing the plug-in, general information on triggering, and other subjects that pertain to various measurement applications.

Installation

The 7B90P is calibrated and ready for use as received. It may be installed in any compartment of a TEKTRONIX 7000-Series programmable mainframe, but is intended primarily for use in a horizontal plug-in compartment. The 7B90P may also be installed in a vertical plug-in compartment to provide a vertical sweep on the CRT. However, when used in this manner, there are no internal triggering or retrace blanking provisions, and the unit may not meet the specifications given in Section 1.

NOTE

Always turn off the mainframe power before installing or removing plug-ins to prevent damage to circuitry.

To install the plug-in, align the upper and lower rails of the 7B90P with the mainframe tracks and insert the plug-in. The front panel will be flush with the front of the mainframe when the plug-in is fully inserted, and the latch at the bottom left corner will be in place against the front panel.

To remove the 7B90P, pull on the latch (inscribed with the identification "7B90P") and the plug-in will unlatch. Continue pulling on the latch to slide the 7B90P out of the mainframe.

Controls, Connector, and Indicators

(1) LEVEL Control

Selects a point on the trigger signal where triggering occurs. When the LEVEL is set in the positive region, triggering occurs on the positive excursion (top half) of the signal; when the LEVEL is set in the negative region, triggering occurs on the negative excursion (bottom half) of the signal.

(2) SLOPE Switch

Determines whether the sweep is triggered on the negative slope or positive slope of the trigger signal. When lit, the trigger switch is set for a positive slope; when unlit, it is set for a negative slope.

(3) TRIG'D Indicator

Illuminates when the sweep is triggered.

(4) READY Indicator

Illuminates when the sweep circuit is armed, and is extinguished when the sweep is completed. (Applies only to single-sweep mode.)

(5) TRIGGERING-MODE Pushbuttons

These three buttons select the triggering mode of the 7B90P according to which button was last pressed:

PP AUTO: Provides a triggered display at any setting of the LEVEL control whenever an adequate trigger signal is applied. The range of the LEVEL control in the Peak-to-Peak Automatic mode is between approximately 10% and 90% of the peak-to-peak amplitude of the trigger signal.

NORM: Provides normal triggering. That is, the sweep is triggered only if a point on the triggering signal corresponds to the conditions set by the LEVEL and SLOPE controls.

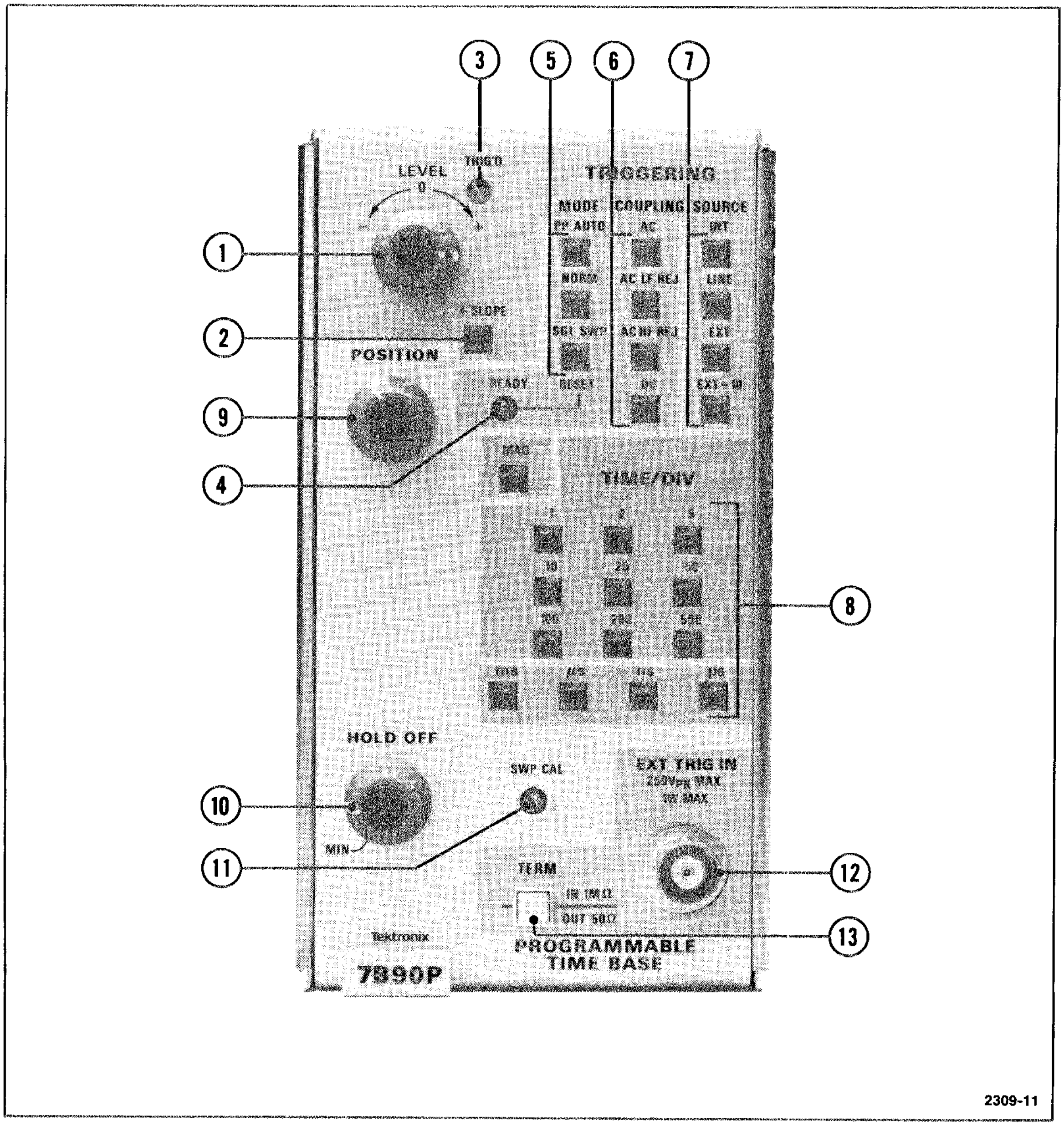

Fig. 2-1. Front panel of the 7B90P.

SGL-SWP/RESET: Sets the 7B90P to single-sweep mode and resets (arms) the sweep. A single sweep will occur when a point on the trigger signal corresponds to the conditions set by the LEVEL and SLOPE controls. Pressing this button a second time rearms the sweep.

(6) TRIGGERING-COUPLING Pushbuttons

These four buttons select the trigger coupling mode according to which button was last pressed:

AC: Selects AC coupling of the triggering signal, thereby blocking any direct-current component of the signal.

AC LF REJ: Selects a trigger-coupling circuit that passes high-frequency AC signals, but blocks DC and low-frequency AC signals.

AC HF REJ: Selects a trigger-coupling circuit that passes low-frequency AC signals, but blocks DC and high-frequency AC signals.

DC: Selects DC coupling of the triggering signal, thereby passing all frequency components of the signal.

(7) TRIGGERING-SOURCE Pushbuttons

These four buttons select the source of the trigger signal according to which button was last pressed:

INT: Selects the internal signal supplied by the mainframe vertical system as the triggering signal.

LINE: Selects a sample of the mainframe AC power input as the triggering signal.

EXT: Selects the signal supplied to the EXT TRIG IN connector as the triggering signal.

EXT÷10: Selects the signal supplied to the EXT TRIG IN connector as the triggering signal, but attenuates it by a factor of 10 to allow greater input voltage range.

(8) TIME/DIV Pushbuttons

The sweep rate (time/division) is entered in engineering notation and therefore both a number and a multiplier must be entered via the following switches:

1,2,5,10,20,50,100,200,500: These switches determine the numeric part of the sweep rate.

ms,μs,ns,ps: These switches determine the multiplier and units of the sweep rate in milliseconds (ms), microseconds (μs), nanoseconds (ns), or picoseconds (ps).

MAG: Selects the magnified 10X sweep rate, thereby generating a sweep speed that is 10 times greater. When lit, the switch is set for magnified sweep; when unlit, the sweep is not magnified.

(9) POSITION Control

Varies the horizontal position of the trace by applying a DC offset voltage.

(10) HOLD-OFF Control

Varies the trigger hold-off period (the time following the end-of-sweep that the sweep generator is inhibited) to improve triggering stability on repetitive signals. Hold-off time is maximum when the control is turned fully clockwise.

(11) SWP CAL Adjustment

This front panel screwdriver adjustment varies the sweep calibration to achieve the desired trace width. This allows for differences in gain between mainframes. All sweep rates are affected by this adjustment.

EXT TRIG IN

(12) **EXT TRIG IN Connector:** Input connector (BNC type) for an external trigger signal.

(13) **TERM:** Terminates the EXTernal TRIGger INput connector with either 50 ohms or 1 megohm of impedance. In the IN position, it selects 1 megohm; in the OUT position, it selects 50 ohms.

CAUTION

The signal to the EXT TRIG IN connector must not exceed 250 volts, DC plus peak AC. If 50 ohms is selected, the power of the input signal must be limited to 1 watt.

Functional Check

The following procedure demonstrates the use of the controls, connector, and indicators of the 7B90P, while at the same time providing a means of checking the basic operation of the instrument. Refer to the description of the controls, connector, and indicators while performing this procedure. If performing the functional-check procedure reveals a malfunction or improper adjustment, first check the operation of the associated mainframe. If the mainframe seems to be working properly, have the 7B90P examined by a qualified service technician.

Preliminary Setup

With the mainframe power off, install the 7B90P into the horizontal plug-in compartment of a 7000-Series programmable mainframe. Install a 7A-Series amplifier unit into the vertical plug-in compartment.

With the mainframe power on, set the mainframe trigger-source switch (if applicable) to select the appropriate vertical compartment. Set the amplifier unit for AC input coupling. Also, adjust the mainframe intensity knob(s), if necessary. NOTE: On some mainframes, both the beam intensity and graticule intensity must be adjusted.

Power-up Sequence

When the mainframe is turned on, the 7B90P is set to a predetermined state as indicated by the lighted front-panel buttons. The status of the front-panel buttons should indicate the following:

TRIGGERING MODE:	PP AUTO
TRIGGERING COUPLING:	AC
TRIGGERING SOURCE:	INT
TRIGGERING SLOPE:	+ SLOPE
TIME/DIV:	1 μs
MAG:	unmagnified (1X)

Also, the outputs of the three front-panel controls (LEVEL, POSITION, and HOLD OFF) are tracked to their current knob settings during the power-up sequence.

Procedure

NORMAL OPERATION

1) After an adequate warm-up period (20 minutes or more), adjust the 7B90P POSITION control for midscreen positioning of the trace; adjust the HOLDOFF control to minimum (fully counterclockwise). Readjust the mainframe intensity knob(s), if necessary.

2) Adjust the amplifier POSITION control so that the trace is vertically centered on the CRT monitor.

3) Set the amplifier unit to a deflection factor of 1 V/div (or 100 mV/div if a 10X probe is being used). The VARIABLE control should be pressed in to the calibrated position.

4) Set the 7B90P sweep speed to 1 ms/div. Adjust the mainframe intensity knob(s) to the proper levels.

5) Connect a 4 volts (peak-to-peak), 1 kilohertz square wave to the input of the amplifier unit, and (if applicable) select the proper input connector.

6) Check the display for one cycle per division. If necessary, adjust the front-panel SWP CAL screwdriver adjustment for one cycle per division over the center 8 graticule divisions.

7) Readjust the 7B90P POSITION control, if necessary.

MAGNIFIED SWEEP

8) Press the MAG button and check that the MAG button illuminates. Note that the center portion of the unmagnified display (the area within one-half division of centerline) is expanded to 10 divisions. Also note that the sweep-speed buttons now indicate 100 μs/div. (Adjust the mainframe intensity knob(s), if necessary.)

9) Reset the 7B90P to unmagnified mode by again pressing the MAG button. Note that the MAG button is no longer lit and that the display is no longer magnified. Also note that the sweep-speed buttons now indicate 1 ms/div. (Adjust the mainframe intensity knob(s), if necessary.)

PP-AUTO TRIGGERING MODE

10) Connect an 8 V P-P, 1 kHz sine wave to the input of the amplifier unit.

11) Rotate the LEVEL control from fully counterclockwise to fully clockwise and note that the signal can be triggered over the full range of the LEVEL control in PP AUTO mode.

12) Reduce the input signal amplitude to 1 V P-P. Note that the signal can still be triggered in PP AUTO mode, as indicated by the TRI'G light.

13) Disconnect the input signal and check for a free-running baseline trace. Note that the TRI'G light is no longer lit.

NORMAL TRIGGERING MODE

14) Press the NORM button. Check that the button is lit and that the baseline trace now disappears in the absence of the trigger signal.

15) Reconnect the 1 V P-P, 1 kHz sine wave to the amplifier input. Note that the waveform is displayed (the 7B90P is triggered) only when the LEVEL control is set near 0.

SINGLE-SWEEP TRIGGERING MODE

16) With the 7B90P set for a triggered display, press the SGL SWP/RESET button. Check that the button is lit and that the displayed waveform disappears from the CRT monitor. The TRI'G light is also extinguished at this time.

17) Again press the SGL SWP/RESET button. Note that one sweep occurs (the waveform briefly appears on the CRT monitor) each time this button is pressed. Also note that the TRI'G and READY lights flash when SGL SWEEP/RESET is pressed. NOTE: It may be necesaary to increase the mainframe intensity during this step.

18) Disconnect the input signal and press SGL SWP/RESET. The READY light should now be lit. Check that TRI'G briefly lights and that READY is extinguished when the input signal is reconnected.

LEVEL CONTROL

19) Press the PP AUTO button and set the LEVEL control fully counterclockwise. Note that the waveform is triggered on the negative excursion (bottom half) of the signal.

20) Set the LEVEL control fully clockwise and note that the input signal is now triggered on the positive excursion (top half) of the signal.

21) Set the LEVEL control to 0 and note that triggering occurs midway between the peak and trough of the signal.

+SLOPE

22) Press the +SLOPE switch. Check that the button is no longer lit and that triggering now occurs on the negative slope of the input signal.

23) To again trigger the input signal on its positive slope, press +SLOPE. The button should now be lit, indicating positive-slope triggering.

HOLD OFF CONTROL

24) Rotate the HOLD OFF control fully clockwise. Note that the trigger hold-off period increases. (On a CRT monitor, this is evidenced by increased flickering of the input signal.)

25) Rotate the HOLD OFF control fully counterclockwise to restore minimum hold-off time.

TRIGGERING COUPLING

26) Press the AC, AC HF REJ, and DC coupling buttons. Note that in each case the respective button is lit and that a stable display is achieved.

27) Press the AC LF REJ button and check that it lights. Note that a stable display is not achieved due to attenuation of the 1 kHz input signal.

EXTERNAL TRIGGERING

28) By means of a BNC T connector, connect the input signal to the amplifier input and also to the EXT TRIG IN connector of the 7B90P. Press the EXT source button. Note that the button lights and that stable triggering now occurs if TERM is pressed in. NOTE: with the TERM switch in the extended (50 ohm) position, the displayed signal amplitude is one-half that displayed when TERM is in the unextended (1 megohm) position.

General Operating Information

Triggering Switch Logic

The MODE, COUPLING, and SOURCE pushbuttons of the TRIGGERING switches are arranged in a sequence that places the most-often used position at the top of each series of pushbuttons. With this arrangement, a stable display can usually be obtained by pressing the top three pushbuttons: PP AUTO, AC, and INT.

When an adequate trigger signal is applied and the LEVEL control is correctly set, the unit is triggered as indicated by the illuminated TRIG'D light. If the TRIG'D light is not on, the LEVEL control is either at a setting outside the range of the trigger signal applied to the 7B90P from the vertical unit, the trigger signal amplitude is inadequate (less than 0.3 divisions), or its frequency is below the lower frequency limit of the AC COUPLING switch on PP AUTO range. If the desired display is not obtained with these buttons lit, other selections must be made. Refer to the following discussions or the instruction manuals for the associated mainframe and amplifier unit for more information.

Triggering Modes

The MODE pushbutton switches select the mode in which the sweep is triggered. The following discussion describes the purpose of each mode:

PP AUTO: The PP AUTO MODE provides a triggered display at any setting of the LEVEL control whenever an adequate trigger signal is applied. The range of the LEVEL control in the PP AUTO MODE is between approximately 10% and 90% of the peak-to-peak amplitude of the trigger signal. The LEVEL and SLOPE controls can be set so that the displayed waveform starts at any point within this range on either slope. The trigger circuits automatically compensate for a change in trigger-signal amplitude. Therefore, if the LEVEL control is set to start the waveform display at a certain percentage point on the leading edge of a low-amplitude signal, it triggers at the same percentage point on the leading edge of a high-amplitude signal if the LEVEL control is not changed. When the trigger repetition rate is outside the parameter given in the Specifications (Section 1), or when the trigger signal is inadequate, the sweep free runs at the rate indicated by the TIME/DIV buttons to produce a bright base-line reference trace (TRIG'D light off). When an adequate trigger signal is again applied, the free-running condition ends and a triggered display is presented.

The PP AUTO MODE is particularly useful when observing a series of waveforms, since it is not necessary to reset the LEVEL control for each observation. The PP AUTO MODE is used for most applications because of the ease of obtaining a triggered display. The NORM and SINGLE-SWP MODE settings may be used for special applications.

NORMAL: The NORM MODE provides a triggered display with the correct setting of the LEVEL control whenever an adequate trigger signal is applied. The TRIG'D light indicates when the display is triggered. When the TRIG'D light is off, no trace is displayed.

The normal trigger mode must be used to produce triggered displays when the trigger repetition rate is below about 30 hertz.

SINGLE SWEEP: When the signal to be displayed is not repetitive, or varies in amplitude, waveshape, or repetition rate, a conventional repetitive-type display mode may produce an unstable presentation. Under these circumstances, a stable display can often be obtained by using the single-sweep mode. The single-sweep mode is also useful in photographing non-repetitive or unstable displays.

To obtain a single-sweep display of a repetitive signal, first obtain the best possible display in the NORM mode. Then, without changing the other TRIGGERING controls, press the SGL SWP button. A single trace is presented each time this button is pressed. Further sweeps cannot be presented until the SGL SWP button is pressed again. If the displayed signal is a complex waveform composed of varying amplitude pulses, successive single-sweep displays may not start at the same point on the waveform. To avoid confusion due to the crt persistence, allow the display to disappear before pressing the SGL SWP button again. At fast sweep rates, it may be difficult to view the single-sweep display. The apparent trace intensity can by increased by reading the ambient light level or by using a viewing hood.

Trigger Coupling

The TRIGGERING COUPLING pushbuttons select the method in which the trigger signal is connected to the trigger circuits. Each position permits selection or rejection of some frequency components of the signal which triggers the sweep.

AC: AC COUPLING blocks the DC component of the trigger signal. Signals with low-frequency components below about 30 hertz are attenuated. In general, AC COUPLING can be used for most applications. However, if the signal contains unwanted frequency components or if the sweep is to be triggered at a low repetition rate or DC level, one of the other COUPLING switch positions will provide a better display.

AC LF REJ: AC LF REJ COUPLING rejects DC, and attenuates low-frequency trigger signals below about 30 kilohertz. Therefore, the sweep is triggered only by the higher-frequency components of the trigger signal. This position is particularly useful for providing stable triggering if the trigger signal contains line-frequency components. Also, the AC LF REJ position provides the best alternate-mode vertical displays at fast sweep rates when comparing two or more unrelated signals.

AC HF REJ: AC HF REJ COUPLING passes all low-freqquency signals between about 30 hertz and 50 kilohertz. DC is rejected and signals outside the above range are attenuated. When triggering from complex waveforms, this position can provide a stable display of the low-frequency components.

DC: DC COUPLING can be used to provide stable triggering from low-frequency signals which would be attenuated in the other COUPLING switch positions. DC COUPLING can be used to trigger the sweep when the trigger signal reaches a DC level set by the LEVEL control. When using internal triggering, the setting of the vertical unit position control affects the triggering point.

Trigger Source

The TRIGGERING SOURCE pushbuttons select the source of the trigger signal that is connected to the trigger circuits.

INTERNAL: The INT button connects the trigger signal from the vertical plug-in unit. Further selection of the internal trigger signal may be provided by the vertical plug-in unit or by the mainframe; see the instruction manuals for these instruments for more information. For most applications, the internal source can be used. However, some applications require special triggering which cannot be obtained in the INT position. In such cases, the LINE or EXT buttons must be used.

LINE: The LINE button connects a sample of the power-line voltage from the mainframe to the trigger circuit. Line triggering is useful when the input signal is time-related (multiple or submultiple) to the line frequency. It is also useful for providing a stable display of a line-frequency component in a complex waveform.

EXTERNAL: The EXT button connects the signal from the EXT TRIG IN connector to the trigger circuit. The external signal must be time-related to the displayed waveform for a stable display. An external trigger signal can be used to provide a triggered display when the internal signal is either too low in amplitude for correct triggering or contains signal components on which triggering is not desired. It is also useful when signal tracing in amplifiers, phase-shift networks, wave-shaping circuits, etc. The signal from a single point in the circuit can be connected to the EXT TRIG IN connector through a probe or cable. The sweep is then triggered by the same signal at all times and allows amplitude, time relationship, or waveshape changes of signals at various points in the circuit to be examined without resetting the TRIGGERING controls.

The EXT÷10 pushbutton attenuates the external trigger signal by a factor of 10. Attenuation of high amplitude external trigger signals is desirable to increase the effective range of the LEVEL control.

Trigger Slope

The SLOPE button determines whether the trigger circuit responds on the positive or negative slope of the trigger signal. When the SLOPE switch is in the (+) position (as indicated by the lighting of the SLOPE button), the display starts on the positive slope of the waveform (see Fig. 2-2). When several cycles of a signal appear in the display, the setting of the SLOPE switch is often unimportant. However, if only a certain portion of a cycle is to be displayed, correct setting of the SLOPE switch is important to provide a display that starts on the desired slope of the input signal.

Trigger Level

The LEVEL control determines the voltage level on the trigger signal at which the sweep is triggered. When the LEVEL control is set in the (+) region, the trigger circuit responds at a more positive point on the trigger signal. When the LEVEL control is set in the (-) region, the trigger circuit responds at a more negative point on the trigger signal. Figure 2-2 illustrates this effect with different settings of the SLOPE switch.

To set the LEVEL control, first select the TRIGGERING MODE, COUPLING, SOURCE, and SLOPE. Then set the LEVEL control fully counterclockwise and rotate it clockwise until the display starts at the desired point.

Horizontal Sweep Rates

The TIME/DIV buttons provide calibrated sweep rates from 500 milliseconds/division to 500 picoseconds/division in a 1-2-5 sequence. In most cases, selecting a sweep rate requires pressing two buttons: a numbered button (1, 2, 5, 10, 20, 50, 100, 200, or 500), and a button representing the multiplier and units (ms, μs, ns, and ps). In some cases, the MAG button is also involved.

When an attempt is made to enter a sweep rate faster than 500 picoseconds/division, the 7B90P internal logic corrects the mistake as follows:

1) If a numbered button other than **500** is pressed while **ps** (picoseconds) is selected, the multiplier button is automatically switched to **ns** (nanoseconds).

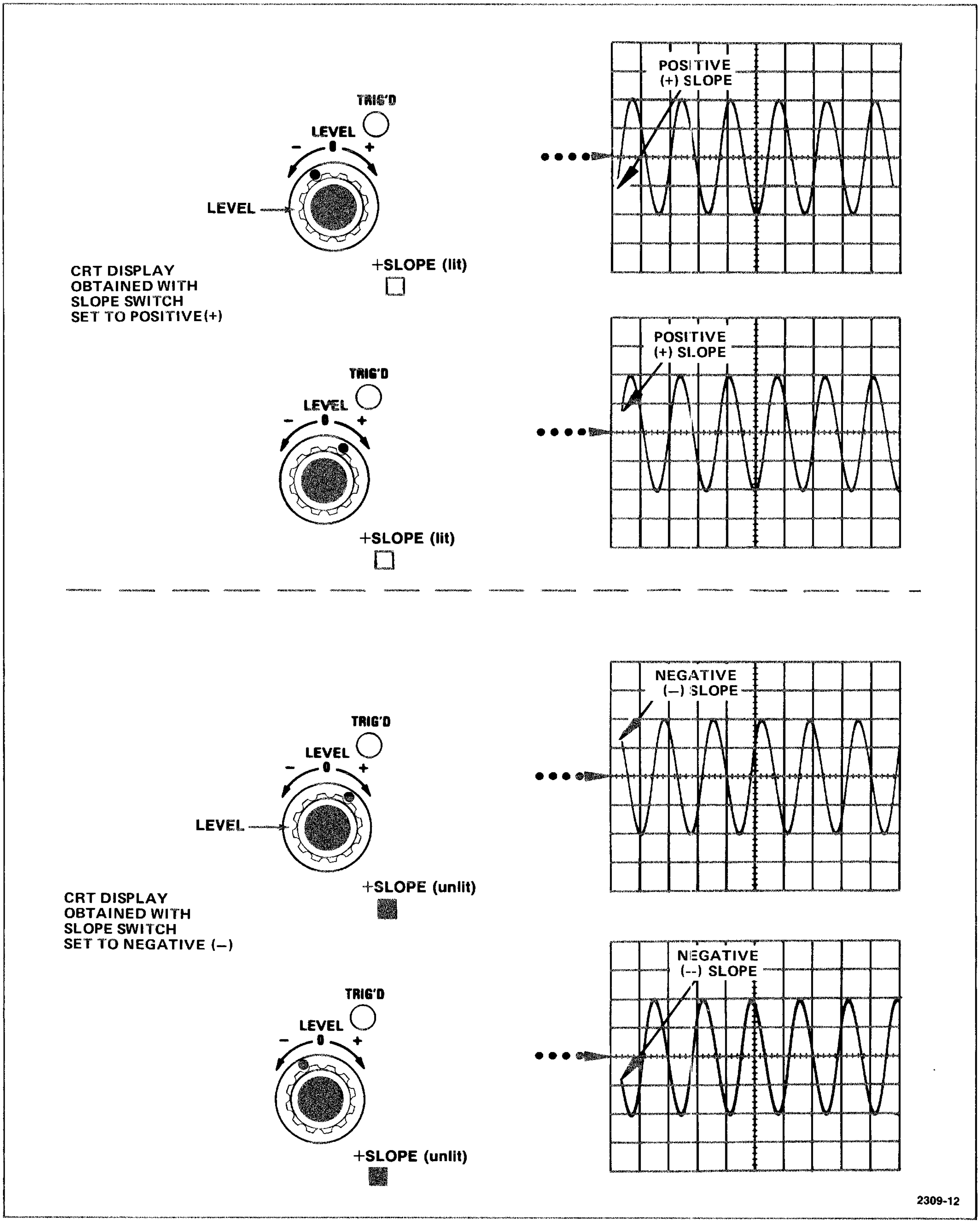

Fig. 2-2. Effect of the LEVEL control and SLOPE switch on CRT display.

2) If the **ps** button is pressed while any numbered button other than **500** is selected, the number is automatically switched to **500**.

In either case, the button just pressed is accepted. This allows the operator to enter a valid sweep rate without regard to the order in which the buttons are pressed. For example, to go from 500 picoseconds/division to 20 microseconds/division, the operator can press **μs** first (intermediate state = 500 μs) and then **20**. Or, **20** can be pressed first (intermediate state = 20 ns) and then **μs**.

The correct sweep speed is always indicated by which buttons are lit. It is not necessary to multiply the indicated sweep speed by a factor of 10 when selecting the MAGnified mode. When the MAG button is pressed, the indicated sweep speed automatically increases by a factor of 10. The correct sweep speed is also indicated by the digital readout displayed on the CRT monitor or other display device.

Sweep Magnification

On a TIME/DIV setting of 10 ns or slower, the MAG button can be used to expand the display by a factor of 10. (When the MAG button is lit, the sweep is magnified.) The center portion of the display is the part that is magnified (see Fig. 2-3). The equivalent length of the magnified sweep is more than 100 divisions; any 10 division portion can be viewed by adjusting the 7B90P POSITION control to bring the desired portion into view.

Magnified sweep mode is automatically selected when a TIME/DIV of 5, 2, or 1 nanoseconds/division or 500 picoseconds/division is selected. When in the magnified mode at a sweep rate of 1 nanoseconds/division or slower, pressing MAG returns the sweep length to 10 divisions and TIME/DIV to a rate 10 times slower. When in the magnified mode at a sweep rate of 500 picoseconds/division, the sweep length is also returned to 10 divisions when MAG is pressed, but TIME/DIV is switched to 10 nanoseconds/division, the fastest unmagnified sweep rate.

Time Measurement

When making time measurements from the graticule, the area between the second and tenth vertical lines of the graticule provides the most linear time measurements (see Fig. 2-4). Position the start of the timing

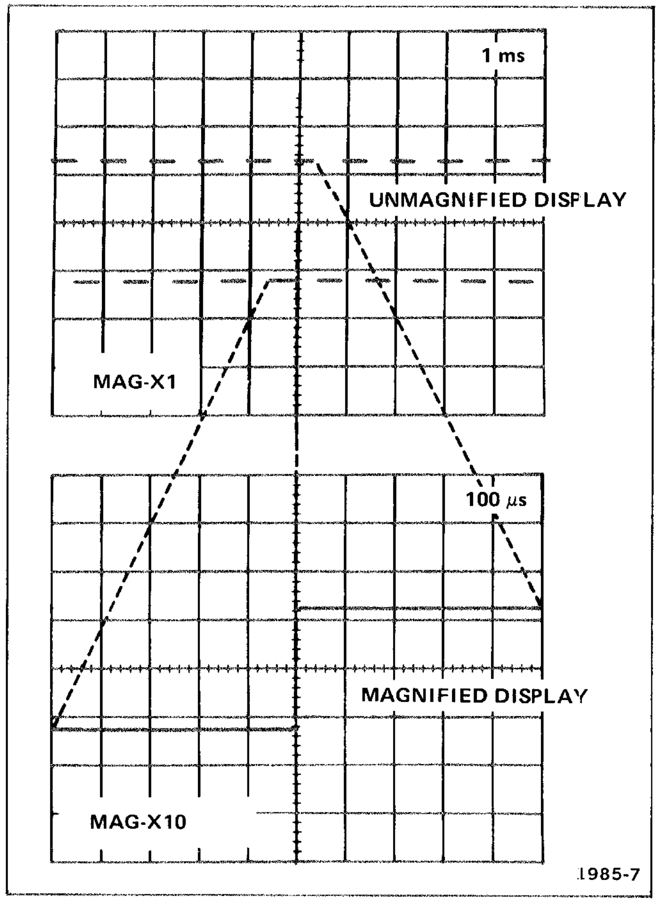

Fig. 2-3. Operation of the sweep magnifier.

area to the second vertical line and adjust the TIME/DIV switch so the end of the timing area falls between the second and tenth vertical lines.

Variable Hold Off

The HOLD OFF control improves triggering stability on repetitive complex waveforms by effectively changing the repetition rate of the horizontal sweep signal. The HOLD OFF control should normally be set to its minimum setting. When a stable display cannot be obtained with the TRIGGERING LEVEL control, the HOLD OFF control can be varied for an improved display. If a stable display cannot be obtained at any setting of the LEVEL and HOLD OFF controls, check the TRIGGERING COUPLING and SOURCE switch settings. (NOTE: When the 7B90P is used in a TEKTRONIX 7912AD Programmable Digitizer, the HOLD OFF control is overridden by the mainframe at certain sweep speeds.

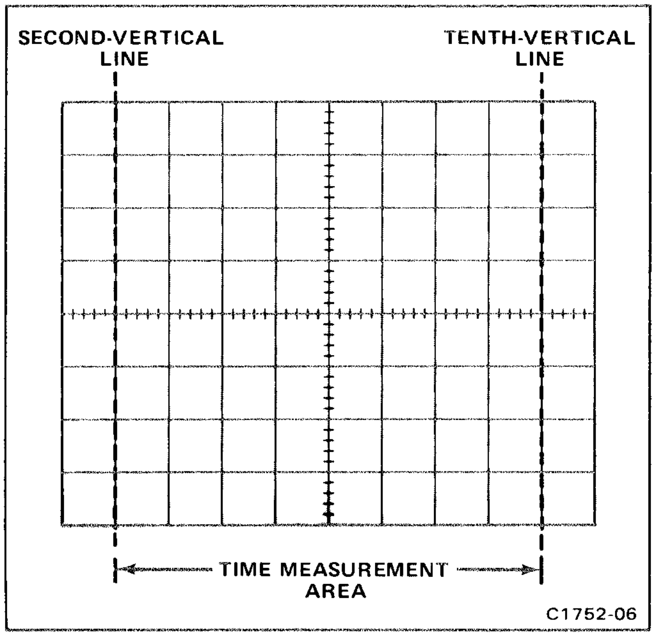

Fig. 2-4. Area of the graticule providing the most accurate time measurement.

Applications

The following information describes procedures and techniques for making basic time measurements with the 7B90P and an associated TEKTRONIX programmable mainframe and amplifier. (To some extent, this information is also applicable to measurements made under program control.) These procedures provide enough detail to enable you to adapt them to other related time measurements. Contact your Tektronix Field Office or representative for assistance in making specific measurements.

Since time is a function of the sweep rate and the horizontal distance (in divisions) that the sweep travels, the time interval between any two points on a waveform can be accurately measured. The following procedures provide methods to measure some of the more common time-related characteristics of a waveform such as period, frequency, rise time, fall time, and pulse width. The procedure for each of these measurements is essentially the same, except for the points between which the measurements are made. The time interval between any two selected points on a displayed waveform can be measured with basically the same technique.

Period and Frequency Measurements

Perform the following procedure to measure the period and determine the frequency of a displayed waveform:

1) Connect the signal to be measured to the selected input of the amplifier unit.

2) Set the TRIGGERING switches and LEVEL control for a stable display (see **General Operating Information** for selecting proper triggering).

3) Set the vertical deflection factor and amplifier POSITION control for about a 5-division display, vertically centered on the graticule.

4) Set the TIME/DIV switches and 7B90P POSITION control for 1 complete cycle displayed within the center 8 graticule divisions as shown in Fig. 2-5.

5) Measure the horizontal distance in divisions over 1 complete cycle of the displayed waveform (see Fig. 2-5).

6) Multiply the horizontal distance measured in Step 5 by the TIME/DIV setting.

Example: Assume that the horizontal distance over 1 complete cycle is 7 divisions, and the TIME/DIV setting is 0.1 ms (see Fig. 2-5).

Using the formula:

Period = Horizontal distance X TIME/DIV setting

Substituting values:

Period = 7 X 0.1 ms = 0.7 millisecond

7) Determine the frequency of the displayed waveform obtained in steps 1 through 6 by taking the reciprocal of the period of 1 cycle.

Example: Assume that the period of the displayed waveform is 0.7 millisecond.

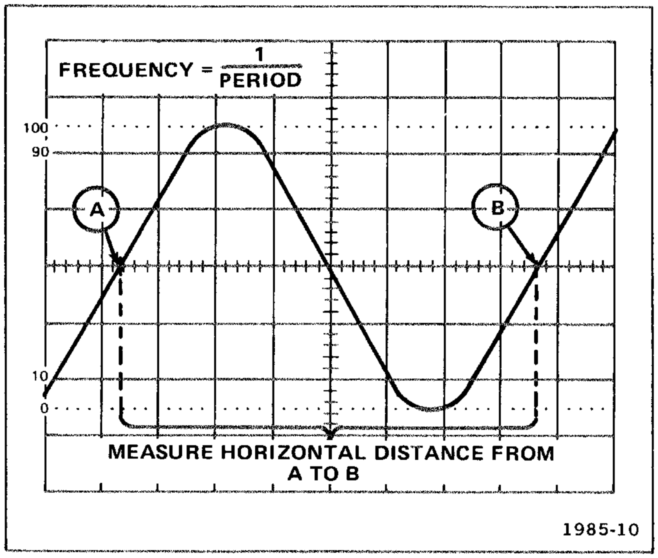

Fig. 2-5. Measuring the period and determining the frequency of a displayed waveform.

Using the formula:

$$\text{Frequency} = \frac{1}{\text{Period}}$$

Substituting values:

$$\text{Frequency} = \frac{1}{0.7 \text{ ms}} = 1.43 \text{ kilohertz}$$

Rise-Time and Fall-Time Measurements

Perform the following procedure to measure the rise time and fall time of a displayed waveform:

1) Connect the signal to be measured to the selected input of the amplifier unit. Obtain a triggered display as previously described.

2) Set the vertical deflection factor and amplifier POSITION control for about a 5-division display, vertically centered on the graticule.

3) Set the TIME/DIV switches and 7B90P POSITION control to display the rising or falling portion of the waveform within the center 8 graticule divisions as shown in Fig. 2-6 (see **General Operating Information** in this section for a discussion of timing measurement accuracy).

4) Determine rise time or fall time by measuring the horizontal distance in divisions between the point on the rising or falling portion of the waveform that is 10% and the point that is 90% of the total display amplitude (see Fig. 2-6)

5) Multiply the horizontal distance measured in step 4 by the TIME/DIV setting.

Example: Assume that the horizontal distance from the 10% to 90% points is 2.5 divisions and the TIME/DIV setting is 0.1 μs (see Fig. 2-6).

Using the formula:

$$\text{Rise Time} = \frac{\text{Horizontal distance}}{\text{(divisions)}} \times \frac{\text{TIME/DIV}}{\text{setting}}$$

Substituting values:

$$\text{Rise Time} = 2.5 \times 0.1\ \mu s = 0.25 \text{ microsecond}$$

Pulse-Width Measurements

Perform the following procedure to measure the pulse width of a displayed waveform:

1) Connect the signal to be measured to the selected input of the amplifier unit. Obtain a triggered display as previously described.

2) Set the vertical deflection factor and amplifier POSITION control for about a 5-division display vertically centered on the graticule.

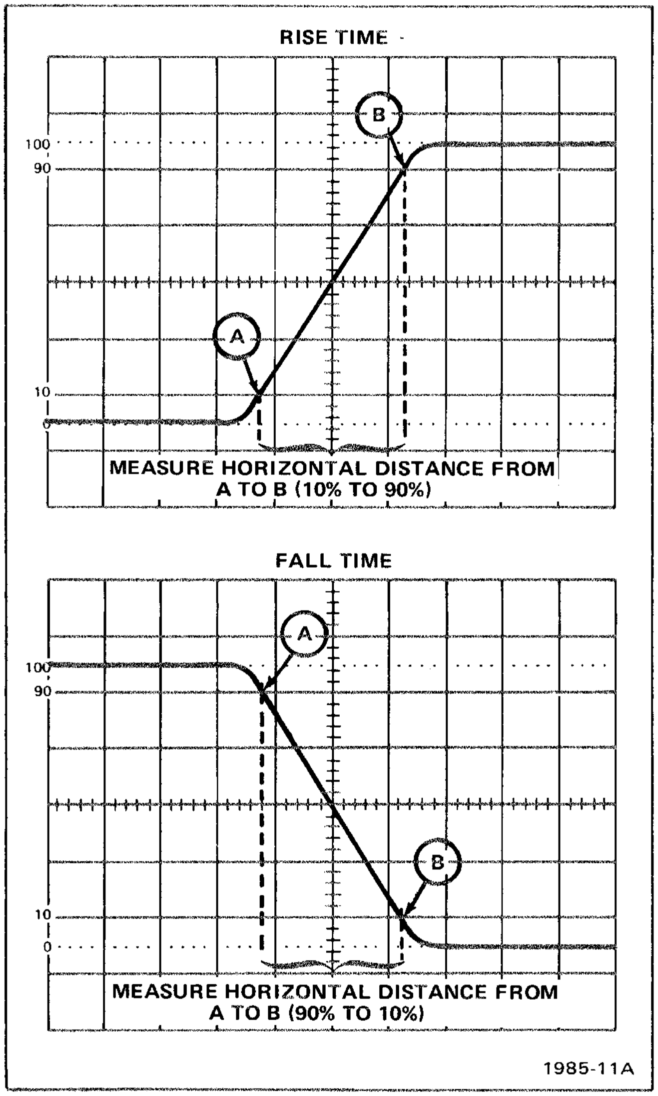

Fig. 2-6. Measuring the rise time and fall time of a displayed waveform.

3) Set the TIME/DIV switches and 7B90P POSITION control for 1 complete pulse displayed within the center 8 graticule divisions as shown in Fig. 2-7.

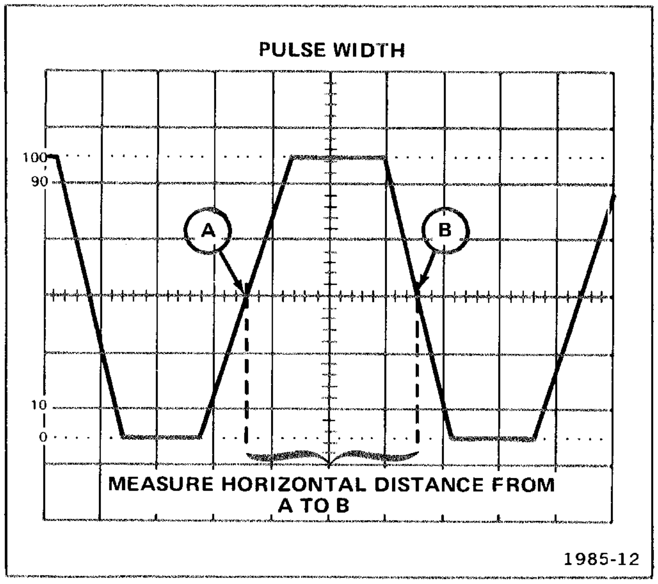

Fig. 2-7. Measuring the pulse width of a displayed waveform.

4) Measure the horizontal distance in divisions between the 50% amplitude points of the displayed pulse (see Fig. 2-7).

5) Multiply the horizontal distance measured in step 4 by the TIME/DIV setting.

Example: Assume that the horizontal distance between the 50% amplitude points is 3 divisions, and the TIME/DIV setting is 0.1 ms (see Fig. 2-7).

Using the formula:

$$\text{Pulse Width} = \begin{matrix}\text{Horizontal}\\ \text{distance}\end{matrix} \times \begin{matrix}\text{TIME/DIV}\\ \text{setting}\end{matrix}$$

Substituting values:

$$\text{Pulse Width} = 3 \times 0.1 \text{ ms} = 0.3 \text{ millisecond}$$

SECTION 3

PROGRAMMING

The 7B90P can be operated by remote control over a versatile instrument bus known as the IEEE 488 bus. A detailed description of the bus is given in IEEE Standard 488-1975 as well as ANSI Standard MC 1.1-1975. A brief introduction to the IEEE 488 standard is included in this section as background information.

The 7B90P is interfaced to the IEEE 488 bus through the mainframe in which it is installed. The mainframe provides a transparent interface between the IEEE 488 bus and the internal 7000-Series bus used to program the plug-ins.

The Remote/Local state of the 7B90P is slaved to the Remote/Local state of the programmable mainframe. When the mainframe is set to Remote mode, the 7B90P can be operated by remote control over the IEEE 488 bus. Either the controller-in-charge or other designated talker and listeners can then set or read any of the 7B90P programmable functions. In Remote mode, the front panel is disabled except for the settings of the Sweep Calibration adjustment (SWP CAL) and the External Trigger Input Terminator switch (TERM); these are the only non-programmable functions on the 7B90P.

After the 7B90P has been set to Remote state, it can be remotely controlled by messages sent over the bus. This remote programming can be accomplished by either of two types of device-dependent messages: a high-level language (ASCII character strings) or a low-level language (hexadecimal codes). The advantage of the high-level language is that messages can be sent with simple, easy-to-remember mnemonics. Since the plug-in itself decodes these high-level commands, it is not necessary to incorporate this decoding capability into special driver software. The main advantage of using the low-level code is that fewer keystrokes and less bus time is required than when programming with the high-level language. When access time is more important than ease of programming, the low-level language of the 7B90P should be used. Both methods of programming the 7B90P are explained following a brief introduction to the IEEE 488 bus.

Introduction to the IEEE 488 Bus

The IEEE 488 bus is a versatile instrument bus designed to provide an effective communications link for data and instructions. The bus itself is entirely passive. The active components of the interface are contained within each device. Instruments designed to operate according to this universal standard can be connected directly to the bus and operated by a controller with appropriate programming. The instructions and data generated by instruments can be coded in either ASCII or binary. The IEEE standard specifies only the mechanical, electrical, and functional aspects of the interface. The operational, or device dependent, aspects of the system are purposely not specified to allow greater flexibility as to the types of devices that can be interconnected.

A Typical System

The IEEE 488 bus uses eight data lines and eight control lines. Information is transferred bit-parallel, byte-serial by an asynchronous handshake. The handshake signals guarantee that each data byte has been transferred properly before allowing another byte to be transferred across the bus. This allows instruments with different data transfer rates to operate together if they conform to the handshake state diagrams defined in the IEEE 488 standard.

Types of Instruments. Instruments connected to the bus can be classified as either controllers, talkers, or listeners. A controller designates which devices are to talk or listen and exercises other bus management functions; at any given time, there can be only one controller. A talker is a device capable of transmitting data and instructions on the Data lines; there can be only one talker at a time to avoid confusion in message and data transfer. A listener is a device capable of responding to data or instructions received on the Data lines; there can be more than one listener at a time since no confusion results.

A device need not be a talker or listener or controller at all times. It may be idle part of the time. Other devices (such as a digital multimeter) may alternately function as a talker or listener depending on whether they are listening to instructions or generating data.

A typical system is diagrammed in Fig. 3-1. It includes a controller (such as a TEKTRONIX CP4165 Controller), a talker (such as a counter or digital multimeter), and a listener (such as a line printer or signal generator). Also included is a TEKTRONIX 7912AD Programmable Digitizer which may either talk or listen.

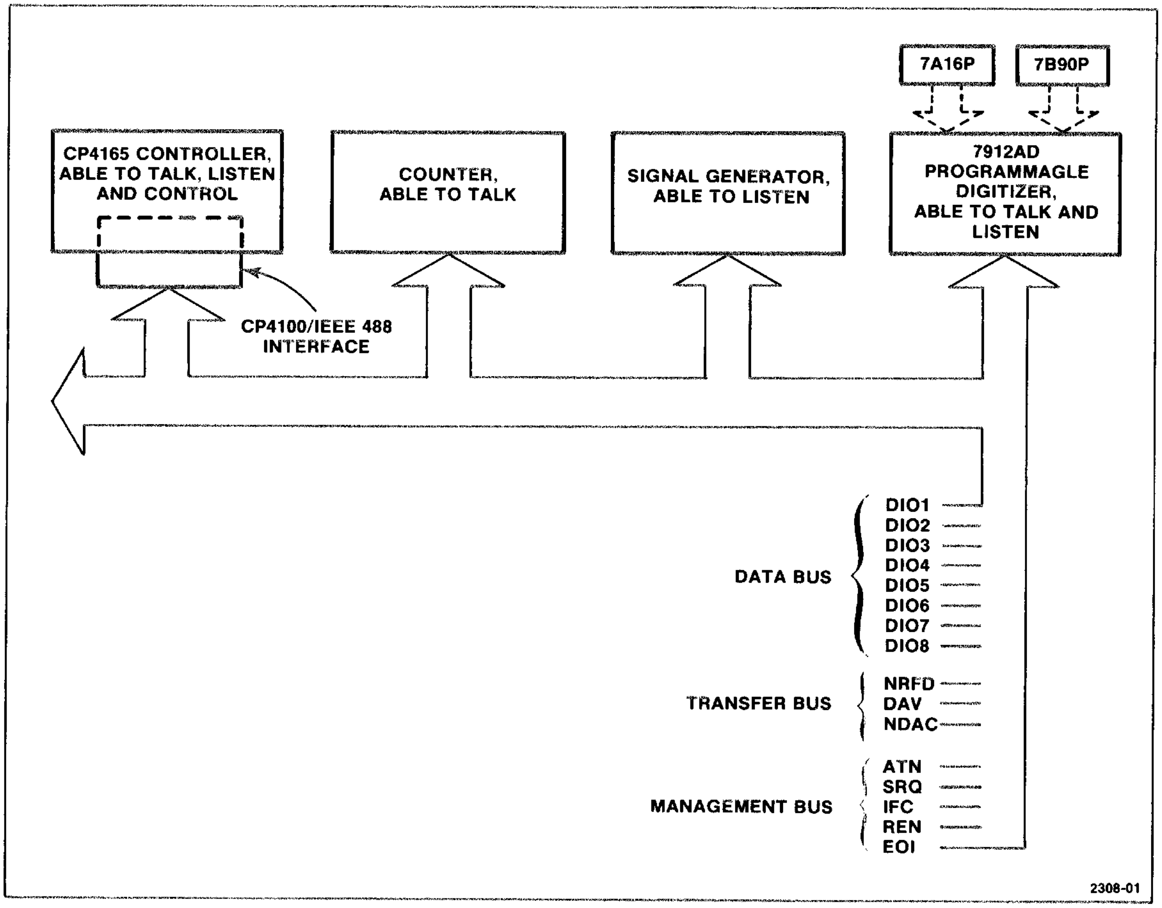

Fig. 3-1. A typical system based on the IEEE 488 Bus.

Types of Messages. Messages on the bus are either interface messages or device-dependent messages. Interface messages are used to manage the interface functions of the instruments. They designate talkers and listeners, determine local or remote operation of devices, indicate service requests, and communicate other important interface conditions. Device-dependent messages, by contrast, are not used to change the state or configuration of the interface, but are used to control the operating modes or device functions of designated instruments. Device-dependent messages can also be data, such as waveform data generated by the TEKTRONIX 7912AD Programmable Digitizer.

Maximum Number of Devices. Up to 15 devices can be connected on the IEEE 488 bus. More than 15 devices can be interfaced if they are not directly connected to the bus but are interfaced through another device. Such a scheme is used for the 7B90P plug-in housed in a 7000-Series programmable mainframe such as the 7912AD; the mainframe provides a transparent interface between the IEEE 488 bus and the plug-ins. Secondary addresses are used for the plug-ins. More than half of the main devices connected at any time must be powered-up for the system to be operational.

Maximum Cable Length. The maximum length of cable that can be used to connect a group of devices on the bus is:

1) 2 meters times the number of devices

2) Or 20 meters, whichever is less

Cables may be connected in either a star or linear configuration, or in a combination of the two methods.

Electrical Specifications. The relationship between the binary logic states of the bus and the voltages present on the signal lines is as follows:

Logical 1 corresponds to a low voltage level (+0.8 V or less) and the signal is said to be "asserted".

Logical 0 corresponds to a high voltage level (at least +2.0 V) and the signal is said to be "unasserted".

The electrical states are based on standard TTL (Transistor-Transistor Logic) levels where the power source does not exceed +5.25 Volts DC referenced to logic ground.

Bus Signal Lines

The IEEE 488 bus is functionally divided into three component busses: an eight-line Data Bus, a three-line Transfer (or handshake) Bus, and a five-line Management Bus. This bus structure is diagrammed in Fig. 3-1.

The eight lines of the **Data Bus** (DI01 through DI08) are bidirectional active-low lines used to convey data or device-dependent messages. Device addresses and universal commands are also transferred over these lines when ATN is asserted. One byte of information is transferred over the bus at a time. DI01 represents the least significant bit in the byte; DI08 represents the most significant bit. Data is transferred in byte-serial, bit-parallel fashion. Data bytes can be formatted in ASCII with or without parity, or they can be formatted in machine-dependent binary code. The term "machine-dependent binary code" refers to an internal binary format used by a device to store certain programs and data.

The **Transfer Bus** is used to communicate a handshake sequence that is executed between the talker and all designated listeners each time a byte is transferred over the Data Bus. This handshake sequence prevents the talker from placing a new byte on the bus until the slowest listener has captured the previous byte. Thus the talker can not transmit at a rate faster than can be received by the slowest listener. The three active-low lines of the Transfer Bus are NRFD, DAV, and NDAC. (See Fig. 3-2 for a basic timing relationship between these signals). Their functions are:

NRFD (Not Ready For Data) -- This signal line is asserted until all assigned listeners are ready to receive the next data byte. When all of the assigned listeners have released NRFD, the NRFD signal is unasserted, thereby allowing the talker to place the next byte on the Data lines.

DAV (Data Valid) -- The DAV signal line is asserted by the talker shortly after placing a valid byte on the Data lines. This tells each listener to capture the byte presently on the Data lines. DAV can not be asserted until NRFD has been unasserted.

NDAC (Not Data Accepted) -- This signal line is asserted by each listener until all have captured the byte currently on the Data lines. When the slowest listener has captured the data byte, NDAC is unasserted thereby allowing the talker to remove the byte from the Data lines. At that point, the DAV line is unasserted and the entire handshake cycle is repeated.

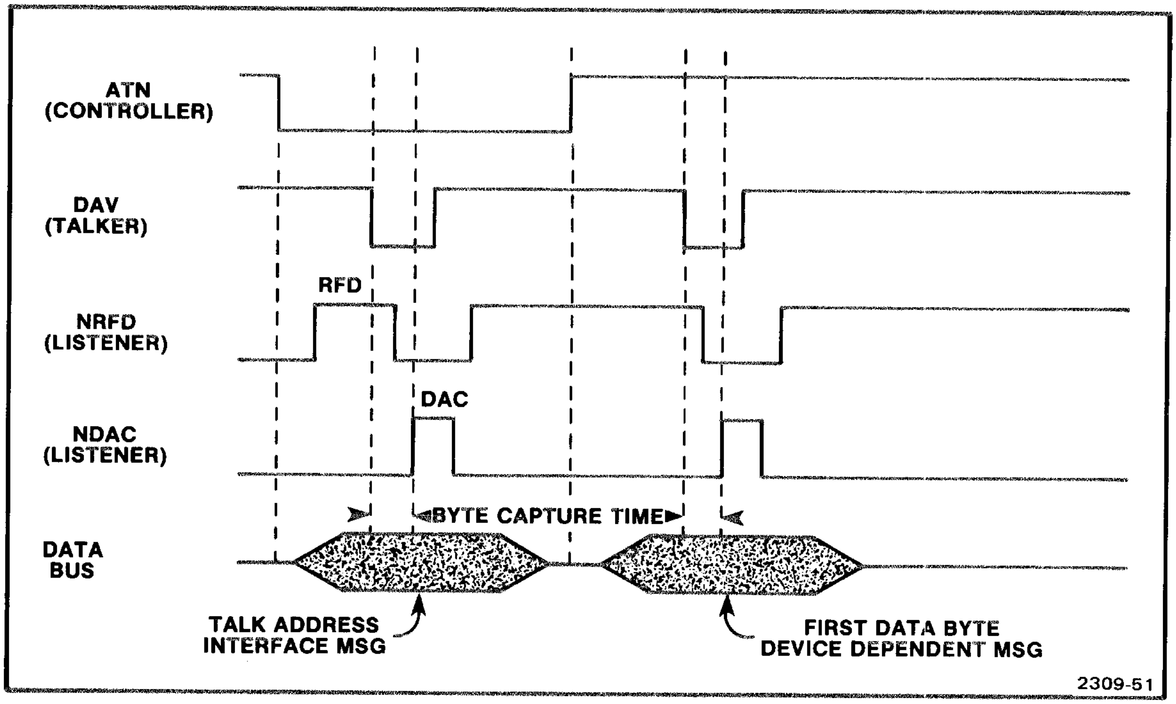

Fig. 3-2. A typical handshake sequence.

The **Management Bus** is a group of signal lines used to control data transfers over the Data Bus. These lines communicate important interface messages such as detecting an interrupt from a device, setting a device to remote control, and denoting the end of a message. The five active-low signal lines are ATN, IFC, SRQ, REN, and EOI; their functions are:

ATN (Attention) -- Asserted by the controller-in-charge to specify how information on the Data Bus is to be interpreted. When ATN is not asserted, the information on the Data Bus is interpreted as device-dependent messages and data. When ATN is asserted, the Data Bus conveys universal commands, addressed commands, talk addresses (MTA), listen addresses (MLA), or secondary addresses (MSA). Just which addresses and commands are sent depends upon the byte currently on the Data Bus. The codes corresponding to various commands and addresses are defined in Appendix E of the IEEE 488 standard.

IFC (Interface Clear) -- Asserted by the system controller to initialize the interface functions of all instruments to a quiescent state and return control to the system. The IFC function does the same thing as UNListen, UNTalk, Serial Poll Disable, and resets all devices except the system controller to the idle state.

SRQ (Service Request) -- Asserted by an instrument to request service from the controller-in-charge. The controller usually interrupts its current task and conducts a serial poll to determine which device interrupted. The controller can then branch to an interrupt service routine where appropriate action is taken. After the interrupt has been processed, the controller may resume execution of the previous task.

EOI (End Or Identify) -- Asserted by a talker to indicate the last byte of its message. When EOI is asserted with ATN, the controller conducts a parallel poll of the devices connected to the bus.

REN (Remote Enable) -- Asserted by the controller-in-charge to allow devices on the bus to go to Remote mode, thereby allowing remote control of their programmable functions. When in Remote mode, the front panels of the instruments are disabled except for any non-programmable functions.

Bus Messages

As previously noted, messages on the Data Bus are either interface messages or device-dependent messages. When the ATN line is asserted by the controller, all devices "pay attention" since interface messages are to be transferred over the Data lines. (By "pay attention" it is meant that all devices handshake and process all bytes transferred on the bus.) Interface messages can generally be classified as follows:

1) talk addresses
2) listen addresses
3) secondary addresses
4) universal commands
5) addressed commands

The first three categories refer to how a device is to be addressed. That is, they designate whether a device is to be a talker or a listener. To designate a device as a talker, the controller asserts ATN and places the device's talk address on the Data lines. Similarly, the controller designates a listener by asserting ATN and placing the address of the listener on the Data lines. In cases where secondary addressing is designed into a particular device, it is necessary to transmit the device's secondary address following the primary talk or listen address.

The fourth category listed above (universal commands) consists of those interface commands which affect all instruments connected to the bus, regardless of whether they are currently addressed as talker or listeners. Examples of universal commands are LLO (Local Lockout) and DCL (Device Clear).

The fifth category in the preceding list (addressed commands) consists of those interface commands which affect all instruments currently addressed as listeners. Examples of addressed commands are GTL (Go To Local) and GET (Group Execute Trigger). A complete list of universal and addressed commands is provided in Appendix E of the IEEE 488 standard.

In contrast to interface messages, device-dependent messages are sent with ATN unasserted and are transmitted only between a designated talker and one or more designated listeners. A device-dependent message can be either an instruction (e.g., set the input polarity to normal) or data (e.g., 3.456 volts). The format of instructions and data is entirely up to the device designer. Instructions and data are normally coded in ASCII or binary, but this is not required by the IEEE standard.

This has only been a brief introduction to the IEEE 488 interface. Further information can be found in IEEE Standard 488-1975, **IEEE Standard Digital Interface for Programmable Instrumentation.** A detailed description of the actual handshake timing sequence is covered in Appendix B of the standard.

7B90P Interface Function Subsets

The IEEE 488 standard is designed in such a way that not all devices on the bus need to have the same capability to comply with the standard. The instrument designer can choose from a "menu" of device functions, and implement only those capabilities (known as "functional subsets") that are appropriate to a particular device. The functional subsets are described in detail in the standard. The degree to which the 7B90P implements each of the ten interface functions is described below.

1) **Source Handshake** Function: SH1
The SH function provides a device with the ability to initiate and terminate transfer of multiline messages on the Data Bus. The 7B90P, in conjunction with the mainframe, conforms to subset SH1, meaning it has full capability with no states omitted.

2) **Acceptor Handshake** Function: AH1
The AH function provides a device with the capability to guarantee proper reception of messages on the Data Bus as well as the capability of delaying initiation or termination of such messages. The 7B90P conforms to subset AH1, meaning it has full capability with no states omitted.

3) **Talker** Function: TE6
The T function enables a device to send device-dependent data (including status information) over the bus to other devices. The 7B90P conforms to subset TE6, meaning it is an extended talker honoring secondary addresses. It has full capability except that it does not have a Talk-Only mode.

4) **Listener** Function: LE4
The L function allows a device to receive device-dependent data over the bus from other devices. This capability exists only when the device is addressed to listen. The 7B90P conforms to subset LE4, meaning it is an extended listener honoring secondary addresses. It has full capability except that it does not have a Listen-Only mode.

5) **Service Request** Function: SR1
The SR function enables a device to asynchronously request service from the controller-in-charge of the interface. The 7B90P conforms to subset SR1, meaning it has full capability.

6) **Remote/Local** Function: RL1
The RL function provides a device with the capability to select between two sources of information: remote (programmed control) or local (front-panel control). The 7B90P, in conjunction with the mainframe, conforms to subset RL1, meaning it has full capability.

7) **Parallel Poll** Function: PPØ
The PP function allows a device to present one bit of status to the controller-in-charge without being previously addressed to talk. The 7B90P conforms to subset PPØ, meaning it has no capability for responding to a parallel poll.

8) **Device Clear** Function: DC1
The DC function allows a device to be cleared (initialized) either by itself or as a group of devices. The 7B90P conforms to subset DC1, meaning it has full capability. When the 7B90P receives a DCL (Device Clear) interface message, its internal buffers are cleared and the front panel is set to the power-up state. However, DCL does not affect plug-in settings in Local mode.

9) **Device Trigger** Function: DT1
The DT function allows the operation of a device to be triggered (initiated) either individually or as part of a group. The 7B90P conforms to subset DT1, meaning it has full capability. The 7B90P does a Single-Sweep Reset when it receives a GET (Group Execute Trigger) command.

10) **Controller** Function: CØ
The C function provides a device with the capability for sending device addresses, universal commands, and addressed commands over the bus. The 7B90P conforms to subset CØ, meaning it cannot serve as controller.

Addressing the 7B90P

It was noted previously that two types of communication occur on the IEEE 488 bus: interface messages and device-dependent messages. The first type of communication occurs when the system controller asserts ATN and begins sending messages to all devices on the bus. The second type of communication occurs when ATN is unasserted; in this case, communication occurs only between a designated talker and one or more designated listeners.

Interface messages can occur without the assignment of talkers and listeners since, by definition, the controller has an active source handshake and all other devices have an active acceptor handshake. On the other hand, before a device-dependent message can be sent, a talker must be assigned and at least one listener must be assigned. The process of assigning talkers and listeners is referred to as "addressing".

Addressing Schemes

There are two types of addressing schemes allowed by the IEEE 488 standard: primary addressing and secondary addressing. It is up to the device designer to decide which type of addressing scheme is to be implemented on a particular device. That is, some devices use only primary addressing while others require secondary addressing. The 7B90P and its mainframe use a secondary addressing scheme.

On a device that uses **primary addressing**, up to 31 possible talk or listen addresses can be assigned to a particular device. Once a talk or listen address has been assigned to a device, this address becomes the "name" by which the controller refers to that device. However, this "name" can usually be changed since the address is generally determined by a bank of switches on the back panel of the instrument. (In some cases, the address is determined by straps on a circuit board inside the instrument.)

On a device that uses **secondary addressing**, a slightly different scheme is used. In this case, there are still 31 possible talk or listen addresses available. However, for each primary address there can be 31 possible secondary addresses corresponding to the primary address. This allows a total of 961 possible addresses for a device incorporating secondary addressing. Secondary addressing is sometimes used on instruments incorporating plug-in modules. An example is the TEKTRONIX 7912AD Programmable Digitizer and its two programmable plug-ins: the 7A16P and the 7B90P.

Primary and secondary addresses are sent over the Data Bus with ATN asserted. Data lines DI01 through DI05 are used to convey the actual device address. DI01 corresponds to the least significant bit and DI05 corresponds to the most significant bit. Data lines DI06 and DI07 determine whether this address is to be interpreted as a primary talk address (abbreviated MTA for My Talk Address), a primary listen address (abbreviated MLA for My Listen Address), or as a secondary address (abbreviated MSA for My Secondary Address). Incidentally, if DI06 and DI07 are ØØ, lines DI01-5 correspond to a universal or addressed command rather than a device address. This scheme is diagrammed in Fig. 3-3.

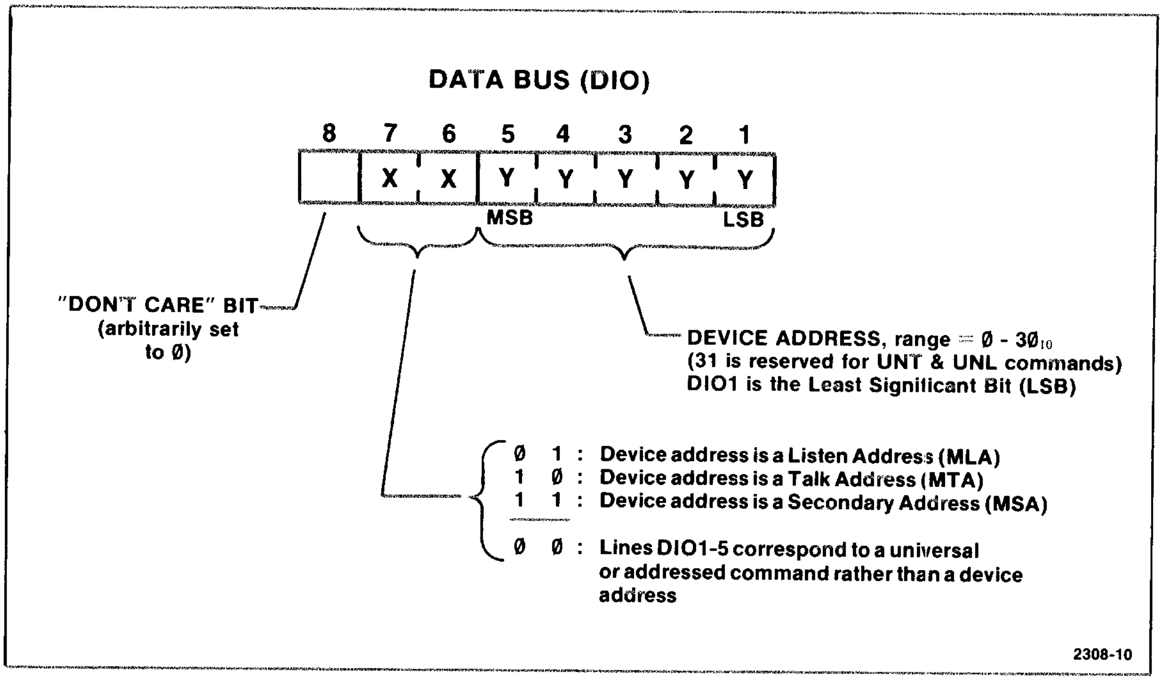

Fig. 3-3. Interpretation of the Data Bus (DI01-8) when ATN is asserted.

Determining Device Addresses

The 7B90P does not have any provision for changing its device addresses since these addresses are a function of the mainframe in which the plug-in is installed. In the case of the TEKTRONIX 7912AD Programmable Digitizer, the MSA of the plug-in installed in the vertical compartment (such as the 7A16P) is interpreted to be the MSA of the 7912AD plus 1. Similarly, the MSA of the plug-in installed in the horizontal compartment (such as the 7B90P) is interpreted to be the MSA of the 7912AD plus 2. However, this rule is not necessarily true for all mainframes. Refer to the manual for your particular mainframe if you need more information on this point.

So far, we have talked about addressing in general terms but have not discussed the actual procedure for addressing the 7B90P for a talk or listen operation. Perhaps an example using the 7912AD will best illustrate the method. Suppose that the 7912AD is set for a primary address of ØØØØØ and a secondary address of ØØØØ1. According to the scheme previously mentioned, the MLA, MTA, and MSA of the mainframe are:

$$MLA = 0100000 = 40_8 = 32_{10} = 20_{16}$$

$$MTA = 1000000 = 100_8 = 64_{10} = 40_{16}$$

$$MSA = 1100001 = 141_8 = 97_{10} = 61_{16}$$

To address the 7B90P as a listener, the controller asserts ATN and sends the MLA of the mainframe (32_{10}) on the Data Bus. With ATN still asserted, the controller sends the MSA of the 7B90P (99_{10}) on the Data Bus. Recall that the MSA of the time base is that of the 7912AD plus 2. ATN can now be unasserted so that the talker can begin sending device-dependent messages to the 7B90P.

To address the 7B90P as a talker, the controller asserts ATN and places the MTA of the mainframe (64_{10}) on the Data Bus. With ATN still asserted, the controller places the MSA of the 7B90P (99_{10}) on the Data Bus. ATN can now be unasserted so that the listener(s) can begin receiving device-dependent messages from the 7B90P.

High-Level Messages

7B90P high-level messages are device-dependent and therefore are not specified in the IEEE 488 standard. However, these high-level messages do conform to Tektronix standards intended to enhance Tektronix compatibility with other bus-compatible instruments. To accomplish this, codes and syntax are designed to be unambiguous, to correspond to those used by other Tektronix devices, and to be as simple and obvious as possible. This minimizes the cost and time required to program the 7B90P by making it easier for the programmer to write and understand the needed device-dependent code.

The 7B90P responds to device-dependent messages that contain one or both of two types of commands: Set and Query. During a Set command, the plug-in acts as a listener and uses the incoming information to effect certain operating modes or front-panel settings. During a Query command, the plug-in initially acts as a listener until receiving an UNListen command; then the plug-in is made a talker and returns the status of a specified function or operating parameter. The syntax of a Set and Query command is explained later.

A device-dependent message begins when the plug-in is addressed as a talker or listener, with ATN asserted. Then ATN is unasserted and the actual device-dependent code is transmitted from talker to listener. The message is terminated when EOI is asserted. EOI is sent concurrent with the last byte of the message, whether it be a data byte, a delimiter, or a format character.

When special driver software is being used, the user need not concern himself with all the details of initiating and terminating each message, since this is done automatically by the software. Most of this section thus deals with message syntax rather than message transmission. However, for those who are not using special-driver software, a brief discussion is included later as to the methods of initiating and terminating a message.

Explanation of Command Syntax

In describing the syntax of high-level commands, a modified form of the Backus-Naur format is used. According to this format, descriptive words such as "header", "format", or "argument" are enclosed in angle brackets (<>). Optional items are enclosed in square brackets ([]). An ellipsis

(...) indicates that the preceding argument may be repeated one or more times. Punctuation marks such as the semicolon and question mark are listed exactly as they are typed; hence they are not enclosed in angle brackets.

The syntax allows format characters at several pcints in each command. Where they are allowed, the word "format" is spelled cut. Format characters are always optional, so the word "format" is always shown in brackets. A format item can be a space, carriage return, line feed, or any combination of these characters.

Set Commands

Unless specifically designated as query (read) only, the headers and arguments listed in Table 3-1 can be used to form Set commands. Set commands are used to set the states of the various 7B90P programmable functions. A Set command for the 7B90P has the following syntax:

[<format>]<header><header delimiter>[<format>]<argument>

As previously noted, a format character is optional and may be a carriage return, line feed, space, or any combination thereof. The header delimiter is a space and is always required. The following are all examples of legal Set commands, where <cr> denotes a carriage return and <lf> denotes a line feed:

1) CPL DC
2) <lf>CPL DC
3) <cr>CPL DC
4) <cr><lf> CPL DC <cr>
5) T/D .ØØ5
6) <cr> T/D .ØØ5

Examples 1 through 4 set the trigger CouPLing to DC and examples 5 and 6 set the Time/Division to 5 milliseconds.

One or more Set commands can be included in the same message as explained later under the heading "Messages".

Query Commands

All of the headers in Table 3-1 can be used to form Query commands. Query commands are used to determine the states of the various 7B90P programmable functions. A Query command has the following syntax:

[<format>]<header>?

Again, <format> refers to an optional carriage return, line feed, space, or any combination thereof. The question mark (?) following the header argument must be typed without a preceding space or other format character.

Examples of Query commands are:

1) CPL?
2) <cr>CPL?
3) <cr><lf> CPL?
4) T/D?
5) <lf>T/D?

Examples 1 through 3 query the state of the CouPLing mode and examples 4 and 5 query the setting of the Time/Division switches.

One or more Query commands can be included in the same message as explained next.

TABLE 3-1

7B90P HIGH-LEVEL (ASCII) COMMAND SET

HEADER	ARGUMENT	DESCRIPTION
MOD	PPA	Peak-to-Peak Automatic triggering mode is selected.
	NOR	Normal triggering mode is selected.
	SSW	Single-sweep triggering mode is selected.
CPL	AC	Trigger signal is AC coupled.
	DC	Trigger signal is DC coupled.
	LFR	Trigger signal is AC coupled with low frequency rolloff.
	HFR	Trigger signal is AC coupled with high frequency rolloff.
SRC	INT	Trigger source is internal.
	LIN	Trigger source is the line voltage.
	EXT	Trigger source is external input.
	E1Ø	Trigger source is external attenuated 10X.
SLO	POS	Positive trigger slope is selected.
	NEG	Negative trigger slope is selected.
LEV	xxxx	Trigger level is set to xxxx; range is -6.4 to +6.35 in .05 steps. Query returns <nr2>.[1]
T/D	xxxx	Time/Division is set to xxxx; range is 5E-10 to 5E-1 in a 1-2-5 sequence. Query returns <nr3>.[1]
MAG	ON	Sweep magnifier is turned on (10X).
	OFF	Sweep magnifier is turned off (1X).
POS	xxxx	Sending POS .001 is not the same as POS ... Horizontal position of sweep is set to xxxx; range is -6.4 to +6.39 in 0.0125 steps (80 steps/division). Query returns <nr2>.[1] POS 1 moves the ...
HOL	xxxx	Trigger holdoff period is xxxx; range is 0 to 63 uncalibrated.
EOS	ON	End-of-Sweep SRQ signal is enabled.

(cont. next page)

TRI	ON OFF	Trigger light is on (read only). Trigger light is off (read only).
SSW	ARM DIS	Single Sweep is armed. A GET (Group Execute Trigger universal command) has the same effect. Single Sweep is disarmed (read only).
ID		Returns the plug-in type: TEK/7B90P,V77.1,LLL This means Tektronix 7B90P with language version 77.1 and low-level language.[2]
SET		Returns the setting of all of the above functions with the exception of the read-only ones.

FOOTNOTES:

1. <nr1>, <nr2>, and <nr3> are numerical formats defined in ANSI Standard X3.42.

2. The 77.1 nomenclature refers to the version of protocol implemented; it may be updated at a future date.

Summary of ANSI X3.42 Numerical Formats

<nr1> Signed or unsigned integers (no decimal point) preceded optionally by spaces (<sp>). The <nr1> representation of value "zero" must not contain a minus sign.

Examples: +1245, <sp>-328, <sp><sp>475, +ØØØØ

<nr2> Signed or unsigned numbers with a decimal point preceded optionally by spaces (<sp>). The <nr2> representation of value "zero" must not contain a minus sign.

Examples: Ø.123, <sp>+5.41, -6.42Ø, <sp><sp>Ø.ØØØ

<nr3> Floating-point numbers expressed in modified scientific notation. The mantissa always includes a decimal point and is preceded by sign (+, -, or <sp>). The exrad following the mantissa begins with the character E followed by a plus or minus sign and then one or more digits for the exponent. The <nr3> representation of value "zero" must contain an <nr2> zero followed by an exrad with plus sign and all zero digits.

Examples: -1.5E+Ø3, <sp>2.E-1, +5.ØE-2, +Ø.ØE+ØØ

Messages

A Set or Query command is referred to as a "message unit". One or more message units can be concatenated to form a message, if each unit is delimited by a semicolon (;). Using the preceding terminology, the syntax of a message may be described as:

<message unit>[;[<format>]<message unit>]...[;][<format>]

Notice that format characters may be included but are not required. Also, the ellipsis indicates that one or more message units, and accompanying optional format characters, may be included if they are delimited by a semicolon.

The simplest message consists of a single Set or Query command. For example, the following Set message sets the Time/Division to 5 milliseconds:

T/D .005

Similarly, the following Query message reads the setting of the Time/Division switches:

T/D?

When the 7B90P is made a talker, it responds by sending the current Time/Division setting. For the case of the preceding example, the following query response would be obtained:

T/D 5.E-3

This indicates that the time/division setting is 5 x 10^{-3} seconds (5 milliseconds).

Messages with Multiple Sets. More than one Set command can be sent in the same message by concatenating them with semicolons. For example:

SLO NEG; MAG OFF

This message sets the triggering SLOpe to the NEGative portion and then turns the sweep MAGnifier OFF.

Here are some other example of messages with multiple Set commands:

1) MOD PPA;CPL AC; MAG OFF;T/D .0005
2) <cr><lf>MOD PPA;<cr><lf>CPL AC;<cr><lf>MAG OFF;<cr><lf>T/D .0005

In each of the preceding two examples, there are four Set commands that accomplish the same settings, namely: triggering MODe is set to Peak-to-Peak Auto, AC CouPLing of the trigger signal is used, the sweep MAGnifier is turned OFF, and the Time/Division is set to 500 microseconds.

Messages with Multiple Queries. In a similar fashion, more than one Query command can be executed in the same message. With the 7B90P addressed as a listener, each query is received and the results are queued internally until the plug-in is made a talker. When the 7B90P is made a talker, the results of the query are output in the same order they were received. The response to the query is valid at the time of the response, rather than at the time the query is received. The following is an example of a multiple-query message and its resulting output:

```
MOD?;CPL?;SRC?;T/D?  <---- query message
MOD PPA;
CPL DC;               } query response
SRC INT;
T/D  5.E-5
```

Notice that the results of the query are executed in sequence and that a semicolon, carriage return, and line feed are generated after all but the last response.

When more than one Query command of the same type is included in the same message, only the last occurrence of the Query is executed. For example:

```
MAG?;EOS?;MAG?
```

Executing the above message would cause an output such as:

```
EOS ON;
MAG OFF
```

Since two MAG queries were executed in the same message, the first one was ignored.

The SET? Query. A special type of Query command is the SET? query. It interogates the status of all the programmable functions of the 7B90P. The SET? query is sent just like any other query message. That is, the 7B90P is made a listener and then SET? is sent over the Data Bus. When the plug-in is made a talker, an output such as the following is obtained:

```
T/D  1.E-6;
POS -Ø.25;
HOL 16;
MAG OFF;
MOD PPA;
CPL AC;
LEV -6.4;
EOS OFF;
SLO POS;
SRC INT
```

Normally, a SET? query will be the only query in a message. When a SET? query follows some other query in the same message, all queries preceding the SET? query are ignored. Also, any queries following the SET? query cause the SET? query to be ignored.

Messages with Sets and Queries. When Set and Query commands are included in the same message, the following action is taken: First, all Set commands are executed in the order they are received. This is true even if there are more than one Set command for the same function. After all Set commands are executed, the plug-in is made a talker and the results of the Query commands are executed in sequence. If more than one query for the same programmable function is received, all but the last occurence of that query is ignored.

To demonstrate the effect of multiple Sets and Queries in the same message, consider the following:

```
MOD PPA; MOD?; MOD NOR; MOD?
```

Executing the above message first sets the triggering mode to Peak-to-Peak Auto mode momentarily. Then, without further delay, the triggering mode is returned to normal as the next Set command is executed. With both Set commands executed, the queries are then executed. Since the MOD? query occurs twice, only the second occurence is honored. When the plug-in is made a talker, the following output is seen:

```
MOD NOR
```

Query Responses. The 7B90P responds to a query by sending the status of the queried function at the time of the response rather than at the time the query is received. A query remains valid (if the plug-in is made a talker, it will return the requested status) until one of the following occurs:

1) the plug-in is made a talker and sends the requested status.
2) a later message unit contains the same query (in this case the old query is cleared and replaced by the new one).
3) a DCL (Device Clear interface message) is received.

This allows you to mix Set and Query commands without regard to where the query is in the message. For example, executing:

```
SLO POS; SLO?; SLO NEG
```

causes a response of:

```
SLO NEG
```

Similarly, executing:

```
MAG ON; SET?; MAG OFF
```

results in an output such as:

```
T/D  1.E-6;
POS -Ø.2Ø;
HOL 17;
MAG OFF;
MOD NOR;
CPL AC;
LEV -6.4;
EOS OFF;
SLO NEG;
SRC INT
```

Notice that in each case, the result of the query is valid as though it was included last in the message.

Low-Level Messages

All of the programmable functions of the 7B90P can be set or queried by a low-level language that is completely redundant to the high-level language. The low-level code merely provides an alternative method of communication that requires less bus time for programming the plug-in because data is moved in fewer bytes. Also, the language is decoded faster.

Unlike the high-level language which allows Set and Query commands to be combined in the same message, the low-level language requires that Sets and Queries be entered as separate messages. However, it is possible to set or query more than one function in the same message, provided certain rules of syntax are followed.

The following conventions are used in discussing the 7B90P low-level code. The term "hexadecimal" or "hex" refers to a base-16 number. Syntax items shown inside square brackets ([]) are optional and can therefore be omitted. Angle brackets (<>) are used to show that the enclosed argument is a descriptive term.

NOTE

> The TEKTRONIX 7912AD Programmable Digitizer has an internal strap that allows it to generate an EOI when a linefeed is detected. If the 7912AD is strapped in this way and a 7B90P is installed, the 7B90P low-level code will not be functional. However, the high-level language will be functional if all messages to the plug-in are terminated by at least 17 spaces.

Set Messages

Both Set and Query messages are implemented in low-level code. The format of a Set message is as follows, where each line is a separate 8-bit byte representing a hexadecimal number:

15
<address>
<data>
<data>
.
.
.
<checksum>

The hex 15 (ASCII NAK character) identifies this message as a low-level Set message. The <address> byte specifies the starting address in 7B90P memory for storing the <data> byte(s) which follow(s). The <address> byte corresponds to a particular programmable function and the first <data> byte corresponds to the setting of that function. (See Table 3-2 for the "hexadecimal" codes corresponding to various functions and their settings). The allowable range for the starting address is ØØ to hex ØC. This address is automatically incremented between <data> bytes if more than one <data> byte is sent. If the address is automatically incremented beyond ØC by sending too many bytes, the extra bytes are ignored. If arguments other than the ones specified in Table 3-2 are sent, the 7B90P may be set to an illegal operating mode, but no damage will result.

The checksum is the 2's complement of the modulo-256 sum of all the preceding bytes of the message (including the 15 and address byte). Therefore the modulo-256 sum of all bytes in the message, including the checksum, is zero (for a correctly transmitted block).

TABLE 3-2a

7B90P LOW-LEVEL (HEXADECIMAL) CODES

ADDRESS	DATA	DESCRIPTION
ØØ		Plug-in Type. (read only)
	9Ø	Any data other than hex 9Ø written to this address causes a command error.
Ø1		Hold-Off
	xx	Range ØØ to FC, low two bits must be zero
Ø2		Position
	xx	High bits
Ø3		Position
	xx	Low bits. Position range moves center of sweep -6.39 divisions (ØØ ØØ) to +6.4 divisions (Ø3 FF). Center screen = Ø2 ØØ. Step size = 0.0125 divisions.
Ø4		Sweep Magnifier[1]
	ØØ	Magnifier Off
	Ø8	Magnifier On
Ø5		Sweep Rate
	xx	High bits, see Table 3-2b
Ø6		Sweep Rate
	xx	Low bits, see Table 3-2b
Ø7		Trigger Level
	xx	Range = -6.4 divisions (ØØ) to +6.35 divisions (FF), with step size of 0.05 div.

(cont. next page)

ADDRESS	DATA	DESCRIPTION
Ø8		Trigger Coupling
	Ø2	AC
	ØE	LFR
	ØB	HFR
	Ø8	DC
Ø9		Trigger Source
	1Ø	Internal
	2Ø	Line
	CØ	External
	4Ø	External÷10
ØA		Trigger Slope
	ØØ	Negative
	Ø8	Positive
ØB		Trigger Mode
	ØØ	Normal
	4Ø	PPA
	8Ø	Single Sweep
ØC		Single Sweep Arm, End-of-Sweep SRQ Enable
	xx	See Table 3-2c

FOOTNOTE

[1] To set read-out and front panel, sweep rate low bits must be changed also. If not changed, sweep is still magnified, but T/D? will return T/D error.

TABLE 3-2b

TIME/DIV CODE

TIME/DIV	MAG OFF	MAG ON
500 ps	- - -	Ø1 18
1 ns	- - -	Ø1 11
2 ns	- - -	ØØ 11
5 ns	- - -	Ø7 11
10 ns	Ø1 15	11 15
20 ns	ØØ 15	1Ø 15
50 ns	Ø7 15	17 15
100 ns	11 19	15 19
200 ns	1Ø 19	14 19
500 ns	17 19	1B 19
1 s	15 12	19 12
2 s	14 12	18 12
5 s	1B 12	27 12
10 s	19 16	25 16
20 s	18 16	24 16
50 s	27 16	2B 16
100 s	25 1A	29 1A
200 s	24 1A	28 1A
500 s	2B 1A	47 1A
1 ms	29 13	45 13
2 ms	28 13	44 13
5 ms	47 13	4B 13
10 ms	45 17	49 17
20 ms	44 17	48 17
50 ms	4B 17	4F 17
100 ms	49 ØB	- - -
200 ms	48 ØB	- - -
500 ms	4F ØB	- - -

TABLE 3-2c

SINGLE-SWEEP, EOS CODE

CODE	DESCRIPTION
xxxØ xxxx	Single Sweep Arm (write only).
Øxxx xxxx	Enable End-of-Sweep SRQ (write only).
1xxx xxxx	Disable End-of-Sweep SRQ (write only).
ØØxx ØØØØ	End-of-Sweep SRQ Enabled (read only).
1Øxx ØØØØ	End-of-Sweep SRQ Disabled (read only).
xØØx ØØØØ	Sweep Triggered (read only).
xØ1x ØØØØ	Sweep Not Triggered (read only).
xØxØ ØØØØ	Single Sweep Armed (read only).
xØx1 ØØØØ	Single Sweep Disarmed (read only).

Computing the Checksum

To compute the checksum, required as the last byte of a low-level Set or Query message, do the following:

1) Find the hexadecimal (base-16) sum of the preceding bytes of the message.

2) If the sum found in step 1 is greater than hex FF (256_{10}), convert it to modulo-256 by successively subtracting FF until the remainder is less than FF but greater than 0.

3) Convert the remainder from step 2 to binary representation.

4) Find the 2's complement by complementing all bits and adding 1.

5) Convert the resulting number back to hexadecimal representation, if desired.

To determine what <data> and <address> bytes are required to set a particular operating parameter, refer to Table 3-2. For example, let's suppose you wanted to set the triggering slope of the 7B90P to negative. By looking at the table, you note that the address of the trigger slope switch is ØA and the value corresponding to negative slope is ØØ. Thus the following hexadecimal numbers should be entered in sequence to effect negative-slope triggering:

15
ØA
ØØ
E1

The last byte sent (E1) is the 2's complement of the modulo-256 sum of the preceding three bytes (hex 1F).

Consider another example. Suppose that we want to set the following trigger parameters via the low-level code:

trigger level: -6.4 divisions
trigger coupling: DC
trigger source: internal
trigger slope: positive
trigger mode: Peak-to-Peak Automatic

To effect these settings, the following hexadecimal numbers must be sent over the Data lines in the sequence listed:

15
Ø7
ØØ
Ø8
1Ø
Ø8
4Ø
84

The explanation for the above numerical sequence is as follows: First a 15 is sent to indicate the beginning of a low-level Set message. Next, a Ø7 is sent which is the address corresponding to the 7B90P trigger level. The ØØ which follows sets the trigger level to -6.4 divisions as shown in Table 3-2a. The rest of the numbers in the sequence (Ø8, 1Ø, Ø8, and 4Ø) correspond to DC trigger coupling, internal trigger source, positive trigger slope, and PP AUTO triggering mode, respectively. The last number in the sequence (84) is the checksum.

When setting more than one programmable function with the same low-level Set message, it must be remembered that the address counter of the plug-in is incremented automatically if more than one data byte is sent. Thus the data bytes must be entered in sequence such that they correspond to the incremented address counter. In other words, successive Set codes can be entered only if they correspond to the normal sequence of the address counter as listed in Table 3-2a. If they do not correspond, then more than one low-level Set message must be used to set more than one programmable function.

Query Messages

Using the same syntax notation as just used for Set messages, the format of a low-level Query message can be defined as:

```
  11
[ <address>
  [<count>] ]
  <checksum>
```

The hex 11 (ASCII DCI character) identifies this message as a low-level Query message. The <address> byte specifies the first address in 7B90P memory to be read. The <count> byte specifies the number of addresses to be read. The <address> byte corresponds to a particular programmable function and the <count> byte designates how many successive functions are to be queried (see Table 3-2). If <address> and <count> are both omitted, all addresses are read beginning with address zero. If just <count> is omitted, only the address specified is read (count defaults to 1).

If the address specified is within range (ØØ to hex ØC), but <count> is too large, no error is reported; however, the output line includes data only up to and including ØC.

The checksum is always required and is computed in the same manner as for the Set message. That is, the checksum is the 2's complement of the modulo-256 sum of all the preceding bytes in the message.

To determine what <address> byte should be used in a particular Query message, refer to Table 3-2. If no <count> byte is included, the specified <address> byte will determine the programmable function to be queried. If a <count> byte is included, the <address> byte determines the first function to be queried, and as the address counter is incremented, additional functions following the first one queried are also queried.

As an example, suppose you wanted to query one function -- the setting of the sweep magnifier switch. In this case, no <count> byte is necessary and thus the following sequence of hexadecimal numbers would work:

11
Ø4
EB

The 11 identifies this message as a low-level query. The number following (4) is the address that contains the current setting of the sweep magnifier switch. Finally, the EB is the 2's complement of the modulo-256 sum of the preceding two bytes (hex 15). When the plug-in is made a talker, the setting of the sweep magnifier switch will be returned.

The response to a low-level Query message looks identical to a corresponding low-level Set message. For instance, if the setting of the sweep magnifier is queried as in the preceding example, a response like the following hexadecimal numbers could be obtained:

15
Ø4
Ø8
DF

The 15 designates a low-level query response. The Ø4 is the <address> byte corresponding to the sweep magnifier, and the Ø8 is the <data> byte corresponding to the OFF position. DF is the checksum.

Consider another example. This time let's query the state of the trigger source, trigger slope, and trigger mode switches. Since these switches correspond to consecutive addresses in Table 3-2, we can query all three settings in a single low-level Query message consisting of the following hexadecimal numbers:

11
Ø9
Ø3
E3

As in the previous example, the 11 identifies this message as a low-level query. The Ø9 which follows is the starting address in 7B90P memory that will be queried; it corresponds to the source of the trigger signal (i.e. internal, line, external, or external÷10). The Ø3 indicates that the address counter is to be incremented twice so that two more functions can be queried. These two successive functions are the trigger slope and trigger mode switches, corresponding to addresses ØA and ØB respectively. The message ends with the checksum E3.

The response to the above multiple-query message might be the following hexadecimal numbers:

15
Ø9
1Ø
Ø8
4Ø
8A

Again, the 15 indicates a response to a low-level query, and the Ø9 indicates the starting <address> byte -- which corresponds to the trigger source. The next three bytes (1Ø, Ø8, 4Ø) indicate that the trigger source is internal, the trigger slope is positive, and the trigger mode is Peak-to-Peak Automatic. The 8A is the checksum.

As a final example, consider the following low-level query:

11
EF

This query contains only the query designator (11) and the checksum (EF). Since the <address> and <count> bytes were both omitted, the state of all functions will be queried (addresses ØØ through ØC inclusive). This is analagous to high level SET? query which indicates all states of the plug-in when the plug-in is made a talker.

Transmitting Messages

The discussion so far has centered around the syntax of the high-level and low-level messages, rather than the process by which these messages are transferred from talker to listener and vice versa. When special driver software is being used, it is sufficient to know only the message syntax since most of the details of message transfer are handled automatically by the software. However, when using controllers for which driver software is not available, it is necessary to know something about the message protocol discussed in the IEEE 488 standard. The following information will provide these details by showing the states of the interface signal lines for typical message transfers.

Transmitting Set Messages

First, consider the case where a talker is transmitting a message to effect a certain front-panel setting on the 7B90P. Here is a summary of the steps involved:

1) **Clear the bus.** Before initiating any message transfer, it is a good idea to clear the bus of any previously assigned talker and/or listener(s). (In some cases, such as immediately following power-up, this step won't be necessary since no talker or listener will have been assigned.) To remove any talker or listener, the controller asserts ATN and sends the UNT and UNL interface messages on the Data lines. (According to Appendix E of the IEEE 488 standard, UNT corresponds to hexadecimal 5F and UNL corresponds to hex 3F.)

2) **Assign the talker and listener(s).** Before communication of device-dependent messages can occur, the controller must designate which device is to talk and which device(s) are to listen. This is done with ATN still asserted. To designate the talker, the controller sends the primary talk address (MTA) of that device. This is followed by the talker's secondary address (MSA) if secondary addressing is employed. Similarly, the controller designates the listener (the 7B90P in this case) by placing its primary listen address (MLA) on the Data lines. This must also be followed by the secondary address (MSA) of the listener since secondary addressing is employed in the 7B90P. The process is repeated for each listener on the bus, although some listeners may not have secondary addresses.

If the ATN signal line is continuously asserted during the period when the talker and listener(s) are assigned, the order in which the talker and listener(s) are assigned is unimportant.

In the case where the controller is to be the talker, it must have addressed itself as such and any other talkers must be idle. (Its talk address does not need to be sent over the bus.)

3) **Send the device-dependent message.** With the talker and listener(s) assigned, the ATN line is now unasserted to initiate transfer of the device-dependent message.

In the case of a high-level message, each ASCII character of the message is transferred in sequence according to the previously explained syntax. Only lines DI01 through DI07 of the Data Bus are used. DI01 corresponds to the least-significant bit of each 7-bit ASCII character and DI07 corresponds to the most-significant bit. Line DI08 of the Data Bus is a "don't care" bit. As each character is transferred over the Data Bus, the entire handshake cycle is executed. This guarantees proper reception of each character before permitting a new character to be transmitted.

In the case of a low-level message, the process is similar except that all eight Data lines (DI01 through DI08) are used for transferring the message. Lines DI01-4 transfer the low-order hexadecimal digit and lines DI05-8 transfer the high-order hexadecimal digit. The handshake sequence is essentially the same as for the high-level message.

4) **Terminate the message.** As the last character or digit of the message is sent, the talker asserts the EOI signal line along with the data byte. This is to inform the controller that the talker is finished so that other operations can begin. (All Tektronix instruments functioning as talkers assert EOI automatically when outputting the last data byte of the message, but this is not necessarily true of instruments from other manufacturers -- particularly those designed prior to the formal release of IEEE 488-1975.)

5) **Clear the bus.** Though step 4 actually terminates the message transfer, it is often desirable to clear the bus of talker and listener(s) so that other operations can proceed immediately. The procedure for doing this is identical to step 1.

As an example of the above steps, assume that the controller is to effect two front-panel settings on a 7B90P: the trigger slope will be set to positive, and the trigger mode will be set to Peak-to-Peak Automatic. (The plug-in is installed in a 7912AD mainframe set for a primary address of ØØØØØ and a secondary address of ØØØ1Ø.) The following steps would accomplish this:

1) The controller asserts ATN, then transmits hexadecimal 5F (UNT) and hex 3F (UNL) over Data lines DI01 through DI07.

2) With ATN still asserted, the controller sends hex 20 (the MLA of the mainframe) followed by hex 64 (the MSA of the 7B90P) on the Data lines. Recall from the subsection on **Addressing the 7B90P** that the MSA of the 7B90P is that of the mainframe plus 2. Since the controller is to be the talker, no talk address is sent.

3) a) In the case of a high-level message, the talker (controller) transmits each of the following ASCII characters over the Data lines:

    SLO POS; MOD PPA

   b) In the case of a low-level message, the following hexadecimal bytes are transferred over the Data lines:

    15
    ØA
    Ø8
    4Ø
    99

4) As the last character or hex byte is transmitted, the talker asserts EOI indicating the end of the message.

5) The controller again clears the bus by transmitting 5F (UNT) and 3F (UNL) over the Data lines.

Figure 3-4 illustrates the above sequence more graphically.

Figure 3-4 does not indicate the status of the IFC, REN, and SRQ signal lines because they are relatively unimportant to the point being made. However, it should be understood that the REN (Remote Enable) line is continuously asserted whenever the plug-in is being operated under remote (program) control, as opposed to local (front-panel) control. The

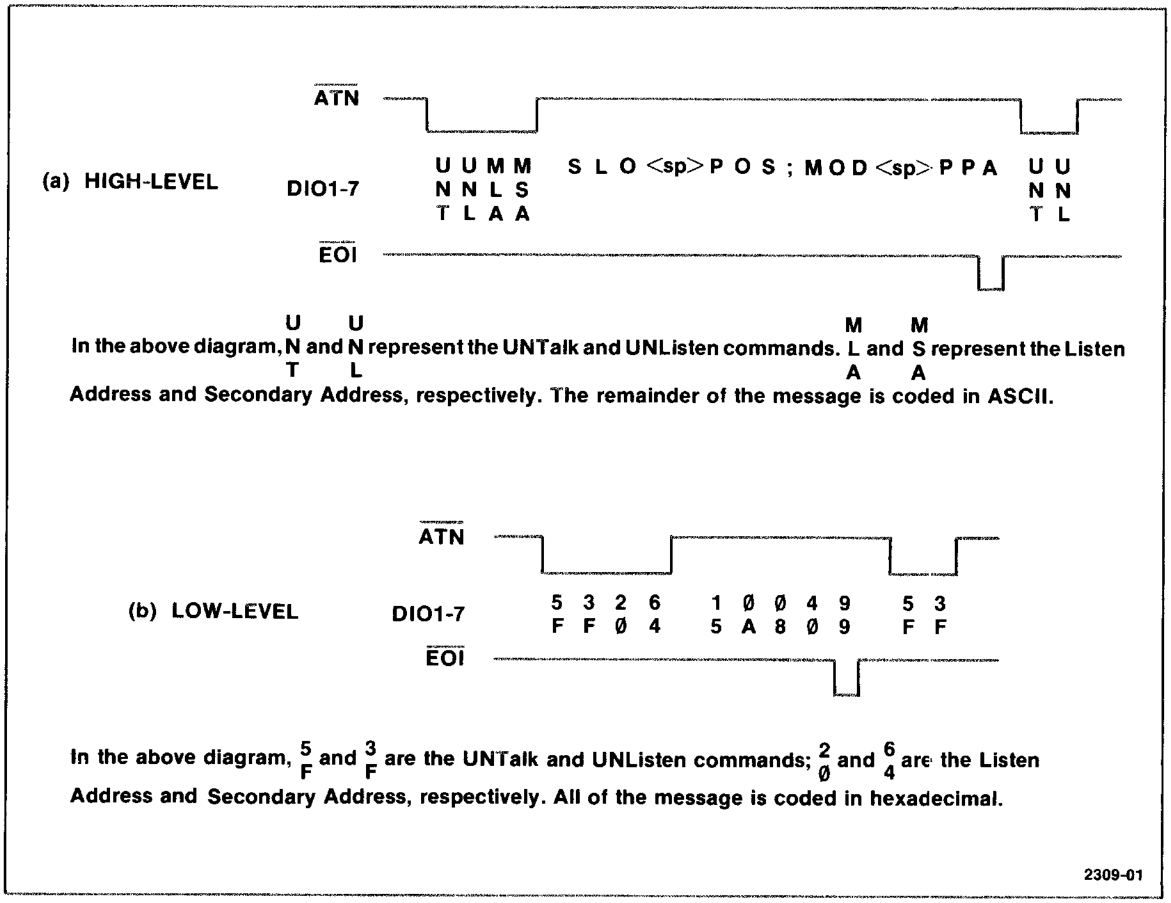

Fig. 3-4. Status of the ATN, EOI, and DIO signal lines during a high-level (a) and low-level (b) Set message.

IFC line will normally be unasserted during the entire sequence. The SRQ line can be asserted whenever a device requests service. However, it is not relevant to the process of data transmission diagrammed in Fig. 3-4 and is not shown.

While the handshake lines (DAV, NRFD, and NDAC) are important in the transmission of messages and data, their status changes several times during the transmission of each character in the message. Appendix B of the IEEE 488 standard gives a detailed description of this handshake cycle.

Transmitting Query Messages

The previous sequence describes the process for transmitting a Set message -- in which case the plug-in is always a listener. A similar sequence occurs when a Query message is sent to the plug-in. However, in this case the plug-in is first made a listener so that it can receive the Query message; then the plug-in is made a talker so that it can transmit its response to the query. Here is a summary of the steps involved:

1) **Clear the bus.** As previously noted, this step is not always necessary but is good practice. The controller asserts ATN and sends UNT (hex 5F) and UNL (hex 3F) over the Data lines.

2) **Assign the talker and listener(s).** The controller designates which device is to send the query and which device or devices are to receive the Query message. This is done with ATN still asserted. To designate the talker, the controller sends the primary talk address (MTA), followed by the talker's secondary address (MSA) if secondary addressing is used for that device. Similarly, the controller designates the listener (the 7B90P in this case) by sending its primary listen address (MLA) and secondary address (MSA). This process is repeated for each listener on the bus.

When the controller is to be the talker, it must have addressed itself as such and any other talkers must be idle. (Its talk address does not need to be sent over the bus.)

3) **Send the device-dependent query.** With the talker and listener(s) assigned, the ATN line is now unasserted to initiate transfer of the device-dependent query. Each ASCII character or hex byte of the message is transferred in sequence over the Data lines according to the previously explained syntax.

4) **Terminate the query.** As the last character or digit of the high-level query or series of queries is sent, the talker asserts EOI along with the message byte. This informs the controller that the talker is finished so that the query response can proceed.

5) **Clear the bus.** At this point it is necessary to clear the bus so that the plug-in can be addressed as a talker. Again, this is done by the controller asserting ATN and by sending the UNT and UNL interface commands over the Data lines.

6) **Assign the talker and listener(s).** With ATN still asserted, the controller now assigns the plug-in as a talker and assigns any additional listeners. If the controller is to be the only listener, it does not need to address itself as a listener.

7) **Send the device-dependent query response.** The ATN line is now unasserted by the controller to initiate transfer of the query response from the talker (plug-in) to any designated listener(s). Each ASCII character or hex byte of the query response is transmitted over the Data lines according to the previously described syntax for a query response.

8) **Terminate the query response.** As the last character or digit of the query response is sent, the talker (plug-in) asserts EOI along with the data byte, thereby indicating the end of the response.

9) **Clear the bus.** Though not required for this operation, the controller can now clear the bus of talker and listener(s) so that further operations can proceed.

As an example of the above steps, assume that the controller is to query and receive the status of two front-panel functions on the 7B90P: the sweep magnifier and the time/division settings. (The plug-in is installed in a 7912AD mainframe set for a primary and secondary address of ØØØ11.) The following steps describe the operations involved:

1) The controller asserts ATN, then transmits hexadecimal 5F (UNT) and 3F (UNL) over the Data lines, thereby clearing the bus.

2) With ATN still asserted, the controller transmits hexadecimal 23 (the MLA of the mainframe) followed by hex 65 (the MSA of the 7B90P) over the Data lines. This assigns the 7B90P as a listener.

3) a) In the case of a high-level message, the talker (controller) transmits each of the following ASCII characters over the Data lines:

MAG?; T/D?

b) In the case of a low-level message, the following hex bytes are transferred over the Data lines:

11
Ø4
Ø3
E8

4) As the last character of the query is transmitted, the talker (controller) asserts EOI.

5) The controller clears the bus of talkers and listeners by asserting ATN and sending hex 5F and 3F on the Data lines.

6) With ATN still asserted, the controller transmits hexadecimal 43 (the MTA of the mainframe) followed by hex 65 (the MSA of the 7B90P) over the Data lines. This assigns the 7B90P as a talker.

7) The talker (7B90P) now sends its query response to the listener (controller).

8) As the last character of the query response is transmitted, the talker (7B90P) asserts EOI.

9) The controller again clears the bus by asserting ATN and sending hex 5F and 3F.

Figure 3-5 illustrates the state of the ATN EOI, and Data lines for the above sequence and a typical query response.

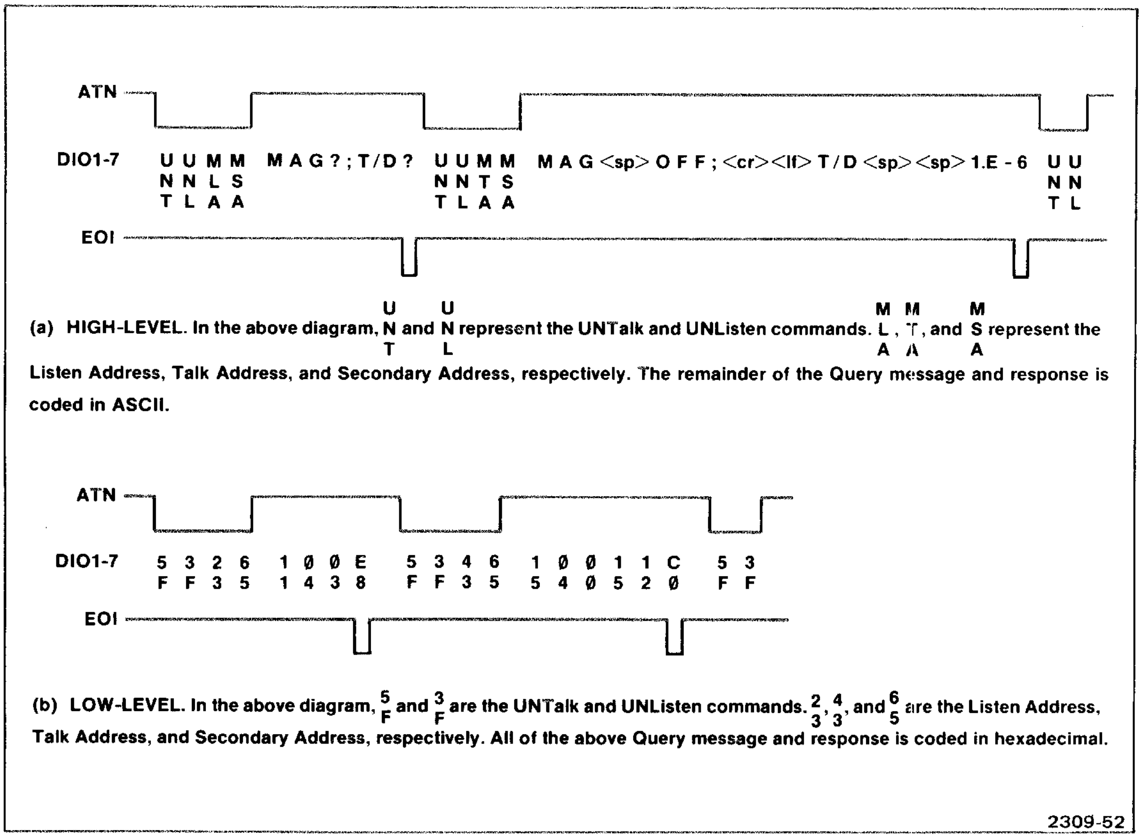

Fig. 3-5. Status of the ATN, EOI, and DIO signal lines during a high-level (a) and low-level (b) Query message and response.

Serial-Poll Responses

The 7B90P reports any of the following errors or special conditions when polled by the controller:

1) Power on
2) Command error
3) Execution error
4) End-of-sweep
5) Busy

If any of the above conditions (except Busy) occurs, the 7B90P asserts the SRQ line to initiate a serial poll. The controller, if programmed to do so, can then process the interrupt and provide an appropriate response. The following is a detailed description of each of the five conditions:

1) **Power on:** Occurs whenever the plug-in goes through its initialize sequence, either at the time that power is first applied, or when it is reapplied following momentarily interruption.

The serial-poll response byte is Ø1Øx ØØØ1, where x is a 1 if the 7B90P is busy, and a Ø otherwise.

2) **Command error:** Occurs whenever the plug-in cannot understand or implement the data it receives.

Command errors detected for low-level messages are: (a) the message is more than 16 bytes long, (b) the modulo-256 sum of all bytes in the message is not zero, (c) the starting address is too large, (d) no address is supplied with a Set message, or (e) an attempt was made to set address Ø (plug-in type) to the wrong value.

Command errors detected for high-level messages are: (a) syntax is incorrect, (b) a Set command refers to a read-only function, or (c) message units are not recognized by the 7B90P.

If an error is detected in a low-level message, the 7B90P ignores the entire command line. If the error is a low-level query address out of range, the output queue is cleared (i.e. if there are any query-responses pending, they are cleared).

If an error is detected in a high-level message, any message unit preceding the one with the error is processed normally. The one with the error and any following are ignored.

The serial-poll response byte for a command error is Ø11xØØØ1, where x signifies the busy status.

Occasionally, the 7B90P may be addressed as a talker, but have nothing to say. When this occurs, the plug-in sends a data byte with all Data lines set to a logical 1 (hex FF) and EOI asserted. Also, the plug-in reports a command error.

3) **Execution error:** Occurs when the numerical argument for a high-level Set command is invalid or out of the allowable range. The command for that function is ignored, as are any subsequent commands in the same message.

The serial-poll response byte for this type of programming error is Ø11xØØ1Ø, where x signifies the busy status.

4) **End of sweep:** Occurs at the end of sweep in the single-sweep mode if the End-of-Sweep SRQ has been enabled.

The serial-poll response byte is 11ØxØØØ1, where x signifies the busy status.

5) **Busy:** Occurs when a serial poll is performed while the plug-in is decoding a command; the response is xxx1xxxx. When not busy, the response is xxxØ xxxx (x is a "don't care" bit). The plug-in will not accept data on the bus while reporting busy.

The 7B90P queues power-up, command error, and execution error reports. If two or three conditions are waiting to be reported, SRQ is reasserted after reporting one error to indicate that there is more to report.

If an error is found in a high-level command string, SRQ is not asserted and the error is not reported until the message has been completely received (i.e. a byte with EOI asserted is received).

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO. REFER TO OPERATORS SAFETY SUMMARY AND SERVICE SAFETY SUMMARY PRIOR TO PERFORMING ANY SERVICE.

SECTION 4

MAINTENANCE

This section contains maintenance information for use in preventive maintenance, corrective maintenance, and troubleshooting of the 7B90P.

Further maintenance information relating to general maintenance can be found in the instruction manuals for the 7000-series mainframes.

Preventive Maintenance

Preventive maintenance, consisting of cleaning, visual inspection, etc., performed on a regular basis, will improve the reliability of this plug-in unit. Periodic checks of the semiconductor devices used in the unit are not recommended as a preventive maintenance measure. See semiconductor-checking information given under Troubleshooting.

The severity of the environment to which this instrument is subjected determines the frequency of maintenance. A convenient time to perform preventive maintenance is preceding adjustment of the instrument.

Cleaning

CAUTION

Avoid the use of chemical cleaning agents which might damage the plastics used in this unit. In particular, avoid chemicals that contain benzene, toluene, xylene, acetone, chlorothane, or similar chemicals.

Exterior. Loose dust may be removed with a soft cloth or a dry brush. Dirt that remains can be removed with a soft cloth dampened with a mild detergent and water solution. Abrasive cleaners should not be used.

Interior. Dust on the interior of the unit should be removed occasionally due to its electrical conductivity under high humidity conditions. Cleaning the interior of the unit should precede calibration, since the cleaning process could alter the settings of the calibration adjustments. Use low-velocity compressed air to blow off the accumulated dust. Hardened dirt can be removed with a soft, dry brush, cotton-tipped swab, or cloth dampened with a mild detergent and water solution.

Visual Inspection

This instrument should be inspected occasionally for such defects as broken connections, improperly seated semiconductors, damaged circuit boards, and heat-damaged parts.

The corrective procedure for most visible defects is obvious. However, particular care must be taken if heat-damaged components are found. Overheating usually indicates other trouble in the instrument; therefore, it is important that the cause of overheating be corrected to prevent recurrence of the damage.

Lubrication

There are no components in this instrument that require a regular lubrication program during the life of the instrument.

Troubleshooting

The following is provided to augment information contained in other sections of this manual when troubleshooting the 7B90P. The schematic diagrams, circuit description, and calibration sections should be used to full advantage. Section 5 gives detailed information on circuit behavior.

Troubleshooting Aids

Schematic Diagrams. Schematic diagrams are provided on foldout pages in Section 8. The circuit number and electrical value of each component are shown on the diagrams. Power supply voltages are also shown. Components that are mounted on circuit boards are outlined on the diagrams with a heavy black line.

Circuit-Board Illustrations. Illustrations of circuit boards are shown opposite the schematic diagrams. Each board-mounted electrical component is identified by its circuit number.

Component-Locator Grids. Schematic diagrams and circuit-board illustrations are bounded by component-locator grids. When used with the associated lookup tables, these grids allow you to quickly locate a component on either the schematic or the circuit board.

Component and Wiring Color Code. Colored stripes or dots on resistors and capacitors signify electrical values, tolerances, etc., according to the EIA standard color code. Components not color coded usually have the value printed on the body.

The insulated wires used for interconnection in the 7B90P are color coded to facilitate tracing wires from one point to another in the unit.

Semiconductor Lead Configuration. The lead configurations of the semiconductor devices used in this instrument are shown in Fig. 4-1.

Rear Interface Connector Pin Locations. The 7B90P SWEEP board couples the plug-in to the associated mainframe. Figure 4-2 identifies the pins on the interface connector as shown on the schematic diagrams.

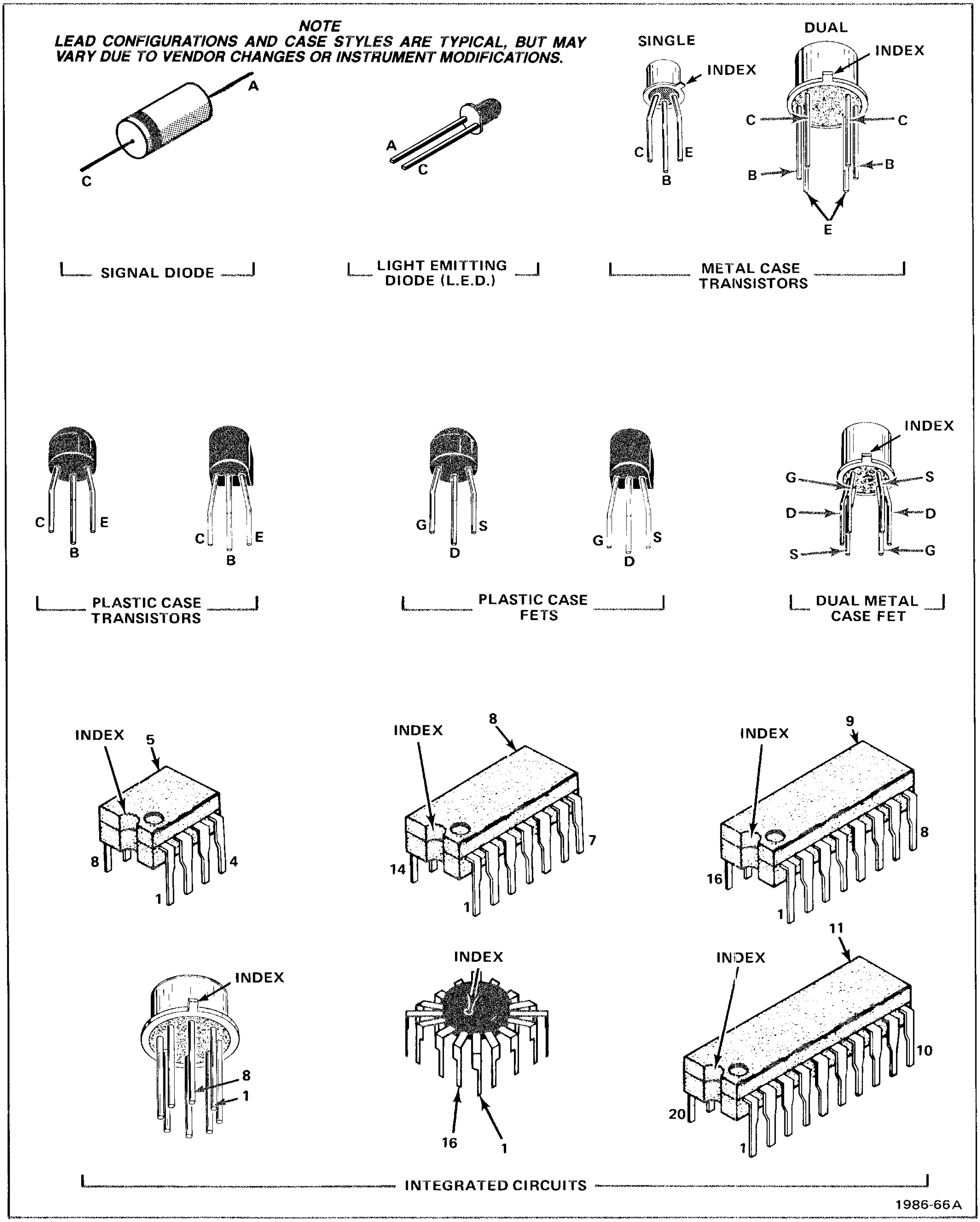

Fig. 4-15. Semiconductor lead configurations.

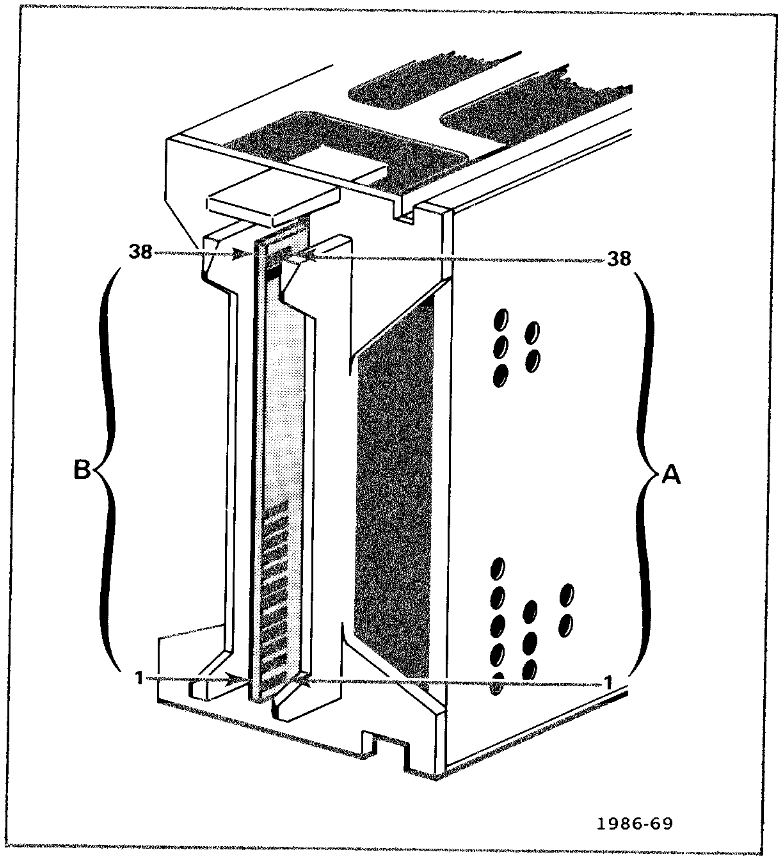

Fig. 4-2. Location of pin numbers on interface connector.

Troubleshooting Equipment

The following equipment is useful for troubleshooting the 7B90P.

1) **Semiconductor Tester** -- Some means of testing the transistors, operational amplifiers, comparitors, diodes, and FET's used in this instrument is helpful. A transistor-curve tracer such as the TEKTRONIX Type 577-177 or 577-178 will give the most complete information.

2) **Multimeter** -- A voltmeter is required for checking voltages within the circuits, and an ohmmeter for checking resistors and diodes. The voltmeter should have an input impedance of at least 10 megohm, a range of at least 0 to 50 volts DC, and an accuracy of 0.01%. The ohmmeter should have a range of 0 to 20 megohms.

3) **Test Oscilloscope** -- A test oscilloscope (with DC-100 MHz bandwidth) is required to view waveforms at different points in the circuits. A

TEKTRONIX 7000-series Oscilloscope equipped with a readout system, 7D13 Digital Multimeter unit, 7B-series Time-Base unit, and a 7A-series Amplifier unit with a 10X probe will meet the needs of both items 2 and 3.

4) **Plug-in Extender --** This fixture permits operation of the 7B90P outside of the plug-in comparment for better accessibility during troubleshooting. Order TEKTRONIX Part Number 067-0589-00.

Troubleshooting Procedure

This troubleshooting procedure is arranged in an order which checks the simple trouble sources before proceeding with extensive troubleshooting. The first few checks ensure proper connection, operation, and adjustment. If the trouble is not located by these checks, the remaining steps aid in locating the component. When the defective component is located, it should be replaced using the replacement procedure given under Corrective Maintenance.

1) **Check Control Settings.** An incorrect setting of the 7B90P controls can indicate a problem that does not exist. If there is any question about the correct function or operation of a control or front-panel connector, refer to the operating instructions provided in Section 2.

2) **Check Associated Equipment.** Before proceeding with troubleshooting of the 7B90P, check that the equipment used with this instrument is operating correctly. If possible, substitute a time-base unit known to be operating correctly into the mainframe and see if the problem persists. Check that any interconnecting cables are not defective.

3) **Visual Check.** Visually check the portion of the instrument in which the trouble is suspected. Many problems can be located by visual indications such as unsoldered connections, broken wires, damaged circuit boards, damaged components, or components bent over and touching other parts or circuit board runs.

4) **Check Instrument Adjustment.** Check the adjustment of the unit or the affected circuit by performing the Performance Check in Section 6. The apparent trouble may only be a result of mis-adjustment and may be corrected by calibration. Complete calibration instructions are given in Section 6.

5) **Isolate Trouble to a Circuit.** To isolate trouble to a circuit, note the trouble symptom. The symptom often identifies the circuit in which the trouble is located. When trouble symptoms appear in more than one circuit, check the affected circuits by taking voltage readings. Incorrect operation of all circuits sometimes indicates trouble in the power supply.

After the defective circuit has been located, proceed with step 6 to locate the defective components.

6) **Check Individual Components.** The following methods are provided for checking the individual components. Components which are soldered in place are best checked by disconnecting one end to isolate the measurement from the effects of surrounding circuitry.

CAUTION

To avoid component damage, disconnect the power source before removing or replacing semiconductors.

NOTE

To locate intermittent or temperature sensitive components mounted on the circuit boards, Quik Freeze (Miller Stephenson, MS-240, TEKTRONIX Part Number 006-0173-01) is recommended. Dry ice or dichloro-difluoromethane (Freon 12, Dupont or Can-O-Gas) may also be used.

A) TRANSISTORS. The best check of transistor operation is actual performance under operating conditions. Transistors that are soldered to the circuit board should first be checked in-circuit using a dynamic transistor tester; then a replacement can be substituted to further verify that the old transistor is bad. Socketed transistors can be checked immediately by substituting a known good component; however, be sure that circuit conditions are not such that a replacement might also be damaged. If substitute transistors are not available, check the old transistor out-of-circut using a dynamic tester (such as the TEKTRONIX Type 577-177). Static-type testers may be used, but since they do not check operation under simulated operating conditions, some defects may go unnoticed. Be sure the power is off before attempting to remove or replace any transistor.

B) INTEGRATED CIRCUITS. Analog IC's such as comparitors and operational amplifiers can usually be checked in-circuit with a voltmeter or test oscilloscope. An understanding of the device and circuit operation is essential for this type of troubleshooting. (For example, an op amp can be tested by measuring the input and output circuit voltages and comparing this ratio to the ratio of input and feedback resistors.) Analog IC's that are socketed can also be checked out-of-circuit using a dynamic tester such as the TEKTRONIX 577-178.

Digital IC's are best checked in-circuit using a logic probe or voltmeter. Use care when checking voltages and waveforms around DIP (Dual-In-line-Package) IC's so that adjacent leads are not shorted together. A convenient means of connecting a test probe to 14- and 16- pins IC's is with an IC test clip. This device also doubles as an extraction tool.

C) DIODES. A diode can be checked for an open or shorted condition by measuring the resistance between terminals with an ohmmeter set to the R X 1k scale. The diode resistance should be very high in one direction and very low when the meter leads are reversed. A diode can also be tested with a dynamic tester (transistor curver tracer).

CAUTION

Do not use an ohmmeter scale that has a high internal current. High currents may damage the diodes under test.

D) RESISTORS. Check resistors with an ohmmeter. Resistor tolerance is given in the **Electrical Parts List.** Resistors normally do not need to be replaced unless the measured value varies widely from the specified value.

E) CAPACITORS. A leaky or shorted capacitor can be detected by checking resistance with an ohmmeter on the highest scale. Use an ohmmeter that will not exceed the voltage rating of the capacitor. (Be careful to observe correct polarity when checking electrolytic capacitors.) The resistance reading should be high after initial charge of the capacitor. An open capacitor can best be detected with a capacitance meter, or by checking whether the capacitor passes AC signals.

7) **Repair and Readjust the Circuit.** Special techniques required to replace components in this unit are given under **Component Replacement.** Be

sure to check the performance of any circuit that has been repaired or that has had any electrical components replaced. Recalibration of the affected circuit may be necessary.

Specific Troubleshooting Information

The following information provides provides an aid to troubleshooting parts of the analog circuitry and the microprocessor system. This information is provided as a guide to troubleshooting the instrument; it is not intended to be a complete troubleshooting procedure. Before troubleshooting the instrument, an understanding of the circuit operation is required. Refer to the Circuit Description for a discussion of the circuit operation.

The following information is provided as an aid to troubleshooting only; it is not intended as a complete troubleshooting procedure.

Analog Circuits. Some of the transistors in the 7B90P are mounted in sockets to allow feedback loops to be opened as an aid to trouble-shooting. For example, when Q406 (part of the sweep-start current switch -- see schematic 2) is removed, the sweep ramp goes high (11 - 14 volts, measured at the collector of Q406) and remains there. If Q406 is replaced and Q400 removed, the sweep ramp stays low. The hold-off start logic, gate generator and sweep-start circuits can also be checked using this technique.

Trigger Circuits. If the trigger circuits are malfunctioning, the following steps may help to isolate the problem:

1) Measure the voltages around the trigger I.C. (U220). Pin 10 should be near D.C. ground, with about 20 millivolts of A.C. signal.

2) One of pins 2, 4, 6, or 8 should be near ground potential. All other pins should be held at about -2 volts. The SOURCE selected determines which pin is grounded as follows:

SOURCE	**GROUNDED PIN**
LINE	2
EXT	4
EXT ÷10	6
INT	8

DS348 and DS440 provide a visual indication of the selected source and check the operation of the associated biasing circuit. The LED's should be lit as follows:

SOURCE	**LEDS ON**
LINE	DS348, DS440
EXT	DS440
EXT ÷10	DS348
INT	DS348, DS440

3) Check the levels on pin 1 of U240. When + SLOPE is selected, pin 1 should be at about 0.5 volts. When - SLOPE is selected, the pin should be at about 4 volts.

Sweep Generator. Trouble in the sweep generator may be isolated using the following steps:

1) For the sweep to run, a GATE input to Q262 or AUTO SENSE to Q264 must be present. If either of these signals are present and there is no sweep, pull Q406 from its socket and check the voltage at TP422. The voltage should be about +5 volts. If not, check Q512, U110, and the associated components.

3) Remove Q400 and measure the voltage at the junction of R512 and R514. The voltage should be near ground.

4) DS001 and DS008 provide a visual indication of the state of the 1, 2, 5 voltage reference (U110). For example, when a multiple of 2 sweep speed (e.g. 2 milliseconds/division, 20 microseconds/division, etc.) is selected, DS001 and DS008 are both on. The LED states for 1, 2, and 5 sweep speed steps are shown below.

SWEEP SPEED STEP	**LEDs LIT**
1	DS008
2	DS001,DS008
5	NONE

Readout Circuits. U1000 accepts digital signals from the microprocessor and the time-slot counter and generates the analog row and column current that is sent to the mainframe. The levels on pins 4 and 5 of U1000 select the sweep speed symbol (milliseconds, microseconds, nanoseconds, or picoseconds) as shown below:

	U1000 PIN NO.	
	4	**5**
ms.	1	1
µs.	1	0
ns.	0	1
ps.	0	0

(1 = high -- +5 volts)

Pins 8 and 9 select the number of zeros in the readout. For example, a readout with two zeros (100, 200, 500) pin 8 is low and pin 9 is high. The levels on pins 8 and 9 are shown in the following table:

	U1000 PIN NO.	
	8	**9**
1,2,5	1	1
10,20,50	1	0
100,200,500	0	1

Pins 11 and 13 select the 1, 2, or 5 multiplier for the readout. The levels are summarized in the table below:

	U1000 PIN NO.	
	11	**13**
1	1	1
2	1	0
5	0	1

Pins 14, 15, 16, and 17 are the time-slot count inputs from U1005. U1005 counts the time-slots in a straight binary sequence and provides time-slot input to U1000.

Microprocessor System. If the 7B90P fails to power-up in the correct state, the following procedure provides an aid to locating the fault without special microprocessor service equipment.

1) Measure all the supply voltages. If they are out of tolerance, the power-up circuit in the plug-in will not initialize the micro-processor system correctly. Check for faults in the plug-in. If none are found, check the mainframe power supplies.

2) Temporarily remove the $\overline{\text{STOP}}$ strap, P1526, on the HORIZONTAL PROGRAMMING board. Press any front panel button (except $\overline{\text{TERM}}$) to cause an interrupt and start the MPU clock. Be sure to replace the $\overline{\text{STOP}}$ strap when you are through troubleshooting the clock circuit.

3) Check for valid two-phase clock signals at TP132 (Phase 1) and TP130 (Phase 2). Refer to the Calibration Procedure for a discussion of the MPU clock adjustment. If the clock signals are present, go to step eight.

4) Check that the clock jumper strap, P130 is correctly placed on the corresponding square pins.

5) Check the output (pin 3) of U010A. This pin should be high (+2.4 to 5.0 volts). If it is not, check the flip-flop formed by U310B and U1630B. The $\overline{\text{STOP}}$ line (pin 5 of U1630B) should be high.

6) Check pin 12 of U310B. If this pin is low, there is a fault in the power-up circuit (assuming the supply voltages are correct).

7) If no faults are found in steps four through six, there is a fault in the clock circuit.

8) Check pin 40 of U1220 ($\overline{\text{MPURES}}$) and pin 34 of U510 (RESET). If either of these lines is low, there is a fault in the power-up circuit.

9) Momentarily short pin 34 of U510 to ground. If the plug-in powers-up correctly, there is a fault in the power-up circuit.

10) Check that pin 2 of U1220 is high and pin 39 is low.

11) Check that pins 36 and 37 of U1220 are tied together.

12) If these tests fail to identify the fault, troubleshooting with a microprocessor debugging aid (such as a Tektronix 8000-series microprocessor lab) may be necessary.

Self Test Addresses. If the 7B90P fails to power-up and the above steps fail to identify the problem, the MPU may have detected a fault while performing the self-test routines. If a fault is detected the MPU "hangs" at a specified address. The fault can be determined by measuring the state of address bus lines (AØ-A11) with a DVM or logic analyzer (such as the Tektronix 7DØ1). Table 4-1 shows the addresses and the fault(s) detected, by the MPU for each address. If a fault is indicated in the ROM, RAM or PIA's, replace the involved components and see if the problem is cured.

TABLE 4-1

7B90P Self Test Hang Addresses

$79\text{Ø}A_{16}$	-	The RAM was filled with ones. Data was read back and complemented, and a non-zero byte was found. The RAM is left filled with zeros.
7915_{16}	-	Any ones left from the previous test hangs the 6800 here.
793Ø_{16}	-	The RAM failed a pattern-sensitivity test.
7958_{16}	-	The PIA control registers were filled with zeroes. The registers were read back and a one was found.
7978_{16}	-	The PIA registers failed a read/write test.
7992_{16}	-	The high-level ROM (U830) failed a checksum test.
$799E_{16}$	-	The low-level ROM (U630) failed a checksum test.

Control Line State Tables. The microprocessor controls the trigger and sweep generator circuits through several control lines. The following tables show the states of these lines for each sweep speed and triggering mode.

Table 4-2 shows the state of the sweep timing control lines (ST0-ST7) and the Intensity Limit (IL) control line for each sweep speed. The selected timing capacitor, reference voltage, decade resistor, and hold-off timing components are also shown for each sweep speed. (Refer to the Circuit Description for a discussion of these parameters.) For example, when the 7B90P TIME/DIV setting is one microsecond per division, sweep timing lines ST2, ST3 and ST5 are high. The remaining lines are low. At this sweep speed, C412 is selected as the timing capacitor (in parallel with C510 - refer to schematic 2) and R203 is selected as the decade resistor. The timing reference voltage is 2 volts (measured at the collectors of U110) and the timing current through Q512 is 500 microamps. The holdoff time is 3.5 microseconds, set by C644. The information in this table provides an aid to troubleshooting the ramp generator and its control circuitry.

Table 4-3 shows the state of the triggering control lines when each combination of TRIGGERING MODE, SOURCE and COUPLING is selected. For example, in PP AUTO MODE with INTernal SOURCE and AC COUPLING, the top row in the table indicates the state of each control line. A complete discussion of each of the control lines is given in the circuit description. The information in this table provides an aid to trouble-shooting the trigger generator and its control circuitry.

TABLE 4-2

Sweep Timing Information

TIME/DIV	SWEEP TIMING CONTROL LINES ST0	ST1	ST2	ST3	ST4	ST5	ST6	ST7	$\overline{\text{MAG}}$	IL	TIMING CAP	RES	REF VOLT	TIMING CURRENT	HOLDOFF CAPACITOR	TIME*
500 ps	1	0	1	0	0	0	0	0	0	0	C510	R108	2 v	5 ma	C644	3.5 µs
1 ns	0	0	1	0	0	0	0	0	0	0	C510	R108	2 v	5 ma	C644	3.5 µs
2 ns	0	1	1	0	0	0	0	0	0	0	C510	R108	1 v	2.5 ma	C644	3.5 µs
5 ns	0	0	0	1	0	0	0	0	0	0	C510	R203	4 v	1 ma	C644	3.5 µs
10 ns	0	0	1	0	0	0	0	0	1	0	C510	R108	2 v	5 ma	C644	3.5 µs
20 ns	0	1	1	0	0	0	0	0	1	0	C510	R108	1 v	2.5 ma	C644	3.5 µs
50 ns	0	0	0	1	0	0	0	0	1	0	C510	R203	4 v	1 ma	C644	3.5 µs
100 ns	0	0	1	0	0	1	0	0	1	0	C412	R108	2 v	5 ma	C644	3.5 µs
200 ns	0	1	1	0	0	1	0	0	1	0	C412	R108	1 v	2.5 ma	C644	3.5 µs
500 ns	0	0	0	1	0	1	0	0	1	0	C412	R203	4 v	1 ma	C644	3.5 µs
1 µs	0	0	1	1	0	1	0	0	1	0	C412	R203	2 v	500 µa	C644	3.5 µs
2 µs	0	1	1	1	0	1	0	0	1	0	C412	R203	1 v	250 µa	C644	3.5 µs
5 µs	0	0	0	0	1	1	0	0	1	0	C412	R202	4 v	100 µa	C622	35 µs
10 µs	0	0	1	0	1	1	0	0	1	0	C412	R202	2 v	50 µa	C622	35 µs
20 µs	0	1	1	0	1	1	0	0	1	0	C412	R202	1 v	25 µa	C622	35 µs
50 µs	0	0	0	1	0	0	1	0	1	0	C420	R203	4 v	1 ma	C620	350 µs
100 µs	0	0	1	1	0	0	1	0	1	0	C420	R203	2 v	500 µa	C620	350 µs
200 µs	0	1	1	1	0	0	1	0	1	0	C420	R203	1 v	250 µa	C620	350 µs
500 µs	0	0	0	0	1	0	1	0	1	0	C420	R202	4 v	100 µa	C626	3.5 ms
1 ms	0	0	1	0	1	0	1	0	1	0	C420	R202	2 v	50 µa	C626	3.5 ms
2 ms	0	1	1	0	1	0	1	0	1	0	C420	R202	1 v	25 µa	C626	3.5 ms
5 ms	0	0	0	1	0	0	0	1	1	0	C410	R203	4 v	1 ma	C730	35 ms
10 ms	0	0	1	1	0	0	0	1	1	0	C410	R203	2 v	500 µa	C730	35 ms
20 ms	0	1	1	1	0	0	0	1	1	0	C410	R203	1 v	250 µa	C730	35 ms
50 ms	0	0	0	0	1	0	0	1	1	0	C410	R202	4 v	100 µa	C730	35 ms
100 ms	0	0	1	0	1	0	0	1	1	1	C410	R202	2 v	50 µa	C730	35 ms
200 ms	0	1	1	0	1	0	0	1	1	1	C410	R202	1 v	25 µa	C730	35 ms
500 ms	0	0	1	1	0	0	0	1	1	1	C410	R200	4 v	10 µa	C730	35 ms

*Times shown in this column are minimum values. (HOLDOFF control fully counterclockwise).

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TABLE 4-3

Trigger Control Line States

MODE			SOURCE				COUPLING				Trigger Control Lines										
P-P AUTO	NORM	SGL SWP	INT	LINE	EXT	EXT.10	AC	AC LF REJ	AC HF REJ	DC	$\overline{PPA}$	$\overline{SS}$	$\overline{IT}$	LT	$\overline{ET1}$	$\overline{ET10}$	$\overline{ACI}$	$\overline{DCI}$	$\overline{ACE}$	$\overline{DCE}$	HFR
*			*				*				0	1	1	0	1	X	0	1	X	X	0
*			*					*			0	1	1	0	1	X	1	1	0	X	0
*			*						*		0	1	1	0	1	X	0	1	X	X	1
*			*							*	0	1	1	0	1	X	X	0	X	X	0
*				*			*				0	1	0	1	1	X	1	1	X	X	0
*				*				*			0	1	0	1	1	X	1	1	0	X	0
*				*					*		0	1	0	1	1	X	1	1	X	X	1
*				*						*	0	1	0	1	1	X	1	1	X	X	0
*					*		*				0	1	0	0	0	1	1	1	0	1	0
*					*			*			0	1	0	0	0	1	1	1	1	1	0
*					*				*		0	1	0	0	0	1	1	1	0	1	1
*					*					*	0	1	0	0	0	1	1	1	X	0	0
*						*	*				0	1	0	0	1	0	1	1	0	1	0
*						*		*			0	1	0	0	1	0	1	1	1	1	0
*						*			*		0	1	0	0	1	0	1	1	0	1	1
*						*				*	0	1	0	0	1	0	1	1	X	0	0
	*		*				*				1	1	1	0	1	X	0	1	X	X	0
	*		*					*			1	1	1	0	1	X	1	1	0	X	0
	*		*						*		1	1	1	0	1	X	0	1	X	X	1
	*		*							*	1	1	1	0	1	X	X	0	X	X	0
	*			*			*				1	1	0	1	1	X	1	1	X	X	0
	*			*				*			1	1	0	1	1	X	1	1	0	X	0
	*			*					*		1	1	0	1	1	X	1	1	X	X	1
	*			*						*	1	1	0	1	1	X	1	1	X	X	0
	*				*		*				1	1	0	0	0	1	1	1	0	1	0
	*				*			*			1	1	0	0	0	1	1	1	1	1	0
	*				*				*		1	1	0	0	0	1	1	1	0	1	1
	*				*					*	1	1	0	0	0	1	1	1	X	0	0
	*					*	*				1	1	0	0	1	0	1	1	0	1	0
	*					*		*			1	1	0	0	1	0	1	1	1	1	0
	*					*			*		1	1	0	0	1	0	1	1	0	1	1
	*					*				*	1	1	0	0	1	0	1	1	X	0	0
		*	*				*				1	0	1	0	1	X	0	1	X	X	0
		*	*					*			1	0	1	0	1	X	1	1	X	X	0
		*	*						*		1	0	1	0	1	X	0	1	X	X	1
		*	*							*	1	0	1	0	1	X	X	0	X	X	0
		*		*		*					1	0	0	1	1	X	1	1	X	X	0
		*		*			*				1	0	0	1	1	X	1	1	X	X	0
		*		*				*			1	0	0	1	1	X	1	1	X	X	1
		*		*					*		1	0	0	1	1	X	1	1	X	X	0
		*			*		*				1	0	0	0	0	1	1	1	0	1	0
		*			*			*			1	0	0	0	0	1	1	1	1	1	0
		*			*				*		1	0	0	0	0	1	1	1	0	1	1
		*			*					*	1	0	0	0	0	1	1	1	X	0	0
		*				*	*				1	0	0	0	1	0	1	1	0	1	0
		*				*		*			1	0	0	0	1	0	1	1	1	1	0
		*				*			*		1	0	0	0	1	0	1	1	0	1	1
		*				*				*	1	0	0	0	1	0	1	1	X	0	0

Corrective Maintenance

Corrective maintenance consists of component replacement and instrument repair. Special techniques required to replace components in this instrument are given here.

Obtaining Replacement Parts

Standard Parts. All electrical and mechanical part replacements for the 7B90P can be obtained through your local Tektronix Field Office or representative. However, many of the electronic components can be obtained locally in less time than is required to order them from Tektronix, Inc. Before purchasing or ordering replacement parts, check the parts list for value, tolerance, rating and description. The vendor's or manufacturer's part number and address are also provided in the parts list.

NOTE

When selecting replacement parts, it is important to remember that the physical size and shape of a component may affect the performance of the instrument, particularly at high frequencies. All replacement parts should be direct replacements unless it is known that a different component will not adversely affect instrument performance.

Order all special parts directly from your local Tektronix Field Office or representative.

Ordering Parts. When ordering replacement parts from Tektronix, Inc., include the following information:

1) Instrument Type.

2) Instrument Serial Number.

3) A description of the part (if electrical, include circuit number found in the Replaceable Electrical Parts list - Section 7).

CKT NUMBERING EXAMPLE:

R162 on A12 Assembly = R12162 in Parts List

Assembly Number

4) TEKTRONIX Part Number.

Soldering Techniques

WARNING

Disconnect the instrument from the power source before soldering.

Circuit Boards. The components mounted on the circuit boards in the 7B90P can be replaced using normal circuit-board soldering techniques. Keep the following points in mind when soldering on the circuit boards:

1) Use a pencil-type soldering iron with a wattage rating from 15 to 50 watts.

2) Apply heat from the soldering iron to the junction between the component and the circuit board.

3) Heat-shunt the lead to the component by using a pair of long-nose pliers.

4) Avoid excessive heating of the junction with the circuit board, as this could separate the circuit board wiring from the base material.

5) Use only 60-40 rosin core, electronic grade solder.

6) Clip off any excess lead length extending beyond the circuit board. Clean off any residual flux with a flux-removing solvent.

Metal Terminals. When soldering metal terminals (TERM switch and EXT TRIG IN connector) use 60-40 tin-lead solder and a 15 to 50 watt soldering iron. Observe the following precautions when soldering metal terminals:

1) Apply only enough heat to make the solder flow freely.

2) Apply only enough solder to form a solid connection. Excess solder may impair the function of the part.

3) If a wire extends beyond the solder joint, clip off the excess.

4) Clean the flux from the solder joint with a flux-removing solvent.

Component Replacement

WARNING

Disconnect the equipment from the power source before replacing components.

Semiconductor Replacement. Some transistors in the 7B90P are socketed. These should not be replaced unless actually defective. If removed from their sockets during routine maintenance, return them to their original sockets. Unnecessary replacement of transistors may effect the calibration of this instrument. When transistors are replaced, check the performance of any part of the instrument that may be affected.

WARNING

CMOS parts are very susceptable to damage due to static discharge. The operator and instrument should be grounded when parts are being replaced. Place CMOS parts on static-free foam during storage.

Replacement semiconductors should be of the original type or a direct replacement. The schematic diagram shows the lead configurations of the semiconductors used in this instrument. If the replacement semiconductor is not of the original type, check the manufacturer's basing diagram for proper basing.

Front-Panel LED's. When replacing any front-panel LED's (Light Emitting Diodes), be sure to place the new one(s) in the same exact alignment with the other LED's to facillitate reassembly of the front panel. When soldering LED's, use the minimum heat required to do the job. (For board removal, see A) Removal of LED and SWITCH Boards.)

Free-Standing Components. When replacing components that are free-standing (not directly mounted to circuit boards), be sure to place the new components in the same physical location and position as the old components. If this is not done, the high frequency characteristics of the plug-in may be altered; also, there may be a possibility of components touching and causing a short circuit.

Circuit Board Removal

The 7B90P contains the following circuit boards:

1) LED board
2) SWITCH board
3) TRIGGER board
4) SWEEP board
5) SHIELD board
6) HORIZONTAL PROGRAMMING board

The LED and SWITCH boards are attached to the front-panel casting. The TRIGGER, SWEEP, SHIELD, and HORIZONTAL PROGRAMMING boards are all connected together via mounting studs and multi-pin (interboard) connectors. These four boards are held to the plug-in frame via special fastening nuts that hold the SWEEP board to the top and bottom plug-in rails. (The SHIELD board simply insulates and shields the SWEEP board from the HORIZONTAL PROGRAMMING board; there are no components mounted to it, and it is electrically grounded to the SWEEP board.)

In general, the HORIZONTAL PROGRAMMING board will rarely need to be removed during troubleshooting since most of its components are readily accessable. The components on the TRIGGER board are also readily accessable, but it may be necessary to remove the TRIGGER board to expose certain components on the SWEEP board. The LED and SWITCH boards must be removed when replacing front-panel components such as the Light Emitting Diodes (LEDs).

The following procedure explains how to remove each of these boards from the rest of the plug-in. Peforming all of these steps in the order listed will result in a complete disassembly of the 7B90P. To reassemble the plug-in, reverse the process.

A) **Removal of LED and SWITCH Boards**

1) Remove the side panels from the plug-in.

2) Remove the front-panel LEVEL, POSITION, and HOLD OFF knobs by loosening their Allen set-screws.

3) Remove the tension spring from the end of the plug-in pull latch (inscribed with the word "7B90P").

4) Dismount the front-panel cover plate by gently prying on the bottom with a regular screwdriver.

5) Remove the jumper wires connecting the LED board to connectors P550 and J436 on the TRIGGER board.

6) Remove the four Phillips screws (one from each corner) of the front-panel casting.

7) Gently rock the front-panel casting to remove the front-panel assembly from the edge connector on the SWEEP board.

8) With the front-panel assembly removed, unsolder capacitor C402 and resistor R400 at the points where they connect to the LED board; also unsolder the ground lead (from the LED board) at the point where it connects to the TERM switch.

Note: The position and length of these components should be noted so that they can be replaced as originally installed. Otherwise, the VSWR may be adversely affected.

9) To dismount the LED board, remove all five Phillips screws; then carefully separate the LED board from the SWITCH board.

B) **Removal of TRIGGER Board**

1) Remove side panel from left side of plug-in, if not previously removed.

2) Disconnect the four coaxial end-leads that connect to J002, J212, J264, and J436 on the TRIGGER board. Also, pull the jumper wire end-lead that connects to P550 on the TRIGGER board.

3) Loosen the four Phillips screws from the studs connecting the TRIGGER board to the SWEEP board. (These do not remove completely; they are captive screws.)

4) Carefully lift the TRIGGER board from the SWEEP board. Use a gentle prying motion to separate the multi-pin (interboard) connectors. (When later replacing these boards, engage the top multi-pins first, then the lower ones. Be careful not to bend the pins.)

C) **Removal of HORIZONTAL PROGRAMMING and SHIELD Boards**

1) Remove side panel from right side of plug-in, if not previously removed.

2) Loosen the six Phillips screws from the mounting studs that hold the HORIZONTAL PROGRAMMING board to the SWEEP board. (These do not remove completely; they are captive screws.)

3) Carefully lift the HORIZONTAL PROGRAMMING board from the SHIELD and SWEEP boards. Use a gentle prying motion to separate the multi-pin (interboard) connectors.

4) To separate the SHIELD board from the SWEEP board, remove the spring retainers from the mounting studs on the SWEEP board.

NOTE

After removing the TRIGGER, HORIZONTAL PROGRAMMING, and SHIELD boards, it should not be necessary to remove the SWEEP board to access its components. However, the following steps are provided in the event that the entire circuit board must be replaced.

D) **Removal of SWEEP Board**

1) If the TRIGGER, HORIZONTAL PROGRAMMING, and SHIELD boards have not been removed, perform all steps of procedures B and C, above.

2) If the front panel has not been removed, remove the 7B90P Rear Interface panel by unscrewing the four Phillips screws at each corner. (The SWEEP board can be removed out the front or rear of the plug-in.)

3) Remove the screws from the top of the three fasteners that hold the SWEEP board to the top and bottom plug-in rails.

4) Slide the SWEEP board assembly out from the plug-in rails. The plastic clip on the top rail should slide with the circuit board.

Recalibration After Repair

After any electrical component has been replaced, the calibration of that particular circuit should be checked, as well as the calibration of other closely related circuits. Refer to Section 6 for these procedures.

Repackaging For Shipment

If the Tektronix instrument is to be shipped to a Tektronix Service Center for service or repair, attach a tag showing: owner (with address) and the name of an individual at your firm that can be contacted. Include complete instrument serial number and a description of the service required.

Save and re-use the package in which your instrument was shipped. If the original packaging is unfit for use or not available, repackage the instrument as follows:

> Surround the instrument with polyethylene sheeting to protect the finish of the instrument. Obtain a carton of corrugated cardboard of the correct carton strength and having inside dimensions of no less than six inches more than the instrument dimensions. Cushion the instrument by tightly packing three inches of dunnage or urethane foam between carton and instrument, on all sides. Seal carton with shipping tape or industrial stapler.

The carton test strength for your instrument is 200 pounds.

SECTION 5

CIRCUIT DESCRIPTION

Introduction

This section describes the 7B90P block diagram and circuit operation in detail. Frequent reference is made to the schematic diagrams at the rear of the manual. Each fold-out schematic is tabbed and numbered for ease of use. As you go through the following descriptions, unfold the appropriate schematics and refer to them as needed.

Block Diagram

Before we begin the detailed circuit descriptions, we will discuss the block diagram shown in Fig. 5-1.

The trigger generator provides a stable display by starting the sweep generator at a controlled point for each sweep. The trigger signal is taken from the INTernal or LINE trigger signals from the mainframe or the EXT TRIG IN connector on the front panel. The sweep logic sets up the control signals for PP AUTO (Peak-to-Peak Auto), NORM (NORMal) or SGL SWP (SinGLe SWeeP) modes. This circuit also generates the hold-off timing for the sweep generator. The sweep generator provides a precise ramp voltage for the sweep outputs. The sweep time is calibrated from 500 picoseconds to 500 milliseconds per division. The horizontal preamp provides differential sweep signals to the mainframe and adds DC current for sweep positioning. If the MAGnifier is selected, the gain of the horizontal preamp is increased by a factor of ten (or 20 for 500 ps/DIV) to magnify the sweep.

The 7B90P sweep speed, triggering, front panel LED's (Light-emitting Diodes) and IEEE 488-1975 interface are controlled by a microprocessor system in the plug-in. The heart of this system is a Motorola M6800 Microprocessing Unit (MPU). A control program, resident in 4K (1K=1024) bytes of Read Only Memory (ROM) directs the MPU activity. The MPU also uses 128 bytes of Random Access Memory (RAM) as a "scratch pad".

Five Peripheral Interface Adapters (PIA's) handle internal communication between the MPU and other circuits in the plug-in. The IEEE 488 (also

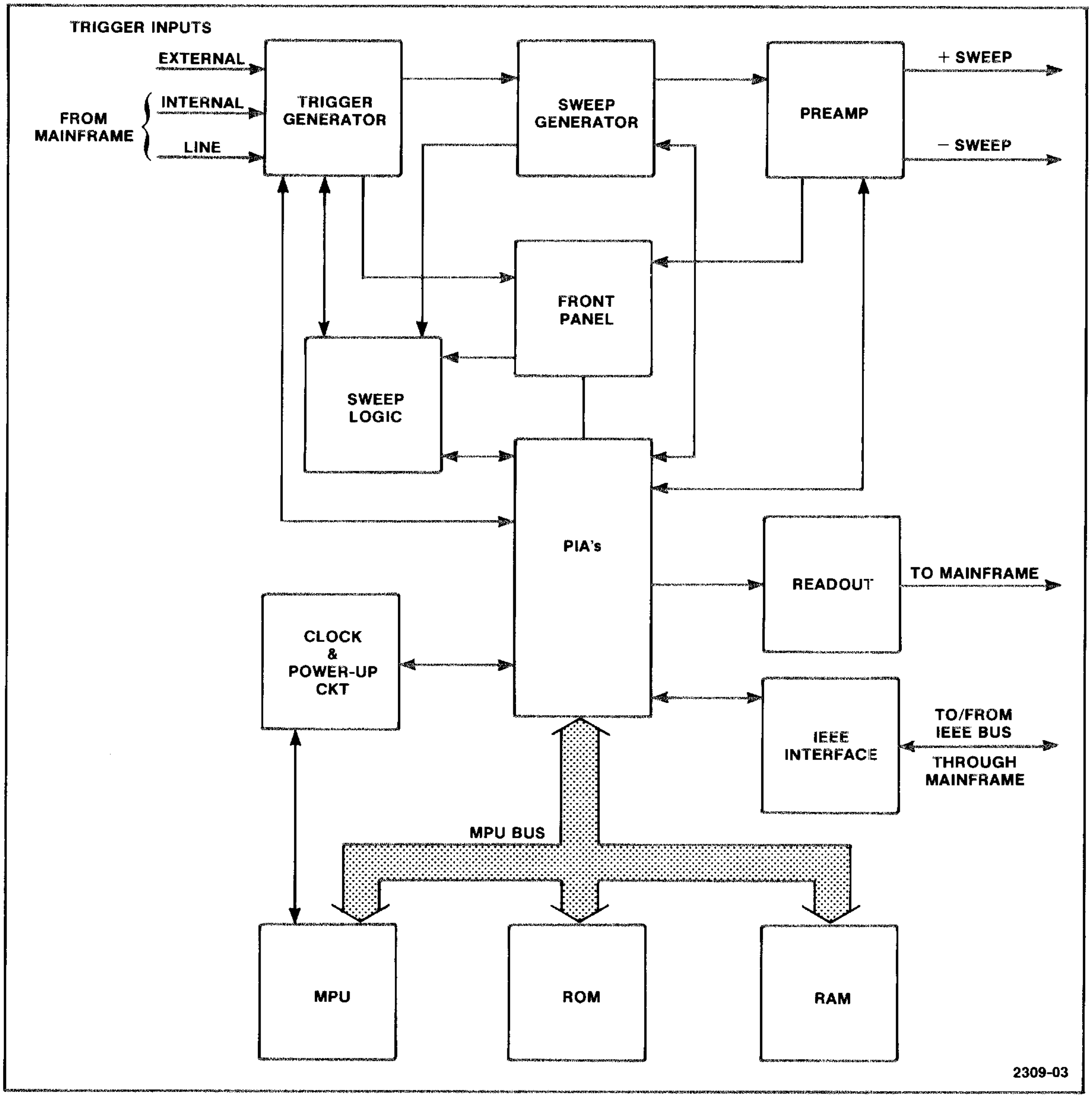

Fig. 5-1. 7B90P Block diagram.

called GPIB - General Purpose Interface Bus) interface controls the handshaking and communication on the IEEE 488 bus. The clock circuit generates the 2-phase clock signals required by the MPU. When power-up occurs, the power-up circuit initializes the MPU and PIA's and starts the clock circuit.

Sweep Generator

The sweep generator is divided into three main parts - the timing current source, the ramp generator and the auxiliary sweep preamp. Fig. 5-2 shows a block diagram of the sweep generator.

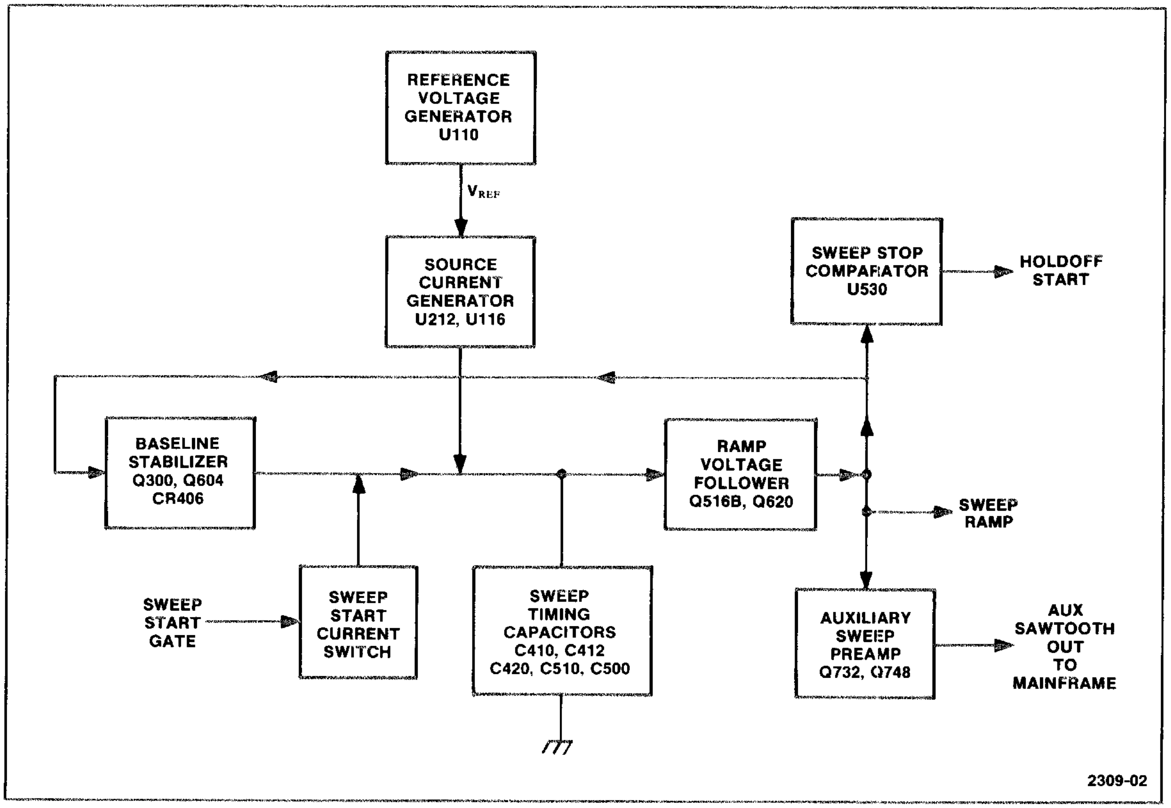

Fig. 5-2. Sweep generator block diagram.

Timing Current Source. The timing current source generates a precise source current for the ramp generator. The amount of current is controlled by signals from the microprocessor. The reference voltage generator and the source current generator comprise the timing current source (see Fig. 5-2).

U110 (top-center of schematic 2) generates a reference voltage for the source current generator that is selectable in 0.5, 1, 2 volt steps. U110E and R103 set the reference voltage for the base of all the transistors in the package. These transistors are well matched, so their base-to-emitter voltages and emitter currents are essentially equal. Twice as much current flows through R102 and the pair of U110A and B, but the current divides equally between U110A and B. As a result, the current through each individual transistor is the same as the other transistors in the package, providing good temperature tracking and current matching. DS001 and DS008 are current-steering diodes that allow control lines ST1 and ST2 (Sweep Timing 1 and 2) to switch the current through U110C and U110A and B. For example, when ST1 is high, DS001 is on and the emitter of U110C goes to about +3.8 volts. This reverse biases the transistor and cuts off its collector current. If ST1 is low, DS001 is off and U110C is on. LED's (Light-Emitting Diodes) are used as current steering diodes because they have a forward bias voltage drop of about 1.2 volts, providing a higher threshold voltage for ST1 and ST2.

The sum of the currents through all the forward biased transistors in U110 flows through R104, R105 and R312. (R312 is located at the bottom-center of schematic 5.) R312 sets the level of current through R105, allowing precise calibration of the timing current and as a result, the sweep speed. The current through these resistors produces a reference voltage at the collectors of U110 that is proportional to the sum of the currents through U110. This voltage is fed to the non-inverting (+) terminal of U116.

U212, U116 and the associated components (left-center of schematic 2) comprise the source current generator. This circuit generates a precise current for the ramp generator. The amount of current is a function of the reference voltage from U110 and the decade range selected by sweep timing lines ST3 and ST4 from the microprocessor.

U212 is a dual four-channel analog multiplexer. ST3 and ST4 drive the A and B inputs through buffers U320D and U320E. These inputs are decoded to select one of the four analog inputs (0,1,2,3). Current is supplied to the analog inputs through the decade resistors, R200, R202, R203 and R108. The values of these resistors are selected to provide current to the analog inputs in decade steps (X1, X10, X100 and X1000). The selected analog input is connected to XCOM and YCOM outputs through separate analog switches in U212 (see Fig. 5-3). As a result, ST3 and ST4 select the level of current at the XCOM output.

The analog switches in U212 have some series resistance (R_{on}) when they are on that changes with temperature. Changes in the value of R_{on} would affect the current at XCOM, so the YCOM output drives a feedback amplifier, U116, that compensates for these changes. The non-inverting (+) terminal of U116 is at the reference voltage set by U110. Since U116 is

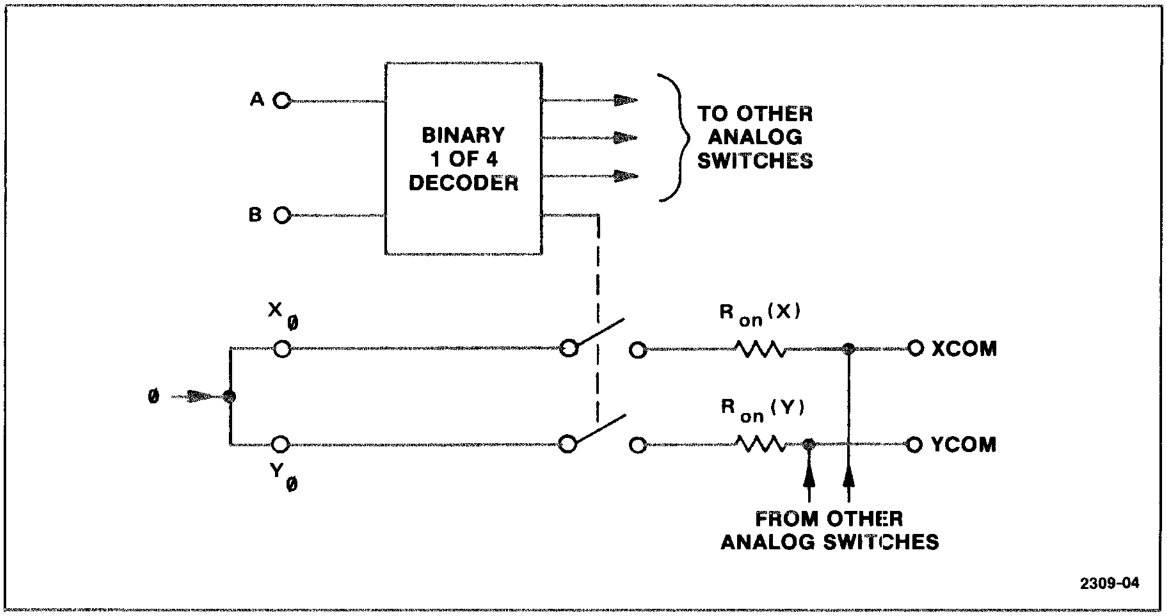

Fig. 5-3. Partial block diagram of the analog multiplexer, U212.

connected as a feedback amplifier, the inverting terminal will also be at this voltage (the feedback path for the amplifier is through the base-emitter junction of Q512, through U212 and back to the inverting terminal of U116). The input impedance of U116 is very high, so almost no current flows through R_{on}(Y) and the analog input terminal of U212 is at the reference voltage. The current into the analog inputs of U212 is set by the voltage drop across the selected decade resistor (R200, R202, R203 and R108). As a result, the current in the analog input and through XCOM is a function of the selected analog input to U212 and the reference voltage from U110, but is independant of changes in R_{on}.

The output timing current from the XCOM output of U212 flows through Q512 to the ramp generator. LR512 compensates for the base-to-emitter capacitance of Q512.

Ramp Generator. The ramp generator uses the constant current from the timing current source to charge capacitors, generating a linear ramp voltage. The sweep starts when the trigger circuit asserts GATE (We'll discuss the trigger circuit later). This turns Q400 on (bottom-center of schematic 2) and turns Q406 off, so CR406 becomes reverse-biased.

The sweep timing capacitors are selected by ST5, ST6 and ST7. These lines are buffered by U320A, U320B and U320C. The outputs of the buffers drive Q410, Q314, and Q312. When the slower sweep rates are selected (100ns/DIV and slower), these transistors switch C412, C314 or C410 in parallel with C500 and C510. The constant current charges the selected capacitors and produces a linear ramp voltage.

Q516B and Q620 at the right-center of schematic 2 form a voltage follower. When the ramp at the emitter of Q620 reaches +5 volts, the end-of-sweep comparator, U530, switches. R536 and R534 set the refernce voltage for the comparator. When the comparator switches, C530 couples the negative-going output pulse at pin 7 back to the A input to improve the switching time and provide hysteresis on the input. The positive-going output pulse on pin 5 of the comparator goes to the sweep logic and the GATE or AUTO SENSE line (depending on the trigger mode selected) goes to -15 volts. This turns Q400 off and Q406 on. Q406 sinks the timing current and discharges the timing capacitors.

If Q406 continued to sink current through the timing capacitors after they are discharged, the ramp voltage would drop below zero volts. The baseline stabilizer circuit prevents the voltage from falling below zero by sourcing current through CR406. Follow the line from the emitter of Q620 at the right-center of the schematic, back to the base of Q300A. When the ramp voltage falls to zero as the timing capacitors discharge, Q300A turns on the current through Q300B decreases. The base of Q604 goes to zero volts and its emitter current decreases. CR406 becomes forward-biased and current flows through the diode and Q406. The current through CR406 keeps the baseline of the ramp from dropping below zero volts while the sweep is off. The baseline is held stable at zero volts until the next sweep starts.

Auxiliary Sweep Preamp. The sweep signal from the voltage follower also drives the auxiliary sweep preamp formed by CR732, Q732 and Q748. The differential stage of CR732 and Q732 provides a high voltage-gain while Q748 drives the output. R746 provides negative feedback to set the stage gain. The non-inverting input to the amplifer at the anode of CR732 is grounded to provide a reference. The output of the amplifier drives the ramp output that is available on some mainframes.

Power Supplies. The circuitry in the upper right corner of schematic 2 distributes, filters and decouples the power supplies from the mainframe. A 5-volt, three-terminal regulator, U020, generates the -5 volt supply required by the holdoff and trigger circuits and some of the logic circuits.

Horizontal Preamplifier

The horizontal preamplifier is shown on schematic 4. This circuit takes the sweep signal from the ramp generator, converts it to a differential drive signal and adds DC positioning current. The circuit is divided into four main parts -- the input differential amplifier, the current follower, the output amplifier and the positioning circuit.

Input Differential Amplifier. The input differential amplifier consists of two differential amplifiers - one for X1 operation (MAG off) and one for X10 MAG operation. Q320, Q220, Q324 and the associated components comprise a constant-current switching circuit. When MAG is off, $\overline{\text{MAG}}$ (center of schematic 4) is high and Q320 is off. Q220 is off and Q324 is on, supplying current to Q224 and Q236 (see Fig. 5-4a). The sweep signal from the ramp genertor drives the base of Q224. DC positioning current is fed to the base of Q236. R236, R237 and R330 set the stage gain. The differential output signal from the collectors of Q226 and Q324 drive the emitters of Q120 and Q242 in a cascode configuration. Since Q220 is off, Q222 and Q234 are also off.

When MAG is on, $\overline{\text{MAG}}$ is asserted (low), so Q320 and Q220 are on and Q324 is off. Current is supplied through Q220 to the X10 MAG amplifier, Q222 and Q234 (see Fig. 5-4b). Since Q324 is off, Q224 and Q236 are also off. R228, R234, R235 and R232 set the gain of the stage. R232 allows the gain to be matched to ten times the X1 gain. R233 and C233 increase the gain of the circuit when the ramp starts at high sweep rates to improve linearity. The differential output signal is fed to Q120 and Q242.

Current Follower. Q120 and Q242 form a differential common-base current follower. This circuit improves the thermal stability and high-frequency characteristics of the input differential amplifiers by holding the base-to-collector voltage of the amplifier transistors near zero volts. To see how this circuit works, let's follow the ramp signal through the X10 input amplifer and current follower (The X1 circuit is identical).

Assume that we are at the beginning of a sweep ramp, so the input voltage is zero. The current through R221 forward biases CR222. The base of Q222 is at zero volts and the base of Q120 is one diode-drop (about 0.6 volts) below the base of Q222. The base-emitter junction of Q120 produces about the same voltage drop, so its emitter is at zero volts. R128 decouples the base-to-collector capacitance of Q222. Since R128 has a low value, it drops very little voltage. As a result, the collector of Q222 is very near

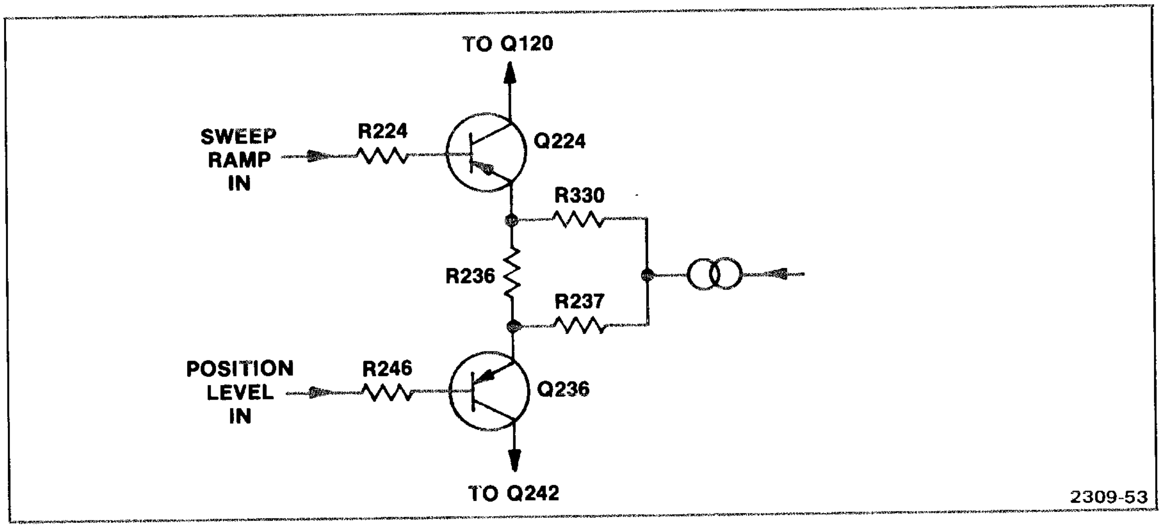

Fig. 5-4a. Simplified schematic of the X1 horizontal preamplifier.

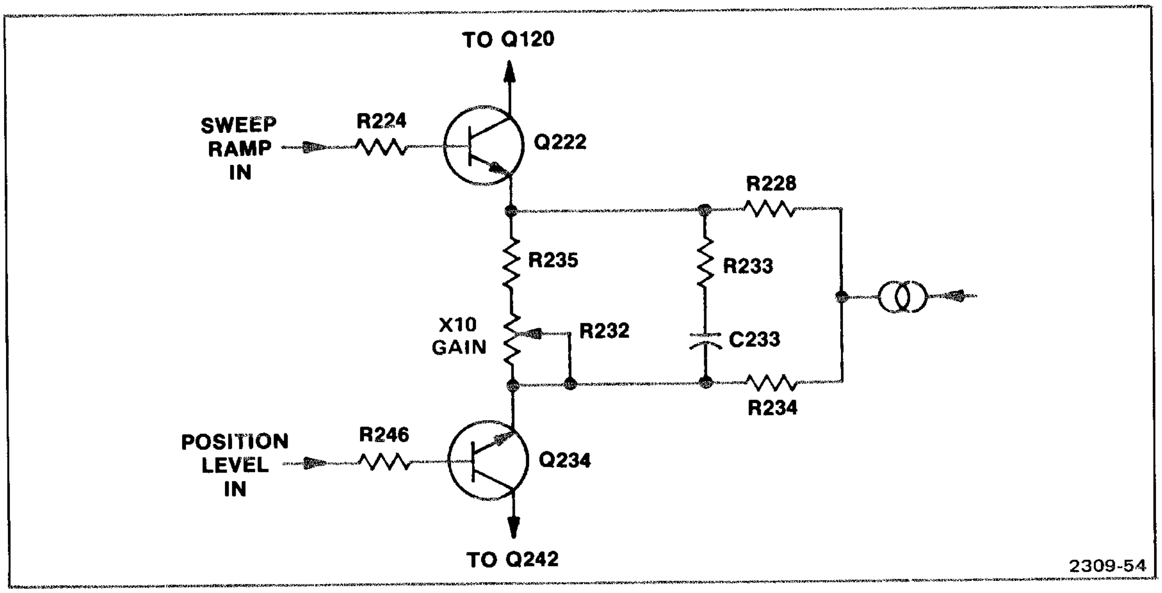

Fig. 5-4b. Simplified schematic of the X10 horizontal preamplifier.

zero volts and its base-to-collector voltage is very low. The low voltage drop causes the device to dissipate very little power, providing good thermal stability. The low base-to-collector voltage also minimizes the effects of the junction capacity.

R220 and C220 improve the high frequency linearity of the circuit.

Output Amplifier. The output amplifier provides a differential drive of 50 millivolts per division (into 50 ohms) to the mainframe and provides a 2X magnification for the 500 picoseconds/division sweep speed. The output of the current follower drives the bases of Q130 and Q132. The network of R122, R238 and R241 provides DC balance for the amplifer.

When the 500 picoseconds/division sweep speed is selected, STOA goes high and Q142 and Q146 saturate. The current through Q146 raises the gate voltage of Q134, forward biasing the gate-to-drain and gate-to-source junctions. This shunts R124 and R133 with a low impedance, changing the emitter current in Q130 and Q132 and doubling the gain of the amplifier. R240 adjusts the 500 picosecond sweep speed by setting the current through Q146 and Q134 which changes the emitter current in Q130 and Q132. When Q134 is off no current flows in the FET (Field-Effect Transistor) so R124 and R133 set the stage gain. CR138 protects the base-emitter junction of Q146 against reverse breakdown when Q142 and Q146 are off.

Positioning Circuit. The DC positioning current comes from the 10-bit Digital-to-Analog Converter (DAC), U330, in the upper-left corner of schematic 4. The output current of the DAC is proporational* to the value of the 10-bit input word. The value of this word can be set from the front panel POSITION control or under program control. We'll discuss the circuit that sets the value of the word in more detail in the MPU Control Example section of this circuit description. R342 sets the gain of the DAC and the output of the DAC drives U340. the gain of this amplifier is set by R343 and R344. When the 2X magnifier is off (500 picoseconds/division not selected), STO is low and the analog switch is in the position shown on the schematic. When the TIME/DIV is set for 500 picoseconds/division, STO goes high and the switch closes, shunting R344 and decreasing the amplifier gain. This causes the POSITION control to have the same resolution at 500 picoseconds/division as it does in other TIME/DIV settings.

When the 2X magnifier is on at 500 ps/DIV, the sweep positioning is shifted to correct for positioning offsets in the instrument. When STO is asserted as just discussed, U430E (bottom-left of schematic 4) is off (switch open). This shifts the positioning by connecting R446 in series with R644.

Trigger Generator

The trigger generator (schematic 1) provides for a stable display by starting the sweep generator at a selected point on the input waveform. The trigger point can be set with the ±SLOPE and LEVEL controls, or with the equivalent commands under program control. The triggering source can be selected from the signal being displayed, a sample of the line voltage, or an external signal applied to the EXT TRIG IN connector. Fig. 5-5 shows a block diagram of the trigger generator.

Line Source. When LINE triggering is selected, LT (at the left edge of schematic 1) is asserted. U410A switches, connecting the LINE input (pin 1) to pin 15. A sample of the line voltage from the mainframe is fed through the analog switch (U410A) to pin 2 of the trigger source selector and amplifer (part of U220). If LINE triggering is not selected, LT is low, so pins 2 and 15 of U410A are connected together, applying -2.5 volts to the LINE input (pin 2) through R414 and R410. This voltage reverse-biases the input transistor in U220, disabling the LINE input.

Internal Source. A differential copy of the displayed signal from the mainframe is fed to the INTernal trigger inputs (upper-left corner of schematic 1). This signal is split into two paths. Frequencies above about 16 KHz are coupled through C220 and R214 to U220. The low frequency path is through U112A, U350 and U358 to U220. The high and low frequency signal components are recombined in U220 to reproduce the original trigger signal.

When INTernal triggering is selected, $\overline{\text{IT}}$ goes high and U410B opens. Frequencies above 16 KHz are coupled through C220 to the INTernal input of U220. R214 and C220 set the roll-off characteristics of the high frequency path. R213, R212 and R214 set the input impedance of this line to about 50 ohms. If internal triggering is not selected, U410B closes, connecting the -5 volt supply to pin 12. R320 and R214 divide the supply voltage down and apply -2.5 volts to the INT input of U220, disabling the input.

The differential internal trigger signal also drives U112A. Low frequencies (below about 16 KHz) are amplified by U112A and passed to analog switches, U310B and U310C. R120, C110, R114 and C114 set the roll-off characteristics of U112A. If DC coupling is selected, $\overline{\text{DCI}}$ goes low and U310B closes, bypassing C312. When AC coupling is selected, $\overline{\text{DCI}}$ goes high, and $\overline{\text{ACI}}$ is asserted, closing U310C. This connects C312 in series with the low frequency path. In either case, the output signal is fed to pin 2 of U350 (upper-right of schematic 1).

U350, R350 and R218 form an inverting buffer. U358 mixes the internal signal from U350 and the external signal. The amplifier provides a gain of 2 from the non-inverting terminal (EXTernal signal) and unity gain from the inverting terminal (INTernal signal) to the output. Since only one of these signals is fed to the inputs of U358 at any time, the output has the

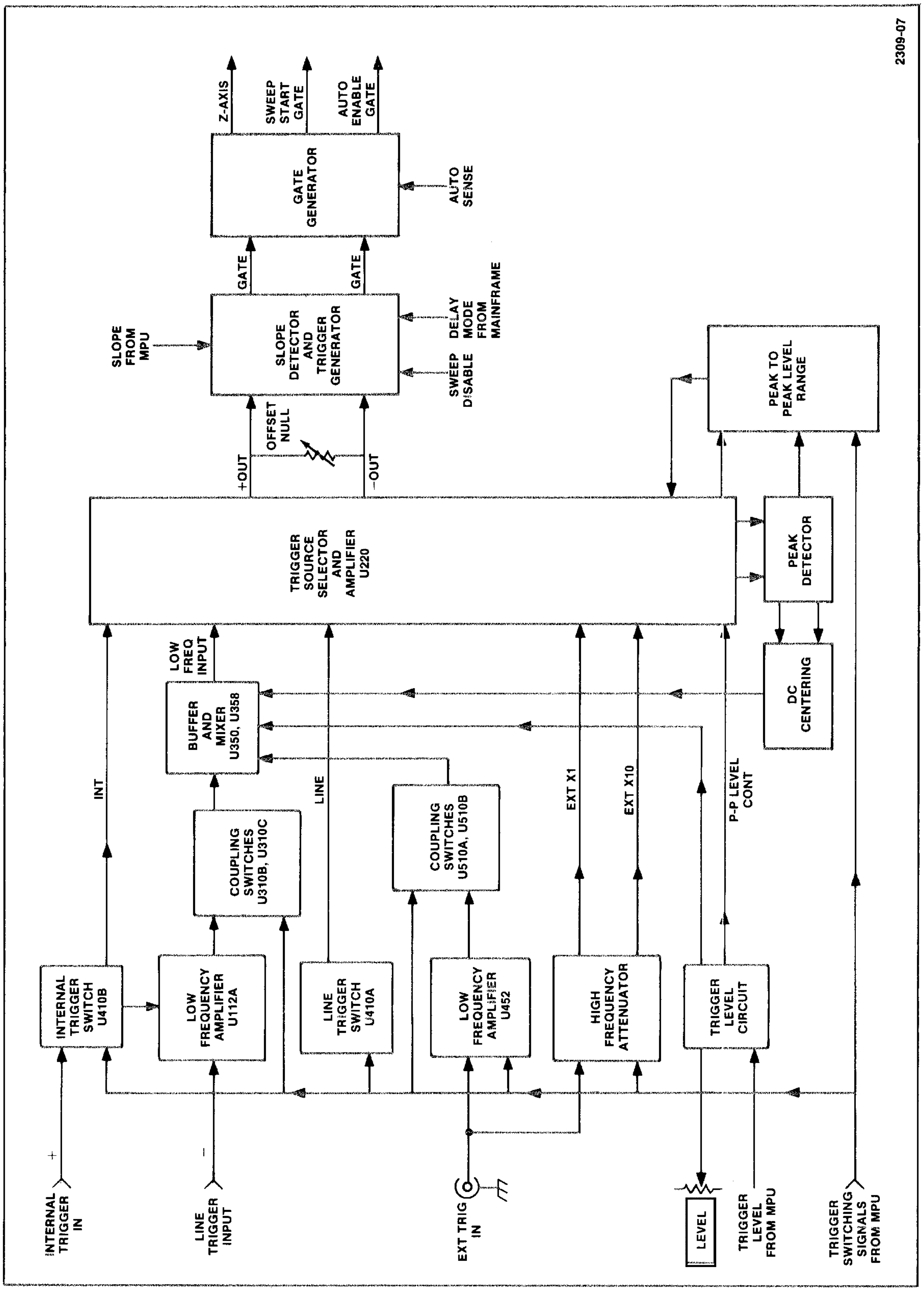

Fig. 5-5. Block diagram of the trigger generator.

low frequency components of the selected trigger signal. The output of this amplifier drives the LOW FREQ INPUT of U220. R116 keeps the offset voltage low by matching the input impedances on U220. C116 and R128 improve the circuit's stability. R134 provides for balancing the trigger internal source low frequency path in NORMal mode.

External Source. The external trigger signal is fed to J001, the EXT TRIG INput on the front panel. When the TERMination switch (S001) is out, R414 and R410 provide 50-ohm termination for the line. C412, E412 (Ferrite Bead Inductor) and R412 keep the VSWR (Voltage Standing-Wave Ratio) on the input low. L412 compensates for the input capacitance to improve VSWR. If 1 megohm input impedance is selected (TERMination pressed in), S001 is open and R400 sets the input impedance. C412, C402, C436, C440 and the stray and cable capacitance comprise the 20 picofarad input capacitance.

The external trigger signal is split into two paths, as we discussed for the internal source. Frequencies below 16 KHz are coupled through R400 to the input amplifier, U452. CR464 and CR466 protect the input of U452 from overdrive. When EXT (X1) triggering is selected $\overline{\text{ET10}}$ (bottom-left corner of schematic 1) is high and U510C is open. In this mode R448 and C448 comprise the feedback for the amplifier. If EXT X10 triggering is selected, $\overline{\text{ET10}}$ goes low and U510C closes. R550 and C540 are connected in parallel with R448 and C448, reducing the gain of the stage by a factor of ten. C448 and C540 set the frequency response of the stage.

The output of the amplifier is fed to the coupling switches (U510D, U510A and U510B). U510D opens the low frequency external trigger path when LINE or INTernal triggering is selected. U510A and B are open when AC LF REJ COUPLING is selected with EXTernal and INTernal source. When EXTernal and DC coupling are selected, $\overline{\text{DCE}}$ is asserted, closing U510A and bypassing C422. $\overline{\text{ACE}}$ goes low and $\overline{\text{DCE}}$ goes high for AC coupling, connecting C422 in series with the signal path. C422 and R454 set the input's AC coupling bandpass. The output of the coupling switches drives the non-inverting input of the mixer stage (U358). The output of the stage drives the LOW FREQuency INPUT of U220 as previously discussed.

Now refer to the left-center of schematic 1. The high frequency components of the external trigger signal pass through C402 and drive the high-frequency divider. C402, C436 and C440 form a capacitive divider that reduces the effects of cable capacitance and divides the signal down for the X1 and X10 EXTernal trigger modes. As a result, the signal at the gate of the top FET (Field-Effect Transistor), Q327, is ten times as large as the signal at the gate of Q440. R434 and C436 set the roll-off characteristics of the X1 attenuator input signal. R444 and C440 perform the same function for the X10 divider. R436 and R442 prevent ringing in the divider.

Signals from the microprocessor control the divider. When EXTernal (X1) triggering is selected, $\overline{\mathrm{ET1}}$ goes low and Q530 saturates. R536 and R537 set the bias level for Q530. R522 and R524 set the current when the transistor is on and provide for DC offset correction for the EXT X1 circuit. C424 and R424 decouple the AC signal from the control logic signals. When Q530 saturates, its collector voltage rises, biasing, the source follower, Q327, into its active region. C422 keeps the DC from the capacitive divider. At high frequencies Q327 begins to rectify the signal and produces a DC offset voltage, so R420 and C326 feed a portion of the signal around the FET to compensate for this effect. Q326 supplies a constant current to the source follower for good thermal stability.

The output of this source follower drives the EXT X1 input of U220. The EXT X1 input and the LOW FREQ INPUT form a differential input pair. The impedance of these inputs must be equal to minimize the offset voltages, so the on resistance of Q326 (about 90 ohms) in series with R324 matches the 1K-ohm impedance on the LOW FREQ INPUT. CR334 and CR342 limit the positive polarity signal amplitude. CR336, DS348 and the associated components limit the negative polarity DC level and the AC amplitude. When the EXT X1 trigger mode is unselected, Q327 is biased off and the output goes to about -2 volts, reverse biasing the EXT X1 input of U220.

The EXT X10 control circuit is identical to the EXT X1 circuit.

Trigger Level Circuit. The trigger level is adjusted by adding a DC level to the LOW FREQ INPUT of U220. The DC level comes from an 8-bit DAC (U106), similar to the one used in the positioning circuit. The output current of the DAC is proportional to the value of the 8-bit input word. The input word can be set from the front panel LEVEL control or under program control. We'll discuss the operation of the circuit in more detail in the MPU Control Example section. U112B and R103 convert the output current of the DAC to a voltage level for the input of U220.

Trigger Source Selector and Amplifier. We have discussed U220 only briefly. Now refer to schematic 1 and the block diagram in Fig 5-6 as we discuss the function of U220 in more detail. The five high-frequency inputs go to the input switching circuit (four of the inputs are used). Unused or disabled inputs are tied to -2.5 volts, reverse biasing the corresponding input transistor. The output of the switching circuit drives the left amplifier of the pair near the center of the block diagram. The LOW FREQuency INPUT also drives the amplifiers. The low- and high-frequency components are recombined in the amplifier and fed to the variable attenuator through the summing junction.

When High Frequency Reject (HF REJ) is selected the $\overline{\text{HFR}}$ control line at the right edge of schematic 1 goes low, reverse-biasing Q128. The HF REJect Select and Biasing circuit at the top of Fig. 5-6 enables the right amplifier of the pair and the high-frequency signals are fed to its non-inverting terminal. C137 sets the roll-off characteristics of the amplifier to reject high frequencies. The output of the amplifier goes through the summing junction to the variable attenuator. In all modes except PP AUTO (Peak-to-Peak Auto), this attenuator is set for X1 attenuation (We'll discuss PP Auto Mode later).

Peak-to-Peak Auto Circuit. U220 also contains the Peak-to-Peak Auto and AGC circuits. The Peak-to-Peak Auto function can be divided into three major blocks. First, the peak detector determines the signal size and DC positioning. Second, a DC centering loop centers the peak-detected output regardless of the DC input and offset voltages. Third, the peak-to-peak level range output voltage is automatically adjusted until the trigger output reaches the clamp level set by the automatic gain control (AGC) to achieve full level range. The peak detector outputs, pin 14 and 15 of U220 (bottom-right of schematic 1), provide a differential rectified copy of the input trigger signal. C146 and C148 filter this output signal. U150B, CR140, U150A and CR050 form a second rectifier and filter stage. We'll discuss U150B and CR140 as an example. The other circuit is identical.

On the positive slope of the signal, the output of U150B follows the input in the positive direction, forward biasing CR140 and charging C140. Since the non-inverting terminal is tied to the anode of CR140, the output voltage follows the PEAK DET OUT signal very closely, without the forward-bias voltage drop of CR140. When the signal begins to go negative, CR140 is reverse-biased and the feedback path for U150B is opened. As a result, the output of the amplifier goes low (about +1 volts) very quickly. C152 slows the transition down to suppress noise. C140 remains charged at the peak output level because it's discharge path is very high impedance. The output of this stage drives the DC centering circuit and the peak-to-peak level range stage.

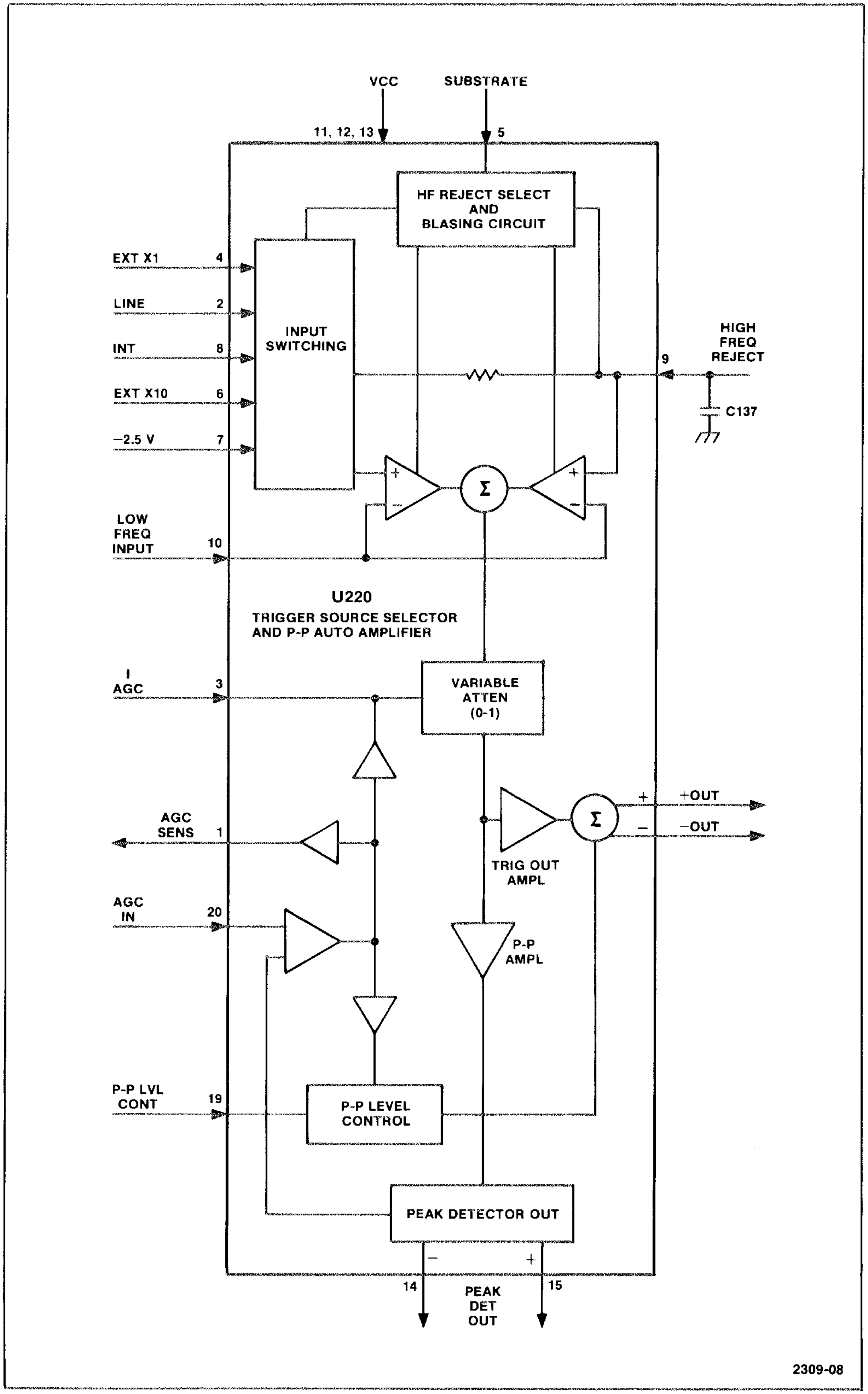

Fig. 5-6. Block diagram of U220.

Operational amplifier U030B adjusts the DC level of the LOW FREQ INPUT of U220 by adding a DC level to the signal. When PP AUTO mode is selected, PPA is asserted, closing U310D and applying the level at the output of U030B to the LOW FREQ INPUT. This level nulls the DC input voltage and any accumulated DC offsets, allowing the trigger outputs at pins 16 and 17 of U220 to balance when the triggering LEVEL is set to zero. DC balance adjustment R243 provides centering for offset voltages resulting from circuitry external to U220 (e.g., U240).

The peak-to-peak level range amplifies the peak detector DC level to provide constant-amplitude trigger signals and to determine the range of the front panel LEVEL control and LEVEL program command.

The peak detector output level is coupled to pin 3 of U030 through R044 and R052. The gain of this feedback amplifier (consisting of U030A and AGC section of U220) increases as the peak detector output decreases. As a result, the trigger output signal level at pins 16 and 17 of U220 is constant.

The range of the front panel LEVEL control and the LEVEL program control is zero at minimum triggering signal amplitude. The range increases as the triggering signal amplitude increases, until the maximum range is reached at the AGC threshold. Q134 is used as a switch. When $\overline{\text{PPA}}$ is high (unasserted) Q134 is off, and the peak-to-peak level range circuit is disabled.

The automatic gain control (AGC) stage limits the trigger signal amplitude to approximately 450 millivolts peak-to-peak (at pins 16 and 17 of U220) regardless of the trigger input signal amplitude. Current into the I AGC input (pin 3) of U220 sets the AGC threshold.

Slope Selector and Trigger Generator. U240 converts the differential trigger signal from the outputs of U220 to a differential gate waveform for use by the gate generator stage. The +SLOPE button (or the SLO command under program control) determines whether the display is triggered on the positive-going or negative-going slope. When the SLOPE is set for positive (+SLOPE button lit or SLO POS set under program control), TL8 goes low. A positive-going signal on pin 13 of U240 produces a differential output pulse on GATE and $\overline{\text{GATE}}$. If the SLOPE is set for negative, TL8 is high and a negative-going signal on pin 13 produces a differential GATE pulse. The +/- SLOPE BALance adjustment provides optimum balance between the +SLOPE and -SLOPE modes.

The delay mode control signal into U240 (pin 16) is used only when the unit is operating as a delayed sweep unit in the B Horizontal compartment of a mainframe with two horizontal compartments. When the 7B90P is operating in the B starts after delay mode (as determined by the delaying-sweep time base in the A horizontal compartment), a high on DELAY MODE (pin 16 of U240) forces a GATE pulse, unless SWEEP DISABLE is asserted.

At the end of each sweep, the sweep logic generates a SWEEP DISABLE pulse. The high on SWEEP DISABLE (pins 6 and 10 of U240) disables the trigger generator long enough to allow the sweep generator to retrace and stabilize before another pulse starts the next sweep.

Gate Generator. The gate generator (bottom-left of schematic 2) provides an AUTO ENABLE GATE to the sweep logic and a SWEEP START GATE and Z AXIS to the sweep generator.

When U240 (right-center of schematic 1) asserts GATE and $\overline{\text{GATE}}$, Q260 turns off and Q262 turns on. The current through Q262 causes SWEEP START GATE to go high, starting the sweep ramp. Q266 and the associated components speed up the transitions on $\overline{\text{GATE}}$ and drive the AUTO ENABLE GATE. At the end of the sweep, GATE goes low and Q262 turns off, ending the sweep ramp as previously discussed. If the time base is in PP AUTO mode and no trigger is received, AUTO SENSE goes high to initiate a sweep. The high on AUTO SENSE turns Q264 on, asserting SWEEP START GATE.

Sweep Logic

The sweep logic (schematic 3) controls the sweep modes and the associated time base functions. The logic also generates control signals for the mainframe. Fig 5-7 shows the block diagram of the sweep logic.

PP Auto Mode. The PP Auto mode provides a free-running trace in the absence of a trigger signal. Since there is no trigger, GATE (bottom-left of schematic 2) and AUTO ENABLE GATE are low. $\overline{\text{PPA}}$, pin 19 of U448 (top-center of schematic 3) is asserted. The low on $\overline{\text{PPA}}$ tells U448 that the time base is in AUTO mode. AUTO SENSE goes low and turns Q264 on (bottom-left of schematic 2). This generates a SWEEP START GATE, initiating a sweep. At the end of the sweep, the end-of-sweep comparator switches, pulsing HO START (Hold-Off Start - pin 16 of U448). AUTO SENSE and SWEEP DISABLE go high and stay high until the hold-off circuit times out (we will discuss the hold-off circuit in the MPU control example section.) If no trigger

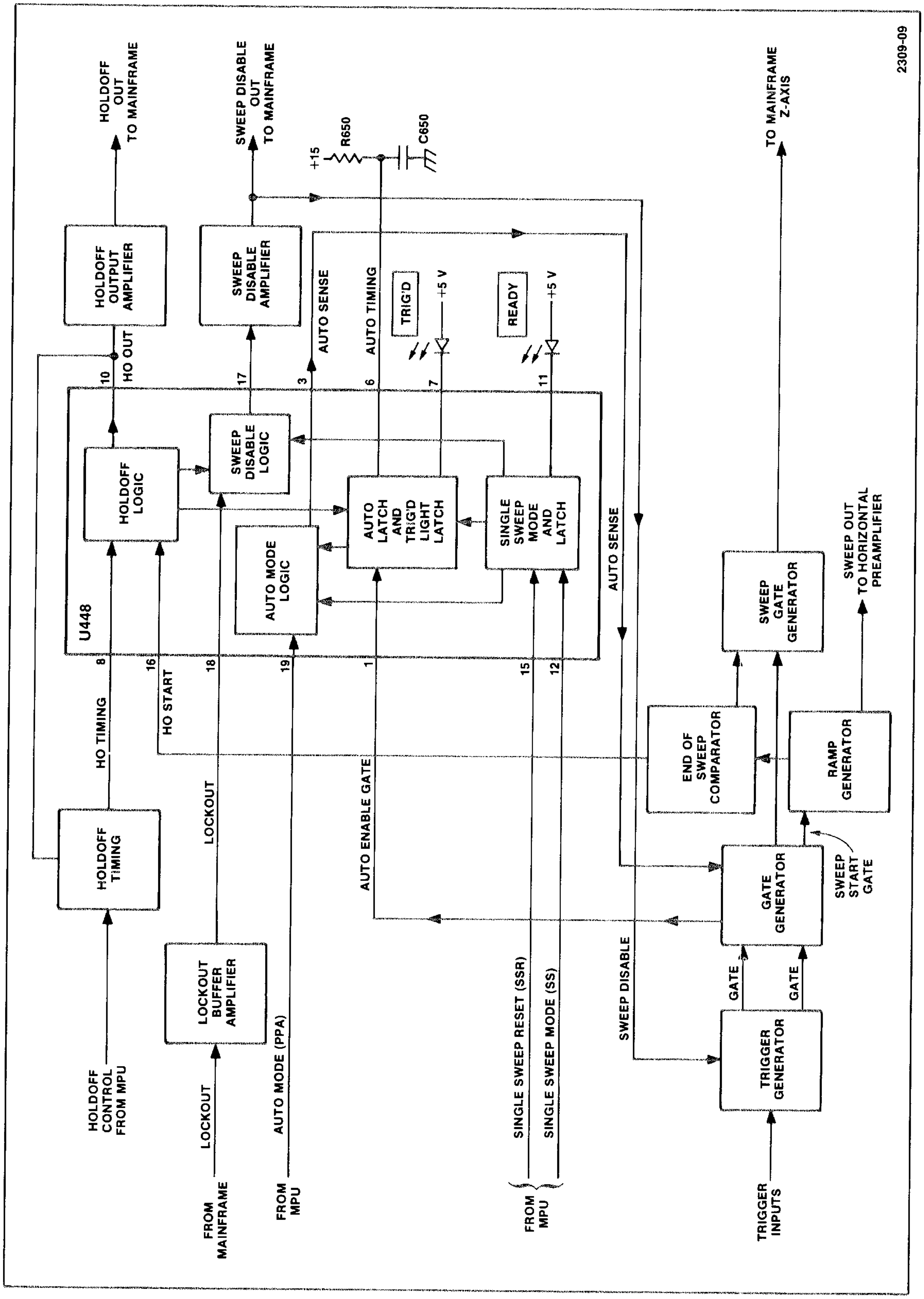

Fig. 5-7. Sweep logic block diagram.

is received, AUTO SENSE goes low after the hold-off time and the process is repeated.

If a trigger is received, the time base functions as if it were in NORMal mode except that the trigger point can be set at any point between 10% and 90% of the peak-to-peak amplitude of the trigger signal. Pin 7 of U448 goes low and the TRIG'D (Triggered) Light comes on. R650 and C650 keep the trace from free-running between triggers by providing a delay. AUTO TIMING, pin 6 of U448, goes low with each trigger pulse. After the pulse, C650 begins charging through R650. If no triggers are received within about 63 milliseconds, the sweep AUTO TIMING goes high and the sweep begins to free-run.

Normal Mode. When NORMal mode is selected, a sweep is initiated only on a valid trigger. In this mode, SS (Single Sweep-pin 12 of U44) is low and AUTO MODE, pin 19, is unasserted (high). When a trigger is received, GATE goes high to initiate a sweep and the TRIG'D light comes on. At the end of the sweep, HO START is asserted and SWEEP DISABLE goes high, disabling the trigger generator. When the hold-off circuit times out, SWEEP DISABLE goes low and the next valid trigger repeats the process.

Single Sweep Mode. When single sweep is selected, SS (pin 12 of U448) is high. If no trigger is received, GATE is low and the READY light is on. When a valid trigger is received, AUTO ENABLE GATE goes high, the TRIG'D (Triggered) light comes on and the sweep starts. At the end of the sweep, HO START is pulsed high, resetting the single-sweep latch in U448 and the READY light goes out. SWEEP DISABLE goes high and stays high until the single sweep latch is reset. When the hold-off circuit times out, the TRIG'D light goes out.

If RESET is pressed or the plug-in receives a SSW ARM command on the IEEE 488 bus, $\overline{\text{SSR}}$ goes low (the single sweep may also be reset by a control line from some mainframes). The low on pin 15 of U448 initiates an internal pulse that resets the single sweep latch. C448 sets the width of this pulse. The SWEEP DISABLE line goes low and the READY light comes on. The time-base waits for the next valid trigger and repeats the process.

Holdoff Circuit. The hold-off circuit disables the sweep to allow the ramp generator to retrace and stabilize for the next sweep. Since larger timing capacitors are used for the slower sweep speeds, the discharge (retrace) time is longer, so the hold-off time must also be longer. U630, at the bottom-left of schematic 3, decodes ST4, ST6 and ST7 and switches timing capacitors into the hold-off timing circuit to change the hold-off time as the sweep speed changes.

When HO START (pin 16 of U448) is pulsed, HO OUT (Hold-Off Output) goes high, turning Q252 on. Q250 drives the mainframe HOLDOFF control line. The collector of Q252 goes low, turning Q740 on and Q648 off. A constant current, generated by Q646 and the associated components, charges the selected holdoff timing capacitors. When the voltage on the capacitors exceeds the reference voltage from U654, the hold-off comparator U644 switches and HO TIMING goes high, terminating the hold-off cycle.

The reference voltage is set by a 6-bit DAC that is similar to the one used in the positioning and trigger level circuits. The value of the input word can be set from the front-panel HOLD OFF control or under program control. This allows the hold-off time to be varied within a fixed range, determined by the sweep speed setting. U654 converts the DAC output current to a reference voltage for the hold-off comparator.

NOTE

Some mainframes disable the holdoff circuit to generate a display graticule.

Lockout Buffer Amplifier. The SWEEP LOCKOUT allows the sweep to be disabled for special mainframe functions or when the 7B90P is operated as a delayed time base in a mainframe with two time-base compartments.

Q552 and Q546 form a differential amplifier that provides good thermal stability for the lockout circuit. When SWEEP LOCKOUT is asserted, Q552 is biased off and CR550 turns on, clamping the base of Q544 to about +0.7 volts. Q544 turns off and its collector goes high. The positive pulse turns Q558 on for a time set by R554, R556 and C544. The low on the collector of Q558 initiates a hold-off sequence, stopping the sweep and inhibiting triggers. At the same time, the high on LO IN (LockOut INput) disables the sweep logic until the SWEEP LOCKOUT line is released.

Microprocessor System

We mentioned in the block diagram discussion that the 7B90P is controlled by a microprocessor system in the plug-in. The major components of the system are shown on schematic 6. Full information on the components that comprise the system is given in the Motorola M6800 Microcomputer System Design Data Manual. It will be helpful to have a copy of this manual for reference as you go through the description.

MPU and Memory. The Motorola M6800 (U920) is an 8-bit Microprocessing Unit (MPU). The MPU has a 16-bit address bus (13 bits are used in this system) that allows it to selectively communicate with the memory and PIA's. A separate 8-bit bi-directional bus carries data to and from the MPU.

If an external device asserts the MPU's $\overline{\text{IRQ}}$ (Interrupt ReQuest) or $\overline{\text{NMI}}$ (Non-Maskable Interrupt) inputs, the normal program execution is interrupted. The processor saves its current status, then determines what caused the interrupt and executes an appropriate service routine. These service routines include such tasks as scanning the front panel buttons or getting a byte from the IEEE 488 bus. While servicing the interrupt, the processor can mask its IRQ input so that further interrupts will not be recognized until the current interrupt has been serviced. The $\overline{\text{NMI}}$ input cannot be masked. We'll discuss the interrupt sequence in more detail later.

The program that controls the MPU's activity resides in two 2048 x 8-bit ROM's (U830 and U1030). The ROM's are accessed by asserting an address in the range 7000_{16}-$7FFF_{16}$. The MPU also uses a 128 x 8-bit RAM (U1130) as a "scratch pad" memory. The RAM occupies addresses from 0 to $7F_{16}$.

PIA's. The processor communicates with other parts of the plug-in and the IEEE 488 bus through five M6820 PIA's (U510, U710, U810, U1110, and U1420). Complete information on these chips is contained in the M6800 Microcomputer System Design Data Manual. We'll discuss only the relevant details here.

Figure 5-8 shows a block diagram of the M6820. Each PIA contains two separate Input/Output (I/O) ports and control registers. Each line of the I/O ports can be programmed as an input or output by setting bits in the data direction registers.

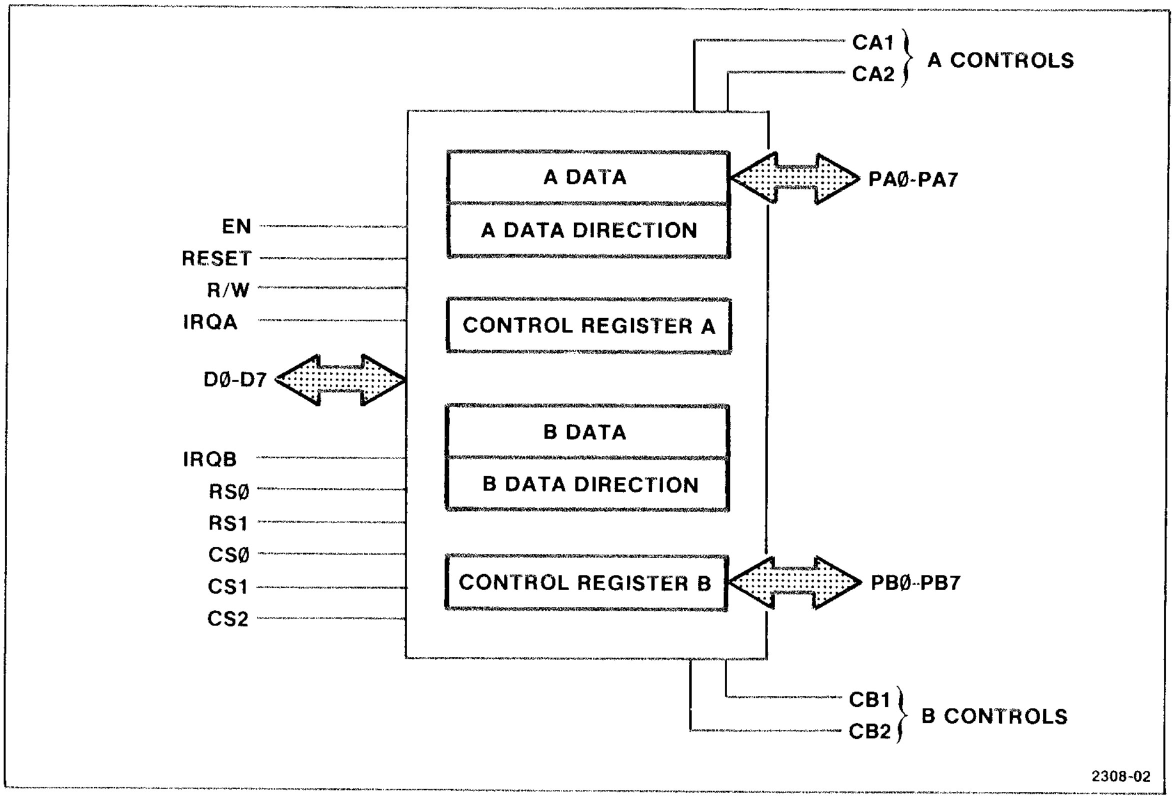

Fig. 5-8. Block diagram of the M6820 PIA.

Two interrupt outputs ($\overline{IRQA}$ and $\overline{IRQB}$) signal the processor that the PIA has data or needs service. When an interrupt occurs, a flag is also set in the appropriate control register. Since the interrupt lines are OR-tied to the MPU's $\overline{IRQ}$ input, the processor must read each PIA's control registers to determine which one generated the interrupt.

Power-up Circuit. When power is applied to the plug-in, the power-up circuit monitors the power supplies and generates initialize signals for the MPU, clock circuit, and PIA's. The power-up circuit is located in the bottom-center of schematic 7.

Comparators U430A, U430B and U430C monitor the power supplies. The outputs of the comparators are OR-tied so that all the supplies must be present before the outputs go high. When they do, C528 begins charging through R430 and R530. When the voltage at the top of R530 reaches about 4.1 volts (about 2 milliseconds after the comparator outputs go high), U430D switches and its output goes low. As a result, POR (Power-On Reset) and the input of U530B go low. The output of U530B and $\overline{POR}$ go high. The POR and $\overline{POR}$ lines initialize the PIA's and assert the TSC (Three-State

Control) input on the MPU (Refer to the M6800 manual for more information on this input).

U1630B and U310B form an R-S flip-flop that controls the clock circuit. Since the output of U530B stays low for 2 milliseconds after the power supplies are stable, this flip-flop powers-up with the output of U310B high. The flip flop will stay in this state until $\overline{\text{STOP}}$ is asserted. We'll discuss the $\overline{\text{STOP}}$ line later.

Since pin 8 of U310B is high, when the output of U530B goes high, the output of U010A also goes high. The low-to-high transition fires U1530A and the Q output goes low for about 13 microseconds. Pin 8 of U010C is high so $\overline{\text{MPURES}}$ (MPU RESet) is asserted until U1530A times out. This negative-going pulse forces the MPU into a reset sequence. (Refer to the M6800 manual for specific information on the MPU reset sequence.)

Clock Circuit. U030A, U030B and the associated components in the upper-right corner of schematic 4 generate the 2-phase MPU clock signal.

Recall that the output of U010A makes a low-to-high transition shortly after power-up. This transition fires U030A, so its $\overline{Q}$ output goes low. About 500 nanoseconds later, U030A times out and the low-to-high transition on the $\overline{Q}$ output fires U030B. U030B times out about 500 nanoseconds later and the negative transition on the Q output fires U030A, repeating the process.

The $\overline{Q}$ outputs of U030A and U030B feed open-collector drivers (U230B and U230A). The outputs of these gates drive phase 1 and phase 2 clock lines. The MPU clock inputs require a shorter rise time than the open-collector drivers can produce with simple pull-up resistors. Q126, Q135 and the associated components form active pull-ups that improve the rise time of the driver outputs. We'll discuss Q126 and the associated circuit as an example.

When the $\overline{Q}$ output of U030B makes a high-to-low transition, C024 couples the negative going pulse to the base of Q126. As a result, Q126 turns on for a short period and pulls the output of U230A up very quickly. The positive-going transition does not affect the circuit since the base of Q126 must go below about 4.5 volts to turn on.

The R-S flip-flop of U1630B and U310B controls the clock generator as previously discussed. When the MPU is idle it asserts 800_{16} on its address bus for about 500 nanoseconds and VMA (Valid Memory Address) goes high (upper left of schematic 6). U630 and U1310 decode the address and assert $\overline{\text{STOP}}$ while the address is on the bus. When $\overline{\text{STOP}}$ goes low, the flip-flop is reset and the output of U010A goes low, disabling the clock. The clock remains off until an interrupt occurs ($\overline{\text{IRQ}}$ is asserted) or an Interface Clear message is received on the IEEE 488 bus ($\overline{\text{IFC}}$ is asserted). Since the MPU is a dynamic device, data is lost if the clock is stopped for more than about 10 microseconds. As a result, when the clock is restarted, a power-on sequence is executed as previously discussed.

Front Panel Buttons. The front panel buttons provide for local control of the 7B90P. Refer to schematic 5 and notice that the front panel buttons are organized in a 4 X 8 matrix (excluding the TERMination button). The microprocessor sets the row lines (R0-R7) low so when a button is pressed, one of the column lines (C0-C3) goes low (pull-ups in the PIA hold the lines high when they are open). If any of the column lines go low, the output of U310A (top-right of schematic 6) goes low, pulsing the CA1 input. This generates an interrupt to the MPU. When the MPU services the interrupt, it takes all the row lines high, then it sets the row lines low one at a time and reads the column lines to determine which button was pressed. When the button is found, the MPU executes an appropriate service routine.

Front Panel Lamp Decoders. U630, U110 (bottom-right of schematic 8) and the associated gates decode the sweep timing lines, and drive the front panel TIME/DIV LED's. Schematic 5 shows the front panel LED's and drivers.

GPIB Interface

The GPIB Interface handles all communication between the MPU and the IEEE 488 bus. This description assumes a basic understanding of the GPIB protocols. Refer to IEEE STD 488-1975 for a complete discussion of the bus.

Before we discuss the GPIB Interface in detail a review of the handshake process is necessary. The IEEE 488 bus uses a three-wire interlocked handshake to transfer all data bytes. When all the addressed listeners on the bus are ready to receive data, $\overline{\text{NRFD}}$ (Not Ready for Data) goes high (not-asserted). The talker asserts data on DIO0-DIO7 and, when the data is stable, asserts $\overline{\text{DAV}}$ (Data Valid). When all the addressed listeners have accepted the data, $\overline{\text{NDAC}}$ (Not Data Accepted) goes high, and the talker releases $\overline{\text{DAV}}$. This process is repeated for every byte that is transferred on the bus. Refer to Appendix B of the IEEE Standard for a complete discussion and timing diagrams of the handshake process.

IEEE Data Bus. The GPIB data bus (DIOØ-DIO7) uses time-slot lines 2 through 9 (TS2-TS9) on the plug-in edge connector as a data bus. These lines are used in non-programmable mainframes for the readout time-slot lines. In a programmable mainframe, $\overline{\text{IFC}}$ (upper-left corner of schematic 7) is tied to a line that is clamped to about +3 volts maximum, turning Q1412 on. U1500 expects the modified time-slot information on TS1 and TS10 while TS2-TS9 are enabled as the GPIB data bus. We'll discuss the readout system later.

Acceptor Handshake. The 7B90P must "listen" to the data bus whenever it has been addressed or $\overline{\text{ATN}}$ (Attention) is asserted. When either of these cases are true, the output of U1630D is high, enabling U1630A, U1720A and U1720D. The MPU asserts BUSY left-center of schematic 7) while it is processing a byte from the bus. When BUSY and $\overline{\text{ATN}}$ are not asserted, the output of U530A is high. The output of U530D is low when $\overline{\text{DATVAL}}$ (DATa VALid) is unasserted and the output of U530A is high. $\overline{\text{NRFD}}$ is high (unasserted), indicating that the interface is ready for data, when the output of U1630D is high and the output of U530A is low. $\overline{\text{NRFD}}$ is asserted (low) if BUSY or $\overline{\text{DATVAL}}$ are asserted, indicating that the MPU is processing a byte or the interface is receiving a byte. When $\overline{\text{ATN}}$ is asserted the plug-in must listen, so $\overline{\text{NRFD}}$ goes high.

With $\overline{\text{NRFD}}$ high (ready for data) the interface is ready for the next step in the handshake process. The talker places data on the bus and, after a settling delay, asserts $\overline{\text{DAV}}$. When $\overline{\text{DAV}}$ goes low the output of U1520D goes high and the clear input of U1730B is released. The MPU pulses $\overline{\text{DATACC}}$ (DATa ACCepted) when it has received the byte. On the rising edge of $\overline{\text{DATACC}}$, U1730B is clocked and the Q output goes low. The low on the input of U1720A causes $\overline{\text{NDAC}}$ to go high. This tells the talker that the data is accepted. Finally, the talker relases DAV and the output of U1520D goes low, clearing U1730B and asserting $\overline{\text{NDAC}}$. If BUSY is asserted (indicating that the input buffer is full or EOI has been received), it is released when the MPU is ready for more data. This completes the acceptor handshake process.

Source Handshake. The source handshake is not implemented as defined by the IEEE 488 Standard. Instead, the plug-in talks through the mainframe using a non-interlocked handshake. The mainframe then generates the standard three-wire GPIB source handshake and transfers the data to the IEEE 488 bus.

When the 7B90P becomes a talker, TALK (left-center of schematic 7) is asserted. The MPU places its data on the bus and pulses $\overline{\text{SEND}}$ low. If $\overline{\text{ATN}}$ is not asserted, the negative transition on $\overline{\text{SEND}}$ fires one-shot U1530B. The Q output of U1530B is asserted for about 1 microsecond and the output of U530C ($\overline{\text{SND}}$) goes low. When U1530B times out, $\overline{\text{SND}}$ goes high and the mainframe latches the data from the plug-in. When the mainframe has completed the transfer, $\overline{\text{DAV}}$ makes a low-to-high transition (recall the discussion of the GPIB handshake process). This transition clocks U1730A and the Q output goes to the current state of $\overline{\text{ATN}}$. If $\overline{\text{ATN}}$ is high (unasserted), SENT goes high, telling the microprocessor that the data transfer is complete. If ATN is asserted during the data transfer, U1530B cleared and $\overline{\text{BADTLK}}$ is asserted, indicating that the transfer was interrupted.

When the 7B90P is listening, U1500 sources current onto the bus. The mainframe can sink this current and control the bus, but other programmable plug-ins cannot. As a result, when one plug-in is talking, all others must be off the bus (U1500 disabled). U1620C gates $\overline{\text{SND}}$ with the Q output of U1530B. If $\overline{\text{SND}}$ is asserted and the Q output of U1530B is low, another plug-in is talking, so the output of U1620C goes low. The output of U1520E and $\overline{\text{ENABLE}}$ go high, disabling U1500.

Readout Circuit

The readout circuit encodes the sweep speed settings and sends the information to the mainframe for display with the sweep signal. Before we begin the detailed circuit description, a review of the basic readout system is necessary. Refer to the mainframe manual for a complete description of the readout system.

Basic Readout Operation. In a non-programmable mainframe, the plug-in receives time-slot pulses on the time-slot lines (TS1-TS10). These lines are asserted (Pulled to -15 volts) sequentially so that only one line is asserted at any time. During these pulses, data is sent to the mainframe in the form of analog current on the row current and column current lines. These currents range from zero to 1 milliamp in 100 microamp steps. The current level on these lines defines a particular character in the character selection matrix shown in the mainframe manual.

The data encoded on the row and column lines is assigned a particular meaning during each time slot (see Table 5-1). For example, data on the lines during time slots 9 and 10 define the units of measurement for the plug-in (seconds in this case).

Table 5-1

Standard Readout Format

Time Slot Number	Description
TS-1	Determines the decimal magnitude (number of zeroes displayed or prefix change information) or the IDENTIFY function. (No display during this time-slot.)
TS-2	Indicates normal or inverted input (no display for normal input).
TS-3	Indicates calibrated or uncalibrated condition of plug-in variable control. (No display for calibrated condition.)
TS-4	1-2-5 scaling
TS-5 TS-6 TS-7	Not encoded by plug-in. Left blank to allow addition of zeroes by Readout System.
TS-8	Defines the prefix which modifies the units of measurement.
TS-9 TS-10	Defines the units of measurement of the plug-in unit. May be standard units of measurement (V,A,S, etc) or special units selected from the character selection matrix.

Summing The Time Slots. Programmable plug-ins and mainframes use time-slot lines TS2-TS9 as a data bus, as previously discussed. The time-slot pulses are transmitted to the plug-in as a stream of pulses on the TS10 line. The summation of the time slot pulses appears at pin 10 of U1500. Q1404 and R1515 shift the level of the -15 volt pulses to TTL-compatible levels. C1400 makes driving the signal for U1520F a low impedance at high frequencies. If C1400 is not present, this signal follows the threshold level of the schmitt input. U1520F inverts the pulses and improves their risetime. The output drives a four-bit counter, U1005 (upper-left of schematic 8). We'll come back to this counter shortly.

TS1 is asserted during its normal time-slot in both programmable and non-programmable mainframes. VR810, R810 and Q904 shift the level of the TS-1 pulse and invert it. This pulse clears U1005 to insure that the counter always starts at zero during time-slot 1.

At the end of time-slot 1, pins 2 and 3 of U1005 go low, enabling the counter. The output of U1520F (TSCLK Time-Slot Clock) also goes low, and the falling edge clocks U1230. U1230 continues to count up in binary until time slot 1 is asserted again at the beginning of the next train of time slot pulses. When time slot 1 is asserted, the counter is cleared and the process repeats. As a result, the Q_A - Q_D outputs of U1230 count from zero to nine and start over. These outputs drive U1100 and U1000.

Selecting Row and Column Currents. U1100 is a four-to-ten line decoder that asserts one output for each binary input word from zero through nine (outputs 3, 7 and 8 are used). Output pins 4, 9 and 10 drive current switches that sink the necessary row and column currents during time-slots 4, 8 and 9. For example, during time-slot 9, Q1308 sinks 400 microamps on the row current line.

U1000 takes the BCD coded time-slot number from U1005 and the information on W1-W12 from the MPU. On the basis of these inputs U1000 sinks a selected amount of current on pin 19. This current and the current in Q1304, Q1308 and Q1310 combine to form the row and column current for each time slot, and as a result, determine the character that is displayed during that time slot.

MPU Control Example

We've discussed the components of the microprocessor system and the analog circuitry. Now let's see how the MPU controls the plug-in by going through one routine in the ROM program.

The sweep positioning, trigger level and hold-off circuits are very similar. We'll discuss the sweep positioning circuit as an example. This discussion of the circuit operation and microprocessor routines apply to all three circuits.

Recall from our discussion of the Positioning Circuit that the DC positioning current came from a 10-bit Digital to Analog Converter (U330). The input word for the DAC is set by the microprocessor. When the plug-in is in remote mode, the POS command sets the value of this word.

If the 7B90P is in local mode, the POSITION control drives a tracking analog-to-digital converter consisting of a comparator circuit, the microprocessor and the DAC. If, for example, the POSITION control (R130 upper-right of schematic 5) is turned clockwise (trace moves right), the voltage at FB20 becomes less negative. The current through R814 increases and the voltage at pin 9 of U940C and pin 10 of U940D becomes positive. As a result, the output of U940C switches high. We'll come back to this point shortly.

FPEN (Front Panel Enable) at the top-center of schematic 7 is asserted when the 7B90P is in local mode. The high on FPEN enables U010B so the phase-2 clock pulses appear at its output high. These clock pulses go to U000A and B and U420A through U420D at the center of schematic 7. When the output of U940C switches high as just discussed, the clock pulses appear at the output of U420B (SPDN Sweep Position DowN). SPDN goes to one of the interrupt inputs of U810 at the bottom-center of schematic 6. The negative transition on this input sets the interrupt request flag in the control register of the PIA. At the same time, $\overline{\text{IRQA}}$ goes low, asserting the $\overline{\text{IRQ}}$ input of the MPU. The MPU saves its current status and sets the interrupt mask bit so that no further interrupts can occur until this one is serviced or the mask is cleared under program control. Then the processor jumps to a routine that reads the PIA control registers looking for a set interrupt flag. When the MPU reads control register A of U810, it finds the SPDN interrupt flag (bit 6 of the register) set. It then clears the flag and jumps to a service routine that takes control of the DAC input word.

The service routine checks if the interrupt was from the SPUP or SPDN comparators. For our example, the SPDN flag was set, so the service routine decrements the value of the DAC input word. As a result, the output current at pin 3 of U330 (top-left of schematic 4) decreases. The output of U340 swings less positive and begins to compensate for the change in the voltage level at the input of the comparators (SPA). If the voltage at the inputs of the comparators is balanced within its stable "window", the outputs of both comparators go low and the SPUP and SPDN outputs both go high.

Since the POSITION control moves very slowly in relation to the MPU's speed, the POSITION service routine decrements the value of the DAC input word by one and then checks all interrupts again. This allows other faster interrupts, such as transfers on the IEEE 488 bus, to be serviced while the operator adjusts the POSITION control. If the output of the DAC rises enough when the input word is decremented to bring the comparator inputs within their stable "window", no further interrupts occur. If the comparators' input voltage is not within this window, the SPDN interrupt occurs again on the next falling edge of the phase 2 clock. The MPU re-enters the interrupt routine and decrements the DAC input word again. This process is repeated until the SPUP interrupt stops occurring or the 10-bit word reaches its maximum value. The positioning current that is added to the signal, as previously discussed, comes from the output of U340 (upper-left of schematic 4).

If no interrupts occur and the MPU becomes idle, it asserts the STOP line. This stops the clock to minimize noise in the analog circuits. When an interrupt occurs or an $\overline{\text{IFC}}$ message is received, the clock restarts and the MPU executes a power-up routine.

The MPU control the front-panel buttons, front-panel LED's and the GPIB interface in a similar interrupt-driven fashion.

SECTION 6

CALIBRATION

Introduction

To assure instrument accuracy, check the calibration of the 7B90P every 1000 hours of operation or every six months if used infrequently. Before complete calibration, thoroughly clean and inspect this instrument as outlined in the Maintenance section.

Tektronix Field Service. Tektronix, Inc., provides complete instrument repair and recalibration service at local Field Service Centers and the Factory Service Center. Contact your local field office or representative for further information.

Performance Check. The performance of this instrument can be checked by performing only the steps listed in the Performance Check procedure. These steps check the instrument against the tolerances listed as Performance Requirements (see Specification section of this manual).

Limits and tolerances given in other check steps are calibration guides and should not be interpreted as instrument specifications. Operator front-panel adjustments are adjusted as part of the Performance Check procedure.

Calibration. To verify proper calibration of the 7B90P and to prevent unnecessary re-calibration of the entire instrument, perform the **Adjust-** portion of a step only if the tolerance given in the **Check-** part of the step is not met.

When performing a complete calibration procedure, make each adjustment to the exact setting even if the **Check-** is within allowable tolerance.

Test Equipment Required

General. The following test equipment and accessories, or its equivalent, is required for complete calibration of the 7B90P. Specifications given for the test equipment are the minimum necessary for accurate calibration. Therefore, the specifications of any test equipment used must meet or exceed the listed specifications. All test equipment is assumed to be correctly calibrated and operating within the listed specifications. Detailed operating instructions for the test equipment are not given in this procedure. Refer to the instruction manual for the test equipment if more information is needed. Table 6-1 shows a complete list of the test equipment.

Calibration Equipment Alternatives. All of the listed test equipment is required to completely check and adjust this instrument. The Calibration procedure is based on the first item of equipment given as an example of applicable equipment. When other equipment is substituted, control settings or the calibration set-up may need to be altered slightly to meet the requirements of the substitute equipment. If the exact item of test equipment given as an example in the Test Equipment list is not available, first check the Specifications column carefully to see if any other equipment is available which might suffice. Then check the Usage column to see what this item of test equipment is used for. If used for a check or adjustment which is of little or no importance to your measurement requirements, the item and corresponding step(s) can be deleted.

Checking Programmable Features. The basic 7B90P calibration procedure does not require a controller. If an IEEE 488 interfaced controller is available, the programmable features of the 7B90P can be tested by sending commands to the plug-in over the IEEE 488 bus. Refer to the programming section of this manual for specific information on the commands.

The commands can also be used to change the 7B90P settings during the calibration procedure. For example, a program could be written to set the 7B90P POSITION DAC (Digital to Analog Converter), simplifying the POSITION adjustments.

TABLE 6-1
Test Equipment

Description	Minimum Specifications	Usage	Examples of Applicable Equipment
Calibration Mainframe	7900-Series programmable mainframe.	Used to provide display.	Tektronix 7912AD Programmable Digitizer and necessary peripherals for display.
Wide-Band Amplifier Plug-in Unit	7A-Series amplifier plug-in unit; Bandwidth - 500 MHz; Deflection factor - 50 mV to 5 V.	Used throughout procedure to provide vertical input to the mainframe.	Tektronix 7A19 Amplifier.
Time-Mark Generator	Marker outputs - 2 ns to 5 s; accuracy - within 0.1%.	Sweep timing check and adjustments.	Tektronix TG501 Time-Mark Generator.[1]
Low-Frequency Sine-Wave Generator	Frequency - 30 Hz to 50 KHz; output amplitude - variable from 50 mV to 8 V into 50 ohms.	Low-frequency triggering checks and adjustments.	Tektronix FG503 Generator.[1]
Mid-Frequency Sine-Wave Generator	Frequency - 250 KHz to 250 MHz; output amplitude range - 5 mV to 5.5 V peak-to-peak.	Mid-Frequency Trigger checks and adjustments	Tektronix SG503 Generator.[1]
High-Frequency Sine-Wave Generator	Frequency - 245 MHz to 500 MHz output amplitude - 0.5 V to 4.0 V.	High Frequency Trigger checks and adjustments	Tektronix SG504 Generator.[1]

TABLE 6-1 (cont.)
Test Equipment

Description	Minimum Specifications	Usage	Examples of Applicable Equipment
Precision Coaxial Cable	50 ohms.	Used with SG503.	Tektronix part number: 012-0482-00.
Digital Volt Meter	Range - from 200 millivolts to 10 volts.	Trigger Level adjustments.	Tektronix DM502.[1]
Test Oscilloscope	Vertical Sensitivity - 500 mV to 1 V Bandwidth - to 10 MHz	Holdoff check procedure.	Tektronix 465 Oscillo-scope.
Plug-in Extender	Tektronix 7000-series extender.	Provides access to internal adjustments and test points.	Tektronix Calibration fixture-part number: 067-0589-00.[1]
Coaxial Cables (2 required)	Impedance - 50 ohms; Type - RG58/U; length 18 and 42 inches; con-nectors - BNC.	Used through-out procedure	Tektronix part number: 18 inch- 012-0057-01 42 inch- 012-0076-00.
BNC T Connector		External trigger checks and adjustments.	
X5 50 ohm attenuator		Trigger checks and adjustments.	Tektronix part number: 011-0060-01.

[1] Requires TM 500-Series Power Module.

Performance Check Procedure

1. Insert the 7B90P and the vertical amplifer unit into the mainframe. Turn on the mainframe and monitor power and allow 20 minutes warm-up time before proceeding.

2. Set the 7912AD to LOCAL and TV modes.

3. Adjust the Graticule Intensity for a sharp graticule.

4. Adjust the Main Intensity and Focus for a visible trace with no blooming.

5. If a Tektronix IEEE 488 interfaced controller and TEK SPS BASIC software are available the 7B90P programmable functions can be checked by running the 7912AD checkout software. Refer to the Checkout Software Manual for information on loading and running the software. Checkout programs can be written for other IEEE 488 interfaced controllers by studying the information given in the programming section of this manual.

CAUTION

The writing beam intensity in the 7912AD is critical. Excessive intensity can permanently damage the scan converter target. Many portions of the Performance Check and Calibration procedures require adjustment of intensity or sweep speed. Remember that reducing sweep speed has the same effect as increasing intensity. Always reduce intensity before reducing sweep speed.

Check Triggering Modes

Test Set-Up

Set the 7B90P controls as follows:

TIME/DIV:	20 microseconds/division
MAG:	Off
MODE:	PP AUTO
COUPLING:	AC
SOURCE:	INTernal
SLOPE:	+ (light on)
POSITION:	Midrange
HOLD OFF:	Fully counterclockwise

1. Connect the low-frequency sine wave generator to the amplifier unit input with the 42-inch BNC cable.

2. Set the generator frequency to 50 kilohertz.

3. Set the low-frequency sine-wave generator and the amplifier unit VOLTS/DIV for approximately two vertical divisions of deflection.

4. **Check-** for a stable display at all TRIGGER LEVEL control settings.

5. Set the TRIGGERING MODE to NORMal.

6. Adjust the LEVEL control for a stable display (TRIG'D light on).

7. **Check-** for no display (TRIG'D light off) when the LEVEL control is set fully clockwise and fully counterclockwise.

8. Set the LEVEL control for a stable display.

9. Set the TRIGGERING MODE to SinGLe SWeeP and the SOURCE to EXTernal.

10. Press the SinGLe SWeeP RESET button (part of the SGL SWP MODE button).

11. **Check-** that the READY light is on.

12. **Check-** for one sweep when the INTernal SOURCE button is pressed. The Mainframe Intensity may need to be increased to view the single sweep display.

13. **Check-** that the READY light goes out at the end of the sweep.

14. Decrease the 7912AD Main Intensity and remove the signal connection.

Check External Level Range

Test Set-Up

Set the 7B90P controls as follows:

TIME/DIV:	500 microseconds
MAG:	Off
MODE:	NORMal
COUPLING:	AC
SOURCE:	EXTernal (X1)
SLOPE:	+ (Light On)
POSITION:	Midrange
HOLD OFF:	Fully counterclockwise
TERM:	IN- one Megohm

1. Connect the low-frequency sine-wave generator to the EXT TRIG IN connector with a 42-inch, 50-ohm BNC cable, a X5, 50-ohm attenuator and a BNC T-connector. Connect the free output of the T-connector to the amplifier unit input with an 18-inch, 50-ohm cable.

2. Set the amplifier unit deflection factor to 0.1 volts per division. Set the sine-wave generator for a six division display at one kilohertz.

3. **Check-** that all levels of the positive slope may be selected for the sweep starting point as the TRIGGERING LEVEL control is rotated throughout its range.

4. **Check-** that the time base is not triggered at either end of the LEVEL control rotation.

5. Set the SLOPE to negative (light off).

6. **Check-** repeat steps three and four for the negative slope of the waveform.

Check Internal/External Low Frequency Triggering Sensitivity

Test Set-Up

Set the 7B90P controls as follows:

TIME/DIV:	One millisecond
MAG:	Off
MODE:	NORMal
COUPLING:	AC
SOURCE:	EXTernal (X1)
SLOPE:	+ (Light On)
POSITION:	Midrange
HOLD OFF:	Fully counterclockwise
TERM:	IN- one Megohm

1. Set the amplifier unit VOLTS/DIV to ten millivolts.

2. Set the low-frequency sine-wave generator for 300 Hertz and an output amplitude of approximately 100 millivolts.

3. Reduce the generator output frequency to 30 Hertz.

NOTE

The 7912AD turns the writing beam off when the time base is set for sweep speeds below 1 millisecond per division.

4. Adjust the LEVEL control for a stable display.

5. **Check-** for a stable display (TRIG'D light on) with the coupling set to:

a. AC
b. AC HF REJ
c. DC

(Adjust the LEVEL control as necessary).

6. Change the TRIGGERING SLOPE to negative (light off) and repeat step five.

7. Set the TRIGGERING MODE to PP AUTO and COUPLING to AC.

8. Set the amplifier unit to 0.1 volt/division and the sine-wave generator for an output amplitude of 500 millivolts at 500 Hertz.

9. Reduce the generator output frequency to 50 Hertz.

10. **Check**- for a stable display (TRIG'D light on) at all settings of the LEVEL control with COUPLING set to:

a. AC
b. DC

11. Set the SLOPE to positive (light on), and repeat step ten.

12. Set the amplifier unit deflection factor for 50 millivolts/division and the sine-wave generator for approximately 125 millivolts at 200 Hertz.

13. Set the SLOPE to negative (light off) and Repeat steps ten and eleven.

14. Set the 7B90P TRIGGERING SOURCE to INTernal.

15. Set the amplifier unit to 0.1 Volt/Division. Adjust the generator for a display amplitude of 3 major divisions at 300 Hertz.

16. Set the amplifier unit to 1 Volt/Division and the generator output frequency to 30 Hertz.

17. Adjust the 7B90P LEVEL control for a stable display (TRIG'D lights on).

18. **Check** - for a stable display with coupling set to:

a. AC
b. AC HF REJ
c. DC

(Adjust the LEVEL control as necessary).

NOTE

The Tektronix FG502 signal generator has a DC offset control. This control must be off (pressed in) for the DC COUPLING checks.

19. Set the SLOPE to negative (light off) and repeat step 18.

20. Set the MODE to PP AUTO and COUPLING to AC.

21. Set the low-frequency sine-wave generator and the amplifier unit for two major divisions of vertical deflection at 500 Hertz.

22. Reduce the generator output frequency to 50 Hertz.

23. **Check** - for a stable display (TRIG'D light on) at all settings of the LEVEL control with COUPLING set to:

a. AC
b. DC

24. Set the SLOPE to positive (light on) and repeat step 23.

25. Set the sine-wave generator frequency to 200 Hertz and the amplifier unit to 0.1 volts per division.

26. Adjust the generator for five major divisions of vertical deflection.

27. Set the amplifier unit to 1 volt per division.

28. Set the SLOPE to negative and repeat steps 23 and 24.

Check Internal/External Mid-Frequency Triggering Sensitivity

Test Set-Up

Set the 7B90P controls as follows:

TIME/DIV:	20 nanoseconds
MAG:	Off
MODE:	NORMal
COUPLING:	AC
SOURCE:	EXTernal (X1)
SLOPE:	+ (Light On)
POSITION:	Midrange
HOLD OFF:	Fully counterclockwise

1. Disconnect the low-frequency sine-wave generator from the T-connector and connect the mid-frequency signal generator to the T-connector with a X5 50 ohm attenuator.

NOTE

The Tektronix SG503 requires a special BNC cable for calibrated operation. Refer to Table 6-1 for more information.

2. Set the amplifier unit deflection factor to 20 millivolts per division and the high-frequency generator for a display amplitude of five divisions at 50 megahertz.

3. **Check-** for a stable display (TRIG'D light on) with the COUPLING set to:

   a. AC
   b. AC LF REJ
   c. DC

(Adjust the LEVEL control as necessary).

4. Set the SLOPE to negative and repeat step three.

5. Set the amplifier deflection factor to 50 millivolts/division and set the mid-frequency signal generator for a 2.5-division display.

6. Set the TRIGGERING MODE to PP AUTO.

7. **Check-** for a stable display (TRIG'D light on) at all settings of the LEVEL control with COUPLING set to:

a. AC
b. DC

8. Set the SLOPE to positive and repeat step seven.

9. Set the TRIGGERING MODE to NORM.

10. Set the amplifier unit to 0.1 Volts/Division and adjust the generator for three major divisions of vertical deflection at 50 Megahertz.

11. Set the amplifier unit to one volt per division.

12. **Check** - for a stable display (TRIG'D light on) with COUPLING set to:

a. AC
b. AC LF REJ
c. DC

(Adjust the LEVEL control as necessary).

13. Set the SLOPE to negative (light off) and repeat step 12.

14. Set the mid-frequency signal generator and the amplifier unit deflection factor for a 0.5 division display.

15. Set the TRIGGERING MODE to PP AUTO.

16. **Check** - for a stable display (TRIG'D light on) at all settings of the LEVEL control with COUPLING set to.

a. AC
b. DC

17. Set the SLOPE to positive (light on) and repeat step 16.

Check Internal/External High Frequency Triggering Sensitivity

Test Set-Up

Set the 7B90P controls as follows:

TIME/DIV:	One nanosecond
MAG:	Off
MODE:	PP AUTO
COUPLING:	AC
SOURCE:	EXTernal (X1)
SLOPE:	+ (Light On)
POSITION:	Midrange
HOLD OFF:	Fully counterclockwise
TERM:	IN- one Megohm

1. Disconnect the mid-frequency sine-wave generator and connect the high-frequency sine-wave generator to the T-connector with a X5, 50-ohm attenuator.

2. Set the high-frequency signal generator for display amplitude of 7.5 divisions at 400 megahertz.

3. **Check** - for a stable display (TRIG'D light on) at all settings of the LEVEL control with COUPLING set to:

   a. AC
   b. DC

4. Set the SLOPE to negative and repeat step three.

5. Set the high-frequency signal generator for a five division display at 400 megahertz.

6. Set the TRIGGERING MODE to NORM and the SLOPE to positive.

7. **Check**- for a stable display (TRIG'D light on) with coupling set to:

   a. AC
   b. AC LF REJ
   c. DC

(Adjust the LEVEL control as necessary).

8. Set the SLOPE to negative (light off) and repeat step seven.

9. Set the high-frequency signal generator and the amplifier unit deflection factor for a 1.5 division display at 400 megahertz.

10. Set the TRIGGERING SOURCE to INTernal.

11. Repeat step seven for both positive and negative SLOPE.

12. Set the 7B90P MODE to PP AUTO.

13. Repeat step seven for both positive and negative SLOPE.

Check Internal Trigger Jitter

Test Set-Up

Set the 7B90P controls as follows:

TIME/DIV:	500 picoseconds
MAG:	Off
MODE:	NORMal
COUPLING:	AC
SOURCE:	INTernal
SLOPE:	Positive (light on)
POSITION:	Midrange
HOLD OFF:	Fully counterclockwise

1. Adjust the LEVEL control for a stable display (TRIG'D light on)

2. **Check-** for a stable display with no more than 0.2 major horizontal divisions (0.1 nanosecond) of jitter.

Check Line Triggering

1. Remove all signal connections and reduce the 7912AD Main Intensity.

2. Set the TRIGGERING SOURCE to LINE and the TIME/DIV to one millisecond.

3. Set the LEVEL control to approximately midrange.

4. **Check-** that the TRIG'D light is on.

5. **Check-** that the TRIG'D light goes out when the LEVEL control is rotated to both limits.

Check Sweep Length and Positioning

Test Set-Up

Set the 7B90P controls as follows:

TIME/DIV:	One millisecond
MAG:	Off
MODE:	PP AUTO
COUPLING:	AC
SOURCE:	INTernal
SLOPE:	Positive (light on)
POSITION:	Midrange
HOLDOFF:	Fully counterclockwise
TERM:	IN- one Megohm

1. Connect the time-mark generator to the amplifier unit with a 50-ohm BNC cable. Set the time-mark generator for one millisecond markers.

2. Adjust the Main Intensity and Focus for a sharp display.

3. Set the 7B90P LEVEL control for a stable display (TRIG'D light on).

4. Set the amplifier for approximately two divisions of vertical deflection and center the display vertically.

5. Adjust the 7B90P POSITION control to place the second time marker on the first graticule line.

6. **Check-** that the end of the sweep is beyond 9.2 major graticule divisions, indicating that the sweep is at least 10.2 divisions long.

7. Set the POSITION control fully clockwise and note the position of the start of the sweep.

8. **Check-** that the start of the sweep is 1.4 divisions to the right of the graticule center ±0.5 div.

9. Set the POSITION control fully counterclockwise.

10. **Check-** that the end of the sweep is to the left of the graticule center.

Check Magnifier Gain

1. Set the time-mark generator for one millisecond markers.

2. Set the 7B90P TIME/DIVISION to one millisecond.

3. **Check** - for one time mark per division over the center eight divisions.

4. **Adjust** - the front-panel screwdriver SWP CAL control for one marker per division over the center eight divisions.

5. Set the 7B90P MAG to on (button lit) and set the POSITION control to midrange.

6. Set the time-mark generator for 0.1 millisecond markers.

7. **Check-** for one marker per horizontal division over the center eight divisions. Adjust the 7B90P POSITION and mainframe Intensity control as necessary.

Check Sweep Timing

Test Set-Up

Set the 7B90P controls as follows:

MAG:	OFF
MODE:	NORMal
COUPLING:	AC
SOURCE:	INTernal
SLOPE:	Positive (light on)
POSITION:	Midrange
HOLD OFF:	Fully counterclockwise
TERM:	IN- one Megohm

1. **Check-** the sweep accuracy for all unmagnified TIME/DIV ranges. Check for one marker per division over the center eight divisions. The time-marks should be within 0.12 division for sweep speeds below 100 nanoseconds and within 0.2 division for the faster sweep speeds. Adjust the TRIGGERING LEVEL, POSITION, and Mainframe Intensity controls as necessary.

NOTE

The sweep timing tolerances are for an ambient temperature range of +15 degrees centigrade to +35 degrees centigrade. If outside this range, see the Specifications section for allowable tolerances.

Check Magnified Sweep Timing

1. Center the display horizontally on the graticule. Set the MAG to on (button lit) and the SOURCE to EXTernal.

2. Set the TERM to 50-ohms (button released).

3. Connect the time-mark generator trigger output to the EXT TRIG IN connector with a 50-ohm BNC cable.

4. **Check-** the sweep accuracy for all unmagnified TIME/DIV ranges. Check for one marker per division over the center eight divisions. (Use one nanosecond markers for 500 picoseconds/division and check for one marker in two divisions.) The time-marks should be within 0.2 division for sweep speeds below 5 nanoseconds and within 0.32 division for faster sweep speeds. Adjust the TRIGGERING LEVEL, POSITION and Mainframe Intensity controls as necessary.

Check Holdoff

1. Connect the GATE OUTput of the 7912AD to the vertical input of the test oscilloscope with a 42-inch BNC cable and a X5 50-ohm attenuator.

2. Adjust the test oscilloscope for a triggered display.

3. **Check -** that the displayed pulse width varys while rotating the 7B90P HOLDOFF control.

4. Repeat step three for all 7B90P TIME/DIV ranges below 200 microseconds and above 5 microseconds. Adjust the test oscilloscope as necessary.

NOTE

The range of the HOLDOFF control is limited by the 7912AD in sweep speeds between 200 microseconds and 50 microseconds. The 7912AD disables the holdoff circuit in TIME/DIV ranges between 20 microseconds and 5 microseconds.

Calibration Procedure

The following procedure is arranged so that the 7B90P can be calibrated with the least interaction of adjustments and re-connection of equipment. The control settings and test equipment set-up throughout the procedure continue from preceding steps unless otherwise noted. Refer to Fig. 6-1a and b for the location of adjustments. The test set up is summarized at the beginning of each section of the calibration procedure. When performing the complete procedure, this summary provides a check of the instrument settings. Any part of the calibration procedure can be performed by setting up the equipment as shown in the tables.

NOTE

Control titles that are printed on the 7B90P front panel are capitalized (e.g., POSITION). Internal adjustments and associated equipment controls are initially capitalized only (e.g., Pulse Amplitude).

Preliminary Procedure for Calibration

1. Remove the 7B90P side panels.

2. Insert the plug-in extender into the mainframe horizontal compartment and plug the 7B90P into the extender.

3. Install the amplifier unit in the mainframe vertical compartment.

4. Turn the mainframe power on and adjust for a visible trace. Allow 20 minutes warm-up time before proceding.

NOTE

This instrument should be calibrated at an ambient temperature of +20 degrees centigrade to +30 degrees centigrade for best overall accuracy. The performance of the instrument can be checked at any temperature from 0 degrees to 40 degrees Centigrade.

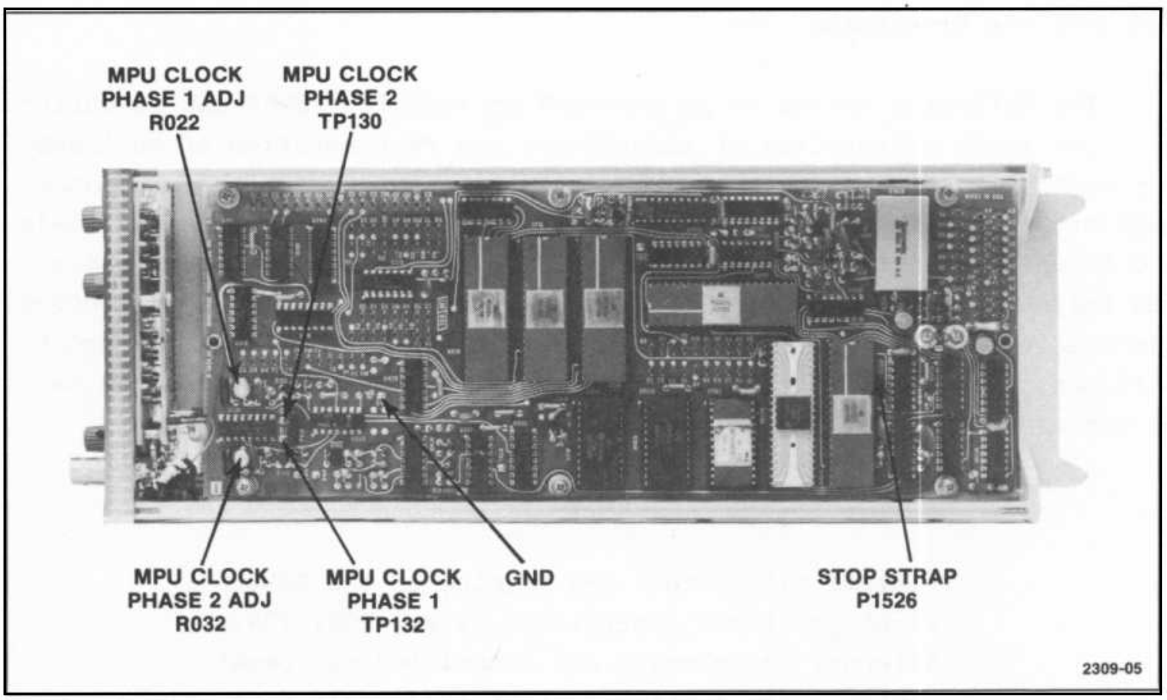

Fig. 6-1a. Test point and adjustment locations horizontal programming board.

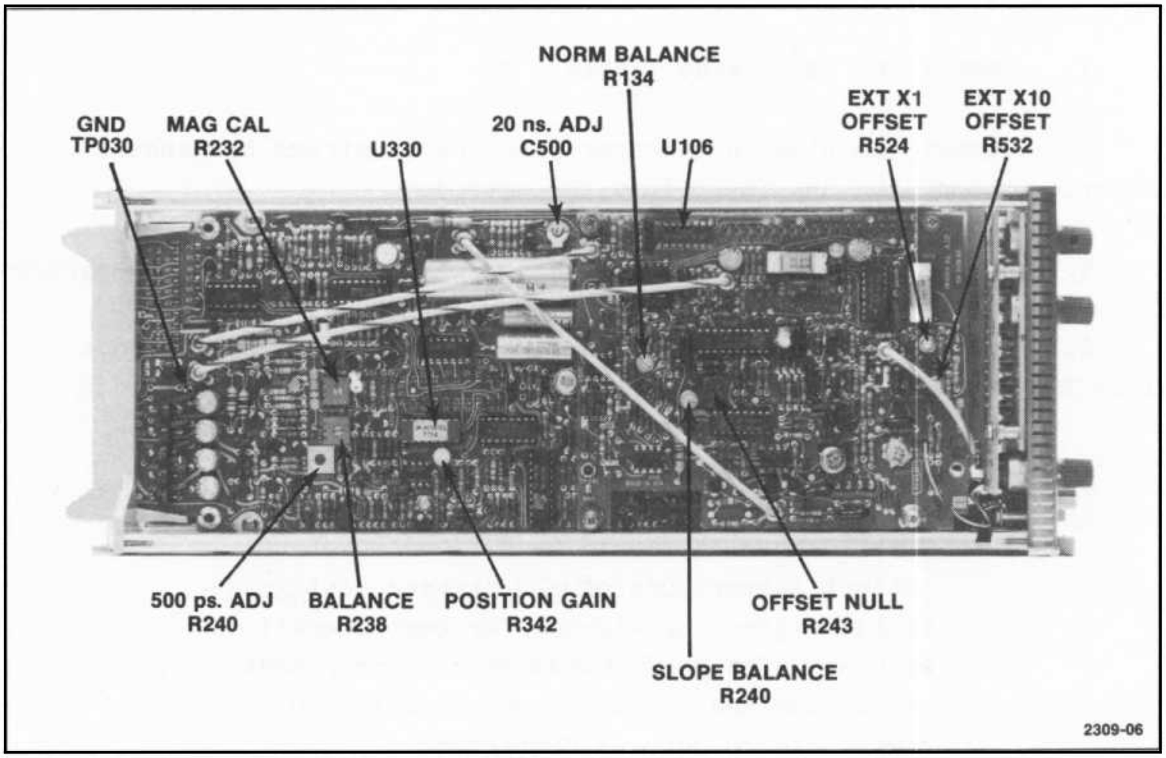

Fig. 6-1b. Test point and adjustment locations sweep and trigger boards.

Check/Adjust MPU Clock Speed

Test Set-Up

Set the 7B90P controls as follows:

TIME/DIV:	100 nanoseconds
MAG:	Off
MODE:	PP AUTO
COUPLING:	AC
SOURCE:	INTernal
SLOPE:	Positive (light on)
POSITION:	Midrange
HOLDOFF:	Fully counterclockwise
TERM:	IN- one Megohm

1. Remove the STOP strap, P1526, on the Horizontal Programming Board (see Fig. 6-1a).

2. Install a X10, 50 ohm probe on the input of the amplifier unit. Set the VOLTS/DIV to one volt. If a X10, 50-ohm probe is not available, use a high input impedance 7000-series amplifier unit and probe.

3. Connect the ground wire of the probe the the ground test point on the Horizontal Programming board (see Fig. 6-1a).

4. Connect the probe to TP132 on the Horizontal Programming Board.

5. Press the +SLOPE button once to start the clock, then press it again to reset the SLOPE to positive.

6. **Check-** that the pulse width (high-time) is between 480 nanoseconds and 520 nanoseconds.

7. **Adjust-** R022 for a 500 nanosecond pulse width.

8. Move the probe to TP130.

9. **Check-** that the pulse width is between 480 nanoseconds and 520 nanoseconds.

10. **Adjust-** R032 for a 500 nanosecond pulse width.

11. Remove the probe and install the $\overline{\text{STOP}}$ strap, P1420.

Check/Adjust Trigger Offset Null, Normal Balance and Slope Balance

Test Set-Up

Set the 7B90P controls as follows:

TIME/DIV:	20 microseonds
MAG:	Off
SLOPE:	Positive (light on)
MODE:	PP AUTO
COUPLING:	AC
SOURCE:	INTernal
POSITION:	Midrange
HOLD OFF:	Fully counterclockwise
TERM:	IN- one Megohm

1. Connect the low frequency sine-wave generator to the amplifier unit with a 50-ohm BNC cable.

2. Set the amplifier unit to 0.1 volts per division.

3. Set the mainframe Intensity and Focus for a sharp display.

4. Adjust the sine-wave generator for a display amplitude of three major divisions at 50 kilohertz.

5. Center the display vertically.

6. Set the amplifier-unit to one volt per division.

7. Set the 7B90P TRIGGERING LEVEL to midrange.

8. Connect the negative lead of the Digital Voltmeter to the ground testpoint, TP030 on the sweep board (see Fig. 6-1b).

9. Measure the voltage at pins 5 through 12 of U106 on the trigger board.

10. Adjust the LEVEL control until pins 6 through 12 are all low (0 V to +0.8 V) and pin 5 is high (+2.4 V to +5.5 V).

11. **Check-** for a stable display with the TRIG'D light on.

12. **Adjust-** Offset Null, R243, for a stable display.

13. Set the SLOPE to negative (light off).

14. **Check-** for a stable display.

15. **Adjust-** Slope Balance, R240 for a stable display.

16. **Interaction-** Repeat adjustment of offset null (R243) and Slope Balance (R240) until a stable display is obtained while changing TRIGGERING SLOPE.

17. Set the TRIGGERING mode to NORMal.

18. **Check-** for a stable display.

19. **Adjust-** Normal Balance, R134 for a stable display.

20. Remove the test leads of the Digital Voltmeter.

21. To check the adjustments, perform the check procedure for the triggering functions. If any of the check procedures cannot be met, repeat the adjustments in this section.

Check/Adjust External X1 and X10 Balance

Test Set-Up

TIME/DIV:	20 microseconds
MAG:	Off
SLOPE:	Positive (light on)
MODE:	PP AUTO
COUPLING:	AC
SOURCE:	INTernal
POSITION:	Midrange
HOLD OFF:	Fully counterclockwise
TERM:	IN- one megohm

1. Connect the low-frequency sine-wave generator to the EXT TRIG IN connector and the input of the amplifier unit through a BNC T-connector.

2. Set the amplifier unit to 0.1 volts per division.

3. Adjust the sine wave generator for a display amplitude of two major divisions at 50 kilohertz.

4. Center the display vertically.

5. Adjust the TRIGGERING LEVEL as described in step ten of the preceding section.

6. Switch the 7B90P SOURCE to EXT (X1) and the MODE to NORMal.

7. **Check-** that the trigger point does not change when switching between INT and EXT.

8. **Adjust-** R524, Ext X1 Offset, for minimum shift in the trigger point while switching between INT and EXT.

9. Set the amplifier unit to 0.5 volts/division.

10. Adjust the sine-wave generator for a two division display.

11. Set the 7B90P SOURCE to EXT X10.

12. **Check-** that the trigger point does not change when switching between INT and EXT X10.

13. **Adjust-** R532, EXT X10 Offset, for minimum shift in the trigger point while switching between INT and EXT X10.

14. Disconnect the low-frequency sine-wave generator.

Check/Adjust Sweep and Magnifier Calibration

Test Set-Up

Set the 7B90P controls as follows:

TIME/DIV: One millisecond

MAG:	Off
SLOPE:	Positive (light on)
MODE:	PP AUTO
COUPLING:	AC
SOURCE:	INTernal
POSITION:	Midrange
HOLD OFF:	Fully counterclockwise

1. Connect the time-mark generator to the amplifier unit input.

2. Set the time-mark generator for one millisecond markers.

3. Adjust the mainframe Intensity and Focus for a sharp display.

4. **Check-** for one marker per division over the center eight divisions. (Adjust the POSITION control as necessary.)

5. **Adjust-** the front panel SWP CAL for one marker per division over the center eight divisions.

6. Set the MAG to on (light on).

7. Set the time-mark generator for 0.1 millisecond markers.

8. **Check-** for one marker per division over the center eight divisions.

9. **Adjust-** R232, Magnifier Calibrate, for one marker per division over the center eight divisions.

Check/Adjust Balance

Test Set-Up

Set the 7B90P controls as follows:

TIME/DIV:	One millisecond
MAG:	On
SLOPE:	Positive (light on)
MODE:	PP AUTO
COUPLING:	AC

SOURCE:	INTernal
POSITION:	Midrange
HOLD OFF:	Fully counterclockwise

1. Set the time-mark generator to one millisecond markers.

2. Adjust the POSITION control to place the first marker on the center graticule line.

3. Set the 7B90P MAG off.

4. **Check-** that the first time marker is positioned at the center graticule line.

5. **Adjust-** R238, Balance, for minimum shift in the marker position while switching the MAG on and off.

Check/Adjust Sweep Timing

Test Set-Up

Set the 7B90P controls as follows:

TIME/DIV:	20 nanoseconds
MAG:	Off
SLOPE:	Positive (light on)
MODE:	PP AUTO
COUPLING:	AC
SOURCE:	INTernal
POSITION:	Midrange
HOLD OFF:	Fully counterclockwise
TERM:	OUT- 50 ohm

1. Set the time-mark generator to 20 nanosecond markers.

2. Adjust the mainframe Intensity and Focus for a sharp display.

3. **Check-** for one marker per division over the center eight divisions. (Adjust- the POSITION control as necessary.)

4. **Adjust** C500, 20 ns. Adj., for one marker per division over the center eight divisions.

5. Set the 7B90P TIME/DIV to 10 nanoseconds and the time-mark generator for 10 nanosecond time markers.

6. **Check-** for one marker per division over the center eight divisions.

7. Set the 7B90P TIME/DIV to 50 nanoseconds and the time-mark generator for 50 nanosecond time markers.

8. **Check-** for one marker per division over the center eight divisions.

9. If the checks in steps five or seven are not met, adjust C500 for the best overall accuracy between 10, 20 and 50 nanoseconds. Then repeat steps one through eight.

10. Connect the trigger output of the time-mark generator to the EXT TRIG IN connector of the 7B90P.

11. Set the TRIGGERING SOURCE to EXTernal and adjust the LEVEL control for a stable display.

12. Set the time-mark generator for one nanosecond markers.

13. Set the 7B90P TIME/DIV to 500 picoseconds.

14. Adjust the mainframe Intensity and Focus for a sharp display.

NOTE

Because of bandwidth limitations the time-mark amplitude may be attenuated.

15. **Check-** for one marker per two divisions over the center eight divisions.

16. **Adjust-** R240, 500 ps. Adj., for one marker per two divisions over the center eight divisions.

17. Check the sweep timing on all TIME/DIV ranges as discussed in the Sweep Timing section of the Performance Check Procedure.

18. Decrease the mainframe intensity.

Check/Adjust Sweep Position

Test Set-Up

Set the 7B90P controls as follows:

TIME/DIV:	One millisecond
MAG:	Off
SLOPE:	Positive (light on)
MODE:	PP AUTO
COUPLING:	AC
SOURCE:	INT
POSITION:	Midrange
HOLD OFF:	Fully counterclockwise
TERM:	OUT- 50 ohms

1. Set the time-mark generator for one millisecond markers.

2. Adjust the POSITION control so the first marker is on the center graticule mark.

3. Press the MAG button and set the first time mark as close as possible to the center graticule mark.

4. Connect the negative lead of the Digital Voltmeter to the ground test point, TP030 on the sweep board (see fig. 6-1b).

5. Measure the voltage on pins 4 through 13 of U330. Voltages in the range of 0 volts to 0.8 volts represent a logical zero. Voltages in the range of 2.0 volts to 5.0 volts represent a logical one. Record the binary word on pins 4 through 13, where pin 13 corresponds to the least significant bit and pin 4 corresponds to the most significant bit.

6. Add 800_{10} (1100100000_2) to this binary word and record the sum.

1440

7. Set the 7B90P MAG to off (light off).

8. Adjust the POSITION control so the eleventh marker is on the center graticule mark.

9. Check the positioning of the mark by turning the MAG on.

10. Measure the binary word on U330 as outlined in step five.

11. **Check-** that this binary word is equal to the sum computed in step six.

12. **Adjust-** R342, Position Gain, until the measured binary word is equal to the sum computed in step six.

13. Disconnect all test equipment.

This completes the 7B90P calibration procedure.

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000	Part first added at this serial number
00X	Part removed after this serial number

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

ACTR	ACTUATOR	PLSTC	PLASTIC
ASSY	ASSEMBLY	QTZ	QUARTZ
CAP	CAPACITOR	RECP	RECEPTACLE
CER	CERAMIC	RES	RESISTOR
CKT	CIRCUIT	RF	RADIO FREQUENCY
COMP	COMPOSITION	SEL	SELECTED
CONN	CONNECTOR	SEMICOND	SEMICONDUCTOR
ELCTLT	ELECTROLYTIC	SENS	SENSITIVE
ELEC	ELECTRICAL	VAR	VARIABLE
INCAND	INCANDESCENT	WW	WIREWOUND
LED	LIGHT EMITTING DIODE	XFMR	TRANSFORMER
NONWIR	NON WIREWOUND	XTAL	CRYSTAL

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
00853	SANGAMO ELECTRIC CO., S. CAROLINA DIV.	P.O. BOX 128	PICKENS, SC 29671
01121	ALLEN-BRADLEY COMPANY	1201 2ND STREET SOUTH	MILWAUKEE, WI 53204
01295	TEXAS INSTRUMENTS, INC. SEMICONDUCTOR GROUP	P.O. BOX 5012	DALLAS, TX 75222
02735	RCA CORPORATION, SOLID STATE DIVISION	ROUTE 202	SOMERVILLE, NY 08876
04222	AVX CERAMICS, DIVISION OF AVX CORP.	P O BOX 867	MYRTLE BEACH, SC 29577
04713	MOTOROLA, INC., SEMICONDUCTOR PROD. DIV.	5005 E MCDOWELL RD,PO BOX 20923	PHOENIX, AZ 85036
07263	FAIRCHILD SEMICONDUCTOR, A DIV. OF FAIRCHILD CAMERA AND INSTRUMENT CORP.	464 ELLIS STREET	MOUNTAIN VIEW, CA 94042
09023	CORNELL-DUBILIER ELECTRONIC DIVISION FEDERAL PACIFIC ELECTRIC CO.	2652 DALRYMPLE ST.	SANFORD, NC 27330
12697	CLAROSTAT MFG. CO., INC.	LOWER WASHINGTON STREET	DOVER, NH 03820
12954	SIEMENS CORPORATION, COMPONENTS GROUP	8700 E THOMAS RD, P O BOX 1390	SCOTTSDALE, AZ 85252
13511	AMPHENOL CARDRE DIV., BUNKER RAMO CORP.		LOS GATOS, CA 95030
14433	ITT SEMICONDUCTORS	3301 ELECTRONICS WAY P O BOX 3049	WEST PALM BEACH, FL 33402
14552	MICRO SEMICONDUCTOR CORP.	2830 E FAIRVIEW ST.	SANTA ANA, CA 92704
17856	SILICONIX, INC.	2201 LAURELWOOD DRIVE	SANTA CLARA, CA 95054
18324	SIGNETICS CORP.	811 E. ARQUES	SUNNYVALE, CA 94086
22229	SOLITRON DEVICES, INC., SEMICONDUCTOR GROUP	8808 BALBOA AVENUE	SAN DIEGO OPERS, CA 92123
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
27014	NATIONAL SEMICONDUCTOR CORP.	2900 SEMICONDUCTOR DR.	SANTA CLARA, CA 95051
32293	INTERSIL, INC.	10900 N. TANTAU AVE.	CUPERTINO, CA 95014
32997	BOURNS, INC., TRIMPOT PRODUCTS DIV.	1200 COLUMBIA AVE.	RIVERSIDE, CA 92507
34371	HARRIS SEMICONDUCTOR, DIV. OF HARRIS CORPORATION	P. O. BOX 883	MELBOURNE, FL 32901
50434	HEWLETT-PACKARD COMPANY	640 PAGE MILL ROAD	PALO ALTO, CA 94304
51984	NEC AMERICA INC. RADIO AND TRANSMISSION DIV.	2990 TELESTAR CT. SUITE 212	FALLS CHURCH, VA 22042
53184	XCITON CORPORATION	5 HEMLOCK STREET	LATHAM, NY 12110
54473	MATSUSHITA ELECTRIC, CORP. OF AMERICA	1 PANASONIC WAY	SECAUCUS, NJ 07094
55680	NICHICON/AMERICA/CORP.	6435 N PROESEL AVENUE	CHICAGO, IL 60645
56289	SPRAGUE ELECTRIC CO.	87 MARSHALL ST.	NORTH ADAMS, MA 01247
57668	R-OHM CORP.	16931 MILLIKEN AVE.	IRVINE, CA 92713
59660	TUSONIX INC.	2155 N FORBES BLVD	TUCSON, AZ 85705
71590	CENTRALAB ELECTRONICS, DIV. OF GLOBE-UNION, INC.	P O BOX 858	FORT DODGE, IA 50501
72982	ERIE TECHNOLOGICAL PRODUCTS, INC.	644 W. 12TH ST.	ERIE, PA 16512
73138	BECKMAN INSTRUMENTS, INC., HELIPOT DIV.	2500 HARBOR BLVD.	FULLERTON, CA 92634
74970	JOHNSON, E. F., CO.	299 10TH AVE. S. W.	WASECA, MN 56093
75042	TRW ELECTRONIC COMPONENTS, IRC FIXED RESISTORS, PHILADELPHIA DIVISION	401 N. BROAD ST.	PHILADELPHIA, PA 19108
78488	STACKPOLE CARBON CO.		ST. MARYS, PA 15857
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
91637	DALE ELECTRONICS, INC.	P. O. BOX 609	COLUMBUS, NE 68601
96733	SAN FERNANDO ELECTRIC MFG CO	1501 FIRST ST	SAN FERNANDO, CA 91341

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
				ASSEMBLIES		
A10	670-5038-00	B010100	B010156	CKT BOARD ASSY:TRIGGER	80009	670-5038-00
A10	670-5038-01	B010157	B019999	CKT BOARD ASSY:TRIGGER	80009	670-5038-01
A10	670-5038-02	B020000	B030979	CKT BOARD ASSY:TRIGGER	80009	670-5038-02
A10	670-5038-03	B030980		CKT BOARD ASSY:TRIGGER	80009	670-5038-03
A20	670-5037-00	B010100	B020454	CKT BOARD ASSY:SWEEP	80009	670-5037-00
A20	670-5037-01	B020455	B031149	CKT BOARD ASSY:SWEEP	80009	670-5037-01
A20	670-5037-02	B031150		CKT BOARD ASSY:SWEEP	80009	670-5037-02
A30	670-5041-00			CKT BOARD ASSY:SWITCH	80009	670-5041-00
A40	670-5040-00			CKT BOARD ASSY:LED	80009	670-5040-00
A50	670-5039-00	B010100	B030586	CKT BOARD ASSY:HORIZONTAL PROGRAMMING	80009	670-5039-00
A50	670-5039-01	B030587	B030761	CKT BOARD ASSY:HORIZONTAL PROGRAMMING	80009	670-5039-01
A50	670-5039-02	B030762	B030837	CKT BOARD ASSY:HORIZONTAL PROGRAMMING	80009	670-5039-02
A50	670-5039-03	B030838	B030844	CKT BOARD ASSY:HORIZONTAL PROGRAMMING	80009	670-5039-03
A50	670-5039-04	B030845	B031149	CKT BOARD ASSY:HORIZONTAL PROGRAMMING	80009	670-5039-04
A50	670-5039-05	B031150		CKT BOARD ASSY:HORIZONTAL PROGRAMMING	80009	670-5039-05
A51	670-7549-00	B030762	B030837	CKT BOARD ASSY:MEMORY ADAPTER	80009	670-7549-00
				A10 TRIGGER		
A10	670-5038-00	B010100	B010156	CKT BOARD ASSY:TRIGGER	80009	670-5038-00
A10	670-5038-01	B010157	B019999	CKT BOARD ASSY:TRIGGER	80009	670-5038-01
A10	670-5038-02	B020000	B030979	CKT BOARD ASSY:TRIGGER	80009	670-5038-02
A10	670-5038-03	B030980		CKT BOARD ASSY:TRIGGER	80009	670-5038-03
A10C020	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	1C10Z5U503Z050B
A10C022	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A10C024	283-0220-00			CAP.,FXD,CER DI:0.01UF,20%,50V	72982	8121N075X7R0103M
A10C040	283-0221-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N087X7R0474M
A10C050	290-0580-00			CAP.,FXD,ELCTLT:0.27UF,20%,50V	56289	196D274X0050HA1
A10C106	283-0728-00			CAP.,FXD,MICA D:120PF,1%,500V	00853	D155F121F0
A10C110	283-0597-00			CAP.,FXD,MICA D:470PF,10%,300V	00853	D155F471K0
A10C112	283-0594-00			CAP.,FXD,MICA D:0.001UF,1%,100V	00853	D151F102F0
A10C114	283-0698-00			CAP.,FXD,MICA D:390PF,1%,500V	09023	CD15FD391F03
A10C116	283-0641-00			CAP.,FXD,MICA D:180PF,1%,100V	00853	DD155F181F0
A10C130	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A10C132	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A10C137	283-0605-00			CAP.,FXD,MICA D:678PF,1%,300V	00853	D153F6780F0
A10C140	290-0580-00			CAP.,FXD,ELCTLT:0.27UF,20%,50V	56289	196D274X0050HA1
A10C146	283-0114-00			CAP.,FXD,CER DI:0.0015UF,5%,200V	59660	805534Y5DO152J
A10C148	283-0114-00			CAP.,FXD,CER DI:0.0015UF,5%,200V	59660	805534Y5DO152J
A10C150	283-0220-00			CAP.,FXD,CER DI:0.01UF,20%,50V	72982	8121N075X7R0103M
A10C152	283-0220-00			CAP.,FXD,CER DI:0.01UF,20%,50V	72982	8121N075X7R0103M
A10C158	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A10C214	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A10C220	283-0220-00			CAP.,FXD,CER DI:0.01UF,20%,50V	72982	8121N075X7R0103M
A10C222	283-0220-00			CAP.,FXD,CER DI:0.01UF,20%,50V	72982	8121N075X7R0103M
A10C224	283-0220-00			CAP.,FXD,CER DI:0.01UF,20%,50V	72982	8121N075X7R0103M
A10C230	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A10C236	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A10C240	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A10C250	283-0600-00			CAP.,FXD,MICA D:43PF,5%,500V	00853	D105E430J0
A10C308	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	ULA1A220TEA

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A10C312	283-0221-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N087X7R0474M
A10C320	283-0642-00			CAP.,FXD,MICA D:33PF,+/-0.5PF,300V	00853	D10-5E330G
A10C322	290-0776-00			CAP.,FXD,ELCTLT:22UF,+50-10%,10V	55680	ULA1A220TEA
A10C324	283-0597-00			CAP.,FXD,MICA D:470PF,10%,300V	00853	D155F471K0
A10C326	283-0107-00			CAP.,FXD,CER DI:51PF,5%,200V	96733	R3017
A10C336	283-0597-00			CAP.,FXD,MICA D:470PF,10%,300V	00853	D155F471K0
A10C344	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A10C346	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A10C348	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A10C350	283-0220-00			CAP.,FXD,CER DI:0.01UF,20%,50V	72982	8121N075X7R0103M
A10C360	283-0644-00	B010100	B010156	CAP.,FXD,MICA D:150PF,1%,500V	00853	D155F151F0
A10C362	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A10C400	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A10C422	283-0221-00			CAP.,FXD,CER DI:0.47UF,20%,50V	72982	8131N087X7R0474M
A10C424	283-0220-00			CAP.,FXD,CER DI:0.01UF,20%,50V	72982	8121N075X7R0103M
A10C426	283-0220-00			CAP.,FXD,CER DI:0.01UF,20%,50V	72982	8121N075X7R0103M
A10C430	283-0107-00			CAP.,FXD,CER DI:51PF,5%,200V	96733	R3017
A10C436	281-0795-00			CAP.,FXD,CER DI:9.3PF,0.1%,500V	59660	374 018 COH0939B
A10C438	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A10C440	283-0642-00			CAP.,FXD,MICA D:33PF,+/-0.5PF,300V	00853	D10-5E330G
A10C442	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A10C448	283-0616-00			CAP.,FXD,MICA D:75PF,5%,500V	00853	D155E750J0
A10C460	283-0644-00			CAP.,FXD,MICA D:150PF,1%,500V	00853	D155F151F0
A10C462	283-0060-00			CAP.,FXD,CER DI:100PF,5%,200V	59660	855-535U2J101J
A10C540	283-0693-00			CAP.,FXD,MICA D:1730PF,1%,500V	00853	D19-5F1731F0
A10CR010	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A10CR022	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A10CR050	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A10CR140	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A10CR330	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A10CR332	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A10CR334	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A10CR336	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A10CR340	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A10CR342	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A10CR344	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A10CR346	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A10CR400	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A10CR402	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A10CR460	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A10CR462	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A10CR464	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A10CR466	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A10DS348	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A10DS440	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A10J000	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A10J212	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A10J264	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A10J436	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A10LR230	108-0328-00			COIL,RF:0.3UH	80009	108-0328-00
A10LR232	108-0328-00			COIL,RF:0.3UH	80009	108-0328-00
A10LR310	108-0543-00			COIL,RF:FIXED,1.1UH	80009	108-0543-00
A10LR314	108-0543-00			COIL,RF:FIXED,1.1UH	80009	108-0543-00
A10LR320	108-0543-00			COIL,RF:FIXED,1.1UH	80009	108-0543-00
A10LR410	108-0543-00			COIL,RF:FIXED,1.1UH	80009	108-0543-00
A10P550	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
A10Q128	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A10Q134	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A10Q260	151-0325-00	B010100	B020414	TRANSISTOR:SILICON,PNP,SEL FROM 2N4258	80009	151-0325-00
A10Q260	151-0221-00	B020415		TRANSISTOR:SILICON,PNP	04713	SPS246
A10Q262	151-0325-00	B010100	B020414	TRANSISTOR:SILICON,PNP,SEL FROM 2N4258	80009	151-0325-00
A10Q262	151-0221-00	B020415		TRANSISTOR:SILICON,PNP	04713	SPS246
A10Q264	151-0325-00	B010100	B020414	TRANSISTOR:SILICON,PNP,SEL FROM 2N4258	80009	151-0325-00
A10Q264	151-0221-00	B020415	B030594	TRANSISTOR:SILICON,PNP	04713	SPS246
A10Q264	151-0342-00	B030595		TRANSISTOR:SILICON,PNP	07263	S035928
A10Q266	151-0223-00			TRANSISTOR:SILICON,NPN	04713	SPS8026
A10Q326	151-1042-00			SEMICOND DVC SE:MATCHED PAIR FET	22229	S2089
A10Q326	----- -----			(FURNISHED AS A UNIT WITH A10Q327)		
A10Q327	151-1042-00			SEMICOND DVC SE:MATCHED PAIR FET	22229	S2089
A10Q327	----- -----			(FURNISHED AS A UNIT WITH A10Q326)		
A10Q439	151-1042-00			SEMICOND DVC SE:MATCHED PAIR FET	22229	S2089
A10Q439	----- -----			(FURNISHED AS A UNIT WITH A10Q440)		
A10Q440	151-1042-00			SEMICOND DVC SE:MATCHED PAIR FET	22229	S2089
A10Q440	----- -----			(FURNISHED AS A UNIT WITH A10Q439)		
A10Q530	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A10Q532	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A10R002	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A10R010	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A10R040	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A10R042	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A10R044	321-0443-00			RES.,FXD,FILM:402K OHM,1%,0.125W	91637	CMF55116G40202F
A10R050	315-0205-00			RES.,FXD,CMPSN:2M OHM,5%,0.25W	01121	CB2055
A10R052	321-0443-00			RES.,FXD,FILM:402K OHM,1%,0.125W	91637	CMF55116G40202F
A10R100	321-0277-00			RES.,FXD,FILM:7.5K OHM,1%,0.125W	91637	MFF1816G75000F
A10R102	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A10R103	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A10R106	321-0306-00			RES.,FXD,FILM:15K OHM,1%,0.125W	91637	MFF1816G15001F
A10R110	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A10R112	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A10R114	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A10R116	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A10R120	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A10R122	321-0431-00			RES.,FXD,FILM:301K OHM,1%,0.125W	91637	MFF1816G30102F
A10R124	315-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.25W	01121	CB1315
A10R125	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A10R126	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A10R127	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A10R128	315-0151-00			RES.,FXD,CMPSN:150 OHM,5%,0.25W	01121	CB1515
A10R130	315-0124-00			RES.,FXD,CMPSN:120K OHM,5%,0.25W	01121	CB1245
A10R132	321-0274-00			RES.,FXD,FILM:6.98K OHM,1%,0.125W	91637	CMF55116G69800F

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A10R134	311-1268-00			RES.,VAR,NONWIR:10K OHM,10%,0.50W	32997	3329P-L58-103
A10R135	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A10R136	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A10R137	315-0392-00			RES.,FXD,CMPSN:3.9K OHM,5%,0.25W	01121	CB3925
A10R140	315-0205-00			RES.,FXD,CMPSN:2M OHM,5%,0.25W	01121	CB2055
A10R142	315-0182-00			RES.,FXD,CMPSN:1.8K OHM,5%,0.25W	01121	CB1825
A10R144	315-0514-00			RES.,FXD,CMPSN:510K OHM,5%,0.25W	01121	CB5145
A10R146	315-0514-00			RES.,FXD,CMPSN:510K OHM,5%,0.25W	01121	CB5145
A10R148	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A10R158	323-0155-00			RES.,FXD,FILM:402 OHM,1%,0.50W	75042	CECT0-4020F
A10R210	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A10R212	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A10R213	315-0560-00			RES.,FXD,CMPSN:56 OHM,5%,0.25W	01121	CB5605
A10R214	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A10R215	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A10R216	315-0183-00			RES.,FXD,CMPSN:18K OHM,5%,0.25W	01121	CB1835
A10R218	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A10R220	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A10R234	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A10R236	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A10R238	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
A10R240	311-1268-00			RES.,VAR,NONWIR:10K OHM,10%,0.50W	32997	3329P-L58-103
A10R243	311-1594-00			RES.,VAR,NONWIR:10 OHM,20%,0.50W	73138	91-93-0
A10R250	315-0911-00			RES.,FXD,CMPSN:910 OHM,5%,0.25W	01121	CB9115
A10R252	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A10R253	315-0181-00	B020000		RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
A10R254	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A10R256	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A10R260	321-0195-00			RES.,FXD,FILM:1.05K OHM,1%,0.125W	91637	MFF1816G10500F
A10R264	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A10R266	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A10R322	315-0822-00			RES.,FXD,CMPSN:8.2K OHM,5%,0.25W	01121	CB8225
A10R324	315-0911-00			RES.,FXD,CMPSN:910 OHM,5%,0.25W	01121	CB9115
A10R330	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A10R332	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A10R336	315-0911-00			RES.,FXD,CMPSN:910 OHM,5%,0.25W	01121	CB9115
A10R340	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A10R342	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A10R350	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A10R352	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A10R360	321-0198-00			RES.,FXD,FILM:1.13K OHM,1%,0.125W	91637	MFF1816G11300F
A10R362	321-0260-00			RES.,FXD,FILM:4.99K OHM,1%,0.125W	91637	MFF1816G49900F
A10R410	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A10R414	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A10R420	315-0820-00			RES.,FXD,CMPSN:82 OHM,5%,0.25W	01121	CB8205
A10R422	315-0560-00			RES.,FXD,CMPSN:56 OHM,5%,0.25W	01121	CB5605
A10R424	321-0452-00			RES.,FXD,FILM:499K OHM,1%,0.125W	91637	CMF55116G49902F
A10R430	315-0820-00			RES.,FXD,CMPSN:82 OHM,5%,0.25W	01121	CB8205
A10R432	315-0560-00			RES.,FXD,CMPSN:56 OHM,5%,0.25W	01121	CB5605
A10R434	321-0437-00			RES.,FXD,FILM:348K OHM,1%,0.125W	91637	CMF55116G34802F
A10R436	315-0910-00			RES.,FXD,CMPSN:91 OHM,5%,0.25W	01121	CB9105
A10R438	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A10R442	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A10R444	321-0378-00			RES.,FXD,FILM:84.5K OHM,1%,0.125W	91637	MFF1816G84501F

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A10R448	321-0397-00			RES.,FXD,FILM:133K OHM,1%,0.125W	91637	CMF55116G13302F
A10R450	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A10R452	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A10R454	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A10R460	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A10R500	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A10R522	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A10R524	311-1258-00			RES.,VAR,NONWIR:50 OHM,10%,0.50W	32997	3329P-L58-500
A10R528	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A10R530	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A10R532	311-1258-00			RES.,VAR,NONWIR:50 OHM,10%,0.50W	32997	3329P-L58-500
A10R534	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A10R536	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A10R537	315-0393-00			RES.,FXD,CMPSN:39K OHM,5%,0.25W	01121	CB3935
A10R538	315-0393-00			RES.,FXD,CMPSN:39K OHM,5%,0.25W	01121	CB3935
A10R550	321-0302-00			RES.,FXD,FILM:13.7K OHM,1%,0.125W	91637	MFF1816G13701F
A10R552	315-0683-00			RES.,FXD,CMPSN:68K OHM,5%,0.25W	01121	CB6835
A10U030	156-0158-00			MICROCIRCUIT,LI:DUAL OPERATIONAL AMPLIFIER	18324	MC1458N
A10U106	156-0509-00			MICROCIRCUIT,DI:8-BIT BINARY,MULT CUR	04713	MC1408L8
A10U112	156-0158-00			MICROCIRCUIT,LI:DUAL OPERATIONAL AMPLIFIER	18324	MC1458N
A10U150	156-0158-00			MICROCIRCUIT,LI:DUAL OPERATIONAL AMPLIFIER	18324	MC1458N
A10U220	155-0126-00			MICROCIRCUIT,LI:TRIGGER AMPLIFIER	80009	155-0126-00
A10U240	155-0109-01			MICROCIRCUIT,LI:MONOLITHIC TRIGGER	80009	155-0109-01
A10U310	156-0723-00	B010100	B030654	MICROCIRCUIT,LI:QUAD SPST ANALOG INVT SW	80009	156-0723-00
A10U310	156-0723-01	B030655		MICROCIRCUIT,LI:QUAD SPST ANALOG INVT SW	80009	156-0723-01
A10U350	156-0067-00			MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	01295	MICROA741CP
A10U358	156-0686-00	B010100	B010156	MICROCIRCUIT,LI:OPNL AMPL,HIGH IMPEDANCE	02735	CA3130S
A10U358	156-1149-00	B010157		MICROCIRCUIT,LI:OPERATIONAL AMP,JFET INPUT	27014	GLEA134
A10U410	156-0515-02			MICROCIRCUIT,DI:TRIPLE 3-CHAN MUX,SEL	80009	156-0515-02
A10U452	156-0132-00	B010100	B030979	MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	34371	HA2-911-5
A10U452	156-0770-00	B030980		MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	27014	LF356H
A10U510	156-0723-00	B010100	B030654	MICROCIRCUIT,LI:QUAD SPST ANALOG INVT SW	80009	156-0723-00
A10U510	156-0723-01	B030655		MICROCIRCUIT,LI:QUAD SPST ANALOG INVT SW	80009	156-0723-01

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				A20 SWEEP		
A20	670-5037-00	B010100	B020454	CKT BOARD ASSY:SWEEP	80009	670-5037-00
A20	670-5037-01	B020455	B031149	CKT BOARD ASSY:SWEEP	80009	670-5037-01
A20	670-5037-02	B031150		CKT BOARD ASSY:SWEEP	80009	670-5037-02
A20C030	283-0178-00			CAP.,FXD,CER DI:0.1UF,+80-20%,100V	72982	8131N145651 104Z
A20C032	283-0178-00			CAP.,FXD,CER DI:0.1UF,+80-20%,100V	72982	8131N145651 104Z
A20C033	283-0051-00	B020455		CAP.,FXD,CER DI:0.0033UF,5%,100V	56289	1C20C0G332J100B
A20C034	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A20C036	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A20C040	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A20C044	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A20C045	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A20C046	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A20C050	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A20C100	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A20C105	283-0067-00			CAP.,FXD,CER DI:0.001UF,10%,200V	59660	835-515-Z5D0102K
A20C140	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A20C156	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A20C202	283-0642-00			CAP.,FXD,MICA D:33PF,+/-0.5PF,300V	00853	D10-5E330G
A20C204	283-0616-00			CAP.,FXD,MICA D:75PF,5%,500V	00853	D155E750J0
A20C220	281-0592-00			CAP.,FXD,CER DI:4.7PF,+/-0.5PF,500V	59660	0301080COH0479 D
A20C233	281-0541-00			CAP.,FXD,CER DI:6.8PF,10%,500V	59660	301-000C0H0689D
A20C248	283-0111-00	B010100	B010156	CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A20C248	283-0220-00	B010157		CAP.,FXD,CER DI:0.01UF,20%,50V	72982	8121N075X7R0103M
A20C252	281-0541-00			CAP.,FXD,CER DI:6.8PF,10%,500V	59660	301-000C0H0689D
A20C300	283-0594-00			CAP.,FXD,MICA D:0.001UF,1%,100V	00853	D151F102F0
A20C302	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A20C304	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A20C310	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A20C312	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A20C340	283-0060-00			CAP.,FXD,CER DI:100PF,5%,200V	59660	855-535U2J101J
A20C352	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A20C358	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A20C404	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A20C410	295-0187-00			CAP SET,MATCHED:(1)EA 10UF,0.1UF,900PF	80009	295-0187-00
A20C412	----- -----			(PART OF C410)		
A20C420	----- -----			(PART OF C410)		
A20C446	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A20C448	283-0220-00			CAP.,FXD,CER DI:0.01UF,20%,50V	72982	8121N075X7R0103M
A20C500	281-0166-00			CAP.,VAR,AIR DI:1.9-15.7PF,250V	74970	187-0109-055
A20C504	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A20C510	283-0629-00	B010100	B031149	CAP.,FXD,MICA D:62PF,1%,500V	00853	D105E620F0
A20C510	283-0639-00	B031150		CAP.,FXD,MICA D:56PF,1%,100V	00853	D151E560F0
A20C512	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A20C530	283-0597-00			CAP.,FXD,MICA D:470PF,10%,300V	00853	D155F471K0
A20C538	283-0648-00			CAP.,FXD,MICA D:10PF,5%,100V	00853	D151C100D0
A20C540	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A20C544	283-0644-00			CAP.,FXD,MICA D:150PF,1%,500V	00853	D155F151F0
A20C608	290-0267-00			CAP.,FXD,ELCTLT:1UF,20%,35V	56289	173D105X0035V
A20C612	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A20C614	283-0599-00			CAP.,FXD,MICA D:98PF,5%,500V	00853	D105F980J0
A20C620	290-0282-00			CAP.,FXD,ELCTLT:0.047UF,10%,35V	56289	162D473X9035BC2

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A20C622	283-0695-00			CAP.,FXD,MICA D:4440PF,1%,300V	00853	D195F4441F0
A20C626	290-0244-00			CAP.,FXD,ELCTLT:0.47UF,5%,35V	56289	173D474X5035U
A20C640	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A20C644	283-0698-00			CAP.,FXD,MICA D:390PF,1%,500V	09023	CD15FD391F03
A20C650	290-0267-00			CAP.,FXD,ELCTLT:1UF,20%,35V	56289	173D105X0035V
A20C654	283-0648-00			CAP.,FXD,MICA D:10PF,5%,100V	00853	D151C100D0
A20C656	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A20C730	290-0284-00			CAP.,FXD,ELCTLT:4.7UF,10%,35V	56289	150D475X9035B2
A20C750	290-0267-00			CAP.,FXD,ELCTLT:1UF,20%,35V	56289	173D105X0035V
A20C844	283-0111-00			CAP.,FXD,CER DI:0.1UF,20%,50V	96733	R2632
A20CR138	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20CR152	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A20CR154	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20CR204	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20CR206	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20CR222	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20CR242	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20CR310	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20CR406	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A20CR450	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20CR452	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20CR454	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20CR544	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20CR550	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20CR600	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20CR602	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20CR610	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20CR732	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A20CR834	152-0075-00			SEMICOND DEVICE:SW,GE,22V,40MA	14433	G866
A20CR850	152-0075-00			SEMICOND DEVICE:SW,GE,22V,40MA	14433	G866
A20CR954	152-0075-00			SEMICOND DEVICE:SW,GE,22V,40MA	14433	G866
A20DS001	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A20DS008	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A20E148	276-0507-00			SHIELDING BEAD,:FERRITE	78488	57-3443
A20E150	276-0507-00			SHIELDING BEAD,:FERRITE	78488	57-3443
A20J020	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A20J022	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A20J304	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A20L122	108-0509-00			COIL,RF:2.45UH	80009	108-0509-00
A20LR032	108-0537-00			COIL,RF:200UH	80009	108-0537-00
A20LR034	108-0537-00			COIL,RF:200UH	80009	108-0537-00
A20LR040	108-0537-00			COIL,RF:200UH	80009	108-0537-00
A20LR046	108-0537-00			COIL,RF:200UH	80009	108-0537-00
A20LR050	108-0537-00			COIL,RF:200UH	80009	108-0537-00
A20LR512	108-0271-00			COIL,RF:0.235NH	80009	108-0271-00
A20P028	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A20Q120	151-0325-00	B010100	B020414	TRANSISTOR:SILICON,PNP,SEL FROM 2N4258	80009	151-0325-00
A20Q120	151-0221-00	B020415		TRANSISTOR:SILICON,PNP	04713	SPS246
A20Q130	151-0472-00			TRANSISTOR:SILICON,NPN	51984	NE41632B
A20Q132	151-0472-00			TRANSISTOR:SILICON,NPN	51984	NE41632B
A20Q134	151-1113-00			TRANSISTOR:FE,N CHANNEL,SILICON	80009	151-1113-00
A20Q142	151-0192-00			TRANSISTOR:SILICON,NPN,SEL FROM MPS652	04713	SPS8801
A20Q144	151-0223-00			TRANSISTOR:SILICON,NPN	04713	SPS8026
A20Q146	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A20Q148	151-0325-00	B010100	B020414	TRANSISTOR:SILICON,PNP,SEL FROM 2N4258	80009	151-0325-00
A20Q148	151-0221-00	B020415		TRANSISTOR:SILICON,PNP	04713	SPS246
A20Q150	151-0223-00			TRANSISTOR:SILICON,NPN	04713	SPS8026
A20Q220	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A20Q222	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A20Q224	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A20Q234	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A20Q236	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A20Q242	151-0325-00	B010100	B020414	TRANSISTOR:SILICON,PNP,SEL FROM 2N4258	80009	151-0325-00
A20Q242	151-0221-00	B020415		TRANSISTOR:SILICON,PNP	04713	SPS246
A20Q250	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A20Q252	151-0223-00			TRANSISTOR:SILICON,NPN	04713	SPS8026
A20Q300	151-0354-00			TRANSISTOR:SILICON,PNP,DUAL	32293	ITS1200A
A20Q312	151-0223-00			TRANSISTOR:SILICON,NPN	04713	SPS8026
A20Q314	151-0223-00			TRANSISTOR:SILICON,NPN	04713	SPS8026
A20Q320	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A20Q324	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A20Q354	151-0301-00			TRANSISTOR:SILICON,PNP	27014	2N2907A
A20Q356	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A20Q400	151-0367-00			TRANSISTOR:SILICON,NPN,SEL FROM 3571TP	04713	SPS 8811
A20Q406	151-0367-00			TRANSISTOR:SILICON,NPN,SEL FROM 3571TP	04713	SPS 8811
A20Q410	151-0223-00			TRANSISTOR:SILICON,NPN	04713	SPS8026
A20Q512	151-0410-00			TRANSISTOR:SILICON,PNP	80009	151-0410-00
A20Q516	151-1036-00			TRANSISTOR:SILICON,JFE,N-CHANNEL,DUAL	17856	DN1663
A20Q542	151-0223-00			TRANSISTOR:SILICON,NPN	04713	SPS8026
A20Q544	151-0223-00			TRANSISTOR:SILICON,NPN	04713	SPS8026
A20Q546	151-0325-00	B010100	B020414	TRANSISTOR:SILICON,PNP,SEL FROM 2N4258	80009	151-0325-00
A20Q546	151-0221-00	B020415		TRANSISTOR:SILICON,PNP	04713	SPS246
A20Q552	151-0325-00	B010100	B020414	TRANSISTOR:SILICON,PNP,SEL FROM 2N4258	80009	151-0325-00
A20Q552	151-0221-00	B010415		TRANSISTOR:SILICON,PNP	04713	SPS246
A20Q558	151-0223-00			TRANSISTOR:SILICON,NPN	04713	SPS8026
A20Q604	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A20Q620	151-0437-00			TRANSISTOR:SILICON,NPN,SEL FROM 2N5769	80009	151-0437-00
A20Q646	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A20Q648	151-0223-00			TRANSISTOR:SILICON,NPN	04713	SPS8026
A20Q732	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A20Q740	151-0223-00			TRANSISTOR:SILICON,NPN	04713	SPS8026
A20Q748	151-0220-00			TRANSISTOR:SILICON,PNP	07263	S036228
A20R002	315-0512-00			RES.,FXD,CMPSN:5.1K OHM,5%,0.25W	01121	CB5125
A20R004	321-0385-04			RES.,FXD,FILM:100K OHM,0.1%,0.125W	91637	MFF1816D10002B
A20R034	322-0224-00			RES.,FXD,FILM:2.15K OHM,1%,0.25W	91637	CMF6042G29400F
A20R054	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A20R100	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A20R101	321-0385-04			RES.,FXD,FILM:100K OHM,0.1%,0.125W	91637	MFF1816D10002B
A20R102	321-0756-04			RES.,FXD,FILM:50K OHM,0.1%,0.125W	91637	MFF1816D50001B

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A20R103	321-0332-00			RES.,FXD,FILM:28K OHM,1%,0.125W	91637	MFF1816G28001F
A20R104	321-0258-00			RES.,FXD,FILM:4.75K OHM,1%,0.125W	91637	MFF1816G47500F
A20R105	321-0238-00			RES.,FXD,FILM:2.94K OHM,1%,0.125W	91637	MFF1816G29400F
A20R106	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A20R107	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A20R108	321-0773-03			RES.,FXD,FILM:400 OHM,0.25%,0.125W	91637	MFF1816D400R0C
A20R116	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A20R118	321-0210-00			RES.,FXD,FILM:1.5K OHM,1%,0.125W	91637	MFF1816G15000F
A20R120	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735
A20R121	323-0243-00			RES.,FXD,FILM:3.32K OHM,1%,0.50W	91637	MFF1226G33200F
A20R122	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
A20R123	321-0134-00			RES.,FXD,FILM:243 OHM,1%,0.125W	91637	MFF1816G243R0F
A20R126	321-0054-00			RES.,FXD,FILM:35.7 OHM,5%,0.125W	91637	MFF1816G35R70F
A20R128	315-0270-00			RES.,FXD,CMPSN:27 OHM,5%,0.25W	01121	CB2705
A20R130	322-0224-00			RES.,FXD,FILM:2.15K OHM,1%,0.25W	91637	CMF6042G29400F
A20R131	321-0134-00			RES.,FXD,FILM:243 OHM,1%,0.125W	91637	MFF1816G243R0F
A20R132	315-0393-00			RES.,FXD,CMPSN:39K OHM,5%,0.25W	01121	CB3935
A20R133	321-0072-00			RES.,FXD,FILM:54.9 OHM,1%,0.125W	91637	MFF1816G54R90F
A20R134	321-0072-00			RES.,FXD,FILM:54.9 OHM,1%,0.125W	91637	MFF1816G54R90F
A20R134	321-0054-00			RES.,FXD,FILM:35.7 OHM,5%,0.125W	91637	MFF1816G35R70F
A20R136	315-0105-00			RES.,FXD,CMPSN:1M OHM,5%,0.25W	01121	CB1055
A20R138	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	01121	CB3035
A20R140	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A20R142	315-0270-00			RES.,FXD,CMPSN:27 OHM,5%,0.25W	01121	CB2705
A20R143	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R144	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A20R145	315-0303-00			RES.,FXD,CMPSN:30K OHM,5%,0.25W	01121	CB3035
A20R146	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A20R148	315-0332-00			RES.,FXD,CMPSN:3.3K OHM,5%,0.25W	01121	CB3325
A20R150	321-0173-00			RES.,FXD,FILM:619 OHM,1%,0.125W	91637	MFF1816G619R0F
A20R152	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A20R156	315-0132-00			RES.,FXD,CMPSN:1.3K OHM,5%,0.25W	01121	CB1325
A20R200	321-0781-06			RES.,FXD,FILM:400K OHM,0.25%,0.125W	91637	MFF1816C40002C
A20R202	321-0924-07			RES.,FXD,FILM:40K OHM,0.1%,0.125W	91637	MFF1816C40001B
A20R203	321-0926-07			RES.,FXD,FILM:4K OHM,0.1%,0.125W	91637	MFF1816C40000B
A20R204	321-0275-00			RES.,FXD,FILM:7.15K OHM,1%,0.125W	91637	MFF1816G71500F
A20R206	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A20R207	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R208	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A20R210	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A20R212	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A20R220	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A20R221	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A20R222	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A20R223	315-0112-00			RES.,FXD,CMPSN:1.1K OHM,5%,0.25W	01121	CB1125
A20R224	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A20R226	315-0511-00			RES.,FXD,CMPSN:510 OHM,5%,0.25W	01121	CB5115
A20R227	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A20R228	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	01121	ORD BY DESCR
A20R230	323-0187-00			RES.,FXD,FILM:866 OHM,1%,0.50W	75042	CECT0-8660F
A20R232	311-1423-00			RES.,VAR,NONWIR:20 OHM,20%,0.50W	73138	72PM R20-1A
A20R233	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A20R234	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	01121	ORD BY DESCR
A20R235	321-0122-00			RES.,FXD,FILM:182 OHM,1%,0.125W	91637	MFF1816G182R0F

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A20R236	321-0356-00			RES.,FXD,FILM:49.9K OHM,1%,0.125W	91637	MFF1816G49901F
A20R237	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	01121	ORD BY DESCR
A20R238	311-1226-00			RES.,VAR,NONWIR:2.5K OHM,20%,0.50W	32997	3386F-T04-252
A20R240	311-1228-00			RES.,VAR,NONWIR:10K OHM,20%,0.50W	32997	3386F-T04-103
A20R241	315-0682-00			RES.,FXD,CMPSN:6.8K OHM,5%,0.25W	01121	CB6825
A20R242	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A20R243	315-0270-00			RES.,FXD,CMPSN:27 OHM,5%,0.25W	01121	CB2705
A20R244	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735
A20R246	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A20R248	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A20R250	321-0210-00			RES.,FXD,FILM:1.5K OHM,1%,0.125W	91637	MFF1816G15000F
A20R252	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A20R253	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A20R254	315-0302-00			RES.,FXD,CMPSN:3K OHM,5%,0.25W	01121	CB3025
A20R255	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A20R256	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A20R257	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A20R258	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A20R300	323-0172-00			RES.,FXD,FILM:604 OHM,1%,0.50W	91637	MFF1226G604R0F
A20R302	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A20R310	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R312	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R314	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R320	315-0152-00			RES.,FXD,CMPSN:1.5K OHM,5%,0.25W	01121	CB1525
A20R330	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	01121	ORD BY DESCR
A20R340	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A20R341	315-0122-00			RES.,FXD,CMPSN:1.2K OHM,5%,0.25W	01121	CB1225
A20R342	311-1266-00			RES.,VAR,NONWIR:2.5K OHM,10%,0.50W	32997	3329P-L58-252
A20R343	321-0178-00			RES.,FXD,FILM:698 OHM,1%,0.125W	91637	MFF1816G698R0F
A20R344	321-0188-00			RES.,FXD,FILM:887 OHM,1%,0.125W	91637	MFF1816G887R0F
A20R346	321-0271-00			RES.,FXD,FILM:6.49K OHM,1%,0.125W	91637	MFF1816G64900F
A20R350	315-0430-00			RES.,FXD,CMPSN:43 OHM,5%,0.25W	01121	CB4305
A20R352	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A20R354	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R356	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A20R357	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A20R358	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A20R400	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A20R402	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A20R404	315-0100-00			RES.,FXD,CMPSN:10 OHM,5%,0.25W	01121	CB1005
A20R405	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R406	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A20R410	307-0114-00			RES.,FXD,CMPSN:6.2 OHM,5%,0.25W	01121	CB62G5
A20R412	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R430	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	01121	ORD BY DESCR
A20R432	321-0193-00			RES.,FXD,FILM:1K OHM,1%,0.125W	01121	ORD BY DESCR
A20R440	315-0393-00			RES.,FXD,CMPSN:39K OHM,5%,0.25W	01121	CB3935
A20R442	321-0231-00			RES.,FXD,FILM:2.49K OHM,1%,0.125W	91637	MFF1816G24900F
A20R444	321-0175-00			RES.,FXD,FILM:649 OHM,1%,0.125W	91637	CMF55116G649R0F
A20R446	321-0280-00			RES.,FXD,FILM:8.06K OHM,1%,0.125W	91637	MFF1816G80600F
A20R454	315-0622-00			RES.,FXD,CMPSN:6.2K OHM,5%,0.25W	01121	CB6225
A20R502	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A20R505	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A20R506	315-0180-00			RES.,FXD,CMPSN:18 OHM,5%,0.25W	01121	CB1805

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A20R512	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A20R514	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A20R516	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A20R520	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A20R522	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A20R524	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A20R526	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A20R530	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R534	321-0168-00			RES.,FXD,FILM:549 OHM,1%,0.125W	91637	MFF1816G549R0F
A20R536	321-0235-00			RES.,FXD,FILM:2.74K OHM,1%,0.125W	91637	MFF1816G27400F
A20R540	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A20R542	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A20R543	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A20R544	321-0239-00			RES.,FXD,FILM:3.01K OHM,1%,0.125W	91637	MFF1816G30100F
A20R546	315-0162-00			RES.,FXD,CMPSN:1.6K OHM,5%,0.25W	01121	CB1625
A20R547	315-0432-00			RES.,FXD,CMPSN:4.3K OHM,5%,0.25W	01121	CB4325
A20R548	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A20R549	315-0821-00			RES.,FXD,CMPSN:820 OHM,5%,0.25W	01121	CB8215
A20R550	315-0223-00			RES.,FXD,CMPSN:22K OHM,5%,0.25W	01121	CB2235
A20R554	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R556	315-0202-00			RES.,FXD,CMPSN:2K OHM,5%,0.25W	01121	CB2025
A20R558	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R600	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A20R602	321-0301-00			RES.,FXD,FILM:13.3K OHM,1%,0.125W	91637	MFF1816G13301F
A20R610	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A20R614	315-0272-00			RES.,FXD,CMPSN:2.7K OHM,5%,0.25W	01121	CB2725
A20R616	321-0202-00			RES.,FXD,FILM:1.24K OHM,1%,0.125W	91637	MFF1816G12400F
A20R622	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A20R640	315-0391-00			RES.,FXD,CMPSN:390 OHM,5%,0.25W	01121	CB3915
A20R642	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R650	315-0184-00			RES.,FXD,CMPSN:180K OHM,5%,0.25W	01121	CB1845
A20R652	321-0256-00			RES.,FXD,FILM:4.53K OHM,1%,0.125W	91637	MFF1816G45300F
A20R656	321-0256-00			RES.,FXD,FILM:4.53K OHM,1%,0.125W	91637	MFF1816G45300F
A20R710	321-0202-00			RES.,FXD,FILM:1.24K OHM,1%,0.125W	91637	MFF1816G12400F
A20R730	321-0257-00			RES.,FXD,FILM:4.64K OHM,1%,0.125W	91637	MFF1816G46400F
A20R732	315-0431-00			RES.,FXD,CMPSN:430 OHM,5%,0.25W	01121	CB4315
A20R740	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A20R742	321-0807-00			RES.,FXD,FILM:900K OHM,1%,0.125W	91637	CMF55116G90000F
A20R744	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A20R746	321-0263-00			RES.,FXD,FILM:5.36K OHM,1%,0.125W	91637	MFF1816G53600F
A20R747	315-0474-00			RES.,FXD,CMPSN:470K OHM,5%,0.25W	01121	CB4745
A20R748	315-0242-00			RES.,FXD,CMPSN:2.4K OHM,5%,0.25W	01121	CB2425
A20R750	321-0377-00			RES.,FXD,FILM:82.5K OHM,1%,0.125W	91637	MFF1816G82501F
A20R752	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A20R754	315-0752-00			RES.,FXD,CMPSN:7.5K OHM,5%,0.25W	01121	CB7525
A20R758	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
A20R814	321-0340-00			RES.,FXD,FILM:34K OHM,1%,0.125W	91637	CMF55116G34001F
A20R830	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A20R832	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A20R834	315-0153-00			RES.,FXD,CMPSN:15K OHM,5%,0.25W	01121	CB1535
A20R836	321-0333-00			RES.,FXD,FILM:28.7K OHM,1%,0.125W	91637	CMF55116G28701F
A20R838	321-0289-00			RES.,FXD,FILM:10K OHM,1%,0.125W	91637	MFF1816G10001F
A20R840	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A20R842	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A20R850	321-0335-00			RES.,FXD,FILM:30.1K OHM,1%,0.125W	91637	CMF55116G30101F
A20R852	321-0349-00			RES.,FXD,FILM:42.2K OHM,1%,0.125W	91637	MFF1816G42201F
A20R854	315-0910-00			RES.,FXD,CMPSN:91 OHM,5%,0.25W	01121	CB9105
A20R930	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A20R932	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A20R936	315-0150-00			RES.,FXD,CMPSN:15 OHM,5%,0.25W	01121	CB1505
A20R944	315-0470-00			RES.,FXD,CMPSN:47 OHM,5%,0.25W	01121	CB4705
A20R950	315-0155-00			RES.,FXD,CMPSN:1.5M OHM,5%,0.25W	01121	CB1555
A20R952	321-0308-00			RES.,FXD,FILM:15.8K OHM,1%,0.125W	91637	MFF1816G15801F
A20R956	321-0340-00			RES.,FXD,FILM:34K OHM,1%,0.125W	91637	CMF55116G34001F
A20T028	120-0444-00			XFMR,TOROID:5 TURNS,BIFILAR	80009	120-0444-00
A20U020	156-0846-00			MICROCIRCUIT,LI:VOLTAGE REGULATOR	04713	MC7905CT
A20U110	156-0197-00			MICROCIRCUIT,LI:5 TRANSISTOR ARRAY	02735	CA3086
A20U116	156-0512-00			MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	27014	LM308N
A20U212	156-0514-02			MICROCIRCUIT,DI:DIFF 4 CHANNEL MUX,SEL	80009	156-0514-02
A20U320	156-0140-02			MICROCIRCUIT,DI:HEX BUFFERS W/OC HV OUT	01295	SN7417 (NP3)
A20U330	156-0927-00			MICROCIRCUIT,LI:DIGITAL TO ANALOG CONVERTER	80009	156-0927-00
A20U340	156-0067-00			MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	01295	MICROA741CP
A20U430	156-0515-02			MICROCIRCUIT,DI:TRIPLE 3-CHAN MUX,SEL	80009	156-0515-02
A20U448	155-0049-02			MICROCIRCUIT,DI:SWEEP CONTROL,W/LOCKOUT	80009	155-0049-02
A20U530	156-0251-00			MICROCIRCUIT,DI:VOLTAGE COMPENSATOR	27014	LM361H
A20U630	156-0513-02			MICROCIRCUIT,DI:8-CHANNEL MUX,SEL	80009	156-0513-02
A20U644	156-0096-00			MICROCIRCUIT,LI:VOLTAGE COMPARATOR	27014	LM311H
A20U654	156-0067-00			MICROCIRCUIT,LI:OPERATIONAL AMPLIFIER	01295	MICROA741CP
A20U710	156-0509-00			MICROCIRCUIT,DI:8-BIT BINARY,MULT CUR	04713	MC1408L8
A20U800	156-0140-02			MICROCIRCUIT,DI:HEX BUFFERS W/OC HV OUT	01295	SN7417 (NP3)
A20U820	156-0140-02			MICROCIRCUIT,DI:HEX BUFFERS W/OC HV OUT	01295	SN7417 (NP3)
A20U840	156-0411-00			MICROCIRCUIT,LI:QUAD-COMP,SGL SUPPLY	27014	LM339N
A20U900	156-0093-02			MICROCIRCUIT,DI:HEX INV BUFFER,BURN-IN	01295	SN74LS00 (NP3)
A20U910	156-0140-02			MICROCIRCUIT,DI:HEX BUFFERS W/OC HV OUT	01295	SN7417 (NP3)
A20U920	156-0140-02			MICROCIRCUIT,DI:HEX BUFFERS W/OC HV OUT	01295	SN7417 (NP3)
A20U940	156-0411-00			MICROCIRCUIT,LI:QUAD-COMP,SGL SUPPLY	27014	LM339N
A20VR210	152-0281-00			SEMICOND DEVICE:ZENER,0.4W,22V,5%	12954	1N969B
A20VR430	152-0195-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZ11755
A20VR434	152-0195-00			SEMICOND DEVICE:ZENER,0.4W,5.1V,5%	04713	SZ11755
A20VR532	152-0127-00			SEMICOND DEVICE:ZENER,0.4W,7.5V,5%	04713	SZG35009K2

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
				A30 SWITCH		
A30	670-5041-00			CKT BOARD ASSY:SWITCH	80009	670-5041-00
A30DS020	150-1029-00			LT EMITTING DIO:GREEN,565NM,35MA	53184	XC209G
A30DS120	150-1033-00			LT EMITTING DIO:AMBER,585NM,40MA MAX	50434	HLMP 1401
A30R020	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A30R114	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A30S002	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S004	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S010	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S012	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S014	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S016	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S020	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S100	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S102	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S110	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S112	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S114	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S120	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S200	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S202	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S204	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S210	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S212	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S214	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S220	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S222	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S224	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S300	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S310	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S312	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00
A30S320	263-0020-00			SWITCH,PB ASSY:MOMENTARY	80009	263-0020-00

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
				A40 LED		
A40	670-5040-00			CKT BOARD ASSY:LED	80009	670-5040-00
A40DS002	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS004	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS010	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS012	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS014	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS016	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS020	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS100	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS102	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS110	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS112	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS114	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS120	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS124	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS200	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS202	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS204	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS210	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS212	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS220	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS222	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS224	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS300	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS310	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS312	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40DS320	150-1036-00			LAMP,LED:RED,3.0V,40MA	01295	TIL 209A
A40J120	131-1228-01			CONN,RCPT,ELEC:CKT BD,30/60 CONTACT	80009	131-1228-01
A40J300	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A40R002	315-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.25W	01121	CB1315
A40R010	315-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.25W	01121	CB1315
A40R030	311-1845-00			RES.,VAR,NONWIR:PNL,5K OHM,0.50W	01121	W8355
A40R102	315-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.25W	01121	CB1315
A40R120	315-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.25W	01121	CB1315
A40R130	311-1845-00			RES.,VAR,NONWIR:PNL,5K OHM,0.50W	01121	W8355
A40R220	315-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.25W	01121	CB1315
A40R300	315-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.25W	01121	CB1315
A40R310	315-0131-00			RES.,FXD,CMPSN:130 OHM,5%,0.25W	01121	CB1315
A40R312	311-1954-00			RES.,VAR,NONWIR:CKT BD,1K OHM,20%,0.25W	12697	CM41724
A40R330	315-0241-00			RES.,FXD,CMPSN:240 OHM,5%,0.25W	01121	CB2415
A40R334	311-1845-00			RES.,VAR,NONWIR:PNL,5K OHM,0.50W	01121	W8355

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
				A50 HORIZONTAL PROGRAMMING		
A50	670-5039-00	B010100	B030586	CKT BOARD ASSY:HORIZONTAL PROGRAMMING	80009	670-5039-00
A50	670-5039-01	B030587	B030761	CKT BOARD ASSY:HORIZONTAL PROGRAMMING	80009	670-5039-01
A50	670-5039-02	B030762	B030837	CKT BOARD ASSY:HORIZONTAL PROGRAMMING	80009	670-5039-02
A50	670-5039-03	B030838	B030844	CKT BOARD ASSY:HORIZONTAL PROGRAMMING	80009	670-5039-03
A50	670-5039-04	B030845	B031149	CKT BOARD ASSY:HORIZONTAL PROGRAMMING	80009	670-5039-04
A50	670-5039-05	B031150		CKT BOARD ASSY:HORIZONTAL PROGRAMMING	80009	670-5039-05
A50C000	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	1C10Z5U503Z050B
A50C020	283-0644-00			CAP.,FXD,MICA D:150PF,1%,500V	00853	D155F151F0
A50C024	283-0060-00			CAP.,FXD,CER DI:100PF,5%,200V	59660	855-535U2J101J
A50C030	283-0644-00			CAP.,FXD,MICA D:150PF,1%,500V	00853	D155F151F0
A50C032	283-0060-00			CAP.,FXD,CER DI:100PF,5%,200V	59660	855-535U2J101J
A50C100	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	1C10Z5U503Z050B
A50C220	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	1C10Z5U503Z050B
A50C410	283-0032-00			CAP.,FXD,CER DI:470PF,5%,500V	59660	0831085Z5E00471J
A50C420	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	1C10Z5U503Z050B
A50C528	283-0032-00			CAP.,FXD,CER DI:470PF,5%,500V	59660	0831085Z5E00471J
A50C530	283-0010-00	B010100	B030837	CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	1C10Z5U503Z050B
A50C628	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	1C10Z5U503Z050B
A50C728	283-0010-00	B010100	B030837	CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	1C10Z5U503Z050B
A50C800	283-0000-00			CAP.,FXD,CER DI:0.001UF,+100-0%,500V	59660	831610Y5U0102P
A50C1020	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	1C10Z5U503Z050B
A50C1100	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	1C10Z5U503Z050B
A50C1106	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	1C10Z5U503Z050B
A50C1120	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	1C10Z5U503Z050B
A50C1300	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	1C10Z5U503Z050B
A50C1400	283-0060-00			CAP.,FXD,CER DI:100PF,5%,200V	59660	855-535U2J101J
A50C1516	290-0746-00			CAP.,FXD,ELCTLT:47UF,+50-10%,16V	55680	ULA1C470TEA
A50C1518	283-0000-00			CAP.,FXD,CER DI:0.001UF,+100-0%,500V	59660	831610Y5U0102P
A50C1520	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	1C10Z5U503Z050B
A50C1530	283-0119-00			CAP.,FXD,CER DI:2200PF,5%,200V	59660	855-536Y5E0222J
A50C1620	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A50C1622	290-0745-00			CAP.,FXD,ELCTLT:22UF,+50-10%,25V	54473	ECE-A25V22L
A50C1630	283-0119-00	B010100	B030586	CAP.,FXD,CER DI:2200PF,5%,200V	59660	855-536Y5E0222J
A50C1630	283-0032-00	B030587		CAP.,FXD,CER DI:470PF,5%,500V	59660	0831085Z5E00471J
A50C1720	290-0746-00	B010100	B030837	CAP.,FXD,ELCTLT:47UF,+50-10%,16V	55680	ULA1C470TEA
A50C1730	283-0010-00			CAP.,FXD,CER DI:0.05UF,+100-20%,50V	56289	1C10Z5U503Z050B
A50CR234	152-0075-00	B010100	B030837	SEMICOND DEVICE:SW,GE,22V,40MA	14433	G866
A50CR800	152-0322-00			SEMICOND DEVICE:SILICON,15V,HOT CARRIER	50434	5082-2672
A50CR1310	152-0141-02			SEMICOND DEVICE:SILICON,30V,150MA	01295	1N4152R
A50E730	276-0507-00	B010100	B030837	SHIELDING BEAD,:FERRITE	78488	57-3443
A50LR1310	108-0543-00			COIL,RF:FIXED,1.1UH	80009	108-0543-00
A50LR1612	108-0537-00			COIL,RF:200UH	80009	108-0537-00
A50LR1614	108-0543-00			COIL,RF:FIXED,1.1UH	80009	108-0543-00
A50LR1616	108-0543-00			COIL,RF:FIXED,1.1UH	80009	108-0543-00
A50P130	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
A50P232	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
A50P1526	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A50Q126	151-0216-00			TRANSISTOR:SILICON,PNP	04713	SPS8803
A50Q135	151-0216-00			TRANSISTOR:SILICON,PNP	04713	SPS8803
A50Q730	151-0190-00	B010100	B030837	TRANSISTOR:SILICON,NPN	07263	S032677
A50Q904	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A50Q1304	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A50Q1308	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A50Q1310	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A50Q1404	151-0190-00			TRANSISTOR:SILICON,NPN	07263	S032677
A50Q1412	151-0216-00			TRANSISTOR:SILICON,PNP	04713	SPS8803
A50Q1514	151-0221-00			TRANSISTOR:SILICON,PNP	04713	SPS246
A50R020	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A50R022	311-1267-00			RES.,VAR,NONWIR:5K OHM,10%,0.50W	32997	3329P-L58-502
A50R024	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A50R030	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A50R032	311-1267-00			RES.,VAR,NONWIR:5K OHM,10%,0.50W	32997	3329P-L58-502
A50R034	315-0221-00			RES.,FXD,CMPSN:220 OHM,5%,0.25W	01121	CB2215
A50R120	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R122	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R124	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A50R126	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R130	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R132	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R134	315-0220-00			RES.,FXD,CMPSN:22 OHM,5%,0.25W	01121	CB2205
A50R136	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A50R220	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R230	321-0324-00	B010100	B030837	RES.,FXD,FILM:23.2K OHM,1%,0.125W	91637	MFF1816G23201F
A50R232	321-0705-00	B010100	B030837	RES.,FXD,FILM:41.7K OHM,1%,0.125W	91637	MFF1816G41701F
A50R234	321-0341-00			RES.,FXD,FILM:34.8K OHM,1%,0.125W	91637	CMF55116G34801F
A50R235	321-0354-00			RES.,FXD,FILM:47.5K OHM,1%,0.125W	91637	CMF55116G47501F
A50R332	315-0681-00			RES.,FXD,CMPSN:680 OHM,5%,0.25W	01121	CB6815
A50R334	321-0378-00	B010100	B030837	RES.,FXD,FILM:84.5K OHM,1%,0.125W	91637	MFF1816G84501F
A50R336	321-0334-00	B010100	B030837	RES.,FXD,FILM:29.4K OHM,1%,0.125W	91637	MFF1816G29401F
A50R410	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A50R430	315-0104-00			RES.,FXD,CMPSN:100K OHM,5%,0.25W	01121	CB1045
A50R530	315-0331-00			RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A50R532	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A50R534	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A50R536	315-0433-00			RES.,FXD,CMPSN:43K OHM,5%,0.25W	01121	CB4335
A50R538	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A50R539	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R730	315-0102-00	B010100	B010160	RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R730	315-0331-00	B010161	B030837	RES.,FXD,CMPSN:330 OHM,5%,0.25W	01121	CB3315
A50R800	321-0344-00			RES.,FXD,FILM:37.4K OHM,1%,0.125W	91637	MFF1816G37401F
A50R810	315-0473-00			RES.,FXD,CMPSN:47K OHM,5%,0.25W	01121	CB4735
A50R812	315-0683-00			RES.,FXD,CMPSN:68K OHM,5%,0.25W	01121	CB6835
A50R900	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R1102	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R1104	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R1200	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R1204	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R1206	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R1220	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A50R1300	315-0753-00			RES.,FXD,CMPSN:75K OHM,5%,0.25W	01121	CB7535

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A50R1302	315-0154-00			RES.,FXD,CMPSN:150K OHM,5%,0.25W	01121	CB1545
A50R1304	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A50R1306	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A50R1310	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A50R1400	321-0344-00			RES.,FXD,FILM:37.4K OHM,1%,0.125W	91637	MFF1816G37401F
A50R1402	315-0753-00			RES.,FXD,CMPSN:75K OHM,5%,0.25W	01121	CB7535
A50R1404	315-0513-00			RES.,FXD,CMPSN:51K OHM,5%,0.25W	01121	CB5135
A50R1406	315-0222-00			RES.,FXD,CMPSN:2.2K OHM,5%,0.25W	01121	CB2225
A50R1408	315-0154-00			RES.,FXD,CMPSN:150K OHM,5%,0.25W	01121	CB1545
A50R1410	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R1412	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A50R1514	315-0472-00			RES.,FXD,CMPSN:4.7K OHM,5%,0.25W	01121	CB4725
A50R1526	315-0103-00			RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A50R1532	315-0203-00			RES.,FXD,CMPSN:20K OHM,5%,0.25W	01121	CB2035
A50R1620	315-0101-00			RES.,FXD,CMPSN:100 OHM,5%,0.25W	01121	CB1015
A50R1630	315-0133-00	B010100	B030586	RES.,FXD,CMPSN:13K OHM,5%,0.25W	01121	CB1335
A50R1630	315-0103-00	B030587		RES.,FXD,CMPSN:10K OHM,5%,0.25W	01121	CB1035
A50R1730	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50R1732	315-0102-00			RES.,FXD,CMPSN:1K OHM,5%,0.25W	01121	CB1025
A50U000	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A50U010	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A50U030	156-0733-02			MICROCIRCUIT,DI:DUAL MONOSTABLE MV,SCRN	01295	SN74LS221N3
A50U100	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A50U110	156-0736-02			MICROCIRCUIT,DI:BCD TO DECIMAL DCDR	80009	156-0736-02
A50U200	156-0541-02			MICROCIRCUIT,DI:DUAL 2 TO 4 LINE DCDR	01295	SN74LS139NP3
A50U230	156-0093-02			MICROCIRCUIT,DI:HEX INV BUFFER,BURN-IN	01295	SN74LS00 (NP3)
A50U310	156-0464-02			MICROCIRCUIT,DI:DUAL 4 INP NAND GATE	01295	SN74LS20
A50U420	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A50U430	156-0411-00			MICROCIRCUIT,LI:QUAD-COMP,SGL SUPPLY	27014	LM339N
A50U500	156-0480-02			MICROCIRCUIT,DI:QUAD 2 INP & GATE	01295	SN74LS08NP3
A50U510	156-0427-00	B010100	B030629	MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	04713	MC6820(L OR P)
A50U510	156-0427-04	B030630		MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	80009	156-0427-04
A50U530	156-0467-02			MICROCIRCUIT,DI:QUAD 2-INP NAND BFR,SCRN	01295	SN74LS38
A50U630	156-0541-02			MICROCIRCUIT,DI:DUAL 2 TO 4 LINE DCDR	01295	SN74LS139NP3
A50U710	156-0427-00	B010100	B030629	MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	04713	MC6820(L OR P)
A50U710	156-0427-04	B030630		MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	80009	156-0427-04
A50U810	156-0427-00	B010100	B030629	MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	04713	MC6820(L OR P)
A50U810	156-0427-04	B030630		MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	80009	156-0427-04
A50U830	156-0978-00	B010100	B030761	MICROCIRCUIT,DI:2048 X 8 ROM,CUSTAM MASK	80009	156-0978-00
A50U830	160-1514-00	B030838		MICROCIRCUIT,DI:2048 X 8 EPROM,PROGRAMMED	80009	160-1514-00
A50U1000	155-0135-00			MICROCIRCUIT,DI:DUAL IN LINE,20 LEAD	80009	155-0135-00
A50U1005	156-0656-02			MICROCIRCUIT,DI:DECADE COUNTER,BURN-IN	01295	SN74LS90
A50U1030	156-0979-00	B010100	B030761	MICROCIRCUIT,DI:2048 X 8 ROM,CUSTOM MASK	80009	156-0979-00
A50U1030	160-1513-00	B030838		MICROCIRCUIT,DI:2048 X 8 EPROM,PROGRAMMED	80009	160-1513-00
A50U1100	156-0736-02			MICROCIRCUIT,DI:BCD TO DECIMAL DCDR	80009	156-0736-02
A50U1105	156-0093-02			MICROCIRCUIT,DI:HEX INV BUFFER,BURN-IN	01295	SN74LS00 (NP3)
A50U1110	156-0427-00	B010100	B030629	MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	04713	MC6820(L OR P)
A50U1110	156-0427-04	B030630		MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	80009	156-0427-04
A50U1130	156-0716-00			MICROCIRCUIT,DI:RAM,128 X 8 STATIC	04713	MCM6810S
A50U1220	156-0426-00	B010100	B020511	MICROCIRCUIT,DI:MICROPROCESSOR	04713	MC6800S
A50U1220	156-0426-05	B020512		MICROCIRCUIT,DI:MICROPROCESSOR,SCREENED	80009	156-0426-05
A50U1310	156-0541-02			MICROCIRCUIT,DI:DUAL 2 TO 4 LINE DCDR	01295	SN74LS139NP3

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
A50U1420	156-0427-00	B010100	B030629	MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	04713	MC6820(L OR P)
A50U1420	156-0427-04	B030630		MICROCIRCUIT,DI:PERIPHERAL INTERFACE ADPTR	80009	156-0427-04
A50U1500	155-0164-00			MICROCIRCUIT,DI:TIME SLOT SWITCH	80009	155-0164-00
A50U1520	156-0645-00			MICROCIRCUIT,DI:EX INV ST NAND GATES,SCRN	01295	SN741LS14(NP3)
A50U1530	156-0405-03			MICROCIRCUIT,DI:DUAL RETRIG MONOSTABLE MV	07263	9602
A50U1620	156-0479-02			MICROCIRCUIT,DI:QUAD 2-INP OR GATE	01295	SN74LS32NP3
A50U1630	156-0382-02			MICROCIRCUIT,DI:QUAD 2-INP NAND GATE	01295	SN74LS00
A50U1720	156-0467-02			MICROCIRCUIT,DI:QUAD 2-INP NAND BFR,SCRN	01295	SN74LS38
A50U1730	156-0388-03			MICROCIRCUIT,DI:DUAL D FLIP-FLOP	07263	74LS74A
A50VR1204	152-0590-00			SEMICOND DEVICE:ZENER,18V,5% AT 7MA	04713	SZG35014K2
A50VR1206	152-0590-00			SEMICOND DEVICE:ZENER,18V,5% AT 7MA	04713	SZG35014K2
A50VR1300	152-0590-00			SEMICOND DEVICE:ZENER,18V,5% AT 7MA	04713	SZG35014K2
A50VR330	152-0437-00	B010100	B031149	SEMICOND DEVICE:ZENER,SI,8.2V,2%,0.4W	14552	TD332679
A50VR330	152-0127-00	B031150		SEMICOND DEVICE:ZENER,0.4W,7.5V,5%	04713	SZG35009K2
A50VR730	152-0508-00	B010100	B030837	SEMICOND DEVICE:ZENER,0.4W,12.6V,5%	80009	152-0508-00
A50VR810	152-0217-00			SEMICOND DEVICE:ZENER,0.4W,8.2V,5%	04713	SZG20
A50W320	131-0566-00			BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A50W635	131-0566-00	B030837		BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A50W730	131-0566-00	B030837		BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A50W735	131-0566-00	B030837		BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0
A50W1720	131-0566-00	B010100	B030837	BUS CONDUCTOR:DUMMY RES,2.375,22 AWG	57668	JWW-0200E0

Component No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Name & Description	Mfr Code	Mfr Part Number
				A51 MEMORY ADAPTER		
A51	670-7549-00	B030762	B030837	CKT BOARD ASSY:MEMORY ADAPTER	80009	670-7549-00
A51U830	160-1514-00	B030762	B030837	MICROCIRCUIT,DI:2048 X 8 EPROM,PROGRAMMED	80009	160-1514-00
A51U1030	160-1513-00	B030762	B030837	MICROCIRCUIT,DI:2048 X 8 EPROM,PROGRAMMED	80009	160-1513-00
				CHASSIS PARTS		
C5402	281-0621-00			CAP.,FXD,CER DI:12PF,1%,500V	59660	301-080 COGO-12F
C5412	281-0593-00			CAP.,FXD,CER DI:3.9PF,10%,500V	04222	7001-C0J-3R9C
E5412	276-0507-00			SHIELDING BEAD,:FERRITE	78488	57-3443
J001	131-0955-00			CONN,RCPT,ELEC:BNC,FEMALE	13511	31-279
L5412	108-0170-01			COIL,RF:FIXED,36ONH	80009	108-0170-01
R5400	321-0481-00			RES.,FXD,FILM:1M OHM,1%,0.125W	91637	CMF55116G10003F
R5402	315-0910-00			RES.,FXD,CMPSN:91 OHM,5%,0.25W	01121	CB9105
R5410	315-0181-00			RES.,FXD,CMPSN:180 OHM,5%,0.25W	01121	CB1815
R5412	315-0510-00			RES.,FXD,CMPSN:51 OHM,5%,0.25W	01121	CB5105
R5414	315-0680-00			RES.,FXD,CMPSN:68 OHM,5%,0.25W	01121	CB6805
S001	260-1666-00			SWITCH,PUSH:1 STA,2 POLE,PUSH-PUSH	71590	2KAB010000-674

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATIONS

Symbols and Reference Designators

Electrical components shown on the diagrams are in the following units unless noted otherwise:

Capacitors = Values one or greater are in picofarads (pF).
Values less than one are in microfarads (μF).

Resistors = Ohms (Ω).

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975.

Logic symbology is based on ANSI Y32.14-1973 in terms of positive logic. Logic symbols depict the logic function performed and may differ from the manufacturer's data.

The overline on a signal name indicates that the signal performs its intended function when it goes to the low state.

Abbreviations are based on ANSI Y1.1-1972.

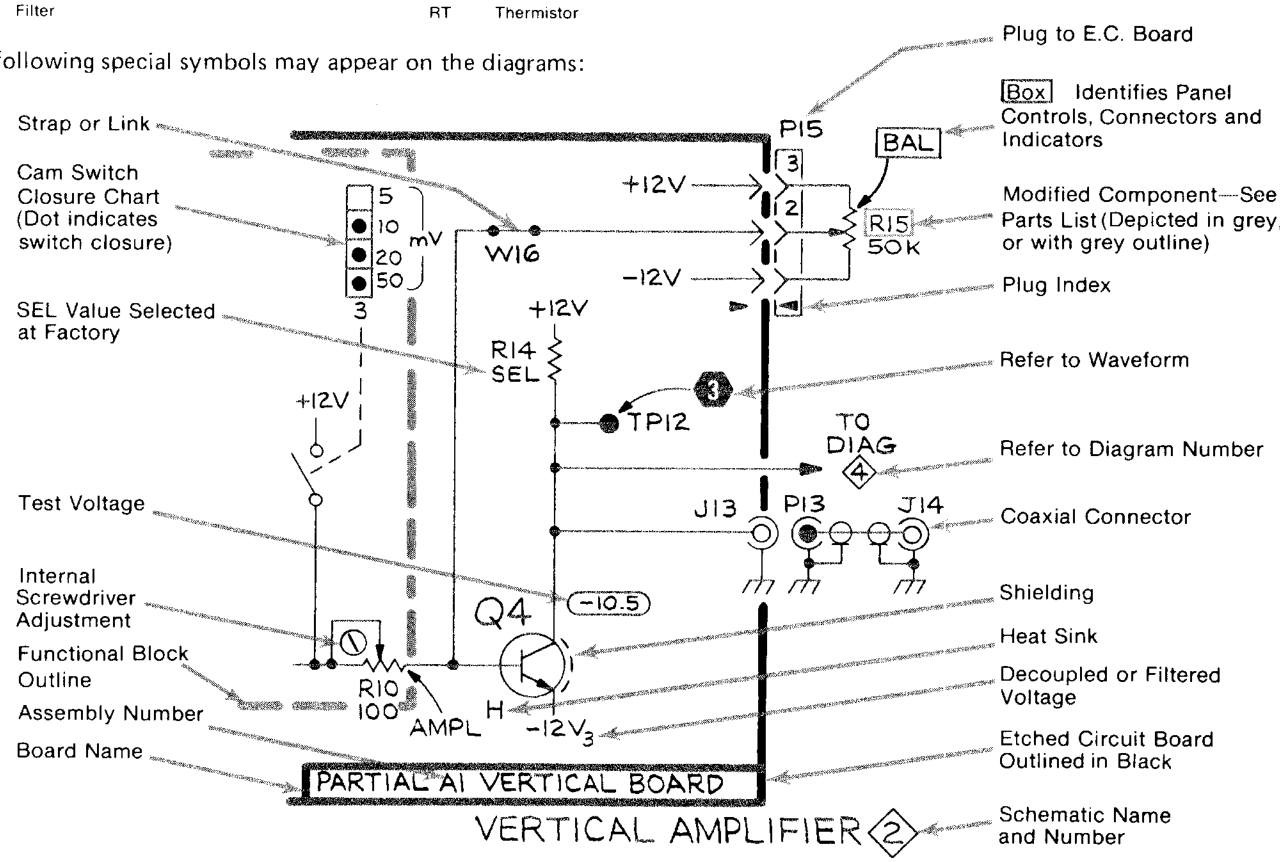
Other ANSI standards that are used in the preparation of diagrams by Tektronix, Inc. are:

Y14.15, 1966	Drafting Practices.
Y14.2, 1973	Line Conventions and Lettering.
Y10.5, 1968	Letter Symbols for Quantities Used in Electrical Science and Electrical Engineering.

The following prefix letters are used as reference designators to identify components or assemblies on the diagrams.

A	Assembly, separable or repairable (circuit board, etc)
AT	Attenuator, fixed or variable
B	Motor
BT	Battery
C	Capacitor, fixed or variable
CB	Circuit breaker
CR	Diode, signal or rectifier
DL	Delay line
DS	Indicating device (lamp)
E	Spark Gap, Ferrite bead
F	Fuse
FL	Filter
H	Heat dissipating device (heat sink, heat radiator, etc)
HR	Heater
HY	Hybrid circuit
J	Connector, stationary portion
K	Relay
L	Inductor, fixed or variable
M	Meter
P	Connector, movable portion
Q	Transistor or silicon-controlled rectifier
R	Resistor, fixed or variable
RT	Thermistor
S	Switch or contactor
T	Transformer
TC	Thermocouple
TP	Test point
U	Assembly, inseparable or non-repairable (integrated circuit, etc.)
V	Electron tube
VR	Voltage regulator (zener diode, etc.)
W	Wirestrap or cable
Y	Crystal
Z	Phase shifter

The following special symbols may appear on the diagrams:



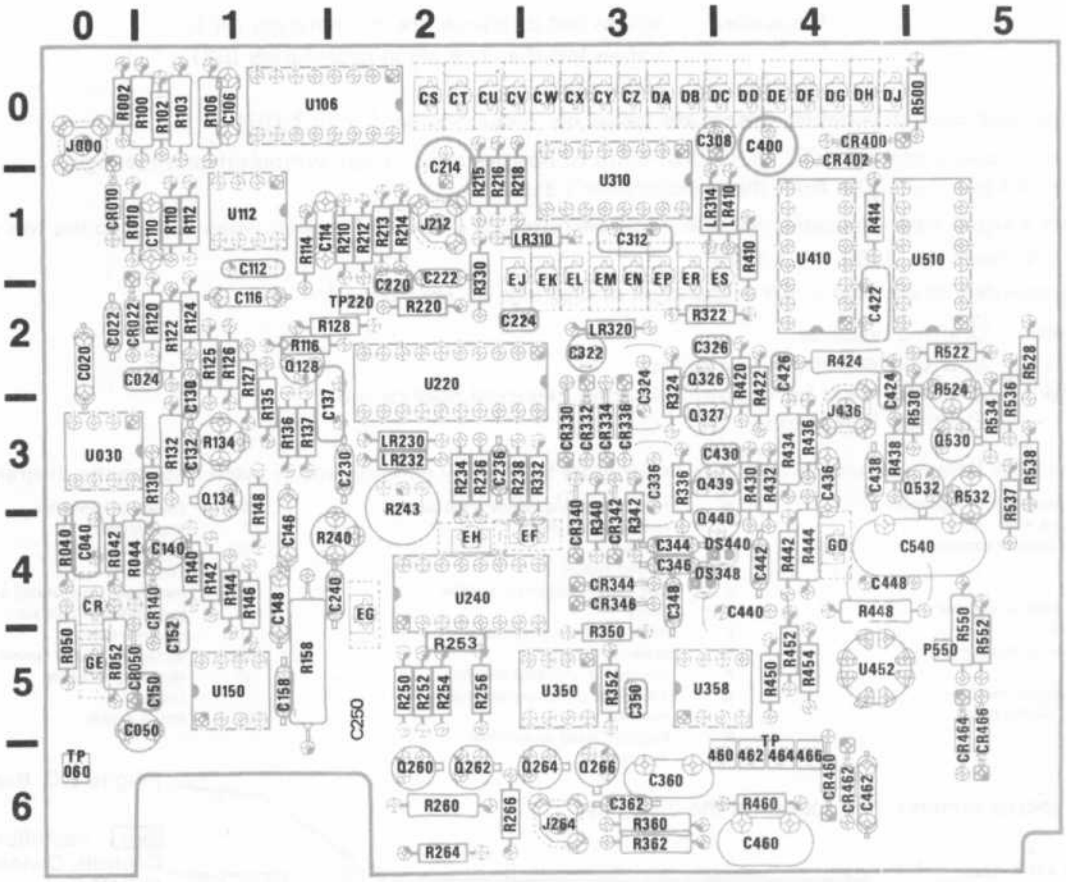


Fig. 8-1. P/O Trigger Board A10.

*See Parts List for serial number ranges.

CKT NUMBERING EXAMPLE

R162 on A12 Assembly = R12162 in Parts List
└Assembly Number

TRIGGER GENERATOR (1)

P/O TRIGGER BOARD A10

COMPONENT NUMBER	SCHEMATIC LOCATION COL	SCHEMATIC LOCATION ROW	BOARD LOCATION COL	BOARD LOCATION ROW
C020	E	5	0	2
C022	E	4	0	2
C024	F	4	0	2
C040	E	6	0	4
C050	E	6	0	5
C106	D	1	1	0
C110	B	1	1	1
C112	E	1	1	1
C114	B	1	1	1
C116	G	3	1	2
C130	E	5	1	3
C132	F	5	1	3
C137	G	5	1	3
C140	E	5	1	4
C146	G	5	1	4
C148	G	6	1	4
C150	F	6	1	5
C152	F	5	1	5
C158	F	3	1	5
C214	H	2	2	1
C220	B	1	2	2
C222	F	4	2	2
C224	B	3	2	2
C230	F	3	2	3
C236	G	4	2	3
C240	G	3	2	4
C308	G	3	3	0
C312	B	2	3	1
C322	G	3	3	2
C324	C	5	3	2
C326	C	5	3	2
C336	D	5	3	3
C344	D	5	3	4
C346	D	5	3	4
C348	C	5	3	4
C360*	G	3	3	6
C400	H	2	4	0
C422	D	3	4	2
C424	B	5	4	2
C426	B	5	4	2
C430	D	5	4	3
C436	B	5	4	3
C438	B	6	4	3
C440	B	6	4	4
C442	C	5	4	4
C448	C	4	4	4
C462	E	2	4	6
C540	C	4	5	4
C5402	B	4	3	0
C5412	A	4	4	0
CR010	G	5	0	1
CR022	D	2	0	2
CR050	F	6	0	5
CR140	F	5	1	4
CR330	D	6	3	3
CR332	D	6	3	3
CR334	D	5	3	3
CR336	D	5	3	3
CR340	D	6	3	4
CR342	D	5	3	4
CR344	D	5	3	4
CR346	D	5	3	4
CR400	C	3	4	0
CR402	C	3	4	0
CR460	E	3	4	6
CR462	E	3	4	6
CR464	C	4	5	6
CR466	C	4	5	5
DS348	D	5	3	4
DS440	D	6	4	4
E5412	A	4	4	1
J000	A	1	0	0
J212	A	1	2	1
J300	B	4	3	0†
J436	B	4	4	3
J5001	A	4	CHASSIS	
L5412	A	4	4	1
LR230	F	5	2	3
LR232	G	5	2	3
LR310	H	2	3	1
LR314	H	2	3	1
LR320	H	3	3	2
LR410	H	2	4	1
P550	B	4	5	5
Q128	G	5	1	2
Q134	E	4	1	3
Q326	C	5	3	2
Q327	C	5	3	3
Q439	D	5	4	3
Q440	D	5	4	4
Q530	B	5	5	3
Q532	B	6	5	3
R002	A	1	0	0
R010	C	2	0	1
R040	E	6	0	4
R042	E	5	0	4
R044	E	5	0	4
R050	F	6	0	5
R052	E	6	0	5
R100	D	1	1	0
R102	D	1	1	0
R103	E	1	1	0
R106	D	1	1	0
R110	A	1	1	1
R112	E	2	1	1
R114	B	1	1	1
R116	G	3	1	2
R120	A	1	1	2
R122	F	4	1	2
R124	F	4	1	2
R125	F	4	1	2
R126	F	4	1	2
R127	G	3	1	2
R128	G	3	1	2
R130	E	4	1	3
R132	F	5	1	3
R134	G	3	1	3
R135	G	4	1	3
R136	G	5	1	3
R137	G	5	1	3
R140	F	5	1	4
R142	E	4	1	4
R144	G	5	1	4
R146	G	6	1	4
R148	E	5	1	4
R158	G	4	1	5
R210	B	1	2	1
R212	B	1	2	1
R213	A	1	2	1
R214	C	1	2	1
R215	B	2	2	1
R216	C	3	2	1
R218	B	1	2	1
R220	C	2	2	2
R234	G	4	2	3
R236	G	4	2	3
R238	G	4	2	3
R240	G	3	2	4
R243	G	4	2	4
R252	H	3	2	5
R253	H	4	2	5
R254	H	4	2	5
R322	A	3	3	2
R324	C	5	3	2
R330	E	3	2	2
R332	E	3	3	3
R336	D	5	3	3
R340	D	5	3	4
R342	D	5	3	4
R350	F	2	3	5
R352	F	2	3	5
R410	B	3	4	1
R414	A	3	4	1
R420	C	5	4	2
R422	C	5	4	2
R424	B	5	4	2
R430	D	5	4	3
R432	B	6	4	3
R434	B	5	4	3
R436	B	5	4	3
R438	B	6	4	3
R442	B	6	4	4

†P/O LED BOARD.

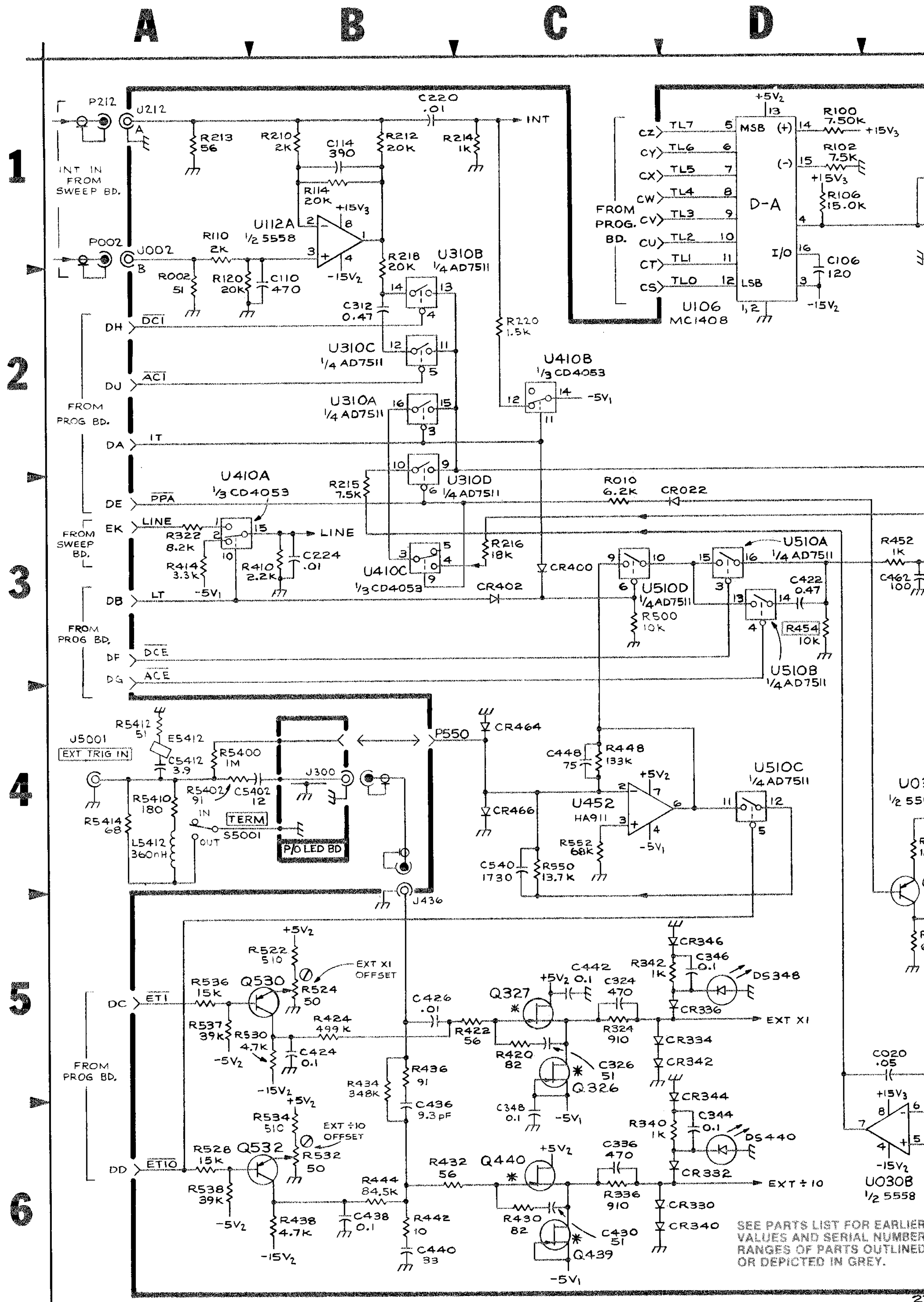
TRIGGER GENERATOR ⟨1⟩

P/O TRIGGER BOARD A10

COMPONENT NUMBER	SCHEMATIC LOCATION		BOARD LOCATION	
	COL	ROW	COL	ROW
CR330	D	6	3	3
CR332	D	6	3	3
CR334	D	5	3	3
CR336	D	5	3	3
CR340	D	6	3	4
CR342	D	5	3	4
CR344	D	5	3	4
CR346	D	5	3	4
CR400	C	3	4	0
CR402	C	3	4	0
CR460	E	3	4	6
CR462	E	3	4	6
CR464	C	4	5	6
CR466	C	4	5	5
DS348	D	5	3	4
DS440	D	6	4	4
E5412	A	4	4	1
J000	A	1	0	0
J212	A	1	2	1
J300	B	4	3	0†
J436	B	4	4	3
J5001	A	4	CHASSIS	
L5412	A	4	4	1
LR230	F	5	2	3
LR232	G	5	2	3
LR310	H	2	3	1
LR314	H	2	3	1
LR320	H	3	3	2
LR410	H	2	4	1
P550	B	4	5	5
Q128	G	5	1	2
Q134	E	4	1	3
Q326	C	5	3	2
Q327	C	5	3	3
Q439	D	5	4	3
Q440	D	5	4	4
Q530	B	5	5	3
Q532	B	6	5	3
R002	A	1	0	0
R010	C	2	0	1
R040	E	6	0	4
R042	E	5	0	4
R044	E	5	0	4
R050	F	6	0	5
R052	E	6	0	5
R100	D	1	1	0
R102	D	1	1	0
R103	E	1	1	0
R106	D	1	1	0
R110	A	1	1	1
R112	E	2	1	1
R114	B	1	1	1
R116	G	3	1	2
R120	A	1	1	2

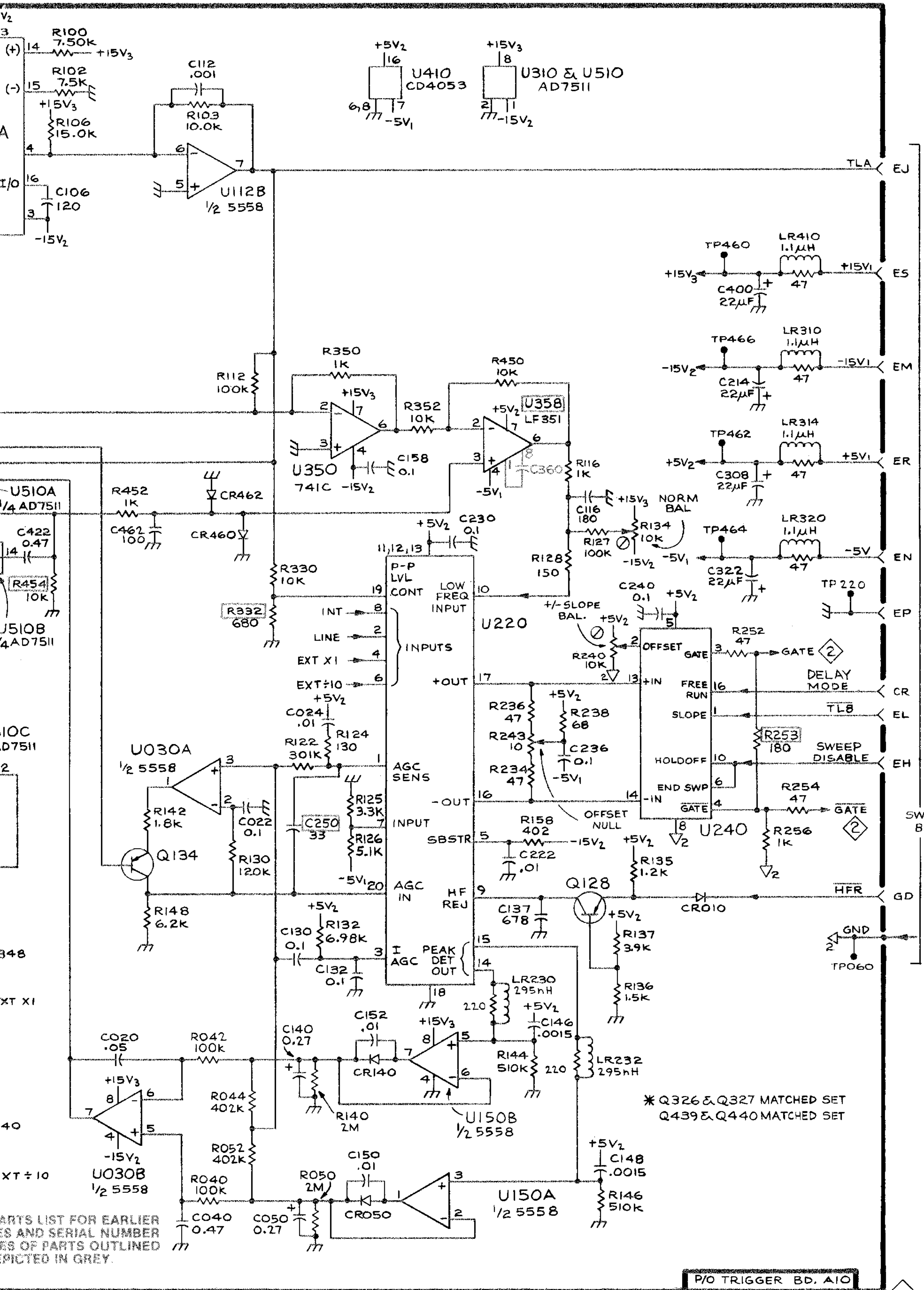
COMPONENT NUMBER	SCHEMATIC LOCATION		BOARD LOCATION	
	COL	ROW	COL	ROW
R122	F	4	1	2
R124	F	4	1	2
R125	F	4	1	2
R126	F	4	1	2
R127	G	3	1	2
R128	G	3	1	2
R130	E	4	1	3
R132	F	5	1	3
R134	G	3	1	3
R135	G	4	1	3
R136	G	5	1	3
R137	G	5	1	3
R140	F	5	1	4
R142	E	4	1	4
R144	G	5	1	4
R146	G	6	1	4
R148	E	5	1	4
R158	G	4	1	5
R210	B	1	2	1
R212	B	1	2	1
R213	A	1	2	1
R214	C	1	2	1
R215	B	2	2	1
R216	C	3	2	1
R218	B	1	2	1
R220	C	2	2	2
R234	G	4	2	3
R236	G	4	2	3
R238	G	4	2	3
R240	G	3	2	4
R243	G	4	2	4
R252	H	3	2	5
R253	H	4	2	5
R254	H	4	2	5
R322	A	3	3	2
R324	C	5	3	2
R330	E	3	2	2
R332	E	3	3	3
R336	D	5	3	3
R340	D	5	3	4
R342	D	5	3	4
R350	F	2	3	5
R352	F	2	3	5
R410	B	3	4	1
R414	A	3	4	1
R420	C	5	4	2
R422	C	5	4	2
R424	B	5	4	2
R430	D	5	4	3
R432	B	6	4	3
R434	B	5	4	3
R436	B	5	4	3
R438	B	6	4	3
R442	B	6	4	4

COMPONENT NUMBER	SCHEMATIC LOCATION		BOARD LOCATION	
	COL	ROW	COL	ROW
R444	B	6	4	4
R448	C	4	4	4
R450	F	2	4	5
R452	E	3	4	5
R454	D	3	4	5
R522	B	5	5	2
R524	B	5	5	2
R528	A	6	5	2
R530	B	5	5	3
R532	B	6	5	3
R534	B	5	5	3
R536	A	5	5	3
R537	A	5	5	4
R538	A	6	5	3
R550	C	4	5	5
R552	C	4	5	5
R5400	A	4	3	0
R5402	A	4	4	0
R5410	A	4	4	1
R5412	A	4	4	1
R5414	A	4	4	1
TP060	H	5	0	6
TP220	H	3	2	2
TP460	G	2	4	6
TP462	G	2	4	6
TP464	G	3	4	6
TP466	G	2	4	6
U030A	E	4	0	3
U030B	E	6	0	3
U106	D	1	1	0
U112A	B	1	1	1
U112B	E	1	1	1
U150A	F	6	1	5
U150B	F	5	1	5
U220	F	3	2	2
U240	G	4	2	4
U310	F	1	3	1
U310A	B	2	3	1
U310B	B	1	3	1
U310C	B	2	3	1
U310D	B	2	3	1
U350	F	2	3	5
U358	F	2	3	5
U410	F	1	4	1
U410A	A	3	4	1
U410B	C	2	4	1
U410C	B	3	4	1
U452	C	4	4	5
U510	F	1	5	1
U510A	D	3	5	1
U510B	D	3	5	1
U510C	D	4	5	1
U510D	C	3	5	1



A
B
C
D
1
2
3
4
5
6
P212
J212
INT IN FROM SWEEP BD.
P002
J002
R213 56
R210 2K
C114 390
R114 20K
R212 20K
C220 .01
R214 1K
INT
U112A 1/2 5558
+15V3
-15V2
R110 2K
R002 51
R120 20K
C110 470
R218 20K
U310B 1/4 AD7511
C312 0.47
U310C 1/4 AD7511
U310A 1/4 AD7511
U310D 1/4 AD7511
R220 1.5K
U410B 1/3 CD4053
-5V1
FROM PROG. BD.
DH
DCI
DJ
ACI
DA
IT
DE
PPA
FROM SWEEP BD.
EK
LINE
U410A 1/3 CD4053
R322 8.2K
R414 3.3K
R410 2.2K
C224 .01
R215 7.5K
R010 6.2K
CR022
R216 18K
U410C 1/3 CD4053
CR400
CR402
DB
LT
DF
DCE
DG
ACE
U510A 1/4 AD7511
U510D 1/4 AD7511
U510B 1/4 AD7511
R500 10K
C422 0.47
R454 10K
R452 1K
C462 100
FROM PROG. BD.
CZ CY CX CW CV CU CT CS
TL7 TL6 TL5 TL4 TL3 TL2 TL1 TL0
MSB
LSB
D-A
I/O
U106 MC1408
+5V2
R100 7.50K
+15V3
R102 7.5K
R106 15.0K
C106 120
-15V2
R5412 51
E5412
C5412 3.9
J5001
EXT TRIG IN
R5400 1M
R5402 91
C5402 12
R5410 180
R5414 68
L5412 360nH
IN
OUT
TERM
S5001
J300
P/O LED BD
P550
J436
CR464
CR466
C448 75
R448 133K
U452 HA911
R552 68K
C540 1730
R550 13.7K
U510C 1/4 AD7511
U03 1/2 55
FROM PROG BD.
DC
ET1
DD
ET10
R536 15K
Q530
R537 39K
R530 4.7K
R522 510
R524 50
EXT X1 OFFSET
R424 499K
C424 0.1
C426 .01
R422 56
Q327
C442 0.1
C324 470
R324 910
R342 1K
C346 0.1
DS348
CR346
CR336
EXT X1
R420 82
C326 51
Q326
C348 0.1
CR334
CR342
CR344
C344 0.1
R340 1K
DS440
CR332
R434 348K
R436 91
C436 9.3 pF
R534 510
EXT ÷10 OFFSET
R532 50
R528 15K
Q532
R538 39K
R438 4.7K
C438 0.1
R444 84.5K
R442 10
C440 33
R432 56
Q440
C336 470
R336 910
EXT ÷10
R430 82
C430 51
Q439
CR330
CR340
C020 .05
U030B 1/2 5558
SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.

7B90P



2309-15
REV B FEB 1980

TRIGGER GENERATOR

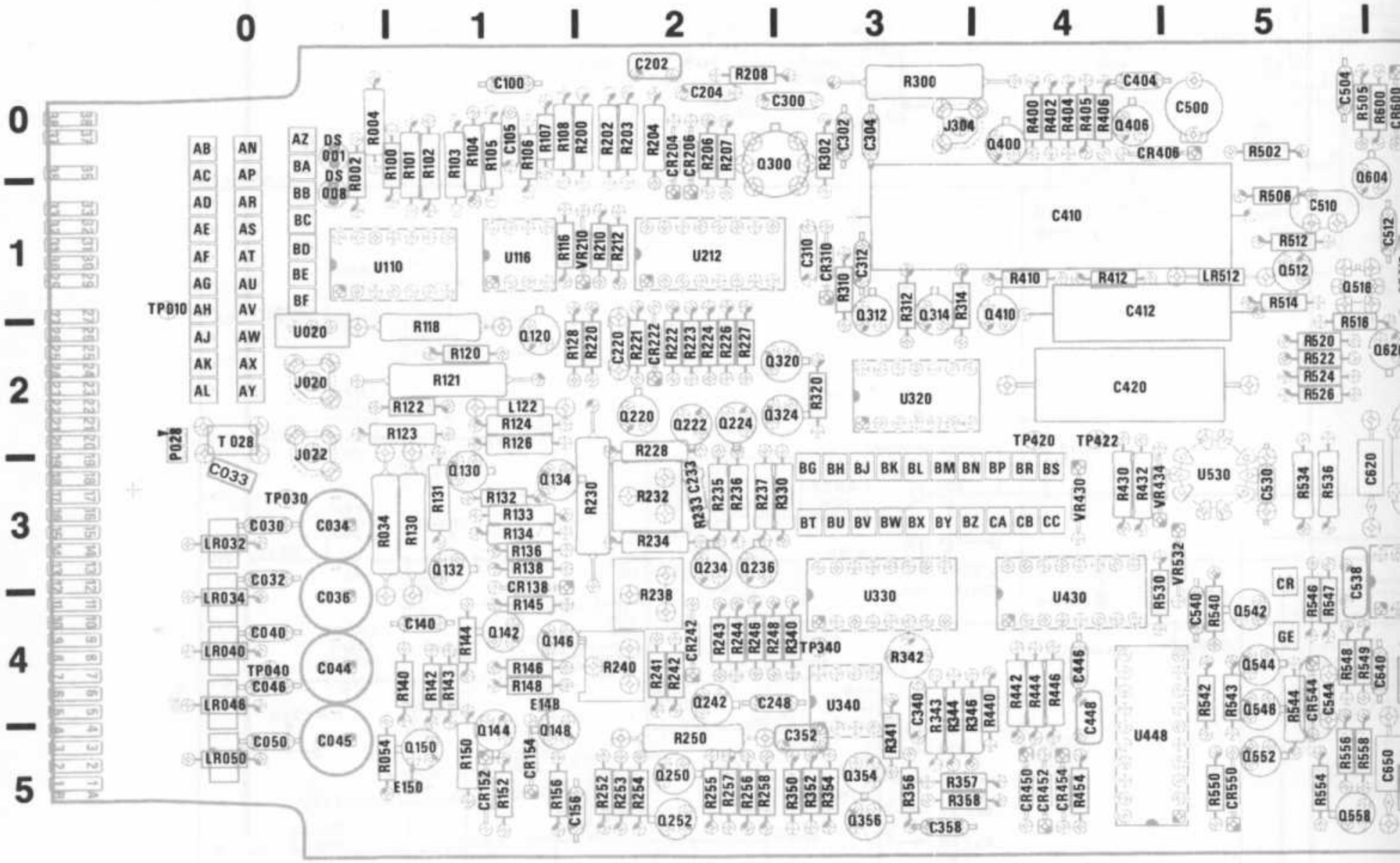
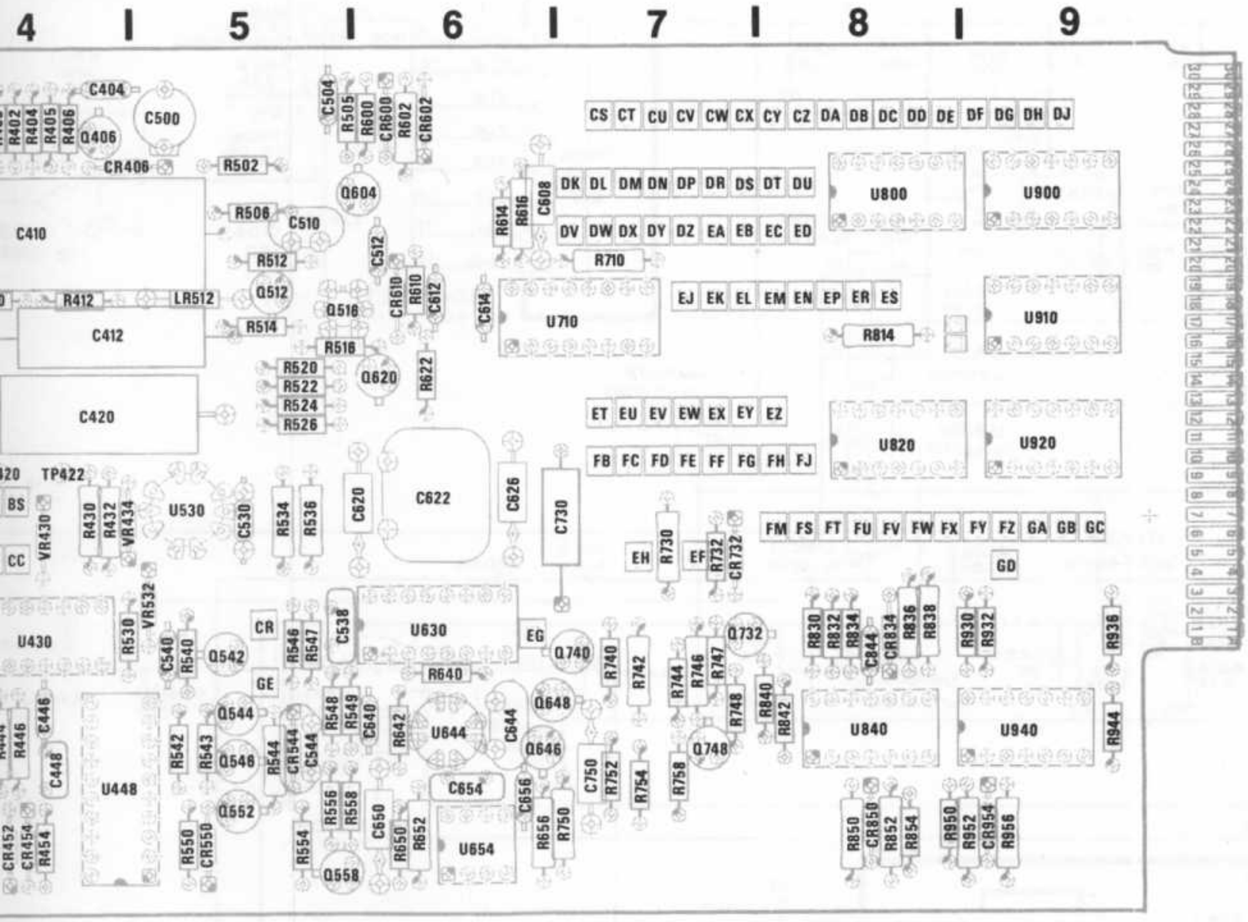


Fig. 8-2. P/O Sweep Board A20.

CKT NUMBERING EXAMPLE

R162 on A12 Assembly = R12162 in Parts List

Assembly Number

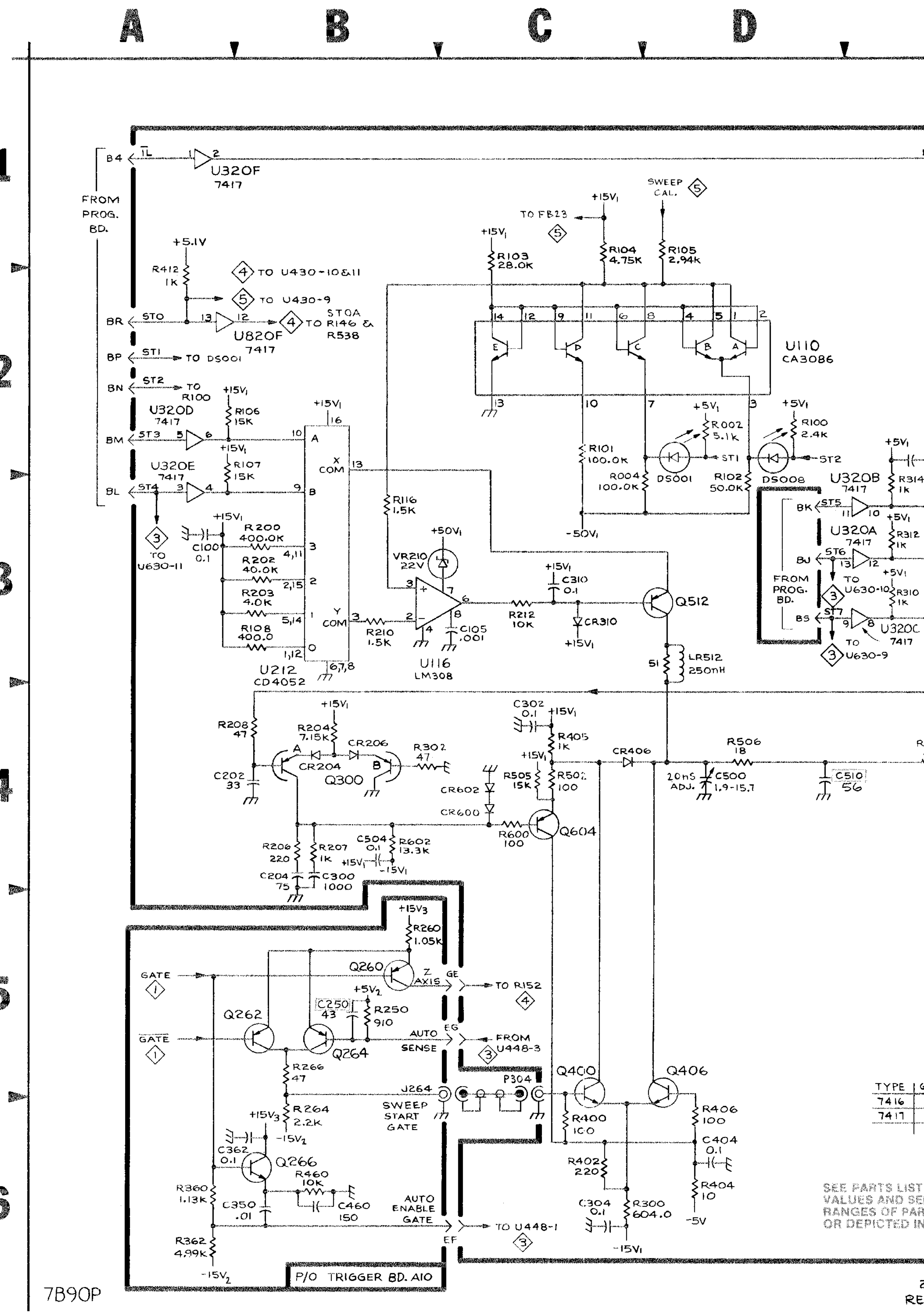


P/O Sweep Board A20.

SWEEP GENERATOR ⟨2⟩

P/O SWEEP BOARD A20

COMPONENT NUMBER	SCHEMATIC LOCATION COL	SCHEMATIC LOCATION ROW	BOARD LOCATION COL	BOARD LOCATION ROW
C030	H	1	0	3
C032	G	1	0	3
C033	G	1	0	3
C034	G	3	0	3
C036	G	2	0	4
C040	G	2	0	4
C044	G	1	0	4
C045	G	2	0	5
C046	G	1	0	4
C050	G	2	0	5
C100	A	3	1	0
C105	B	3	1	0
C140	G	2	1	4
C202	A	4	2	0
C204	B	4	2	0
C300	B	4	3	0
C302	C	4	3	0
C304	C	6	3	0
C310	C	3	3	1
C312	E	2	3	1
C404	D	6	4	0
C410	E	3	4	1
C412	E	3	4	1
C420	E	3	4	2
C500	D	4	5	0
C504	B	4	5	0
C510	D	4	5	1
C512	F	4	6	1
C530	G	4	5	3
C612	F	5	6	1
CR204	B	4	2	0
CR206	B	4	2	0
CR310	C	3	3	1
CR406	C	4	4	0
CR600	C	4	6	0
CR602	C	4	6	0
CR610	F	4	6	1
CR732	G	5	7	3
DS001	D	2	0	0
DS008	D	2	0	0
LR032	G	1	0	3
LR034	G	1	0	4
LR040	G	2	0	4
LR046	G	1	0	4
LR050	G	2	0	5
LR512	D	3	5	1
P028	G	3	0	2
Q300	B	4	3	0
Q312	E	3	3	1
Q314	E	3	3	1
Q400	C	5	4	0
Q406	D	5	4	0
Q410	E	3	4	1
Q512	C	3	5	1
Q516A	F	4	5	1
Q516B	F	4	5	1
Q604	C	4	6	0
Q620	F	4	6	2
Q732	G	5	7	3
Q748	G	5	7	4
R002	D	2	0	0
R004	C	2	0	0
R100	D	2	1	0
R101	C	2	1	0
R102	D	2	1	0
R103	C	1	1	0
R104	C	1	1	0
R105	C	1	1	0
R106	A	2	1	0
R107	A	2	1	0
R108	A	3	1	0
R116	B	3	1	1
R144	G	1	1	4
R200	A	3	2	0
R202	A	3	2	0
R203	A	3	2	0
R204	B	4	2	0
R207	B	4	2	0
R208	A	4	2	0
R210	B	3	2	1
R212	C	3	2	1
R300	C	6	3	0
R302	B	4	3	0
R310	E	3	3	1
R312	E	3	3	1
R314	E	2	3	1
R400	C	6	4	0
R402	C	6	4	0
R404	D	6	4	0
R405	C	4	5	0
R406	D	6	4	0
R410	E	3	4	1
R412	A	1	4	1
R430	G	4	4	3
R432	G	4	4	3
R502	C	4	5	0
R505	C	4	5	0
R506	D	4	5	1
R512	E	4	5	1
R514	E	4	5	1
R516	F	4	5	2
R520	F	4	5	2
R522	F	4	5	2
R524	F	4	5	2
R526	F	4	5	2
R534	G	4	5	3
R536	G	3	5	3
R600	C	4	6	0
R602	B	4	6	0
R610	F	4	6	1
R622	F	5	6	2
R730	F	4	7	3
R732	G	5	7	3
R744	G	5	7	4
R746	G	5	7	4
R747	F	5	7	4
R748	G	5	7	4
R758	G	5	7	5
TP010	G	2	0	1
TP030	H	2	0	3
TP040	G	5	0	4
TP420	F	4	4	2
TP422	F	4	4	2
U020	G	2	0	2
U110	D	2	1	1
U116	B	3	1	1
U212	B	3	2	1
U320A	D	3	3	2
U320B	D	3	3	2
U320C	D	3	3	2
U320C	A	2	3	2
U320D	A	2	3	2
U320E	A	3	3	2
U320F	A	1	3	2
U530	G	4	5	3
U820F	A	2	8	2
VR210	B	3	2	1
VR434	G	4	4	3
VR532	G	5	5	3
P/O TRIGGER BOARD A10. See Fig. 8-1				
C250	B	5	2	5
C350	B	6	3	5
C362	A	6	3	6
C460	B	6	4	6
J264	B	5	3	6
J304	C	5	3	0
Q260	B	5	2	6
Q262	A	5	2	6
Q264	B	5	3	6
Q266	B	6	3	6
R250	B	5	2	5
R260	B	6	2	6
R264	B	6	2	6
R266	B	5	2	6
R360	A	6	3	6
R362	A	6	3	6
R460	B	6	4	6



A
B
C
D
1
2
3
4
5
6
FROM PROG. BD.
U320F 7417
SWEEP CAL.
TO FB23
R412 1K
+5.1V
TO U430-10&11
TO U430-9
STOA TO R146 & R538
U820F 7417
TO DS001
TO R100
U320D 7417
U320E 7417
R103 28.0K
R104 4.75K
R105 2.94K
U110 CA3086
R101 100.0K
R004 100.0K
R002 5.1K
R100 2.4K
DS001
DS008
R102 50.0K
-50V
R106 15K
R107 15K
R116 1.5K
R200 400.0K
R202 40.0K
R203 4.0K
R108 400.0
C100 0.1
TO U630-11
U212 CD4052
VR210 22V
+50V
U116 LM308
R210 1.5K
C105 .001
R212 10K
C310 0.1
CR310
Q512
LR512 250nH
U320B 7417
R314 1K
U320A 7417
R312 1K
R310 1K
U320C 7417
TO U630-10
TO U630-9
R208 47
C202 33
R204 7.15K
CR204
CR206
Q300
R302 47
C302 0.1
R405 1K
R505 15K
R502 100
CR602
CR600
CR406
R506 18
20nS ADJ.
C500 1.9-15.7
C510 56
R600 100
Q604
R206 220
R207 1K
C504 0.1
R602 13.3K
C204 75
C300 1000
R260 1.05K
Q260
Z AXIS
GE
TO R152
GATE
Q262
Q264
C250 43
R250 910
AUTO SENSE
EG
FROM U448-3
R266 47
J264
SWEEP START GATE
P304
Q400
Q406
R400 100
R406 100
R264 2.2K
C362 0.1
Q266
R460 10K
C460 150
R360 1.13K
C350 .01
R362 4.99K
AUTO ENABLE GATE
EF
TO U448-1
R402 220
C304 0.1
R300 604.0
C404 0.1
R404 10
-5V
P/O TRIGGER BD. A10
TYPE
7416
7417
SEE PARTS LIST

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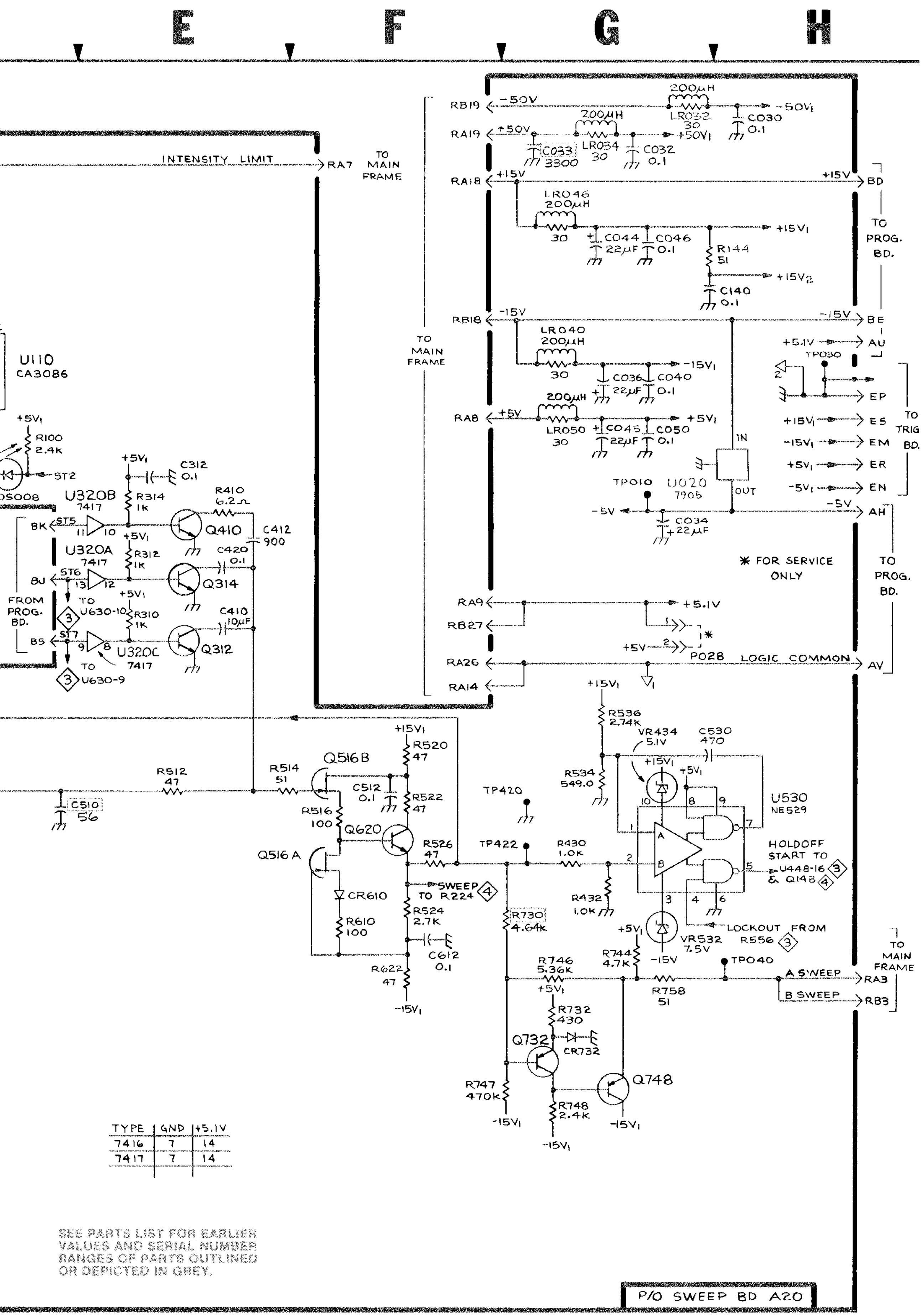


TYPE	GND	+5.1V
7416	7	14
7417	7	14

SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.

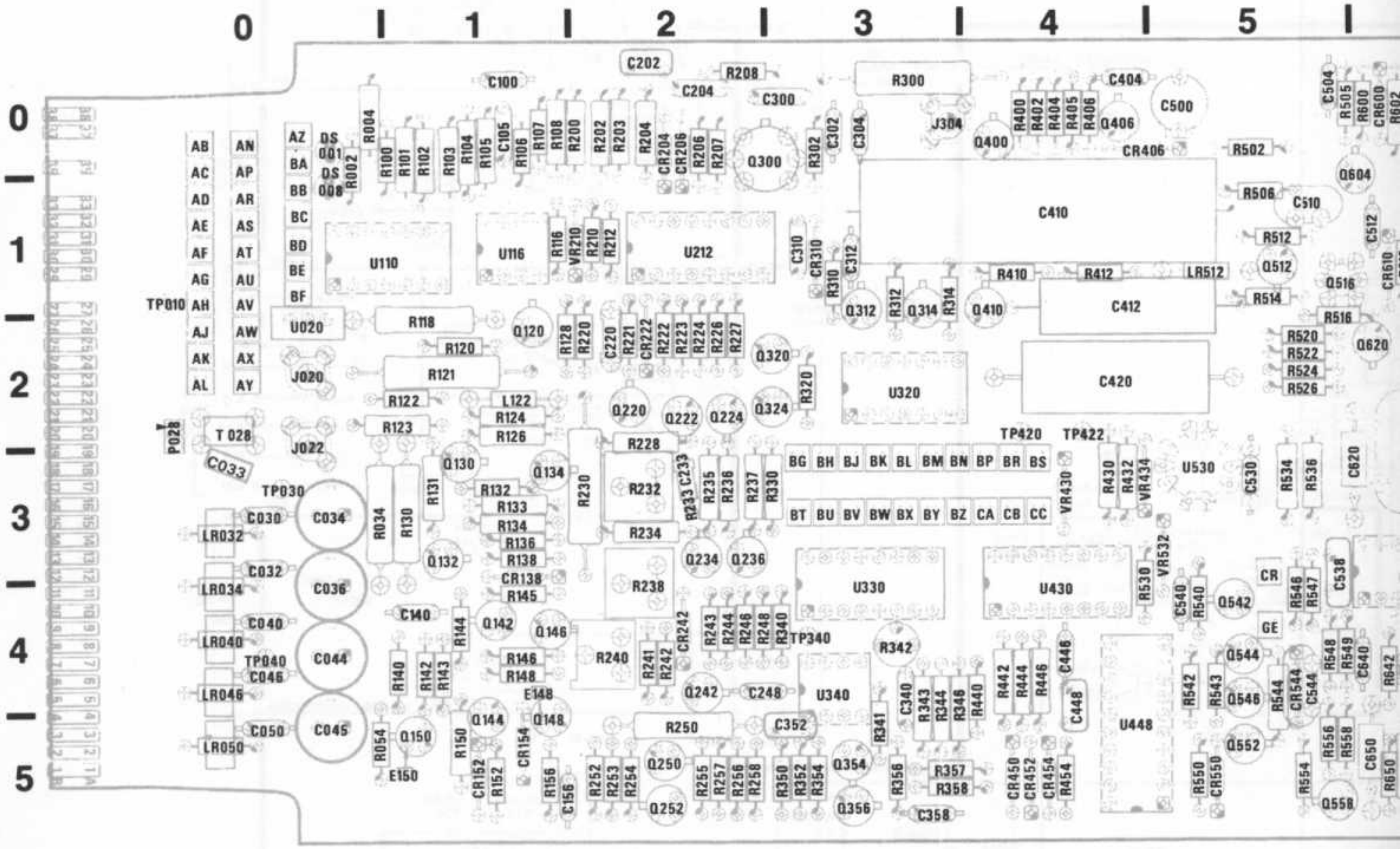


Fig. 8-3. P/O Sweep Board A20.

CKT NUMBERING EXAMPLE

R162 on A12 Assembly = R12162 in Parts List

Assembly Number

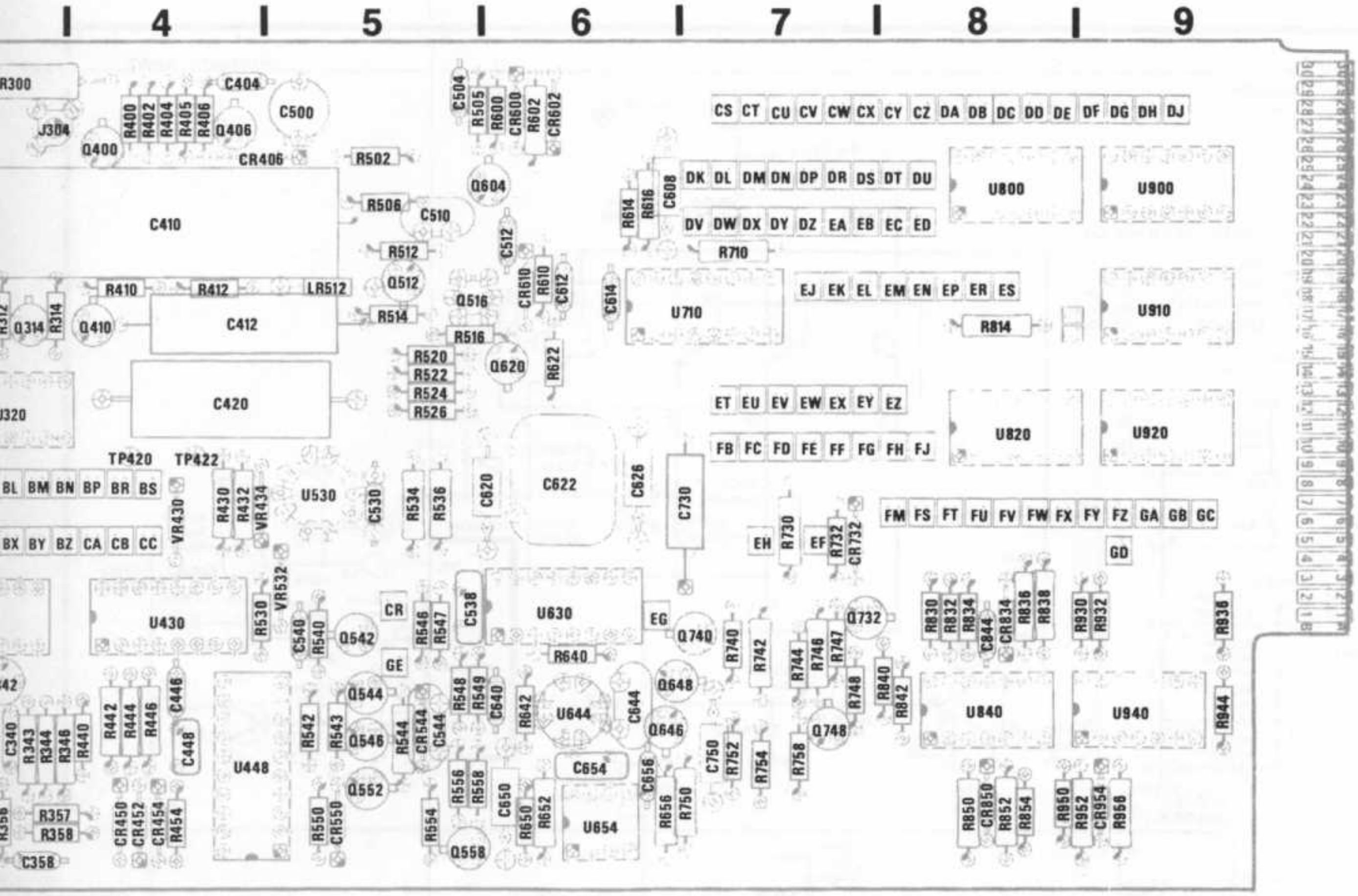
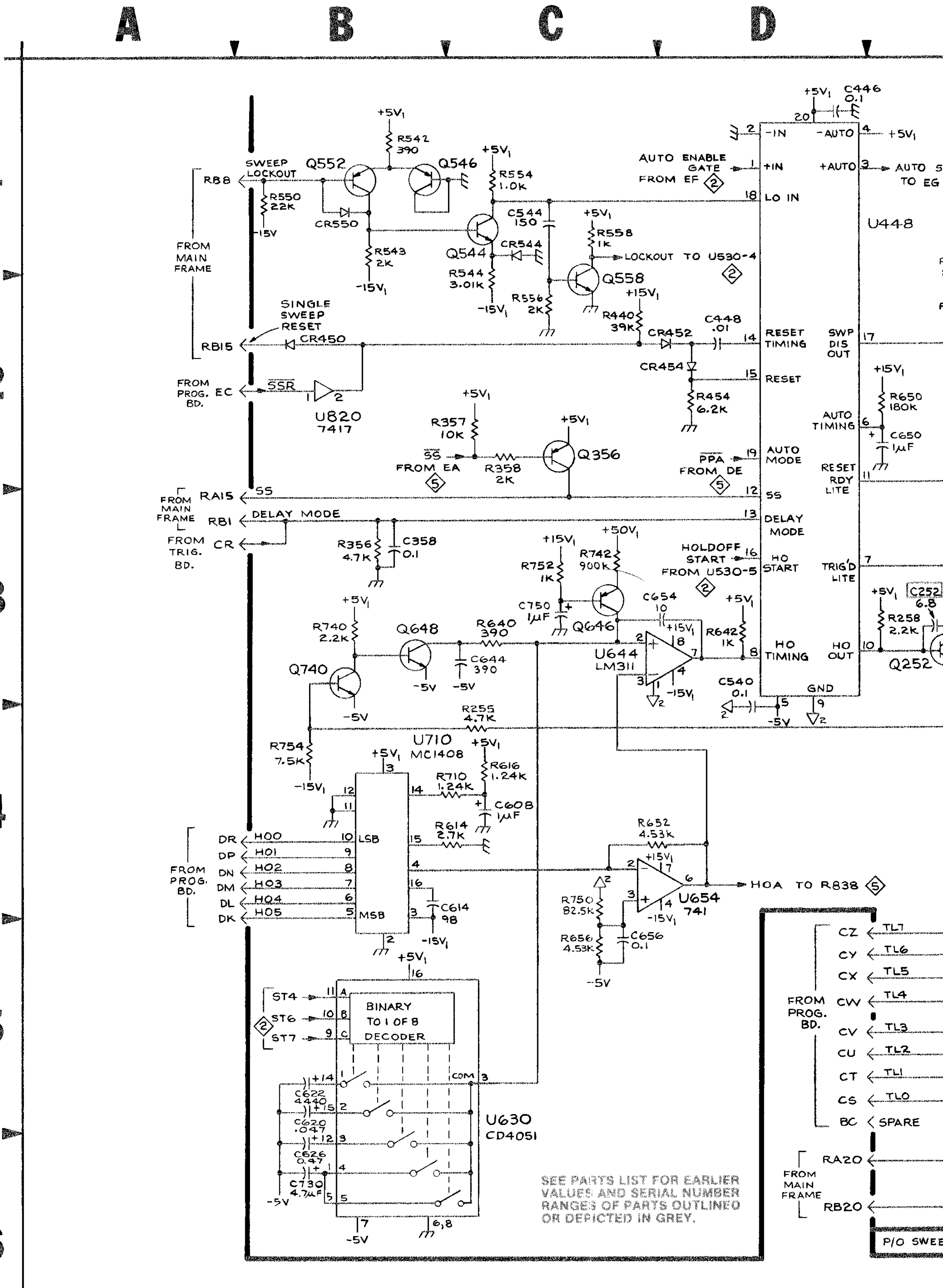


Fig. 8-3. P/O Sweep Board A20.

SWEEP LOGIC 3

P/O SWEEP BOARD A20

COMPONENT NUMBER	SCHEMATIC LOCATION		BOARD LOCATION		COMPONENT NUMBER	SCHEMATIC LOCATION		BOARD LOCATION	
	COL	ROW	COL	ROW		COL	ROW	COL	ROW
C352	F	2	3	5	R257	E	4	2	3
C358	B	3	3	5	R258	D	3	2	5
C446	D	1	4	4	R350	F	2	3	5
C448	C	2	4	4	R352	F	2	2	5
C538	F	2	5	3	R354	F	2	3	5
C540	C	3	5	4	R356	B	3	3	5
C544	B	1	5	4	R357	B	2	3	5
C608	B	4	6	1	R358	B	2	3	5
C614	B	4	6	1	R440	C	2	4	4
C620	A	5	6	3	R454	C	2	4	5
C622	A	5	6	3	R540	E	2	5	4
C626	A	6	6	3	R542	B	1	5	4
C640	E	1	6	4	R543	B	1	5	4
C644	B	3	6	4	R544	B	1	5	4
C650	D	2	6	5	R546	E	2	5	4
C654	C	3	6	5	R547	E	2	5	4
C656	C	5	6	5	R548	E	1	5	4
C730	A	6	7	3	R549	E	1	6	4
C750	C	3	7	5	R550	A	1	5	5
CR450	A	2	4	5	R554	B	1	5	5
CR452	C	2	4	5	R556	B	2	5	5
CR454	C	2	4	5	R558	C	1	5	5
CR544	B	1	5	4	R614	B	4	6	1
CR550	A	1	5	5	R616	B	4	6	1
J020	E	6	0	2	R640	B	3	6	4
J022	E	6	0	2	R642	C	3	6	4
Q250	E	3	2	5	R650	D	2	6	5
Q252	D	3	2	5	R652	C	4	6	5
Q354	F	2	3	5	R656	C	5	6	5
Q356	C	2	3	5	R710	B	4	7	1
Q542	E	1	5	4	R740	B	3	7	4
Q544	B	1	5	4	R742	C	3	7	4
Q546	B	1	5	4	R750	C	4	7	5
Q552	B	1	5	5	R752	C	3	7	5
Q558	C	2	5	5	R754	A	4	7	5
Q646	C	3	6	4	T028	E	6	0	2
Q648	B	3	6	4	U448	D	1	4	5
Q740	B	3	7	4	U630	B	5	6	3
R253	B	3	2	5	U644	C	3	6	4
R254	E	3	2	5	U654	C	4	6	5
R255	B	4	2	5	U710	B	4	7	1
R256	D	3	2	5	U820	A	2	8	2

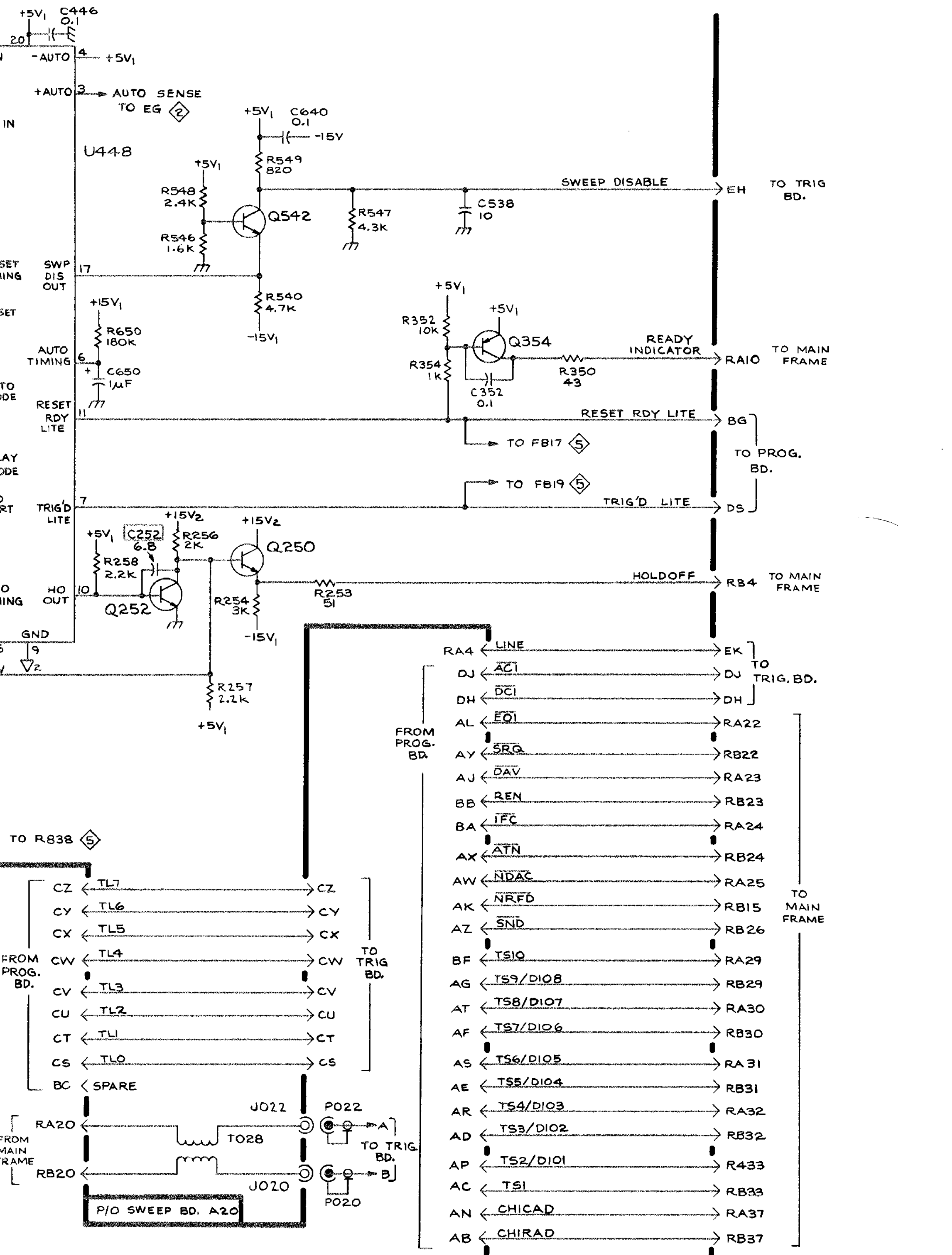


SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.

2309-
REV B F

7B90P

E F G H



2309-19
REV B FEB 1980

Sweep Logic 3

SWEEP LOGIC

3

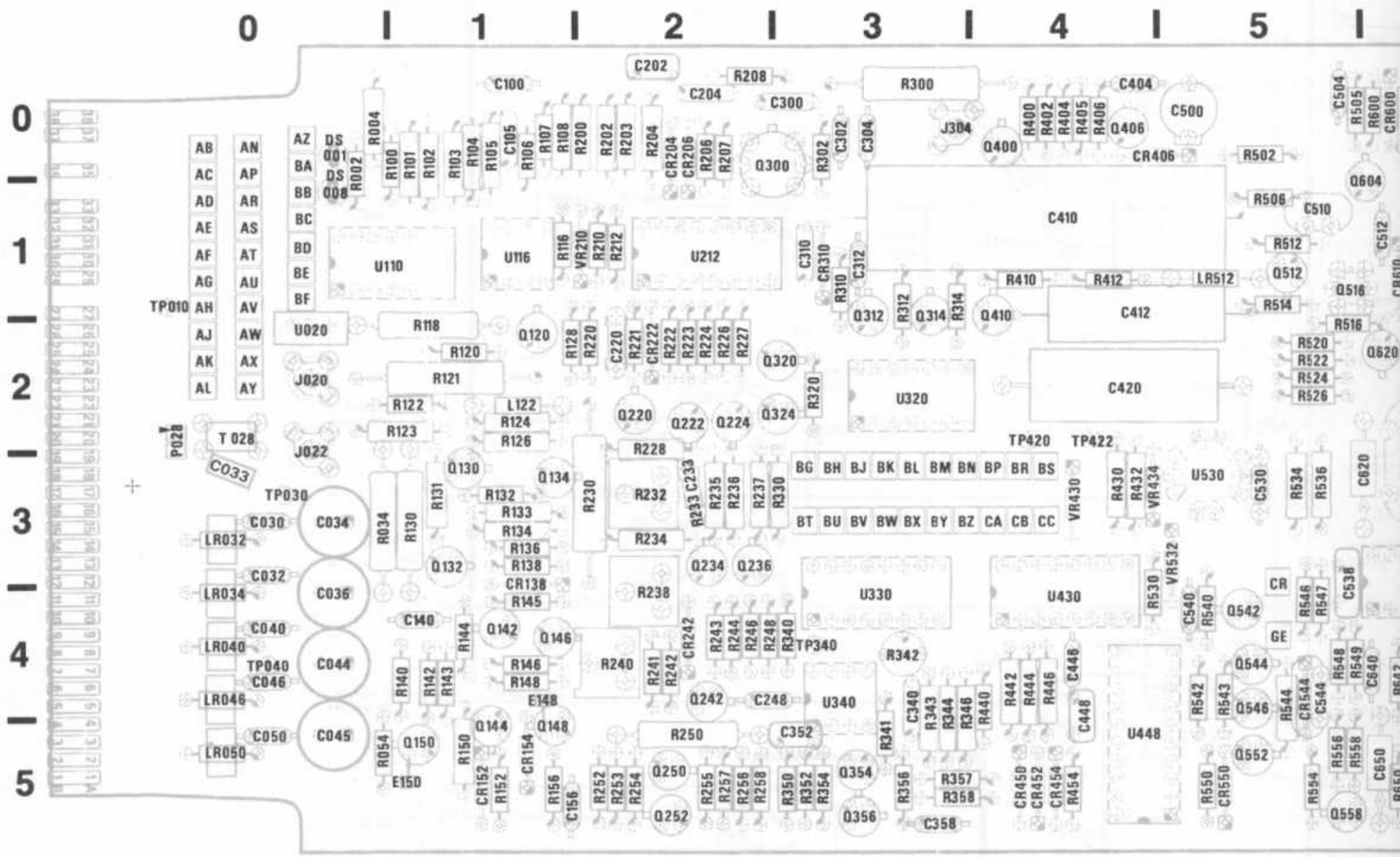


Fig. 8-4. P/O Sweep Board A20.

CKT NUMBERING EXAMPLE

R162 on A12 Assembly = R12162 in Parts List

Assembly Number

FIG. 8-4. P/O SWEEP BOARD A20

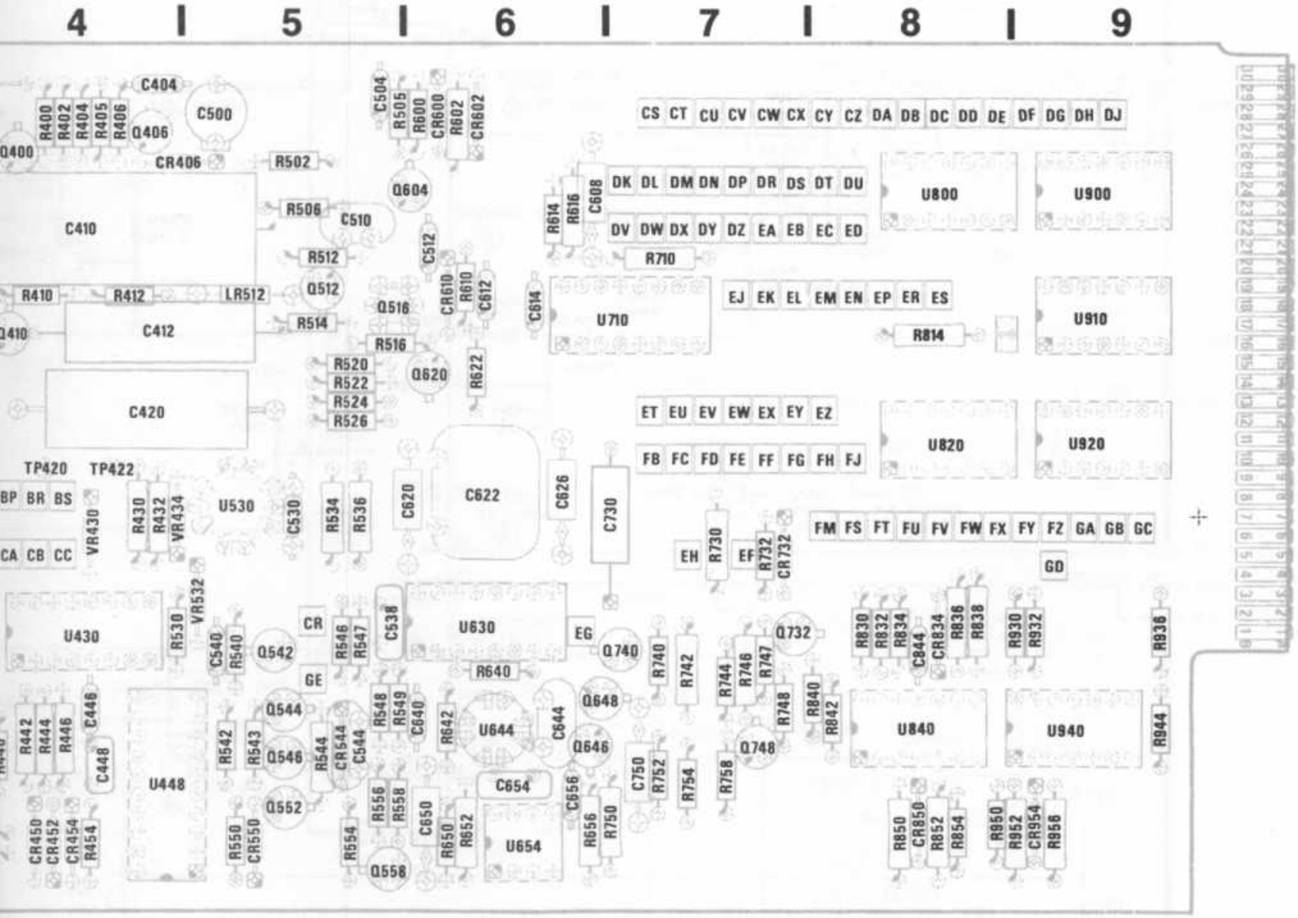
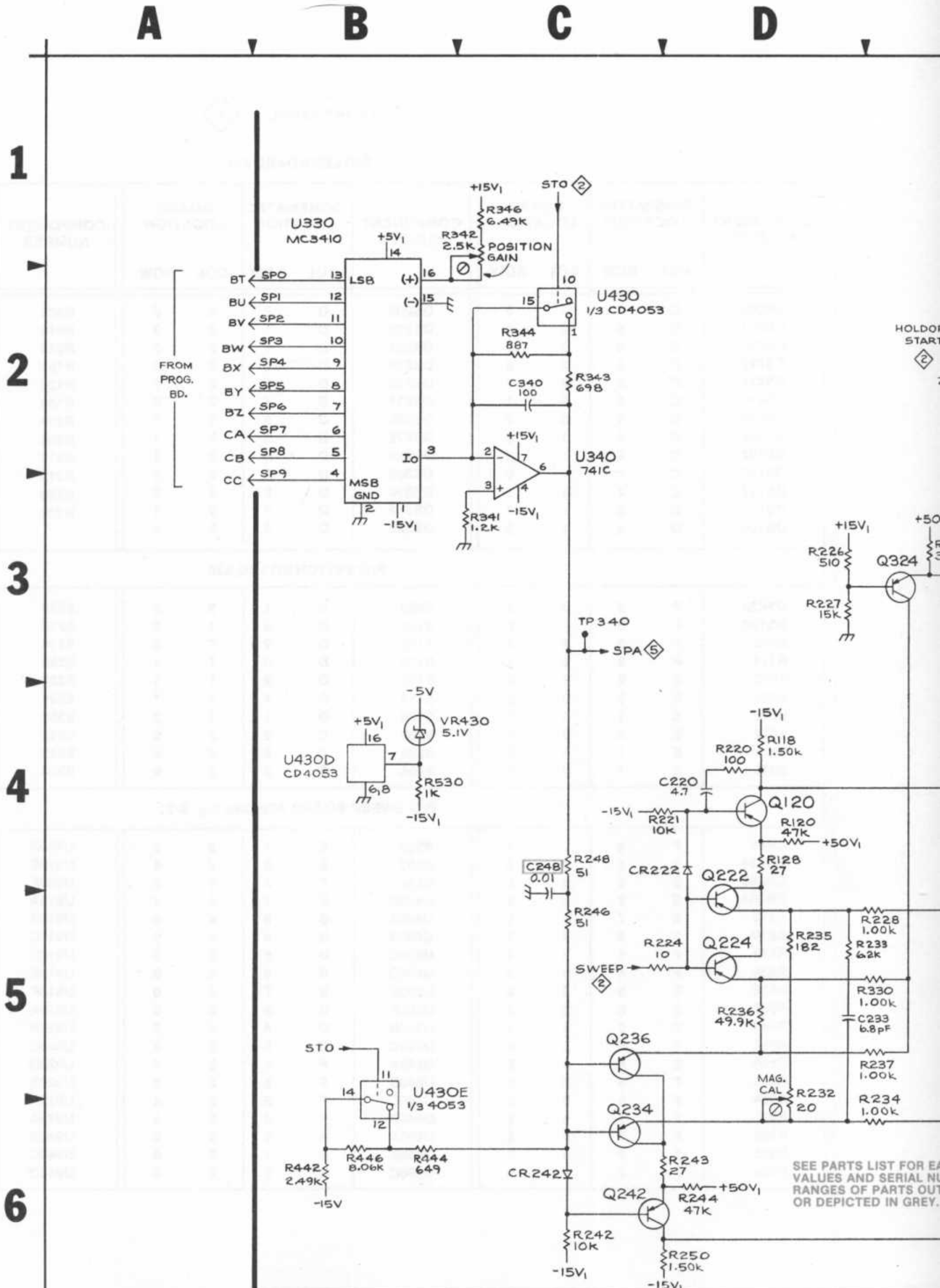


Fig. 8-4. P/O Sweep Board A20.

HORIZ PREAMP ⟨4⟩

P/O SWEEP BOARD A20

COMPONENT NUMBER	SCHEMATIC LOCATION		BOARD LOCATION		COMPONENT NUMBER	SCHEMATIC LOCATION		BOARD LOCATION	
	COL	ROW	COL	ROW		COL	ROW	COL	ROW
C156	E	1	1	5	R145	F	5	1	4
C220	C	4	2	2	R146	G	5	1	4
C233	D	5	2	3	R148	G	5	1	4
C248	B	4	2	4	R150	F	1	1	5
C340	B	2	3	4	R152	E	2	1	5
CR138	F	5	1	3	R156	E	1	1	5
CR152	E	1	1	5	R220	C	4	2	2
CR154	E	1	1	5	R221	C	4	2	2
CR222	C	4	2	2	R222	E	3	2	2
CR242	C	6	2	4	R223	E	3	2	2
E148	E	1	1	4	R224	C	5	2	2
E150	F	2	1	5	R226	D	3	2	2
L122	E	5	1	2	R227	D	3	2	2
Q120	C	4	1	2	R228	D	4	2	2
Q130	E	4	1	3	R230	E	5	2	3
Q132	E	6	1	3	R232	D	5	2	3
Q134	E	5	1	3	R233	D	5	2	3
Q142	F	5	1	4	R234	D	5	2	3
Q144	E	2	1	5	R235	D	5	2	3
Q146	F	5	1	4	R236	C	5	2	3
Q148	E	2	1	5	R237	D	5	2	3
Q150	F	1	1	5	R238	E	5	2	4
Q220	E	3	2	2	R240	F	5	2	4
Q222	C	4	2	2	R241	E	6	2	4
Q224	C	5	2	2	R242	C	6	2	4
Q234	C	5	2	3	R243	C	6	2	4
Q236	C	5	2	3	R244	C	6	2	4
Q242	C	6	2	4	R246	C	4	2	4
Q320	E	3	3	2	R248	C	4	2	4
Q324	D	3	3	2	R250	C	6	2	5
R034	F	4	0	3	R252	F	5	2	5
R054	F	2	0	5	R320	E	3	3	2
R118	D	4	1	2	R330	D	5	3	3
R120	D	4	1	2	R340	E	3	3	4
R121	D	3	1	2	R341	B	3	3	5
R122	E	4	1	2	R342	B	1	3	4
R123	E	4	1	2	R343	C	2	3	4
R124	E	5	1	2	R344	B	2	3	4
R126	E	4	1	2	R346	B	1	3	4
R128	D	4	1	2	R442	A	6	4	4
R130	F	6	1	3	R444	B	6	4	4
R131	E	6	1	3	R446	B	6	4	4
R132	F	5	1	3	R530	B	4	5	3
R133	E	5	1	3	TP340	C	3	3	4
R134	E	6	1	3	U330	B	2	3	4
R136	F	5	1	3	U340	C	2	3	4
R138	F	5	1	3	U430	C	1	4	4
R140	F	2	1	4	U430D	B	4	4	4
R142	F	1	1	4	U430E	B	5	4	4
R143	F	1	1	4	VR430	B	4	4	3


A
B
C
D
1
2
3
4
5
6
U330
MC3410
+5V1
LSB
MSB
GND
-15V1
BT SP0
BU SP1
BV SP2
BW SP3
BX SP4
BY SP5
BZ SP6
CA SP7
CB SP8
CC SP9
FROM PROG. BD.
+15V1
R346 6.49K
R342 2.5K
POSITION GAIN
STO
U430 1/3 CD4053
R344 887
C340 100
R343 698
U340 741C
R341 1.2K
TP340
SPA
-5V
VR430 5.1V
U430D CD4053
R530 1K
HOLDOFF START
R226 510
R227 15K
Q324
-15V1
R220 100
R118 1.50k
C220 4.7
R221 10K
Q120
R120 47K
+50V1
C248 0.01
R248 51
R246 51
CR222
R128 27
Q222
Q224
R224 10
SWEEP
R235 182
R228 1.00k
R233 6.2k
R330 1.00k
R236 49.9K
C233 6.8pF
Q236
R237 1.00k
MAG. CAL
R232 20
R234 1.00k
Q234
U430E 1/3 4053
R442 2.49k
R446 8.06k
R444 649
-15V
CR242
R243 27
R244 47K
Q242
R242 10K
R250 1.50k

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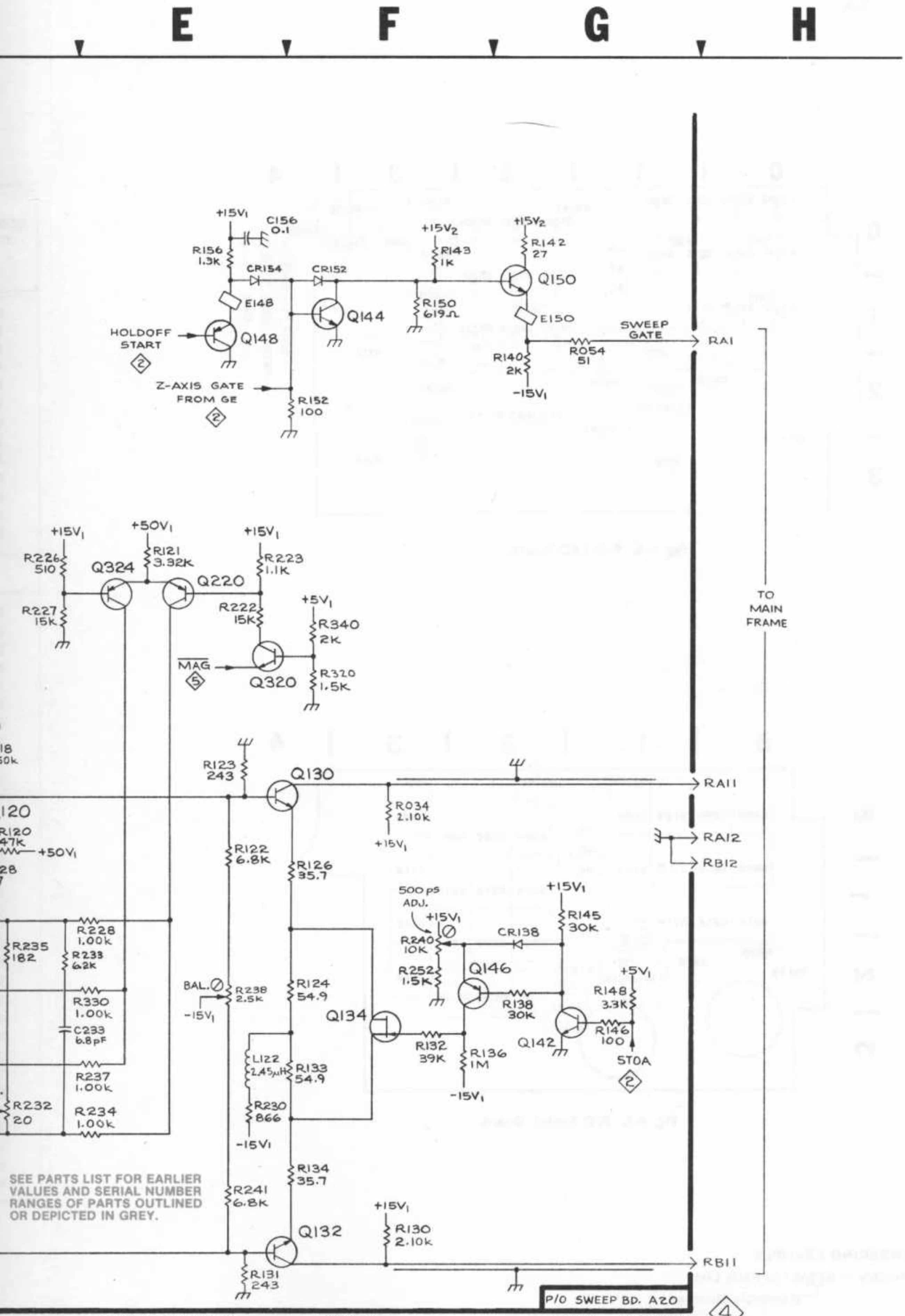


SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.

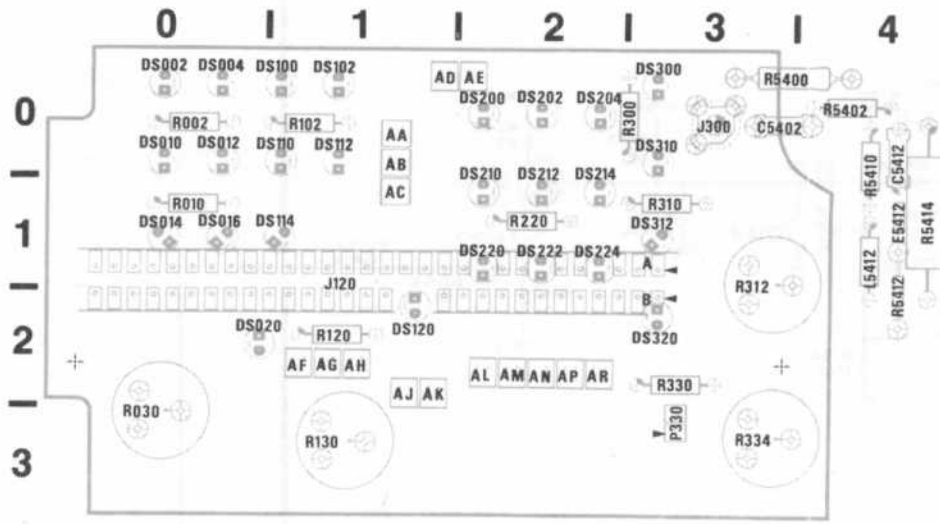


Fig. 8-5. P/O LED Board.

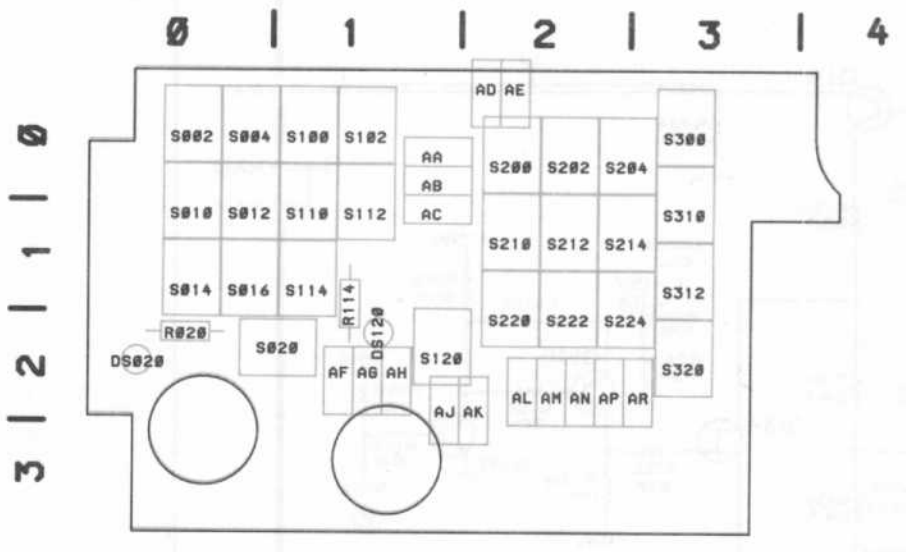


Fig. 8-6. P/O Switch Board.

CKT NUMBERING EXAMPLE

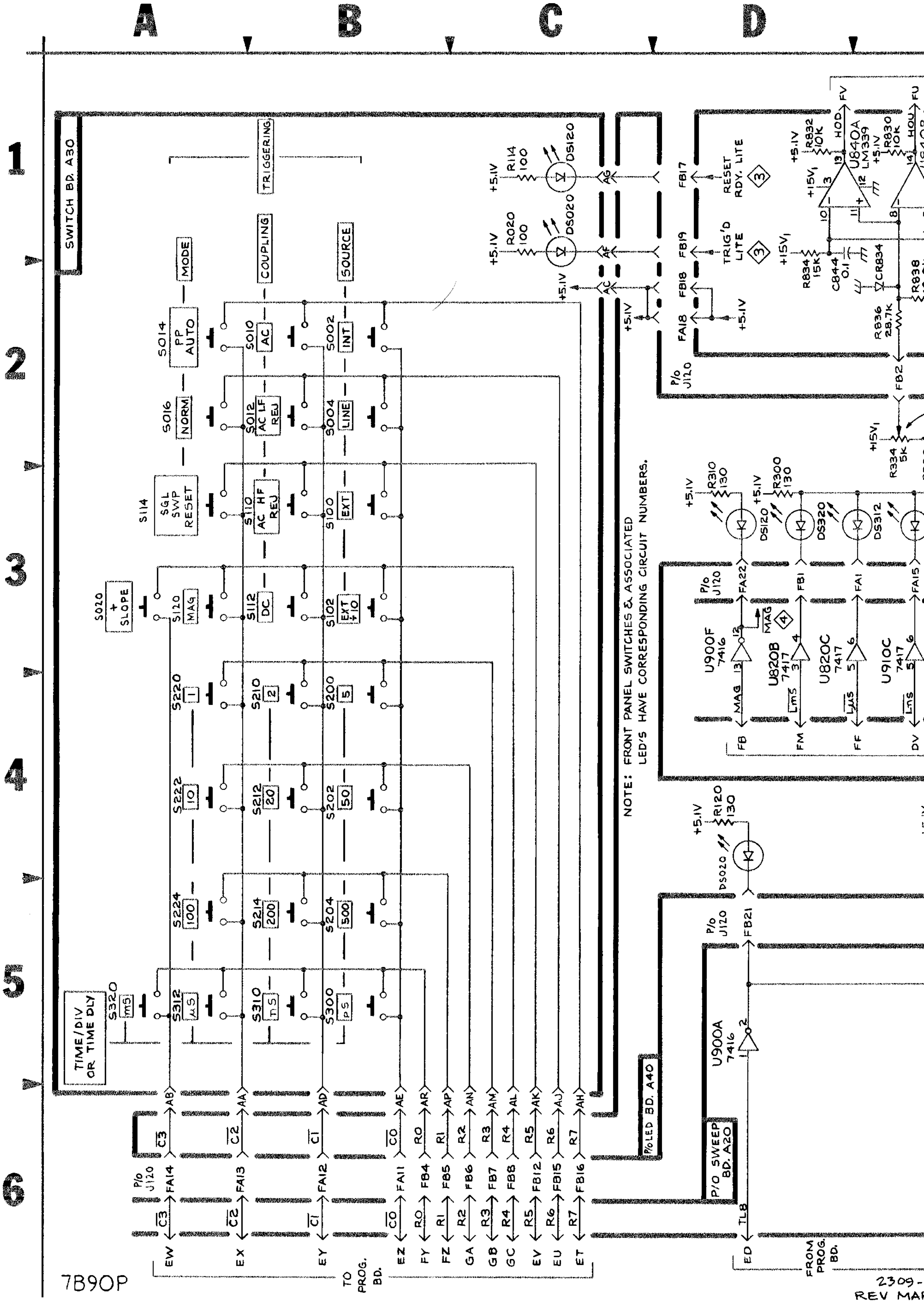
R162 on A12 Assembly = R12162 in Parts List
Assembly Number

COMP NUM
DS
DS
DS
CS
DS
DS
DS
DS
DS
DS
DS
DS
DS
DS0
DS1
R02
R11
S00
S00
S01
S01
S01
S01
C84
CR0
CR0
CR9
R81
R83
R83
R83
R83
R83
R84
R84
R85
R85
R85
R93
R93
R93
R94

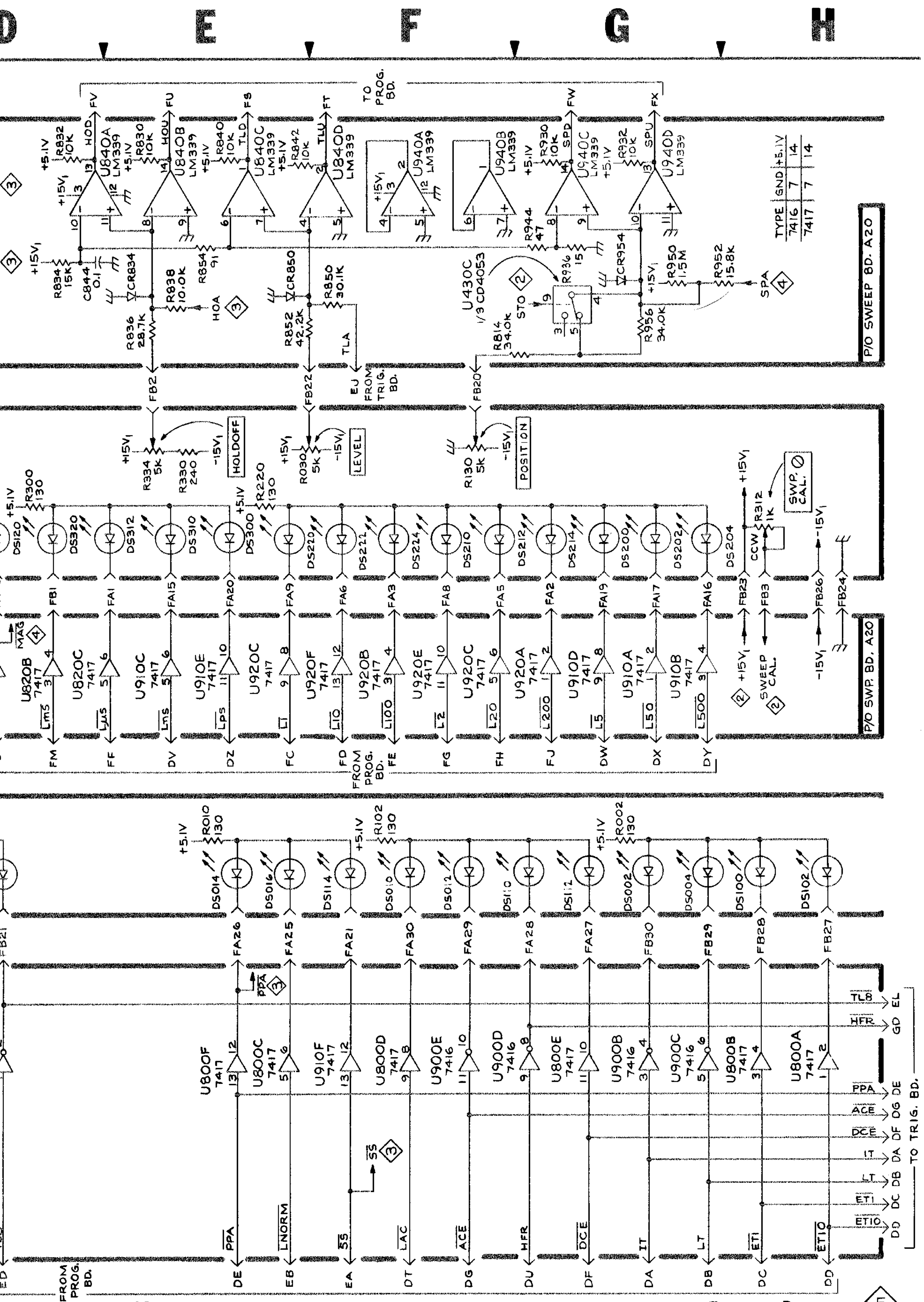
@

FRONT PANEL 5

COMPONENT NUMBER	SCHEMATIC LOCATION		BOARD LOCATION		COMPONENT NUMBER	SCHEMATIC LOCATION		BOARD LOCATION		COMPONENT NUMBER	SCHEMATIC LOCATION		BOARD LOCATION	
	COL	ROW	COL	ROW		COL	ROW	COL	ROW		COL	ROW	COL	ROW
P/O LED BOARD A40														
DS002	C	7	0	0	DS200	D	7	2	0	R002	C	7	0	0
DS004	C	6	0	0	DS202	D	7	2	0	R010	C	5	0	1
DS010	C	6	0	0	DS204	D	7	2	0	R030	E	6	0	3
CS012	C	6	0	0	DS210	D	6	2	0	R102	C	6	1	0
DS014	C	5	0	1	DS212	D	6	2	0	R120	C	4	1	2
DS016	C	5	0	1	DS214	D	7	2	0	R130	E	6	1	3
DS020	C	4	0	2	DS220	D	5	2	1	R220	D	5	2	1
DS100	C	8	1	0	DS222	D	6	2	1	R300	D	4	3	0
DS102	C	8	1	0	DS224	D	6	2	1	R310	D	4	3	1
DS110	C	7	1	0	DS300	D	5	3	0	R312	D	8	3	1
DS112	C	7	1	0	DS310	D	5	3	0	R330	E	5	3	2
DS114	C	6	1	1	DS312	D	5	3	1	R334	E	5	3	3
DS120	D	4	1	2	DS320	D	4	3	2					
P/O SWITCH BOARD A30														
DS020	F	3	0	2	S020	D	1	0	2	S210	C	2	2	1
DS120	F	3	1	2	S100	D	2	1	0	S212	C	2	2	1
R020	F	3	1	2	S102	D	2	1	0	S214	B	2	2	1
R114	F	3	1	1	S110	D	2	1	1	S220	C	1	2	2
S002	E	2	0	0	S112	D	2	1	1	S222	C	1	2	2
S004	E	2	0	0	S114	D	1	1	1	S224	B	1	2	2
S010	E	1	0	1	S120	D	1	1	2	S300	B	2	3	0
S012	E	2	0	1	S200	C	2	2	0	S310	B	2	3	1
S014	E	1	0	1	S202	C	2	2	0	S312	B	1	3	1
S016	E	1	0	1	S204	B	2	2	0	S320	B	1	3	2
P/O SWEEP BOARD A20. See Fig. 8-2.														
C844	F	4	8	4	R950	E	7	8	5	U900D	B	7	9	0
CR834	E	5	8	3	R952	E	8	9	5	U900E	B	6	9	0
CR850	E	5	8	5	R956	E	7	9	5	U900F	D	4	9	0
CR954	E	7	9	5	U430C	E	7	4	4	U910A	D	7	9	1
R814	E	7	8	1	U800A	B	8	8	0	U910B	D	7	9	1
R830	F	5	8	3	U800B	B	8	8	0	U910C	D	5	9	1
R832	F	4	8	3	U800C	B	5	8	0	U910D	D	7	9	1
R834	F	4	8	3	U800D	B	6	8	0	U910E	D	5	9	1
R836	E	5	8	3	U800E	B	7	8	0	U910F	B	6	9	1
R838	E	5	8	3	U800F	B	5	8	0	U920A	D	7	9	2
R840	F	5	8	4	U820B	D	4	8	2	U920B	D	6	9	2
R842	F	5	8	4	U820C	D	5	8	2	U920C	D	5	9	2
R850	E	6	8	5	U840A	F	4	8	4	U920D	D	6	9	2
R852	F	5	8	5	U840B	F	5	8	4	U920E	D	6	9	2
R854	F	5	8	5	U840C	F	5	8	4	U920F	D	6	9	2
R930	F	7	9	3	U840D	F	6	8	4	U940A	F	6	9	4
R932	F	7	9	3	U900A	B	4	9	0	U940B	F	6	9	4
R936	F	7	9	3	U900B	B	7	9	0	U940C	F	7	9	4
R944	F	7	9	4	U900C	B	7	9	0	U940D	F	7	9	4



A
B
C
D
1
2
3
4
5
6
SWITCH BD. A30
TRIGGERING
MODE
COUPLING
SOURCE
S014 PP AUTO
S016 NORM
S114 SGL SWP RESET
S010 AC
S012 AC LF REJ
S110 AC HF REJ
S112 DC
S002 INT
S004 LINE
S100 EXT
S102 EXT ÷10
S020 + SLOPE
S120 MAG
S220 1
S222 10
S224 100
S210 2
S212 20
S214 200
S200 5
S202 50
S204 500
S320 mS
S312 µS
S310 nS
S300 pS
TIME/DIV OR TIME DLY
+5.1V
R114 100
DS120
R020 100
DS020
FB17
FB19
FB18
FA18
RESET RDY. LITE
TRIG'D LITE
P/O J120
FB2
+15V
R334 5K
R832 10K
U840A LM339
R830 10K
R834 15K
C844 0.1
CR834
R836 28.7K
R838
HOD
HOU
FV
FU
NOTE: FRONT PANEL SWITCHES & ASSOCIATED LED'S HAVE CORRESPONDING CIRCUIT NUMBERS.
R310 130
R300 130
DS320
DS312
FA22
FB1
FA1
FA15
U900F 7416
U820B 7417
U820C 7417
U910C 7417
MAG
FB
FM
FF
DV
R120 130
FB21
U900A 7416
P/O LED BD. A40
P/O SWEEP BD. A20
TLB
ED
FROM PROG. BD.
AB AA AD AE AR AP AN AM AL AK AJ AH
C3 C2 C1 C0 R0 R1 R2 R3 R4 R5 R6 R7
FA14 FA13 FA12 FA11 FB4 FB5 FB6 FB7 FB8 FB12 FB15 FB16
EW EX EY EZ FY FZ GA GB GC EV EU ET
TO PROG. BD.
7B90P
2309-
REV MAR



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FRONT PANEL 5

FRONT PANEL

5

FIG. 8-7. P/O PROG. LOGIC BOARD A50

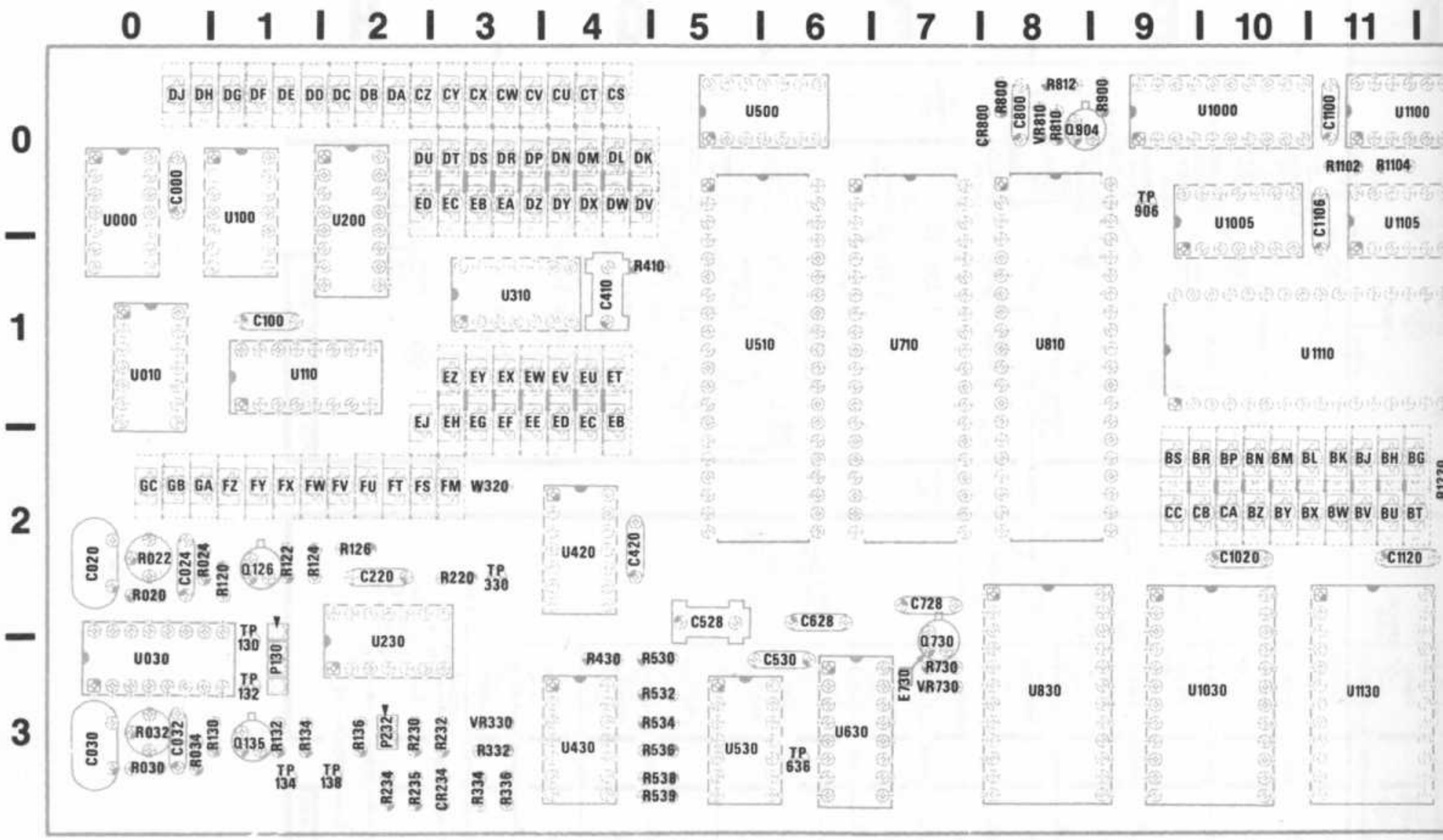


Fig. 8-7A. P/O Horizontal Programming Board A50 (SN B030837 & below).

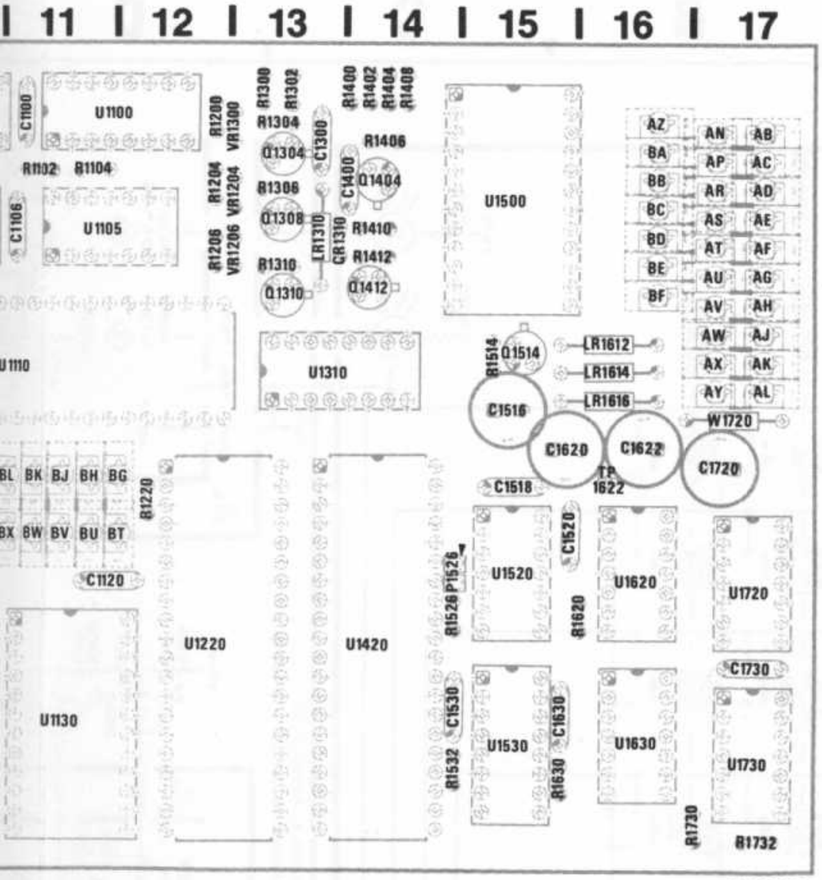
MICROPROCESSOR ⟨6⟩

P/O PROGRAMMING LOGIC BOARD A50 (SN B030837 & below).

COMPONENT NUMBER	SCHEMATIC LOCATION COL	SCHEMATIC LOCATION ROW	BOARD LOCATION COL	BOARD LOCATION ROW	COMPONENT NUMBER	SCHEMATIC LOCATION COL	SCHEMATIC LOCATION ROW
C410	G	1	4	1	U200B	G	2
C728	E	1	7	2	U230C	B	3
E730	E	1	7	3	U230F	G	2
P232	B	3	2	3	U310A	G	1
P1526	C	3	15	2	U500	B	4
Q730	E	1	7	3	U510	B	6
R126	G	2	2	2	U630	B	2
R136	B	3	2	3	U710	D	5
R410	G	1	4	1	U810	G	6
R730	E	1	7	3	U830	E	2
R1220	A	2	12	2	U1030	F	2
R1526	C	3	15	2	U1110	E	6
TP134	A	3	1	3	U1130	D	1
TP906	A	3	9	0	U1220	B	1
U100A	G	2	1	0	U1310	C	2
U100D	G	2	1	0	U1620A	C	3
U200A	G	3	2	0	VR730	E	1

CKT NUMBERING EXAMPLE

R162 on A12 Assembly = R12162 in Parts List
└Assembly Number



2309-25

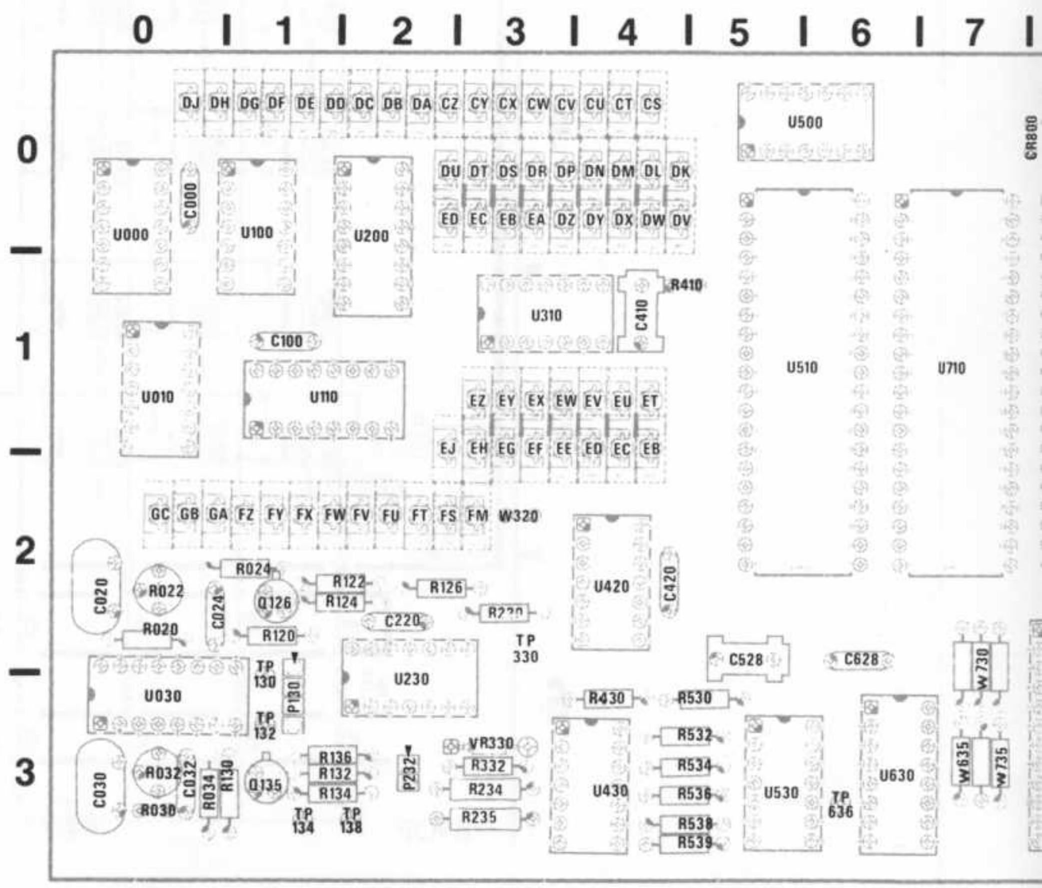
7 & below).

30837 & below).

SCHEMATIC LOCATION		BOARD LOCATION	
COL	ROW	COL	ROW
G	2	2	0
B	3	2	3
G	2	2	3
G	1	3	1
B	4	5	0
B	6	5	1
B	2	6	3
D	5	7	1
G	6	8	1
E	2	8	3
F	2	10	3
E	6	11	1
D	1	11	3
B	1	12	2
C	2	13	1
C	3	16	2
E	1	7	3

P/O PROGRAM

COMPONENT NUMBER	SCHEMATIC LOCATION	
	COL	ROW
C410	G	1
P232	B	3
P1526	C	3
R126	G	2
R136	B	3
R410	G	1
R1220	A	2
R1526	C	3
TP134	A	2
TP906	A	3
U100A	G	2
U100D	G	2
U200A	G	3
U200B	G	2
U230C	B	3
U230F	G	1



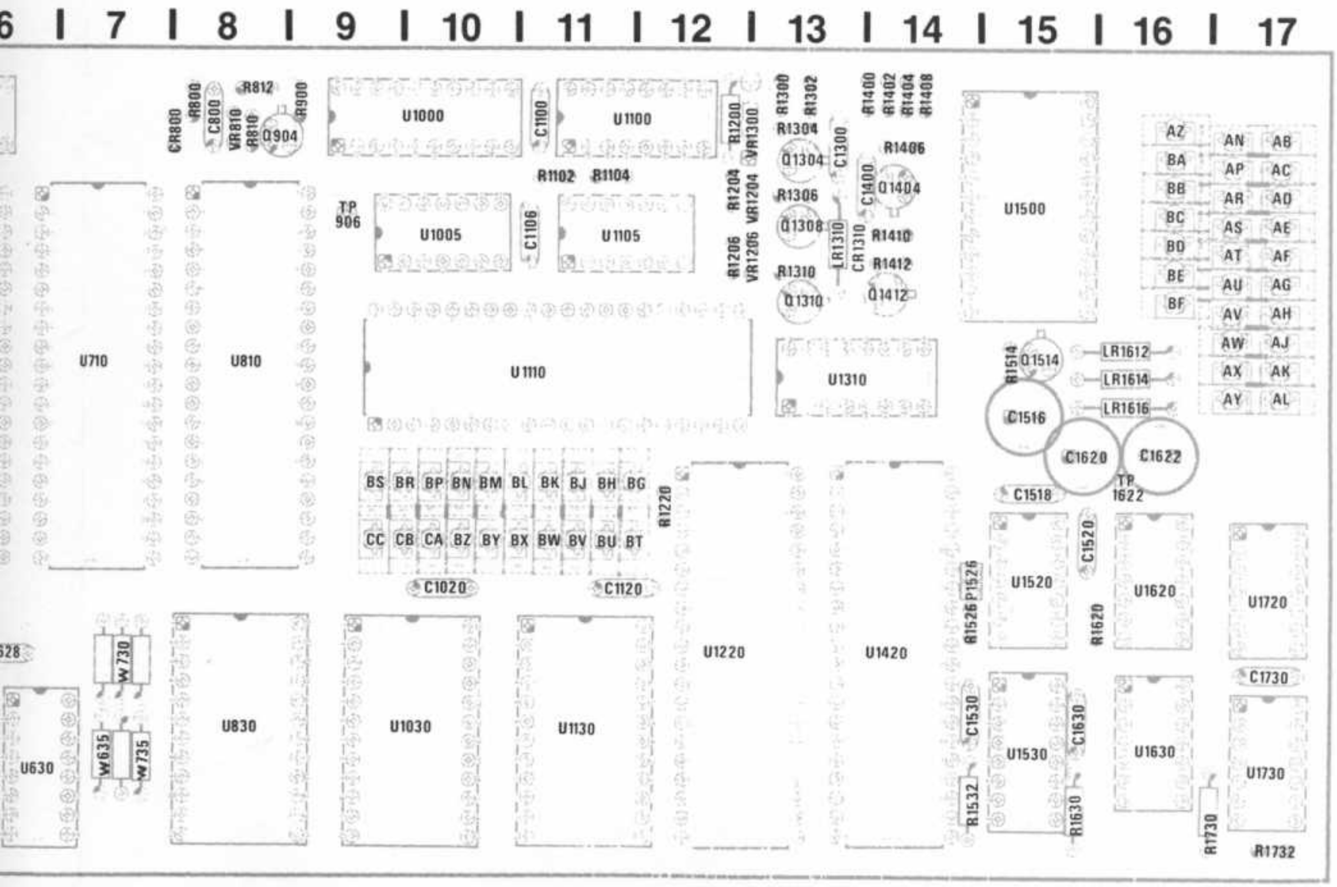
REV SEP 1982

Fig. 8-7B. P/O Horizontal P

MICROPROCESSOR ⟨6⟩

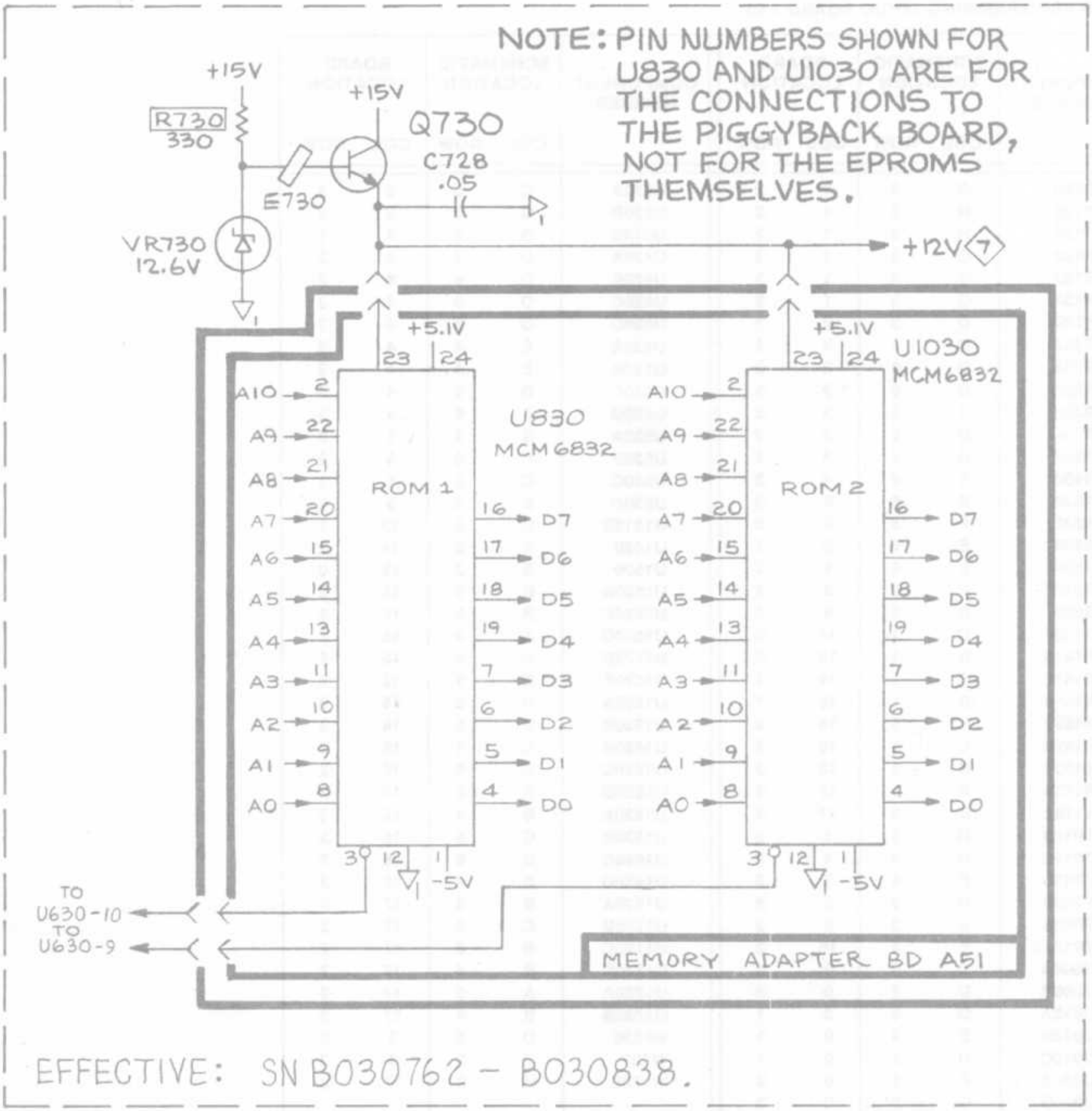
P/O PROGRAMMING LOGIC BOARD A50 (SN B030838 & up).

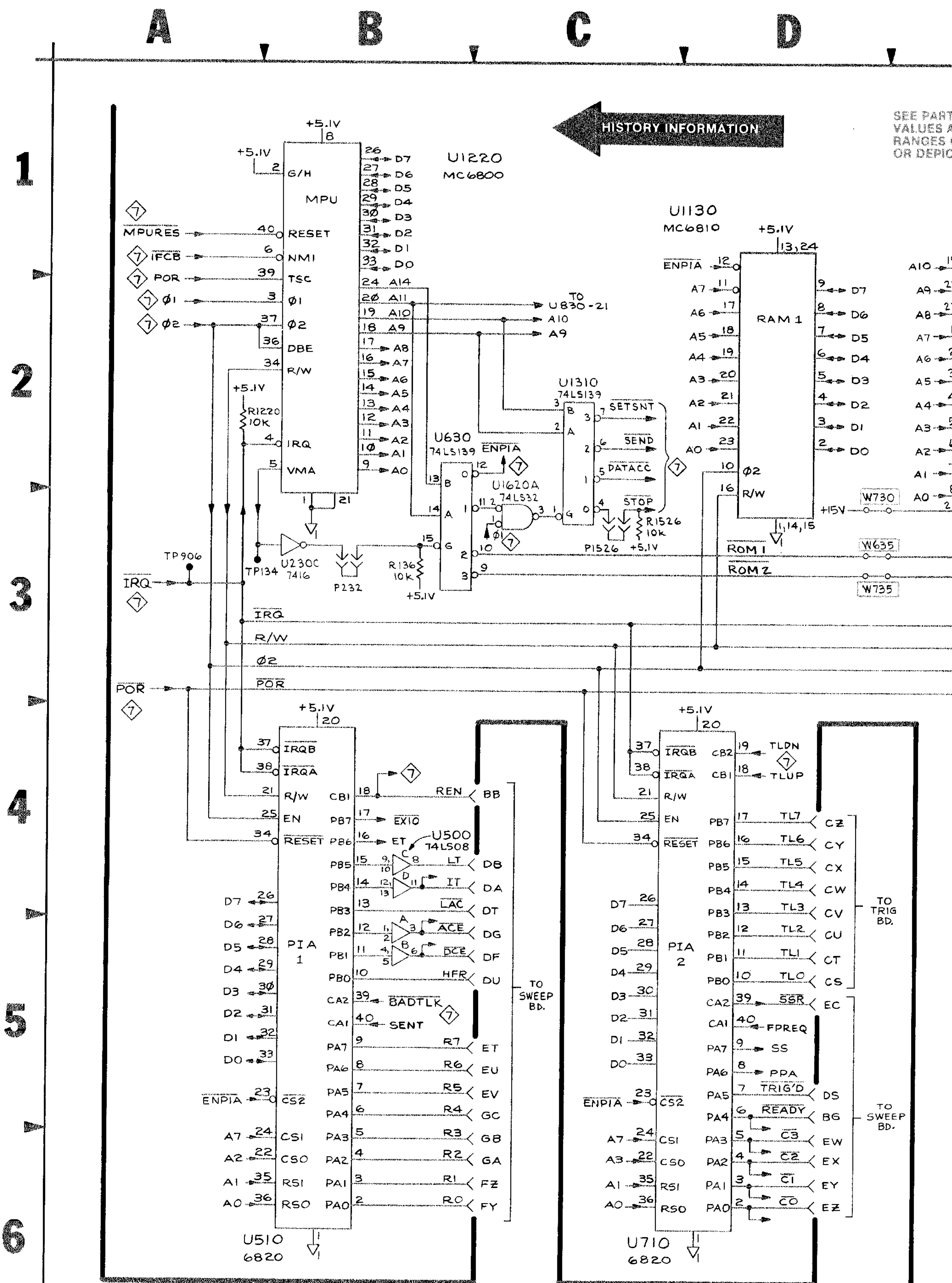
NT	SCHEMATIC LOCATION		BOARD LOCATION		COMPONENT NUMBER	SCHEMATIC LOCATION		BOARD LOCATION	
	COL	ROW	COL	ROW		COL	ROW	COL	ROW
	G	1	4	1	U310A	G	1	3	1
	B	3	2	3	U500	B	4	5	0
	C	3	15	2	U510	B	6	5	1
	G	2	2	2	U630	B	2	6	3
	B	3	2	3	U710	D	5	7	1
	G	1	4	1	U810	G	6	8	1
	A	2	12	2	U830	E	2	8	1
	C	3	15	2	U1030	F	2	10	3
	A	2	12	2	U1110	E	6	11	1
	A	3	1	3	U1130	D	1	11	3
	G	2	1	0	U1220	B	1	12	2
	G	2	1	0	U1310	C	2	13	1
	G	3	2	0	U1620A	C	3	16	2
	G	2	2	0	W635	D	3	7	3
	B	3	2	3	W730	D	3	7	2
	G	1	3	1	W735	D	3	7	3



B. P/O Horizontal Programming Board A50 (SN B030838 & up).

2309-55


NOTE: PIN NUMBERS SHOWN FOR U830 AND U1030 ARE FOR THE CONNECTIONS TO THE PIGGYBACK BOARD, NOT FOR THE EPROMS THEMSELVES.
+15V
R730
330
+15V
Q730
C728
.05
E730
VR730
12.6V
+12V
7
+5.1V
U830
MCM6832
ROM 1
U1030
MCM6832
ROM 2
A10
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
D7
D6
D5
D4
D3
D2
D1
D0
-5V
TO U630-10
TO U630-9
MEMORY ADAPTER BD A51
EFFECTIVE: SN B030762 - B030838.



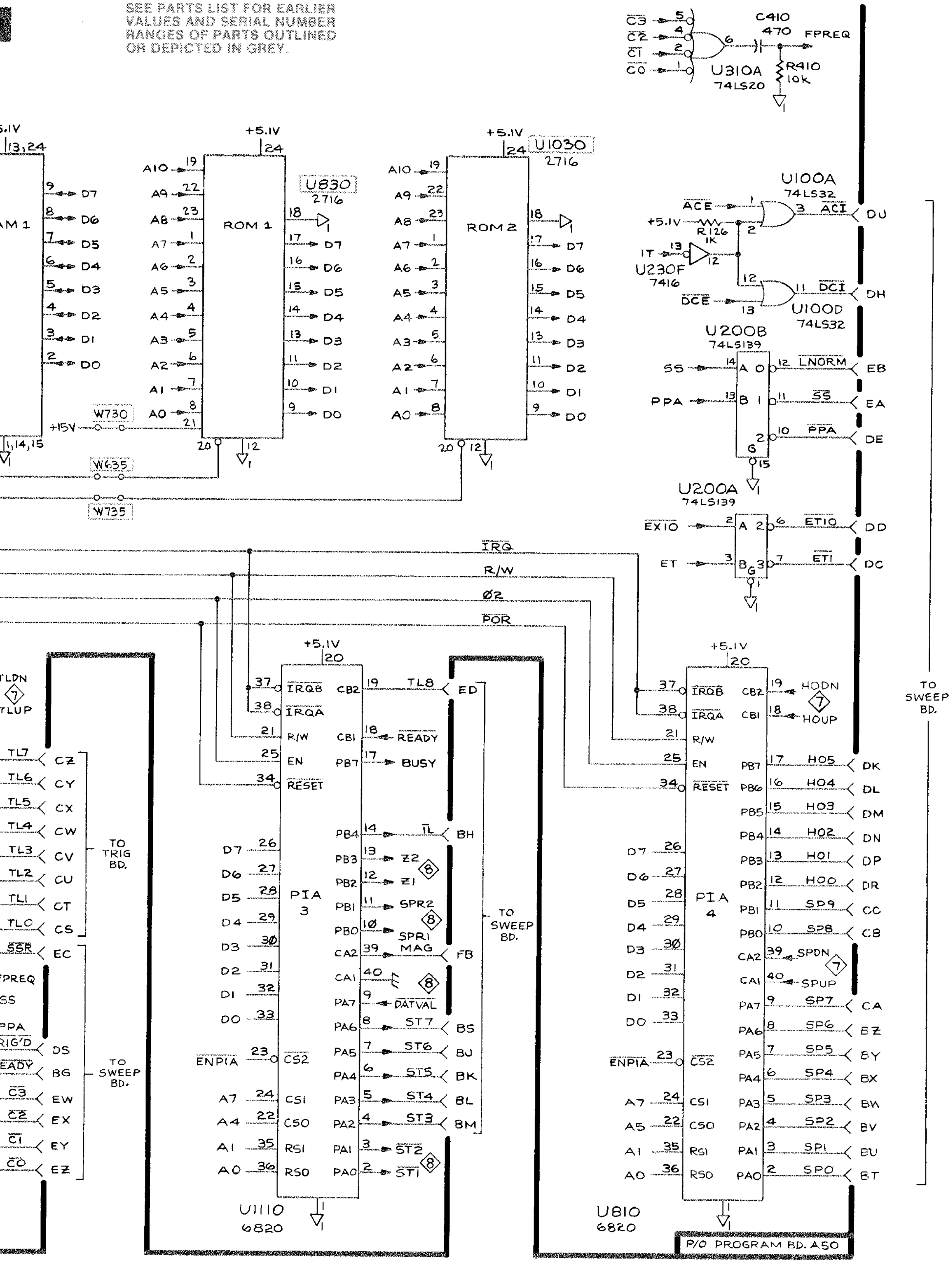
7B90P

2309-26

REV JAN 1983

D E F G H

SEE PARTS LIST FOR EARLIER VALUES AND SERIAL NUMBER RANGES OF PARTS OUTLINED OR DEPICTED IN GREY.



2309-26
REV JAN 1983

MICROPROCESSOR 6

MICROPROCESSOR 6

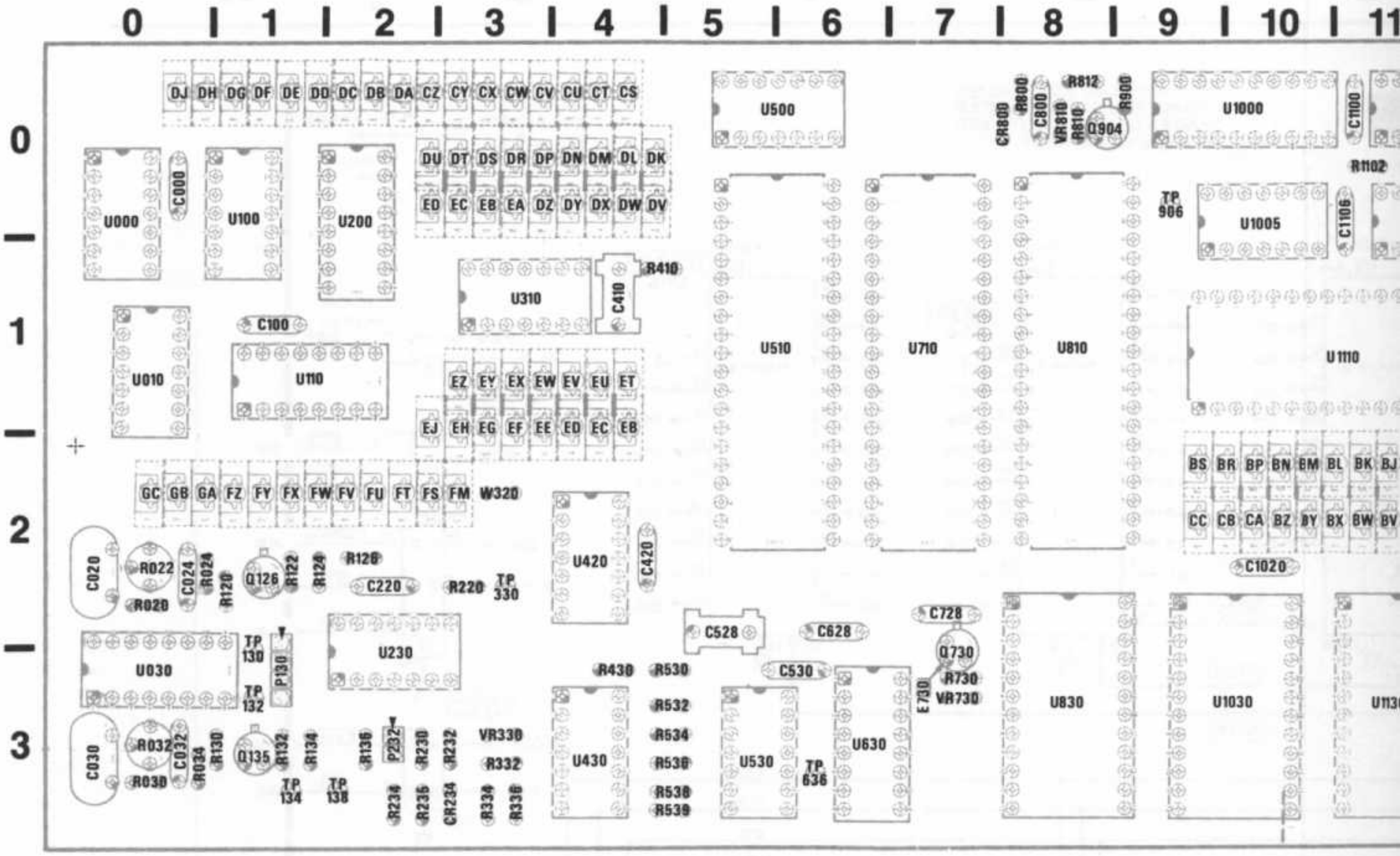


Fig. 8-8. P/O Horizontal Programming Board A50.

CKT NUMBERING EXAMPLE

R162 on A12 Assembly = R12162 in Parts List

Assembly Number

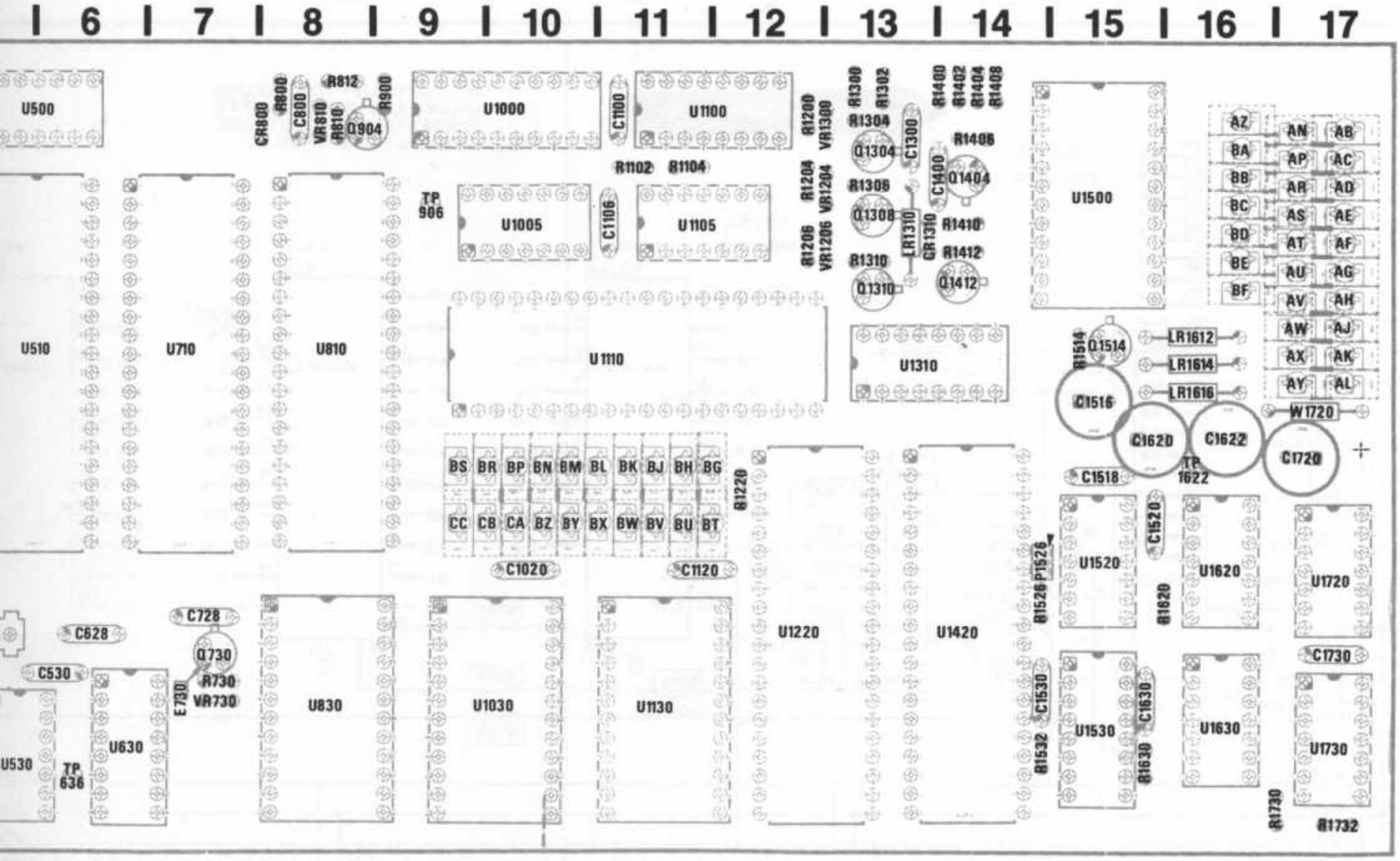


Fig. 8-8. P/O Horizontal Programming Board A50.

2309-27

*See Parts List for serial number ranges.

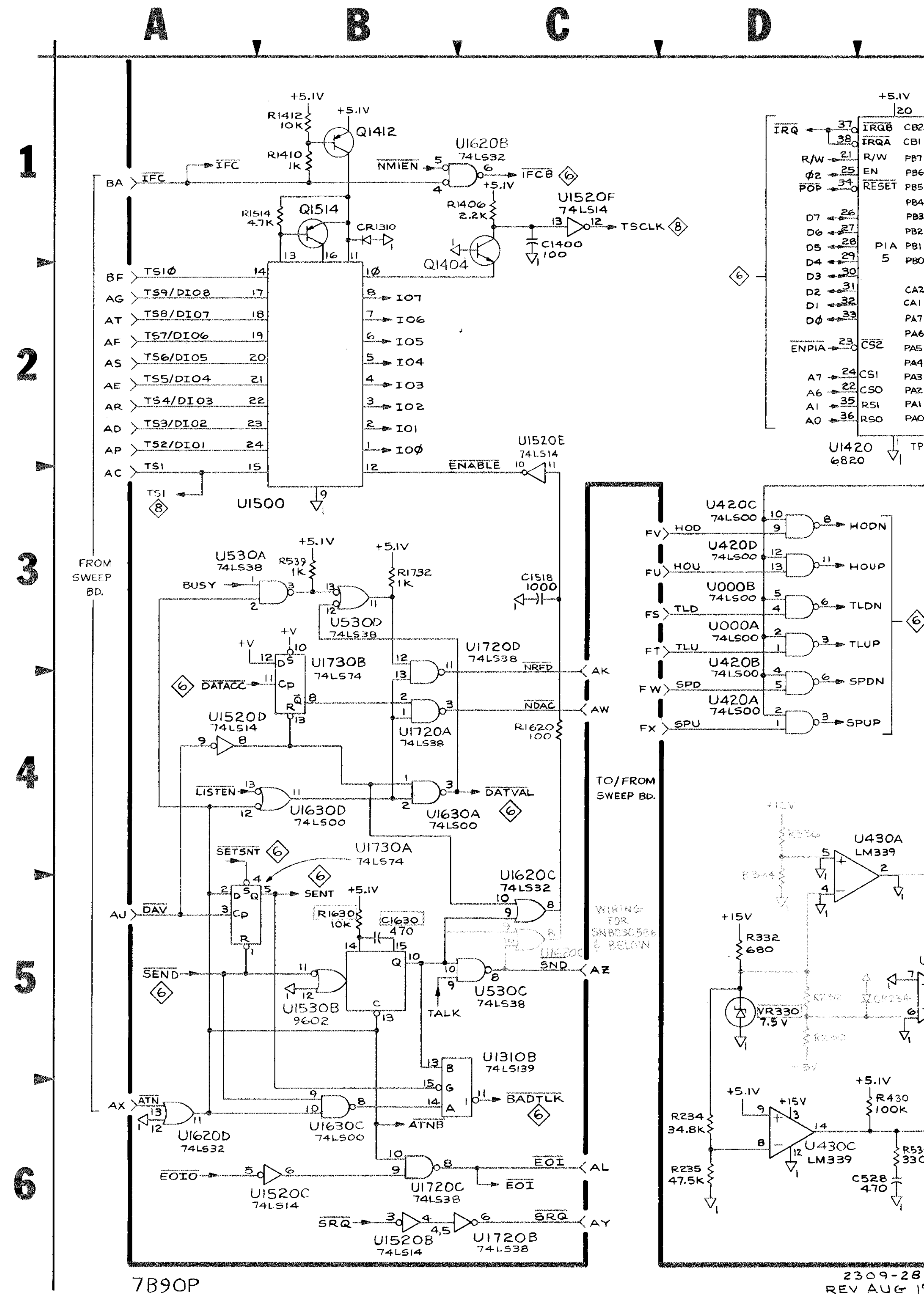
MPU CLOCK/GPIB INTERFACE ⟨7⟩

P/O PROGRAMMING LOGIC BOARD A50.

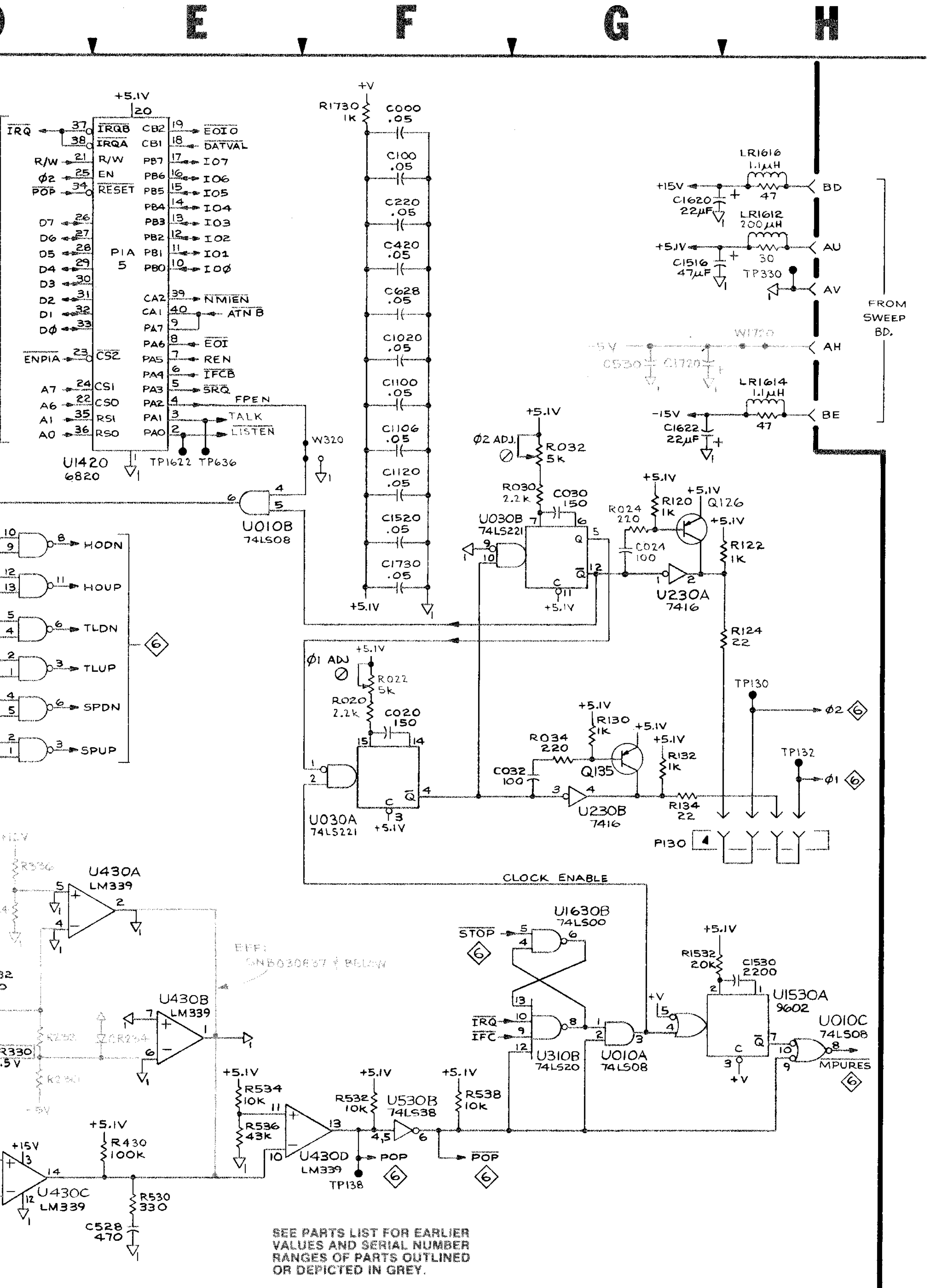
COMPONENT NUMBER	SCHEMATIC LOCATION		BOARD LOCATION	
	COL	ROW	COL	ROW
C000	F	1	0	0
C020	F	3	0	2
C024	G	3	0	2
C030	G	3	0	3
C032	G	4	0	3
C100	F	1	1	1
C220	F	1	2	2
C420	F	1	4	2
C528	E	6	5	2
C530	G	2	6	3
C628	F	2	6	2
C1020	F	2	10	2
C1100	F	2	11	0
C1106	F	2	11	0
C1120	F	3	11	2
C1400	C	1	14	0
C1516	H	1	15	1
C1518	C	3	15	2
C1520	F	3	15	2
C1530	H	5	15	3
C1620	H	1	16	2
C1622	G	2	16	2
C1630	B	5	15	3
*C1720	G	2	17	2
C1730	F	3	17	3
*CR234	E	5	3	3
CR1310	B	1	13	1
CR1614	H	2	16	1
CR1616	H	1	16	1
LR1612	H	1	16	1
P130	G	3	1	3
Q126	G3	1	2	
Q135	G	3	1	3
Q1404	C	1	14	0
Q1412	B	1	14	1
Q1514	B	1	15	1
R020	F	3	0	2
R022	F	3	0	2
R024	G	3	0	2
R030	G	3	0	3
R032	G	2	0	3
R034	G	4	0	3

COMPONENT NUMBER	SCHEMATIC LOCATION		BOARD LOCATION	
	COL	ROW	COL	ROW
R120	G	3	1	2
R122	H	3	1	2
R124	H	3	1	2
R130	G	3	1	3
R132	G	3	1	3
R134	G	3	1	3
*R230	D	5	2	3
*R232	D	5	3	3
R234	D	6	2	3
R235	D	6	2	3
R332	D	5	3	3
*R334	D	5	3	3
*R336	D	4	3	3
R430	E	6	4	3
R530	E	6	5	3
R532	F	5	5	3
R534	E	5	5	3
R536	E	6	5	3
R538	F	5	5	3
R539	B	3	5	3
R1406	C	1	14	0
R1410	B	1	14	0
R1412	B	1	14	1
R1514	B	1	15	1
R1532	H	5	15	3
R1620	C	4	16	2
R1630	B	5	15	3
R1730	F	1	17	3
R1732	B	3	17	3
TP130	H	3	1	3
TP132	H	4	1	3
TP138	F	6	2	3
TP330	H	2	3	2
TP636	E	2	6	3
TP1622	E	2	16	2
U000A	D	3	0	0
U000B	D	3	0	0
U010A	G	5	0	1
U010B	E	3	0	1
U010C	H	5	0	1
U030A	F	3	0	3
U030B	G	3	0	3

COMPONENT NUMBER	SCHEMATIC LOCATION		BOARD LOCATION	
	COL	ROW	COL	ROW
U230A	G	3	2	3
U230B	G	3	2	3
U310B	G	5	3	1
U420A	D	4	4	2
U420B	D	4	4	2
U420C	D	3	4	2
U420D	D	3	4	2
U430A	E	4	4	3
U430B	E	5	4	3
U430C	D	6	4	3
U430D	F	6	4	3
U530A	B	3	5	3
U530B	F	6	5	3
U530C	C	5	5	3
U530D	B	3	5	3
U1310B	C	5	13	1
U1420	E	2	14	2
U1500	B	2	15	0
U1520B	B	6	15	2
U1520C	B	6	15	2
U1520D	A	4	15	2
U1520E	C	3	15	2
U1520F	C	1	15	2
U1530A	H	5	15	3
U1530B	B	5	15	3
U1620B	C	1	16	2
U1620C	C	5	16	2
U1620D	A	6	16	2
U1630A	B	4	16	3
U1630B	G	5	16	3
U1630C	B	6	16	3
U1630D	B	4	16	3
U1720A	B	4	17	2
U1720B	C	6	17	2
U1720C	B	6	17	2
U1720D	B	4	17	2
U1730A	A	5	17	3
U1730B	B	4	17	3
VR330	D	5	3	3
W320	F	2	3	2
*W1720	H	2	17	2



A
B
C
D
1
2
3
4
5
6
+5.1V
R1412
10K
R1410
1K
Q1412
Q1514
R1514
4.7K
CR1310
U1620B
74LS32
NMIEN
IFCB
IFC
R1406
2.2K
U1520F
74LS14
TSCLK
C1400
100
Q1404
BA
BF
AG
AT
AF
AS
AE
AR
AD
AP
AC
TS1Ø
TS9/DIO8
TS8/DIO7
TS7/DIO6
TS6/DIO5
TS5/DIO4
TS4/DIO3
TS3/DIO2
TS2/DIO1
TS1
IO7
IO6
IO5
IO4
IO3
IO2
IO1
IOØ
ENABLE
U1520E
74LS14
U1500
FROM
SWEEP
BD.
U530A
74LS38
BUSY
R539
1K
R1732
1K
U530D
74LS38
C1518
1000
+V
U1730B
74LS74
DATACC
U1720D
74LS38
NRFD
NDAC
AK
AW
U1720A
74LS38
R1620
100
U1520D
74LS14
LISTEN
U1630D
74LS00
U1630A
74LS00
DATVAL
TO/FROM
SWEEP BD.
SETSNT
U1730A
74LS74
SENT
R1630
10K
C1630
470
U1620C
74LS32
WIRING
FOR
SN B030586
& BELOW
AJ
DAV
SEND
U1530B
9602
SND
AZ
U530C
74LS38
TALK
U1310B
74LS139
BADTLK
AX
ATN
U1620D
74LS32
U1630C
74LS00
ATNB
EOIO
U1520C
74LS14
U1720C
74LS38
EOI
AL
SRQ
U1520B
74LS14
U1720B
74LS38
AY
7B90P
IRQ
IRQB
IRQA
R/W
Ø2
EN
POP
RESET
D7
D6
D5
D4
D3
D2
D1
DØ
PIA
5
ENPIA
CS2
A7
A6
A1
A0
CS1
CS0
RS1
RS0
U1420
6820
U420C
74LS00
HOD
HODN
U420D
74LS00
HOU
HOUP
U000B
74LS00
TLD
TLDN
U000A
74LS00
TLU
TLUP
U420B
74LS00
SPD
SPDN
U420A
74LS00
SPU
SPUP
FV
FU
FS
FT
FW
FX
U430A
LM339
+15V
R332
680
VR330
7.5 V
R234
34.8K
R235
47.5K
U430C
LM339
R430
100K
C528
470
2309-28
REV AUG



P/O PROGRAM BD. A50

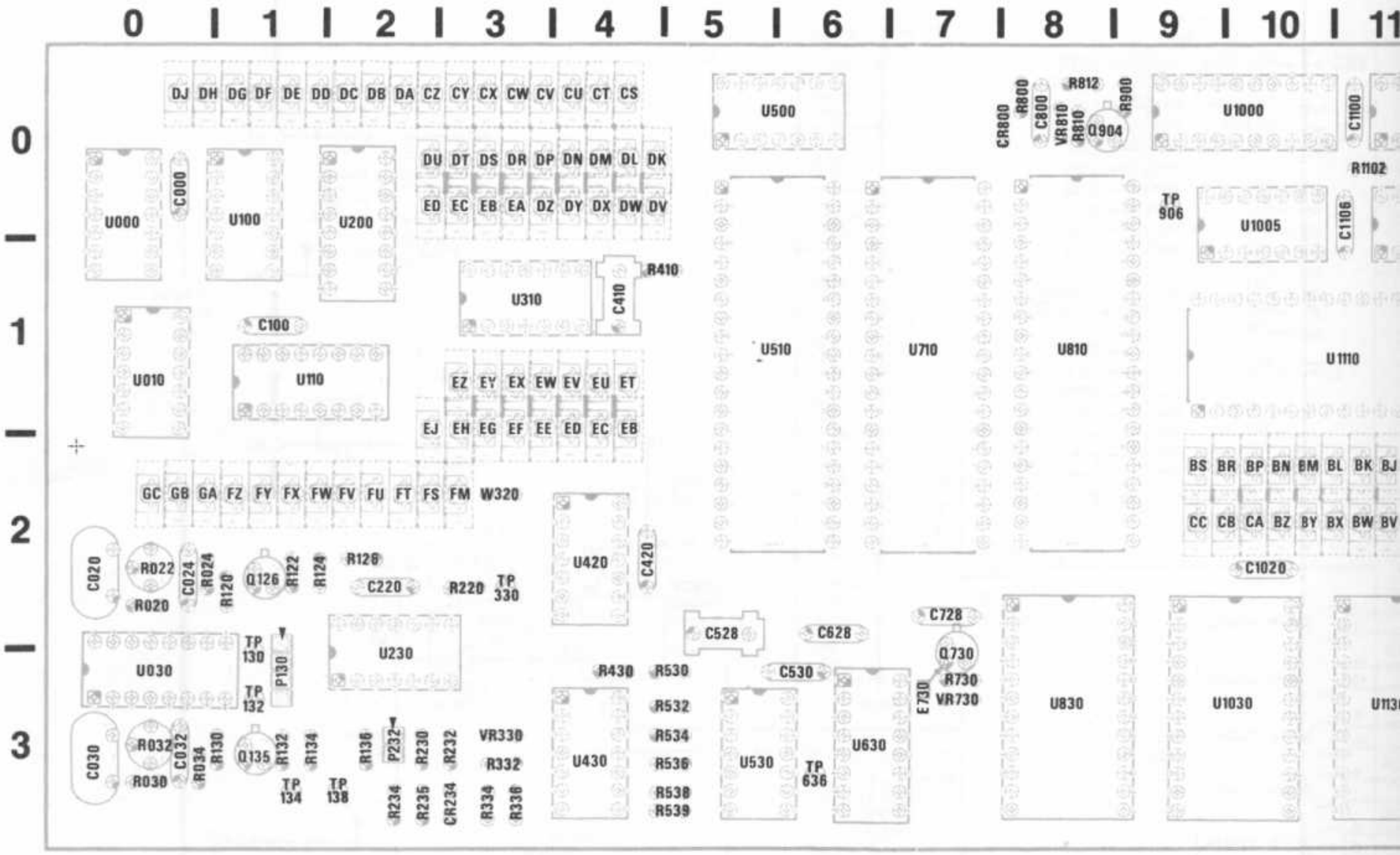


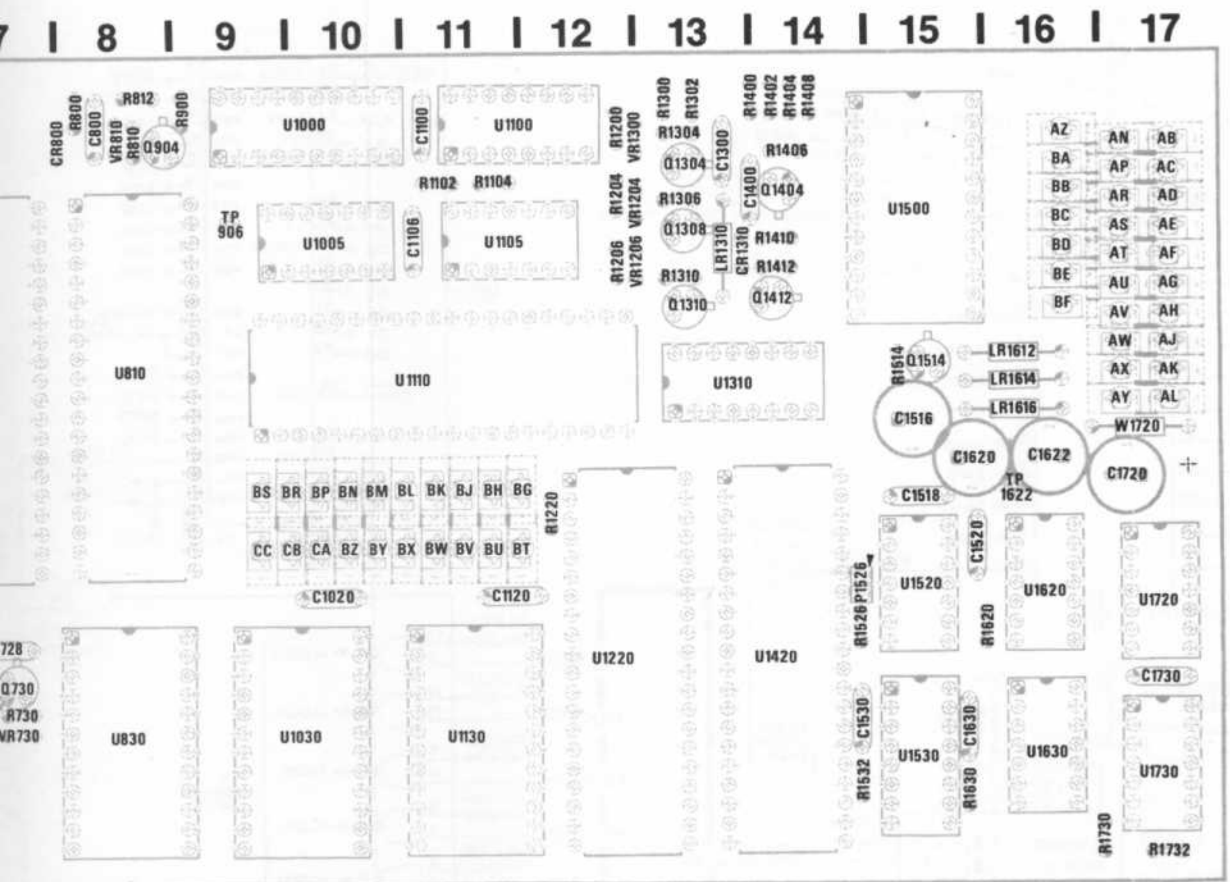
Fig. 8-9. P/O PROG. Logic Board A50.

READOUT ⟨8⟩

P/O PROGRAMMING LOGIC BOARD A50.

COMPONENT NUMBER	SCHEMATIC LOCATION COL	SCHEMATIC LOCATION ROW	BOARD LOCATION COL	BOARD LOCATION ROW	COMPONENT NUMBER	SCHEMATIC LOCATION COL	SCHEMATIC LOCATION ROW	BOARD LOCATION COL	BOARD LOCATION ROW	COMPO NUM
C800	F	3	8	0	R1206	D	1	12	0	U6
C1300	E	1	13	0	R1300	F	2	13	0	U1
CR800	F	3	8	0	R1302	F	2	13	0	U1
LR1310	E	1	13	1	R1306	E	2	13	0	U1
Q904	B	2	8	0	R1310	E	1	13	1	U1
Q1304	E	1	13	0	R1400	F	2	14	0	U1
Q1308	E	2	13	0	R1402	F	2	14	0	U1
Q1310	E	1	13	1	R1404	F	1	14	0	U1
R220	E	3	3	2	R1408	F	2	14	0	U1
R800	F	3	8	0	U000C	C	3	0	0	U1
R810	B	1	8	0	U000D	E	5	0	0	U1
R812	B	2	8	0	U010D	D	3	0	1	VR
R900	B	1	9	0	U100B	D	3	1	0	VR
R1102	E	3	11	0	U100C	D	5	1	0	VR
R1104	E	3	11	0	U110	E	5	1	1	VR
R1200	D	1	12	0	U230D	E	4	2	3	VR
R1204	D	2	12	0	U230E	F	4	2	3	

FIG. 8-9. P/O PROG. LOGIC BOARD A50



9. P/O PROG. Logic Board A50.

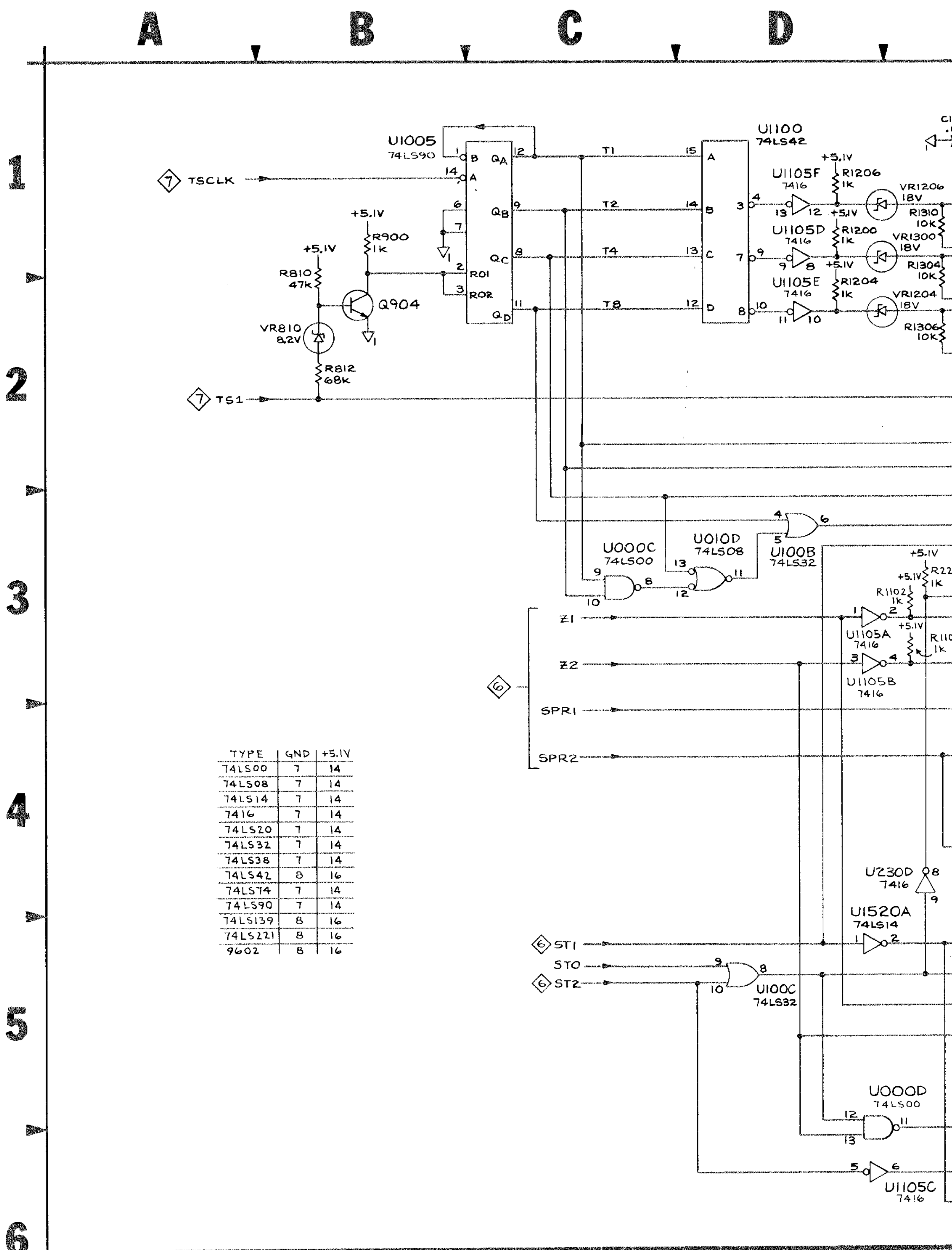
READOUT 8

OGRAMMING LOGIC BOARD A50.

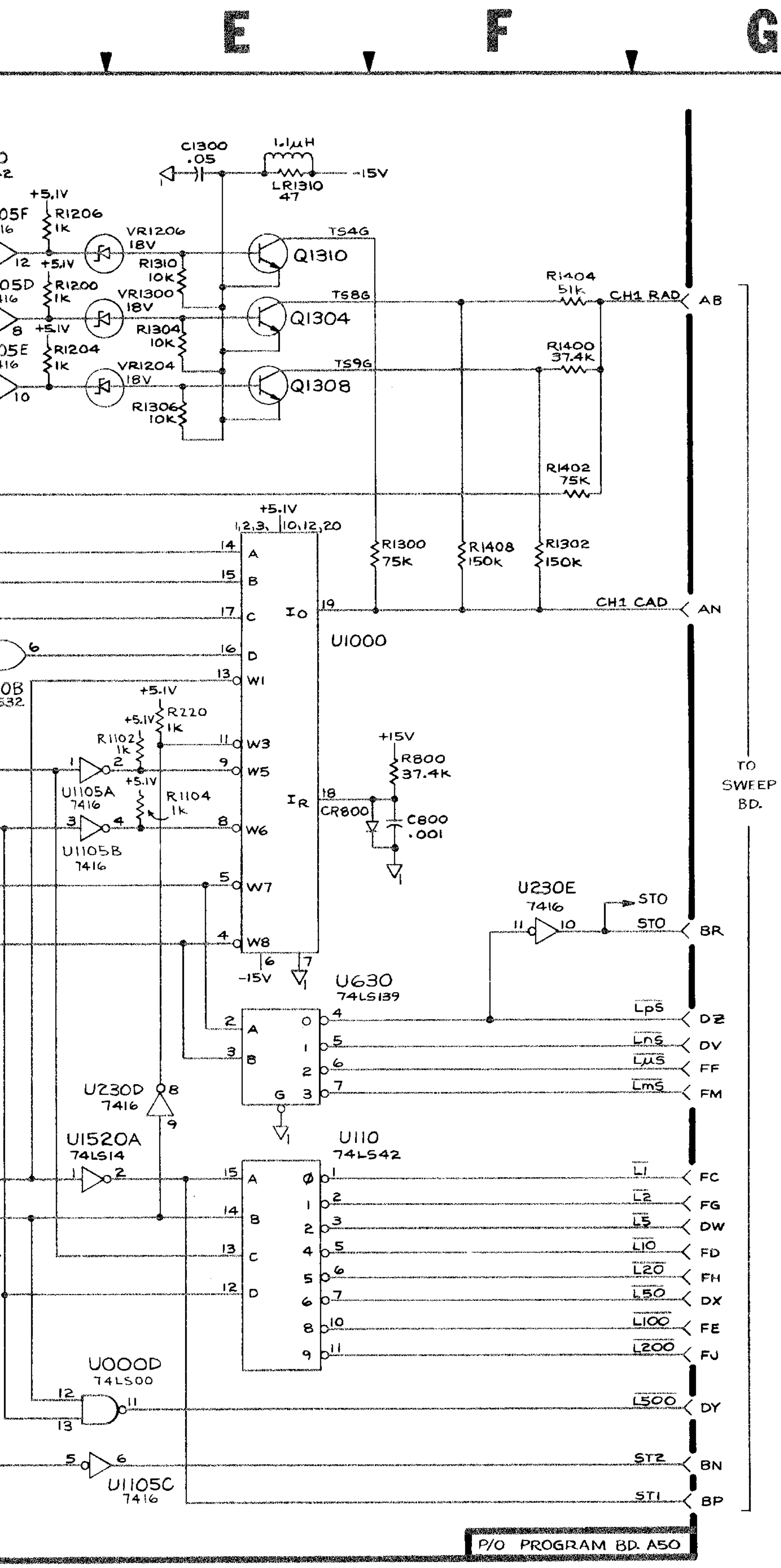
NENT ER	SCHEMATIC LOCATION		BOARD LOCATION		COMPONENT NUMBER	SCHEMATIC LOCATION		BOARD LOCATION	
	COL	ROW	COL	ROW		COL	ROW	COL	ROW
6	D	1	12	0	U630	E	4	6	3
0	F	2	13	0	U1000	E	3	10	0
2	F	2	13	0	U1005	B	1	10	0
6	E	2	13	0	U1100	D	1	11	0
0	E	1	13	1	U1105A	E	3	11	0
0	F	2	14	0	U1105B	E	3	11	0
2	F	2	14	0	U1105C	E	6	11	0
4	F	1	14	0	U1105D	D	1	11	0
8	F	2	14	0	U1105E	D	2	11	0
C	C	3	0	0	U1105F	D	1	11	0
D	E	5	0	0	U1520A	D	5	15	2
D	D	3	0	1	VR810	B	2	8	0
B	D	3	1	0	VR1204	E	2	12	0
C	D	5	1	0	VR1206	E	1	12	0
	E	5	1	1	VR1300	E	1	12	0
D	E	4	2	3	VR1304	E	2	12	0
E	F	4	2	3					

CKT NUMBERING EXAMPLE

R162 on A12 Assembly = R12162 in Parts List
Assembly Number



TYPE	GND	+5.1V
74LS00	7	14
74LS08	7	14
74LS14	7	14
7416	7	14
74LS20	7	14
74LS32	7	14
74LS38	7	14
74LS42	8	16
74LS74	7	14
74LS90	7	14
74LS139	8	16
74LS221	8	16
9602	8	16


E
F
G
H
C1300
.05
1.1µH
LR1310
47
-15V
+5.1V
R1206
1K
VR1206
18V
R1310
10K
Q1310
TS46
R1200
1K
VR1300
18V
TS86
Q1304
R1304
10K
R1204
1K
VR1204
18V
TS96
Q1308
R1306
10K
R1404
51K
CH1 RAD
AB
R1400
37.4K
R1402
75K
+5.1V
1,2,3, 10,12,20
R1300
75K
R1408
150K
R1302
150K
CH1 CAD
AN
U1000
R220
1K
R1102
1K
U1105A
7416
R1104
1K
U1105B
7416
+15V
R800
37.4K
CR800
C800
.001
TO
SWEEP
BD.
U230E
7416
STO
BR
U630
74LS139
DZ
DV
FF
FM
U230D
7416
U1520A
74LS14
U110
74LS42
L1
FC
L2
FG
L5
DW
L10
FD
L20
FH
L50
DX
L100
FE
L200
FJ
U000D
74LS00
L500
DY
ST2
BN
U1105C
7416
ST1
BP
P/O PROGRAM BD. A50

REPLACEABLE MECHANICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

SPECIAL NOTES AND SYMBOLS

X000 Part first added at this serial number

00X Part removed after this serial number

FIGURE AND INDEX NUMBERS

Items in this section are referenced by figure and index numbers to the illustrations.

INDENTATION SYSTEM

This mechanical parts list is indented to indicate item relationships. Following is an example of the indentation system used in the description column.

1 2 3 4 5 Name & Description

Assembly and/or Component
Attaching parts for Assembly and/or Component
- - - * - - -
Detail Part of Assembly and/or Component
Attaching parts for Detail Part
- - - * - - -
Parts of Detail Part
Attaching parts for Parts of Detail Part
- - - * - - -

Attaching Parts always appear in the same indentation as the item it mounts, while the detail parts are indented to the right. Indented items are part of, and included with, the next higher indentation. The separation symbol - - - * - - - indicates the end of attaching parts.

Attaching parts must be purchased separately, unless otherwise specified.

ITEM NAME

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

ABBREVIATIONS

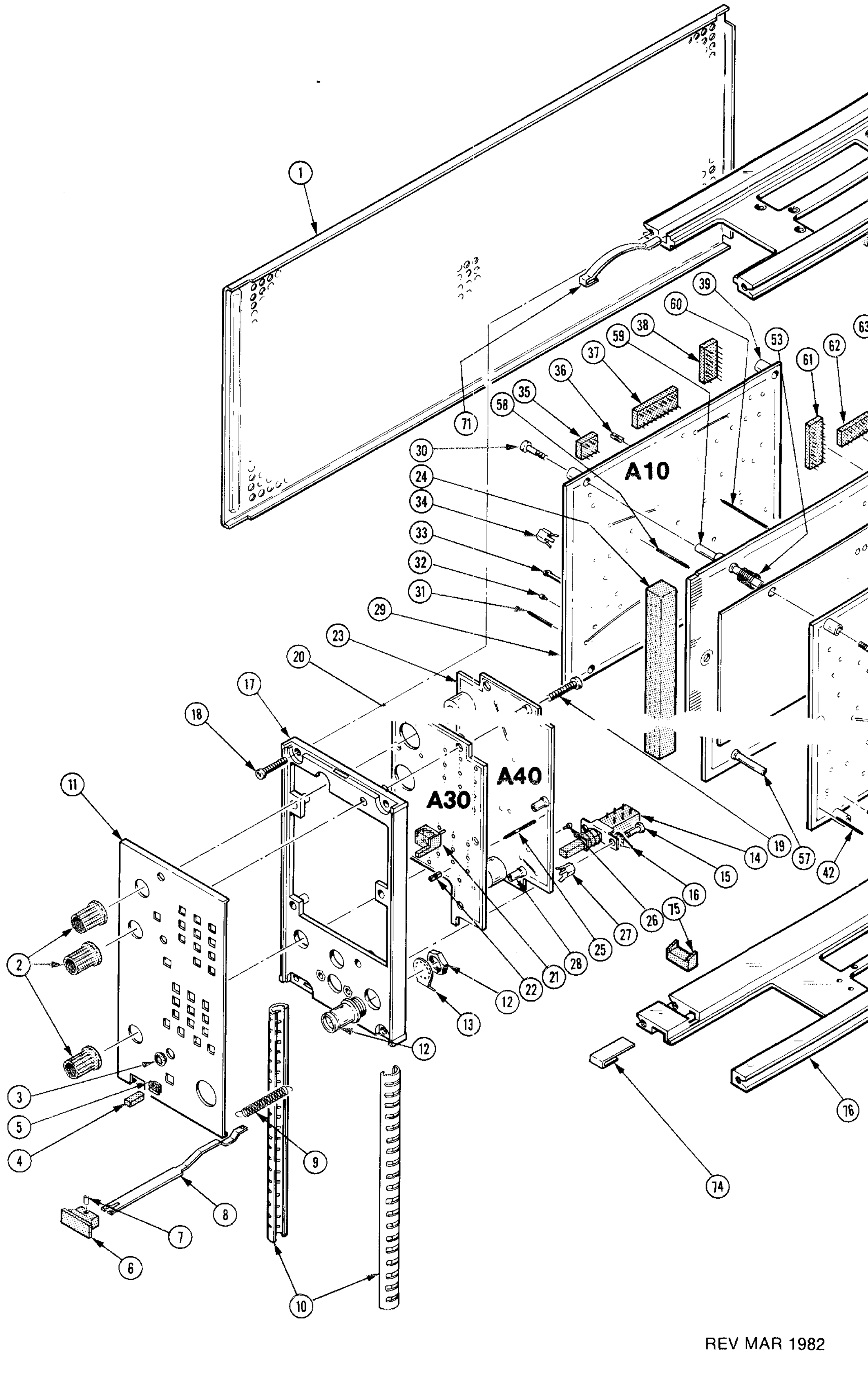
"	INCH	ELCTRN	ELECTRON	IN	INCH	SE	SINGLE END
#	NUMBER SIZE	ELEC	ELECTRICAL	INCAND	INCANDESCENT	SECT	SECTION
ACTR	ACTUATOR	ELCTLT	ELECTROLYTIC	INSUL	INSULATOR	SEMICOND	SEMICONDUCTOR
ADPTR	ADAPTER	ELEM	ELEMENT	INTL	INTERNAL	SHLD	SHIELD
ALIGN	ALIGNMENT	EPL	ELECTRICAL PARTS LIST	LPHLDR	LAMPHOLDER	SHLDR	SHOULDERED
AL	ALUMINUM	EQPT	EQUIPMENT	MACH	MACHINE	SKT	SOCKET
ASSEM	ASSEMBLED	EXT	EXTERNAL	MECH	MECHANICAL	SL	SLIDE
ASSY	ASSEMBLY	FIL	FILLISTER HEAD	MTG	MOUNTING	SLFLKG	SELF-LOCKING
ATTEN	ATTENUATOR	FLEX	FLEXIBLE	NIP	NIPPLE	SLVG	SLEEVING
AWG	AMERICAN WIRE GAGE	FLH	FLAT HEAD	NON WIRE	NOT WIRE WOUND	SPR	SPRING
BD	BOARD	FLTR	FILTER	OBD	ORDER BY DESCRIPTION	SQ	SQUARE
BRKT	BRACKET	FR	FRAME or FRONT	OD	OUTSIDE DIAMETER	SST	STAINLESS STEEL
BRS	BRASS	FSTNR	FASTENER	OVH	OVAL HEAD	STL	STEEL
BRZ	BRONZE	FT	FOOT	PH BRZ	PHOSPHOR BRONZE	SW	SWITCH
BSHG	BUSHING	FXD	FIXED	PL	PLAIN or PLATE	T	TUBE
CAB	CABINET	GSKT	GASKET	PLSTC	PLASTIC	TERM	TERMINAL
CAP	CAPACITOR	HDL	HANDLE	PN	PART NUMBER	THD	THREAD
CER	CERAMIC	HEX	HEXAGON	PNH	PAN HEAD	THK	THICK
CHAS	CHASSIS	HEX HD	HEXAGONAL HEAD	PWR	POWER	TNSN	TENSION
CKT	CIRCUIT	HEX SOC	HEXAGONAL SOCKET	RCPT	RECEPTACLE	TPG	TAPPING
COMP	COMPOSITION	HLCPS	HELICAL COMPRESSION	RES	RESISTOR	TRH	TRUSS HEAD
CONN	CONNECTOR	HLEXT	HELICAL EXTENSION	RGD	RIGID	V	VOLTAGE
COV	COVER	HV	HIGH VOLTAGE	RLF	RELIEF	VAR	VARIABLE
CPLG	COUPLING	IC	INTEGRATED CIRCUIT	RTNR	RETAINER	W/	WITH
CRT	CATHODE RAY TUBE	ID	INSIDE DIAMETER	SCH	SOCKET HEAD	WSHR	WASHER
DEG	DEGREE	IDENT	IDENTIFICATION	SCOPE	OSCILLOSCOPE	XFMR	TRANSFORMER
DWR	DRAWER	IMPLR	IMPELLER	SCR	SCREW	XSTR	TRANSISTOR

CROSS INDEX—MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip
000CY	NORTHWEST FASTENER SALES, INC.	7923 SW CIRRUS DRIVE	BEAVERTON, OR 97005
000FW	WESTERN SINTERING CO INC.	2620 STEVENS DRIVE	RICHLAND, WA 99352
00779	AMP, INC.	P.O. BOX 3608	HARRISBURG, PA 17105
09922	BURNDY CORPORATION	RICHARDS AVENUE	NORWALK, CT 06852
13511	AMPHENOL CARDRE DIV., BUNKER RAMO CORP.		LOS GATOS, CA 95030
22526	BERG ELECTRONICS, INC.	YOUK EXPRESSWAY	NEW CUMBERLAND, PA 17070
22599	ESNA, DIV. OF AMERACE CORPORATION	16150 STAGG STREET	VAN NUYS, CA 91409
73803	TEXAS INSTRUMENTS, INC., METALLURGICAL MATERIALS DIV.	34 FOREST STREET	ATTLEBORO, MA 02703
80009	TEKTRONIX, INC.	P O BOX 500	BEAVERTON, OR 97077
83385	CENTRAL SCREW CO.	2530 CRESCENT DR.	BROADVIEW, IL 60153
87308	N. L. INDUSTRIES, INC., SOUTHERN SCREW DIV.	P. O. BOX 1360	STATESVILLE, NC 28677
92101	SCHULZE MFG, 50 INGOLD RD BURLINGAME, CA 94010		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5 Name & Description	Mfr Code	Mfr Part Number
1-1	337-1064-04	B010100	B030959	2	SHIELD,ELEC:SIDE PLUG-IN UNITS	80009	337-1064-00
	337-1064-12	B030960		2	SHIELD,ELEC:SIDE FOR PLUG-IN UNIT	80009	337-1064-12
-2	366-1189-00			3	KNOB:GY,0.127 ID X 0.5 OD X 0.53	80009	366-1189-00
	----- -----			-	EACH KNOB INCLUDES:		
	213-0153-00			1	.SETSCREW:5-40 X 0.125,STL BK OXD,HEX	000CY	ORD BY DESCR
-3	358-0301-01			1	BUSHING,SLEEVE:GRAY,MOLDED	80009	358-0301-01
-4	366-1512-00			1	PUSH BUTTON:GRAY,0.18 SQ X 0.83 INCH LG	80009	366-1512-00
-5	426-1072-00			1	FRAME,PUSH BTN:PLASTIC	80009	426-1072-00
-6	366-1058-74			1	KNOB:LATCH,MARKED 7B90P	80009	366-1058-74
					**************(ATTACHING PARTS)***********		
-7	214-1095-00			1	PIN,SPG,SPLIT:0.094 OD X 0.187 INCH LONG	22599	52-022-094-0187
					************(END ATTACHING PARTS)*********		
-8	105-0076-02	B010100	B030849	1	REL BAR,LATCH:PLUG-IN UNIT	80009	105-0076-02
	105-0076-04	B030850		1	RELEASE BAR,LCH:PLUG-IN UNIT	80009	105-0076-04
-9	214-1280-00			1	SPRING,HLCPS:0.14 OD X 1.126"L,0.16"DIA	80009	214-1280-00
-10	348-0235-00			2	SHLD GSKT,ELEC:4.734 INCH LONG	92101	ORD BY DESCR
-11	333-1213-10			1	PANEL,FRONT:	80009	333-1213-10
-12	131-0955-00			1	CONN,RCPT,ELEC:BNC,FEMALE	13511	31-279
-13	210-0255-00			1	TERMINAL,LUG:0.391 ID,LOCKING,BRS CD PL	80009	210-0255-00
-14	----- -----			1	SWITCH,PUSH:(SEE S001 REPL)		
					**************(ATTACHING PARTS)***********		
-15	211-0012-00			2	SCREW,MACHINE:4-40 X 0.375,PNH STL CD PL	83385	ORD BY DESCR
-16	210-0261-00			1	TERMINAL,LUG:0.14 ID,PLAIN,BRASS	80009	210-0261-00
					************(END ATTACHING PARTS)*********		
-17	386-1447-88			1	SUBPANEL,FRONT:	80009	386-1447-88
					**************(ATTACHING PARTS)***********		
-18	213-0192-00			4	SCR,TPG,THD FOR:6-32 X 0.50 INCH,PNH STL	87308	ORD BY DESCR
-19	211-0016-00			5	SCREW,MACHINE:4-40 X 0.625 INCH,PNH STL	83385	ORD BY DESCR
					************(END ATTACHING PARTS)*********		
-20	----- -----			1	CKT BOARD ASSY:SWITCH(SEE A30 REPL)		
-21	----- -----			26	.SWITCH,PB ASSY:(SEE S30002,S30004,S30010,		
	----- -----			-	.S30012,S30014,S30016,S30020,S30100,S30110		
	----- -----			-	.S30110,S30112,S30114,S30120,S30200,S30220		
	----- -----			-	.S30204,S30210,S30212,S30214,S30220,S30222		
	----- -----			-	.S30224,S30300,S30310,S30312,S30320 REPL)		
-22	136-0263-04			15	.SOCKET,PIN TERM:FOR 0.025 INCH SQ PIN	22526	75377-001
-23	----- -----			1	CKT BOARD ASSY:L.E.D.(SEE A40 REPL)		
-24	131-1228-01			1	.CONN,RCPT,ELEC:CKT BD,30/60 CONTACT	80009	131-1228-01
-25	131-0590-00			15	.CONTACT,ELEC:0.71 INCH LONG	22526	47351
	131-0608-00			1	.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
-26	136-0252-04			1	.SOCKET,PIN TERM:U/W 0.016-0.018 DIA PINS	22526	75060-007
-27	131-1003-00			1	.CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
-28	361-0865-00			5	.SPACER,SLEEVE:0.28 L X 0.14 ID,BRS,CU,SN	80009	361-0865-00
-29	----- -----			1	CKT BOARD ASSY:TRIGGER(SEE A10 REPL)		
					**************(ATTACHING PARTS)***********		
-30	211-0155-00			4	SCREW,EXT,RLV B:4-40 X 0.375 INCH,SST	80009	211-0155-00
					************(END ATTACHING PARTS)*********		
	----- -----			-	CKT BOARD ASSY INCLUDES:		
-31	131-0608-00			1	.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
-32	136-0252-07			4	.SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-33	214-0579-00			6	.TERM,TEST POINT:BRS CD PL	80009	214-0579-00
-34	131-1003-00			4	.CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
-35	136-0514-00	B010100	B010999	1	.SKT,PL-IN ELEC:MICROCIRCUIT,8 DIP	09922	DILB8P-108
	136-0727-00	B011000	B031109	1	.SKT,PL-IN ELEK:MICROCKT,8 CONTACT	09922	DILB8P-108
-36	136-0263-07			31	.SOCKET,PIN TERM:U/W 0.025 SQ PIN	22526	ORD BY DESCR
-37	136-0634-00	B010100	B010999	1	.SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
	136-0752-00	B011000		1	.SKT,PL-IN ELEK:MICROCIRCUIT,20 DIP	09922	DILB20P-108
-38	136-0260-02	B010100	B010999	4	.SKT,PL-IN ELEK:MICROCIRCUIT,16 DIP,LOW CL	09922	DILB16P-108T
	136-0729-00	B011000	B031109	4	.SKT,PL-IN ELEK:MICROCKT,16 CONTACT	09922	DILB16P-108T
	136-0729-00	B031110		1	.SKT,PL-IN ELEK:MICROCKT,16 CONTACT	09922	DILB16P-108T
-39	361-0238-00			4	.SPACER,SLEEVE:0.25 OD X 0.34 INCH LONG	80009	361-0238-00
-40	----- -----			1	CKT BOARD ASSY:HORIZ PRGRM(SEE A50 REPL)		
					**************(ATTACHING PARTS)***********		
-41	211-0155-00			6	SCREW,EXT,RLV B:4-40 X 0.375 INCH,SST	80009	211-0155-00
					************(END ATTACHING PARTS)*********		

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5 Name & Description	Mfr Code	Mfr Part Number
1-	----- -----			-	CKT BOARD ASSY INCLUDES:		
-42	131-0608-00			8	.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
-43	214-0579-00			8	.TERM,TEST POINT:BRS CD PL	80009	214-0579-00
-44	136-0578-00	B010100	B029999	4	.SKT,PL-IN ELEK:MICROCKT,24 PIN,LOW PRFL	09922	DILB24P-108
	136-0578-00	B030000	B030761	5	.SKT,PL-IN ELEK:MICROCKT,24 PIN,LOW PRFL	09922	DILB24P-108
	136-0578-00	B030762	B030844	4	.SKT,PL-IN ELEK:MICROCKT,24 PIN,LOW PRFL	09922	DILB24P-108
	136-0757-00	B030845		4	.SKT,PL-IN ELEK:MICROCKT,40 PIN	09922	DILB40P-108
-44.1	----- -----	B030762	B030837	2	.CKT BOARD ASSY:MEMORY ADAPTER(SEE A51 REP		
-44.2	131-0608-00	B030762	B030837	48	..TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
-44.3	136-0578-00	B030762	B030837	2	..SKT,PL-IN ELEK:MICROCKT,24 PIN,LOW PRFL	09922	DILB24P-108
-45	136-0263-04			109	.SOCKET,PIN TERM:FOR 0.025 INCH SQ PIN	22526	75377-001
-46	136-0623-00	B010100	B030629	6	.SOCKET,PLUG-IN:40 DIP,LOW PROFILE	09922	DILB40P-108
	136-0623-00	B030630	B030844	1	.SOCKET,PLUG-IN:40 DIP,LOW PROFILE	09922	DILB40P-108
	136-0757-00	B030845	B031109	1	.SKT,PL-IN ELEK:MICROCKT,40 PIN	09922	DILB40P-108
-47	136-0634-00	B010100	B030844	1	.SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
	136-0752-00	B030845		1	.SKT,PL-IN ELEK:MICROCIRCUIT,20 DIP	09922	DILB20P-108
-48	131-0993-00			4	.BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
-49	361-0238-00			6	.SPACER,SLEEVE:0.25 0D X 0.34 INCH LONG	80009	361-0238-00
-50	386-1402-00			1	PANEL,REAR:	80009	386-1402-00
					**************(ATTACHING PARTS)***********		
-51	213-0192-00			4	SCR,TPG,THD FOR:6-32 X 0.50 INCH,PNH STL	87308	ORD BY DESCR
					************(END ATTACHING PARTS)*********		
-52	388-5632-01			1	CIRCUIT BOARD:SHIELD	80009	388-5632-01
-53	214-1140-00			6	SPRING,HLCPS:0.251 OD X 0.375"L,SST WIRE	80009	214-1140-00
-54	386-1657-00			3	SUPPORT,CKT BD:	80009	386-1657-00
-55	----- -----			1	CKT BOARD ASSY:SWEEP(SEE A20 REPL)		
					**************(ATTACHING PARTS)***********		
-56	211-0116-00			3	SCR,ASSEM WSHR:4-40 X 0.312 INCH,PNH BRS	83385	ORD BY DESCR
					************(END ATTACHING PARTS)*********		
	----- -----			-	CKT BOARD ASSY INCLUDES:		
-57	351-0188-00			2	.GUIDE-POST,LOCK:0.65 INCH LONG	80009	351-0188-00
-58	131-0592-00			14	.CONTACT,ELEC:0.885 INCH LONG	22526	47353
-59	351-0186-00			4	.GUIDE-POST,LOCK:0.84 INCH LONG	80009	351-0186-00
-60	131-0595-00			17	.CONTACT,ELEC:1.37 INCH LONG	22526	47355
	131-0590-00			92	.CONTACT,ELEC:0.71 INCH LONG	22526	47351
	131-0608-00			2	.TERMINAL,PIN:0.365 L X 0.025 PH BRZ GOLD	22526	48283-036
-61	136-0634-00	B010100	B010999	1	.SOCKET,PLUG-IN:20 LEAD DIP,CKT BD MTG	73803	CS9002-20
	136-0752-00	B011000		1	.SKT,PL-IN ELEK:MICROCIRCUIT,20 DIP	09922	DILB20P-108
-62	136-0260-02	B010100	B010999	5	.SKT,PL-IN ELEK:MICROCIRCUIT,16 DIP,LOW CL	09922	DILB16P-108T
	136-0729-00	B011000	B031109	5	.SKT,PL-IN ELEK:MICROCKT,16 CONTACT	09922	DILB16P-108T
-63	214-0579-00			7	.TERM,TEST POINT:BRS CD PL	80009	214-0579-00
-64	136-0252-07	B010100	B031109	16	.SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
	136-0252-07	B031110		6	.SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
-65	136-0269-02	B010100	B010999	1	.SKT,PL-IN ELEK:MICROCIRCUIT,14 DIP	09922	DILB149P-108
	136-0728-00	B011000	B031109	1	.SKT,PL-IN ELEK:MICROCKT,14 CONTACT	09922	DILB14P-108
-66	131-0993-00			1	.BUS,CONDUCTOR:2 WIRE BLACK	00779	850100-01
-67	131-1003-00			3	.CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
-68	351-0185-00			4	.GUIDE-POST,LOCK:0.65 INCH LONG	80009	351-0185-00
-69	220-0547-01			3	NUT,BLOCK:0.38 X 0.26 X 0.282 (2)4-40	000FW	ORD BY DESCR
					**************(ATTACHING PARTS)***********		
-70	211-0105-00			3	SCREW,MACHINE:4-40 X 0.188,100 DEG,FLH ST	83385	ORD BY DESCR
					************(END ATTACHING PARTS)*********		
-71	214-1061-00			1	SPRING,GROUND:FLAT	80009	214-1061-00
-72	344-0210-00			1	CLIP,SPR TNSN:	80009	344-0210-00
-73	426-0505-01			1	FR SECT,PLUG-IN:TOP	80009	426-0505-01
-74	214-1054-00			1	SPRING,FLAT:0.825 X 0.322,SST	80009	214-1054-00
-75	105-0075-00			1	BOLT,LATCH:7A & 7B SER PL-IN	80009	105-0075-00
-76	426-0499-01			1	FR SECT,PLUG-IN:BOTTOM	80009	426-0499-01
	198-3730-00			1	WIRE SET,ELEC:	80009	198-3730-00



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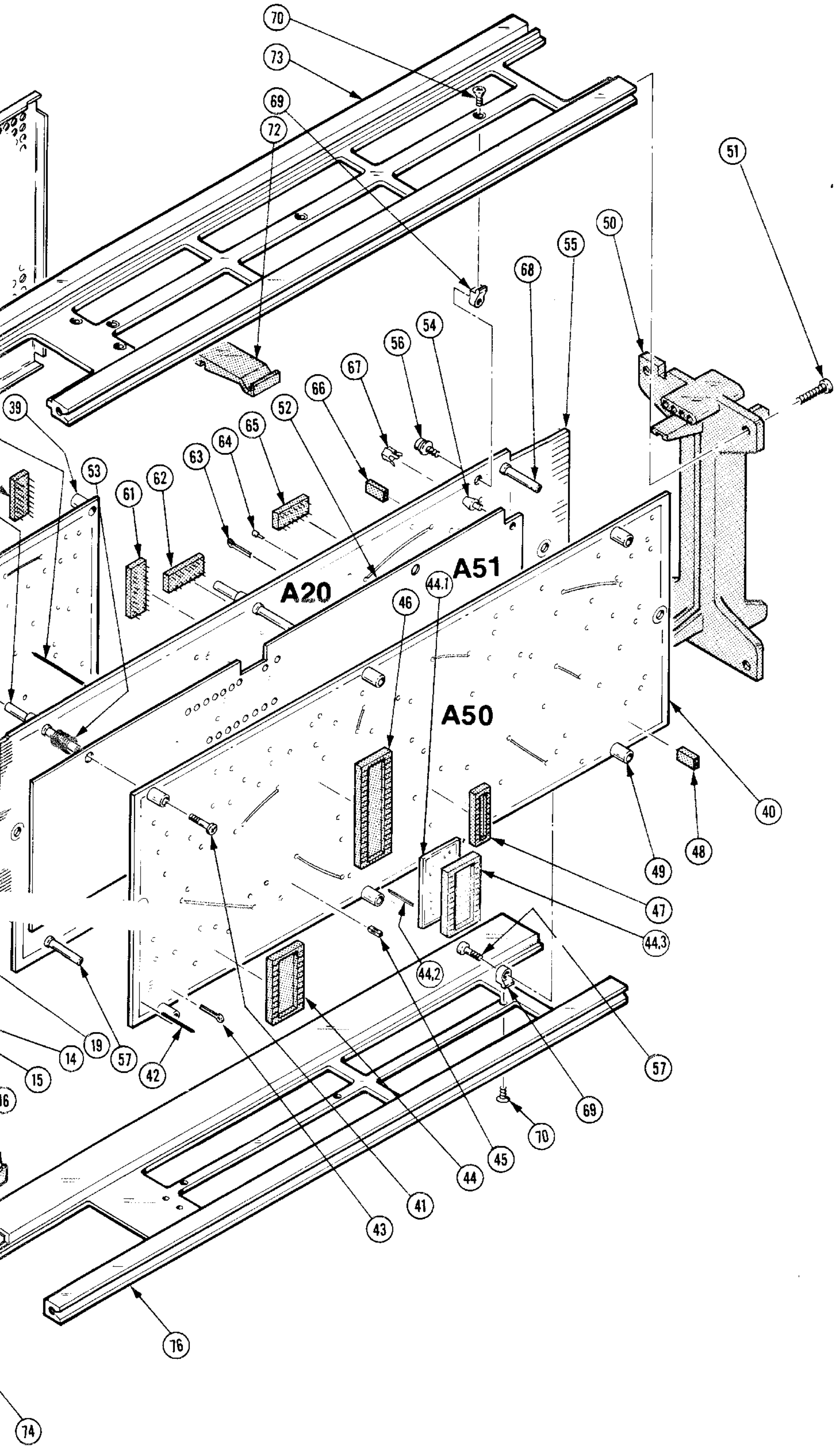

FIG 1 EXPLODED

Fig. & Index No.	Tektronix Part No.	Serial/Model No. Eff	Dscont	Qty	1 2 3 4 5 Name & Description	Mfr Code	Mfr Part Number
	070-2309-00			1	MANUAL,TECH:INSTRUCTION	80009	070-2309-00

ACCESSORIES

TABLE B
TIME/DIV CODE

Time/Div	Mag Off	Mag On
500 ps	- - -	Ø1 18
1 ns	- - -	Ø1 11
2 ns	- - -	ØØ 11
5 ns	- - -	Ø7 11
10 ns	Ø1 15	11 15
20 ns	ØØ 15	1Ø 15
50 ns	Ø7 15	17 15
100 ns	11 19	15 19
200 ns	1Ø 19	14 19
500 ns	17 19	1B 19
1 μs	15 12	19 12
2 μs	14 12	18 12
5 μs	1B 12	27 12
10 μs	19 16	25 16
20 μs	18 16	24 16
50 μs	27 16	2B 16
100 μs	25 1A	29 1A
200 μs	24 1A	28 1A
500 μs	2B 1A	47 1A
1 ms	29 13	45 13
2 ms	28 13	44 13
5 ms	47 13	4B 13
10 ms	45 17	49 17
20 ms	44 17	48 17
50 ms	4B 17	4F 17
100 ms	49 ØB	- - -
200 ms	48 ØB	- - -
500 ms	4F ØB	- - -

ANSI X3.42 Numerical Formats

<NR1> Integers with or without signs.
<NR2> Numbers (with decimal points) with or without signs.
<NR3> Signed scientific notation.

TABLE C
SINGLE-SWEEP, EOS CODE

Code	Description
xxxØ xxxx	Single sweep arm (write only).
Øxxx xxxx 1xxx xxxx	Enable end-of-sweep SRQ (write only). Disable end-of-sweep SRQ (write only).
ØØxx ØØØØ 1Øxx ØØØØ	End-of-sweep SRQ enabled (query only). End-of-sweep SRQ disabled (query only).
xØØx ØØØØ xØ1x ØØØØ	Sweep triggered (query only). Sweep not triggered (query only).
xØxØ ØØØØ xØx1 ØØØØ	Single sweep armed (query only). Single sweep disarmed (query only).

SERIAL-POLL RESPONSES

Status Byte	8	7	6	5	4	3	2	1
1) Power-on	Ø	1	Ø	x	Ø	Ø	Ø	1
2) Command error	Ø	1	1	x	Ø	Ø	Ø	1
3) Execution error	Ø	1	1	x	Ø	Ø	1	Ø
4) End-of-sweep	1	1	Ø	x	Ø	Ø	Ø	1
5) Busy	x	x	x	1	x	x	x	x

IEEE 488 Multiline Interface Messages

The 7B90P responds to the following messages:
GTL, LLO, SDC, DCL, SPE, SPD

The 7B90P does not respond to the following messages:
PPC, PPU, TCT, GET

7B90P Interface Function Subsets

SH1, AH1, TE6, LE4, SR1, RL1, PPØ, DC1, DT1, CØ

7B90P PROGRAMMABLE TIME BASE

PROGRAMMING AID

Tektronix®
COMMITTED TO EXCELLENCE

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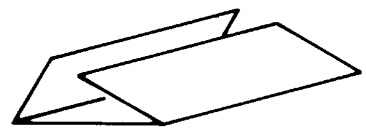
PA-2309

Remove programming aid at perforation. Fold along crease as shown:



FOLD

For additional copies of this programing aid, contact your local Tektronix Sales Engineer

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PA-2309

7B90P HIGH-LEVEL (ASCII) COMMANDS

Header	Argument	Description
MOD	PPA	Select PP Auto trigger mode.
	NOR	Select Normal trigger mode.
	SSW	Select Single-sweep triggering.
CPL	AC	Set trigger coupling to AC.
	DC	Set trigger coupling to DC.
	LFR	Set coupling to AC LF REJ.
	HFR	Set coupling to AC HF REJ.
SRC	INT	Select Internal trigger source.
	LIN	Select Line-freq trigger source.
	EXT	Select External trigger source.
	E1Ø	Select EXT÷10 trigger source.
SLO	POS	Set trigger slope positive.
	NEG	Set trigger slope negative.
LEV	xxxx	Set trigger level (−6.4 to +6.35 div).[1]
T/D	xxxx	Set TIME/DIV (5E-10 to 5E-1 sec).[2]
MAG	ON	Turn sweep magnifier on.
	OFF	Turn sweep magnifier off.
POS	xxxx	Set trace position (−6.4 to +6.39 div).[1]
HOL	xxxx	Set trigger hold-off (0 to 63, uncal).[3]
EOS	ON	Enable end-of-sweep SRQ.
	OFF	Disable end-of-sweep SRQ.
TRI	ON	Trigger light is on. } query only
	OFF	Trigger light is off. } query only
SSW	ARM	Arm single sweep.
	DIS	Single sweep is disarmed. } query only
ID		Returns plug-in type. } query only
SET		Queries all functions. (except the query-only ones.) } query only

[1] Accepts <NR1>, <NR2>, or <NR3>; query returns <NR2>.
[2] Accepts <NR1>, <NR2>, or <NR3>; query returns <NR3>.
[3] Accepts <NR1>; query returns <NR1>.

TABLE A
7B90P LOW-LEVEL (HEXADECIMAL) CODES

Address	Data	Description
ØØ		Plug-in Type. (query only)
	9Ø	Any data other than hex 9Ø written to this address causes a command error.
Ø1		Trigger Hold-Off
	xx	Range ØØ to FC; low two bits must be zero.
Ø2	xx	Trace Position (high two bits)
Ø3	xx	Trace Position (low eight bits) Position range is −6.39 divisions (ØØØØ) to +6.4 divisions (Ø3FF). Center screen = Ø2ØØ. Step size = 0.0125 div.
Ø4		Sweep Magnifier[1]
	ØØ	Magnifier Off
	Ø8	Magnifier On
Ø5		Sweep Rate
	xx	High bits, see Table B (reverse side).
Ø6		Sweep Rate
	xx	Low bits, see Table B (reverse side).
Ø7		Trigger Level
	xx	Range is −6.4 divisions (ØØ) to +6.35 divisions (FF). Step size = 0.05 div.
Ø8		Trigger Coupling
	Ø2	AC
	ØE	AC LF REJ
	ØB	AC HF REJ
	Ø8	DC

[1] To set read-out and front panel, sweep rate low bits must be changed also. If not changed, sweep is still magnified, but T/D? will return T/D error.

LOW-LEVEL CODES (cont)

Address	Data	Description
Ø9		Trigger Source
	1Ø	Internal
	2Ø	Line-frequency
	CØ	External
	4Ø	External÷10
ØA		Trigger Slope
	ØØ	Negative
	Ø8	Positive
ØB		Trigger Mode
	ØØ	Normal
	4Ø	PP Auto
	8Ø	Single Sweep
ØC		Single Sweep Arm, End-of-Sweep SRQ Enable.
	xx	See Table C (reverse side).

HIGH-LEVEL MESSAGE FORMATS:

SET: <header> <argument>

QUERY: <header> ? ; responds with <argument>

LOW-LEVEL MESSAGE FORMATS

SET: 15*
<address>
<data>
[<data>
.
.]
<checksum>

QUERY: 11*
[<address>
[<count>]]
<checksum>

* hexadecimal

The <address> and <data> bytes are taken from Table A. The <checksum> is the 2's complement of the modulo-256 sum of the preceding message bytes.

MANUAL CHANGE INFORMATION

At Tektronix, we continually strive to keep up with latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipping requirements, we can't get these changes immediately into printed manuals. Hence, your manual may contain new change information on following pages.

A single change may affect several sections. Since the change information sheets are carried in the manual until all changes are permanently entered, some duplication may occur. If no such change pages appear following this page, your manual is correct as printed.