Tektronix®
COMMITTED TO EXCELLENCE

PLEASE CHECK FOR CHANGE INFORMATION AT THE REAR OF THIS MANUAL.

CG 5001/CG 551AP

PROGRAMMABLE CALIBRATION GENERATOR

(SN B050000 AND UP)
VOL. 1
With Options

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
Beaverton, Oregon 97077

070-4768-00
Product Group 76

Serial Number _____

First Printing AUG 1983
Revised JAN 1985

INSTRUMENT SERIAL NUMBERS

Each instrument has a serial number on a panel insert, tag, or stamped on the chassis. The first number or letter designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

B000000	Tektronix, Inc., Beaverton, Oregon, USA
100000	Tektronix Guernsey, Ltd., Channel Islands
200000	Tektronix United Kingdom, Ltd., London
300000	Sony/Tektronix, Japan
700000	Tektronix Holland, NV, Heerenveen, The Netherlands

TABLE OF CONTENTS

VOLUME 1

TABLE OF CONTENTS (cont)

WARNING

The remaining portion of this Table of Contents lists information that may expose personnel to hazardous voltages. The information listed in the remaining sections of this manual is for qualified personnel only.

TABLE OF CONTENTS (cont)

TABLE OF CONTENTS (cont)

TABLE OF CONTENTS (cont)

NOTE

The following sections and information is contained in Volume 2 of this manual.

LIST OF ILLUSTRATIONS

VOLUME 1

LIST OF TABLES

VOLUME 1

OPERATORS SAFETY SUMMARY

The general safety information in this part of the summary is for both operating and servicing personnel. Specific warnings and cautions will be found throughout the manual where they apply, but may not appear in this summary.

TERMS

In This Manual

CAUTION statements identify conditions or practices that could result in damage to the equipment or other property.

WARNING statements identify conditions or practices that could result in personal injury or loss of life.

As Marked on Equipment

CAUTION indicates a personal injury hazard not immediately accessible as one reads the marking, or a hazard to property including the equipment itself.

DANGER indicates a personal injury hazard immediately accessible as one reads the marking.

SYMBOLS

In This Manual

This symbol indicates where applicable cautionary or other information is to be found.

As Marked on Equipment

DANGER — High voltage.

Protective ground (earth) terminal.

ATTENTION — refer to manual.

Power Source

This product is intended to operate in a power module connected to a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power module power cord is essential for safe operation.

Grounding the Product

This product is grounded through the grounding conductor of the power module power cord. To avoid electrical shock, plug the power cord into a properly wired receptacle before connecting to the product input or output terminals. A protective ground connection by way of the grounding conductor in the power module power cord is essential for safe operation.

Danger Arising From Loss of Ground

Upon loss of the protective-ground connection, all accessible conductive parts (including knobs and controls that may appear to be insulating) can render an electric shock.

Use the Proper Fuse

To avoid fire hazard, use only the fuse of correct type, voltage rating and current rating as specified in the parts list for your product.

Refer fuse replacement to qualified service personnel.

Do Not Operate in Explosive Atmospheres

To avoid explosion, do not operate this product in an explosive atmosphere unless it has been specifically certified for such operation.

Do Not Operate Without Covers

To avoid personal injury, do not operate this product without covers or panels installed. Do not apply power to the plug-in via a plug-in extender.

SERVICE SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary.

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

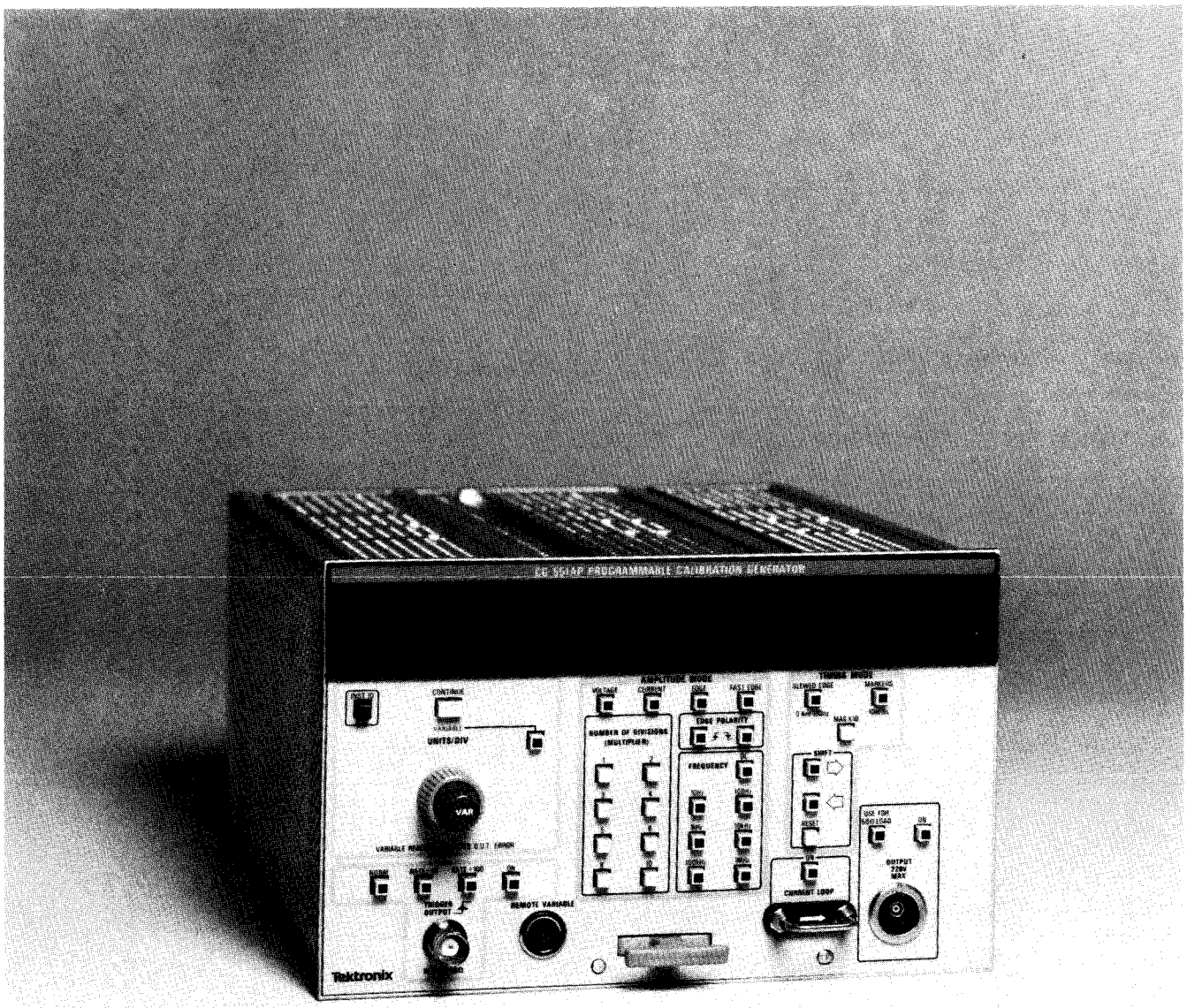
Use Care When Servicing With Power On

Dangerous voltages exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

This product is intended to operate in a power module connected to a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power module power cord is essential for safe operation.



2690-1

CG 551AP Programmable Calibration Generator.

SPECIFICATION

INTRODUCTION

Manual Overview

Operating and service instructions for the TEKTRONIX CG 5001/CG 551AP Programmable Calibration Generator are found in a two volume Instruction manual and a pocket size Reference Guide.

Volume I contains the Specification, Operating Instructions, Programming, and Theory of Operation.

Volume II contains the Calibration (Performance Check and Adjustment Procedures), Maintenance, the Electrical and Mechanical Parts Lists, Block Diagrams, Schematic Diagrams, Parts Location Tables, and Troubleshooting Flow Charts.

The Reference Guide is a condensed version of the Programming Instructions found in Volume I.

Instrument Description

The TEKTRONIX CG 5001/CG 551AP Programmable Calibration Generator is a source of calibrated timing signals, voltage and current waveforms, and pulses with low distortion edges. The CG 5001/CG 551AP is used to calibrate and check oscilloscope performance characteristics.

The CG 5001/CG 551AP operates in six basic modes:

VOLTAGE— as a voltage source it is used to check the gain accuracy of vertical and horizontal amplifiers.

CURRENT— as a current source it is used to check the accuracy of current probes and amplifiers.

EDGE— as a source of low distortion edges it is used to check the transient response of amplifiers and attenuator networks.

FAST EDGE— with the Pulse Head accessory attached, it is used to check the transient response (risetime) of vertical amplifiers (beyond the EDGE mode capability).

MARKERS— as a time mark source it is used to check the timing accuracy of horizontal sweep rates up to 10 ns/division.

SLEWED EDGE— this mode generates a timing signal to check the timing accuracy of horizontal sweep rates up to 0.2 ns/division.

The Comparator Head accessory (optional) can be used to check oscilloscope internal calibrator amplitude accuracy.

The Remote Variable accessory (optional) allows the operator freedom of movement at the testing location.

All of the CG 5001/CG 551AP output signals are programmable via high level and low level commands sent over the general purpose interface bus (GPIB). The CG 5001/CG 551AP has the capability of outputting data to a GPIB controller. The data is related to the status of the front panel controls and the actual percentage deviation (error) of the oscilloscope vertical sensitivity and sweep timing. With the use of a controller and hard copy peripheral, a complete printout of oscilloscope performance can be made available to the user.

Instrument Options

The following options to the standard CG 5001/CG 551AP are available. Contact your nearest Tektronix Field Office or Service Facility for details.

Option 01 Adds a temperature compensated, 5 MHz crystal oscillator for a higher accuracy time base.

Option 02 Deletes the standard Pulse Head accessory.

Standard Accessories

2 Instruction Manuals, Volume 1 and Volume II. (Vol. II 070-4767-00)
1 Reference Guide.
1 50 Ω Output Cable.
1 Pulse Head.
1 Pulse Head instruction manual.

Optional Accessories

The following accessories for the CG 5001/CG 551AP are available upon request. Contact your nearest Tektronix Field Office or Service Facility for details and ordering information.

1. Comparator Head with instruction manual.
2. Remote Variable with instruction manual.

NOTE

Refer to the tabbed Accessories page in the rear of this manual for more information.

IEEE 488 (GPIB) Function Capability

The CG 5001/CG 551AP is capable of being remotely programmed via the digital interface specified in IEEE Standard 488-1975, "Standard Digital Interface for Programmable Instrumentation". In this manual, the interface is commonly called the General Purpose Interface Bus (GPIB).

The IEEE standard identifies the interface function repertoire of an instrument on the GPIB in terms of interface function subsets. The subsets are defined in the standard. The subsets that apply to the CG 5001/CG 551AP are listed in Table 1-1.

NOTE

Refer to IEEE Standard 488-1975 and the latter part of the Programming section of this manual for more detailed information. The standard is published by the Institute of Electrical and Electronics Engineers, Inc., 345 East 47th Street, New York, New York 10017.

Table 1-1
INTERFACE FUNCTION SUBSETS

Function	Subset	Capability
Source Handshake	SH1	Complete: CG 5001/CG 551AP allows a settling time on the GPIB data lines before asserting DAV. T_1 in the standard: $\geqslant 2\ \mu s$.
Acceptor Handshake	AH1	Complete.
Basic Talker	T6	Responds to Serial Poll. Untalk if My Listen Address (MLA) is received.
Basic Listener	L4	Unlisten if My Talk Address (MTA) is received.
Service Request	SR1	Complete.
Remote-Local	RL1	Complete.
Parallel Poll	PPØ	Does not respond to Parallel Poll.
Device Clear	DC1	Complete.
Device Trigger	DT1	Complete.
Controller	CØ	No Controller function.
Bus Drivers		Tri-State

ELECTRICAL CHARACTERISTICS

Performance Conditions

The limits stated in the Performance Requirements column are valid only if the CG 5001/CG 551AP has been calibrated at an ambient temperature between +20°C and +30°C and is operating at an ambient temperature between 0°C and +50°C, unless otherwise stated.

Information given in the Supplemental Information column of the following tables is provided for user information only, and should not be interpreted as Performance Requirements.

The CG 5001/CG 551AP must be in an environment whose limits are described under Environmental Characteristics.

Allow at least 30 minutes warm-up time for operation to specified accuracy, 60 minutes after storage in high humidity environment.

Table 1-2
VOLTAGE (AMPLITUDE MODE)

Characteristics	Performance Requirements	Supplemental Information
Output Amplitude Limits		
1 MΩ Load (or greater)	40 μV to 200 V	
50 Ω Load	40 μV to 5 V	
Accuracy	±0.25%, ±1 μV	
Aberrations	Duration ≤5% of period and less than 15% ±10 mV of amplitude	
Settling Time		
40 μV to 10 V		<2 μs to .25% accuracy.
12 V to 200 V		<15 μs to .25% accuracy.
Variable Range	±9.9%	
Frequency		Frequency selected in decade steps.
40 μV to 80 mV	10 Hz to 10 kHz	
100 mV to 10 V	10 Hz to 100 kHz, or DC	
12 V to 200 V	10 Hz to 10 kHz, or DC	
Polarity	Positive	
Source Resistance		50 Ω
Current Limit		
40 μV to 5 V	100 mA Minimum	Checked for 5 V across a 50 Ω load.
12 V to 200 V	10 mA Minimum	Checked for 100 V across a 10 kΩ load.
Short Circuit Current		
40 μV to 10 V	Less than 200 mA	
12 V to 200 V	Less than 30 mA	

Table 1-2 (cont)

Characteristics	Performance Requirements	Supplemental Information
Displayed Information		
Units/Div		10 μV/Div to 50 V/Div 1, 2, 5 sequence.
Multipliers		1, 2, 3, 4, 5, 6, 8, or 10. 40 μV is 10 μV X 4 or 20 μV X 2. 200 V is 20 V X 10 or 50 V X 4.
Error Range (DUT)		From 9.9% LOW to 9.9% HIGH LOW = −, HIGH = + on the bus.
UNCAL Indicator		Operational only in the 10 V to 200 V range. Illuminated when current limits are exceeded.

Table 1-3
CURRENT (AMPLITUDE MODE)

Characteristics	Performance Requirements	Supplemental Information
Output		
Amplitude Limits	1 mA to 100 mA	Available from current loop or main output connector.
Accuracy	± (0.25% + 2μA)	
Variable Range	±9.9%	
Frequency	DC or 10 Hz to 1 MHz	Frequency selected in decade steps.
Polarity		Positive voltage with respect to ground at main output connector.
Aberrations (10 Hz to 100 kHz)	Duration ≤5% of period and less than 15%, (±100 μA) of amplitude	
Tilt or Droop	≤1% of peak-to-peak amplitude	
Voltage Limit	5 V minimum	Checked for 100 mA into 50 Ω
Open Circuit Voltage	Less than 10 V	
Displayed Information		
Units/Div		1 mA/Div to 100 mA/Div 1, 2, 5 sequence.
Multipliers		1, 2, 3, 4, 5, 6, 8, or 10. 100 mA is 10 mA X 10 or 20 mA X 5.
Error Range (DUT)		From 9.9% LOW to 9.9% HIGH. LOW = −, HIGH = + on the bus.
UNCAL Indicator		Illuminated when voltage limit is exceeded.

Table 1-4
EDGE (AMPLITUDE MODE)

Characteristics	Performance Requirements	Supplemental Information
Low Amplitude Range		
(50 Ω Load Only)	20 mV to 1 V, peak-to-peak	
Risetime or Falltime	≤1.3 ns	
Aberrations	±2% of square wave amplitude	
Long Term Flatness		±0.5% after first 10 ns
Polarity	Positive or negative transition	Selected by EDGE POLARITY buttons. Negative voltage rising to ground or positive voltage falling to ground.
Frequency	10 Hz to 1 MHz	Selected in decade steps.
Amplitude Accuracy	±3%	
Variable Amplitude		At least ±9.9%.
Source Resistance		50 Ω.
Current Limit	20 mA minimum	Checked for 1 V across a 50 Ω load.
Short Circuit Current	Less than 40 mA average	
DC Offset		0.2% of amplitude.
Displayed Information		
Units/Div		20 mV/Div to 1 V/Div in a 1, 2, 5 sequence.
Multipliers		1, 2, 3, 4, 5, 6, 8, or 10.
Error Readout		VAR indicated in display window; Percent (%) error not indicated.
UNCAL Indicator		Not used.
High Amplitude Range		
1 MΩ (or greater) load	1.2 V to 100 V, peak-to-peak	
Risetime	Less than 100 ns	
Aberrations	±2% of square wave amplitude	
Long Term Flatness		±0.5% after first 500 ns
Polarity	Positive transition only	Negative voltage rising to ground.
Frequency	10 Hz to 100 kHz	Selected in decade steps.
Amplitude Accuracy	±3%	
Variable Amplitude		At least ±9.9%.
Source Resistance		50 Ω.
Current Limit	10 mA minimum	Checked for 100 V across a 10 kΩ load (20—100 V range) and 10 V across a 1 kΩ load (1.2—16 V range).

Table 1-4 (cont)

Characteristics	Performance Requirements	Supplemental Information
Short Circuit Current	30 mA maximum average	
DC Offset		0.2% of amplitude.
Displayed Information		
Units/Div		.2 V/Div to 20 V/Div in a 1, 2, 5, sequence.
Multipliers		1, 2, 3, 4, 5, 6, 8, or 10.
Error Readout		VAR indication. Percent (%) error not indicated.
UNCAL Indicator		Illuminated when current limit is exceeded (1.2 V to 100 V range).

Table 1-5
MARKERS (TIMING MODE)

Characteristics	Performance Requirements	Supplemental Information
Timing Range	10 ns to 5 sec	
X10 MAG	Increases marker rate by a factor of ten	.1 μs to 5 sec range only. Every tenth marker boosted in amplitude.
Variable Range	±9.9%	
Marker Accuracy		
Standard Time Base	±0.01%	
Option 01 Time Base	±0.0003%	15°C to 50°C.
Output Amplitude		
50 Ω load	1 V minimum	
Displayed Information		
Units/Div, MAG Off		10 ns/Div to 5 s/Div in a 1, 2, 5 sequence.
Units/Div, MAG On		.1 μs/Div X10 MAG to 5 s/Div in a 1, 2, 5 sequence.
Error Readout (DUT)		From 9.9% SLOW to 9.9% FAST FAST = +, SLOW = − on the bus.
EXT REF Indicator		Illuminated when external reference frequency is applied through rear interface.
UNCAL Indicator		Not used.

Table 1-6
SLEWED EDGE (TIMING MODE)

Characteristics	Performance Requirements	Supplemental Information
Timing range	.4 ns and .5 ns to 100 ns	
X10 MAG	Increases slewed edge rate by a factor of ten	5 ns to 100 ns range only.
Variable Range	±9.9%.	
Slewed Edge Accuracy		
Standard Time Base	±.01%	
Option 02 Time Base	±.0003%	
Edge Position Uncertainty		±40 ps.
Output Amplitude		
50 Ω Load	1 V minimum	
Displayed Information		
Units/Div, MAG Off		.4 ns/Div and .5 ns/Div to .1 μs/Div in a 1, 2, 5 sequence (except .4 ns).
Units/Div, MAG On		5 ns/Div X10 MAG to .1 μs/Div in a 1, 2, 5 sequence.
Error Readout (DUT)		From 9.9% SLOW to 9.9% FAST FAST = +, SLOW = − on the bus.
EXT REF Indicator		Illuminated when external reference frequecy is applied through rear interface.
UNCAL Indicator		Not used.

Table 1-7
TRIGGER OUTPUT

Characteristics	Performance Requirements	Supplemental Information
Markers Mode		
Normal	Slaved to marker rate from 5 sec to 100 ns; remains at 100 ns for faster rates	No change in trigger rate for the X10 MAG mode.
Rate ÷ 10	Reduces normal trigger rate by a factor of ten	
Rate ÷ 100	Reduces normal trigger rate by a factor of one hundred	Not available for X10 MAG mode.

Table 1-7 (cont)

Characteristics	Performance Requirements	Supplemental Information
Slewed Edge Mode		
Normal		One trigger pulse per slewed edge. Approximate range: 180 kHz (100 ns/Div) to 300 kHz (.4 ns/Div).
Rate ÷ 10 and Rate ÷ 100		Not available.
All Other Modes		
Normal		Output frequency.
Rate ÷ 10		One-tenth output frequency.
Rate ÷ 100		One-hundredth output frequency.
Output Amplitude		
All Modes (50 Ω Load)	1 V minimum	

Table 1-8
REFERENCE FREQUENCY AND GPIB INDICATORS

Characteristics	Description
Internal Reference Frequency	
Output Frequency	1 MHz with internal time base accuracy.
Output Amplitude	TTL compatible.
External Reference Frequency	
Input Frequency	Must be any integral multiple of 1 MHz up to 5 MHz.
Input Amplitude	1 V to 10 V, rms, indicated by EXT REF indicator on front panel.
Required Accuracy	±0.001%.
Input Resistance	10 kΩ (nominal).
GPIB Indicators	
Remote (REM)	Illuminated when controller program places instrument in Remote State (REMS) or Remote With Lockout State (RWLS).
Talk (TLK)	Illuminated when instrument enters the Talker Active State (TACS).
Listen (LSN)	Illuminated when Attention (ATN) bus line is true or when the instrument enters the Listener Active State (LACS).

Table 1-9
EXTERNAL ACCESSORIES

Characteristics	Description
FAST EDGE Function	Performance requirements found in the Pulse Head instruction manual.
COMPARATOR Function	Performance requirements found in the Comparator instruction manual.
REMOTE VARIABLE Function	Performance requirements found in the Remote Variable instruction manual.

Table 1-10
MISCELLANEOUS (ELECTRICAL)

Characteristics	Description
Power Consumption	65 Volt—Amperes

PHYSICAL CHARACTERISTICS

Table 1-11
ENVIRONMENTAL

Characteristics	Description	
Temperature		
Operating	0°C to +50°C.	Meets MIL-T-28800B, class 5, with exception to non-operating temperature.
Non-operating	−40°C to +65°C.	
Humidity		
Operating and Non-operating	90—95% RH for 5 days to +50°C.	Exceeds MIL-T-28800B, class 5.
Altitude		
Operating	15,000 ft (4.5 km).	Exceeds MIL-T-28800B, class 3.
Non-operating	50,000 ft (15 km)	
Vibration		
Operating	Displacement (peak-to-peak), 0.38 mm (.015″). Vibrating frequencies, 10 Hz—55 Hz. Total time, 75 minutes.	Meets MIL-T-28800B, class 5.

Table 1-11 (cont)

Characteristics	Description	
Shock		
Non-operating	30 g's, half sine, 11 ms duration, 3 shocks in each direction along 3 major axes; total shocks, 18.	Meets MIL-T-28800B, class 5.
Bench Handling		
Operating	45° or 4 inches or point of balance, whichever occurs first.	Meets MIL-T-28800B, class 5.
EMI Compatability		Meets MIL-T-28800B, class 3, MIL-STD-461A, when performed in accordance with MIL-STD-462 with the following exception: RE02, tested to 30 dB above specification from dc to 700 MHz.
Electrostatic Discharge		
Operating Maximum Test Voltage	20 kV.	Charge applied to each protruding area except the output terminals.
Transportation Package		
Vibration and Drop (Non-operating)	25 mm (1″) at 270 rpm for 1 hour. 10 drops from 3 ft (1 m).	Qualified under National Safe Transit Association Preshipment Procedures 1A-B-1 and 1A-B-2.

Table 1-12
MECHANICAL

Characteristics	Description
Maximum Overall Dimensions	
Height	4.971 inches (12.626 cm).
Width	7.960 inches (20.218 cm).
Length	11.975 inches (30.442 cm).
Net Weight	
CG 5001/CG 551AP	9.5 lbs. (4.3 kg).
With Option 01	9.6 lbs. (4.4 kg).
With Option 02	8.75 lbs. (3.97 kg).
Finish (Front Panel)	Plastic/Aluminum laminate.

OPERATING INSTRUCTIONS

INTRODUCTION

This section of the manual describes the functions of the CG 5001/CG 551AP front panel controls and connectors. An operator's familiarization procedure is also provided in this section as an aid in understanding how to operate the CG 5001/CG 551AP under local (manual) control only.

Complete information for programming the CG 5001/CG 551AP via the GPIB is found in the Programming section of this manual.

NOTE

The CG 551AP must be installed in a TM 500-Series power module designed for GPIB compatible instruments. Refer to the power module instruction manual before installing the CG 551AP.

The CG 5001 must be installed in three compartments of a TM 5000-Series power module.

PREPARATION FOR USE

Installation and Removal

NOTE

If the CG 5001/CG 551AP is to be remotely programmed via the General Purpose Interface Bus (GPIB), the five-bit address code and message terminator switches must be set prior to installation. Refer to Fig. 3-1 in the Programming section of this manual for details concerning these switches.

Make sure that the line selector block on the power module is positioned correctly and that both the CG 5001/CG 551AP and the power module have the proper fuse installed. Be certain that the power plug for the power module has the proper grounding conductor.

CAUTION

To prevent damage to the CG 5001/CG 551AP, turn the power module off before instrument installation or removal from the power module. Do not use excessive force to install or remove.

Align the CG 5001/CG 551AP chassis with the upper and lower guides of the selected power module compartments. Push the CG 5001/CG 551AP into the mainframe and press firmly to seat the rear connectors in their respective jacks at the rear of the power module.

Connect the power cord to the power source and apply power to the CG 5001/CG 551AP by operating the power module POWER switch.

NOTE

IEEE Standard 488-1975 states that a complete system on the GPIB must be operated with power applied to at least one or more than half the devices in the system. Powering up a device while the system is running may cause faulty operation.

To remove the CG 5001/CG 551AP from the power module, pull the release latch (located at the lower center part of the front panel) until the interface connection disengages.

FRONT PANEL CONTROLS AND CONNECTORS

General Information

All but twelve of the front panel pushbuttons are illuminated when their associated functions are activated. These buttons are: CONTINUE, INST ID, RESET, MAG X10, and the eight NUMBER OF DIVISIONS (MULTIPLIER) buttons. See Fig. 2-2.

The UNITS/DIV and the VARIABLE controls have no numeric notation on the front panel. The settings for these controls are displayed in the readout window.

Display Window

Typical displays for the CG 5001/CG 551AP are shown in Fig. 2-1. The far left side of the window displays the settings for the UNITS/DIV control. These are expressions of oscilloscope sweep speed and deflection factors and are displayed, for the indicated operating mode, as follows:

VOLTAGE; volts per division (V/D), millivolts (mV/D), or microvolts (μV/D).

CURRENT; milliamperes per division (mA/D).

EDGE; volts per division (V/D) or millivolts (mV/D). VAR is displayed if the VARIABLE button is illuminated.

FAST EDGE; When the FAST EDGE function is activated with the Pulse Head attached to the OUTPUT connector, the readout will display 1 V x 1. VAR is displayed if the VARIABLE button is illuminated.

SLEWED EDGE; microseconds per division (μs/D), or nanoseconds (ns/D).

MARKERS; seconds per division (s/D), milliseconds (ms/D), microseconds (μs/D), or nanoseconds (ns/D).

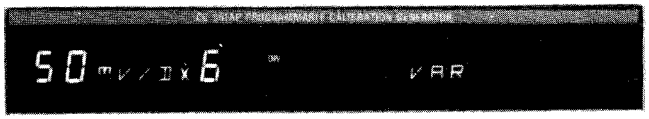
UNITS/DIV | MAG X10 or MULTIPLIER | DUT Error | GPIB

VOLTAGE mode, 40 μV/Div.

Markers mode, 10 ns/Div.

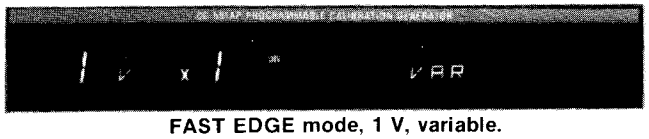
CURRENT mode, 100 mA/Div.

Internal error via self test routine.

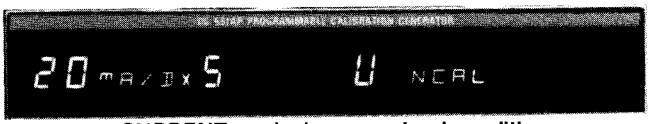


EDGE mode, 300 mV/Div, variable.

Invalid programming command.



FAST EDGE mode, 1 V, variable.



CURRENT mode, improper load condition.

Slewed Edge mode, 0.5 ns/Div.

Invalid key push via front panel.

2690-2

Fig. 2-1. Typical displays on the CG 5001/CG 551AP.

The window (left center) displays a multiplication factor that is to be applied to the UNITS/DIV value being displayed. When operating in an Amplitude Mode (except FAST EDGE), the NUMBER OF DIVISIONS (MULTIPLIER) buttons are the multipliers, i.e., pressing the 2 button will display X2 DIV. When operating in the SLEWED EDGE or MARKERS mode, X10 MAG will be displayed when the MAG X10 button is pressed.

The window (center) displays the percent deviation (error) of the device under test (DUT). Sweep speed errors are displayed as FAST or SLOW, amplitude errors as HIGH or LOW.

The window (far right) displays four operating state indicators: EXT, REM, TLK, and LSN.

EXT, when illuminated, indicates an external reference frequency is applied, (through the rear interface), to the time reference circuits.

REM, when illuminated, indicates that the CG 5001/CG 551AP is operating under remote program control via the GPIB.

TLK, when illuminated, indicates that the CG 5001/CG 551AP is in the Talker Active State (TACS).

LSN, when illuminated, indicates that the Attention (ATN) line on the GPIB has been asserted, or that the CG 5001/CG 551AP is in the Listener Active State (LACS).

The window also displays the word "ERROR" followed by a numeric code number to indicate internal errors, self-check errors, operating errors, and programming errors. See CG 5001/CG 551AP Error Messages.

If an attempt is made to activate an invalid function, the CG 5001/CG 551AP will display the words "ENTRY ERROR" in the window.

Keyboard Switches, Controls and Connectors

The following is a descriptive list of the CG 5001/CG 551AP front panel keyboard switches, controls, and connectors. See Fig. 2-2. Where applicable, an item includes the high level programming mnemonic that activates the function (associated with the switch, control, or connector) via commands received from the GPIB. Refer to the Programming section in this manual for more information (␣ = ASCII space).

(1) CONTINUE — OPC␣ON or OPC␣OFF

This button is pushed by the operator to make the percentage error and units/division readout available to a GPIB controller after the CG 5001/CG 551AP receives a READ? query. The CONTINUE button is always under local control. It is also used to sequence through the calibration procedure or to assert SRQ under program control. The CONTINUE button is also used to clear error codes in the display window.

(2) INST ID — REM␣ON or REM␣OFF

Depressing this button causes the instrument to display its bus address and generate a Service Request (SRQ) on the GPIB. If the displayed address is 31, the CG 5001/CG 551AP will not respond to programming via the bus.

(3) VARIABLE — VAR or FXD

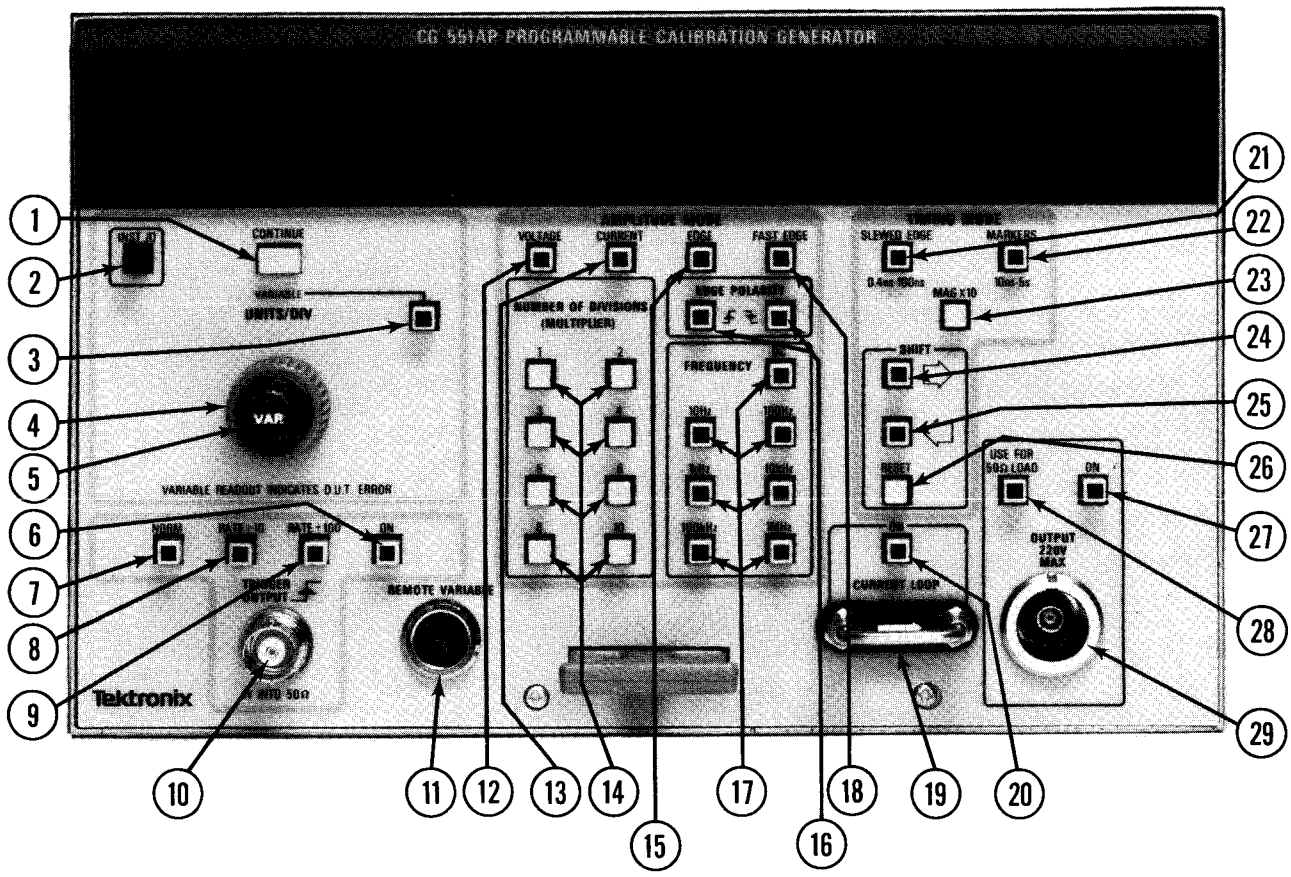
When this button is not illuminated, the CG 5001/CG 551AP generates a calibrated fixed voltage, current, or timing signal. When this button is illuminated, the instrument generates a calibrated variable voltage, current, or timing signal under control of the VARIABLE knob. When the CG 5001/CG 551AP is operating in the EDGE or FAST EDGE modes, the variable amplitude function is not calibrated.

(4) UNITS/DIV Control — U/D␣<numeric>

This control is set to match the appropriate settings of the device under test. When changing modes of operation, the instrument reverts to the last used setting of the selected mode. If this control is turned beyond (outside) the specified limits of the mode selected, no further change in the readout or output waveform occurs.

(5) VARIABLE (VAR) — PCT␣<value> or FXD

The VARIABLE control is active when the VARIABLE button is illuminated. This control is used to adjust the output voltage, current, or timing signal to reflect a calibration error for the device under test. The error range is from −9.9% to +9.9%. A negative number is returned over the GPIB data bus for a LOW or SLOW indication, a positive number is returned for a HIGH or FAST indication. When this control is used in the EDGE or FAST EDGE mode to vary the output amplitude, the percent error display is replaced with the word VAR.



2690-3

Fig. 2-2. CG 5001/CG 551AP front panel controls, connectors, and display window.

(6) TRIGGER ON — TRIG∮ON or TRIG∮OFF

Pressing this button turns the trigger signal at the TRIGGER OUTPUT connector on or off. The trigger output cannot be turned off when the instrument is operating in the SLEWED EDGE mode.

(7) TRIGGER NORM — TRIG∮NORM

When this button is illuminated, the trigger rate is slaved to the output signal rate. In the MARKERS mode, the trigger rate limits at 100 ns. In the SLEWED EDGE mode, one trigger pulse is generated for every slewed edge.

(8) TRIGGER RATE ÷ 10 — TRIG∮X.1

When this button is illuminated, the instrument generates trigger signals at one-tenth the normal rate. Pressing this button also turns on the trigger output if the trigger ON function is off. This button is inoperative in the SLEWED EDGE mode.

(9) TRIGGER RATE ÷ 100 — TRIG∮X.01

When this button is illuminated, the instrument generates trigger pulses at one-hundredth the normal rate. Pressing this button also turns on the trigger output if the trigger ON function is off. This button is inoperative in the SLEWED EDGE mode.

(10) TRIGGER OUTPUT

This connector is the source for trigger pulses.

(11) REMOTE VARIABLE

This is the connection for the Remote Variable accessory.

(12) VOLTAGE — Mode♭V or MODE♭VOLTAGE

When this button is illuminated, the CG 5001/CG 551AP generates voltage signals from 40 μV to 200 V. Output voltage is positive going from ground.

(13) CURRENT — Mode♭CUR or MODE♭CURRENT

When this button is illuminated, the CG 5001/CG 551AP generates current signals (fixed or variable) within the limits of 1.0 mA to 100 mA. The selected current signals can be routed through the CURRENT LOOP or to the OUTPUT connector.

(14) NUMBER OF DIVISIONS (MULTIPLIER) — MULT♭<number>

These pushbuttons (1, 2, 3, 4, 5, 6, 8, or 10) cause the CG 5001/CG 551AP to multiply the UNITS/DIV setting by the chosen MULTIPLIER. The multipliers are applicable for the VOLTAGE, CURRENT, and EDGE modes only. The signal equivalent to the multiplied UNITS/DIV setting is applied to the selected output connector (OUTPUT or CURRENT LOOP). The multiplying factor appears in the readout display.

(15) EDGE — MODE♭EDGE

When this button is illuminated, the CG 5001/CG 551AP generates pulses with low distortion edges. This mode has two amplitude ranges. For the high amplitude range (1.2 V to 100 V, 1 MΩ load), the risetime is 100 ns or less. The output pulse is a positive transition (rising from a negative rest potential to ground). Output polarity is not selectable for the high amplitude range. For the low amplitude range (20 mV to 1 V, 50 Ω load), the risetime is 1.3 ns or less. The output polarity is selectable via the EDGE POLARITY buttons. The pulse amplitude is either fixed or variable. Percentage error information is replaced with the word VAR when the VARIABLE function is on.

(16) EDGE POLARITY — POS or NEG

An EDGE POLARITY button, when illuminated, selects the desired polarity for the edges discussed under item 15 (EDGE mode) or item 18 (FAST EDGE mode). For the EDGE mode, the pulse polarity is either rising to ground from a negative rest potential (POS) or falling to ground from a positive rest potential (NEG).

(17) FREQUENCY — FREQ♭<numeric>

When illuminated, a button within this group selects the output frequency for the VOLTAGE, CURRENT, EDGE, and FAST EDGE modes. The DC function is not available for voltages less than 100 mV. The DC function is not applicable to the EDGE or FAST EDGE modes. Refer to the specifications for frequency limits associated with each mode.

(18) FAST EDGE — MODE♭FE or MODE♭FASTEDGE

This button, when illuminated (with the Pulse Head accessory connected to the OUTPUT), causes the external Pulse Head to generate a 1 V signal with a risetime equal to or less than 200 picoseconds. The output amplitude is variable, via the front panel VARIABLE control.

Holding this button in for approximately 1 second will delay the fast edge signal from the output trigger by about 120 ns. This mode is used for Pulse Head calibration purposes. The mode is indicated by simultaneous illumination of the SHIFT buttons. Escape from this mode is accomplished by pressing the FAST EDGE pushbutton, or any other mode button.

(19) CURRENT LOOP

When the CG 5001/CG 551AP is operating in the CURRENT mode, selected currents pass through this loop if the current ON button (item 20) is illuminated.

(20) ON (Current Loop) — LOOP♭ON or LOOP♭OFF

When illuminated, this button turns the CURRENT LOOP on and turns the main OUTPUT off.

(21) SLEWED EDGE — MODE♭SLWD or MODE♭SLEWED

When this button and the trigger ON button are illuminated, slewed edges are available with 0.4 ns to 100 ns spacing between edges. The SLEWED EDGE function consists of multiple edges generated on successive sweeps, one at a time.

If the UNITS/DIV control is set for a slewed edge rate slower than 100 ns/D, the CG 5001/CG 551AP automatically switches to the MARKERS mode. The number of edges in a displayed pattern is programmable via the GPIB.

Holding this button in for approximately 1 second puts the CG 5001/CG 551AP in a continuous slewing mode. This mode is used for CG 5001/CG 551AP calibration purposes. The mode is indicated by simultaneous illumination of the SHIFT buttons. Escape from this mode is accomplished by pressing the SLEWED EDGE pushbutton, or any other mode button.

(22) MARKERS — MODE␣MKRS or MODE␣MARKERS

When this button is illuminated, the CG 5001/CG 551AP outputs shaped time marks in the 10 ns to 5 sec range. (Both markers and slewed edges are available between 10 ns and 100 ns.) If the UNITS/DIV control is set for time marks faster than 10 ns, the CG 5001/CG 551AP automatically switches to the SLEWED EDGE mode.

NOTE

In the overlapping region (10 ns to 100 ns), the instrument generates the last used (previous) signal set by the UNITS/DIV control. The CG 5001/CG 551AP continues to generate that type of signal until the UNITS/DIV control is switched beyond the upper or lower limit of the overlapping region, or until another button is activated.

(23) MAGX10 — MAG␣X10

Pressing this button reduces the period of the time marks (100 ns to 5 sec range) or the slewed edges (5 ns to 100 ns range) by a factor of ten. This button turns on the MAG indicator in the readout and converts the magnification factor from X1 to X10.

(24) SHIFT — RSHF or SHFT␣<+value>

When this function is activated with the MAG X10 indicator off, the slewed edges are shifted one division at a time to the right on the crt display.

When this function is activated with the MAG X10 indicator on, the slewed edges are shifted ten divisions at a time to the right on the crt display.

(25) SHIFT — LSHF or SHFT␣<−value>

When this function is activated with the MAG X10 indicator off, the slewed edges are shifted one division at a time to the left on the crt display.

When this function is activated with the MAG X10 indicator on, the slewed edges are shifted ten divisions at a time to the left on the crt display.

(26) RESET — ZSHF or SHFT␣0

Pressing this button resets the group of slewed edges to the zero shift position.

NOTE

All front panel indicator and pushbutton lights (except for TLK and LSN) can be tested by holding the RESET button closed. The SHIFT and RESET functions are not applicable to the MARKERS mode.

(27) ON (Main Output) — OUT␣ON or OUT␣OFF

Pressing this button turns the OUTPUT on. When the CG 5001/CG 551AP is programmed to change modes, the OUTPUT is automatically disconnected and must then be turned on.

(28) USE FOR 50 Ω LOAD — LDZ␣50 or LDZ␣HI

When this button is illuminated, the output is calibrated for a 50 Ω load. This function is manually selectable only in the VOLTAGE mode. The function is automatically selected when the CG 5001/CG 551AP is operating in the low amplitude range (20 mV to 1 V) for the EDGE mode. It must be used at all times when driving a 50 Ω load. For the VOLTAGE mode, current limiting occurs above 5 V across 50 Ω (100 mA). For the EDGE mode, current limiting occurs above 1.2 V across 50 Ω.

(29) OUTPUT 220 V MAX

WARNING

220 V may exist at the OUTPUT connector.

This connector is the output for timing signals, voltage amplitude signals, or pulses. It is also the driving signal source for the Pulse Head and the Comparator Head. The connector has a sensing contact to detect the presence of the external accessories. If the CURRENT LOOP is off and the instrument is operating in the CURRENT mode, this output will act as a high impedance current source.

OPERATORS FAMILIARIZATION PROCEDURE

INTRODUCTION

This procedure allows the operator to become familiar with local operation and front panel control functions of the CG 5001/CG 551AP. Any irregularities encountered during this exercise should be referred to qualified service personnel.

NOTE

The only extra equipment needed for this procedure is an oscilloscope, and, for some steps, a 50 Ω feedthrough termination. This procedure is NOT to be used as a Performance Check Procedure for the CG 5001/CG 551AP or the oscilloscope. Specific detailed instructions for setting the oscilloscope controls are not given in this procedure. Observe all limits, capabilities, and operating procedures for the oscilloscope used.

Install the CG 5001/CG 551AP in the power module as outlined under Preparation For Use. Connect the output cable (furnished with the instrument) or the Pulse Head accessory from the CG 5001/CG 551AP OUTPUT connector to the oscilloscope vertical input. Connect a 50 Ω coaxial cable from the CG 5001/CG 551AP TRIGGER OUTPUT connector to the oscilloscope external trigger input. Apply power to the CG 5001/CG 551AP by operating the power switch on the power module. Set the oscilloscope vertical deflection factor for 1 V/Div and the horizontal sweep rate to 1 ms/Div.

NOTE

It is highly recommended that the CG 5001/CG 551AP TRIGGER OUTPUT always be connected to the oscilloscope external trigger input. The oscilloscope triggering controls should be set for external, positive slope. Failure to do this will prevent the use of the SLEWED EDGE mode and will cause misuse of the EDGE modes.

Power Up Self Test

Immediately following application of power, the CG 5001/CG 551AP performs a self test routine. The words SELF TEST will be displayed during this period. If all circuits are functioning properly, the CG 5001/CG 551AP will assume the standard power up default settings and assert the SRQ line on the GPIB. If (during self test), a circuit malfunction is encountered, an ERROR code is displayed in the readout window. See CG 5001/CG 551AP Error Messages in the Programming Section of this manual.

Press the CONTINUE button to clear the error code displays. Refer the error conditions (if any) to qualified service personnel.

Lamp Test

Press and hold the RESET button. In approximately one second, the illuminated pushbuttons and all segments of every display device in the display window will light. These lights will remain illuminated for approximately two seconds after the RESET button is released.

Instrument Identification

Press and hold the INST ID button. The GPIB address will be displayed in decimal notation. The SRQ line on the GPIB will also be asserted.

Operating the Front Panel Controls

Sequence the CG 5001/CG 551AP through the following modes of operation. During this exercise the CG 5001/CG 551AP will not accept an invalid command. If an attempt is made to activate an invalid function, the words ENTRY ERROR will appear in the display window. Also, if the UNITS/DIV control is rotated beyond specified limits, no further change in the displayed value will occur.

VOLTAGE MODE. When the VOLTAGE button is illuminated, the CG 5001/CG 551AP will generate voltage signals ranging in amplitude from 40 μV to 200 V at the OUTPUT. These signals are positive transitions from ground. The signal reference amplitude is set with the UNITS/DIV control and the value will be displayed. Pressing one of the NUMBER OF DIVISIONS (MULTIPLIER) buttons automatically multiplies the displayed UNITS/DIV by the selected multiplier. The output signal amplitude is adjusted with the VARIABLE control to display the calibration error of the oscilloscope. Along with the percentage error displayed, the word HIGH or the word LOW will appear to indicate error direction. The output signal frequency is selected by pressing one of the FREQUENCY buttons. The DC button is effective for the 100 mV to 200 V range only.

1. Press the VOLTAGE button and the 4 (MULTIPLIER) button. The VOLTAGE button should be illuminated. Press the CG 5001/CG 551AP OUTPUT ON.

2. Rotate the UNITS/DIV control through its range to see that values from 10 μV/D X4 to 50 V/D X4 are displayed. Change oscilloscope control as necessary.

3. Step through the NUMBER OF DIVISIONS (MULTIPLIER) buttons; the selected multiplier will be displayed. Attempting to set any combination of V/D times NUMBER OF DIVISIONS that would result in less than 40 μV/D or more than 200 V/D causes an ENTRY ERROR.

4. Press the VARIABLE button. The button should be illuminated and 0.0% displayed.

Rotate the VARIABLE control clockwise and counterclockwise to see that both HIGH and LOW percentages are displayed.

5. Step through the FREQUENCY buttons. Notice that attempting to set a frequency outside the specified limits of the CG 5001/CG 551AP results in an ENTRY ERROR.

6. The voltage signal polarity is not selectable; attempting to select EDGE POLARITY results in an ENTRY ERROR.

7. Reset the CG 5001/CG 551AP controls for 1 V/D X1, 1 kHz output.

8. Press the CG 5001/CG 551AP OUTPUT ON and TRIGGER OUTPUT ON buttons and obtain a 1 kHz squarewave signal display on the oscilloscope crt screen.

9. Rotate the CG 5001/CG 551AP VARIABLE control and note the increasing and decreasing amplitude of the displayed signal. The CG 5001/CG 551AP displays a HIGH percentage error when the amplitude is decreasing below 0.0% error and a LOW percentage error when the amplitude is increasing above 0.0% error.

10. Connect a 50 Ω termination between the CG 5001/CG 551AP OUTPUT and the oscilloscope vertical input. Reset the CG 5001/CG 551AP controls for 1 V/D X1 output.

11. Use the CG 5001/CG 551AP UNITS/DIV control to increase the output signal amplitude until the word UNCAL appears in the display window. Reset the CG 5001/CG 551AP output for 1 V/D X1.

12. Press the USE FOR 50 Ω LOAD button on the CG 5001/CG 551AP and then increase the output amplitude. The output amplitude can not be set for more than 5 V/D X1.

13. Retain the 50 Ω termination for the CURRENT mode.

CURRENT MODE. When the CURRENT button is illuminated, current signals ranging in amplitude from 1 mA to 100 mA are generated. These signals are switched from the OUTPUT to the CURRENT LOOP by pressing the CURRENT LOOP ON button. The current signal reference amplitude is set with the UNITS/DIV control. Pressing a NUMBER OF DIVISIONS (MULTIPLIER) button automatically multiplies the displayed Units/Div by the selected multiplier. The output signal is adjusted with the VARIABLE control to display a HIGH or LOW percentage error for the device under test. The output signal frequency is selected by pressing one of the FREQUENCY buttons.

NOTE

This is a simulated procedure for the CURRENT mode. If accuracy in terms of current is desired, a current probe must be connected between the oscilloscope current input and the CG 5001/CG 551AP CURRENT LOOP. Be sure the CG 5001/CG 551AP output cable is terminated with a 50 Ω load.

1. Press the CURRENT button and the 1 (MULTIPLIER) button. The CURRENT button should be illuminated.

2. Press the CG 5001/CG 551AP OUTPUT ON and TRIGGER OUTPUT ON buttons. Rotate the UNITS/DIV control through its range and examine that values from 1 mA/D to 20 mA/D are displayed in the display window. Change the oscilloscope controls as necessary for proper displays.

3. Step through the NUMBER OF DIVISIONS (MULTIPLIER) buttons; the selected multiplier will be displayed. Attempting to set any combination of mA/D times NUMBER OF DIVISIONS that results in more than 100 mA/D causes ENTRY ERROR to be displayed.

4. Press the VARIABLE button. The button should be illuminated and 0.0% displayed.

Rotate the VARIABLE control clockwise and counterclockwise to see that both HIGH and LOW percentages are displayed. Note the amplitude changes on the oscilloscope.

5. Step through the FREQUENCY buttons. All frequencies are valid in this mode.

6. Current signal polarity is not selectable; attempting to select EDGE POLARITY results in an ENTRY ERROR display.

7. Remove the 50 Ω termination and connect the output cable directly to the oscilloscope vertical input.

8. Attempting to pass signals through the OUTPUT without a proper load results in an UNCAL condition. The proper current load is a resistance that will not cause the selected output current to develop more than 5.5 V at the OUTPUT.

EDGE MODE. When the EDGE button is illuminated, pulses are generated at the OUTPUT. These pulses are generated in two ranges. High range pulses (1.2 V to 100 V) are positive transitions only, with a maximum rise time of 100 nanoseconds (into a 1 MΩ load). The low range pulses (20 mV to 1 V) are either positive or negative transitions with a maximum rise time of 1.3 nanoseconds (into a 50 Ω load). The low range pulse polarity is selectable via the EDGE POLARITY buttons. The pulse amplitude can be varied over the entire VARIABLE range, but the percentage error display is replaced with the word VAR. The EDGE pulse frequency is selected by pressing one of the FREQUENCY buttons. The DC button is not effective in this mode.

1. Press the EDGE, 1 kHz, and the 1 (MULTIPLIER) buttons. Select positive edge polarity. Press the CG 5001/CG 551AP OUTPUT ON.

2. Rotate the UNITS/DIV control through its range to see that values from 20 mV/D to 20 V/D are displayed. Change the oscilloscope controls as necessary throughout this procedure.

3. Step through the NUMBER OF DIVISIONS (MUTLIPLIER) buttons; the selected multiplier will be displayed. Only those buttons that do not exceed 100 V/D are valid.

LOW RANGE—Combinations of V/D times NUMBER OF DIVISIONS resulting in displays from 20 mV/D to 1 V/D cause the 50 Ω load button to light. For an accurate EDGE signal within this range to be generated, the CG 5001/CG 551AP OUTPUT must be terminated into 50 Ω.

HIGH RANGE—Combinations of V/D times NUMBER OF DIVISIONS ranging from 1.2 V/D to 20 V/D can be terminated into 10 kΩ or greater. The 50 Ω load button is not lighted in this range and attempting to do so will result in an ENTRY ERROR.

4. Press the VARIABLE button. The button should be illuminated and the word VAR displayed. Rotate the CG 5001/CG 551AP VARIABLE control and note the amplitude changes on the oscilloscope.

5. Step through the FREQUENCY buttons. All buttons except DC are valid in the low range (20 mV/D to 1 V/D). In the high range all buttons except DC and 1 MHz are valid.

6. The EDGE POLARITY is selectable in the low range only. High range polarity is positive only; attempting to select negative polarity in this range will result in an ENTRY ERROR.

7. All TRIGGER OUTPUT buttons are active in this mode.

NOTE

Neither negative edge polarity nor 1 MHz frequency is allowed for output amplitudes greater than 1 V/D. If you are operating at 1 MHz and desire to increase the output amplitude above 1 V, select positive edge polarity and reduce the frequency to 100 kHz or below.

FAST EDGE MODE. Attempting to enter the FAST EDGE mode without the Pulse Head attached will cause an ENTRY ERROR.

When the FAST EDGE button is activated with the Pulse Head attached, the CG 5001/CG 551AP will generate a 1 V pulse with a maximum risetime of 200 picoseconds at the Pulse Head output.

NOTE

For the FAST EDGE mode the Pulse Head must be terminated with a 50 Ω load.

1. The EDGE POLARITY buttons on the CG 5001/CG 551AP will select the desired signal polarity.

2. The fast rise pulse frequency can be selected by the CG 5001/CG 551AP FREQUENCY buttons. The DC, 10 Hz and 1 MHz buttons, when pressed, will cause an ENTRY ERROR.

3. Set the oscilloscope controls to observe the output signals in this mode.

4. Rotate the CG 5001/CG 551AP VARIABLE control to observe changes in signal amplitude.

NOTE

Refer to the Pulse Head instruction manual if more information is desired.

MARKERS MODE. When the MARKERS button is illuminated, the CG 5001/CG 551AP generates triangular shaped timing signals at the OUTPUT. These markers have equal rise and fall times, and are approximately 4% of the period width at the baseline (i.e., a 100 ms/Div marker will be about 4 ms wide). Marker spacing is set with the UNITS/DIV control from 10 ns/D to 5 s/D. If the UNITS/DIV control is set faster than 10 ns/D, the CG 5001/CG 551AP automatically switches to the SLEWED EDGE mode and outputs slewed edges instead of time marks.

With the VARIABLE button illuminated, the VARIABLE control adjusts the output signal to reflect a FAST or SLOW sweep speed error for the oscilloscope. The MAG X10 function reduces the marker spacing by a factor of 10. The SHIFT functions are inoperative in this mode.

NOTE

A 50 Ω load is not required, though recommended, when using the MARKERS mode.

1. Press the MARKERS button. The button should be illuminated.

2. Rotate the UNITS/DIV control through its range to see that values from 10 ns/D to 5 s/D are displayed. When the UNITS/DIV control is switched from 10 ns/D to 5 ns/D, the CG 5001/CG 551AP automatically switches from the MARKERS mode to the SLEWED EDGE mode. Return to the MARKERS mode.

3. Press the VARIABLE button. The button should be illuminated and 0.0% displayed. Rotate the VARIABLE control clockwise and counterclockwise to observe that both FAST and SLOW percentages are displayed.

4. Press the CG 5001/CG 551AP OUTPUT ON, and trigger ON, and NORM buttons. Set the UNITS/DIV control to display .5 ms/D markers. Set the oscilloscope and CG 5001/CG 551AP controls to obtain a visible, stable display of one marker per division across the oscilloscope graticule.

5. Rotate the CG 5001/CG 551AP VARIABLE control and observe horizontal movement of the markers.

6. Press the MAG X10 button. X10 MAG should be displayed in the display window. On the oscilloscope display, observe that the marker period has been reduced by a factor of 10 (10 markers have been compressed into 1 division). Also, every 10th marker is higher in amplitude than the others. If the oscilloscope is so equipped, activate the magnified sweep feature. Observe that the high amplitude markers are now spaced 10 divisions apart with 1 lower amplitude marker per division between them.

7. Press the MAG X10 button to deactivate this function and return the oscilloscope to normal sweep.

8. The only valid functions in this mode are UNITS/DIV, VARIABLE, MAG X10, OUTPUT ON, and the trigger functions. Attempting to activate any of the others (except for a mode change) will result in an ENTRY ERROR.

SLEWED EDGE MODE. When the SLEWED EDGE button is illuminated, the CG 5001/CG 551AP generates timing signals called "slewed edges" at the OUTPUT. These signals consist of a series of step functions, generated one at a time on successive triggered oscilloscope sweeps. After 15 edges have been generated, the function resets and starts over. The CG 5001/CG 551AP TRIGGER ON function must be active and connected to the oscilloscope external trigger input when operating in this mode.

Slewed edge spacing is set with the UNITS/DIV control at .4 ns/D or from .5 ns/D to .1 μs/D. If the UNITS/DIV control is set slower than .1 μs/D, the CG 5001/CG 551AP automatically switches to markers instead of slewed edges. With the VARIABLE button illuminated, the VARIABLE control adjusts the output to reflect a FAST or SLOW oscilloscope sweep speed error.

The slewed edges displayed on the oscilloscope can be shifted right or left one division at a time via the SHIFT buttons. If the MAG X10 button is illuminated, the slewed edges will be shifted 10 divisions at a time. Edges which have been shifted can be repositioned to trace start at any time by pressing the RESET button.

NOTE

A 50 Ω load is not required, though recommended, for the SLEWED EDGE mode.

1. Press the SLEWED EDGE button. The button should be illuminated.

2. Rotate the UNITS/DIV control through its range to observe values from .4 ns/D to .1 μs/D. When the UNITS/DIV control is rotated to display .2 μs/D, the CG 5001/CG 551AP automatically switches to the MARKERS mode. Return to the SLEWED EDGE mode.

3. Press the VARIABLE button. The button should be illuminated and 0.0% displayed. Rotate the VARIABLE control clockwise and counterclockwise to see that both FAST and SLOW percentages are displayed.

4. Press the CG 5001/CG 551AP OUTPUT ON button. Set the UNITS/DIV control to display .1 μs/D. In this mode the TRIGGER ON and NORM buttons are automatically illuminated and cannot be extinguished. Set the oscilloscope and CG 5001/CG 551AP controls to obtain a visible, stable display of one edge per division on the oscilloscope.

5. Adjust the CG 5001/CG 551AP VARIABLE control and observe the slewed edges horizontal movement.

6. Press the SHIFT buttons. Observe that the edges are shifted right and left, one division at a time, on the oscilloscope display.

7. Return the edges to trace start by pressing the RESET button.

8. Press the MAG X10 button; X10 MAG should be displayed. On the oscilloscope display observe that the period of the edges is reduced by a factor of 10 (all edges have been compressed into one division). The MAG X10 function is not valid at rates faster than 5 ns/D.

If the oscilloscope is so equipped, activate the magnified sweep feature. Adjust the oscilloscope's horizontal position control for one edge per division across the oscilloscope display.

Repeatedly press the SHIFT buttons and observe that the edges are shifted 10 divisions at a time.

9. RESET the slewed edges. Press the MAG X10 button to deactivate this function. Return the oscilloscope to normal sweep.

10. The only valid functions in this mode are UNITS/DIV, VARIABLE, MAG X10, SHIFT, RESET, and MAIN OUTPUT ON. Attempting to activate any others (except for a mode change) will result in an ENTRY ERROR.

11. This completes the Operators Familiarization Procedure.

NOTE

Operating instructions for the Comparator Head and Remote Variable accessories are located in their respective instruction manuals.

REPACKAGING FOR SHIPMENT

When returning your instrument to a Tektronix Service Center for service or repair, attach a tag to the instrument showing the owner (with address) and the name of an individual to be contacted, complete instrument serial number, and a description of the service required.

Save and re-use the package in which the instrument was shipped. If the original packaging is unfit for use or not available, repackage the instrument as follows:

1. Obtain a carton of corrugated cardboard having inside dimensions no less than six inches more than the instrument dimensions; this will allow for cushioning. The shipping carton test strength for your instrument is 200 pounds.

2. Surround the instrument with polyethylene sheeting to protect the finish.

3. Cushion the instrument on all sides by tightly packing dunnage or urethane foam between carton and instrument, allowing three inches on all sides.

4. Seal the carton with shipping tape or industrial staples.

5. Mark the shipping carton "FRAGILE", "DELICATE INSTRUMENT".

PROGRAMMING

INTRODUCTION

This section of the manual contains information and instructions for programming the TEKTRONIX CG 5001/CG 551AP operational functions via a remote controller.

Programming and remote control of the CG 5001/CG 551AP is via a digital interface specified and described in IEEE Standard 488-1975, "Standard Digital Interface for Programmable Instrumentation". In this manual, the digital interface is referred to as the General Purpose Interface Bus (GPIB).

NOTE

A basic concepts discussion for a typical GPIB system is located at the end of this section.

All of the CG 5001/CG 551AP output functions are programmable via high-level (ASCII) or low-level (binary) commands.

The CG 5001/CG 551AP has the capability of outputting data in response to a GPIB controller. The data is related to the status of the front panel controls, the actual errors (accuracy deviations) for the oscilloscope under test, and the CG 5001/CG 551AP internal status.

REMOTE-LOCAL FUNCTIONS

The Remote-Local functions of the CG 5001/CG 551AP are controlled by the system controller and the front panel controls. There are four states associated with the Remote-Local functions of the CG 5001/CG 551AP; two "local" states and two "remote" states.

Local State (LOCS)

While in LOCS, the front panel controls are under the control of the operator; the front panel settings cannot be changed via setting commands from the bus. However, the instrument will respond to and execute query commands via the bus (REN bus line need not be asserted). In a "local" state, all front panel controls are operational.

Local With Lockout State (LWLS)

If the CG 5001/CG 551AP enters the Local With Lockout State, the REM indicator light will not be lit and the instrument operates exactly as it does in the Local State (LOCS), except when it receives its listen address (MLA), it enters the Remote With Lockout State (RWLS).

Remote With Lockout State (RWLS)

When the CG 5001/CG 551AP enters the Remote With Lockout State, the operator cannot return the instrument to local control by depressing a front-panel key.

While in RWLS, the REM indicator will be illuminated, all setting commands, queries, and interface messages will be executed, and all front-panel controls will be ignored.

If a READ? query is pending and the instrument is in the talker active state (TACS), the CONTINUE button and VARIABLE control are enabled.

If the GTL (Go To Local) message is received while in RWLS, the instrument returns to the Local With Lockout State (LWLS).

NOTE

The CG 5001/CG 551AP returns to the Local State (LOCS) any time the REN bus line becomes unasserted (false). Any time the CG 5001/CG 551AP leaves a "remote" state and enters a "local" state, the current values of the front panel settings are assumed. When leaving a "local" state and entering a "remote" state, local control settings are used until overridden by a remote control message.

Remote State (REMS)

When the CG 5001/CG 551AP receives its listen address (with the REN bus line asserted) it enters the Remote State (REMS) and the REM indicator light is illuminated.

While in REMS, the CG 5001/CG 551AP responds to and executes all setting commands, queries, and interface messages. For all commands having corresponding front panel controls, the front panel is updated to display the new settings as the commands are executed.

If the CG 5001/CG 551AP is in REMS, there are three conditions under which it will return to the Local State (LOCS): 1) when a valid front panel control or remote variable head control (any control that changes the settings) is changed by the operator, 2) when the instrument receives the GTL interface message, or 3) if the REN bus line becomes unasserted (false). A "return to local" request is honored as soon as the current command is executed.

NOTE

The CG 5001/CG 551AP can be in either the Local State (LOCS) or Remote State (REMS) when the Local Lockout (LLO) interface message is received. If in LOCS, it will enter the Local With Lockout State (LWLS) or if in REMS, it will enter the Remote With Lockout State (RWLS) when LLO is received. The LWLS and RWLS functions are completely controlled by the controller.

GPIB ADDRESS AND MESSAGE TERMINATOR SWITCHES

The bus address and end of message terminator for input data are user set by a bank of six internal switches. These switches are located under an instrument cut-out through the right side panel, in the upper left front. The switches are illustrated in Fig. 3-1.

Address Switches

Switches 1 through 5 (Fig. 3-1) are used to encode, in binary form, the GPIB primary address. These switches can be set for any decimal address location over the full range allowed by the IEEE 488 standard. The decimal address range is from 0 through 30.

The switches can be set with a soft-pointed instrument, such as a pencil. For example, to set a switch to the ON (1) position, push on the upper part of the switch.

Setting the GPIB address switches automatically establishes both the primary listen and primary talk addresses, since they share the same five least significant bits on the GPIB data bus.

The controller program decides when the CG 5001/CG 551AP will talk or listen by setting data bits 7 and 6 in the address byte; 01 for listener and 10 for talker. Data bits 5 through 1 are set for the address location. The CG 5001/CG 551AP has no provision for the secondary addressing scheme defined by the IEEE 488 standard; secondary addresses are ignored.

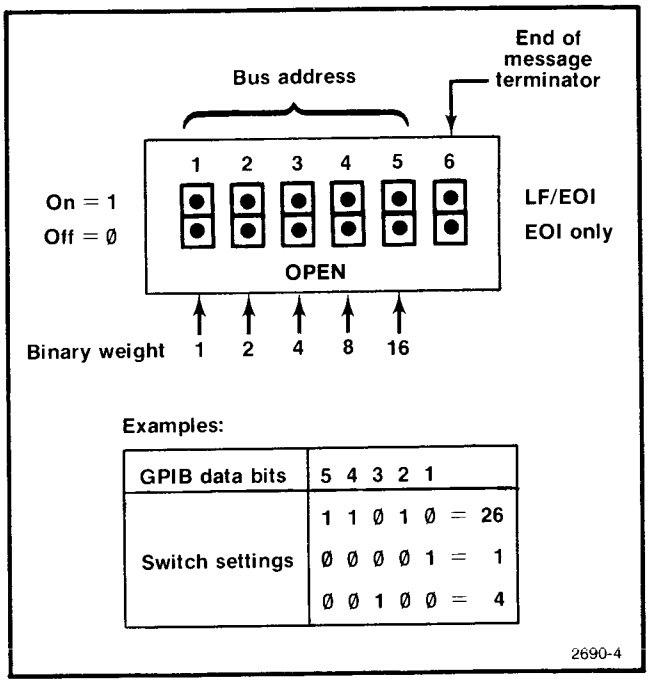


Fig. 3-1. Bus address and message terminator switches.

When powered up, the CG 5001/CG 551AP GPIB address can be determined by pressing the front panel INST ID pushbutton; the address location will be displayed in the display window. If the address switches are set for address 31, commands from the bus are handshaked, but ignored; effectively disconnecting the CG 5001/CG 551AP from the GPIB.

Input End of Message Terminator

Switch number 6 (Fig. 3-1) can be set for the CG 5001/CG 551AP to respond, when listening, to one of two possible end of message terminators that may occur on the GPIB: LF (line feed character) or EOI asserted. In the ON position for switch number 6, the CG 5001/CG 551AP responds to either LF or EOI; in the OFF position, it responds only to the assertion of the EOI line.

The GPIB EOI line may be asserted concurrently with the last byte in the message, whether it is data, format character, or a low-order delimiter, such as a semicolon. This is the common end of message terminator for Tektronix instruments.

The ASCII code for LF may be sent as a byte following the message and any format character or low-order delimiter. This is an alternative terminator provision for compatibility with various controllers.

When using the low-level language format, switch number 6 must be set to EOI only. The low level EOI data byte is the checksum byte.

Output End of Message Terminator

The CG 5001/CG 551AP outputs data or messages as follows. Each message unit is delimited by a semicolon <;> and terminated in one of two ways:

1. With switch number 6 in the EOI only position (OFF), the termination is <semicolon—EOI>.

2. With switch number 6 in the LF/EOI position (ON), the termination is <semicolon><carriage return><LF-EOI>.

GETTING STARTED

Power Up Sequence

The CG 5001/CG 551AP power up state can be one of two states:

1. Default settings as described in the following paragraphs.

2. Last used instrument settings, before power was turned off. The power up state is selected via an internal jumper.

NOTE

Refer the jumper setting to qualified service personnel.

When power is applied, the CG 5001/CG 551AP performs a self test routine, with the words SELF TEST appearing in the display window. The self test routine checks the instruments internal memory, internal shift registers, circuit conditions in the amplitude and timing sections, and checks for saved calibration constants in the battery back-up memory, etc.

The instrument may be programmed to execute its self test routine by sending the TEST command via the GPIB. After self test, the instrument will be set to its default settings. This allows a self test routine to be performed without cycling the power.

NOTE

After recognizing the TEST command, the CG 5001/CG 551AP GPIB interface will not function during the self test.

There is no capability to perform the TEST or INIT sequence via the front panel, other than using the main power switch.

When the self test routine is complete, the instrument enters the Local State (LOCS) and sets its standard power up default values: 1 V/D X1, 1 kHz, VARIABLE OFF, main OUTPUT off, CURRENT LOOP off, TRIGGER OUTPUT off, and the SRQ line on the GPIB asserted.

The CG 5001/CG 551AP must be serial polled to clear the power on service request (SRQ). Using the TEKTRONIX 4050-series controller in the "immediate" mode, the command format is:

POLL X, Y: <bus address> <carriage return>
PRINT X, Y <carriage return>

X indicates where the SRQ was found and Y has the status byte. Refer to the TEKTRONIX 4050-series documentation for further information related to the POLL command.

NOTE

The power on SRQ cannot be cleared by sending the Device Clear (DCL) or Selected Device Clear (SDC) interface messages. The power on request for service can only be cleared by handshaking the status byte via a serial poll sequence.

If an internal fault prevents the self test routine completion, an error code will appear in the display window (see CG 5001/CG 551AP Error Messages). The internal error will be reported to the controller when the CG 5001/CG 551AP is serial polled.

Depressing the front panel CONTINUE button clears the error code displays, but not the GPIB buffer. Refer the self-test error code conditions (if any) to qualified service personnel.

Reset Under Program Control

The CG 5001/CG 551AP may be set to its power up default settings by sending the INIT command via the GPIB, without executing the self test function.

Power Down Sequence

There are no special power down sequences. If there is a power failure transient of sufficient duration, or power supply failure for the microprocessor, a microprocessor reset condition will occur. Once the power is restored, the microprocessor will initiate the power up sequence.

```
LIST
100 ON SRQ THEN 190
110 DIM A$(200)
120 PRINT "ENTER SETTING(S) OR
          QUERY COMMANDS:"
130 INPUT C$
140 PRINT @4:C$
150 IF POS(C$,"?",1)=0 THEN 120
160 INPUT @4:A$
170 PRINT A$
180 GO TO 120
190 POLL X,Y;4
200 PRINT "SRQ STATUS BYTE:";Y
210 RETURN
```

Comments

100 Informs controller of SRQ handler.

110 Dimensions response string length.

120 Prompts user to input commands.

130 Loads high level commands from keyboard.

140 Commands are sent to the instrument at GPIB address 4.

150 Command is checked to see if it was a query.

160 If command was a query, get the response. A$ is the response.

170 Print response to user.

190 SRQ subroutine.

210

NOTE

Only one query command per command string allowed. Set CG 5001/CG 551AP end of message terminator to EOI only.

(2690-5)4768-05

Fig. 3-2. Talker/Listener program for the CG 5001/CG 551AP with 4050-series controller.

Talker-Listener Program

When using a TEKTRONIX 4050-series controller, set the CG 5001/CG 551AP end of message terminator switch to EOI only. The controllers input message delimiter is assumed to be <CR> (set by PRINT @ 37,0:0).

To retrieve information from the CG 5001/CG 551AP use, for example:

INPUT @ A9:A$

A9 represents the GPIB address and A$ must be dimensioned for the size of the response string (maximum characters is 150). This is also the format for high level responses.

To send setting or query commands to the CG 5001/CG 551AP use, for example:

PRINT @ A9:C$ or

PRINT @ A9: "MODE V;MULT 1"

```
0: dim A$[150]
1: dev "cg",701
2: rem 7
3: oni 7,"srq"
4: eir 7
5: ent "command-
  ",A$
6: cmd 7,"?"
7: wrt "cg",A$
8: if pos(A$,
  "?")>0;red "cg"
  ,A$;prt A$;prt
9: cmd 7,"_?"
10: gto 5
11: "srq":rds(70
  1)→A;cmd 7,"_";
  prt "srq",A;
  eir 7;iret
```

Comments

The 9825A must be configured with String, General I/O, and Extended I/O Rompack.

Set the CG 5001/CG 551AP end of message terminator to the LF position.

(2690-6A)4768-02

Fig. 3-3. Simple handler for the Hewlett-Packard 9825A Desktop Computer.

A9 represents the GPIB address and C$ is a string which contains the commands to be sent.

The program segments listed in Fig. 3-2 and Fig. 3-3 can be used as simple talker-listener programs. The segments allow the CG 5001/CG 551AP user to input high level commands and note the response.

IEEE 488 (GPIB) INTERFACE CONTROL MESSAGES

Sending Interface Control Messages

There are five groups of interface control messages sent with the GPIB Attention (ATN) line asserted. The WBYTE form given below for these messages are for the TEKTRONIX 4050-series controllers.

1. Talk Address Group (TAG)

   WBYTE @ A: causes CG 5001/CG 551AP to talk.

   WBYTE @ 95: causes CG 5001/CG 551AP to untalk.

   A = 64 + address (0-30). Address 31 causes CG 5001/CG 551AP to untalk.

2. Listen Address Group (LAG)

   WBYTE @ A: causes CG 5001/CG 551AP to listen.

   WBYTE @ 63: causes CG 5001/CG 551AP to unlisten.

   A = 32 + address (0-30). Address 31 causes CG 5001/CG 551AP to unlisten.

3. Address Command Group (ACG)

   WBYTE @ A, 1, 63: Go to Local (MLA, GTL, UNL).

   WBYTE @ A, 4, 63: Selected Device Clear (MLA, SDC, UNL).

   WBYTE @ A, 8, 63: Group Execute Trigger (MLA, GET, UNL).

   A = MLA = 32 + address (0-30).

   1 = GTL, 4 = SDC, and 8 = GET.

   63 causes CG 5001/CG 551AP to unlisten (UNL).

NOTE

Parallel Poll Configure (PPC) and Take Control (TCT) are not implemented in the CG 5001/CG 551AP.

4. Universal Command Group (UCG)

   WBYTE @ A, 17, 63:

   WBYTE @ 17: LLO (Local Lockout).

   First command sets CG 5001/CG 551AP to RWLS if REN is true. Second command sets CG 5001/CG 551AP to LWLS.

   WBYTE @ 20: DCL (Device Clear).

   WBYTE @ 24: SPE (Serial Poll Enable).

   WBYTE @ 25: SPD (Serial Poll Disable).

NOTE

Parallel Poll Unconfigure (PPU) is not implemented in the CG 5001/CG 551AP.

5. Secondary Command Group (SCG).

   WBYTE @ A: Not implemented; ignored by CG 5001/CG 551AP .

   A = 96 + address (0-30).

Response to Interface Control Messages

The CG 5001/CG 551AP responds to the following GPIB control messages in the following manner. All of the control messages, except IFC (Interface clear), are sent with ATN (Attention) asserted. See Fig. 3-6, ASCII & IEEE 488 (GPIB) Code Chart.

DCL ($14)— Device Clear. This interface message causes the CG 5001/CG 551AP to respond as follows:

Clear talk errors and displayed error codes.

Mask errors 1, 2, and 3.

Set all changed settings.

Resets pending settings, repeatable queries, present query, pending READ? query, the response to SRQ? query, pending GET message, and all SRQ's except the power on service request and the busy bit.

Go to the following system command default settings: OPC OFF, DT OFF (DTØ), RQS ON, and REM ON. (See Tables 3-1, 3-2, and 3-3.)

GET ($08)— Group Execute Trigger. If the CG 5001/CG 551AP is in the DT1 mode, decoded setting commands are buffered but not executed until the receipt of the GET message. DT1 mode is set by the DT ON command.

GTL ($01)— Go to Local. Causes the CG 5001/CG 551AP to go to a local state. In a local state, device-dependent messages continue to be accepted by the instrument; only those commands that do not affect the state of the front-panel controls are executed, such as a query command.

LLO ($11)— Local Lockout. If the CG 5001/CG 551AP is in the Remote State (REMS), this message causes the instrument to lock out all front-panel controls. If in the Local State (LOCS), this message causes the instrument to lock out all front-panel controls as soon as the instrument is set to a remote state.

SDC ($04)— Selected Device Clear. Same as DCL message.

SPE ($18), SPD ($19)— Serial Poll Enable and Serial Poll Disable; Configures instrument for serial poll capability.

IFC (Uniline)— Interface Clear. This message resets the CG 5001/CG 551AP interface functions only; it does not affect the operating modes. Untalks and Unlistens all instruments on the bus.

REMOTE CONTROL MESSAGES (HIGH LEVEL)

Introduction

Remote control messages for the CG 5001/CG 551AP are device dependent messages on the GPIB. As such, they are not specified in the IEEE 488 standard. High level remote control messages for the CG 5001/CG 551AP conform to the rules outlined in the following text. Low level remote control messages are described later in this section.

The CG 5001/CG 551AP responds to device dependent messages that contain one or both types of commands; set and query. A set command causes the CG 5001/CG 551AP to set its internal circuits and front panel controls to output specific signals for the desired operation. A query command causes the CG 5001/CG 551AP to return to the controller the status of a specified operating parameter.

High level remote control messages are sent in ASCII and the CG 5001/CG 551AP responds in ASCII. The CG 5001/CG 551AP ignores the parity bit on ASCII input and always sets it to zero on ASCII output. For high level language, lower level ASCII letters are interpreted as upper case.

Listen Mode

A remote control message begins when the CG 5001/CG 551AP is addressed as a listener and the controller begins talking. For set commands, the REN line on the GPIB must be asserted and the CG 5001/CG 551AP must be in REMS or RWLS. For query commands, the CG 5001/CG 551AP can be in a "local" state and the REN line need not be asserted. The message ends when the terminator is detected by the CG 5001/CG 551AP. The CG 5001/CG 551AP buffers all messages it receives and it does not begin execution of the commands until the terminator is received.

When listening, the CG 5001/CG 551AP responds to either of two message terminators, depending on the setting of an internal switch (see Fig. 3-1).

With EOI only selected as the message terminator, any combination of format characters can be inserted at the beginning of a message or after a delimiter. Format characters are:

<carriage return>, <line feed>, or <space>.

Format characters can also be used with LF (line feed) selected as the message terminator. However, the CG 5001/CG 551AP interprets LF as the end of the message. This interpretation holds up the data transfer because the CG 5001/CG 551AP does not continue to buffer the input, but first executes all commands received to that point before continuing to handshake data.

When the CG 5001/CG 551AP receives a query command, the response is generated when it is addressed to talk. After the message terminator is received, a pending query condition is set up. If a new message is then sent to the CG 5001/CG 551AP before the query response has been output, the query pending status will be reset and, when the instrument is addressed to talk, the response will be $FF-EOI (talked with nothing to say).

Talk Mode

When talking, the CG 5001/CG 551AP always uses EOI to terminate a message. It asserts the EOI line concurrently with the last byte in the message, normally the message unit delimiter (a semicolon). However, if the terminator switch is

set for LF/EOI as the message terminator, the CG 5001/CG 551AP adds <carriage return> and <line feed> beyond the normal end of the message (<semicolon>) and asserts EOI with LF. After the message terminator is sent, the CG 5001/CG 551AP does not send more data until it is retalked or serial polled. If the CG 5001/CG 551AP does not have a message to send when it is addressed to talk, it responds with $FF-EOI.

Command Syntax

The following format symbols are used:

< > indicates a defined element.

[ ] indicates the element or group of elements are optional and may be omitted.

. . . follows an element or group of elements that may be repeated.

NOTE

Formats given for the set and query commands are intended as guides and are not intended to fully define the format.

The following message delimiters are used to punctuate commands for the CG 5001/CG 551AP:

Delimiter	Follows
<space>	Header
<comma>	Argument
<semicolon>	Message Unit (Command)

Numbers

The CG 5001/CG 551AP maintains a "friendly" interface; all number formats are acceptable as input via the GPIB. When received, the number is interpreted to the correct format as an argument to a command. For example, 1 is interpreted as 001, 1E0, 1.0, etc. Numbers are rounded internally to two significant digits.

A suffix may be used to replace scientific units, where applicable, as follows:

K = Kilo = 1E+3
MEG = Mega = 1E+6
M = milli = 1E−3
U = micro = 1E−6
N = nano = 1E−9

For example, U/D 1n or 1N is the same as U/D 1.0E−9.

Three kinds of numbers are used to represent the arguments to commands:

Representation	Description
<nr1>	Signed or unsigned integers, including zero. The plus sign is optional for positive integers. Examples of these numbers are: 1, 2, 3, −1, −10, etc.
<nr2>	Signed or unsigned decimal numbers. The plus sign is optional for positive decimal numbers. Examples for decimal numbers are: −3.2, +5.0, 1.2, etc.
<nr3>	Floating point numbers expressed in scientific notation. The mantissa includes a decimal point and is preceded by a sign. The exrad following the mantissa begins with the character E, followed by a plus or minus sign and then one or more digits for the exponent of the multiplier. Examples: +1.0E−3 (for 1.0×10^{-3}), −1.E+4 (for -1×10^{4}), <space> 0.E+0 (for zero).

NOTE

An explicit definition of these types of numbers is given in ANSI X3.42-1975, "American National Standard for Representation of Numeric Values in Character Strings for Information Exchange".

Setting Commands

Headers and arguments in Table 3-1 are used as setting commands. The format for a single command is:

<header> <space> <argument> <semicolon>

Examples of single set commands are:

MODE V;

OUT ON;

More than one set command can be sent as part of a single message. This format requires the following syntax:

<set command> <semicolon><set command>

[<semicolon> <set command>] . . .
[<semicolon>]

An example of set commands in a single message is:

MODE V; U/D 20E−3; MULT 2; OUT ON;

One rule must be followed if more than one set command is transmitted as part of the same message: only one query command can be contained in the same message string. Query commands are commands that generate output data. The command string must be syntactically correct in its entirety in order to be executed. The string must also be a valid combination of settings.

Refer to Fig. 3-4 for an illustration of the CG 5001/CG 551AP functional modes and the high level setting commands associated with those functions.

Table 3-1

CG 5001/CG 551AP SETTING COMMANDS
(Setting Commands Not Executed in Local Mode)

Header	Argument	Description
A/D	<**nr3**>**A**	Sets mode to current and sets units per division.
CHOP	**OFF**	For amplitude modes only. Sets output signal level to 0 V.
	ON	Restores normal amplitude frequency output.
COMP	**CG**	Sets comparator head to CG 5001/CG 551AP output.
	DUT	Sets comparator head to device under test (dut) output.
	AUTO	Sets comparator head to chop between CG 5001/CG 551AP output and dut output.
CS	**ON**	Sets continuous slewing for SLEWED EDGE mode. Used for calibration.
	OFF	Restores normal slewing mode.
DEC		Subtracts 0.1 from present percent error readout for HIGH and FAST indications or adds 0.1 for LOW and SLOW indications.
DLY	**ON**	Sets delayed trigger for FAST EDGE mode. Used for calibration.
	OFF	Restores normal trigger mode for FAST EDGE.
DSP	**ON**	Enables variable display for EDGE or FAST EDGE modes.
	OFF	Disables variable display for EDGE or FAST EDGE modes.
DT	**OFF**	Sets status to DTØ mode; settings executed after receipt of EOI.
	ON	Sets status to DT1 mode; buffer the decoded settings and execute on receipt of the GET message.
EDGE	<**nr1**>	Sets number of edges generated for one slewing cycle. Number can be from 1 to 15.
FREQ	**DC**	Sets chop frequency to DC.
	<**nr3**>	Sets chop frequency from 10 Hz to 1 MHz.
FXD		Sets instrument to 0.0% error with error display off.
HOLD	<**nr1**>	For the SLEWED EDGE mode. Changes trigger period in 0.82 μs increments (.5 ns/div—100 ns/div) or in 1.02 μs increments (.4 ns/div). Number can be -1, 0, $+1$, $+2$, or $+3$.
INC		Adds 0.1 to present dut error readout for HIGH and FAST indications or subtracts 0.1 for LOW and SLOW indications.

Table 3-1 (cont)

Header	Argument	Description
LDZ	50	Informs instrument to compensate for 50 Ω termination. Turns on USE FOR 50 Ω LOAD button.
	HI	Informs instrument to compensate for high-impedance termination. Turns off USE FOR 50 Ω LOAD button.
LOOP	ON	Turns current loop on.
	OFF	Turns current loop off (power up condition).
LSHF		Decrements shift counter by 1.
MODE	V or VOLTAGE	Sets instrument to VOLTAGE mode.
	CUR or CURRENT	Sets instrument to CURRENT mode.
	EDGE	Sets instrument to EDGE mode.
	FE or FASTEDGE	Sets instrument to FAST EDGE mode. Pulse Head must be attached.
	MKRS or MARKERS	Sets instrument to MARKERS mode.
	SLWD or SLEWED	Sets instrument to SLEWED EDGE mode.
MAG	X1	Sets time/division magnifier to X1.
	X10	Sets time/division magnifier to X10.
MASK	<nr1>	Mask error so that SRQ will not be sent. Only one argument allowed. Argument can be 1, 2, or 3.
MULT	<nr1>	Sets NUMBER OF DIVISIONS multiplier. Number can be 1, 2, 3, 4, 5, 6, 8, or 10. Does not apply to FAST EDGE mode.
NEG		Sets negative EDGE polarity.
NM	ON	Set narrow markers mode. Reduces marker pulse width by a factor of 10 (10 μs—5 sec range).
	OFF	Disables narrow markers mode. Returns markers to normal pulse width.
OUT	ON	Sets main OUTPUT on.
	OFF	Sets main OUTPUT off (power up condition).
POS		Sets positive EDGE polarity.
PCT	<nr2>	Sets dut percent error readout. Instrument operation with this command is similar to that when using the front panel VARIABLE control. Argument can be −0.1 to −9.9 for LOW or SLOW or +0.1 to +9.9 for HIGH or FAST.
RSHF		Increments shift counter by 1.
S/D	<nr3>S	Sets markers or slewed edge modes to appropriate units per division. For argument range refer to the UNITS/DIV data listed in Table 3-7.

Table 3-1 (cont)

Header	Argument	Description
SHFT	<**nr1**>	Sets shift counter to argument value. Argument value can be as follows: .4 ns/div— −25 to +25. .5 ns/div— −99 to +99. 1 ns/div— −99 to +99. 2 ns/div— −99 to +99. 5 ns/div— −99 to +99. 10 ns/div— −40 to +40. 20 ns/div— −20 to +20. 50 ns/div— −10 to +20. .1 μs/div— −5 to +20.
TRIG	**ON**	Turns TRIGGER OUTPUT on.
	OFF	Turns TRIGGER OUTPUT off. Output cannot be turned off when operating in SLEWED EDGE mode.
	NORM	Sets trigger rate same as output signal rate.
	X.1	Turns on TRIGGER OUTPUT and sets trigger rate to one-tenth output signal rate (except slewed edges).
	X.01	Turns on TRIGGER OUTPUT and sets trigger rate to one-hundredth output signal rate (except slewed edges).
U/D	<**nr3**>	Sets desired units per division.
UMSK	<**nr1**>	Unmasks error that was masked. Only one argument allowed. Number can be 1, 2, or 3.
VAR		Sets instrument to display dut percent error readout.
V/D	<**nr3**>**V**	Sets instrument to VOLTAGE mode and desired number of units/division.
ZSHF		Resets shift counter to zero. Same as SHFT Ø.

Query Commands

Refer to Table 3-2 for CG 5001/CG 551AP query commands and their description.

A query command is executed in either remote or local mode. A message that contains only a query command requires the following syntax:

<header> <question mark> [<semicolon>]

An example is:

PCT?

A message string should contain only one query command. The query may be preceded by one or more set commands. A message that contains both set commands and a query command requires the following syntax:

<set command> <semicolon> [<set command> <semicolon>] . . .

<query command> [<semicolon>]

An example is:

MODE MKRS;SET?

If more than one query command is received in a message, the last one received is the only query interpreted as valid.

The CG 5001/CG 551AP responds to a query with a message similar to the set command format when it is next made a talker. The syntax is, for example:

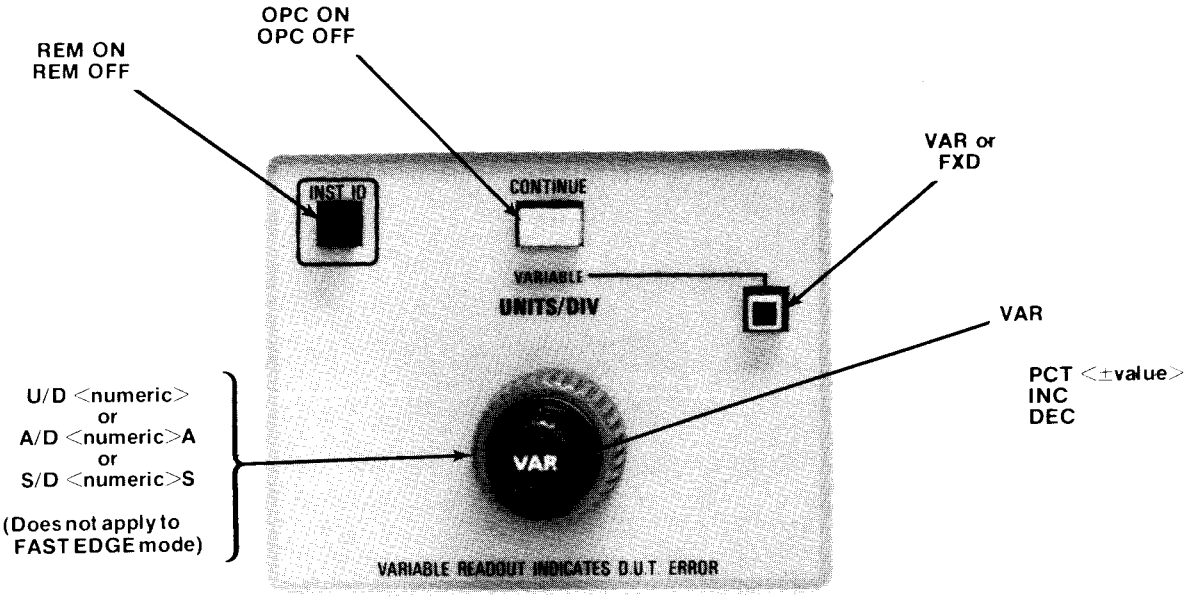
PCT? is answered as **PCT 0.2;**

DSPL? is answered as **PCT 0.1; U/D 1.0E—1;**

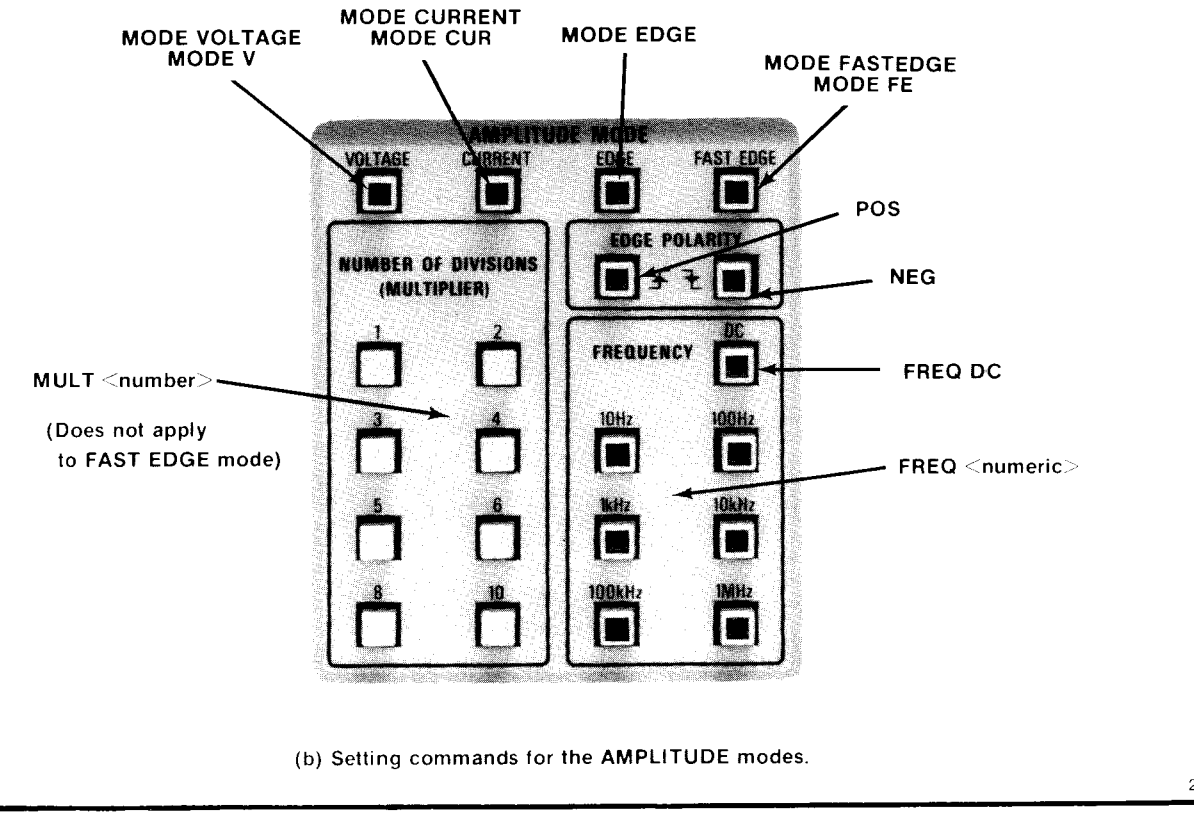
Table 3-2

CG 5001/CG 551AP QUERY COMMANDS

Query	Response	Description
CSET?	<**message unit**>...	Returns changed settings information to the controller. Value is "NONE" if settings have not changed.
DSPL?	<**message unit**>...	Returns present units/division and dut percent error information.
ERR?	<**nr1**>	Returns number codes for error conditions. More than one argument allowed. If no errors, response is ERR Ø.
ID?	**TEK/CG 551AP, V79.1, LLL or TEK/CG 5001, V79.1, Fxx**	Returns identity of instrument.
PCT?	<**message unit**>	Returns present dut percent error information.
READ?	<**message unit**>...	Returns present units/division and dut percent error after operator presses CONTINUE key.
RPT?		CG 5001/CG 551AP repeats last message sent.
SET?	<**message unit**>...	Returns settings of instrument in device-dependent format.
SRQ?		Returns reason for Service Request (SRQ).
TSET?	**NULL**	Returns null message.
U/D?	<**nr3**>	Returns present units/division.
VERS?	**H**<**IDVVCCCC**>	Responds with: ID — Most significant byte of ROM base address. VV — Version number. CCCC — 16-bit checksum. Where each character is a hexadecimal digit (0—9, A—F).



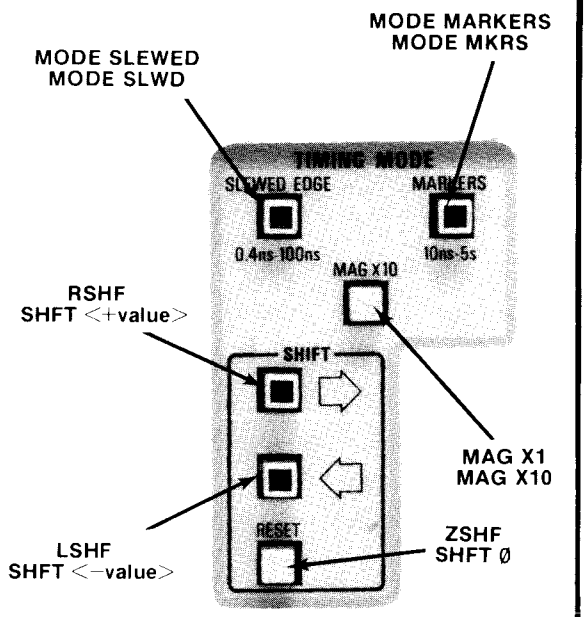
(a) Setting commands for the UNITS/DIV, VARIABLE, INST ID, and CONTINUE functions.



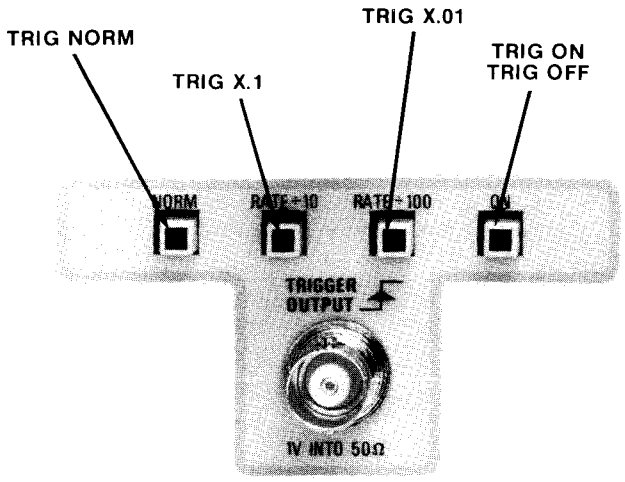
(b) Setting commands for the AMPLITUDE modes.

2690-7

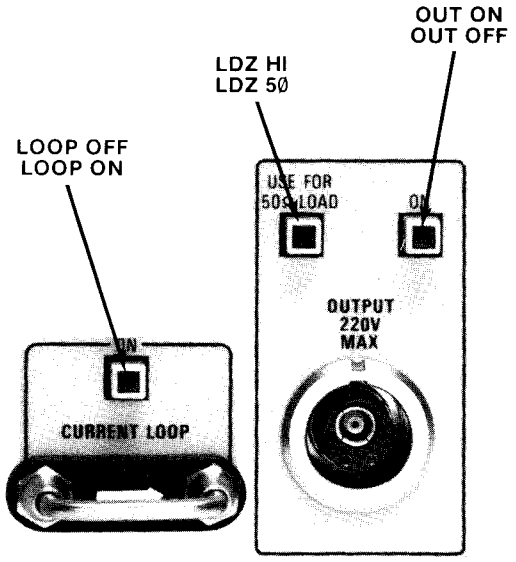
Fig. 3-4A. Setting commands for the CG 5001/CG 551AP.



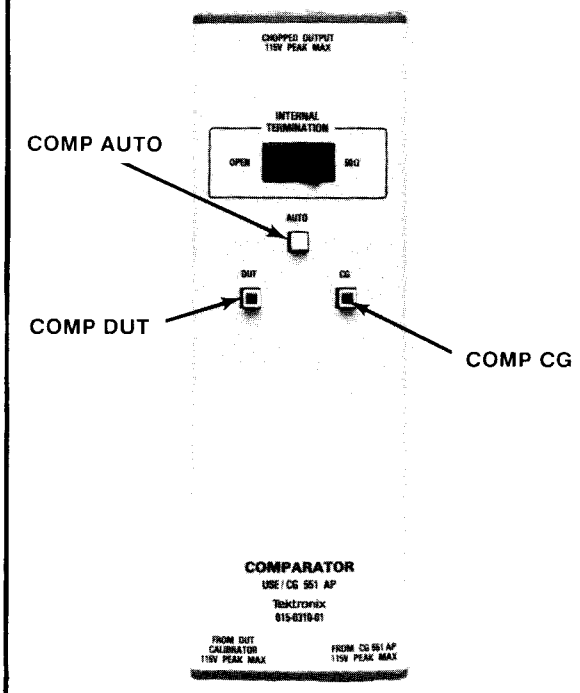
(c) Setting commands for the TIMING modes.



(d) Setting commands for the TRIGGER OUTPUT functions.



(e) Setting commands for the CURRENT LOOP and main OUTPUT functions.



(f) Setting commands for the COMPARATOR functions.

2690-8

Fig. 3-4B. Setting commands for the CG 5001/CG 551AP.

System Commands

The CG 5001/CG 551AP will respond to the system commands as described in Table 3-3.

Table 3-3

SYSTEM COMMANDS

Header	Argument	Description
INIT		Sets instrument to default settings or to the last used settings when powered down.
TEST		Activates instrument power on self test routine.
RQS	**OFF** **ON**	Controls instrument capability to send Service Request (SRQ). Powers up with SRQ asserted (RQS ON).
REM	**OFF** **ON**	Controls generation of SRQ function when INST ID button is pressed. Powers up with REM ON.
OPC	**OFF** **ON**	Controls generation of SRQ for operation complete when the CONTINUE is pressed. Powers up with OPC OFF.

STATUS BYTE INFORMATION

Introduction

The CG 5001/CG 551AP status byte (reported to the controller when the instrument is serial polled) contains the following information:

Bit 8 — System status = 0 (most significant bit).

7 — Service requested = 1; service not requested = 0.

6 — Abnormal condition = 1; normal condition = 0.

5 — Busy decoding, executing, or waiting to complete READ? query operation = 1; normal = 0.

4 — Encoded system status.

3 — Encoded system status.

2 — Encoded system status.

1 — Encoded system status.

Normal Condition System Status

The following status bytes are returned under normal operating conditions:

8	**7**	**6**	**5**	**4**	**3**	**2**	**1**	
0	1	0	X	0	0	1	0	—Operation complete, CONTINUE button pressed.
0	0	0	0	0	0	0	0	—Nothing to report.
0	1	0	X	0	0	0	1	—Power-on condition.
0	1	0	X	0	0	0	0	—SRQ query request (INST ID button was pressed).

The power-on condition cannot be cleared by the Device Clear (DCL or SDC) message. The power-on request for service (rsv) is cleared only by handshaking out the status byte to the controller.

The SRQ query request is similar to the ERR query request. The controller should send SRQ? to retrieve the status byte.

Abnormal Condition Status

Abnormal conditions (errors) are reported before other status (except when replaced by the power-on condition). There are three abnormal condition status bytes; they are:

8 7 6 5 4 3 2 1

0 1 1 X 0 0 0 1 — Command error.

0 1 1 X 0 0 1 0 — Execution error.

0 1 1 X 0 0 1 1 — Internal error.

Command error indicates that the instrument has received a command which it cannot understand or implement under any circumstances. The command will not affect the state of the instrument.

Execution error indicates that the instrument has received a command which it understands, but cannot execute due to present state of the instrument or the command is out of instrument range.

Internal error indicates that the instrument is uncalibrated or has detected a hardware failure; error may result from the self-test routine.

NOTE

Refer to CG 5001/CG 551AP Error Messages for more information concerning error messages that cause the CG 5001/CG 551AP to assert SRQ.

CG 5001/CG 551AP ERROR MESSAGES

The error messages listed in Table 3-4 may be displayed and, when requested, reported to the GPIB controller.

NOTE

Error messages 11, 12, 95 through 98, and the read only memory (ROM) errors do not cause the CG 5001/CG 551AP to assert the SRQ line on the GPIB. All others will cause SRQ to be asserted except when they are prevented from doing so by a high level command, such as MASK or RQS OFF.

Table 3-4

CG 5001/CG 551AP ERROR MESSAGES

Message Number	Error Message
	(Operational Errors)
1	Current overload, UNCAL.
2	Voltage overload, UNCAL.
3	Edge overload, UNCAL.
4	No pulse head attached; FASTEDGE command received from GPIB.
5	Accessory head shorted.

NOTE

Errors 1, 2, and 3 cause UNCAL to be displayed, but error message number is reported to the controller.

Table 3-4 (cont)

Message Number	Error Message
	(Internal Errors)
11	CMOS ram memory failure.
12	NMOS ram memory failure.
13	Error in saved settings, set to defaults.
14	Main loop out of lock.
15	Reference loop out of lock.
16	Offset loop out of lock.
17	Internal calibration constants out of cal. If in AMPLITUDE mode and this error was indicated at power on, a U will be displayed where /D would normally be displayed.

NOTE

Errors 11 and 12 will not allow operation of the CG 5001/CG 551AP after an error condition is indicated.

	(GPIB High Level Errors)
21	Invalid command keyword.
22	Combined decoded settings not executable.
23	Last response may not be repeated (RPT?).
24	Value error—argument not in range.
25	Format error—invalid use of semicolon.
26	Input buffer overflow (too many characters in message).
27	Invalid character in command.
28	Hex argument error.
	(GPIB Low Level Errors)
31	Invalid command byte.
32	Invalid subcommand (invalid setting for MODE).
33	Invalid subcommand.
35	Format error.
36	Checksum error.
	(GPIB General Errors)
41	Unrecognized addressed command group (ACG) message.
43	System error (invalid error code).
44	Invalid output encoding.
45	Unrecognized universal command group (UCG) message.
46	Output request error.
47	Output buffer overflow.

Table 3-4 (cont)

Message Number	Error Message			
	(Self Test Error)			
	Voltage Mode			Related circuit block
51	1 V	50 Ohm	DC	Low SAC
52	1 V	Hi-Z	DC	Low SAC
53	1 V	50 Ohm	1 kHz	Low SAC
54	20 V	Hi-Z	DC	High SAC
55	20 V	Hi-Z	1 kHz	High SAC
	Current Mode			Related circuit block
56	100 mA	50 Ohm	DC	Current Amplifier and Chopper
57	100 mA	50 Ohm	1 kHz	Current Amplifier and Chopper
	Negative Edge Mode			Related circuit block
81	+1 V	50 Ohm	DC	Low Edge Generator
82	+1 V	50 Ohm	1 kHz	Low Edge Generator
	Positive Edge Mode			Related circuit block
83	−1 V	50 Ohm	DC	Low Edge Generator
84	−1 V	50 Ohm	1 kHz	Low Edge Generator
85	−5 V	Hi-Z	DC	Mid Edge Generator
86	−5 V	Hi-Z	1 kHz	Mid Edge Generator
87	−20 V	Hi-Z	DC	High Edge Generator
88	−20 V	Hi-Z	1 kHz	High Edge Generator
	Time Mode			Related circuit blocks
91	1 sec timing accuracy with respect to 10 kHz reference frequency.			Count Down Circuit, Reference Divider.
92	.5 sec timing accuracy with respect to 10 kHz reference frequency.			Count Down Circuit, Reference Divider.
93	.2 sec timing accuracy with respect to 10 kHz reference frequency.			Count Down Circuit, Reference Divider.
94	Cannot perform timing accuracy tests.			TS1 Error Gates.
	Data Registers			Related circuit blocks
95	TS1 data register not functioning.			Data Registers, Slewing Data Register, Trigger Data Register, and Slewing Control.
96	TS2 data register not functioning.			Marker Data Register.
97	VS1 data register not functioning.			Reference Data Register, Data Isolators, and Floating Data Register.
98	VS2 data register not functioning.			Power On Test, Output Relay Control.

Note

Errors 95 through 98 will not allow operation of the CG 5001/CG 551AP after error indication.

REMOTE CONTROL MESSAGES (LOW LEVEL)

Introduction

Low level language is a protocol that allows rapid decoding of the setting commands, query commands, and the rapid data transfer on response to these commands. The memory space required to save low level commands and data is much less (and may be more efficient) than the space required to store high level commands in the controllers memory. The low level commands have no English-like comparison to the function performed, like the high level command counterparts.

The commands and queries available in the low level format are a subset of commands and queries available in high level. Only the functions of changing the 13 basic settings and the setting query (SET?) are implemented in low level language.

With the CG 5001/CG 551AP low level language, you have the ability to perform the translation of setting information between high level and low level (and vice versa). For example, you can send setting information in high level, then use the low level SET? query (DC1,$11) to get the low level translation.

A restriction is that low level language may not be included in the same message as high level. The low level language has a restricted format, which does not allow extraneous characters. Since no checks for validity of data (other than mode) are made, data integrity is checked by using a checksum byte.

General Format

Low level messages begin with an ASCII control character to denote that a low level command string follows the control character. An exception to this is that leading ASCII <CR> or <LF> is interpreted as high level formatting characters and is not allowed in the low level transmission. The low level control characters for the CG 5001/CG 551AP are described in Table 3-6.

The control character at the beginning of the low level message is followed by device dependent data in 8-bit binary bytes.

The values for the device dependent data are shown in Table 3-7 and Table 3-8. Following the formatted data is an 8-bit checksum as the last byte in the message. The EOI line is asserted concurrently with this last byte. The checksum is the 2's complement sum (modulo 256) of all the preceding bytes of the message. The syntax, for example, is:

<control character> [<data byte>]... <checksum-EOI>.

Error Checking

It is not necessary to check low level language for errors beyond assuming that the format and checksum are correct. The programmer must ensure that only valid settings data is

Table 3-5

LOW LEVEL FORMAT DESCRIPTION

Function	Hex Byte	Decimal Equivalent	Setting
Control Character	$15	21	Command for "all settings"
Edge Polarity	$00	0	Positive edge polarity
Frequency	$02	2	100 Hz
Units/Division	$15	21	2 mV
Multiplier	$04	4	4
Load Compensation	$00	0	Hi-Z, 50 Ω off
Shift-Slewed Edge	$00	0	0
Magnifier	$00	0	Normal (X1)
Mode	$01	1	Voltage
Current Loop	$00	0	Off
Output	$FF	255	ON
Trigger Rate	$81	129	ON, Rate ÷ 10
Variable	$FF	255	ON
Error Variable	$F1	241	1.5% LOW
Checksum—EOI	$5F	−95	

sent to the instrument. By using the built in translation process, or other application programs, the validity will be ensured; the CG 5001/CG 551AP always responds with valid setting information in the high-level format. The CG 5001/CG 551AP's microprocessor only ensures that a code will not be passed to the instrument setting registers, which may damage the instrument.

Low Level All Settings Commands

The low level setting information listed in Table 3-7 is used with the NAK command listed in Table 3-6. The following is an example of a low level all settings command string. The explanation of this format is found in Table 3-5.

150002150400000000100FF81FFF15F

Table 3-6

LOW LEVEL CONTROL CHARACTERS AND QUERY COMMANDS

Control Character		Description
Hex Code	**ASCII Name**	
$15	**NAK**	All settings command followed by 13 nonspaced bytes of position dependent setting information, ending with checksum with EOI asserted (15 bytes total).[c]
$16	**SYN**	An item command followed by individual bytes to set specific settings (not all 13 pieces of setting information required), ending with checksum and EOI asserted.[d]
$11	**DC1**	Query all settings command. Response is <$15><13 bytes of settings><checksum—EOI>.[a b]
$12	**DC2**	Query changed settings command. Response same as for $11 query.
$13	**DC3**	Low level form of READ? query, but response is in high level format.

Notes:

[a]Format for queries: <query byte> <checksum-EOI>.

[b]Checksum definition: 2's complement of the sum (modulo 256) of all the preceding bytes of the message. The checksum is the last byte of the message.

[c]Setting information used with the NAK command is found in Table 3-7.

[d]Setting information for the SYN command is found in Table 3-8.

Table 3-7
POSITION DEPENDENT LOW LEVEL SETTING INFORMATION
Send in the order listed

Order	Setting	Hexadecimal Value			
1	EDGE POLARITY	$00	positive		
		$FF	negative		
2	FREQUENCY	$00	DC		
		$01	10 Hz		
		$02	100 Hz		
		$03	1 kHz		
		$04	10 kHz		
		$05	100 kHz		
		$06	1 MHz		
3	UNITS/DIV	$00	.4E-9	$11	1E-3
		$01	.5E-9	$12	.2E-3
		$02	1E-9	$13	.5E-3
		$03	2E-9	$14	1E-3
		$04	5E-9	$15	2E-3
		$05	10E-9	$16	5E-3
		$06	20E-9	$17	10E-3
		$07	50E-9	$18	20E-3
		$08	.1E-6	$19	50E-3
		$09	.2E-6	$1A	.1E0
		$0A	.5E-6	$1B	.2E0
		$0B	1E-6	$1C	.5E0
		$0C	2E-6	$1D	1E0
		$0D	5E-6	$1E	2E0
		$0E	10E-6	$1F	5E0
		$0F	10E-6	$20	10E0
		$10	50E-6	$21	20E0
				$22	50E0
4	NUMBER OF DIVISIONS (MULTIPLIER)	$01	1		
		$02	2		
		$03	3		
		$04	4	$07 and $09	
		$05	5	not allowed	
		$06	6		
		$08	8		
		$0A	10		
5	USE FOR 50 Ω LOAD	$00	Hi-Z, 50 Ω Off.		
		$FF	50 Ω On.		
6	SHIFT	2's complement number for shift position, -128_{10} to $+127_{10}$. For allowed ranges, see high level SHIFT command, Table 3-1.			
7	MAG X10	$00	Off (Normal, MAG X1)		
		$FF	On		
8	Modes	$00	CURRENT		
		$01	VOLTAGE		
		$02	EDGE		
		$03	FAST EDGE		
		$04	SLEWED EDGE		
		$05	MARKERS		

Table 3-7 (cont)

Order	Setting	Hexadecimal Value
9	CURRENT LOOP	$00 Off $FF On
10	OUTPUT	$00 Off $FF On
11	Trigger Rates e.g., for NORMAL, ON, byte = $80 for RATE ÷ 10, ON, byte = $81	**8 7 6 5 4 3 2 1** 1 0 0 0 0 0 X X ON 0 0 0 0 0 0 X X Off X 0 0 0 0 0 0 0 NORMAL X 0 0 0 0 0 0 1 RATE ÷ 10 X 0 0 0 0 0 1 1 RATE ÷ 100
12	VARIABLE	$00 Off (fixed) $FF On
13	Error Variable Setting	Use 2's complement number -99_{10} to $+99_{10}$. $FF → $9D = −0.1 → −9.9 (LOW or SLOW) $01 → $63 = +0.1 → +9.9 (HIGH or FAST)

Low Level Item Commands

The commands listed in Table 3-8 are provided to eliminate the need to send all thirteen parameters to change settings. This format differs from the Low Level All Settings Commands in that the item for a new setting is not position dependent. Each item is encoded with the setting parameter it will change. The basic format is:

<$16> <setting(s) in device-dependent low level format>
<Checksum-EOI>, where $16 is the hexadecimal equivalent of the ASCII <SYN> character. See Table 3-6.

The low level item commands may be used in any sequence. The commands for UNITS/DIV, SHIFT, and the Error Variable require two bytes for setting information.

The following is an example of how to use the low level item commands:

To set the CG 5001/CG 551AP to VOLTAGE MODE, 2 DIVISIONS, VARIABLE ON, PCT −3.7, OUTPUT ON, send:

<$16> <$17> <$23> <$FB> <$0C> <$C9> <$F9> <$E7 with EOI>.

To change to 3 DIVISIONS simply send:

<$16> <$33> <$B7 with EOI> (hex)
22 51 183 (decimal)

Table 3-8
LOW LEVEL ITEM COMMANDS

Setting	Value		
EDGE POLARITY	Basic Form	$X0,	where X conveys polarity information.
		$F0	negative edge
		$00	positive edge
FREQUENCY	Basic Form	$X1,	where X indicates decade.
		$01	DC
		$11	10 Hz
		$21	100 Hz
		$31	1 kHz
		$41	10 kHz
		$51	100 kHz
		$61	1 MHz
UNITS/DIV	This is a two byte command.		
		$02 $00	.4E9 (See UNITS/DIV, Table 3-7)
		$02 $01	.5E9
		.	
		.	
		$02 $22	50E0
NUMBER OF DIVISIONS (MULTIPLIER)		$13	1 Division
		$23	2 Divisions
		.	
		.	$73 and $93 not allowed
		.	
		$A3	10 Divisions
USE FOR 50 Ω LOAD		$F4	50 Ω ON
		$04	Hi-Z, 50 Ω Off
SHIFT			This is a two byte command where XX is hexadecimal representation of the 2's complement number indicating shift value.
	Basic Form	$05 XX.	
		$05 $FF	SHFT −1 (left)
		$05 $02	SHFT 02 (right)
MAG X10	Basic Form	$X6	
		$F6	On
		$06	Off (NORMAL, MAG X1)
Modes	Basic Form	$X7	
		$07	CURRENT
		$17	VOLTAGE
		$27	EDGE
		$37	FAST EDGE
		$47	SLEWED EDGE
		$57	MARKERS
CURRENT LOOP	Basic Form	$X8	
		$F8	ON
		$08	OFF

Table 3-8 (cont)

<table>
<tr><th>Setting</th><th>Value</th></tr>
<tr><td>OUTPUT</td><td>Basic Form $X9
$F9 ON
$09 OFF</td></tr>
<tr><td>Trigger Rates</td><td>Basic Form $XA, where X = MSB, A = LSB
<table>
<tr><th colspan="2">X = MSB</th><th>LSB</th></tr>
<tr><th>Trigger Output</th><th>Rate</th><th>A</th></tr>
<tr><td>ON = 1</td><td>0 0 0</td><td>1 0 1 0</td></tr>
<tr><td>OFF = 0</td><td>0 0 1</td><td>1 0 1 0</td></tr>
<tr><td></td><td>0 1 0</td><td>1 0 1 0</td></tr>
</table>
Examples:
$8A TRIG ON, NORMAL
$9A TRIG ON, RATE ÷ 10
$AA TRIG ON, RATE ÷ 100</td></tr>
<tr><td>VARIABLE</td><td>$FB ON
$0B Off (fixed)</td></tr>
<tr><td>Error Variable</td><td>Basic Form $0C XX. This is a two byte command where XX is the hex equivalent of the 2's complement representation of the desired value for the error variable multiplied by 10.
Examples:
$0C $FF PCT −0.1
$0C $63 PCT 9.9</td></tr>
</table>

GPIB SYSTEM CONCEPTS

INTRODUCTION

The GPIB is a digital interface that allows efficient communication between the components of an instrumentation system.

The primary purpose of the GPIB is to connect self-contained instruments to other instruments or devices. This means that the GPIB is an interface system independent of device functions.

There are four elements of the GPIB: mechanical, electrical, functional, and operational.

Of these four, only the last is device-dependent. Operational elements state the way in which an instrument reacts to a signal on the bus. These reactions are device-dependent characteristics and state the way in which the instruments use the GPIB via application software.

Mechanical Elements

The standard defines the mechanical elements: cables and connectors. Standardizing the connectors and cables ensures that GPIB-compatible instruments can be physically linked together with complete pin compatibility.

The connector has 24 pins, with 16 assigned to specific signals and eight to shields and grounds. Instruments on the bus may be arranged in a linear or star configuration.

Electrical Elements

The voltage and current values required at the connector nodes for the GPIB are based on TTL technology (power source not to exceed +5.25 V referenced to logic ground). The standard defines the logic levels as follows. Logical 1 is true state, low-voltage level ($\leq$+0.8 V), signal line is **asserted**. Logical 0 is false state, high-voltage level ($\geq$+2.0 V), signal line is **not asserted**.

Messages can be sent over the GPIB as either active-true or passive-true signals. Passive-true signals occur at a high-voltage level and must be carried on a signal line using open-collector devices. Active-true signals occur at a low-voltage level.

Functional Elements

The functional elements of the GPIB cover three areas:

1. **Ten interface functions** (listed in Table 3-9) that define the use of specific signal lines so that an instrument can receive, process, and send messages. The ten interface functions—with their allowable subsets—provide an instrumentation system with complete communications and control capabilities.

Not every instrument on the bus has all ten functions because only those functions important to a particular instrument's purpose need be implemented.

2. The **specific protocol** by which the interface functions send and receive their limited set of messages.

3. The **logical and timing relationships** between allowable states for the interface signal lines.

Table 3-9
MAJOR GPIB INTERFACE FUNCTIONS

Interface Functions	Symbol
Source Handshake	SH
Acceptor Handshake	AH
Talker or Extended Talker	T or TE
Listener or Extended Listener	T or LE
Service Request	SR
Remote-Local	RL
Parallel Poll	PP
Device Clear	DC
Device Trigger	DT
Controller	C

A TYPICAL GPIB SYSTEM

Figure 3-5 illustrates an example of the GPIB and the nomenclature for the 16 active signal lines. Only four instruments are shown, but the GPIB can support up to 15 instruments connected directly to the bus. However, more than 15 devices can be interfaced to a single bus if they do not connect directly to the bus but are interfaced through a primary device. Such a scheme can be used for programmable plug-ins housed in a mainframe where the mainframe is addressed with a primary address code and the plug-ins are addressed with a secondary address code.

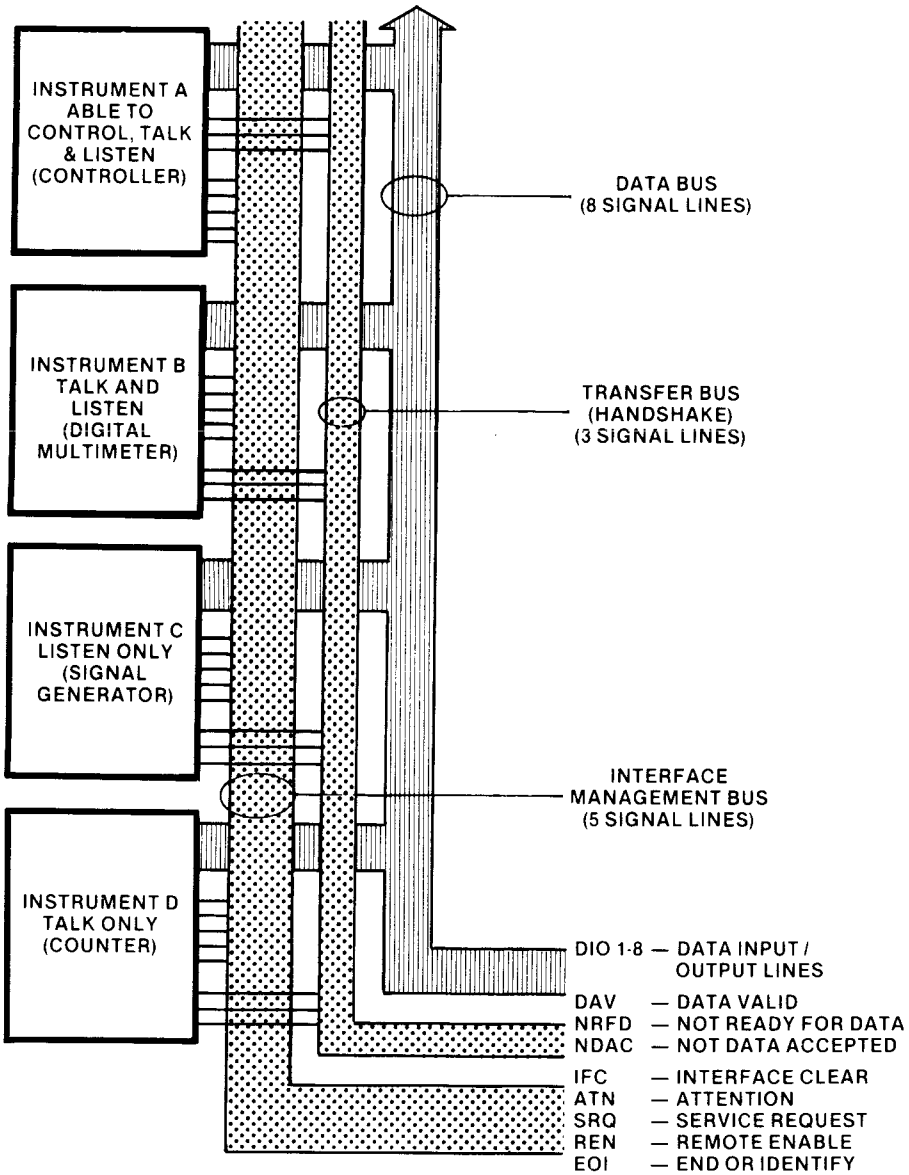


Fig. 3-5. A typical system using the general purpose interface bus (GPIB).

The instruments connected to a single bus cannot be separated by more than 20 meters (total cable length) and at least one more than half the number of instruments must be in the power-on state. To maintain the electrical characteristics of the bus, a device load must be connected for each two meters of cable length. Although instruments are usually spaced no more than two meters apart, they can be separated farther if the required number of device loads are lumped at any one point.

Controllers, Talkers, and Listeners

A **talker** is an instrument that can send data over the bus; a **listener** is an instrument that can accept data from the bus. No instrument can communicate until it is enabled to do so by the controller in charge of the bus.

A **controller** is an instrument that determines, by a software routine, which instrument will talk and which instruments will listen during any given time interval. The controller also has the ability to assign itself as a talker or listener whenever the program routine requires. In addition to designating the current talker and listeners for a particular communication sequence, the controller has the task of sending special codes and commands (called **interface messages**) to any or all of the instruments on the bus.

Interface Messages

The IEEE standard specifies that the interface messages, as shown in Fig. 3-6, ASCII & IEEE 488 (GPIB) Code Chart, be used to address and control instruments interfaced to the GPIB. Interface messages are sent and received only when the controller asserts the ATN bus line. The user can correlate interface message coding to the ISO 7-bit code by relating data bus lines DI01 through DI07 to bits 1 through 7, respectively.

Interface messages include the primary talk and listen addresses for instruments on the bus, addressed commands (only instruments previously addressed to listen respond to these commands), universal commands (all instruments, whether they have been addressed or not respond to these), secondary addresses for devices interfaced through their primary instrument, and secondary commands. At present, the standard classifies only two interface messages as secondary commands, Parallel Poll Enable (PPE) and Parallel Poll Disable (PPD). (Parallel Poll Enable means that *after* the controller configures the system for a parallel poll (PPC command), all instruments respond at the same time with status information on receipt of PPE.)

Device Dependent Messages

The IEEE standard does not specify coding of device-dependent messages, messages that control the device's internal operating functions. After addressing (via interface messages) a talker and listener(s), the controller unasserts the ATN bus line. When ATN becomes false, any commonly-understood 8-bit binary code may be used to represent a device-dependent message.

The standard recommends that the alphanumeric codes associated with the numbers, symbols, and upper case characters (decimal 32 to decimal 94) in the ASCII Code Chart be used for device-dependent messages. One example of a device-dependent message is the ASCII character string

MODE V; U/D 5E-3; FREQ 1E3

which may tell an instrument to set its front-panel controls to the voltage mode, with 5.0 millivolt output at a frequency of 1000 Hz.

When 8-bit binary codes other than the ISO 7-bit code are used for device-dependent messages, the most significant bit must be on data line DI08 (for bit 8).

To summarize the difference between interface and device-dependent messages, remember that any messages sent or received when the ATN line is asserted (true) is an interface message. Any message (data bytes) sent or received when the ATN line is unasserted (false) is a device-dependent message.

GPIB SIGNAL LINE DEFINITIONS

Figure 3-5 shows the 16 signal lines of the GPIB functionally divided into three component busses: an eight-line data bus, a three-line transfer control (handshake) bus, and a five-line management bus.

The Data Bus

The data bus has eight bidirectional signal lines, DI01 through DI08. Information, in the form of data bytes, is transferred over this bus. A handshake sequence between an enabled talker and the enabled listeners transfers one data byte (eight bits) at a time. Data bytes in an interface or device-dependent message are sent and received in a byte-serial, bit-parallel fashion over the data bus.

ASCII & IEEE 488 (GPIB) CODE CHART

B7 B6 B5 / BITS / B4 B3 B2 B1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	CONTROL		NUMBERS SYMBOLS		UPPER CASE		LOWER CASE	
0 0 0 0	0 NUL 0 0	20 DLE 10 16	40 SP 20 32	60 0 30 48	100 @ 40 64	120 P 50 80	140 ` 60 96	160 p 70 112
0 0 0 1	1 GTL SOH 1 1	21 LLO DC1 11 17	41 ! 21 33	61 1 31 49	101 A 41 65	121 Q 51 81	141 a 61 97	161 q 71 113
0 0 1 0	2 STX 2 2	22 DC2 12 18	42 " 22 34	62 2 32 50	102 B 42 66	122 R 52 82	142 b 62 98	162 r 72 114
0 0 1 1	3 ETX 3 3	23 DC3 13 19	43 # 23 35	63 3 33 51	103 C 43 67	123 S 53 83	143 c 63 99	163 s 73 115
0 1 0 0	4 SDC EOT 4 4	24 DCL DC4 14 20	44 $ 24 36	64 4 34 52	104 D 44 68	124 T 54 84	144 d 64 100	164 t 74 116
0 1 0 1	5 PPC ENQ 5 5	25 PPU NAK 15 21	45 % 25 37	65 5 35 53	105 E 45 69	125 U 55 85	145 e 65 101	165 u 75 117
0 1 1 0	6 ACK 6 6	26 SYN 16 22	46 & 26 38	66 6 36 54	106 F 46 70	126 V 56 86	146 f 66 102	166 v 76 118
0 1 1 1	7 BEL 7 7	27 ETB 17 23	47 ' 27 39	67 7 37 55	107 G 47 71	127 W 57 87	147 g 67 103	167 w 77 119
1 0 0 0	10 GET BS 8 8	30 SPE CAN 18 24	50 (28 40	70 8 38 56	110 H 48 72	130 X 58 88	150 h 68 104	170 x 78 120
1 0 0 1	11 TCT HT 9 9	31 SPD EM 19 25	51) 29 41	71 9 39 57	111 I 49 73	131 Y 59 89	151 i 69 105	171 y 79 121
1 0 1 0	12 LF A 10	32 SUB 1A 26	52 * 2A 42	72 : 3A 58	112 J 4A 74	132 Z 5A 90	152 j 6A 106	172 z 7A 122
1 0 1 1	13 VT B 11	33 ESC 1B 27	53 + 2B 43	73 ; 3B 59	113 K 4B 75	133 [5B 91	153 k 6B 107	173 { 7B 123
1 1 0 0	14 FF C 12	34 FS 1C 28	54 , 2C 44	74 < 3C 60	114 L 4C 76	134 \ 5C 92	154 l 6C 108	174 ¦ 7C 124
1 1 0 1	15 CR D 13	35 GS 1D 29	55 − 2D 45	75 = 3D 61	115 M 4D 77	135] 5D 93	155 m 6D 109	175 } 7D 125
1 1 1 0	16 SO E 14	36 RS 1E 30	56 . 2E 46	76 > 3E 62	116 N 4E 78	136 ^ 5E 94	156 n 6E 110	176 ~ 7E 126
1 1 1 1	17 SI F 15	37 US 1F 31	57 / 2F 47	77 UNL ? 3F 63	117 O 4F 79	137 UNT _ 5F 95	157 o 6F 111	177 RUBOUT (DEL) 7F 127
	ADDRESSED COMMANDS	UNIVERSAL COMMANDS	LISTEN ADDRESSES		TALK ADDRESSES		SECONDARY ADDRESSES OR COMMANDS	

KEY

octal: 25 PPU — GPIB code
NAK — ASCII character
hex: 15 21 — decimal

2690-10

Fig. 3-6. ASCII & IEEE 488 (GPIB) Code Chart.

Since the GPIB handshake sequence is an asynchronous operation, the data transfer rate is only as fast as the slowest instrument involved in a data byte transfer at any one time. A talker cannot place data bytes on the bus faster than any one listener can accept them.

Figure 3-7 illustrates the flow of data bytes when a typical controller sends ASCII data to an assigned listener on the bus. The first data byte, decimal 44, enables device 12 as a primary listener and the secondary address, decimal 108, enables a plug-in device as the final destination of the data to follow. The data is the two ASCII characters, A and B (decimal 65 and decimal 66).

The decimal value for B is specified as negative to activate the EOI line and signify the end of the device-dependent message. The controller activates the ATN line again and sends the universal unlisten (UNL) and untalk (UNT) commands to clear the bus. Six handshake cycles on the Transfer Bus are required to send the six data bytes.

The Transfer Bus (Handshake)

Each time a data byte is sent over the data bus, an enabled talker and all enabled listeners execute a handshake sequence via the **transfer bus**. The transfer-bus signal lines are defined below. Figure 3-8 illustrates the basic timing relationship between the three signals. The ATN line is shown to illustrate the controller's role in the process. A flowchart for the handshake sequence is shown in Fig. 3-9.

Not Ready For Data (NRFD). An asserted NRFD signal line indicates one or more assigned listeners are not ready to receive the next data byte from the talker. When all of the assigned listeners for a particular data byte transfer have released NRFD, the NRFD line becomes unasserted (high). The RFD message (Ready For Data) tells the talker it may place the next data byte on the data bus.

Data Valid (DAV). The DAV signal line is asserted (low) by the talker after the talker places a data byte on the data bus. When asserted, DAV tells each assigned listener that a new data byte is on the data bus. The talker is inhibited from asserting DAV as long as any listener holds the NRFD signal line asserted.

Not Data Accepted (NDAC). Each assigned listener holds the NDAC signal line low-true (asserted) until the listener accepts the data byte currently on the data bus. When all assigned listeners accept the current data byte, the NDAC line becomes unasserted, telling the talker to remove the data byte from the bus. The DAC message (Data Accepted) tells the talker that all assigned listeners accepted the current data byte.

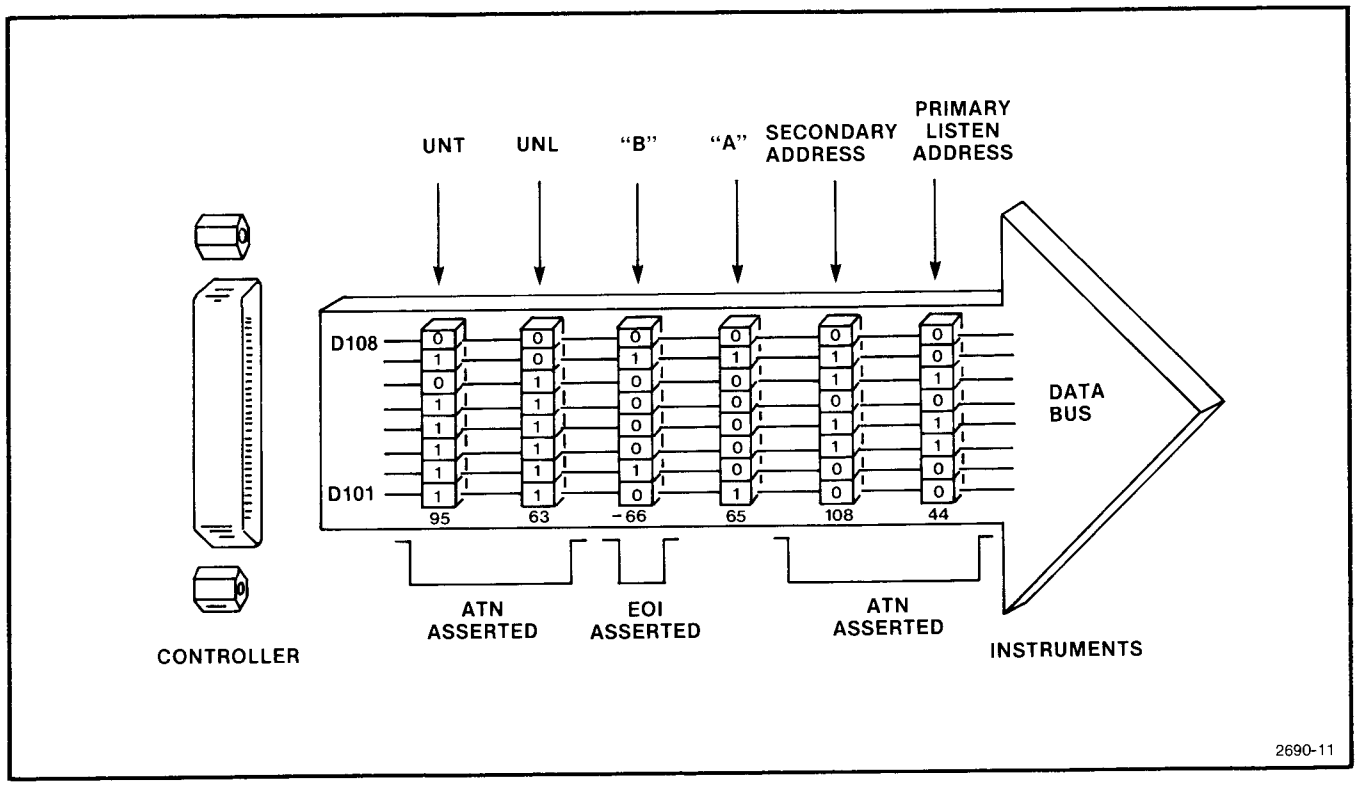


Fig. 3-7. An example of data byte traffic on the GPIB.

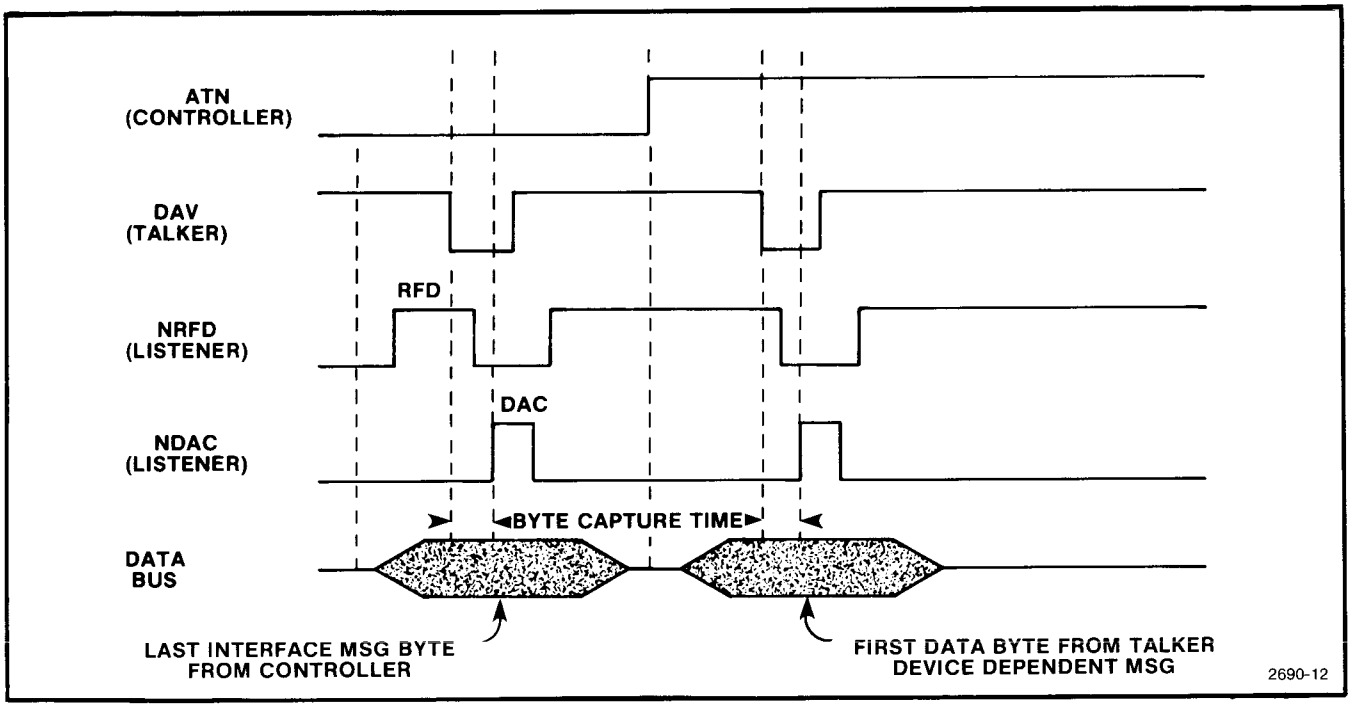


Fig. 3-8. A typical handshake timing sequence (idealized). Byte capture time is dependent on the slowest instrument involved in the handshake.

When one handshake cycle transfers one data byte, the listeners reset the NRFD line high and the NDAC line low before the talker asserts DAV for the next data byte transfer. NDAC and NRFD both high at the same time is an invalid state on the bus.

The Management Bus

The management bus is a group of five signal lines which are used to control the operation of the GPIB: IFC, ATN, SRQ, REN, and EOI.

Interface Clear (IFC). The system controller asserts the IFC signal line to place all interface circuitry in a predetermined quiescent state which may or may not be the power-on state.

Only the system controller can generate this signal. The IEEE standard specifies that only three interface messages (universal commands) be recognized while IFC is asserted: Device Clear (DCL), Local Lockout (LLO), and Parallel Poll Unconfigure (PPU).

Attention (ATN). A controller asserts the ATN signal line when instruments connected to the bus are being enabled as talkers or listeners and for other interface control traffic. As long as the ATN signal line is asserted (ATN = 1), only instrument address codes and control messages are transferred over the data bus. With the ATN signal line unasserted, only those instruments enabled as a talker and listener(s) can transfer data. Only the controller can generate the ATN signal.

Service Request (SRQ). Any instrument connected to the bus can request the controller's attention by asserting the SRQ line. The controller responds by asserting ATN and executing a serial poll to determine which instrument is requesting service. (An instrument requesting service identifies itself by asserting its DI07 line after being addressed.) After the instrument requesting service is found, program control is transferred to a service routine for that instrument. When the service routine is completed, program control returns to the main program. When polled, the instrument requesting service unasserts the SRQ line.

Remote Enable (REN). The system controller asserts the REN signal line whenever the interface system operates under remote program control. Used with other control messages, the REN signal causes an instrument on the bus to select between two alternate sources of programming data. A remote-local interface function indicates to an instrument that the instrument will use either information input from the front-panel controls (Local) or corresponding information input from the interface (Remote).

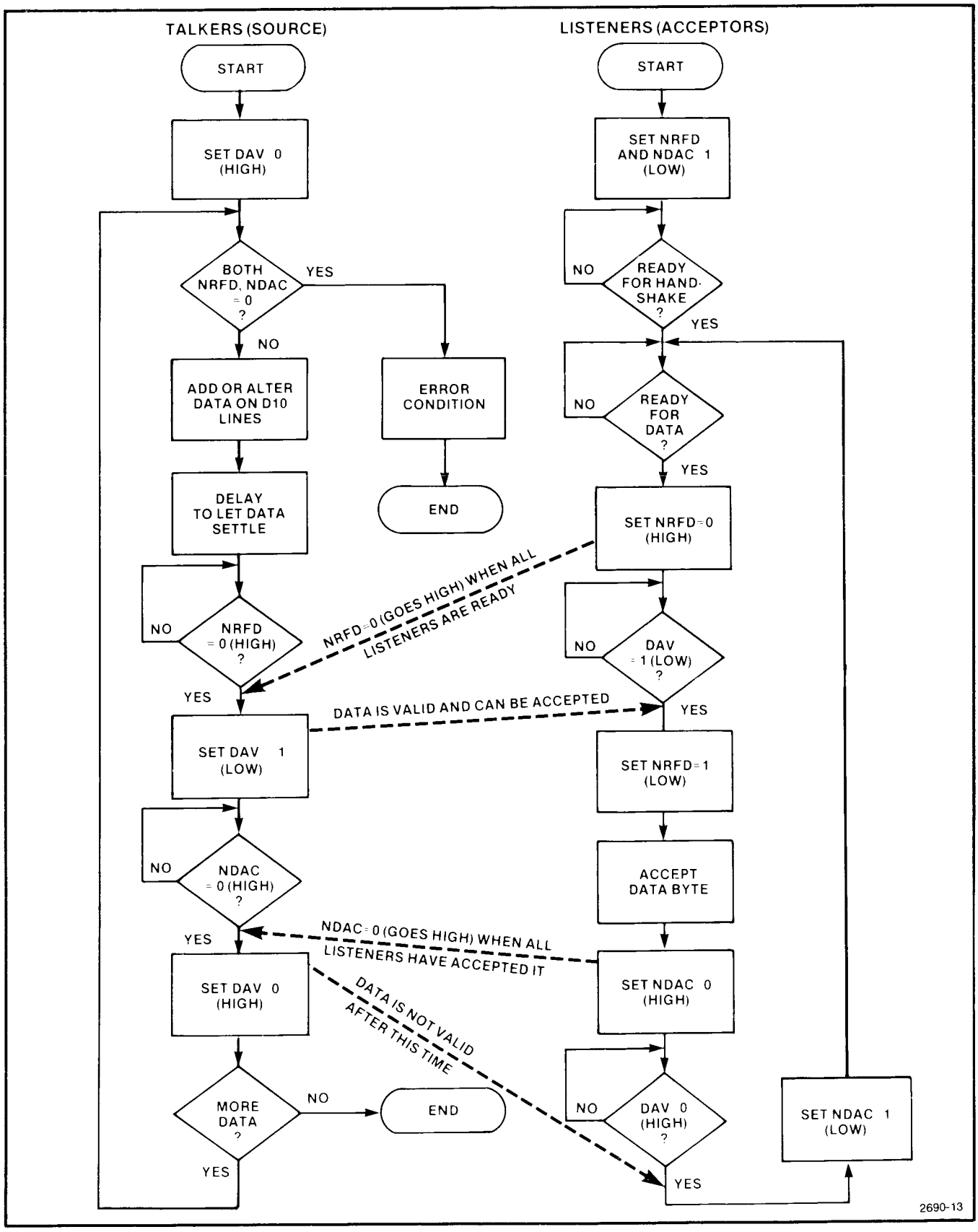


Fig. 3-9. The handshake flow chart.

End or Identify (EOI). A talker can use the EOI to indicate the end of a data-transfer sequence. The talker asserts the EOI signal line as the last byte of data is transmitted In this case, EOI is essentially a ninth data line and must observe the same setup times as the DI0 lines. When the controller is listening, it assumes that a data byte received is the last byte in the transmission (if the EOI signal line has been asserted). When the controller is talking, it may assert the EOI signal line as the last byte is transferred. The EOI signal is also asserted with the ATN signal if the controller conducts a parallel polling sequence. EOI is not used during serial polling.

NOTE

For detailed information on GPIB specifications, refer to IEEE 488-1975 (Revised 1978), published by the Institute of Electrical and Electronics Engineers, 245 East 47th Street, New York, New York 11117.

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO. REFER TO OPERATORS SAFETY SUMMARY AND SERVICE SAFETY SUMMARY PRIOR TO PERFORMING ANY SERVICE.

THEORY OF OPERATION

GENERAL INFORMATION

Introduction

This section is composed of three parts. The first part, General Information, presents a brief overview of the TEKTRONIX CG 5001/CG 551AP as a system. Also included is information concerning the arrangement of the block and schematic diagrams and some general notes on the electronic circuitry. The second part, CG 5001/CG 551AP System Description, discusses the CG 5001/CG 551AP in block diagram form, while the third part, Detailed Circuit Description, presents more detailed information about the electronic circuitry within the functional blocks.

Block Diagrams

Block diagrams for the CG 5001/CG 551AP are located in the foldout pages in Volume 2 of this manual. Block diagrams A through D portray the CG 5001/CG 551AP as a system. Each functional block on the four diagrams is assigned a circuit board assembly number and the schematic number(s). Each function on the block diagrams has the same functional name on its associated schematic diagram.

The connectors for the A2 assembly (Main Interconnect—schematic diagram 3) and the A3 assembly (Time Interface—schematic diagrams 4 and 5) are not shown on the block diagram. Keep in mind, while tracing through any two functional blocks that do not have the same assembly number, that signal flow may go through the connectors for A2 or A3, or both. For example, signals to (from) subassemblies A3A1 through A3A8 on the Time Interface board must go through the main connectors for A3 and A2 if they go to (originate at) the microprocessor on assembly A9 (CPU). Refer to Fig. 4-1 for a simplified overview of the CG 5001/CG 551AP system.

In general, the CG 5001/CG 551AP has three sections: amplitude, timing, and central processing. The amplitude section generates the required voltage and current waveforms for calibrating the vertical amplifier of an oscilloscope. The timing section generates two different types of timing signals (time marks and slewed edges) for calibrating the horizontal sweep rates. The central processing section controls all of the output signals. The central processing section receives its operating instructions via the front panel keyboard or via programmed instructions sent over the GPIB.

Schematic Diagrams

The schematic diagrams are arranged in a numerical sequence consistent with the sequence of the alphanumeric circuit board assembly numbers, A1 (Front Panel) through A9A1 (GPIB). Most circuit board assemblies have more than one associated schematic diagram.

The following are general comments about the CG 5001/CG 551AP circuitry:

1. The circuit descriptions use positive logic, except for the logic specified for the IEEE 488 bus (GPIB) which uses negative logic, where a high voltage level = 0 and a low voltage level = 1.

2. The digital logic circuits use ECL, TTL, CMOS, and NMOS devices. A TTL high is $\geq$2.4 V and a TTL low is $\leq$0.8 V. The high and low levels for NMOS devices operating from a +5 V source are approximately the same as for TTL devices. CMOS devices operate between approximately 5 V and ground. The high and low levels for ECL devices are approximately +4.1 V and +3.3 V, respectively. A bar over a signal name means that the signal line is asserted low true.

3. Logic devices are drawn according to the functions they perform in the circuit and may appear different from that shown on the manufacturer's data sheet. Some ECL devices have both inverted and noninverted outputs.

4. Inputs to ECL devices have internal pulldown resistors. Unused inputs are not tied to external voltages unless noted.

5. The outputs of some devices may be tied together to perform the wired-OR function.

6. The operation of linear integrated circuits in this instrument are described individually, using operating waveforms, specific voltage levels, or other techniques.

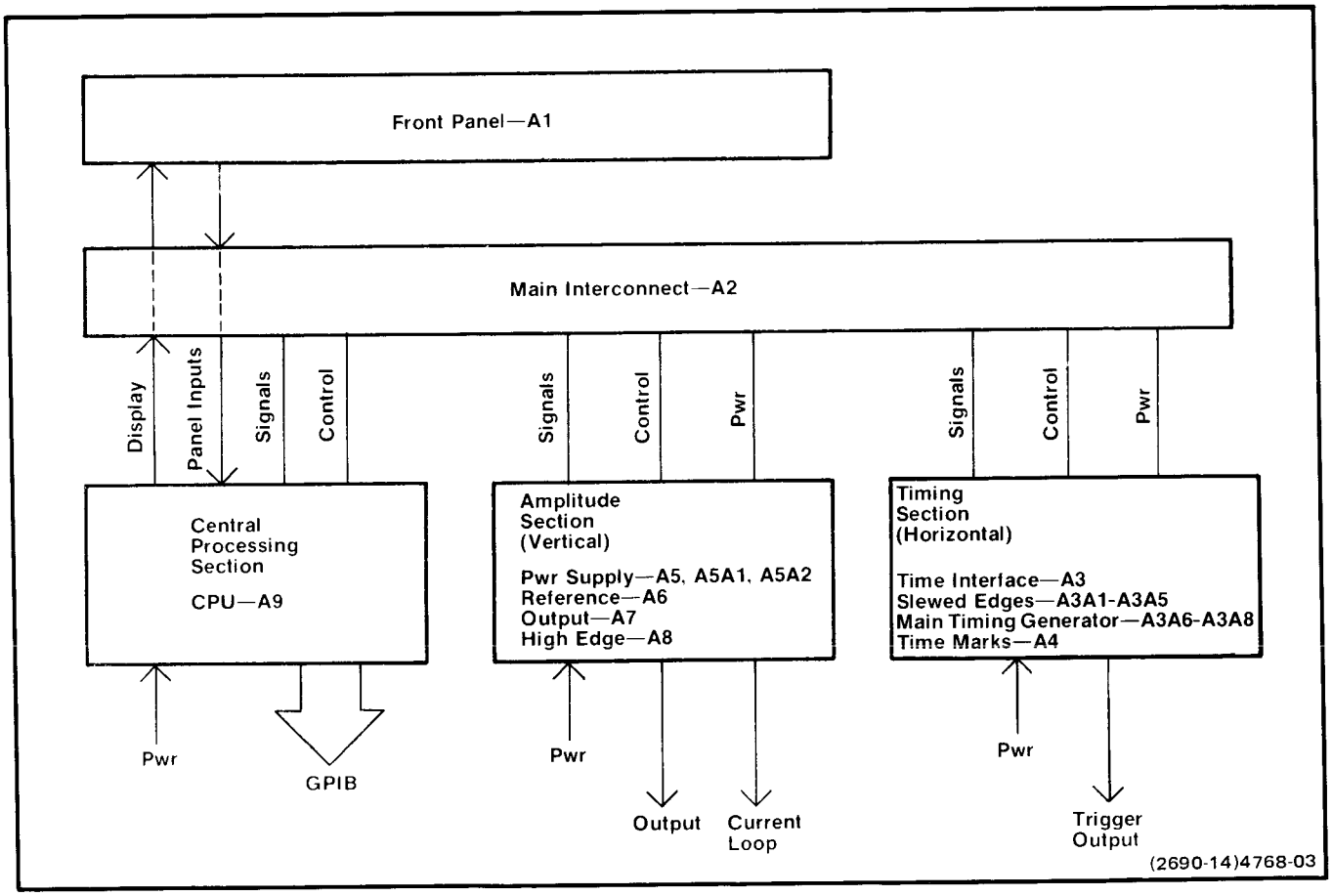


Fig. 4-1. CG 5001/CG 551AP system overview.

CG 5001/CG 551AP SYSTEM DESCRIPTION

CENTRAL PROCESSING (BLOCK DIAGRAM A)

Introduction

The central processing section of the CG 5001/CG 551AP controls the internal operation of the entire instrument and can be thought of as a single block, as portrayed in Block Diagram A.

The architecture for the total system is designed around the capabilities of a microprocessor located on the CPU circuit board (A9). The microprocessor has a 16-bit address bus, an 8-bit bidirectional data bus, and fully decoded control outputs. Combining the microprocessor with memory and input-output circuits completes the central processing module.

For specific details concerning the internal operation of the microprocessor refer to "M6800 Microcomputer System Design Data", published by Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036 or to "An Introduction to Microcomputers", Vol. 1, published by Adam Osborne and Associates, Inc., P.O. Box 2036, Berkeley, CA 94702.

Microprocessor and System Clock

The microprocessor controls the functions performed by the other components in the system. The microprocessor fetches instructions from memory, decodes the desired operation and executes the instructions. In addition, it recognizes and responds to certain external control signals, such as IRQ and NMI (interrupt requests). The IRQ interrupt may be internally masked (not recognized) whenever the microprocessor desires, but the non-maskable interrupt, NMI, always causes the microprocessor to respond immediately.

The clock for setting microprocessor timing is generated on chip with an outboard 4 MHz crystal. The microprocessor E line is used for setting the timing of all data transfers. The E line toggles at a 1 MHz rate.

Memory (ROM and RAM)

The read only memory contains preprogrammed firmware instructions to operate the system. The ROM contains 16,384 address locations where instructional data bytes may be stored. These data bytes (8 bits each) tell the microprocessor what operation must be performed.

Temporary memory storage requirements are provided by the random access memory block (RAM). When necessary, the microprocessor can store and retrieve data in the RAM. The RAM is battery backed-up so that the contents can be retained while the main power is off. Half of the RAM is write-protected to ensure that the calibration factors retained in that area cannot be altered except when the instrument is in the calibration (CAL) mode. The address configuration for the CG 5001/CG 551AP is shown in Fig. 4-2.

Power On-Off Detect

The power on-off detect circuitry performs two functions. The first is to ensure that the RAM cannot be written into while the microprocessor is uncontrolled because of improper power supplies. The second task is to generate the reset pulse required to initialize the system on power up.

Peripheral Interface Adapters (PIA)

Two peripheral interface adapters are used to meet the communication requirements for the front panel controls and for programming the amplitude and timing circuits of the CG 5001/CG 551AP.

Each PIA has two 8-bit data ports and four control lines. The data port lines are programmed by the microprocessor to serve either as an input or output.

The Program Bus and Data Registers

When a front panel control or pushbutton is changed or when a command is received via the GPIB to change the front panel settings, the microprocessor responds by sending serial data from memory to control data registers in the amplitude and timing sections of the CG 5001/CG 551AP.

The program bus and data register configuration is shown in Fig. 4-3. The data registers are composed of cascaded eight-stage serial shift registers having a storage latch associated with each stage. Serial data is shifted through the registers on positive transitions of a data clock signal. The serial data in each shift register is transferred (latched) to parallel output stages by the high level strobe signals (TS1, TS2, VS1, or VS2). The latched data in each register determines the output waveforms, voltage or current levels, and type of timing signals from the CG 5001/CG 551AP.

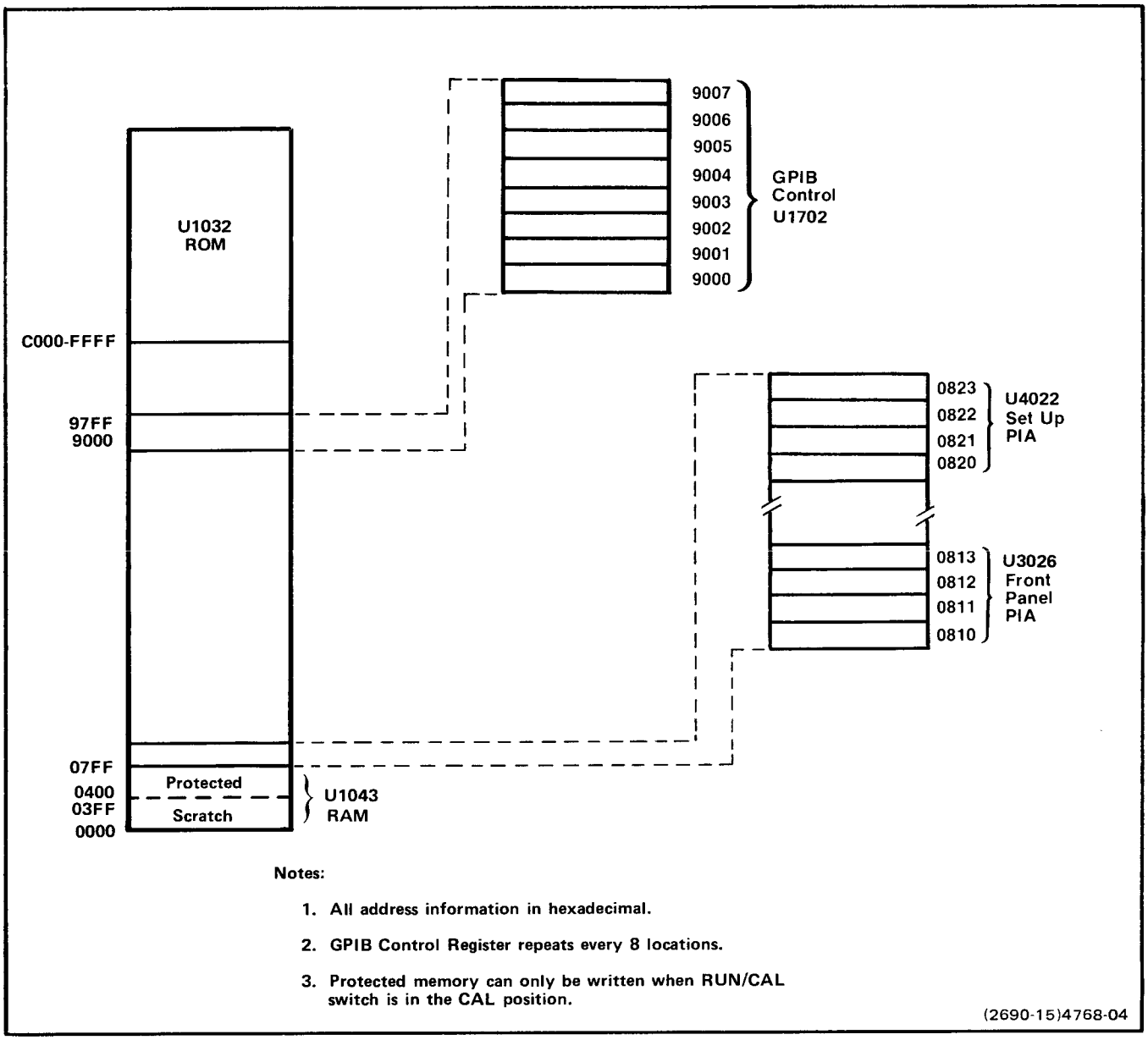


Fig. 4-2. CG 5001/CG 551AP address configuration.

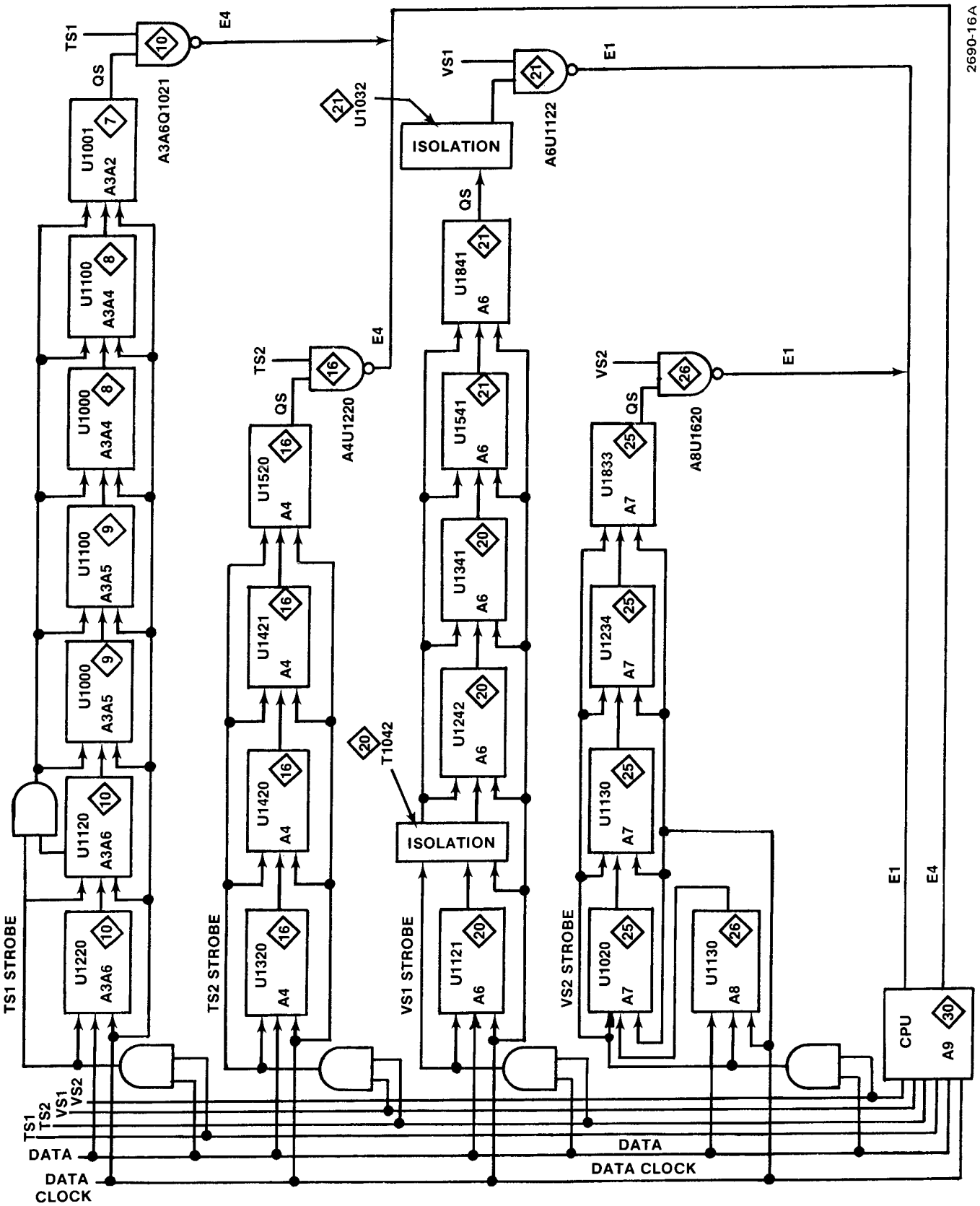


Fig. 4-3. CG 5001/CG 551AP program bus and data registers.

The Status Bus

An internal status bus is used by the microprocessor to retrieve status information from various circuit board modules in the system. The information is identified by status lines E1, E2, E3, and E4. The status is reported to the microprocessor via the Error Gating circuits shown on Block Diagrams B, C, and D.

The circuit boards and their associated status codes are shown in Table 4-1. The information is related to instrument errors, operating errors, or data retrieved during a self-check routine by the microprocessor. Refer to the Programming section of this manual for more error codes related to operating the system.

Front Panel Circuit

The Keyswitch decoder circuit on the Front Panel circuit board is a row-column array whose output is buffered by the Switch Buffer circuit (on the Main Interconnect board). The buffered Keyswitch output information is periodically read by the microprocessor to identify the pushbutton that was pressed by the operator. A software routine is then executed to debounce the keyswitches, change the output settings, and update the front panel display via the Display Multiplexer circuits. The microprocessor also changes the output settings and the display when it receives a programming command via the GPIB.

The Display Multiplexer is a two port memory that is loaded, by the microprocessor, with segment information causing the appropriate LED characters (Displays) and pushbutton lights to be illuminated. The Display Multiplexer circuit is under the control of the freerunning Front Panel Clock, operating at a 2.5 kHz rate.

The front panel status information is continually updated and stored in the RAM. When the CG 5001/CG 551AP is powered up, the microprocessor recovers this data and sets the front panel outputs and display to specific default settings, dependent on the position of an internal switch. Refer to Maintenance Section for details concerning internal switches.

The Optical Switch contains two Gray encoded discs. When rotated, the slotted discs interrupt a light source that strikes on four internal photocells. The output of these photocells provides positional information to the microprocessor via four lines, two for the VARIABLE control and two for the UNITS/DIV control. The microprocessor interprets the light source interruptions and determines which control has been turned and in which direction (cw or ccw). The microprocessor then increments or decrements an internal firmware counter, programs the amplitude or timing section for the appropriate output, and then updates the display.

The Head Sense circuit utilizes three comparators and a current source to detect a particular voltage level on the control pin associated with the main OUTPUT connector. The circuit can detect and inform the microprocessor of any one of the following four conditions:

(1) Programmable Pulse Head accessory attached, (2) Comparator Head accessory attached, (3) no accessory head attached, and (4) reserved-spare.

The Remote Variable accessory, when attached and used, interrupts the microprocessor with input information. The microprocessor performs the required task and then returns data to the accessory to illuminate the appropriate indicator light(s).

Table 4-1
INTERNAL STATUS CODES

Circuit Board	E1	E2	E3	E4
Time Interface (A3) TS1 (time strobe 1)	ROL — Reference Loop Out of Lock	MOL — Main Loop Out of Lock	OOL — Offset Loop Out of Lock or Counter Test	Data Return
Time Mark (A4) TS2 (time strobe 2)	External Reference	(Spare)	Counter Test Signal Gates	Data Return
Reference (A6) VS1 (voltage strobe 1)	Data Return	Uncal	(Not Used)	(Not Used)
High Edge (A8) VS2 (voltage strobe 2)	Data Return	Power On Test	Head Error	Edge Error

NOTE

Refer to the desired accessory instruction manual for Operating Instructions and Theory of Operation related to the Comparator, Pulse Head, or Remote Variable.

GPIB Circuits

The ROM contains firmware which allows the microprocessor to communicate through the GPIB interface adapter (GPIA) on the IEEE 488-1975 standard instrumentation bus. The GPIA contains circuitry to handle handshaking of data, address recognition, and serial poll.

The Address Switches are set by the user prior to attaching the CG 5001/CG 551AP to the GPIB. When the Address Switch circuit is enabled by an address select line from the GPIA, the microprocessor reads and stores the CG 5001/CG 551AP address code for future use.

Two GPIB Buffers are required to buffer the 16 bus lines between the GPIA and the IEEE-488 bus. Each buffer channel provides a non-inverting receiver and driver plus the required terminations. Data direction is controlled by the GPIA.

CPU Power Supply

The power supply circuits on the CPU board (A9) convert the ±26 V nominal source from the power module to ±12 V and convert the +8 V nominal source from the power module to +5 V and +2.5 V.

The +2.5 V level is used as a sensing level for the Power On-Off Detect circuits and as a reference for the +5 V supply. The ±12 V supply is used only for the comparator circuit in the Head Sense circuit. The +5 V supply furnishes power for devices on the CPU (A9), Main Interconnect (A2), and Front Panel (A1) circuit board assemblies.

MAIN TIMING GENERATOR (BLOCK DIAGRAM B)

Introduction

The Main Timing Generator generates the timing signals required for all modes of operation. The basic structure of the Main Timing Generator consists of three feedback loops: Reference Loop, Steering Loop, and Sampling Loop.

The Main Timing Generator, under microprocessor control, generates a timing reference signal at 100 MHz (±9.9%) in 100 kHz (0.1%) steps. The timing reference signal is phase locked to internal 1 MHz Reference Oscillator, which, in turn, can be phase locked to a temperature compensated crystal oscillator (Optional TCXO), or to an external reference.

The 100 MHz timing reference signal is used only in the MARKERS and SLEWED EDGE modes. In the AMPLITUDE modes, the 1 MHz Reference Oscillator signal is used to generate the chopping signals for voltage and current waveforms.

Automatic Reference Select

If an external reference is applied through the power module interface, the Automatic Reference Select circuit automatically disables the output of the Optional TCXO and turns on the External Reference Indicator and applies the external reference signal to the External Reference Phase-lock circuit. The microprocessor recognizes this status via the TS2 Error Gates and turns on the EXT REF indicator on the front panel.

Reference Loop

The 1 MHz Reference Oscillator is phase locked to the external reference or to the Optional TCXO by the External Reference Phase Lock circuit. Phase lock occurs on integral multiples of 1 MHz, up to a maximum of five. If the internal 1 MHz Reference Oscillator does not lock to the external reference or the Optional TCXO, the Reference Loop Out of Lock Indicator is illuminated and the status is reported to the microprocessor via the TS1 Error Gates.

The output from the 1 MHz Buffer is applied to the Reference Divider. The Reference Divider divides by 10 and 100 to produce two output signals: a 100 kHz signal that gates out every tenth pulse of the 1 MHz Reference Oscillator to strobe the Sampling Phase Gate, and a 10 kHz signal used as a reference signal for the Coarse Steering Circuit associated with the Steering Loop for the Main VCO.

During the self test sequence at power on, the microprocessor checks the output of the Reference Divider and the Count Down circuit (block diagram C) by counting a burst of 10 kHz pulses from the Reference Divider. Three burst gates (1 sec, .2 sec, and .5 sec) for the counter test are derived from the Count Down circuit via the TS2 Error Gates (block diagram C).

Steering and Sampling Loops

The Main VCO operates at a nominal center frequency of 100 MHz and changes its output frequency in 100 kHz steps as the VARIABLE control is turned. The purpose of the Steering Loop is to set the Main VCO to the correct

harmonic of 100 kHz. Once the Main VCO is on the correct harmonic, the Steering Loop disconnects itself and the Sampling Loop takes over to keep the Main VCO on that correct harmonic. 100 MHz corresponds to 0.0% timing error for the device under test. The Main VCO output frequency is determined by the data stored in the Data Registers. The stored number is dependent on the VARIABLE control.

The Sampling Loop has very low noise, but it cannot differentiate between different harmonics. The Steering Loop operates only to get the Sampling Loop to the correct harmonic of 100 kHz.

When the Main VCO is at 100 MHz and 0.0% error, the Prescaler output is 10 MHz. The number stored in the Data Registers causes the Programmable Divider to divide by 1000. Both input frequencies to the Coarse Steering Circuit are then 10 kHz (and in phase) with the Steering Loop disconnected from the Loop Filter circuit.

If the Programmable Divider output is not 10 kHz, the Coarse Steering Circuit produces steering pulses. The Loop Filter circuit translates the steering pulses to a dc level required to tune the Main VCO to the correct harmonic of 100 kHz.

A 100 kHz Strobe Holdoff signal from the Reference Divider is used in the Sampling Phase Gate circuit to gate out every tenth pulse from the 1 MHz Reference Oscillator. Since the strobing rate is 100 kHz, the Main VCO can lock to multiples of that rate, up to ±9.9% of the center frequency. The output of the Sampling Phase Gate is a dc level. The dc level is proportional to the phase difference between the strobe signal and the Main VCO signal. The dc level is amplified by the Loop Filter and used to lock the Main VCO to the correct harmonic (100 kHz step).

For a locked on condition, the output of the Programmable Divider is always 10 kHz and in phase with the 10 kHz signal from the Reference Divider. If the Steering Loop remains out of lock, the Main Loop Out of Lock Indicator is illuminated and strobing of the Sampling Phase Gate is inhibited. This status is reported to the microprocessor via the TS1 Error Gates.

When a timing error other than 0.0% is programmed, the microprocessor enters new data into the Data Registers. The range of the Programmable Divider is from 901 to 1099 with 1000 corresponding to 0.0% error. A +3.0% FAST timing error changes the output of the Programmable Divider to 9.708 kHz (÷N = 1030), creating a frequency difference with respect to the 10 kHz reference. The Coarse Steering Circuit and the Loop Filter operate to shift the Main VCO toward a new frequency (103 MHz) and the Sampling Phase Gate tunes and holds it to exactly 103 MHz. The output of the Prescaler has changed to 10.3 MHz and the output of the Programmable Divider is, again, 10 kHz for a stable, phase locked condition.

The Coarse Steering Circuit is continuously operating and monitoring whether there is any phase or frequency change. If that happens, a phase error signal is activated to tune the Main VCO to a new frequency, or to correct the error.

Main VCO Divider and 100 MHz Buffer

The Main VCO Divider divides the Main VCO output by two. The output signals are used as a reference source for the Offset Loop and Trigger Counter circuits associated with the SLEWED EDGE mode (Block Diagram C). The Main VCO output (± percent error) is buffered by the 100 MHz Buffer for application to the Time Mark Generator circuits (Block Diagram C).

Main Loop and Slewing Power Switches

Two data bits in the Data Register control the power switching to various circuit board assemblies. When operating in the VOLTAGE, CURRENT, EDGE, or FAST EDGE modes only the chopping signal circuits in the timing section are required. Therefore, power for part of the A3A6 and A3A7 assemblies is disabled through the Main Loop Power Switch, while power for the A3A1 through A3A5 assemblies is disabled through the Slewing Power Switch. When operating in the MARKERS mode, the slewed edge circuits are disabled, except for the final Marker Amplifier and Trigger Amplifier circuits, which are common to both modes. See Block Diagram C.

12 V Regulators

The 12 V regulator is a dual (positive and negative) regulator IC with external series-pass elements. The regulators furnish 12 Vdc power to the circuit board assemblies as shown on the block diagram.

SLEWED EDGE GENERATOR (BLOCK DIAGRAM C)

Introduction to Slewed Edges

When the CG 5001/CG 551AP operates in the SLEWED EDGE mode, incrementally delayed successive pulses appear to be slewed, or delayed, horizontally across the oscilloscope crt graticule. See Fig. 4-4c.

This new type of timing signal replaces the procedure of attempting to force a 1 GHz sine-wave signal through the

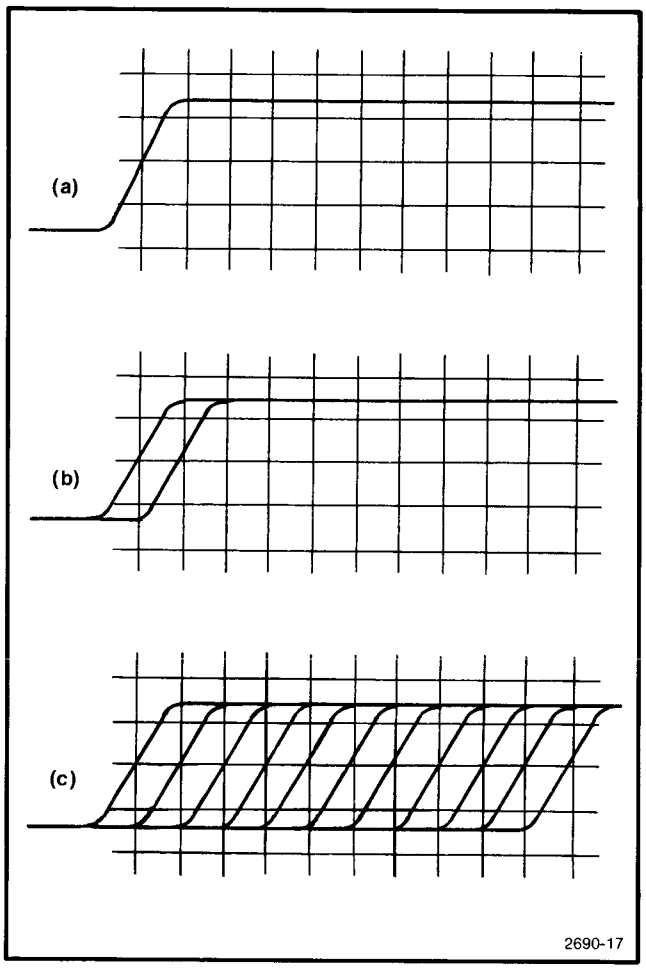


Fig. 4-4. Incrementally delayed pulses.

200 MHz vertical amplifier of an oscilloscope to check sweep rates at 1 ns/div, or faster.

A trigger signal is applied to the oscilloscope to start the sweep running. When the sweep reaches the first graticule line, the leading edge of a slewed pulse occurs, causing the crt display to appear as shown in Fig. 4-4a. As soon as the sweep ends and the sweep circuit is reset, another trigger signal starts the second sweep. The second slewed pulse occurs and the display appears as shown in Fig. 4-4b. This process of generating one trigger pulse and one delayed pulse is repeated until eleven or more edges have been generated. The entire process is then repeated, starting again with the first division. The process is repeated very rapidly to maintain adequate intensity, without flicker, and the crt display has the appearance as shown in Fig. 4-4c.

The spacing between the edges is variable so that the slewed edges can be aligned with the graticule lines. The deviation from the standard (percent error) is read out digitally.

How Are Slewed Edges Generated?

Refer to Fig. 4-5. The generation of slewed edges requires two oscillators, A and B. Oscillator B is running at a slightly lower frequency than oscillator A. The minimum spacing between the edges depends on the ratio, f_B/f_A. To obtain calibrated slewing, f_B must have a certain relationship to f_A. If the two oscillators are arranged so that

$$\frac{f_B}{f_A} = \frac{40}{41}$$

and f_A = 50 MHz (corresponding to a period of 20 ns), the f_B pulse will be incrementally delayed from f_A by a time interval equal to 0.5 ns. Oscillator B, operating at approximately 48.78 MHz corresponds to a period of 20.5 ns. There is a time coincidence point between every 41st pulse from oscillator A and every 40th pulse from oscillator B.

Both signals are divided down by the Trigger and Slewing Counters so that their repetition rates will be slower than the maximum sweep rate of the oscilloscope. This prevents skipping a trace and ending up with a hole in the crt display. It also provides a means for spacing the slewed edges by any multiple of 0.5 ns.

An edge counter counts the desired number of slewed edges during the slewing cycle. At the end of the desired count, a control circuit is reset so that the next slewing cycle can start at the time coincidence point.

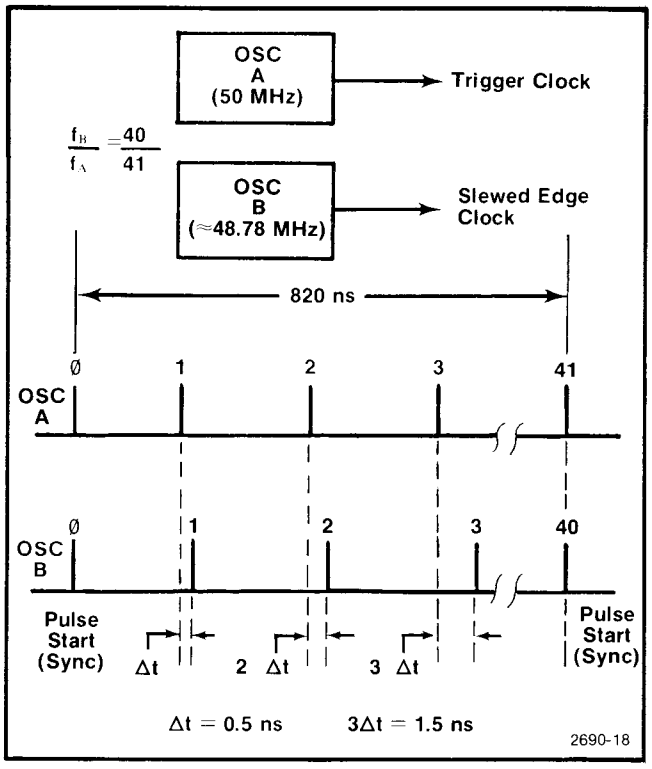


Fig. 4-5. Generating slewed edges.

Oscillator A is referred to as the trigger clock and oscillator B the slewing clock. Since the basic increment, for this example, is 0.5 ns, it is possible to select any pair of pulses (trigger and slewing) to obtain multiples of 0.5 ns/div. The microprocessor calculates the data necessary to select the correct pair of pulses so that the maximum repetition rate of the oscilloscope sweep generator is not exceeded.

Offset Loop (Block Diagram C)

The slewing clock pulses are derived from the Offset VCO, while the trigger clock pulses are derived from the Main VCO Divider. When operating in the SLEWED EDGE mode and the VARIABLE control is set for 0.0%, the output of the Main VCO Divider is 50 MHz (20 ns period).

The Mixer circuit operates to output the difference between the Main VCO Divider output frequency (f_A) and the Offset VCO output frequency (f_B) to get $f_A - f_B$. The Offset Divider divides the output of the Offset VCO by 40 or 50, depending on the offset desired.

The Mixer output and Offset Divider output are frequency- and phase-compared in the Offset Loop Phase Detector, where an error signal output drives the loop to make the two frequencies equal:

$$f_A - f_B = \frac{f_B}{40}$$

Solving for f_B gives the desired relationship:

$$f_B = \frac{40}{41} f_A .$$

Expressed in terms of oscillator period instead of frequency,

$$t_B = \frac{41}{40} t_A .$$

If period t_A = 20 ns, then:

$$t_B = \frac{41}{40} \text{ X } 20 \text{ ns} = 20.5 \text{ ns},$$

providing the required 0.5 ns period difference.

For a period difference (basic offset) of 0.4 ns (.4 ns/div scale), the Offset Divider is switched to divide by 50. The relationship then becomes

$$t_B = \frac{51}{50} t_A$$

and for t_A = 20 ns,

$$t_B = \frac{51}{50} \text{ X } 20 \text{ ns} = 20.4 \text{ ns}$$

The Offset Loop Out of Lock Indicator is illuminated when the Offset Loop is out of lock. The microprocessor senses this status through the TS1 Error Gates. If the Offset Loop is far from lock, the Acquisition Circuit operates to start a search cycle to tune the Offset VCO so that the difference frequency from the Mixer filter circuit can start clocking the Offset Loop Phase Detector. The error signal from the Offset Loop Phase Detector then becomes the only source controlling the tuning voltage for the Offset VCO.

Slewing Control, Counters, and Generators

These circuits generate the trigger and output signals for the slewed edge display on a crt screen.

The Trigger and Slewing Counters count down their respective clock signals to obtain the desired incremental delay between trigger and signal outputs. This allows enough time between successive triggers for the oscilloscope sweep to recover. The time between successive triggers will always exceed 3.5 μs.

The microprocessor calculates two numbers for each counter. The first, called "shift count", determines an initial trigger-to-first edge delay. This delay allows the operator (by using the SHIFT commands) to horizontally position the beginning of the slewed edge pattern to any point on the crt. The second, called "slewing count", determines the spacing between edges in the pattern, according to the selected time scale (units per division).

The shift and slewing counts for the Trigger Counter are loaded into separate registers in the Trigger Data Register. The counts for the Slewing Counter are loaded into the Slewing Data Register. These registers program the count of their respective counters.

The Slewing Control circuit activates the registers holding the shift counts for generation of the first edge in each pattern. The Slewing Control then switches to the registers holding the slewing counts for the remaining edges in the pattern.

The Slewing Control circuit also contains an edge counter that determines the number of edges per pattern. The number of edges in a pattern is normally fifteen, but can be programmed for 1 to 15 edges, via the GPIB only.

The Trigger Generator and the Slewed Edge Generator circuits convert the pulses from their respective counters to rectangular waveforms. The positive going edges of these waveforms constitute the trigger and slewed edge output signals.

TIME MARK AND TRIGGER GENERATORS (BLOCK DIAGRAM C)

Introduction

When the MARKERS mode is programmed, the Time Mark Generator section produces triangular shaped time marks in the 10 ns to 5 sec range. For this discussion fast markers are defined as 10, 20, 50, 100, 200, and 500 ns markers, while slow markers are defined as all markers equal to 1 μs or slower. Each marker step follows a normal 1, 2, 5 sequence.

The width of the slow time marks at the baseline is about four percent of the period. Thus, normal 100 ms markers will be about 4 ms wide at the baseline. The width of the fast markers is constant (about 5 ns).

Output trigger pulses for the normal (NORM) trigger mode are at the same rate as the selected marker rate, except when operating in the 10 ns to 100 ns range, where the trigger rate remains at 100 ns (10 MHz).

Chopping signals for the VOLTAGE, EDGE, and CURRENT modes also come from the Time Mark section.

Marker Data Register

The microprocessor sends serial data to the Marker Data Register which selects and sets up the Time Mark Generator, Trigger Generator, and Chopping circuits for the required operation. The registers are loaded with 32 bits of serial data (four 8-bit bytes) to select the proper circuits for the timing mode selected.

Line Receiver and 1 MHz Amplifier

The Line Receiver operates as a high speed amplifier. The output signals from the Line Receiver to the Fast Marker Divider and the Divide By 10 circuits are 100 MHz (10 ns), plus or minus the percentage error. The 1 MHz Amplifier operates as a dual line receiver, providing the reference output to the rear interface and conditioning the fixed 1 MHz signal from the Reference Loop for proper operation of the TTL devices in the Count Down Circuit.

Fast Marker Divider

The Fast Marker Divider circuit produces pulses of approximately 5 ns duration with periods as previously defined, and indicated on the block diagram. Fast markers are generated by gating through the negative pulse period of the 100 MHz input signal (5 ns) from the Line Receiver. For example, to generate 50 ns marker, a logic gate is enabled at a 20 MHz rate to pass the 5 ns pulses occurring at a 100 MHz rate. Since the frequency division principle corresponds to time multiplication, the Fast Marker Divider multiplies the basic period of 10 ns by 1, 2, 5, or 10. In order to multiply by 20 and 50 for the 200 ns and 500 ns markers, the gating signal (MKR GATE) is derived from the Count Down Circuit and injected into the Fast Marker Divider circuit.

Fast Marker Shaper and Marker Amplifier

The purpose of the Fast Marker Shaper circuit is to accept the rectangular pulse train from the Fast Marker Divider and convert them to 5 ns pulses with constant pulse width and amplitude. The slew rate of the Marker Amplifier shapes the pulse to a triangular shape. The Marker Amplifier block contains two independent amplifiers, one for time marks and one for slewed edges.

Divide By 10 and Sync Gates

The Divide By 10 circuit produces the 10 MHz trigger drive signals to the Fast Trigger Generator and has a 10 MHz output to the Count Down Circuit.

The Sync Gates ensure that the two counters (Fast Marker and Divide By 10) are synchronized, keeping the trigger pulses coincident with the time marks.

Count Down Circuit and Chop Amplifier

In the Markers mode, the Count Down Circuit divides the 10 MHz signal (from the Divide By 10 circuit) by the appropriate factor to get the selected marker period.

In the VOLTAGE, CURRENT, and EDGE modes, the 10 MHz input is disabled, and the fixed 1 MHz reference is switched into the Count Down Circuit to provide square wave drive to the Chop Amplifier at the selected frequency. The Chop Amplifier converts the single ended input signal to a differential output signal which drives the Chop Isolator circuit (Block Diagram D).

The Count Down Circuit is automatically checked via the TS2 Error Gates during the power on, self test sequence. Refer to the Reference Loop description under Main Timing Generator (Block Diagram B).

Slow Marker Shaper

The Slow Marker Shaper circuit accepts the marker drive from the Count Down Circuit and forms symmetrical triangular markers, whose width is proportional to the selected rate. The markers' symmetry and controlled rise and fall times make them brighter and easier to align with oscilloscope crt graticule lines than fast rise, slow decay markers.

Fast Trigger Generator

The Fast Trigger Generator operates with the Fast (.5 μs to 10 ns) Markers, providing positive triggers synchronized with the 100 MHz clock. The trigger rate is equal to the marker rate for .5 μs, .2 μs, and .1 μs scales, and remains at .1 μs (10 MHz) for the 50 ns, 20 ns and 10 ns scales.

Trigger Divider and Trigger Amplifier

The Trigger Divider contains two cascaded decade dividers to provide RATE ÷ 10 and RATE ÷ 100 gates to the Trigger Amplifier. When RATE ÷ 10 or RATE ÷ 100 is selected, the Trigger Amplifier is enabled only for every 10th or every 100th trigger.

The RATE ÷ 10 gate also controls a marker boost circuit in the Marker Amplifier. This circuit is enabled when MAG X10 is selected, and increases the amplitude of every tenth marker. The marker boost function is not applicable for marker rates faster than 1 μs.

STANDARD AMPLITUDE CALIBRATOR (BLOCK DIAGRAM D)

Power Supplies

The purpose of the Power Supply Interface board (A5A2) is to route the nonregulated dc voltages (+26 V nominal and +8 V nominal) and the mainframe series pass transistor connections from the power module to the regulators on the Power Supply Main board (A5). There are no active components on the A5A2 assembly.

The +26 Vdc nominal is the source for the high and low voltage Preregulators. The nonregulated +8 Vdc nominal from the power module furnishes power for a relay strobe circuit on the Output board (A7). The regulated +5 Vdc furnishes power for all of the circuit board assemblies except A9, A9A1, A2, and A1.

The regulators are positive regulators with external series pass elements. When necessary, to meet operational requirements, the microprocessor will automatically enable or disable the high or low voltage Preregulator output which, in turn, enables or disables the Low and High Voltage Power Supplies.

The HV and LV Power Supplies are isolated dc to dc converters. Their function is to accept the preregulated dc voltages and convert them to various stable dc potentials.

The LV Power Supply converts approximately +15 V to +18 Vdc to −25 V, −15 V, +15 V, and +25 Vdc potentials. The HV Power Supply generates two power sources of 120 V, both floating with respect to ground. The microprocessor uses the Floating Data Registers and the HV Switching circuit to enable, on demand, the proper output level and polarity.

The Preregulators are referenced to chassis ground and the dc to dc converters are referenced to a common floating ground point.

Reference and Floating Data Registers

The purpose of the Reference Data Register and the Floating Data Register is to accept and store data from the microprocessor. The data enables or sets up the Programmable Voltage Reference, Precision Divider, Level Translator, and the Voltage to Current Converter circuits for the operating characteristics associated with the AMPLITUDE modes (VOLTAGE, CURRENT, EDGE, and FAST EDGE). The floating ground system for the Floating Data Register is separated from the chassis ground system for the Reference Data Register by the Data Isolators (transformers).

These registers are eight stage serial shift registers having a storage latch associated with each stage for strobing data from serial inputs to parallel outputs.

On power up, the microprocessor conducts a diagnostic routine on the data registers by retrieving known data shifted through the data registers and the VS1 Error Gating circuit.

Programmable Voltage Reference (DAC)

The Programmable Voltage Reference includes a multiplying digital to analog converter. The purpose is to convert a 10-bit string of 1's and 0's to an equivalent dc analog value. The output voltage from the voltage reference is equivalent to $V_o = -5\ V\ [1/(1 + x)]$. The value for x includes the indicated percent error variable, a calibration factor, and a calculated correction factor. The microprocessor performs the necessary calculations and then loads the data registers to latch the required 10-bit input code for the Programmable Voltage Reference (DAC).

Precision Divider and Level Translator

The Precision Divider is programmed to select one of eight voltage levels derived from a precision resistive divider. The resistive divider input is determined by the Programmable Voltage Reference output level. The microprocessor programs an output voltage level dependent on the selection of a front panel keyswitch associated with the NUMBER OF DIVISIONS (MULTIPLIER) and the selected units per division.

The output of the Precision Divider is referenced to floating ground. The Level Translator contains an operational amplifier and switching circuit that accepts the Precision Divider output, multiplies it by 2 or 4 (depending on the operation required), and changes the reference from floating ground to a −25 Vdc reference level.

Voltage to Current Converter and SAC Chopper

The Voltage to Current Converter and its associated switching circuitry operate in conjunction with the Precision Divider to generate a range of output current (100 μA to 10 mA). The output currents are related to the entire range of amplitudes required for the VOLTAGE, CURRENT, and EDGE modes.

When operating in the VOLTAGE mode, the Voltage to Current Converter sets the current reference for the Low or High SAC (Standard Amplitude Calibrator) circuits. For the EDGE mode it sets the current reference for the Low SAC (which produces the source voltage for the High and Mid Edge Generators) or the Low Edge Generator. For the CURRENT Mode, the converter sets the current reference for the Current Amplifier.

The Voltage to Current Converter output is chopped by the SAC Chopper before it is applied to the Low or High SAC currents. The chopping signal frequency is derived from the Count Down Circuit (Block Diagram C) and routed through the Chop Isolator. The Count Down Circuit is programmed by the microprocessor when a FREQUENCY keyswitch is pressed, or a command is received via the GPIB.

Low SAC and High SAC

The Low SAC block contains an operational amplifier circuit whose output is in the 0.1 V to 10 V range. When a voltage amplitude in the 40 μV to 10 V range is outputted from the CG 5001/CG 551AP, a relay is activated to route the Low SAC signal through the SAC Attenuators to the main OUTPUT connector.

When the EDGE mode is selected the output of the Low SAC circuit is routed to the Mid-Edge and High Edge Generator circuits.

For Pulse Head accessory operation the Low SAC circuit operates as a dc supply source. This voltage is applied to the control pin of the OUTPUT connector.

The High SAC block contains an operational amplifier circuit with output amplitudes in the 10 V to 200 V range. When required, the microprocessor activates a relay to route the High SAC signals through the SAC Attenuators to the OUTPUT connector.

Current Amplifier and Chopper

This functional block contains an operational amplifier and chopping circuit that produces output currents in the 1 mA to 100 mA range. When the CURRENT mode is selected, a relay is activated to direct output currents through the front panel CURRENT loop, or through the SAC Attenuators to the OUTPUT connector.

SAC Overload Sense

The SAC Overload Sense block contains a monostable multivibrator circuit that notifies the microprocessor when either the Low SAC or High SAC circuits exceed their current limits, or when the Current Amplifier circuit exceeds its voltage limit. When the microprocessor senses the error via the VS1 Error Gating circuits, the front panel UNCAL indication is displayed. The microprocessor then reports an error to the GPIB controller: ERR 1 for an overloaded Current Amplifier or ERR 2 for an overloaded SAC amplifier.

Edge Generator Circuits

These circuits generate output pulses with fast risetimes (or falltimes) with low amplitude aberrations when the CG 5001/CG 551AP is operated in the EDGE mode. The percentage error variable for accurate amplitudes is not applicable in the EDGE mode. However, the output amplitude can be adjusted by the VARIABLE control.

The Low Edge Generator block contains current sources and differential amplifiers which produce either positive or negative going pulses into a 50 Ω load. The reference voltage for the Low Edge Generator is set across a resistor on the Output board (A7). The Low Edge Generator output is attenuated X2, X5, X10, X20, or X50 by the Low Edge Attenuators. The output pulses are in the 20 mV to 1 V range with edges faster than 1.3 ns. Total aberrations are less than 4 percent.

The Mid and High Edge Generator blocks contain operational amplifier circuits that generate the low distortion edges in the high amplitude range. The Mid Edge Generator operates in the 1.2 V to 20 V range, while the High Edge Generator operates in the 20 V to 100 V range. The output pulses from these generators are positive going only, and current limited to 10 mA. The high amplitude pulse risetime is less than 100 ns and the total aberrations are less than 4 percent.

Edge Overload Sense

This block contains a circuit that locks up when the CG 5001/CG 551AP becomes overloaded in the EDGE mode (internal circuits exceed their current limits). If an overload is sensed when operating in the 1.2 V to 100 V range, a status signal is reported to the microprocessor via the Edge Overload Sense circuit. When the microprocessor senses the error through the VS2 Error Gating circuit, it generates the UNCAL indication and reports ERR 3 to the GPIB controller.

Pulse Head Drive

The functional block containing the Pulse Head Drive circuit is programmed through the Output Relay Control block to produce the required driving signals for the Pulse Head accessory when the CG 5001/CG 551AP is operating in the FAST EDGE mode. The output of this circuit is normally positive or negative going square waves, 5 V in amplitude at a frequency from 10 Hz to 100 kHz. This circuit also contains an adjustable delay circuit for setting the time delay between the output trigger and the 200 picosecond pulse (risetime) from the Pulse Head accessory.

Output Relay Control and Output Switching

The Output Relay Control block contains output data registers and a relay strobe circuit. The data registers activate the proper latching relay(s) through the various high current drivers which in turn directs the output signals to the Main OUTPUT connector. The latching relays are in the functional blocks for the Output Switching and Low Edge Attenuator circuits. The Output Relay Control circuitry also controls nonlatching relays for the SAC Attenuators and the CURRENT loop outputs.

Head Programmer

The Head Programmer functional block contains a data register through which a relay is activated to switch the Low SAC output voltage to supply power for the Pulse Head accessory.

If the Comparator Head is applied to the OUTPUT connector, the microprocessor turns on the power for the Comparator Head.

The Head Programmer block also contains a detection circuit that recognizes an over-loaded or under-loaded condition for the Pulse Head or Comparator Head. If an accessory head is defective, a status signal is generated through the VS2 Error Gating circuit to notify the microprocessor. An error code (ERR 5) is then displayed on the front panel and reported to the GPIB controller when requested.

NOTE

The presence and identification of a Pulse Head or a Comparator Head accessory is determined through the Head Sense circuits (Block Diagram A). If a Pulse Head accessory is not attached when the FAST EDGE mode is entered, the microprocessor causes the words ENTRY ERROR to be displayed on the front panel, or when requested via the GPIB, reports ERR 4 to the controller. Refer to the discussion of Block Diagram A.

Power On Test & VS2 Error Gating

The functional block for the Power On Test contains a data register, attenuators, operational amplifiers, and a voltage window comparator which generates error signal through the VS2 Error Gating circuit if the Standard Amplitude Calibrator section of the CG 5001/CG 551AP is unable to produce a desired output signal. At power on, the microprocessor tests the operational capabilities of the Low SAC, High SAC, Current Amplifier, all three Edge Generators, and the shift register in the Output Relay Control circuit.

DETAILED CIRCUIT DESCRIPTION

Introduction

Complete schematic diagrams are found in the Diagrams and Illustrations section in Vol. 2 of this manual. Refer to the preceding CG 5001/CG 551AP System Description and to the indicated schematic diagram numbers throughout the following circuit descriptions.

CENTRAL PROCESSING

Microprocessor (U3041) 28

The 6808 microprocessor, U3041, controls the internal operation of the CG 5001/CG 551AP. It accepts and decodes commands from the front panel or the GPIB and sets other hardware operating parameters in response to these commands.

During an instruction fetch (the first one, two, or three machine cycles, depending on the instruction), successive data bytes of an instruction word are loaded from the program memory (ROM) into the microprocessor. The microprocessor decodes the byte(s) and generates the machine states and control signals necessary to execute the instruction.

Refer to a 6808 data manual for more detailed information if necessary.

System Clock 28

The system clock is generated on board the 6808 microprocessor (U3041). The output of the microprocessor is the E line which runs at a 1 MHz rate and is used to synchronize all memory and peripheral accesses. Y3032, a 4 MHz crystal, is the frequency determining element of the clock circuit and sets the basic accuracy for some of the self-tests.

Reset 29

The reset signal is generated by pulse stretching the power on-off detect signal. Q3061 is used to rapidly discharge the reset timing cap C3073. When the power on-off signal indicates power is stable, capacitor C3073 charges through R2067 and CR3063. When C3073 is discharged, U3062 generates a low output to reset the GPIA, PIAs, and microprocessor. When C3073 is fully charged, U3062 allows R2042 to pull the reset line to +5 V.

Microprocessor Interrupts (IRQ, NMI) 28

Interrupt Request (IRQ). This input, when asserted, requests an interrupt sequence in the 6808. The processor completes the current instruction before accepting the interrupt. The processor then tests the interrupt mask bit, and if set, ignores the interrupt; otherwise, the current processor conditions are pushed into memory and execution starts at an address specified by a vector located at address locations FFF8 and FFF9.

The GPIA (U3021) and Set Up PIA (U4022) are wire-ORed together to this input. Internal routines determine the source of the IRQ, and perform the required activities to resolve the request.

Non-Maskable Interrupt (NMI). The NMI input operates in a similar fashion. The only differences are that the interrupt mask is not checked and the location of the vector is different. This interrupt is not used in this instrument.

CPU Regulator 31

U4065, the npn series-pass transistor, and U4071 as a reference, furnish regulated +5 V power to the A1 (Front Panel), A2 (Main Interconnect), and A9 (CPU) boards. U4071 also supplies +2.5 V used by the power on-off detect as a reference. Current limiting on the +5 V supply is done by sensing the voltage across R4064. When approximately 2.5 A flows through R4064, the .6 V drop turns on a transistor which removes drive from the npn series pass. Over-voltage protection is supplied by VR5052, C5061, R5061, and Q3066. When the +5 V supply exceeds 6.2 V, VR5052 conducts enough current to turn on the SCR (Q3066) blowing the fuse F4085. C5061 and R5061 keep short duration noise from triggering Q3066.

The +12V is generated by U4074, a single chip, adjustable, three terminal regulator. The −12 V is similarly generated by U4086.

Power On-Off Detect 29

Starting with main power off, the power up sequence is:

1. Q2065 is turned off, disabling the RAM (U1043).

2. Power is applied to the instrument.

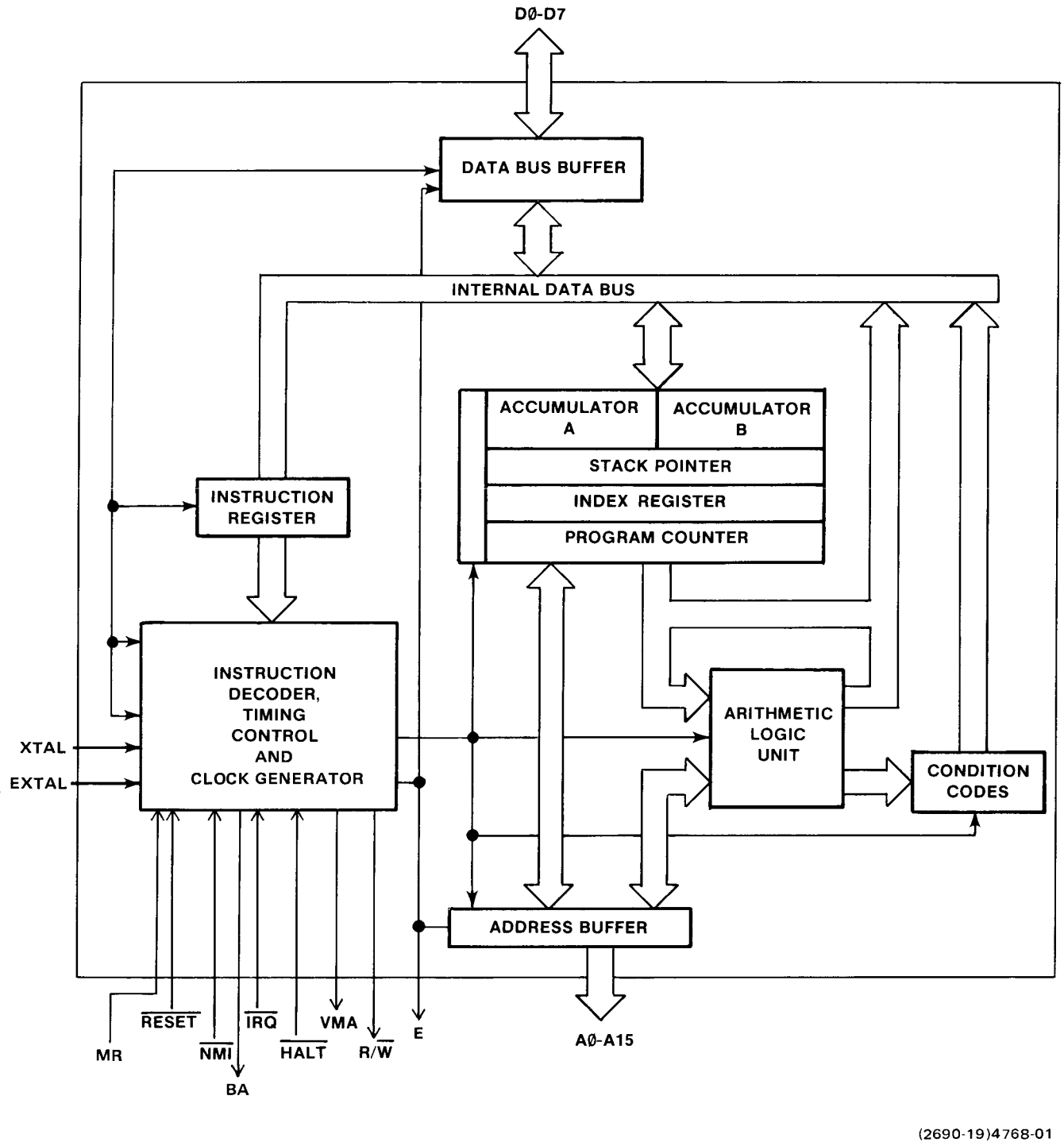


Fig. 4-6. Block diagram of the M6808 microprocessor.

3. The 2.5 V reference (U4071) stabilizes at about 4 V on the +11.5 V/+8 V supply.

4. The +12, −12, and 5 V exceed 10% low in voltage.

   a. In an old mainframe there is no connection to the cathode of CR4094, so the output of U1021C goes high.

   b. In a new mainframe, the PWR signal rises approximately two seconds after power is stabilized, allowing U1021C's output to rise.

5. $\overline{\text{Reset}}$ is low due to the discharge state of C3073, causing the output of U3062 to pull to ground.

6. Q2065 turns on, enabling the RAM (U1043).

7. C3073 charges through R2067, CR3063, and R3074.

8. U3062's output turns off, allowing $\overline{\text{Reset}}$ to rise to +5 V.

9. The microprocessor begins its self-test.

Starting with the main power on, all conditions are where left in the previous discussion. When the main power is turned off, the +11.5 V/+8 V supply begins sagging. When this supply descends below 6.4 V, the following sequence is initiated:

1. The output of U1021C goes low, turning off Q2065, and thereby disabling the RAM (U1043).

2. The output of U1021C being low causes Q3061 to rapidly discharge C3073, causing the output of U3062 to go low, resetting the microprocessor, and holding it there until the power is sufficiently low as to no longer matter.

C2021 and R2022 around U1021C set hysteresis and pulse stretch any incoming signals so that if a long enough noise pulse to disable the RAM occurs, it will also partially discharge C3073 through Q3061. C3071 and R3072 around U3062 perform the same function, pulse stretching the $\overline{\text{Reset}}$ line to about 3 μs; sufficient to guarantee microprocessor reset conditions.

Addressing Memory and Peripherals 

The microprocessor accepts, decodes, and transmits commands using the program memory (ROM and RAM), the GPIB controller (U1702), and the Peripheral Interface Adapters (U3026 and U4022). Communications between these devices is via an 8-bit data bus, a 16-bit address bus, and a set of address decoding devices. The address lines are unbuffered. The data buffer, U2051, is always enabled.

Table 4-2 shows the memory map (address space allocations) for the CG 5001/CG 551AP. The ROM contains the CG 5001/CG 551AP operating firmware.

Table 4-2
CG 5001/CG 551AP MEMORY MAP

Hex Addresses	A (Upper) 15 14 13 12 11 10 9 8	A (Lower) 7 6 5 4 3 2 1 Ø	Comments
F F F F	1 1 X X X X X X	X X X X X X X X	ROM
C Ø Ø Ø	1 1 X X X X X X	X X X X X X X X	U1032 (16K bytes)
9 Ø Ø 7	1 0 0 1 0 X X X	X X X X X 1 1 1	GPIB Control
9 Ø Ø Ø	1 0 0 1 0 X X X	X X X X X 0 0 0	U1702 (repeats every 8 locations to 97FF)
Ø 8 2 3	0 0 0 0 1 X X X	X X 1 0 X X 1 1	Set up PIA
Ø 8 2 Ø	0 0 0 0 1 X X X	X X 1 0 X X 0 0	U4022
Ø 8 1 3	0 0 0 0 1 X X X	X X 0 1 X X 1 1	Front Panel PIA
Ø 8 1 Ø	0 0 0 0 1 X X X	X X 0 1 X X 0 0	U3026
Ø 7 F F	0 0 0 0 0 1 X X	X X X X X X X X	Write Protected RAM
Ø 4 Ø Ø	0 0 0 0 0 1 X X	X X X X X X X X	1/2 U1043
Ø 3 F F	0 0 0 0 0 0 X X	X X X X X X X X	Scratch RAM
Ø Ø Ø Ø	0 0 0 0 0 0 X X	X X X X X X X X	1/2 U1043

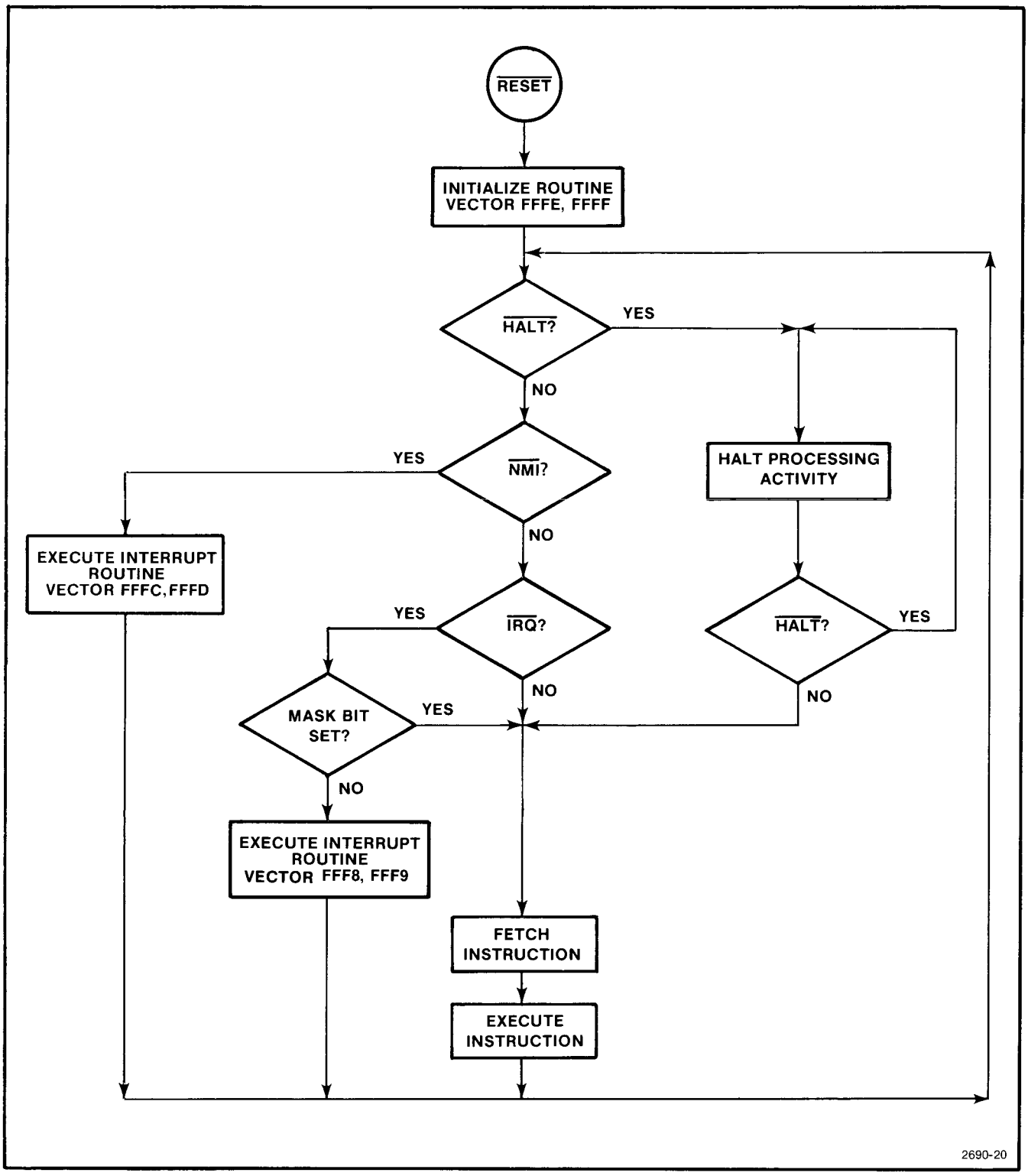


Fig. 4-7. Flow chart of the M6808's main decision paths.

ROM. Selection of the ROM occurs when address lines A14 and A15 are both high. At this time the output of U1063A goes low enabling U1032. The $\overline{OE}$ output enable line into the ROM is driven by U1063B such that VMA (valid memory address) and $\phi 2$ (the Enable operation line from the processor) must both be high to enable the ROM. AØ—A13 select the particular byte in the ROM that the processor desires to access. The data in that byte appears on the DØ—D7 lines where it can be read by the microprocessor.

RAM. Alterable memory requirements for the various programmed operations are met by the RAM. This memory is totally battery backed up, but only part is actually used for keeping information over a power down, power up cycle.

U1043 is a 2K X 8-bit CMOS memory that meets all of the variable data storage requirements for the CG 5001/CG 551AP. It is used in two separate ways. The lower half of the RAM (addresses ØØØØ through Ø3FF) are the main operational temporary storage and the locations for settings, allowing the instrument to power up to its last used state.

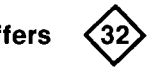
The upper half of the RAM (Ø4ØØ through Ø7FF) are not only kept alive by the battery, but also protected from being written when not in the calibration mode. This is accomplished by the logical combination of Q2069, Q2041, Q2061, and S1061. When the switch S1061 is in the RUN position, Q2069 and Q2041 form a discrete NAND gate, the output of which is inverted by Q2061. This combination of parts forces the RAM chip's AlØ line to remain low (addressing the ØØØØ—Ø3FF block) when attempting to write to the upper portion of the RAM. When reading the upper portion of the RAM both AlØ and R/$\overline{W}$ will be high allowing the RAM's AlØ line to go high, reading the correct location. When the switch S1061 is in the calibrate position, Q2041 is shorted out, allowing Q2069 and Q2061 to act as a non-inverting buffer, enabling both read and write access to the entire RAM.

BT4041 supplies the power for the RAM (U1043) when the main power is off. R3051 and CR3065 provide protection against short circuits and reverse charging. When operating, the power requirements of the RAM expand significantly. Q3063 supplies the extra power requirements while the +11.5 V/8 V power supply is higher than the 5 V supply. CR3067 ensures that reverse β of the transistor Q3063 does not short the battery to +5 as the main power supply dies.

The RAM address decoding involves inverting the $\overline{RAMSEL}$ output of U2065 with U2064A and then combining this signal with $\phi 2$ at U2064D. This output is low (enabling RAM) when the $\overline{RAMSEL}$ line is low and $\phi 2$ is high.

GPIB Controller. The GPIB controller is accessed directly by the $\overline{GPIBSEL}$ line coming from U2065.

PIAs. The PIAs require three lines to be in the correct states to enable them. One of these, PIASEL, comes from inverting the output of U2065. This line is common to both PIAs. Additionally, each PIA looks at two address lines, requiring one to be high and one to be low. The Front Panel PIA requires A5 to be low and A4 to be high. The Set Up PIA requires A4 to be low and A5 to be high.

Address Switch, GPIB Control, and Buffers 

Address Switch. The Address Switch Register, U2028, buffers 8 bits of information. These include the six address switch positions plus the Last Used Settings (LUS) jumper and the Wait For Continue (WFC) jumper. Switches AØ through A4 set the CG 5001/CG 551AP's primary IEEE 488 address. The remaining switch sets the terminator sequence (CR-LF/EOI or EOI only). This information is acquired by the processor at power up by reading address 9ØØ4 which causes U1702 to bring $\overline{ASE}$ low, enabling U2028.

GPIB Control. U1702 controls much of the microprocessor's interaction with the IEEE 488 bus. The specific tasks of handshaking information onto and off of the bus, command decoding in many instances, and serial polling are handled by U1702. This frees the microprocessor to deal with operational parameters, leaving the details of bus operation to U1702.

U1702 supplies the 16 lines required by IEEE 488 plus two lines to control the bus buffers. These two lines (TR1 and TR2) are used as follows. TR1 goes high whenever the GPIB controller is outputing data except for during a parallel poll. TR2 goes high whenever the controller is outputing data, including during a parallel poll.

Buffers. The two buffer IC's (U1081 and U2081) perform the basic operations of handling IEEE 488 drive and termination requirements. U1081 contains 8 bidirectional buffers for buffering the data lines. Additionally the device can be operated either tri-state or open collector. The PE line controlls the method of driving the bus. Being connected to TR1, the bus is driven tri-state under normal conditions, and open collector during a parallel poll. The TE line on U1081 is high during any transmission, and enables the drivers, disabling the receivers during a transmission.

On U2081, since the CG 5001/CG 551AP does not have control capability, the DC line is wired permanently high. The TE line on U2081 turns around the drivers and receivers on the DAV, NDAC, NRFD, and EOI lines.

Depending upon whether the instrument is a CG 5001 or CG 551AP, either J1111 or the jumpers W3091 and W2091 will be installed. The CG 5001 has J1111 which attaches to the A8A1 board, interfacing to the TM 5000 mainframe's GPIB connector. The CG 551AP has W2091 and W3091, making connection to the rear interface pins used in the modified TM 500 mainframes.

Peripheral Interface Adapters ◇30

Address selection (assertion of the PIASEL line) for the U3026 and U4022 has been previously discussed. A brief discussion of the internal architecture of these devices will be helpful in understanding how the microprocessor communicates with the instrument's internal circuits.

Two separate input-output ports, two data direction registers, and two control registers comprise each device. See Fig. 4-8. Each line in the input-output ports can be programmed to be an input or output by setting corresponding bits in the data direction registers. Two interrupt outputs, IRQA and IRQB, can be used to signal the microprocessor that the PIA has data to be read or needs service. It is not always necessary that the microprocessor be interrupted before it reads data from these devices. The IRQB interrupt is not used in the CG 5001/CG 551AP.

Two interrupt inputs (CA1 and CB1) are individually programmable as positive or negative edge sensitive. Two more lines (CA2 and CB2) can be programmed as edge-sensitive interrupt inputs or peripheral control outputs. The states of these inputs and outputs are programmed through the control registers. The internal interrupt flags are also read from the control registers.

The chip select lines (CS0—CS2) are used to address the PIA, while the register select lines (RS0—RS1) select the individual registers within the PIA.

Front Panel Interface (U3026). Communication with the instruments front panel is via U3026. The signal lines for U3026 are briefly described below:

DSØ—DS7 (PAØ—PA7). These eight, dual purpose lines are used to load the Display Multiplexer circuit (schematic 2) with the information for illuminating the seven-segment displays, the alphanumeric displays, and the lighted pushbuttons on the front panel. When the microprocessor is not required to update the front panel information, these eight lines are programmed to be inputs. DSØ—DS3 are used to read the buffered column information (KCØ—KC3) from the keyboard switch matrix on assembly A1 (Front Panel). DS4—DS7 are used for reading the internal errors and status codes (E1—E4) from the amplitude and timing sections (see Table 4-1).

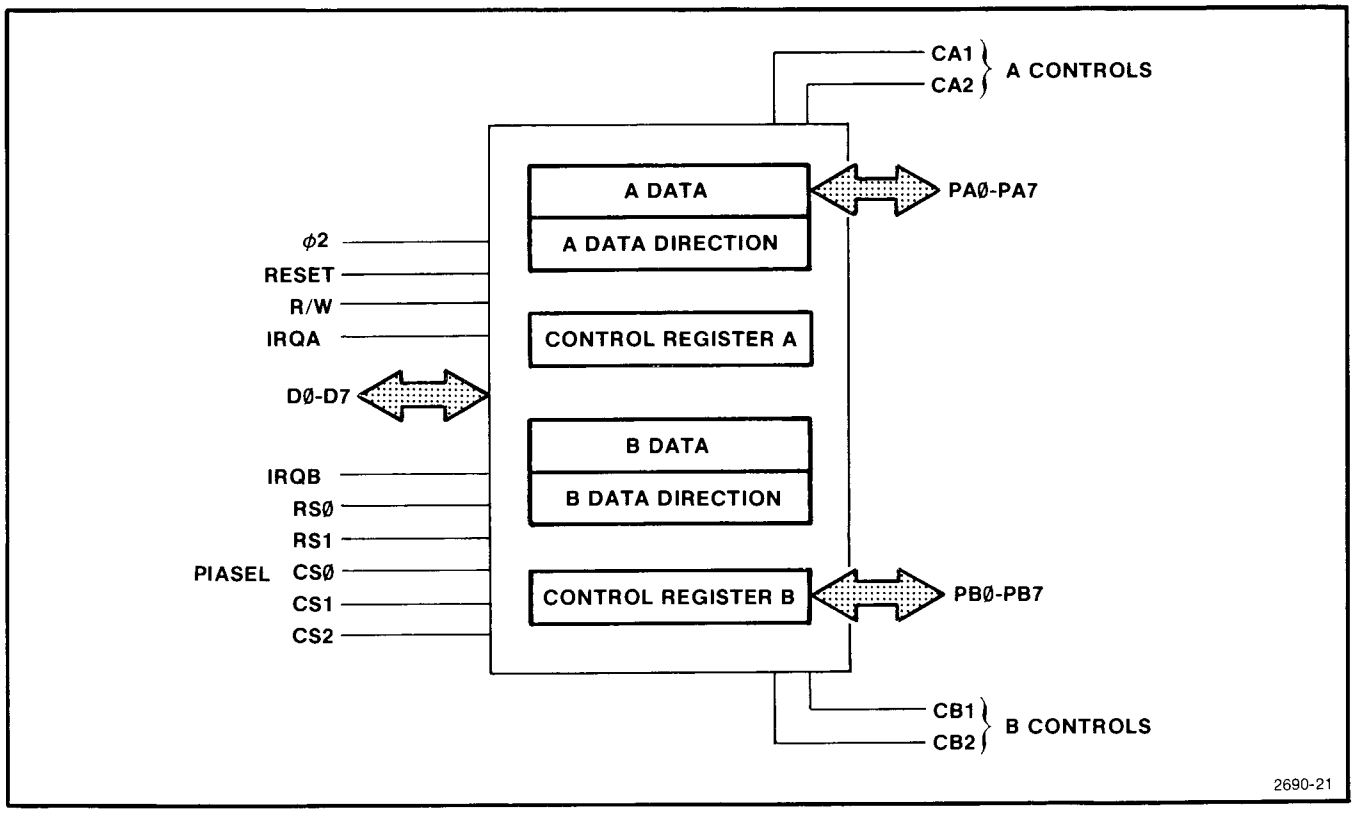


Fig. 4-8. Block diagram of a peripheral interface adapter.

DAØ—DA3 (PBØ—PB3). These four lines are programmed to be outputs at all times, but have two purposes:

1) when updating the display they are used to designate the word address for the Display Multiplexer;

2) at other times, they are used to scan the row addresses for the front panel keyboard switch matrix (KRØ—KR3).

WØ—W1 (PB4—PB5). These two lines are programmed to be output at all times and are used to write data on lines DSØ—DS7 into the Display Multiplexer circuits.

DSPL/LOAD. Programmed as an output control line for the Display Multiplexer and keyboard switch matrix scan. When this line is low, the Display Multiplexer is configured for loading with DAØ—DA3 word address information; the display is blanked during display updating. When this line is high, it enables the Display Multiplexer circuits and allows the microprocessor to read the keyboard switch matrix column information (KCØ—KC3).

COMPARATOR DRIVE (CA2). Programmed as an output for the Comparator Head accessory. When low, the comparator drive is off; when high, the comparator drive is on.

Setup Interface (U4022). Programming of the instrument's internal functions is via U4022. The signal lines for U4022 are briefly described below:

KNOB INTRPT (CA1). Programmed as an interrupt input. When the position of either knob associated with the Optical Switch is changed, U1621 detects this change and interrupts the microprocessor, telling it to update either the units/division status or the variable status (percent error).

ALS1, ALS2, BLS1, BLS2 (PAØ—PA3). Programmed as inputs. These lines are used to read the position status of the Optical Switch. After one knob has been turned, the interrupt processing routine reads the new position data. When compared with the old position data, directional information can then be determined. ALS1 and ALS2 indicate the units/division status. BLS1 and BLS2 indicate the variable status (percent error).

SIGNATURE ANALYSIS JUMPER (PA4). This jumper controls whether the instrument powers up in signature analysis mode, or normal operation mode. See Section 6, Diagnostic Procedures, for more information.

RMTVAR OUT (PA6). Programmed to output serial information to the Remote Variable accessory.

RMTVAR IN (PA7). Programmed as an input to accept serial data from the Remote Variable accessory.

RMTVAR CLK (CA2). Programmed as an output or input. Normally an input—more specifically an interrupt input. When something changes on the Remote Variable accessory, this line is asserted low, interrupting the microprocessor. The microprocessor then programs this line as an output to act as a data clock signal to read in serial data information and then uses it to output serial information to illuminate the appropriate pushbuttons on the accessory. This line is then restored as an interrupt input. Also, any time the front-panel display is updated, this line is programmed as an output to update the Remote Variable lights.

DATA (PBØ). This line is used as an output to send serial data information to the amplitude and timing hardware shift registers.

DATA CLK (CB2). Programmed as an output. Used to clock data information to the hardware shift registers in the amplitude and timing sections.

VS2 (PB1), VS1 (PB7), TS1 (PB2), TS2 (PB3). Programmed as outputs. These lines are used to strobe data information into the output registers of the hardware shift registers.

HS1—HS3 (PB4—PB6). Programmed as inputs. Used to sense what type of accessory head is attached to the main output connector.

Head Sense 

U1531 is a triple-differential voltage comparator operating to detect four different load conditions for the sensing element associated with the main output connector. A specific load condition sets up a specific code on the HS1, HS2, HS3 signal lines for U4022 which the microprocessor reads to determine what type of accessory head is attached. The accessory input codes to U4022 are as follows:

HS1	HS2	HS3	Accessory Type
0	0	0	None
1	0	0	Programmable Pulse Head
1	1	0	Not Used, Reserved
1	1	1	Comparator

Voltage divider networks set the dc comparison levels on pins 5 (1 V), 12 (3 V), and 3 (4.95 V) of U1531. Q5041 operates as a current source (about 7.5 mA) for a specific load resistance located in each type of accessory head. The voltage level on the sensing element and on pins 6, 13, and 2 of U1531 with no accessory attached is about 5 V, a level that is greater than any of the three comparison voltages. The output of each comparator will then be low, (all zeros on the HS signal lines), indicating no accessory attached. When the Comparator Head accessory is attached, the dc level on pins 6, 13, and 2 of U1531 is driven below 1 V and the output of each comparator is at a high level (all one's on the HS signal lines).

Front Panel Display and Keyboard ◇1◇2

The front panel display and most of the pushbuttons (keyboard) are continually scanned and addressed, under the control of a 2.5 kHz Front Panel Clock signal at pin 8 of U1631, located on the Main Interconnect board (A2). The clock circuit, U1641E, operates on the principle of a hysteresis switch.

The seven-segment LED's, the sixteen-segment alphanumeric LED's, and the pushbutton lights on the keyboard are considered as digits, characters, or addresses to which the microprocessor sends data when updating the front-panel display. Refer to Fig. 4-9 for the digit select designations and a typical display scanning sequence.

U1631 is a programmable counter whose outputs (RAØ—RA3) may be preset to any state by asserting pin 1 low true and entering the desired data (DAØ—DA3). The outputs will change to agree with the input data, independent of the state of the Front Panel Clock.

The microprocessor has full control over the front panel displays via pin 1 of U1631. When it desires to update the display and keyboard lights, pin 1 of U1631, pin 12 of U1621A, and pin 13 of U1441 are asserted low true. The display is blanked at this instant while the microprocessor writes complete update data to RAM pairs, U1521-U1531, and U1522-U1532. Each RAM device can contain 16 4-bit words (256 total bytes).

The front panel display circuits appear as a 16 row X 13 column matrix to the Display Multiplexer. The RAM devices output 16-bit binary information to the anodes of the display LED's via sixteen current drivers (transistors), while the digit (row) select information is derived from the SØ through S12 signal lines.

The displays are not illuminated until the microprocessor sets pin 1 of U1631 high (DSPL). When pin 1 goes high, U1631 contains a binary number (the last number left by the microprocessor) on its output lines, and on the next clock edge, starts to count up through sixteen counts for a complete display scanning cycle. As the count changes, so do

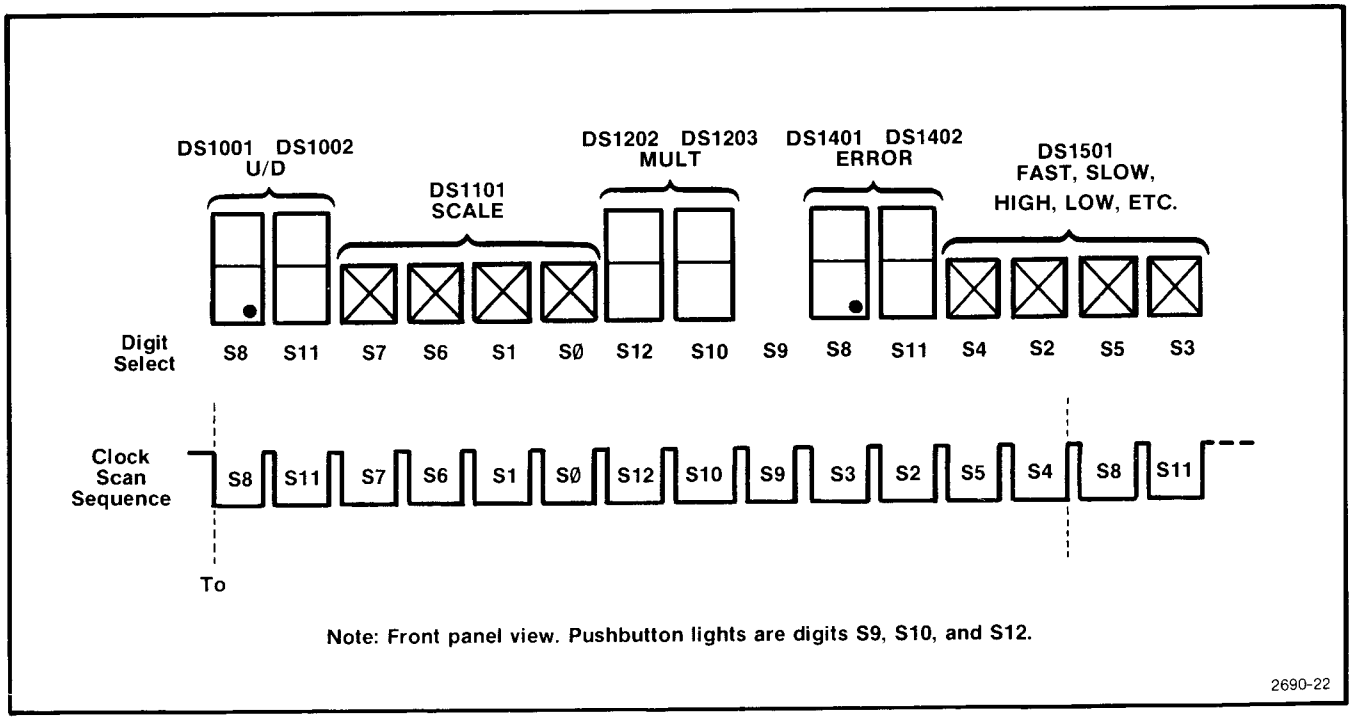


Fig. 4-9. Display scanning sequence.

the states on the RA∅—RA3 data lines. U1432 and U1441 decode the changing data to select the proper digit (address) during the scanning cycle.

Front panel digital information from the keyboard switches is buffered by U1621A. When the microprocessor is loading the RAM devices to update the display, all of the inverters in U1621A are gated off by the high level on pin 1. This locks out the keyswitch matrix column information (KC∅—KC3) from data lines DS∅—DS3.

During display time, pin 1 of U1621A is set low. This allows the microprocessor to perform a routine which addresses the keyswitch decoder, U1221, to obtain column information. Complete addressing of U1221 requires ten 4-bit address codes on the KR∅—KR3 lines. As each 4-bit code addresses U1221, one of the output lines (row) goes low. If a particular key is closed, a low level is placed on one of the column lines (KC∅—KC3). This information is read by the microprocessor via the front-panel peripheral interface adapter, U1701 (schematic 29). Each output line of U1221 is addressed more than once during the routine to make sure that a keyswitch has been closed.

The Optical Switch, S1121, is a photoelectric coder for the UNITS/DIV and VARIABLE (error) knobs. The switch uses a Gray-encoded disk divided into four bands with transparent and opaque segments. A light source, DS1121, is placed on one side of the disk and a set of four photoelectric transistors on the other side, arranged so that one cell is behind each band on the coded disk. The Gray-coded output from S1121 is buffered by U1641A, B, C, and D and applied to the ALS1, ALS2, BLS1, and BLS2 signal lines on U1721 (schematic 29). Refer to the previous discussion for these four lines, under Peripheral Interface Adapters (Setup Interface, U1721).

MAIN TIMING GENERATOR

Introduction

Before reading this circuit description, refer to the block diagram discussion for the Main Timing Generator (Block Diagram B).

±12 V Regulators (A4 Time Mark Board) 

U1610 is a dual polarity tracking regulator with balanced positive and negative 12 volts outputs. Both output voltages are adjusted by a single resistor, R1400.

U1610 contains a reference unit, a positive voltage regulator, and a negative voltage regulator. The reference unit inputs are pins 10 and 11. The voltage on pin 10 sets up the negative voltage regulator output (pin 8) which, in turn, controls the positive voltage regulator output (pin 1). Frequency compensation is provided by C1601 and C1602. Overvoltage protection is provided by VR1631 and VR1630.

The normal current through R1625 and R1601 when the supply is regulating is about 1.2 mA, causing the series-pass transistors in the mainframe to be normally on and conducting. The current limiting transistors, Q1601 and Q1600, are normally off.

R1627 and R1626 are the current sensing resistors. If the +12 V supply current exceeds about 500 mA the voltage drop across R1627 turns on Q1601, robbing current from pin 3 of U1610. This causes the pnp series-pass transistor in the mainframe to act as a constant-current source. Current protection for the −12 V supply operates in a similar manner when the load current exceeds about 270 mA through R1626. Both supplies are individually short-circuit protected by fuses, F1630 or F1631.

Automatic Time Reference Select 

The external time reference signal is ac coupled from pin 24B of P1006 through C1600 and R1611 and applied to pin 3 of U1510. This signal can be any whole multiple of 1 MHz, up to a maximum of 5 MHz. U1510 converts the ac input to complementary TTL output signals.

When an external time reference signal is applied, CR1410 and CR1411 develop a positive dc level on the base of Q1410; Q1410 then conducts to illuminate DS1410 on assembly A4 (Time Mark board) and set a low level on pin 4 of U1400B. This, in turn, sets a high level on pin 9 of U1400C. This action locks out the 5 MHz signal from the Optional TCXO, Y1501, and allows the TTL signal from pin 9 of U1510 to appear at pin 12 of U1400D. If the Optional TCXO is installed, pin 4 of U1400B is high with no external signal applied, allowing the 5 MHz signal to appear at pin 12 of U1400D.

Pin 13 of U1400D is set high (enabled) only for the MARKER and SLEWED EDGE modes. For the other modes, U1400D is disabled via U1400A, allowing the 1 MHz Reference Oscillator (schematic 12) to free run (not phase locked to an external reference).

Reference Loop and External Reference Phase Lock 

The 1 MHz Reference Oscillator, Q1220 and Y1200, with their associated components, is phase locked to an external reference frequency or to an optional, temperature compensated 5 MHz crystal oscillator, Y1501 (schematic 17).

The External Reference Phase Lock circuit, (U1112A, U1112B, CR1020, CR1012, R1020, R1022, and C1020) operates as a digital phase-frequency detector. This circuit is followed by a transconductance amplifier, U1024, operating as a loop filter. The output of U1024 is turned on and off by a dc level on pin 5. The dc level is derived from the external reference frequency via the rectifier circuit consisting of C1120, CR1130, CR1132, and C1130. The output of U1024, when enabled, controls the bias voltage across the voltage-variable capacitance diodes, CR1214 and CR1212, in the 1 MHz Reference Oscillator circuit. The higher the bias voltage applied to CR1214 and CR1212, the lower the capacitance and the higher the frequency.

Since U1024 is a transconductance amplifier, a voltage input controls the current output; the output impedance is always high. If no signal is present on pin 5 of P1106, the gain of U1024 is reduced to zero and the current output of U1024 has no effect on the 1 MHz Reference Oscillator or the Reference Loop Out-of-Lock Indicator circuit.

The negative edge of the 1 MHz Reference Oscillator clocks U1112A at pin 1, while the negative edge of the external reference signal clocks U1112B at pin 5. Because pin 14 of U1112A is tied high, pin 12 can only be clocked high. When U1112B is clocked, it goes to whatever state U1112A is in at that time.

For initial conditions, if pin 12 of U1112A and pin 8 of U1112B are both assumed low, pin 12 of U1112A will be clocked high by the negative edge of the 1 MHz reference signal. Then, U1112B is clocked to the same state by the external reference signal, causing pin 8 to go low (see Fig. 4-10). This immediately resets U1112A via pin 2. Pin 8 of U1112B remains low, holding U1112A reset and causing it to skip the next negative clock edge of the 1 MHz reference signal. Since U1112A is in the reset state (pin 12 low), U1112B will follow on the next negative edge of the external reference signal. On the next clock edge, pin 8 of U1112B goes high, leaving pin 12 of U1112A free to go high when it is next clocked.

In order for the phase detector to work properly, there must be a slight phase difference between the two input clock signals. When the input clocks are 1 MHz, the outputs of U1112A (pin 12) and U1112B (pin 8) have a frequency that is one-half the input clock rates (500 kHz).

The output of U1112A charges storage capacitor C1020 through R1022 and CR1020. The output of U1112B discharges C1020 through R1020 and CR1012. For the output current of U1024 to remain constant (Reference Loop locked), the voltage across C1020 must average a constant 2.5 V. This means that the net charge added to C1020 by the output of U1112A must balance the net charge subtracted by the output of U1112B. Since R1020 is twice the value of R1022, the output of U1112B must be low for twice as long as the high level output from U1112A for the charges to balance. It is the net charge conditions for C1020 that detects the phase difference between the 1 MHz Reference Oscillator and external reference frequencies.

If the external reference frequency is other than 1 MHz (2, 3, 4, or 5 MHz), the waveforms in Fig. 4-10 are changed somewhat, but the principle is still the same. Operation is similar to that with a 1 MHz external reference, with the following exceptions: 1) the duration of the pulses from U1112A and U1112B is less, 2) the higher the external reference frequency the narrower the pulses, and, 3) for a 5 MHz reference signal, the output frequency is 1 MHz, instead of 500 kHz. For a phase locked condition, time T_2 (Fig. 4-10) is twice the T_1 interval.

If the Reference Loop is out of lock, the net charges added to and subtracted from C1020 do not balance and a beat frequency signal appears on pin 2 of U1024. This signal is amplified by U1024 and ac coupled via C1132. The signal is then rectified by CR1134 and CR1133 to turn on Q1133. DS1131 is then illuminated to indicate that the Reference Loop is out of lock.

The purpose of the 1 MHz Buffer circuit, U1110 and U1100, is to generate a symmetric square wave from the non-symmetric waveform at the emitter of Q1220. Integrated circuit, U1110, is a dual-line receiver with very high gain, and is used as a squaring amplifier. It provides two isolated square-wave outputs at pins 1 and 7. Integrated circuit, U1100, operates as an automatic biasing circuit. The two oppositely phased outputs from pins 1 and 7 of U1110 are filtered to obtain the dc average of each, and are applied to the differential inputs of U1100. Any asymmetry in the two square waves will be in the opposite directions, generating a dc offset across the inputs to U1100. This forces the output (U1100, pin 6) to adjust the bias on pin 3 of U1110A to make the square wave outputs symmetric. When they are symmetric, the voltages at the differential inputs of U1100 become equal. This assumes infinite gain; actually, the voltage difference will be a fraction of a millivolt to generate whatever output is needed to bias U1110 for symmetric square waves.

Sampling Loop (Sampling Phase Gate, Loop Filter, Main VCO) ◇12◇

The purpose of the Sampling Loop is to lock the Main VCO to harmonics of 100 kHz. This permits the Main VCO to be phase locked in 100 kHz steps over the plus or minus 9.9% range of the variable control; corresponding to 0.1% steps at 100 MHz.

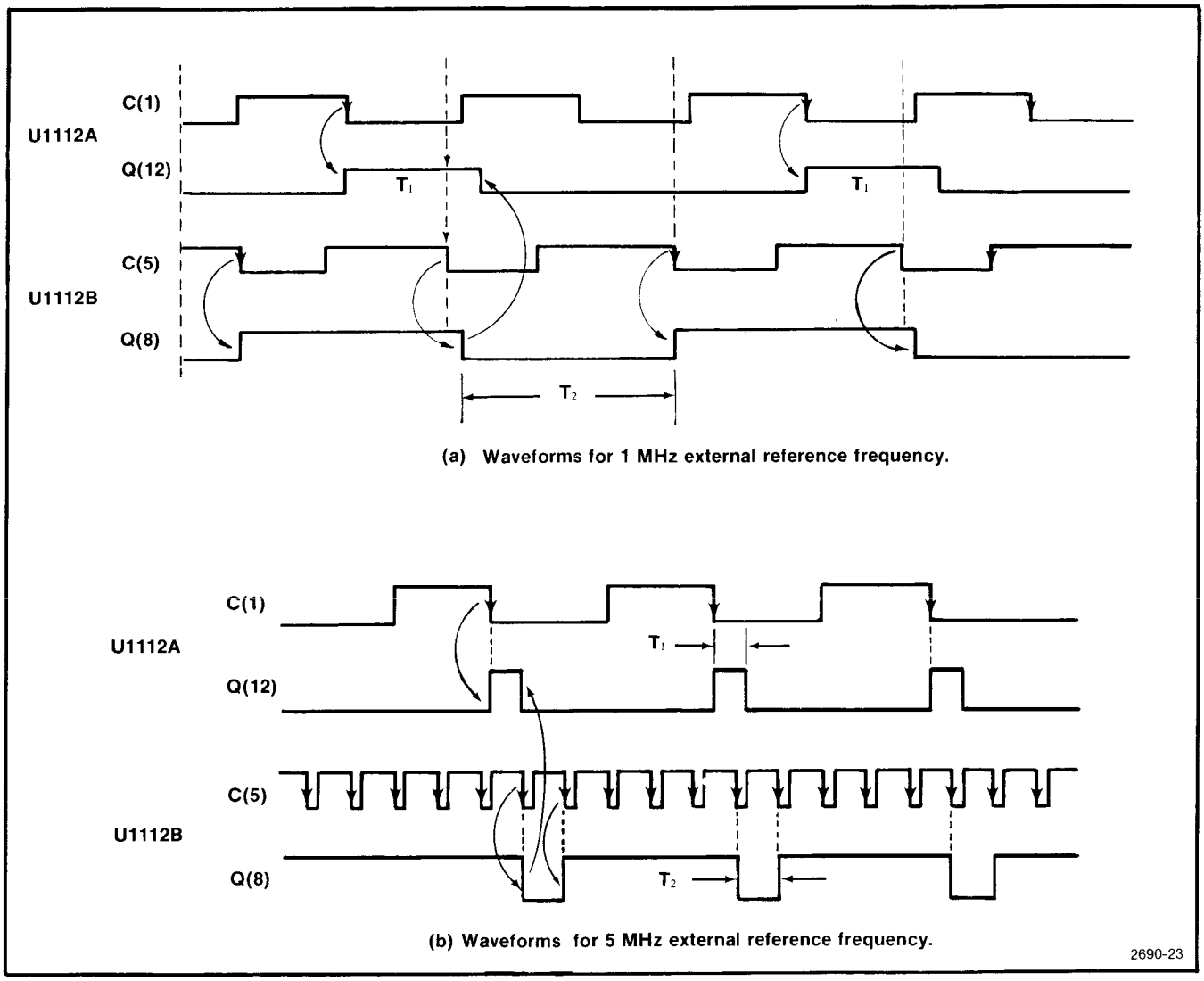


Fig. 4-10. Phase detector waveforms (U1112), External Reference Phase Lock.

The collector current output of the 1 MHz Reference Oscillator, Q1220, is gated through CR1232 or CR1230. The collector current is gated through CR1232 and diverted from the primary winding of T1230 during the positive portion of the 100 kHz strobe holdoff signal that originates in the Reference Divider circuit (schematic 11). During the negative pulse period of the 100 kHz signal, the collector current is gated through CR1230 and the primary of T1230. The 100 kHz strobe holdoff signal allows only every tenth pulse from the 1 MHz Reference Oscillator to be passed on to the Sampling Phase Gate circuit.

The narrow pulses from T1230 are subharmonic relative to the 100 MHz sine-wave signal injected across R1240. The narrow pulses through CR1244 and CR1240 sample this sine-wave signal every 10 μs, charging C1242 and C1244. The sum of the voltages across C1242 and C1244 with respect to their common point is proportional to the phase difference between the Main VCO and the strobe pulses from the 1 MHz Reference Oscillator. The voltages are summed into the Loop Filter circuit through R1144 and R1146.

The Loop Filter circuit, U1140, provides the dc tuning voltage for the voltage-variable capacitance diodes, CR1012 and CR1011, in the Main VCO circuit. Coarse steering signals for the Loop Filter input are injected into the Sampling Loop via CR1031 and CR1030. These signals originate from U1121A and U1221C in the Coarse Steering circuit (schematic 11) and operate only to bring the Sampling Loop on to the correct 100 kHz harmonic. When the frequency is correct, the Coarse Steering Loop is balanced and CR1031 and CR1030 are cut off, disconnecting the Coarse Steering circuit from the Sampling Loop.

The Main VCO frequency is controlled by the control voltage across CR1012 and CR1011; a more positive bias voltage corresponds to a lower frequency. Q1002 and Q1001 operate as ECL level translators for the 100 MHz signals that go to the Steering circuit board assembly (A3A6-100 MHz Buffer, schematic 10 and Main VCO Divider, schematic 11). Note that the power for the Main VCO is derived from two sources, a filtered 10.5 V source via Q1042 and a switched −12 V source derived from the Main Loop Power Switch circuit (schematic 10). The Main VCO is enabled only for the MARKERS and SLEWED EDGE modes.

Main Loop and Slewed Edge Power Switches ◇10◇

The Main Loop Power Switch is turned on in the timing modes only. The microprocessor loads data into data register U1120 that sets pin 13 to a high level. The collector of Q1102 goes low to switch on the 5 V power for the Main Timing Generator ($+5\ V_{SW1}$) and the −12 V power at the collector of Q1010 ($-12\ V_{SW1}$).

Power for the Main Loop Power Switch and the Slewed Edge Power Switch is derived from a non-switched 5 V source at pins 3, 4, and 5 of P1502. These connections are used as the sensing point for the 5 V regulator on the Power Supply Main board (A5). See schematics 4, 3, and 18.

When the SLEWED EDGE mode is programmed, the microprocessor loads data to set pin 14 of U1120 to a high level. Q1002 is turned on to switch on the 5 V power at the collector of Q1001 ($+5\ V_{SW2}$) and the −12 V power at the collector of Q1020 ($-12\ V_{SW2}$). See schematics 11, 4, 5, and 6 through 9.

Coarse Steering Loop ◇11◇ ◇10◇

The Coarse Steering Loop is comprised of the 100 MHz Buffer, Prescaler, Programmable Divider, and the Coarse Steering Circuit. The Coarse Steering Circuit has two inputs: a 10 kHz signal from the Programmable Divider and a 10 kHz signal from the Reference Divider.

When the collector of Q1102 in the Main Loop Power Switch circuit goes low, pin 7 of the Reference Divider, U1230 (schematic 11), goes low to start the internal counters. The Reference Divider divides by 10 and 100 to produce the 100 kHz strobe holdoff signal for the Sampling Phase Gate circuit (previously discussed) and the 10 kHz reference signal for the Coarse Steering Circuit (pin 3 of U1121A).

The 100 MHz signal from the Main VCO, plus or minus the percent error, is buffered by U1311A before being applied to the Prescaler circuit, U1310. The Main VCO signal is converted to balanced ECL signals for transmission to the Time Mark board (A4). The Prescaler, U1310, divides the Main VCO signal by 10 and Q1301 translates it to TTL levels. The output of U1201A is connected to clock three, four-bit counters in parallel at pin 2 of the Programmable Divider (U1211, U1210, and U1110).

The Programmable Counter is a 12-bit synchronous counter capable of counting up to 4096_{10} (FFF_{16}). When the variable control is set to 0.0%, the microprocessor loads the Data Registers, U1220 and U1211, with a hexadecimal number, 218_{16}. Because pin 6 (bit 12) of U1211 is hardwired to a high level (logical 1) and pins 3 and 4 are connected to see the same bit value, the counter is actually loaded with the binary number equivalent to the decimal number 3096_{10} ($C18_{16}$). The counter is continually counting up from 3096_{10} to 4096_{10}. This is a total of 1000 counts, causing the Programmable Counter to divide the Main VCO signal by the number N = 1000. The corresponding numbers for the limits of the complete range of the Programmable Divider are listed in Table 4-3.

When the coarse steering loop is balanced, the output of the Programmable Divider (pin 15 of U1211) will be 10 kHz, equal to the 10 kHz reference frequency from the Reference Divider. The output of the Programmable Divider is applied to pin 11 of U1121B in the Coarse Steering Circuit (schematic 11).

Table 4-3
DATA FORMAT FOR THE PROGRAMMABLE DIVIDER

Timing Error	Hex Data	Counter sees equivalent decimal value	U1211	U1210	U1110
9.9% SLOW	27B	3195 (N = 900)	1100	0111	1011
0.0%	218	3096 (N = 1000)	1100	0001	1000
9.9% FAST	1B5	2997 (N = 1100)	1011	1011	0101

The Coarse Steering Circuit consists of a phase detector using two D-type flip-flops, (U1121A and U1121B) and logic gate U1221A, followed by a phase-slip gate (U1130A, U1130B, and U1221C). The steering pulses from U1121A and U1121B are used to tune the Main VCO to the correct harmonic at 100 kHz.

When the reference clock signal on pin 3 of U1121A and the clock signal from the Programmable Divider are equal to 10 kHz and in phase, the loop is balanced. The output of U1221C (pin 10) is high with Main Loop Out of Lock Indicator, DS1130, cut off. The high level on the anode of CR1231 also cuts off diodes CR1030 and CR1031 (schematic 12) and no steering pulses are transmitted to the Loop Filter circuit.

Note that U1130A is clocked by the 10 kHz signal from the Programmable Divider and that U1130B is clocked by the 10 kHz reference signal. When there is no phase difference, U1121A and U1121B are clocked at the same instant and immediately reset through U1221A. U1130A and U1130B are also clocked at the same time. This establishes a low level on pin 5 of U1130A and pin 9 of U1130B. With a low level clocked through U1130A and U1130B, pins 8 and 9 of U1221C are normally low with its output high, cutting off Q1230 and DS1130.

When the phase of the signal from the Programmable Divider is lagging the reference signal phase, U1121A and U1130B are clocked ahead of U1121B and U1130A. Pin 1 of U1121A goes high and pin 2 goes low before pin 12 of U1121B. Later, when U1121B and U1130A are clocked by the lower frequency signal, the high level on pin 5 of U1130A is transferred to pin 8 of U1221C, causing its output to go low. At the same time, pin 12 of U1121B goes low to reset U1121A and U1121B through U1221A.

As long as the clock signal from the Programmable Divider lags the reference signal, the positive steering pulse on pin 1 of U1121A has a longer duration than the negative steering pulse on pin 12 of U1121B. For a leading phase, the conditions are reversed and pin 9 of U1221C is set to a high level by the 10 kHz reference signal. For either a lagging or leading phase, the output of U1221C goes low to turn on Q1230, illuminate DS1130, and turn off CR1231 and CR1230. Positive steering pulses are injected into the Loop Filter circuit via CR1031 (schematic 12); negative steering pulses are injected via CR1030. Positive steering pulses correspond to the Programmable Divider signal lagging the reference; negative pulses correspond to a leading phase.

When Q1230 turns on to illuminate DS1130 for an out-of-lock condition, a high level is transmitted through CR1232 on the steering board (schematic 11) and CR1232 on the Main PLL board (schematic 12). This signal holds off the sampling pulses from the 1 MHz Reference Oscillator to the Sampling Phase Gate.

Main VCO Divider 

The Main VCO Divider, U1410A and U1410B, provides two isolated 50 MHz outputs for use in the slewed edge generator circuits. These signals are plus or minus the percent timing error. The outputs are kept in phase by connecting both D inputs (pins 7 and 10) to the same output (pin 14). Since the outputs from U1410B are double-ended ECL levels and referenced to the switched 5 V source, balun T1401 and C1402 convert them to a single-ended output at pin 4.

TS1 Error Gates 

When the microprocessor checks the operation of the Data Registers for the Programmable Divider (U1220 and U1120, schematic 10), the Slewing Data Register (U1000 and U1100, schematic 9), and the Trigger Data Register (U1000 and U1100, schematic 8) it clocks a one-zero bit pattern into the registers without disturbing the latched data. The known bit pattern is retrieved via Q1021 (schematic 10). While loading the bit pattern, pin 4 of U1020B is held low and Q1021 is cut off. When retrieving the E4 data, pin 4 is set high and CR1030 is cut off to enable Q1021. The E4 data string is read via the PA7 port of the PIA on schematic 30 (U1701, pin 9).

Two status signals for the Main Timing Generator, E1(ROL) and E2(MOL), are interpreted from the logic states of U1030C and U1030D, respectively. The state of U1030A indicates the status of the Offset Loop.

When checking the frequency of the 1 MHz Reference Oscillator and the 10 kHz output of the Reference Divider, the microprocessor sets pin 12 of U1120 to a high level. This enables U1020D and the TS1 strobe signal is gated through to enable U1030B for the E3 counter test. For the E3 counter test, the microprocessor tests the Count Down Circuit on the Time Mark board by comparing it with the 10 kHz output from the Reference Divider.

All of the status signals, E1, E2, E3, and E4 are read via their respective data ports associated with U1701 (PIA).

TIME MARK AND TRIGGER GENERATORS

Introduction

Before reading this circuit description, refer to the block diagram discussion for the Time Mark and Trigger Genera-

tors (Block Diagram C) and the detailed circuit description for the Main Timing Generator (Block Diagram B).

Fast Marker and Fast Trigger Circuits 

By previous definition, the fast marker rates are 10, 20, 50, 100, 200, and 500 ns, plus or minus the timing error. The input to the Line Receiver, U1001, is the Main VCO signal (100 MHz = 10 ns), plus or minus the error. The output signals from U1001 (pins 7, 2, and 15) are also at a 10 ns rate, plus or minus the error.

The Fast Marker Divider consists of a four-bit counter, U1101, and its associated circuit components. The circuit is capable of divide by one (X1), divide by two (X2), divide by five (X5), and divide by ten (X10) functions.

The Fast Marker Divider circuit is enabled and disabled via Q1011. When 500 ns markers, or faster, are programmed, the A3 bit in the Marker Data Register (U1421, pin 7, schematic 16) is set to a logical one. This turns off Q1011 and CR1012 to remove the forced, disabling high level at the wired-OR junction (pin 13 of U1101A). The A3 bit also turns off Q1110 and CR1111, enabling the Sync Gates and the Fast Trigger Generator.

The Divide By 10 counter, U1102, is enabled for both slow and fast markers by the low level on pin 6; the output signal on pin 15 is the 10 MHz drive for the Count Down Circuit (schematic 14). The only time that U1102 is disabled is momentarily at start up, when U1101 and U1102 are out of synchronization.

At start up, U1101 and U1102 begin their count in arbitrary states. On the ninth count of the 100 MHz clock (pin 13), the terminal count output (pin 4) of U1102 goes low. This disables U1102 via pins 5 and 6 of the Sync Gates. On the next count of nine, pins 4 and 7 of the Sync Gates will both be high due to the ÷2 and ÷5 outputs from U1101. Pin 6 of U1102 then goes low to enable the Divide By 10 counter. At this point, the fast triggers and fast markers become coincident with the outputs of U1101 and the ninth count output from pin 4 of U1102. See Fig. 4-11.

For the 10 ns marker rate, the wired-OR junction is held low by the high levels on both set inputs (pins 5 and 11) of U1101. The high levels are due to both of the X2F and X5F data bits in the Marker Data Register (pins 4 and 5 of U1420, schematic 16) being set to logical zeros. These data bits are inverted by U1110C and U1110B, respectively. With pin 13 of U1110A held low for the X1 function, the 100 MHz signal on pin 2 of the Line Receiver, U1001, is gated through U1110A with no inversion.

When the appropriate data bit (X2F, X5F, or both) is set, U1101 divides by two for the 20 ns rate, divides by five for the 50 ns rate, or divides by ten for the 100 ns rate. The pulse train on pin 12 of U1110A has a negative pulse duration of about 5 ns. The negative pulses are gated through U1110A by the signals on pin 13. Refer to Fig. 4-12 for the waveform timing relationships for gating the 20 ns, 50 ns, and 100 ns markers through U1110A. Note that the X10 function for U1101 is the wired-OR combination of the X2 and X5 functions.

When the 200 ns or 500 ns markers are programmed, the X2F and X5F data bits are set for the X10 function of U1101 and data bit MM in the Marker Data Register (U1520, schematic 16, pin 6) is set to enable the middle marker gate (U1431C, schematic 14). When enabled, the output of U1431C is either a 2 MHz (500 ns) or 5 MHz (200 ns) signal, depending on which of the X2 or X5 data bits in register U1320 (schematic 16) is set. These signals are inverted by Q1010 and applied to the wired-OR junction. The resultant waveform on pin 3 of U1110A is either the wired-OR combination of the X10 function for U1101 and the 5 MHz signal or the wired-OR combination of the X10 function and the 2 MHz signal.

For all fast marker rates, the output of U1110A is a negative 5 ns pulse occurring at the programmed rate.

The purpose of the Fast Marker Shaper circuit, U1010A and U1010B, is to produce (at pins 14 and 15) complementary pulses of constant pulse width regardless of the input pulse repetition rate. In order to do this, the signal going to pin 10 of U1010B is inverted by U1010A and delayed about 5 ns by the RC network. The adjustment of C1011 sets the delay so that both input terminals of U1010B are both low for the proper interval, about 5 ns out of the total period.

Marker Amplifier 

Fast and slow time marks are output from the collector of Q1021. Slewed edges are output from the collector of Q1024. Time signals are routed through J1111 to the Output circuit board assembly (A7). See schematics 3 and 25.

The fast markers from the Fast Marker Shaper circuit are converted to a triangular shape by the Marker Amplifier. The Marker Amplifier has a risetime slower than the risetime of the fast marker pulses from U1010B. Slow markers, shaped by the Slow Marker Shaper circuit, are injected into the Marker Amplifier at the base of Q1021.

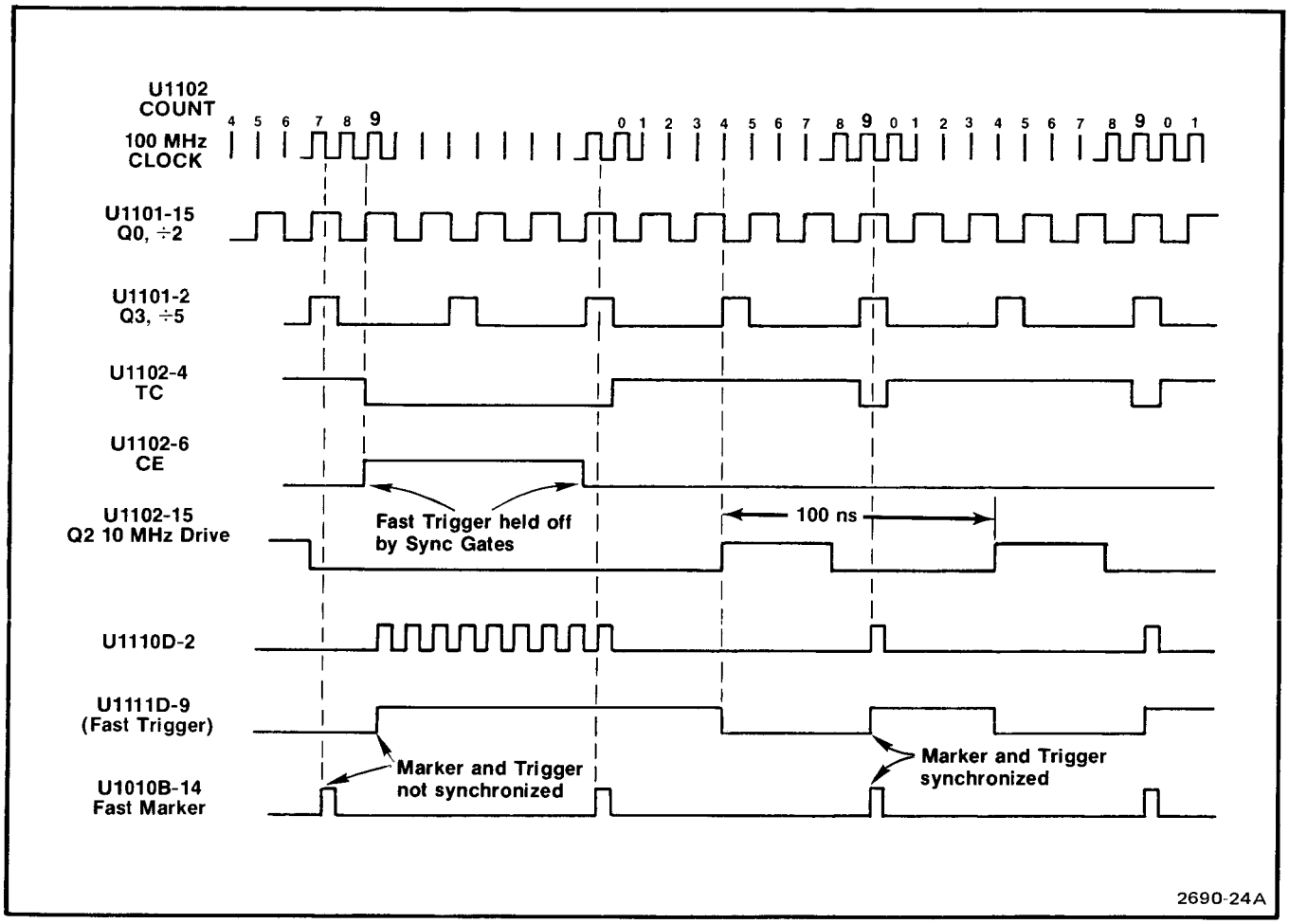


Fig. 4-11. Fast Marker Divider waveforms (100 ns markers).

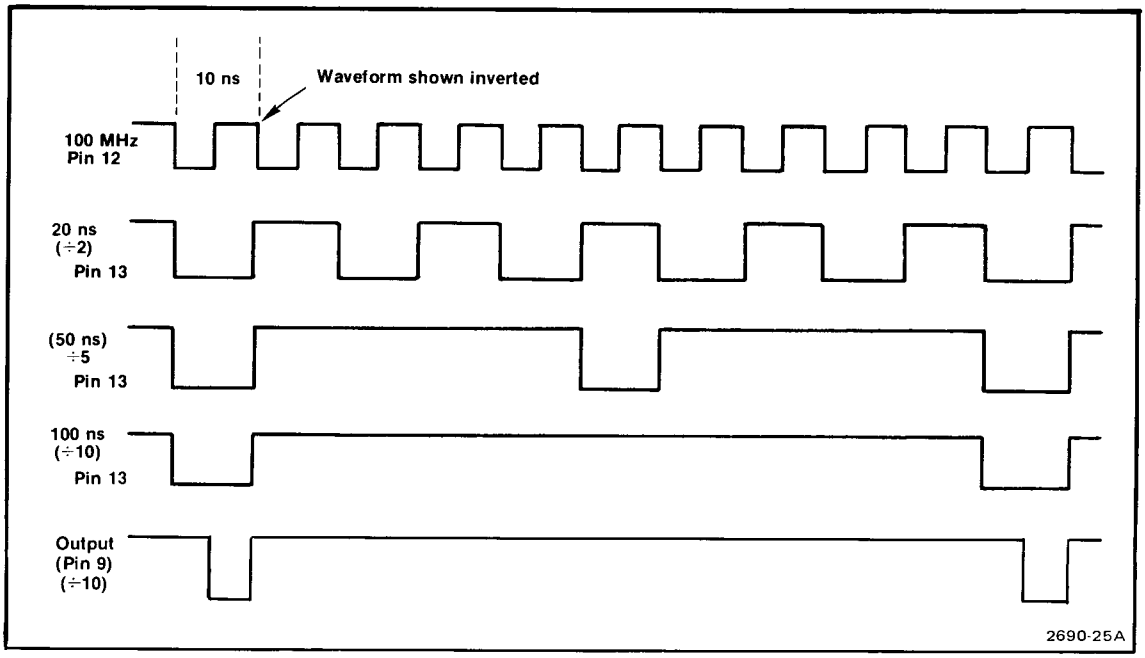


Fig. 4-12. Timing waveforms for the Fast Marker Shaper (U1110A).

When operating in the MARKERS mode, Q1131 is turned on by the MKR data bit in data register U1421 (pin 6). This turns on the current source transistors for the marker amplifier, Q1030 and Q1031.

For marker rates of 1 μs or slower, and with the MAG X10 function activated, the base of Q1133 is set low. This allows the marker BOOST gate from the Trigger Divider circuit (schematic 15) to increase the conduction of Q1031 and Q1021. The marker BOOST gate increases the amplitude of every tenth marker. When MAG X10 is programmed for basic marker rates up to, and including, 1 μs/div, the microprocessor increases the marker rate by a factor of ten and turns off Q1133.

For the SLEWED EDGE mode, Q1030 and Q1031 are cut off. Transistor Q1130 is turned on to act as a current source for Q1024 and Q1025 in the slewed edge amplifier circuit.

Count Down Circuit and 1 MHz Amplifier 

The Count Down Circuit contains the divider chain and logic components from which the slow markers are derived. The circuit is also used to provide the chopping signals for other modes that are related to the front panel FREQUENCY pushbuttons.

The 10 MHz drive signal from the Divide By 10 counter (U1102 and Q1100, schematic 13) is inverted by Q1620 before it is used to clock U1530A and U1530B. Since this signal is derived from the Main VCO, via the Line Receiver and Divide By 10 counter, it will contain the timing error. The output on pin 12 of U1530B is 5 MHz (divides by two) and the output on pin 11 is 2 MHz (divides by five).

Integrated circuit, U1430, is used to select the 1, 2, 5 sequence within a marker decade. Decade selection is performed by addressing the decade divider farther down the divider chain, U1521.

The output of U1430 is either 10 MHz, 5 MHz, or 2 MHz, depending on the settings of the X1, X2, or X5 bits in data register U1320. As previously discussed, under Fast Marker and Fast Trigger Generator circuits, logic gate U1431C is enabled only for 5 MHz and 2 MHz outputs (200 ns-500 ns fast marker gates).

A synchronizing circuit consisting of U1630 and a D-type flip-flop, U1422A, is used to eliminate jitter in the divider chain. The divider chain consists of U1531B, A, C, D, and U1521.

For slow markers equal to or slower than 10 μs, Q1530 is turned on and U1630 is enabled at pins 4 and 13 to use the complete divider chain. For this range of markers the output of U1531D will be a square wave with a period of 10 μs, 20 μs, or 50 μs, dependent on the selected output of U1430. See Fig. 4-13A.

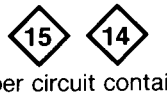
The decade divider, U1521, is addressed to select the proper decade by the A2, A1, and AØ bits on pins 12, 13, and 14, respectively. For N = 0, the decade select data from register U1421 is A2 = 0, A1 = 0, AØ = 0. The data follows the normal binary sequence up to 1, 0, 1 for N = 5.

For 10 μs markers (N = 0) the output of the synchronizing gates, U1630, will be a 5 μs signal clocking U1422A for the 10 μs markers, a 10 μs signal clocking the 20 μs markers, or a 25 μs signal clocking the 50 μs markers. The sequence of the synchronizing signals .5 μs, 10 μs, 25 μs from U1630 repeats for N = 1 through N = 5.

When 1, 2, or 5 μs markers are programmed, Q1530 is turned off to reconfigure the divider chain as shown in Fig. 4-13B. For these marker rates, U1630 is disabled at pin 13 and enabled at pin 4.

When the instrument is operating in a mode that requires the microprocessor to program the divider chain to output chopping signals, the chain is reconfigured as shown in Fig. 4-14A or Fig. 4-14B. Transistor Q1530 is cut off for the complete range of chopping signal. The 1 MHz signal from the Reference Loop (via the 1 MHz amplifier) is gated through Q1331 to U1531C and U1630. For chopping signals of 100 kHz or less, U1630 is enabled only at pin 13 and the decade divider is addressed to select the proper decade. For chopping signals of 100 kHz or less, U1321B is enabled at pin 10 and disabled at pin 12. When the fast chop signal (1 MHz) is required, U1321B is disabled completely and the output of the 1 MHz Amplifier is gated through U1321A (pin 3).

Chopping signals of 100 kHz or less are clocked through U1422A to pin 3 of U1321A by the synchronizing signal from U1630. For slow chopping signals, the microprocessor enables U1321A and pin 4.

Slow Marker Shaper 

The Slow Marker Shaper circuit contains a tracking current source, four ramp-generating capacitors, and a comparator-reset circuit.

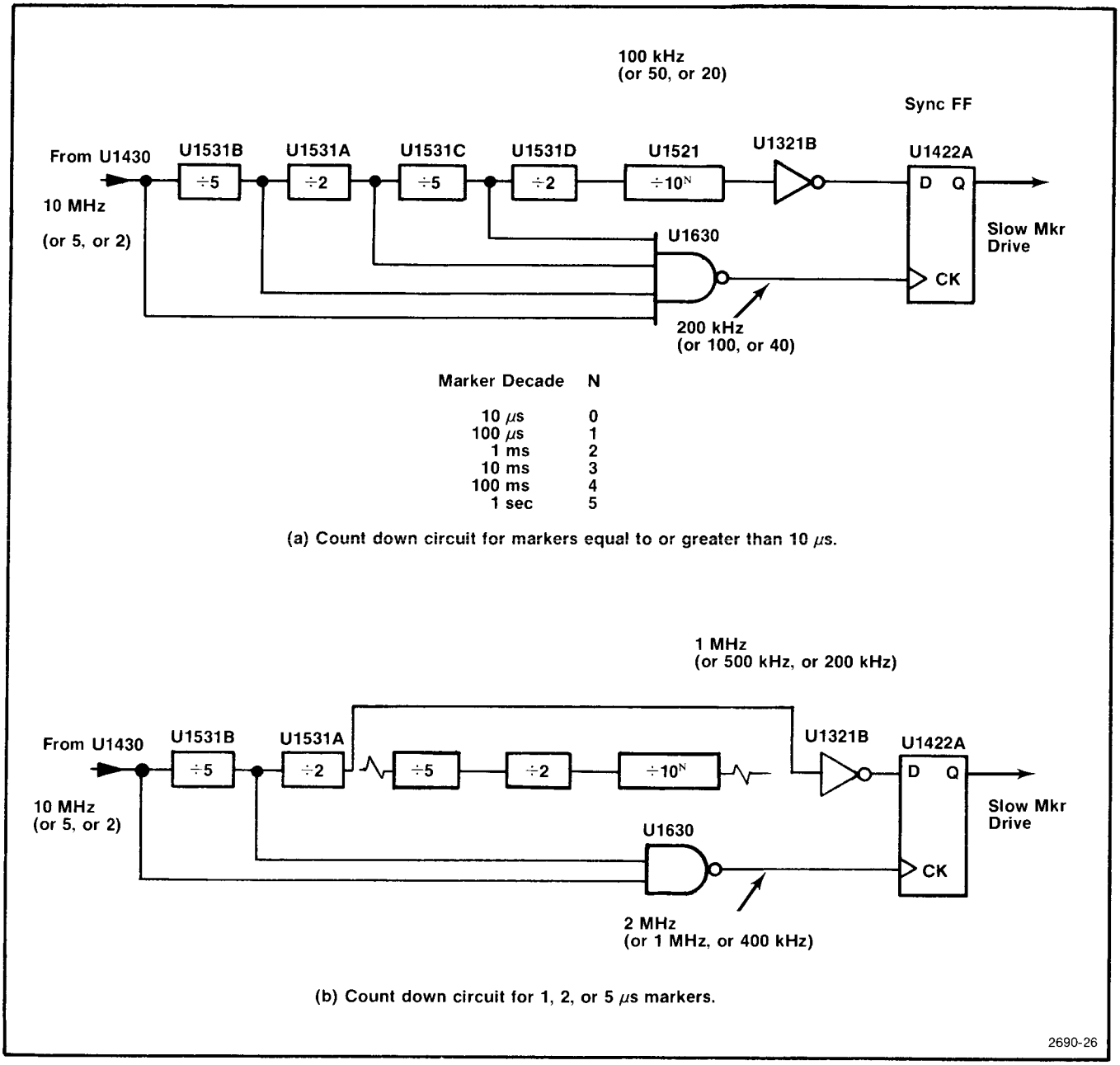


Fig. 4-13. Divider chain configurations for slow time marks.

When slow markers are programmed, the microprocessor sets a high level on pin 12 of U1422B (schematic 14). The selected marker rate then clocks U1442B to produce the square wave drive for the Slow Marker Shaper circuit. Note that the reset line for U1422B (pin 13) is connected to the output of the comparator circuit in the Slow Marker Shaper circuit (schematic 15).

Before a shaped marker is generated, the normal level at the base of Q1217 and on the gate terminal of Q1215 is close to zero volts. None of the four ramp-generating capacitors (C1212, C1213, C1214, or C1211) are considered charged and the collector of Q1314 is at a high level.

When the output of U1422B (pin 9) is clocked high to start the marker ramp, diode CR1313 is cut off and one of the selected capacitors begins to charge through CR1211 and Q1311B. A positive going ramp appears at the base of Q1217 and Q1315. When the ramp reaches the 1.7 V reference established on the base of Q1313, the collector of Q1314 goes low to reset U1422B. When U1422B is reset, CR1310 and CR1211 in the diode bridge are cut off. The

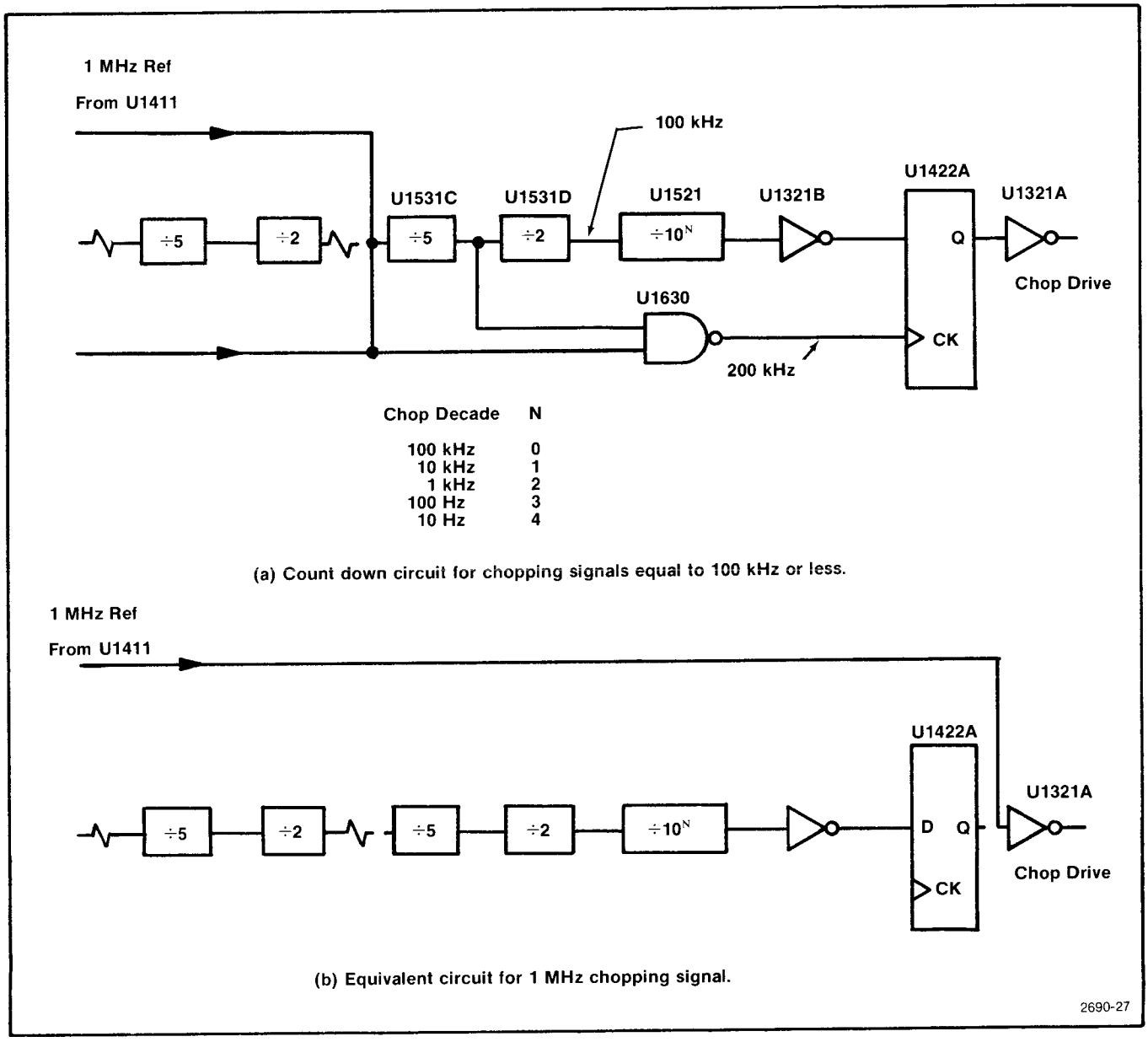


Fig. 4-14. Divider chain configurations for chopping signals.

selected capacitor now begins to discharge through CR1212 and Q1310B, generating a negative going ramp during the second half of the positive clock pulse period on pin 11 of U1422B. When the marker ramp falls below the 1.7 V reference, the collector of Q1314 goes to a high level and the circuit is ready to generate another shaped marker. Since the output of U1422B was reset to a low level during the positive clock period, the next shaped marker is not generated until the next positive transition of the clock signal (selected marker rate) from U1422A (schematic 14).

In order to maintain a relative constant duty cycle over the full range of the slow time marks, the microprocessor sets the proper data bits in register U1420 to select the proper capacitor and the available charging current in the tracking current source. The data format for U1420 is listed in Table 4-4.

Table 4-4
DATA FORMAT FOR U1420 (MARKERS MODE)

Slow Markers	X5F	X2F	Capacitor Select			Current Select		
			C3	C2	C1	I3	I2	I1
5 sec	0	0	1	0	0	0	0	0
2 sec	0	0	1	0	0	0	0	1
1 sec	0	0	1	0	0	0	1	0
.5 sec	0	0	1	0	0	0	1	1
.2 sec	0	0	1	0	0	1	0	0
.1 sec	0	0	1	0	0	1	0	1
50 ms	0	0	0	1	0	0	0	0
20 ms	0	0	0	1	0	0	0	1
10 ms	0	0	0	1	0	0	1	0
5 ms	0	0	0	1	0	0	1	1
2 ms	0	0	0	1	0	1	0	0
1 ms	0	0	0	1	0	1	0	1
.5 ms	0	0	0	0	1	0	0	0
.2 ms	0	0	0	0	1	0	0	1
.1 ms	0	0	0	0	1	0	1	0
50 μs	0	0	0	0	1	0	1	1
20 μs	0	0	0	0	1	1	0	0
10 μs	0	0	0	0	1	1	0	1
5 μs	0	0	0	0	0	0	1	1
2 μs	0	0	0	0	0	1	0	0
1 μs	0	0	0	0	0	1	0	1
Fast Markers								
.5 μs	1	1	0	0	0	0	0	0
.2 μs	1	1	0	0	0	0	0	0
.1 μs	1	1	0	0	0	0	0	0
50 ns	1	0	0	0	0	0	0	0
20 ns	0	1	0	0	0	0	0	0
10 ns	0	0	0	0	0	0	0	0
Other Modes	0	0	0	0	0	0	0	0

The available charging current is controlled by the data on pins 13, 14, and 15 of U1410. To increase the available charging current, the total input resistance to pin 3 of U1300 is decreased and U1300 responds by driving the bases of Q1311 more negative. The currents through Q1311 and Q1310 for any given marker rate are always equal. For a selected capacitor value, increasing the available charging current generates faster ramps.

Trigger Divider and Trigger Amplifier 

These circuits are controlled by data bits in registers U1320 and U1421. There are two input signals to these circuits, the slow trigger drive from U1321A (schematic 14) or the fast triggers from the Fast Trigger Generator (schematic 13).

For the MARKERS mode, the bases of Q1330 and Q1134 are set low, applying 5 V power to U1330 and disconnecting Q1134 from the Trigger Divider circuit. For the SLEWED EDGE mode, Q1330 is turned off, U1330 is disabled, Q1134 is turned on, and Q1135 is cut off. Trigger signals are then injected into the Trigger Amplifier output stage via CR1220 and CR1221. The ÷10 and ÷100 trigger functions are not applicable to the SLEWED EDGE mode (one trigger per slewed edge).

The output stage (differential pair Q1221 and Q1220) obtains its power via the constant current source consisting of U1232 and Q1333. The reference level for the current source is at the junction of R1334 and R1335.

Decade counters, U1231 (RATE ÷10) and U1230 (RATE ÷100), are programmed according to the data format listed in Table 4-5. When Q1134 is turned off for the MARKERS mode, the ripple carry output (pin 15) of the counters is free to change states on the proper count of the clock signal on pin 2. Each counter is hardwired (preset) for a count of nine. Setting up a low level (binary 0) on the load inputs (pin 9) disables the counters. For NORMAL triggers and the MAG X10 function off, both counters are disabled. Table 4-5 shows which counter is enabled for the MAG X10 function.

When U1231 is enabled for the RATE ÷10 function (pin 9 high), it holds its ripple carry output low while counting nine clock edges. With pin 15 low, CR1231 is on, holding the base of Q1135 low, and diverting current from the differential output stage for a period of nine trigger pulses. On the tenth clock edge, pin 15 of U1231 goes high, cutting off CR1231 and Q1135. This allows the constant current source to supply current to the output stage for the tenth trigger pulse to be output to the front panel.

Table 4-5
DATA FORMAT FOR U1231 and U1230
(TRIGGER RATES)

Trigger Rates	MAG X10 OFF		
	T_O	T_A	T_B
NORMAL	1	0	0
RATE ÷10	1	1	0
RATE ÷100	1	1	1
OFF	0	X	X
	MAG X10 ON		
NORMAL	1	1	0
RATE ÷10	1	1	1
RATE ÷100	Not Available		
OFF	0	X	X

The RATE ÷100 counter, U1230, operates in a similar manner, except that its ripple carry output goes high on the 100th clock edge to cut off CR1230 and Q1135, outputting the 100th trigger pulse to the front panel.

The ripple carry output from U1231 also serves as the marker boost gate for the Marker Amplifier circuit. This signal is used in the slow marker range to increase the output amplitude of every tenth marker if the MAG X10 function is activated. See Marker Amplifier description, schematic 13.

Marker Data Registers 

The microprocessor clocks these four registers (U1320, U1420, U1421, and U1520) on pin 3 when loading serial data. The data sets up the circuits on the Time Mark board (A4). The TS2 strobe (pin 1 on each register) causes the loaded data to be latched at the Q outputs. Data is loaded using four 8-bit bytes, one byte for each register.

All of the 32 control lines from the four registers have been previously discussed under specific circuit descriptions. The descriptions included all of the schematic diagrams related to the Time Mark and Trigger Generator functions shown on Block Diagram C.

Complete data format tables for the Marker Data Register are listed in the Maintenance section of this manual.

Chop Amplifier 

When chopping signals are to be used for the other operating modes associated with the front panel FREQUENCY pushbuttons, pin 5 of data register U1421 is set high to turn on Q1212 and Q1204. Transistor Q1204 acts as a current source for the balanced output stage consisting of Q1200 and Q1201.

Chopping signals from the Count Down Circuit (schematic 14) drive emitter follower Q1210. These signals are dependent on the count down divider chain configurations shown in Fig. 4-14.

Chopping signals from the Chop Amplifier go to the Chop Isolator circuit (schematic 23) and to the Head Programmer circuit (schematic 24). Both circuits are on the Output (A7) board.

SLEWED EDGE GENERATOR CIRCUITS

Introduction

Before reading this circuit description, refer to the block diagram discussion for the Slewed Edge Generator (Block Diagram C).

Offset Loop ◇6◇

The purpose of the Mixer circuit, U1100 and associated components, is to accept two input signals and produce an output signal (pins 3 and 13) equal to the difference between the two inputs. The two inputs are the Main VCO signal (f_A) at pins 10 and 11, and the Offset VCO signal (f_B) on pins 5 and 9.

The output of the Mixer is filtered by C1102, L1210, L1212, C1104 and terminated by R1210. The output of the filter is applied, through Q1114 and Q1118, to the Offset Loop Phase Detector (U1220B, pin 5) and to an out-of-range detector, U1030B, in the Acquisition Circuit.

The phase-frequency error signal at the base of Q1030 is normally near zero when the loop is locked. Transistor Q1030 is cut off and the output of the lock-up multivibrator, pin 3 of U1130A, is normally high.

The Offset VCO also outputs a signal from Q1002 to the Offset Divider circuit, U1002 and U1000. The complete Offset Divider circuit divides the Offset VCO signal by 40 or 50, depending on the voltage level set on pin 7 of U1000. The microprocessor sets pin 7 via pin 13 of data register U1001 (schematic 7); pin 7 will be high for division by 40 (.5 ns—.1 μs range), or low for division by 50 (.4 ns/div).

The Offset Loop Phase Detector circuit is clocked by two signals, the difference frequency (f_A—f_B) from the Mixer circuit and the output of the Offset Divider. If the Offset Loop is far from lock, there is no clock signal on pin 5 of U1220B because the difference frequency output from the Mixer is above the cutoff frequency of the Mixer filter circuit.

Pin 9 of U1220B is low, or goes low as soon as pin 12 of U1220A is clocked high by the Offset Divider signal on pin 1. When pin 12 of U1220A is clocked high, Q1030 is turned on and its collector goes low to turn on the Offset Out of Lock Indicator, DS1142. This action also grounds pins 4 and 5 of U1130B through R1242, starting the multivibrator. Pin 3 of U1130A (normally high) goes low when the multivibrator starts. This pulls down on pin 2 of U1030A, forcing the output (pin 1, TUNE) to its high limit. When the multivibrator completes one cycle, the input to U1030A is released.

When the multivibrator releases the input to U1030A, the current to the Loop Filter is supplied by the out-of-range detector, U1030B. The output of U1030B is high as long as the difference frequency is above the cutoff of the low pass filter circuit, L1020 and C1016.

The high level output from U1030B causes the output of U1030A to ramp downward. The negative ramp causes the output frequency of the Offset VCO (f_B) to increase until the difference frequency is able to start clocking U1220B.

As soon as the difference frequency is below the cutoff frequency determined by L1020 and C1016, the rectified signal level on pin 6 of U1030B drives pin 7 full low, reverse biasing CR1140 and allowing the Offset Loop Phase Detector circuit to be the only source controlling the TUNE voltage for the Offset VCO. When lock up is reached, the predominately low level signal on pins 9 and 12 of U1220 (filtered by C1132) is not enough to keep Q1030 turned on. The Offset Loop Out of Lock Indicator is then turned off and the lock up multivibrator is prevented from starting another cycle.

Integrated circuits, U1130C and U1230, operate to delay the reset pulse to pins 2 and 6 of U1220. This delay is used to linearize the phase detector response around the zero-phase difference point (loop null).

Trigger and Slewing Counters, Generators and Slewing Control Circuits ◇7◇◇8◇◇9◇

The Trigger Counter and Slewed Edge Counter are identical synchronous counters, which generate an output after a programmed number of clock inputs. The Trigger Counter is located on the A3A4 circuit boad, schematic 7; the Slewed Edge Counter is on the A3A5 circuit board, schematic 8.

Each counter consists of two 4-bit binary counters U1010 and U1110, one flip-flop U1210B, and appropriate gating. The terminal state of the counter (all ones) is detected by gate U1112B, whose output goes low at the terminal count. That low activates the Preset Enable (PE) inputs of U1010 and U1110 (pin 5), which causes the next clock pulse to load the data present at data inputs P0 through P3 (pins 7, 9, 10, and 11). When the data is loaded, the Preset Enable inputs return to the high state, and counting begins again with the next clock pulse.

The numbers stored in the Data Registers, U1000 and U1100, determine the length of the count and hence the time between outputs. The "shift" count is stored in U1000 and the "slewing" count in U1100. The tri-state outputs of the registers are bussed together, so that their Enable inputs (pin 15) determine which data is presented to the counter. The "shift" count is switched in for timing the first edge; then the "slewing" count is enabled for the remaining 14 edges of the slewed-edge pattern.

Flip-flop U1210A generates the output signal (Trigger Generator or Slewed Edge Generator). The flip-flop is reset low during a counting cycle by gate U1200B, which detects a counter state occurring 95 clock periods (1.9 μs) before the terminal count. Integrated circuit U1210A is toggled high on pin 9 by the first clock pulse after gate U1112B activates its CE (Clock Enable) input (pin 6), which occurs at the terminal state of the counter.

The Slewing Control circuit on the A3A2 circuit board (schematic 7), starts the counters at the proper time and provides the enabling signals to switch from "shift" to "slewing" counts. After the complete pattern of 15 edges has been generated, the Slewing Control circuit stops the counters to resynchronize them for repeating the sequence.

In the Slewing Control circuit, flip-flops U1012B and U1012A provide RUN control signals to the Trigger and Slewing Counter. The edge counter, U1011, determines when the last edge in the slewed edge pattern has been generated; the pattern is then repeated.

Initially, both flip-flops, U1012B and U1012A, are in the low state. Pins 3 and 14 are both high, disabling both Trigger and Slewing counter. The edge counter, U1011, is being held in the preset condition by the high level at its PE (Preset Enable) input (pin 1).

Synchronizing pulses (pin 9 of U1012B) from the Offset Divider (A3A6 circuit board, schematic 6) occur each time the Main VCO 50 MHz clock and the Offset Clock are phase coincident. This event occurs at 820 ns intervals. With the circuit in its initial state as described above, a sync pulse occurs, toggling both U1012A and U1012B to the high state. This enables both the Trigger and Slewing counters via the T-RUN and S-RUN signal lines. Both lines go low at the same time.

Both counters (schematics 8 and 9) then begin counting their respective clocks. At the counter state for which all inputs to AND gates U1200D and U1200C become high, the output of U1200B resets the output flip-flop U1210A. The output of U1200B in the Trigger Counter also clocks the edge counter, U1011 (Slewing Control Circuit), via the Edge Counter Clock line (P1207-3). When the Trigger Counter reaches its terminal count (all ones), the output of the terminal count gate U1112B drops low, enabling the PE (Preset Enable) inputs of the counters and the CE (Clock Enable) input of Trigger Generator U1210A. Then, the next clock pulse loads the counter, and clocks U1210A high, generating the trigger output (pins 2 and 3). The presetting of the counters causes gate U1112B output to return high, and counting begins again upward from the preset state. This continues, generating a trigger output for each programmed number of trigger clock pulses.

Similarly, the Slewing Counter and Slewed Edge Generator generates a slewed edge output for each programmed number of offset clock pulses.

The process repeats, generating a trigger and an edge for each counting cycle until the edge counter (Slewing Control circuit) counts down to zero, causing its CO (Carry Out) output, pin 7, to go low. This sets up the circuits to stop the counters as soon as they generate their next outputs, and to load the shift counts in preparation for starting the pattern over.

This is accomplished as follows. The low at the CO output of the Edge Counter switches the Slew Enable line (P1300-7) low and the Shift Enable line (P1300-6) high. This changes the data presented to the counter data inputs from the slewing count to the shift counter. The low level on the Slew Enable line enables gate U1112C (Trigger and Slewing Counters). When the Trigger Counter reaches terminal count, the next clock pulse loads the counter with the shift count and generates a trigger output from U1210A. The negative going output at U1210A, pin 3, passes through the now-open gate U1112C, becoming a positive pulse at the gate output. This pulse resets flip-flop U1012B (Slewing Control circuit) via the T-RESET line. This sets the T-RUN line high, stopping the Trigger Counter.

The Trigger Counter is now idle, having just been loaded with the shift count, and is ready to begin a new sequence. The sync pulses cannot clock flip-flop U1012B high now because the CO (Carry Out) output of the edge counter, U1011, is low. This holds both flip-flops, U1012A and U1012B, inputs (pins 7 and 10) high through Q1103.

Similarly, when the Slewing Counter reaches its terminal count, it generates the last edge of the slewed edge pattern, resetting flip-flop U1012A in the Slewing Control Circuit through the S-RESET line. This, in turn, stops the Slewing Counter by setting the S-RUN line high.

When U1012A sets S-RUN high with its output on pin 3, pin 2 goes low. This turns on Q1114, which presets the edge counter, U1011, to the programmed number of edges per pattern (normally 15) stored in data register U1001. As soon as the preset is effective, the CO output (pin 7) goes high, turning on Q1103. Both control flip-flops, U1012A and U1012B, are then enabled by setting their inputs (pins 7 and 10) low. The next sync pulse on pin 9 can now set them both high, beginning the entire sequence again.

STANDARD AMPLITUDE CALIBRATOR CIRCUITS

Introduction

Before reading this circuit description, refer to the block diagram discussion for the Standard Amplitude Calibrator (Block Diagram D).

+5 V Regulator and Pre-regulators ◇18

Integrated circuit U1011 is the gain element, reference generator, and current limit sense for the +5 V supply. Feedback comes from the +5 V sense line (P1411-6A) which is connected to the Steering circuit board (A3A6, schematic 10). The reference for the +5 V supply is generated inside U1011 and is accessed at pin 6. The voltage on pin 6 is then divided by R1001, R1002, and R1004 to supply the reference voltage for the internal operational amplifiers (pin 5, U1011). The +5 V supply is adjusted by R1004.

Power for the internal operational amplifiers (U1011, pin 12) is derived from the +33.5 V unregulated source in the power module. The unregulated +11.5 V from the power module provides the collector voltage for a transistor internal to U1011 and a relay strobe circuit on the Output board (schematic 25). Frequency compensation for the +5 V regulator is provided by C1002.

Transistor Q1021 and the npn series pass transistor in the power module form a Darlington circuit, with Q1021 providing increased gain to drive the series pass element. In normal operation both of these transistors are conducting, with about 120 mA through Q1021. Should the load current exceed about 2.5 A, the voltage drop across R1022 becomes great enough to turn on a transistor internal to U1011. This action reduces the voltage on the base of Q1021 and the driving voltage to the series pass transistor; thereby limiting the load current.

Overvoltage protection for the +5 V supply is provided by VR1041, Q1041, and CR1041. If the +5 V supply exceeds about 6.6 V, a 1 V level across R1041 turns on Q1041 and CR1041. This action essentially grounds the +11.5 V and +33.5 V sources in the power module and causes both fuses (F1041 and F1141) to open.

Integrated circuits U1113 and U1121 operate as Preregulators for the HV and LV Power Supplies (schematic 19), respectively.

The low voltage regulator, U1121, is enabled for all amplitude modes and ranges, while the high voltage regulator, U1113, is enabled whenever the CG 5001/CG 551AP requires an output amplitude of 12 V or greater in the VOLTAGE mode, or whenever the output amplitude in the EDGE mode is 20 V or greater. When required, the Preregulators are disabled by setting a low level on pin 13 (via Q1111 or Q1011). The microprocessor sends data to U1121 (schematic 20) to enable the Preregulators.

The high voltage preregulator, U1113, along with Q501, operates to maintain about a 20 V level at the input to the HV Power Supply (TP1104). This level is referenced to chassis ground; the regulator does not sense the output of the floating HV Power Supply. Potentiometer R1106 is adjusted to set +237 V at the output of the HV Power Supply (TP1702, schematic 19).

Resistor R1113 is the load current sensing resistor for the HV Power Supply. If the load current exceeds about 330 mA, the voltage drop across R1113 activates the internal circuits of U1113 to reduce the base drive to Q501; thereby limiting the load current.

Overvoltage protection for the high voltage regulator (U1113) is provided by VR1043 and Q1041. If the voltage level at TP1104 exceeds about 25 V, Q1041 is turned on by the voltage drop across R1041. This action also causes both fuses (F1141 and F1041) to open, disconnecting the +33.5 V and +11.5 V power sources. Fuse F1041 opens due to grounding the cathode of CR1041 through Q1041.

The low voltage preregulator, U1121, has a feedback path for sensing the output of the LV Power Supply. The floating +15 V potential is fed back to the voltage divider network consisting of R1101, R1104, and R1103. Potentiometer R1104 is adjusted for a regulated +15 V output from the LV Power Supply (TP1103, schematic 19). The output of the preregulator (junction of R1131 and R1121) may vary from +12 V to +18 V, depending on load conditions.

The 7 V reference from U1121 (pin 6) is divided down by R1132 and R1133 to set an open circuit level of about 3.5 V on pin 5 of U1121. This voltage is used to power up the LV supply and sets the minimum voltage supplied. After powerup, the voltage level on pin 5 of U1121 is controlled by U1111 and U1112. For an open circuit condition (power supply disconnected) the output of the regulator is about 12 V. The collector of the transistor in the optical isolator, U1112, is held constant by the 15 V Zener diode, VR1141. Zener diode VR1101 sets the 6.4 V reference for the comparator circuit, U1111.

If the +15 V floating supply drops below +15 V, pin 6 of U1111 goes more positive with respect to the floating sup-

ply and increases the current through optical isolator U1112. This causes pin 5 of U1121 to go more positive and increase the output voltage at pin 3. If the floating supply goes above +15 V, the drive to U1112 is decreased by U1111 and the output at pin 3 of U1121 decreases.

Resistor R1121 is the current limiting resistor for the LV Power Supply. A current limit of about 600 mA through R1121 turns on a transistor internal to U1121. This reduces the base drive to Q1031 and the pnp series pass transistor in the power module, limiting the load current.

Overvoltage protection is provided by VR1042 and Q1041. If the low voltage regulator output exceeds about 25 V, VR1042 turns on and the 1 V level across R1041 turns on Q1041 and CR1041. If this happens, both fuses (F1141 and F1041) open, disconnecting the +11.5 V and +33.5 V sources in the power module from the Preregulators.

LV and HV Power Supplies 

The outputs of the high and low voltage Preregulators are connected to four feedthrough capacitors on the shield can for the Power Supply Isolator board (A5A1). These capacitors are C541, C542, C552, and C551. Transformer T1010 operates as a common mode filter for both outputs from the Preregulators. Zener diode VR1021 developes a +9 V source for the CMOS devices in both the LV and HV Power Supplies; U1000, U1020, U1010, and U1011.

The LV and HV Power Supplies operate as dc to dc converters, accepting their respective dc inputs at the center taps of transformers T1210 and T1230. An ac voltage is developed across the secondary of each transformer by alternately grounding each end of the primary windings. The primary windings are individually grounded by turning on Q1120 or Q1220 for the LV Power Supply, and turning on Q1110 or Q1210 for the HV Power Supply. The rate at which the primary windings are switched to floating ground is determined by the output switching frequencies of U1010A and U1010B. Integrated circuit U1010B is clocked by the output signal on pin 1 of U1010A which, in turn, is clocked by an oscillator signal from U1000.

The oscillator signal from U1000 (pin 3) is about 200 kHz with a duty cycle of about 60—65%. Integrated circuit U1010A divides this signal by two to develop a 100 kHz switching waveform (50% duty cycle) for Q1120 and Q1220. The output of U1010A is again divided by two to develop a 50 kHz switching waveform (50% duty cycle) for Q1110 and Q1210.

Transistor Q1020 and its associated components operate as a voltage-lockup protection circuit for the primary supply switching components. If the oscillator, U1000, fails to start or the signal on pin 3 of U1000 is absent, the +9 V source applies a high level to the set and reset inputs of U1010A and U1010B. This sets all outputs from the D-type flip-flops to a high level, cutting off all four switching transistors in the primary windings of T1210 and T1230.

Both power supplies contain simple bridge rectifiers, three-pole filters, and common mode filters in the secondary windings of their respective power transformers. The floating dc power developed by these isolated supplies is brought back onto the Power Supply Main board (A5) via eight feedthrough capacitors. The HV Power Supply develops two 120 V voltage sources from two secondary windings for application to the HV Switching circuit.

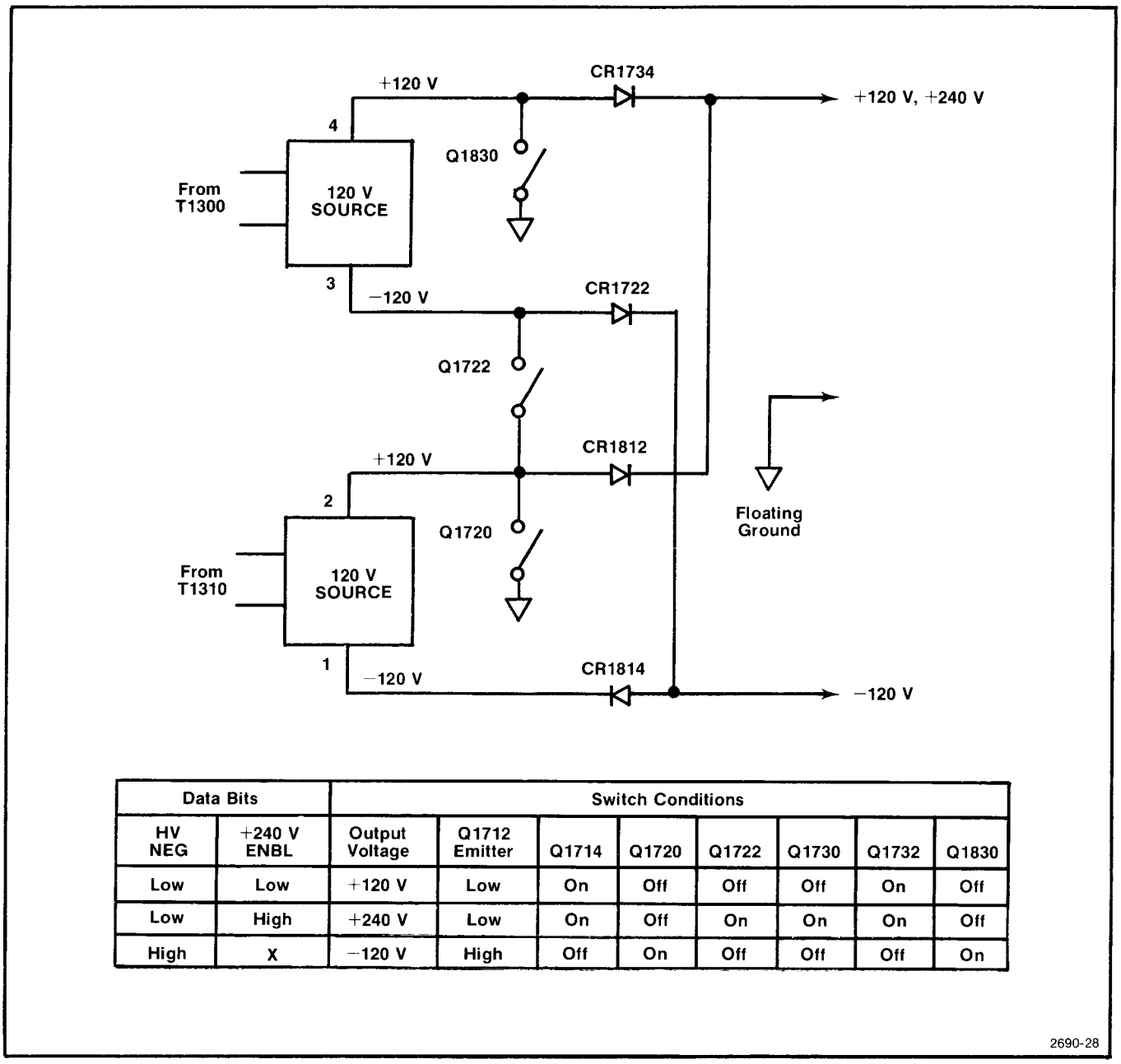
HV Switching 

The HV Switching circuit outputs three separate dc voltages. These voltages are +120 V or +240 V to the Reference board (A6) and −120 V to the High Edge board (A8) circuits. The selection of one of the three voltages is determined by the microprocessor sending data to U1341 (schematic 20) and setting the proper voltage levels on the bases of Q1712 and Q1730. A simplified diagram and switch condition code chart for the HV Switching circuit is shown in Fig. 4-15.

For +240 V output the voltage sources are stacked; Q1714 and Q1722 are on, Q1830 is off. With Q1714 on, the minus side of the lower voltage source is connected to floating ground, and load current passes through CR1734.

For +120 V output the lower voltage source is used; Q1714 is on, grounding the minus side of this source, Q1722 is off to disconnect the return path for the upper voltage source, Q1720 is off, and load current passes through CR1812.

For −120 V output both voltage sources are used; Q1714 is off to disconnect the minus side of the lower voltage source from ground, Q1830 is turned on to connect the plus side of the upper voltage source to ground, Q1720 is on to ground the plus side of the lower supply, Q1722 is off, and load current passes through CR1722 an CR1814.



Data Bits		Switch Conditions							
HV NEG	+240 V ENBL	Output Voltage	Q1712 Emitter	Q1714	Q1720	Q1722	Q1730	Q1732	Q1830
Low	Low	+120 V	Low	On	Off	Off	Off	On	Off
Low	High	+240 V	Low	On	Off	On	On	On	Off
High	X	−120 V	High	Off	On	Off	Off	Off	On

Fig. 4-15. Simplified diagram for the HV Switching circuit.

Data Registers and Data Isolators 20 21

The microprocessor sends data to the Reference Data Register, U1121, and to the Floating Data Registers, U1242, U1341, U1541, and U1841 to set up the Standard Amplitude Calibrator circuits for the desired operation in the amplitude modes.

Data on pin 2 of each register is shifted serially through these registers on the positive clock transitions on pin 3 of each register. The data in each stage is transferred to an internal storage register when the strobe inputs on pin 1 of each register goes high. Data in the storage registers appear at the parallel outputs when they are enabled by a high level on pin 15 of each register. Any time the registers are disabled by pin 15 being low, the parallel outputs go to a high impedance state. The serial data outputs from each register appears on pin 10.

It is undesirable to allow the HV ENBL (pin 4) line or the LV ENBL (pin 5) line of U1121 to operate and enable the power supply Preregulators (schematic 18) before the microprocessor has completed its initialization routine. Therefore, the Reference Data Register, U1121, is provided

with a lock-out circuit made up of U1123A, R1121, C1121, R1011, and R1012.

At power up, the high level on pin 10 of U1123A resets U1123A and holds pin 15 of U1121 low. The two pull-up resistors, R1011 and R1012, hold the LV ENBL and HV ENBL lines at a high level until C1121 is fully charged. The parallel outputs from U1121 are then enabled when the microprocessor next sends the VS1 strobe to the Reference board.

The floating ground system for the Floating Data Register is separated from the chassis ground system of the Reference Data Register by the Data Isolator circuits. Serial data is sent via Q1041 and T1042, while the strobe and clock signals are sent via Q1141-T1041 and Q1241-T1241, respectively. Transistor pair, Q1143 and Q1142, reshape the data pulses before application to U1242.

Programmable Voltage Reference 

The Programmable Voltage Reference basically contains a digital-to-analog converter, U1241; two amplifiers, U1332 and U1331; and a precision voltage source, U1432.

Integrated circuit U1241 is a R, 2R resistive ladder network whose output current from pin 1 is dependent on the binary bit pattern set on pins 4 through 13. Integrated circuit U1332 operates as a current to voltage converter, using a feedback resistor internal to U1241. Resistors R1231 and R1234 set the current drive to U1331.

The complete circuit is an operational amplifier circuit where U1241 acts as a programmable feedback element (R_f) connected between pins 6 and 2 of the main amplifier (U1331, Q1431, and associated components). Resistors R1331 and R1232 act as the input element (R_i) for the operational amplifier. The input element is driven by a precision 10 V voltage source, U1432.

The voltage reference set on TP1304 is equivalent to $V_o = -5\ V\ [1/(1 + x)]$. The value for x includes the indicated percent error variable, a calibration factor, and a calculated correction factor. The microprocessor performs the necessary calculations and then loads U1242 and U1341 to latch the required 10-bit binary pattern on the inputs to U1241.

Potentiometer R1324 sets the DAC gain and R1325 adjusts the DAC offset. Resistors R1435 and R1431 improve the circuits temperature stability.

Precision Divider and Level Translator 

The Precision Divider, U1531, is programmed by latched data in register U1541 (pins 5, 6, 7). The data selects one of eight voltage levels from the precision resistive network connected to input pins 0 through 7 of U1531. The input voltage to the divider is the output of the Programmable Voltage Reference. The microprocessor programs a negative voltage level on pin 3 of U1531 according to commands from the NUMBER OF DIVISIONS (MULTIPLIER) pushbuttons and the UNITS/DIV control.

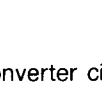
The Level Translator, U1631 and associated components, changes the reference level from floating ground to −25 V dc and multiplies the input level on pin 3 of U1631 by two or four. The output voltage from the Level Translator circuit is developed across R1642.

Integrated circuit U1631 and field-effect transistor Q1645 operate as a current source for the resistive divider composed of R1642, R1641, and R1541. It is the ratio of R1642 to R1541 or the sum of R1541 and R1641 that determines whether the input to the Level Translator is multiplied by four or two.

If the data bit level on pin 4 of U1541 is low, Q1631 turns on, which turns on Q1641 and Q1640. When Q1642 turns on, Q1541 turns off. Feedback to U1631 is then through Q1641 with Q1640 shorting out R1641. This causes the circuit to multiply by four.

If the data bit level is high, Q1631 is off, which turns off Q1642, Q1641, and Q1640. When Q1642 turns off, Q1541 turns on. Feedback to U1631 is then through Q1541 and R1641 is not shorted out. This causes the circuit to multiply by two.

Multiplication by two (2X) is the normal mode when the CG 5001/CG 551AP is driving a high impedance load. Multiplication by four is only necessary when driving a 50 Ω load. The 5 V level from the Precision Divider is never multiplied by four for any load.

Voltage-to-Current Converter 

The purpose of the Voltage-to-Current Converter circuit is to accept a variable voltage source on pin 3 of U1632 and generate an accurate current to one of five possible outputs. This circuit contains two digitally controlled switching circuits that operate independently of each other to select the proper current and the correct output.

Field-effect transistors, Q1733, Q1831, Q1832, Q1731, and Q1732, operate as current sources for their respective outputs. The current setting resistors for the converter are R1644, R1645, R1646, and R1647. Combinations of these resistors are switched into the path of the current sources according to latched data in registers U1841 (pins 4 through 6) and U1541 (pin 11).

The data lines are named according to the value of the current flowing through the current setting resistors. When Q1741 is turned on the current is at a minimum. When Q1745 is turned on the current is at a maximum.

The current sources are enabled via their respective transistor switch according to the signal nomenclature on the data lines from U1841.

The current is controlled by U1632 setting the voltage across the current setting resistors and pulling any excess current from the gate node of the selected transistor through one of five diodes associated with that node.

SAC Chopper and Chop Isolator 

The SAC Chopper circuit on schematic 21 is composed of Q1521, Q1522 and associated components. This circuit is enabled when the SAC Chop Enable bit in data register U1341-7 (schematic 20) is set low.

The chopping signal, selected by one of the front panel FREQUENCY buttons, is derived from the Count Down Circuit on schematic 14. It then passes through the Chop Amplifier (schematic 16) and the Chop Isolator circuit (schematic 23) before being applied to the base of Q1522.

Only two of the reference current sources, Q1733 or Q1832, are chopped by the square wave signal on the collector of Q1521. These current sources are the inputs to the Low SAC and High SAC circuits on schematic 22. The chopping signal is amplitude limited by diode pairs, CR1525-CR1526 and CR1523-CR1527.

Transistors Q1521 and Q1522 form a current switch. When the SAC Chop line is high, Q1521 is on and Q1522 is off. Current is diverted from the inputs of the Low SAC and High SAC circuits through diodes CR1524 and CR1422. When the SAC Chop is low, Q1521 is off and Q1522 is on. Reference current is then sent to the Low SAC and High SAC amplifiers. The voltage across R1621 is used to chop the Current Amplifier.

The Chop Isolator circuit (schematic 23) operates as a Schmitt amplifier circuit, outputting differential square wave signals at the collectors of Q1505 and Q1504. Transistor Q1406 operates as a current source, with its base reference voltage set by a voltage divider, R1401 and R1403. The square-wave signal for the SAC Chopper is derived from the collector of Q1507.

Low SAC and High SAC 

The Low SAC circuit accepts a selected chopped current input on pin 2 of U1211 and converts it to an accurate voltage output at TP1200. The calibrated output voltage range is from 100 mV to 10 V.

The Low SAC operates as a negative feedback amplifier circuit with R1201 acting as the feedback resistor and R1111 (in the SAC Switching circuit) acting as a partial load resistor in series with the external load. Transistors Q1312, Q1311, Q1321, Q1212, and Q1421 operate to provide a small amount of gain and the buffering necessary to drive a 50 Ω load.

Transistors Q1322 and Q1221 are normally off. If the output current exceeds about 220 mA (external load shorted to ground), the voltage increases across R1323 and R1210, turning on Q1322 and Q1221 to limit the output current.

Integrated circuit U1211 is a fast amplifier that uses an accurate amplifier, U1311, to compensate for input offset voltage drift. Potentiometer R1203 is used to adjust the Low SAC Offset while C1201 is used to adjust the overshoot on the Low SAC output waveform.

The input current to pin 3 of U1311 is not chopped. This input to the Low SAC is used only to apply −10 V dc level to the Head Programmer circuit on schematic 26. The input is enabled via Q1831 (schematic 21) if the Pulse Head accessory is attached to the CG 5001/CG 551AP.

The High SAC circuit accepts a chopped current input to pin 2 of U1411 and converts it to an output voltage in the 12 V to 200 V range at TP1401. Transistors Q1510 and Q1412 are the High SAC output transistors, while Q1512 and Q1514 operate only as buffers. Biasing diodes, CR1521 and CR1522 ensure that the buffers are always on and conducting. The positive high voltage supply for the High SAC circuit is enabled via the HV Switching circuit on schematic 19 (previously discussed).

The High SAC operates as a negative feedback amplifier (similar to the Low SAC) with R1312 acting as the feedback resistor. The normal maximum output from the High SAC is 10 mA at 200 V. If the output current exceeds about 12 mA, the voltage increase across R1404 turns on Q1411 and turns off Q1510, limiting the current.

Potentiometer R1411 is used to adjust the High SAC Offset, while C1401 is used to adjust the overshoot on the High SAC output waveform.

Current Amplifier and Chopper 

The Current Amplifier circuit operates as a precision current source with an operational amplifier configuration. The output current is in the 1 mA to 100 mA range. The output current is chopped by the Chopper circuit consisting of Q1701 and Q1702.

Integrated circuit U1611 acts as a preamplifier for U1612, and Q1711 operates as the output transistor of the Current Amplifier. Field-effect transistors, Q1612 and Q1611, operate to divert any base leakage current in Q1711 back to the output at the collector of Q1711. Resistor R1614 acts as the feedback resistor for the Current Amplifier.

This circuit converts a selected dc reference current through R1615 to a dc voltage at pin 3 of U1611 and produces an output current through Q1711 and R1616 that is ten times the input current. For example, if the selected reference current through R1615 is 10 mA it develops 2.5 V across R1615; the output current will then be 100 mA with 2.5 V developed across R1616.

To chop the output current, the Current Chop Enable bit in data register U1341-6 (schematic 20) is set low to turn off Q1537. This allows the chopping signal from the SAC Chopper (schematic 21) to drive the base of Q1701. All of the output current is then diverted through Q1702 for one-half period of the square wave chopping signal.

SAC Overload Sense and VS1 Error Gating 

The SAC Overload Sense circuit has three inputs: the Low SAC operational amplifier output through CR1624 and CR1622, the High SAC operational amplifier output through CR1623 and CR1621, and the Current Amplifier output through Q1811 and Q1821.

Integrated circuit U1621 operates as two comparator circuits. If the Low SAC or High SAC circuits exceed their current limits, the output of U1211 (pin 6) or U1411 (pin 6) will swing above 13 V. This drives pin 3 of U1621 above 12 V on the positive half cycle. If the operational amplifier limits to a negative level, it will drive pin 6 more negative than −12 V. There is no output from U1621 as long as the input levels on pins 3 and 6 do not exceed the reference levels set on pins 2 and 5, +12 V and −12 V, respectively.

If either the Low SAC or High SAC circuits are current limited, Q1621 turns on and off at the same rate as the chopping signal. When Q1621 is turned on by the first positive pulse from U1621, a trigger signal is generated via U1031 that fires the monostable multivibrator circuit, U1131A. Pin 7 of U1131A goes low and Q1121 is turned on to set a constant high level on pin 1 of U1122A, the VS1 Error Gate. When the microprocessor strobes the VS1 Error Gating circuit on pin 2 of U1122A, it senses the UNCAL condition on pin 3 and causes UNCAL to be displayed in the front panel readout.

If the voltage at the Current Amplifier output rises above 6.8 V, transistors Q1811 and Q1821 turn on to trigger the monostable multivibrator, U1131A. The microprocessor then senses the UNCAL condition for the CURRENT mode and causes UNCAL to be displayed in the front panel readout.

SAC Switching 

Relays K1101, K1111, and K1102 are enabled via their respective current drivers, Q1112, Q1111, and Q1211. Relay K1101 connects the High SAC circuit and K1111 connects the Low SAC circuit to the SAC Attenuators (schematic 25). For the CURRENT mode, K1102 connects the Current Amplifier to the SAC Attenuator and current loop relay, K1225 (schematic 25).

NOTE

Refer to the Relay State Table in the foldout pages for complete data concerning the state of all relays in the CG 5001/CG 551AP. The foldout pages are located in Volume 2.

Low Edge Generator 

The Low Edge Generator consists of two parts: a negative edge generator and a positive edge generator. The negative edge output is through CR1724 and the positive edge output is through CR1624. Negative and positive low edge aberrations are adjusted by C1721 and C1621, respectively. The Low Edge Generators develop a maximum of 1 V across an external load of 50 Ω; rise and fall times are less than 1.3 ns. The output polarity of these low amplitude edges are selected by K1739 and K1737 on schematic 25.

The Low Edge Generators are driven by identical 48 mA current sources: U1824-Q1814 for the negative edge and U1619-Q1601 for the positive edge. The 48 mA output from the collectors of Q1725 and Q1624 is shared by the respective terminating networks and the external 50 Ω load.

Before the low edge reference current source (Q1732, schematic 21) is enabled by the microprocessor, the 48 mA current sources are off and no current flows through Q1725 or Q1624. When the 1 mA reference current is enabled, the voltage drop across R1803 increases to about 1 V and turns on Q1814 to supply current for the negative edge output. Integrated circuit U1802 and field-effect transistor Q1808 operate as a voltage translator circuit. This circuit responds to the 1 V across R1803 and causes 1 V to occur across R1809 and R1618, turning on the current source for the positive edge output.

Three stages of differential amplifiers are used to speed up the edges and to chop the current through CR1724 and CR1624. The differential amplifiers are driven by the differential outputs from the Chop Isolator circuit. When Q1715 or Q1614 turn on at the selected chopping rate, all of the available current (48 mA) is diverted from the output stage, cutting off CR1724 or CR1624.

Attenuation of the 1 V low edge output signals is provided, when required, by AT1634, AT1632, and AT1630 in the Output Switching circuit (schematic 25).

Mid Edge Generator 

The Mid Edge Generator circuit provides output signals to K1434 in the Output Switching circuit (schematic 25). The output amplitudes are in the range from 1.2 V to 16 V. The output signal is a negative voltage rising to ground.

Field-effect transistors, Q1528 and Q1527, operate as switches, being turned on or off at the selected chopping rate. Transistor Q1528 switches the negative voltage level to ground to develop a positive-going edge with a risetime of 100 ns or less.

For output amplitudes in the Mid Edge range, the microprocessor programs the Voltage to Current Converter (schematic 21) for the proper reference current to be applied to the Low SAC circuit (schematic 22). The output voltage from the Low SAC circuit is used to drive the reference input to the Mid Edge Generator (pin 8B on P1511).

Integrated circuit U1412, transistor Q1413, R1422, R1421, and associated components form an operational amplifier circuit with a gain of −10. The input reference voltage level to this circuit varies from .12 V to 1.6 V. The microprocessor disables this circuit by setting a high level on the anode of CR1413. Driving pin 3 of U1412 high sets the collector of Q1413 to about −25 V. Since Q1528 is biased off, no current is drawn through the output transistors.

Resistor R1414 is the current limit sensing resistor. If the output current exceeds about 16 mA, Q1412 is turned on to protect Q1413, Q1527, and Q1528. If the circuit goes into current limit, pin 6 of U1412 rises above 6.3 V. The 0.6 V drop across R1427 then turns on Q1410 to report a Mid Edge Error when the microprocessor strobes the output of Edge Overload Sense circuit on schematic 27 (VS2 Error Gating).

The chopping signal for the Mid Edge Generator is applied to grounded base transistors, Q1516 and Q1513, to switch the output transistors. This signal is applied via Q1502 in the Chop Isolator circuit (schematic 23) when the microprocessor sets pin 13 of Data Register U1341 low (schematic 20). A low level on pin 9B of P1511 (schematic 23) does two things to enable the Mid Edge Generator; it turns off Q1407 in the Chop Isolator circuit and disconnects CR1413 from the positive input terminal of the operational amplifier in the Mid Edge Generator circuit.

Zener diode VR1422 and diode CR1424 operate to limit the voltage swing on the gate terminal of Q1527.

High Edge Generator 

The High Edge Generator circuit provides output signals to K1535 in the Output Switching circuit (schematic 25). The output amplitudes are in the 20 V to 100 V range. The voltage swing is a negative voltage rising to ground with a risetime of 100 ns or less.

Transistors Q1502 and Q1051 operate as switches, turning on or off at the selected chopping rate. Q1600 operates as a current source, supplying the base current for Q1501. This current is switched by Q1500. Q1511 supplies turn on current for Q1502, while Q1502 is turned off by the voltage across R1511. The reverse voltage on the base of Q1502 is limited by CR1511. Q1511 and Q1500 are driven by grounded base transistors Q1515 and Q1510, respectively. These transistors, in turn, are driven by the output of the Chop Isolator circuit (schematic 23).

Integrated circuit U1410, transistors Q1424, Q1411, Q1410, and resistors R1400, R1323 form an operational amplifier circuit with a gain of −100. For output signals in the High Edge range, the microprocessor programs the Voltage to Current Converter (schematic 21) for the proper

reference current to be applied to the Low SAC circuit (schematic 22). The output voltage from the Low SAC is used to drive the input reference voltage to the operational amplifier. The input voltage range is from .2 V to 1 V.

Resistor R1426 is the current limit sensing resistor. If the output current exceeds about 16 mA, Q1412 is turned on to protect Q1411, Q1410, Q1501, and Q1502.

Edge Overload Sense ◇27◇

The Edge Overload Sense circuit has two inputs: one from the Mid Edge Generator circuit at the collector of Q1420, the other from the High Edge Generator circuit on the base of Q1421.

If the High Edge Generator circuit goes into current limit, pin 6 of U1410 goes more negative than −10 V to turn off Q1421 and VR1430. This turns on Q1420, turns off U1430, and sets a high level on pin 5 of U1620B in the VS2 Error Gating circuit. Capacitor C1430 keeps U1430 off long enough to prevent the output of U1430 from being a pulse. The Edge Overload error signal (UNCAL, Error 3) is reported to the operator when the microprocessor strobes U1620B on pin 4.

In order to prevent the High Edge Generator from generating the Edge Overload error when the instrument is operating in the Mid Edge range, a high level is set on the base of Q1503 via pin 14 of data register U1130 (schematic 26). This turns on Q1503 and U1532 and pulls down on the base of Q1420, disconnecting Q1420 from the Edge Overload Sense circuit.

Pulse Head Drive ◇24◇

If the Pulse Head accessory is attached to the CG 5001/CG 551AP OUTPUT connector or the FAST EDGE mode is called up by the operator, the microprocessor programs the Pulse Head Drive circuit and sets the voltage level on the Control Pin. The voltage level on the Control Pin (schematic 26) will be +10 V or −10 V, dependent on what the Pulse Head internal circuits are required to do.

NOTE

Refer to the Pulse Head instruction manual for programmed input waveforms to the Pulse Head internal circuits.

The purpose of the Pulse Head Drive circuit is to provide programming and chopping signals to the circuits in the Pulse Head. This circuit outputs, through K1433, either a +5 V signal or a −5 V signal chopped to ground, or a dc level.

Integrated circuit U1210, Q1301, and associated components operate as a programmable ±5 V power supply. The polarity of the supply on pin 6 of U1210 is programmed via the voltage level of the polarity bit at pin 4 of data register U1020 in the Output Relay Control circuit (schematic 25). The output of the supply will be about +5.8 V when the data bit level is high or −5.8 V when the data bit level is low. Potentiometer R1202 sets the −5.8 V level and R1300 with R1209 sets the +5.8 V level.

Transistors Q1117 and Q1217 operate as output buffers and drivers for the Pulse Head chopping signals. These complementary emitter followers are turned on and off at the selected chopping rate by switching their bases from the dc output of U1210 to ground via Q1120 or Q1121. Emitter follower Q1217 is switched on and off to produce the +5 V square wave output and Q1117 is turned on and off to produce the −5 V square wave signal. Q1120 is used when a +5 V signal is required and Q1121 is used when a −5 V signal is required.

Transistor Q1010 operates as a paraphase circuit to develop the complementary drive for the chopping circuit. Diode CR1210 is turned on to speed up the trailing edge of the +5 V signal, while CR1113 is turned on to speed up the trailing edges of the −5 V signal.

Transistor Q1012 is turned on to disable the chopping circuit during relay switching or when this circuit is adjusted during calibration (the output level at TP1200 stays at +5.25 V or −5.25 V).

Transistor Q1109 is driven by the negative-going edge of the chop signal from the input to T1407 in the Chop Isolator circuit (schematic 23). Transistor Q1200, potentiometer R1200, C1200, along with Q1010 operate as a delay circuit to generate a total delay of about 120 ns between the TRIGGER OUTPUT pulse and the displayed fast edge from the Pulse Head. This function is not normally used, except for the Performance Check and Adjustment Procedures. The delay function is bypassed via Q1108 when its base is programmed to a high voltage level. Delay programming is via pin 5 of data register U1020 (schematic 25).

Output Relay Control, SAC Attenuators, Low Edge Attenuators, and Output Switching ◇25◇

Refer to Fig. 4-16 for a simplified diagram of all of the relays in the CG 5001/CG 551AP and to the Relay State Table in the foldout pages of Volume 2.

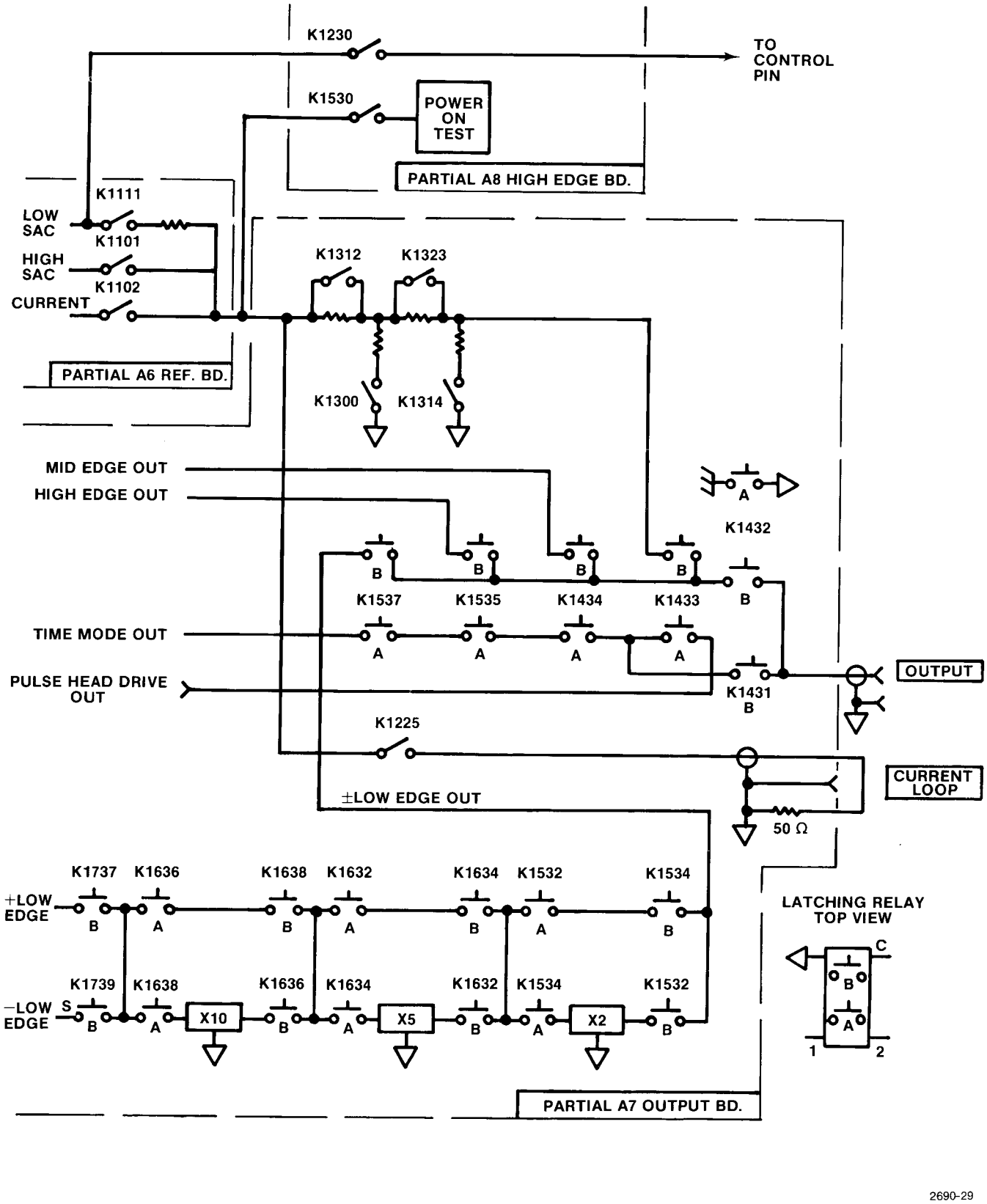


Fig. 4-16. Simplified diagram for all CG 5001/CG 551AP relays.

Relays in the Output Switching and Low Edge Attenuator blocks are magnetic latching relays, relays for the SAC Attenuators and Low SAC connection to the SAC/CUR OUT are mercury-wetted type relays, and all other relays are reed type relays.

After the microprocessor loads the data registers on the Output circuit board (U1020, U1130, U1234, and U1833) it strobes pin 1 of each register to latch the parallel data to the output lines. At the same time it strobes the magnetic latching relays via the relay strobe circuit composed of Q1032, Q1030, Q1133, and associated components.

The VS2 strobe signal on the base of Q1032 is a positive pulse of about 5 ms duration. Transistors Q1032, Q1133, and Q1030 are initially off. When the VS2 strobe pulse goes high, Q1032 turns on, which turns on Q1133. The current flow through R1030, R1032, and VR1032 develops a relay strobe pulse about 8 V in amplitude. When the voltage across R1030 reaches about .7 V, Q1030 turns on and operates as a voltage regulator, limiting the amplitude swing of the relay strobe pulse. When the VS2 strobe pulse returns to 0 V, the relays remain in their latched position. Capacitor C1034 prevents the relay strobe circuit from oscillating.

Head Programmer 

The Head Programmer circuit is used by the microprocessor to supply +10 V or −10 V dc power to the Pulse Head accessory by closing relay K1230. The circuit is also used to supply about −11 V dc power to the Comparator accessory via Darlington transistor Q1330 (K1230 is open). If the Comparator accessory is attached to the CG 5001/CG 551AP OUTPUT connector, the microprocessor sends programming signals via Q1323 and Q1330 to set the Comparator accessory to the selected operating mode. When the programming is completed, the emitter of Q1323 is kept high and Q1330 is turned on to furnish dc power to the Comparator. The connection of either accessory to the CG 5001/CG 551AP is detected via the Head Sense circuit (schematic 30).

The Head Programmer circuit also performs the functions of reporting to the microprocessor, via Q1320 or Q1322, that the load connected to the control pin is either shorted or missing. The load is located in the accessory heads.

If an accessory head is not attached to the CG 5001/CG 551AP OUTPUT connector (missing), pins 2 and 3 of U1211 will be at equal potentials with practically 0 V across R1230. This establishes a 0 V level on TP1300 and less than 0.6 V on the base of Q1321. For this condition, Q1322 is turned on to pull down on pin 13 of U1620D in the VS2 Error Gating circuit.

The direction and amount of current flow through R1230 depends on which accessory is attached to the OUTPUT connector. If the Pulse Head is connected, it also depends on the polarity of the output voltage from the Low SAC circuit. For either polarity or direction of current flow, the voltage level on TP1300 equals the voltage drop across R1230.

Under normal load conditions, the voltage level on the base of Q1321 is greater than 0.6 V, but less than 6.8 V. This voltage range is sufficient to keep Q1321 saturated, Q1322 turned off, and not great enough to cause VR1324 to conduct.

Integrated circuits, U1221A and U1221B, operate as an absolute value amplifier, generating an output voltage that is about 43 times the voltage drop across R1230. If an accessory head is shorted, there will be too much current through R1230 and the output voltage from the window comparator will rise above 6.8 V. Zener diode VR1324 then conducts, Q1320 is also turned on, setting a low level on pin 13 of U1620D. When VR1324 conducts, a high level is also set on the base of Q1323, decreasing the drive to Q1330 and limiting the current supplied to the control pin.

The Comparator programming signals consist of a sequence of pulses generated by the microprocessor. The number of pulses in a sequence sets the operating mode of the Comparator accessory.

NOTE

Refer to the Pulse Head and Comparator instruction manuals for more detailed information concerning their input circuits and operating instructions.

Power On Test and VS2 Error Gating 

The Power On Test and VS2 Error Gating circuits are used whenever the microprocessor initiates the self-test routine. The self-test rountine is performed at power up or when the TEST command is received via the GPIB. These circuits are used to report, in sequence, errors 51 through 88 (if they exist). Refer to Table 3-4, (CG 5001/CG 551AP Error Messages), in the Programming section, for description of the self test errors.

The Power On Test circuit is programmed via data register U1130 (pins 4, 5, and 6) to close K1530 and test for ±1 V, ±5 V, or ±20 V. The voltage on TP1302 will be a dc level or a 1 kHz square wave, dependent on what circuit condition is being tested at the time.

The data bit code (listed on the schematic) for pins 5 and 6 of U1130 turns Q1101 and Q1201 on or off to set the input attenuation for the first operational amplifier, U1110. For any input voltage, the attenuation or gain is such that the voltage on TP1100 will be −5 V for positive inputs or +5 V for negative inputs.

Integrated circuit U1210 and associated components, operate as an absolute value generating circuit whose output equals one-half the absolute value of the input. For negative voltages on TP1100, diode CR1219 is turned on and the amplifier feedback components operate to divide by two. For positive voltages on TP1100, diode CR1219 is turned off; division by two is then performed by the voltage divider network consisting of R1213, R1214, and R1216.

Integrated circuits, U1220A and U1220B, operate as a voltage window comparator. The voltage value on TP1210 is one-half the absolute value on TP1100. Test point TP1202 is set to +2.73 V by potentiometer R1300.

If the input voltage to the Power On Test circuit (TP1302) is correct, the output of the window comparator will be positive. Diodes CR1125 (or CR1222) and CR1330 will be turned off, setting a high level on pin 10 of U1620C in the VS2 Error Gating circuit. When the microprocessor strobes U1620C on pin 9, the low level output on pin 8 is interpreted as no error for the appropriate test. Pin 8 of U1620C will be high if an error is indicated.

For aid in understanding the signal paths from the related VOLTAGE, CURRENT, and EDGE mode circuit blocks to the input of the Power On Test circuit, refer to Fig. 4-14.

If the microprocessor is performing the 50 Ω load tests (errors 51, 53, 56, 57, 81, 83, and 84), it uses the CURRENT LOOP as a 50 Ω load by closing K1225 (schematic 25) and other necessary relays to complete the signal path. For example, when the Mid Edge tests are performed, the following relays are closed: K1434B, K1433B, K1323, K1312, and K1530.

For the 1 kHz tests, the signal input to the Power On Test circuit causes pin 8 of U1620C to alternate between high and low levels at a 1 kHz rate. The microprocessor checks for the proper level once every 0.5 ms to verify the chopping functions.

The Power On Test sequence is performed only to verify the functionality, not accuracy, of the related VOLTAGE, CURRENT, and EDGE mode circuits.