3½ digit A/D converter set

designed for . . .

- **High Performance Digital Voltmeters**
- **Digital Panel Meters**
- **Digital Instrumentation Readouts**
- **Microprocessor A/D Interface Subsystem**
- **Auto-Zeroed Microvolt or Strain-Gauge Systems**

Siliconix

BENEFITS

- Two Voltage Ranges (1.999 V and 199.9 mV) with Single Resistor Change
- High System Performance Ensured by Basic 0.05% ±1 Count Accuracy
- Wide Sampling Rate: 1/3 to 12/Second
- Reduced Signal Loading with PMOS Input ($Z > 10^9\ \Omega$)
- Auto-Zero System Minimizes Internal and External Offsets and Drift Over Temperature
- Auto-Polarity with Single Reference
- Easy Interface to Displays with Strobed BCD Output Format
- Overrange and Underrange Signals Available
- External Latch Inhibit Control Serial BCD Output, Active High or Low Output Control, and ÷512 Output for Use in Sophisticated Data Transmission and Formatting Schemes

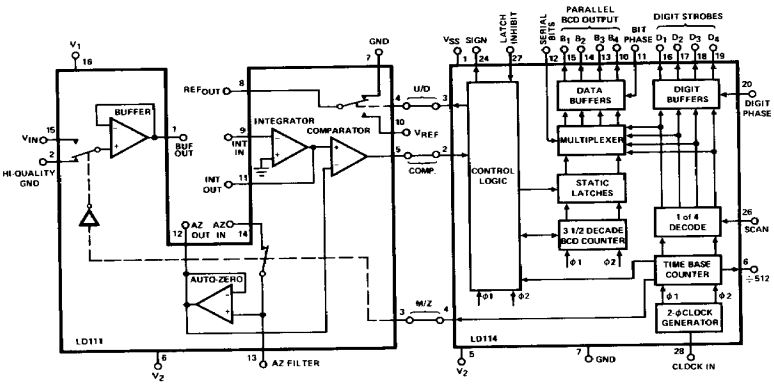
DESCRIPTION

Replace LD111 with LD111A for New Designs

The LD111 analog processor contains a bipolar comparator, a bipolar integrating amplifier, two MOSFET input unity gain amplifiers, several P-channel enhancement mode analog switches and the necessary level shifting drivers to allow the analog and digital processors to be directly interfaced. A wide range of conversion rates (1/3 to 12 samples per second) as well as two voltage ranges can be accommodated using externally determined RC time constants. All amplifiers are internally compensated.

The PMOS LD114 digital processor combines the counting storage and data multiplexing functions with the random logic necessary to control the quantized charge-balancing function of the analog processor. Seventeen static latches, in response to external control, store the 3 1/2 digits of BCD data as well as underrange and polarity information. Ten push-pull output buffers (capable of driving one standard TTL load) provide the clock frequency ÷512, sign, digit strobe and multiplexed BCD data. Four data output format options allow the user to tailor the BCD output to his circuit requirements.

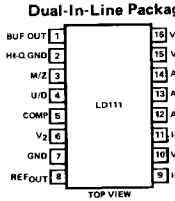
FUNCTIONAL DIAGRAM



SWITCH STATES ARE FOR A LOGIC "0" AT U/D AND M/Z INPUTS.

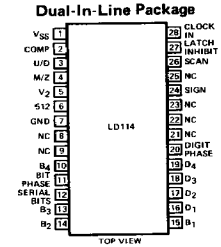
PIN CONFIGURATIONS

Dual-In-Line Package



ORDER NUMBER LD111CJ
SEE PACKAGE 8

Dual-In-Line Package



ORDER NUMBER LD114CR
SEE PACKAGE 13

ABSOLUTE MAXIMUM RATINGS

I_{IN} (Pin 15, 2, LD111) . . . . . ±1 mA
$V_1 - V_2$ (LD111) . . . . . 30 V
V_{SS} . . . . . 6 V
$V_{SS} - V_2$ (LD114) . . . . . 20 V
Voltage on any pin relative to V_{SS} (LD114) 0.3 V to −20 V
V_{REF} . . . . . V_1
Operating Temperature . . . . . 0 to 70°C

Storage Temperature . . . . . −65 to +125°C
Power Dissipation (Package, LD111)* . . . . 470 mW
Power Dissipation (Package, LD114)* . . . . 1200 mW

*Device mounted with all leads welded or soldered to PC Board. Derate 6.3 mW/°C above 25°C (for LD114, derate 16 mW/°C above 70°C).

Absolute Maximum Ratings are stress limits only. Exceeding these limits may cause device damage. Electrical Characteristics define the functional operating limits.

ELECTRICAL CHARACTERISTICS

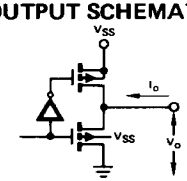
All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters to assure conformance with specifications.

		CHARACTERISTIC		MIN	TYP	MAX	UNIT	TEST CONDITIONS V_1 = 12 V, V_2 = −12 V, V_{SS} = 5 V, V_{REF} = 8.2 V, T_A = 25°C
1	INPUT	f_{IN}	Clock Frequency		30.7		kHz	
2		I_{IN}	Input Bias Current		4		pA	T_A = 25°C
3					40			T_A = 70°C
4		NMR	Normal Mode Rejection		40		dB	f_L = 60 Hz
5		I_{CL}	Clock Input Current Low			−500	µA	$V_{CLOCK\ IN}$ = 0.4 V
6		I_{INL}	Comparator			−100		V_{INL} = −12 V
7		I_{INL}	Latch Inhibit		−180	−600		V_{INL} = −12 V
8		I_{INH}	Format Option Inputs		25	400		V_{INH} = V_{SS}
9	OUTPUT	V_{OL1}	Digits, ÷512			0.4	V	I_{OL} = 1.6 mA
10		V_{OL2}	Sign Voltage, Low			0.6		I_{OL} = 1.6 mA
11		V_{OH1}	Digits, Sign, ÷512	2.4				I_{OH} = −800 µA
12		V_{OH2}	Data Bit Voltage, Low			0.4		I_{OL} = 1.6 mA
13		V_{OH2}	Data Bit Voltage, High	2.4				I_{OH} = −200 µA
14		V_{OL3}	M/Z Voltage, Low			0.4		I_{OL} = 150 µA
15		V_{OH3}	M/Z Voltage, High	2.4				I_{OH} = −200 µA
16		V_{OL4}	U/D Voltage, Low			0.4		I_{OL} = 250 µA
17		V_{OH4}	U/D Voltage, High	2.4				I_{OH} = −200 µA
18	SWITCH	$r_{DS(on)}$	ON Resistance, Auto Zero Switch		11	50	KΩ	$V_{AZ(in)}$ = −4.0 V, I_S = −30 µA
19		$r_{DS(on)}$	ON Resistance, U/D Switch		650	3000	Ω	I_S = 1 mA
20		TC	U/D Switch, Temperature Coefficient		0.2	0.5	%/°C	
21	SUPPLY	I_1	Supply Current		2.2	3.5	mA	
22		I_{2A}	Supply Current, LD111		−1.8	−3.0		
23		I_{2D}	Supply Current, LD114		−17	−23		
24		I_{SS}	Supply Current		17.4	24		
25		$PSRR_1$	Power Supply Rejection Ratio V_1	80	85		dB	
26		PSRR	Power Supply Rejection Ratio, V_2	60	65			
27			Reference Current Rejection Ratio	35	41		nA/LSB	R_{REF} = R_2 = 100K Ω, V_{IN} = 2 V

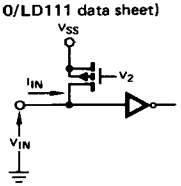
Typical values for Design Aid ONLY, not guaranteed and not subject to Production Testing.

LD111-CMAF/LD114-IPAN II

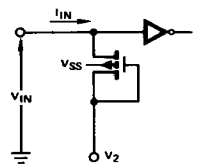
INPUT/OUTPUT SCHEMATICS (See also LD110/LD111 data sheet)



Output Buffers
(Digits, Bits, Sign, 512, M/Z, U/D)



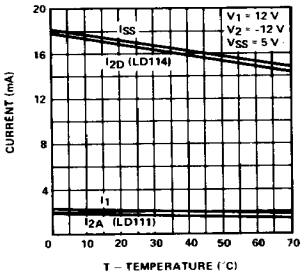
Comparator, Clock, Latch Inhibit Inputs



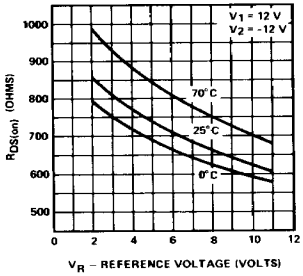
Format Option Inputs
(Bit Phase, Digit Phase, Scan, Serial Bits)

TYPICAL CHARACTERISTICS

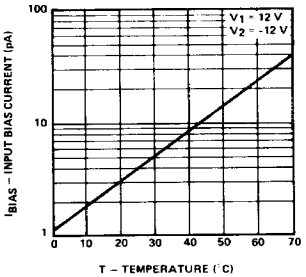
Supply Currents vs Temperature



$R_{DS(on)}$ (U/D Switch) vs V_{REF} and Temperature



Input Bias Current vs Temperature



DESCRIPTION OF PIN FUNCTIONS – LD114

V_{SS} – Positive Supply Voltage. Recommended level is +5 volts ±10%.

V_2 – Negative Supply Voltage. Recommended level is −12 volts ±10%.

CLOCK IN – This input accepts a TTL or MOS level clock to drive the synchronous digital circuitry. Acceptable duty cycles on the external clock range from 30% high, 70% low to 70% high, 30% low for clock frequencies from 2 kHz to 75 kHz. Although any clock frequency between 2 kHz and 75 kHz may be used, clock frequencies that are integer divisions of $2048F_L$ ($F_{IN} = 2084F_L/n$, n = 2, 3, 4 . . . 51), (F_L = Line Frequency) provide measure and zero periods that are integer multiples of the line frequency period ($T_{zero} = n/F_L$, $T_{measure} = 2n/F_L$). Line frequency interference is minimized by the selection of one of these 50 frequencies.

This input has an active pull-up to V_{SS}.

M/Z – Measure/Zero Logic Output. This 0 to 5 volt logic output successively provides Autozero and Measurement intervals of 2048 and 4096 clock periods respectively. This output is compatible with CMOS logic and directly interfaces with the LD111 analog processor.

÷ 512 – This TTL compatible output (1 standard load) provides the necessary clock frequency division for a phase locked loop digital clock. The line frequency rejection will be held at the maximum level (> 80 dB) when locked to the line frequency. The typical application circuit of Figure 6 shows a phase locked loop clock as an alternative to the 555 timer clock. As shown, the center frequency of the PLL will be 30.72 kHz (512 times 60 Hz). This circuit can be used to track line frequencies of 50 Hz by changing R_{17} from 5.6 KΩ to 4.7 KΩ.

U/D – Up/Down Logic Output. This output has logic levels of 0 and +5 volts to provide pulse-width modulation of the reference current when used with the LD111 analog processor. This output is CMOS compatible.

COMP – Analog Comparator Input. This input has an active pull-up to V_{SS} for a comparator "high" state. This pin must be pulled down to V_2 for a "low" comparator state.

An End-of-Conversion Signal can be decoded from the three interconnecting logic lines (M/Z, U/D, Comp) using the following CMOS logic.

$\overline{M/Z + U/D + Comp}$ = E.O.C.

B_1, B_2, B_3, B_4 – BCD Data Bit Output. B_4 represents the most significant bit and B_1 the least significant bit of the BCD output. Bit 4 of digit 4 goes high for an underrange condition (less than 100 counts). These outputs are compatible with 1 standard TTL load.

MUX Underrange = $B_4 \cdot D_4$ (5% of full scale)

D_1, D_2, D_3, D_4 – Digit Strobe Outputs. D_4 is the most significant and D_1 the least significant digit of the 3 1/2 digit output. The digit strobes are each selected in turn when the BCD data bits for that digit appear at the bit outputs (see Figure 4).

MUX Overrange = $\overline{D_1 + D_2 + D_3 + D_4}$ (100% of full scale, count ⩾ 2000).

SIGN – Sign of Analog Input Polarity. This TTL level output is a static signal which is either 0 or V_{SS} for a negative or positive input polarity respectively.

BIT PHASE – The bit outputs will be active high (positive) logic if this pin is left open or connected to V_2. The application of V_{SS} to this pin will give a complemented output (negative logic).

DIGIT PHASE – The Digit Strobe outputs will be of positive logic if this pin is left open or connected to V_2 (an active pull-down is internally connected to V_2). Applying V_{SS} to this pin will complement the outputs to give negative logic. Negative logic may simplify interfacing with Common Anode LED, Gas Discharge and Liquid Crystal Displays.

DESCRIPTION OF PIN FUNCTIONS— LD114 (Cont'd)

SCAN – Sequential/Interlace Digit Scan. The digit strobe format will be an interlaced format of digits 1, 3, 2 and 4 if this pin is left open or is connected to V_2. This format is useful for display digits packaged two to an envelope and which require an interdigit blanking period (Beckman Displays). By alternating from envelope to envelope, an interdigit blanking period is effectively provided.

The application of V_{SS} to this pin will give a sequential scan of digits 1, 2, 3 and 4. This format may be more useful in interfacing with data acquisition equipment.

SERIAL BITS – Parallel/Serial Bit Output Format. The BCD data bits for each digit will appear simultaneously with the digit strobe if the parallel bit option is selected. The timing for this output format is shown in Figure 4. This format is useful for driving multiplexed displays. The parallel bit format is available when this pin is left open or connected to V_2.

The application of V_{SS} to this pin will put all of the BCD data bits in a serial order at the bit 4 output, as shown in the timing diagram of Figure 5. Bit outputs 1, 2 and 3 contain time markers to identify the data. The most significant bit of the last digit (D_4) is identified by a marker at the bit 2 output. The least significant bit of the first Digit (D_1) is identified by a marker at bit 3. Bit 1 shows a marker for the least significant bit of each digit.

Computer interface and other systems applications may be more easily accomplished with this output format. Figure 9 shows an A/D multiplexing scheme using this format.

All output format options are independent of one another (i.e., the serial bit output can have either sequential or interlace scan, Positive or Negative logic).

LATCH INHIBIT – Connecting this pin to V_2 will prevent updating of the internal static latches, thus providing a "hold" function. Leaving this pin disconnected will allow the latches to be updated once each sampling period.

An "external trigger" function can be added to the A/D converter as shown in Figure 7. When the external trigger input is high the static latches of the LD114 will be updated each conversion (normal operation). A low trigger input allows the A/D converter to make one *complete* measurement before the latches are inhibited. This insures that the latched output is a valid representation of the input. An end of conversion signal is made available.

This circuit can be combined with a sample and hold circuit as shown in Figure 8 to provide a sampling A/D converter.

GND – Digital Processor or Ground. Should be kept seperate from Analog Grounds. Common connection should be made at the power supply.

DESCRIPTION OF PIN FUNCTIONS – LD111

BUF OUT – The output of this unity gain input buffer amplifier is applied to the integrator summing node through a scaling resistor R_2. The value of this resistor is typically 10 KΩ for a 200.0 mV full-scale and 100 KΩ for a 2.000 V full-scale. The digital output is inversely proportional to the value of this resistor,

$$\text{Count} = \frac{V_{IN}}{V_{REF}} \frac{R_1}{R_2} \quad 8192$$

HI-QUALITY GND – This pin, typically connected to a High Quality Ground point for single ended inputs **CAN BE USED AS THE INVERTING INPUT FOR DIFFERENTIAL SIGNALS.** The digital output will be $V_{IN} - V_{HI-Q}$. When using this differential mode, it is important that resistor R_3 equal Resistor R_2 for proper operation.

M/Z – Measure/Zero Logic Input. Internal level shifting drivers operate the PMOS switches in response to this digital signal.

U/D – Up/Down Logic Input. The logic signal applied to this pin operates a SPDT switch to provide Quantized pulses of charge to the integrator.

COMP – This analog comparator output is an open collector configuration which goes to V_2 when "low."

V_2 – Negative Supply Voltage. Recommended level is −12 V ±10%.

GND – Analog Processor Ground. Should be well isolated from Digital Ground Noise.

REF_{out} – This voltage output of the SPDT U/D switch, converted to a current by resistor R_1, supplies the reference current to the integrator.

INT. IN – Integrator Summing Node.

V_{REF} – A stable positive reference voltage (5 to 11 V) applied to this pin is the standard to which the input voltage V_{IN} is measured. Ratio measurements can be made by applying a variable to this input (1.0 to 11 V).

INT. OUT – The output of the integrating amplifier is made available for application to the Auto-Zero amplifier by means of resistor R_4.

AZ OUT – The output of the unity gain Auto-Zero Amplifier provides a second negative reference current to the integrator through resistor R_3.

AZ FILTER – The RC filter (R_5 and C_{STRG}) connected to this pin stores D.C. voltage components to balance amplifier offset and drift components.

AZ IN – This input is switched into the AZ filter during the Zeroing interval.

V_{IN} – Analog Voltage Input. The A/D System digitizes the voltage appearing at this input.

V_1 – Positive Supply Voltage. The recommended level is +12 volts ±10%.

FUNCTIONAL OPERATION

The connection diagram of Figure 1 and the timing diagrams of Figures 2 and 3 will be referred to in this discussion of functional operation.

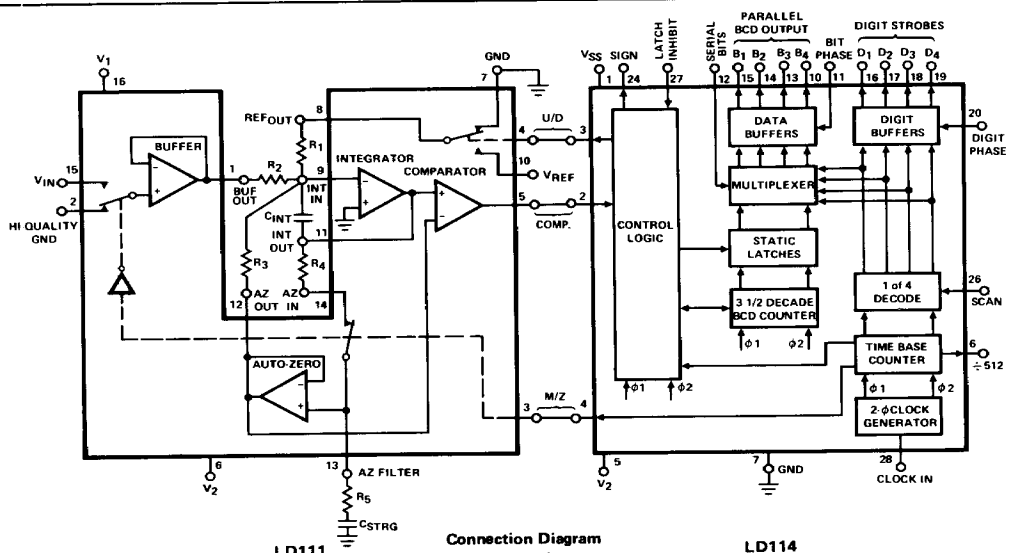
Time Base Counter — An external clock signal drives a 2-ϕ clock generator on the synchronous digital chip. The clock frequency is divided by the time base counter into sampling intervals of 6144 pulses of which 4096 constitute the measurement interval and 2048 the auto-zero interval. Intermediate frequency divisions are utilized by both the control logic and the 1 of 4 decoder for the digit enables and bit scan.

Auto-Zero Interval — The connection diagram of Figure 1 shows the analog circuitry in the auto-zero mode. The buffer amplifier input is switched to ground and supplies the relatively minor current of V_{OS}/R_2 to the integrator input summing node. The output of the unity gain auto-zero amplifier V_{AZ} is a low-pass filtered version of the integrator output. V_{AZ}/R_3 and the pulsed reference current V_{REF}/R_1 constitute the major currents flowing into the integrator input summing node. The reference current is pulsed at a 50% duty cycle (4 clock cycles on and 4 clock cycles off) by the control logic during this interval. The on state of the reference current corresponds with a down state of the Up/Down logic. Equilibrium will be attained by the closed loop system of integrator and AZ amplifier when the sum of the average currents at the integrator summing junction equals zero. The current through R_3 will then be constant at $-1/2\ V_{REF}/R_1$. The storage capacitor C_{STRG} will maintain the AZ amplifier at the AZ equilibrium voltage when the AZ switch is opened at the end of the zero interval. During the subsequent measure interval then, V_{AZ} will equal V_{STRG}.

The output of the integrator as a function of time during the auto-zero interval is shown in the timing diagram of Figure 2 along with the pertinent timing points. The beginning of this interval is characterized by a brief override period during which the 50% duty cycle of the U/D logic is inhibited while the integrator output is brought to V_{STRG}.

Measure Interval — At the start of the measure interval, the Measure/Zero logic switches the analog input voltage into the input buffer amplifier. This amplifier in conjunction with R_2 acts as a voltage to current converter. The additional current flowing into the integrator summing node disrupts the balance achieved during the AZ interval driving the output of the integrator away from the AZ equilibrium voltage maintained as a reference by C_{STRG}.

The comparator transmits the sense of the deviation to the control logic which attempts to re-establish the system equilibrium by using one of the two duty cycles available during the measure interval. The U/D logic is "up" one clock cycle and "down" 7 cycles for a high comparator output in the clock cycle preceding a set of 8 cycles. This will be designated duty cycle "A" as shown in Figure 3. With a low comparator output in clock cycle number 7 the U/D logic will be "up" for 7 cycles and "down" for 1 cycle in the following 8 clock cycles. This is duty cycle "B." The effect of these two reference current duty cycles on the integrator output is shown in Figure 3. It can be seen that the "up" state of the U/D logic drives the integrator output voltage up. The synchronous up/down BCD counter increments by each clock pulse when the U/D logic is "up" and decrements by each clock pulse when the U/D logic is "down." Consequently the net count goes up 6 counts for a "B" duty cycle and down 6 for an "A" duty cycle to give a maximum count of approximately 3100 counts. This counting procedure is inverted when $V_{IN} < 0$.

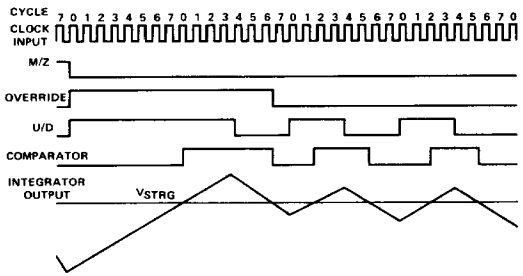


Connection Diagram
Figure 1

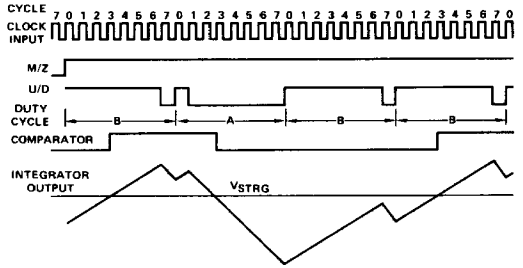
The polarity of V_{IN} is determined by the state of the U/D logic when the BCD counter state is zero. This information, stored in the sign flip-flop, is loaded into the static latch once each measure-zero cycle.

The BCD counter accumulates a number of counts proportional to the input voltage during the measure interval as the control logic works to maintain equilibrium. Since the system equilibrium is established in steps there will exist, in all probability, a residual voltage error ΔV at the end of the measure period. This voltage and the corresponding counter error are accounted for by a brief override interval at the beginning of the auto-zero period. The counter continues its count until the integrator output V_O equals the auto-zero equilibrium voltage and the U/D is "down." At this time the BCD counter is put on "hold" and its contents are loaded into the latches along with underrange information decoded from the counter contents (5% of full scale). The counter is then cleared. The contents of the static latches are multiplexed to the push-pull data output buffers in BCD format.

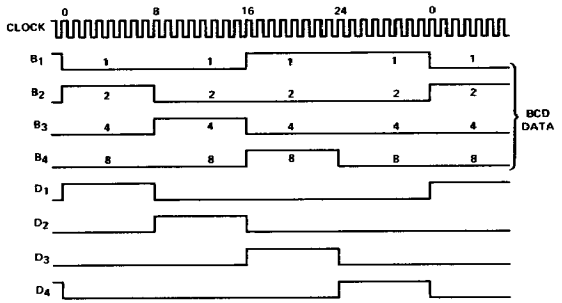
The presence of a count of 2000 or greater in the BCD counter (100% of full scale) causes the digit strobes to stay low during the zero cycle. This causes a strobed display to blink at a rate equal to the sampling rate.



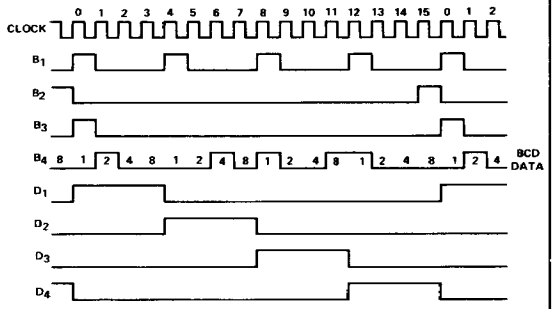
Auto-Zero Timing
Figure 2



Measure Interval Timing
Figure 3

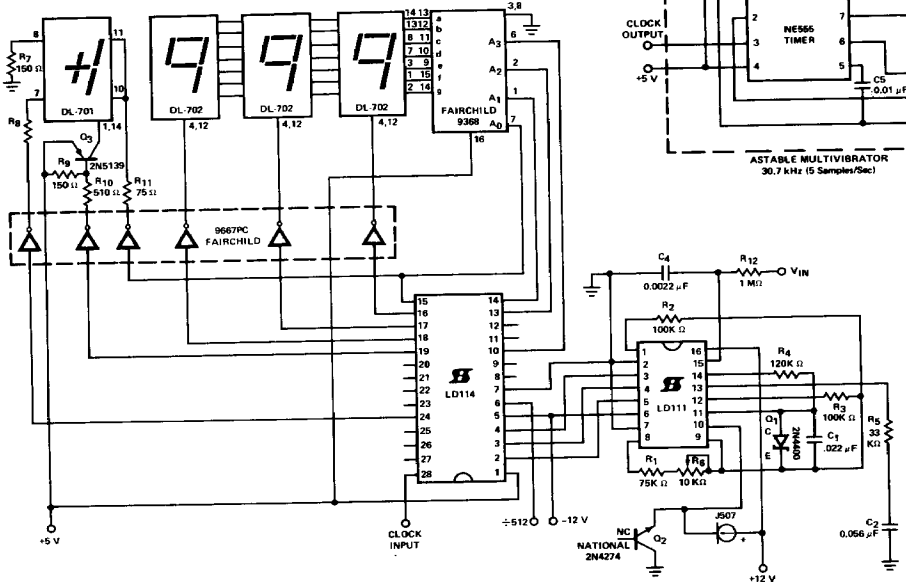


Parallel BCD Output Format
(Output = 1942, Sequential Scan)
Figure 4



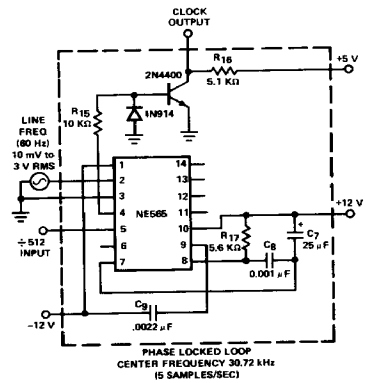
Serial BIT Output Format
(Output = 1942, Sequential Scan)
Figure 5

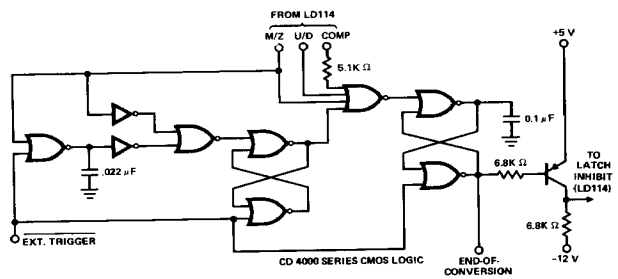
APPLICATIONS (refer also to Application Notes AN74-1 and AN76-4 in Index 4 of this book for additional applications information)



3 1/2 Digit DVM (±200.0 mV)
Figure 6

NOTE. C_1, C_2 should be mylar, polycarbonate.

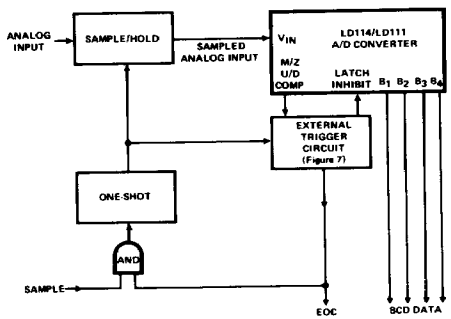




External Trigger Circuit
Figure 7

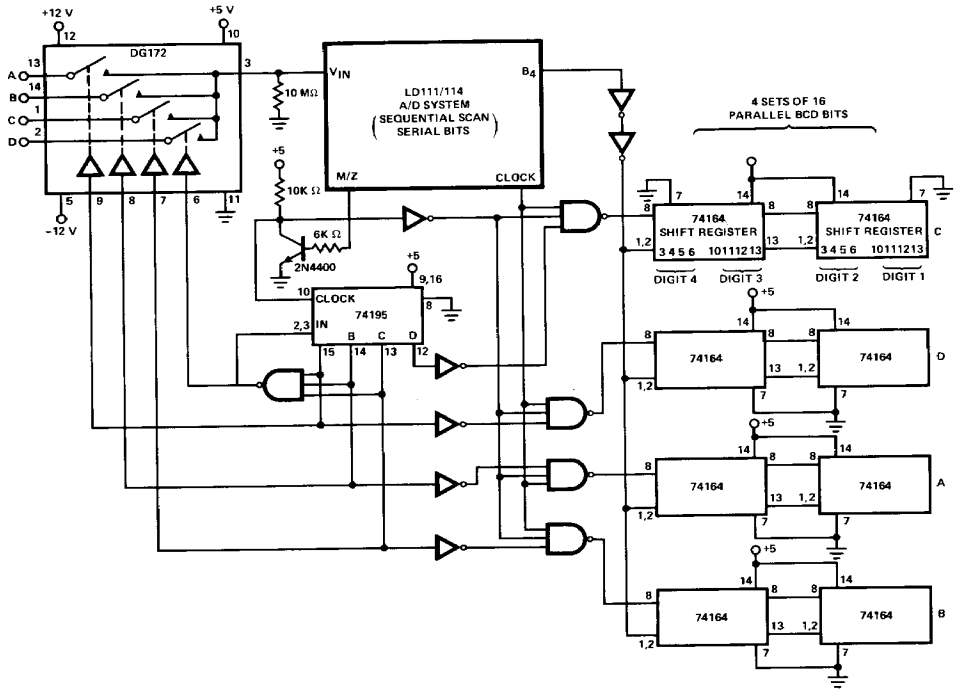
The external trigger circuit of Figure 7 will latch the BCD data in the LD114 when one complete measurement has been made after the trigger signal goes low.

This circuit can be used in the Sample/Hold A/D circuit shown in block form in Figure 8. This circuit will sample the analog signal and hold it indefinitely in a digital format. The maximum time between the sample command and the end of conversion signal is $10240/F_{IN}$.



Sampling A/D
Figure 8

APPLICATIONS (Cont'd)



Multiplexed A/D Converter
Figure 9