DDR2 SDRAM

MT47H128M4 – 32 Meg x 4 x 4 banks
MT47H64M8 – 16 Meg x 8 x 4 banks
MT47H32M16 – 8 Meg x 16 x 4 banks

Features

- Vdd = +1.8V ±0.1V, VddQ = +1.8V ±0.1V
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4*n*-bit prefetch architecture
- Duplicate output strobe (RDQS) option for x8
- DLL to align DQ and DQS transitions with CK
- 4 internal banks for concurrent operation
- Programmable CAS latency (CL)
- Posted CAS additive latency (AL)
- WRITE latency = READ latency - 1 ^{t}CK
- Selectable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Industrial temperature (IT) option
- Automotive temperature (AT) option
- RoHS compliant
- Supports JEDEC clock jitter specification

Options[1]	Marking
• Configuration	
– 256 Meg x 4 (32 Meg x 4 x 4 banks)	128M4
– 128 Meg x 8 (16 Meg x 8 x 4 banks)	64M8
– 64 Meg x 16 (8 Meg x 16 x 4 banks)	32M16
• FBGA package (Pb-free) – x16	
– 84-ball FBGA (12mm x 12.5mm) Rev. B	CC
– 84-ball FBGA (10mm x 12.5mm) Rev. D	BN
– 84-ball FBGA (8mm x 12.5mm) Rev. F	HR
• FBGA package (Pb-free) – x4, x8	
– 60-ball FBGA (12mm x 10mm) Rev. B	CB
– 60-ball FBGA (10mm x 10mm) Rev. D	B6
– 60-ball FBGA (8mm x 10mm) Rev. F	CF
• FBGA package (lead solder) – x16	
– 84-ball FBGA (12mm x 12.5mm) Rev. B	GC
– 84-ball FBGA (10mm x 12.5mm) Rev. D	FN
– 84-ball FBGA (8mm x 12.5mm) Rev. F	HW
• FBGA package (lead solder) – x4, x8	
– 60-ball FBGA (12mm x 10mm) Rev. B	GB
– 60-ball FBGA (10mm x 10mm) Rev. D	F6
– 60-ball FBGA (8mm x 10mm) Rev. F	JN
• Timing – cycle time	
– 2.5ns @ CL = 5 (DDR2-800)	-25E
– 2.5ns @ CL = 6 (DDR2-800)	-25
– 3.0ns @ CL = 4 (DDR2-667)	-3E
– 3.0ns @ CL = 5 (DDR2-667)	-3
– 3.75ns @ CL = 4 (DDR2-533)	-37E
– 5.0ns @ CL = 3 (DDR2-400)	-5E
• Self refresh	
– Standard	None
– Low-power	L
• Operating temperature	
– Commercial (0°C ≤ T_C ≤ 85°C)	None
– Industrial (–40°C ≤ T_C ≤ 95°C; –40°C ≤ T_A ≤ 85°C)	IT
– Automotive, Revision :D only (–40°C ≤ T_C, T_A ≤ 105°C)	AT
• Revision	:B/:D/:F

Note: 1. Not all options listed can be combined to define an offered product. Use the Part Catalog Search on www.micron.com for product offerings and availability.

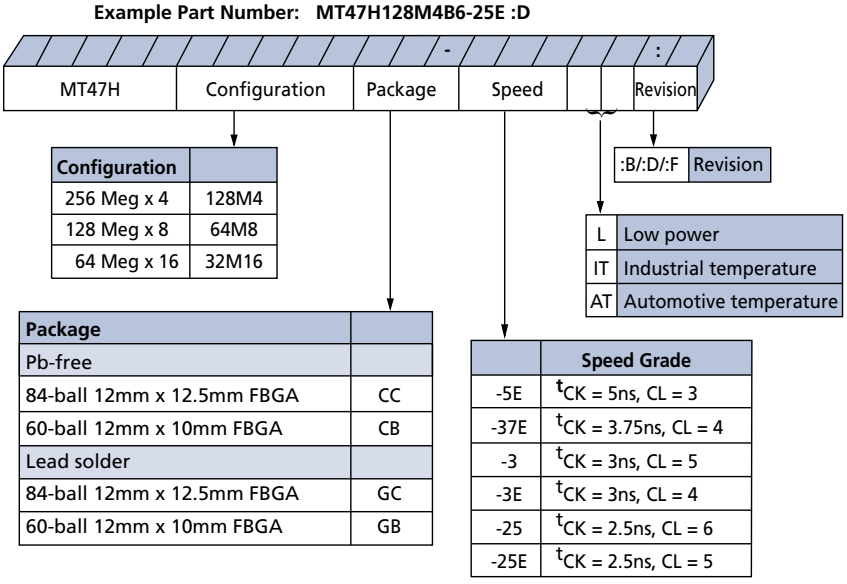
Table 1: Key Timing Parameters

Speed Grade	Data Rate (MT/s)				^tRC (ns)
	CL = 3	CL = 4	CL = 5	CL = 6	
-25E	400	533	800	800	55
-25	400	533	667	800	55
-3E	400	667	667	n/a	54
-3	400	533	667	n/a	55
-37E	400	533	n/a	n/a	55
-5E	400	400	n/a	n/a	55

Table 2: Addressing

Parameter	128 Meg x 4	64 Meg x 8	32 Meg x 16
Configuration	32 Meg x 4 x 4 banks	16 Meg x 8 x 4 banks	8 Meg x 16 x 4 banks
Refresh count	8K	8K	8K
Row address	A[13:0] (16K)	A[13:0] (16K)	A[12:0] (8K)
Bank address	BA[1:0] (4)	BA[1:0] (4)	BA[1:0] (4)
Column address	A[11, 9:0] (2K)	A[9:0] (1K)	A[9:0] (1K)

Figure 1: 512Mb DDR2 Part Numbers



Note: 1. Not all speeds and configurations are available in all packages.

Figure 5: 32 Meg x 16 Functional Block Diagram