THEORY OF OPERATION

INTRODUCTION

This section of the manual contains a description of the electrical circuits in the FG 501A. Refer to the block diagram and schematic diagrams on the fold out pages in the back of the manual to aid in understanding this description. Diamond enclosed numbers appearing throughout this section refer to the schematic diagram on which the circuit being discussed is located.

LOOP ①

FREQUENCY CONTROL AND SUMMING AMPLIFIER

The voltage developed across the frequency control divider string, R1429, R1321, R500 and R510, is applied to pin 5 of operational amplifier U1540B. This voltage is buffered by the amplifier and a current is developed through R1551. This current is applied to pin 2 of summing amplifier U1540A where it is summed with any currents developed by a voltage applied to the VCF inputs. The VCF inputs are J510 (front panel) through R1553, and pin 21B (rear interface) through R1103. These summed currents are buffered by Q1445 and flow through R1543. The voltage developed across R1543 is proportional to the frequency.

CURRENT SOURCES AND SWITCH

The voltage developed across R1543 is buffered by U1440 and Q1541 which form the negative current source for the main loop timing circuitry. This same voltage is also buffered by U1540C and Q1543 which form a current source identical to U1440 and Q1541. The output current from Q1543 flows through Q1527, Q1525, and Q1421, which form a current mirror that inverts this current to provide the positive current source for the main loop timing circuitry. The current through R1521 is the timing capacitor charging current; the current through R1536 is the discharging current. The Top Dial Symmetry Cal, R1421, adjusts the balance between these two currents so they are equal in magnitude.

In the normal mode of operation (fixed symmetry) R520 and R540 are in the emitter circuit of Q1541 and Q1543. In this condition, equal amounts of current will flow in both the positive and negative current sources. When S500, VAR SYMM, is activated, R530 is switched into the current source emitter circuits. As R530 is varied from one end to the other, unequal amounts of current flow through the positive and negative current sources. In this manner the symmetry of the waveform generated by the loop is varied. These currents are switched into the junction of CR1531 and CR1533 where they alternately charge and discharge the timing capacitor, producing a triangle waveform. The current switch is formed by Q1531, CR1531, Q1433 and CR1533.

TIMING CAPACITORS AND CAPACITANCE MULTIPLIER ②

The timing capacitors provide for triangle generation in the five fastest MULTIPLIER ranges. They are switched into and out of the circuit in decade steps from 10^5 (C1631) down to 10^1 (C1741).

For the four lower MULTIPLIER ranges, 10^0 down to 10^{-3}, C1741 is switched into the feedback loop of U1930 forming an integrator. Current from the current switch is applied to operational amplifier U1940. A voltage is developed at the output of this amplifier that is proportional to the applied current times the value of R1941 (1 kΩ). This voltage is applied, across one of four resistors, to the input of U1930. These resistors, R1831, R1841, R1842, and R1843, are switched into and out of the circuit in decade steps with the MULTIPLIER switch S1731. This arrangement provides very large values of effective capacitance. The output of U1930 is now the triangle that is applied to the buffer stage.

TRIANGLE BUFFER ①

The voltage developed by the timing capacitor or multiplier (U1930) is applied to the triangle buffer. Q1725 and Q1723 form the differential input stage of this circuit. Q1821 serves as a constant current source for the input differential pair. Q1721 and Q1712 complete the feedback for the amplifier such that the voltage at the emitter of Q1712 is equal to the voltage at the Gate of Q1725.

Loop delay compensation is provided by a network comprised of R1712, R1812, C1712, and C1714. The buffered timing capacitor voltage is applied through this network to the level comparators.

LEVEL COMPARATORS

The level comparators detect upper and lower threshold levels. U1700A is the upper level detector and U1700B the lower. The reference level for these comparators is supplied by U1400B and C. As the threshold levels are detected, the respective comparator triggers U1600B.

REFERENCE VOLTAGES

The reference voltage supplies are composed of U1400B (−) and U1400C (+) and associated components. The upper (positive) level threshold voltage is established by adjusting R1412. This resistor is in a voltage divider string from zener diode VR1413. The voltage developed across R1412 is buffered by U1400C and set to approximately +400 mV at the output. This voltage is applied to pin 5 of U1700A as the upper threshold level reference. This same voltage is also applied to pin 9 of inverter U1400B. R1511 is used to adjust the gain of this stage so that the output is nominally −400 mV. This voltage is applied to pin 13 of U1700B as the lower threshold level reference.

LOOP LOGIC

When a rising voltage at pin 6 of U1700A passes through the threshold level set at pin 5, the output (pin 8) goes low pulling pin 10 of U1600B low. This action sets the flip-flop causing pin 9 (Q) to go high and pin 8 ($\overline{Q}$) to go low. Pin 8 of U1600B is tied back, through R1403, to the junction of CR1431 and VR1532. VR1532 serves as a level shifter to change the TTL output gate to the correct level to drive the current switch (Q1531, CR1531, Q1433, CR1533).

As the voltage at the junction of R1532 and R1534 drops, it pulls the bases of Q1531 and Q1433 low. Q1531 is turned on and Q1433 is turned off. Any current from the positive current source, through R1521, now flows through Q1531 and is shunted to the −15 V supply. With Q1433 turned off, any current flow through the negative current source must come from the positively charged timing capacitor through CR1533.

The falling voltage on the timing capacitor is buffered through the triangle buffer and applied to the level comparators U1700A and U1700B. As the voltage at pin 12 of U1700B falls through the threshold level set at pin 13, the output (pin 1) goes low pulling pin 13 of U1600B low. This action resets the flip-flop causing pin 9 (Q) to now go low and pin 8 ($\overline{Q}$) to go high. Taking this high at pin 8 back to the current switch, Q1531 will be turned off and Q1433 turned on. This allows the timing capacitor to charge in the positive direction.

The action just described generates one entire cycle of a triangle wave.

TRIGGER GENERATOR

The square wave output at pin 8 ($\overline{Q}$) of U1600B also drives the trigger output amplifier. This circuit is composed of emitter follower Q1431 and associated components. Q1440, in conjunction with R1440, serves as output short circuit protection. The output of this circuit (at J2043) is a square wave 180° out of phase with the main loop signal. The output amplitude is greater than +4 V into an open circuit, and at least +2 V into a 50 Ω load.

SQUARE WAVE GENERATOR

The output at pin 9 (Q) of U1600B is a square wave, but 180° out of phase with that at pin 8. This signal is used to drive the square wave generator composed of differential pair Q1801, Q1901, and associated components. The base of Q1901 is held at a constant voltage by divider network R1815 and R1818. R1728 and R1816 form a constant current source for the differential pair. The square wave from U1600B alternately switches this constant current to ground through Q1801 or through R1819 and Q1901. In this manner, a square wave voltage is developed with dc levels sufficient to drive the output amplifier for the square wave function.

PHASE CLAMP THRESHOLD DETECTOR

The output of the triangle buffer, in addition to possibly being fed to the Output Amplifier through S1901B, is connected to the base of Q1711. Q1711 and Q1611 form a differential amplifier. Q1621 and associated components provide a constant current source for the differential pair. This amplifier senses the level of the triangle waveform and compares it to the output voltage of U1400A. The output voltage of U1400A is determined by the setting of the VAR Ø control, R550. The voltage range of R550 is established by reference voltage supplies U1400B (−) and U1400C (+). These are the same reference voltages supplied to the Level Comparators. This arrangement permits comparison of the triangle voltage with the maximum possible positive and negative levels, and all levels between.

When the triangle voltage exceeds the reference voltage set by the VAR Ø control, Q1711 turns off. Any current flowing through Q1621 now flows through Q1611.

CURRENT AMPLIFIER

Current flowing through Q1611 also flows through R1622 and is amplified by Q1521. Temperature compensation for this amplifier is provided by CR1621. Differential pair Q1511 and Q1523 serve as a current switch. With Q1511 turned off, any current amplified by Q1521 passes through Q1523 to the junction of CR1531 and CR1533. When the timing capacitor voltage rises to the threshold level set by the VAR Ø control, R550, it is clamped. Q1523 now draws exactly the amount of current that the positive current source supplies. Because the square wave at pin 5 (Q) of U1600A drives the base of Q1511, the clamping action only happens during the positive edge of the triangle wave. On the negative transition, Q1523 is shut off, and Q1511 is on. In this manner, the timing capacitor voltage can be clamped at any desired positive level.

TRIG/GATE AMP AND SINE SHAPER ③

TRIG/GATE AMP AND LOGIC

The input trigger amplifier consists of an emitter coupled differential pair (Q1320 and Q1322), current amplifier Q1324, and the required logic circuitry to control the operation of the main loop phase clamp. Input circuit protection is provided by R1203, R1204, CR1220 and CR1221. Triggering signals are applied either through front panel connector J520 or interface connections on the rear edge of the Main circuit board.

The differential pair, Q1320-Q1322, responds to the input signal when the voltage rises above (+ SLOPE) the reference voltage at the base of Q1320. This reference voltage is established by divider network R1312 and R1314. The position of S1400D, SLOPE switch, determines whether a positive or negative going input will cause the amplifier Q1324 to conduct. When the threshold level is exceeded and conduction starts, current flow through the circuit causes a voltage to be developed across R1322. This voltage is applied to the base of Q1324. The output at the collector of Q1324 is a TTL compatible waveform to drive the logic circuit, U1310. CR1320 provides temperature compensation for Q1324.

Three modes of operation are selectable with S1400; Triggered, Gated, and Free Running.

In the TRIG mode, S1400A and S1400C are positioned such that the output, pin 6, of U1310B is connected to pin 4, set input, of U1600A. In this mode, a very narrow, negative going voltage pulse is developed by U1310B each time the input waveform passes through the trigger threshold. This low sets U1600A, which deactivates the phase clamp until the triangle generator again starts in the positive direction, and allows the generator to complete one full cycle.

In the GATE mode, S1400A and S1400C are positioned such that the output, pin 3, of U1310A is connected to pin 4, set input, of U1600A. In this mode, a low level is produced whenever the input waveform exceeds the threshold if + SLOPE is selected. The generator free runs as long as this condition exists. As soon as the level at the input connector drops below the threshold, the output voltage of U1310A rises. This high level causes the generator to again stop running when the phase clamp reaches its threshold level at the end of the last complete cycle.

In the FREE RUN mode, S1400A is positioned such that pin 4 of U1600A is held low. The generator now outputs continuous waveforms.

SINE SHAPER

The Sine Shaper is composed of three separate circuit functions: a Transconductance Amplifier, the Shaper Circuitry, and an Output Buffer.

Transconductance Amplifier. Emitter coupled transistors Q1210 and Q1212 along with current source Q1200 form the Transconductance Amplifier. The amplifier converts the triangle voltage at the base of Q1212 to a differential current. This current flows through two sets of diode wired transistors, U1120C, U1120D, U1220C, and U1220D, to the input of the shaper.

Shaper. The active portion of the Shaper is formed by two sets of emitter coupled transistors U1220A, U1220B, U1120A and U1120B. These devices have their inputs wired in series and their outputs cross coupled. U1120E and U1220E are current sources for these devices. The circuit operates by generating a power series approximation to the sine function. The devices in U1120 generate the first order term while those in U1220 generate the second order term in the approximation.

Output Buffer. The Output Buffer is an operational amplifier that converts the differential current from Q1010 and U1020D to a single ended voltage that is applied, through the function switch, to the output amplifier. U1020E is a current source for the emitter coupled differential input pair U1020A and U1020B. Q1012 serves as a current mirror for U1020A and as an active load for U1020B. U1020C is the output emitter follower and R1020 is the feedback resistor.

OUTPUT AMPLIFIER & ATTENUATORS ④

The output amplifier is basically a noninverting operational amplifier whose plus input is the base of Q2101 and minus input is the base of Q2113.

The three basic waveforms are selected by S1901 and applied across R560B and R2335 to the input stage of the amplifier. R560B varies the amplitude of the selected waveform. The feedback network consists of R2011 and R2012, connected from the output to the minus input of the amplifier. C2011 provides high frequency compensation for the feedback, and is used to adjust the squarewave front corner. The input pair, Q2101 and Q2113, amplify the difference between the input waveform and the fedback waveform.

An offset current is also summed with the feedback signal at the base of Q2113 when S510A is closed. This allows R560A to control the dc offset of the output signal.

The output of Q2101 is applied directly to Q2111 which is cascoded with Q2011. The output of Q2113 passes through an inverting amplifier, Q2211, before passing to Q2213 cascoded with Q2311. CR2111 provides temperature compensation for Q2211. The two cascodes form drivers for the amplifier output stage.

The output stage consists of Q2013 and Q2123 in parallel with Q2121 for amplification of positive going signals. Q2321 and Q2323 in parallel with Q2325 form the amplifier for negative going signals. The output is taken at the junction of R2026 and R2228. The 50 Ω output impedance is determined by parallel 100 Ω resistors R2033 and R2131. C2121 in this network provides high frequency compensation for the output impedance. The attenuator circuit is a constant impedance resistive divider network, switch selectable in 20 dB steps.

POWER SUPPLY ⑤

The FG 501A receives its power from the power module via interface connections on the rear edge of the Main circuit board. The power module supplies plus (+) and minus (—) 33.5 Vdc (unregulated) from which the following regulated voltages are generated.

+20 V SUPPLY

The +33.5 V from the power module is filtered and applied to voltage regulator U1210 (pins 11 and 12). This regulator contains its own reference, operational amplifier, and current limiting elements. The output of the regulator is applied to Q1231 which serves as a driver the the series pass transistor located in the power module. The +20 V output is applied across voltage divider R1201, R1301, and R1315. The output level of the supply is set by R1301 (+15 V Adj) which compares the supply output to the internal reference level of the regulator. This supply is current limited through the action of R1121 and the current limiting element in the regulator. When excessive amounts of current are drawn from the supply, the voltage developed across R1121 turns on the current limiting element in the regulator (U1210). This action reduces the base drive, through Q1231, to the series pass transistor causing the supply to reduce output. This supply is the reference for other supplies in the FG 501A.

+15 V SUPPLY

The +15 V supply consists of U1230D and Q1221. U1230D serves as an error amplifier which compares the +15 V output of the supply to a +15 V reference developed by divider network R1231, R1232 and R1233 from the +20 V supply. Since this supply is sourced from the +20 V, it is inherently current limited by the +20 V supply.

+5 V SUPPLY

The +5 V supply consists of U1230C and Q1331. U1230C serves as an error amplifier which compares the +5 V output to a +5 V reference developed by divider network R1231, R1232 and R1233 from the +20 V supply. Since this supply is sourced from the +15 V and referenced to the +20 V supply, it is inherently current limited under the same conditions that limit those supplies.

—20 V SUPPLY

The —20 V supply is derived from —33.5 V supplied by the power module. The output of operational amplifier U1230A is applied, through Q1245, to the base of Q1241, which serves as a driver for the series pass transistor located in the power module. This supply is also referenced to the +20 V. The supply is current limited through the action of R1141 and Q1243. When excessive amounts of current are drawn through R1141, a voltage sufficient to turn Q1243 on develops across R1141. This action reduces the base drive to the series pass transistor causing the supply to reduce output.

—15 V SUPPLY

The —15 V supply consists of operational amplifier (U1230B) and a series pass feedback regulator (Q1345). The output of the supply is fed back through divider network R1247, R1341, and R1245. The output level is adjusted by R1341. Because this supply is sourced from the —20 V supply, it is current limited by the —20 V supply.