070-7205-00
Product Group 45

RTD 710A DIGITIZER Service Volume I

WARNING

THE INSTRUCTIONS INCLUDED IN THIS MANUAL ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO. REFER TO THE SERVICE SAFETY SUMMARY PRIOR TO PERFORMING ANY SERVICE

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INSTRUMENT SERIAL NUMBERS

Each instrument has a serial number on a panel insert, tag, or stamped on the chassis. The first number or letter designates the country of manufacture. The last five digits of the serial number are assigned sequentially and are unique to each instrument. Those manufactured in the United States have six unique digits. The country of manufacture is identified as follows:

B000000	Tektronix, Inc., Beaverton, Oregon, USA
100000	Tektronix Guernsey, Ltd., Channel Islands
200000	Tektronix United Kingdom, Ltd., London
300000	Sony/Tektonix, Japan
700000	Tektronix Holland, NV, Heerenveen, The Netherlands

PREFACE

GUIDE TO RTD 710A DOCUMENTATION

The RTD 710A Digitzer documentation provides information necessary to install, operate, and service the instrument. It consists of:

- an **Instruction Manual** that describes the instrument, tells how to prepare the instrument for use, explains the controls and connectors, provides operator familiarization, includes the IEEE 488 command set and programming examples, and provides instructions for internal control settings and rackmounting instructions for service personnel.
- an optional two volume **Service Manual** that provides information for qualified service personnel to troubleshoot, repair, and calibrate the instrument.
- an **Instrument Interfacing Guide** that helps the user get started using the instrument by providing more detailed interface and programming information.
- a **Rackmount Kit for the RTD 710A** instruction sheet that provides installation instructions and parts lists for the RTD 710A rack mounting kit.

Table 0-1 lists the Tektronix part numbers and titles of the available RTD 710A documentation.

Table 0-1
RTD 710A DOCUMENTATION

Part Number	Document Title
070-7204-XX	Instruction Manual
070-7205-XX	Service Manual, Volume 1
070-7206-XX	Service Manual, Volume 2
070-7207-XX	Instrument Interfacing Guide
070-7208-XX	Rackmount Kit for RTD 710/RTD710A

ABOUT THIS MANUAL

The RTD 710A Service Manual, which is contained in two volumes, provides information to troubleshoot, repair, and calibrate the instrument.

VOLUME 1

Section 1 - Theory of Operations contains a block diagram and detailed circuit description for the RTD 710A circuit operation.

Section 2 - Diagnostics contains detailed descriptions for the diagnostic routines contained in the RTD 710A Firmware and how to use them.

Section 3 - Maintenance contains four major subsections. Static-Sensitive Components contains information about handling and servicing static-sensitive components. Preventive Maintenance provides information about inspecting, cleaning, and calibrating the instrument, Troubleshooting and Repair provides information about replacement parts, and describes what tools (software, hardware, and documentation) are available for troubleshooting and repairing the instrument. Removal and Replacement Procedures contains instructions for removing and reinstalling all circuit boards in the in instrument.

Section 4 - Performance Check/Adjustment Procedures contains a list of test equipment and the procedures required to perform check and/or adjust the instrument.

Section 5 - Replaceable Electrical Parts contains a list of all electronic parts in the instrument.

VOLUME 2

Section 6 - Test Point and Adjustment Locations contains an illustration showing the location of the test points and adjustable components for each circuit board adjusted during calibration.

Section 7 - Troubleshooting Charts contains flow charts that can be used with the internal diagnostics to isolate an instrument problem.

Section 8 - Diagrams and Circuit Board Illustrations contains schematic diagrams and circuit board illustrations for each printed circuit board in the instrument.

Section 9 - Replaceable Mechanical Parts contains exploded view illustrations and parts lists for the mechanical parts and assemblies in the instrument.

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BLOCK DIAGRAM DESCRIPTION

ACQUISITION MODULES

The RTD 710A acquisition modules (Figure 1-1) accept 2-Channel analog input signals, convert those signals to digital form, and apply time base and other information in preparation for further processing.

Input Amplifier

The input amplifier modules contain input attenuators, input amplifiers, amplifier control circuits, and an auto-calibration reference signal generator.

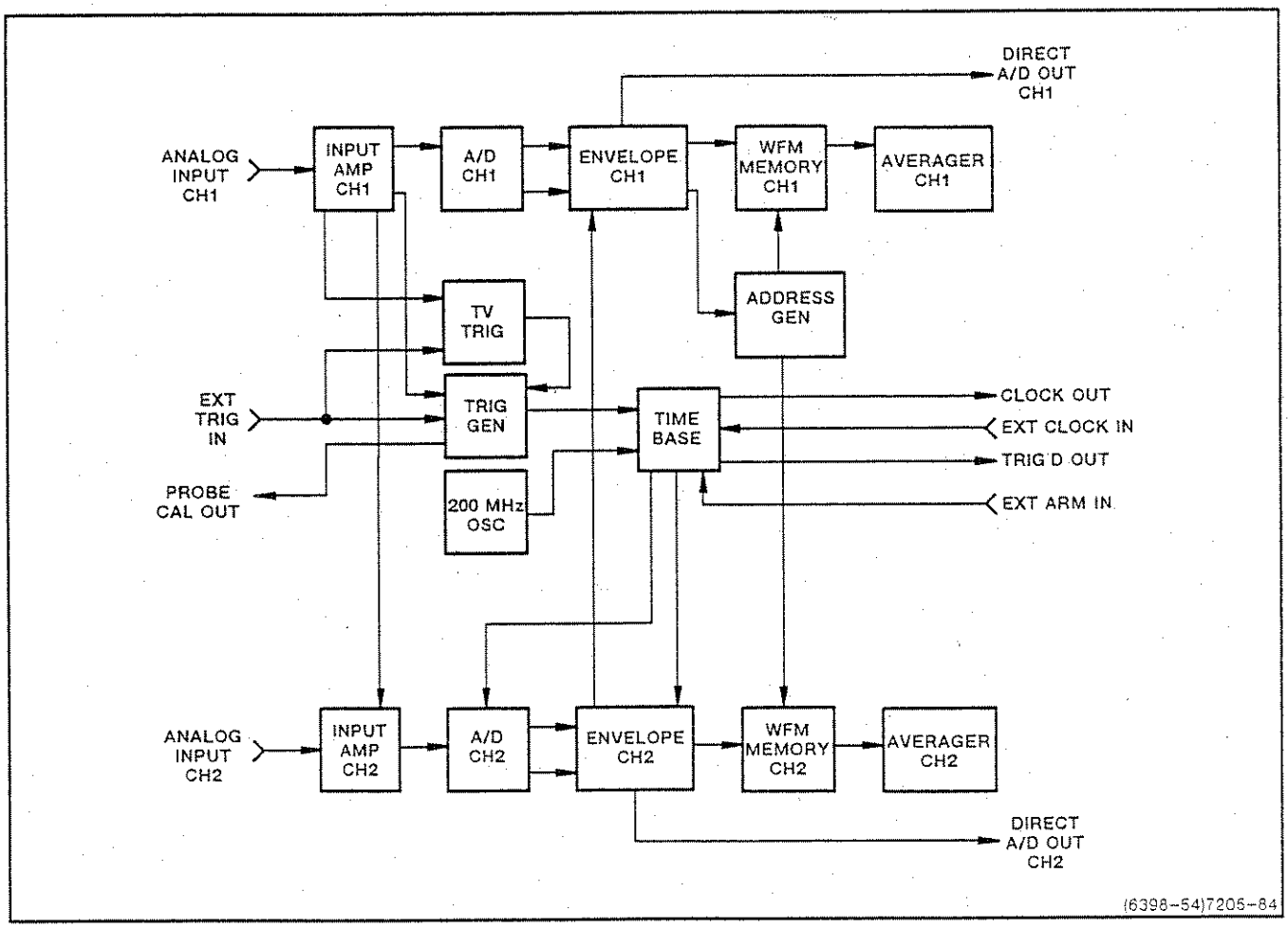


Fig. 1-1 Simplified Block Diagram of RTD 710A

Analog signals connected to Channel 1 and 2 are applied to the input amplifiers through 1 megohm attenuators. These attenuators provide 1X, 10X or 100X attenuation to reduce the input signal level to the dynamic range of the input amplifiers. Input coupling may be either ac or dc. The analog input connectors have a probe coding ring that provides a probe attenuation signal to the MPU.

Each input amplifier amplifies the signal as appropriate to drive the A/D converters, provides input dc offset, 20 MHz bandpass filtering, and internal trigger signals. When the sampling mode is set to high speed (interleave sampling mode), the Channel 1 signal is fed directly into the Channel 2 input amplifier, thus applying identical input signals to both A/D converters. The input amplifier range, offset, vertical mode, auto calibration, and bandwidth limit are controlled by the MPU.

The auto-calibration reference signal generator generates a 1 kHz square waveform for gain calibration and a 28.57 MHz sawtooth waveform for phase calibration. The timing signals for these reference signals are supplied respectively by the DMA module and the Time Base module.

When the TV Trigger (Option 05) is installed, the Channel 1 signal and a buffered Channel 1 input signal from the front-end of the Channel 1 input amplifier are applied to the TV Trigger Board for the back-porch clamping and TV line or Field triggering capabilities. The TV Trigger Board provides a Channel 1 offset signal to the Channel 1 amplifier to control back-porch clamping.

A/D Converter

The A/D converter modules consist of a sample-and-hold (track-and-hold) circuit and a 10-bit A/D converter for each channel. Each A/D converter samples the input signal(s) from an input amplifier at some specified clock rate and digitizes each sample (point) into 10-bit binary data. When the sampling clock is set to 5 ns (high-speed sampling mode), the Channel 1 input is fed to both A/D Converters and their sampling clocks run at 10 ns with a 180 degree phase relation between them. With this combination of sampling clock rates and phase relationship, the effective sampling frequency (10 ns) is doubled (5 ns). The digitized data and clocks, which are delayed through A/D circuitry are sent to the Envelope Board where the two 10-bit data words (one per channel) are synchronized with the clock signal for writing to memory.

The A/D converters also produce an overrange signal when the input signal exceeds the input range limit. This signal is sent to the front panel via the MPU.

Envelope

The envelope module receives 10-bit data from both A/D converters and synchronizes these two data when in the high-speed sampling mode. This data also is buffered and sent to the Direct A/D Out connector on the rear panel.

If the envelope mode is not selected, digitized data from the A/D converter is sent directly to the data shift circuit, where it is prepared to be sent simultaneously to memory as two consecutive 10-bit data words. This extends the cycle time for writing to memory. The shifted data is latched by a latch clock with a frequency of half the sampling clock to make up 40-bit (20 bits per channel) data lines.

Waveform Memory

The waveform memory module receives and shifts the 20 bit per channel data into 80 bits per channel to extend the cycle time for memory to 1/8th of the sampling clock. Each waveform memory can be loaded with data at clock intervals as short as 80 ns and also can be written by the MPU. Stored data can be read by either the MPU or the averager module. Output lines from the waveform memory are connected so as to organize data into 10 bits per channel.

Average

The averager module contains an averaging memory, adder circuit, and an address generator. A 24-bit wide, 8K word per channel deep averaging memory allows a maximum of 16,384 averages of 10-bit words.

This module receives 10-bit data from the waveform memory after an acquisition is completed, adds it to previous summed data in the averager memory, and restores the newly added data into the averager memory. After N-times acquisition process is complete, the added data in the average memory is divided by N.

Trigger Generator

The trigger circuit detects the occurrence of a trigger meeting the level and setup conditions. It consists of a source selector, trigger coupling selector, trigger detector (high-speed comparator), slope selector, and reference voltage sources. A source-selected trigger signal is applied through the trigger coupling selector to a comparator where the trigger pulse is generated if the signal meets the level and setup conditions. This trigger pulse is applied through a slope selector to the Time Base module.

The trigger module provides a 4 V, 1 kHz probe calibration signal to a front panel connector for making low-frequency probe adjustments.

TV Trigger Circuit (Option 05)

The TV trigger circuit performs both video processing and trigger generation. A video processor stabilizes the input signal selected by the trigger source selector and separates the video sync signals (horizontal and vertical sync pulses) from the input video signal. A wide range of video signals are accommodated through automatic gain control that sets the level into the sync separator. Separated sync pulses are counted to permit the user to select the specific TV line number that will produce the trigger event. Back-porch clamping is available for the Channel 1 input, and when selected, removes or reduces the level of ac line hum that may accompany the composite video signal.

Time Base

The time base module contains a sampling clock generator, envelope clock generator, breakpoint controller, arm timing controller, acquisition start/stop control, automatic clock-phase control circuit, and reference clock signal generator.

The sampling and envelope clock generators include a counter that scales either the internal 200 MHz oscillator, or external clock signals, to provide selectable sample and envelope clock rates. The clock source is selected by a clock source selector.

In pre-trigger mode (negative trigger delay), the instrument continues to write the waveform until the specified memory segment is full, then a trigger is accepted. If the memory fills and no trigger is received, the memory address returns to the beginning of the specified segment and overwrites the data in a cyclic ring-like action. When a trigger signal occurs, pre-trigger writing terminates and the specified number of samples after the trigger are acquired.

In post-trigger mode (positive trigger delay), waveform data is written after the trigger occurs and the specified delay time has elapsed.

The breakpoint control circuit checks the writing memory address, and when it reaches the breakpoint address, a new sample interval is programmed into the sampling clock generator.

The arm delay timing circuit provides conventional trigger holdoff, which inhibits the trigger pulse until the arm delay period has elapsed.

The reference clock generator produces a 28.57 MHz clock signal that are applied to the auto-cal reference signal generator in the input amplifier.

The time base module outputs a TRIG'D signal whenever it detects a valid trigger. It also provides a buffered clock output at the rear panel.

200 MHz Oscillator

The 200 MHz oscillator module generates the 200 MHz system clock and applies it to the time base module.

Address Generator

The address generator module assigns the address to which waveform data is stored in memory. It consists of a writing address generator and an address select circuit, whose outputs are applied to the waveform memory module. The writing address generator also supports the memory segmentation function. When the MPU reads from or writes to waveform memory, the address selector selects the address signal generated by the MPU.

PROCESSING/COMMUNICATION MODULES

The instrument processing/communication modules control digitizer operations, provide the display and human interface, and provide for communications external to the instrument.

Display Controller

The display controller generates the display drive signals. It consists of the display RAM, D/A converter, read address generator, and drive amplifier. Acquired waveform data in waveform memory is sent to the display RAM by the MPU and DMA controller, converted to XYZ analog values by the D/A converter, and applied through drive amplifiers to the CRT monitor.

Keyboard

The keyboard module provides for direct operator interface and includes a key matrix, 7-segment LED displays, and indicator LEDs. Except for STATUS LEDs, the LEDs are controlled by the MPU. All buttons and switches, except the front-panel On-Stand-By Power Switch, are sensed by the MPU.

68000 MPU

The MPU module (Figure 1-2) directly controls signal processing, and consists of a 68000 CPU with 8 MHz clock, system ROM, system RAM, 23-bit address bus, and separate 16-bit data bus that requires no multiplexing. It also controls all instrument functions. The MPU address and data bus are connected to all acquisition modules for programming by the

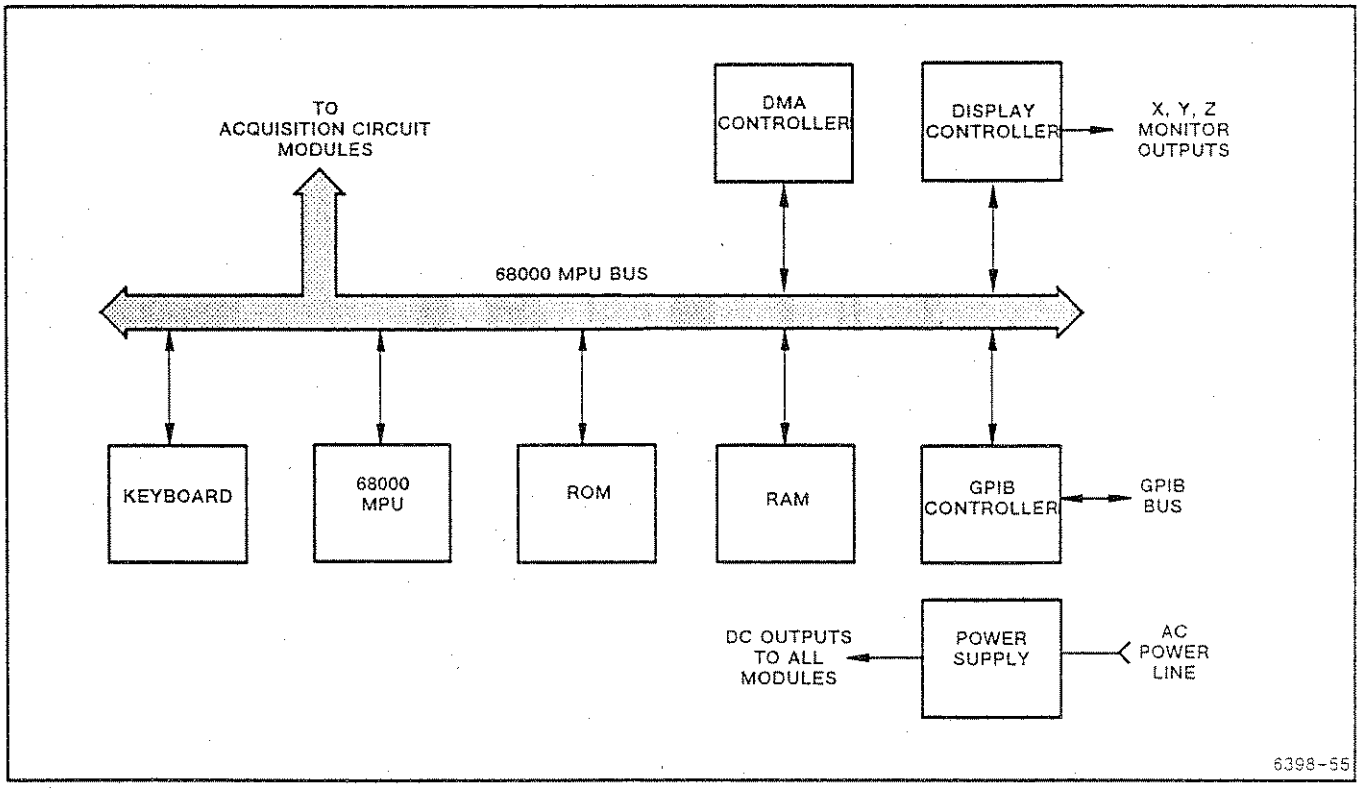


Fig. 1-2 68000 MPU System

MPU. Addresses are decoded to access the memory mapped devices on the data bus. An interrupt circuit enables devices on the bus to request servicing when necessary. A power-up reset circuit permits an orderly power on and off sequence.

RAM

The system RAM module provides temporary storage of data for various control functions. It consists of two 32K x 8 RAMs.

ROM

The system ROM module provides for storage of the firmware program that controls the operation of the instrument. It consists of two 128K X 8 EPROMs.

DMA Controller

The DMA controller module controls high-speed data transfers between waveform memory and the GPIB. It also contains non-volatile memory for storing front-panel settings. This non-volatile memory contains battery back up to maintain the stored settings when the power is off.

GPIB Controller

The GPIB controller module controls all external communications to or from the instrument using the built-in capabilities of an LSI 9914 talker/listener device.

Power Supply

The high-efficiency switching power supply module provides power for all instrument modules. Ac input power of 48 Hz to 66 Hz is rectified and used to drive a switching circuit at a frequency of approximately 50 kHz. Regulation of the switching transformer is controlled by pulse width modulation (PWM) using feedback from one of the rectified outputs to control the on-time of the switching transistors. Automatic overvoltage and overcurrent sensing circuits shut down switching if either overload occurs. The ac input includes an EMI filter, primary line fuse, and principal power switch. Thermal cutoff shuts down the power supply in the event of overheating.

Secondary regulators remove ac noise and ripple from the rectified output voltages. Each regulator automatically limits the output current to prevent it from exceeding the normal power limit.

The power supply module also provides a power fail interrupt signal to notify the MPU of anomalies in the power supply.

DETAILED CIRCUIT DESCRIPTION

This subsection describes the detailed electrical operation and circuit relationships of the instrument. It describes only those circuits that are unique to the instrument. It does not describe circuits common to the electronics industry. Referenced figures and tables are included in text; referenced schematic diagrams are located in the Diagrams and Circuit Board Illustrations section of Volume 2 of this manual.

INPUT AMPLIFIER

Each input amplifier (one for each channel) provides for selectable amplification of the input signal (with minimum distortion and maximum stability) for application to the A/D Converters. Figure 1-3 is a block diagram of the Input Amplifier. Except for the TV Trigger option, vertical mode switching, and MPU interface, the Channel 2 input amplifier has the same configuration as Channel 1. Therefore, only the operation of Channel 1 is explained here; Channel 2 is explained later under its relevant schematic diagram.

The input signal is applied to the input attenuator, which attenuates the signal by selectable factors of 1, 10, or 100. After impedance transformation at the source follower and output buffer, the signal is applied to a input amplifier for gain switching.

This combination enables settings from a $\pm$0.1 to 50 V full scale through a 1, 1.25, 1.6, 2, 2.5, 3.2, 4, 5, 6.2 and 8 sequence.

The input amp IC includes a bandwidth-limiting filter (fc = 20 MHz). A TV trigger pick off circuit provides a trigger signal to the TV trigger option circuit. The trigger buffer supplies a trigger signal for the internal trigger. Vertical mode switching connects the Channel 1 signal to the interface amplifiers of both Channels 1 and 2 in the high-speed sample mode.

CH1 AND CH2 ATTENUATORS (DIAGRAM 1)

The attenuator consists of input coupling, gain cal reference signal selector, attenuator, source follower, and output buffer (Figure 1-4). Attenuators for both channels are basically the same.

Source follower Q100 tranforms the high-impedance input signal to low impedance and applies it to output buffer U100. The gain cal (GC) reference signal GC SIG is applied through reed relay K104.

The output buffer U100 further transforms the source follower output to low impedance and drives the 75 ohm cable. Buffer output ATT OUT1 is applied through the 75 ohm cable to the Input Amplifier.

CH1 AND CH2 AMPLIFIER (DIAGRAM 2)

Output from the attenuator is applied to the amplifier IC for gain-switching then coupled to the Interface Amplifier stage. Maximum signal output voltage of the Interface Amplifier is 3 Vp-p. The Interface Amplifier output is amplified through output buffers to both A18 A/D Converter Board and A22 Trigger Board.

This circuit block includes a Vertical mode switching circuit that works during the High-speed sampling mode to provide the output of the Channel 1 amplifier IC to both Channel 1 and Channel 2 Interface amplifiers and to perform the Channel 2 dc and gain calibration.

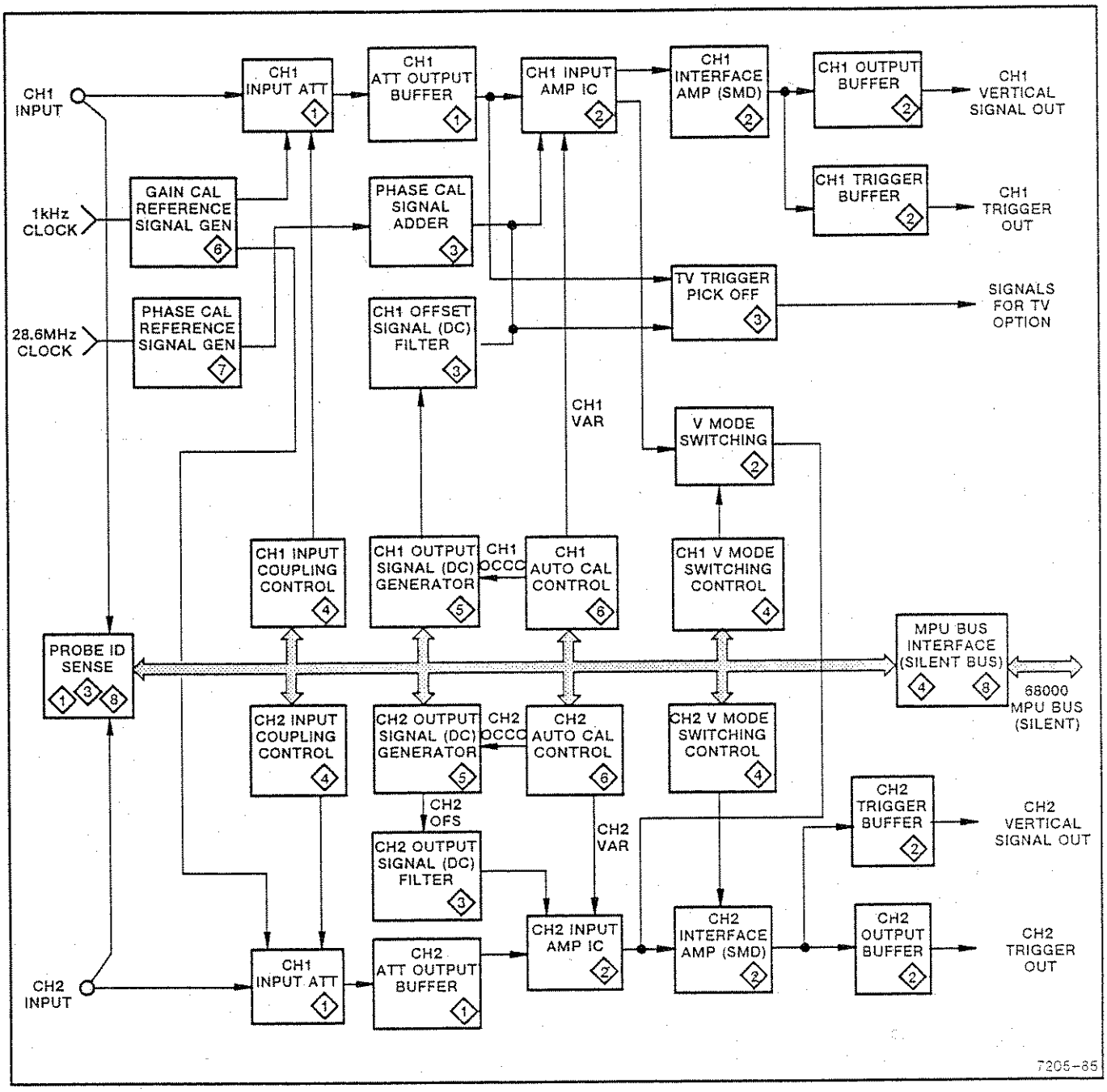


Fig. 1-3 Input Amplifier Block Diagram

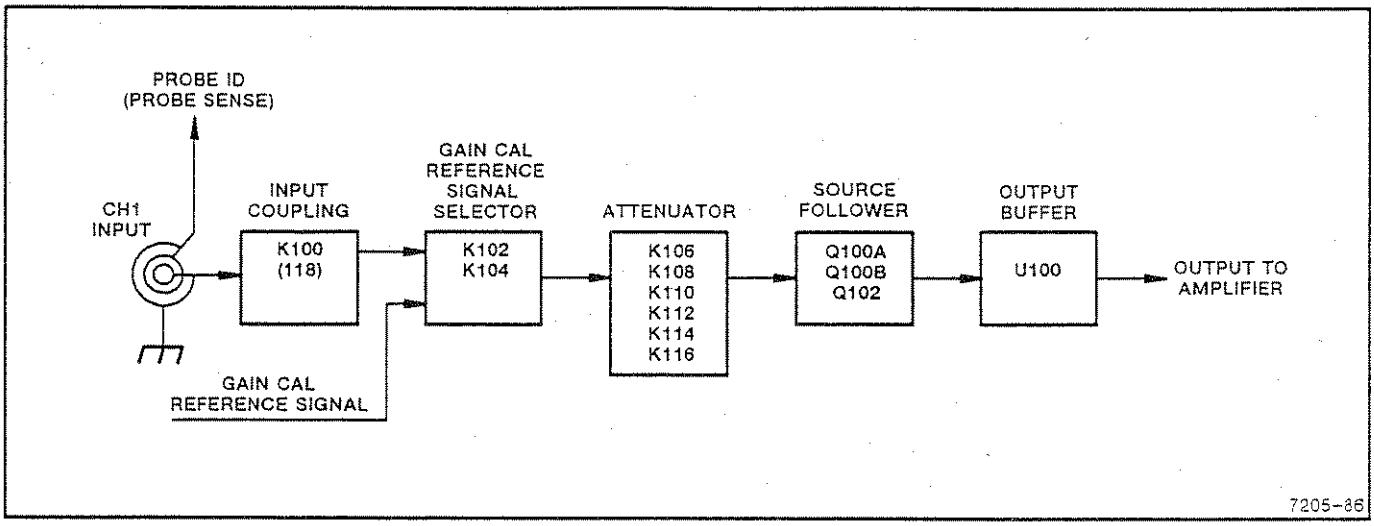


Fig. 1-4 Attenuator Block Diagram

Input Amplifier

The input amplifier IC U100 is a wideband general purpose differential amplifier with a BW limit filter, output buffers and a control logic. Its operation is controlled through control logic by the MPU.

The output, ATT OUT1, from the Attenuator is applied to a non-inverting output of differential amplifier U100. The ATT OUT1 signal, along with offset signal CH1 OFS is fed to the signal inverting input of a differential amplifier. The is amplified differentially and gain switched by both the U100 TTL level gain select input signals, 1G0, 1G1, and 1G2 and gain control analog input signal CH1 VAR. The total gain of the amplifier IC U100 is determined as follows:

GAIN = Gnom x (CH1 VAR + 1) /2

where Gnom is the amplifier's pre-fixed nominal gain selected by the 1G0, 1G1, 1G2 inputs as shown by the following table:

1G2	1G1	1G0	Gnom
1	1	-	1.2
1	0	-	3.0
0	1	1	6.0

CH1 VAR is an analog input voltage capable of continously varying the GAIN control from 0 to Gnom. The CH1 VAR signal is measured in volts.

Thus the RTD710A Input Amplifier, with MPU control of these signals (1G0, 1G1, 1G2, and CH1 VAR), is gain controlled at each input range settings as shown in Table 1-1.

Other TTL digital control inputs to the amplifier IC U100 are BW, EN and INV. BW signal to B1 input (pin 33) enables/disables internal 20 MHz Bandwidth filter; EN signal enables/disables the amplifier's output buffer. Inputs EN1 through EN3 (pin 12, 16, and 18) are the enable/disable signals for the output buffers OB1, OB2, and OB3. OB1 is enabled by pulling-up the EN1 output, and OB2 is disabled by connecting EN2 input to the ground. OB3 is the only controllable input and is enabled by the 1EN3 signal when the High-speed sample mode is selected. For channel 2, both the EN2 and EN3 inputs of the Channel 2 amplifier IC are disabled and the EN1 input is controlled by 2EN1 signal. 2EN1 goes low to disable output buffer OB1 when the High-speed sample mode is selected. INV is used to invert the output of the amplifier IC. Pulling INV low (grounded) inverts the output. Control input, HF ADJ adjusts gain over 100 MHz.

Gain-switching brings the maximum output voltage (full-scale voltage) of the amplifier IC U100 at any input range settings to 0.6 Vp-p. Figure 1-5 shows gain distribution and maximum output on each amplifier stage of the Input amplifier including the Attenuator. The gain-switched differential output signal from the output buffer of the amplifier IC has a 100 ohm output impedance. Externally connected load resistance R200 and R202 divide the amplifier IC gain to the desired value.

Interface Amplifier & Output Buffers

The differential analog output signal from amplifier U100 is applied to interface amplifier U200, a SMD (Surface Mounting Devices) module. U100 amplifies the signal by 5 times, converts the signal to single-ended, and applies its output to the load resistance R204. Thus the maximum output voltage at this stage is 3 Vp-p. Both the Q250 circuit and the Q265 circuit supply power to CR300 a limiter diode. This limiter circuit is provided to prevent the amplifier from saturating when an extremely high input signal is applied, and reduces recovery time. R214 is a coarse DC level control to adjust the U200 output to zero volt when its differential input is zero volt.

Signal output from U200 is applied to both output buffers U300 and U350. These buffers are the same SMD modules as U100 on the Attenuator Board and convert the output of the Interface amplifier U200 to low impedance. U300 drives a 75 ohm cable and U350 drives a 50 ohm cable, the cables apply the output of the input amplifier to the A18 A/D Board and the A22 Trigger Board. R352 is inserted to attenuate the signal output for the Trigger Board to 2 Vp-p.

Vertical Mode Switching

Vertical mode switching circuit is composed of relay K100, analog switch U650 and their associating components. When the High-speed sample mode is selected, MPU turns both 1EN3 and HI/NO signals to high and both 2EN1 and ISO to low (refer to schematic 4). The output buffer OB1 of the Channel 2 amp IC U500 is disabled by the 2EN1 signal while the output buffer OB3 of the Channel 1 amp IC U100 is enabled by the 1EN3 signal. Relay K100 is switched to the Channel 1 positions by the ISO signal.

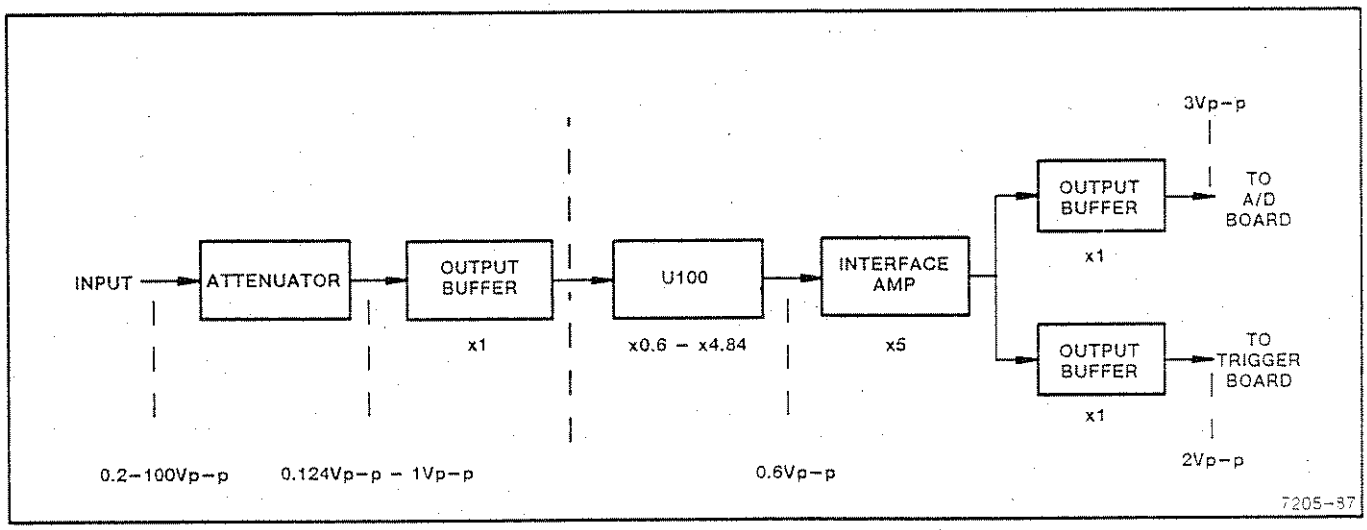


Fig. 1-5 Gain Distribution of the Input Amplifier

Thus the output signal of Channel 1 amp IC is applied to both the Channel 1 and Channel 2 interface amplifiers. At the same time the analog switch U650 is switched to its Channel 1 positions by the HI/NO signal, the Channel 2 interface amplifier U600 is automatically calibrated by its zero DC level and gain signals (HSDCC and HSGC) from the A14 AUTO CAL Board. The HSDCC signal compensates the DC level of amplifier U600 in the High-speed sample mode and the HSGC signal makes the U600 gain in the High-speed mode identical with the Channel 1 interface amplifier U200 by changing U600 board resistor R664.

TV TRIGGER PICK OFF

The TV Trigger Pick Off circuit provides the necessary signals along with the TV option circuit. The Phase Cal Signal Adder switches during phase calibration to add a reference signal to the Input Amplifier. The Offset Signal Filters remove harmful noises from the DC offset voltages. The CH1 Probe Sense senses and applies the probe ID signal to the bus.

TV Trigger Pick Off

This circuit is comprised of differential amplifier Q400A, B, Q410A, B, operational amplifier U400, analog switch U410 and their associated components. The TV sync pulse is at the maximum amplitude of the composite video signal. Thus, if the signal is clipped by the limiter when an excessive input is received, the sync pulse is reduced to a point where it becomes impossible to obtain stable triggering. To prevent this, a signal from input connector J110 of the input amplifier is converted to a single-ended signal by Q400A, Q400B, and U400A, and applied to the TV trigger circuit.

The TV Clamp option (back-porch clamp) circuit requires a stable signal with the same amplitude as the input signal, to obtain this, the CH1 DC signal is converted to a single-ended signal and applied without change. The SSA signal sent to the sync separator circuit cannot have large amplitude variation over the input range. To obtain a stable SSA signal amplitude, it is passed through a simple attenuator to ensure a signal with minimum amplitude variation. Note that this circuit is not provided in Channel 2.

Phase Cal Signal Adder

During the time phase calibration relay K160 is turned on by the PCSC signal, the reference signal PC SIG is applied to the –VIN input of amplifier U100 along with the CH1 OFS dc level control voltage. The PCSC signal and PC SIG signal are supplied from the A14 AUTO CAL Board.

Offset Signal Filters & CH1 Probe Sense

L150, C150, C152, R150, and R152 comprise a low pass filter for the Channel 1 offset signal CH1 OFS. A similar filter is provided for Channel 2.

Probe sense circuits U450 and U822B produce the signal that indicates whether a probe is being used. U450 and U822B are connected to the Probe Coding Ring of the input BNC connectors. If X10 probes are connected, the probe sense signal for the Channel (PRS1) is set high.

AMP MPU INTERFACE (Diagram 4)

The AMP MPU interface (Figure 1-6) facilitates communication between the MPU and the acquisition input circuitry, including input coupling, input range, BW limiter and VMODE select.

The input amplifier is particularly sensitive to the effects of digital circuit noise. Because the MPU bus generates noise when it is active, it is disabled during acquisition. During acquisition the MPU uses a nearly noise free Silent Bus that is enabled only when the MPU needs to access the interface circuitry. This bus, which also can be used by the input amplifier, has its buffered structure on the A22 Trigger Board. Channel 1 and Channel 2 configuration are almost similar, so Channel 1 is described below.

Input Coupling Control

The Silent MPU bus loads GD0-GB3 data (gated data bus 0 to 3) into latches U812A, U812B, U812C, and U812D, and source-drives input coupling switching reed relays U818A, U818B, U818C, and U818D. Devices U810A, U810B, U810C, and U810D provide read-back buffers for latched data during diagnostics.

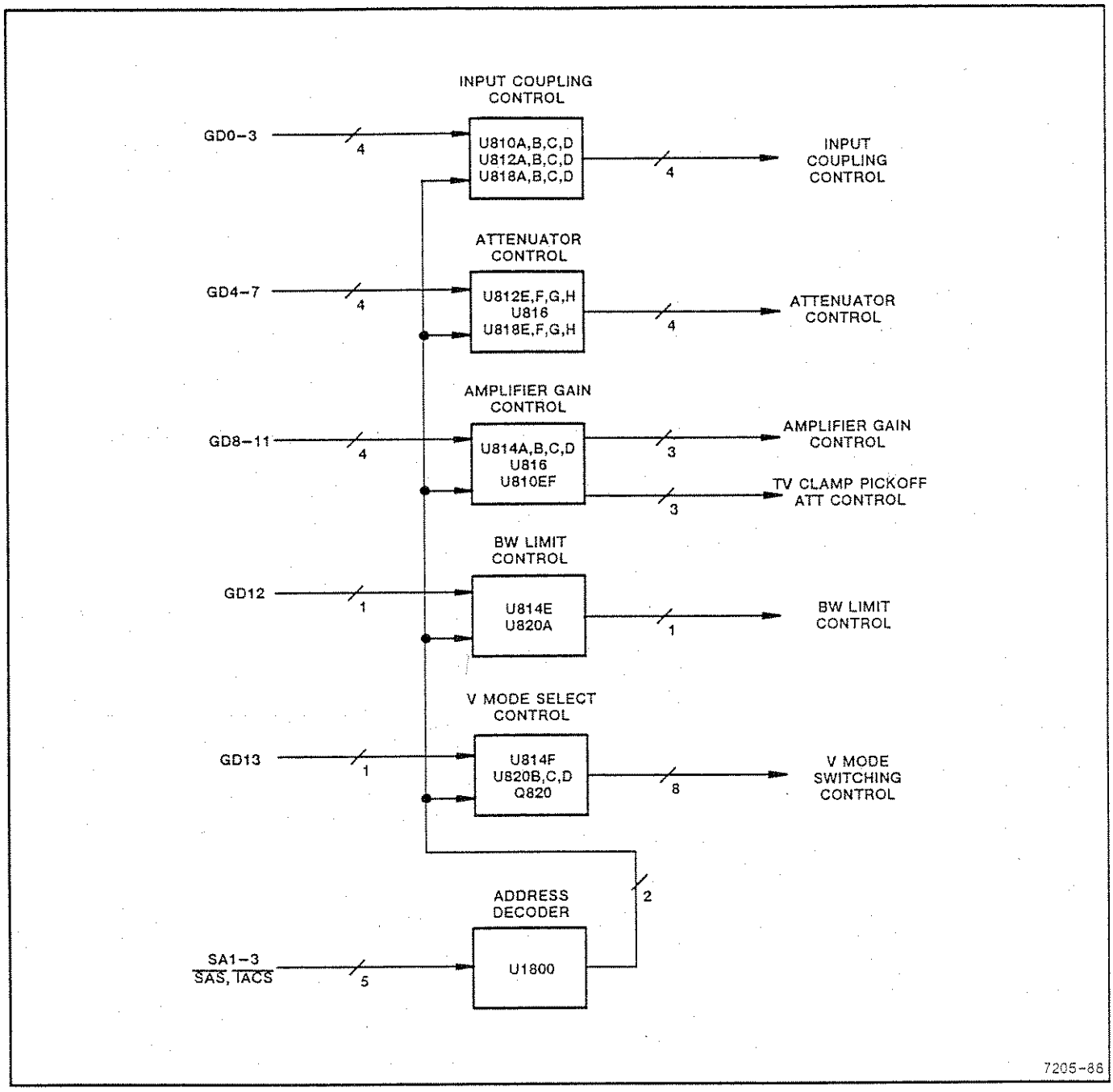


Fig. 1-6 CH1 MPU Interface Block Diagram

Input Range Control

Input range control is provided by the attenuator and amplifier gain control circuits, which will be described later.

Attenuator Control

MPU bus data GD4-GD7 is loaded into latches U812E, U812F, U812G, and U812H. Address ROM U816, used to source-drive attenuator reed relays K106 through K116 for U818E, U818F, U818G, and U818H. ROM U816 increases attenuator feed-through characteristics by opening the reed relays K106 through K116 when input coupling is set to ground.

Amplifier Gain Control

MPU data bus GD8-GD11 is loaded into latches U814A, U814B, U814C, U814D, then addresses ROM U816.

The ROM outputs 1G0-1G2 is used as the gain control signals of the input amplifier. U814 with latched data (GD9-GD11) is also used as the attenuator control signal for the TV trigger pickoff circuit. U810E, and U810F provide read-back buffers for latched data during diagnostics.

BW Limit and Vertical Mode Switching Control

After latching, MPU bus data bits GD12 and GD13 are used as the BW limit signal and vertical mode control signals (1EN3, H1/NO, 2EN1, and ISO) as described above.

Address Decoder

MPU bus address decoder U800 is used by the silent address strobe ($\overline{SAS}$) and input amplifier chip select ($\overline{IACS}$) to decode silent address bus (SA) data 1 to 3 to control latches U812 and U814 or line driver U810 described above.

CH1 AND CH2 INPUT OFFSET (Diagram 5)

The input offset circuit converts input offset data from the front panel keys or GPIB to appropriate voltages as determined by the input ranges and applies them to the input amplifier. Control voltage for DC calibration is applied to the D/A converter in this circuit. (Figure 1-7).

Polarity Selector

A positive or negative regulated reference voltage that agrees with the polarity of the specified offset is selected by analog switch U100A and U100B and through operational amplifier U100A and U100B applied to the D/A converter through U110A and U100B. When the input offset is set positive, a negative reference is selected; when the input offset is set negative, a positive reference is selected.

D/A Converter

D/A converter U120 with a built in data latch produces a dc output voltage corresponding with the input offset value. The operational amplifier circuit is comprised of U140A, resistors R100, R102, and R104. R104 is provided to add the DC calibration control voltage CH1 DCCC from the automatic calibration control circuit to the D/A converter output to provide both the input offset voltage and the dc calibration control voltage for the input amplifier.

Input Range Selector

The input range selector adjusts attenuation to provide an input offset voltage suitable for the selected input range. It consists of precision resistor array R110 and R210 and analog switches U150, U160, U210, and U220. Input range data CD0-CD3 is passed from the input offset control circuit described below under AUTO CAL MPU INTERFACE for schematic 8.

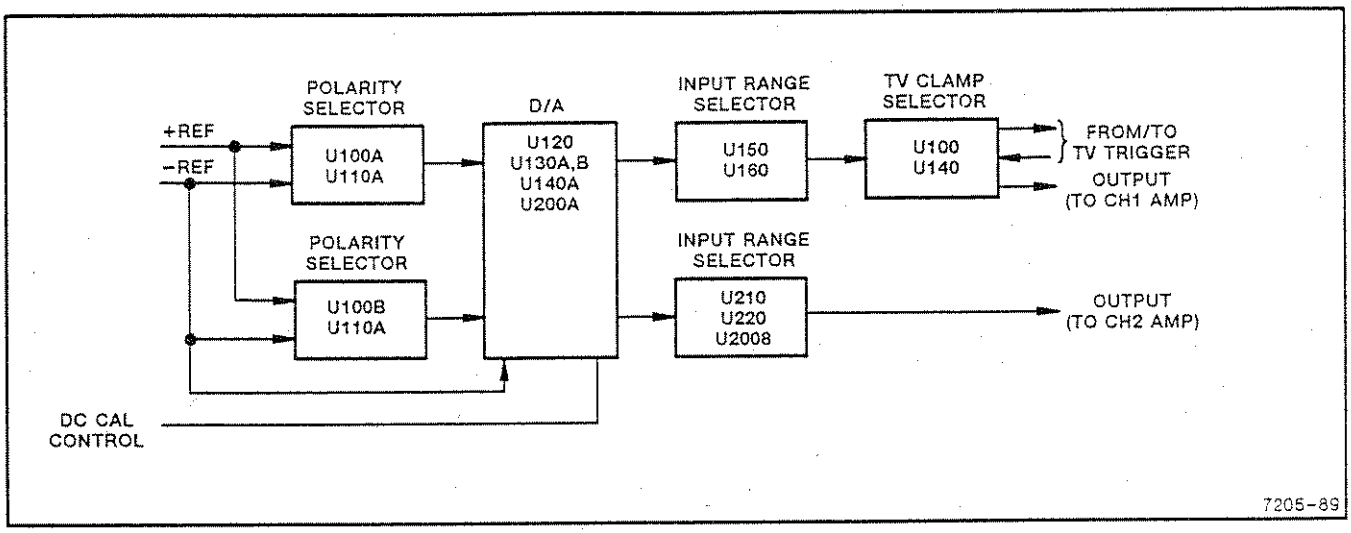


Fig. 1-7 Input Offset Block Diagram

TV Clamp Selector

TV clamp selector U100C provides switching between the usual input offset and the TV clamp offset required when the TV option is installed. If input coupling is set to TV clamp, the circuit switches to the TV OFS side, and a back-porch clamp voltage TV OFS is applied to the output buffer U140B. This circuit is for Channel 1 only.

GAIN CALIBRATION SIGNAL GENERATOR AND AUTOMATIC CALIBRATION CONTROL (Diagram 6)

The gain calibration signal generator operates only during gain calibration and diagnostics (Figure 1-8). For gain calibration, it supplies a precise 1 kHz square wave of an amplitude determined by the selected input range. When set for diagnostics, it provides a signal to the input amplifier.

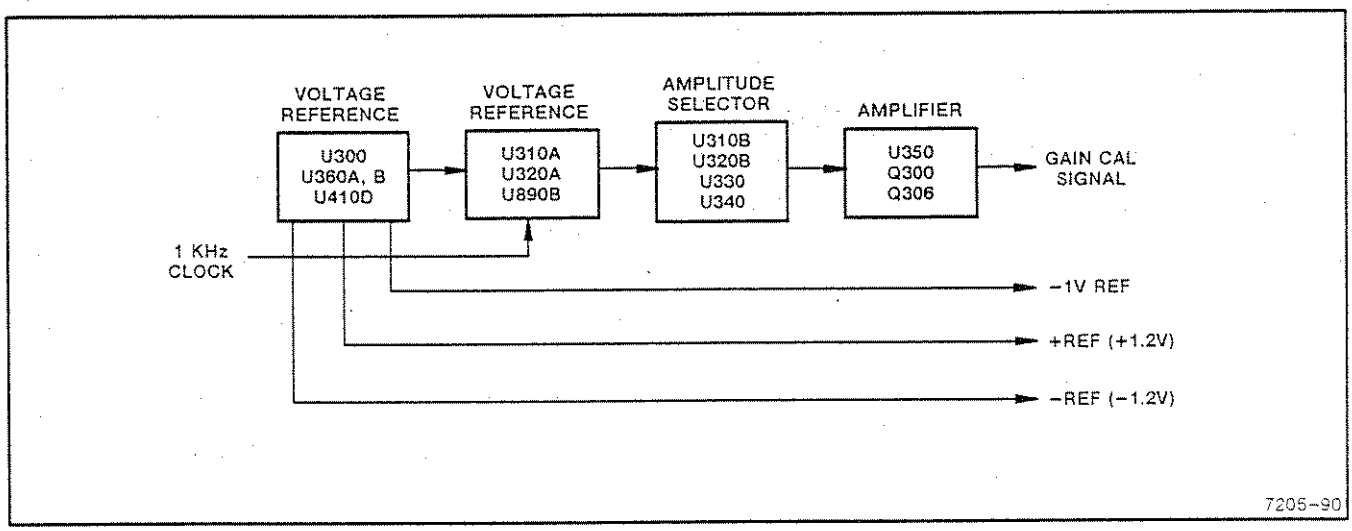


Fig. 1-8 Gain Calibration Block Diagram

Voltage Reference

Voltage reference U300 supplies stable +5.00 Vdc and –5.00 Vdc. +5V reference is converted to –1.2 V, 1.2 V, and –1 V by operational amplifiers U360A, U360B, and U410D respectively. These voltages are then used as references for the automatic calibration control and input offset circuits.

Switching

The buffered calibration clock signal (BCCLK) applied to pin 4 of U890B is a precise 1 kHz pulse with a 50% duty cycle. When gain cal is selected, GC SIG ON is high, and the clock signal switches U310A at a 1 kHz rate. When pin 10 of U310A is high, pins 15 and 1 are connected, and –5V is connected to voltage follower U320A. When pin 10 of U310 is low, pins 15 and 2 are connected and +5V is connected to U320A. Repeating this action ensures a 1 kHz square wave of precisely the required amplitude.

Amplitude Selector

The amplitude selector sets the gain calibration signal amplitude to a value suitable for the selected input range. Figure 1-9 shows gain calibration signal amplitude, Figure 1-10 shows the gain calibration signal selector circuit, and Table 1-2 shows the selector switch arrangements based on the input ranges selected.

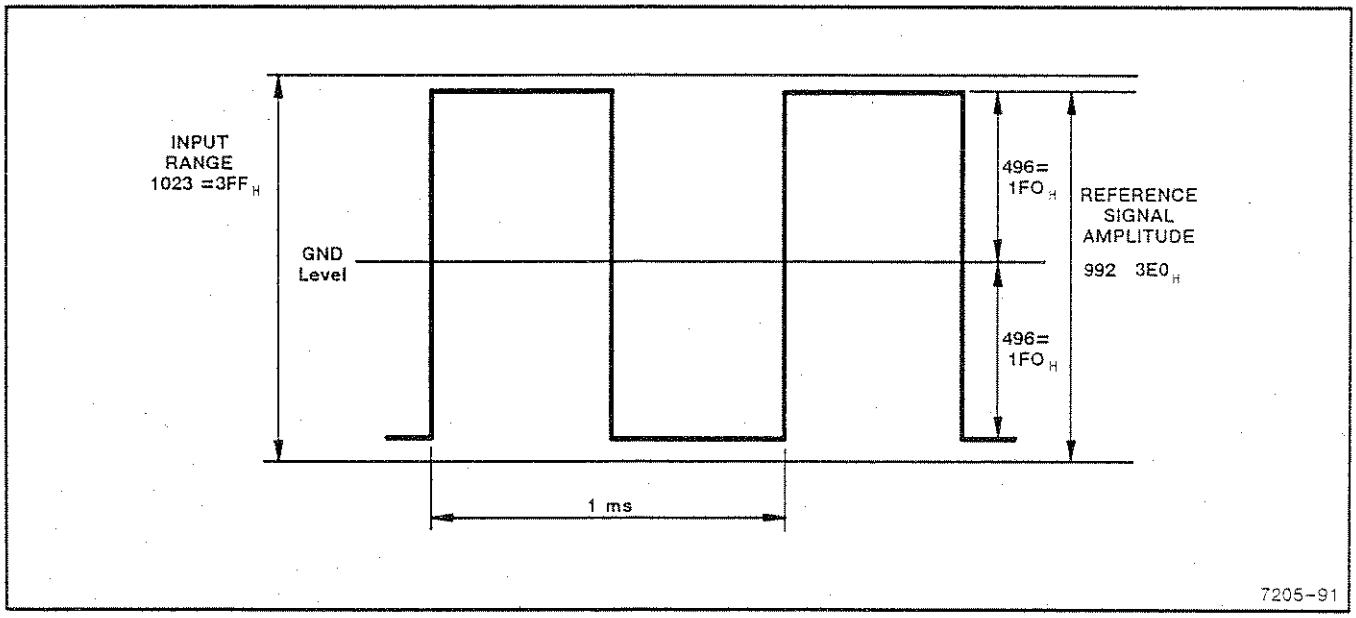


Fig. 1-9 Amplitude of Gain Calibration Signal

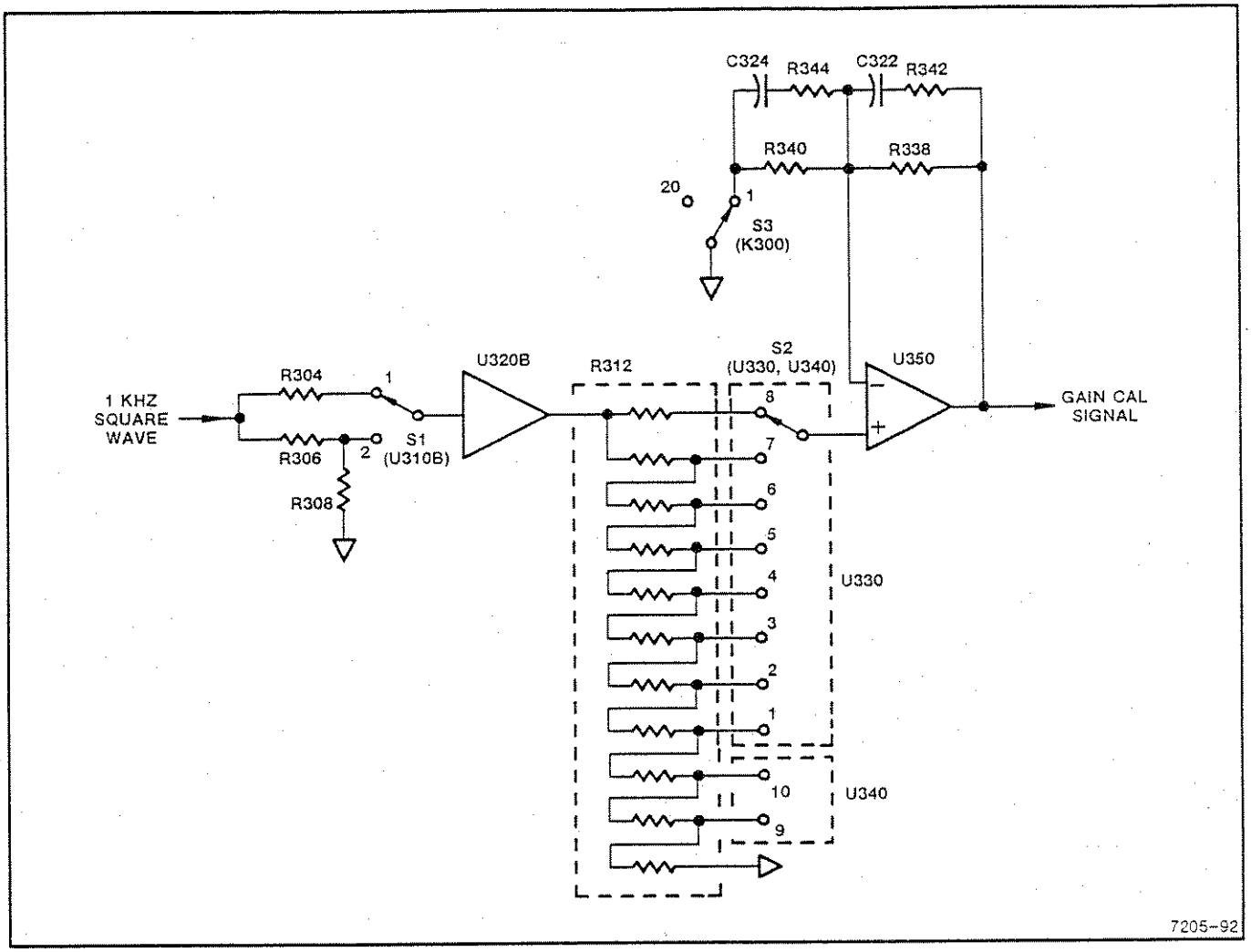


Fig. 1-10 Gain Calibration Signal Amplitude Selector Circuit

Automatic Calibration Control

The automatic calibration control circuit consists of the dc calibration control and gain calibration control circuits shown in Figure 1-11. These functions are almost the same for both Channel 1 and Channel 2. Channel 2 has the dc and gain calibration control circuits for the High-speed sample mode.

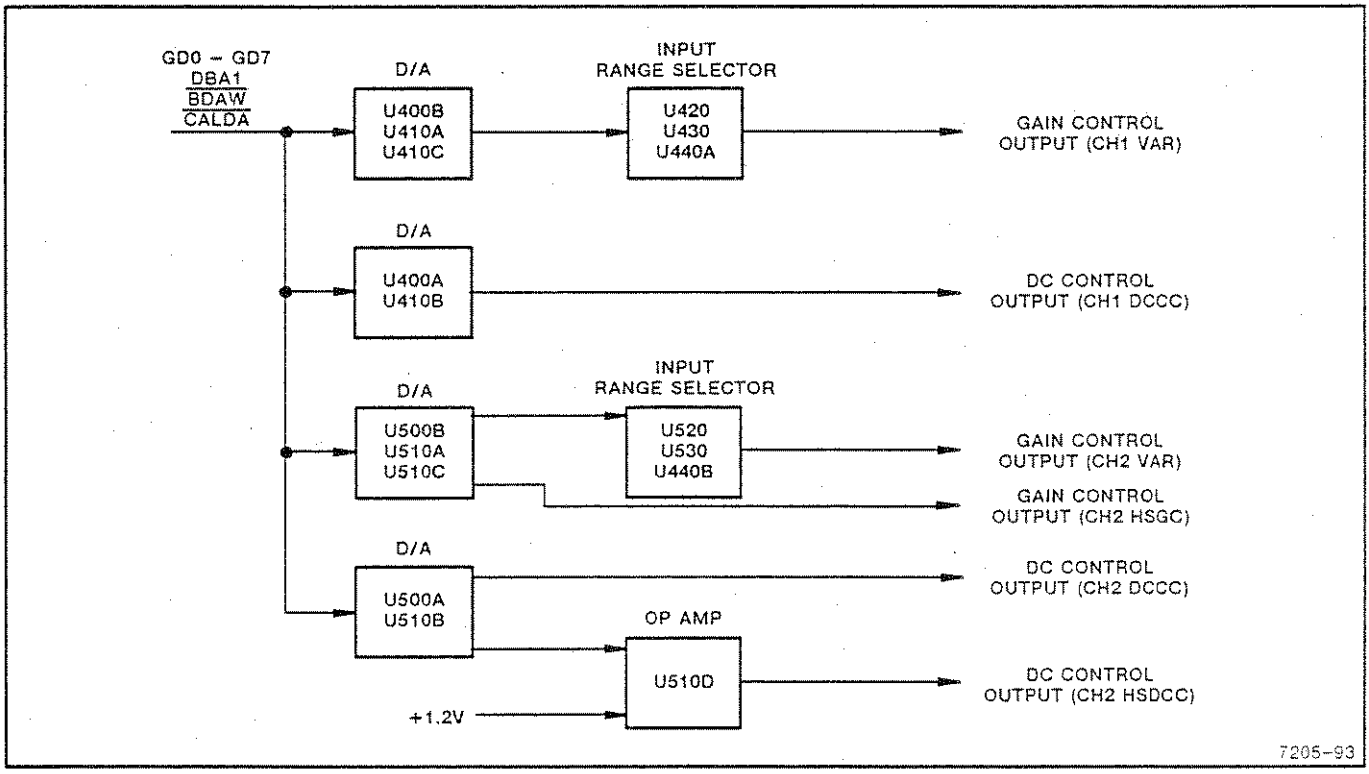


Fig. 1-11 Automatic Calibration Control Block Diagram

Table 1-2
SWITCH POSITIONS OF AMPLITUDE SELECTOR

Input Range [V]	S1	S2	S3
0.1	1	1	1
0.125	1	2	1
0.16	1	3	1
0.2	1	4	1
0.25	1	5	1
0.32	1	6	1
0.4	1	7	1
0.5	1	8	1
0.62	2	9	1
0.8	2	1	0
1.0	2	1	1
1.25	2	2	1
1.6	2	3	1
2.0	2	4	1
2.5	2	5	1
3.2	2	6	1
4.0	2	7	1
5.0	2	8	1
6.2	2	9	2
8.02	1	0	2
10.0	2	1	2
12.5	2	2	2
16.0	2	3	2
20.0	2	4	2
25.0	2	5	2
32.0	2	6	2
40.0	2	7	2
50.0	2	8	2

DC CALIBRATION CONTROL. DC calibration control consists of D/A converter U400A and operational amplifier U410B. The D/A converter generates a dc voltage based on the 8-bit data written by the MPU. This voltage is applied through the buffer U410B to the input offset circuit as the Channel 1 DC calibration control signal CH1 DCCC.

GAIN CALIBRATION CONTROL

Gain calibration control consists of D/A converter U400B, operational amplifier U401A, U410C, U440A, analog switch U420, U430, and their associated components. Circuit configuration is same as the input offset circuit so the description is omitted. The CH1 VAR output voltage of this circuit is applied to the VAR input of the Channel 1 input amp IC U100 at the input amplifier and set the U100 gain. MPU adjusts this CH1 VAR voltage and set the input amplifier gain properly when in Auto calibration.

Auto Calibration Control in High-speed Sample Mode

CH2 HSGC signal from D/A converter U500B and the CH2 HSDCC signal from operational amplifier U510D provide the gain and dc calibration control voltages for the high-speed sample mode. They are applied through the vertical mode switching circuit to the Channel 2 input amplifier as described. Because the Channel 2 input amplifier IC U500 is disabled, and the interface amplifier U600 is connected to the Channel 1, Channel 2 gain and DC level is calibrated by these control voltages.

PHASE CALIBRATION SIGNAL GENERATOR (DIAGRAM 7)

The phase calibration signal generator develops the sawtooth waveform used for calibration. Figure 1-12 is a simplified diagram of the generator and Figure 1-13 shows the waveforms generated.

When the instrument enters the phase calibration mode, a 28.6 MHz (in reality: 200 MHz ÷ 7 = 28.571428 MHz) ECL level clock from the Time Base (see schematic 33a) causes the generator (transistors Q600 through Q608) to develope an 800 mV p-p sawtooth waveform. The waveform is applied through the phase cal signal adder (refer to schematic 3) to the input amp IC. Transistors Q604 and Q606 are current sources for charging integrating capacitor C606, and transistors Q600 and Q602 are current switches for discharging it. Transistor Q608 is an emitter follower.

When the phase calibration clock (PCCLK) is high, the Q602 current switch turns off, and C606 is charged by current sources Q604 and Q606. When PCCLK is low, Q602 turns on discharging C606. Charge current then becomes less than discharge current. Repetition of this sequence creates a sawtooth waveform, which is applied through emitter follower Q608 to the input amplifier board.

AUTOMATIC CALIBRATION MPU INTERFACE

The automatic calibration MPU interface has the silent MPU bus buffer enabled only when MPU accesses the analog section and provides for communication between the MPU and the Channel 1 input offset control, Channel 2 input offset control, gain calibration reference signal control, phase calibration

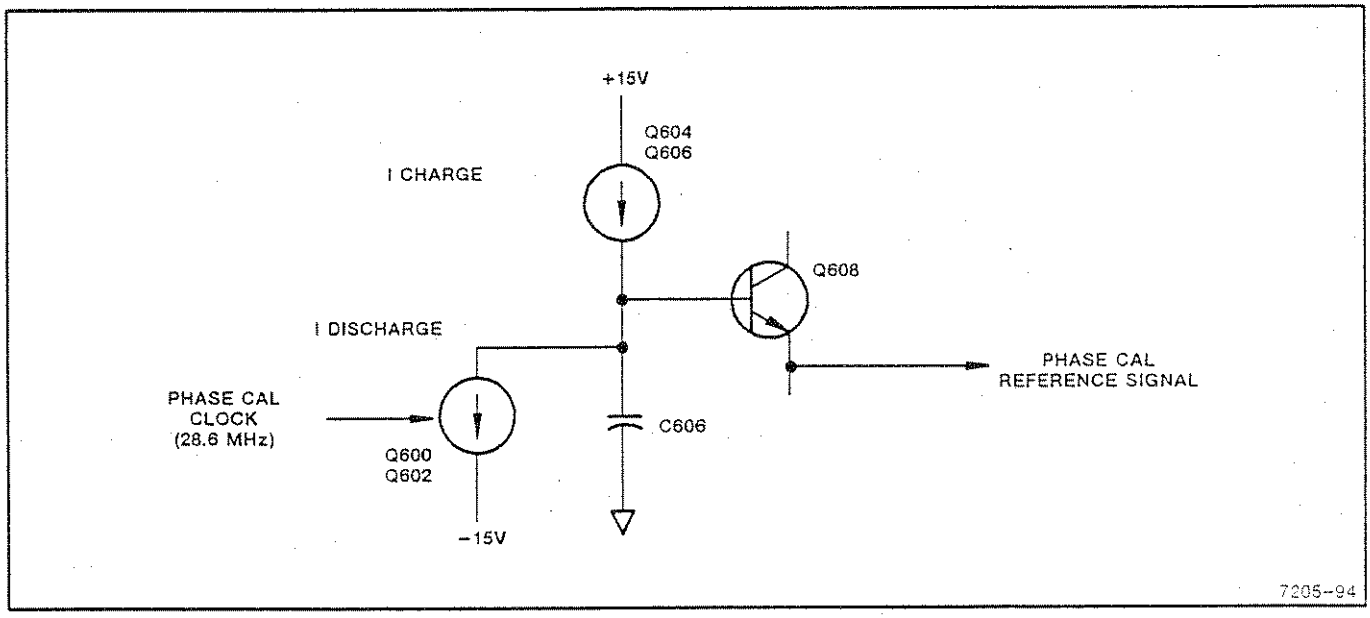


Fig. 1-12 Phase Calibration Generator Simplified Diagram

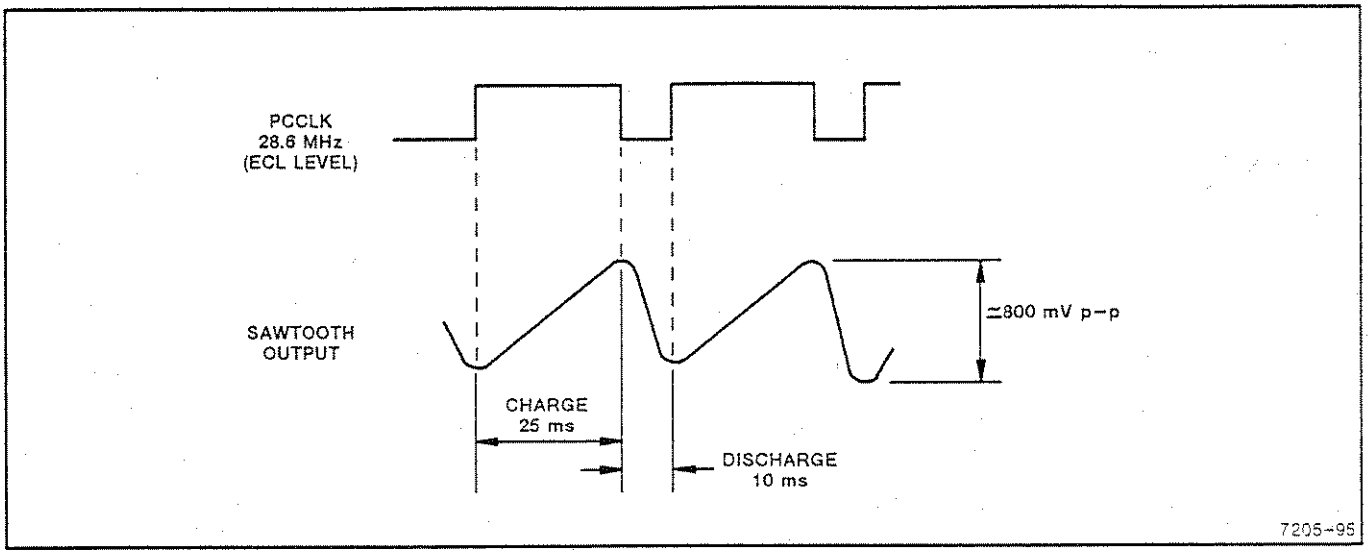


Fig. 1-13 Phase Calibration Generator Waveforms

reference signal control, and address decoder (see Figure 1-14).

Silent MPU Bus Buffer

Buffers U800 and U810 couple the sent MPU bus data from the A22 trigger board to this interface, which is then used for the settings of Channel 1, Channel 2, or auto cal. When analog circuit control is being performed, the input amplifier enable (IAEN) signal becomes low, enabling U800 and U810 and performing read and write operations. In all other instances, this buffer is disabled, which disconnects the bus.

CHANNEL 1 INPUT OFFSET CONTROL. MPU bus data latched by U850 stores the signal that controls the input range selectors of the input offset circuit or the auto cal control circuit. This signal also controls the TV clamp selector.

CHANNEL 2 INPUT OFFSET CONTROL. MPU bus data latched by U860 stores the signal that controls the input range selectors of the input offset circuit or the auto cal control circuit; this channel doesn't have TV clamp control.

GAIN CALIBRATION REFERENCE SIGNAL CONTROL. MPU bus data latches U870A, U870B, U870C, U870D, U870E, U870F, and U870G, store the signals that control the gain calibration reference signal generator amplitude selector. The one bit used to control the amplifier gain (U870 pin 15) drives reed relay K300 through Q800.

PHASE CALIBRATION REFERENCE SIGNAL CONTROL. MPU bus data latch U870H and transistor Q840 produce the PCSC signal that controls the phase calibration signal adder relay K160 (see schematic 3) on and off. When phase calibration is being executed, the phase calibration reference signal is added to the inverting input of input amp IC. When in normal operation (phase calibration is not executed) the phase calibration reference signal line is disconnected from inverting input of the input amp IC by relay K160. At the same time, phase calibration clock (PCCLK) from the TIME BASE board (see schematic 33a) is stopped by disabling $\overline{\text{PCEN}}$ (phase cal enable) signal.

Address Decoder

MPU address decoders U820, U830 and U880 recognize both the input amplifier channel address and the calibration mode. Decoder U820 outputs the latch enable signal, while U830 outputs an automatic calibration control D/A converter enable signal and input offset D/A converter enable signal. Since the D/A converter access time is long, the enable signal pulse is somewhat longer than usual. U880 outputs the input offset polarity signals.

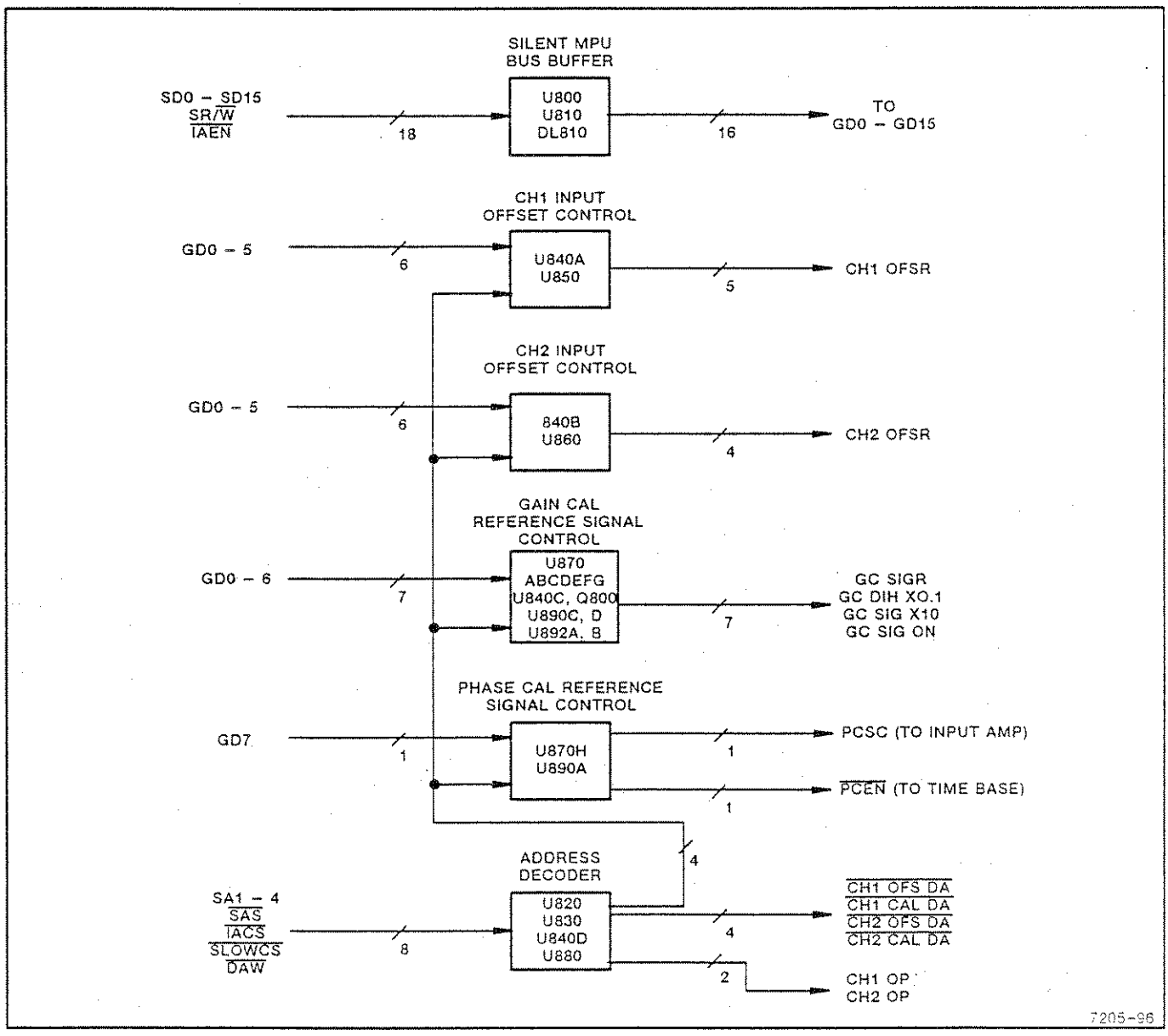


Fig. 1-14 Automatic Calibration MPU Interface

AUTO CALIBRATION

The instrument has three auto calibration modes: DC Calibration, Gain Calibration, and Phase Calibration. These modes and their reference signals are shown in Table 1-3.

Table 1-3
AUTO CALIBRATION MODES AND REFERENCE SIGNALS

Autocal Modes	Reference Signals
Auto dc calibration	Zero-volt level
Auto gain calibration	1 kHz square wave
Auto phase calibration	28.6 MHz sawtooth

DC Calibration

The automatic dc calibrator (Figure 1-15) procedure (Figure 1-16) corrects the input amplifier's dc offset to exactly 0 V, so that digitized data is adjusted to the ground level (512 level = 200H) whenever the input is grounded. This compensates for any dc drift of the input amplifiers and A/D converters.

Initial instrument settings during dc calibration are:

Input Offset:	0
Input Coupling:	GND
Trigger Coupling:	DC
Arm Delay:	0
Trigger Delay:	0
Trigger Mode:	Auto
Sample Interval:	See Table 1-4
Clock Source:	See Table 1-4
Break Point:	All cleared
Record Mode:	Normal

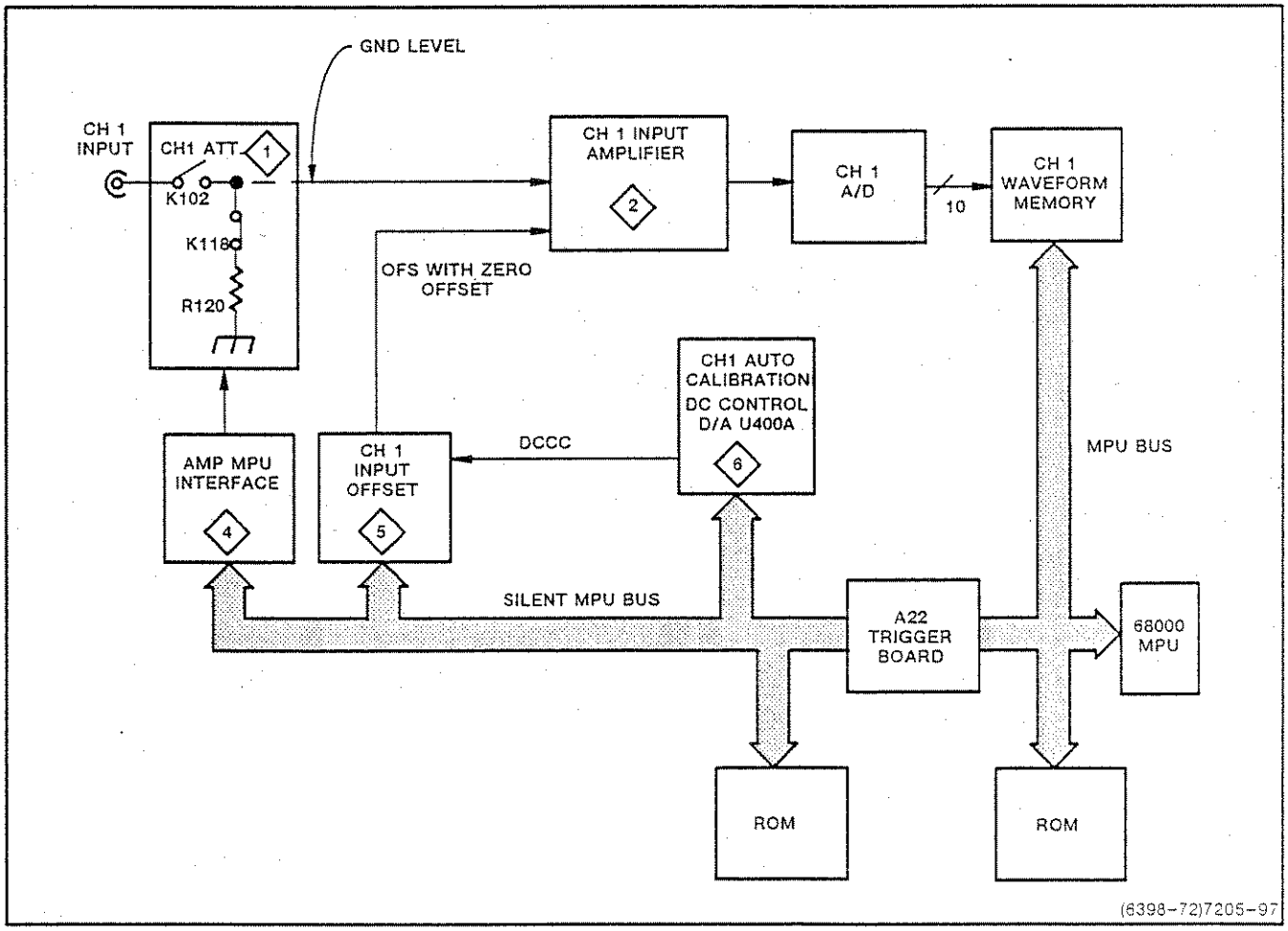


Fig. 1-15 Automatic DC Calibrator Block Diagram

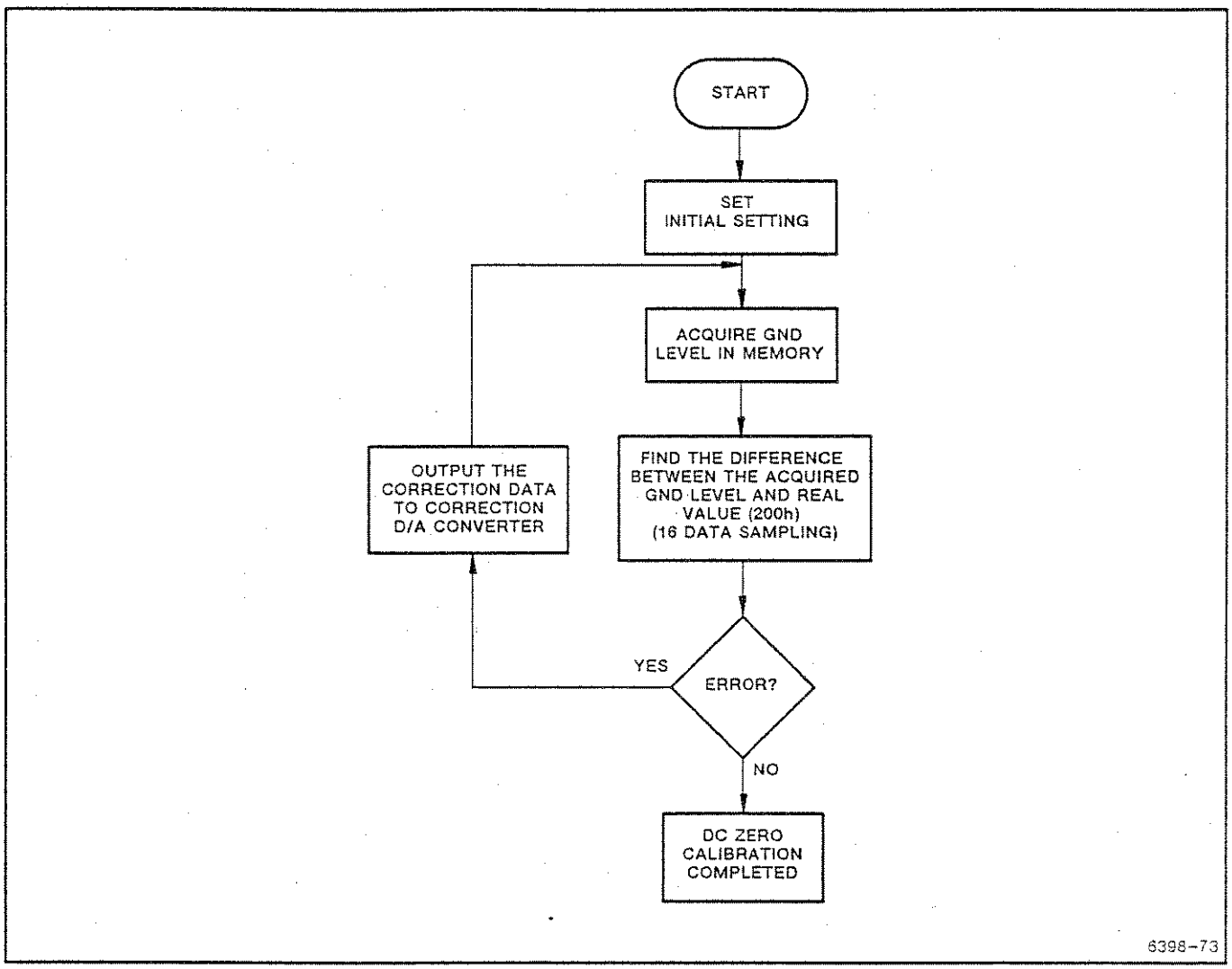


Fig. 1-16 Automatic DC Calibration Procedure

Table 1-4
CLOCK SOURCE AND SAMPLE RATE

SAMPLE RATE SETTING WHEN AUTO CALIBRATION IS STARTED		SAMPLE RATE OF DC CALIBRATION	
Clock Source	Sample Rate	Clock Source	Sample Rate
INT	100 MHz (normal)	INT	100 MHz (10n)
INT	50 MHz (normal)	INT	50 MHz (20n)
INT	others (normal)	INT	10 MHz (100n)
EXT	(normal)	INT	10 MHz (100n)
INT	200 MHz (high speed)	INT	200 MHz (5n)
INT	100 MHz (high speed)	INT	100 MHz (10n)
INT	others (high speed)	INT	20 MHz (50n)
EXT	(high speed)	INT	20 MHz (50n)

Gain Calibration

The automatic gain calibrator (Figure 1-17) procedure (Figure 1-18) corrects for attenuation ratio error in the input attenuators, gain and drift error in the input amplifiers, and full-scale range errors and drift in the A/D converters. A 1 kHz square waveform of an appropriate amplitude for the range selection is applied to the attenuator circuitry, which is then adjusted to the reference value (3E0h).

Initial instrument settings during gain calibration are:

Input Offset:	0
Input Coupling:	For gain cal.
Trigger Level:	0
Trigger Source:	INT (CH1 & CH2)
Trigger Coupling:	DC
Arm Delay:	0
Trigger Delay:	See Table 1-5
Trigger Mode:	Single
Sample Interval:	See Table 1-4
Clock Source:	See Table 1-4
Break Point:	All cleared
Record Mode:	Normal

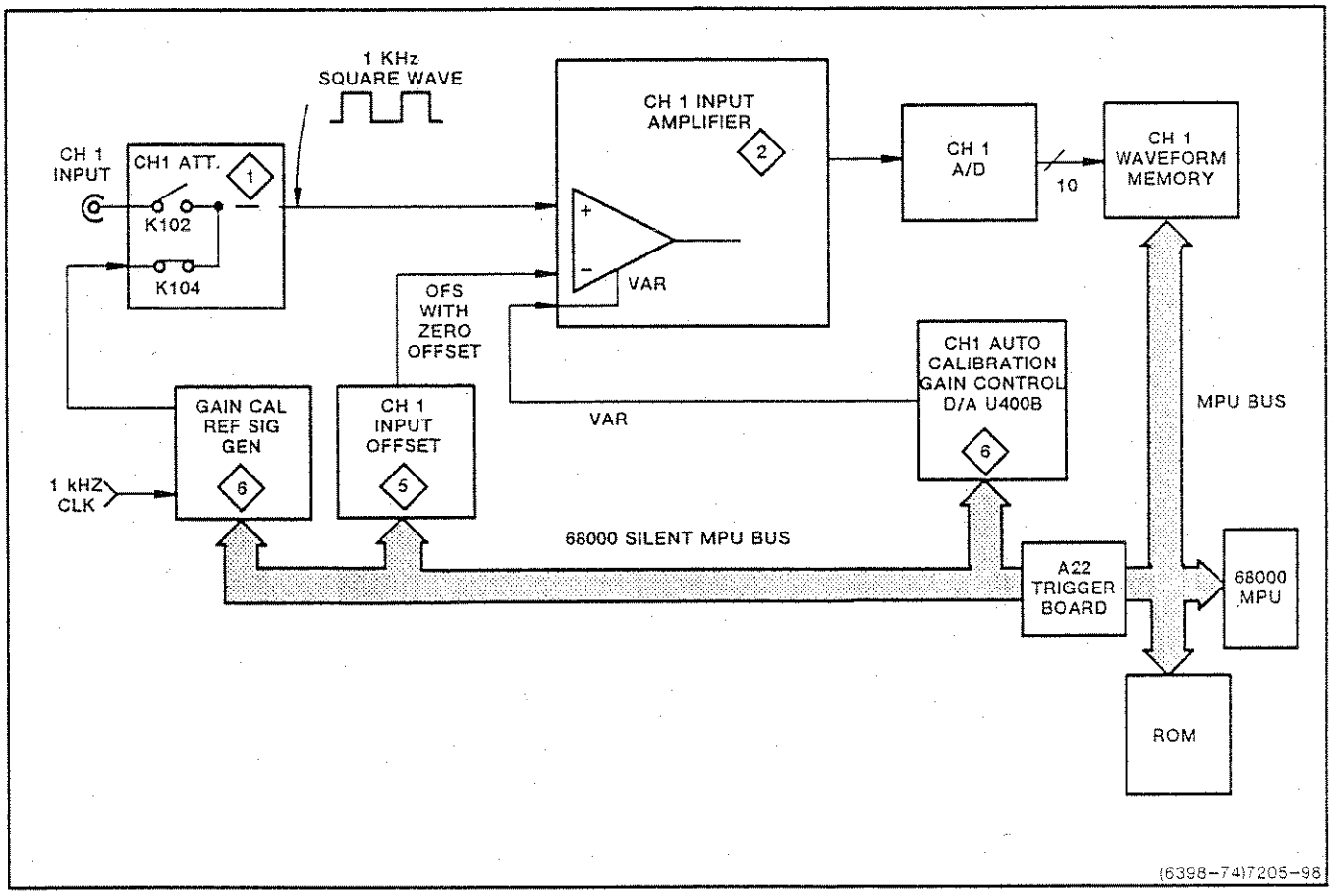


Fig. 1-17 Automatic Gain Calibration Block Diagram

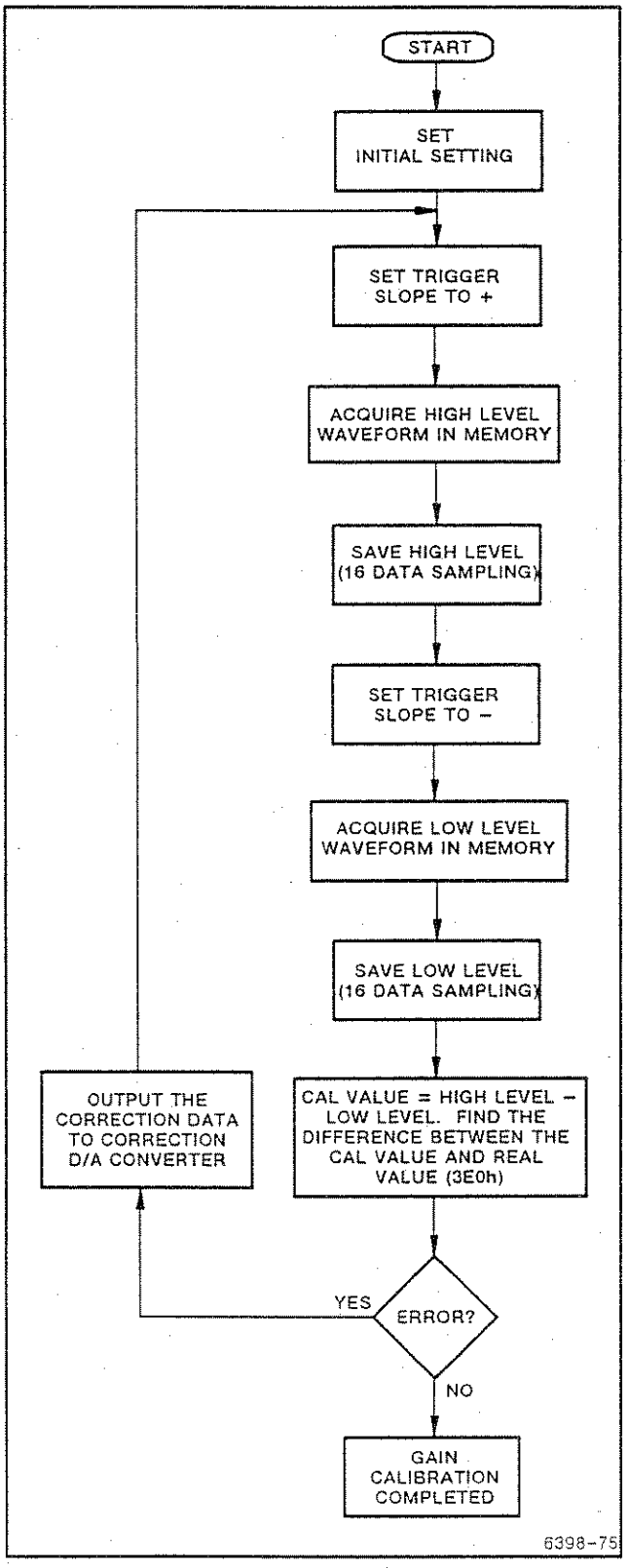


Fig. 1-18 Automatic Gain Calibration Procedure

Table 1-5
TRIGGER DELAY COUNT FOR GAIN CALIBRATION

SAMPLE RATE SETTING WHEN AUTO CALIBRATION IS STARTED		SAMPLE RATE OF GAIN CALIBRATION
Trigger Source	**Sample Rate**	**Delay Count**
INT	100 MHz (normal)	38400 counts
INT	50 MHz (normal)	19200 counts
INT	others (normal)	3840 counts
EXT	(normal)	3840 counts
INT	200 MHz (high speed)	76800 counts
INT	100 MHz (high speed)	38400 counts
INT	others (high speed)	7680 counts
EXT	(high speed)	7680 counts

Phase Calibration

The automatic phase calibrator (Figure 1-19) procedure (Figure 1-20) adjusts the phase between Channel 1 and Channel 2 sampling points to exactly 180 degrees during high-speed mode operation.

In high speed mode operation, the same analog input is applied to both A/D converters simultaneously (Figure 1-21), but their outputs occur with a 180 degree phase difference. This is accomplished by clocking the A/D converters at a 180 degree phase difference from the clock generator. Multiplexing then converts the digital outputs from the A/D converters into serial data at twice the sampling speed.

When the Φ1 and Φ2 clock pulses have a phase difference other than 180 degrees, aperture time errors are generated (Figure 1-22). At high frequency, these aperture errors are magnified, but with automatic phase calibration, any drift from the 180 degree phase difference is automatically compensated.

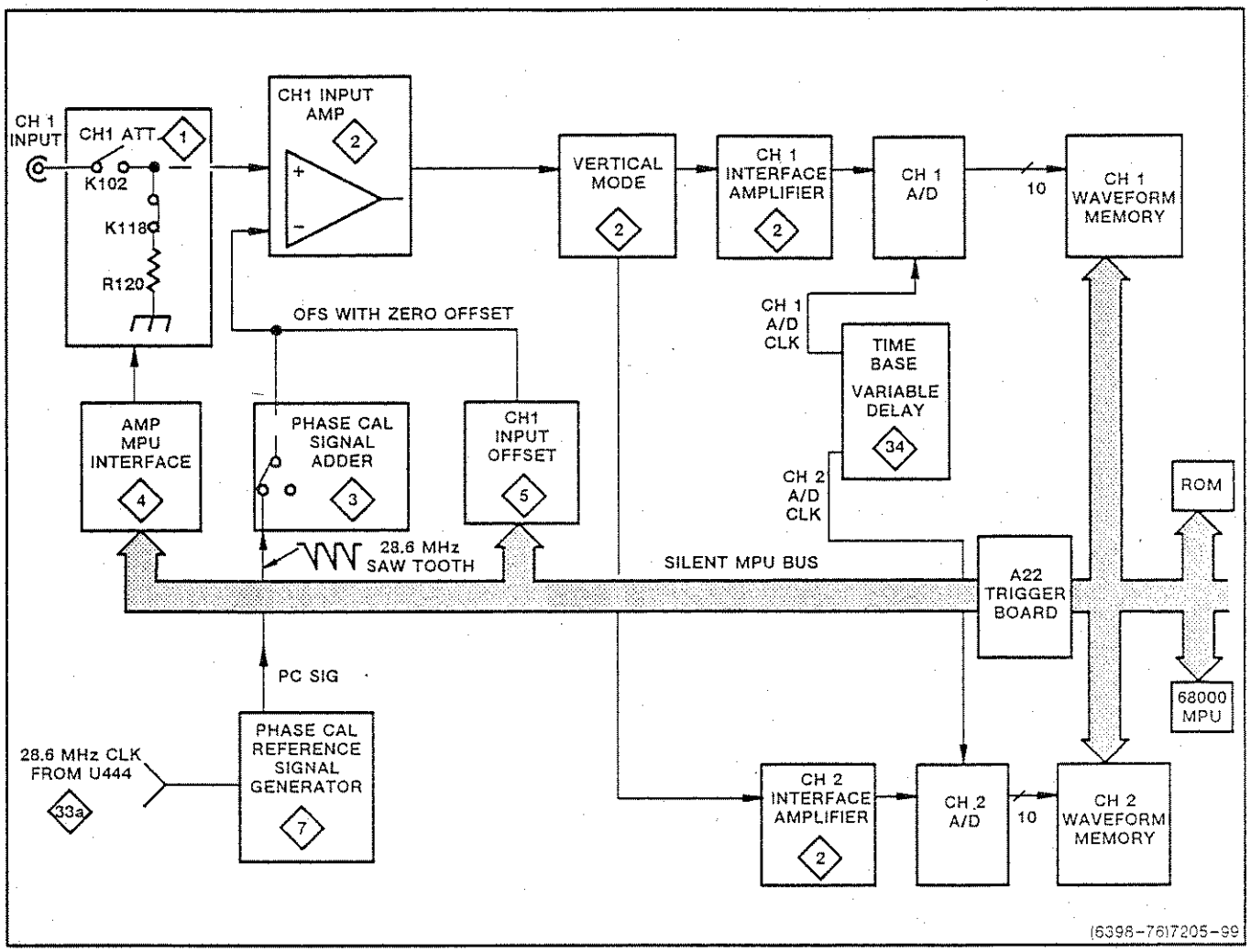


Fig. 1-19 Automatic Phase Calibrator Block Diagram

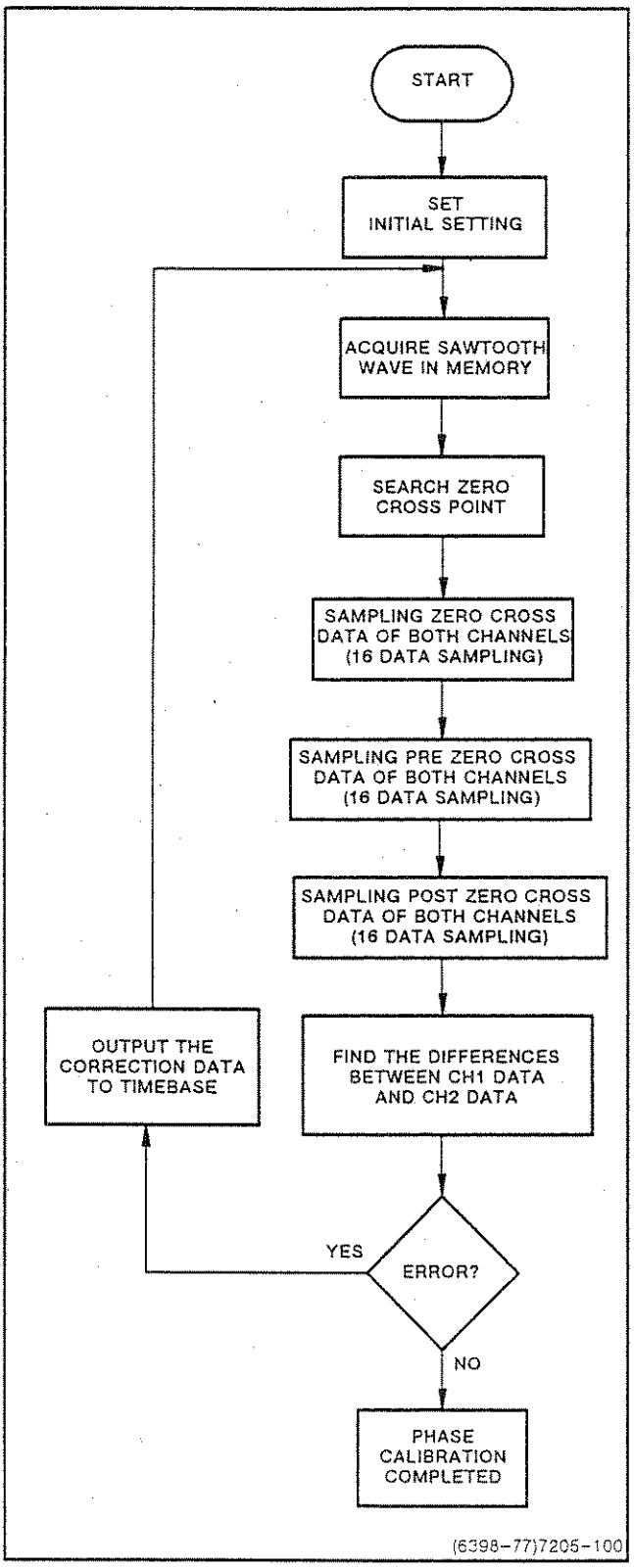


Fig. 1-20 Automatic Phase Calibrator Procedure

Initial instrument settings during gain calibration are:

Input Range:	0.8 V
Input Offset:	0
Input Coupling:	GND
BW Limit 20 MHz:	Off
Trigger Level:	0
Trigger Source:	INT (CH1)
Trigger Slope:	+
Trigger Coupling:	DC
Arm Delay:	0
Trigger Delay:	-800
Trigger Mode:	Single
Sample Interval:	200 MHz
Clock Source:	INT
Break Point:	All cleared
Record Mode:	Normal

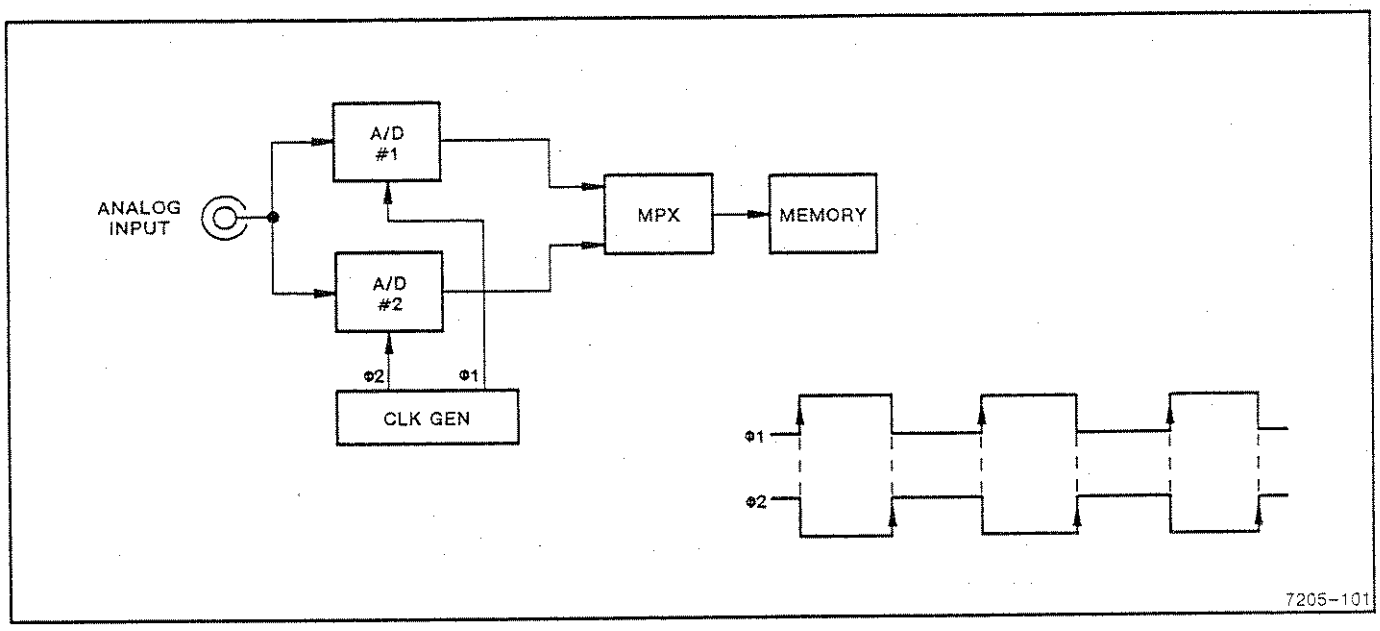


Fig. 1-21 Process of How A/D Converters Produce Serial Data

BLOCK DIAGRAM DESCRIPTION OF A/D CONVERTER

A/D converter operation is identical for both Channel 1 and Channel 2. Each A/D converter (Figure 1-23) is a 10-bit, 2-stage converter with a maximum sampling rate of 100 MHz.

Output of a track and hold (T/H) IC tracks continuous input signal and holds the voltage for a specified time (hold time). While in the hold state, the converter performs its A/D conversion. Because the converter makes its conversions on a stable voltage held at a specified level, it can operate independently of the ramp (frequency) of input signals. This reduces the possibility of aperture time errors even for high-frequency input signals.

The analog signal from the T/H circuit is converted to a 32-level (5-bit) digital signal by the first A/D converter. This data is once latched, formed into a waveform, sent to the 5-bit D/A converter, and then sequentially converted to one of 32 analog levels. The waveform shown in Figure 1-24(c) is obtained by subtracting the reproduced step-form analog waveform from the delayed output of the T/H circuits. The resultant output is coupled to the second 5-bit A/D converter, which produces a second digital signal with 32 possible values. The 10-bit resolution data output is obtained by combining the first and second 5-bit A/D digital outputs. Digital error correction is added to compensate the accuracy of the first 5-bit A/D converter.

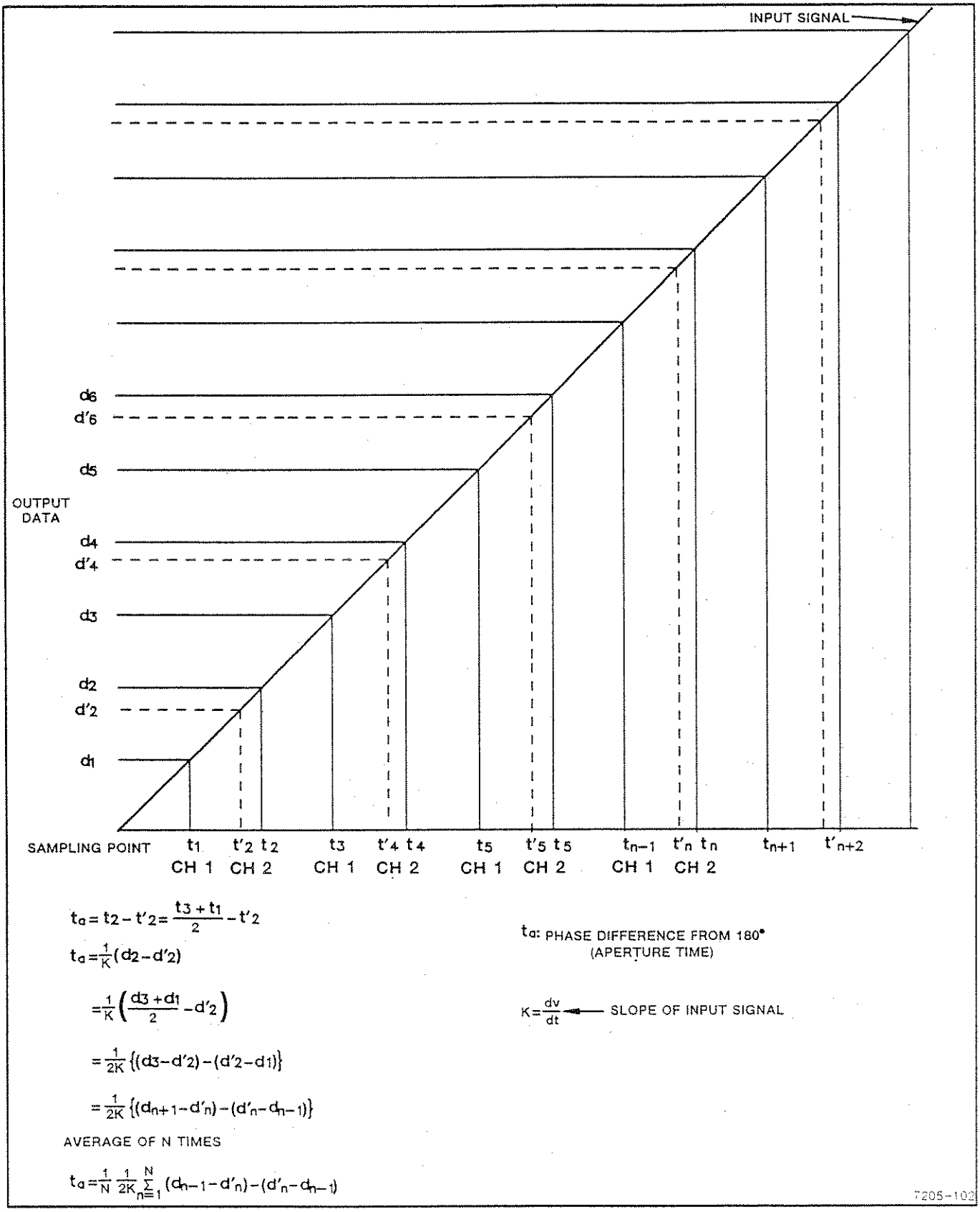


Fig. 1-22 Aperture Time Error Chart

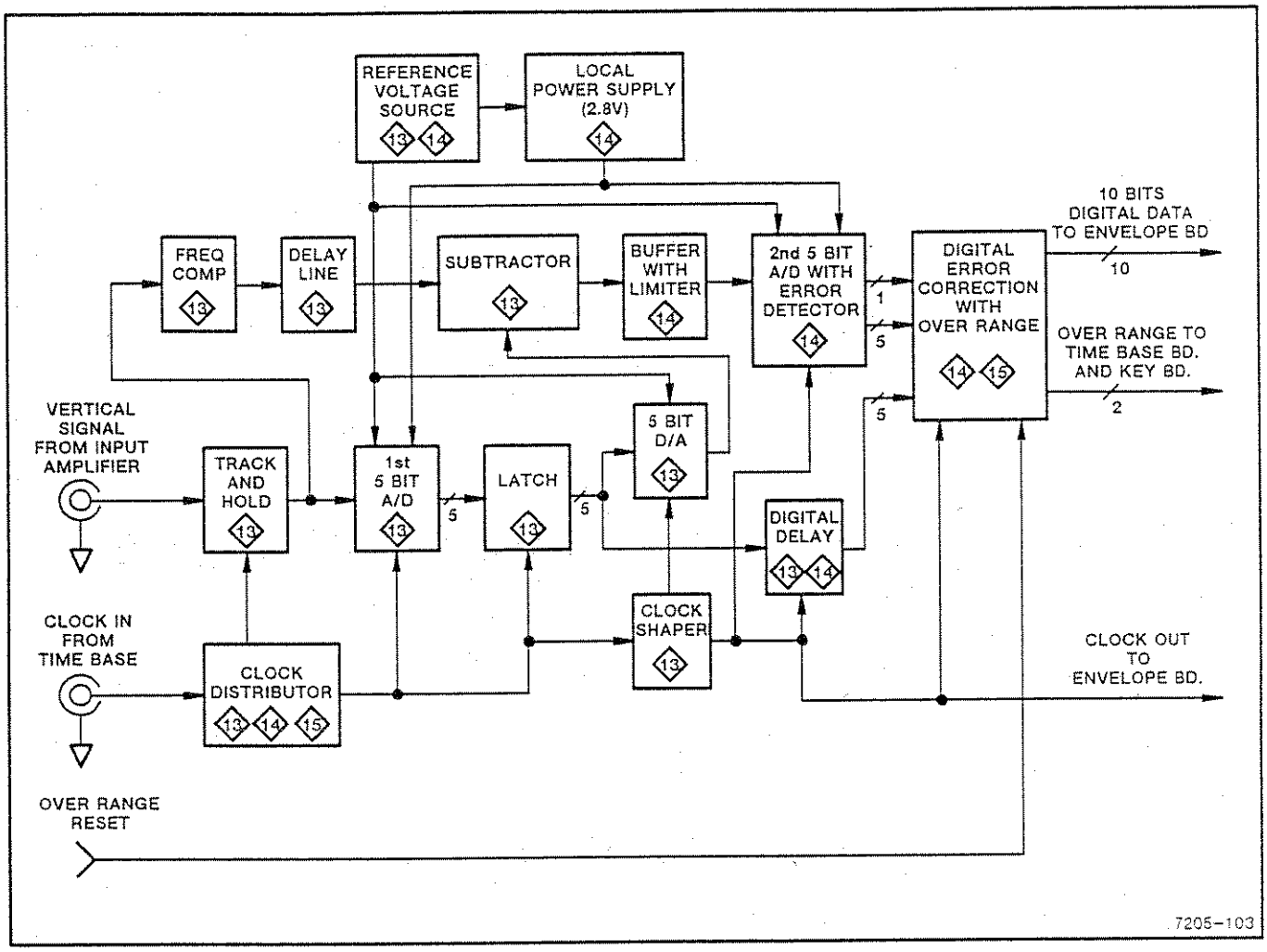


Fig. 1-23 A/D Converter Block Diagram

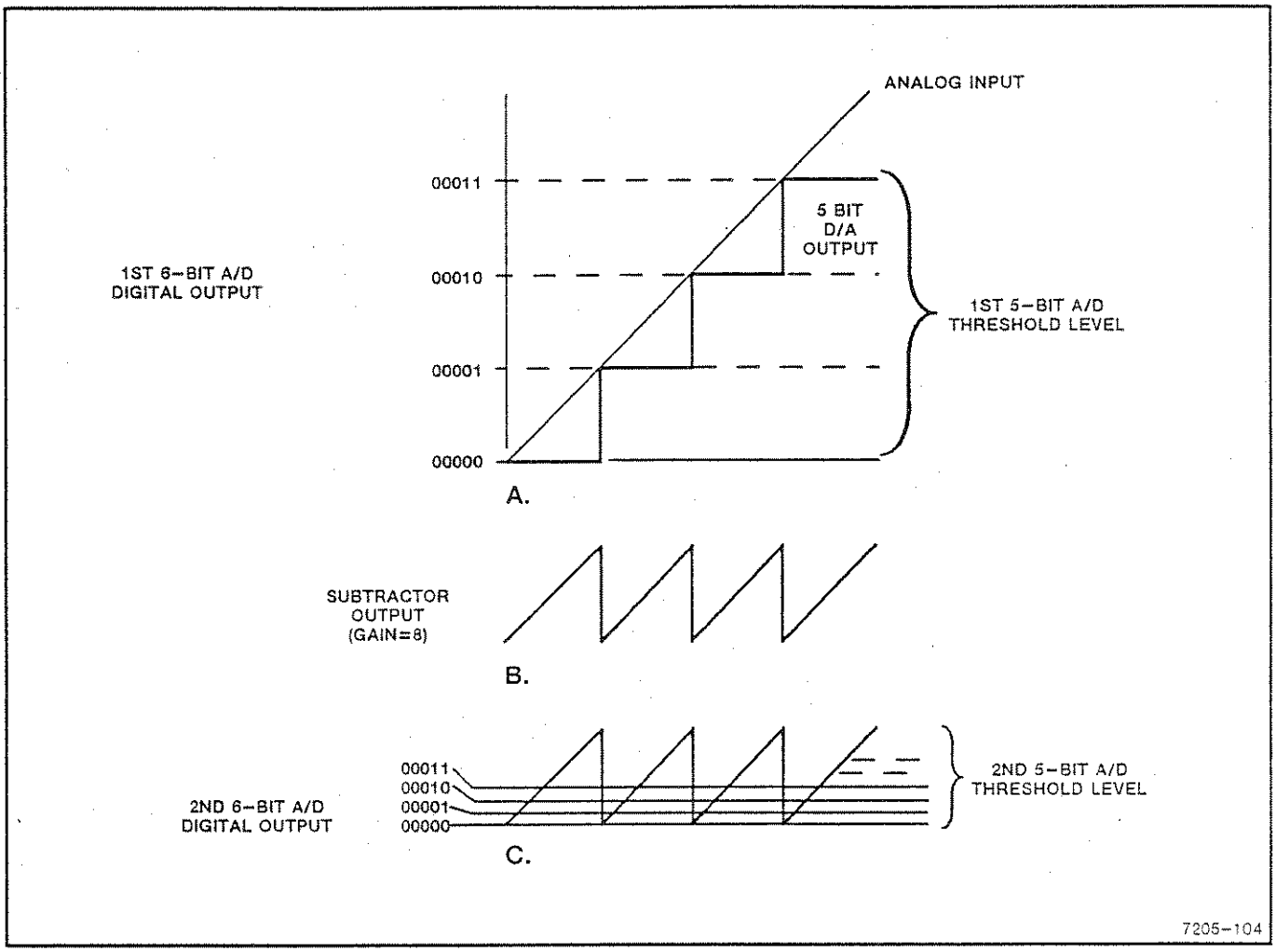


Fig. 1-24 Basic Operation of A/D Converter

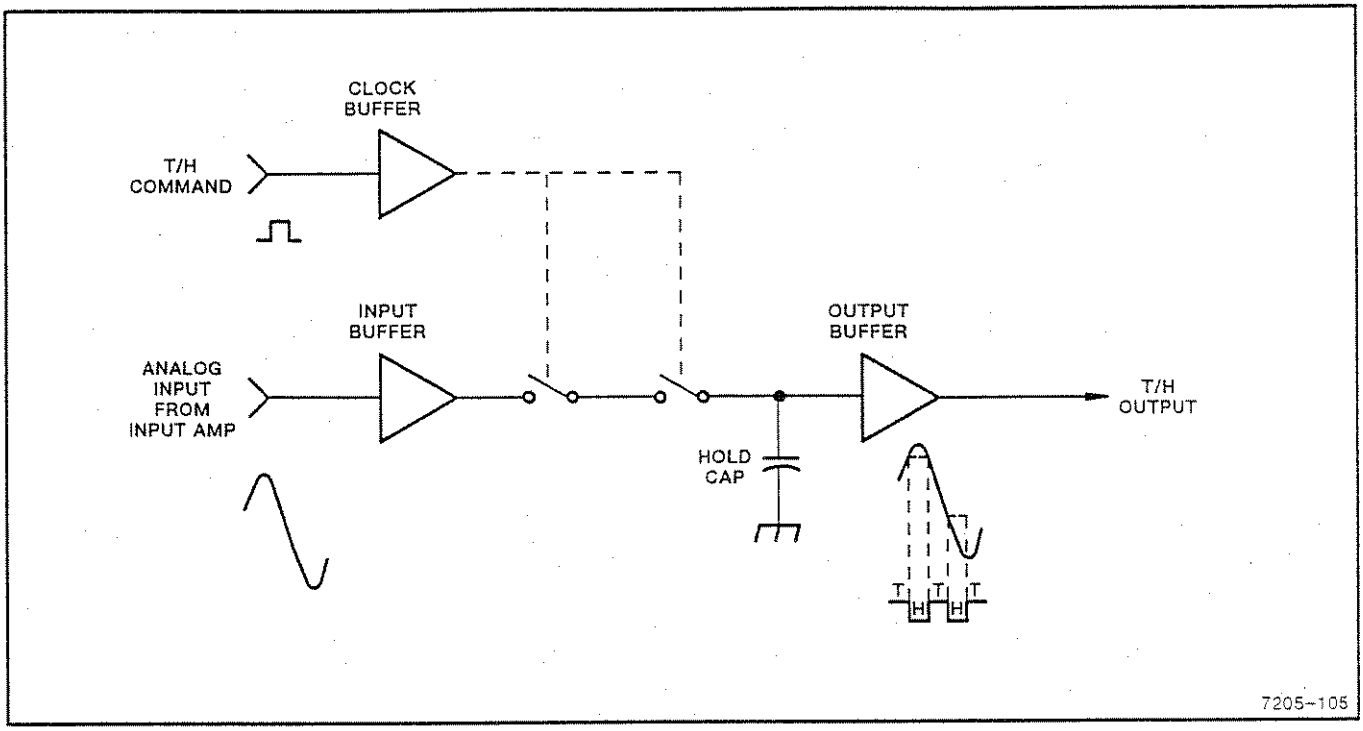


Fig. 1-25 Simplified Track and Hold Circuit Diagram

TRACK/HOLD AND FIRST A/D CONVERTER (DIAGRAM 13 & 14)

The track and hold (T/H), first 5-bit A/D converter, and 5-bit D/A converter temporarily convert the analog signal into the most significant five output bits, which is subtracted from the T/H output.

Track/Hold and Limiter

The track/hold and limiter circuits (Figure 1-25) and their associated timing (Figure 1-26) capture segments of the input signal for conversion to digital data.

The T/H circuitry consists of an input buffer for impedance conversion, two switches, a clock buffer to drive the switches, a capacitor to hold analog signals, and an output buffer for impedance transformation. These circuits are constructed of hybrid ICs to improve high frequency characteristics.

Variable resistor R110 is used to adjust the T/H output dc offset.

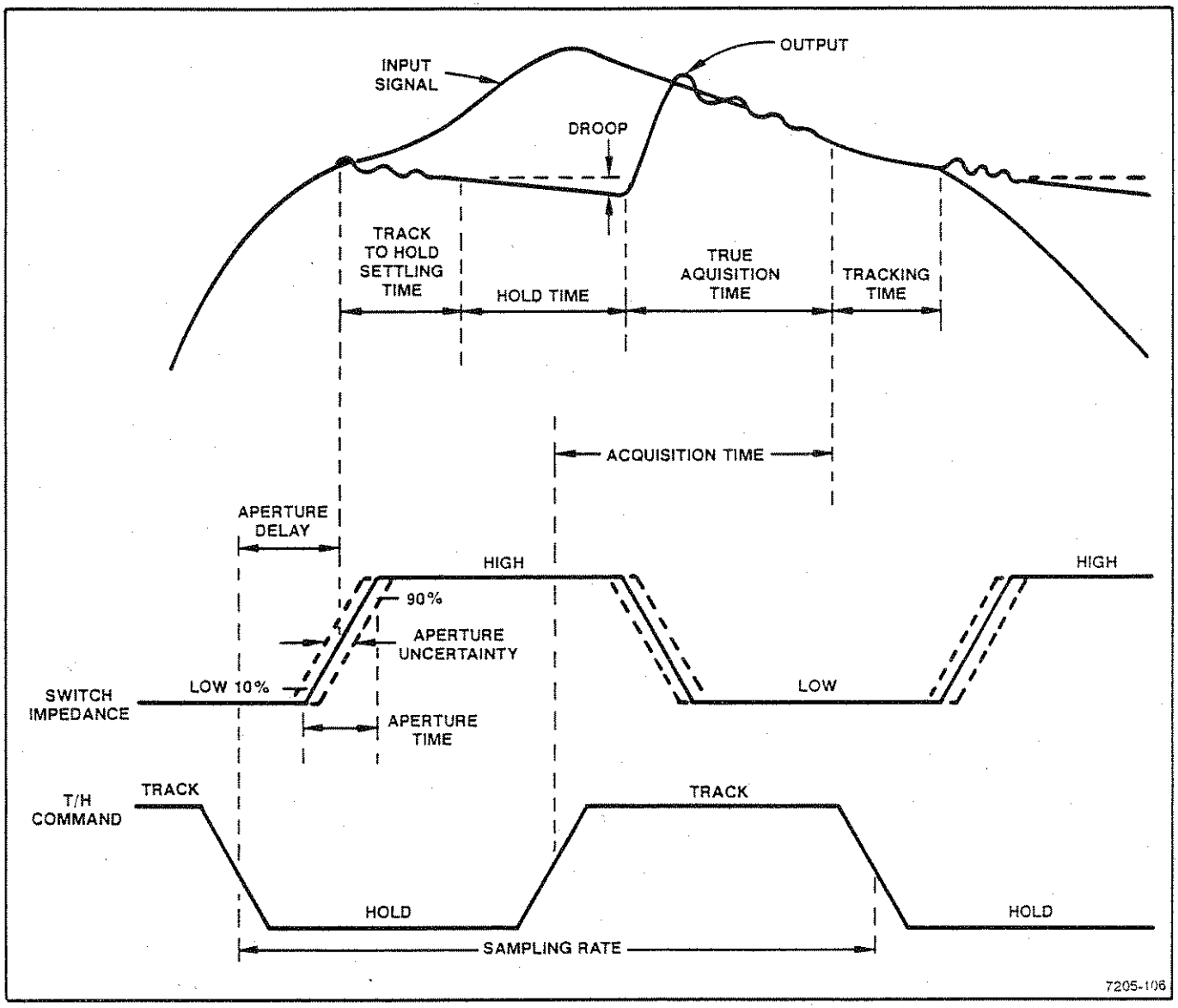


Fig. 1-26 Track and Hold Timing Relationships

Delay Line and Frequency Compensation

A 50 ohm coaxial cable provides an approximate 26 ns delay line. Device U150 compensates the delay-line frequency response.

First 5-Bit A/D Converter and Latch

The first 5-bit A/D converter U200 is a high-speed, fully parallel device. Its reference voltage is adjusted for a subtractor output that is symmetrical around 0 V. This maximizes the effectiveness of digital error correction, and also has these effects.

1. The first 5-bit A/D converter input offset voltage is cancelled and nonlinear distortion is reduced.
2. The 5-bit D/A converter nonlinear distortion is reduced.
3. The dc offset of the buffer with limiter is cancelled.

As a result of these effects, the first 5-bit A/D converter input range is set to approximately ±1 V.

Latch U210 is used as a buffer because the noise margin is low with respect to the first 5-bit A/D converter digital output, and because drive capacity with respect to load is insufficient.

5-Bit D/A Converter

The 5-bit D/A converter U300 is a 6-bit, low-glitch, ECL converter with its LSB always set to 1. A bias amplifier (operational amplifier) to keep the D/A output stable, and a pass/hold (gated) latch are combined within this D/A converter. However, a reference voltage (capable of sinking 1.25 mA) must be applied externally. The current is supplied by U800 (from +10 volt supply on schematic 14) and R304 (8K ohm). The D/A converter output is 20 mA (=$\overline{I}$o when all data are 0) at full scale. Thus, U350 produces +1 V to convert the D/A output to ±1 V, and the load is set at 100 ohms.

Subtractor

Subtractor U400 subtracts the 5-bit D/A output from the delayed T/H output. It is a differential amplifier with a built-in limiter and a gain of 8. The limit voltage is ±2.5 V maximum. Because dc or gain variation can affect the subtraction result and reduce the overall accuracy of the 10-bit A/D converter, U400 has a built in stabilizer circuit.

Digital Delay

The digital delay circuit delays the most significant five data bits (first 5-bit A/D converter outputs D5-D9) in order to adjust its phase to the phase of the least significant five data bits (second 5-bit A/D converter outputs D0-D4). It uses latches U212 and U214 on schematics 13 and 14, respectively.

Reference Voltage Source

The reference voltage source circuit supplies reference voltages for the first and second A/D converters, 5-bit D/A converter, and the local power supply.

U800 (schematic 14) generates an ultralow drift (5 ppm/°C maximum gradient) regulated dc reference voltage of +10 V. This reference voltage is divided by precision resistors to produce the necessary voltages for each circuit. U250 and U350 (schematic 13) and U550 and U650 (schematic 14) are impedance transformation devices. U810 produces ±10 V for adjusting the U250, U550, and U650 output voltages using R250 and R260 (schematic 13) and R550, R650, and R660 (schematic 14). Q810 is a current booster (schematic 14).

Clock Distributor

The clock distributor applies clock pulses sequentially to the T/H, first 5-bit A/D converter, latch, clock shaper, digital delay, second 5-bit A/D converter, and digital error correction circuit at the required fixed delays.

U900 forms the clock pulse from the Time Base into two fixed-width pulses of 5.8 ns and 6.2 ns (Figure 1-27). Pulse $\overline{Q1}$ (5.8 ns) is supplied by gate U902B to the T/H circuit only. The T/H hold time then becomes 5.8 ns. Pulse $\overline{Q2}$ (6.2 ns) is supplied through DL900 to DL916 and U902 to U910 to each of the circuits in sequence.

Clock Shaper

As shown in Figure 1-28, shaper U904 has two types of outputs: One is the result of shaping the input clock pulse width from 6.2 ns to 3.5 ns. The second is the same width as the input clock pulse. The first clock pulse is supplied to the 5-bit D/A converter; the second clock is delayed and supplied to subsequent circuits.

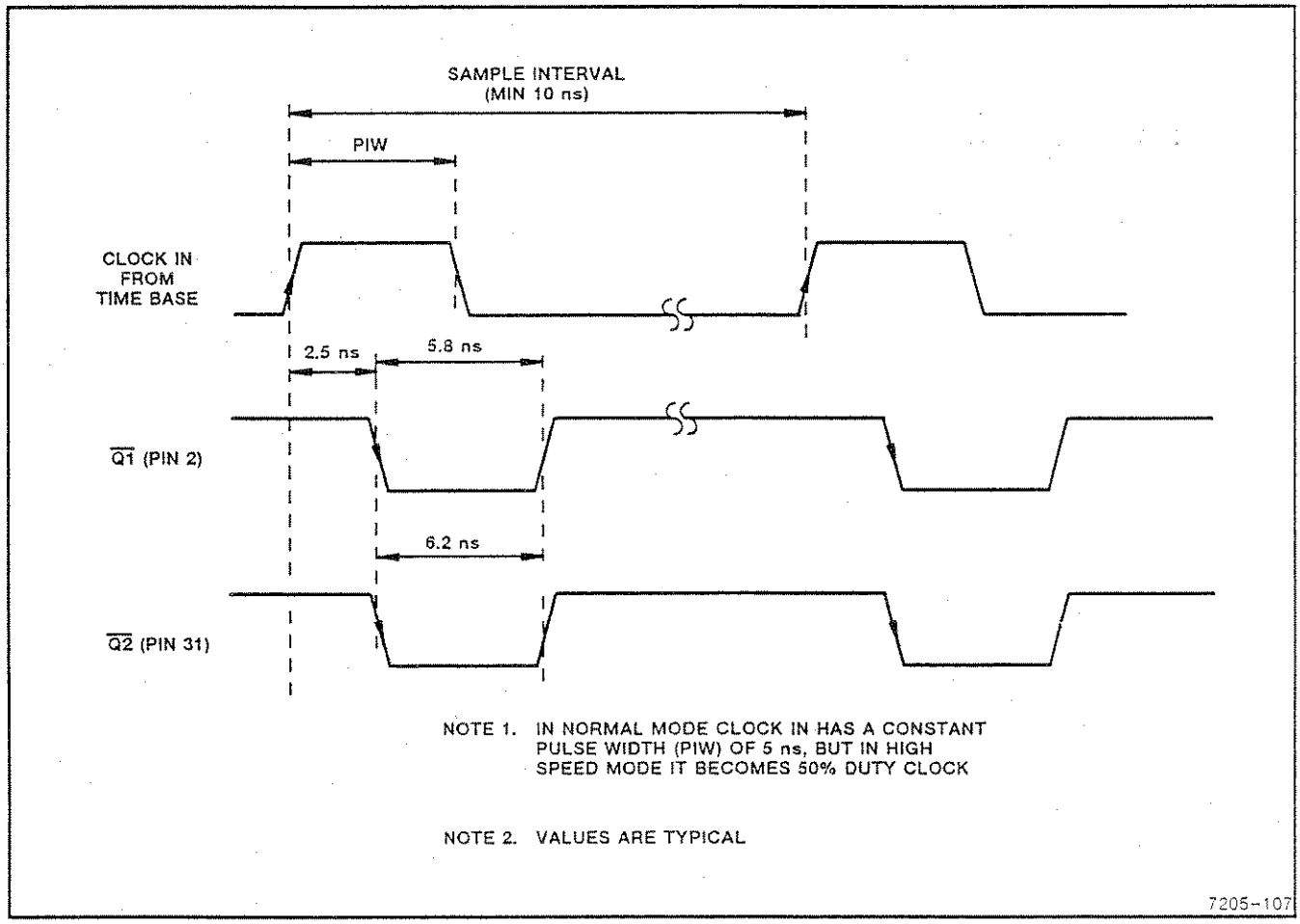


Fig. 1-27 Timing Events for U900

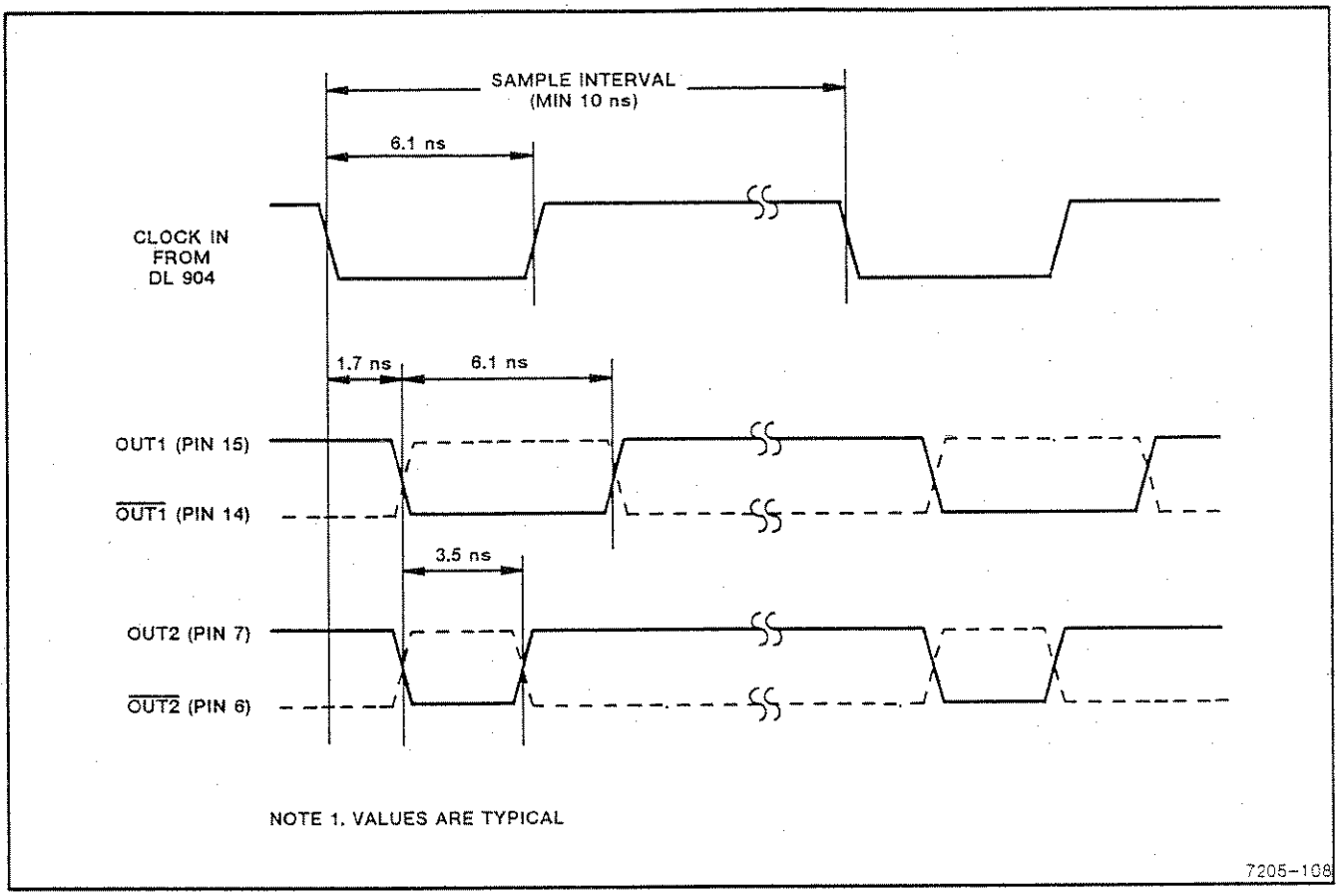


Fig. 1-28 Timing Events for U904

SECOND A/D CONVERTER, BUFFER, AND POWER SUPPLY (DIAGRAM 14)

This part discusses buffer, second 5-bit A/D converter, and local power supply circuit blocks.

Buffer with Limiter

The buffer with limiter consisting of Q450 through Q464 is added to the subtractor output (schematic 13) to overcome the input capacitance (approximately 15 pF) of the second 5-bit A/D converter, which ensures that the subtractor output frequency range does not deteriorate. Subtractor U400 has a built-in limiter, but it is not sufficient to control the high-frequency response. Therefore, a separate limiter (U450) is included at the buffer input to ensure that a signal with excessive amplitude is not applied to the second 5-bit A/D converter.

The buffer amplifier provides a gain of approximately 1 and the ability to effectively drive the capacitive load.

Second 5-Bit A/D Converter with Error Detector

Two 5-bit A/D converters (U500 and U600) form a second 5-bit A/D converter to provide a 10-bit resolution A/D converter. These two converters are configured to form a 6-bit A/D converter (64 threshold levels). Table 1-6 shows the word structure of the second 5-bit A/D converter.

Table 1-6
WORD STRUCTURE OF SECOND 5-BIT A/D CONVERTER

5-Bit A/D Converter (U500)					5-Bit A/D Converter (U600)						2nd 5-Bit A/D Converter (Words Needed)					
B5	B4	B3	B2	B1	OR	B5	B4	B3	B2	B1	EC	D4	D3	D2	D1	D0
1	1	1	1	1	1	0	0	0	0	0	1	1	1	1	1	1
1	1	1	1	0	1	0	0	0	0	0	1	1	1	1	1	0
1	1	1	0	1	1	0	0	0	0	0	1	1	1	1	0	1
0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0
0	0	0	0	0	0	1	1	1	1	1	0	1	1	1	1	1
0	0	0	0	0	0	1	1	1	1	0	0	1	1	1	1	0
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

When the input signal of the second 5-bit A/D converter is greater than O V, U500 A/D converts it. All U600 outputs at this point are 0, and the error correction bit (EC) is supplied. When the input signal is less than O V, U600 converts it, and all U500 outputs are 0. This converter configuration provides 64 threshold levels because bits B1, B2, B3, B4, and B5 of U500 and U600 are wire-OR'd.

Because the second 5-bit A/D converter consists of two 5-bit A/D converters connected in parallel, nonlinearity errors are generated at the connection points by the internal threshold level errors in the devices. Variable resistors R550, R650, and R660 are adjusted to compensate for this error.

Local Power Supply (2.8 V)

The 2.8 V local supply (Vcc) for A/D converters U200, U500, and U600 is produced by dividing the +10 V VREF from U800 by the voltage divider R850 and R852. U850 is an impedance converter; Q852 is a current booster; CR850, CR852, and R856 protect Q852 in case of an output short; C850 and C852 are filters; and C854 and C856 are filters to isolate the 2.8 VD and 2.8 VL supplies.

DIGITAL ERROR CORRECTION (DIAGRAM 15)

Digital error correction circuitry combines data from the first 5-bit A/D converter with that from the second 5-bit A/D converter to produce error corrected 10-bit data.

Digital Error Correction with Overrange

The output signal of the Buffer with Limiter (explained above for schematic 14) includes nonlinear distortion and dc drift generated from the first 5-bit A/D converter. These sources of error can cause lost bits. However, this is prevented by extending the quantizing range of the second 5-bit A/D converter to 6 bits (64 threshold levels). The digital error correction circuit connects the data from the second 5-bit A/D converter (D0-D4) with data from the first 5-bit A/D converter (D5-D9).

Figure 1-29 is a simplified digital error correction circuit block diagram and Figure 1-30 shows its logic.

Latch U700 (schematic 14) is used to adjust the upper 5 bits (D5-D9) to the timing of the lower 5 bits (D0-D4). Adder U708 sums the 6-bit data. When the analog input has a greater plus value than the 10-bit A/D converter input range, the U708 carry output ($\overline{Xc}$) makes all 10-bit data 1s. Xc is also used as the plus-side overflow bit. Buffers U704 and U706 pass $\overline{Xc}$ to bits D0-D9. Digital error corrected data is stored in latches U710 and U712, then supplied as the final 10-bit A/D converter data output. This data is in complementary form, with positive data being transferred to the envelope board and negative data being used to produce the minus-side overflow bit.

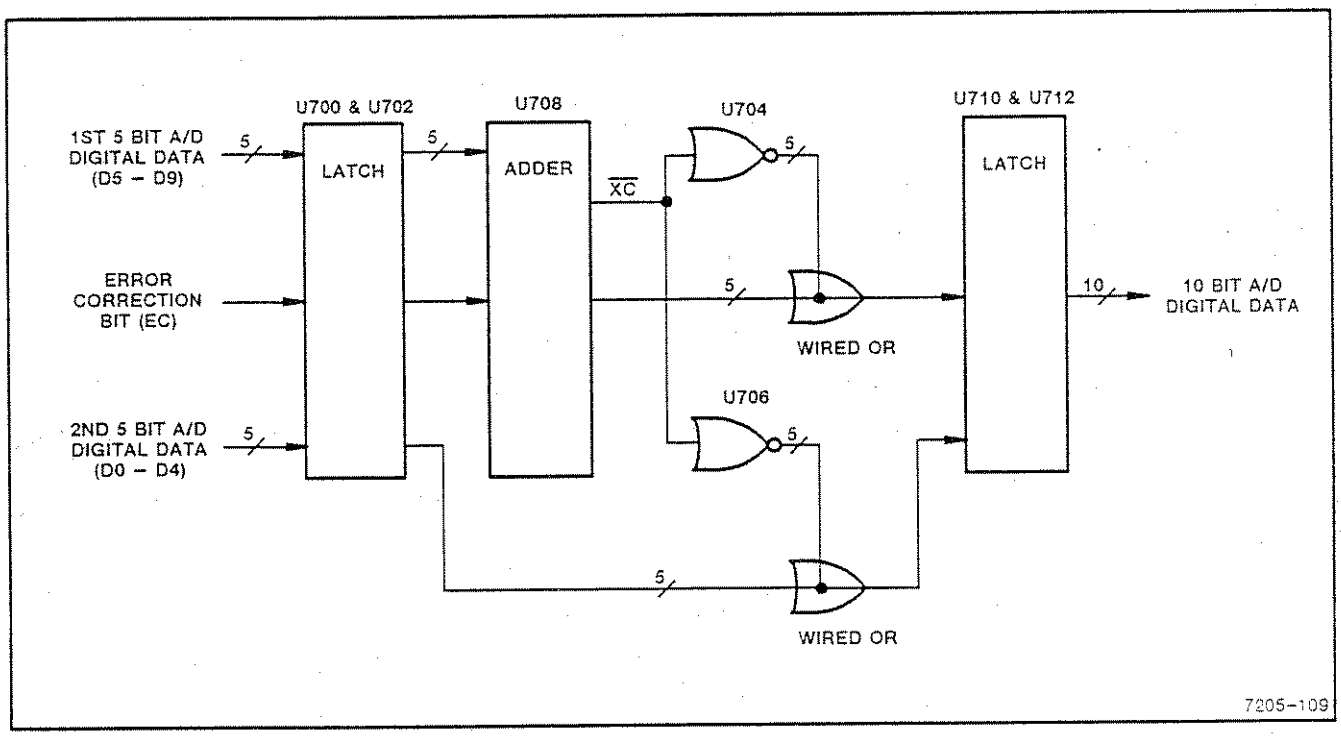
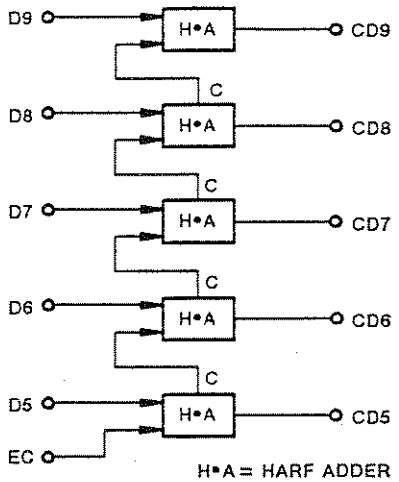


Fig. 1-29 Digital Error Correction Block Diagram



BOOLEAN EQUATIONS FOR 10 BIT AND DIGITAL DATA

CD0 = D0
CD1 = D1
CD2 = D2
CD3 = D3
CD4 = D4
CD5 = D5⊕EC
CD6 = D6⊕(EC•D5)
CD7 = D7⊕(EC•D5•D6)
CD8 = D8⊕(EC•D5•D6•D7)
CD9 = D9⊕(EC•D5•D6•D7•D8)

EC = ERROR CORRECTION BIT

7205-110

Fig. 1-30 Digital Error Correction Logic

Negative data passes through inverters U750 and U752, whose outputs are wire-OR'd such that they become 0 only when all 10-bit data (positive) is 0. This inverted output is used as the minus-side overflow bit. Translator U754 converts data from ECL level to TTL level; U756 is a resettable latch.

Figure 1-31 shows the timing from the input of the analog signal until it becomes a 10-bit digital signal relative to the time base clock pulse.

TRIGGER CIRCUIT

The trigger circuit, shown in Figure 1-32 as a block diagram and in Figure 1-33 as a simplified circuit diagram, performs the necessary detection and processing of the internal or external trigger signal for generating a trigger pulse.

An internal trigger signal of approximately ± 1 volt at ± full scale from an input amplifier is transformed

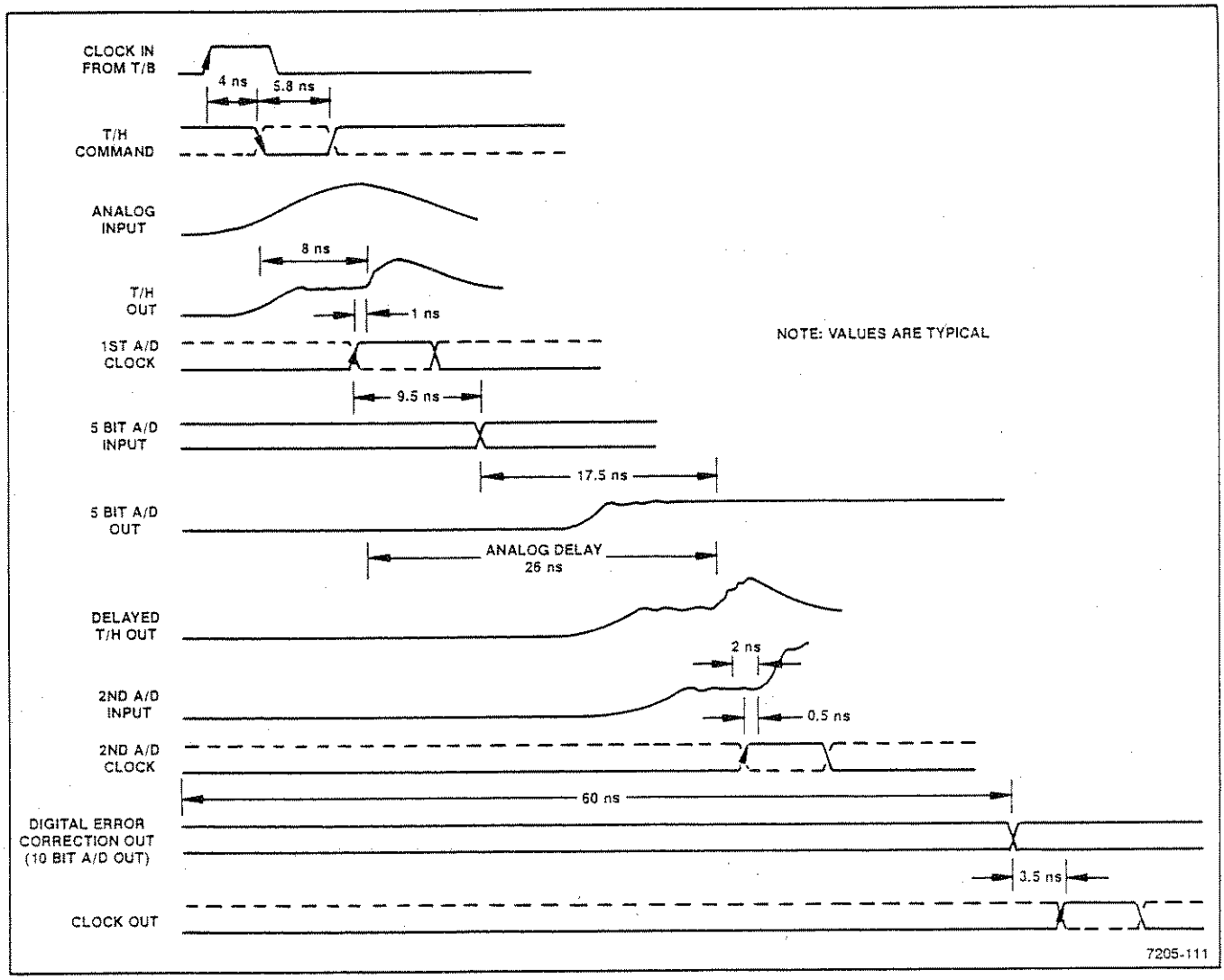


Fig.1-31 Timing Sequence for A/D Conversion of Analog Signal

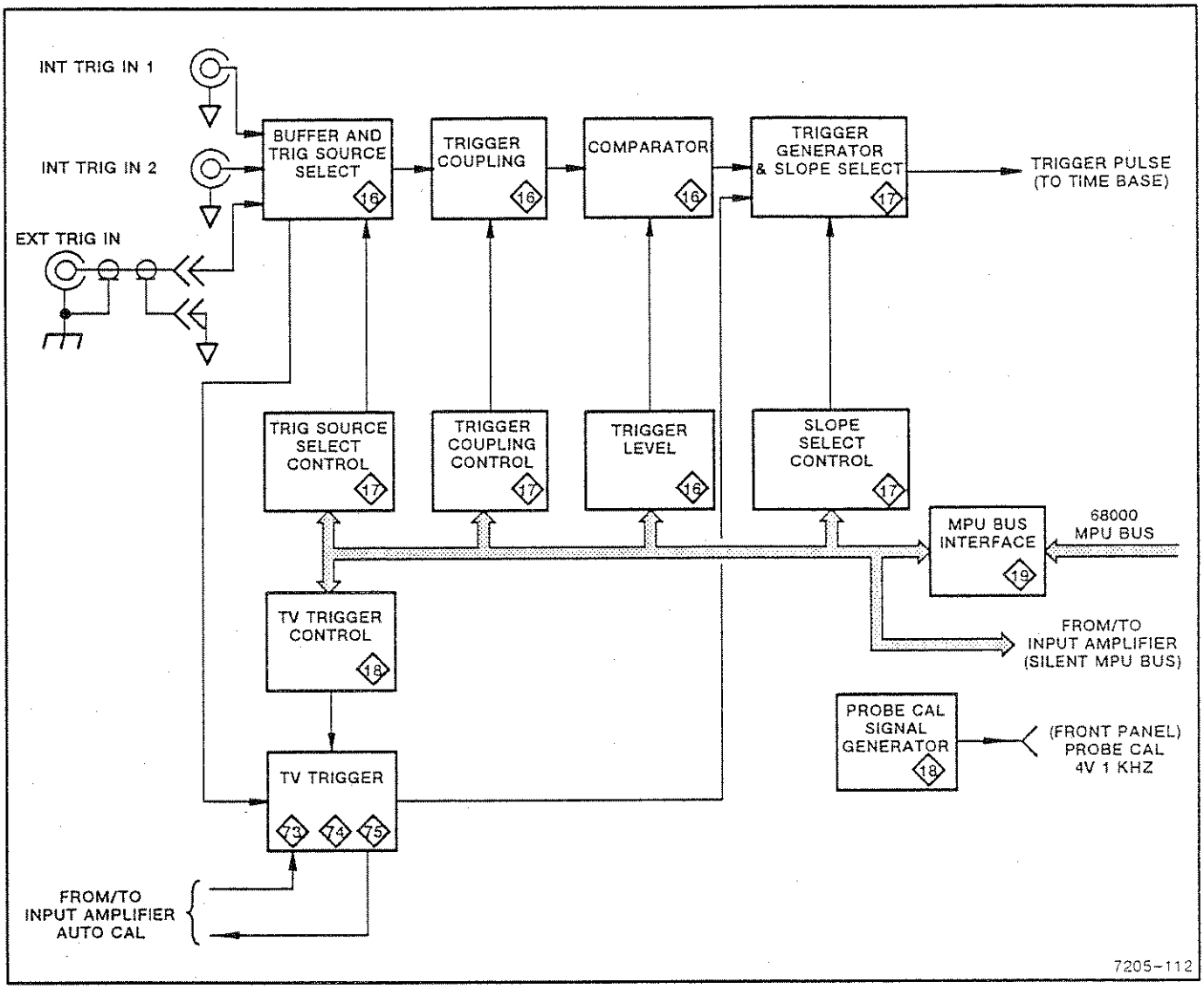


Fig. 1-32 Trigger Circuit Block Diagram

to low impedance by an emitter follower and buffer. The external trigger signal is transformed to low impedance in the same way through a FET source follower and emitter follower.

Channel 1, Channel 2, or external trigger signals are selected individually by FET switches and applied to the trigger coupling circuit. From there, they are converted to digital signals by a high-speed comparator and slope-selecter, and sent to the time base circuit as a trigger pulse.

The trigger circuit also interfaces with the Option 05 TV Trigger control and generates the 4-V, 1 kHz Probe Cal signal used for probe calibration.

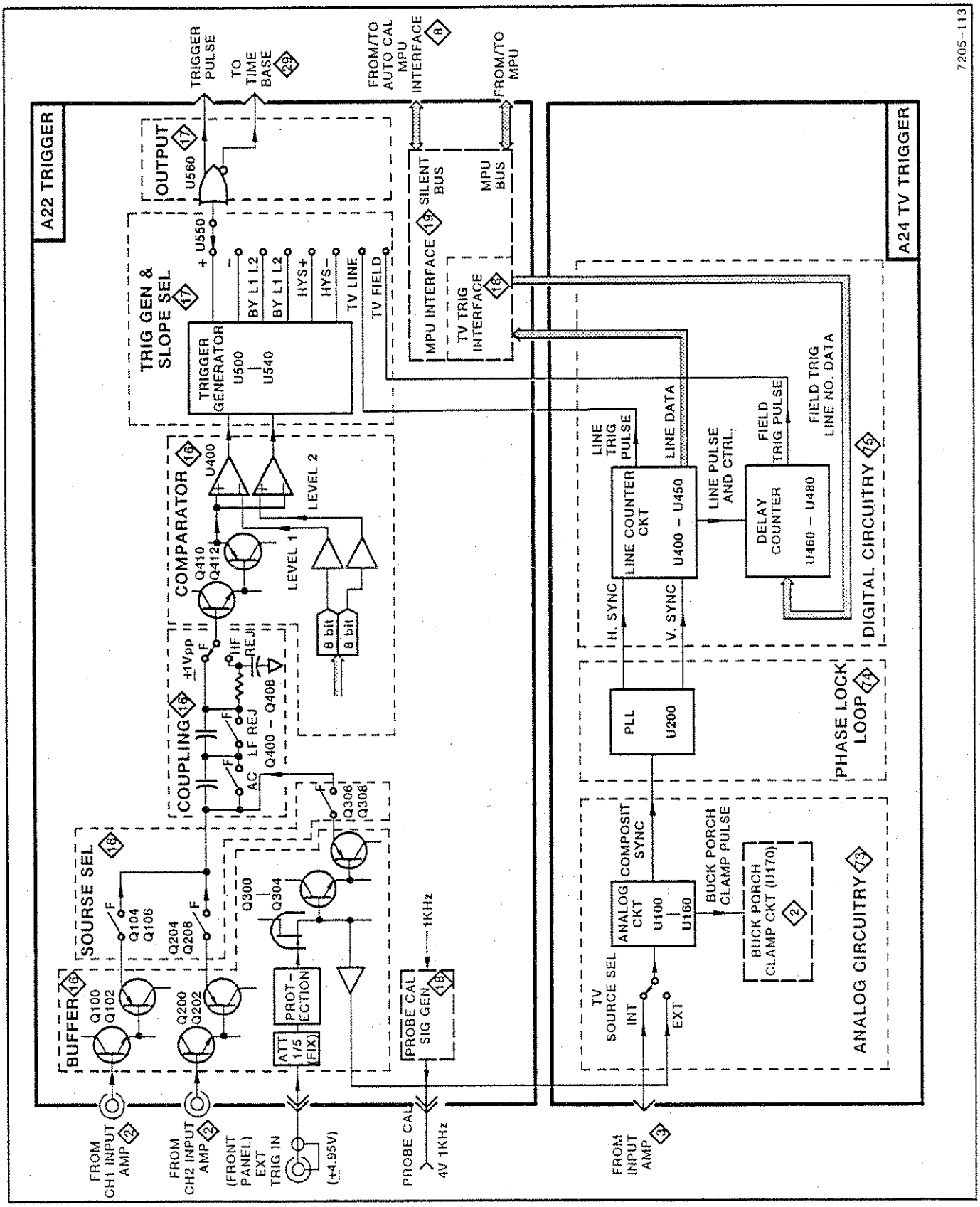


Fig. 1-33 Trigger Simplified Circuit Diagram

TRIGGER GENERATOR (DIAGRAM 16)

The trigger generator selects the internal or external trigger signal from the input amplifier and produces a trigger pulse. It consists of a buffer and trigger source select circuit, trigger coupling circuit, high-speed comparator, and trigger level circuit.

Buffer and Trigger Source Select

The buffer and trigger source select circuit (Figure 1-34) provides trigger source selection.

Internal trigger input 1 from the input amplifier is converted to low impedance by the emitter follower circuit Q100 and Q102. Subsequently, the trigger signal passes through FET switch Q106 to the coupling circuit. When a trigger signal is selected, Q106 turns on and Q104 turns off. If a trigger signal is not selected, switch Q106 turns off, cutting off the signal. At this point Q104 conducts and Q102 is completely cut off. The signal is fully cut off by Q102 and Q106, which improves the feedthrough characteristic.

Although there are different circuit designators, the above description also applies to the internal trigger input 2 and the external trigger input circuits, except that FET source follower Q300A is added to the external trigger, which increases input impedance. An attenuator also is included to adjust the external trigger input level to $\pm$ 4.95 V (99%). For the Option 05 TV trigger, the signal from the source follower is passed through the buffer by operational amplifier U300 and then output as the EXT SIG signal for the TV trigger.

Trigger Coupling Select

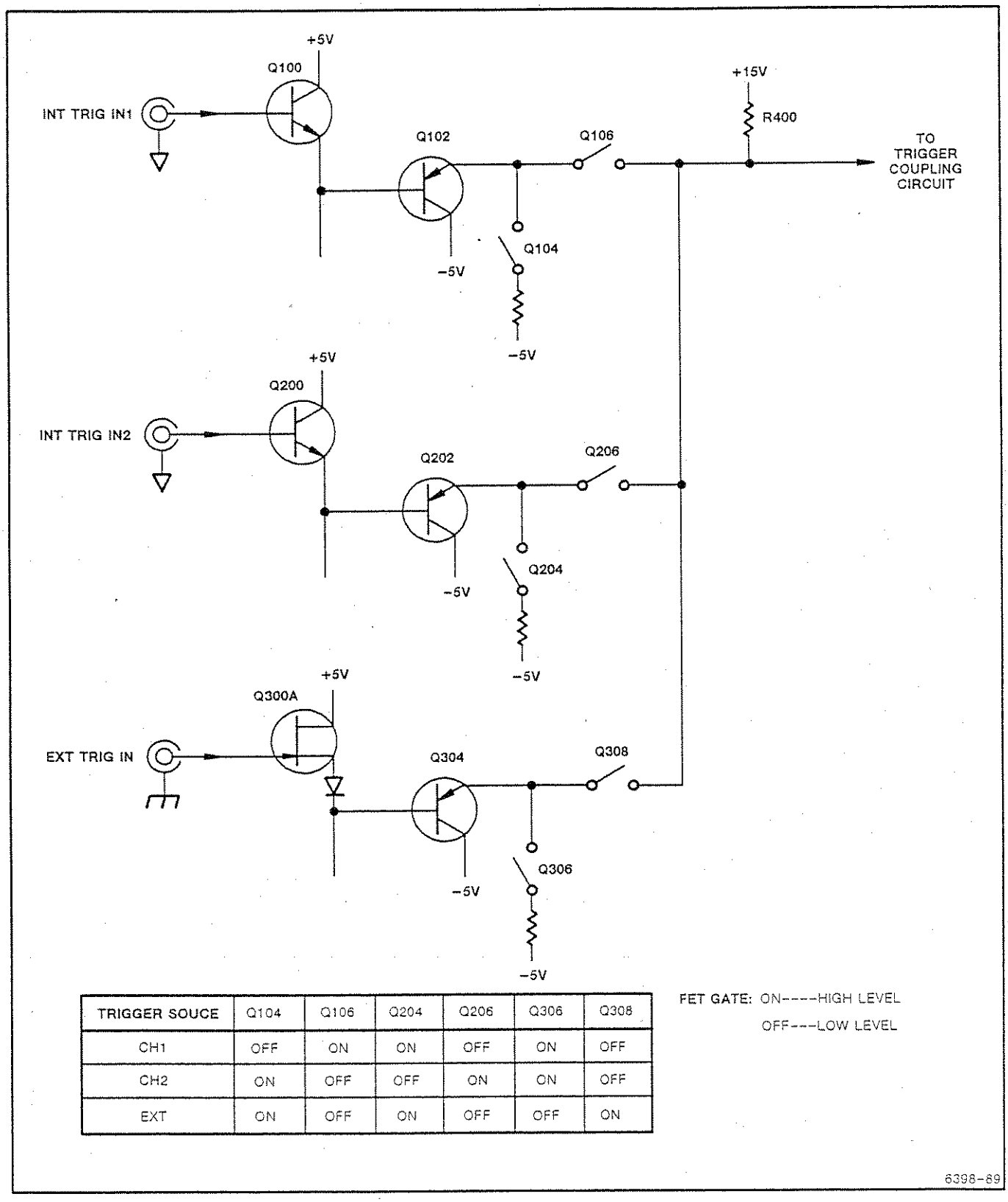
The trigger coupling select circuit (Figure 1-35) switches trigger coupling to DC, HF REJ, LF REJ, or AC. Switching is performed by seven FET switches Q400, Q402, and Q404-Q408. The dc HF REJ circuits Q404 to Q408 are T-configured to improve the feedthrough characteristic.

Comparator

The comparator circuit converts the signal selected by trigger coupling to an ECL level digital signal. It consists of buffers Q410 and Q412 and comparators U400A and U400B. Stabilizing comparator operation generates some hysteresis. The comparator output signal is divided into $\overline{\text{COMP1}}$ (comparator 1 output) from U400A with trigger level 1 used as the threshold level and $\overline{\text{COMP2}}$ (comparator 2 output) from U400B with trigger level 2 used as the threshold level, and then supplied to the trigger generator. When positive going trigger signal goes across the threshold level, $\overline{\text{COMP1}}$ goes low. Conversely when negative going trigger signal goes across the threshold level, $\overline{\text{COMP2}}$ goes low.

Trigger Level

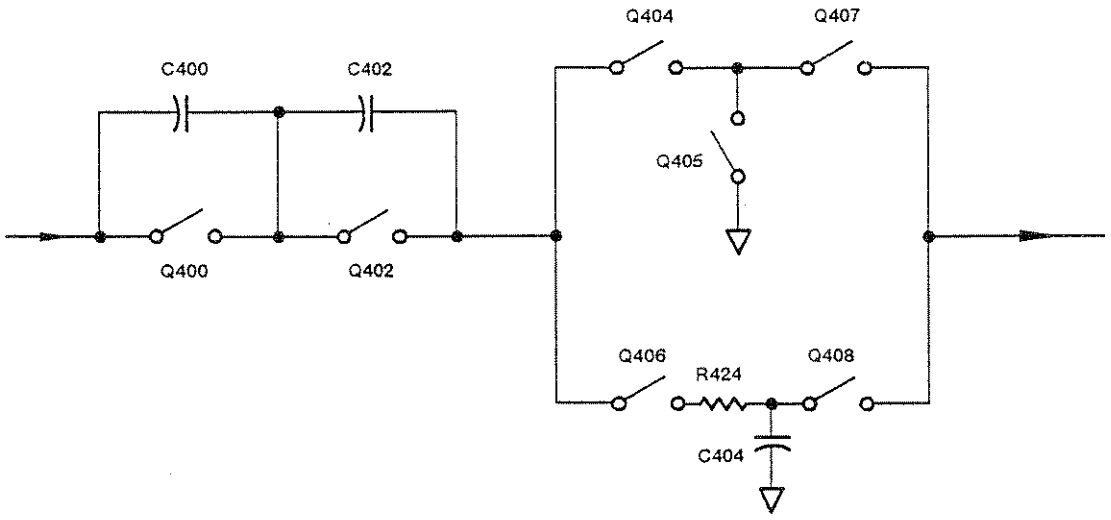
The trigger level circuit generates the dc voltage to set the comparator threshold level. Regulators U410 and U420 generate positive and negative reference voltages. These are selected by U430A and U430B for adjusting the polarity of the specified trigger level, which is applied to the output D/A converter U450. This output voltage is the specified trigger level that is used as the comparator threshold level.



TRIGGER SOUCE	Q104	Q106	Q204	Q206	Q306	Q308
CH1	OFF	ON	ON	OFF	ON	OFF
CH2	ON	OFF	OFF	ON	ON	OFF
EXT	ON	OFF	ON	OFF	OFF	ON

FET GATE: ON----HIGH LEVEL
OFF---LOW LEVEL

Fig. 1-34 Buffer and Trigger Source Select Simplified Circuit Diagram



TRIGGER COUPLING	Q400	Q402	Q404	Q405	Q407	Q406	Q408
DC	ON	ON	ON	OFF	ON	OFF	OFF
DC HF REJ	ON	ON	OFF	ON	OFF	ON	ON
LF REJ	OFF	OFF	ON	OFF	ON	OFF	OFF
AC	OFF	ON	ON	OFF	ON	OFF	OFF

6398-90

Fig. 1-35 Trigger Coupling Select Simplified Circuit Diagram

TRIGGER SLOPE CONTROL (DIAGRAM 17)

The trigger slope control circuit ensures that the trigger pulse conforms to the slope needs of the time base circuit (must be a positive-going pulse). It also switches the Option 05 TV trigger pulse. The circuit includes part of the MPU interface that is required for trigger circuit setting. This is explained further below on schematic 19.

Trigger Generator and Slope Selector

The trigger generator and slope selector (Figure 1-36) provide the associated trigger timing (Figure 1-37) for the time base. The $\overline{\text{COMP1}}$ and $\overline{\text{COMP2}}$ signals from the comparator are inverted by U505A and U505B to produce COMP1 and COMP2.

Trigger pulses corresponding to each trigger slope are produced using all four COMP signals.

When a positive slope is selected (Figure 1-37A) COMP1 is selected by U500A and the COMP1 positive-going edge becomes the trigger. When a negative slope is selected, $\overline{\text{COMP1}}$ is selected by U510A.

When BI slope is selected and Trigger Level 1 is greater than Trigger Level 2 (Figure 1-37B), the positive-going edges of COMP1 and COMP2 form the trigger. In the actual circuitry, the negative-logic OR of $\overline{\text{COMP1}}$ and $\overline{\text{COMP2}}$ is selected by U510B. When BI slope is selected and Trigger Level 1 is less than Trigger Level 2 (Figure 1-37C), the positive-going edges of COMP1 and COMP2 form the triggers. In the actual circuit, the logic AND from U500C is selected by U500D.

When HYS+ is selected and Trigger Level 1 is greater than Trigger Level 2 (Figure 1-37B), the trigger is reset on the positive-going edge of COMP2, then the next positive-going edge of COMP1 caused a trigger. Once the trigger occurs, it doesn't recur until it is reset. Even if Trigger Level 1 is less than Trigger Level 2 (Figure 1-37C), the trigger operation is exactly the same. In the actual circuit, the positive-going edges of COMP1 and COMP2 are detected by U520A and U520B, which set and reset U530A. The Q output of U530A, which is selected by U510C, becomes the trigger pulse.

When HYS– is selected and Trigger Level 1 is greater than Trigger Level 2 (Figure 1-37B), the trigger is reset on the positive-going edge of COMP1, then the COMP2 positive-going edge causes the trigger. Once the trigger occurs, it cannot recur until it is reset. Even if Trigger Level 1 is less than Trigger Level 2 (Figure 1-37C), the trigger operation is exactly the same. In the actual circuit, the positive-going edges of COMP1 and COMP2 are detected by U540A and U540B, which set and reset U530B. The Q output of U530B, which is selected by U510D, becomes the trigger pulse.

HYS+ and HYS– operate similar to the above descriptions, but they have different initial states (the condition before signals are input), and are implemented using two different sets of circuits.

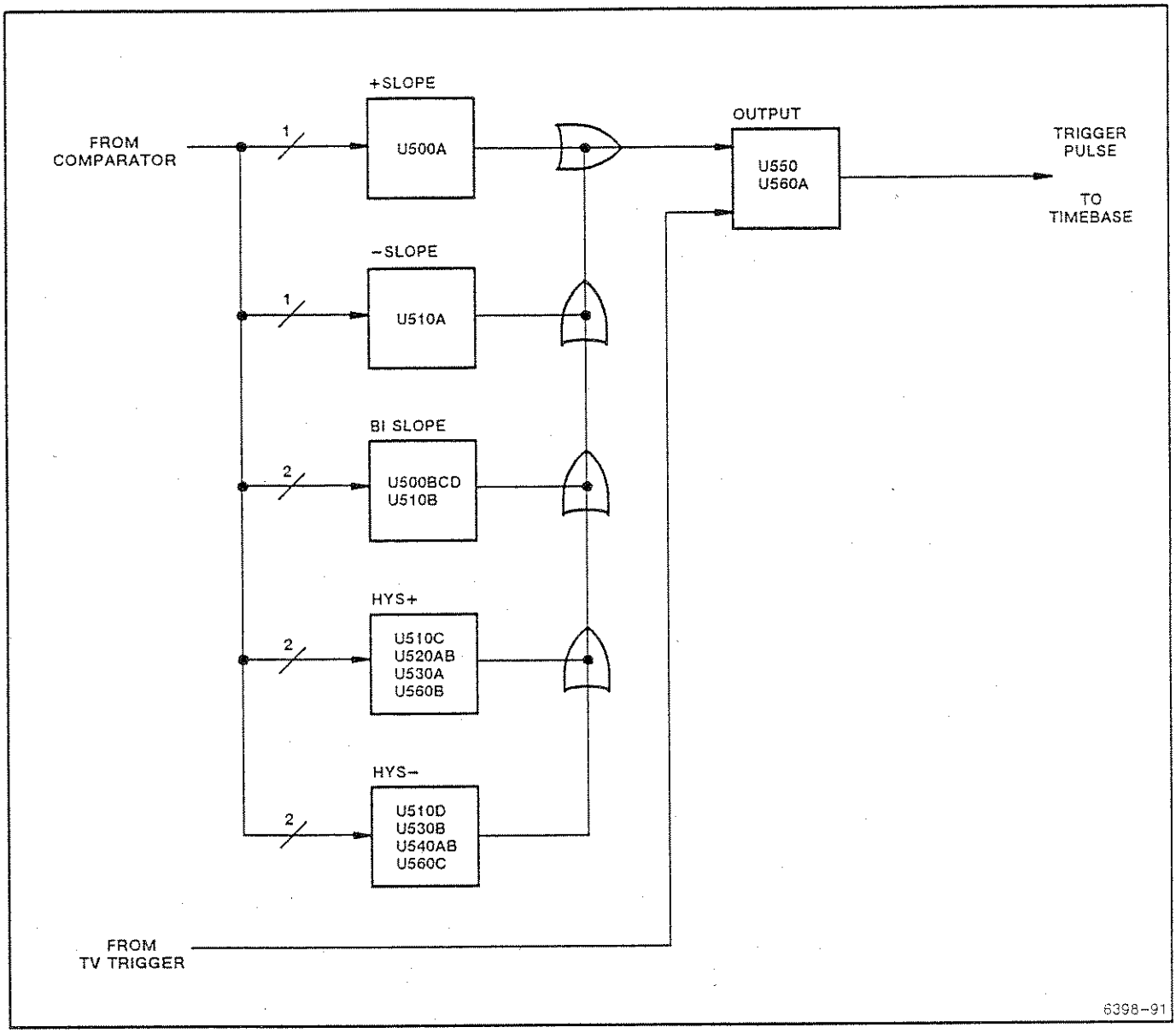


Fig. 1-36 Trigger Generator & Slope Selector Block Diagram

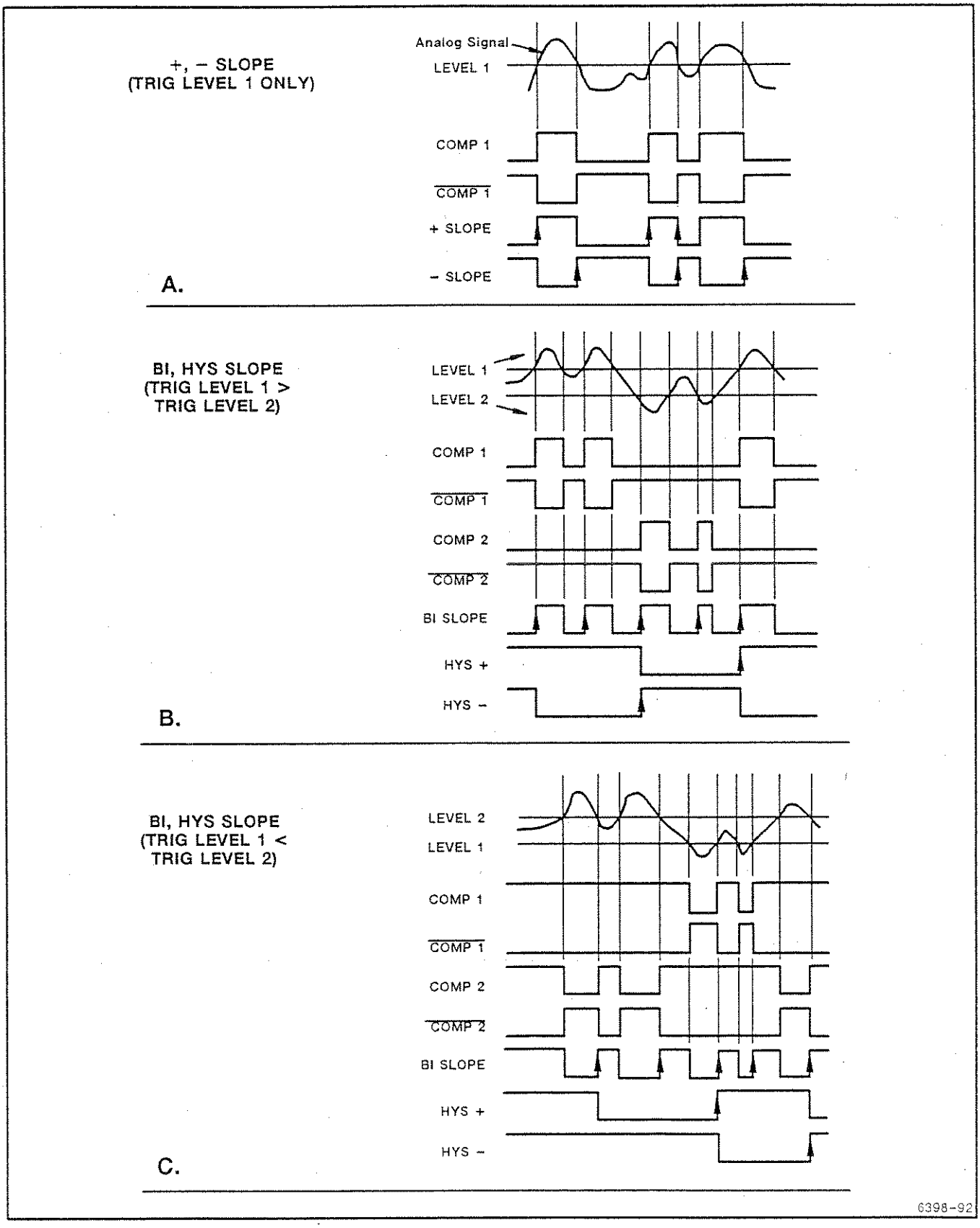


Fig. 1-37 Trigger Generator Timing Diagram

TRIGGER MPU INTERFACE (DIAGRAM 18)

Trigger MPU interface 1 consists of a trigger readback buffer, TV trigger interface, and a probe calibration signal generator. These interface circuits are explained under Trigger MPU Interface 2 (schematic 19 below).

Probe Calibration Signal Generator

The probe calibration signal generator consists of gates U700D and U700E, and drivers Q800, and Q802. The buffered TTL calibration clock (BCCLK) outputs an accurate 1 kHz, 50% duty cycle puise, which is converted to an accurate 4 V pulse by Q800 and Q802. Strap J800 is used for 4 V adjustment.

TRIGGER MPU INTERFACE 2 (DIAGRAM 17, 18, 19)

Trigger MPU interface circuitry (Figure 1-38) performs all interface functions between the trigger circuits and other instrument circuits shown on schematics 17, 18, and 19.

Schematic 17 shows the trigger source select control, trigger coupling control, and trigger slope select control; schematic 18 shows the trigger readback, TV trigger set up, and TV trigger readback circuits; and schematic 19 shows the address decoder, trigger polarity control, and silent MPU bus buffer circuits.

Trigger Source Select Control

The trigger source select control circuit controls the trigger source FET switch. MPU bus data latched by U600A, U600B, and U600C is complemented by U620, U630A, and U630B to control the FET switch gates.

Trigger Coupling Control

The trigger coupling control circuit controls the FET switch for trigger coupling switching. MPU bus data latched by U600D, U600E, and U600F is complemented by U630C, U630D, and U640 to control the FET switch gates. Only the dc HF Rej control signal is generated as a complement signal.

Trigger Slope Select Control

The trigger slope select control circuit controls the trigger generator slope selector ECL gate. MPU bus data latched by U600G, and U600H, and U610 is converted from a TTL to ECL level at R604, R606, and R608, to control the slope selector ECL gate.

Trigger Readback

The trigger readback circuit is used by diagnostics for trigger pulse readback and latch data readback. Level shifter U580 converts signals from an ECL to TTL level and applies them through driver U650 to the MPU bus.

TV Trigger Setup

The TV trigger setup circuit sets up each circuit of the Option 05 TV Trigger option. MPU bus data latched by U680 and U690 is supplied through the main interconnect board to perform TV trigger circuit setup. Buffers U700A and U700B provide readback bit fault isolation.

TV Trigger Readback

The TV trigger readback circuit detects whether Option 05 TV trigger is installed or not, what the current TV line number is, and performs readback functions for diagnostics. All data is linked to the MPU bus through U660 and U670.

MPU interface circuits for the TV trigger option must be identified whether or not the option is installed; therefore, this circuit is included in the standard instrument.

Address Decoders

Address decoders U760, U770, and U780 provide MPU bus address decoding for the trigger level setting D/A converter (U760), the latches required for each setup relating to the trigger generator and readback buffer (U770), and circuits relating to the TV

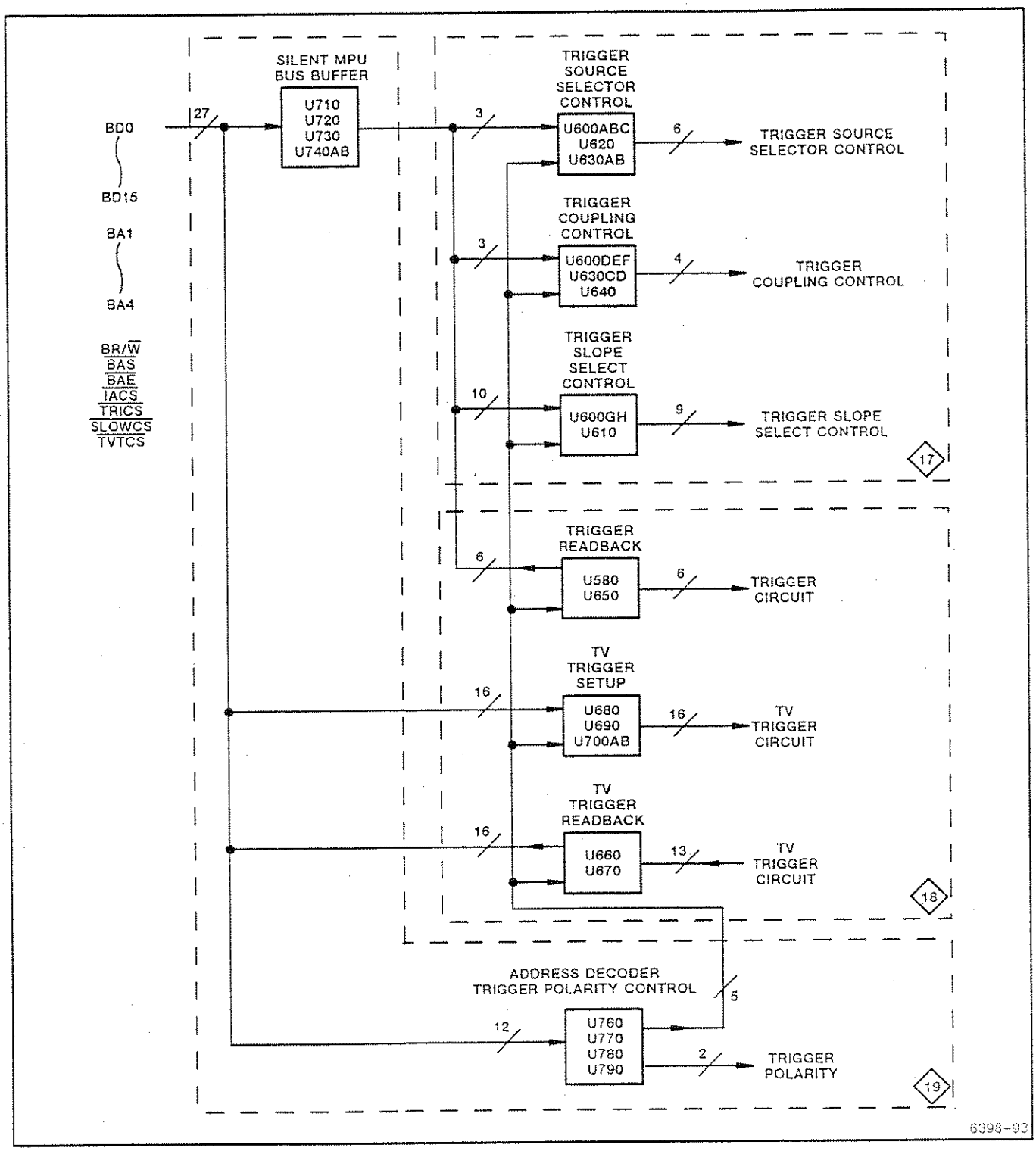


Fig. 1-38 Trigger MPU Interface Block Diagram

trigger (U780). Addressable latch U790 stores the trigger level polarity setting.

Silent MPU Bus Buffer

As explained earlier, input analog circuits are highly susceptible to noise, especially from the MPU bus. Therefore, an unusual MPU bus, referred to as the silent bus (Figure 1-39), is used to minimize the noise effects.

During waveform acquisition, the MPU bus is disabled. It is enabled only when the MPU accesses the analog section (except for the TV trigger, which is connected to the normal MPU bus). Buffers U710 and U720 handle data from the bus, and buffer U730 handles address and control functions.

When the MPU accesses the analog section (except for the TV trigger), the buffered analog enable signal $\overline{BAE}$ is set low and buffer U730 is enabled. This enables the address bus and the control bus. When the required chip-select signals (input amplifier chip select: $\overline{IACS}$; trigger chip select: $\overline{TRICS}$; and slow chip select: $\overline{SLOWCS}$) are received through U740A and U730, they enable U710 and U720. Under these conditions, the silent MPU bus and normal MPU bus operate identically.

When an MPU read/write cycle is completed, the chip-select signal becomes high disabling U710 and U720. If $\overline{BAE}$ is released, U730 is disabled, and the MPU bus is disconnected from the entire MPU to eliminate noise generation and to ensure its silence.

If $\overline{BAE}$ cannot be released while it is active and an interrupt is applied to the MPU, the chip-select signal is released to disable U710 and U720 and prevent MPU bus data contention. The negative-logic OR of $\overline{IACS}$ and $\overline{SLOWCS}$ is applied through U730 to produce the input amplifier enable signal $\overline{IAEM}$, which is sent to the A16 Channel 2 input amplifier for use as the input amplifier MPU bus buffer control signal.

ACQUIRED DATA STORAGE

The acquired data storage circuits (Figure 1-40) accept data from the Channel 1 and 2 A/D converters and prepare it for storage in memory.

In the high speed mode, 10-bit data from the Channel 1 A/D converter is temporarily stored in the Channel 1 first latch by the Channel 1 clock (SCK1). Then at the Channel 2 clock (SCK2), it is loaded into the Channel 1 second latch. Channel 2 data is simultaneously loaded into the Channel 2 first latch.

In normal mode, the Channel 1 first latch is set to the through mode, and at SCK2, Channel 1 data is stored in the Channel 1 second latch, while Channel 2 data is stored in the Channel 2 first latch. Data stored in each latch is shifted 2 bits in the odd and even data registers of each channel, then loaded synchronously into the SYNC (synchronized) data latch. From there it passes through an ECL-to-TTL conveter and is shifted 4 bits by a high-speed shifter. This 4-bit shifted data is then loaded into the memory input latch. The result of these operations is that the data from the A/D converter is shifted 8 bits, thus extending word rate to 1/8 of sampling clock for writing into waveform memory.

Waveform memory consists of a 128K X 10-bit CMOS memory for each channel. An address generator generates the memory address and the write pulse. After data is loaded into the memory input latch and a write pulse generated, the memory address is updated. Since the same pins are used for both data input and output to the waveform memory, 8 words X 10-bits of data is converted to 1 word X 10-bits of data in the memory data buffer then applied through the data bus buffer to the MPU bus. These buffers are interchangeable, so waveform data can be transferred from memory to the MPU, or visa versa. When averaging is selected, an averager circuit between the memory data buffer and the data bus buffer averages the acquired data.

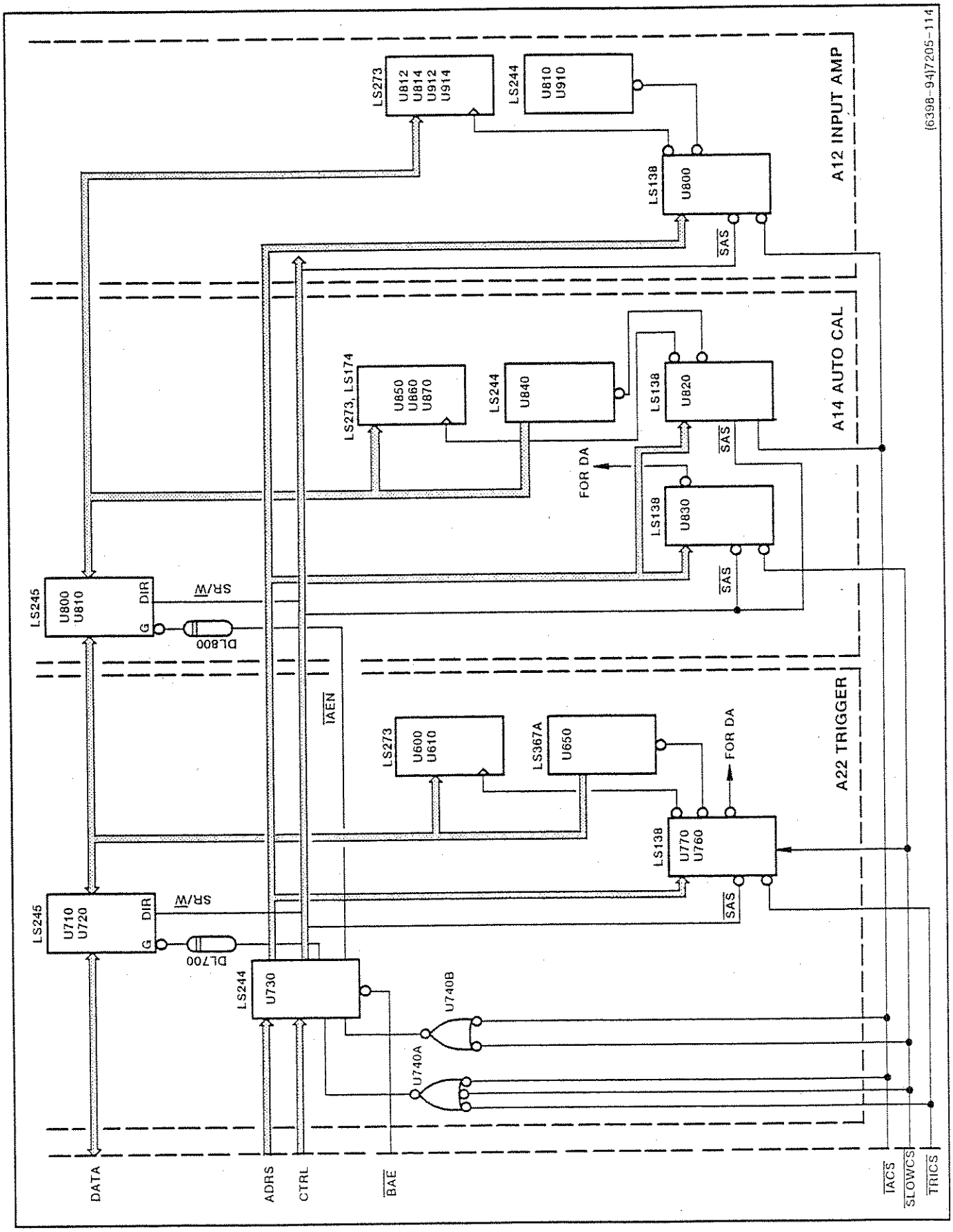


Fig. 1-39 Silent Bus Block Diagram

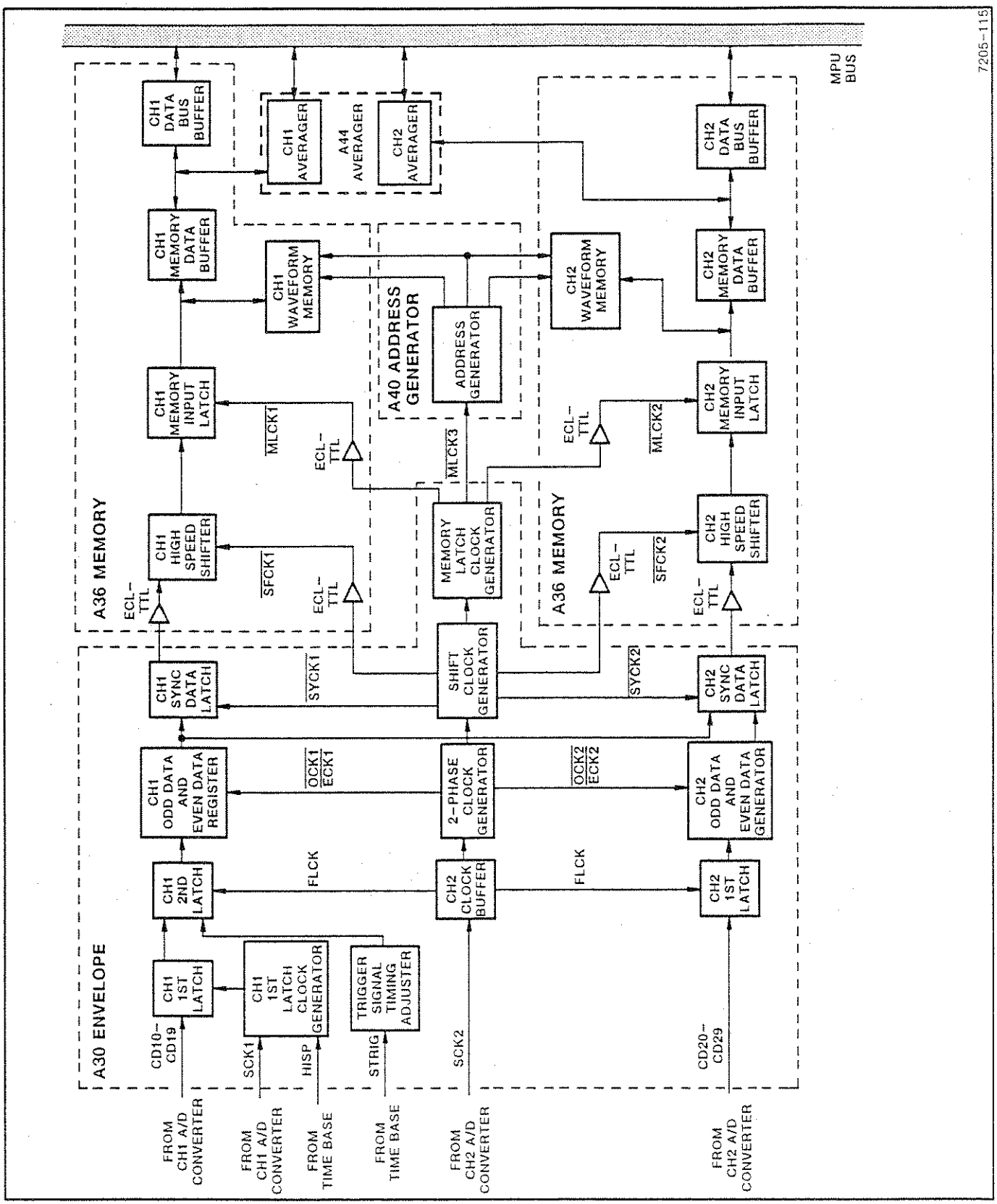


Fig. 1-40 Acquired Data Storage Block Diagram

CHANNEL 1 INPUT AND DIRECT A/D OUTPUT (DIAGRAM 20)

The Channel 1 input and direct A/D output circuits (Figure 1-41) accept and latch data from the Channel 1 A/D converter and supply outputs to the second latches and through output buffer to the rear panel A/D output connector. These circuits include a Channel 1 first latch timing generator, Channel 1 first latch, Channel 1 second latch, Channel 1 odd data register, Channel 1 even data register, Channel 1 direct A/D out circuit, and the trigger signal timing adjuster.

Channel 1 First Latch Timing Generator

The Channel 1 first latch timing generator determines whether the A/D converter data is latched by the Channel 1 first latch or whether it is set in the through mode. It consists of U300D, U300A, DL300, AND U316.

The Channel 1 clock signals (SCK1 and $\overline{SCK1}$) are applied to line receiver U300A. Its positive output is applied to U302E and its negative output is connected to U302D through delay line DL300. During high-speed mode acquisition, control signal HISP is

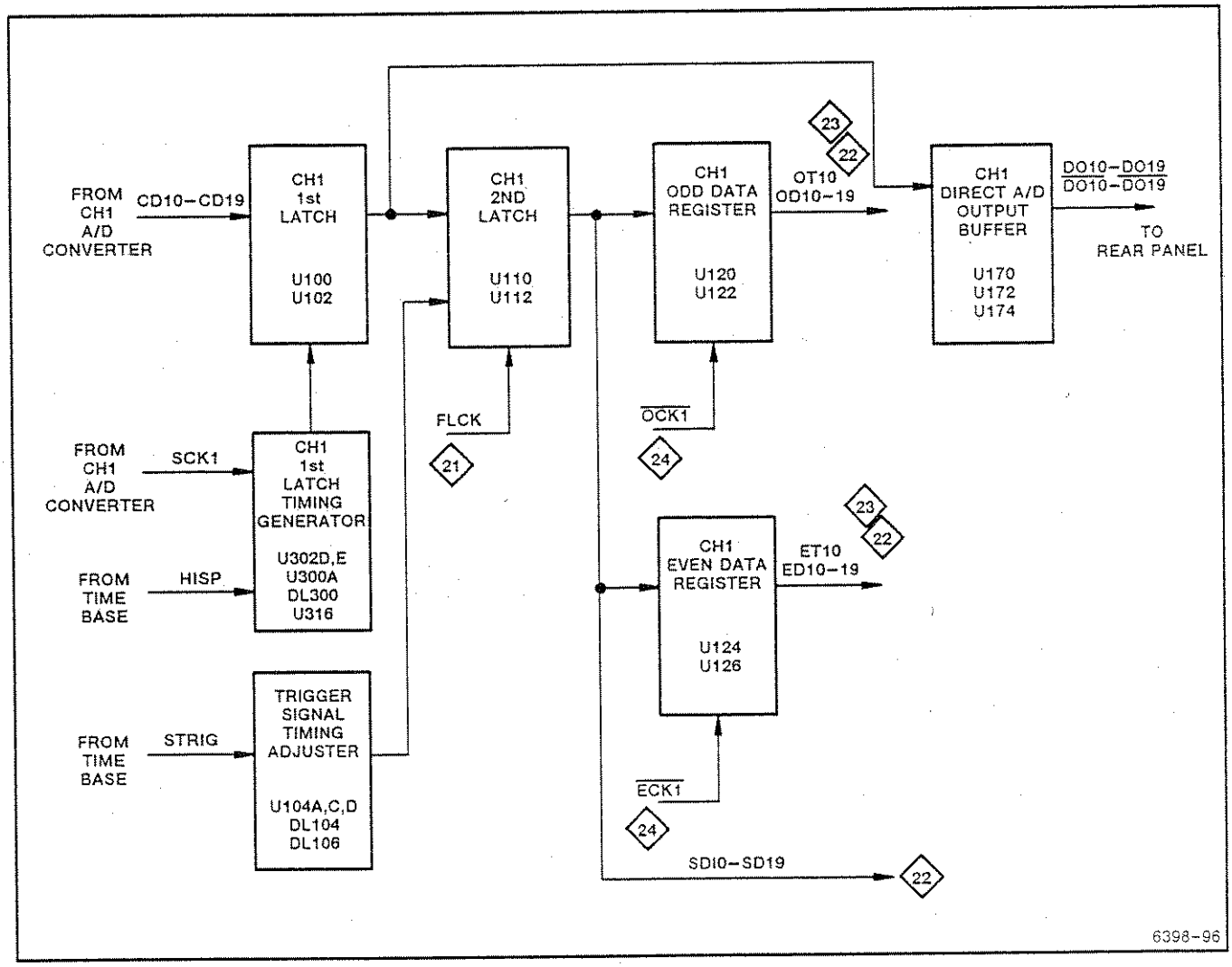


Fig. 1-41 Channel 1 Input & Direct A/D Output Block Diagram

set high to enable gates U302D and U302E. The outputs of these gates are applied to the Ea and Eb pins of latches U100 and U102, respectively. Since Ea and Eb are OR'd within U100 (U102) and the Ea pin signal arrives at a delay of about 2 ns with respect to Eb pin signal, the OR'd output of these latches becomes the clock signal.

In the normal acquisition mode, HISP becomes low, inhibiting U302E and U302D. This causes pins Ea and Eb to go low, setting latches U100 and U102 in the through mode.

Channel 1 First Latch and Second Latch

The Channel 1 first latch (U100 and U102) and the Channel 1 second latch (U110 and U112) are used to store the A/D converter output data. The primary use of the Channel 1 first latch is during high-speed mode where the Channel 1 data is acquired at a 180 degree phase difference with respect to Channel 2 data.

During high-speed mode, the clock signal from the Channel 1 first latch timing generator latches the data into the Channel 1 first latch. Then the data stored in the Channel 1 first latch is transferred to the Channel 1 second latch on the Channel 2 clock signal (FLCK). This action ensures that writing of the acquisition data is synchronized with the Channel 2 clock signal. During normal mode, the Channel 1 first latch is set to through mode. Thus, the Channel 1 data is loaded into the Channel 1 second latch after the gate delay time.

Channel 1 Odd and Even Data Registers

The Channel 1 odd data registers (U120 and U122) and even data registers (U124 and U126) perform a 2-bit data shift. To accomplish this data shift, data stored in the Channel 1 second latch is transferred alternately to the Channel 1 odd and Channel 1 even data registers on the clock signals $\overline{\text{OCK1}}$ and $\overline{\text{ECK1}}$, which are 2-phase clock pulses produced from the Channel 2 acquisition clock SCK2. These clock signals are explained in more detail under the Two-Phase Clock Generator and Two-Phase Clock Buffer topic for schematic 24.

Channel 1 Direct A/D Output Buffer

The Channel 1 direct A/D output buffers (U170, U172, and U174) supply A/D output data to the rear panel connector. Each complementary output of the Channel 1 first latch is stored in these buffers and then output through connector J302, the A/D OUT connector on the rear panel.

Trigger Signal Timing Adjuster

The trigger signal timing adjuster compensates for the difference between the analog signal A/D conversion delay time and the trigger signal delay through gates U104A, U104C, and U104D, and delay lines DL104 and DL106. The timing of trigger signal (STRIG) is adjusted with the P106 strap on delay line DL106 to ensure that the timing of the data from the A/D converter agrees with that of the triggered data.

CHANNEL 2 INPUT AND DIRECT A/D OUT (DIAGRAM 21)

The Channel 2 input and direct A/D out circuits (Figure 1-42) perform a similar function as those for Channel 1, except Channel 2 doesn't have a second latch or its associated timing circuits. They consist of the Channel 2 first latch, Channel 2 clock buffer, Channel 2 odd data register, Channel 2 even data register, and Channel 2 direct A/D OUT buffer.

Channel 2 First Latch/Clock Buffer

The Channel 2 first latches (U212 and U210) are loaded with the output of the Channel 2 A/D converter on clock signal FLCK, which is the Channel 2 clock signal (SCK2) from buffer U302A. Channel 2 clock signal (SCK2) is buffered through U302B and U302C to create clock signals MCK1 and MCK2, which then become the source clock for the acquisition timing generator schematic 24.

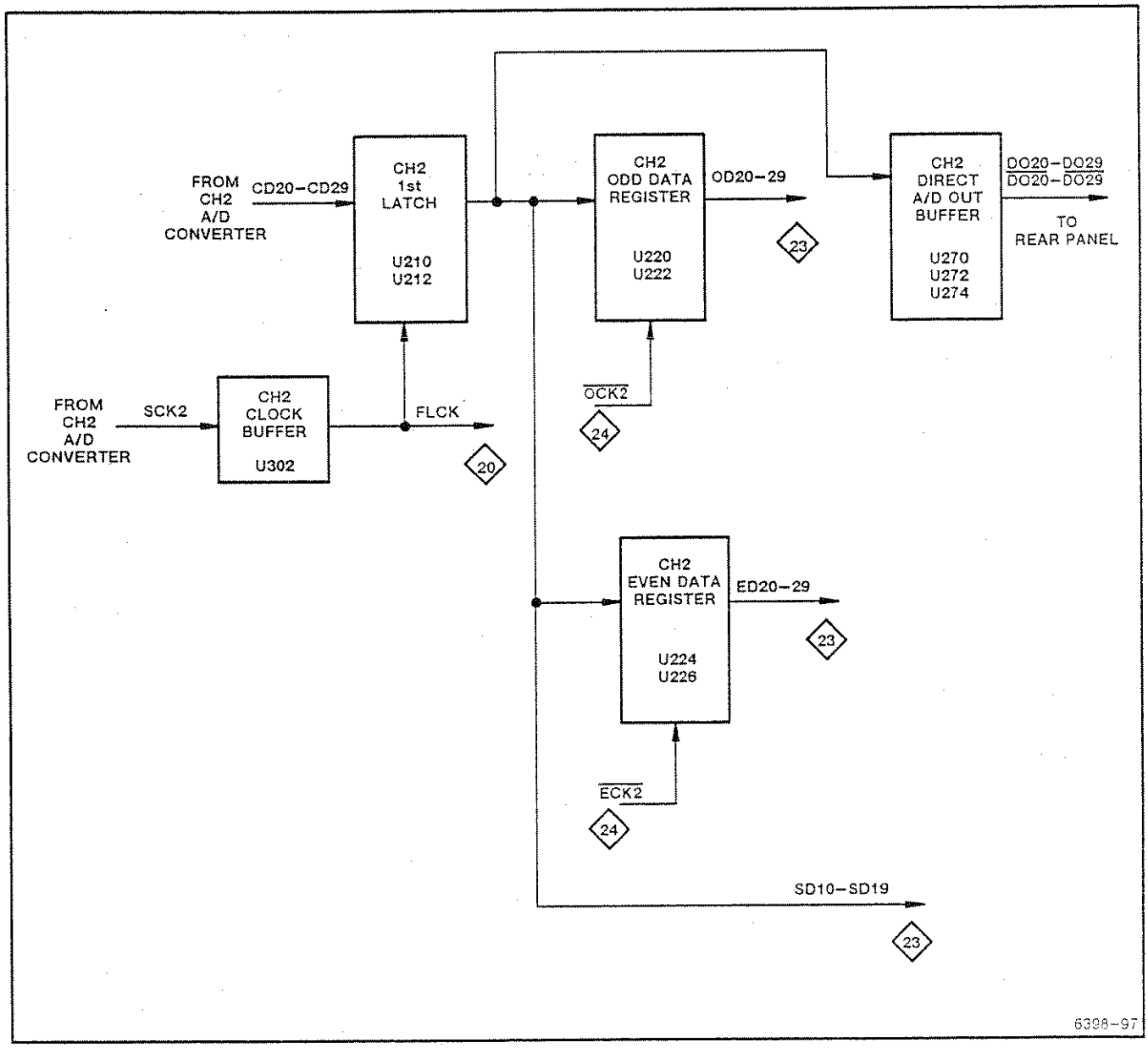


Fig. 1-42 Channel 2 Input & Direct A/D Output Block Diagram

Channel 2 Odd Data Register/Even Data Register

The Channel 2 odd and even data registers (U220 and U222, and U224 and U226) operate exactly the same as the Channel 1 odd and even data registers.

Channel 2 Direct A/D Out Buffer

The Channel 2 direct A/D output buffer consisting of complementary output gates U270, U272, and U274 operate exactly the same as the Channel 1 direct A/D OUT buffers.

CHANNEL 1 COMPARATOR AND SYNC DATA LATCH (DIAGRAM 22)

The Channel 1 maximum and minimum comparators (Figure 1-43) are not used at this time.

The Channel 1 sync data latch (U130, U132, U134, and U136) (Figure 1-43) stores the shifted Channel 1 data providing an extended data valid time for transfer of data to memory. Two-phase separated data from the odd and even data registers are synchronously loaded into the Channel 1 sync data latch on the $\overline{\text{SYCK1}}$ clock signal. Data stored in the Channel 1 sync data latch is converted from ECL to TTL on the memory board, then applied to the 4-bit shift register.

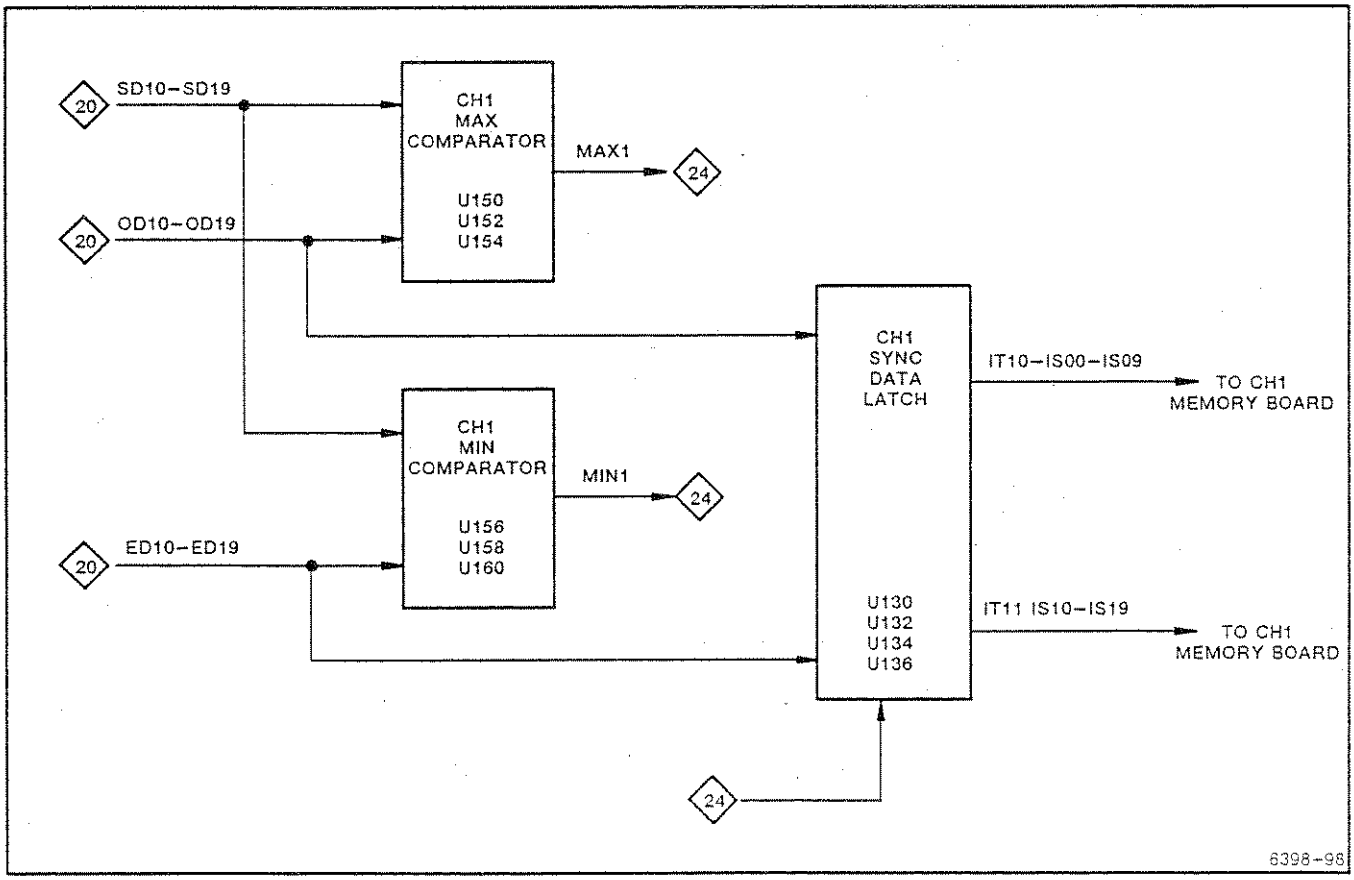


Fig. 1-43 Channel 1 Comparator and Sync Data Latch Block Diagram

CHANNEL 2 COMPARATOR AND SYNC DATA LATCH (DIAGRAM 23)

The Channel 2 maximum and minimum comparators (Figure 1-44) are not used at this time.

The Channel 2 sync data latch (U230, U232, U234, U236, U238, and U240) comprise a latching multiplexer. In the Channel 1 only mode, the CH1 ONLY signal from the time base board is set high, pin 13 of U316 becomes low, and the multiplexer selects the Channel 1 odd and even data register data. In all other modes, the Channel 2 odd and even data register data is selected. Selected data is loaded into the latch section on the clock signal $\overline{\text{SYCK2}}$.

ACQUISITION TIMING GENERATOR (DIAGRAM 24)

The acquisition timing generator (Figure 1-45) produces clock pulses for storing data from the A/D converter into the registers and for storing data in the 4-bit register on the memory board. It also generates clock pulses for the memory input latch and address generator board. The envelope mode strobe generator and envelope mode timing generator are not used.

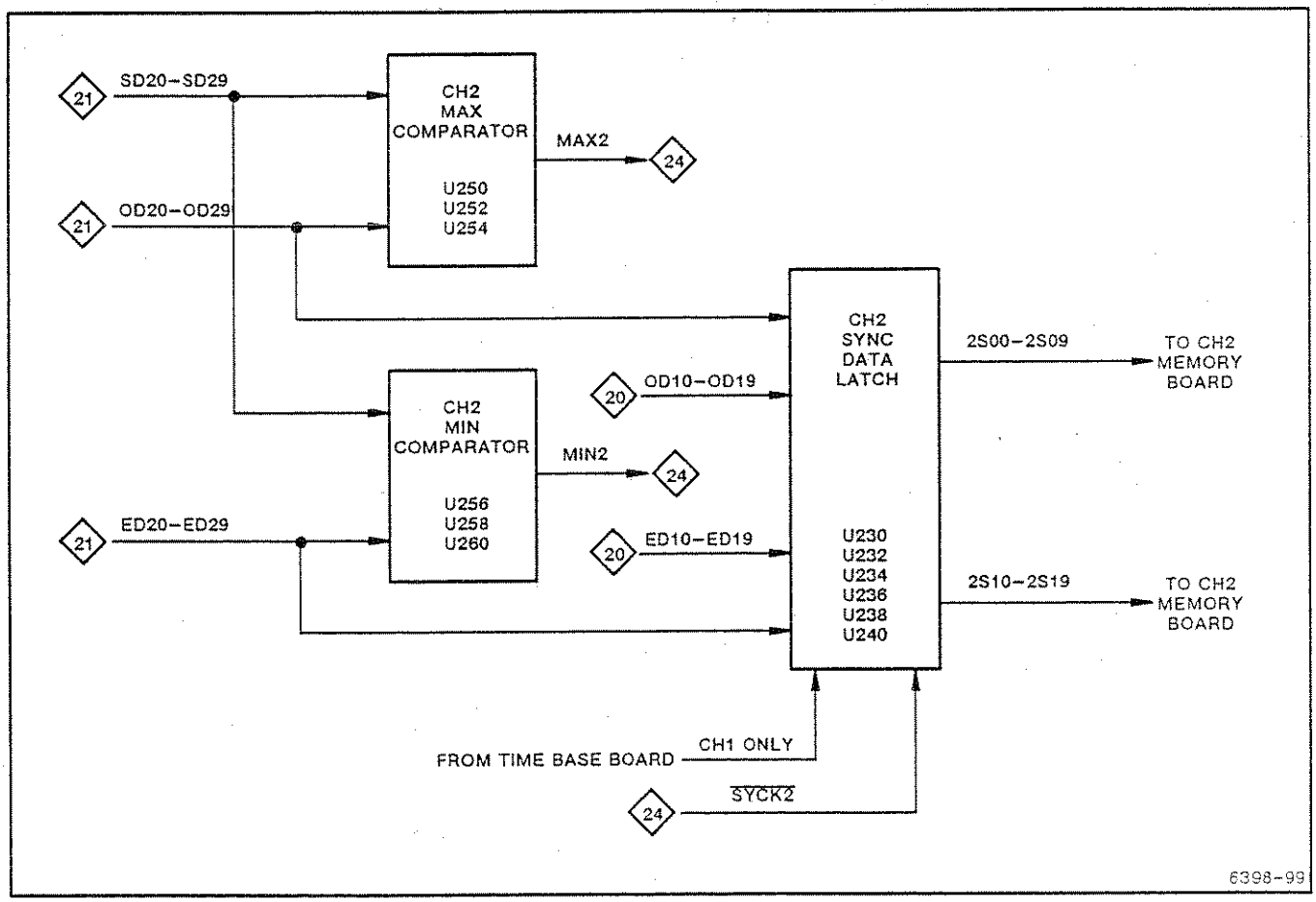


Fig. 1-44 Channel 2 Comparator & Sync Data Latch Block Diagram

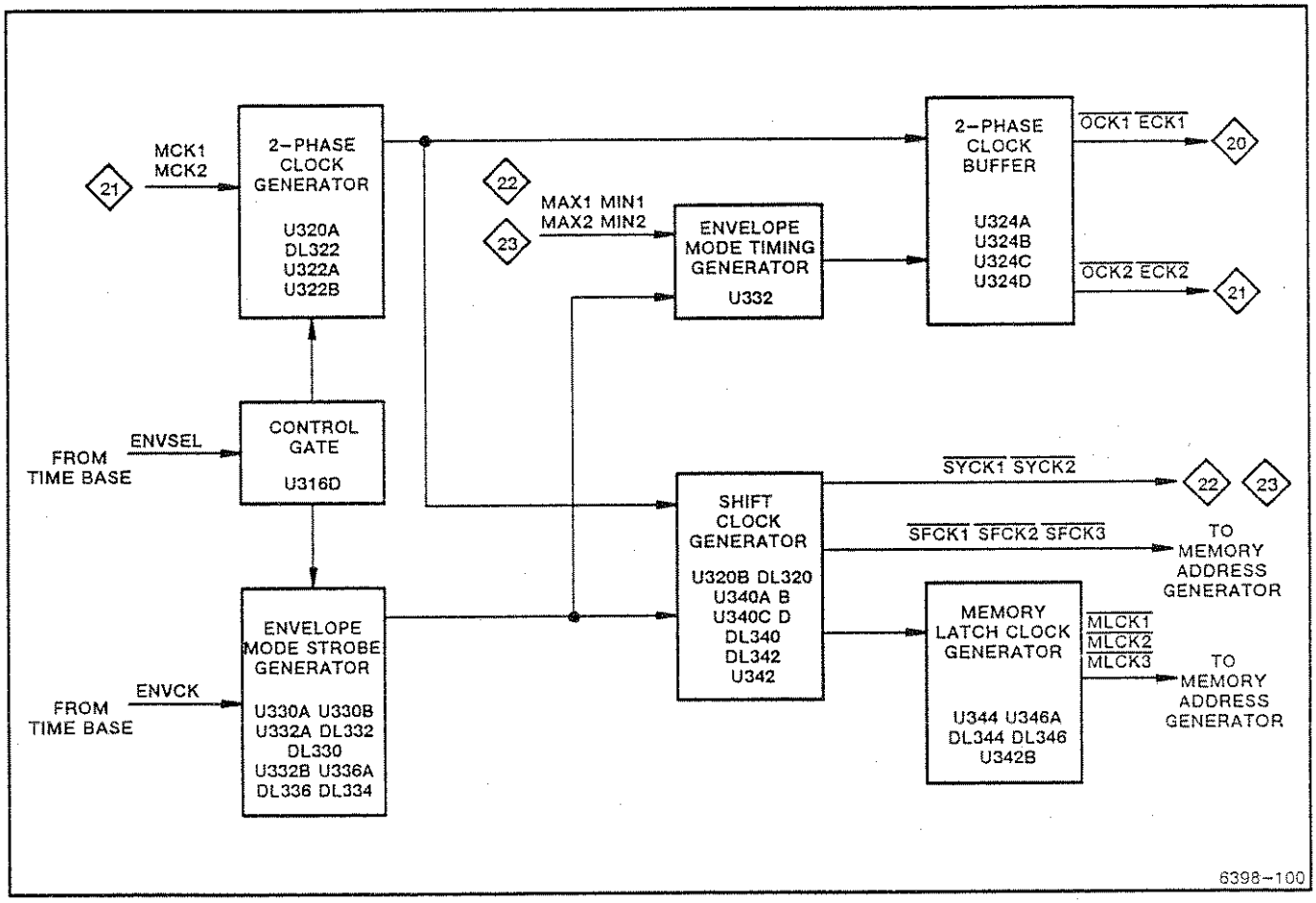


Fig. 1-45 Acquisition Timing Generator Block Diagram

Two-Phase Clock Generator and Two-Phase Clock Buffer

The two-phase clock generator consisting of D-type flip flops U320A, U322A, U322B, and delay line DL322 generate clock pulses for the Channel 1 and Channel 2 odd and even data registers.

Channel 2 clock pulse (SCK2) is divided into two buffered signals (MCK1 and MCK2) by U302B and U302C in the clock buffer. These signals then drive flip flop U320A and DL322 to produce a two phase, approximate 4 ns clock which is applied through flip-flops U322A and U322B and two-phase clock buffers U324A, U324B, U324C, and U324D to become clock signals OCK1, OCK2, ECK1, and ECK2. The timing relationships for creation of these clock signals is shown in Figure 1-46.

Shift Clock Generator

The shift clock generator produces the $\overline{\text{SYCK1}}$ and $\overline{\text{SYCK2}}$ clock signals for loading data into the Channel 1 and Channel 2 sync data latches, the shift clock pulses $\overline{\text{SFCK1}}$ and $\overline{\text{SFCK2}}$ required for the 4-bit shift register in the memory circuits, and other pulses. It consists of D-type flip-flop U320B, delay lines DL320, DL340, and DL342, and gates U340A, U340B, U340C, and U340D.

Flip flop U320B and delay line DL320 produce a 5 ns pulse on the rising edge of the two-phase clock generator flip-flop U322B Q and apply it to gates U340A, U340B, U340C, and U340D. Gates U340A and U340B create the $\overline{\text{SYCK1}}$ and $\overline{\text{SYCK2}}$ clock pulses for the sync data latches.

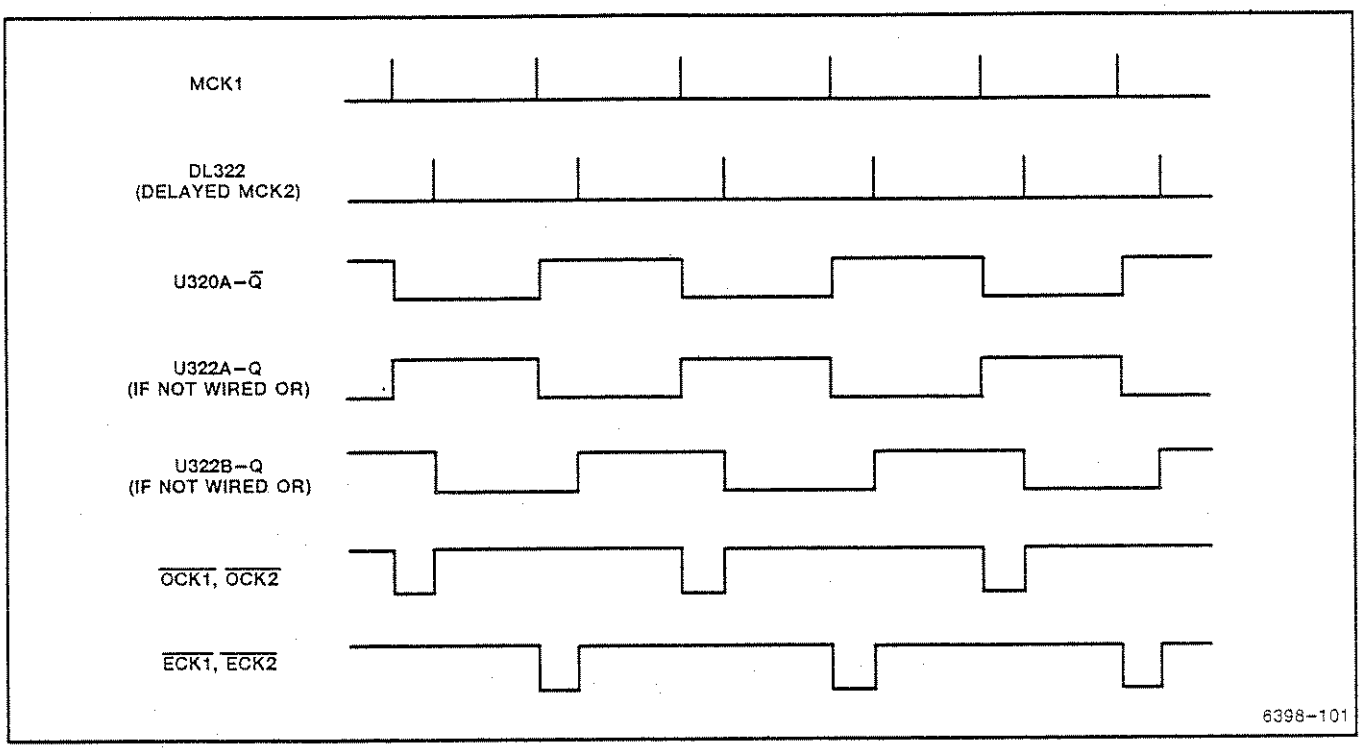


Fig. 1-46 Two-Phase Clock Generator Timing Diagram

The signal from gate U340C is applied through delay line DL340 to gate U342A to become shift clock pulses $\overline{SFCK1}$ and $\overline{SFCK2}$ for the high-speed shifter on the A36 memory board, and clock pulse $\overline{SFCK3}$ for the A40 address generator board trigger data shift circuit. The output of gate U340D provides input to the memory latch clock generator.

Memory Latch Clock Generator

The memory latch clock generator operates as a one-shot pulse generator to produce clock signals for the memory and address generator boards. It consists of counter U344, gates U346A and U342B, and delay lines DL344 and DL346.

Counter U344 converts each four shift clock generator pulses into a 7 ns pulse at Q2 (pin 15). This pulse is applied through DL346 and U342B to create signals $\overline{MLCK1}$, $\overline{MLCK2}$ and $\overline{MLCK3}$, then distributed to the Channel 1 and Channel 2 memory board and address generator board.

MEMORY

The memory circuits (Figure 1-47) consist of an ECL-TTL translator and high-speed shift register, a memory input latch, waveform memory, and the memory MPU interface. There are two memory sections, one for Channel 1 and one for Channel 2. Each memory is identical and provides a 128K word X 10-bit capacity. The A30 envelope circuits supply data and clock pulses, and the A40 address generator provides signals for memory control, addressing, and chip select.

ECL data arriving from the envelope circuit is converted to TTL by the ECL-TTL translator, converted from serial data to parallel data by the high-speed shifter, then latched into the memory input latch for writing into waveform memory. The memory interface circuits consists of the memory data and data bus buffers.

ECL-TTL Translator and High-Speed Shift Register (DIAGRAM 25)

The ECL-TTL translator (U100, U102, U104, U106, U108, and U110) converts IS00-IS19 data and the two clock pulses $\overline{\text{MLCK1}}$ (memory latch clock 1) and $\overline{\text{SFCK1}}$ (shift clock 1) from ECL to TTL levels. This converted data is applied to the high-speed shifter consisting of the 20 shift registers (U200-U238), which converts the serial TTL data to parallel TTL data under control of the buffered shift clocks $\overline{\text{BFCK1}}$ and $\overline{\text{BFCK2}}$.

MEMORY STORAGE LATCH (DIAGRAM 26)

The memory storage latch temporarily stores data while it is being read into memory. It consists of 10 flip flops (U240-U258). When the high-speed shifter data has been shifted four times, its output is stored in the memory latch on the memory latch clock signal ($\overline{\text{BMCK}}$). This stored data is then output on the memory latch enable signal ($\overline{\text{MLE}}$).

WAVEFORM MEMORY (DIAGRAM 26 & 27)

Waveform memory consists of 24 RAMs (U300-U346). Data from the memory input latch is written into the RAM selected by $\overline{\text{MSA}}$ through $\overline{\text{MSH}}$ (memory chip select A through H) when pulses $\overline{\text{WTEL1}}$ (write enable for lower byte1), $\overline{\text{WTEL2}}$ and $\overline{\text{WTEU}}$ (write enable for upper byte) occur. Normally when acquisi-

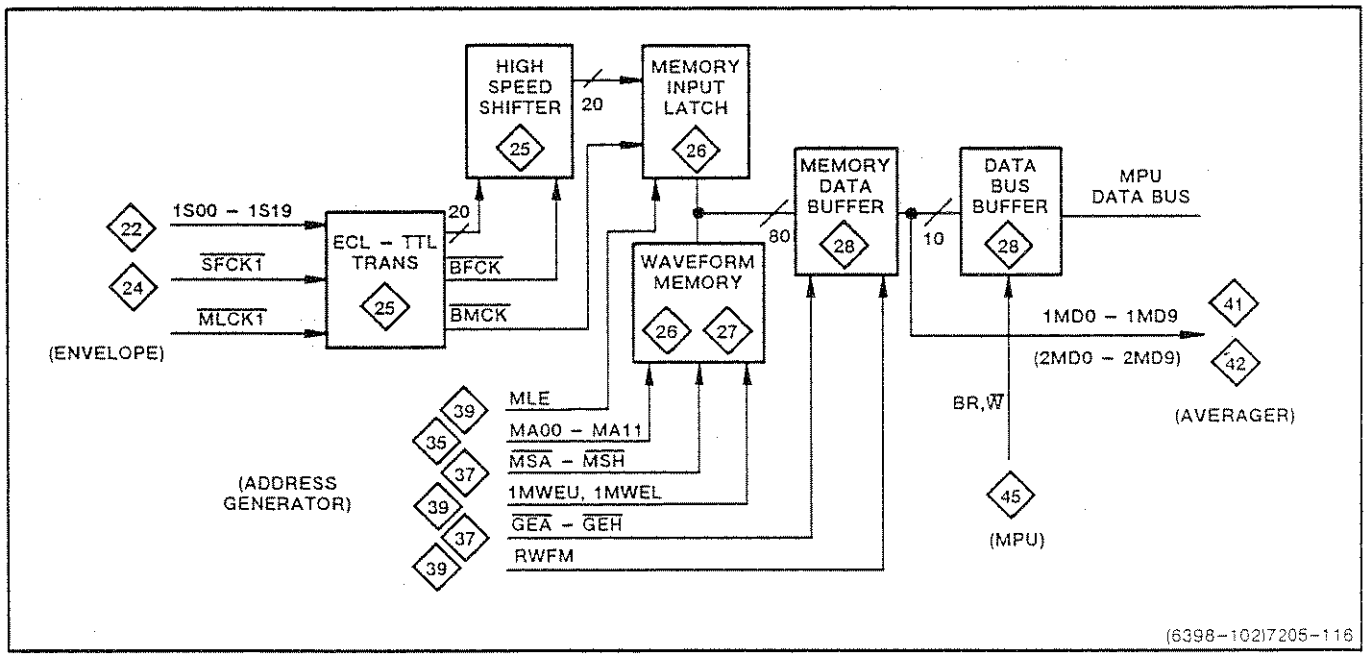


Fig. 1-47 Memory Block Diagram

tion is being performed, all chip select signals (MSA-MSH) become low to enable writing of data to all RAMs simultaneously. However, when the MPU accesses the memory, only the chip select signal for the required memory becomes low to prevent contention.

Each memory RAM has a 16K word X 4-bit capacity. They are used in 8 groups of three to provide the required 10-bit storage. Channel 1 and 2 memories each have a 128K word X 10-bit capacity. When the DUAL channel vertical mode is selected, the Channel 1 input waveform data is stored in Channel 1 memory, and the Channel 2 input waveform data is stored in Channel 2 memory.

When the CH1 Only vertical mode is selected, Channel 1 and 2 memories are combined to provide a 256K word X 10-bit storage capacity. When the sampling mode is set to high speed, odd numbered data is stored in Channel 1 memory and even numbered data is stored in Channel 2 memory. Each memory can be divided into 1, 2, 4, 8, 16, 32, 64 or 128K word record lengths for waveform data storage. All control functions for these operations are performed by the address generator.

MEMORY MPU INTERFACE (DIAGRAM 28)

The memory MPU interface provides all communications between the memory circuitry and the MPU. It consists of the memory data buffer and data bus buffer.

Memory Data Buffer

The 16 memory data buffer transceivers (U400-U430) transfer data between memory, the data bus buffers, and the averager. These 8-bit bus transceivers comprise eight groups of two buffers each to transfer 10-bit data. Each group of data buffers corresponds to one RAM set, which is opened and closed with a $\overline{\text{GEA}}$-$\overline{\text{GEH}}$ (gate enable A through H) signal from the address generator. The transfer direction is determined by the RWFM (read/write for memory) signal.

Data Bus Buffer

The data bus buffer (U440, U442, and U444) connects the memory circuit bus to the MPU data bus. Buffer U444 sets the unused upper six bits low during an MPU read operation.

TIME BASE

The time base (Figure 1-48) generates the sampling clock for the A/D converters, provides the count for the breakpoint function to change the sampling clock frequency, issues the control signals for sorting data in the waveform memories, and generates the ARM and TRIG signals. It consists of an address decoder, 10 kHz oscillator, internal arming delay divider, arm control, trigger control, breakpoint location counter, comparator, breakpoint location RAM, address counter clock generator, breakpoint location RAM address counter, sampling interval RAM, rate latch, decade divider and prescale divider, 200 MHz oscillator, clock source selector, phase calibration generator, envelope clock generator, half-divider and clock buffer, sampling clock generator, breakpoint clock generator, high-speed clock generator, and sampling clock out selector.

ARM AND TRIGGER (DIAGRAM 29)

The arm and trigger circuitry (Figure 1-49) consists of an address decoder to generate the pulses required for time base setting; an arm start flip-flop; a 10-kHz oscillator; an internal arming delay divider; an arm mode selector; trigger control circuitry to establish trigger conditions; a one-shot pulse generator for the auto and manual triggers; and the trigger signal generator to produce the trigger signal.

Address Decoder

The address decoder (U100, U102, U244A, U130A, U246B, U136A, U136B, U136C, and U136D) decodes MPU address signals (BA1-BA4) when control signals $\overline{\text{TBCS}}$ and $\overline{\text{BAS}}$ are low and generates the pulses for reading and writing the data and status signals required for setting the time base. An $\overline{\text{ARMSTRT}}$ pulse initiates acquisition, and a $\overline{\text{MANTRIG}}$ signal produces a trigger when the manual trigger key is pressed.

Arm-Start Flip Flop

When the MPU sends the $\overline{\text{ARMSTRT}}$ pulse to set the arm start flip flop U124, the acquisition sequence is started. The output of U124A resets divider U120,

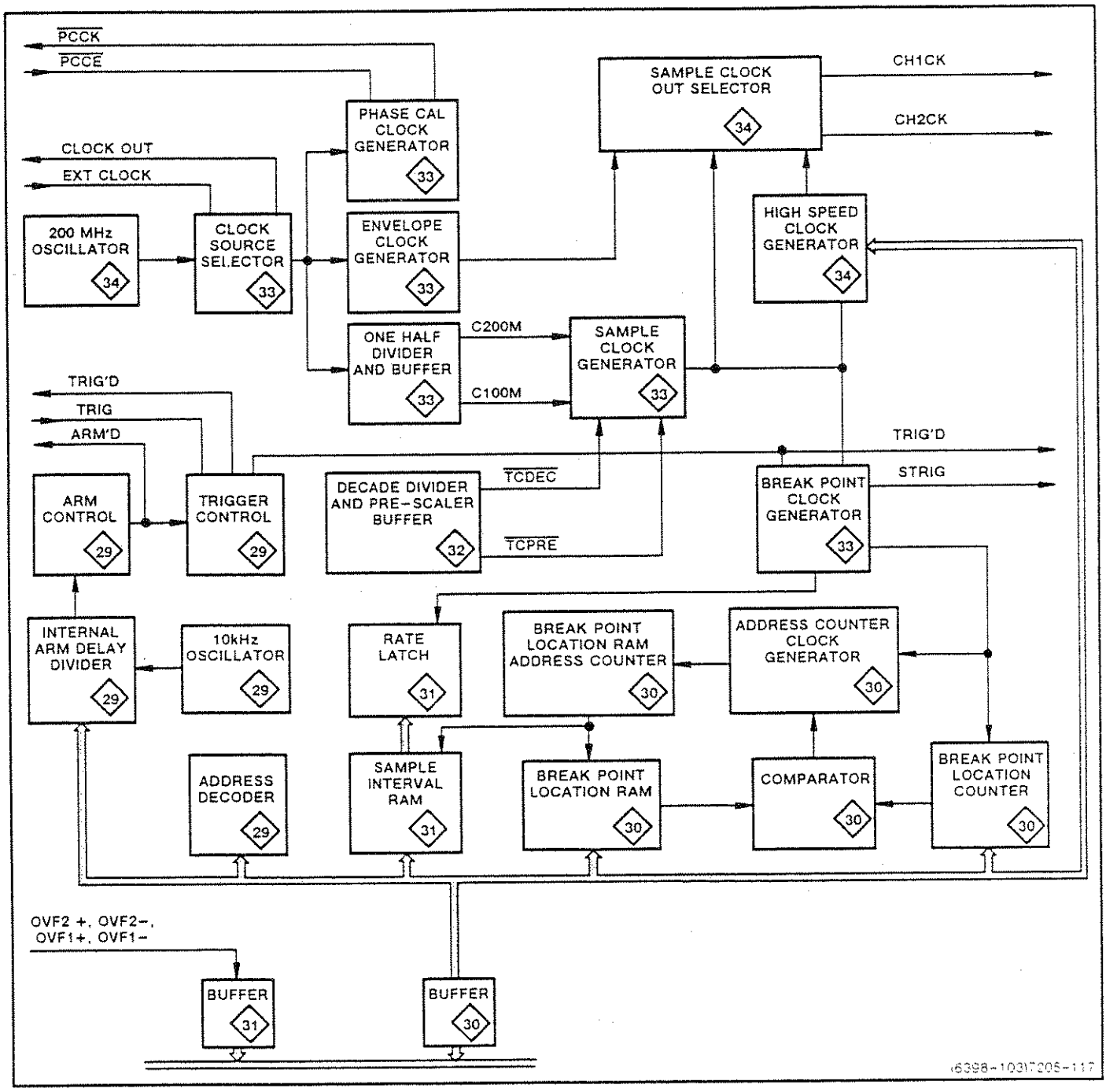


Fig. 1-48 Time Base Block Diagram

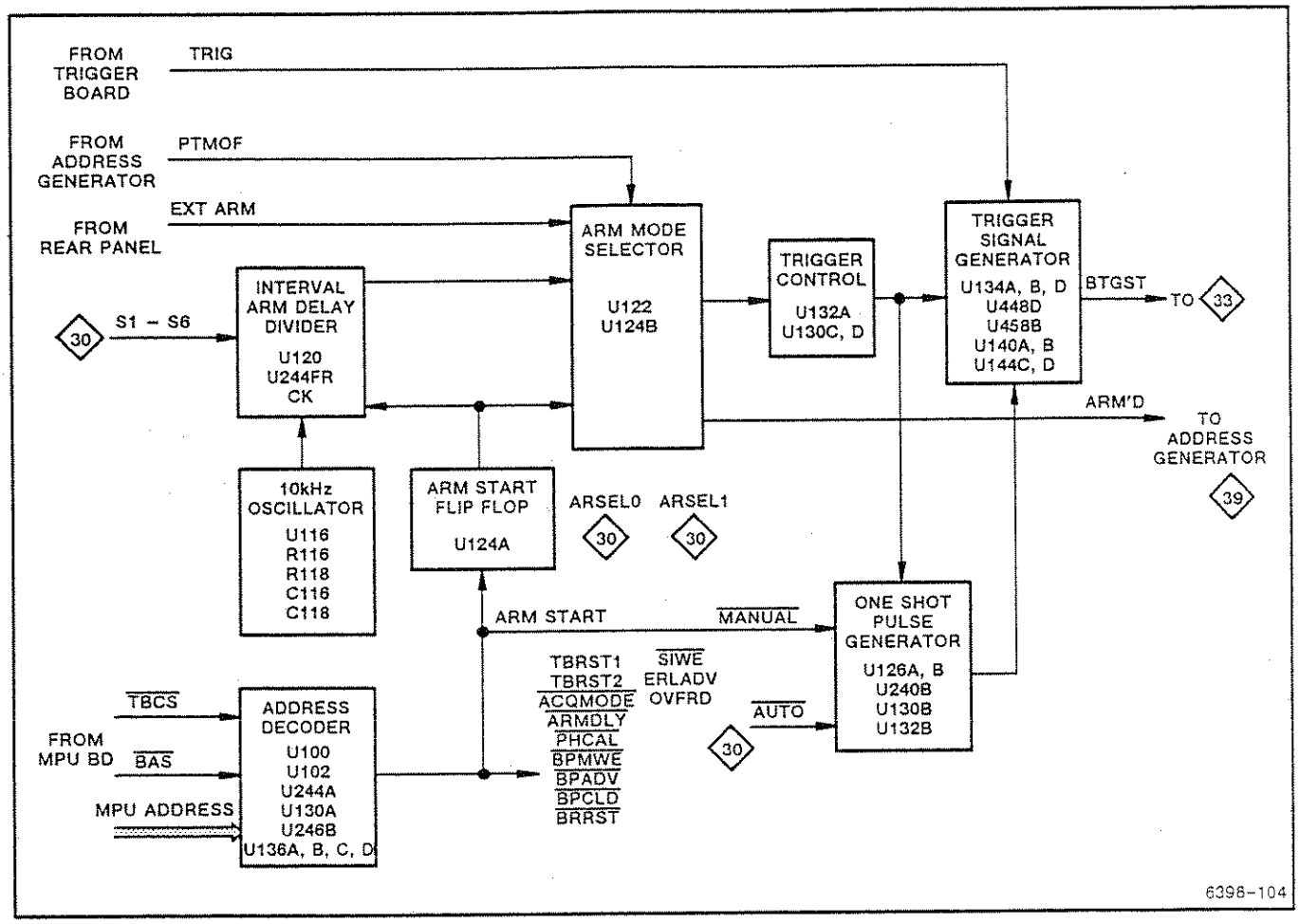


Fig. 1-49 Arm and Trigger Block Diagram

which is used in the internal arming delay mode, and is applied to the arm mode selector circuit.

10 kHz Oscillator

The 10 kHz oscillator (U116, R116, R118, C116, and C118) produces the clock signal that is divided to form the arming delay signal. Its output is supplied to the internal arm delay divider.

Internal Arm Delay Divider

The internal arm delay divider (U120 and U244F) sets the internal arming delay time by dividing the 10 kHz clock in 1-2-5 steps between 10 ms and 10 s. The division ratio is determined by data written to the arm delay divider latch (U108) by the MPU (see schematic 30). The divided signals are applied to the arm mode selector.

Arm Mode Selector

The arm mode selector (U122 and U124B) selects one of three arming modes: external arming delay, internal arming delay, and zero arming delay. The external arming delay signal from the rear panel is applied through connector J332 to the input of U122, which selects the external arm delay signal in the external arming mode, the output of divider U120 in the internal arming mode, or the $\overline{\text{ARMSTRT}}$ signal in the zero arming mode. The selection depends upon the ARSEL0 and ARSEL1 outputs from the arming delay divider latch (U108) (refer to schematic 30). The selected signal is applied to the U124B clock terminal setting its output high to complete the arming operation.

Trigger Control

Trigger control gates U130C, U130D, and U132A initiate the trigger generation process.

When arming operations are completed and the PTHOF (pre-trigger hold off end) signal from the address generator becomes high, the output of U130D becomes high, enabling the one-shot pulse generator and trigger signal generator, and illuminating the ARM'D indicator on the front panel. The PTHOF signal becomes high when acquisition begins if plus trigger delay is set. When minus trigger delay is set, PTHOF becomes high after one record of waveform data is acquired.

One-Shot Pulse Generator

The one-shot pulse generator (U126A, U126B, U130B, U132B, and U240B) enables the pulse generator in either automatic or manual mode.

In auto trigger mode, output signal $\overline{\text{AUTO}}$ from the mode control latch U110 (refer to schematic 30) becomes low. Then when the trigger is enabled, U126B generates an approximate 20 ms pulse and the output of U240B becomes high. If the trigger signals TRIG and $\overline{\text{TRIG}}$ do not arrive from trigger board A22 within 20 ms after the trigger is enabled, a high output from U240B drives the trigger signal generator.

The $\overline{\text{MAN TRIG}}$ signal that is asserted from address decorder U100 when the MAN TRIG key on the front panel is pressed and the trigger signal $\overline{\text{TR}}$ from the GPIB/Monitor board A56 are applied through gate U130B to drive one-shot multivibrator U126A, which drives in the same way as the U126B trigger signal generator.

Trigger Signal Generator

The trigger signal generator (U134A, U134B, U134D, U140A, U140B, U144C, U144D, U448D, and U458B) generates a trigger signal in response to the TRIG and $\overline{\text{TRIG}}$ signals.

After the trigger enable condition has occurred, the output from the one-shot pulse generator is applied through gate U134A to D flip flop U458B. Its output is applied simultaneously through gate U144D to illuminate the TRIG'D indicator and through U144C to the TRIG'D OUT connector on the rear panel.

The trigger signal BTGST initiates the sample clock operation.

BREAKPOINT LOCATOR (DIAGRAM 30)

The breakpoint locator (Figure 1-50) stores the breakpoint location set from the front panel and detects those breakpoint locations during acquisition. It consists of an MPU interface buffer, a breakpoint location RAM and RAM address counter, an address counter clock generator, a breakpoint location counter, a comparator, a mode control latch, and an arm delay divider latch.

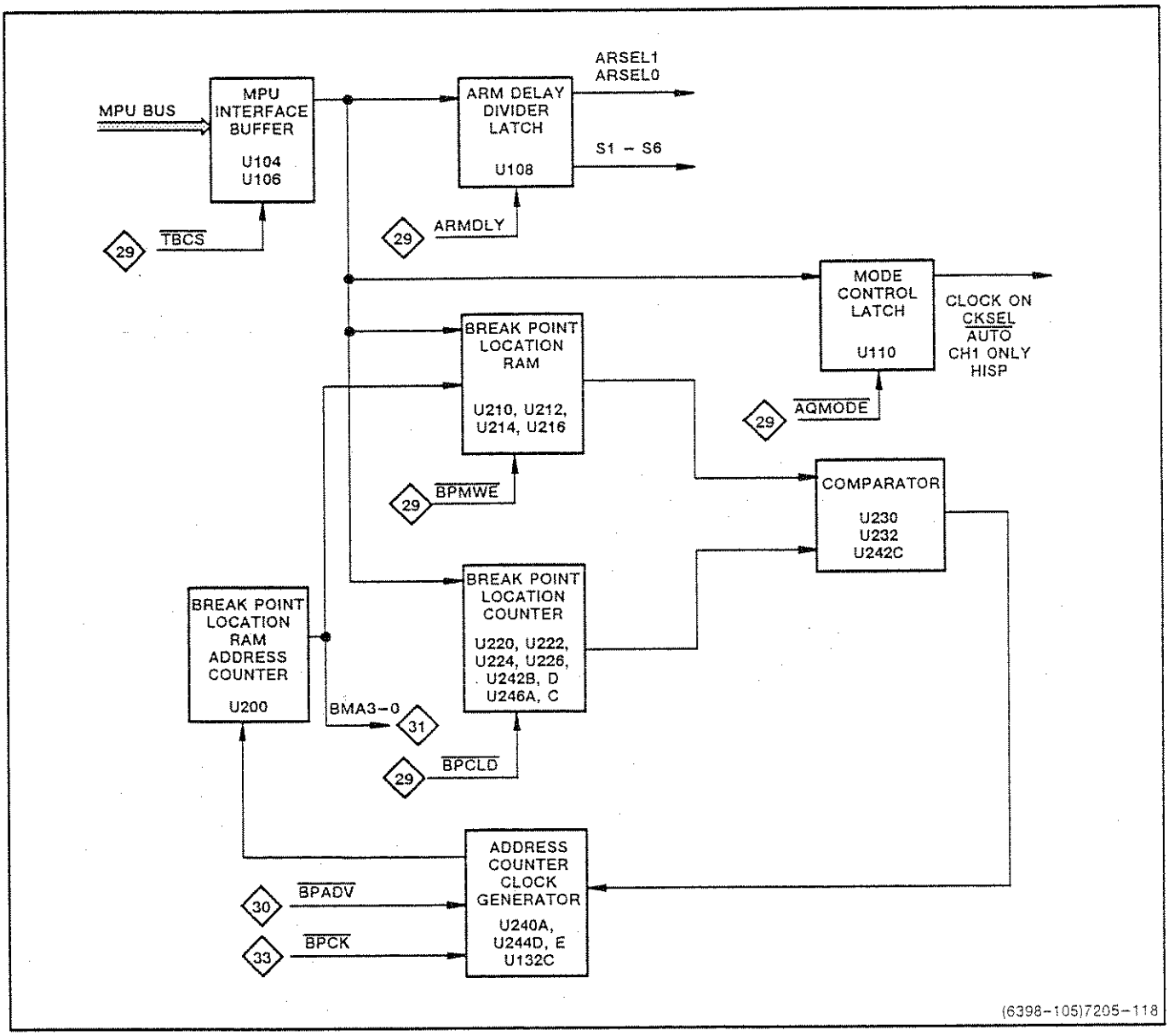


Fig. 1-50 Breakpoint Locator Block Diagram

The breakpoint location is stored in the breakpoint location RAM. After a trigger is generated, the breakpoint location counter is incremented at each 1/8 sampling interval and compared to the contents of the breakpoint RAM.

When the breakpoint location is reached, the comparator generates an agreement signal. This causes the address counter clock generator to generate a pulse, the breakpoint location RAM address counter to increment, and the RAM address to update. The new breakpoint location is read from the breakpoint location RAM and the new sample interval is output from the sampling interval RAM. When this breakpoint operation is complete, the breakpoint location counter outputs a carry.

MPU Interface Buffer

The MPU interface buffer provides the communications path between the MPU and the breakpoint circuitry. It consists of bidirectional, 3-state buffers U104 and U106. Control signals BR/W and $\overline{\text{TBCS}}$ from the MPU control the data and status signals for setting the time base breakpoint operations.

Breakpoint Location RAM

The breakpoint location RAM (U210, U212, U214, and U216) stores the breakpoint settings from the front panel in response to the address decoder output signal $\overline{\text{BPMWE}}$. The breakpoint location RAM address is established by the breakpoint location RAM address counter.

Breakpoint Location RAM Address Counter

Breakpoint location RAM address counter U200 is cleared by address decoder output signal $\overline{\text{BPRST}}$ and the address is updated on the output pulse from the address counter clock generator.

Address Counter Clock Generator

Address counter clock generator U132C, U240A, U244D, and U244E generates the clock signal for address counter U200. When the MPU generates a counter clock pulse decoder U102 outputs the $\overline{\text{BPADV}}$ signal.

Breakpoint Location Counter

Breakpoint location counter U220, U222, U224, and U226 and gates U242B, U242D, U246A, and U246C provide the breakpoint address for comparison with the RAM address set. Gate U246C selects a count mode or load mode for the counters and is operated by mode control latch U110 output signal $\overline{\text{LDEN}}$. The MPU sets $\overline{\text{LDEN}}$ low and the decoder outputs $\overline{\text{BPCLD}}$ when the MPU has data for the counter. The breakpoint location counter starts upcounting continuously at 1/8 the sampling interval clock rate ($\overline{\text{BPCK}}$) once data acquisition begins and a trigger is generated. It stops counting when the counter carry signal ERE (output of gate U134C) is generated.

Comparator

Comparator U230, U232, and U242C compares the output of the breakpoint location RAM with the breakpoint location counter. If the contents agree, U242C output signal COMP becomes high, and the address counter clock generator outputs a pulse. The COMP signal is applied to the MPU readback buffer U112 (refer to schematic 31) for use in diagnostic functions such as breakpoint location RAM tests and breakpoint location counter tests.

Mode Control Latch

Mode control latch U110 stores status data to establish the time base mode. Each bit can be independently set by the MPU.

Arm Delay Driver Latch

Arm delay divider data latch U108 stores the control data used by the MPU to establish the arm delay time and the arm mode prior to acquisition. Table 1-7 lists the programming codes.

Table 1-7
ARM MODE AND ARM DELAY CODES

Signal Name			Data Bus D7 (ARSEL1)	D6 (ARSEL0)	D5 (SS6)	D4 (SS5)	D3 (SS4)	D2 (SS3)	D1 (SS2)	D0 (SS1)
Arm Mode		ZERO	0	0	x	x	x	x	x	x
		10 ms	0	1	0	0	0	0	1	0
		20 ms	0	1	0	1	0	0	1	0
		50 ms	0	1	1	0	1	0	1	0
	Internal Arm	100 ms	0	1	0	0	0	0	1	1
		200 ms	0	1	0	1	0	0	1	1
		500 ms	0	1	1	0	1	0	1	1
		1 s	0	1	0	0	0	1	0	0
		2 s	0	1	0	1	0	1	0	0
		5 s	0	1	1	0	1	1	0	0
		10 s	0	1	0	0	0	1	0	1
	External Arm		1	0	x		x	x	x	x

Note: x denotes don't care.

INTERVAL DATA RAM (DIAGRAM 31)

The interval data ram (Figure 1-51) consists of a sampling interval RAM, a TTL-ECL translator, a gate, a rate latch, an A/D overflow data buffer, and a control signal level translator.

Sampling Interval RAM, TTL-ECL Translator, and Gates

The sampling interval RAM (U300 and U302) stores the interval codes for each breakpoint. Table 1-8 lists the sampling intervals and their corresponding codes.

Table 1-8
SAMPLE INTERVAL WORD

Internal Sample Interval	Data Bus D7	D6	D5	D4	D3	D2	D1	D0	Hex	External Divide Ratio: High-Speed Sample Mode	External Divide Ratio: Normal Mode
5 ns	1	1	1	1	0	1	1	1	F7	1E0	
10 ns	1	1	1	1	1	1	1	1	FF	2E0	1E0
20 ns	1	1	1	0	1	1	1	1	EF	4E0	2E0
30 ns	1	1	0	1	1	1	1	1	DF	6E0	3E0
40 ns	1	1	0	0	1	1	1	1	CF	8E0	4E0
50 ns	1	0	1	1	1	1	1	1	BF	1E1	5E0
60 ns	1	0	1	0	1	1	1	1	AF	---	---
70 ns	1	0	0	1	1	1	1	1	9F	---	---
80 ns	1	0	0	0	1	1	1	1	8F	---	---
90 ns	0	1	1	1	1	1	1	1	7F	---	---
100 ns	0	1	1	0	1	1	1	1	6F	2E1	1E1
200 ns	1	1	1	0	1	1	1	0	EE	4E1	2E1
300 ns	1	1	0	1	1	1	1	0	DE	6E1	3E1
400 ns	1	1	0	0	1	1	1	0	CE	8E1	4E1
500 ns	1	0	1	1	1	1	1	0	BE	1E2	5E1
600 ns	1	0	1	0	1	1	1	0	AE	---	---
700 ns	1	0	0	1	1	1	1	0	9E	---	---
800 ns	1	0	0	0	1	1	1	0	8E	---	---
900 ns	0	1	1	1	1	1	1	0	7E	---	---
1 µs	0	1	1	0	1	1	1	0	6E	2E2	1E2
2 µs	1	1	1	0	1	1	0	1	ED	4E2	2E2
3 µs	1	1	0	1	1	1	0	1	DD	6E2	3E2
4 µs	1	1	0	0	1	1	0	1	CD	8E2	4E2
5 µs	1	0	1	1	1	1	0	1	BD	1E3	5E2
6 µs	1	0	1	0	1	1	0	1	AD	---	---
7 µs	1	0	0	1	1	1	0	1	9D	---	---
8 µs	1	0	0	0	1	1	0	1	8D	---	---
9 µs	0	1	1	1	1	1	0	1	7D	---	---
10 µs	0	1	1	0	1	1	0	1	6D	2E3	1E3

Table 1-8 (Cont.)
SAMPLE INTERVAL WORD

Internal Sample Interval	Data Bus D7	D6	D5	D4	D3	D2	D1	D0	Hex	External Divide Ratio	
										High-Speed Sample Mode	Normal Mode
20 µs	1	1	1	0	1	1	0	0	EC	4E3	2E3
30 µs	1	1	0	1	1	1	0	0	BC	6E3	3E3
40 µs	1	1	0	0	1	1	0	0	CC	8E3	4E3
50 µs	1	0	1	1	1	1	0	0	BC	1E4	5E3
60 µs	1	0	1	0	1	1	0	0	AC	---	---
70 µs	1	0	0	1	1	1	0	0	9C	---	---
80 µs	1	0	0	0	1	1	0	0	8C	---	---
90 µs	0	1	1	1	1	1	0	0	7C	---	---
100 µs	0	1	1	0	1	1	0	0	6C	2E4	1E4
200 µs	1	1	1	0	1	0	1	1	EB	4E4	2E4
300 µs	1	1	0	1	1	0	1	1	DB	6E4	3E4
400 µs	1	1	0	0	1	0	1	1	CB	8E4	4E4
500 µs	1	0	1	1	1	0	1	1	BB	1E5	5E4
600 µs	1	0	1	0	1	0	1	1	AB	---	---
700 µs	1	0	0	1	1	0	1	1	9B	---	---
800 µs	1	0	0	0	1	0	1	1	8B	---	---
900 µs	0	1	1	1	1	0	1	1	7B	---	---
1 ms	0	1	1	0	1	0	1	1	6B	2E5	1E5
2 ms	1	1	1	0	1	0	1	0	EA	4E5	2E5
3 ms	1	1	0	1	1	0	1	0	DA	6E5	3E5
4 ms	1	1	0	0	1	0	1	0	CA	8E5	4E5
5 ms	1	0	1	1	1	0	1	0	BA	1E6	5E5
6 ms	1	0	1	0	1	0	1	0	AA	---	---
7 ms	1	0	0	1	1	0	1	0	9A	---	---
8 ms	1	0	0	0	1	0	1	0	8A	---	---
9 ms	0	1	1	1	1	0	1	0	7A	---	---
10 ms	0	1	1	0	1	0	1	0	6A	2E6	1E6
20 ms	1	1	1	0	1	0	0	1	E9	4E6	2E6
30 ms	1	1	0	1	1	0	0	1	D9	6E6	3E6
40 ms	1	1	0	0	1	0	0	1	C9	8E6	4E6
50 ms	1	0	1	1	1	0	0	1	B9	1E7	5E6
60 ms	1	0	1	0	1	0	0	1	A9	---	---
70 ms	1	0	0	1	1	0	0	1	99	---	---
80 ms	1	0	0	0	1	0	0	1	89	---	---
90 ms	0	1	1	1	1	0	0	1	79	---	---
100 ms	0	1	1	0	1	0	0	1	69	2E7	1E7
200 ms	1	1	1	0	1	0	0	0	E8	4E7	2E7

Note: --- means not defined.

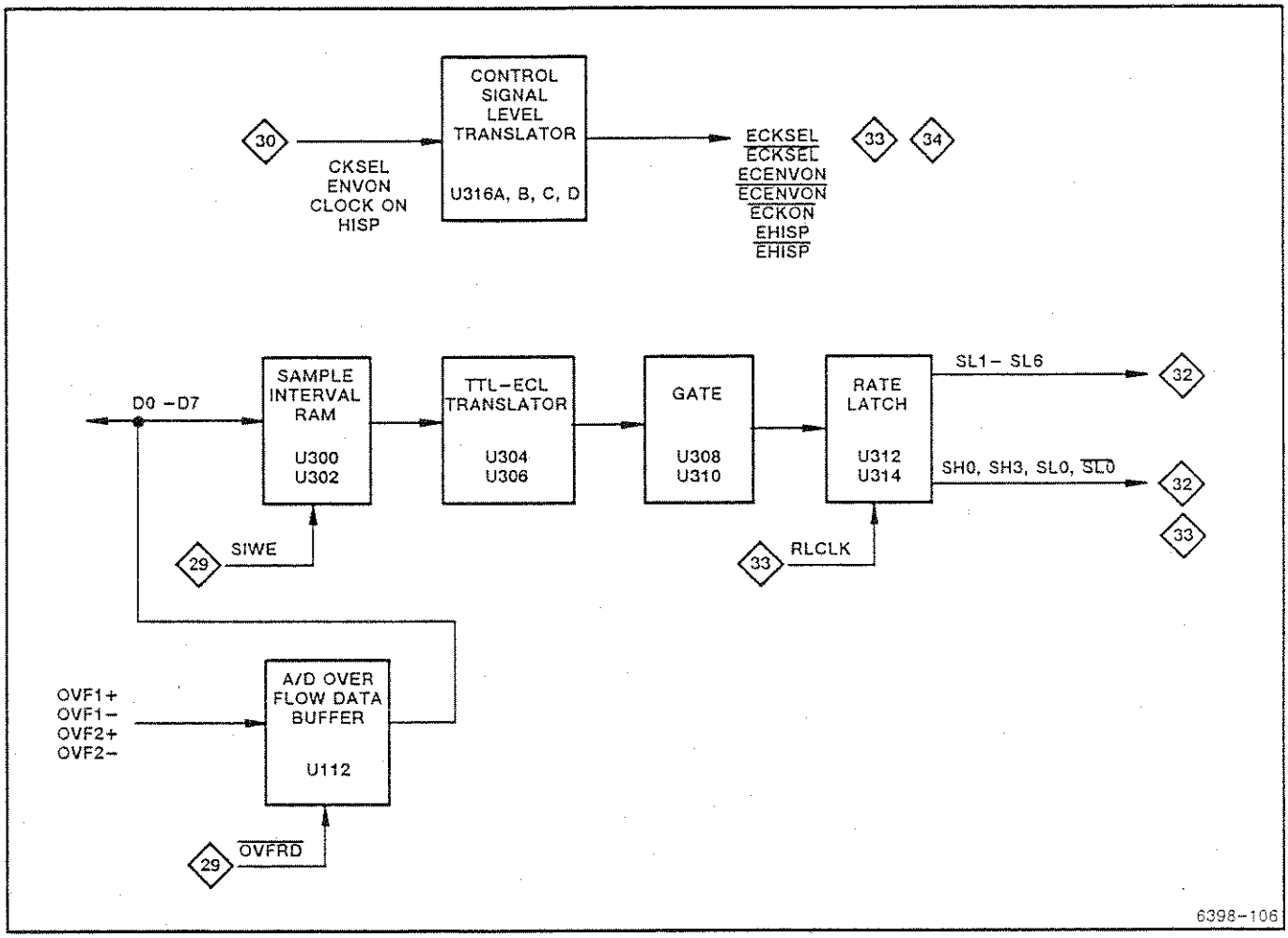


Fig. 1-51 Interval Data RAM Block Diagram

The MPU performs code-writing operations before acquisition starts.

The MPU address decoder (U102) (refer to schematic 29) output signal ($\overline{SIWE}$) writes MPU data into the RAM. The RAM address is established by the breakpoint location RAM address counter outputs (BMA0-BMA3) (refer to schematic 30). Codes set in the sampling interval RAM are transformed from TTL to ECL levels by U304, and U306, applied through gates U308 and U310, and loaded into the rate latch on the sampling clock generator rate latch clock pulse signal (RLCLK).

Rate Latch

Rate latch U312 and U314 temporarily store the codes to be applied to the prescaler divider and decade divider (refer to schematic 32).

A/D Overflow Data Buffer

A/D overflow data buffer U112 stores overflow bits 1 and 2 from the A/D converter. It is read when the MPU outputs the $\overline{\text{OVFRD}}$ signal.

Control Signal Level Translator

Control signal level translator U316 transforms the TTL signal set in the mode control latch to an ECL level.

PROGRAMMABLE COUNTER (DIAGRAM 32)

The programmable counter (Figure 1-52) consists of a prescaler divider and decade divider. The carry signals from these dividers are applied to the sampling clock generator (refer to schematic 33).

Pre-Scaler Divider

The prescaler divider is a presettable programmable counter (U320) that divides the 100 MHz clock signal (C100M1) by a value from 1 to 10. The division ratio is established by rate latch output data SH0, SH1, SH2, and SH3. Counting continues until the carry signal ($\overline{\text{TCPRE}}$) becomes low, which loads rate latch output data SH0 to SH3, and the upcount begins again. Figure 1-53 shows a divide-by-4 operation when SH0, SH1, SH2, and SH3 are 1100. The counter carry signal ($\overline{\text{TCPRE}}$) is connected to the normal mode sampling clock generator gate U434B (refer to schematic 33).

Decade Divider

The decade divider is a counter that divides the 100 MHz clock in a ratio from 10-1 to 10-7. It consists of presettable programmable counters U322, U324, U326, U328, U330, U332, U334, and their associated gates.

Each counter is cascade-connected and divides the output signal from the prescaler ($\overline{\text{TCPRE}}$) by a value between 10-1 and 10-7. When the prescaler carry signal ($\overline{\text{TCPRE}}$) becomes low, the C100M2 clock signal is applied through gate U340B in parallel to the clock pins of all counters. Rate latch output data SL1 to SL6, and SL0 are connected to the input pins of the counters allowing them to load either 0110 or 1111.

When 0110 is loaded, and 9-clock ticks occur, it reaches its terminal count causing the count signal to become low enabling the next counter. Input data is loaded at the tenth clock tick, and the counter

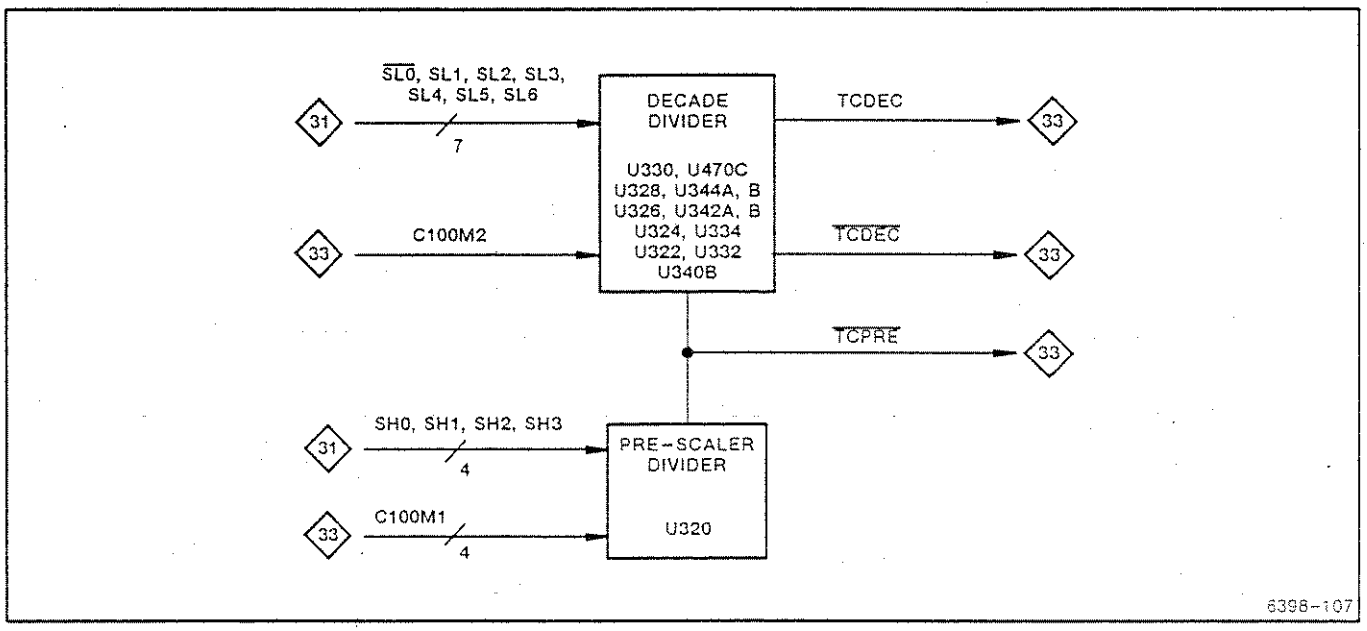


Fig. 1-52 Programmable Counter Block Diagram

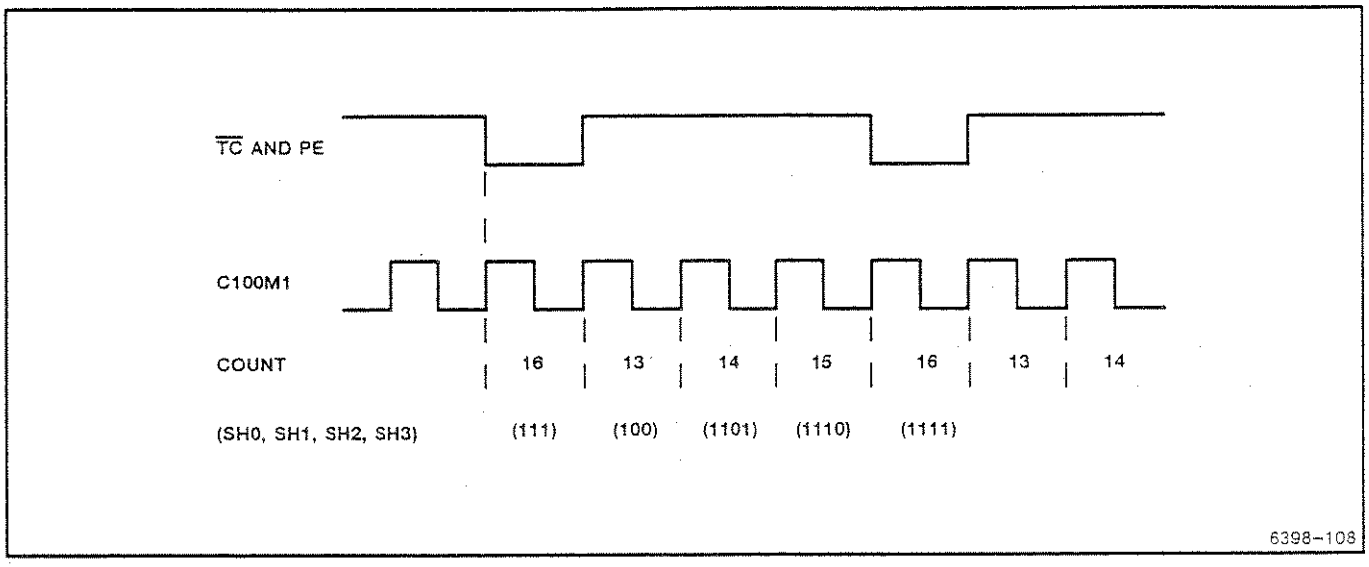


Fig. 1-53 Timing Diagram for Prescaler Divide-by-Four Operation

begins upcounting. Thus, the counter divides $\overline{\text{TCPRE}}$ into tenths.

If 1111 is loaded into a counter, the terminal count signal becomes low at that point, enabling the next counter.

Table 1-9 shows the sampling interval RAM output SD0 to SD3 and the 7-bit rate latch output code input to the decade divider. The terminal count signals of each of the decade counters are applied to gates U344A, U344B, and U342B, and the wired-OR of the outputs of these gates are applied through gate U470 to the sample clock generator.

Table 1-9
DECADE COUNTER PROGRAMMING CODES

Input Binary Value			Seven-Bit Output Code							Division Ratio
2	1	0	U322	U324	U326	U328	U330	U332	U334	
0	0	0	0	0	0	0	0	0	0	7
0	0	1	1	0	0	0	0	0	0	6
0	1	0	1	1	0	0	0	0	0	5
0	1	1	1	1	1	0	0	0	0	4
1	0	0	1	1	1	1	0	0	0	3
1	0	1	1	1	1	1	1	0	0	2
1	1	0	1	1	1	1	1	1	0	1
1	1	1	1	1	1	1	1	1	1	0

SAMPLE CLOCK GENERATOR (DIAGRAM 33a & 33b)

The sample clock generator (Figure 1-54) consists of a clock buffer, a phase cal signal generator, an envelope clock generator, a 1/2 divider and buffer, a high-speed mode sampling clock generator, a normal-mode sampling clock generator, a breakpoint clock generator, a rate latch clock generator, a fast clock switcher, and a sync circuit.

Clock Buffer

Clock buffer multi-output gates U400A and U400B, and regular gates U402A, U402B, U402C, and U402D are controlled by the ECKSEL signal to select either

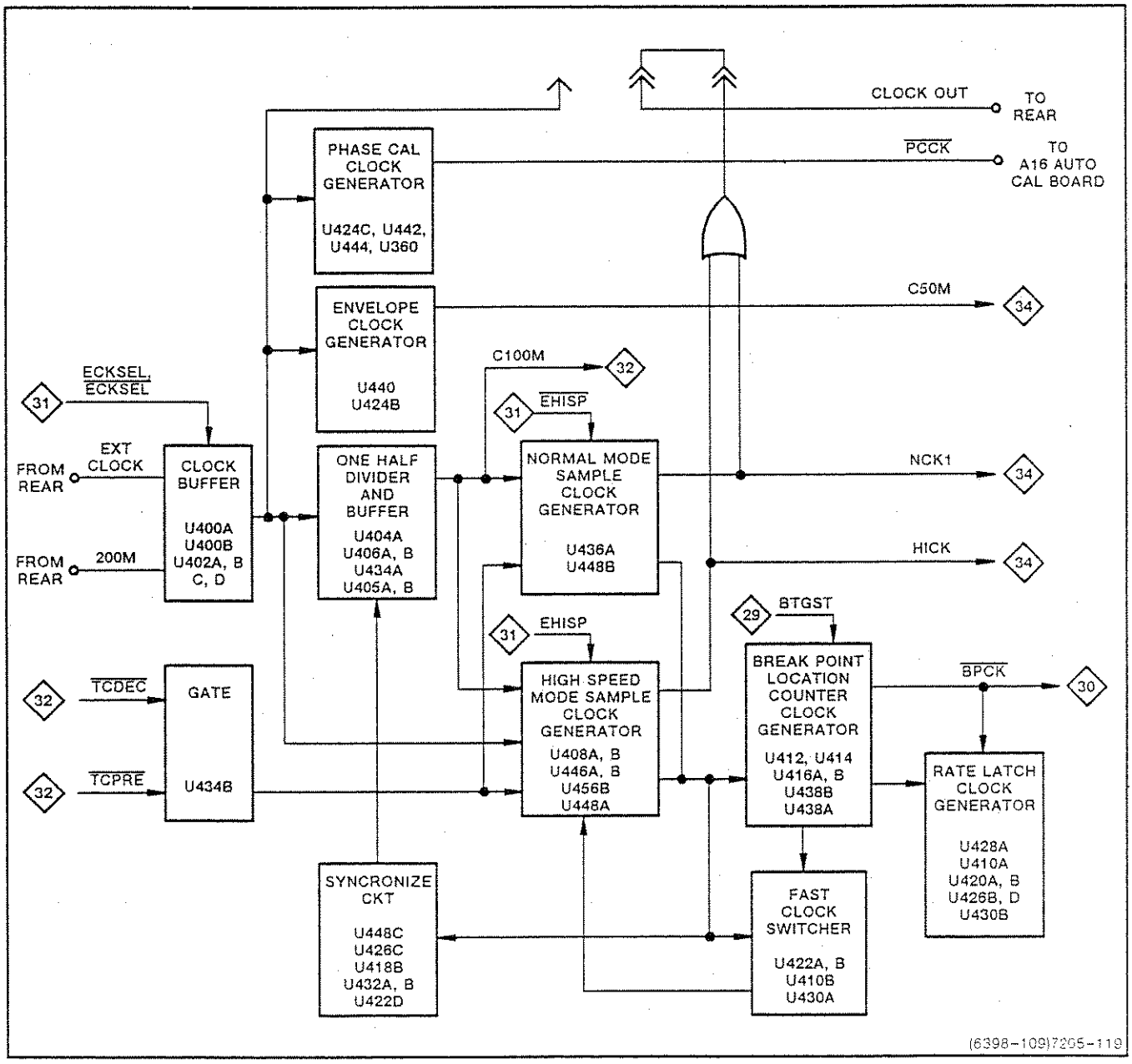


Fig. 1-54 Sample Clock Generator Block Diagram

the internal 200 MHz or external clock signal. Gates U400A and U400B, which are used simultaneously as buffers and selectors, are wired-ORed and applied as the source clock for the phase calibration signal generator and the envelope clock generator circuits and through gates U402A as the rear panel CLOCK OUT signal, and through gates U402B, U402C, and U402D as the source clock for the clock generator.

Phase Calibration Clock Generator

The phase calibration clock generator consists of shift registers U442 and U444, and gates U136D and U424C.

During phase calibration, the $\overline{\text{PCCE}}$ signal from the A14 Auto Cal Board becomes low, and operation of shift registers U442 and U444 is controlled by the 200 MHz clock. The load mode is entered when a low from U444 pin 15 and the data pin high level is loaded, then the shift mode is entered once again. This causes a 10 ns wide, 70 ns long $\overline{\text{PCCK}}$ cycle pulse to be applied to the A14 Auto Cal Board.

Envelope Clock Generator

Envelope clock generator U424B and U440 are not used at this time.

1/2 Divider and Buffer

The 1/2 divider and buffer (U404A, U405A, U434A, U406A, and U406B) passes or divides the selected clock in half and applies it to various circuits through buffers.

When external clock is used while in normal sample mode, gate U405A disables the 1/2 divider and external clock through gate U402B passes gate U405B. In all other cases 1/2 divider U404A divides in half selected clock into C100M1 prescaler clock, which is then buffered by U434A to become the C100M2 clock signal. Gate U406A adjusts to the output timing of U406B to drive the high-speed mode sampling clock generator. When in the internal clock mode the 2.5 ns C100M1 signal created by the gate U406B which ANDs output of U404A and the 200 MHz clock through gate U402C is sent to the high-speed mode sampling clock generator.

Gate

The prescaler and decade divider carry signals ($\overline{\text{TCPRE}}$ and $\overline{\text{TCDEC}}$) are combined in AND gate U434B to produce a clock cycle of $\overline{\text{TCDEC}}$ with a width of $\overline{\text{TCPRE}}$. This signal is applied to the high-speed mode sampling clock generator and to the normal-mode sampling clock generator.

High Speed Mode Sample Clock Generator

The high-speed mode sampling clock generator (U448A, U408A, U408B, U446A, U446B, and U456B) produces the high-speed sampling clock. During high-speed sampling, signals $\overline{\text{EHISP}}$ and $\overline{\text{ECKON}}$ become low when acquisition starts causing gate U448A output to become low. This applies the clock signals from gates U406A and U406B to U408A and U408B. High-speed switcher U430A outputs Q and $\overline{\text{Q}}$ are supplied to the inputs of gates U408A and U408B, respectively, whose outputs are wired-ORed. The gate outputs are divided in half by flip-flop U456B to produce the 50% duty-cycle pulse $\overline{\text{HICK}}$, which is applied to the gate with complementary output circuit U472B (refer to schematic 34).

Normal Mode Sample Clock Generator

The normal mode sampling clock generator (U436A and U448B) produces the normal mode sampling clock. During normal mode, the output of U448B becomes low, enabling U436A. U436A sets the width of the clock generated by gate U434B to 5 ns, which is then applied to the normal mode sampling clock delay circuit gate U472A (refer to schematic 34).

Breakpoint Location Counter Clock Generator

The breakpoint location counter clock generator consists of U412, U414, U416A, U416B, U438A, and U438B. 4-bit shift registers U412 and U414 enter the load mode on acquisition when their S1 and S2 pins become low. Their output pins become low when the clock pulse is applied. When acquisition starts and arming is complete, the $\overline{\text{EARM}}$ signal becomes low. At the next clock pulse, pin S1 becomes high, and U412 and U414 begin shifting left.

The BTGST signal is low before a trigger occurs, thus all shift register outputs are low. When the trigger occurs, BTGST becomes high, and at the first clock, U412 Q0 (pin 14) becomes high, which is sequentially shifted to U414. At the fifth clock pulse, U414 Q1 (pin 15) becomes high, and at the sixth clock pulse, U416A $\overline{Q}$ becomes low causing pin S1 of the shift register to become low, putting the shift register into the load mode. At the seventh clock pulse, U412 and U414 input data D0 to D3 are loaded.

After loading is completed pin S1 becomes high on the next clock pulse, and U412 and U414 begin shifting left again. Thus, U412 Q0 provides a 1/8 sampling clock cycle pulse. This output passes through U438A and U144 and becomes the $\overline{BPCK}$ breakpoint counter clock signal.

Rate Latch Clock Generator

The rate latch clock generator consists of U428A, U410A, U420A, U420B, U426B, U426D, and U430B. In the normal sampling mode, the breakpoint location can be set as high as eight times the sampling interval from the trigger position (or as high as 16 times the sampling interval in the high-speed mode), and one rate latch clock is issued for every eight sampling interval clocks. The rate latch clock signal (RLCLK) is generated in different circuits depending on the sampling interval.

For the following discussion assume a sample interval of 200 ns or longer. The breakpoint location counter clock register shift register U412 Q0 is synced, input, and latched in U428A by TCDEC and output as RLCLK. Since U420A SL0 is high and U426B $\overline{SL0}$ is low they are disabled. Figure 1-55 shows the timing relationship of the U412 Q0, TCDEC, NCK2, and RLCLK signals. When RLCLK becomes high, a new sampling interval rate is input to the rate latch changing the sampling interval.

When a 100 ns or faster sampling rate is selected, only the prescaler divider carry signal $\overline{TCRRE}$ is used for the sampling interval clock, thus disabling U428A. At this point, the SL0 signal becomes low, gate U420A is enabled, and RLCLK is generated at the timing required to set shift registers U412 and U414 to load mode (Figure 1-56).

In high-speed mode with a sampling interval of 5 ns, the $\overline{200M}$ signal becomes low causing the U430B data pin to become high. U430B generates RLCLK with the same timing as shown in Figure 1-56, but clock HCK3, which is used for high-speed acquisition, clocks U430B causing the propagation delay to become even shorter than the interval at which U410A and U420A generate RLCLK.

Fast Clock Switcher

Fast clock switcher U422A, U422B, U410B, and U430A operates during high-speed mode to switch gates U408A and U408B to generate sampling interval clocks of 5 ns and less than 10 ns. During 5 ns sampling, the $\overline{200M}$ signal from the sampling interval RAM is low. The U410B Q output becomes low at the same time as the RLCLK clock, and on the next high-speed clock, the U430A Q output becomes low. When the U430A Q output becomes low, a 5 ns sampling interval is generated by U408A.

Synchronize Circuit

The synchronize circuit (U448C, U426C, U418D, U432A, U432B, and U422D) generates the 1/2 divided 100 MHz clock output C100M1 (U404A) in synchronization with the 5 ns clock when the sampling interval changes from 5 ns to 10 ns.

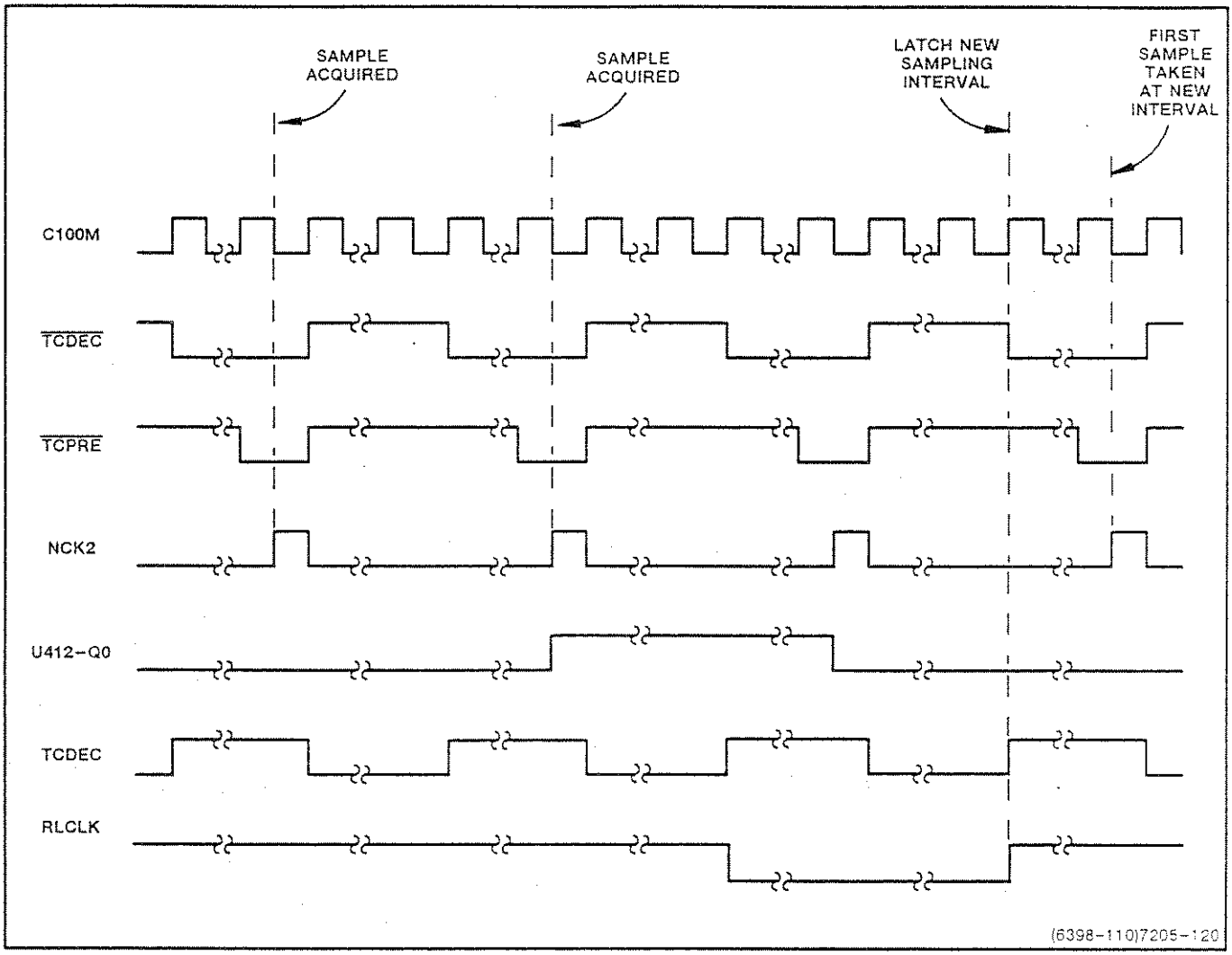


Fig. 1-55 Timing of RLCLK Pulse at Slower Clock Sampling Rates

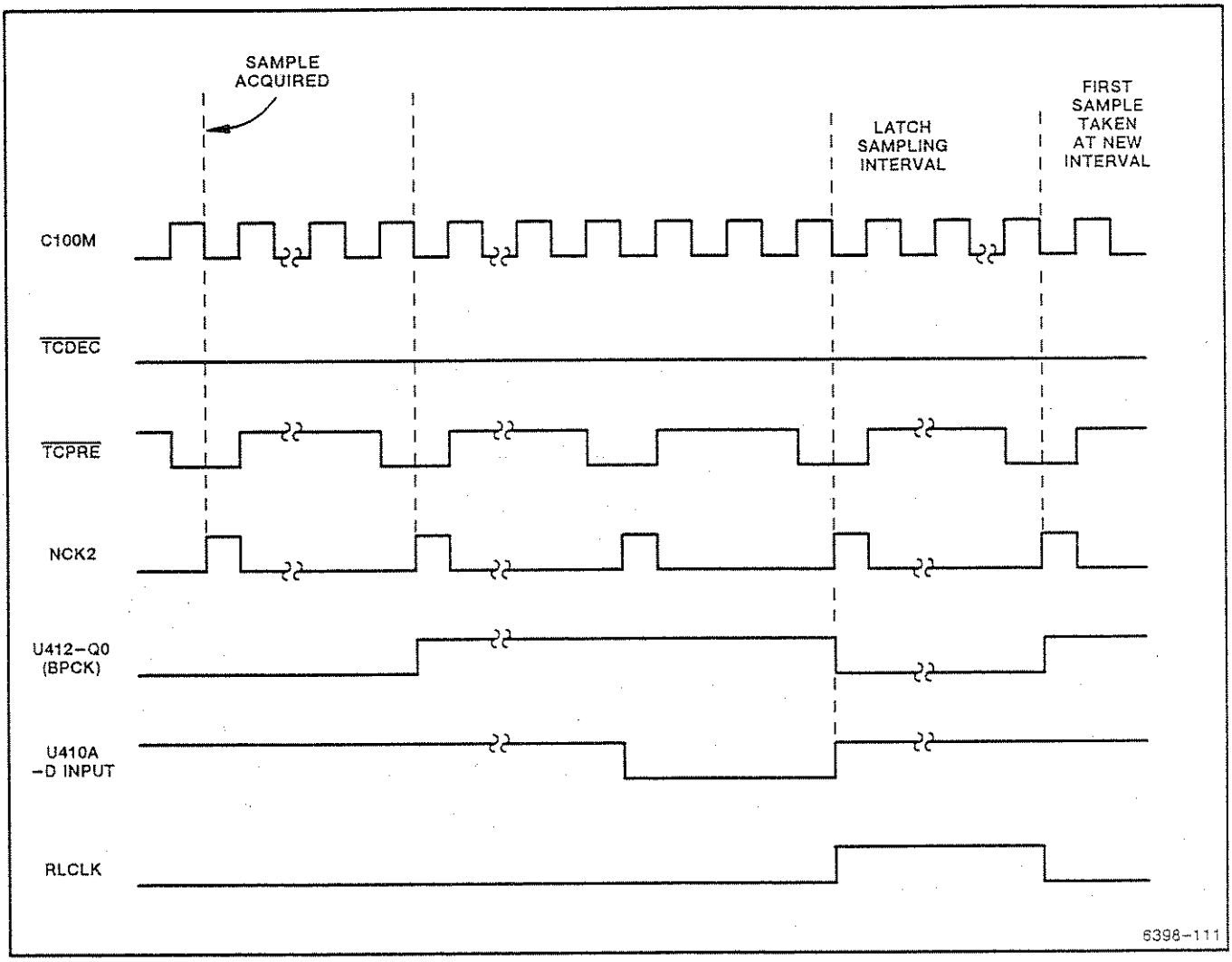


Fig. 1-56 Timing of RLCLK Pulse at 100 ns or Faster Sampling Rates

SAMPLE CLOCK OUTPUT AND 200 MHZ OSC (DIAGRAM 34)

The sample clock output selects the high-speed or normal sampling interval from the sample clock generator (Figure 1-57).

The sample clock output consists of a normal mode sampling clock delay, a gate with complementary output, a variable delay, a Channel 1 clock delay adjust, a selector, and an envelope clock gate. The 200 MHz oscillator is the source for the internal clock.

Normal Mode Sample Clock Delay

In normal mode, the NCK1 signal is used as the clock source. In high-speed mode, clock signal NCK1 is applied through gates U472A, U472C, and U452C for timing adjustment and applied to the input of selector U454.

Gate With Complementary Output

The gate with complementary output U472B establishes the 180 degree timing difference between Channel 1 and 2 in the high-speed mode. The 50%

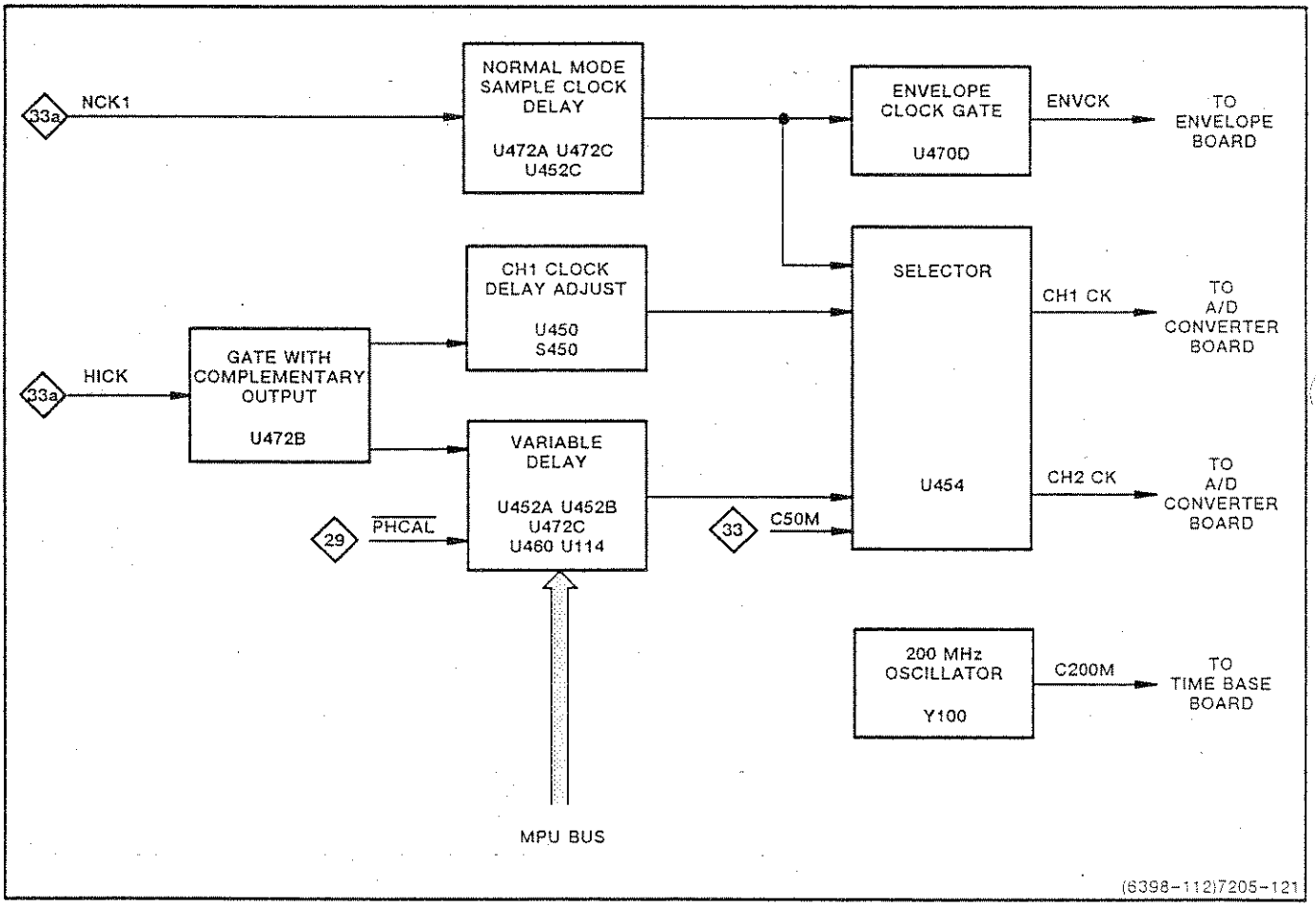


Fig. 1-57 Sample Clock Output and 200 MHz Oscillator

duty cycle signal from the high-speed mode sampling clock generator flip-flop U456B ($\overline{HICK}$) (refer to schematic 33a) is used as the high-speed mode sampling clock source. During high-speed mode, the Channel 1 A/D and Channel 2 A/D perform interleaved sampling, thus $\overline{HICK}$ is applied to complimentary gate U472B to produce a clock with a phase difference of 180 degrees.

Variable Delay

Variable delay U114, U452A, U452B, and U460 provides for automatic adjustment of the Channel 2 clock delay to provide an exact 180 degree clock difference between Channel 1 and 2 during phase calibration.

Variable delay is extended by C456 and R459 at the falling edge of the differential buffer U452A input clock. Also, the D/A converter output reference voltage (another input to buffer to U452A) is varied to control the falling edge of the input clock delay time. Differential buffers U452A and U452B are coupled to provide a variable delay with a constant duty cycle. This compensation is performed by writing data into latch U114 while phase calibration is being performed. The Channel 2 clock compensation range is approximately 1.5 ns.

CH1 Clock Delay Adjust

The Channel 1 clock delay adjustment (U450 and DIP switch S450) provides for selective adjustment of the Channel 1 clock delay about the center of the Channel 2 clock variation range.

Selector

Selector U454 selects either the normal acquisition clock or the high-speed acquisition clock. Selector output signals CH1CK and CH2CK are applied through connectors J326-1 and J326-2, respectively, to the A/D converters.

Envelope Clock Gate

The envelope clock gate U470D generates the ENVCK signal, which is not used.

200 MHZ OSC

The 200 MHz oscillator (Y100) generates an ECL level clock signal C200M that is applied through connector J762 to the A32 Time Base Board.

ADDRESS GENERATOR

The address generator (Figure 1-58) consists of the memory address, segmentation logic, memory chip select, trigger delay counter, and memory write control. It generates all memory addresses and signals that control memory and addressing.

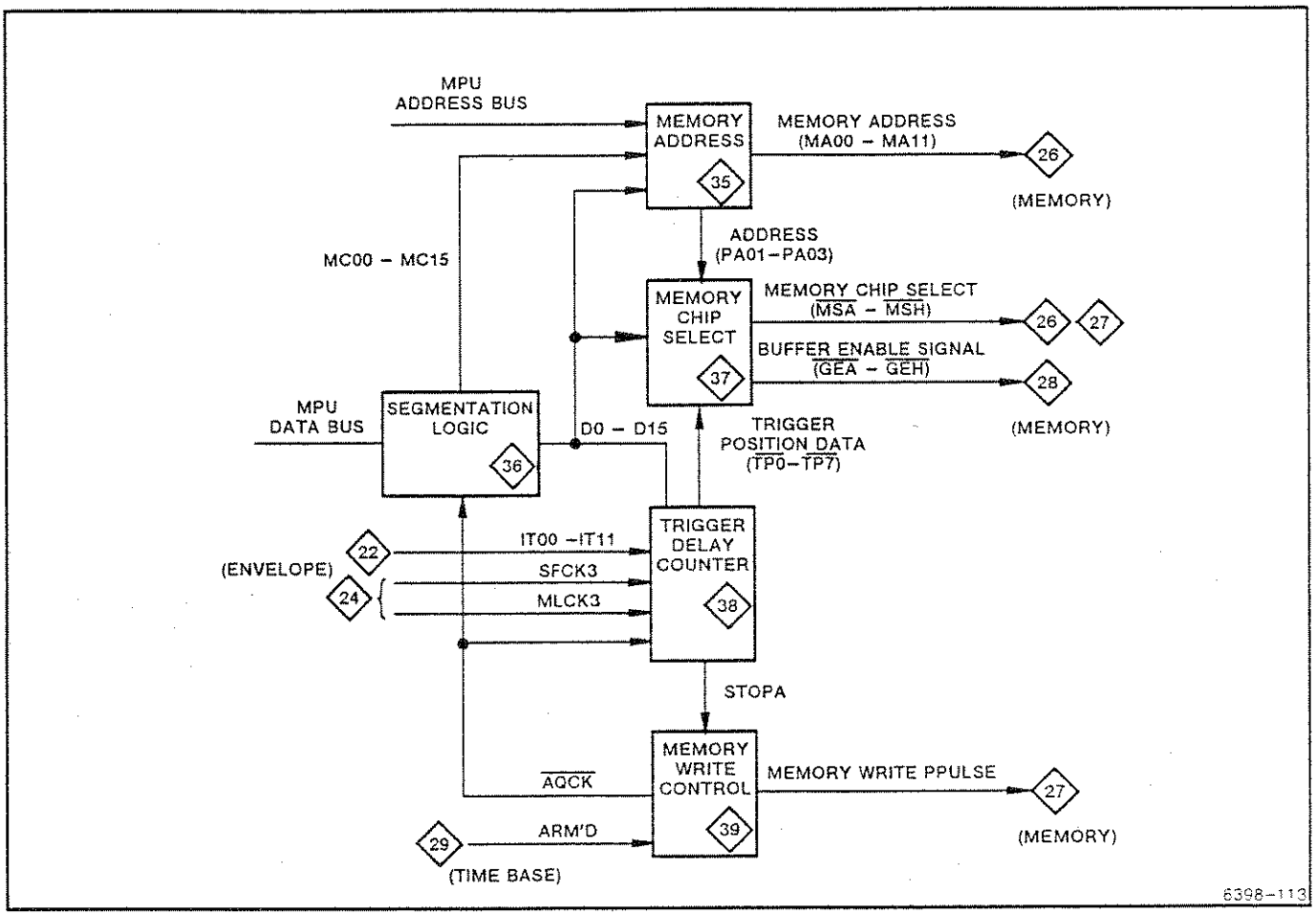


Fig. 1-58 Address Generator Block Diagram

MEMORY ADDRESS (DIAGRAM 35)

The memory address circuit (Figure 1-59) consists of the address shift, address decode, address select, and address generator control circuits.

Address Shift

Address shift uses five selectors (U100, U102, U104, U106, and U108) in all sampling modes to switch memory between the A and B inputs.

At the A input, address bus bits BA1 to BA20 are sequentially connected to the A input, while at the B input, bit BA2 is set to the lowest address, then subsequent bits though BA18 are each shifted down one bit with BA1 residing at the original position BA18.

NOTE

As explained earlier in the description about memory, when high-speed mode is selected, waveform data is stored alternately in the Channel 1 and Channel 2 memories. Thus, if the MPU reads data without reading alternately from the Channel 1 and Channel 2 memories, it cannot read continuous waveform data. The address shift circuit solves this problem with hardware.

With the ALT (alternative) signal set high and the B input selected, BA1 is placed at the original position of BA18, the Channel 1 memory area (800000hex to 83FFFFhex) and the Channel 2 memory area (840000hex to 87FFFFhex) are accessed alternately each time BA1 changes. This enables the MPU to read continuous waveform data by sequentially accessing addresses 800000hex to 87FFFFhex.

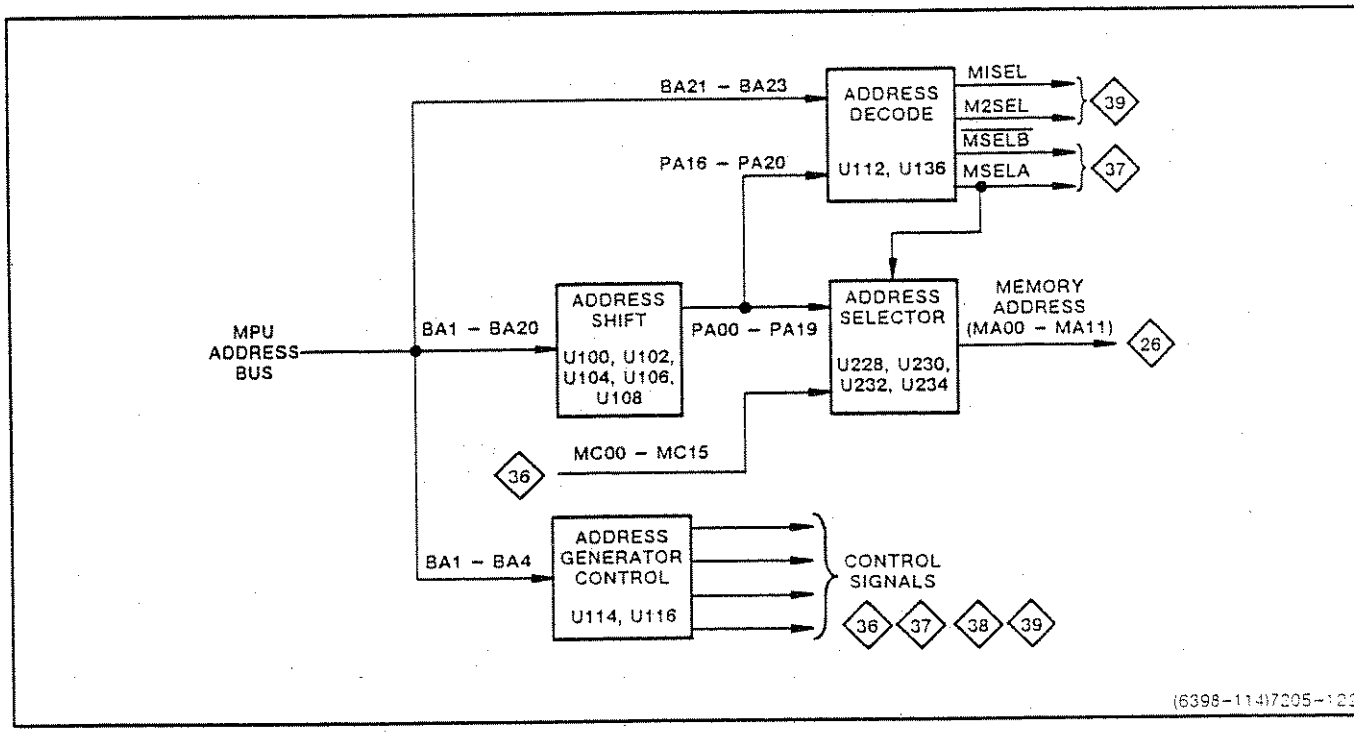


Fig. 1-59 Memory Address Block Diagram

Address Decode

The address decode circuit (U112, U136A, U136B, and U136C) decodes the top address, and U130 buffers the contents of U112 during readback by the MPU. This circuit generates the Channel 1 memory area (800000hex to 83FFFFhex) decode signal (M1SEL), Channel 2 memory area (840000hex to 87FFFFhex) decode signal (M2SEL), and the signals indicating that addresses 800000hex to 87FFFFhex have been decoded (MSELA and $\overline{\text{MSELB}}$)

Address Generator Control

The address generator control circuit generates various control signals by decoding an address. It consists of two 3-to-8 decoders (U114 and U116). The control signals are explained with the circuits that use them.

Address Selector

The address selector (U228, U230, U232, and U234) selects the source of address information based on the mode of operation. During data acquisition and in response to the MSELA signal, it selects the A input to which the outputs MC00 to MC15 from the address counter (described below) are connected. When the MPU is accessing memory, it selects the B input to which PA04 to PA19 are connected.

SEGMENTATION LOGIC (DIAGRAM 36)

The segmentation logic circuitry (Figure 1-60) performs memory segmentation by establishing the start and end address in memory. It consists of a bus buffer, a trigger location read buffer, an end address register, a start address register, an address counter, an address counter control, an address counter read buffer, and a segment full flip-flop.

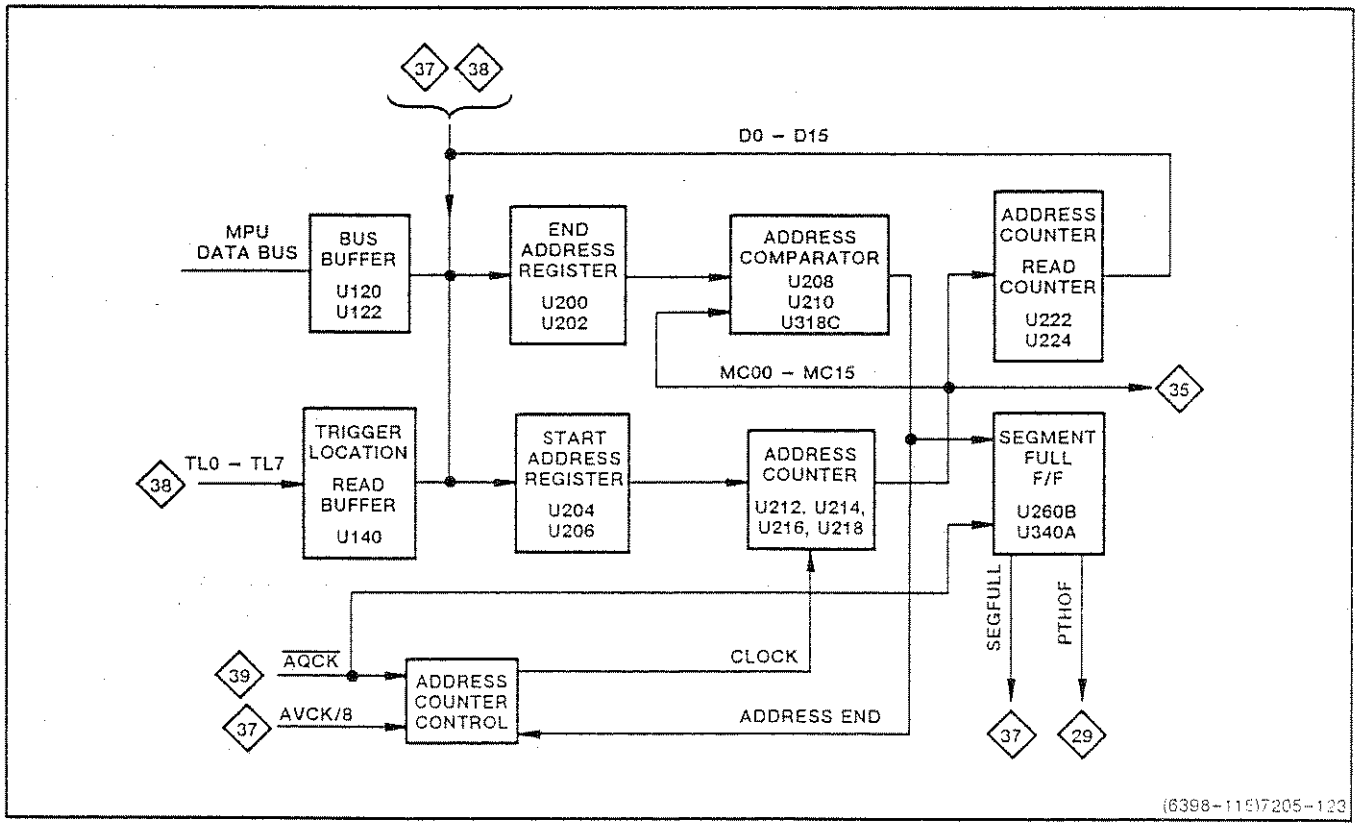


Fig. 1-60 Segmentation Logic Block Diagram

Bus Buffer

Bus buffer U120 and U122 acts as an interface between the MPU data bus and the address generator internal data bus.

Start Address Register

The start address register (U204 and U206) latches the start address as computed by the MPU according to settings made on the front panel.

End Address Register

The end address register (U200 and U202) latches the end address as computed by the MPU according to settings made on the front panel. Its output is sent to the address comparator.

Address Counter

The address counter (U212, U214, U216, and U218) is loaded with a start address before acquisition operations are initiated by the $\overline{\text{MAPE}}$ (Memory Address Parallel Enable) and $\overline{\text{MARL}}$ (Memory Address Load Pulse) signals. It then upcounts in synchronization with the $\overline{\text{AQCK}}$ (acquisition clock) signal during acquisition.

Address Counter Control

The address counter control (U220A, U220B, U220C, U220E, U236A, U236B, U236C, U276A, U322C, and U322D) outputs the address counter clock and control signals required for the address counter in response to input signals $\overline{\text{MAPE}}$, $\overline{\text{MARL}}$, and $\overline{\text{AQCK}}$, STORE/AVE (store or average), and AVCK/8 (average clock/8). It also provides the PE pin control signals.

Address Comparator

The address comparator (U208, U210, and U318C) compares the address counter and end address register during acquisition to determine where acquisition is to stop. The A input is applied to the end address register, while the B input is connected to the address counter output. If the address counter agrees with the end address register, the outputs of both U208 and U210 become low causing the ADDRESS END signal of gate U318C to become high. As a result, the address counter control circuit sets the address counter in the load mode, and the contents of the start address register are loaded into the address counter at the next $\overline{\text{AQCK}}$ pulse.

When the address comparator output becomes high and the ADDRESS END signal becomes low, the address counter enters the count mode an incrementing restarts in sychronizataion with the $\overline{\text{AQCK}}$ signal. The sequence continues until acquisition is determined by a change in front panel settings, a trigger, or some other action. During acquisition, waveform data is written continuously into memory in the area between the specified start and end addresses.

SEGMENT FULL FLIP-FLOP

Segment full flip-flop U260B, U276D, and U340A generates the SEGFUL (segment full) and PTHOF (pre-trigger hold off) signals. When the ADDRESS END signal from the address comparator becomes high, the U260B Q output (SEGFUL) becomes high on the rising edge of $\overline{\text{AQCK}}$. If pre-trigger is selected, the PTHOF signal becomes low, preventing generation of the trigger until data is written once between the specified start and end addresses. When SEGFULL becomes high, U260B $\overline{\text{Q}}$ goes low and PTHOF goes high, cancelling hold off.

Address Counter Read Buffer

Address counter read buffer U222 and U224 is used when the MPU reads back the contents of the address counter.

Trigger Location Read Buffer

Trigger location read buffer U140 is used when trigger data is read back from the MPU.

MEMORY CHIP SELECT (DIAGRAM 37)

The memory chip select circuit (Figure 1-61) decodes memory addresses to generate the memory chip select and buffer enable signals. It consists of an average pointer, an address decoder, a buffer enable, a chip select, a status register, and miscellaneous control circuits.

Average Pointer

The average pointer consists of counter U270, average pointer U272, and four gates U136D, U220D, U264A, and U264B. It generates the buffer enable signal when averaging is being performed. During averaging, signal $\overline{AVON}$ (average on) becomes low to indicate inititation of averaging, U272 is enabled, signal $\overline{AVCK}$ (average clock) is generated, and the counter U270 starts incrementing. The output of U270 is connected to the address input of U272, so U272 output becomes low by turns, which opens one group of memory data buffers at a time, with the result that the contents of the RAM corresponding to the opened group of buffers is applied to the averager. Output signal AVCK/8 from U136D is used as the address counter clock during averaging.

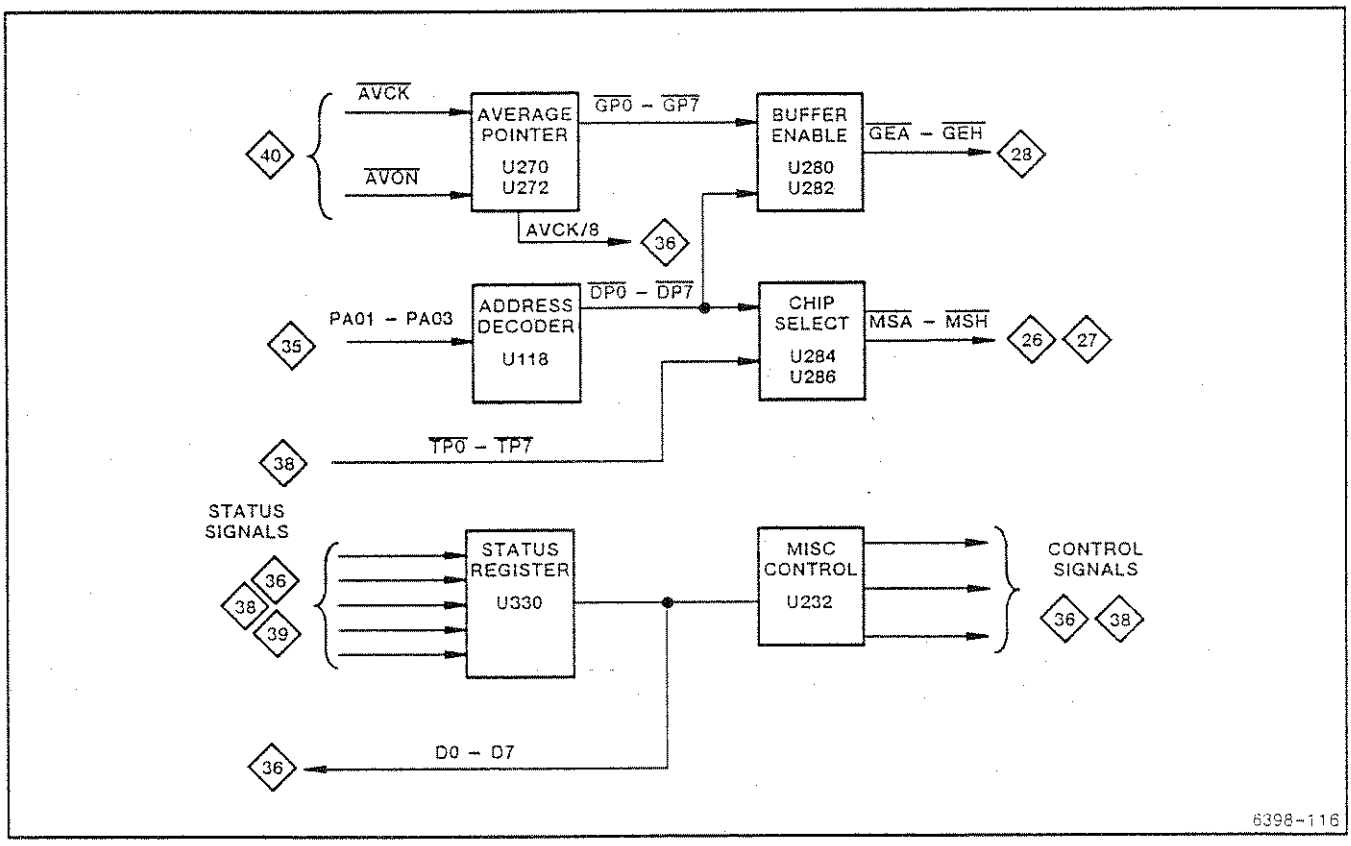


Fig. 1-61 Memory Chip Select Block Diagram

Address Decoder

Address decoder U118 generates the chip select and buffer enable signals when the MPU acesses memory by decoding the lower-order address.

Buffer Enable

Buffer enable U280 and U282 selects the buffer enabling signal when the MPU wants to access memory in the averaging mode. During data acquisition, $\overline{GP0}$-$\overline{GP7}$ are selected as they are in the averaging mode. But the average pointer U272 is disabled causing $\overline{GP0}$-$\overline{GP7}$ to become high closing all memory data buffers.

Chip Select

Chip select U284 and U286 select the memory chip select signal. Signals $\overline{TP0}$ to $\overline{TP7}$ are selected when data acquisition or averaging is being performed, while $\overline{DP0}$ to $\overline{DP7}$ are selected when the MPU is accessing memory. Chip select outputs $\overline{MSA}$ to $\overline{MSH}$ are sent to memory in the same manner as the buffer enable signals $\overline{GEA}$ to $\overline{GEH}$.

Status Register

Status register U330 is used when the MPU reads back the acquisition status signals. The contents of this register are supplied to the MPU when the $\overline{HARD}$ INT1 and $\overline{HARD}$ INT2 signals are generated by gates U334A and U334B in response to the CLKFLAG (clock flag) or ACQ DN (acquisition done) signal.

Miscellaneous Control

Miscellaneous control U332 generates the control signals MSKB1 and MSKB2 used to mask the interrupt signals.

TRIGGER DELAY COUNTER (DIAGRAM 38)

Trigger delay counter (Figure 1-62) generates the trigger delay set from the front panel. It consists of delay counter control, a delay counter, a STOPA flip-flop, a delay read buffer, a trigger data shift, an ECL-TTL translator, a trigger data latch, a trigger circuit control, and an acquisition chip select circuit.

ECL-TTL Translator

ECL-TTL translator U290 transforms the envelope circuit trigger data 1T10 and 1T11 and clocks $\overline{SFCK3}$ and $\overline{MLCK3}$ from an ECL to a TTL level.

Trigger Data Shift

Trigger data shift circuits U238 and U240 shift trigger data TD10 and TD11 four times on the $\overline{BFCK1}$ clock and apply it to the trigger data latch.

Trigger Data Latch

Trigger data latch U250 latches data from the trigger data shift in synchronization with the $\overline{BMCK1}$ clock. Until latched, trigger data from the envelope passes through exactly the same circuit configuration as waveform data. Its timing is also the same. Thus, waveform and trigger data are shifted and latched simultaneously.

Trigger Circuit Control

Trigger circuit control flip-flop U312B and its associated gate stop the U250 clock when the TL7 output from the trigger data latch U250 becomes high (indicating that a trigger has been generated), sets the TRIG ON signal high, and sets the delay counter to the count mode.

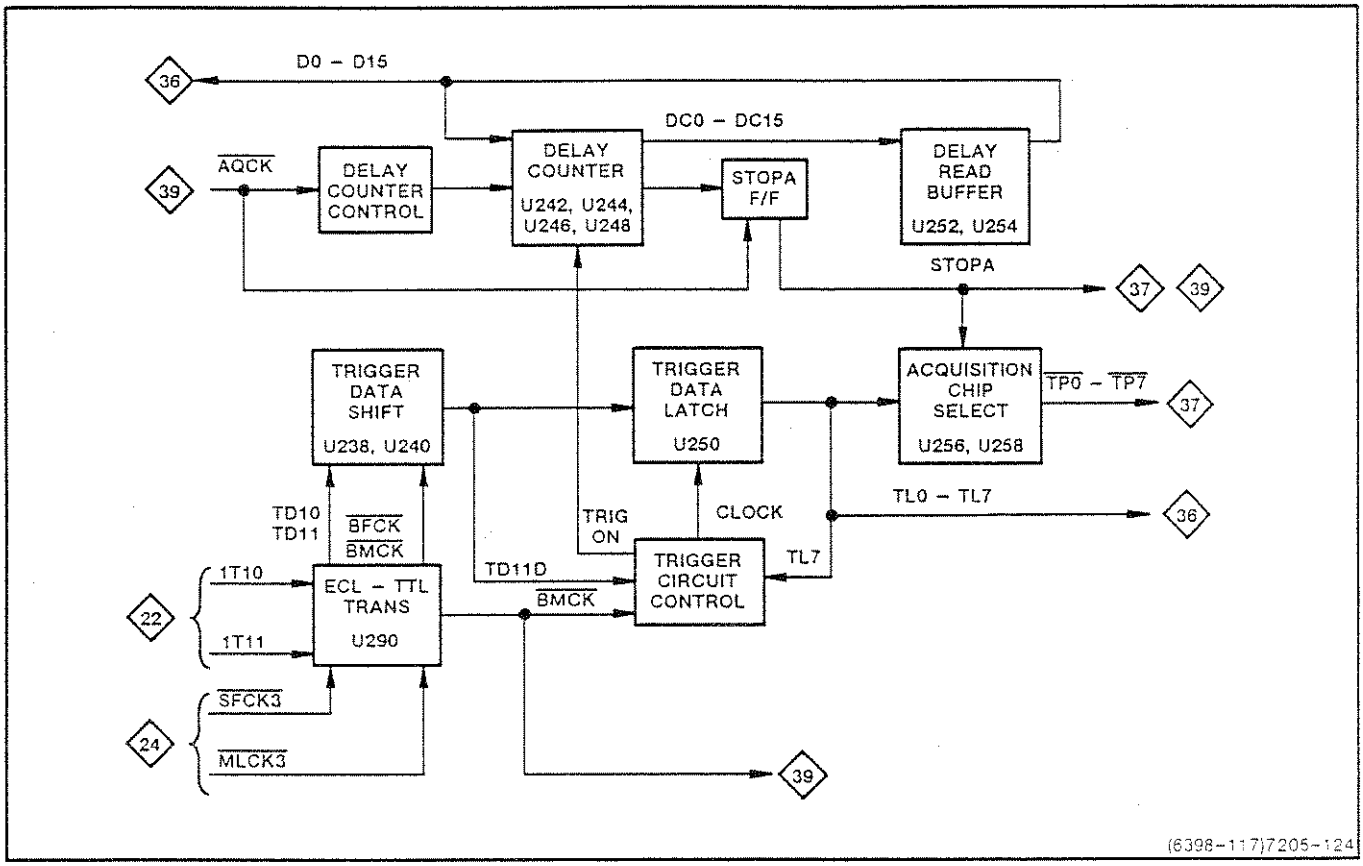


Fig. 1-62 Trigger Delay Counter Block Diagram

Delay Counter Control

Delay counter control U266A, U266B, U266C, U268A, U268B, and U262D supplies the clock pulse to the delay counter and loads the trigger delay. The MPU sets the trigger counter and loads the trigger delay. The MPU sets the trigger delay in response to the $\overline{\text{DLPE}}$ (delay counter parallel enable) and $\overline{\text{DLYL}}$ (delay load) signals before the delay counter enters the count mode.

Delay Counter

The delay counter consists of counters U242, U244, U246, and U248. When the counter is set to the count mode by the TRIG On signal, it increments in synchronization with the $\overline{\text{AQCK}}$ signal. When it reaches FFF, the U242 TC output (pin 15) becomes high, indicating to the STOPA flip-flop that the specified trigger delay time has elapsed.

STOPA Flip-flop

The STOPA flip-flop (U260A) receives the carry output signal from the delay counter, sets its Q output STOPA (stop acquisition) high, and switches the acquisition chip select circuit. It also generates the ACQDN (acquisition done) signal in the acquisition clock circuit (refer to schematic 39.)

Acquisition Chip Select

Acquisition chip select circuits U256, U258, U262C, U276B, and U318D generate the memory chip select signals ($\overline{\text{TP0}}$-$\overline{\text{TP7}}$) when acquisition or averaging are being performed.

During acquisition (except when the last data is being written), STOPA is low. This selects the output of U262C, whose output is low because its $\overline{\text{STORE}}$ input is low. Thus, during acquisition all chip select signals become low. When the last data is written, STOPA becomes high selecting the output of trigger data latch U250.

During averaging, the OE (output enable) pins of U256 and U258 are high when AVON becomes low, thus all outputs are set low.

Delay Read Buffer

Delay read buffer U252 and U254 is used when the MPU reads the contents of the delay counter.

MEMORY WRITE CONTROL (DIAGRAM 39)

Memory write control (Figure 1-63) generates the $\overline{\text{AQCK}}$ (acquisition clock) signal, which is used as the clock for both the address and delay counters. It is also used to produce the memory write pulse. It consists of a bus buffer enable, a memory write pulse, and an acquisition clock.

Acquisition Clock

The acquisition clock circuit produces the $\overline{\text{AQCK}}$, $\overline{\text{ACQDN}}$, and CLKFLAG signals. It consists of flip-flops U310A, U310B, U312A, and U340B; delay lines DL310, DL312, and DL314; and gates U300C, U320A, U320B, and U320C.

The $\overline{\text{AQCK}}$ signal is produced from the $\overline{\text{BMCK1}}$ signal. When the D output (ARM'D) of U340B becomes high, its Q output becomes high on the risk edge of $\overline{\text{BMCK1}}$. This causes the D input of U310A to become high, and its Q output to become high on the rising edge of the next $\overline{\text{BMCK1}}$. This output is then delayed 40 ns by DL310, inverted by U320B, and returned to the reset pin of U310A, generating a pulse width of 40 ns at the $\overline{\text{Q}}$ output of U310A. This pulse is then delayed 10 ns by DL314, creating the resultant $\overline{\text{AQCK}}$ signal (Figure 1-64).

U310B generates and ACQDN (acquisition done) signal when the STOPA flip-flop output described above becomes high. Flip-flop U312A generates a CLKFLAG (clock flag) signal for use in the real-time trace mode.

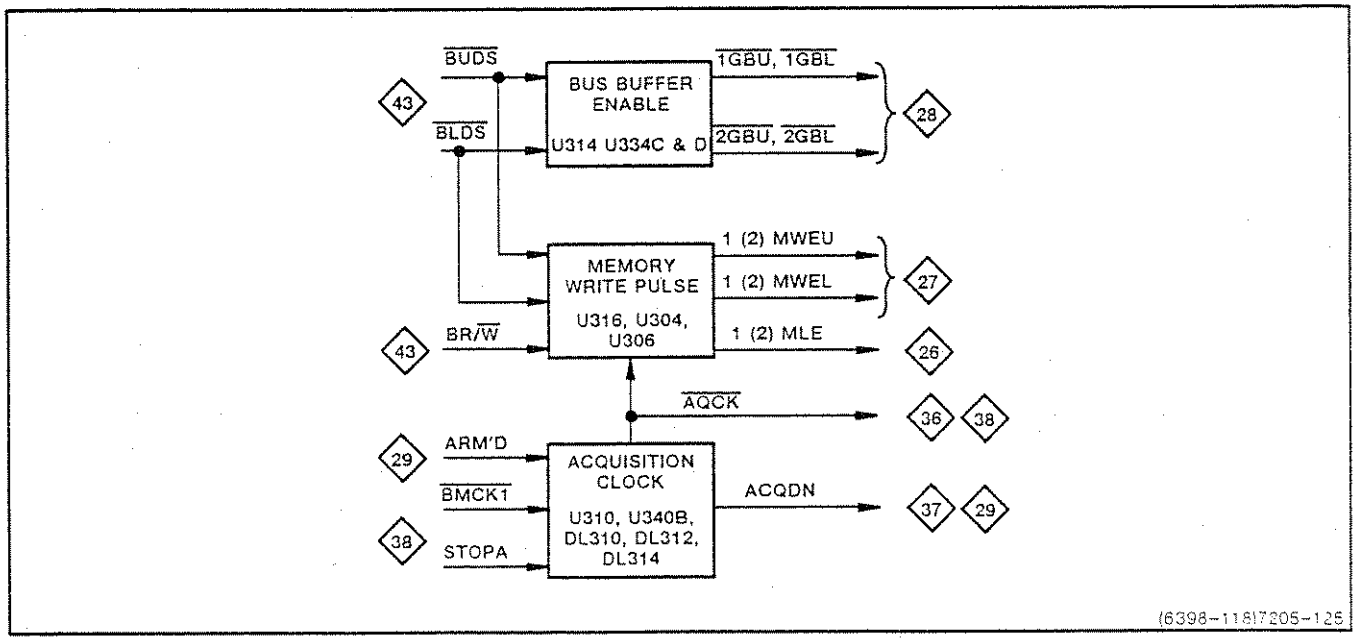


Fig. 1-63 Memory Write Control Block Diagram

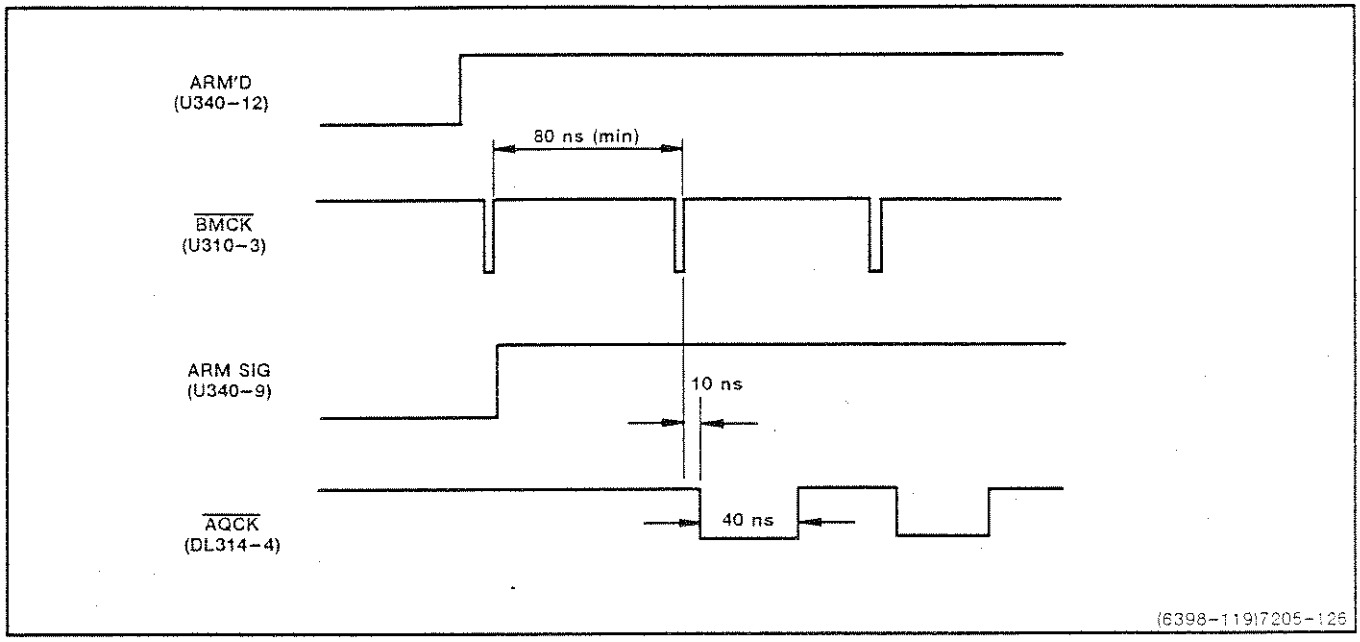


Fig. 1-64 AQCK Timing Chart

Bus Buffer Enable

The bus buffer enable NAND gates (U314A, U314B, U314C, and U314D) and inverters (U334C and U334D) generate the memory data bus buffer enable signal (refer to schematic 28). Inverters U334C and U334D invert the data strobe signals BUDS (buffered upper data strobe) and BLDS (buffered lower data strobe) issued by the MPU, and apply one of them to the input of each NAND gate. Then, either the M1SEL (memory Channel 1 select signal or M2SEL (memory Channel 2 select) signal, generated by the address decode circuit (refer to schematic 35), is connected to the other NAND gate input, to produce the Channel 1 memory bus buffer enable signals (1GBU and 1GBL) and the Channel 2 memory bus buffer enable signals (2GBU and 2GBL).

Memory Write Pulse

The memory write pulse circuit consists of gates U266F, U300A, U300B, U304A, U304B, U304C, U304D, U306A, U306B, U306C, U306D, U316A, U316B, U316C, U316D, U318A, U318B, U322A, and U322B. When the MPU accesses memory, the BR/W (buffered read/write MPU signal) is separated into a signal for the upper byte and one for the lower byte by U318A and U318B in response to the BUDS and BLDS signals. These separated signals are further divided into M1SEL and M2SEL for Channel 1 and Channel 2, respectively, by U316A, U316B, U316C, and U316D.

The signals applied to Channel 1 (U304A, U304B, and U304C) are 1MWEU (Channel 1 memory write enable for upper byte), 1MWEL (Channel 1 memory write enable for lower byte), and 1MLE (Channel 1 memory latch enable). The corresponding signals applied to Channel 2 (U306A, U306B, and U306C) are 2MWEU, 2MWEL, and 2MLE.

During acquisition, the AQCK output from DL314 is divided into signals for Channel 1 and Channel 2 by U322A and U322B, respectively. The signals for Channel 1 are applied to U304A, U304B, and U304C; those for Channel 2 are applied to U306A, U306B, and U306C. These signals respective channel write enable and latch enable signals.

In the Channel 1 only mode, the CH1 ONLY signal is high. Then, when the MC SIG (memory channel signal, addresses bit 14) signal is low, U322A is selected, and when it is high, U322B is selected. This controls the Channel 1 and channel 2 write operations.

AVERAGER

The averager (Figure 1-65) sums data while in the averaging mode. It consists of average control, Channel 1 average memory, and Channel 2 average memory. The MPU reads the summed data, which is then shifted to produce average data. Both Channel 1 and Channel 2 average memories have an 8K word x 24-bit capacity. Since both averager memories are the same, only the Channel 1 memory is explained.

AVERAGE CONTROL (DIAGRAM 40)

Average control (Figure 1-66) performs averaging start and stop control, average memory read/write control, and other control functions. It consists of an average start, an average clock, an MPU read/write control, a Channel 1 chip select, a Channel 1 average control, a Channel 1 buffer enable, a Channel 2 chip select, a Channel 2 average control, and a Channel 2 buffer enable circuit. There are chip select, average control, and buffer enable circuits in both Channel 1 and 2.

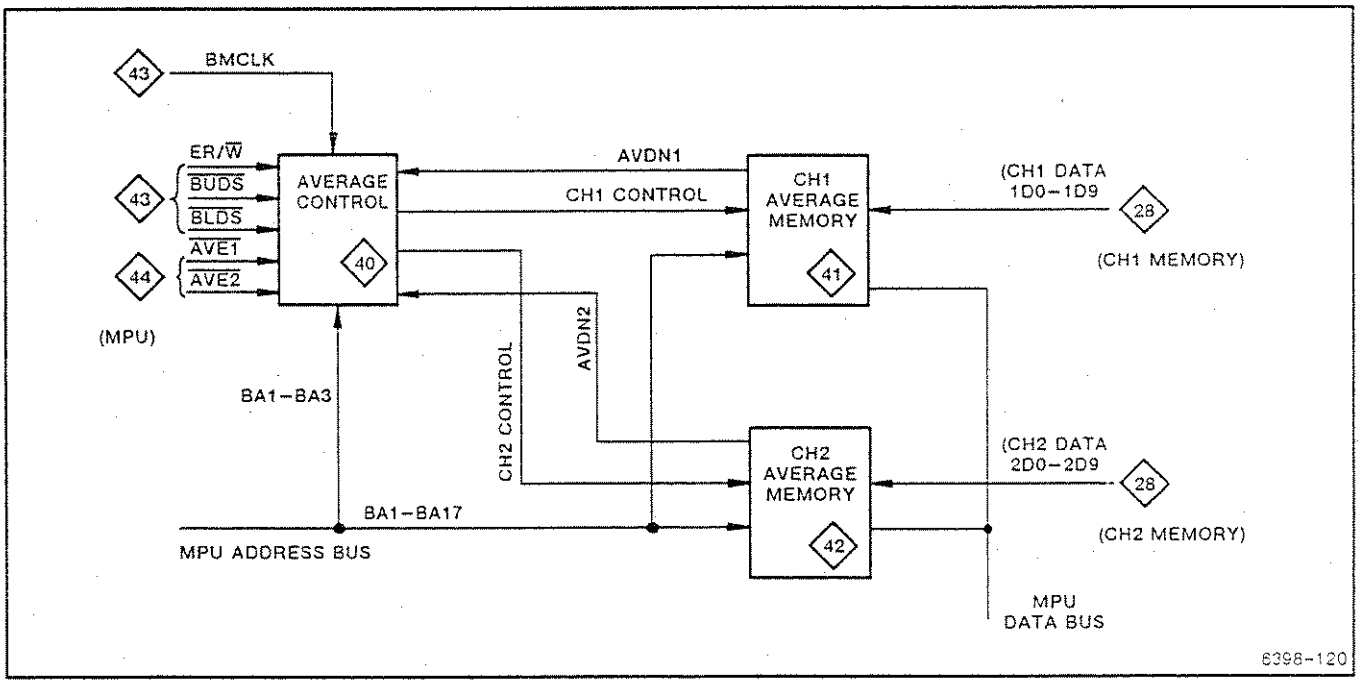


Fig. 1-65 Averager Block Diagram

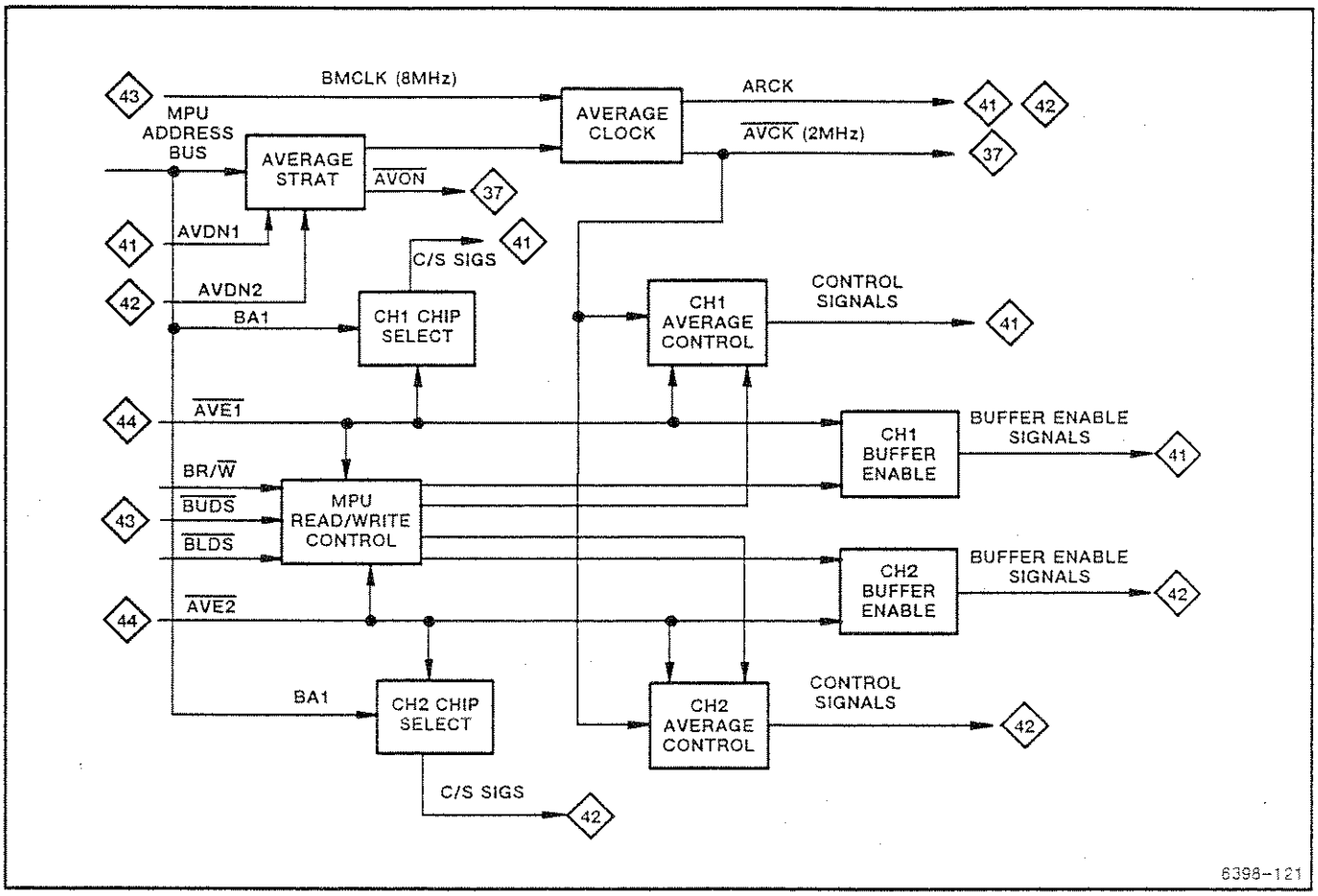


Fig. 1-66 Average Control Block Diagram

Average Start

The average start circuits (U100, U104C, U104D, U108A, and U160A) perform start, stop and other average control functions.

U100 decodes the low-order address bits (BA1-BA3) from the MPU on the $\overline{\text{AVECS}}$ (averager chip select) signal. This generates the $\overline{\text{AVSTRT}}$ (average start) and other control signals.

When $\overline{\text{AVSTRT}}$ becomes low, the flip-flop U160A Q output becomes high, the reset of the average clock circuit flip-flop U162A is cleared, and the averager starts operating. Also, the U160A $\overline{\text{Q}}$ output becomes low setting the U104C $\overline{\text{AVON}}$ output low indicating to the address generator that the averager is operating. When averaging is complete, AVDN1 (average done 1) and AVDN2, from the Channel 1 and 2 average memories, respectively, are applied to U104D. The rising edge of this OR gate output becomes the U160A clock and the Q output becomes low stopping the average clock.

Average Clock

The average clock consists of flip-flops U160B, U162A, U162B, and NOR gates U150A, U150B, and U150C. Either clock pulse BMCLK (8 MHz), generated by the MPU, or the test clock AVSTEP from U100 is selected by NOR gates U150B and U150C on the $\overline{\text{AVCKSL}}$ and AVCKSL (average clock select) signals from U170 (refer to schematic 42). The BMCLK signal used during averaging is divided by U160B whose $\overline{\text{Q}}$ output is applied to U162A and Q output applied to U162B. BMCLK is further divided through U162A and applied to the input and reset pins of U162B, thus generating averager basic clock $\overline{\text{AVCK}}$ (average clock) and ARCK signals. $\overline{\text{AVCK}}$ is supplied to the average control circuits of both Channel 1 and Channel 2, and the address generator,

which becomes the clock for the average pointer (refer to schematic 37).

MPU Read/Write Control

MPU read/write control consists of OR gates U104A U104B, U106A, U106B, U106C, and U106D, AND gate U108B, and inverters U112A and U112B. They apply the BR/$\overline{W}$, $\overline{BUDS}$, and $\overline{BLDS}$ signals to the respective Channel 1 and 2 circuits.

Channel 1 Chip Select

Channel 1 chip select switcher U102A and AND gates U110A and U110B generate the Channel 1 average memory chip select signal.

The average memory chip select 10 signal ($\overline{AMCS10}$) is used for high-order words when the MPU accesses long words (short address); $\overline{AMCS11}$ is the signal for low-order words (long address). The BA1 signal at the input of U102A performs switching between them. When the U160A $\overline{Q}$ output is low during averaging, both $\overline{AMCS10}$ and $\overline{AMCS11}$ are low.

Channel 1 Average Control

Channel 1 average control consists of AND gates U200A, U200B, U200C, and U200D, OR gates U114A and U114B, inverter U112C, and delay line DL100.

During averaging, $\overline{AVCK}$ is supplied through U114B producing $\overline{AVCK1}$, which is applied to U200A, U200B, U200C, and U200D to produce signals $\overline{AWE1U}$, $\overline{AWE1L}$, $\overline{ADCK1}$, and $\overline{AREK1}$ (Figure 1-67).

While the MPU is accessing memory, the $\overline{AWE1U}$ (average write enable Channel 1 upper) and $\overline{AWE1L}$ (average write enable Channel 1 lower) follow the data strobe signals ($\overline{BUDS}$ and $\overline{BLDS}$), respectively. During data writing, they are low.

Signal $\overline{ADCK1}$ is set low for 40 ns by U112C, U114A, and DL100 when the average enable Channel 1 signal ($\overline{AVE1}$) becomes low. On the next rising edge, the specified address is loaded into the Channel 1 address counter (refer to schematic 41). Signal $\overline{AREK1}$ is held high when the MPU accesses memory.

CH1 Buffer Enable

Channel 1 buffer enable U202 operates when the Channel 1 buffer enable signal $\overline{AVE1}$ is low (when the MPU accesses memory). It generates the Channel 1 data buffer enable signal (refer to schematic 41) in response to $\overline{BUDS}$, $\overline{BLDS}$, and $\overline{BA1}$.

CHANNEL 1 AVERAGE MEMORY (DIAGRAM 41)

Channel 1 average memory (Figure 1-68) sums the waveform data from waveform memory. It consists of a Channel 1 data buffer, a Channel 1 data adder, a Channel 1 data latch, a Channel 1 average memory, a Channel 1 address counter, an AVDN flip-flop, and a status read buffer.

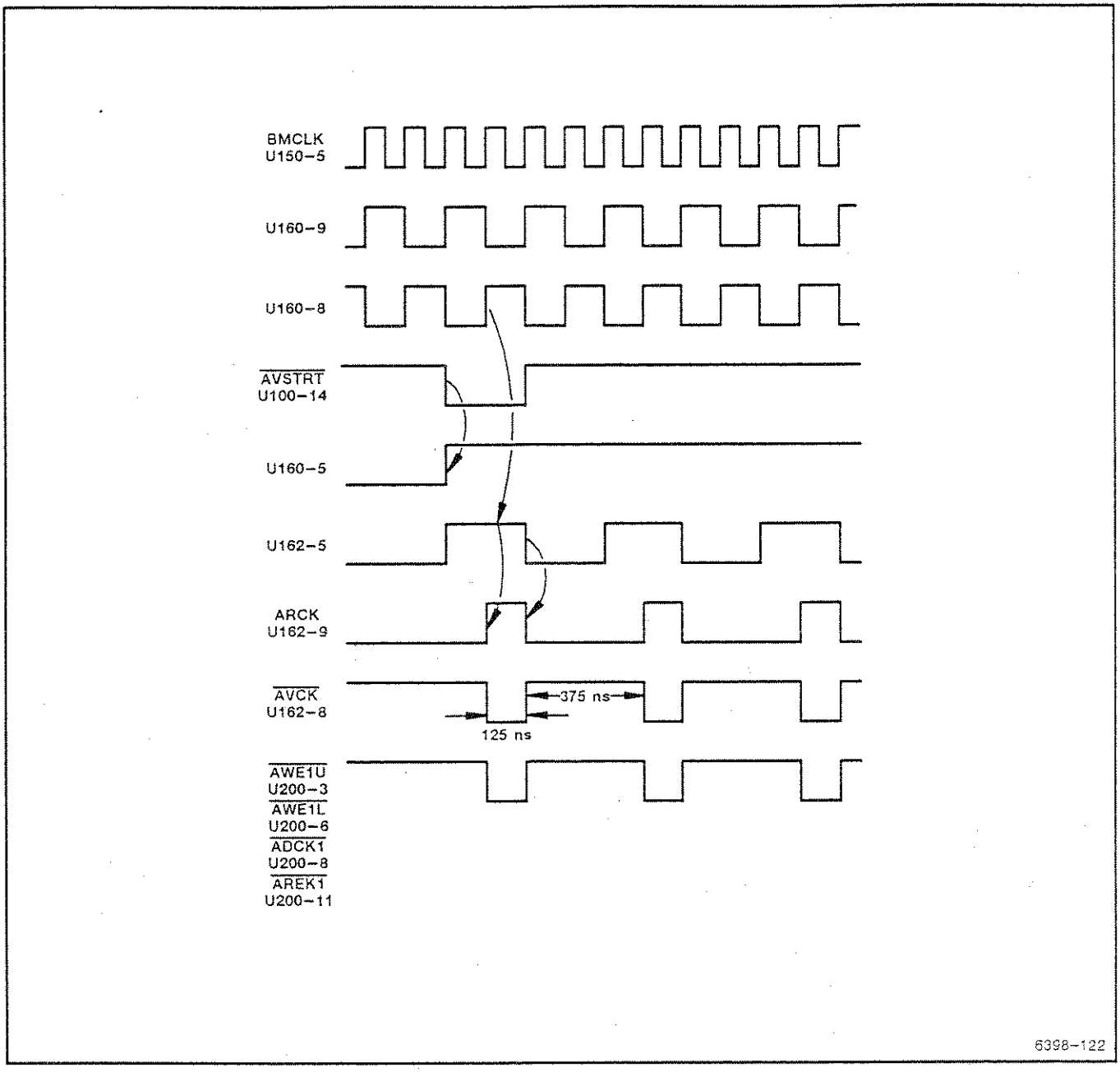


Fig. 1-67 Average Control Timing

Channel 1 Data Buffer

When the MPU accesses long words from average memory, it uses four data buffers (U260, U262, U264 and U266). However, since average memory is 24 bits long, the high-order eight bits are set permanently high by U266 and R266.

Channel 1 Data Adder

A 24-bit channel 1 data adder is formed by six adders (U220, U222, U224, U226, U228, and U230). The current cycle data from waveform memory (1MD0-1MD9) is added to the previously summed data read from the Channel 1 average memory (1D0-1D23), then output.

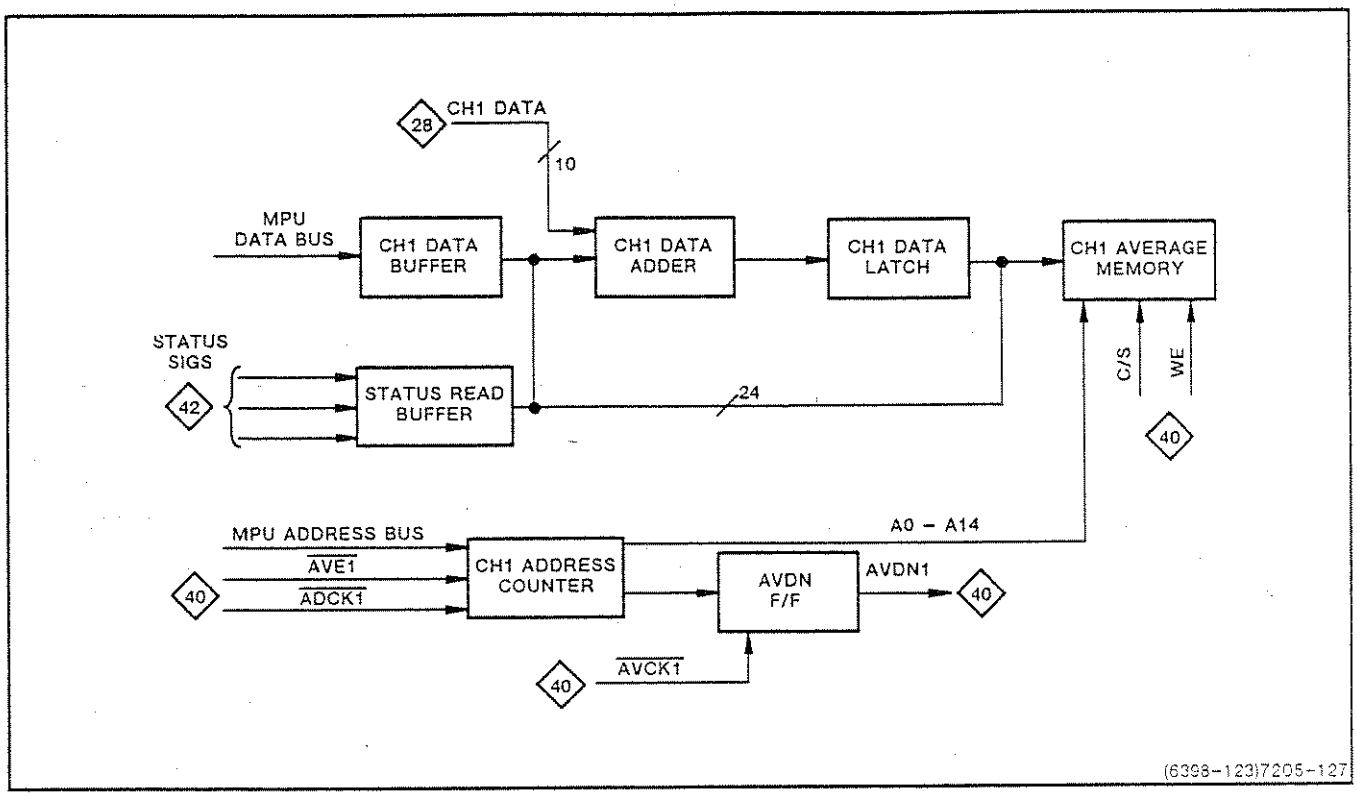


Fig. 1-68 CH1 Average Memory Block Diagram

Channel 1 Data Latch

The Channel 1 data latch (U240, U242, and U244) stores the newly averaged data. Output from the Channel 1 data adder is captured on the rising edge of ARCK and output while $\overline{\text{AREK1}}$ is low. The average memory chip select signals ($\overline{\text{AMCS10}}$ and $\overline{\text{AMCS11}}$) are always low during averaging (i.e., when chip select is valid), so $\overline{\text{AREK1}}$ is kept high (except when the average memory is in the write mode) and the latch output is set to high impedance in order to prevent contention between the output of this latch and average memory.

Channel 1 Average Memory

The 8K word X 24-bit Channel 1 average memory RAMs (U250, U252, and U254) store the averaged data.

During averaging, but before the Channel 1 data latch is written, the MPU clears previous data from the average memory by writing 0s into all memory address. The first data is then added to memory by the adder. Because the contents of average memory is 0, the newly arrived data is loaded into the data latch as is, then written to average memory.

When the data transfer from waveform memory to average memory is complete, the next waveform data is loaded into waveform memory. Then the next data sequence is added to it, and the result is written to average memory. This sequence continues for the selected number of averages. When averaging is completed, the contents of average memory are loaded into the MPU, processed, and sent to waveform memory.

Channel 1 Address Counter

The channel 1 address counter (U210, U212, U214, and U216) generates the average memory addresses.

When the MPU is accessing average memory, the Channel 1 average memory area decode signal ($\overline{\text{AVE1}}$) becomes low to enable the address counter PE pin. While this condition exists, a 40 ns pulse is applied to signal line $\overline{\text{ADCK1}}$. An address is loaded

into the address counter on the rising edge of this pulse, then output. Thus, while the MPU is accessing average memory, this circuit acts as an address latch. The start address must be loaded into the address counter before averaging begins. This is done by read-accessing the start address on the $\overline{AVE1}$ and $\overline{ADCK1}$ signals.

For up-counting, the $\overline{AVE1}$ signal becomes high causing the address counter to start counting on each rising edge of the $\overline{ADCK1}$ signal from the Channel 1 average control circuit. The start address is established such that the counter output becomes FFFF when averaging is completed. Thus, the U216-15 carry out signal (CO) becomes high when the counter reaches FFFF.

AVDN Flip-Flop

The AVDN (average done) flip-flop U180A monitors the carry output of the Channel 1 address counter and sets its AVDN1 high when carry out is high. This signal is sent to U104D (refer to schematic 40) in the average control circuit when averaging is completed.

Status Read Buffer

Status read buffer U182 buffers signals such as $\overline{AVDN1}$ when they are read by the MPU.

MPU SYSTEM

The MPU system (Figure 1-69) controls all processing and internal hardware interfaces to the 68000 MPU, and interfaces between the instrument and external devices, such as the monitor and GPIB.

Transfer of data between waveform memory and the GPIB is performed by a high-speed DMAC (DMA controller). Waveform data is provided to an external monitor, by sending it to display memory and doing a D/A conversion, then sending the resultant analog signals to the monitor.

A nonvolatile memory can store up to 20 user-selected front-panel settings and one power-down front panel settings.

The analog section of the MPU bus is buffered on the Trigger board and used as a silent bus to reduce the effects of noise.

MPU (DIAGRAM 43)

The MPU (Figure 1-70) consists of the a 68000 MPU, some buffers, an interrupt encoder, and a clock generator.

68000 MPU

The 68000 MPU (U170) controls internal operation of the instrument through a 16-bit data bus, a 23-bit address bus, and six signals that control these bus functions:

- M6800 Peripheral Control
- System Control
- Bus Arbitration
- Asynchronous Bus Control
- Processor Status
- Interrupt Control

The 68000 data bus (D0-D15) is a 16-bit, bidirectional bus. It is the data transfer path between the MPU and all peripheral devices. Transferred data is either a word (16 bits) or a byte (8 bits).

The 68000 address bus (A1-A23) is a 23-bit bus. It provides addresses during all bus cycles, except the interrupt cycle. During the interrupt cycle, it provides interrupt level information that reflects the level of the interrupt currently being processed.

The M6800 peripheral control signals E (enable), VMA (valid memory address), and VPA (valid peripheral address) are signals to capture data in synchronization with the M6800. In this instrument, only VPA is used as an input signal to initiate operation in the autovector mode when an interrupt is input to the MPU, rather than for peripheral address control.

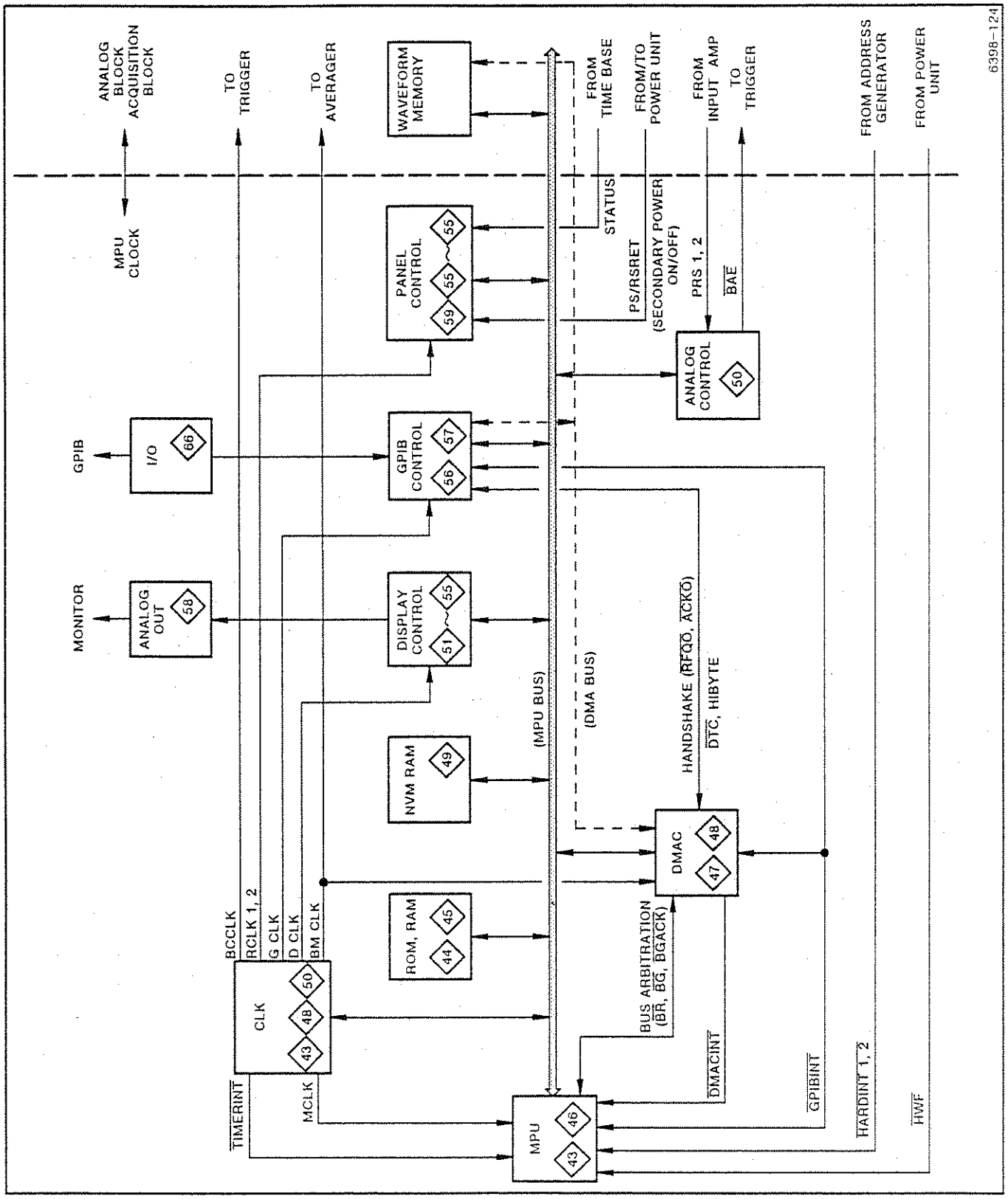


Fig. 1-69 MPU System Block Diagram

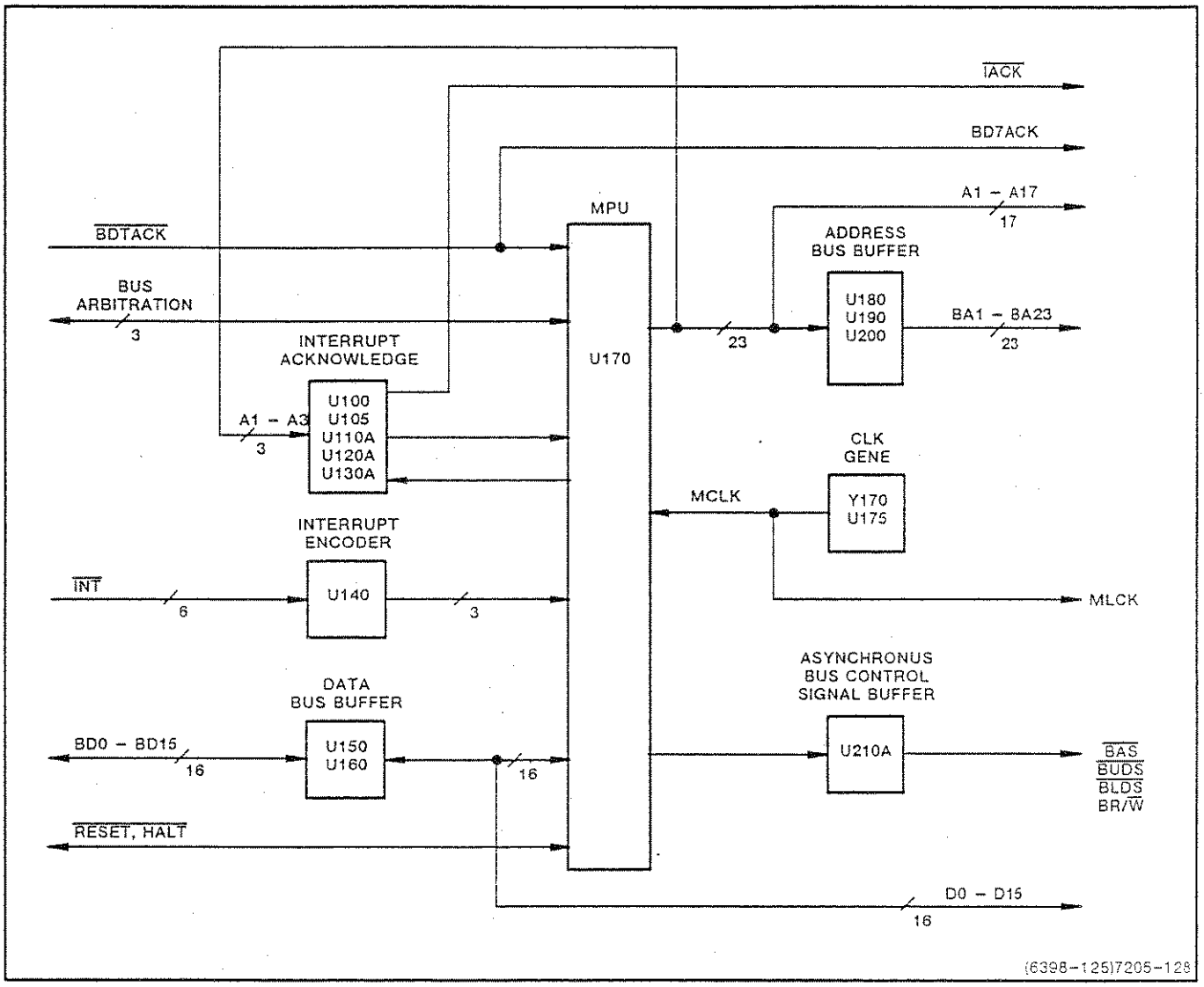


Fig. 1-70 MPU Block Diagram

System control signals are BERR (bus error), RESET, and HALT. BERR is not used. The bidirectional RESET signal resets the MPU and other applicable instrument circuitry. The MPU is reset when the RESET and HALT signals are simultaneously input at a low level, such as when power is applied.

Bus arbitration control signals BR (bus request), BG (bus grant), and BGACK (bus grant acknowledge) are used to identify and control bus mastership. Input signal BR informs the MPU that another device wants bus control. Output signal BG informs the requesting device that the MPU will release control of the bus at the end of the current cycle. Input signal BGACK informs the MPU that the requesting device is now controlling bus operation.

Asynchronous bus control signals AS (address strobe), R/W (read/write), UDS (upper data strobe), LDS (lower data strobe), and DTACK (data transfer acknowledge) provide control of asynchronous data transfers. AS signals the peripheral device that the address on the address bus is valid. R/W signals the peripheral device of the data transfer direction. UDS and LDS identify which byte(s) are being transferred from the MPU to the peripheral device. DTACK signals the MPU that a peripheral device has acquired or presented the data, and the data transfer is complete.

Processor status signals FC0, FC1, and FC2 (function codes 1, 2, and 3) identify the MPU state (user/supervisor), cycle type (data/program), and acknowledge interrupt requests. In this instrument, only the interrupt request acknowledge function code is used.

Interrupt control signals IPL0, IPL1, and IPL2 are binary encoded interrupt priority level signals to the MPU that define priority levels 0-7. Level zero indicates that no interrupts are requested; level seven is the highest level of interrupts (1-7).

Interrupt requests are detected between instruction executions. If a requested interrupt is at a higher level than the current processor priority, the MPU gets the interrupt vector from the interrupting device (via the data bus), or from an autovector location in memory, and initiates interrupt processing. If the requesting interrupt is at a lower level, or at a level equal to the current processor priority, MPU processing continues until the processor priority is at a lower priority than the requesting interrupt.

Buffers

Data buffers U150 and U160 are used by the data bus to distinguish between the MPU board bus and Mother board bus. When the MPU is the bus master, $\overline{\text{BGACK}}$ is high and U110 pin 9 is low. This enables the buffers only when the MPU accesses an external device with I/O low. Bus bits BD0-BD15 form the data bus on the Mother board.

Address bus buffers U180, U190, and U200 are enabled when the MPU is the bus master. Bits BA1-BA23 form the address bus on the Mother Board. One section of them is decoded by the address decoder to produce the chip select signals. U210A is the asynchronous bus control signal buffer, which is enabled only when the MPU is the bus master.

Interrupt Encoder

Interrupt encoder U140 is an 8-line-to-3-line priority encoder that outputs 3-bit binary data corresponding to its low inputs. Of its seven inputs (1 to 7), top priority is assigned when input 7 is low, with input 1 having the lowest priority. 3-Bit binary data (IPL0-IPL2) is input to the 68000 to establish the interrupt level. The binary levels are decoded as follows: level 7 ($\overline{\text{HWF}}$), level 6 ($\overline{\text{HARDINT2}}$), level 5 ($\overline{\text{TIMER INT}}$), level 4 ($\overline{\text{DMACINT}}$), level 3 ($\overline{\text{GPIBINT}}$), and level 2 ($\overline{\text{HARDINT1}}$).

$\overline{HWF}$, which is issued by the power supply, occurs when there is an abnormal condition in the power supply. $\overline{HARDINT2}$ is issued by the A40 Address Generator Board when the instrument is operating in the roll mode each time data is written to the waveform memory. $\overline{TIMER\ INT}$ is issued by the hardware timer every 20 ms. $\overline{GPIBINT}$ is issued from the GPIB adaptor TMS9914A. In all other operation modes besides the roll mode, $\overline{HARDINT1}$ is issued by the A40 address generator each time an acquisition is completed.

On interrupt, the MPU enters an interrupt acknowledge cycle where it outputs a code to the interrupt acknowledge circuit (U100, U105, U110A, U120A, and U130A) that is identical to the input interrupt level on address lines A1-A3. Also, signal outputs FC0-FC2 become high, $\overline{AS}$ becomes low, and the $\overline{VPA}$ input becomes low from a decode operation at U100. At this point, the MPU enters the autovector mode and automatically jumps to the address corresponding to the interrupt level. Other actions that occur are: $\overline{DMACINT}$ does not input a signal to $\overline{VPA}$, the U100 decode output is gated at U110A and input to DMAC (refer to schematic 47) as an $\overline{IACK}$ signal. Thus, in the user-vector mode, the MPU jumps to the address written into the DMAC interrupt register by the firmware program.

Clock Generator

The 16 MHz pulse from the clock generator (Y170) is divided down to an 8 MHz, 50% duty cycle MPU clock by U175A. This clock also is used as the DMAC clock, and further divided for other clocks.

ADDRESS DECODER AND RAMS (DIAGRAM 44)

The address decoder and RAMs (Figure 1-71) decode the MPU address outputs to generate chip select signals. System RAM temporarily stores data while the MPU is executing various functions. It consists of $\overline{DTACK1}$ delay, address decoder, $\overline{DTACK5}$ delay, $\overline{DTACK8}$ delay, and system RAMs.

$\overline{DTACK1}$ Delay

The $\overline{DTACK1}$ delay (U220C, U220D, U260A, U270, DL270, and U280B) delays the $\overline{DTACK1}$ output from U280B by one clock cycle. When U260A output becomes high, this circuit operates for chip selecting average memory ($\overline{AVE1}$ and $\overline{AVE2}$). If a one-clock wait cycle is necessary for accessing average memory, this circuit must be used.

$\overline{DTACK}$ signals ($\overline{DTACK1}$-$\overline{DTACK9}$) are produced by decoding the address output from the MPU, then returning it to terminate the MPU cycle. Thus, the DTACK signal can be delayed to ensure accurate data transfer for devices requiring a longer access time.

Address Decoder

The address decoder (U220B, U230, U240, and U250) derives the chip select signals for system ROM, the average memory, and other circuit functions.

$\overline{ROM}$ is the chip select signals for accessing system ROM; $\overline{AVE1}$ and $\overline{AVE2}$ are the chip select signals for accessing average memory for both Channel 1 and Channel 2 on the A44 Averager board; $\overline{DRAMCS}$ is the chip select signal for accessing display RAM on the A54 Display board; $\overline{HARD1CS}$ and $\overline{HARD3CS}$ are chip select signals that are further decoded on the A52 DMA Board; $\overline{KEYCS}$ is the chip select signal used on the A60 Panel Control Board for KEY SENSE and turning LEDs on and off; $\overline{DMACCS}$ is the chip select signal used to access internal registers of the DMAC (68450) on the A52 DMA Board; $\overline{NVMCS}$ is the chip select signal used to access nonvolatile memory on the A52 DMA Board; and $\overline{DLED}$ is the chip select signal used to turn the MPU system diagnostic LEDs off.

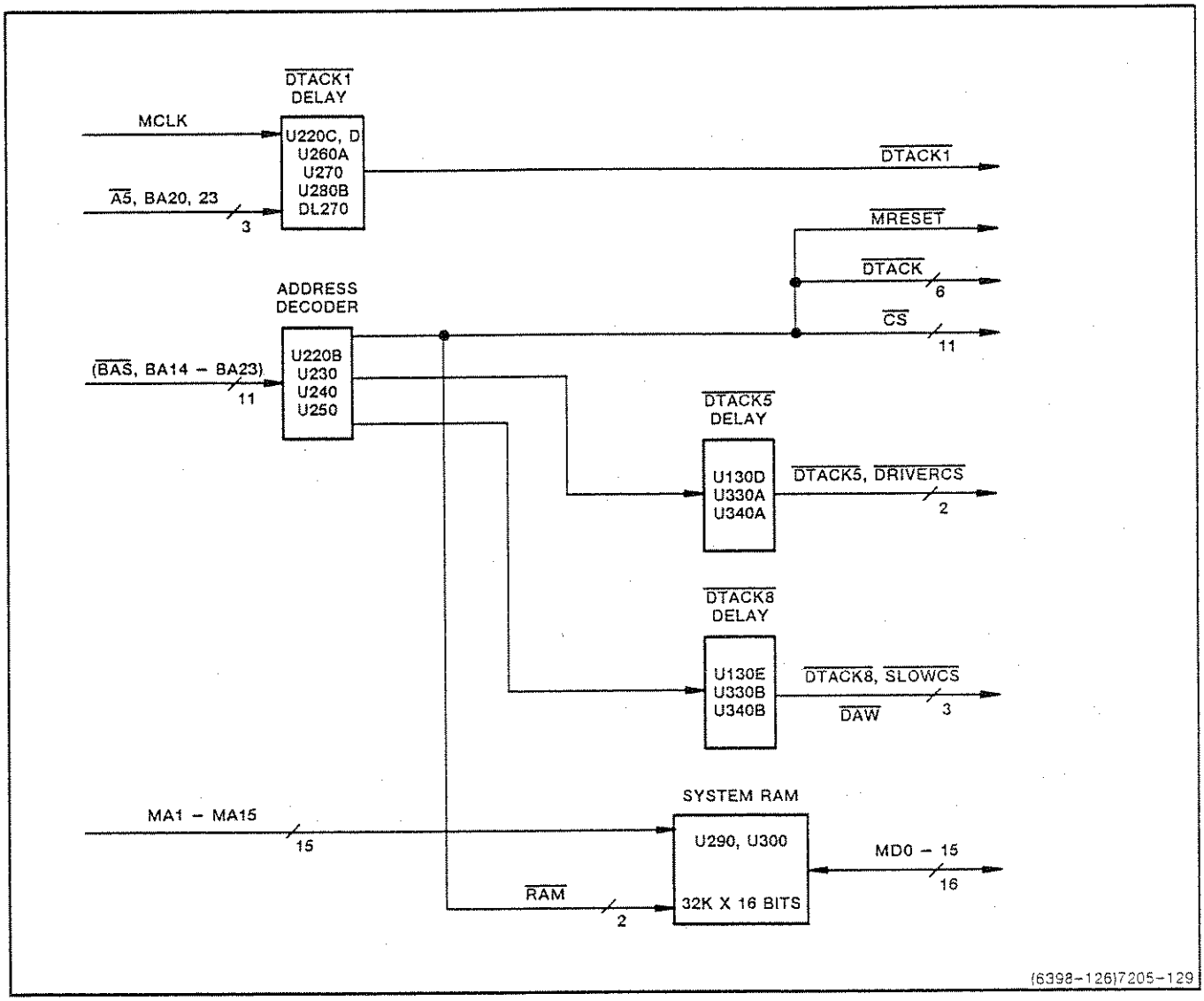


Fig. 1-71 Address Decoder and RAMs Block Diagram

DTACK5 Delay

The DTACK5 delay (U130D, U330A, and U340A) delays the DTACK5 signal to control the panel indicator drivers. When the 12-pin output of address decoder U250B becomes low, the negative pulse selected by C330 and R330 is supplied by the U330A Q output (pin 4) causing the U340 output (DTACK5) to become low on its rising edge. When the DTACK signal returns to the MPU, it terminates the MPU cycle. This process causes the DRIVERCS signal to become a wider negative pulse, thus ensuring a signal of sufficient length to access the 7-segment driver on the A60 Panel Control Board.

DTACK8 Delay

The DTACK8 delay (U130E, U330B, and U340B) is exactly the same as the DTACK5 delay, except SLOWCS is the chip select signal to access the D/A converters on the A14 AUTO CAL Board and the A22 TRIGGER Board and DAW is the write pulse to the D/A converters.

System RAMs

The two system RAMs (U290 and U300) combined to provide 32K words of memory. The upper-byte RAM is U300; the lower-byte RAM is U290.

ROMS (DIAGRAM 45)

The ROMs circuitry (Figure 1-72) generate read and write signals, and permanently store MPU commands. They include buffers, ROMs, and read/write logic.

Buffer

Memory address buffers U350, U360, and U365 (for ROM and RAM) are enabled when the BGACK signal is low and the MPU is the bus master. Buffer outputs MA1-MA17 form the bus on the A50 MPU Board, but they are not connected to circuits external to that board.

ROM

System ROM consists of U390-U420; however, U410 and U420 are used only for special options, and are not installed in a standard instrument. The lower-byte ROMs are U390 and U410; the upper-byte ROMs are U400 and U420. The standard ROM set (U390 and U400) provides a memory capacity of 128K words.

Read/Write Logic

The read/write logic (U130F, U370, and U380A) generates the read and write signals for RAMs, ROMs, and other circuit. These include $\overline{UOE}$ (upper-byte output enable), $\overline{UWE}$ (upper-byte write enable), $\overline{LOE}$ (lower-byte output enable), and $\overline{LWE}$ (lower-byte write enable), which are generated from the $\overline{BUDS}$, $\overline{BLDSW}$, and BR/$\overline{W}$ signals. These signals allow access to individual bytes of memory. It also generate

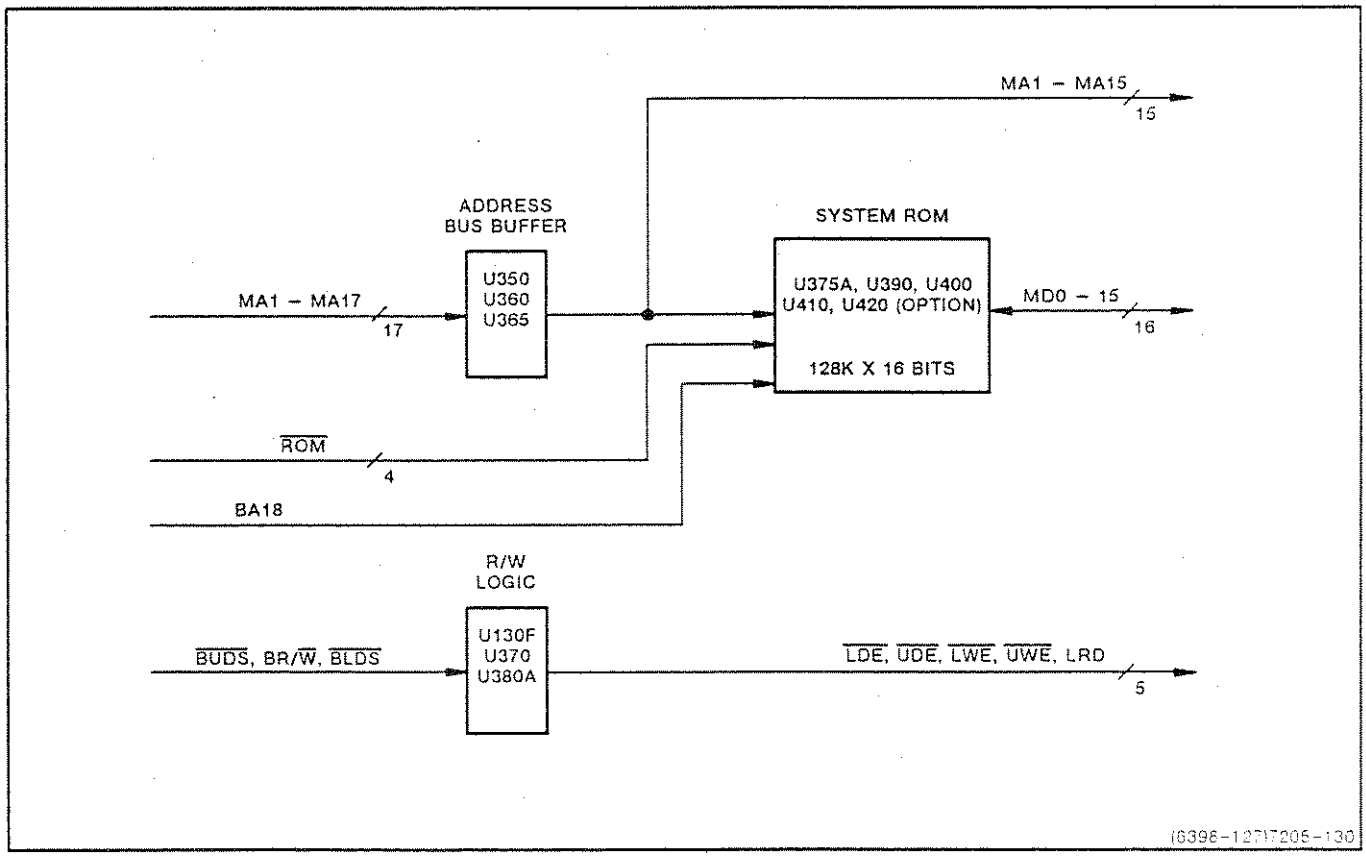


Fig. 1-72 ROMs Block Diagram

a high LRD signal used to read the GPIB adaptor TMS9914A internal register.

DTACK (DIAGRAM 46)

The DTACK (Figure 1-73) generates signals to terminate an MPU cycle and outputs the MPU RESET and other signals. It consists of a DTACK circuit, a buffer, a diagnostic LED driver, and a reset circuit.

DTACK

The DTACK circuit consists of gates U220E, U260B, U470, and U475A. Gates U260B, and U220E generate the DTACK signal when the MPU is accessing waveform memory. The $\overline{DDTACK}$ signal is supplied by the DMAC DTACK pin when the MPU accesses the internal register of the 68450 DMAC. The negative-logic OR of the $\overline{DTACK}$, $\overline{DTACK2}$-$\overline{DTACK9}$ signals, and $\overline{ROM}$ from U470 and U475A is shaped by U210B and applied to MPU DTACK pin as the $\overline{BDTACK}$ signal to terminate the MPU instruction cycle. This same sequence occurs when the DMAC becomes the bus master, and the $\overline{BDTACK}$ signal is applied to the DMAC DTACK pin to terminate the transfer of one data record.

Buffer

Data bus buffers U500 and U510 for ROM, RAM, and LED driver U490 are enabled whenever ROM, RAM, or LED driver U490 is accessed. Signal lines MD0-MD15 form the data bus on the A50 MPU Board, but are not connected to circuits external to that board.

Diagnostic LED Driver.

The diagnostic LED driver (U490) controls the kernel diagnostic indicators. When power is applied, U490 is reset by the $\overline{BRESET}$ signal setting all outputs low. This illuminates the diagnostic LEDs (DS490-DS492) indicating that +5 V is normal. When

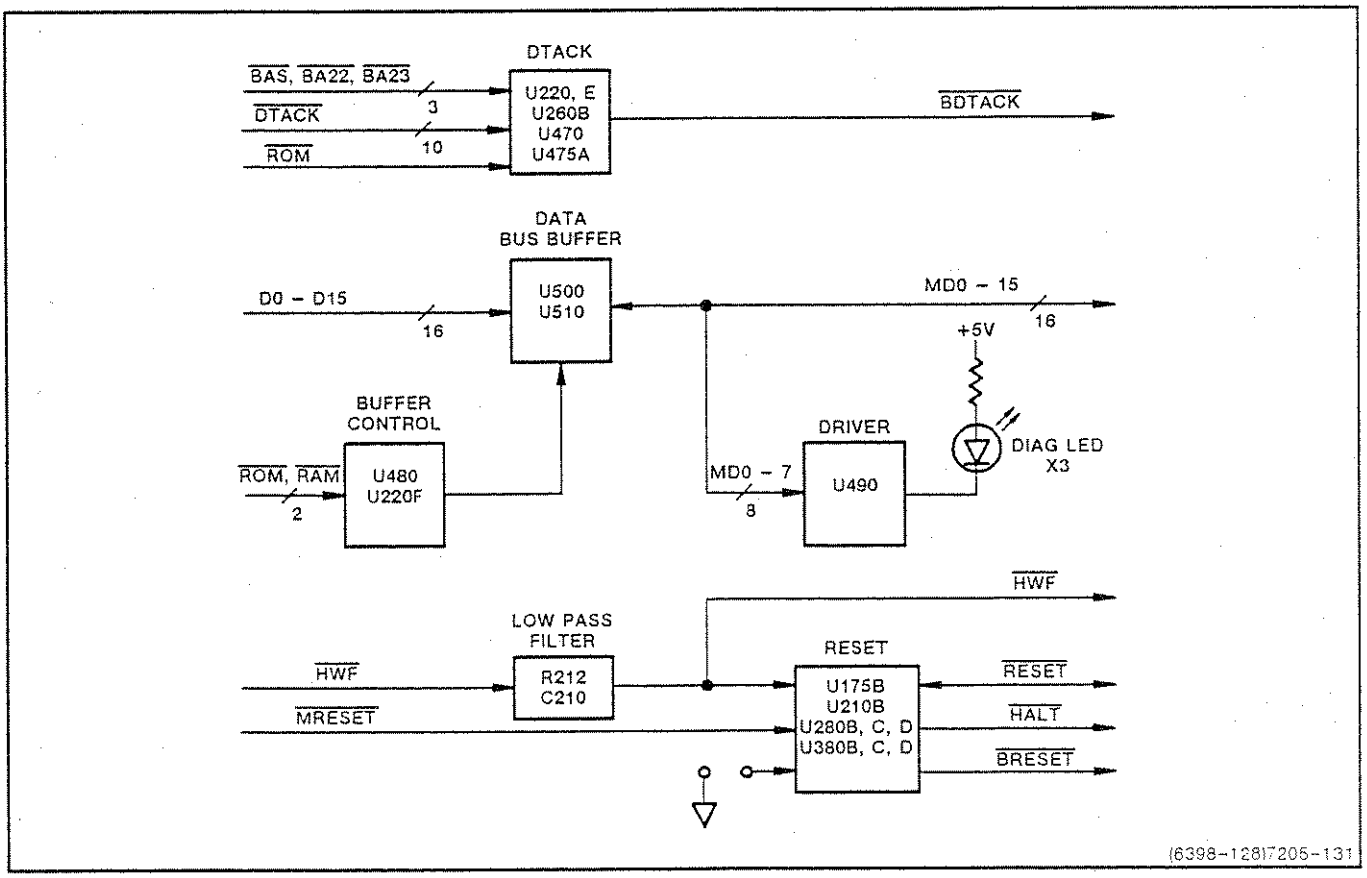


Fig. 1-73 $\overline{DTACK}$ Block Diagram

the MPU accesses U490 to initiate power-on diagnostics, it sets pin 2 high, turning off DS490. Then the diagnostics ROM is checked, and if OK, DS491 is turned off. The diagnostics RAM is checked next, and if OK, DS492 is turned off.

Reset

The reset circuit (U175B, U280D, U380B, and U380D) together with the time constant circuit (C175, CR175, and R177) generate the RESET and HALT signals when power is applied to the instrument.

When power is applied, U175B is cleared by the time-constant circuit through U380B and U380D causing $\overline{\text{RESET}}$ and $\overline{\text{HALT}}$ signals to become low resetting the MPU. Approximately 300 ms later, the $\overline{\text{HWF}}$ signal transitions from low to high, causing the U175B output and the $\overline{\text{RESET}}$ and $\overline{\text{HALT}}$ signals to become high, clearing the MPU reset condition and initiating normal operation. The $\overline{\text{BRESET}}$ signal resets all hardware other than the MPU at the same timing as the $\overline{\text{RESET}}$ signal.

When the $\overline{\text{HWF}}$ signal is driven low because of an abnormal power supply condition, the MPU performs nonvolatile memory (NVM) checksum calculations. R212 and C210 are lowpass filters that reduce the noise components caused by the $\overline{\text{HWF}}$ signal, which is shaped by U210B. When the NVM calculations are completed, a $\overline{\text{MRESET}}$ signal is output to access the address decoder and handle the instantaneous power drop out. $\overline{\text{MRESET}}$ passes through U380C to clear U175B in the power-on reset circuit. Figure 1-74 shows the $\overline{\text{HWF}}$ and $\overline{\text{RESET}}$ signal conditions when power is applied to the instrument and during instantaneous interruption.

The 68000 MPU RESET signal pin is bidirectional; it can output a $\overline{\text{RESET}}$ signal in response to a software reset. A RESET command is executed when address errors, illegal instructions, or divide-by-zero occur. The same operations are performed as for clearing the MPU reset condition when power is applied.

The J280 strap RESET signal is generated by U210B, J280, R281, C280, R282, and CR280.

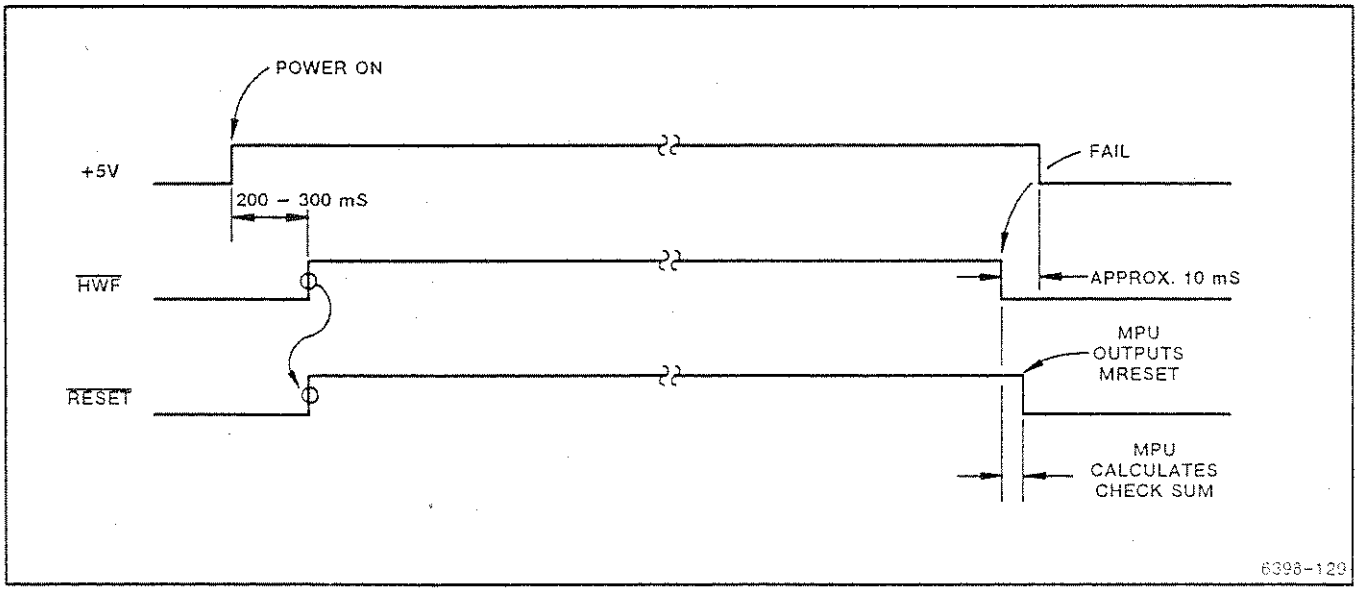


Fig. 1-74 Timing Diagram for +5 V, $\overline{\text{HWF}}$, and $\overline{\text{RESET}}$

68450 DMAC (DIAGRAM 47)

The 68450 DMAC (Figure 1-75) controls DMA transfers. It consists of a 68450 DMAC, a buffer and latch, DTACK control, and encoder circuits.

68450 DMAC

The 68450 DMAC (U190) contains a 16-bit data bus and a 23-bit address bus. When the MPU is bus master the MPU performs both read and write opera-

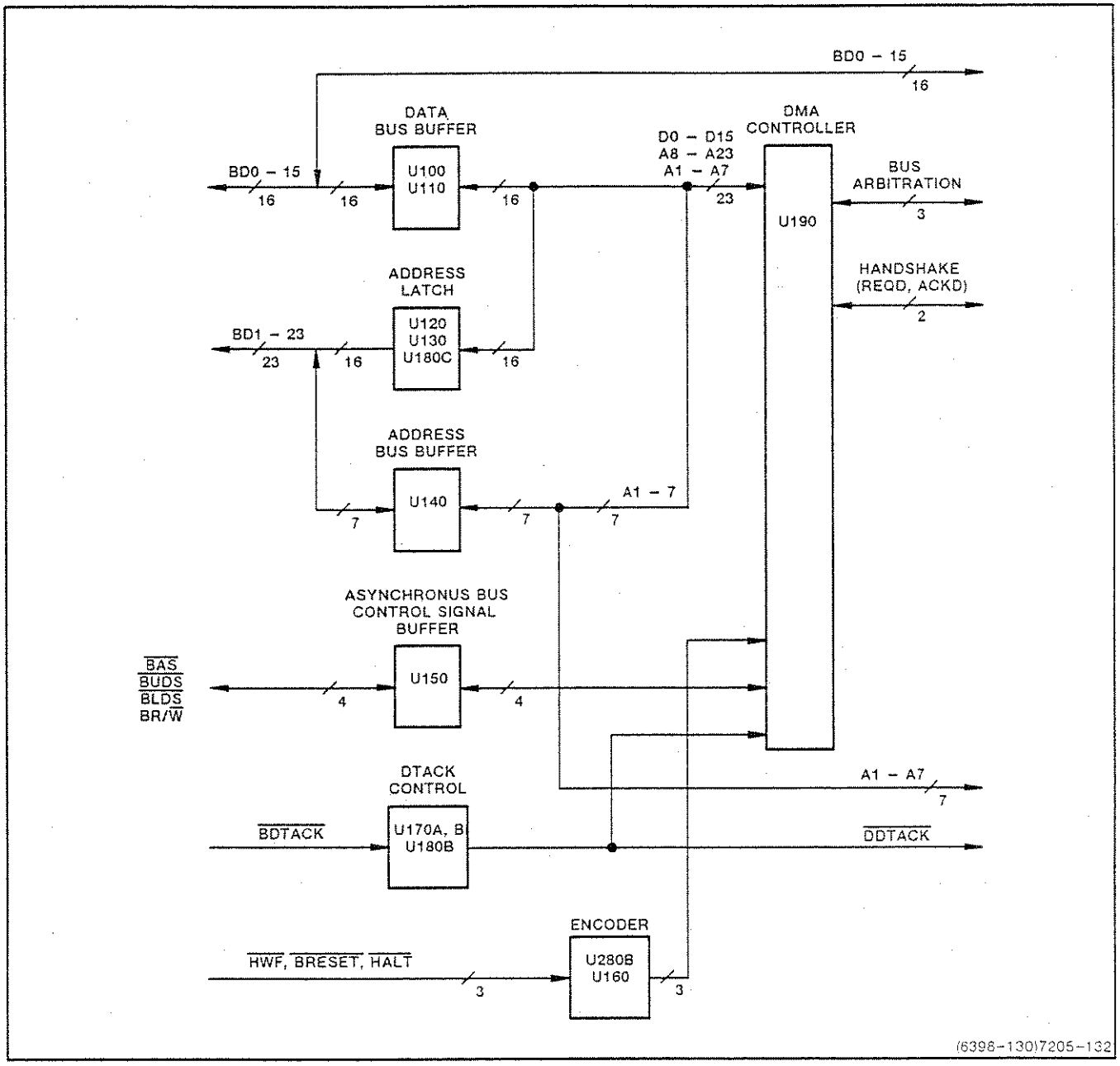


Fig. 1-75 DMAC Block Diagram

tions to the DMAC internal registers. DMAC performs DMA transfer control operations when the DMAC becomes the bus master. The MPU sets the DMA operating conditions such as the number of data words to be transferred and the transfer address when reading from or writing to DMAC internal registers.

The DMAC performs 4-channel DMA transfers but RTD 710A uses only Channel 0. Data is transferred between waveform memory on the A36 Memory Board and the data registers of the TMS9914A GPIB adaptor on the A56 GPIB/Monitor Board. Transfers are performed by handshaking between a TMS9914A external transfer request signal ($\overline{REQ0}$) and $\overline{ACK0}$ signal from the DMAC when it receives a $\overline{REQ0}$ signal.

When the MPU sends a START command to the DMAC, bus arbitration is performed between the MPU and DMAC bus master. The first data record is transferred immediately, while succeeding data records are transferred only on a $\overline{REQ0}$ request.

In the cycle-steal bus hold mode, DMAC holds the bus as long as the $\overline{REQ0}$ signal is applied within a time interval set by the DMAC internal register. Bus arbitration is performed whenever this time interval is exceeded returning bus priority to the MPU. When $\overline{REQ0}$ is input again, bus priority passes back to the DMAC and a transfer is performed. As long as the data transfer speed between the instrument and the GPIB peripherals is not excessively low, transfers over the GPIB are continued that allows the DMAC to maintain bus priority until all data is transferred.

Buffer and Latch

Data bus buffers U100 and U110 are enabled whenever the MPU performs read or write operations on the DMAC internal register, or the DMAC performs DMA transfers in dual addressing mode (dual addressing mode is not used with the RTD 710A). During these times, the data bus on the Mother Board and DMAC are connected.

Address bus buffers U120 and U130 are used separately when the 68450 DMAC uses the same pins for address outputs (A8-A23) and data input/outputs (D0-D15). Thus, the address data output must be latched outside the DMAC, then output to the address bus.

Address buffer U140 establishes the address input/output direction whenever the MPU accesses the DMAC internal register or non-volatile memory, or the DMAC outputs the address for a DMA transfer.

Asynchronous bus control buffer U150 establishes the input/output direction according to MPU or DMAC bus mastership.

DTACK Control

When the MPU accesses the DMAC internal register, the 68450 DMAC outputs the $\overline{DTACK}$ signal from the DTACK pin. Also, during a DMA transfer it inputs the $\overline{BDTACK}$ signal at the DTACK pin to terminate the data record transfer. Input and output of the DTACK signal is controlled by U170A, R170B, U180B. When U170A is disabled and U170B enabled, DTACK is enabled for output; when U170A is enabled and U170B is disabled, DTACK is disabled for output.

Encoder

Encoder U160 is an 8-line-to-3-line priority encoder. When the $\overline{HWF}$ or $\overline{BRESET}$ signal becomes low, the output of U280B, and all outputs of U160 become low. This results in a zero input to the DMAC signal lines ($\overline{BEC0}$-$\overline{BEC2}$), which resets the DMAC hardware. If the $\overline{HALT}$ signal at U160-1 becomes low, the $\overline{BEC0}$-$\overline{BEC2}$ signals assume a binary value of 011 causing the DMAC to HALT and pass bus priority to the MPU temporarily suspending the DMA transfer. When $\overline{HALT}$ again becomes high, the HALT condition clears, $\overline{REQ0}$ becomes low, and the DMA transfer restarts. If $\overline{REQ}$ is still high, the DMA transfer restarts when it becomes low.

ADDRESS DECODER (DIAGRAM 48)

The address decoder (Figure 1-76) further decodes the address on the A50 MPU Board to produce several signals. It consists of an address decoder, buzzer, timer interrupt control, and DMAC HALT control circuits.

Address Decoder

Address decoder U200 decodes the following chip select signals and supplies them through the Mother board to their respective boards for further processing: $\overline{IACS}$ (Input Amp Board Chip Select), $\overline{TRICS}$ (Trigger Board Chip Select), $\overline{TVTCS}$ (TV Trigger Board Chip Select), $\overline{ENVCS}$ (Envelope Board Chip Select), $\overline{TBCS}$ (Time Base Board Chip Select), $\overline{RE1CS}$ (not used), $\overline{ADGCS}$ (Address Generator Board Chip Select), $\overline{AVECS}$ (Average Board Chip Select).

Address decoder U220 decodes the following chip select signals and supplies them through the Mother board (except $\overline{DMAMISCS}$) to their respective boards for further processing: $\overline{MPUMISCS}$ (MPU Board $\overline{MISCS}$), $\overline{DMAMISCS}$ (DMA Board $\overline{MISCS}$), $\overline{DISPMISCS}$ (Display Board $\overline{MISCS}$), and $\overline{GPIBMISCS}$ (GPIB/Monitor Board $\overline{MISCS}$).

The $\overline{9914CS}$ signal is used to access the internal register of the GPIB adaptor TMS9914A on the A56 GPIB/Mother board. $\overline{PRSCS}$ is for the vertical input BNC connector probe sense signal. U230 further decodes the $\overline{DMAMISCS}$ signal.

Buzzer

The buzzer circuit (U240, U250, Q250, LS250) performs ON/OFF control of the LS250 buzzer. Timer U250 and components R253, R254, and C251 compose an oscillator that outputs a pulse to turn buzzer driver Q250 on and off.

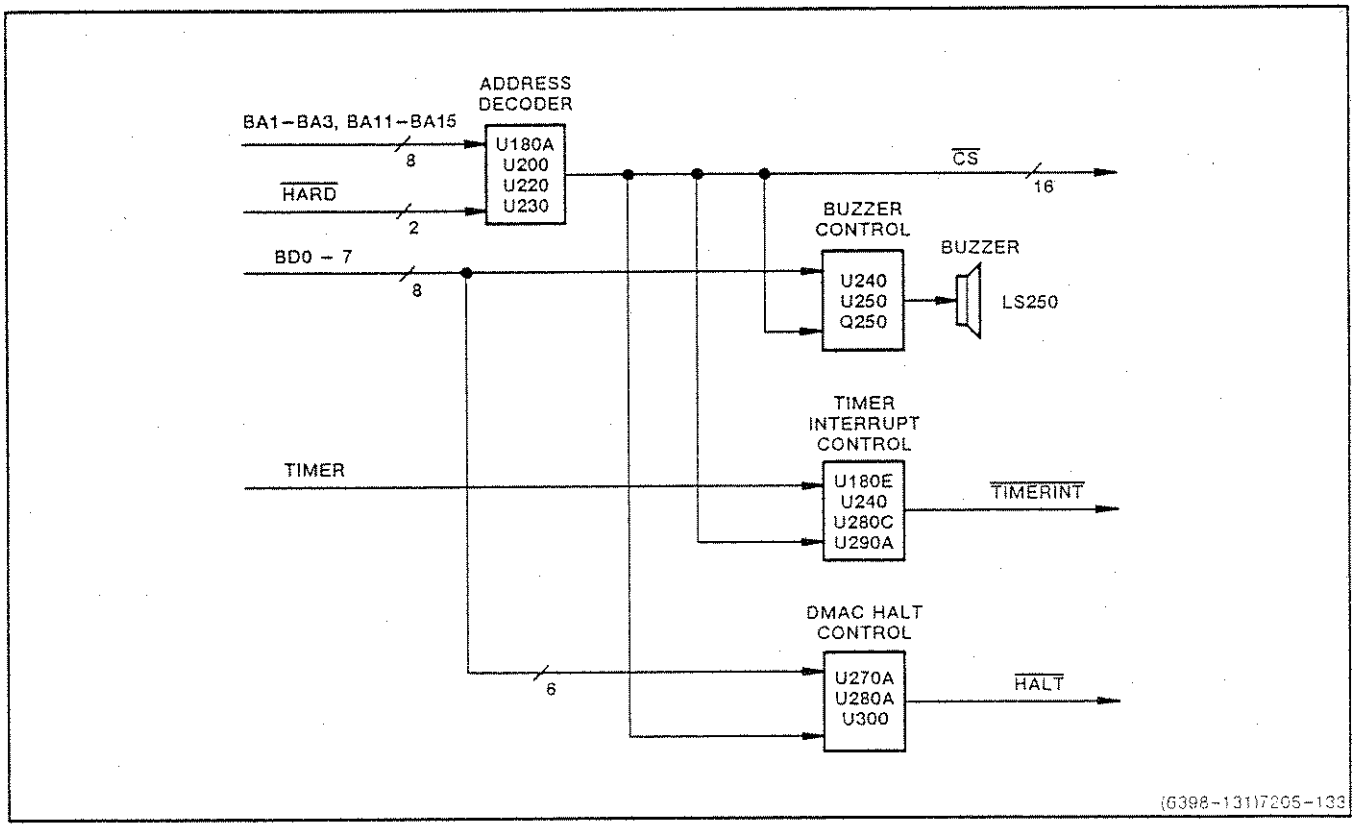


Fig. 1-76 Address Decoder Block Diagram

Timer Interrupt Control

The timer interrupt control (U180E, U240, U280C, and U290A) performs control of the hardware timer interrupt. A 50% duty cycle, 50 Hz timer clock is constantly input into U290A pin 11. When 290A pin 12 is low and pin 9 is high, its output becomes low on the rising edge of the timer clock.

This signal is applied to the MPU as the $\overline{\text{TIMERINT}}$ (timer interrupt) signal. While interrupted, MPU performs operations such as key sense and set pin 12 of the address decoder U230 low to preset the U290A to generate the $\overline{\text{TIMERINT}}$ signal again on the next timer clock. Figure 1-77 shows the conditions under which $\overline{\text{TIMERINT}}$ is generated.

DMAC Halt Control

The DMAC halt control (U270A, U380A, and U300) controls the application of the $\overline{\text{HALT}}$ signal to the DMAC. When the DMAC is performing data transfers between waveform memory and the GPIB, U300 pin 15 is set low. When the $\overline{\text{GPIBINT}}$ signal from GPIB adaptor TMS9914A is applied through U270A to U280A during data transfer, the $\overline{\text{HALT}}$ output of U280A is set low causing the DMAC to halt. Once the DMA transfer is suspended, the MPU restarts operation and the HALT signal is maintained low, thus setting U300 pin 10 low. Subsequently, the MPU reads the TMS9914A interrupt status register, then analyzes and processes it. When the register is read, $\overline{\text{GPIBINT}}$ becomes high. When data transfer is resumed by the DMAC, U300 pin 10 is set high.

NON-VOLITILE MEMORY (NVM) (DIAGRAM 49)

Non-volitile memory (NVM) (Figure 1-78) provides for the storage of front-panel setting when the power is turned off. It consists of the +5 V watch, write protect, switch, battery check, NVM, and buffer circuits.

+5 V Watch

The +5 V watch circuit (U310 and U315) monitors the +5 V voltage. If it increases to more than approximately 4.65 V, pin 2 of U310 will be at a higher potential than pin 3 causing the output of U310 to

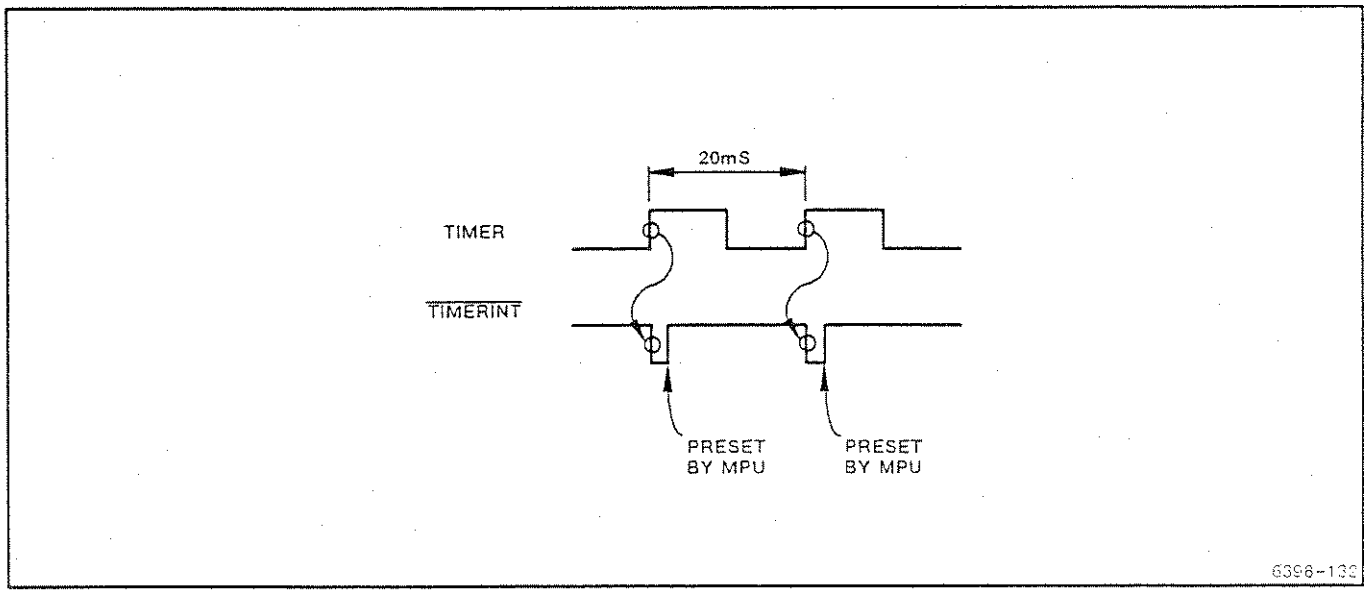


Fig. 1-77 $\overline{\text{TIMERINT}}$ Timing Diagram

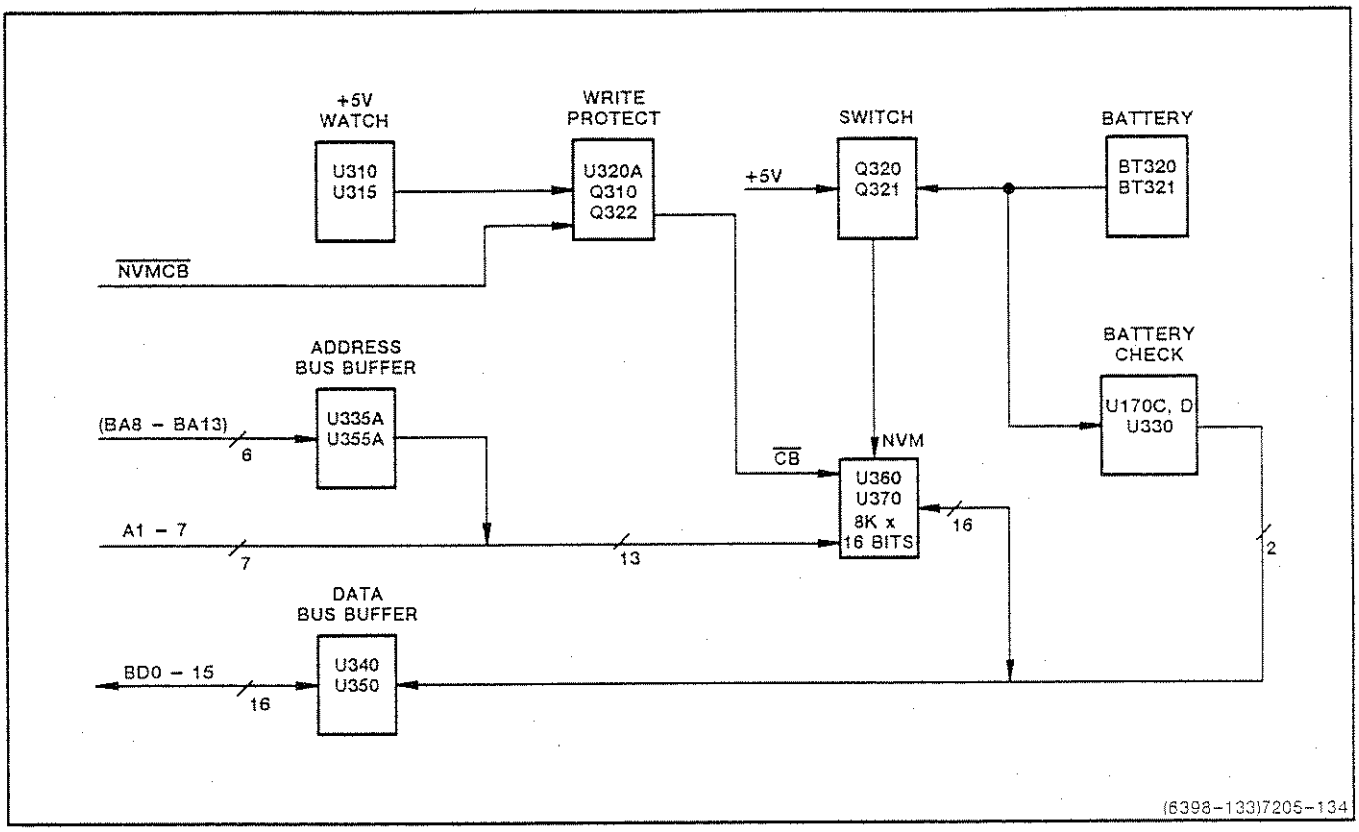


Fig. 1-78 Non-Volatile Memory Block Diagram

become low. Conversely, if it decreases below approximately 4.65 V, the output of U310 becomes high. R312 and R313 provide circuit hysterisis.

Write Protect

The write protect circuit (Q310, Q322, and U320A) prevents the contents of NVM from being destroyed when power is turned on or off. The $\overline{CE}$ pin of NVM must be set high before Vcc decreases below 4.5 V to prevent its contents from being destroyed. Therefore, when power is turned off causing the +5 V supply voltage to fall below 4.65 V, the U310 output in the +5 V watch circuit becomes high, turning Q310 off. This causes the output of gate U320A to become low, turning Q322 off. Thus, the NVM chip select pin goes high and the contents of the NVM are preserved.

When power is turned on and the +5 V voltage reaches 4.65 V, the output of U310 becomes low, turning Q310 on. The R319 and C311 time-constant of the circuit is sufficiently long that the write protect is applied and U320A pin 1 is kept low until the +5 V voltage stabilizes. When the +5 V voltage reaches its stabilized state, U320A pins 1 and 2 become high. When the MPU wants to write to the NVM it sends a $\overline{NVMCS}$ (non-volitile memory chip select) signal to U320A causing Q322 on and NVM $\overline{CE}$ pins low.

Switch

The switch circuit (Q320, Q321, R322, and R323) controls the application of power to the NVM. When the +5 V voltage is normal, both Q320 and Q321 are on, thus power is supplied to the NVM Vcc pin from the +5 V supply. When the +5 V supply voltage falls below approximately 2.5 V, Q320 and Q321 turn off, thus power is supplied from the batteries (BT320 and BT321). CR320 and CR321 prevent the batteries from charging when the +5 V supply is being used; R325 and R326 are current-limiting resistors.

Battery Check

The battery check circuit (U330, U170C, and U170D) monitors the condition of the batteries (BT320 or BT321). If the voltage of either battery falls below approximately 2.4 V, the output of its respective operational amplifier (U330A or U330B) becomes low. During power-on diagnostics the condition of the batteries is checked by reading the outputs of U170C and U170D with the $\overline{\text{BAT.TEST}}$ signal. A diagnostic error message is sent if the voltages are found to be 2.4 V.

Non-Volitile Memory

The non-volitile memory (U360 and U370) is used to store up to 20 sets of user-selected front panel settings, and the current panel setting for a total of 21 settings. When the power is turned off, a level 7 interrupt is sent to the MPU on the falling edge of the $\overline{\text{HWF}}$ signal. This causes the MPU to immediately perform an NVM checksum calculation and write the result to NVM. When the front panel power switch is turned off, the +5 V voltage is maintained for about 10 ms after the falling edge of the $\overline{\text{HWF}}$ signal to allow storage of the settings, which are restored when the instrument is powered-up.

Buffer

Buffer U335A and U355A are bus buffers for the address NVM. Buffers U340 and U350 are data buffers enabled during MPU read or write operations to hardware on the A52 Board other than the DMAC.

DOT CLOCK AND TIMER (DIAGRAM 50)

The dot clock and timer (Figure 1-79) divides an 8 MHz clock to produce several different clock pulses. It consists of a divider, oscillator, PRS buffer, and analog enable control circuit.

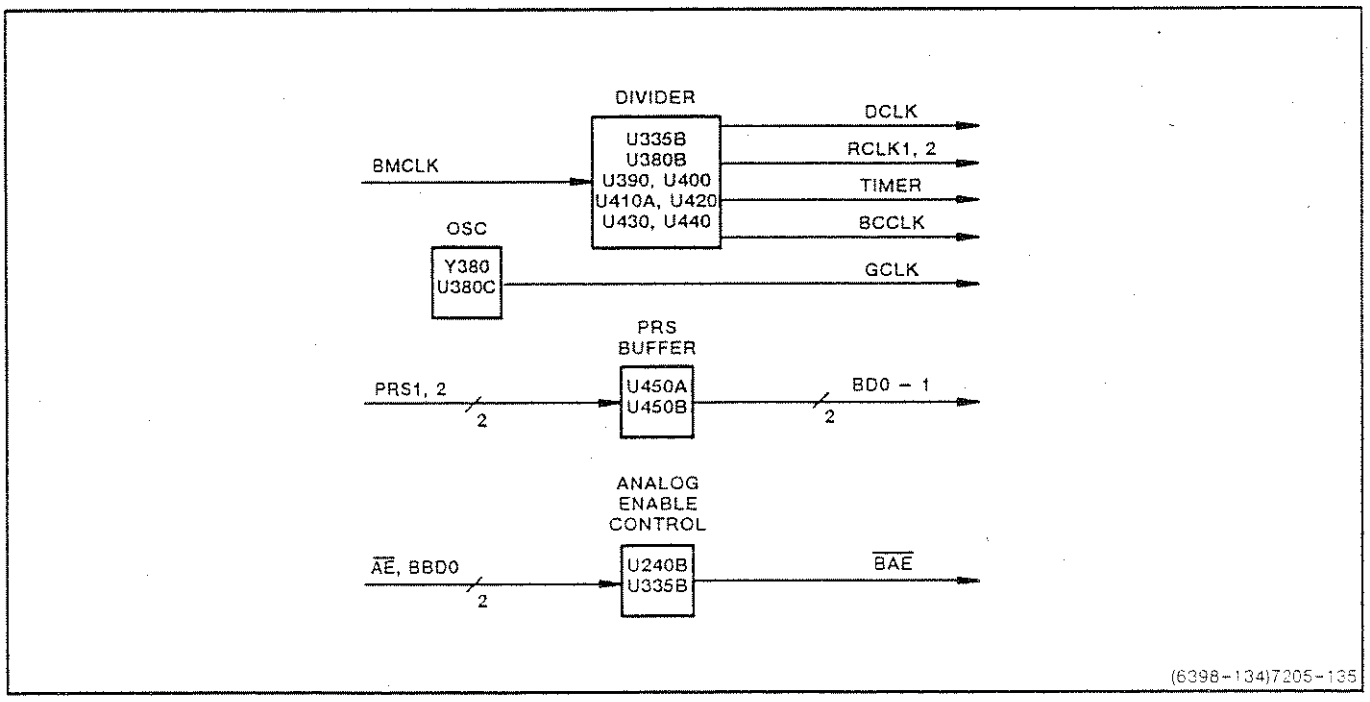


Fig. 1-79 Dot Clock and Timer Block Diagram

Divider

The divider (U380B, U390, U400, U410A, U420, U430, and U440) divides the 8 MHz BMCLK clock pulses into several different clock rates.

The BMCLK pulse from the MPU is divided by U390 and selected by U410A as a 1.6 MHz DCLK clock signal for reading data from the A54 Display Control board display RAM to the Monitor Out terminal.

The output of U390-11 (RCLK2) and the output of U400B-13 (RCLK1) are clock pulses for sensing the variation in the angle of rotation of the parameter entry knob on the front panel.

Two clocks provided through dividers U420, U430, and U440 are the 50 Hz timer clock signal (TIMER) for generating the hardware timer interrupt, and a 1 kHz clock signal (BCCLK) for generating the probe calibration signal and the gain calibration reference signal.

Oscillator

Oscillator Y380 is a 5 MHz oscillator buffered through U380C to produce the GCLK clock signal for the TMS9914A GPIB adaptor on the A56 GPIB/Monitor Board.

PRS Buffer

The PRS buffers (U450A and U450B) sense whether the probe connected to the input BNC connector is X1 or X10. The MPU reads data from these buffers at 300 ms intervals to control the input range indicator on the front panel.

Analog Enable Control

The analog section of the MPU bus is buffered at its entrance to the Trigger board to create a silent bus. The analog enable control circuit (U290B) controls the $\overline{BAE}$ (buffered analog enable) signal that controls this buffer. $\overline{BAE}$ is set high to disable the buffer when the MPU is not accessing the analog section. This separates it from the MPU bus reducing the effect of noise in the analog section.

ADDRESS MULTIPLEXER (DIAGRAM 51)

The address multiplexer (Figure 1-80) controls the addresses assigned to the display RAM. It consists of buffers, an H scroll register file, an adder, and address multiplexer circuits.

Buffers

Buffers U100 and U110 are address bus buffers; buffers U180, U190, U230, and U240 are data bus buffers. Buffer outputs BBD0-BBD15 are supplied to the Display board registers; outputs from U230 and U240 are supplied to the data bus and display RAM input/output pins. Data bus buffers are separated to enable the MPU to perform operations on the registers while continuously transferring display memory data to the monitor.

H Scroll Register File

The H scroll register file (U120, U130, and U140) provides for horizontal scrolling. Each register has a 4-bit X 4-address structure, with two of the four addresses being used for Channel 1 and 2 horizontal scrolling. Read and write operations can be per-

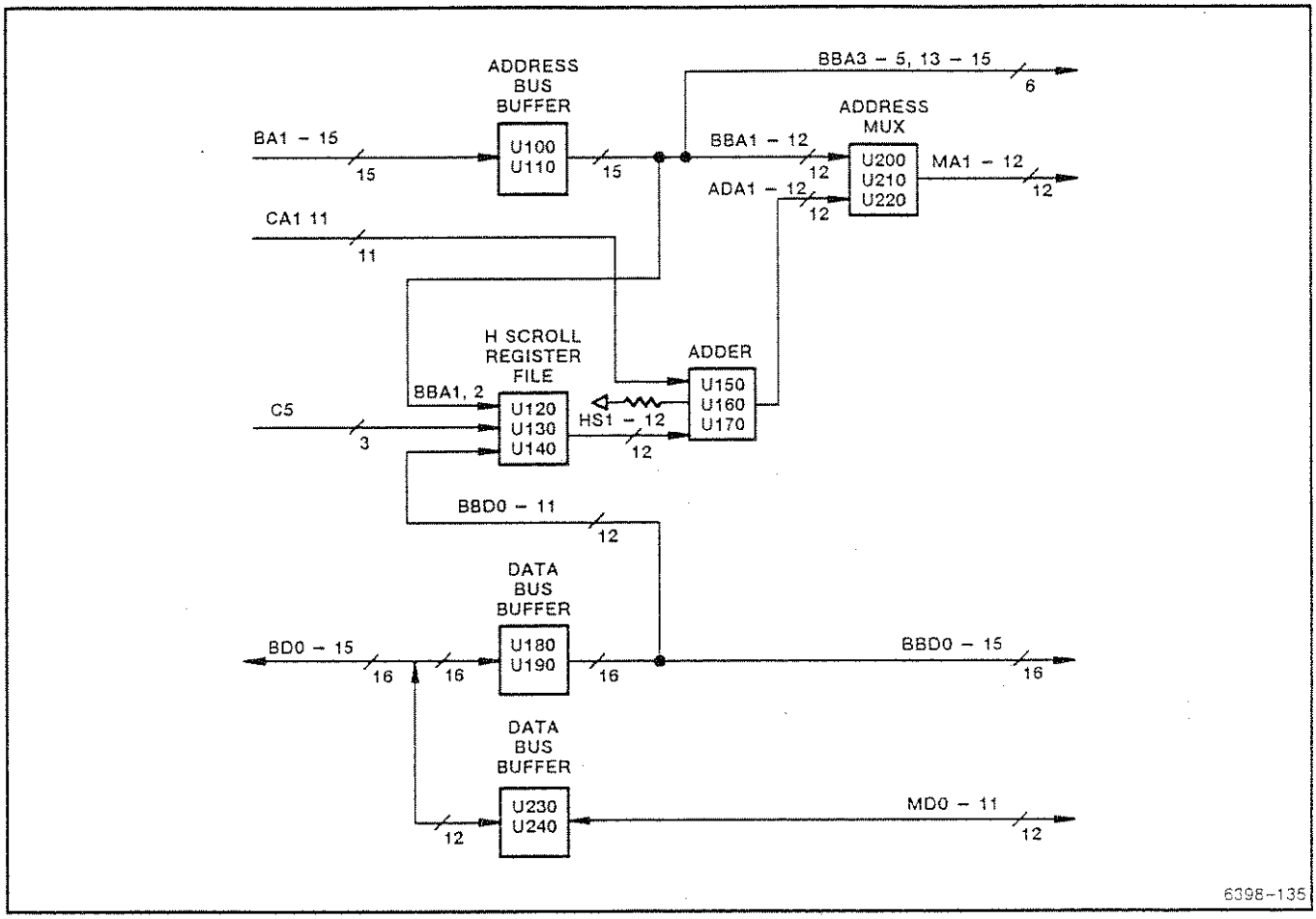


Fig. 1-80 Address Multiplexer Block Diagram

formed on these registers at any time. Thus, the MPU can write to the registers, and at the same time readout their contents to the monitor. During write operations, the GW pin is set low, and WA and WB are decoded to select the register for writing data. During read operations, GR is set low and readout is performed in the same way. The contents of this register are continuously updated to cause scrolling.

Adder

Adders U150, U160, and U170 form a 12-bit adder that modifies the display RAM address during operation of the horizontal scroll function. The read counter output (CA1-CA11) provides the display RAM address when the contents of the display RAM are being output to the monitor. The H scroll register file outputs (HS1-HS12) are changed to vary the position of the window for reading data from the display RAM.

Address Multiplexer

Address multiplexers U200, U210, and U220 form a 12-bit address multiplexer for selecting addresses from the display RAM. Either adder output ADA1-ADA12, or MPU address bits BBA1-BBA12, are input to the multiplexer. When the MPU accesses the display RAM, address bits BBA1-BBA12 are output; when the contents of the display RAM are output to the monitor, adder output ADA1-ADA12 are output.

ADDRESS GENERATOR (DIAGRAM 52)

The address generator (Figure 1-81) generates the display RAM address when the contents of the display memory are being output to the monitor. It consists of a read counter run/stop, a read counter, and blank control circuits.

Read Counter Run/Stop

The read counter run/stop circuit (U270B, U290, U300A, U300B, U300D, U310B, and U320A) controls a read counter to ensure a stable monitor display control regardless of the timing that the MPU uses to access the display RAM.

The DCLK clock signal (1.6 MHz) is divided by 2 by U290. When the $\overline{CST}$ signal from the blank control register (refer to schematic 55) becomes low, U290 output is fixed either high or low. When the MPU accesses the display RAM, $\overline{CST}$ is set low, stopping the clock input to the read counter. When access is completed, $\overline{CST}$ is set high, and the clock is again applied to the read counter. These operations ensure a stable monitor display, no matter when the MPU accesses the display RAM. The clock is divided to 800 kHz by U290 and to 400 kHz by U320A, then applied to the read counter.

When the trigger point or cursor is displayed on the monitor, TP or CSOR goes low causing U270B-9 or U270B-13 to become low. When retrace blanking (refer to the section on blank control below) is being performed, U270B-12 becomes low. This causes the U320A Q output to be fixed at high or low, thus stopping the read counter.

The timing pulse for latching data from the display RAM (DLP) is output by U310B.

Read Counter

The 11-bit read counter (U340, U350, and U360) generates the address for the display RAM location whose contents are to be output to the monitor. This counter upcounts from 0 to 2047 repeatedly, addressing 2K words of the 4K words of the display RAM. CA11 is the carry signal.

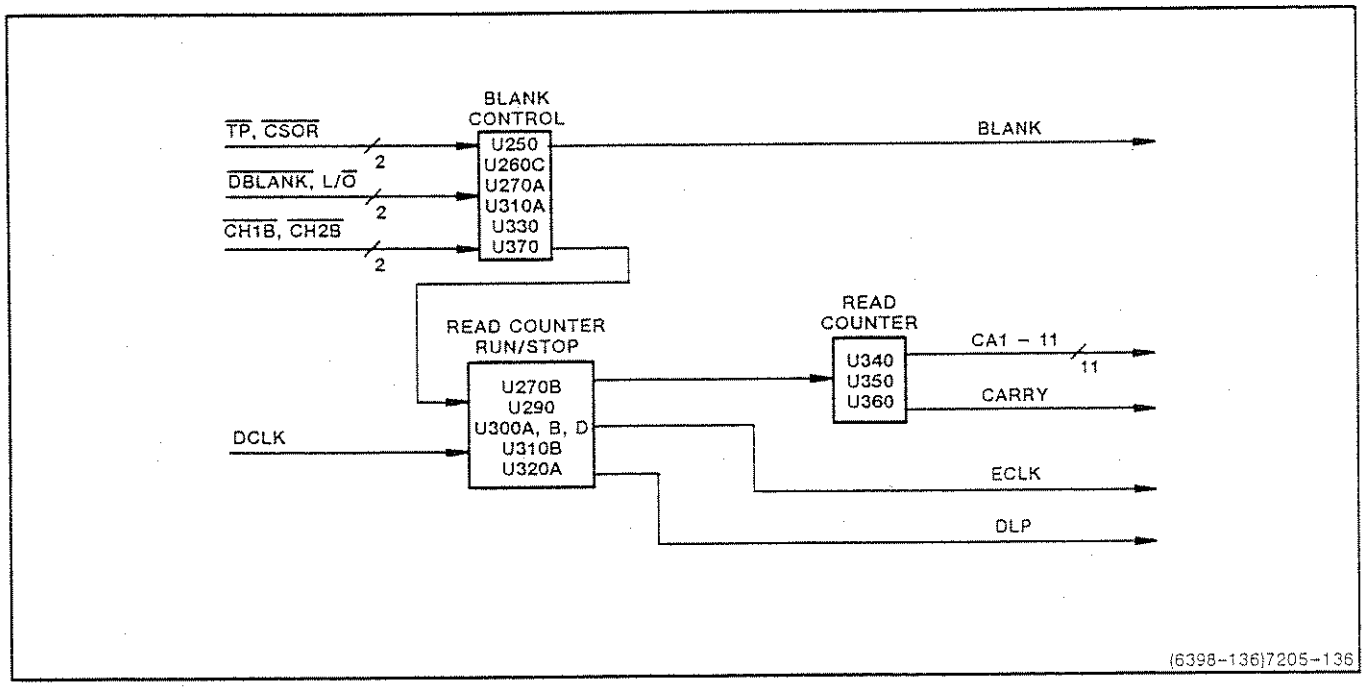


Fig. 1-81 Address Generator Block Diagram

Blank Control

Blank control U370 is a one-shot multivibrator that generates the pulse to blank the space between dots on the monitor. Gate U250C establishes whether or not this pulse is enabled. If the DOT/LINE key on the front panel is switched to DOT, L/$\overline{D}$ is low and the pulse is transmitted; if LINE is selected, L/$\overline{D}$ and the output of U250C is high, keeping the pulse from being transmitted (blanking doesn't occur).

When 2K words of display RAM data have been accessed, the read counter carry signal becomes low causing U310A to become low, which generates a pulse from one-shot multivibrator U330. This pulse provides retrace blanking while the electron beam returns to the left edge of the monitor.

These two blanking pulses and $\overline{DBLANK}$ and $\overline{CST}$ are logically summed by U270A. $\overline{DBLANK}$ blanks single-dot units on the monitor; $\overline{CST}$ generates a blanking signal to prevent scattering when the MPU is accessing the display RAM. U250A, U250B, U250D, and U260C blank data displayed on the monitor screen from either Channel 1, Channel 2, or both. When Channel 1 (or Channel 2) is blanked, $\overline{CH1B}$ (or $\overline{CH2B}$) becomes low; while the contents of the Channel 1 (or Channel 2) display RAM are read, $\overline{CH1CS}$ ($\overline{CH2CS}$) becomes low and blanking is performed. The timing for blanking signals sent to the monitor are shown in Figure 1-82.

DISPLAY RAM CHIP SELECT (DIAGRAM 53)

The display RAM chip select circuit (Figure 1-83) generates chip select signals for the display RAM. It consists of a carry counter, a display Channel set, a comparator, an address decoder, and mode control circuits.

Carry Counter

Carry counter U300E, U380, U410, U500B, and U530C counts the carry output from the read counter. Each time 2K words of display RAM are read out, it increments. For example, if U380-2 and U380-5 are both set to 0, the U410 output repeats the hexadecimal sequence C, D, E, F.

Display Channel Set

Registers U420 and U430 select the display RAM channel for output. The lower byte is stored in U420 and the upper byte in U430, but only one at a time cannot be accessed. They are word accessed.

Comparator

Comparator U450-U480 compares the display channel set outputs (U420 and U430) with the carry counter output (U410) in 4-bit units. For example, if U380-2 and U380-5 are set to 0 and 1, respectively, and if U420 and U430 are set to 0F0E, (because the output from U410 is E) a high is output from U450. Then, $\overline{CH1CS}$ from gate U495A becomes low causing Channel 1 display RAM data to be output to the monitor.

When a carry is output after 2K words of Channel 1 display RAM are read out, U410 output becomes F and U470 output becomes high. Then $\overline{CH2CS}$ becomes low causing Channel 2 display RAM data to be output to the monitor. When 2K words have been read, another carry is output and the output of U410 becomes E. This sequence is repeated to display Channel 1 and 2 data on the monitor.

Comparators U460 and U480 are used in the envelope mode. When their outputs become high, the outputs of U490A and U500A become high causing the order of the data being read out of the display RAM to be reversed. At this point, the cursor dis-

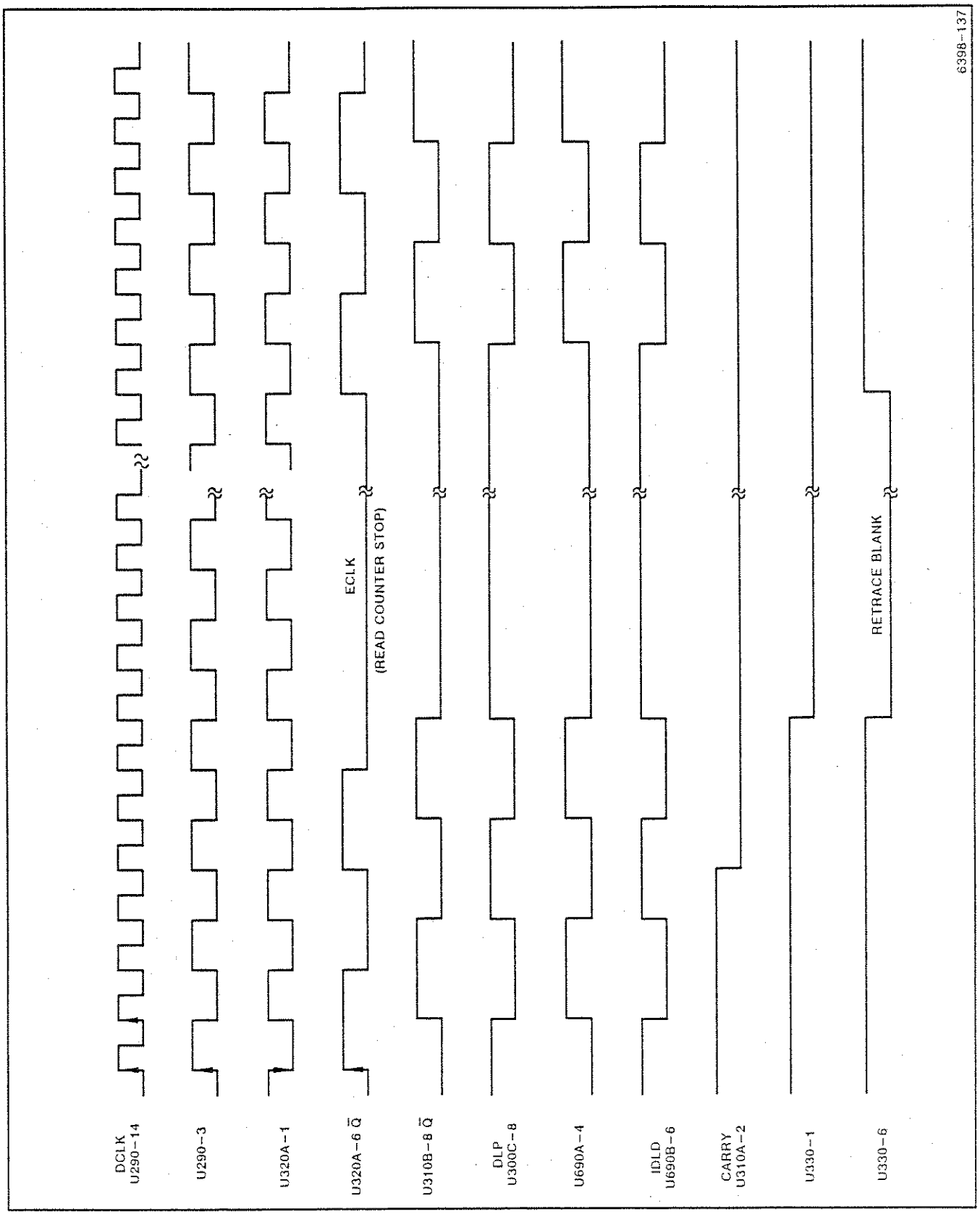


Fig. 1-82 Display Control Timing and Blanking Diagram

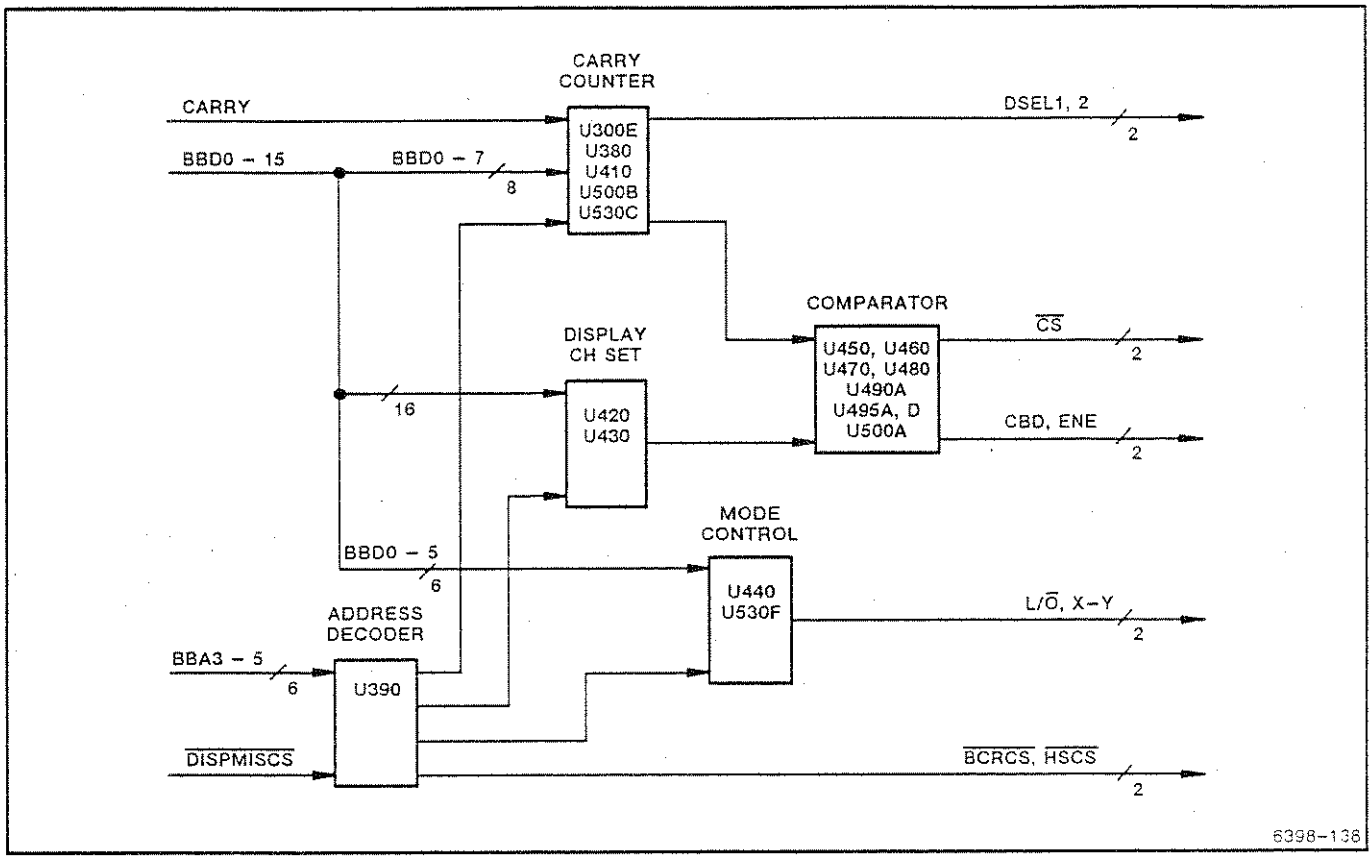


Fig. 1-83 Display RAM Chip Select Block Diagram

play is disabled (CSD). Thus, envelope waveforms are displayed by repeatedly setting U450, U460, U470 and U480 outputs high.

Address Decoder

Address decoder U390 decodes the $\overline{\text{DISPMISCS}}$ signal from the DMA board to generate chip select signals as follows: $\overline{\text{BCRCS}}$ is the blank control register chip select signal (refer to schematic 55), and $\overline{\text{HSCS}}$ is the horizontal scroll register chip select signal.

Mode Control

Mode control U440 controls the line/dot and Y-T/X-Y displays. When U440-5 is high, line display is selected; when low, dot display is selected. When U440-2 is low, Y-T display is selected; when high, X-Y display is selected.

DISPLAY RAM (DIAGRAM 54)

Display RAM (Figure 1-84) stores data to be displayed on the monitor. It consists of display RAM, memory access control, and scroll register chip select circuits.

Display RAM

RAMs U540, U550, and U560 comprise the Channel 1 display RAM; RAMs U570, U580, and U590 comprise the Channel 2 display RAM. Each section has a 4K word X 12-bit structure, of which 10 bits are display data from waveform memory and two bits are attribute bits. These two attribute bits determine whether dot unit normal display, blank, TP (trigger point, break point) display, or cursor display is selected. 2K words of the 4K words are output and displayed on the monitor.

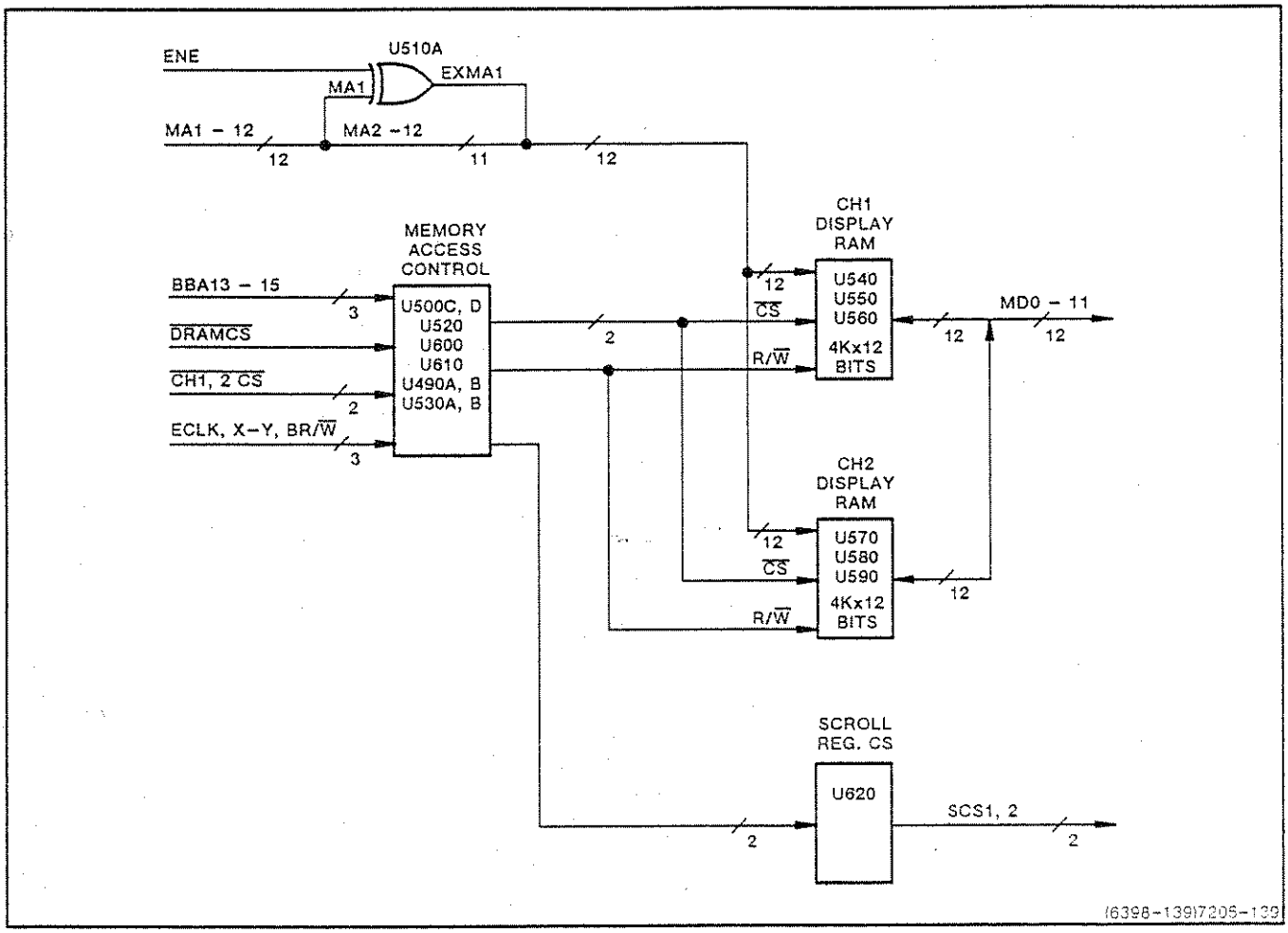


Fig. 1-84 Display RAM Block Diagram

Gate U510A inverts the MA1 signal during envelope waveform display. In envelope display, when the first 2K words of data are read out, the ENE signal is low causing the EXMA1 and MA1 signals the same. Thus, data is read out in order from locations 0, 1, 2 ... 2047. At the second data readout, ENE becomes high and MA1 is inverted to become EXMA1. Thus, data is read out from locations 1, 0, 3, 2 ... 2046. Subsequent data is read out in the same repeated sequences.

Memory Access Control

The memory access control circuits (U490A, U490B, U500C, U500D, U520, U530A, U530B, U600, and U610) control the display RAM chip select signals. Address decoder U520 is used when the MPU accesses the Channel 1 or Channel 2 display RAM. Logic circuitry U600 and U610 select whether data is sent to the monitor from Channel 1 or 2, or whether the display RAM is accessed by read counter or the MPU is performing a read/write operation.

When data is read out using addresses from the read counter, and $\overline{CH1CS}$ ($\overline{CH2CS}$) becomes low, U600A-1 (U600B-13) becomes low.

In the Y-T mode, the X-Y signal is low, thus U600A-2 (U600B-2) becomes low causing the output of U600A (U600B) to become low. When U600C-4 (U600D-10) becomes low with U600C-5 (U600D-9) low, the output of U610C (U610D) becomes low causing the Channel 1 (Channel 2) display RAM chip select signal to become low.

If the MPU does not access the display RAM, $\overline{DRAMCS}$ is high making U600C-5 and U600D-9 low. At this point, U520-14 and U520-15 are high, making the output of U500C high causing the output of U490B ($\overline{WE}$) for Channel 1 (Channel 2) to become

high. Thus the read counter address has selected Channel 1 (Channel 2) data for read out.

When the MPU accesses the Channel 1 (Channel 2) display RAM, $\overline{\text{DRAMCS}}$ becomes low making the output of U600C (U600D) high. Next, U520-15 (U520-14) becomes low making the output of U610C (U610D) low, causing the chip select to become low. With the output of U500C low, the BR/$\overline{\text{W}}$ signal is supplied. Thus, the MPU can read or write to the Channel 1 (Channel 2) display RAM.

In the X-Y mode, the X-Y signal becomes high. Channel 2 data is read out when the ECLK signal is high; Channel 1 data is read out when it is low. The read counter upcounts on the rising edge of the ECLK signal, which updates the display RAM address. This allows X-Y mode data to be read from the same addresses in Channel 1 and Channel 2.

Scroll Register Chip Select

The scroll register chip select circuit (U620) outputs the the chip select signals (SCS1 and SCS2) that address the horizontal scroll register file. These two signals enable selection of two of the four register file addresses. When data from the Channel 1 display RAM is output to the monitor, $\overline{\text{CH1CS}}$ is low and $\overline{\text{CH2CS}}$ is high, thus SCS1 and SCS2 both become 0. When data from the Channel 2 display RAM is output to the monitor, $\overline{\text{CH1CS}}$ is high and $\overline{\text{CH2CS}}$ is low, thus SCS1 and SCS2 become 0 and 1, respectively.

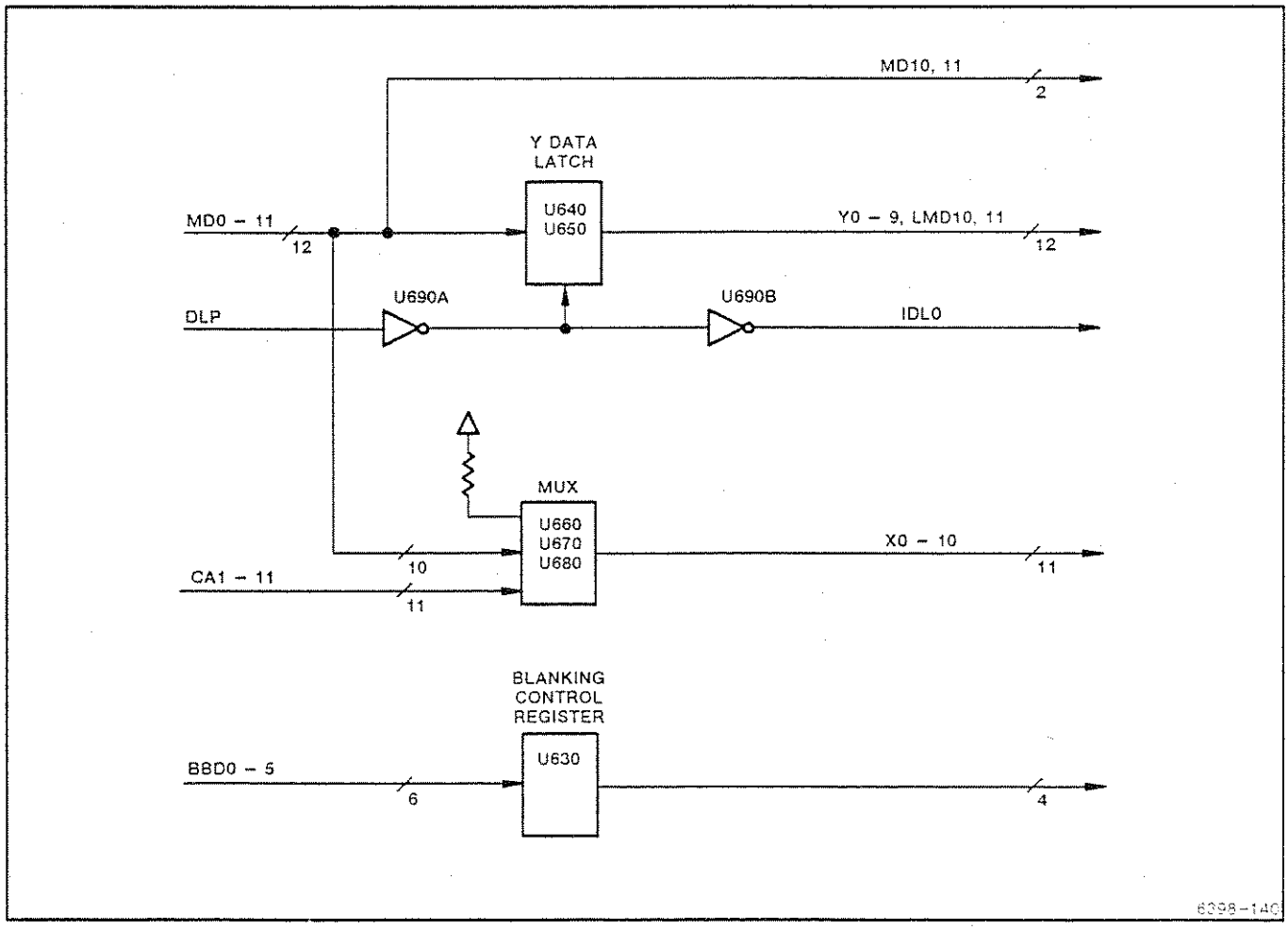


Fig. 1-85 Display Data Output Block Diagram

DISPLAY DATA OUTPUT (DIAGRAM 55)

The display data output circuit (Figure 1-85) outputs digital data to the D/A converter on the A56 GPIB/Monitor Board. It consists of the Y data latch, a multiplexter, and blank control register circuits.

Y Data Latch

Y data latch U640 and U650 latches data from the display RAM for output to the monitor. In X-Y mode, the Channel 2 display output (Y output) is latched and has its timing adjusted to the Channel 1 display RAM output (X output).

Multiplexer

Multiplexer U660, U670, and U680 selects either read counter output (X output to the monitor), or display RAM output. In the X-Y mode, $\overline{\text{X-Y}}$ is set low, thus outputs MD0-MD9 from the display RAM are output to lines X0 to X10 (lines X1-X10 correspond to bits MD0-MD9; U660-2 low input is output to X0). In the Y-T mode, X-Y becomes high, and CA1-CA11 are output to lines X0-X10.

Blank Control Register

Blank control register U630 controls monitor blanking. $\overline{\text{CH1B}}$ blanks the Channel 1 display; $\overline{\text{CH2B}}$ blanks the Channel 2 display. $\overline{\text{CST}}$ controls the read counter run/stop; it blanks the display when stop is selected. $\overline{\text{CRST}}$ resets the read counter.

CURSOR AND TRIGGER POINT CONTROL (DIAGRAM 56)

The cursor and trigger point control circuit (Figure 1-86) generates the pulses for the cursor and trigger point display. It consists of a cursor and trigger point generator, an address decoder, TR control, and GPIB address buffer circuits.

Cursor and Trigger Point Generator

The cursor and trigger point generator circuitry (U100B, U100C, U100D, U100E, U110, U120, U130A, U130B, U140, and U150) generates the pulses for displaying the cursor and the trigger point. When the bit pattern of the upper two bits of the display RAM (D11 and D10) is binary 01, the cursor is generated; when they are binary 10, the trigger point (including the breakpoint) is generated.

In the X-Y mode ($\overline{\text{X-Y}}$ low), if MD11 and MD10 are binary 1 and 0 (0 and 1), respectively, then the output of gate U130B (U130A) becomes high. Thus, the output of U110D (U110C) becomes low, and on the rising edge of the DLP signal from the A54 Display Control board, the negative pulse $\overline{\text{TP}}$ ($\overline{\text{CSOR}}$) from one-shot U150B (U150A) multiplexes.

In the Y-T mode, when LMD 11 and LMD 10 are 1 and 0 (0 and 1), the output of U120B (U120A) becomes high. At this point, the output of U120D (output of U120C) becomes low, and the $\overline{\text{TP}}$ ($\overline{\text{CSOR}}$) negative pulse is output. The read counter stops during this negative pulse, but output to the monitor does not change. Thus, the monitor electron beam stops moving, and brightness increases to generate a cursor or trigger point dot.

Address Decoder

Address decoder U160 provides access to the registers on the GPIB/Monitor Board (refer to schematic 57).

The chip select signal $\overline{\text{CLRE}}$ reads the checksum adder (refer to schematic 57). The chip select signal $\overline{\text{CLRE}}$ clears the adder, while the chip select signal $\overline{\text{WTE}}$ writes to the adder. The chip select signal $\overline{\text{RESEL}}$ reads out data from the counter that senses the changes in the angle of rotation of the parameter entry knob on the front panel.

TR Control (GPIB)

TR control U230A controls the TR signal output sent from the TMS9914A GPIB adaptor to the time base. When the TRE (trigger enable) output of U230A is high, the TR signal is sent to the time base as the trigger signal from the GPIB.

GPIB Address Buffer

GPIB address buffers U180 and U190 read the GPIB address switch settings from the rear panel. The MPU reads the contents of this buffer at 300 ms intervals. The TR input from the GPIB adaptor is used during power-up diagnostics: when the *fget* command (force group execute trigger) is set in the GPIB adaptor TMS9914A general-purpose command register. TR becomes high to indicate that the TMS9914A is operating correctly.

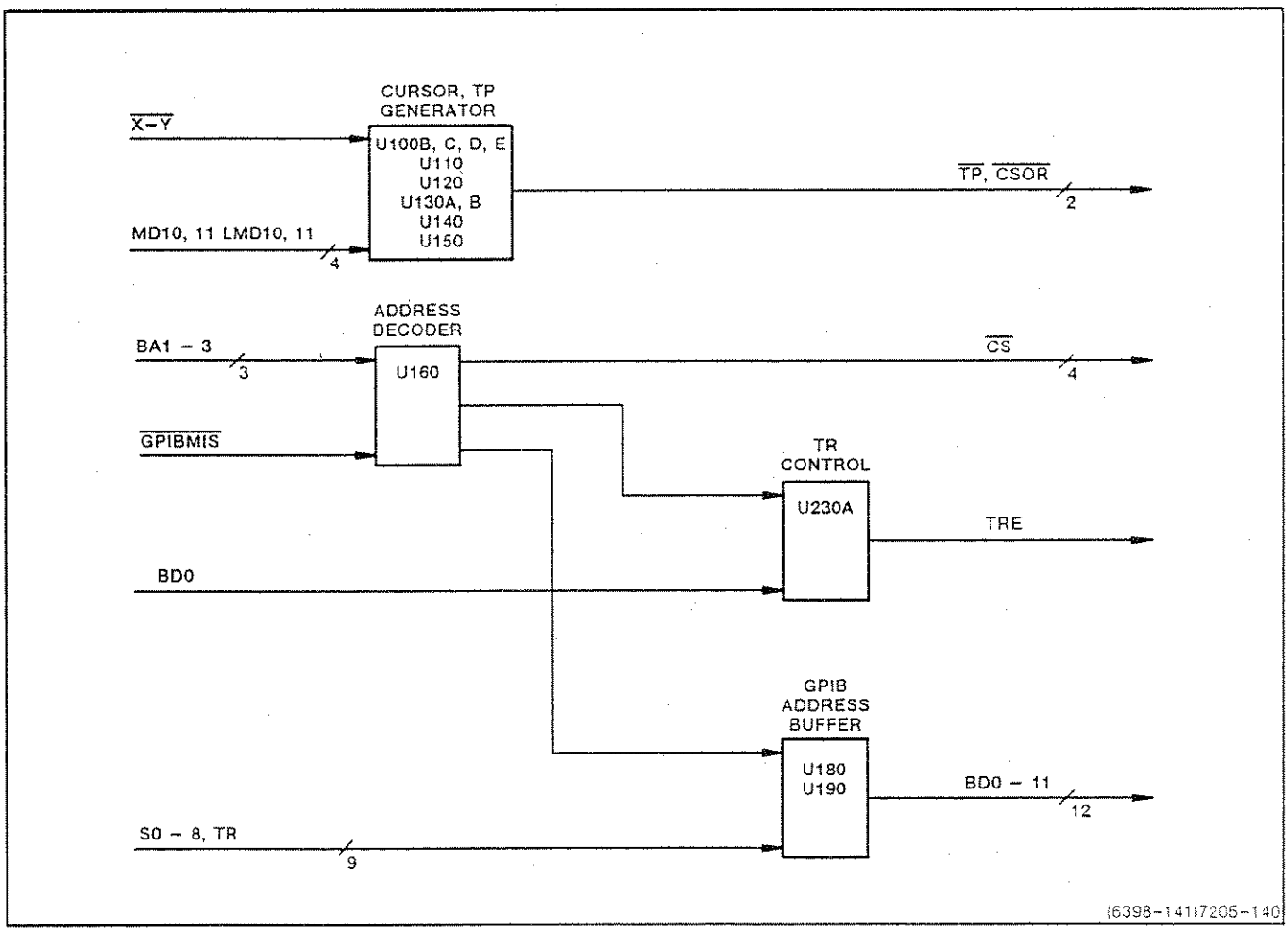


Fig. 1-86 Cursor and Trigger Point Control Block Diagram

GPIB (DIAGRAM 57)

The GPIB circuit (Figure 1-87) controls the transfer of data and commands over the GPIB. It consists of an adder, a read/write pulse generator, a buffer, a GPIB adaptor, and TR control circuits.

Adder

8-bit adder U210, U240, U250, and U260 computes the checksum data during GPIB data transfers. A data transfer is initiated when U260 is cleared and the first data (BD0-BD7) is added to 0 by U240 and U250, and latched into U260. Next, the second batch of data (BD0-BD7) is added to the latched data (LED0-LED7), and the lower eight bits, excluding any carry bit, are again latched into U260. These operations are repeated during data transfer.

When data is sent over the GPIB, checksum data in U260 is sent at the completion of the transfer. When data is received over the GPIB, the checksum received in U260 is compared with the checksum of the actual data received to determine if the received data is the same as that sent.

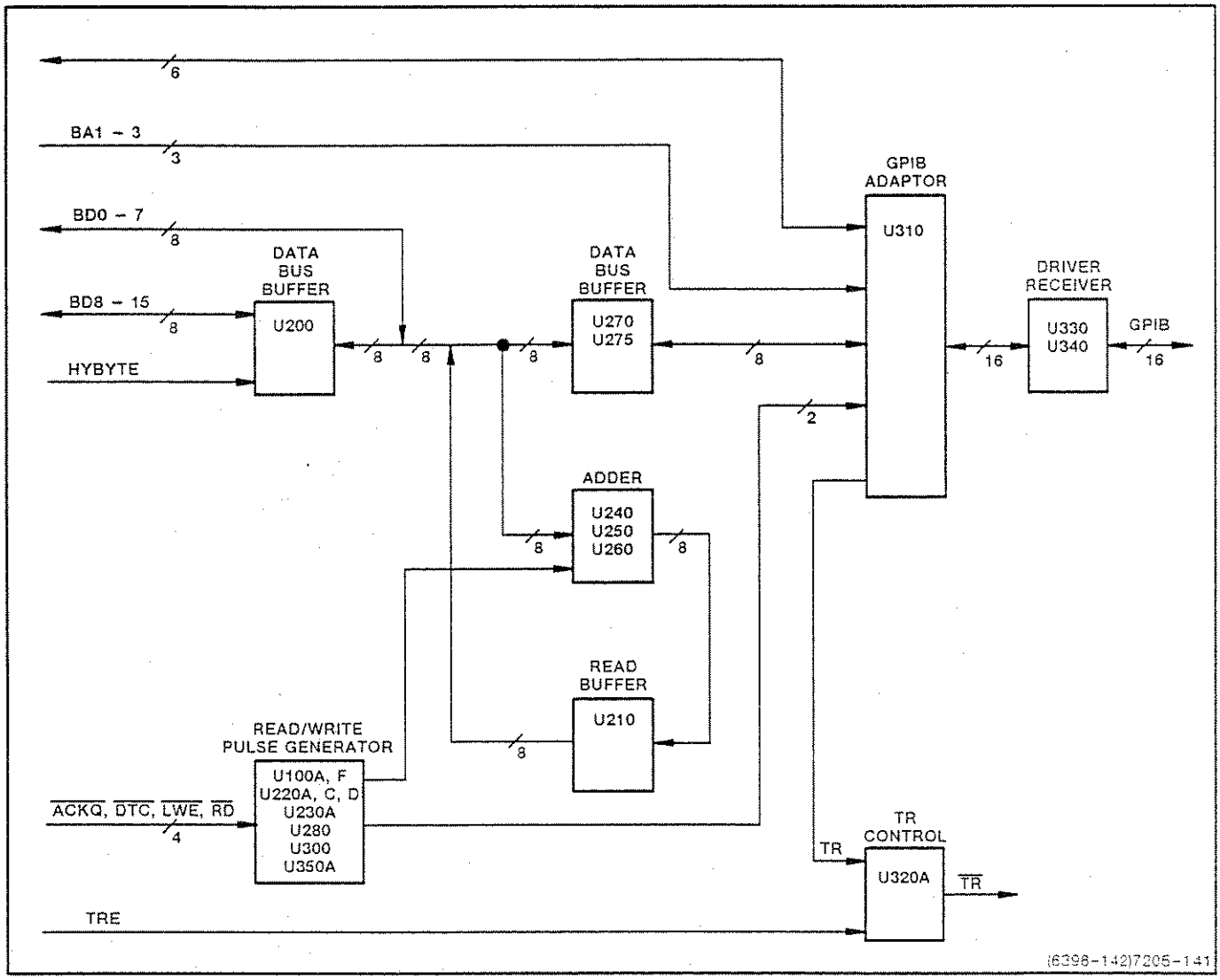


Fig. 1-87 GPIB Block Diagram

Read/Write Pulse Generator

The read/write pulse generator (U100A, U100F, U220A, U220C, U220D, U230A, U280, U300, and U350A) generates the adder latch timing pulse and the TMS9914A GPIB adaptor read/write timing pulse used during GPIB data transfers using the DMAC and handshaking with the TMS9914A. When the MPU reads or writes to the TMS9914A internal register, the LRD or $\overline{LWE}$ signal selected by U300 is used. When the DMAC performs an access operation, the $\overline{BGACK}$ signal is set low, and U300A and U300C are enabled. When the MPU accesses the internal register, $\overline{BGACK}$ is high and U300B and U300D are enabled.

When data is transferred using the DMAC and TMS9914A, a low is output at the TMS9914A $\overline{ACCRQ}$ pin. Signal $\overline{REQ0}$ becomes low to indicate the DMAC has received a DMA transfer request, thus $\overline{ACK0}$ is set low and input to the TMS9914A $\overline{ACCGR}$ pin.

When data is being written to the TMS9914A internal register, U100A output becomes high on the low transition of the $\overline{ACQ0}$ signal. Then on its rising edge, the outputs of flip-flops U230A and U280A are both driven low. When the DMAC BR/$\overline{W}$ signal is high and U280B-10 is low, the output of U280B becomes low. This causes the TMS9914A signal $\overline{WE}$ and the adder U260 clock input pin low. If the data is valid, the $\overline{DTC}$ signal from the DMAC becomes low causing the U230A output and the $\overline{WE}$ signal to become high, thus writing data and latching adder data.

When data is being read from the TMS9914A, both BR/$\overline{W}$ and $\overline{ACK0}$ are low causing the output of U280C to become low. This causes DBIN low and data is output. When a DMA transfer is performed using the $\overline{ACCRQ}$ and $\overline{ACCGR}$ signals, data is read when DBIN is low. $\overline{DTC}$ is also low, thus the U260 clock input pin becomes low. When the data transfer is completed, $\overline{DTC}$ becomes high, and the added data is latched. $\overline{REQ0}$, $\overline{ACQ0}$, and $\overline{DTC}$ are handshaked every time one data transfer is performed.

Buffer

Buffers U200, U270, and U275 provide buffering of bus data. U200 controls whether the upper or lower eight bits of the 16-bit bus are connected to the TMS9914A data bus. When the DMAC is used for data transfer between waveform memory and the TMS9914A, switching must be performed at every data byte transferred because waveform memory is 16 bits, while the TMS9914A is only eight bits.

When the DMAC is transferring the upper byte (BD8-BD15), the lower byte (BD0-BD7) is switched to the high impedance state, and $\overline{HIBYTE}$ becomes low, enabling U200. $\overline{ACK0}$ also goes low, enabling U275, and BD8-BD15 are connected to GD0-GD7. To transfer the lower byte (BD0-BD7), $\overline{HIBYTE}$ becomes high, disabling U200, ACK0 goes low connecting BD0-BD7 to GD0-GD7.

When the MPU accesses the TMS9914A internal register, only the lower byte is accessed. $\overline{9914CS}$ becomes low, enabling U270, and BD0-BD7 are connected to GD0-GD7.

GPIB Adaptor

The GPIB adapter TMS9914A (U310) has talker, listener, and controller functions, but this instrument utilizes only the talker and listener functions. The MPU data bus uses the internal register to connect with the GPIB.

Bus transceivers U330 and U340 communicate with the GPIB when data is being transferred to and from the waveform memory during a DMA transfer using the $\overline{ACCRQ}$ and $\overline{ACCGR}$ signals. When commands are being exchanged with external devices on the GPIB, a $\overline{GPIBINT}$ signal is output from the $\overline{IRQ}$ pin, an interrupt is issued to the MPU, and handshaking is performed.

TR Control

TR control gage U320A controls the TR signal output from U310. When U320-9 (TR enable) is high, a low $\overline{TR}$ signal is generated and sent to the time base to become the trigger signal. When a DT (device trigger) signal is received form the GPIB controller, the instrument sets U230-9 (TR enable) high. In this condition a *get* (group execute trigger) signal received from the controller, sets U320-9 high causing $\overline{TR}$ to become low, thus enabling application of a trigger from the controller to the instrument.

ANALOG OUT (DIAGRAM 58)

The analog out circuit (Figure 1-88) converts digital signals to analog signals and outpugs them to the monitor. It consists of a latch, a Y analog output, an X analog output, and Z control circuits.

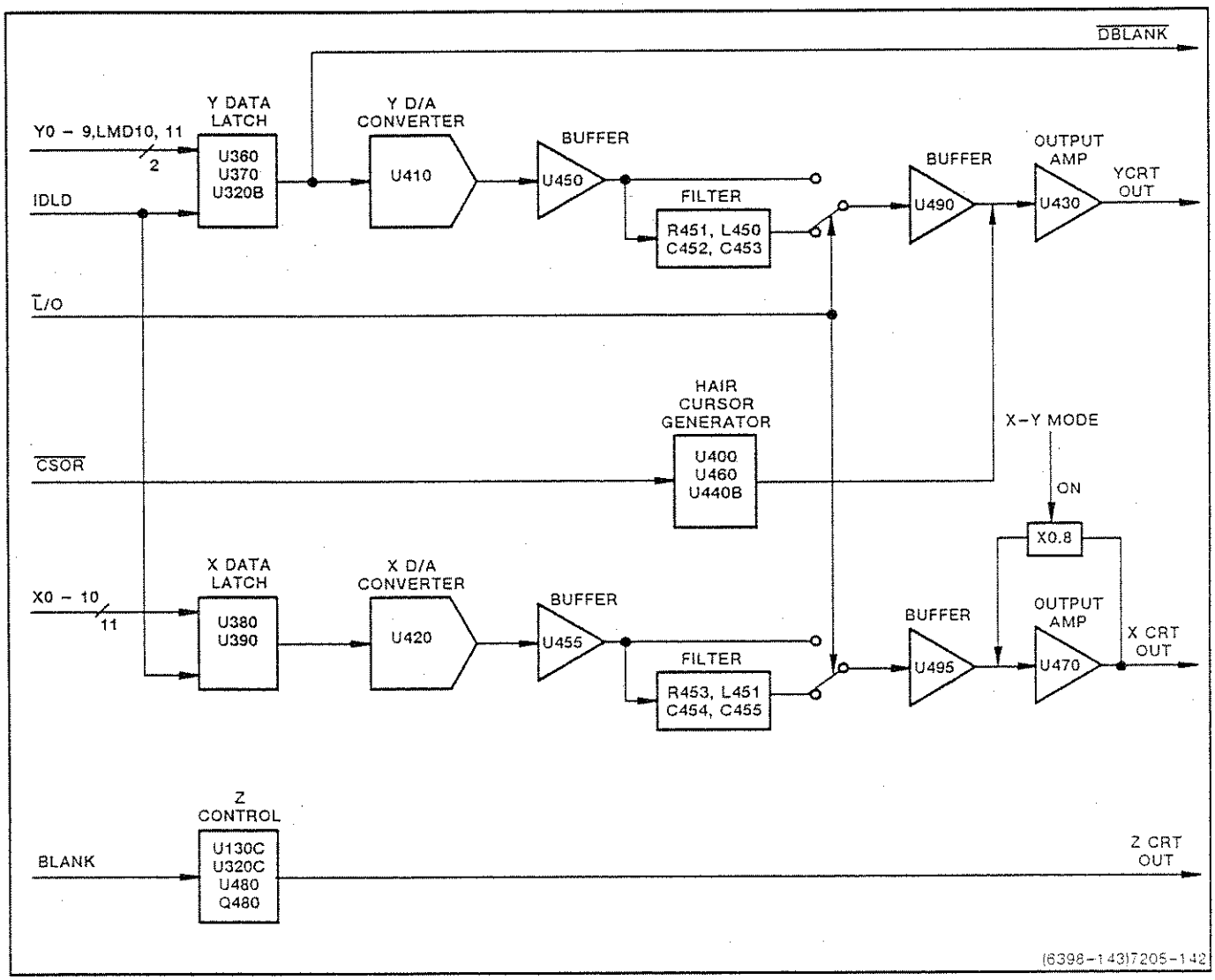


Fig. 1-88 Analog Out Block Diagram

Latch

Latches U360 and U370 latch Y digital data (Y0-Y9); latches U380 and U390 latch X digital data (X0-X10). Both latching operations occur on the rising edge of the IDLD signal. Device U320B generates a $\overline{\text{DBLANK}}$ signal that blanks data when both attribute bits from the display RAM are 1.

Y Analog Output

The Y analog output produces an analog signal from Y digital data and supplies it to the monitor. Data latched by U360 and U370 is converted to analog signals by D/A converter U410. C412 reduces glitches in the D/A converter output. R451, C452, L450, and C453 comprise a filter used in the line display mode to make the lines that connect the dots wider. This has the effect of hiding the dots. In the dot display mode, signals pass through R450 rather than this filter. Switch U440A selects between the line and dot display modes. U440A selects between the line and dot display modes. U450 and U490 form a buffer to separate these circuits before and after the filter. The output from U490 is amplified five times by U430 and its peripheral circuits. The Y level jumper (P430) is used to select the 5 Vp-p or 1 Vp-p signal from J431.

Devices U400, U440B, U460 generate the hair cursor. When $\overline{\text{CSOR}}$ becomes low, a positive pulse is generated by C400, R401, and U400. With U440B-13 and U440B-14 connected together for positive feedback, an oscillation is generated at the output of U460. This is input to U430 to expand its amplitude in the vertical direction and display the hair cursor.

X Analog Output

The X analog output produces an analog signal from X digital data and supplies it to the monitor. Data latched by U380 and U390 is converted to analog signals by D/A converter U420. R453, C454, L451, and C455 comprise a filter used in the line display mode to make the lines that connect the dots wider. This has the effect of hiding the dots. In the dot mode, signals pass through R452 rather than this filter. Switch U440C selects between the line and dot display modes. Buffers U455 and U495 separate these circuits before and after the filter. The output from U495 is amplified five times by U470 and its peripheral circuits. The X level jumper (P470) is used to select the 5 Vp-p or 1 VP-p signal from J471.

In the X-Y mode, B($\overline{\text{X-Y}}$) becomes low, turning on Q471 and driving its collector to +5 V turning on Q470. This changes the output amplifier gain to 5 X 0.8, which reduces the X-axis gain and sets the maximum amplitude for the X and Y axes equal in the X-Y mode.

Z Control

Z control U130C, U320C, U480, and Q480 provides monitor blanking and brightness control. Blanking polarity is selected by Z POL (P480). When a positive blanking signal is selected, the blanking signal is high; for a negative blanking signal, the blanking signal is low. The Z level jumper (P481) selects a 5 Vp-p or 1 Vp-p Z signal from J482.

ROTARY ENCODER (DIAGRAM 59)

The rotary encoder is the interface circuit between the front panel parameter entry knob and the MPU. It consists of an up-down counter and buffer circuits.

Up-Down Counter

The up-down counter (U500, U510, U520A, U530, U540, U560A, and U560B) converts changes in the angle of rotation of the parameter entry knob to changes in the counter. The encoder has two sets of fifty contacts that open or close (ground) the RA or RB signal lines at the input of U560A and U560B as it rotates. These ground-open cycles cause a high-to-low-to-high pulse from U560A and U560B at a 90 degree phase difference between RA and RB. As the encoder is rotated to the right (clockwise), RA advances by 90 degrees; as it rotates to the left, RB advances 90 degrees. This phase lead or lag and number of pulses are counted up and down by U530 and U540.

Buffer

Buffer U550 reads the output of up-down counter U530 and U540, and when the $\overline{\text{RESEL}}$ signal becomes low, the 8-bit counter output (BD0-BD7) is written to the MPU.

PANEL MPU INTERFACE (DIAGRAM 60)

The panel MPU interface (Figure 1-89) provides an interface between the panel control circuitry bus and the MPU bus. It consists of a buffer, an address decoder, and option bit circuits.

Buffer

Buffer U100 buffers address bits BA1-BA5 and signals $\overline{BUDS}$, $\overline{BLDS}$, and BR/$\overline{W}$. The buffered outputs are pulled up by R101 to convert from a TTL to CMOS level. Buffers U130 and U140 are data bus buffers. Their buffered outputs are pulled up by R130 and R140 to convert from a TTL to CMOS level. These buffers are used for MPU data writing to registers on the Board. Buffers U180 and U190 are data bus buffers for reading key sense data.

Address Decoder

The address decoder (U110A, U110B, U120A, U150, U160, U170, and U200) provides chip select signals ($\overline{DR1}$-$\overline{DR4}$) for the 7-segment LED driver ICs. $\overline{MSEL}$ is the chip select signal that sets the 7-segment LED driver mode.

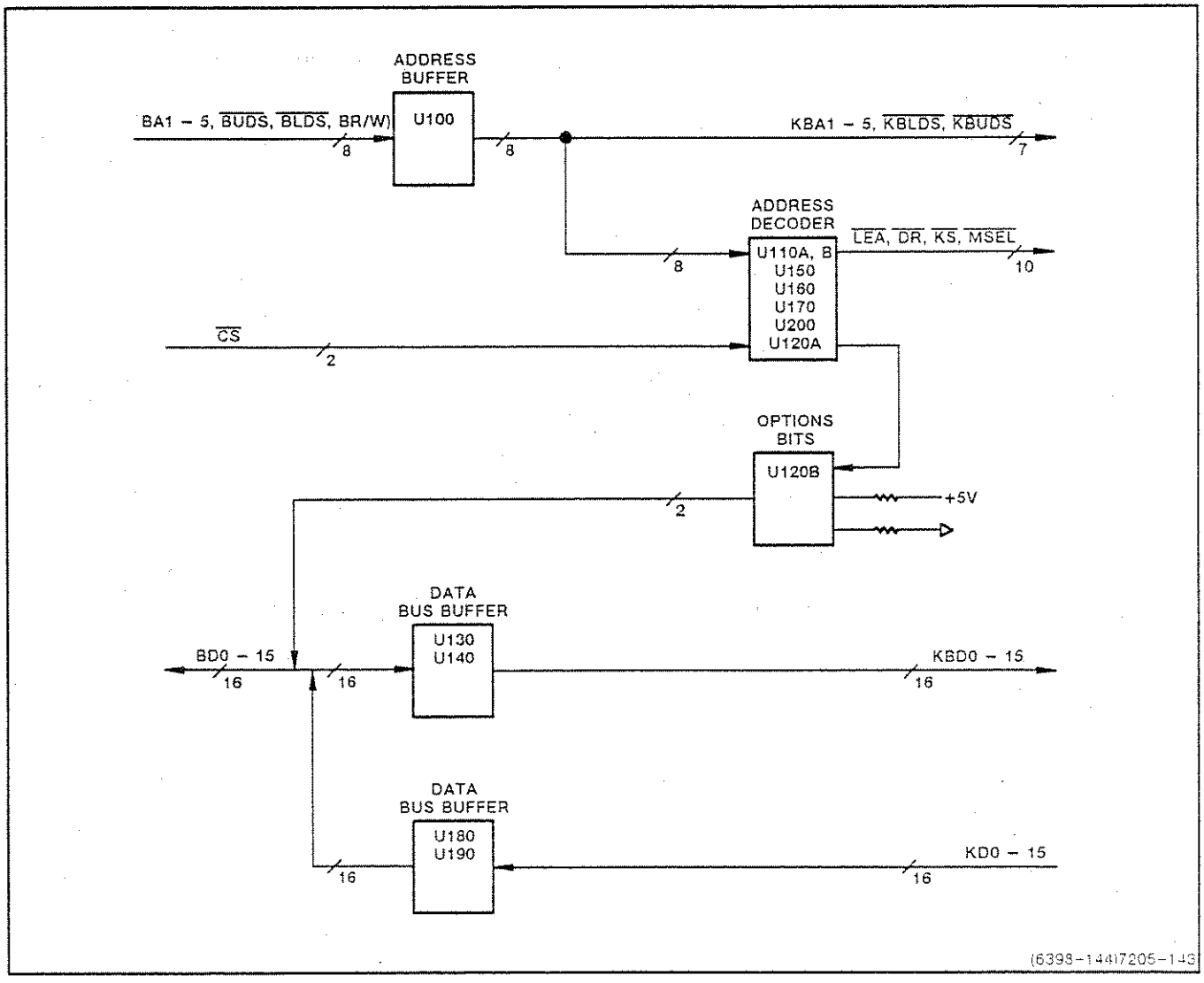


Fig. 1-89 Panel MPU Interface Block Diagram

Signals $\overline{KS1}$-$\overline{KS4}$ are key sense chip select signals, which are simultaneously set low by the MPU on a $\overline{TIMERINT}$ signal. Then, when a key is pressed, $\overline{KS1}$-$\overline{KS4}$ are applied by turns specify the selected key.

The $\overline{KRD}$ and $\overline{LEDCS}$ signals are generated by U110A, U110B, and U120. $\overline{KRD}$ is decoded as the read address (key sense); $\overline{LEDCS}$ is decoded as the write address (LED lighting control).

Option Bit

Buffer U120B reads an option bit to identify whether the Panel Control board (A60) or Indicator board (Option 19; A64) is installed in the instrument. If the Panel Control board is installed, D1 and D0 are 1 and 0, respectively; if the Indicator board is installed, D1 and D0 are 0 and 1.

LED DECODER (DIAGRAM 61)

The LED decoder (Figure 1-90) generates chip select signals to control LED illumination. It consists of an address decoder, a 7-segment LED mode set, an LED driver, a secondary power switch, and rotary encoder circuits.

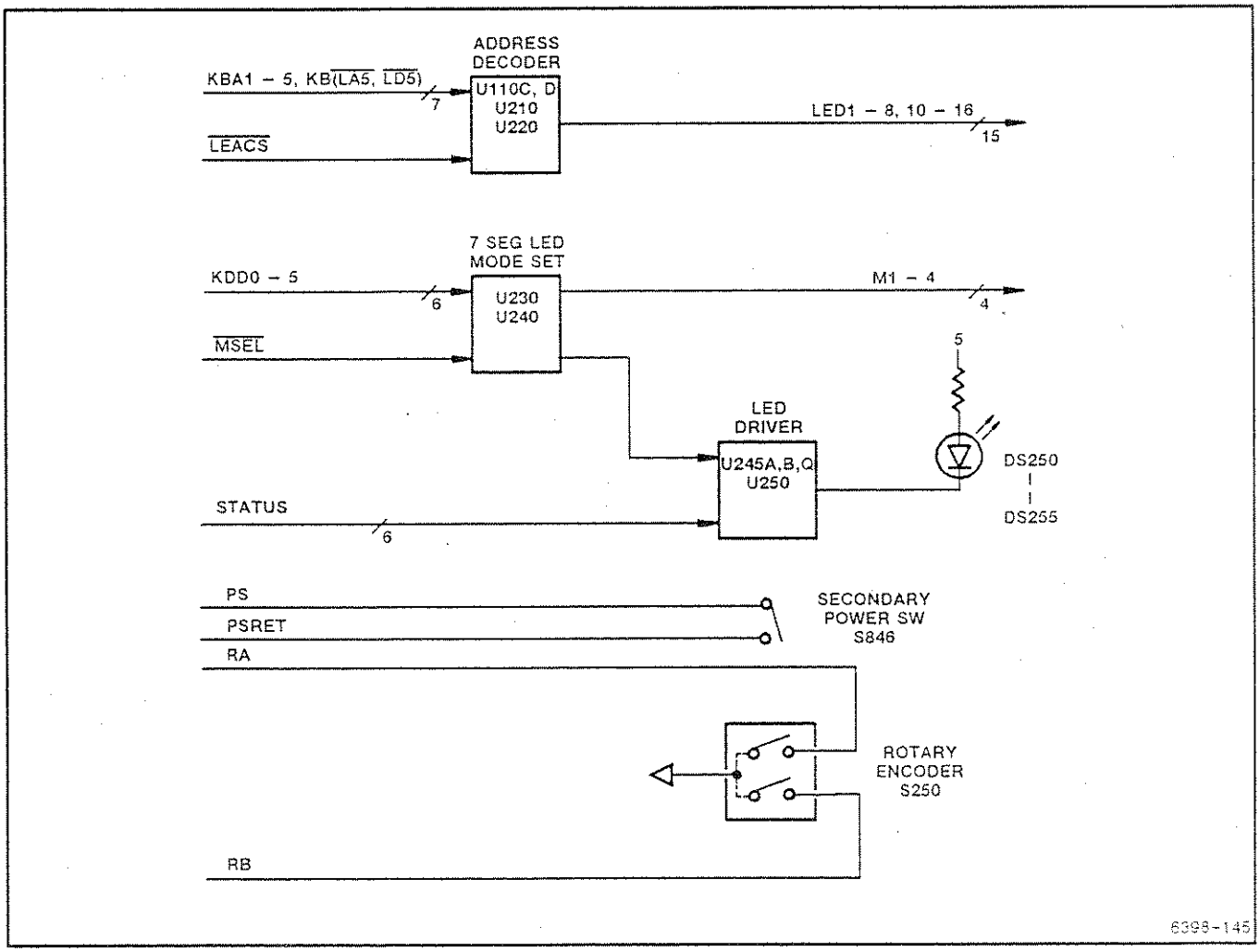


Fig. 1-90 LED Decoder Block Diagram

Address Decoder

Address decoder U110C, U110D, U210 and U220 provides chip select signals to the LED drivers for LED1-LED8 and LED10-LED15 to control illumination.

7-Segment LED Mode Set

The 7-segment LED mode set circuits (U230 and U240) control the M1-M4 signals that set the 7-segment LED display mode. When the U240 enable pins are low, M1-M4 are high and the hexadecimal code (0,1,2,...9,A,B,...F) is selected; when using the U240 enable pins are high M1-M4 become high impedance and code B (0,1,2,...9,...,E,H,L,P,(blank) is selected.

LED Driver

LED driver U250 drives the front panel overflow LED, ARM'D LED, and TRIG'D LED. When the Channel 1 only mode is selected, U245A and U245B disable the Channel 2 overflow LED.

Secondary Power Switch

The secondary power switch S846 on the front panel is connected to the power supply module through the Panel Control board and the Mother board. It turns the power module on and off.

Rotary Encoder

Switch S450 is the rotary encoder.

7-SEGMENT LED (DIAGRAM 62)

The 7-segment LED (Figure 1-91) is a front-panel display. It consists of 7-segment LEDs and their associated drivers and control signals.

7-Seg LED and Driver

Drivers U260, U270, U280, and U290 control the displayed segments of the 7-segment INPUT display LEDs (DS260-DS267), TRIGGER display LEDs (DS270-DS276), TIME BASE display LEDs (DS280-DS282), RECORDING display LEDs (DS277 and DS283-DS287) and CONTROL display LEDs (DS290-DS297).

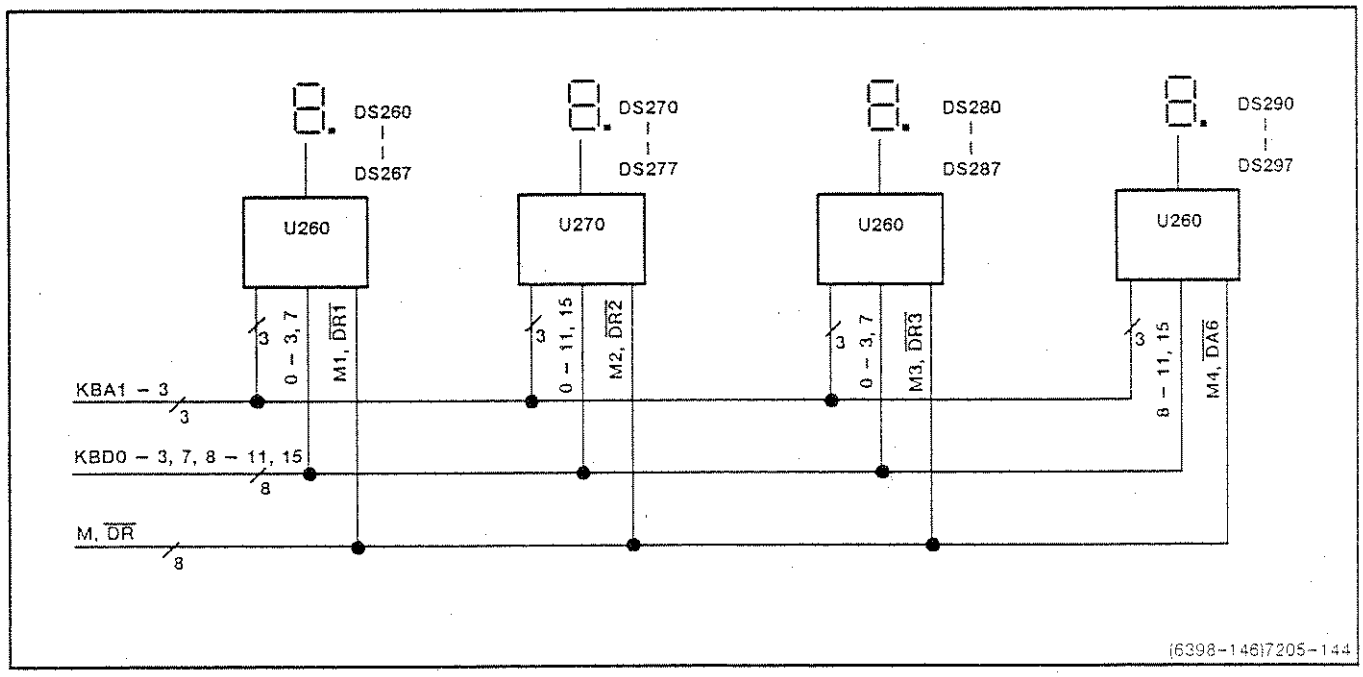


Fig. 1-91 7-Segment LED Block Diagram

LED-1/LED-2 (DIAGRAM 63 & 64)

Drivers U320 through U390 (refer to schematic 63) and U395 through U450 (refer to schematic 64) select the LEDs for illumination.

SWITCH MATRIX (DIAGRAM 65)

Switch matrix S101-S313 are tact switches, and S400-S410 are lever switches for making front panel function selections. The MPU periodically senses whether the switch contacts are shorted (making a selection) or open.

I/O (DIAGRAM 66)

The I/O board contains the interface connectors and wiring from the rear panel GPIB connector J740 to the A56 GPIB/Monitor board. Switch S740 is a DIP switch for setting the GPIB operating parameters and the instrument's GPIB address.

FRONT AND REAR PANEL (DIAGRAM 67)

The front and rear panel Schematic 67 shows the sources and destinations of the signal connectors on the rear panel. It also shows the straight-through front/rear panel connectors (TO FRONT PANEL and FROM REAR). The Probe Cal signal from the A22 TRIGGER Board is output to the front panel PROBE CAL connector through W703 and the voltage limiter mounted inside the front panel.

POWER SUPPLY (DIAGRAM 68 - 72 & 90)

The Power Supply (Figure 1-92) provides nine regulated voltages (+5 V_L, +15 V_L, +59.2 V_L, –5 V_L, –15 V_L, –59.2 V_D, –5 V_D, –2 V_D, and +5 V_D). It consists of the line input, inverter, control, regulator-analog, and regulator-digital circuits, shown on schematics 69, 70, 71, 72, and 90, respectively. All outputs are interrupted when a short to ground or when excessive current is applied. Also, all outputs contain circuit protection functions.

Line Input

Ac line input passes through line filter FL010, switch S010, and fuse F800 to filter T020 (refer to schematic 68). Then it passes through the 115 V/230 V selector strap W810 to rectifier module CR030. When strap W810 is set to 115 V, CR030 performs voltage-doubler rectification; when it is set to 230 V, it performs bridge rectification. The rectified output is smoothed by capacitors C040, C041, C042, C043, C044, and C045.

Resistor R024 and triac Q020 provide surge current protection. At inverter start up, line voltage passes through R024 to the primary rectification diode in CR030, preventing surge currents. After inverter start up, Q020 turns on connecting line voltage directly to CR030.

Inverter

The smoothed output is shaped into an approximate 50-60 kHz square wave by switching transistors Q070 and Q080 and applied to the secondary voltage supplies through switching transformer T060. Switching transistor drive is provided by Q090 and Q092 through drive transformers T070 and T080. The duty cycle of the drive pulses generated by switching regulator controller U202 is controlled by the +5 VDS signal resulting from feedback from the regulator digital circuit (refer to schematic 72A) +5 VD output. Switching regulator controller U202 includes a pulse width modulation (PWM) oscillator, comparator, error-amplifier, output driver, and reference voltage regulator circuit. The +5 V_D supply is regulated by U202 using PWM.

Transistor Q220 and its peripheral circuits control U202 with the POWON signal from the control circuit (refer to schematic 70). It controls the inverter circuit at power on/off, or whenever any of the protection circuits operate. Transformer T100 and its peripheral circuits protect Q070 and Q080 from ex-

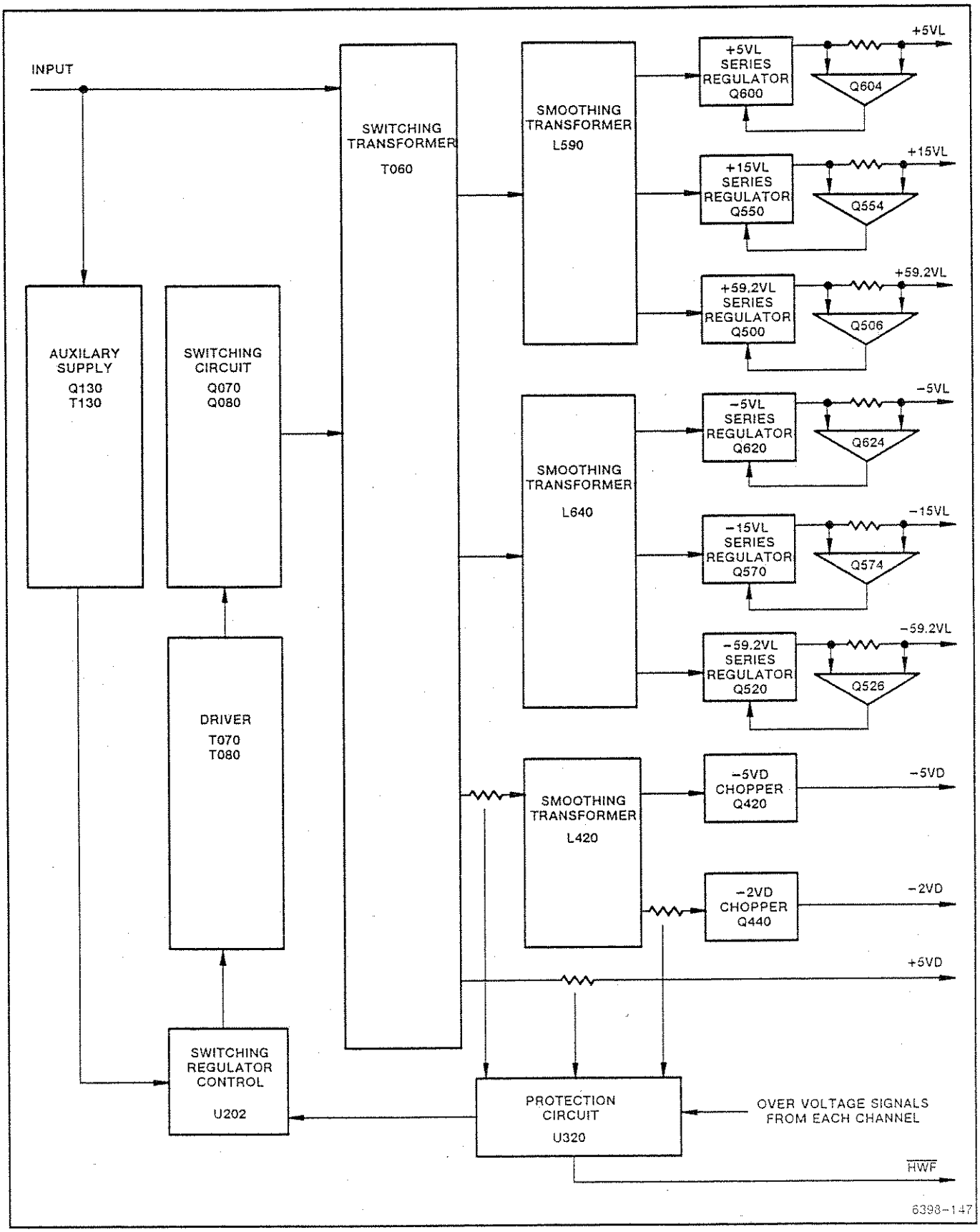


Fig. 1-92 Power Supply Block Diagram

cessive current. Direct feedback to U202 occurs when this protection circuit operates.

The inverter circuit includes internal power supply for the controller U202 and the control circuit (refer to schematic 70) and when the rear panel Principal Power switch is turned on, the control circuit is activated by this supply. The internal power supply circuit (refer to schematic 69B) applies the switching transformer smoothed primary dc voltage to the blocking oscillator formed by Q130 and T130 through fused resistor R110, causing it to oscillate at approximately 100 kHz. Power from T130 is applied to the secondary side, rectified, and smoothed by CR170 and C170. This voltage passes through the divider resistance to be sensed by U150. Then after comparison with a reference voltage, it controls the oscillation frequency of Q130, thus regulating the output using a built-in photocoupler.

Control

The control circuit consists of nine circuit blocks: Error Detection, Flasher, Secondary Power Switch Interface, Start-Up, Power Fail Signal Stabilizer, Inverter Start/Stop Interface, $\overline{\text{HWF}}$ Generator, Flasher Reset, and Overvoltage Protection.

ERROR DETECT. The error detect circuit accepts and processes signals from abnormal power supply condition error sense circuits.

Transistor Q340 stops circuit operation in response to the A86CK signal that indicates when the power supply internal interface cable W824 is disconnected. Gate U320B accepts the +5 V_D, or −2 V_D overcurrent detection signal OCC (refer to schematic 72B), takes the wired-OR output of it and other error signals, and sends the result to U320A-6. Undervoltage detection circuits U320C and U320D perform a wired-OR of the −5 V_D and −2 V_D error detection signals and other error signals, and apply the results to U320A-6. Gates U320A and U282D receive the $\overline{\text{ERROR}}$ signal from the +59.2 V_L, −59.2 V_L, −15 V_L, +15 V_L, +5 V_L and −5 V_L imbalance detection circuit (refer to schematic 71B), the $\overline{\text{ERROR}}$ signal from the overheat sensor (refer to schematic 72B), and the signals from U320B, U320C, and U320D described above, and supplies them to the Flashing Circuit.

Ac line sense circuits U900C and U900D detect abnormal conditions in the ac line. Detection circuit U900B detects abnormal power supply voltage drop in the control circuit.

FLASHING. The flashing circuit (U280A, U280B, and U282C) causes a flashing LED with a period of about four to five seconds when the power fails.

SECONDARY POWER SWITCH INTERFACE. The secondary power switch interface circuit (U300A) is controlled by the front panel ON/STANDBY switch that sends a signal to the start-up circuit to apply or turn off power to the instrument.

START-UP. Start-up circuit U290A, U902A, U902B, and U902C applies or removes power from the instrument in response to signals from the secondary power switch interface circuit.

POWER FAIL SIGNAL STABILIZER. Power fail signal stabilizer U290B, U300B, U282A, U282B, and U270A starts operation of the power supply protection system upon receipt of valid signals from the abnormal condition detection circuits.

INVERTER START/STOP INTERFACE. The inverter start/stop interface (U270C, U270D, and U200C) performs start/stop control of the inverter circuit in response to signals such as start-up and power fail.

HWF GENERATOR. The $\overline{\text{HWF}}$ generator (U200A, U200D, U270B, and Q280) generates the on/standby and abnormal power supply condition signals that are monitored by the MPU.

FLASHING RESET. The flashing reset circuit (U900A) stops the flashing LED when power supply operation becomes normal.

OVERVOLTAGE PROTECTION. Overvoltage protection circuits U200B and Q232 provide a response priority to overvoltage conditions over other protection conditions to ensure that the inverter circuit is stopped in response to an OVC signal (refer to schematic 71B) to prevent damage to the instrument. When this protection circuits operate flashing does not occur, and the stopped condition of the power supply is maintained. The ac line must be turned off, then on to restore normal operation.

Regulator-Analog

The output from switching transformer T060 is applied to the regulator analog (refer to schematic 71A) through J840. There it is rectified by CR590, CR592, CR594, CR596, CR640, CR642, CR644, and CR646, whose positive outputs are connected to chokes L590-x, and negative outputs are connected to chokes L640-x. Each voltage is described separately below.

The absolute values of the output voltages are monitored by U500A, and all outputs are interrupted if any vary from the specified values. Overvoltages detected by Q830 and Q840 cause all outputs to be interrupted instantaneously.

+5 V_L. After passing through choke L590-3, the roughly regulated output for +5 V_L is regulated to +5 V by Q600. Amplifier U600C provides feedback for +5 V_L. Overcurrents are detected by R604 and A605, and controlled by A604.

–5 V_L. After passing through choke L640-3, the roughly regulated output for –5 V_L is regulated to –5 V by Q620. Amplifier U600D provides feedback for –5 V_L. Overcurrents are detected by R625 and controlled by Q624.

+15 V_L. After passing through choke L590-2, the roughly regulated output for +15 V_L is regulated to +15 V by Q550. Amplifier U600B provides feedback for +15 V_L. Overcurrents are detected by R554, and controlled by Q554.

–15 V_L. After passing through choke L640-2, the roughly regulated output for –15 V_L is regulated to –15 V by Q570. Amplifier U600A provides feedback for –15 V_L. Overcurrents are detected by R574, and controlled by Q574.

+59.2 V_L. After passing through choke L590-1, the roughly regulated output for +59.2 V_L is regulated to +59.2 V by Q500. Amplifier U500C provides feedback for +59.2 V_L. Overcurrents are detected by R506, and controlled by Q506.

–59.2 V_L. After passing through choke L640-1, the roughly regulated output for –59.2 V_L is regulated to –59.2 V by Q520. Amplifier U500D provides feedback for –59.2 V_L. Overcurrents are detected by R526, and controlled by Q526.

Regulator-Digital

The regulator-digital circuits convert the +5 and –12 V outputs from switching transformer T060 to the +5 V_D, –5 V_D, and –2 V_D supply voltages.

+5 V_D. Outputs from switching transformer T060 for +5 VD are applied to the regulator-digital circuit through transformer T460; rectified through CR400, CR402, and CR404 and filtered by L400, C408, C410, and L402. The output voltage is fed back to the inverter circuit though R408 (+5 VDS), divided by R386 and R388, and input to the PWM comparator (input 1) of controller U202. Another PWM comparator input pin on the controller U202 is connected to the regulator digital trimmer R401 through R380 enabling adjustment of +5 V_D by R401.

–5 V_D. The –12 V output from switching transformer T060 is applied to the regulator-digital circuit through J866; rectified by CR420 and CR422; smoothed by filter L420, C428, and C430 to provide a roughly regulated –12 V. The resultant square waveform is chopped at approximately 100 kHz by Q420, rectified by L422, CR426, C436, and smoothed to –5 V_D. Duty cycle control for this circuit is performed by U360C, U350A, and U350D (refer to schematic 72B) to provide a stable output. Chopper outputs pass through filter L424 and C438.

–2 V_D. –2 V_D uses the same chopper regulation method as the –5 VD supply. It is chopped at approximately 100 kHz by Q440 from the –12 V roughly regulated output described above, rectified by L440, CR440, and C450, and then smoothed. U360D, U350B, and U350C (refer to schematic 72B) perform duty cycle control to stabilize the output. The chopper output passes through filter L442 and C452.

TV TRIGGER OPTION

The TV trigger option (Figure 1-93) adds hardware to allow triggering on and viewing of television signals. It consists of an analog and phase locked loop section, and a digital section.

The analog section contains composite video signal processing circuitry including signal amplification, automatic gain control, back-porch clamping, sync pickoff, and sync separation. Clocks at the horizontal (line) rate and a field indicator signal are sent to the digital section.

The digital section contains the line number detect counter and delay counter.

A trigger signal is connected to the Trigger Slope Select circuit on the A22 Trigger board. The trigger is generated when the selected horizontal sync pulse (line) occurs.

Waveforms produced by the TV trigger option are shown in Figure 1-94.

ANALOG AND PHASE LOCKED LOOP CIRCUITRY (DIAGRAM 73 & 74)

The TV option analog and phase locked loop circuitry (refer to schematics 73 and 74) processes the composite video to produce the back-porch level control, horizontal clock, and vertical field signals for other circuitry in the instrument.

TV Trigger Source Selector

The TV trigger source selector (U100A) switches between the Channel input amplifier and the composite video signal from the EXT TRIG IN connector, and applies it to the variable gain amplifier.

When the SSA SEL signal is low, U100A-10 becomes low selecting the SSA signal from the CH1 Input Amplifier. When the SSA SEL signal is high, the EXT SIG signal is selected. Diodes CR101 and CR103 provide input protection for U100A.

Variable Gain Amplifier

The variable gain amplifier (U110, U120B, and Q100) amplifies the input composite video signal. The front panel SLOPE switch determines whether the amplifier is inverting or noninverting.

Differential amplifier U110, which amplifies the composite video signal, contains two pairs of switching transistors that provide signal inversion when needed. The Sync Tip Clamp and Automatic Gain Control circuitry controls the channel resistance of Q100, which determines the gain of the amplifier. The gain is automatically adjusted to maintain proper sync-tip level. With no input signal, the gain is maximum.

The composite video signal is applied to one input of the differential amplifier U110-3 and to Dc Offset amplifier U120B. The input to U120B is filtered by low pass filter R112 and C100 making its output the dc component of the composite video signal. This filtered output is applied to U110-11.

Four transistors in U110 are controlled by the SLOPE signal from J240-35. When SLOPE is high, the transistors connected to U110-2 and U110-9 are biased on, causing the collector signal U110-8 to drive Q102. When SLOPE is low, the transistors connected to U110-13 and U110-6 are on causing the collector signal at U110-14 to be inverted with respect to both the input signal and the signal at U110-8 to drive Q102.

Level shifter Q102 shifts the signal from U110 to provide the voltage gain to drive U130D. For stable triggering, the composite video signal that drives U130D must be sync-negative; if the displayed input signal is sync-positive, the SLOPE switch must be selected to invert the signal.

Fixed Gain Amplifier and Back-Porch Clamp

The fixed gain amplifier and back-porch clamp provide additional gain to the video signal and additional start-up circuitry to set amplifier parameters when a TV signal is first applied.

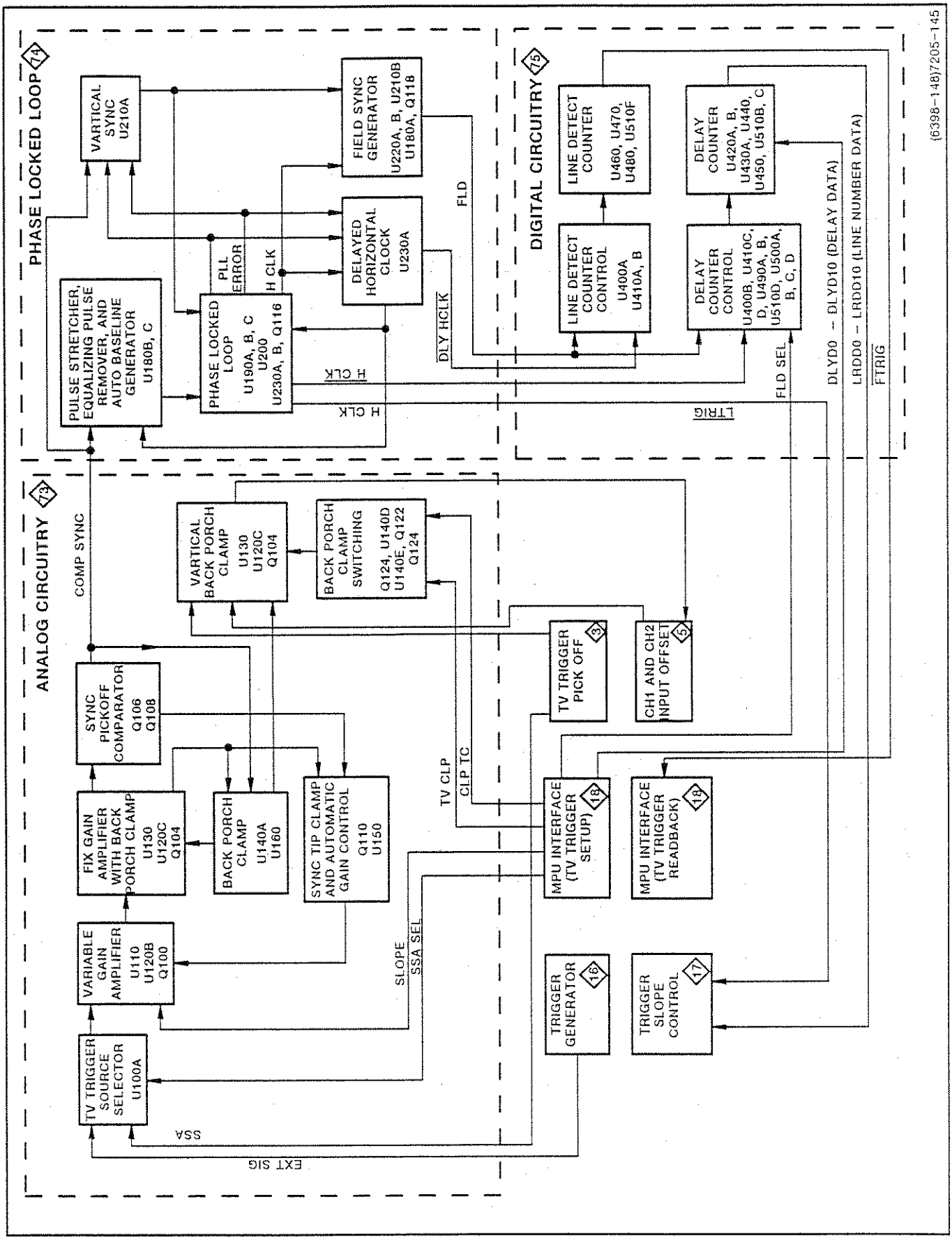


Fig. 1-93 TV Trigger Block Diagram

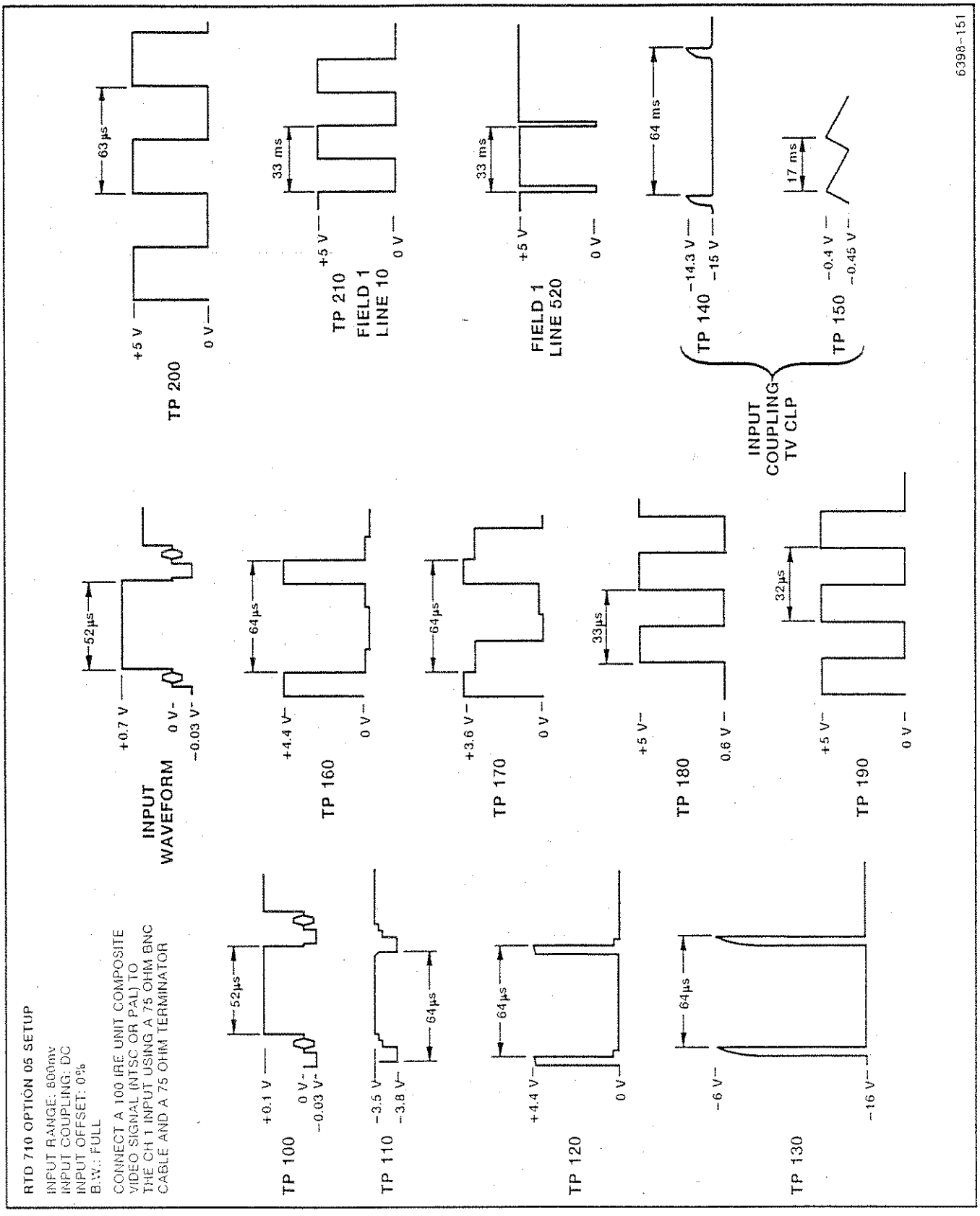


Fig. 1-94 TV Trigger Waveforms

Additional amplification is provided by U130. Devices U130A and U130B form a differential amplifier whose emitter current is provide by U130C. The output of U130B drives the input of the Sync Pickoff comparator.

When a TV signal is first applied, the channel resistance of Q100 is minimum, and the amplifier operating levels are established by feedback. This sets up a condition of maximum feedback and gain, which enables the back porch clamp, sync tip clamp, and automatic gain control.

Once a signal is applied, Q104 and its associated circuitry increase the dc level associated with the input signal if any of its signal values are below the ground reference level. When any signal is below ground, diode CR104 becomes forward biased, shutting off Q104 and forward biasing CR102. This reduces the output voltage of U120C, decreases the base drive voltage on U130B, raises the transistor's collector voltage, and turns off CR104.

Sync Pickoff Comparator

The sync pickoff comparator (Q106 and Q108) is switched by the sync pulse. The switching threshold is set by the values of resistors R164 and R166 at approximately the 50% sync level. The composite sync waveform appears at the collector of Q108, and its inverse appears at Q106.

Sync-Tip Clamp and Automatic Gain Control

Transconductance operational amplifier U150 acts as a sync-tip clamp to control the gain of U110 by altering the channel resistance of Q100. Its gain is determined by the current into pin 5, and it is enabled on sync tips when pin 5 (U150) is high (–14.4 V). One input of the amplifier is grounded, while the other has the signal from U130B applied to it through R176. The amplifier is enabled when the start of the sync pulse at the collector of Q108 becomes low. This alters the channel resistance of Q100, which keeps the signal level at the collector of U130B at about 0.5 V for the duration of the sync pulse. When U150-5 is low (–15 V), U150 is turned off and C104 acts as a sample and hold to maintain bias on Q100.

Diode CR106 reduces amplifier gain when the sync tip is below –0.2 V. If the diode becomes forward biased, Q110 turns on, if it is not already on. Amplifier U150 can then increase the channel resistance of Q100, thus reducing the amplifier gain.

Back-Porch Clamp

Transconductance operational amplifier U160 performs back-porch clamping to control the video signal level during the TV back-porch period. Its gain is determined by the current into U160-5. When the amplifier is enabled, U160-5 is high (–14.6 V). When the collector of Q106 becomes negative, the resulting pulse is applied through C120 to turn off U140A. A positive-going signal on the collector of U140A enables U160 during the back-porch period. The output of U160 drives voltage-follower U120C, which in turn establishes the base voltage of U130B. The collector signal of U130B is applied through R176 and R178 to drive U160-3. This feedback loop establishes zero volts on U160-3 during the back-porch period holding the collector of U130B to approximately 4.5 V. When U160-5 is low (–15 V), U160 is turned off and C114 acts as a sample and hold to maintain the bias on U130B.

Vertical Back-Porch Clamp

The vertical back-porch clamp circuit clamps the back-porch level of the displayed signal to approximately zero volts.

Input to level comparator U170 is a sample of the signal (CH1DC) in the Channel 1 amplifier. The output of the clamp (TV OFS) supplies a dc offset to the channel 1 amplifier. The level comparator supplies a dc offset of such a magnitude to cause CH1DC to be approximately the same as CH1 OFS TV (Channel 1 input offset voltage) during the back-porch interval.

Any color burst on the signal is removed by R194 and C126. The signal is then compared to the CH1 OFS TV by U170 during the back-porch interval. Any dc offset required to bring the back-porch level up to the input offset voltage is sampled and held by C130 and C132. Operational amplifier U120A supplies the drive required by the channel 1 amplifier.

The CLP TC (Clamp Time Constant) signal passes through Q120 to control gate Q112, which varies the back-porch clamp time constant by turning C130 on and off. CLP TC is fixed at a low level because it always operates with the sample and hold capacitor C130.

Back-Porch Clamp Switching

The back-porch clamp switching circuitry determines when the vertical back porch clamp is active and which of its level comparators is used.

When the back-porch clamp is disabled, TV CLP is low, turning on Q122. A high at the collector of Q122 turns on Q124, and Q114, which keeps comparator U170 off and the input to U120A grounded. With this circuitry disabled, the Channel 1 amplifier cannot receive a dc offset voltage from the comparators.

When the back-porch clamp is enabled, TV CLP is high, turning off Q122. A low at the collector of Q122 turns off Q114 enabling U120A and allowing U140E and U140D to turn off Q124, which turns on comparator U170. While U170 is gated on during the back-porch interval, U140A turns off. With the vertical back porch clamp enabled, the back porch of the displayed signal is clamped to the Channel 1 OFFSET. However, when the phase locked loop is not locked, the vertical back-porch clamp is turned off through R227.

If the back-porch clamp is enabled during the back-porch interval, device U140A turns on U170. Since the dc offset generated by U170 must be maintained during the entire horizontal interval, when U170 is turned off between back porch intervals, the required offset is maintained by C132 and C130.

Pulse Stretcher, Equalizing Pulse Remover, and Auto Baseline Generator

The pulse stretcher and equalizing pulse remover stretches the horizontal sync pulses and removes every other equalizing pulse from the input composite sync. The auto baseline generator generates the HORIZ CLK signal used for generating triggers.

The leading edge of each sync pulse turns on U180C, which reverse biases CR116 turning off U180B. A high at the collector of U180B keeps U180C on and reverse biases CR112. The collector remains high until C144 charges to approximately 1.4 V. The resulting square wave applied through CR118, becomes the HORIZ CLK signal.

To avoid passing every equalizing pulse and serrated pulse, the output of the delayed horizontal clock circuit is coupled through R250, keeping U180B turned on and its collector low midway between horizontal sync pulses.

After the HCLK is delayed by R256 and C146, the auto baseline generator ORs the horizontal sync stripped from the input signal and the HCLK clock from the phase locked loop divider.

Phase Locked Loop

The phase locked loop (PLL) generates signals used to identify an individual TV field in the interlaced scan system.

PLL U200 operates at twice the horizontal clock frequency. Its output is divided by two by U230B, producing both HCLK and $\overline{\text{HCLK}}$. Horizontal sync from the input signal is applied to U200-14. The $\overline{\text{HCLK}}$ signal generated by the PLL through U230B is applied to U200-3. Equalizing pulses and vertical sync are removed from the PLL inputs by U190B and U190C (see Figure 1-95).

Phase locked loop U200-1 is low whenever the signals on U200-3 ($\overline{\text{HCLK}}$) and U200-14 (horizontal sync) do not coincide. The PLL error signal (U200-1) is stretched by R272 and C154, then inverted by Q116. When the collector of Q116 is high, vertical sync (U210A) and the delayed horizontal clock (U230A) are reset, thus applying the equalizing pulses and vertical sync to U190B and U190C, respectively. This allows the phase locked loop to see the entire input signal while attempting to lock onto the input.

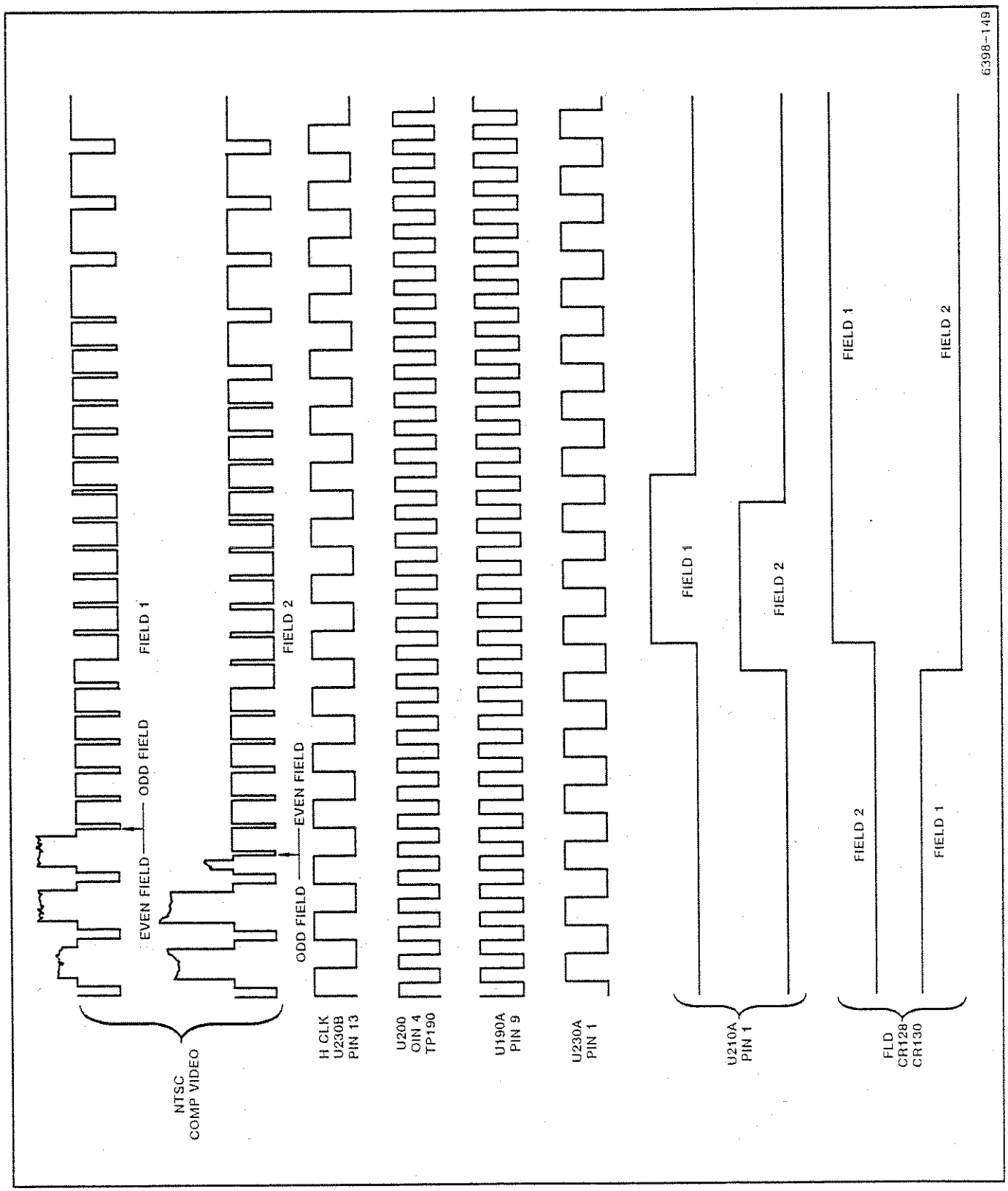


Fig. 1-95 TV Trigger Option Timing Diagram

Delayed Horizontal Clock

The delayed horizontal clock is used to remove equalizing pulses from the horizontal sync. The horizontal clock signal (HCLK) is clocked through U230A by the PLL output signal to delay the horizontal clock by 1/4 of a horizontal clock cycle.

Vertical Sync

The vertical sync circuitry outputs a pulse for both the Field 1 and the Field 2 vertical sync pulses. The vertical sync signal is produced by clocking the $\overline{\text{COMPOSITE SYNC}}$ signal into U210A using an inverted 2X horizontal clock. During the vertical sync period, the $\overline{\text{COMPOSITE SYNC}}$ signal becomes high on the rising edge of the PLL output (U190A-9). During the remainder of the field, the $\overline{\text{COMPOSITE SYNC}}$ becomes low on the rising edge of the PLL output (U190A-9).

Field Sync Generator

The field sync generator develops the FLD signal from the horizontal clock (HCLK) and vertical sync signals. For interlaced scan signals, it identifies the field; for noninterlaced scan signals, it identifies only the vertical sync. Counters in the digital section use the FLD signal when selecting either the Field 1 or Field 2 line counter.

Field ID, which identifies the fields of the interlaced scan signal, is generated by U220A and U220B at the same time. During interlaced scanning, U220A-2 is high during Field 1 and low during Field 2. For noninterlaced scanning systems, the changing field ID is absent. This absence at U220B is detected by the interlaced scan detector (U220B, U180A, and Q118) causing the interlaced scan detector to enable circuitry that generates a FLD signal at the vertical rate.

During interlaced scan signals, the changing field ID signal from U220B keeps U180A and Q118 turned on. A low at the collector of U180A allows U220A to continue generating a normal FLD signal. A high at the collector of Q118 keeps U210B set, preventing it from affecting the FLD signal.

During a noninterlaced scan signal, the field ID signals generated by U220B and U220A are static, causing the dc level on U220B to be blocked by C158, turning off U180A and Q118. A high at the collector of U180A resets U220A preventing it from affecting the FLD signal. A low at the collector of Q118 allows the vertical sync signal to clock U210B, producing FLD. This FLD signal generated by U210B has no relation to Field 1 or Field 2.

AND gate CR128, CR130, and R294 selects the signal from either U220A or U210B as the FLD signal.

DIGITAL CIRCUITRY (DIAGRAM 75)

The digital circuitry comprises a TV line detect counter to detect the line number of the composite input signal, a delay counter to generate a field trigger pulse, and the associated control circuitry. A timing diagram associated with these circuits is shown in Figure 1-96. The outputs from this circuitry is connected to the A22 Trigger board, and through that board to the MPU bus.

Line Detect Counter Control

The line detect counter control (U400A, U410A, and U410B) applies a horizontal pulse to the counter in one frame interval, and outputs the latch pulse and counter reset pulse after counting is completed. The FLD pulse is divided in half by U400A to generate a single frame pulse to apply the $\overline{\text{DLYHCLK}}$ signal through U410A as the counter clock. The rising edge of the 1-frame pulse is applied to the latch of the line detector counter as the latch pulse. A counter reset pulse is produced by taking the negative-logic AND of the FLD pulse and the frame pulse at U410B.

Line Detect Counter

Devices U420A, U420B, and U430A comprise an 11-bit binary counter, and devices U440 and U450 comprise a latch. These devices are controlled by the clock, latch pulse, and reset pulse from the line detect counter control circuit. Devices U510B and U510C comprise a buffer for the reset signal when power is turned on.

Delay Counter Control

The delay counter control circuitry (U400B, U410C, U410D, U490A, U490B, U500A, U500B, U500C, U500D, and U510D) ensures that the trigger is correctly applied to the specified field and line in the TV field trigger mode.

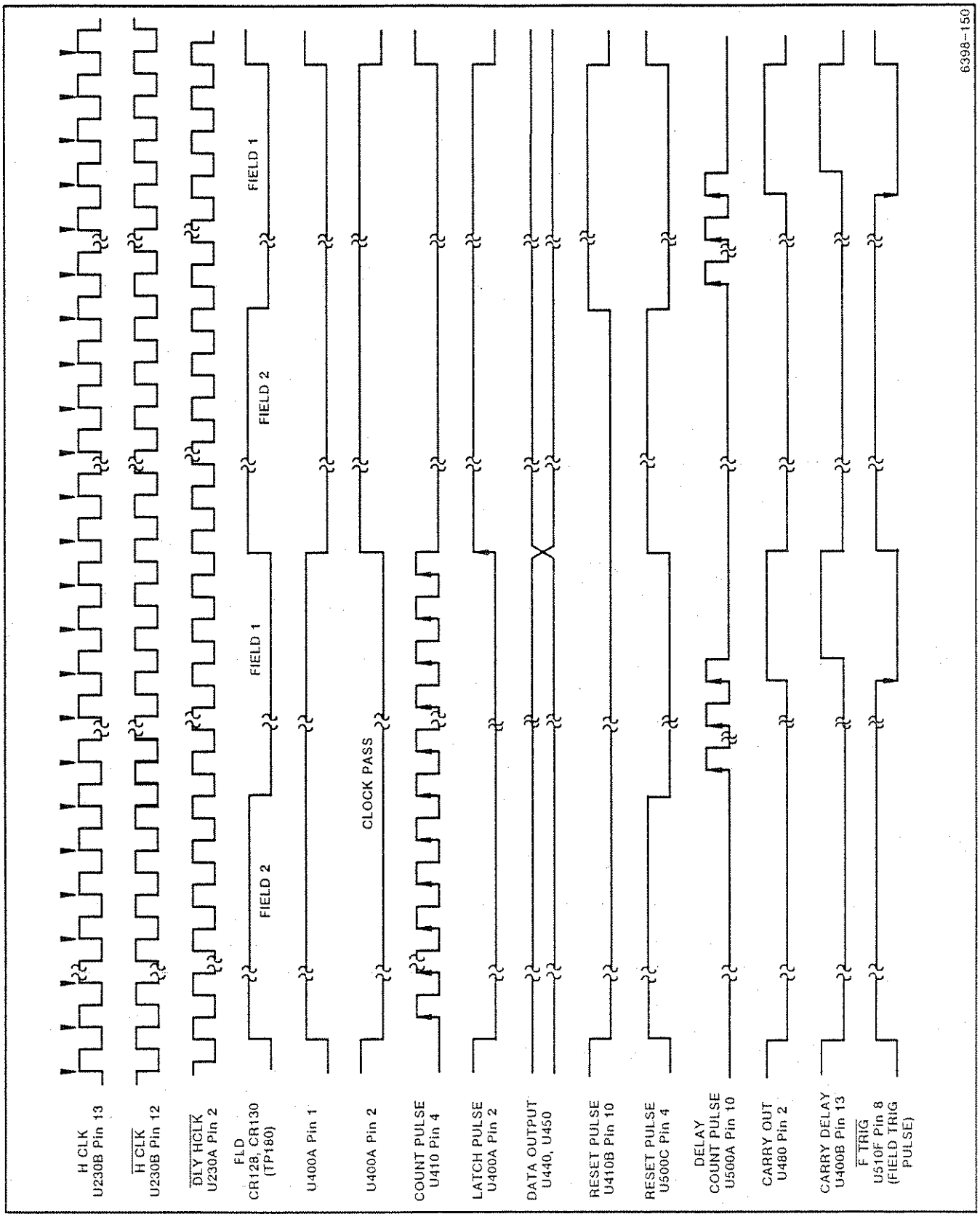


Fig. 1-96 TV Line Number Detect Counter and Delay Counter Timing Diagram

When Field 1 is selected, the FLD SEL signal becomes high, U510D-12 becomes low, disabling U490A and U500B. The preset data (DLYD0-DLYD10) corresponding to the specified line number is applied to the 11-bit binary counter and the pulse used to preset the counter is generated from the field pulse applied through U500D and U500C. While the preset pulse is high, U410D-3 is low, cutting off the $\overline{\text{HCLK}}$ signal from the counter.

When the specified field is reached, the preset pulse is released, $\overline{\text{HCLK}}$ is applied to the counter through U410C, U490B, and U500A, and the count begins. If the preset data is the same as the clock number, a carry signal (U480-2) is output, causing U400B to close gate U410C at the end of a half clock delay, thus stopping clock $\overline{\text{HCLK}}$. This carry signal corresponds to the specified field and line, thus it becomes the field trigger pulse. This sequence repeats for each frame.

If field 2 is selected, the preset pulse is applied to the counter through U410D, U500B, and U500C, and $\overline{\text{HCLK}}$ is applied through U410C, U490A, and U500A to the counter. At this point the operation of the circuit is similar to that for field 1. When the field has been exceeded and the line number is specified, (i.e., when the specified line number does not fall in the specified field, such as in NTSC, when line 520 is specified for field 1), the MPU automatically switches to the correct field for the specified line number. This ensures that the trigger is correctly applied to the specified field and line.

Delay Counter

The delay counter (U460, U470, U480, and U510F) is controlled by the clock and reset pulses from the delay counter control circuit, and by delay data from the MPU. It uses binary incremental configuration to ensure output of a stable carry output. Delay data are supplied to the delay counter in two's complement. The carry output is applied simultaneously to the delay counter control circuit, and the A22 Trigger board through buffer U510F as the field trigger pulse $\overline{\text{FTRIG}}$.

INDICATOR (DIAGRAM 76)

The indicator circuit board (A64) is installed when the blank front panel option (Option 19) is installed. It controls the front panel LEDs, and consists of an LED driver, option bit, a power indicator, and secondary power switch circuits.

LED Driver

LED driver U100A controls the trigger status indicators DS100 and DS101 (ARM'D and TRIG'D); LED driver U110 controls the GPIB status indicator DS110 (GPIB SRQ).

Option Bit Buffer

Option bit buffer U100B holds option bit data that determines whether or not the Panel Control Board (A60) or the Indicator Board (A64) is installed in the instrument. When the Indicator Board is installed, BD1 and BD0 are 0 and 1, respectively.

Power Indicator

Power indicator LED DS001 indicates whether or not the power module is applying power to the instrument.

Secondary Power Switch

The secondary power switch (S846) on the front panel is connected to the power module through the Indicator board and Mother board to control the on/standby condition of the power module.

MAIN INTERCONNECT (DIAGRAM 77 - 89)

The Main Interconnect board shown in schematics 77-89 (also referred to as the Mother board) is located at the bottom of the instrument. It is used to interconnect signals among the instrument boards. This board contains a number of filter capacitors for preventing and reducing noise generated by the buses on this board.

Section 2
DIAGNOSTICS

INTRODUCTION TO DIAGNOSTICS

The RTD 710A Digitizer contains three levels of internal diagnostics:

- Level 1 (Power Up Verification Routines)
- Level 2 (Predefined Fault Isolation, Exercise, and Calibration Routines)
- Level 3 (User Defined routines used with the GPIB Commands: DEPosit, EXEcute, and FETch)

The instrument also detects internal circuit defects during normal operation, which it reports and displays as "E" plus a 3-digit Event Code, rather than an "E" plus a 5-digit Error Code, which relates to a diagnostic test number.

LEVEL 1 DIAGNOSTICS

Level 1 diagnostics are called *Power-up Verification Routines* as they run automatically each time the instrument is turned on, or whenever the power is cycled off then on. These diagnostics include a set of kernel verification routines and a set of functional verification routines. If no failures occur when these routines are run, the instrument proceeds directly into normal operation. When the MPU system detects and Address Error, Illegal Instruction, or Zero Divide during Normal Operation, Level 1 Diagnostic, Level 2 Diagnostic, or Level 3 Diagnostic, the Power-up Verification routines may be run automatically. Figure 2-1 shows the routine execution flow for Level 1 diagnostics.

When a functional verification routine detects a failure, an "E" plus a 5-digit error code is displayed in the 7-segment LED Control indicator on the front panel, and the verification routine continues. Each time a different failure is detected, a new error code is displayed and testing continues. When the functional verification tests are completed with failures, the instrument enters the Level 2 diagnostics "command state" and waits for operator intervention. In this state, the operator can use front-panel key selections (or GPIB commands) to return the instrument

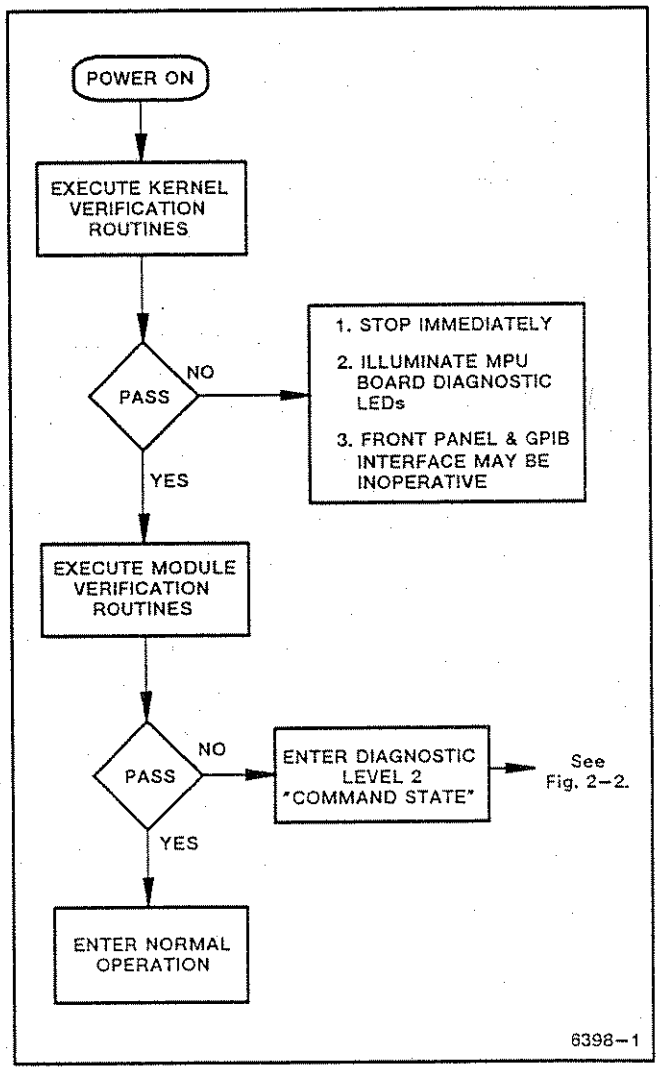


Fig. 2-1 State diagram for level 1 diagnostics

to normal operation, or to execute Level 2 or 3 diagnostic routines.

When a kernel verification routine detects a failure in some part of the kernel that prevents an error code from being displayed in the Control indicator, or disables the front-panel controls, or prevents the GPIB interface from controlling or querying the instrument, a set of internal MPU LEDs provide an indication of the defective kernel device.

LEVEL 2 DIAGNOSTICS

Level 2 diagnostics are called Level 2 because they execute only from the Level 2 "command state" where the execution sequence and operating mode settings (such as, loop until fail, loop until pass, etc.) are controlled by the operator. These diagnostics consist of *Predefined Fault Isolation, Exercise, or Calibration Routines*, which are contained in ROM.

Fault Isolation Routines consist of all Level 1 routines, except GPIB Control IC Test (40101), and a number of Level 2 routines that would require too much time to be run at power up. *Exercise Routines* are more complex routines that require operator intervention to set up additional testing hardware, or to analyze the result of a display. *Calibration Routines* are mainly used to generate specific waveform patterns for adjusting the analog circuitry in the instrument. Figure 2-2 shows the routine execution flow for Level 2 diagnostics.

LEVEL 3 DIAGNOSTICS

Level 3 diagnostics are referred to as *User-Defined Routines*, as they must be created by the user and input through the GPIB interface. The Programming Command Set provides three GPIB commands (DEPosit, EXEcute, and FETch) to store, call, and execute these routines.

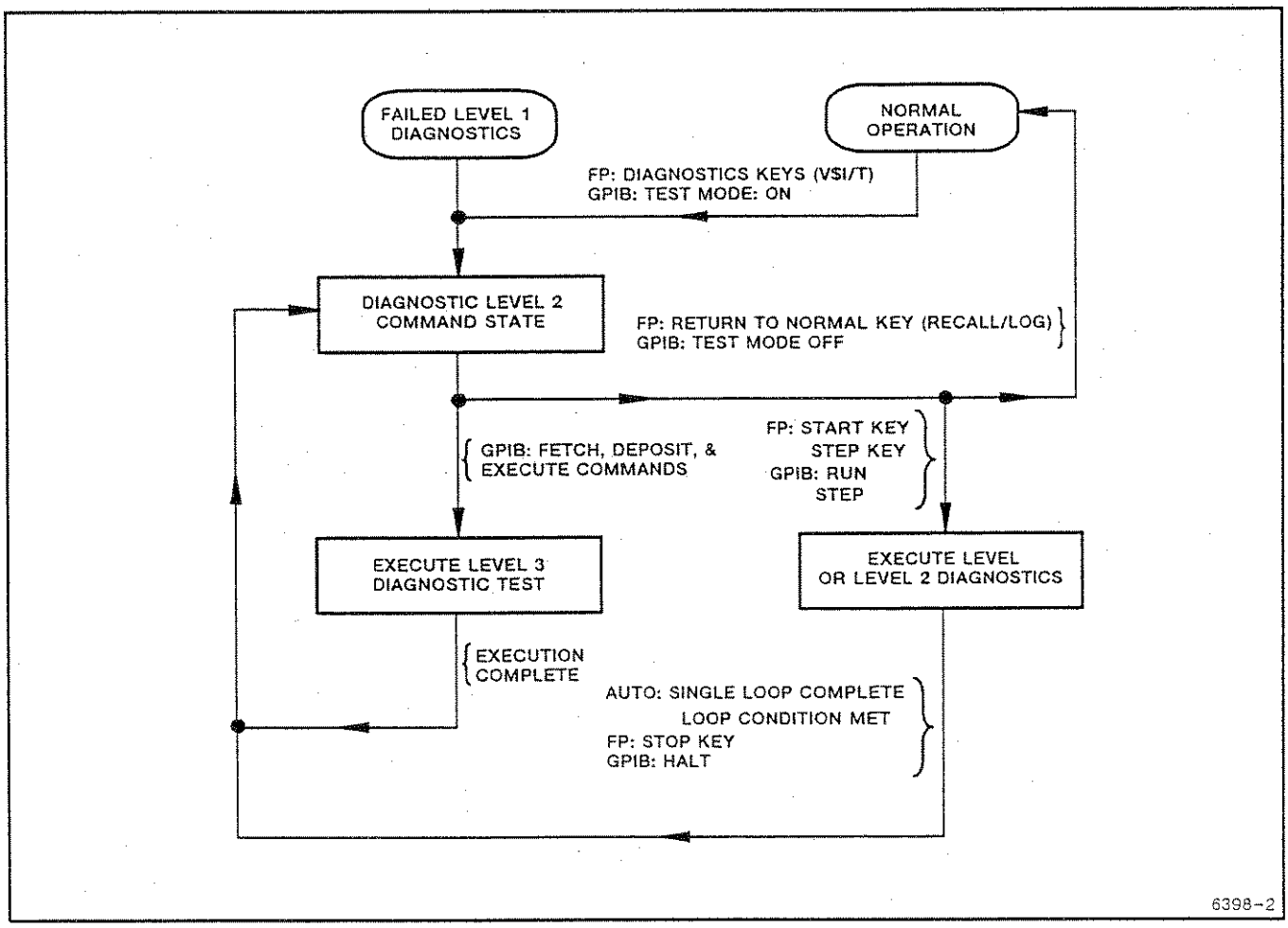


Fig. 2-2 State diagram for level 2 diagnostics

NORMAL OPERATION ERRORS REPORTED AS EVENT CODES

Table 2-1 summarizes the errors that may be detected during normal operation and displayed in the Control indicator as a 3-digit Error Code number preceded by the character "E". This number coincides with the Event Code response that would occur with an Event? query.

Table 2-1
ERROR/EVENT CODES

Error/Event Code	Description
302	System Error or DMA Controller Error. This error means a DMA Controller error has occurred, or transmission to or from the GPIB has failed. It generates an SRQ if the INR request mask is ON. Use the 20000-series of diagnostic tests to determine the cause of failure.
350	Auto Calibration Failed. This error means the DC, Gain, or Phase calibration function failed, which means the Auto-Cal function started, but didn't finish. It generates an SRQ if the INR service request mask is ON. Use the 70201 diagnostic test to determine the cause of failure.
351	Nonvolatile Memory (NVM) Checksum Error. This error means the SAVE or RECALL function checksum test failed. It generates an SRQ if the INR service request mask is ON. Use the 20400, 20501, 20502, or 20503 diagnostics tests to determine the cause of failure.

HOW TO USE DIAGNOSTICS

This subsection describes the front-panel controls and indicators, and the GPIB commands used to select and run the various diagnostic routines.

Diagnostics are entered in four ways:

1. Level 1 diagnostics are entered automatically when the instrument is powered up, power is cycled off, then on, or when the MPU detects an address error, illegal instruction, or zero divide.
2. Level 2 diagnostics are entered automatically when the instrument fails Level 1 diagnostics.
3. Level 2 diagnostics are entered voluntarily from the Level 2 Diagnostics mode "command state" when the operator makes certain front-panel key selections, or sends specific GPIB commands.
4. Level 3 diagnostics are entered voluntarily from the Level 2 Diagnostics mode "command state" when the operator creates, stores, and calls diagnostic routines with specific GPIB commands.

LOCAL CONTROLS AND INDICATORS/ REMOTE GPIB COMMANDS

Figure 2-3 identifies the diagnostic function performed by selected front-panel keys on the RTD 710A. In the description of the diagnostic function of each key, the GPIB command used to remotely implement the same function is listed. Since each GPIB command is explained in the RTD 710A Instruction Manual, it is not repeated here.

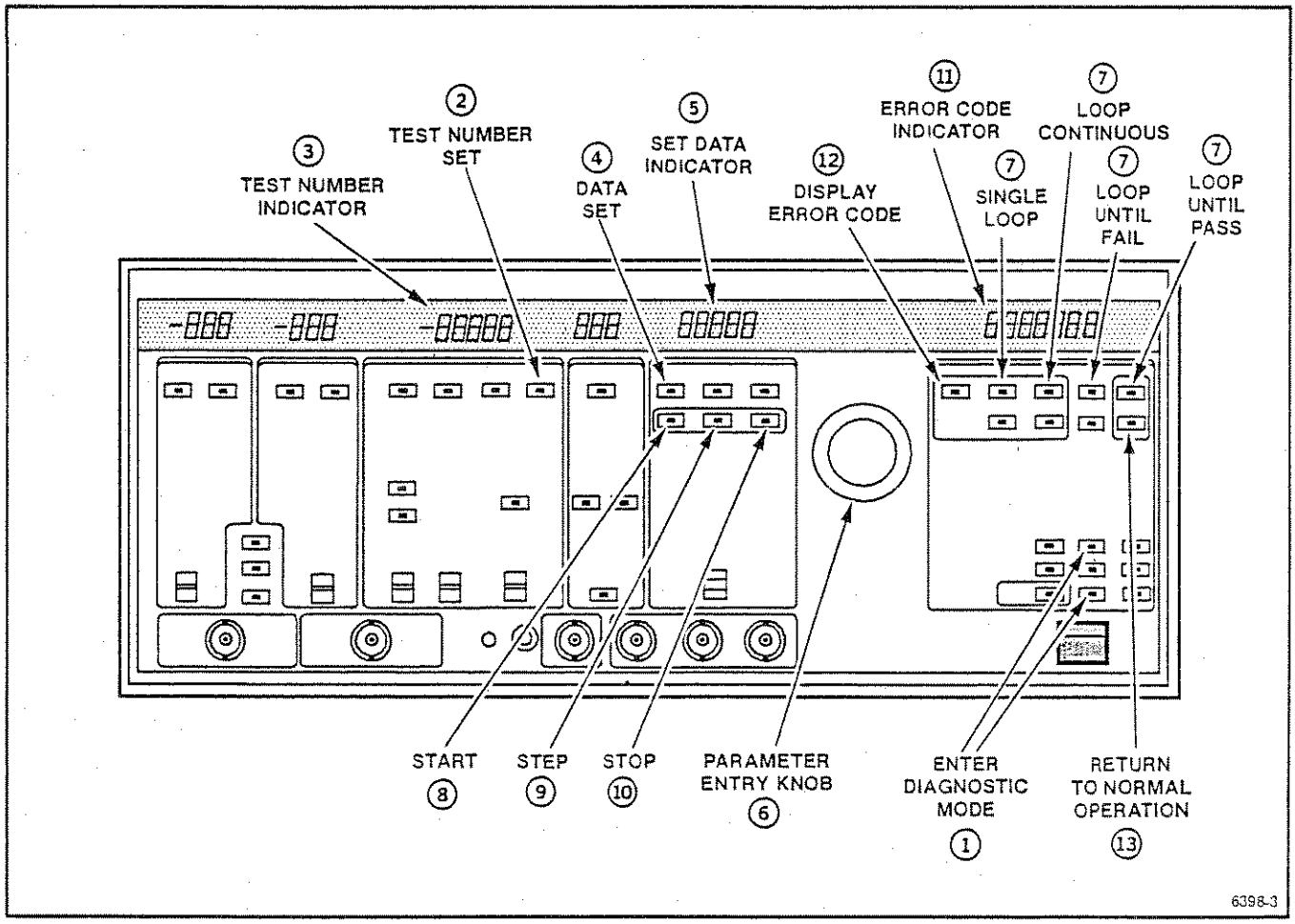


Fig. 2-3 Front-panel control and indicator functions in diagnostic mode

1 Enter Diagnostic Mode

Enters the Level 2 diagnostics, operator-controlled "command mode" when both keys are pressed simultaneously.

GPIB Commands: TESt MODe:ON

TESt TYPe:SELFDiag

TESt TYPe:EXTDiag

2 Test Number Set

Activates the test number setting function, which allows a test number to be entered with the Parameter Entry Knob.

GPIB Command: TESt NUMber:<NRx>

3 Test Number Indicator

Displays the test number being set. After the **Start** key is pushed, it displays the number of each test as it is being performed.

GPIB Command: TESt? NUMber

4 Data Set

Activates a data setting function for *Exercise* or *Calibration Routines*, which allows a data item to be set with the Parameter Enter Knob. This data is written to a hardware register, which can then be checked or verified using an oscilloscope or logic analyzer.

GPIB Command: TESt DATa:<NRx>

5 Data Set Indicator

Displays the data item being entered.

GPIB Command: TESt? DATa

6 Parameter Entry Knob

Used to input a numeric parameter or data on some tests.

GPIB Command: TESt DATa:<NRx>

7 Diagnostic Mode Keys

Selects a single pass or looping mode of diagnostic operation:

Single Loop: Causes the diagnostic to execute once, then stop.

GPIB Command: TESt LOOp:ONE

Loop Continuous: Causes the diagnostic to execute in a continuous loop until the **Stop** key is pushed, or the **HALt** command is sent over the GPIB.

GPIB Command: TESt LOOp:CONt

Loop Until Fail: Causes the diagnostic to execute in a continuous loop until a failure occurs, the **Stop** key is pushed, or the **HALt** command is sent over the GPIB.

GPIB Command: TESt LOOp:FAIl

Loop Until Pass: Causes the diagnostic to execute in a continuous loop until it passes the test, the **Stop** key is pushed, or the **HALt** command is sent over the GPIB.

GPIB Command: TESt LOOp:PASs

8 Start

Starts the selected test number. The cumulative result of the completed test is displayed in the Control indicator. It may be an error code, test result value, or zero (0) if the test is a calibration routine, or no error is detected. The key indicator blinks during the diagnostic test.

GPIB Command: RUN

9 Step

Whenever a failure occurs in the Single Loop mode, or a stop condition is met in the Loop Until Failure/Pass modes, diagnostic operation halts immediately. Pressing the **Step** key advances the diagnostics to the next step and causes execution to resume. The key indicator blinks during the diagnostic test.

GPIB Command: STEp

10 Stop

Pressing this key causes an executing routine to stop immediately and return to the Level 2 diagnostics "command state". The key indicator illuminates when pushed.

GPIB Command: HALt

11 Error Code Indicator

Displays the error code whenever an error is detected during diagnostics. It is updated with a new error code each time a new error is detected. Up to 40 error codes are stored in system RAM as they occur. A display of zero (0) indicates that no error was detected.

GPIB Command: ERRor?

12 Display Error Code

Pushing the key allows the operator to sequence backward through previously displayed error codes with rotating the Parameter Entry Knob.

GPIB Command: ERRor?

13 Return to Normal Operation

Pushing the key returns the instrument to normal operation. Any failures reported by the previously executed diagnostics are ignored. This allows the operator to operate the instrument in the presence of nonfatal errors.

GPIB Command: TESt MODe:OFF

RUNNING A LEVEL 2 DIAGNOSTIC

To run a Level 2 diagnostic test starting from normal operation:

1. Enter the Level 2 Diagnostic Mode by simultaneously pressing the V and 1/T Measure keys.
2. The Test Number Set key LED should be blinking, the Start key LED should be extinguished, and the Test Number Indicator should be displaying a zero (0). If the Parameter Entry Knob is rotated clockwise, a 5-digit test number should appear in the Test Number Indicator.
3. To start a diagnostic, rotate the Parameter Entry Knob in either direction until the desired number is selected in the Test Number Indicator, then push the Start key. The Start key LED should be blinking and the Test Number Set LED should be illuminated.
4. When an automatic test (A) finishes executing, the Start key LED extinguishes and the Test Number Set LED starts blinking. When a manual (M) exercise or calibration test finishes executing, the Stop key must be pushed before the Start key LED extinguishes and the Test Number Set key LED starts blinking.
5. Whenever the Test Number Set key LED is blinking, a new test number can be entered with the Parameter Entry Knob.

OPTION 19 BLANK FRONT PANEL DIAGNOSTIC OPERATION

The Option 19 Blank Front Panel instrument executes diagnostics the same as an instrument with a front panel, except 1) all diagnostic manipulation is done with GPIB commands, and 2) The ERROR? query command must be executed after each test, or test sequence to determine if there were any failures.

When the instrument is powered up, Level 1 diagnostics automatically execute, and if no failure is detected, and SRQ is generated, which turns on the GPIB RQS ID indicator. If a failure is detected, or if the GPIB port fails, the GPIB RQS ID indicator blinks. If for some reason diagnostics cannot be controlled through the GPIB, the blank front panel must be replaced with a standard front panel for diagnostics.

GENERAL DIAGNOSTIC DESCRIPTIONS

LEVEL 1 DIAGNOSTICS

Kernel Definition

Before the instrument can execute the Level 1 functional verification routines, or the Level 2 and Level 3 diagnostic routines, the following kernel devices must be operational:

Power Supply
MPU Clock Circuitry
MPU
Data and Address Bus to ROM
Address Decoder to ROM
ROM (at least readable)
Stack Area of System RAM

As soon as the instrument is turned on, the first routines executed are the kernel verification routines. If no kernel failures are detected, then the functional verification routines are executed.

Diagnostic LEDs

There are three LEDs mounted on the MPU board to isolate defective kernel circuitry when the instrument appears to be completely dead. A dead instrument is defined as one that cannot display any intelligible error message on the front panel or respond to an ERRor? query over the GPIB. The operation of these LEDs is shown in Table 2-2, and described in the Kernel Verification topic below.

Table 2-2
DIAGNOSTIC LED OPERATION

LED Meaning	LED1	LED2	LED3
Power Supply Failure		Did not turn on	
MPU failure	ON	ON	ON
Diagnostic ROM failure	OFF	ON	ON
Diagnostics RAM failure	OFF	OFF	ON
Kernel Operational	OFF	OFF	OFF

Kernel Verification

As soon as the instrument is turned on, the power supply turns on the three LEDs on the MPU board to indicate that the +5 Vd power supply is operational, then the MPU turns off LED1 to indicate that it is operational, sets its root node (0), and begins executing instructions from system ROM.

The first test checks approximately 10 bytes from first area of ROM. If it passes, LED2 is turned off.

The second test checks that portion of System RAM used by the MPU (addresses EF800-EFFFF). If it passes, LED3 is turned off to indicate that the RAM memory required for diagnostics is operational.

Module Functional Verification Testing

If all kernel verification tests are passed, module functional verification testing beings. The first verification test checks all front panel key and indicator LEDs by turning them on (7-segment LEDs display "8." in each segment) for about two (2) seconds. Next, all front panel key controls are tested for shorts. At this point, all remaining Level 1 module and other functional tests are executed. If a failure is detected during any of the functional verifications tests, the error code is continually updated, displayed in the Control indicator, and stored in memory (up to 40 error codes can be stored for future recall).

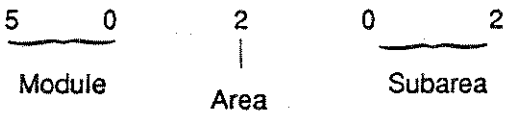
LEVEL 2 DIAGNOSTICS

Diagnostics Structure

Level 2 diagnostics are hierarchically structured into three levels, a Module level, an Area level, and a Subarea level, and defined with a 5-digit number such as:

50202

whose level structure is decoded as:



or as

Module:	50000
Area:	200
Subarea:	02

Failure detection is based on starting at the lowest system level (the kernel), then testing each successive module with the knowledge that previously tested modules are functioning properly. When a module fault is detected, diagnostics are isolated to that module level and additional testing proceeds downward through the module to the Area or Subarea level.

Diagnostics Execution Rules

When diagnostic test numbers are individually selected and executed in Level 2, the level of the test number selected establishes the execution rules as follows:

1. If the test number selected is at the Module level, such as:

   10000

   then all areas and subareas of the module set designated as Auto (A) are executed.

2. If the test number selected is at the Area level, such as:

   10100

   then all the subareas of the area set designated as Auto (A) are executed.

3. If the test number selected is at the Subarea level, such as:

   10101

   only that subarea test is executed.

DIAGNOSTIC CODES AND DESCRIPTIONS

This subsection contains a table-like listing of the diagnostic codes and their descriptions. The meaning of column coding is:

Level Column: A number in this column indicates at which diagnostic level the test can be executed.

Loop Column: L/S means Loop/Single. Loop (L) means the test can be executed in a loop mode. Single (S) means the test is executed only once each time it is started.

A/M Column: A/M means Auto/Manual. Auto (A) means the test can be executed without operator intervention. Manual (M) means the test requires operator intervention to do a test setup, or to review a display, or to make a test or adjustment, or the test takes too much time to complete to be an automatic test. Manual tests are available only at the Subarea level.

ROOT NODE DIAGNOSTICS

Test Number	Level	Loop	A/M	Description
0	2	L,S	A	Root Node of Level 2 Diagnostics **Operation:** Runs all Level 2 diagnostic tests designated as Auto (A) in column 4, except 40101. As each test is executed, its number is displayed in the Test Number Indicator.

Test Number	Level	Loop	A/M	Description
				10000 - MPU MODULE DIAGNOSTICS (A50)
10000	2	L,S	A	MPU Module Test; A50 MPU Board. **Operation:** Runs all 10xxx system area and subarea tests designated as Auto (A) in column 4. As each test is executed, its number is displayed in the Test Number Indicator.
10100 - System ROM Tests				
10100	2	L,S	A	System ROM Test in MPU Module. **Operation:** Runs all 101xx subarea tests designated as Auto (A) in column 4. As each test is executed, its number is displayed in the Test Number Indicator, and when finished, 10100 is redisplayed. This test calculates the checksum of each ROM using all except the last two bytes, then checks the calculation against the checksum that is permanently stored in the last two bytes of each ROM. Devices tested: Decoder Buffers (A50U180, U190, & U200) Address Decoder (A50U230, & U375A) Address Buffers (A50U350, U360, & U365) Data Buffers (A50U500 & U510).
10101	1,2	L,S	A	**Operation:** Tests ROM 00, A50U400. While executing, START key LED blinks and Test Number Set LED is on. When finished executing, START key LED goes out and Test Number Set LED blinks.
10102	1,2	L,S	A	**Operation:** Tests ROM 01, A50U390. While executing, START key LED blinks and Test Number Set LED is on. When finished executing, START key LED goes out and Test Number Set LED blinks.

Test Number	Level	Loop	A/M	Description
10200 - System RAM Tests				
10200	2	L,S	A	System RAM Test. **Operation:** Runs all 102xx subarea tests designated as Auto (A) in column 4. As each test is executed, its number is displayed in the Test Number Indicator. This test writes a 55H pattern to all RAM locations, then verifies the pattern in each location. Then it writes an AAH pattern to all locations and again verifies the pattern in each location. That part of RAM 11, which is used for the MPU stack, is tested with the kernel verification routine in Level 1 diagnostics rather than this routine. Devices tested: Address Decoder Buffers (A50U180, U190, U200) Address Decoders (A50U240) Address Buffers (A50U350, U360, & U365) Data Buffers (A50U500 & U510).
10201	1,2	L,S	A	**Operation:** Tests RAM 00, A50U300. While executing, START key LED blinks and Test Number Set LED is on. When finished executing, START key LED goes out and Test Number Set LED blinks.
10202	1,2	L,S	A	**Operation:** Tests RAM 01, A50U290. While executing START key LED blinks and Test Number Set LED is on. When finished executing, START key LED goes out and Test Number Set LED blinks.

Test Number	Level	Loop	A/M	Description
				20000 - DMA MODULE DIAGNOSTICS (A12/A16/A50/A52)
20000	2	L,S	A	DMA Module Test (A52 DMA Board). **Operation:** Runs all 20xxx area and subarea test designated as Auto (A) in column 4. When executed, the 3rd and 5th test number digits flicker to show that it is sequencing through the automatic tests.

Test Number	Level	Loop	A/M	Description
20100 - DMAC Tests				
20100	2	L,S	A	DMAC (DMA Controller) Test. **Operation:** Runs all 201xx subarea tests designated as Auto (A) in column 4.
20101	1,2	L,S	A	DMAC Internal Register R/W (Read/Write) Test. **Operation:** This test checks the following registers by writing a "55" pattern into each register, then verifies the pattern in the register. Then it writes an "AA" pattern into each register and again verifies the pattern. Channel Status — Channel Error (Read Only) Device Control — Operation Control Sequence Control — Channel Control Memory Address — Memory Transfer Counter Device Address — Device Function Code Base Address — Normal Interrupt Vector Channel Priority — Error Interrupt Vector General Control — Memory Function Code Base Transfer — Base Function Codes Devices tested: DMA Controller (A52U190) Data Bus Buffers (A52U100 & U110) Address Buffer (A52U140) Address Decoders (A50U240 & U250) Other (A50U470 & U210 and A52U150, U170 & U180).
20102	2	L,S	M	Transfers CH1 Waveform Memory to CH1 Display Memory. **Operation:** Tests the CH0 DMAC by writing a center line on 8K bytes of CH1 waveform memory (800000-801FFF), then transfers it to CH1 display memory (90000-91FFF) and compares the data in both memories. Tests the same devices as 20101 plus Address Latch (A52U120 & U130 and A52U180).

Test Number	Level	Loop	A/M	Description
20103	2	L,S	M	Transfers CH2 Waveform Memory to CH2 Display Memory. **Operation:** Tests the CH1 DMAC by writing a center line on 8K bytes of CH2 waveform memory (87E000-87FFFF), then transfers it to CH2 display memory (92000-93FFF) and compares the data in both memories. Tests the same devices as 20102.
20104	2	L,S	M	Transfers CH1 and CH2 Waveform Memory to CH1. and CH2 Display Memory. **Operation:** Tests CH2 DMAC by writing a center line on 16K bytes of waveform memory (83E000-841FFF), then transfers it to display memory (90000-93FFF) and compares the data in both memories. Tests the same devices as 20102.
20105	2	L,S	M	DMAC halt. **Operation:** Tests the availability of the DMAC halt operation by asserting the HALT signal, then starting a DMA transfer, and later verifies its completion. Next it deasserts the HALT signal, which automatically starts a DMA transfer. Later it verifies that the DMA transfer is complete and that the waveform and display memories are the same. Tests A52U300 & U280 and A52U160.

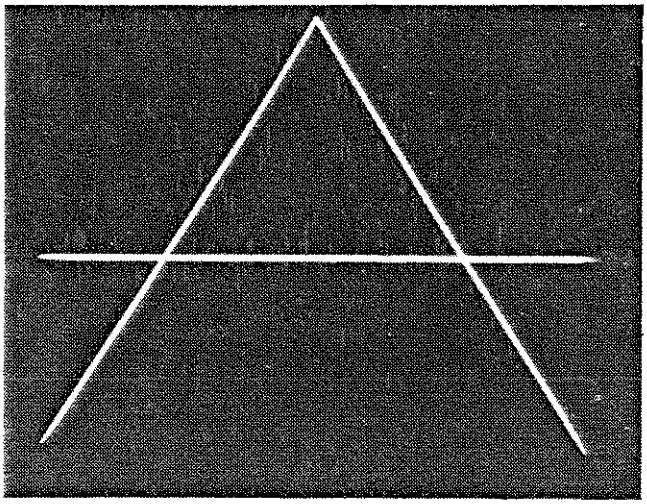
Test Number	Level	Loop	A/M	Description
20200 - Buzzer Tester				
20200	2	L,S	A	Buzzer Test. **Operation:** None.
20201	2	S	M	Enables the buzzer. **Operation:** Tests the buzzer by continually sending it a set of high-to-low frequencies in an increasingly faster repetitive pattern. Devices tested: Buzzer (A52LS250) Timer (A52U250) Register (A52U240) Decoder (A40U240). Push the STOP key to end the test.
20300 - Timer Test				
20300	2	L,S	A	Timer Test. **Operation:** None.
20301	1,2	L,S	A	Timer Interrupt Test. **Operation:** Tests the timer interrupt by clearing and enabling it, then verifying it is not zero. Next, the timer interrupt is disabled and cleared, then verified that it is zero. Devices tested: Timer Interrupt (A52U180) Timer Counter (A52U390, U420, U430, & U440) Enable/Disable Control (A52U290) Interrupt Decoder (A50U140).

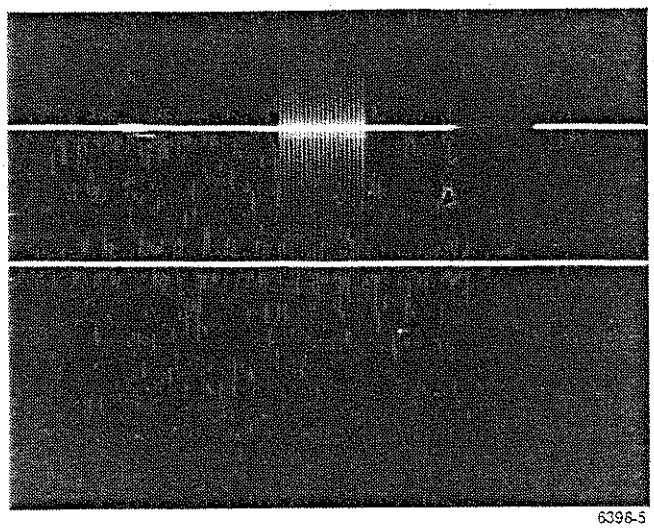
Test Number	Level	Loop	A/M	Description
20400 - Backup Battery Test				
20400	2	L,S	A	Backup Battery Test. **Operation:** Runs test 20401.
20401	1,2	L,S	A	Battery Test. **Operation:** Tests both batteries for sufficient voltage by reading two battery check bits. Tests Battery Check ICs (A52U330, U170, and U340).
20500 - Nonvolatile Memory Tests				
20500	2	L,S	A	Nonvolatile Memory (NVM) Test. **Operation:** None.
20501	1,2	L,S	M	Check Sum Test of NVM. **Operation:** Verifies that panel setup NVM hasn't changed since power down. When the instrument is powered down, current front panel settings are saved setting the NVM checksum. When the instrument is next powered up, it resets the front-panel settings to those that existed at power down. If the instrument is placed in the Level 2 diagnostics mode and this test executed, it should pass. If the instrument is placed in normal operation and has one front panel setting changed, then it is returned to Level 2 diagnostics and this diagnostic run, and error code E20501 should occur. Also, if this test is run again after running 20502, an error code E20501 should occur. Devices tested: NVM (A52U360 & U370) Address Buffer (A52U335A, U355A, & U140) Data Bus Buffer (A52U340 & U350) Address Decoder (A50U250A & U240) Chip Select (A52U180D, U280D, U320A, Q322).

Test Number	Level	Loop	A/M	Description
20502	2	L,S	M	Read/Write and Clear Test for NVM. **Operation:** Tests each NVM by first writing a "55" pattern to it, which is read and verified. Next, an "AA" pattern is written to each NVM, which also is read and verified. When the test is finished, all NVMs are cleared and a panel setup is initiated. This test is referenced in the calibration procedure as a means of clearing the Nonvolatile Memory. Tests the same devices as 20501.
20503	2	L,S	M	Read/Write Test for NVM. **Operation:** Performs the same test as 20502, except for Clear. When the test starts, the contents of the NVM under test are saved in System RAM. After the test, the saved contents are retrieved into the NVM tested. Tests the same devices as 20501.

Test Number	Level	Loop	A/M	Description
20600 - Probe Sense Tests				
20600	2	L,S	A	Probe Sense Test. **Operation:** None.
20601	2	S	M	CH1 Probe Sense Test. Setup: Connect an X1 probe to CH1, then run the test. Next, connect an X10 probe to CH1 and run the test. **Operation:** Checks for CH1 probe attenuation. With an X1 probe, a 1 is displayed in the Error Code Indicator; with an X10 probe, a 10 is displayed. With no probe attached, a 1 is displayed. Devices tested: CH1 Input (J100) Probe Sense (A12U450 & U822B) Read IC (A52U450A) Address Decoder (A52U220). Push the STOP key to end the test.
20602	2	S	M	CH2 Probe Sense Test. **Setup:** Connect an X1 probe to CH2, then run the test. Next, connect an X10 probe to CH2 and run the test. **Operation:** Checks for CH2 probe attenation. With an X1 probe, a 1 is displayed in the Error Code Indicator; with an X10 probe, a 10 is displayed. With no probe attached, a 1 is displayed. Devices tested: CH2 Input J102 Probe Sense (A14U910 & U840H) Read IC (A52U450B) Address Decoder (A52U220). Push the STOP key to end the test.

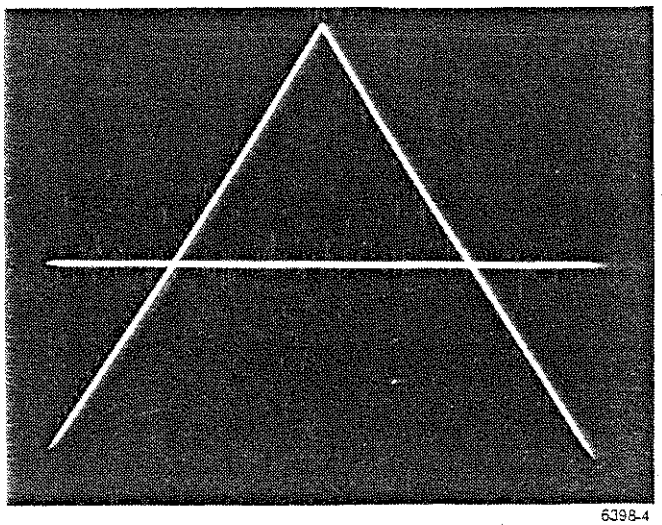
Test Number	Level	Loop	A/M	Description
				30000 - DISPLAY MODULE DIAGNOSTICS (A54/C56)
30000	2	L,S	A	Display Module Test. **Operation:** Runs test 30101 and 30102.
30100 - Display RAM Tests				
30100	2	L,S	A	Display RAM Test. **Operation:** Runs tests 30101 and 30102.
30101	1,2	L,S	A	CH1 Display RAM Test. **Operation:** Tests the Read/Write capability of the CH1 display RAM by writing an x555H (x is don't care) pattern on it, then reading and verifying the pattern. Next, an xAAAH pattern is written on the display RAM, then read and verified. During execution of the test, the monitor trace is momentarily blanked. Devices tested: CH1 Display RAM (A54U540, U550, and U560) Address Buffer (A54U100 & U110) Address MUX (A54U200, U210, U220, & U240) Memory Data Bus Buffer (U54U230) Address Decoder (A54U520) Control (A54U490, U510A, U600, U610).
30102	1,2	L,S	A	CH2 Display RAM Test. **Operation:** Tests the Read/Write capability of the CH2 display RAM by writing a x555H (x is don't care) pattern on it, then reading and verifying the pattern. Next, a xAAAH pattern is written on the display RAM, then read and verified. During execution of the test, the monitor trace is momentarily blanked. Tests the same devices as 30101, except CH1 Display RAM, plus CH2 Display RAM (A54U570, U580, & U590).

Test Number	Level	Loop	A/M	Description
30103	2	S	M	CH1 Display RAM, Write Test. **Operation:** Tests the write capability of the CH1 display RAM by writing center lines and triangle patterns on all display RAMs. During execution, the following pattern is displayed on the monitor:  6398-4 Devices tested: CH1 Display RAM (A54U540, U550, and U560) Read Data Latch (A54U640 & U650 and U56U360 & U370) D/A Converter (A56U410) CRT Drive (A56U430, U440A, U450, U470, U490, Q470, & Q471) Horizontal Counter (A54U340, U350, & U360) Address Adder (A54U150, U160 & U170) Address MUX (A54U200 & U210, U220) Data MUX (A54U660, U670, & U680) Data Latch (A56U380 & U390) X-Axis D/A Converter (A56U420). Push the STOP key to end the test.

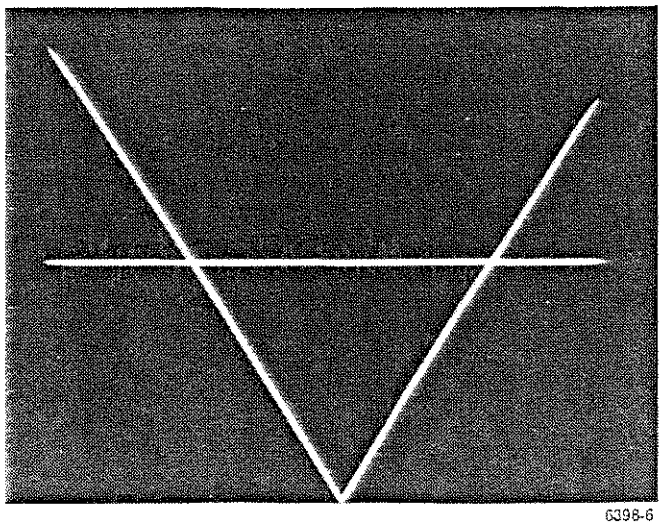
Test Number	Level	Loop	A/M	Description
30104	2	S	M	CH2 Display RAM, Write Test. **Operation:** Performs test 30103 on CH2 display RAM and has the same Monitor display. Tests the same devices as 30103, except CH1 Display RAM, plus CH2 Display RAM (A54U570, U580, & U590). Push the STOP key to end the test.
30105	2	S	M	CH1 Display RAM, Attribute Test. **Operation:** Tests the Lines, Dot Blank, Cursor, and Trigger Point attributes of the CH1 display RAM. This test writes center lines, vertical lines, a trigger point, cursor points, and dot blanks on the display RAMs. During execution, the following pattern is displayed on the monitor:  6396-5 Devices tested: Attribute Control (A56U100, U110, U120, U130, U140, & U150) Cursor Generator (A45U400 & U460) Retrace Control (A54U310A, U330, & 270B) Blanking (A54U270A, A56U480, Q480). Push the STOP key to end the test.

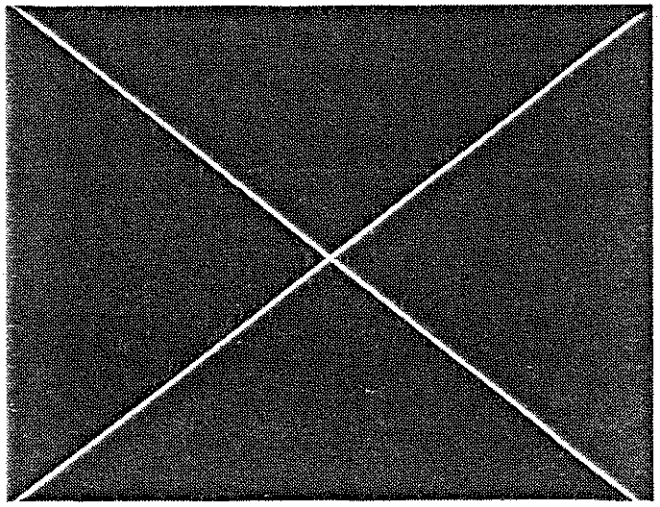
Test Number	Level	Loop	A/M	Description
30106	2	S	M	CH2 Display RAM, Attribute Test. **Operation:** Tests the Lines, Dot Blank, Cursor, and Trigger Point attributes of the CH2 display RAM by performing the same tests as for 30105 above. See 30105 above for monitor display. Tests the same devices as 30105 above. Push the STOP key to end the test.

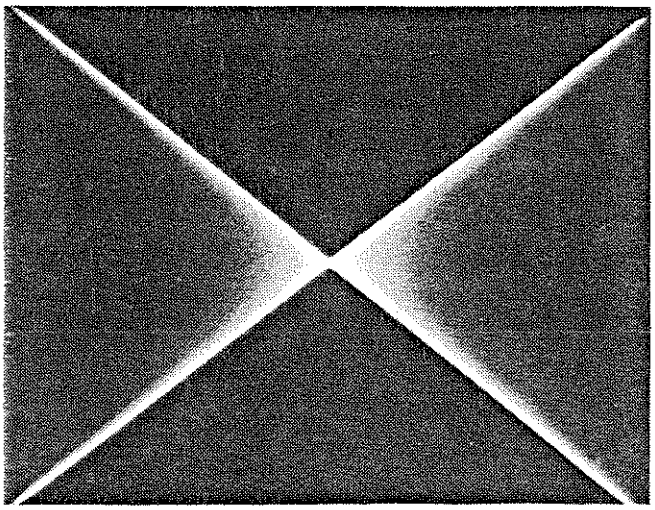
Test Number	Level	Loop	A/M	Description
30200 - Horizontal Scroll Tests				
30200	2	L,S	A	Horizontal Scroll Test. **Operation:** None.
30201	2	S	M	CH1 Horizontal Scroll Test. **Operation:** Tests the horizontal scroll capability of the CH1 display RAM. This test writes center lines and triangle patterns on the display RAM. Next, it scrolls the patterns from right to left to right. During execution, monitor pattern 1 below continuously scrolls 1/2 display to the left until it looks like monitor pattern 2, then it scrolls 1/2 display to the right to the original pattern, then repeats.



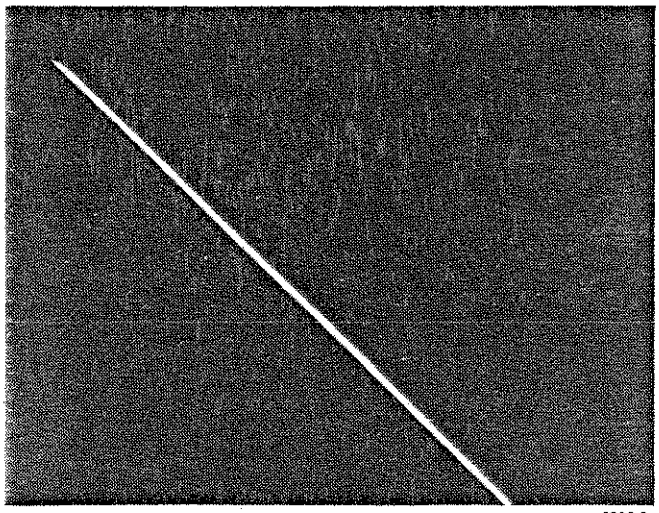
6398-4

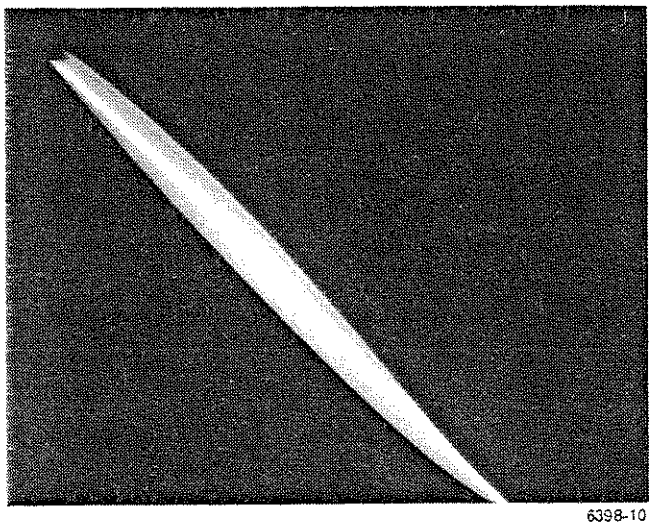
Test Number	Level	Loop	A/M	Description
Test 30201 (Cont.)				 6396-6 Devices tested: Scroll Register (A54U120, U130, & U140) Data Bus Buffer (A54U180 & U190) Address Adder (A54U150, U160 & U170) Address Buffer (A54U100 & U110) Address Decoder (A54U390) Other (A54U620). Push the STOP key to end the test.
30202	2	S	M	CH2 Horizontal Scroll Test. **Operation:** Tests the horizontal scroll capability of the CH2 display RAM by performing the same test as for 30201 above. During execution, this test has the same pattern as 30201 above. Tests the same devices as 30201 above. Push the STOP key to end the test.

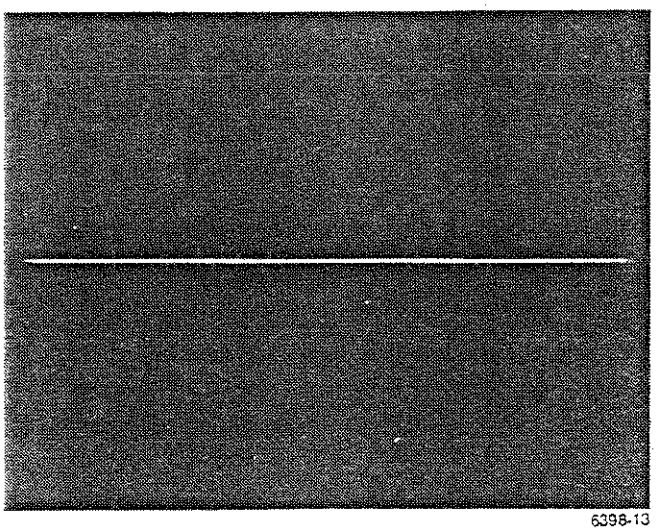
Test Number	Level	Loop	A/M	Description
30300 - Display Mode (YT/XY) Tests				
30300	2	L,S	A	Display Mode Test. **Operation:** None.
30301	2	S	M	Y-T (Dual Normal) and Dot Mode Test. **Operation:** Used to check the X, Y, and Z outputs in dot mode during calibration of the A56 Monitor Control Board. During execution, the following pattern is displayed on the monitor.  6398-7 Devices tested: Carry Counter Register (A54U380) Carry Counter (A54U410) Display Channel Select (A54U420 & U430) Mode Set (A54U440) Address Decoder (A54U390) Other (A54U450, U460, U470, U480, U495, & U500). Push the STOP key to end the test.

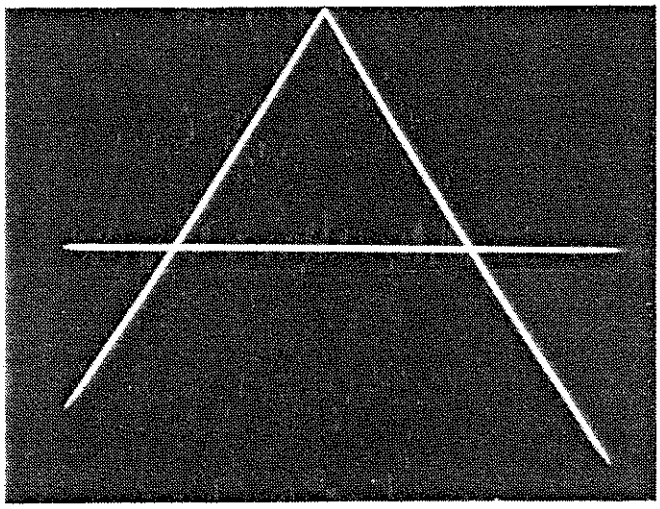
Test Number	Level	Loop	A/M	Description
30302	2	S	M	Y-T (Dual Normal) and Line Mode Test. **Operation:** Used to check and adjust the X, Y, and Z outputs, and Y bandwidth in line mode during calibration of the A56 Monitor Control Board. During execution, the following pattern is displayed on the monitor:  6398-8 Tests the same devices as 30301. Push the STOP key to end the test.
30303	2	S	M	Y-T (CH1: ENV, CH2: Normal) and Dot Mode Test. **Operation:** Tests the Y-T dot display mode. See 30301 above for setup location and monitor display. Tests the same devices as 30301. Push the STOP key to end the test.

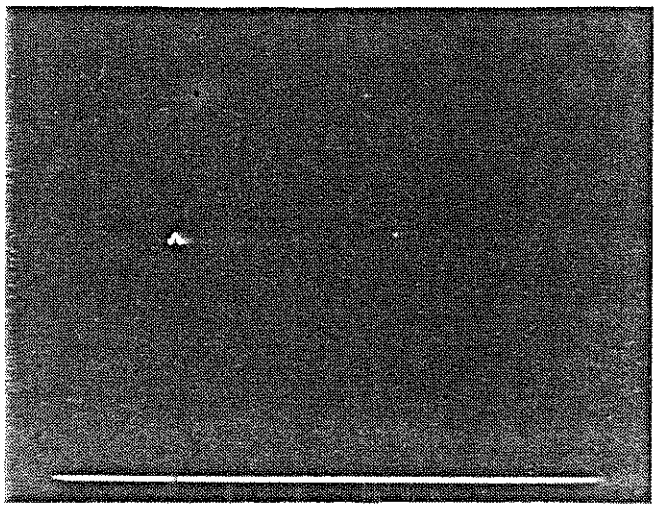
Test Number	Level	Loop	A/M	Description
30304	2	S	M	Y-T (CH1: ENV, CH2: Normal) and Line Mode Test. **Operation:** Tests the Y-T line display mode. See 30303 above for setup location and monitor display. Tests the same devices as 30301. Push the STOP key to end the test.
30305	2	S	M	Y-T (CH1: Normal, CH2: ENV) and Dot Mode Test. **Operation:** Tests the Y-T dot display mode. See 30301 above for setup location and monitor display. Tests the same devices as 30301. Push the STOP key to end the test.
30306	2	S	M	Y-T (CH1: Normal, CH2: ENV) and Line Mode Test. **Operation:** Tests the Y-T line display mode. See 30302 above for setup location and monitor display. Tests the same devices as 30301. Push the STOP key to end the test.
30307	2	S	M	Y-T (Dual ENV) and Dot Mode Test. **Operation:** Tests the Y-T dot display mode. See 30301 above for test setup and monitor display. Tests the same devices as 30301. Push the STOP key to end the test.
30308	2	S	M	Y-T (Dual ENV) and Line Mode Test. **Operation:** Tests the Y-T line display mode. See 30302 above for setup location and monitor display. Tests the same devices as 30301. Push the STOP key to end the test.

Test Number	Level	Loop	A/M	Description
30309	2	S	M	X-Y and Dot Mode Test. **Operation:** Used to check the X bandwidth in dot mode during calibration of the A56 Monitor Control Board. During execution, the following pattern is displayed on the monitor: Tests the same devices as 30301.  6398-9 Push the STOP key to end the test.

Test Number	Level	Loop	A/M	Description
30310	2	S	M	X-Y and Line Mode Test. **Operation:** Used to check and adjust the X bandwidth in line mode during calibration of the A56 Monitor Control Board. During execution, the following pattern is displayed on the monitor: Tests the same devices as 30301.  6398-10 Push the STOP key to end the test.

Test Number	Level	Loop	A/M	Description
30400 - Display Blanking Tests				
30400	2	S	A	Display Blanking Test. **Operation:** None.
30401	2	S	M	CH1 Blanking Test. **Operation:** Tests the blanking capability of the CH1 display RAM. This test writes a center line into CH2 display RAM and a triangle pattern into CH1 display RAM. Then during execution, the following pattern is displayed on the monitor (Note that the triangle pattern for CH1 is blanked):  6398-13 Push the STOP key to end the test.
30402	2	S	M	CH2 Blanking Test. **Operation:** Test the blanking capability of the CH2 display RAM. This test writes a center line into CH1 display RAM and a triangle pattern into CH2 display RAM. Then during execution, the following pattern is displayed on the monitor (Note that the triangle pattern for CH2 is blanked): Push the STOP key to end the test.

Test Number	Level	Loop	A/M	Description
30403	2	S	M	Read Counter Start/Stop Test. **Operation:** Tests the display RAM counter. This test writes a center line into CH1 display RAM and a triangle pattern into CH2 display RAM. Then it starts and stops the read counter, which turns the displays on and off. During execution, the following pattern is blanked off and on.  6398-4 Push the STOP key to end the test.

Test Number	Level	Loop	A/M	Description
30500 - Display Adjust Test				
30500	2	L,S	A	Display Adjust Test. **Operation:** None.
30501	2	S	M	Y Glitch Cancel Test. **Operation:** Used to check and adjust the Y Glitch Cancel during calibration of the A56 Monitor Control Board. This test displays center lines on all display RAMs, then writes F000H patterns from 0 to 988, writes an F9FFH pattern at 990, writes F200H + 1,2,...,F from 992 to 1022, writes F20FH - 0,1,2,...,F from 1024 to 1052, writes F9FFH pattern at 1054, and writes F000H patterns from 1056 to 4094. During execution, the following pattern is displayed on the monitor:  6396-12 Tests Y Glitch Cancel (A56C412). Push the STOP key to end the test.

Test Number	Level	Loop	A/M	Description
				40000 - GPIB MODULE DIAGNOSTICS (A56)
40000	2	L,S	A	GPIB Module Test. **Operation:** Runs test 40201.
40100 - TR Function Test				
40100	2	L,S	A	TR Function Test. **Operation:** None.
40101	1	S	A	9914 TR Function Test. **Operation:** (*Level 1 power-up diagnostic only*) Tests the 9914A. This test waits one second after power up, then verifies that the TR output is LOW. Next it issues a *fget, c/s=0* (Force Group Execute Trigger) command and waits 1 ms, then verifies that the TR output is HIGH. Finally, it issues a *fget, c/s=1* command and waits 1 ms. This test cannot be called from Level 2 diagnostics. Devices tested: GPIB TR Output (A56U310 pin 39 Gate IC (A56U320A) Buffer (A56U190).

Test Number	Level	Loop	A/M	Description
40200 - GPIB ADDER TESTS				
40200	2	L,S	A	GPIB Adder Test. **Operation:** Runs Test 40201.
40201	2	L,S	A	Adder Clear/Read/Write Test. **Operation:** Tests the /Read/Write and Clear capability of the adder used for GPIB transfer checksums. This test clears the adder, then writes a 5A pattern on it and reads and verifies the pattern. Next, it clears the adder and writes an A5 pattern on it and reads and verifies that pattern. Finally it writes a 11 pattern on the adder and reads and verifies the pattern. At the end of the test, it clears the adder. Devices tested: Adder (A56U240 & U250) Buffer (A56U200 & U210) Latch (A56U260).
40203	2	L,S	M	Adder Read/Write Check. **Operation:** Checks the Read/Write capability of the adder used for GPIB transfer checksums by writing a 5A pattern to the adder, then reading and verifying the pattern. Tests the same devices as 40201.

Test Number	Level	Loop	A/M	Description
40300 - Rotary Encoder Test (Parameter Entry Knob)				
40300	2	L,S	A	Rotary Encoder Test. **Operation:** None.
40301	2	S	M	Rotary Encoder Counts Test. **Operation:** Tests the up/down counting capability of the Rotary Encoder (Parameter Entry Knob). Once the START key is pushed, the Parameter Entry Knob can be infinitely rotated to set any value from 0 to 255 in the Error Code Indicator. When the value reaches 255, the next clockwise click sets it to 0; when it reaches 0, the next counterclockwise click sets it to 255. Devices tested: Rotary Encoder: (S250) Counter (A56U530 & U540) Control (A56U560, U500, U510, & U520) Buffer (A56U550). Push the STOP key to end the test.

Test Number	Level	Loop	A/M	Description
				50000 - KEY MODULE DIAGNOSTICS (A56/A60/A64)
50000	2	L,S	A	Key Module Test. **Operation:** Runs tests 50101, 50201, 50301, and 50401. The Test Number Indicator displays each test number as it runs. When finished, 50000 is redisplayed. If the START key is pushed and held during the test, an E50101 error code is forced.
50100 - Key Tests				
50100	2	L,S	A	Key Short Test. **Operation:** Runs test 50101. The Test Number Indicator displays the test number as it runs. When finished, 50100 is redisplayed. If the START key is pushed and held during the test, an E50101 error code is forced.
50101	1,2	L,S	A	Rough Sense Test. **Operation:** Tests front-panel key switches for shorts. If the START key is pushed and held during the test, an E50101 error code is forced. If an error code is displayed in the Error Code Indicator, that code is cleared when the test is started. Devices tested: Keys (A60S101-S410) Sense (A60U170 pin 15 & U200) Buffer (A60U180 & U190).

Test Number	Level	Loop	A/M	Description
50102	2	S	M	Key Sense Test. **Operation:** Used to test each push-to-select and toggle key. When this test is started, it turns off any key LEDs that were on and disables the Parameter Entry Knob. Whenever a push-to-select key is pushed, its LED illuminates. Whenever a toggle key is pushed up, all selections illuminate. Tests the same devices as 50101 plus Sense (A60U170 pins 11-14). Push the STOP key to end test. LEDs that were extinguished when the START key was pushed are turned on.

Test Number	Level	Loop	A/M	Description
50200 - Key LED Tests				
50200	2	L,S	A	Key LED Write Test. **Operation:** Runs test 50201.
50201	1,2	L,S	A	Key LED Write Test. **Operation:** Used during calibration to check all LEDs, except CH1/CH2 overflow arrow LEDs, 7-segment LEDs, and ARM'D/TRIG'D LEDs. When the test is started, it illuminates all LEDs, except those noted above. Devices tested: LEDs (A60DS101-DS451) LED Drivers (A60U320-U450).
50202	2	S	M	LED Set #1 Test. **Operation:** None. Push the STOP key to end test.
50203	2	S	M	LED Set #2 Test. **Operation:** Turns on these LEDs or indicators: BUSY NO-OPTION GPIB (LOCK & REM) Tests LED Driver A630U390 and its associated LEDS. Push the STOP key to end test.
50204	2	S	M	LED Set #3 Test. **Operation:** Turns on these LEDs or indicators: RANGE OFFSET TRIG LEVEL ARM DELAY TRIG DELAY Tests LED Driver A60U395 and its associated LEDS. Push the STOP key to end test.

Test Number	Level	Loop	A/M	Description
50205	2	S	M	LED Set #4 Test. **Operation:** Turns on these LEDs or indicators: VERT MODE — TRIG SOURCE BW LIM 25 MHZ — CLK SOURCE AUTO CAL Tests LED Driver A60U320 and its associated LEDs. Push the STOP key to end test.
50206	2	S	M	LED Set #5 Test. **Operation:** Turns on these LEDs or indicators: AVE/ENV # OF TIMES — Breakpoint SET SAMPLE INTERVAL — Breakpoint DISPLAY RECORD LENGTH — SAVE/LOC RECORD LOCATION — RECALL/LOC Tests LED Driver A60U400 and its associated LEDs. Push the STOP key to end test.
50207	2	S	M	LED Set #6 Test. **Operation:** Turns on these LEDs or indicators: SAMPLE MODE — SCROLL RESET/HOLD — GPIB RQS ID Tests LED Driver A60U330 and its associated LEDs. Push the STOP key to end the test.
50208	2	S	M	LED Set #7 Test. **Operation:** Turns on these LEDs or indicators: DISPLAY (CH1/CH2) — DISPLAY LOCATION VERT ZOOM — VERT POSN HORIZ ZOOM — CURSOR 1, 2 Tests LED Driver A60U410 and its associated LEDs. Push the STOP key to end test.

Test Number	Level	Loop	A/M	Description
50209	2	S	M	LED Set #8 Test. **Operation:** Turns on these LEDs or indicators: DISPLAY (Dot/Line) MEASURE (V, T & 1/T) DISPLAY (YT/XY) INIT MON CAL PLOT Tests LED Driver A60U340 and its associated LEDs. Push the STOP key to end test.
50210	2	S	M	LED Set #9 Test. **Operation:** Turns on these LEDs or indicators: Trigger COUPLING (REJ & TV) Tests LED Driver A60U420 and its associated LEDs. Push the STOP key to end test.
50211	2	S	M	LED Set #10 Test. **Operation:** Turns on these LEDs or indicators: Input COUPLING (CH1 & CH2) Tests LED Driver A60U350 and its associated LEDs. Push the STOP key to end test.
50212	2	S	M	LED Set #11 Test. **Operation:** Turns on these LEDs or indicators: Trigger SLOPE RECORD MODE Test LED Driver A60U430 and its associated LEDs. Push the STOP key to end test.
50213	2	S	M	LED Set #12 Test. **Operation:** Turns on these LEDs or indicators: Trigger MODE Tests LED Driver A60U360 and its associated LEDs. Push the STOP key to end test.

Test Number	Level	Loop	A/M	Description
50214	2	S	M	LED Set #13 Test. **Operation:** Turns on the units of measure displays for the 7-segment Trigger Indicator. Tests LED Driver A60U440 and its associated LEDs. Push the STOP key to end test.
50215	2	S	M	LED Set #14 Test. **Operation:** Turns on the units of measure displays for the 7-segment Input Indicator. Tests LED Driver A60U370 and its associated LEDs. Push the STOP key to end test.
50216	2	S	M	LED Set #15 Test. **Operation:** Turns on the units of measure displays for the 7-segment Control Indicator. Tests LED Driver A60U450 and its associated LEDs. Push the STOP key to end test.
50217	2	S	M	LED Set #16 Test. **Operation:** Turns on the units of measure displays for the 7-segment Time Base and Recording Indicators. Tests LED Driver A60 U380 and its associated LEDs. Push the STOP key to end test.

Test Number	Level	Loop	A/M	Description
50300 - Keyboard Option Test				
50300	2	L,S	A	Keyboard Option Test. **Operation:** Runs the 50301 test.
50301	1,2	L,S	A	Keyboard Option Read Test. **Operation:** Tests the availability of the front-panel option signal. It reads the signal and verifies that the option signal is valid. Devices tested: Standard Keyboard IC (A60U120B) Option 19 Keyboard IC (A64U100B).

Test Number	Level	Loop	A/M	Description
50400 - 7-Segment LED Tests				
50400	2	L,S	A	7-Segment LED Test **Operation:** Runs test 50401.
50401	1,2	L,S	A	7-Segment LED Write Test. **Operation:** Used during calibration to check all 7-segment LED indicators. Writes "8." into all 7-segment LEDs. Devices tested: 7-Segment LEDs (A60DS260-DS297) LED Drivers (A60U260-U290) Control (A60U230 & U240).
50402	2	S	M	7-Segment Driver Code & CH2 Overflow Bit Test. **Operation:** Writes "P." into all 7-segment LEDs for about 2 seconds, then writes "E." into all 7-segment LEDs for about 2 seconds, then repeats until the STOP key is pushed. Devices tested: LED Drivers (A56U260-U290) Mode Select (A60U240). Push the STOP key to end test.
50403	2	S	M	7-Segment Driver #1 Test. **Operation:** Writes "8." to the 7-segment Input Indicator. Tests LED Driver A60U260. Push the STOP key to end test.
50404	2	S	M	7-Segment Driver #2 Test. **Operation:** Writes "8." to the 7-segment Trigger Indicator and the left end segment of Recording Indication. Tests LED Driver A60U270. Push the STOP key to end test.

Test Number	Level	Loop	A/M	Description
50405	2	S	M	7-Segment Driver #3 Test. **Operation:** Writes "8." to the 7-segment Time Base and Recording Indicators (except left end segment). Tests LED Driver A60U280. Push the STOP key to end test.
50406	2	S	M	7-Segment Driver #4 Test. **Operation:** Writes "8." to the 7-segment Control Indicator. Tests LED Driver A60U290. Push the STOP key to end test.

Test Number	Level	Loop	A/M	Description
				60000 - INPUT, DC-CAL, GAIN-CAL, TRIGGER, AND TV TRIGGER DIAGNOSTICS (A12/A14/A22/A24)
60000	2	L,S	A	Input Amplifier Test. **Operation:** Runs all 60xxx area and subarea tests designated as Auto (A) in column 4. The only indication that the test numbers are being displayed is a flicker in the 3rd and 5th digits of the the 7-segment Test Number Indicator.
60100 - CH1 Input Tests				
60100	2	L,S	A	CH1 Input Amplifier Test. **Operation:** Runs all 601xx subarea tests designated Auto (A) in column 4. The only indication that the test numbers are being displayed is a flicker in the 5th digit of the the 7-segment Test Number Indicator.
60101	1,2	L,S	A	CH1 Input Coupling Test. **Operation:** Tests these functions of the CH1 Input Coupling Register: DC and Phase Calibration AC Coupling Input GND DC Coupling Gain Calibration. Devices tested: CH1 Input Coupling Register (A12U812) Buffer (A12U810A, B, C, & D).
60102	1,2	L,S	A	CH1 Amplifier Gain Test. **Operation:** Tests the CH1 Amplifier Gain Register by writing a value to it, then reading the value and comparing it to the register. In this test, signal lines of GD10 and GD11 are verified. Devices tested: CH1 Amplifier Gain Register (A12U814) Buffer (A12U810E, F, & G).

Test Number	Level	Loop	A/M	Description
60103	1,2	L,S	A	CH1 Amplifier Register Test. **Operation:** Tests the Read/Write capability of the CH1 Amplifier hardware register by writing a value to it, then reading the value and comparing it to the register. In this test, read back bit (GD15) of A12U814 is verified. Tests the same devices as 60102.
60107	2	S	M	CH1 DC CAL Span Test. **Operation:** Used to check the CH1 DC CAL function during calibration. Devices tested: CH1 D/A Converter (A14U400) Other (A14U410) Push the STOP key to end the test.
60109	2	S	M	CH1 Gain CAL Span Test. **Operation:** Used to check CH1 GAIN CAL function during calibration. Devices tested: CH1 D/A Converter (A14U400) Other (A14U410, U420, U430, & U440). Push the STOP key to end the test.
60115	2	S	M	CH1 DC CAL Signal Test. **Operation:** Used to check and adjust the CH1 DC BALANCE and to check the CH1 DC CAL function during calibration. Tests CH1 DC Balance (A14R108 (for M377)) and A12R214 (for interface amp module)). Push the STOP key to end the test.

Test Number	Level	Loop	A/M	Description
60157	2	S	M	CH1 DC CAL Span Test in High Speed Mode. **Operation:** Tests the CH1 DC CAL function while in the High-Speed Mode. For test setups and procedures, use the calibration procedures where test 60107 is used for checking CH1 DC CAL. Tests the same devices as 60107. Push the STOP key to end the test.
60159	2	S	M	CH1 Gain CAL Span Test in High Speed Mode. **Operation:** Tests the CH1 Gain CAL function, while in the high-speed mode. For test setups and procedures, use the calibration procedures where test 60109 is used for checking CH1 GAIN CAL. Tests the same devices as 60109. Push the STOP key to end the test.

Test Number	Level	Loop	A/M	Description
60200 - CH2 Input Tests				
60200	2	L,S	A	CH2 Input Amplifier Test. **Operation:** Runs all 602xx subarea tests designated as Auto (A) in column 4. The only indication that the tests are being run and their numbers are being displayed is a flicker in the 5th digit of the 7-segment Test Number Indicator.
60201	1,2	L,S	A	CH2 Input Coupling Test. **Operation:** Tests these functions of the CH2 Input Coupling Register: DC and Phase Calibration AC Coupling Input GND DC Coupling Gain Calibration. Devices tested: CH2 Input Coupling Register (A12U912) Buffer (A12U910A, B, C, & D).
60202	1,2	L,S	A	CH2 Amplifier Gain Test. **Operation:** Tests the CH2 Amplifier Gain Register by by writing a value to it, then reading the value and comparing it to the register. In this test signal lines of GD10 and GD11 are verified. Devices tested: CH2 Amplifier Register (A12U914) Buffer (A12U910E, F, & G).
60203	1,2	L,S	A	CH2 Amplifier Register Test. **Operation:** Tests the Read/Write capability of the CH2 Amplifier hardware register by writing a value to it, then reading the value and comparing it to the register. In this test, read back bit (GD15) of A12U914 is verified. Tests the same devices as 60202.

Test Number	Level	Loop	A/M	Description
60207	2	S	M	CH2 DC CAL Span Test. **Operation:** Used to check the CH2 DC CAL function during calibration. Adjust A12R654 to match the offset voltage between CH1 and CH2 amp. Devices tested: CH2 D/A Converter (A14U500) Other (A14U510). Push the STOP key to end the test.
60209	2	S	M	CH2 Gain CAL Span Test. **Operation:** Used to check the CH2 GAIN CAL function during calibration. Devices tested: CH2 D/A Converter (A14U500) Other (A14U510, U520, U530, & U440). Push the STOP key to end the test.
60215	2	S	M	CH2 DC CAL Signal Test. **Operation:** Used to check and adjust the CH2 DC BALANCE, and to check the CH2 DC CAL function during calibration. Tests CH2 DC Balance (A14R208 (M377) and A12R654). Push the STOP key to end the test.

Test Number	Level	Loop	A/M	Description
60257	2	S	M	CH2 DC CAL Span Test in High Speed Mode. **Operation:** Tests the CH2 DC CAL function while in the High-Speed Mode. For test setups and procedures, use the calibration procedures where test 60207 is used for checking CH2 DC CAL. Adjust A14R516 to match the CH2 offset voltage of A12U600 to that of H1 (A12U200). Devices tested: CH2 D/A Converter (A14U500) Other (A14U510B, U510D and A12U650). Push the STOP key to end the test.
60259	2	S	M	CH2 Gain CAL Span Test in High Speed Mode. **Operation:** Tests the CH2 GAIN CAL function while in the high-speed mode. For test setups and procedures, use the calibration procedures where test 60209 is used for checking CH2 GAIN CAL. Devices tested: CH2 D/A Converter (A14U500) Other (A14U510A and A12U650, & Q650). Push the STOP key to end the test.

Test Number	Level	Loop	A/M	Description
60300 - Calibration Tests				
60300	2	L,S	A	Calibration Test. **Operation:** Runs all 603xx subarea tests designated as Auto (A) in column 4.
60301	1,2	L,S	A	Gain CAL Signal Setup Test. **Operation:** Tests the Gain CAL signal setup register by writing a value to it, then reading the value and comparing it to the register. Devices tested: Gain Cal Setup Register (A14U870) Buffer (A14U840A, B, & C).
60302	1,2	L,S	A	CH1 Input Offset Range Setup Test. **Operation:** Tests the CH1 Input Offset Range register by)ting a value to it, then reading the value and comparing it to the register. Devices tested: CH1 Input Offset Register (A14U850) Buffer (A14U840A, B, & C).
60303	1,2	L,S	A	CH2 Input Offset Range Setup Test. **Operation:** Tests the CH2 Input Offset Range register by writing a value to it, then reading the value and comparing it to the register. Devices tested: CH2 Input Offset Register (A14U860) Buffer (A14U840A, B, & C).
60304	1,2	L,S	A	CH1/CH2 Input Offset Polarity Setup Test. **Operation:** Tests the Input Offset Polarity register by writing a value to it, then reading the value and comparing it to the register. Devices tested: Input Offset Polarity Register (A14U880) Buffer (A14U840D).

Test Number	Level	Loop	A/M	Description
60306	2	S	M	Gain CAL Reference Signal Test. **Operation:** Used to check and adjust the GAIN CAL Reference Signal waveform during calibration. When this test is selected and started, the Test Number Set and START key LEDs illuminate, the Data Set LED blinks, and the Parameter Entry Knob can be used to set a value of 0-27 in the Set Data Indicator. Tests Gain Cal Ref (A14U300, U310, U320, U330, U340, U350, & Q300-Q306). Push the STOP key to end the test.
60307	2	S	M	Gain CAL Reference Signal Test. **Operation:** Used to check and adjust the GAIN CAL Reference signal voltage during calibration. When this test is selected and started, the Test Number Set and START key LEDs illuminate, the Data Set LED blinks, and the Parameter Entry Knob can be used to set a value of 0-27 in the Set Data Indicator. Tests the same devices as 60306.

Test Number	Level	Loop	A/M	Description
60400 - Trigger Tests				
60400	2	L,S	A	Trigger Test **Operation:** Runs all 604xx subarea tests designated Auto (A) in column 4.
60401	1,2	L,S	A	Trigger Generator Setup Test #1. **Operation:** Tests the Read/Write capabilities of the Trigger Generator register by writing a value to it, then reading the value and comparing it to the register. Devices tested: Trigger Generator Register (A22U600) Buffer (A22U650).
60402	1,2	L,S	A	Trigger Generator Setup Test #2. **Operation:** Tests the Read/Write capabilities of the Trigger Generator register by writing a value to it, then reading the value and comparing it to the register. Devices tested: Trigger Generator Register (A22U610) Buffer (A22U650).

Test Number	Level	Loop	A/M	Description
60500 - TV Trigger Tests				
60500	2	L,S	A	TV Trigger Test. **Operation:** Runs all 605xx subarea tests designated as Auto (A) in column 4.
60501	1,2	L,S	A	TV Trigger Setup Test. **Operation:** Tests the TV Trigger register by writing a value to it, then reading the value and comparing it to the register. Devices tested: TV Trigger Register (A22U680) Buffer (A22U670).
60502	1,2	L,S	A	TV Clamp Time Constant Test. **Operation:** Tests the TV Trigger time constant register by writing a value to it, then reading the value and comparing it to the register. Devices tested: TV Trigger Register (A22U690) Buffer (A22U670).
60503	1,2	L,S	A	TV Option ID Test. **Operation:** Tests the TV Option register (A24U860) by writing a value to it, then reading the value and comparing it to the register. Devices tested: TB Option Register (A22U670) Cable Assembly (W240).

Test Number	Level	Loop	A/M	Description
60504	2	S	M	TV Line Counter Test. **Operation:** Tests the TV Line Counter function. When a standard amplitude TV signal is applied to CH1, the number of lines of the TV signal is displayed in the Error Code Indicator. Devices tested: Line Counter (A24U420 & U430A) Latch (A24U440 & U450) Buffer (A22U660 & U670). Push the STOP key to end test.

Test Number	Level	Loop	A/M	Description
60900 - Trigger Circuit Tests				
60900	1,2	L,S	A	Vertical System/Trigger circuit Test. **Operation:** Runs all 609xx subarea tests designated as Auto (A) in column 4.
60901	1,2	L,S	A	CH1 Vertical System/Trigger Circuit Test. **Operation:** Tests the CH1 1 Input and trigger circuits, CH1 A/D Converter, main signal path of the Envelope board, and that part of waveform memory not tested by 80200. The test uses the 1 kHz Gain Cal Reference Signal as a known signal, which is fed to the trigger circuit by setting the trigger source to CH1. The trigger output at A22TP500 should be a 1 kHz square wave. The MPU checks the trigger pulse width, and if both the positive and negative pulse widths are 500 us, the test passes. Also, the 1 kHz signal is digitized and stored into waveform memory using the 1us sampling interval, NORMal sampling mode, and 10 V input range settings. When the acquisition is completed, the acquired signal is checked. This acquisition test is not performed when the Battery Backup strap on the A40 Address Generator board is set to the backup position, which may have been done to prevent erasure of the previously acquired waveform data. In this case, only the trigger circuit is tested. This test assumes the Gain Cal Reference Signal, CH1 Input Amp, Time Base, and Address Generator are working. This test may generate the following event codes: E00340 CH1 trigger error. E00341 CH1 ACQ not stopped. E00342 CH1 vertical system error. Tests: All trigger circuits except CH2, External Trigger selector, and TV Trigger. The Trigger Output signal (RDBK3) is read through buffer A22U650).

Test Number	Level	Loop	A/M	Description
60902	1,2	L,S	A	CH2 Vertical System/Trigger Circuit Test. **Operation:** This test is identical to 60901, except it tests the CH2 Input and trigger circuits, CH2 A/D Converter, main signal path of the Envelope board, and that part of waveform memory not tested by 80200. Tests the same devices as 60901. This test may generate the following event codes: E00345 CH2 trigger error. E00346 CH2 ACQ not stopped. E00347 CH2 vertical system error.

Test Number	Level	Loop	A/M	Description
70000 - TIME BASE, AUTO-CAL, AND PHASE-CAL DIAGNOSTICS (A32)				
70000	2	L,S	A	Timebase/Auto-Cal Test. **Operation:** Runs tests 70701 and 70702. Tests the clock delay setting switch A32S450.
70100 - Phase Cal Reference Waveform Tests				
70100	2	L,S	A	Phase CAL Test. **Operation:** None.
70101	2	S	M	Phase CAL Reference Waveform Test. **Operation:** Used to check and adjust the Phase CAL Reference Signal during calibration of the Phase Calibrator. When this test is started, the overrange indicators are cleared, the START key LED blinks, and the ARM'D and TRIG'D LEDs blink. Push the STOP key to end test.

Test Number	Level	Loop	A/M	Description
70200 - Auto-Cal Test				
70200	2	L,S	A	Auto CAL Test. **Operation:** None.
70201	2	L,S	M	Auto Calibration Test. **Operation:** Tests the Auto CAL function. When this test is started, the ARM'D and TRIG'D LEDs flash once. This test is typically run after an E350 Auto CAL failure Event Code occurs. It may generate any of the following Error Codes. E00360 CH1 DC Cal acquisition not stopped. E00361 CH1 DC Cal too high. E00362 CH1 DC Cal too low. E00363 CH1 DC Cal not terminated. E00364 CH2 DC Cal acquisition not stopped. E00365 CH2 DC Cal too high. E00366 CH2 DC Cal too low. E00367 CH2 DC Cal not terminated. E00368 CH1 gain Cal acquisition not stopped. E00369 CH1 gain Cal too high. E00370 CH1 gain Cal too low. E00371 CH1 Gain Cal not terminated. E00372 CH2 Gain Cal acquisition not stopped. E00373 CH2 Gain Cal too high. E00374 CH2 Gain Cal too low. E00375 CH2 Gain Cal not terminated. E00376 Phase Cal acquisition not stopped. E00377 Phase Cal clock advanced. E00378 Phase Cal clock delayed. E00379 Phase Cal not terminated. E00380 Phase Cal address not found.

Test Number	Level	Loop	A/M	Description
70500 - Phase Cal Tests				
70500	2	L,S	A	Phase CAL Span Test. **Operation:** None.
70501	2	S	M	Phase Calibration Compensation D/A Test. **Operation:** Tests the Phase Calibration D/A using the Parameter Entry Knob. When this test is started, the Test Number Set and START key LEDs illuminate, and the Data Set LED blinks indicating the Parameter Entry Knob can be used to enter a value from 0-225. Check the output of the Phase Cal D/A Converter (A32U460) with an Oscilloscope or DVM to verify that the output voltage varies from –0.32 to –0.86 V when the Parameter Entry Knob is rotated in both directions. Devices tested: Phase Cal D/A (A32U460) Data Register (A32U114) Data Bus Buffer (A32U106) Address Decoder (A32U100). Push the STOP key to end test.

Test Number	Level	Loop	A/M	Description
70700 - Breakpoint Tests				
70700	2	L,S	A	Breakpoint Tests. **Operation:** Runs all 707xx subarea tests designated as Auto (A) in column 4.
70701	1,2	L,S	A	Breakpoint Location Test. **Operation:** Tests the breakpoint location RAM by writing a 5555H to even addresses and an AAAAH to odd addresses and writing AAAAH to the breakpoint location counter. Next, the breakpoint location RAM address counter is cleared and up counting is started. During the upcount, the comparator output is verified to be turning on and off with the upcount. Devices tested: Breakpoint RAM (A32U210, U212, U214, & U216) Location Counter (A32U220, U222, U224, & U226) Address Counter (A32U200) Comparator (A32U230 & U232) Other (A32U242).
70702	1,2	L,S	A	Breakpoint Location Counter Test. **Operation:** Tests the breakpoint location counter by writing a 4FFFH pattern on the breakpoint location RAM, loading a 501FH pattern on the breakpoint location counter, and setting the break point location to counter mode. Next, verify that the comparator output is turned on after 1FH counts. Tests the same devices as 70701.

Test Number	Level	Loop	A/M	Description
70900 Sampling Clock Test				
70900	2	L,S	A	Sampling Clock Test. **Operation:** Runs test 70901.
70901	1,2	L,S	A	Sampling Clock Test. **Operation:** This test uses the CH2 clock path to verify that the internal sampling clock is operating properly. The test sets the sample interval clock to 1 ms, then sends it through the A/D board to the A30 Envelope board where it is divided down to 8 ms and sent to the Clock Flag flip-flop on the A40 Address Generator board. The MPU then checks the Clock Flag for an 8 ms clock. Tests: 200 MHz crystal oscillator (A76Y100) Clock Source Selector (A32U400) 1/2 Divider (A32U404) Normal Sample Clock Generator (A32U436) Buffer (A32U472A & C) Clock Output Selector (A32U454) Pre-Scaler (A32U320) Decade Divider (A32U322 thru U334, U342, U344, U470C) Sample Interval RAM (A32U300 & U302) Sample Interval Code Decoder (A32U308 & U310) Rate Latch (A32U312 & U314) CH2 A/D Clock Path Clock Buffer (A30U300C & U302) 1/2 Divider (A30U320 & U322) 1/4 Divider and Timing Ckts (A30U344, U340D, U346A, U342B, and delay lines.) Buffer (A40U290) Clock Flag Flip-Flop (A40U312A) Buffer (A40U330) Data Bus Buffer (A40U122) Address Decoder (A40U116).

Test Number	Level	Loop	A/M	Description
				80000 - MEMORY (A36/A40/A44)
80000	2	L,S	A	Memory/Averager/Address Generator Test. **Operation:** Runs all 80xxx area and subarea tests designated as Auto (A) in column 4. During execution, each test number is displayed in the Test Number Indicator while it is running.
80200 - Acquisition Memory Tests				
80200	2	L,S	A	Acquisition Memory Test. **Operation:** Runs all the 802xx subarea tests designated as Auto (A) in column 4. This test writes a 2AAH pattern on acquisition memory, then reads and verifies the pattern. Next, it writes a 155H pattern on acquisition memory, then reads and verifies the pattern. During execution, each test number is displayed in the Test Number Indicator while it is running.
80201	1,2	L,S	A	CH1 Acquisition RAM (A36U300) and Data Buffers (U400 & U440) Test.
80202	1,2	L,S	A	CH1 Acquisition RAM (A36U302) and Data Buffers (U400, U402 & U440) Test.
80203	1,2	L,S	A	CH1 Acquisition RAM (A36U304) and Data Buffers (U402 & U442) Test.
80204	1,2	L,S	A	CH1 Acquisition RAM (A36U306) and Data Buffers (U404 & U440) Test.
80205	1,2	L,S	A	CH1 Acquisition RAM (A36U308) and Data Buffers (U404, U406 & U440) Test.

Test Number	Level	Loop	A/M	Description
80206	1,2	L,S	A	CH1 Acquisition RAM (A36U310) and Data Buffers (U406 & U442) Test.
80207	1,2	L,S	A	CH1 Acquisition RAM (A36U312) and Data Buffers (U408 & U440) Test.
80208	1,2	L,S	A	CH1 Acquisition RAM (A36U314) and Data Buffers (U408, U410 & U440) Test.
80209	1,2	L,S	A	CH1 Acquisition RAM (A36U316) and Data Buffers (U410 & U442) Test.
80210	1,2	L,S	A	CH1 Acquisition RAM (A36U318) and Data Buffers (U412 & U440) Test.
80211	1,2	L,S	A	CH1 Acquisition RAM (A36U320) and Data Buffers (U412, U414 & U440) Test.
80212	1,2	L,S	A	CH1 Acquisition RAM (A36U322) and Data Buffers (U414 & U442) Test.
80213	1,2	L,S	A	CH1 Acquisition RAM (A36U324) and Data Buffers (U416 & U440) Test.
80214	1,2	L,S	A	CH1 Acquisition RAM (A36U326) and Data Buffers (U416, U418 & U440) Test.
80215	1,2	L,S	A	CH1 Acquisition RAM (A36U328) and Data Buffers (U418 & U442) Test.
80216	1,2	L,S	A	CH1 Acquisition RAM (A36U330) and Data Buffers (U420 & U440) Test.
80217	1,2	L,S	A	CH1 Acquisition RAM (A36U332) and Data Buffers (U420, U422 & U440) Test.
80218	1,2	L,S	A	CH1 Acquisition RAM (A36U334) and Data Buffers (U422 & U442) Test.
80219	1,2	L,S	A	CH1 Acquisition RAM (A36U336) and Data Buffers (U424 & U440) Test.
80220	1,2	L,S	A	CH1 Acquisition RAM (A36U338) and Data Buffers (U424, U426 & U440) Test.
80221	1,2	L,S	A	CH1 Acquisition RAM (A36U340) and Data Buffers (U426 & U442) Test.
80222	1,2	L,S	A	CH1 Acquisition RAM (A36U342) and Data Buffers (U428 & U440) Test.

Test Number	Level	Loop	A/M	Description
80223	1,2	L,S	A	CH1 Acquisition RAM (A36U344) and Data Buffers (U428, U430 & U440) Test.
80224	1,2	L,S	A	CH1 Acquisition RAM (A36U346) and Data Buffers (U430 & U442) Test.
80225	1,2	L,S	A	CH2 Acquisition RAM (A36U300) and Data Buffers (U400 & U440) Test.
80226	1,2	L,S	A	CH2 Acquisition RAM (A36U302) and Data Buffers (U400, U402 & U440) Test.
80227	1,2	L,S	A	CH2 Acquisition RAM (A36U304) and Data Buffers (U402 & U442) Test.
80228	1,2	L,S	A	CH2 Acquisition RAM (A36U306) and Data Buffers (U404 & U440) Test.
80229	1,2	L,S	A	CH2 Acquisition RAM (A36U308) and Data Buffers (U404, U406 & U440) Test.
80230	1,2	L,S	A	CH2 Acquisition RAM (A36U310) and Data Buffers (U406 & U442) Test.
80231	1,2	L,S	A	CH2 Acquisition RAM (A36U312) and Data Buffers (U408 & U440) Test.
80232	1,2	L,S	A	CH2 Acquisition RAM (A36U314) and Data Buffers (U408, U410 & U440) Test.
80233	1,2	L,S	A	CH2 Acquisition RAM (A36U316) and Data Buffers (U410 & U442) Test.
80234	1,2	L,S	A	CH2 Acquisition RAM (A36U318) and Data Buffers (U412 & U440) Test.
80235	1,2	L,S	A	CH2 Acquisition RAM (A36U320) and Data Buffers (U412, U414 & U440) Test.
80236	1,2	L,S	A	CH2 Acquisition RAM (A36U322) and Data Buffers (U414 & U442) Test.
80237	1,2	L,S	A	CH2 Acquisition RAM (A36U324) and Data Buffers (U416 & U440) Test.
80238	1,2	L,S	A	CH2 Acquisition RAM (A36U326) and Data Buffers (U416, U418 & U440) Test.
80239	1,2	L,S	A	CH2 Acquisition RAM (A36U328) and Data Buffers (U418 & U442) Test.

Test Number	Level	Loop	A/M	Description
80240	1,2	L,S	A	CH2 Acquisition RAM (A36U330) and Data Buffers (U420 & U440) Test.
80241	1,2	L,S	A	CH2 Acquisition RAM (A36U332) and Data Buffers (U420, U422 & U440) Test.
80242	1,2	L,S	A	CH2 Acquisition RAM (A36U334) and Data Buffers (U422 & U442) Test.
80243	1,2	L,S	A	CH2 Acquisition RAM (A36U336) and Data Buffers (U424 & U440) Test.
80244	1,2	L,S	A	CH2 Acquisition RAM (A36U338) and Data Buffers (U424, U426 & U440) Test.
80245	1,2	L,S	A	CH2 Acquisition RAM (A36U340) and Data Buffers (U426 & U442) Test.
80246	1,2	L,S	A	CH2 Acquisition RAM (A36U342) and Data Buffers (U428 & U440) Test.
80247	1,2	L,S	A	CH2 Acquisition RAM (A36U344) and Data Buffers (U428, U430 & U440) Test.
80248	1,2	L,S	A	CH2 Acquisition RAM (A36U346) and Data Buffers (U430 & U442) Test.

Test Number	Level	Loop	A/M	Description
80300 - Average Memory Tests				
80300	2	L,S	A	Average Memory Test. **Operation:** Runs all 803xx subarea tests designated as Auto (A) in column 4. This test writes an AAH pattern on average memory, then reads and verifies the pattern. Next, it writes a 55H pattern on average memory, then reads and verifies the pattern. Each test number is displayed in the Test Number Indicator while it is running. Devices tested: CH1 Data Bus Buffer (A44U260, U262, & U264) CH1 Address Counter (A44U210, U212, U214, & U216) CH2 Data Bus Buffer (A44U360, U362, & U364) CH2 Address Counter (A44U310, U312, U314, & U316).
80301	2	L,S	A	CH1 Average Memory (A44U254) Test.
80302	2	L,S	A	CH1 Average Memory (A44U252) Test.
80303	2	L,S	A	CH1 Average Memory (A44U250) Test.
80304	2	L,S	A	CH2 Average Memory (A44U354) Test.
80305	2	L,S	A	CH2 Average Memory (A44U352) Test.
80306	2	L,S	A	CH2 Average Memory (A44U350) Test.

Test Number	Level	Loop	A/M	Description
80700 - Address Generator Tests				
80700	2	L,S	A	Address Generator Test. **Operation:** Runs all 807xx subarea tests designated as Auto (A) in column 4. When the test is started, the 5th digit of the test number in the Test Number Indicator flickers to show the tests are being sequenced.
80701	1,2	L,S	A	Acquisition Start & End Address Register Test. **Operation:** Tests the Read/Write capability of the Start and End register. This test first writes an AAAAH pattern on the start address register and verifies that the memory address counter is at AAAAH. Then it writes an AAAAH pattern on the end address register and verifies the status is at address end. Next, the test writes 5555H on the start address register and verifies that the memory address counter is at 5555H. Then it writes a 5555H on the end address register and verifies the status is at address end. Devices tested: Start Address Register (A40U204, & U206) End Address Register (A40U200 & U202) Memory Address Counter (A40U212, U214, U216, & U218) Address Counter Buffer (A40U222 & U224) Data Bus Buffer (A40U120 & U122) Acquisition Status Register (A40U330).

Test Number	Level	Loop	A/M	Description
80702	1,2	L,S	A	Memory Address Counter Test. **Operation:** Tests the Read/Write capability of the Memory Address Counter by writing an F00H value on the start address register, then executing the count pulse 100H times, then verifying that the memory address counter is at 1000H. Devices tested: Memory Address Counter (A40U204, U206) Data Bus Buffer (A40U120 & U122) Start Address Counter (A40U204 & U206) Address Counter Buffer (A40U222 & U224) Other (A40U114, U220, U322, & U236).
80703	1,2	L,S	A	Trigger Delay Counter Test. **Operation:** Tests the Read/Write capability of the Trigger Delay Counter by writing an F00H value on the trigger delay counter, then executing a count pulse 100H times, then verifying that the trigger delay counter is at 1000H. Devices tested: Trigger Delay Counter (A40U242, U244, U246, & U248) Trigger Delay Counter Buffer (A40U252 & U254) Data Bus Buffer (A40U120 & U122) Other (A40U114, U266, U268, & U262D).

Test Number	Level	Loop	A/M	Description
80704	1,2	L,S	A	Average Pointer Test. **Operation:** Tests the writing and counting capability of the Average Pointer by writing an FF0H value on the start address register, then clocking the average pointer 80H times, then verifying that the memory address counter is at 1000H. Devices tested: Average Pointer Register (A40U270 & U272) Data Bus Buffer (A40U120 & U122) Start Address Register (A40U204 & U206) Memory Address Counter (A40U212, U214, U216, & U218) Other (A40U116, U264, & U136D).
80705	1,2	L,S	A	Average Memory Address Counter Test. **Operation:** Tests the writing and counting capability of the CH1 and CH2 average counters by setting the CH1 and CH2 start addresses for average, then starting the averager and clocking it 100H times, then checking for Average Done status. Devices tested: CH1 Address Counter (A44U210, U212, U214, and U216) CH1 Carry Latch (A44U180A) CH2 Address Counter (A44U310, U312, U314, & U316) CH2 Carry Latch (A44U180B) Status Register (A44U182) /AVCK1, /AVCK2, and /AUSTEP Signal IC (A44U100).

Section 3
MAINTENANCE

This section contains information about static-sensitive components, preventive maintenance, troubleshooting and repair procedures, and removal and replacement procedures.

STATIC-SENSITIVE COMPONENTS

This instrument contains static-sensitive components that can be damaged when subjected to static voltage discharge. Table 3-1 lists various device classes and their relative susceptibility to damage from static discharge. Static voltages of 1 kV to 30 kV are common in unprotected environments.

CAUTION

Static discharge may damage semiconductor components in this instrument.

Table 3-1
RELATIVE SUSCEPTIBILITY TO STATIC DISCHARGE DAMAGE

Semiconductor Classes	Relative Susceptibility Levels[1]
MOS or CMOS microcircuits or discretes, or linear microcircuits with MOS inputs (Most Sensitive)	1
ECL	2
Schottky signal diodes	3
Schottky TTL	4
High-frequency bipolar transistors	5
JFETs	6
Linear Microcircuits	7
Low-power Schottky TTL	8
TTL (Least Sensitive)	9

[1]Voltage equivalent for levels: (Voltage discharged from a 100 pF capacitor through a resistance of 100 Ω.)
1 = 100 to 500 V 4 = 500 V 7 = 400 to 1000 V (est.)
2 = 200 to 500 V 5 = 400 to 600 V 8 = 900 V
3 = 250 V 6 = 600 to 800 V 9 = 1200 V

SERVICING PRECAUTIONS

When performing maintenance, observe the following precautions:

1. Minimize handling of static-sensitive components.
2. Transport and store static-sensitive components or assemblies in their original containers, on a metal rail, or on conductive foam. Label any package that contains static-sensitive assemblies or components.
3. Discharge the static voltage from your body by wearing a grounded antistatic wrist strap while handling these components. Servicing of static-sensitive assemblies or components should be performed only at a static-free work station.
4. Nothing capable of generating or holding a static charge should be allowed on the work station surface.
5. Keep the component leads shorted together whenever possible.
6. Pick up components by the body, never by the leads.

7. Do not slide components over any surface.
8. Avoid handling components in areas that have a floor or work surface covering capable of generating a static charge.
9. Use a soldering iron that is connected to earth ground.
10. Use only approved antistatic, vacuum-type desoldering tools for component removal.

PREVENTIVE MAINTENANCE

INTRODUCTION

Preventive maintenance consists of periodic cleaning, visual inspection, and checking instrument performance. The severity of the operating environment in which the instrument is used determines the required frequency of maintenance. An appropriate time to perform preventive maintenance is just before instrument adjustment.

GENERAL CARE

The instrument cabinet covers and air filters minimize the accumulation of dust and dirt inside the instrument and they should be in place during normal operation.

INSPECTION AND CLEANING

Inspection

The air filters located at the rear of each Side Cabinet Cover and on the Rear Panel should be inspected every few weeks and cleaned or replaced if dirty. More frequent inspection is required when the instrument is operated in a severe environmental condition. Removal and replacement instructions are provided under "Removal and Replacement Procedures" in this section. Cleaning instructions are provided below under "Cleaning".

The instrument should be visually inspected for damage and cleanliness as often as operating conditions indicate. Accumulations of dirt or dust in the instrument can cause overheating and component failure. Dirt on components acts as an insulating blanket, preventing efficient heat dissipation. It also provides an electrical path that could result in instrument failure, especially under high-humidity conditions. The condition and frequency of required cleaning of the air filters is a good indication of when the instrument may need to be inspected for internal damage and accumulations of dust or dirt.

Cleaning

CAUTION

Avoid the use of chemical cleaning agents which might damage the plastics used in this instrument. Use a nonresidue-type cleaner, preferably isopropyl alcohol or a solution of 1% mild detergent with 99% water. Before using any other type cleaner, consult your Tektronix Service Center representative.

EXTERIOR DUST OR DIRT. Loose dust on the outside of the instrument can be removed with a soft cloth or small soft-bristle brush. Also, the brush is useful for dislodging dirt on and around the controls and connectors. Dirt that remains can be removed with a soft cloth dampened in a mild detergent and water solution. Do not use abrasive cleaners.

Clean the red, front-panel, 7-Segment LED Display Filter with a soft lint-free cloth dampened with either isopropyl alcohol or a mild deteregent and water solution.

INTERIOR DUST OR DIRT. Loose dust inside the instrument is removed with dry, low-pressure air (approximately 9 psi). Remove any remaining dust with a soft-bristle brush or a cloth dampened with a mild detergent and water solution. A cotton-tipped applicator is useful for cleaning in narrow spaces and on circuit boards.

If these methods do not remove all the dust or dirt, the instrument may be spray washed using a solution of 5% mild detergent and 95% water as follows:

1. Gain access to parts to be cleaned by removing easily accessible shields and panels.
2. Spray wash dirty parts with the detergent and water solution, then rinse with clean water.
3. Dry all parts with low-pressure air.
4. Clean switches with isopropyl alcohol, wait 60 seconds for the majority of the alcohol to evaporate, then completely dry the part with low-pressure air.
5. Dry all components and assemblies in an oven or drying compartment using low-temperature (125° - 150° F) circulating air.

AIR FILTERS. To clean an air filter:

1. Flush loose dirt from the filter with a stream of hot water.
2. Soak the filter in a solution of hot water and mild detergent for a few minutes.
3. Squeeze the filter to force out any remaining dirt.
4. Rinse the filter in clear water to remove any further dirt or detergent, then allow it to dry.

PERIODIC ADJUSTMENT

To ensure accurate operation, instrument performance should be checked every 2000 hours of operation, or if used infrequently, once a year. Also, whenever components are replaced, that portion of the instrument should be performance checked and adjusted as necessary.

TROUBLESHOOTING AND REPAIR

TROUBLESHOOTING AIDS

Diagnostics

The operating firmware in this instrument contains diagnostic routines that aid in locating malfunctions. When instrument power is applied, a set of power-up tests are performed. If a failure is detected, this information is displayed as an error code in the instrument display panel, and the instrument automatically enters an extended diagnostic mode (Level 2). If the failure is such that the instrument processor and the diagnostic circuitry is still functional, additional diagnostic routines can be executed to further pin-point the failure. Complete information on diagnostics is contained in the "Diagnostics" section.

Troubleshooting Charts

The troubleshooting charts located in the "Troubleshooting Charts" section are used in conjunction with the "Diagnostics" section to locate malfunctioning circuitry. To use the charts, start with the Initial Troubleshooting Chart, then follow the instructions contained on the charts.

Troubleshooting Equipment

Test equipment required for servicing can be selected from the equipment list in the "Performance Check/Adjustment" section.

Schematics

Complete schematic diagrams are located in the "Diagrams and Circuit Board Illustrations" section. On the schematics, heavy black lines enclose portions of circuitry for a specific circuit board. The assembly number ("A" number) and name of the circuit board is shown near the top or bottom edge of the diagram. Component numbers and their electrical value are shown on the diagrams. Refer to the first page of the "Diagrams and Circuit Board Illustrations" section for an explanation of the reference designators and symbols used to identify components. Also see the "Grid Coordinate System/Component Reference Chart" topic below.

Circuit Board Illustrations

Circuit board illustrations show the physical locations of each component on a circuit board. An illustration of each board is found in the "Diagrams and Circuit Board Illustrations" section facing the first schematic diagram on which the board appears. Also see the "Grid Coordinate System/Component Reference Chart" topic below.

Grid Coordinate System/Component Reference Chart

Each schematic diagram and circuit board illustration has a grid border along its left and top edges. A table located adjacent to each schematic diagram lists the grid coordinates of each component shown on that diagram. To aid in physically locating components on the circuit board, this table also lists the grid coordinate of each component on the circuit board illustration. As an aid to circuit tracing, the table also lists all other schematics where the board appears.

Circuit Board Locations

The placement within the instrument of each circuit board is shown at the beginning of the Diagrams and Circuit Board Illustrations" section.

Multipin Connectors

Multipin connector orientation is shown in Figure 3-1. The circuit board pins are indexed with a triangle symbol identifying pin 1. From the triangle, each pin is sequentially numbered (2, 3, 4, etc.).

Tektronix connectors are indexed by a triangle symbol that identifies slot 1 (Figure 3-1A). Each slot is sequentially numbered (2, 3, 4, etc.) from the triangle symbol.

Fujitsu connectors are indexed by an 'F' mark that identifies slot 1, and a • that identifies the *n*th slot (if it is a 5-slot connector, the • identifies the 5th slot (Figure 3-1B). Each slot is sequentially numbered (2, 3, 4, etc.) from the 'F' mark.

Normally the wiring in each of the connector slots is color coded similar to resistor color coding (pin 1 is brown, pin 2 is red, pin 3 is orange, etc.).

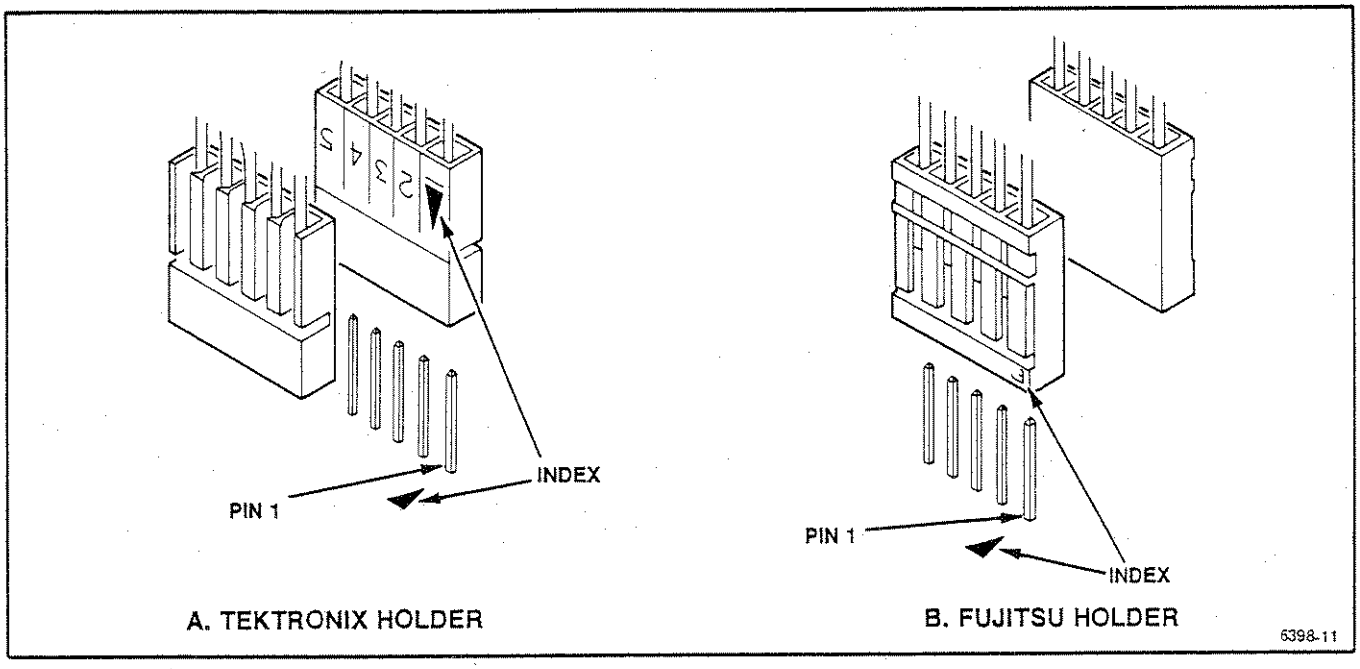


Fig. 3-1 Multipin connector

148-0199-02 REED RELAY SOLDERING ATTENTION

1. Leave at least 2mm interval from an end of the switch body to a soldering point. See Figure 3-2.
2. Soldering temperature must not exceed 300°C.
3. Solder one point within three (3) seconds.
4. Use solder containing 63% tin and 37% lead.
5. Do not use flux except a Rosin system flux.
6. When wiring the switch to external, keep the wiring at least 0.3 mm distant from any other conductors.
7. Do not bend the switch lead. If unavoidable, never stress the switch.

OBTAINING REPLACEMENT PARTS

Most electrical and mechanical parts can be obtained through your local Tektronix Field Office or representative. However, many of the standard electronic components and hardware usually can be obtained from a local commercial source. Before purchasing or ordering a part from a source other than Tektronix, please check the replaceable parts list for the proper value, rating, tolerance, and description.

NOTE

Physical size and shape of a component may affect instrument performance, particularly at high frequencies. Always use direct-replacement components, unless it is known what a substitute will not degrade instrument performance.

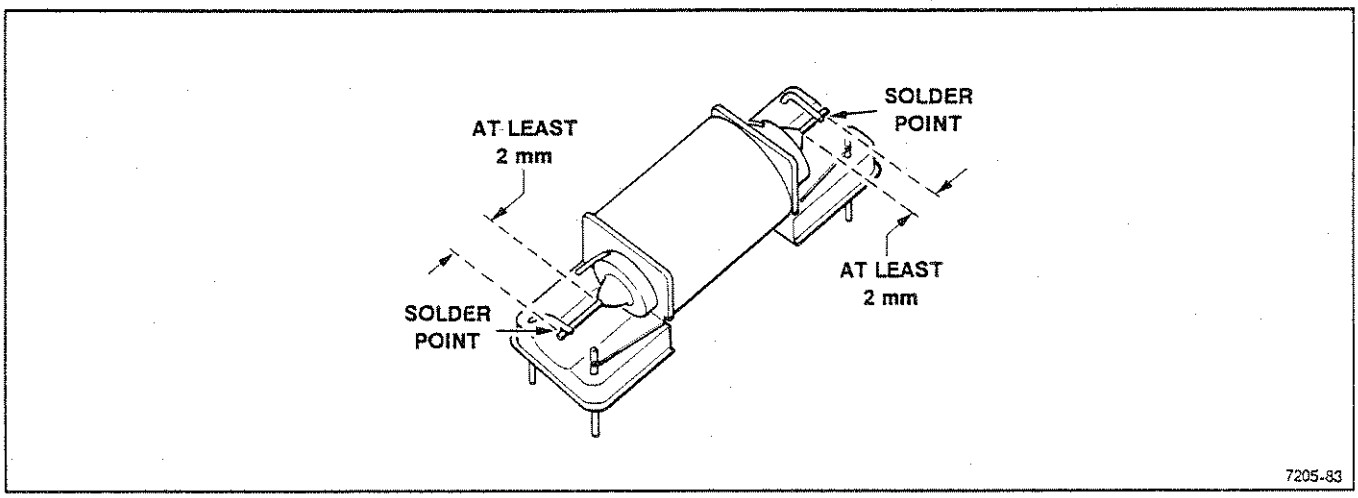


Fig. 3-2 Special soldering techniques for reed relay

Special Parts

Many parts in this instrument are manufactured or selected by Tektronix, Inc. to meet specific performance requirements, or are manufactured for Tektronix, Inc. in accordance with our specifications. The various manufacturers are identified in the "Cross Index - MFR Code Number to Manufacturer" column in the "Replaceable Electrical Parts" list. Most of the mechanical parts used in this instrument were manufactured by Tektronix, Inc. Order all special parts directly from your local Tektronix Field Office representative.

Ordering Parts

When ordering replacement parts from Tektronix, Inc., please include all the following information:

1. Instrument type (include modification or option numbers).
2. Instrument serial number.
3. A description of the part (if electrical, include its full circuit component number, such as A60R205).
4. Tektronix part number.

SELECTABLE COMPONENTS

Several components in the instrument are selected to obtain optimum circuit operation. Value selection of these components is done during the initial factory calibration procedure. Further selection is not usually necessary for subsequent adjustments unless a component has been changed that affects the circuitry containing the selected component.

Each of the selected components are identified as such on the schematics. Also, each component is identified in the procedure in the "Performance Check/Adjustment" section where it affects performance.

MAINTENANCE AIDS

The items listed in Table 3-2, or suitable substitutes, are required to perform most of the maintenance procedures on the instrument.

Table 3-2
MAINTENANCE AIDS

Description	Specification	Usage	Example
Soldering Iron	15-25 W.	General soldering and unsoldering.	Antex Precision Model C.
Screwdrivers	11" shank with a flat blade 3/32 width tip, and Phillips #1 and #2 tips.	Assembly and disassembly.	Magna Type, EDP #37038-3 magnetic screwdriver holder for 1/4" hex insert bits; Phillips tip P1 and P2; and screwdriver tip 6-8.
Nutdrivers	1/4, 7/32, 5/16, and 1/2 inch.	Assembly and disassembly.	Xcelite #7, #8, #10, and #16.
Pin Punch	1/16"	Carrying Handle removal.	
Open-end Wrench	7/16, 3/8, and 1/2 inch.	Assembly and disassembly.	
Hex Wrench	1/16"	Assembly and disassembly.	Allen Wrench.
Long-nose Pliers		Component removal and replacement.	Diamalloy Model LN55-3.
Diagonal Cutters		Component removal and replacement.	Dimalloy Model M554-3.
Vacuum Solder Extractor	No static charge retention.	Unsoldering static sensitive devices and components on multilayer boards.	Pace Model PC-10.
Contact Cleaner and Lubricant	No-Noise R.	Switch and potentiometer cleaning and lubrication.	Tektronix Part Number 006-0442-00.
Pin-Replacement Kit		Replace circuit board connector pins.	Tektronix Part Number 040-0542-00.
IC Removal Tool		Removing DIP IC packages.	Augat T114-1.
Isopropyl Alcohol	Reagent grade.	Cleaning attenuator and front-panel assemblies.	2-isopropanol.
Isolation Transformer [1]		Isolate the instrument from ac source for safety.	Tektronix Part Number 006-5953-00.

[1]An isolation transformer should be used to connect the instrument to a power source when troubleshooting the instrument.

REMOVAL AND REPLACEMENT PROCEDURES

When reading removal and replacement procedures, any reference to left or right, or toward the left or right, means the left or right side of the instrument when facing the front panel, unless otherwise specified in the instruction.

AIR FILTERS

Removal

To remove an air filter, pick up a corner of the filter by your fingers and pull it out of its chassis pocket. Be careful not to drop accumulated dirt into the instrument.

An alternate method of removing the rear-panel air filter is to remove the four (4) corner retaining screws in the Rear Air Filter Cover, then remove the cover and filter.

Replacement

To replace an air filter, place it into its chassis pocket as best as possible. Then use a pair of tweezers and a flat tool (tongue depressor or screwdriver blade) to work the filter into place. Sometimes, rubbing your finger on the filter in the direction you want it to move helps to position it.

If the Rear Air Filter Cover was removed to access the filter, place the filter on the cover, then set the cover in place on the instrument and reinstall attaching screws.

TOP, BOTTOM, AND LEFT SIDE CABINET COVERS

WARNING

Hazardous voltages exist inside this instrument when the power cord is connected to a power source. To avoid injury, disconnect the power cord before removing any instrument covers.

Removal

To remove the top, bottom, or left side cabinet covers:

NOTE

Before removing the left side Cabinet Cover, remove its air filter.

1. Remove the rear corner retain attaching screws and corner retainers that are associated with the cabinet cover to be removed (Figure 3-3).

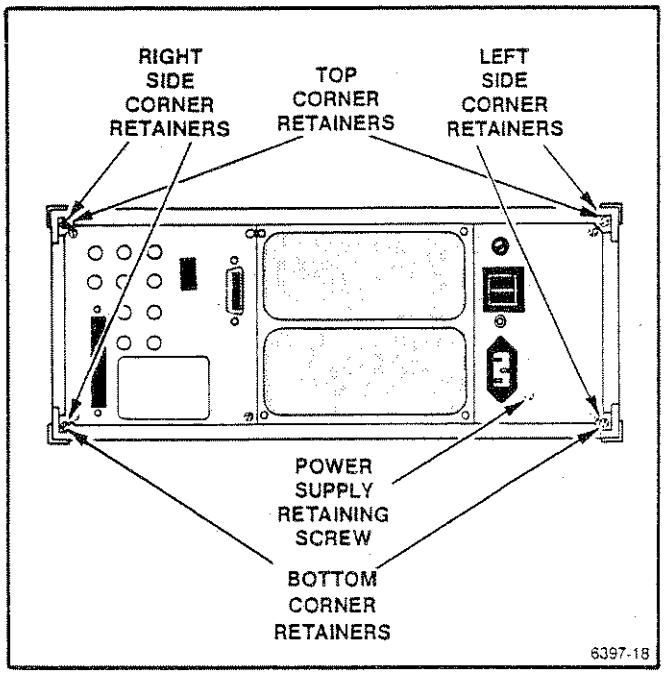


Fig. 3-3 Cabinet cover removal

2. Carefully remove the cabinet cover by sliding it toward the rear of the instrument.

Replacement

Reinstall the top, bottom, or left side cabinet cover in the reverse order of removal by sliding it into its respective cover grooves from the rear of the instrument. Then reinstall the rear corner retainers and attaching screws.

NOTE

After installing the left side Cabinet Cover, reinstall its air filter.

RIGHT SIDE CABINET COVER/CARRYING HANDLE

WARNING

Hazardous voltages exist inside this instrument when the power cord is connected to a power source. To avoid injury, disconnect the power cord before removing any instrument covers.

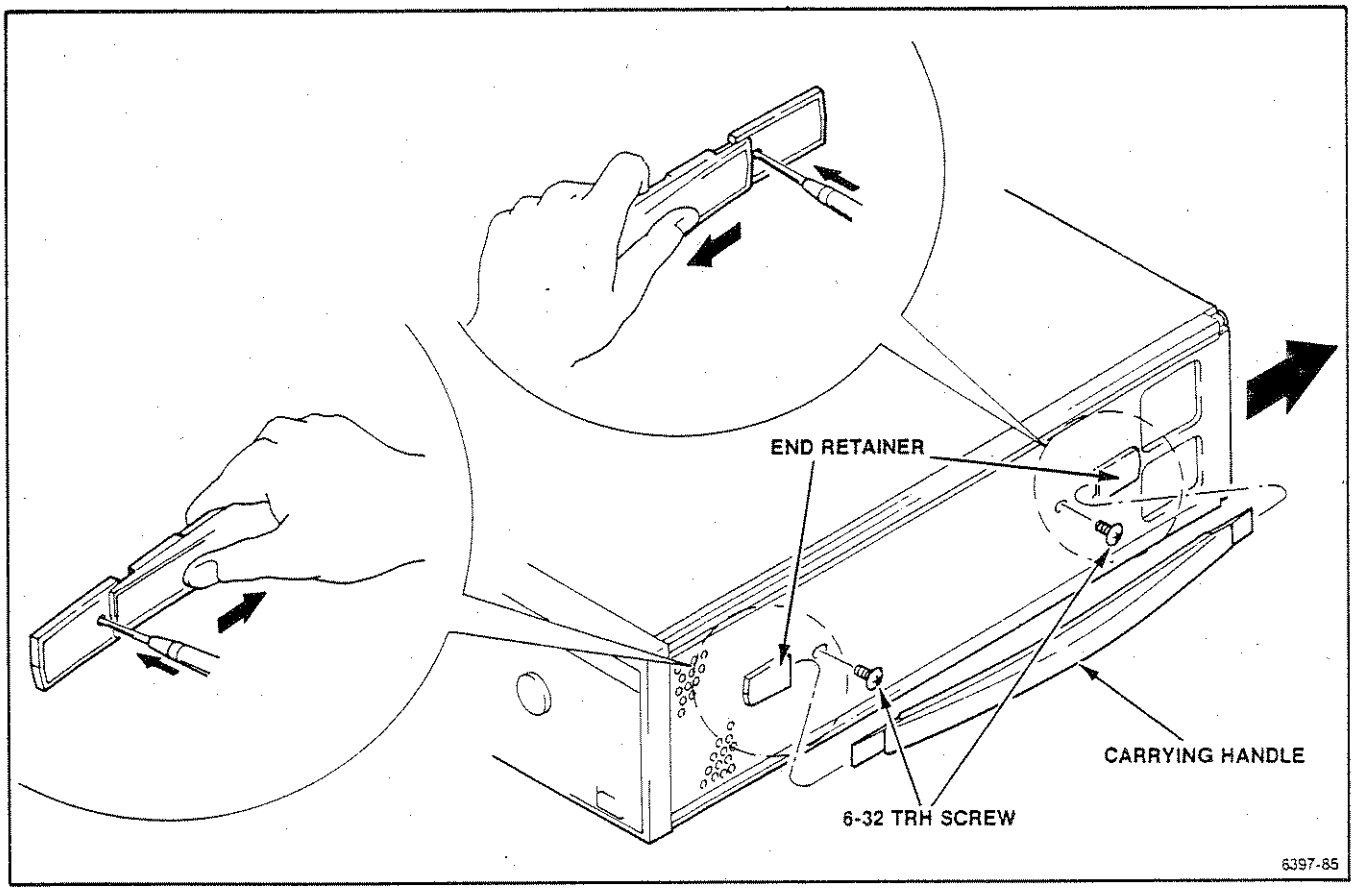


Fig. 3-4 Right side cabinet cover carrying handle removal

Removal

To remove the right side cabinet cover:

NOTE

Before removing the right side Cabinet Cover, remove its air filter.

1. Remove the two (2) screws under the Carrying Handle. These screws may be removed either by using an offset screwdriver, or by removing the Carrying Handle and then removing the screws.

To remove the Carrying Handle:

a. Pull one end of the Carrying Handle out of its end retainer to expose the small hole in the retainer (Figure 3-4).

b. While continuing to pull the handle out of its end retainer, push a small punch-type tool into the retainer hole to release the handle. As soon as the handle releases, remove the punch-type tool and pull the handle completely out of its retainer.

c. Repeat steps 1a. and 1b. to remove the other end of the handle.

2. Remove the attaching screws for the two rear corner retainers associated with the right side cabinet cover (Figure 3-3).

3. Carefully remove the cover by sliding it toward the rear of the instrument.

Replacement

To install the right side cabinet cover:

1. Install the right side cabinet cover by sliding it into its cover groves from the rear of the instrument.

NOTE

After installing the right side Cabinet Cover, reinstall its air filter.

2. Install the two screws normally located under the Carrying Handle.

CAUTION

When the Carrying Handle is reinstalled in the next step, verify that both ends are locked into their respective end retainers before using the handle to carry the instrument.

3. Position the Carrying Handle with its curve side facing away from the cabinet cover.

4. One end at a time, push the handle's metal end connector into its end retainer until it locks in place.

FRONT PANEL

Removal

To remove the Front Panel:

1. Remove the Rotary Encoder Knob (Parameter Entry Knob) using a 1/16" allen wrench.

2. Remove the Top Cabinet Cover

NOTE

The next step requires a #2 Phillips screwdriver with at least a 7" shank.

3. Remove the four (4) Front Panel attaching screws (Figure 3-5). There are two (2) about 6" in from each side at the top of the panel and one (1) at each bottom inside corner of the panel.

CAUTION

When removing the Front Panel in the next step, do not force or pry on the Front Panel itself as it may crack or break. Be sure to push the panel out as far as possible with the Front Panel Brackets inside at each side of the panel. If the bottom of the panel (especially the lower

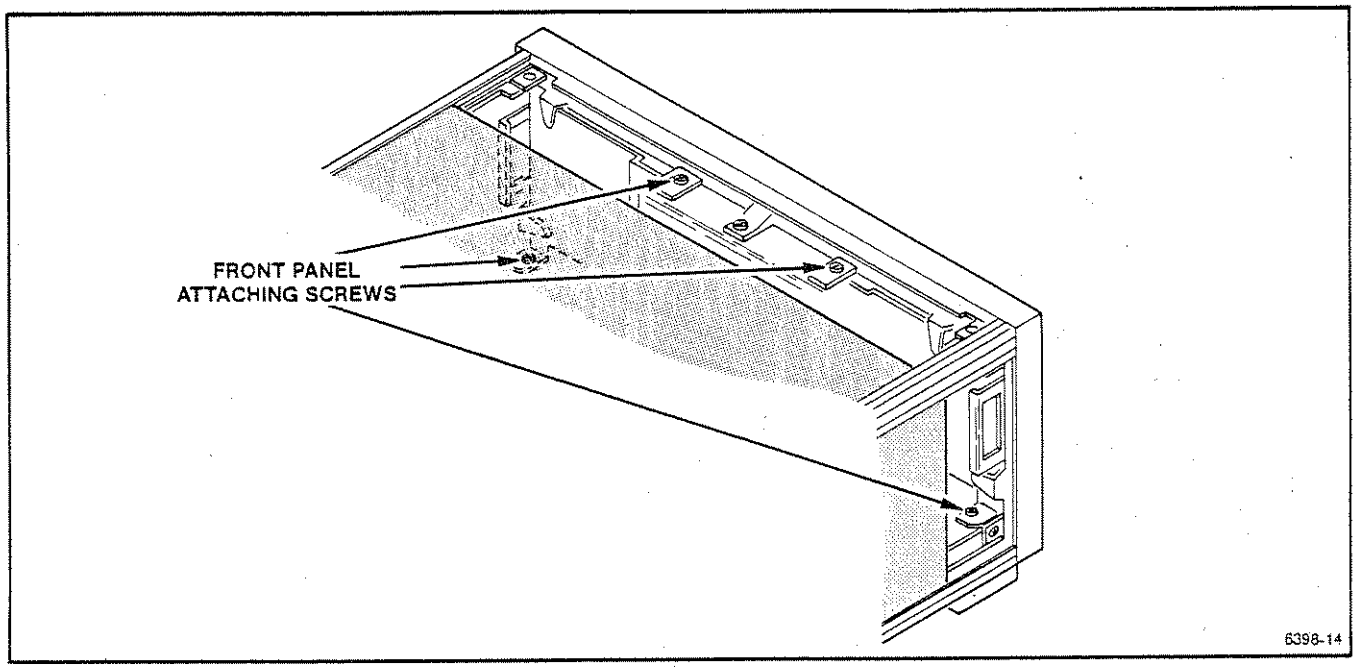


Fig. 3-5 Front panel removal

left side corner) appears to bind, very carefully insert a small, pocket-type screwdriver in the space between the bottom of the panel and the Front Frame and gently pry outward on the metal assembly holding the spring-type grounding strip that can be seen inside behind the bottom of the panel.

4. Push the Front Panel out of the instrument using the left and right Front Panel Brackets, but do not pull it completely away from the instrument before completing the next step.

NOTE

Before disconnecting the cable from the ON/STANDBY switch in the next step, note that is shaped such that it won't catch the bottom lip of the Front Panel when it is installed, and that it is routed across J700 and under the bottom right row of key switches.

5. Disconnect the power ON/STANDBY switch cable from J846.

6. Pull the Front Panel completely away from the chassis.

Replacement

To reinstall the Front Panel:

1. Set the Front Panel near the front of the instrument and connect the power ON/STANDBY switch cable to J846. Shape the cable and route it across J700 and under the bottom row switches as noted above.

CAUTION

When pushing the Front Panel into the chassis in the next step, watch that the key switches do not catch on the edge of their openings. Also, ensure that the panel is fully seated into its cutout around the edges. If it isn't, it is likely that the power ON/STANDBY switch cable to J846, or some other cable, may be caught or pinched under the Front Panel.

2. Carefully push the Front Panel straight into the chassis and reinstall the attaching screws.

3. Reinstall the Rotary Encoder Knob. Be sure to leave a space between the knob and the Front Panel so it doesn't rub on the panel when rotated.

A60 PANEL CONTROL BOARD

Removal

To remove the A60 Panel Control Board

1. Remove the Front Panel.
2. Disconnect the 3-wire cable at J250.
3. Remove the eight (8) board attaching screws.
4. Gently lift the board slightly up and forward, then disconnect the ribbon cable at J700 and remove the board.

Replacement

To install the A60 Panel Control Board:

1. Set the board next to the front of the chassis with its controls facing you.
2. Connect the ribbon cable to J700.
3. Reinstall the board and its attaching screws.
4. Connect the 3-wire cable to J250 and carefully route the wire under the board so it doesn't interfere with the Front Panel when it is installed.

BLANK FRONT PANEL (OPTION 19 ONLY)

The Option 19 Blank Front Panel removes the same as the standard Front Panel.

A64 INDICATOR BOARD (OPTION 19 ONLY)

Removal

To remove the A64 Indicator Board:

1. Remove the Option 19 Blank Front Panel.
2. Disconnect the ON/STANDBY switch cable from J846.
3. Remove the four (4) board attaching screws.
4. Gently lift the board slightly up and forward and disconnect the ribbon cable at J700, then remove the board.

Replacement

CAUTION

When reinstalling the A64 Indicator Board, ensure that the power indicator ON LED is properly located to enter its cutout in the Blank Front Panel; otherwise, its leads may be bent.

Reinstall the A64 Indicator Board (Option 19 Only) in the reverse order or removal.

A24 TV TRIGGER BOARD (OPTION 05 ONLY)

Removal

To remove the A24 Trigger Board:

1. Remove the Front Panel.
2. Remove the A60 Panel Control Board (standard instrument only) or A64 Indicator Board (Option 19 only).
3. Remove the four (4) TV Trigger Shield attaching screws.
4. Remove the four (4) TV Trigger board attaching screws.
5. Pull the bottom of the board slightly away from the chassis.
6. Disconnect the cables at J240 and J241 and remove the board.

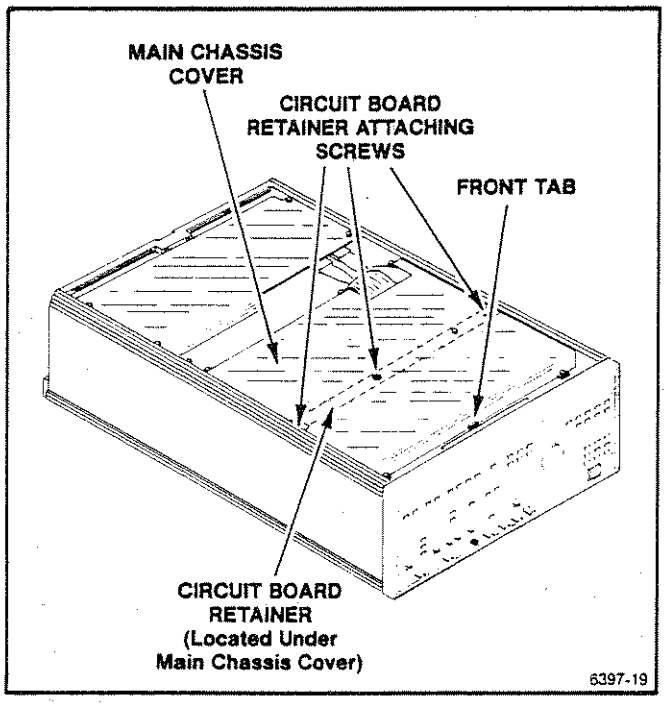


Fig. 3-6 Main chassis cover & circuit board retainer removal

Replacement

Reinstall the A24 TV Trigger Board in the reverse order of removal.

MAIN CHASSIS BOARDS

For the purpose of the following removal and replacement procedures, these boards are considered Main Chassis Boards:

A12 Input Amplifier
A14 Auto-Cal
A18/CH1 A/D
A18/CH2 A/D
A22 Trigger
A30 Envelope
A32 Time Base
A36/CH1 Memory
A36/CH2 Memory
A40 Address Generator
A44 Averager
A50 MPU
A52 DMA
A54 Display Control
A56 GPIB/Monitor

Removal

1. Remove the Top Cabinet Cover.
2. Remove the six (6) Main Chassis Cover attaching screws (Figure 3-6). There are three (3) at the rear edge, two (2) at the front edge, and one (1) at the center of the right side.
3. Unscrew the three (3) Circuit Board Retainer screws just so the retainer is free of the chassis (Figure 3-6).
4. Disconnect the cable and wires attached to whichever board is being removed (see "Main Chassis Board Removal Notes" below).
5. Simultaneously lift up on both Circuit Board Ejectors to unseat the board to be removed.
6. Carefully lift the board up and out of the main chassis.

Main Chassis Board Removal Notes

A12 INPUT AMPLIFIER BOARD/A14 AUTO-CAL BOARD. These boards are connected together and must be removed as a unit. The boards must be partially removed before disconnecting the cables attached to J110, J112, J124, and J165. When replacing the board, reconnect these cables before fully reinstalling the board.

A18/CH1 A/D BOARD. This board must be partially removed before disconnecting the cables attached to J150, J326, and J400. When replacing the board, reconnect these cables before fully reinstalling the board.

A18/CH2 A/D BOARD. This board must be partially removed before disconnecting the cables attached to J150, J326, and J400. When replacing the board, reconnect these cables before fully reinstalling the board.

A22 TRIGGER BOARD. Disconnect the cable at J222, then partially remove the board and disconnect the coaxial cables at J124 and J165. When replacing the board, reconnect the coaxial cables at J124 and J165 before fully installing the board.

A30 ENVELOPE BOARD. Disconnect the ribbon cable at J302 before removing the board.

A32 TIME BASE BOARD. Remove the coaxial cables connecting J322, J323, J324, J325, J326-1, J326-2, and J762, and the ribbon cable on the A30 board at J302 before removing the board.

A36/CH1/MEMORY, A36/CH2 MEMORY, A40 ADDRESS GENERATOR, AND A44 AVERAGER BOARDS. Remove the ribbon cable at A30 board and J302 before removing any of these boards.

A50 MPU, A52 DMA, AND A54 DISPLAY CONTROL BOARDS. Remove the ribbon cable on the A56 board at J330 before removing these boards.

A56 GPIB/MONITOR BOARD. Disconnect the ribbon cable at J330 before removing this board. Then partially remove the board before disconnecting the cable at J431, J471, and J482. Reconnect these cables before fully reinstalling the board.

Replacement

Reinstall the Main Chassis Boards in the reverse order of removal. Table 3-3 may be used to verify the recabling of any board.

Table 3-3
BOARD CABLING INFORMATION

From Board/Connector	Type Cable	To Board/Connector
A10J110	Coaxial cable, black, marked #1	A12J110
A10J112	Coaxial cable, black, marked #2	A12J112
A12J123-1	Coaxial cable, black, marked #1	A18/CH1 J123
A12J123-2	Coaxial cable, black, marked #2	A18/CH2 J123
A12J124	Coaxial cable, white w/brown stripe; tied w/A12J165	A22J124
A14J330	1-conductor shielded wire, white w/brown stripe	A32J330
A12J165	Coaxial cable, white w/red stripe; tied w/A12J124	A12J165
A18/CH1 J123	Coaxial cable, black, marked #1	A12J123-1
A18/CH2 J123	Coaxial cable, black, marked #2	A12J123-2
A18/CH1 J150	Coaxial cable, black	To Delay Line Assembly on bottom of instrument.
A18/CH2 J150	Coaxial cable, black	To Delay Line Assembly on bottom of instrument.
A18/CH1 J326	Coaxial cable, gray, marked #1	A32J326-1
A18/CH2 J326	Coaxial cable, gray, marked #2	A32J326-2
A18/CH1 J400	Coaxial cable, black	From Delay Line Assembly on bottom of instrument.

Table 3-3 (Cont.)
BOARD CABLING INFORMATION

From Board/Connector	Type Cable	To Board/Connector
A18/CH2 J400	Coaxial cable, black	From Delay Line Assembly on bottom of instrument.
A22J124	Coaxial cable; white w/brown stripe; tied w/A22J165	A12J124
A22J165	Coaxial cable; white w/red stripe; tied w/A22J124	A12J165
A22J222	1-conductor shielded; white w/brown stripe	Goes under shield to front panel.
A30J302	Ribbon cable	Rear Panel A/D OUT connector.
A32J322	Coaxial cable; white w/green stripe	Rear Panel EXT ARM IN connector.
A32J323	Coaxial cable; white w/yellow stripe	Rear Panel TRIG'D OUT connector.
A32J324	Coaxial cable; white w/blue stripe	Rear Panel CLK OUT connector.
A32J325	Coaxial cable; white w/purple stripe	Rear Panel EXT CLK IN connector.
A32J326-1	Coaxial cable; gray, marked #1	A18/CH1 J326
A32J326-2	Coaxial cable; gray, marked #2	A18/CH2 J326
A32J330	1-conductor shielded wire; white w/brown stripe	A14J330
A32J762	Coaxial cable; gray	A76J762
A56J431	Coaxial cable; white w/red stripe	Rear panel CRT MONITOR OUT -Y connector.
A56J471	Coaxial cable; white w/brown stripe	Rear panel CRT MONITOR OUT -X connector.
A56J482	Coaxial cable; white w/orange stripe	Rear panel CRT MONITOR OUT -Z connector.
A56J330	Ribbon cable	A74J330
A76J762	Coaxial cable; gray	A32J762

A10 ATTENUATOR MODULE

Removal

To replace the Attenuator Module:

1. Remove the A12/A14 Boards (they are connected as one unit) using the instructions in the MAIN CHASSIS BOARDS topic above.
2. Remove the Bottom Cabinet Cover.
3. Set the instrument on its left side.
4. Remove the four (4) attaching screws from the tabs at the side of the Attenuator Module (the screws on the top of the module are for the module cover).
5. Lift the module completely out of the chassis.

Replacement

Replace the A10 Attenuator Module in the reverse order of removal.

A70 MAIN INTERCONNECT BOARD

Removal

1. Remove the Top and Bottom Cabinet Covers.
2. Remove the A60 Panel Control Board to the point where the ribbon cable at J700 can be disconnected and disconnect the cable.
3. Remove the Main Chassis Boards.
4. Turn the instrument over so its bottom is facing up.
5. Disconnect the Power Supply Module connectors at J842, J864, J868, and J870, Front Panel connector at J703, A76 Oscillator Board connector at J704, and if Option 05 is installed, the TV Trigger Board connector at J240 and J241.
6. Remove the center attaching screw for the delay line assembly and move it slightly toward the front of the instrument.
7. Remove the 10 Main Interconnect Board attaching screws.
8. Slide the board toward the front of the instrument to unhook the seven (7) board holding tabs, then carefully lift the board up and off the chassis.

Replacement

Reinstall the Main Interconnect Board in the reverse order of removal. Reconnect the cables at J700, J703, J704, J842, J864, J868, J870, and if Option 05 is installed, J240 and J241.

A74 I/O BOARD

Removal

To remove the A74 I/O Board:

1. Remove the Top Cabinet Cover.
2. Remove the Power Supply Module.
3. Disconnect the two (2) ribbon cables at J330 and J740.
4. Remove the three (3) 1/4" attaching nuts at the top corners and bottom center of the board.
5. Carefully pull the board toward the front of the instrument. When it is free, lift it out of the main chassis.

Replacement

Reinstall the A74 I/O Board in the reverse order of removal.

A76 OSCILLATOR BOARD

Removal

To remove the A76 Oscillator Board:

1. Remove the Top Cabinet Cover.
2. Remove the Power Supply Module.
3. Disconnect the coaxial cable at J762 and 5-wire cable at J760.
4. Remove the two (2) board attaching screws.
5. Slide the board toward the front of the instrument and when its tabs clear the chassis, remove it.

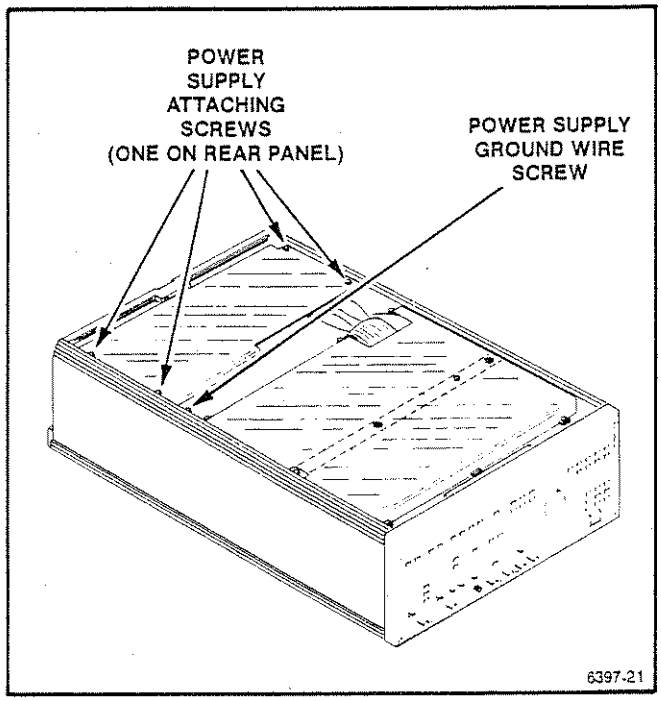


Fig. 3-7 Power supply removal

Replacement

Reinstall the A76 Oscillator Board in the reverse order of removal.

POWER SUPPLY MODULE

WARNING

Hazardous voltages exist inside this instrument when the power cord is connected to a power source. To avoid injury, disconnect the power cord before removing any instrument covers.

Removal

To remove the Power Supply Module:

1. Remove the Top Cabinet Cover.
2. Disconnect the power supply connectors J842, J864, J868, and J870. Their locations are marked on top of the power supply.
3. Remove the five (5) power supply attaching screws. There are two (2) on each side on the top of the module (Figure 3-7). The other one is located on the rear panel near the lower right corner of the power cord receptacle (Figure 3-2).
4. Remove the ground wire attaching screw (Figure 3-7). The ground wire is a green/yellow wire located at the top left front corner of the power supply module.
5. Carefully slide the power supply toward the front of the instrument until the fuse holder, power switch, ground terminal, and power cord receptacle clear the rear panel.
6. Carefully lift the power supply up and out of the main chassis.

Replacement

Install the Power Supply Module in t he reverse order of removal.

NOTE

Be sure to reconnect the ground wire at the top left corner of the power supply module.

CAUTION

If the power supply was removed to change its line voltage selector jumper, be sure to change the Line Voltage Indicator "INTERNALLY SET FOR" screw on the rear panel to reflect the correct line voltage selected by the jumper. Failure to make this change may cause an operator to connect the instrument to an incorrect line voltage, which may damage the instrument.

A80 LINE INPUT BOARD

Removal

To remove the A80 Line Input Board:

1. Remove the Power Supply Module.
2. Remove the module's left Chassis Side panel (on the same end as the Principal Power Switch).
3. Disconnect the cable connectors at J800 and J820.
4. Remove the four (4) board attaching screws.
5. Pull the bottom of the board slightly toward you, then lift the bottom right corner (facing the board) up and out of the chassis enclosure. Then using the same board angle, carefully pull the board to the right and completely out of the chassis.

Replacement

To reinstall the A80 Line Input Board:

1. Set the Power Supply Module on its right end with the Line Input Board enclosure facing upward.
2. Set the board down into its enclosure from the right side of the enclosure and install the attaching screws (the large screws install in the transformer tab holes).
3. Connect the cables to J800 and J820.
4. Set the left Chassis Side panel in place and install its attaching screws.
5. Replace the Power Supply Module.

A82 INVERTER BOARD

Removal

To remove the A82 Inverter Board:

1. Remove the Power Supply Module.
2. Remove the A88 Control Board.
3. Remove the module's six (6) left Chassis Side panel attaching screws (panel is on the end adjacent to the Principal Power Switch where the A80 Line Input Board is located) and remove the panel.
4. Disconnect the cable at J820, which is in the enclosure where the A80 Line Input Board is located.
5. Pull off the small plastic cable insulating strip installed on the chassis to hold down the cables connected to J840, J860, and J866.
6. Disconnect the cables at J840, J860, and J866.
7. Disconnect the ribbon cable at J824.
8. Remove the five (5) attaching screws and two (2) spacer posts for the Inverter Board.
9. Lift up the end of the board that has its name written on it until it clears the end of the chassis. Then pull the board toward that end until the small tail on the board clears the enclosed section behind the Principal Power Switch.

Replacement

To reinstall the A82 Inverter Board:

1. Set the Power Supply Module on its top.
2. Guide the small tail of the board down and into the opening in the enclosure housing the A80 Line Input board. Then finish setting the board down into the chassis and installing the five (5) attaching screws. The two (2) large screws are installed in the transformer tabs and the two (2) spacer posts are installed at the same end as the board name).
3. Connect the cable in the enclosure behind the Principal Power Switch to J820.
4. Set the left Chassis Side panel in place and install its attaching screws.
5. Connect the ribbon cable to J824.

CAUTION

Be sure the ribbon cable connector is connected to both rows of pins on J824 as it can be misconnected to only one row.

6. Set the Power Supply Module on its fans.

7. Connect the cables to J840, J860, and J866.
8. Reinstall the small plastic cable insulating strip on the chassis to hold down the cables attached to J840, J860, and J866.
9. Replace the A88 Control Board.
10. Replace the Power Supply Module.

A84 REGULATOR ANALOG BOARD

Removal

To remove the A84 Regulator Analog board:

1. Remove the Power Supply Module.
2. Remove the A86 Regulator Digital Board.
3. Set the Power Supply Module on its bottom with the Principal Power Switch facing you.
4. Disconnect the ribbon cable at J824.
5. Disconnect the cable at J840.
6. Remove the six (6) board attaching screws and remove the board.

Replacement

To replace the A84 Regulator Analog Board:

1. Set the Power Supply Module on its bottom.
2. Set the board on its chassis spacers and reinstall its attaching screws.
3. Connect the ribbon cable to J824.

CAUTION

Be sure the ribbon cable connector is connected to both rows of pins on J824 as it can be misconnected to only one row.

4. Connect the cable to J840.
5. Replace the A86 Regulator digital Board.

A86 REGULATOR DIGITAL BOARD

Removal

To remove the A86 Regulator Digital Board:

1. Remove the Power Supply Module.
2. Remove the seven (7) Rear Chassis panel attaching screws and remove the panel.
3. Remove the 12 Top Chassis panel attaching screws and remove the panel.
4. Disconnect the ribbon cable at J824.
5. Disconnect the cables at J860 and J866.
6. Disconnect the fan cables at J862 and J863 (these are latching connectors whose latch tabs must be sprung slightly to be unlatched).
7. Lift the board up and out of the chassis.

Replacement

To replace the A86 Regulator Digital Board:

1. Set the Power Supply Module on its fans.
2. Insert each end of the board into its board Retainer guides and slide the board down into the chassis.
3. Connect the fan cables to J862 and J863. Ensure they are pushed on far enough to latch.
4. Connect the cables to J860 and J866.
5. Connect the ribbon cable to J824.

Be sure the ribbon cable connector is connected to both rows of pins on J824 as it can be misconnected to only one row.

6. Set the Power Supply Module on its bottom.
7. Set the Top Chassis panel in place and install the six (6) attaching screws that attach to the chassis (not the board).
8. Slightly adjust the board to line up its attaching screw holes, then install the remaining six (6) panel/board attaching screws (do not tighten the screws until all of them are partially installed).

9. Set the Rear Chassis panel in place and install its attaching screws.

10. Replace the Power Supply Module.

A88 CONTROL BOARD

Removal

To remove the A88 Control Board:

1. Remove the Power Supply Module.

2. Set the Power Supply Module on its fans.

3. Remove the module's seven (7) Rear Chassis panel attaching screws and remove the panel.

4. Set the Power Module on its top.

5. Remove the module's five (5) Chassis Bottom panel attaching screws (2 are on the bottom at same end as Principal Power Switch, 2 are on the same panel as the fans, and 1 is on the end of the module at the opposite end of the Principal Power Switch), then remove the panel.

6. Disconnect the ribbon cable at J824.

7. Remove the two (2) board attaching screws and lift the board out of the chassis.

Replacement

To replace the A88 Control Board:

1. Set the Power Supply Module on its top.

2. Set the board on its chassis spacer posts and install the attaching screws.

3. Connect the ribbon cable to J824.

CAUTION

Be sure the ribbon cable connector is connected to both rows of pins on J824 as it can be misconnected to only one row.

4. Set the Chassis Bottom in place and install its attaching screws.

5. Set the Power Supply Module on its fans.

6. Set the Rear Chassis panel in place and install its attaching screws.

7. Replace the Power Supply Module.

INTERNAL JUMPER SELECTORS

LINE VOLTAGE SELECTOR

Procedures for changing the internal Line voltage Selector are contained in the RTD 710A Instruction Manual. See the Preface of this manual for the manual number.

EXTERNAL ARM SIGNAL JUMPER

Procedures for changing the External Arm Signal jumper are contained in the RTD 710A Instruction Manual. See the Preface of this manual for the manual number.

CRT MONITOR OUTPUT JUMPERS

Procedures for changing the CRT Monitor Output jumpers are contained in the RTD 710A Instruction Manual. See the Preface of this manual for the manual number.

CLOCK OUTPUT JUMPER

Procedures for changing the clock output jumper are contained in the RTD 710A Instruction Manual. See the Preface of this manual for the manual number.

RACKMOUNTING INSTRUCTIONS

Instructions for rackmounting the RTD 710A are contained in the RTD 710A Instruction Manual and in the Rackmount Kit for the RTD 710A manual. See the Preface of this manual for manual numbers.

Section 4
PERFORMANCE CHECK/ADJUSTMENT PROCEDURES

This section contains a combined procedure for performance checking and adjusting the RTD 710A, and a separate procedure for verifying its functional operation after being checked and adjusted.

PRELIMINARY INFORMATION

INTRODUCTION

The Performance Check/Adjustment Procedures are designed to compare the performance of the instrument against measurement instruments of known accuracy, and to detect, correlate, and eliminate by adjustment any variation from the electrical specifications of the RTD 710A contained in Appendix B of the RTD 710A Instruction Manual.

If the Procedures are to be used to Performance Check the instrument, then the **ADJUST** steps can be eliminated.

The separate Functional Operation Check Procedures may be used either as a pre- or post-performance check/adjustment check, or following the initial power up self-test to further ensure that the instrument is operational.

ANNOTATION

Where capital letters appear in text, they identify front- or rear-panel controls, connectors, or indicators on the RTD 710A (e.g., RANGE, CONTROL Indicator, etc.), or internal adjustment names (e.g., XO.1 ADJ, AC OFS, etc.). When used to identify internal adjustment names, a component identifier also appears (e.g., AC OFS, R 414).

Where italicized capital letters appear in text, they identify controls, connectors, or indicators on the test instruments (e.g., *STD AMPL, VOLTS/DIV, etc.*).

Where initial capital letters appear in test, they identify generic test instrument names (e.g., Function Generator, X, Bandwidth, etc.).

TERMS

When used in a performance check/adjust instruction, the terms **CHECK** and **ADJUST** are defined as follows:

CHECK: Indicates that the instruction accomplishes an electrical specification check.

ADJUST: Indicates a RTD 710A adjustment that is to be made to meet an electrical specification. It may precede a series of checks that are made to verify the adjustment, or it may follow a check where it is used to return the adjustment to a specific value.

TEST POINT AND ADJUSTMENT LOCATIONS

Circuit board illustrations showing the location of test point and adjustment locations are contained in the "Test Point and Adjustment Locations" section.

EQUIPMENT REQUIRED

The test equipment and other terms needed to perform the Performance Check/Adjustment Procedures are listed in Table 4-1. The Procedures are based on the firm item listed in Table 4-1. If other equipment is substituted, control settings or setups may differ. If the exact item of equipment is not available, refer to the minimum specifications column to see if other equipment may be substituted. Then check the Purpose column. If the measurement needs are not affected by the substitution, then use the substitute item and vary the procedure as needed to adapt the substitute item.

Table 4-1
EQUIPMENT REQUIRED

Description	Minimum Specifications	Usage	Examples of Applicable Equipment
Oscilloscope	Bandwidth, 500 MHz; Sensitivity, 5 mV/div.	Trigger, timing, and waveform measurements.	Tektronix 7904 with 7A26 Amplifier and 7A19 or 7A29 Amplifier and 7B80 Delayed Time Base.
X10 FET Probe		Check/adjust timing.	Tektronix P6201.
X10 Probe (2)	Input impedance, 10M ohm; Capacitance load, 15 pF; bandwidth, 250 MHz.	Oscilloscope input.	Tektronix P6106.
Digital Voltmeter	Accuracy 0.015%; Range ± 65 V.	Various voltage measurements.	Tektronix DM5010[1], or Keithley 191.
Sine Wave Generator	Frequency, 50 kHz and 250 kHz to 120 MHz; Amplitude stability, ± 1%.	Check vertical bandwidth.	Tektronix SG503[2] Leveled Sine Wave Generator.
Frequency Counter	Frequency, up to 200 MHz; Accuracy, 0.0002%.	Check/adjust system clock.	Tektronix DC5010[1].
Function Generator	Frequency, up to 1 MHz; Triangle waveform.	Check A/D Converter linearity.	Tektronix FG503[2] or FG502[2].
Calibration Generator	Rise time, 1 ns or less.	Check input rise time and check/adjust frequency compensation.	Tektronix PG506[2].
NTSC TV Generator	Conforms to TV system requirements.	Check TV triggers for backporch and clamp operation for Option 05.	Tektronix 1410 with SPG2 (For NTSC).
Waveform Monitor w/Cables	Accepts 1 or 5 Vp-p X,Y, and Z inputs.	Bandwidth and HF Transient Response Checks.	Tektronix 620.
50 ohm Feedthrough Termination	Connectors, male/female BNC.	Terminate various generators.	Tektronix Part 011-0049-01.
75 ohm Feedthrough Termination	Connectors, male/female BNC.	Terminate TV signal generator.	Tektronix Part 011-0055-00.
50-75 ohm Attenuator	Minimum Loss (ac coupled); Connectors, male/female BNC.	Check TV clamp.	Tektronix Part 011-0112-00.

Table 4-1 (Cont.)
EQUIPMENT REQUIRED

Description	Minimum Specifications	Usage	Examples of Applicable Equipment
50 ohm 10X Attenator	Connectors, male/female BNC.	Check/adjust frequency compensation.	Tektronix Part 067-0539-00.
Input RC Normalizer	Capacitance, 24 pF; Impedance, 1M ohm; Connectors, male/female BNC.	Check/adjust frequency compensation.	Tektronix Part 067-0539-00.
Input RC Normalizer	Capacitance, 40 pF; Impedance, 1M ohm; Connectors, male/female BNC.	Check/adjust frequency compensation.	Tektronix Part 067-0935-00.
T-Connector	2 female/1 male BNC.	Check Average Mode.	Tektronix Part 103-0030-00.
50 ohm Coaxial Cable (5)	Connectors, male BNC.	Monitor and signal interconnection.	Tektronix Part 012-0057-01.
75 ohm Coaxial Cable (2)	Connectors, male BNC.	Signal interconnection.	Tektronix Part 012-0047-00.
Dual Input Coupler	Connectors, 2 male/1 female BNC.	Connects one signal to two inputs.	Tektronix Part 067-0525-02.
High Frequency to BNC connector	Connectors, 1 female BNC, 1 female high-frequency connector.	Check/adjust frequency compensation.	Tektronix Part 131-1315-01.
Alignment Tool	Bit size, 3/32 in.; Low capacitance; Insulated; such as JFD Adjustment Tool 5284.	Used to make adjustments.	Tektronix Part 003-0489-00 or 003-675-00.
Alignment Tool	Bit size, 3/32 in.; Shank length at least 3-1/2"; insulated.	Used to make power supply adjustments.	
Service Kit		Provides extender boards, cables, and delay line adjustment tool needed to check and adjust the RTD 710A.	Tektronix Part 067-1376-00.

[1]Requires a TM5000 Mainframe.
[2]Requires a TM500 Mainframe.

INSTRUMENT PREPARATION

INSTRUMENT DISASSEMBLY

Before connecting the instrument to a power source and turning it on, remove the Top, Bottom, and Left Side (facing the front panel) Cabinet Covers. Do not remove the cover containing the Carrying Handle. Then remove the Main Chassis Cover over the circuit boards and the Circuit Board Retainer.

WARM-UP TIME

Before performing the Performance Check/Adjustment Procedures, the instrument must have been allowed to warm up for 20 minutes in an ambient temperature between 20°C and 30°C. Where a step in the procedure requires the instrument to be turned off to install or remove an extender board, the instrument should be allowed to again warm up for at least three (3) minutes.

MONITOR

Connect the Monitor's X, Y, and Z inputs through three (3) 50 ohm coaxial cables to their respective output connectors on the RTD 710A. Leave the Monitor connected throughout the Performance Check/Adjustment procedure, except when testing the RTD 710A's X, Y, and Z outputs.

PROCEDURAL INSTRUCTIONS

Each subsection (e.g., B. INPUT AND AUTO CAL, C. FREQUENCY COMPENSATION, etc.) is designed to be performed in order from start to finish. As such, test equipment settings may not be repeated at the beginning of each procedure within the subsection. For example, if procedure B1. Adjust Gain Cal Reference Signal were performed and the same test equipment was to be used for B2. CHECK CH1 OPERATION, then the test equipment connection and setup may not be described at the beginning of B2.

A. POWER SUPPLY

Equipment Required:

- Digital Voltmeter
- Oscilloscope
- Function Generator
- 50 ohm Termination
- Dual Input Coupler
- 10X Probe
- 50 ohm Coaxial Cable

A1. CHECK/ADJUST POWER SUPPLY VOLTAGES (A86/A84/A70)

a. Set the Digital Multimeter up to 200 Vdc.

b. Set the rear-panel PRINCIPAL POWER SWITCH and front-panel power switch to ON.

c. Push INIT twice to initialize the RTD 710A, then set CH1/CH2 RANGE to 500 mV.

d. Connect the Function Generator through a 50 ohm cable, 50 ohm termination, and Dual Input Coupler to CH1 and CH2. Set the generator for a 50 kHz, 1 Vp-p sine wave.

e. Set RESET/HOLD key to RESET (Acquisition).

f. Set the Oscilloscope bandwidth limit to 20 MHz.

g. Connect the Digital Voltmeter and Oscilloscope between the test points shown in Table 4-2 and L-GND (J842-1), on the A70 Main Interconnect Board and **CHECK** for the voltage and ripple limits indicated.

h. If +5 VD (J868-1) is out of tolerance, **ADJUST** +5VD Adj, R401 (A86) to +5.000 V.

i. If –5 VD (J870-5) is out of tolerance, **ADJUST** –5VD Adj, R245 (A86) to –5.000 V.

j. If +59.2 VL (J842-2) is out of tolerance, **ADJUST** +59.2 VL Adj, R748(A84) to +59.20 V.

CAUTION

Use a fully insulated alignment tool with at least a 3-1/2" shank to reach the above adjustments.

k. If any adjustments were made in h through g above, repeat step g.

Table 4-2
POWER SUPPLY OUTPUT AND RIPPLE VOLTAGES

Supply Name	Test Points (A70)	Output Voltage	Maximum Ripple Voltage (mV)	MaximumSpike Voltage (mV)
+5 VD	J868-1	+4.90 to +5.10	50	50
–5 VD	J870-5	–4.90 to –5.10	50	50
–2 VD	J870-12	–1.80 to –2.20	50	50
+15 VL	J842-5	+14.775 to +15.225	10	20
–15 VL	J842-6	–14.775 to –15.225	10	20
+5 VL	J842-9	+4.925 to +5.075	10	20
–5 VL	J842-10	–4.925 to –5.075	10	20
+59.2 VL	J842-2	+58.61 to +59.79	5	20
–59.2 VL	J842-3	–58.61 to –59.795	5	20

B. INPUT (A12) AND AUTO CAL (A14)

Equipment Required:

Oscilloscope	X10 Probe
Digital Voltmeter	50 ohm Cable
Calibration Generator	Alignment Tool

B1. CHECK +5 V REFERENCE VOLTAGE (A14)

a. Turn the front-panel power switch to STANDBY and the rear-panel PRINCIPAL POWER SWITCH to OFF.

b. Remove the Input Amp Module (A12 and A14), install the Extender (672-1303-00) from the Service Kit, and reinstall the Input Amp Module on the Extender.

c. Turn the rear-panel PRINCIPAL POWER SWITCH and front-panel power switch to ON.

d. Push INIT twice to initialize the RTD 710A.

e. Connect the Digital Voltmeter between TP300 and ground (TP030) on A14.

f. **CHECK** that the voltage is +5 V (±3 mV).

B2. CHECK ±1.2 V REFERENCE VOLTAGE (A14)

a. Connect the Digital Voltmeter between TP 360 and ground (TP030) on A14.

b. **CHECK** that the voltage is −1.2 V (±24 mV).

c. Connect the Digital Voltmeter between TP370 and ground (TP030) on A14.

d. **CHECK** that the voltage is +1.2 V (±24 mV).

e. Disconnect the Digital Voltmeter.

B3. ADJUST CH2 GAIN (A12)

a. Enter diagnostics mode by simultaneously pressing the MEASURE function keys V or V and 1/T or 1 ΔT.

b. Set diagnostic to 60259.

c. Push BREAK POINT SET to start the diagnostic routine.

d. Set RECORD LENGTH to 128.

e. Connect the STD AMPL signal from the Calibration Generator through a 50 ohm cable to CH1. Set the Generator output amplitude to 0.2 V.

f. Connect the Oscilloscope through a 10X probe to pin 14 of U300 and ground (TP200) on A12 and set the Oscilloscope as follows:

Volts/div:	100 mV
Time/div:	200 µs
BW:	20 MHz

g. Set the Oscilloscope variable gain for 4 division (oscilloscope) display.

h. Move the Oscilloscope 10X probe to pin 14 of U700 on A12.

i. **ADJUST** R662 on A12 for a 4 division Oscilloscope display.

j. Disconnect the Calibration Generator and Oscilloscope.

k. Push BREAK POINT CLR to stop the diagnostic routine.

B4. ADJUST AMPLIFIER IC (M377) OFFSET (A12/A14)

a. Set diagnostic to 60107.

b. Push BREAK POINT SET to start the diagnostic routine.

c. Set RECORD LENGTH to 128.

d. Connect the Digital Voltmeter between pin 7 and pin 9 of U200 on A12.

e. **ADJUST** M377 OFFSET1, R132 on A14 to 0V (±1 mV).

f. Connect the Digital Voltmeter between pin 14 of U300 and ground (TP200) on A12.

g. **ADJUST** CH1 DC, R214 on A12 to 0 V (+5 mV).

h. Push BREAK POINT CLR to stop the diagnostic routine.

i. Set diagnostic to 60207.

j. Push BREAK POINT SET to start the diagnostic routine.

k. Set RECORD LENGTH to 128.

l. Connect the Digital Voltmeter between pin 7 and pin 9 of U600 on A12.

m. **ADJUST** M377 OFFSET2, R232 on A14 to 0 V (±1 mV).

n. Connect the Digital Voltmeter between pin 14 of U700 and ground (TP200) on A12.

o. **ADJUST** CH2 DC, R654 on A12 to 0 V (±5 mV).

p. Push BREAK POINT CLR to stop the diagnostic routine.

q. Set diagnostic to 60257.

r. Push BREAK POINT SET to start the diagnostic routine.

s. Set RECORD LENGTH to 128.

t. **ADJUST** CH2 I.A OFS, R516 on A14 to 0 V (±5 mV).

u. Push BREAK POINT CLR to stop the diagnostic routine.

v. Disconnect the Digital Voltmeter.

B5. CHECK GAIN CAL REFERENCE OUTPUT (A14).

a. Connect the Digital Voltmeter between TP350 and ground (TP010) on A14.

b. Set diagnostic to 60307.

c. Push BREAKPOINT SET to start the diagnostic routine.

d. CHECK the Gain Cal Reference Output using Table 4-3. First set RECORD LENGTH as shown in the table. Then note the negative voltage with the J710 jumper in the NORM position (pins 1-2 jumpered). Then note the positive voltage with the J710 jumper in the TEST position (pins 2-3 jumpered). Finally, calculate the voltage difference and **CHECK** it against the table value.

e. Push BREAK POINT CLR to stop the diagnostic routine.

f. Disconnect the Digital Voltmeter.

B6. CHECK/ADJUST INPUT OFFSET (A14)

a. Push RECALL/LOC to return to normal operation.

b. Set the RTD 710A as follows:

CH1 and CH2 RANGE:	500 mV
CH1 and CH2 COUPLING:	GND
SAMPLE INTERVAL:	100 ns

Table 4-3
GAIN CAL REFERENCE OUTPUT VOLTAGE

RECORD LENGTH Setting	Voltage Difference (p-p)	RECORD LENGTH Setting	Voltage Difference (p-p)
0	0.1934-0.1941	1	0.2417-0.2426
2	0.3093-0.3106	3	0.3867-0.3882
4	0.4834-0.4853	5	0.6187-0.6212
6	0.7734-0.7765	7	0.9668-0.9707
8	1.1988-1.2037	9	1.5469-1.5531
10	1.9336-1.9413	11	2.4171-2.4268
12	3.0938-3.1062	13	3.8672-3.8827
14	4.8343-4.8536	15	6.1876-6.2124
16	7.7345-7.7655	17	9.6686-9.7073
18	11.9889-12.0370	19	15.4690-15.5310
20	19.3362-19.4137	21	24.1715-24.2684
22	30.9380-31.0620	23	38.6725-38.8275
24	48.3431-48.5368	25	61.8760-62.1240
26	77.3450-77.6550	27	96.6862-97.0737

c. Set CH1 OFFSET to 99%.

d. **ADJUST** INPUT OFFSET1, R107 on A14 so that the channel 1 Δ over-range indicator lights when Auto Calibration is made by pushing the AUTO CAL key.

e. Set CH1 OFFSET to 98%.

f. **CHECK** that the Δ over-range indicator exstinguishes when Auto Calibration is made by pushing the AUTO CAL key.

g. Set CH2 OFFSET to 99%.

h. **ADJUST** INPUT OFFSET2, R207 on A14 so that the channel 2 Δ over-range indicator lights when Auto Calibration is made by pushing the AUTO CAL key.

i. Set CH2 OFFSET to 98%.

j. **CHECK** that the Δ over-range indicator extinguishes when Auto Calibration is made by pushing the AUTO CAL key.

C. FREQUENCY COMPENSATION

Equipment Required:

Oscilloscope	Alignment Tool
Sine Wave Generator	50 ohm Cable
Calibration Generator	50 ohm Termination
Waveform Monitor	24 pF Normalizer

C1. ADJUST CH1 FREQUENCY COMPENSATION (A12)

a. Push INIT twice to initialize the RTD 710A, then set CH1 and CH2 RANGE to 500 mV.

b. Connect the positive FAST RISE output from the Calibration Generator through a 50 ohm cable and a 50 ohm termination to CH1. Set the generator for a 1 MHz, 5 division display.

c. Turn the rear-panel PRINCIPAL POWER SWITCH and front-panel power switch to OFF.

d. Remove the Trigger Board (A22) and disconnect W124 from the Trigger Board, then reinstall the Trigger Board.

e. Connect the Oscilloscope through a 50 ohm cable and a High-Frequency/BNC connector to W124. Set the Oscilloscope as follows:

Volts/div:	200 mV
Time/div:	2 ns

f. Turn the rear-panel PRINCIPAL POWER SWITCH and front-panel power switch to ON.

g. Push RECALL/LOC to return to normal operation.

h. **ADJUST** C128 and C131 located on U200 SMD on A12 for the best transient response on the Oscilloscope display and a rise time of about 2.6 ns. Figure 4-1 shows the effect of increasing or decreasing capacitors C128 and C131.

i. Turn the rear-panel PRINCIPAL POWER SWITCH and front-panel power switch to OFF.

j. Remove the Trigger Board and replace W124 to J124, then reinstall the Trigger Board.

k. Disconnect the Calibration Generator.

C2. CHECK/ADJUST CH1 BAND WIDTH (A12)

a. Turn the rear-panel PRINCIPAL POWER SWITCH and front-panel power switch to ON.

b. Connect the Sine Wave Generator through a 50 ohm cable and a 50 ohm termination to CH1. Set the Generator for a 50 kHz, six (6) division display on the monitor.

c. Set the Sine Wave Generator frequency to 115 MHz.

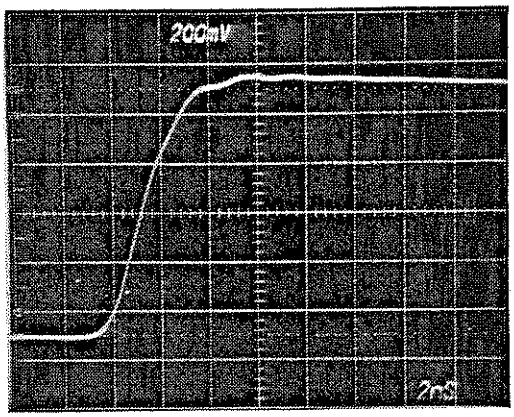
d. **CHECK** for a Monitor display of 4.2 divisions. If the display is not 4.2 divisions, **ADJUST** C131 located on U200 SMD on A12 for 4.2 division.

C3. ADJUST CH2 FREQUENCY COMPENSATION (High-speed sample mode) (A12)

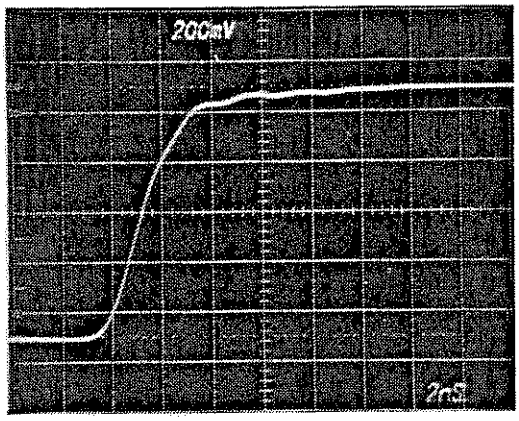
a. Set the RTD 710A as follows:

SAMPLE MODE:	HI SPD
SAMPLE INTERVAL:	5 ns
DISPLAY DOT/LINE:	DOT

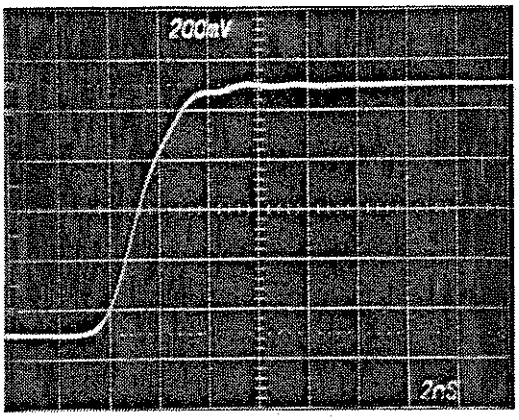
b. Set the Sine Wave Generator for a 28.6 MHz, six (6) division display on the monitor.



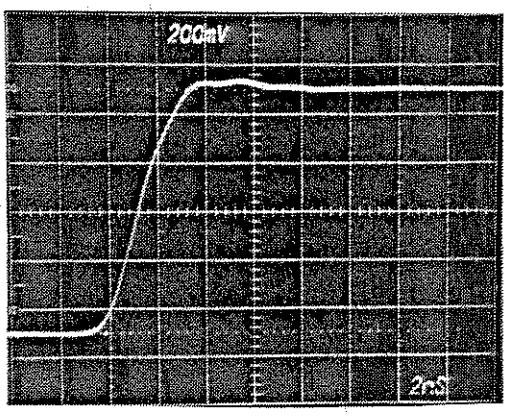
A. C128 TOO LARGE



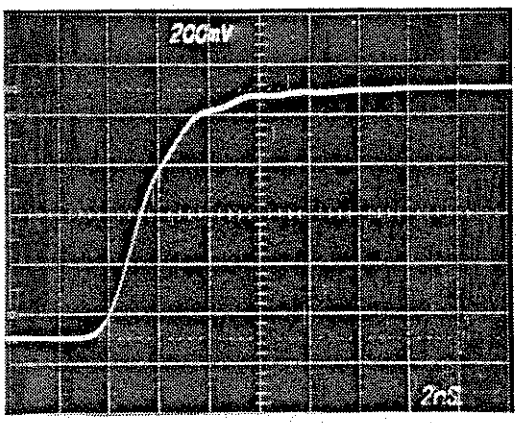
B. C128 TOO SMALL



C. ADJUSTED



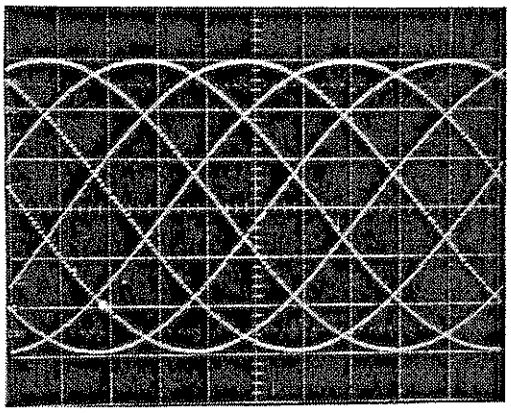
D. C131 TOO LARGE



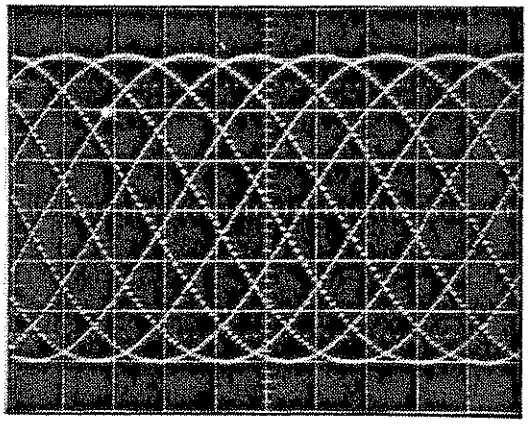
E. C131 TOO SMALL

7205-80

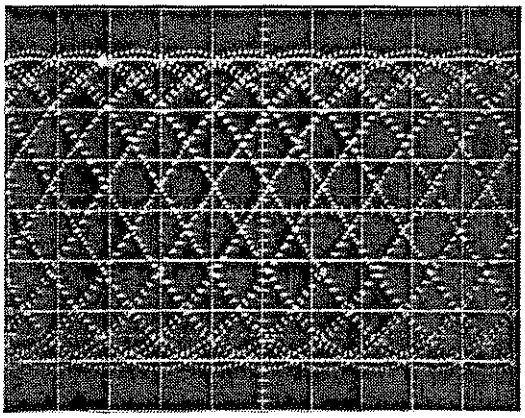
Fig. 4-1 Waveforms for adjusting CH1 Frequency Compensation



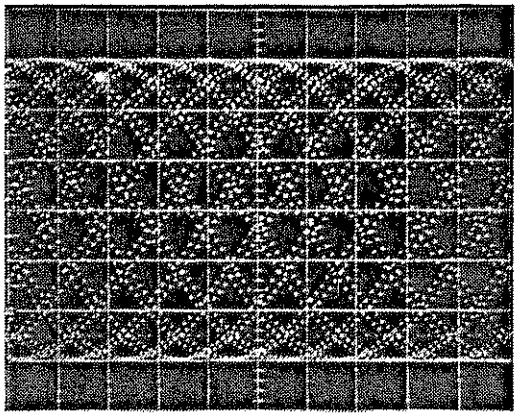
A. 28.6 MHz ADJUSTED



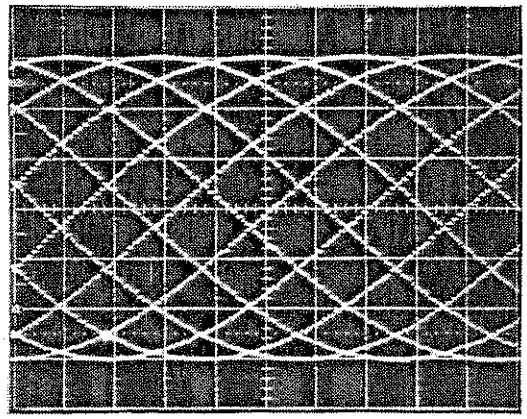
B. 44.4 MHz ADJUSTED



C. 91.0 MHz GAIN NOT COINCIDENT



D. 91.0 MHz NOT COINCIDENT



E. 91.0 MHz ADJUSTED

7205-81

Fig. 4-2 Waveforms for adjusting phase and gain

c. **ADJUST** C128 and C131 (mainly C128) located on U600 SMD on A12 so the phase and gain of the beat waveform coincide (minimum or no double-dot line patterns) Figure 4-2, when the AUTO CAL key is pushed.

d. Set the Sine Wave Generator to 4.4 MHz.

e. **ADJUST** C128 and C131 (mainly C131) located on U600 SMD on A12 so that phase and gain of the beat waveform coincide (minimum or no double-dot patterns) Figure 4-2, when the AUTO CAL key is pushed.

f. Set the Sine Wave Generator to 91.0 MHz.

g. **ADJUST** HI SPD HF, R114 on A12 so the phase and gain of the beat waveform coincide (minimum or no double-dot line patterns) Figure 4-2, when the AUTO CAL key is pushed.

h. Repeat steps b through g for the best possible coincidence of the phase and gain of the waveform.

i. Disconnect the Sine Wave Generator.

C4. ADJUST CH2 FREQUENCY COMPENSATED (A12)

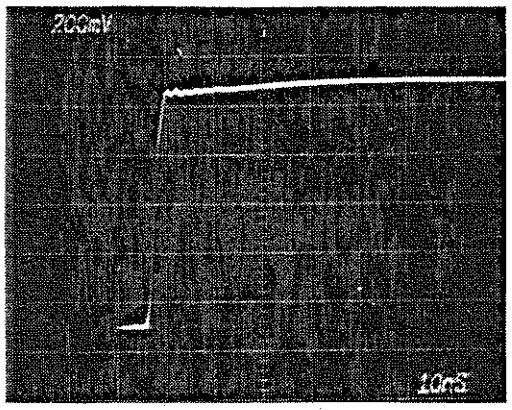
a. Push INIT twice to initialize the RTD 710A, then reset these controls:

CH2 RANGE: 500 mV
CH2 DISPLAY LOCATION: 1

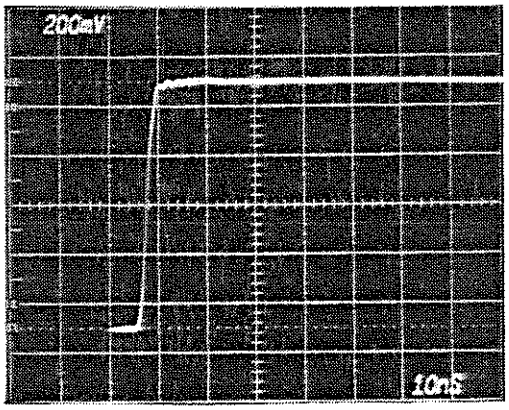
b. Connect the positive FAST RISE output from the Calibration Generator through a 50 ohm cable and a 50 ohm termination to CH2. Set the generator for a 1 MHz, 5 division Monitor display.

c. Turn the rear-panel PRINCIPAL POWER SWITCH and front-panel power switch to OFF.

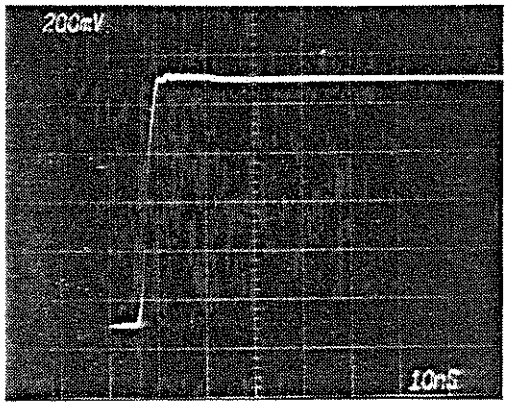
d. Remove the Trigger Board (A22) and disconnect W165 from the Trigger Board, then reinstall the Trigger Board.



A. C503 TOO LARGE



B. ADJUSTED



C. C503 TOO SMALL

7205-82

Fig. 4-3 Waveforms for adjusting CH2 Frequency compensation

e. Connect the Oscilloscope through a 50 ohm cable and a High-Frequency/BNC connector to W165. Set the Oscilloscope as follows:

Volts/div:	200 mV
Time/div:	10 ns

f. Turn the rear-panel PRINCIPAL POWER SWITCH and front-panel switch to ON.

g. Push RECALL/LOC to return to normal operation.

h. **ADJUST** C503 on A12 for the best transient response on the Oscilloscope display. Figure 4-3 shows the effect of increasing or decreasing capacitor C503.

i. Turn the rear-panel PRINCIPAL POWER SWITCH and front-panel power switch to OFF.

j. Remove the Trigger Board and replace W165 to J124, then reinstall the Trigger Board.

k. Disconnect the Calibration Generator.

C5. CHECK CH2 BAND WIDTH (A12)

a. Turn the rear-panel PRINCIPAL POWER SWITCH and front-panel power switch to ON.

b. Connect the Sine Wave Generator through a 50 ohm cable and a 50 ohm termination to CH2. Set the Generator for a 50 kHz, six (6) division display on the monitor.

c. Set the Sine Wave Generator frequency to 115 MHz.

d. **CHECK** for a Monitor display of at least 4.2 divisions.

C6. ADJUST CH1 ATTENUATOR COMPENSATION (A10)

a. Push INIT twice to initialize the RTD 710A, then reset these controls:

CH1 RANGE:	500 mV
CH1 COUPLING:	DC
CH2 COUPLING:	GND

b. Connect the Calibration Generator HIGH AMPL output through a 50 ohm cable, 50 ohm termination, and 24 pF Normalizer to CH1. Set the generator for a 1ms (1 kHz), 6-division monitor display.

c. **ADJUST** C104 on A10 for aberrations of ±2% or less.

d. Set CH1 RANGE to 620mV.

e. Set the Calibration Generator for an 6-division Monitor display.

f. **ADJUST** C116 on A10 for aberrations of ±2% or less.

g. Set the Calibration Generator for a 0.1 ms (10 kHz), 6-division Monitor display.

h. **ADJUST** C118 on A10 for **ADJUST** C118 on A10 for aberrations of ±2% or less.

i. Set CH1 RANGE to 6.2V.

j. Set the Calibration Generator for a 1 ms (1 kHz), 6-division Monitor display.

k. Set CH1 VERT ZOOM to 2.

l. **ADJUST** C110 on A10 for aberrations of ±2% or less.

m. Set the Calibration Generator for a 0.1 ms (10 kHz), 6-division Monitor display.

n. **ADJUST** C112 on A10 for aberrations of ±2% or less.

o. Disconnect the Calibration Generator.

C7. ADJUST CH2 ATTENUATOR COMPENSATION (A10)

a. Push INIT twice to initialize the RTD 710A, then reset these controls:

CH2 RANGE:	500 mV
CH2 COUPLING:	DC
CH1 COUPLING:	GND

b. Connect the Calibration Generator HIGH AMPL output through a 50 ohm cable, 50 ohm termination, and 24 pF Normalizer to CH2. Set the generator for a 1 ms (1 kHz), 6-division Monitor display.

c. **ADJUST** C204 on A10 for aberrations of ±2% or less.

d. Set CH2 RANGE to 620 mV.

e. Set the Calibration Generator for a 6-division Monitor display.

f. **ADJUST** C216 on A10 for aberrations of +2% or less.

g. Set the Calibration Generator for a 0.1 ms (10 kHz), 6-division Monitor display.

h. **ADJUST** C218 on A10 for aberrations of ±2% or less.

i. Set CH2 RANGE to 6.2 V.

j. Set the Calibration Generator for a 1 ms (1 kHz), 6-division Monitor display.

k. Set CH2 VERT ZOOM to 2.

l. **ADJUST** 210 on A10 for aberrations of ±2% or less.

m. Set the Calibration Generator of a 0.1 ms (10 kHz), 6-division Monitor display.

n. **ADJUST** C212 on A10 for aberrations of ±2% or less.

o. Disconnect the Calibration Generator.

D. A/D CONVERTER

There are two A/D Converter Boards in the RTD 710A, one for CH1 (A18/CH1) and one for CH2 (A18/CH2). Both boards are covered by the same procedures in this subsection. Rather than repeat the procedures, we list the procedures once using CH1 references, and include the CH2 references in parentheses. To accomplish this procedure, first perform all the procedures on CH1, then repeat the procedures for CH2.

Equipment Required:

Oscilloscope	X10 FET Probe
Digital Voltmeter	10X Probe
Sine Wave Generator	50 ohm Cable (2)
Functional Generator	50 ohm Termination (2)

D1. CHECK CH1 (CH2) A/D VOLTAGES AND VOLTAGE SUPPLIES (A18)

a. Turn the RTD 710A front-panel power switch to STANDBY and the rear-panel PRINCIPAL POWER SWITCH to OFF.

b. Remove the CH1 A/D Board A18/CH1 (CH2 A/D Board A18/CH2), install the A/D Extender from the Service Kit (067-1376-00), and reinstall the A/D Board on the extender.

c. Turn the RTD 710A rear-panel PRINCIPAL POWER SWITCH and the front-panel power switch to ON.

d. Connect the Digital Voltmeter between the test points listed in Table 4-4 and ground (TP001 through TP007 are grounds) on A18/CH1 (A18/CH2) and **CHECK** that the supplied voltage at each test point is within the Voltage Limits shown.

Table 4-4
SUPPLIED VOLTAGES

TEST POINTS	SUPPLIED VOLTAGE LIMITS (VOLTS)
TP040 (+15VL)	–14.775 - –15.225
TP050 (–15VL)	–14.775 - –15.225
TP060 (+5VL)	–4.925 - –5.075
TP070 (–5VL)	–4.925 - –5.075
TP020 (–5VD)	–4.900 - –5.100
TP030 (–2VD)	–1.800 - –2.200

e. Connect the Digital Voltmeter between the test points listed in Table 4-5 and ground (TP001 through TP007 are grounds) on A18/CH1 (A18/CH2) and **CHECK** that each A/D voltage supply is within the Voltage Limits shown.

Table 4-5
A/D POWER SUPPLY VOLTAGES

TEST POINTS	VOLTAGE LIMITS (VOLTS)
TP810 (+10 V)	9.985 - 10.015
TP820 (–10 V)	–9.750 - –10.25
TP 850 (+3 V)	2.80 - 2.83
TP250	0.99 - 1.09
TP260	–0.90 - –1.00
TP550	0.475 - 0.525
TP560	–0.01 - +0.01
TP650	–0.025 - +0.025
TP660	–0.475 - –0.525

D2. ADJUST DAC CLOCK (A18)

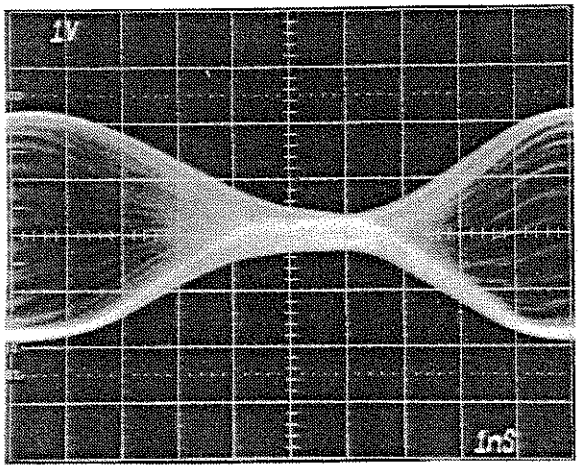
a. Push INIT twice to initialize the RTD 710A, then reset CH1 (CH2) RANGE to 500 mV.

b. Connect the Sine Wave Generator through a 50 ohm Cable and 50 ohm Termination to CH1 (CH2). Set the generator for a 49.2 MHz, 6-division Monitor display.

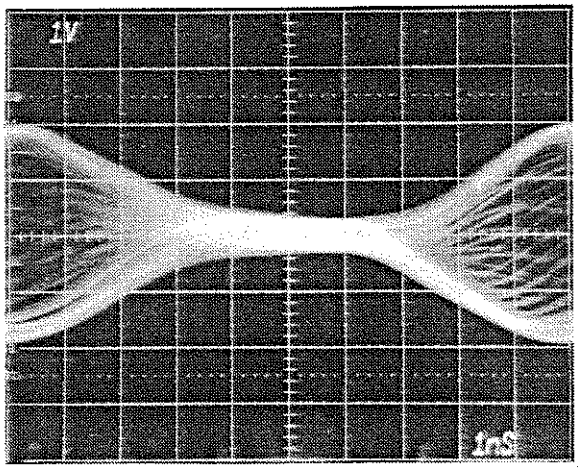
c. Connect the Oscilloscope through a X10 Probe from the EXT TRIG INPUT to TP200 on A18/CH1 (A18/CH2). Also connect the Oscilloscope X10 FET Probe to TP450 and its associated ground on A18/CH1 (A18/CH2) and set it as follows:

VOLTS/div:	1 V
TIME/div:	1 ns
TRIGGER:	Norm, AC, Ext

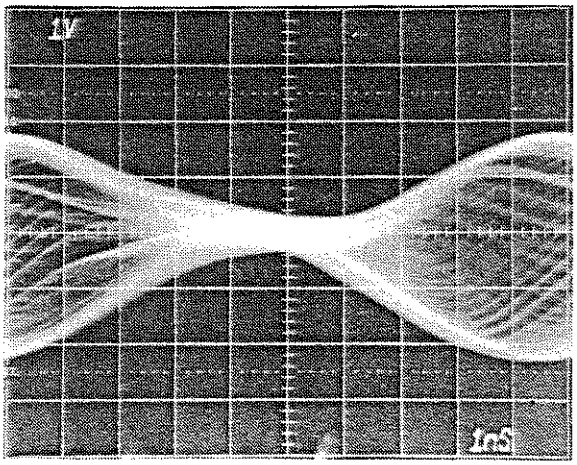
d. Move the delay control of DL904 on A18/CH1 (A18/CH2) to the rightmost position to maximize the clock delay.



A. DELAY TIME OF DL904 IS TOO LONG



B. DL904 IS ADJUSTED SATISFACTORILY



C. DELAY TIME OF DL904 IS TOO SHORT

6398-22

Fig. 4-4 Differential output waveform

e. Adjust the Oscilloscope to obtain a reference waveform display similar to Figure 4-4A.

f. **CHECK** that the Oscilloscope waveform changes as shown in Figure 4-4 as the delay control on DL904 is moved.

g. **ADJUST** DL904 for the longest flat portion of the Oscilloscope waveform as shown in Figure 4-4B.

D3. ADJUST 2ND A/D STROBE PULSE (A18)

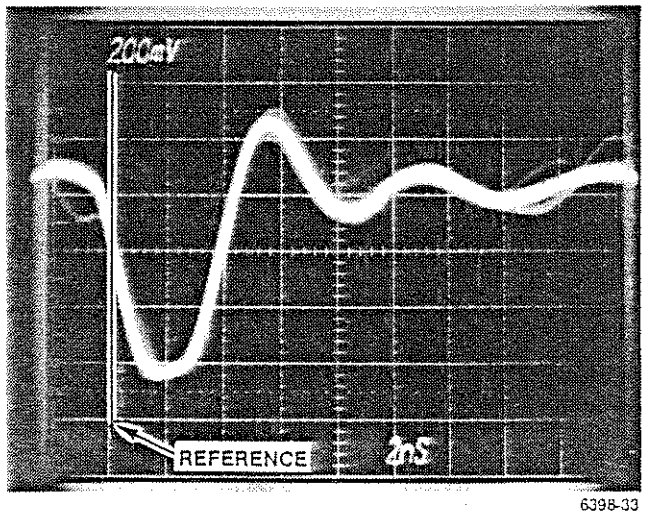
a. Move the Oscilloscope X10 FET Probe to TP300 and its associated ground on A18/CH1 (A18/CH2). Set the Oscilloscope as follows:

VOLTS/div:	200 mV
TIME/div:	2 ns

b. Adjust the delayed sweep on the Oscilloscope to obtain a reference waveform display similar to Figure 4-5.

c. Move the X10 FET Probe from TP300 to TP500 and its associated ground on A18/CH1 (A18/CH2) and set SAMPLE INTERVAL to 100 ns.

d. **ADJUST** DL910 on A18/CH1 (A18/CH2) so the time between CLK5 (TP300) and CLK7 (TP500) is 14.8 ns ±0.1 ns (Figure 4-6).



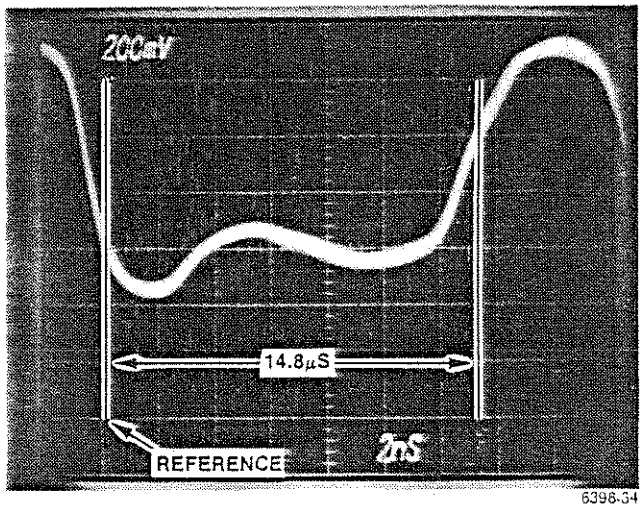
6398-33

Fig. 4-5 2nd A/D strobe pulse reference waveform

e. Disconnect the Sine Wave Generator and Oscilloscope.

D4. ADJUST TRACK AND HOLD DC OFFSET VOLTAGE (A18).

a. Turn the RTD 710A front-panel power switch to STANDBY and the rear-panel PRINCIPAL POWER SWITCH to OFF.



6398-34

Fig. 4-6 Waveform to adjust 2nd A/D strobe pulse delay

b. Remove the 75 ohm coaxial cable W123 from the connector J123 on A18/CH1.

c. Turn the RTD 710A rear-panel PRINCIPAL POWER SWITCH and the front-panel power switch to ON.

d. Push RECALL/LOC to return to normal operation.

e. Push MEASURE V Δ V key and CURSOR1 key.

f. Adjust R110 on A18/CH1 (A18/CH2) as close to 0V as possible.

g. Turn the RTD 710A front-panel power switch to STANDBY and the rear-panel PRINCIPAL POWER SWITCH to OFF.

h. Replace the W123 cable.

D5. ADJUST LINEARITY OF 1ST A/D CONVERTER (A18)

a. Push INIT twice to initialize the RTD 710A, then reset the RTD 710A as follows:

CH1 (CH2) RANGE:	500 mV
CH1 (CH2) COUPLING:	DC
CH2 (CH1) COUPLING:	GND
SAMPLE INTERVAL:	500 ns

b. Connect the Function Generator through a 50 ohm Cable and 50 ohm Termination to CH1 (CH2). Set the generator for a 1 kHz, 750 mV (6-division Monitor display) triangle waveform.

c. Connect the Oscilloscope EXT TRIG INPUT through a 10X Probe to TP200 on A18/CH1 (A18/CH2).

d. Set the Oscilloscope as follows:

Volts/div:	200 mV
Time/div:	10 ns
Trigger:	Norm, AC, EXT
Coupling:	GND

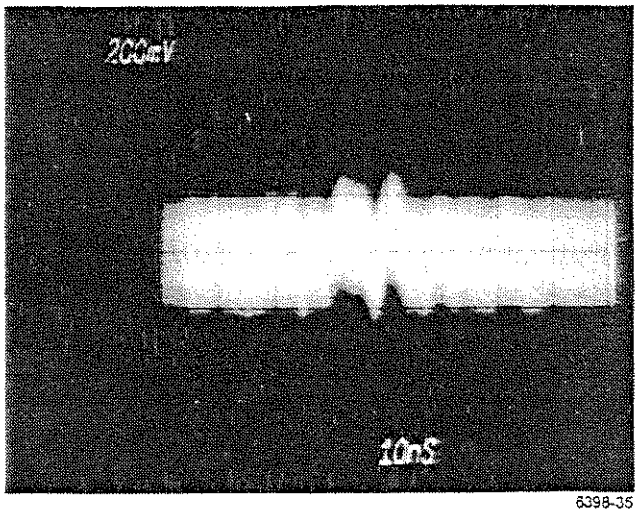
e. Set the Oscilloscope trace to graticule center.

f. Change Oscilloscope coupling to DC.

g. Connect the Oscilloscope through a X10 FET Probe to TP450 and its associated ground on A18/CH1 (A18/CH2).

h. **ADJUST** R250 and R260 on A18/CH1 (A18/CH2) so the center pulsed portion of the waveform is centered about 0 V and the display image has the least amount of fuzziness (Figure 4-7). In some cases, the pulsed portion is level or lower than the flat portion.

i. Disconnect the Function Generator and Oscilloscope.



6398-35

Fig. 4-7 Waveform to adjust 1st A/D linearity

D6. CHECK/ADJUST BEAT WEAVEFORM (A18)

a. Set the RTD 710A as follows:

CH1 (CH2) COUPLING:	AC
SAMPLE INTERVAL:	10 ns
TRIG DELAY:	–2040

b. Connect the Sine Wave Generator through a 50 ohm Cable and 50 ohm Termination to CH1 (CH2). Set the generator for a 50 MHz, 7-division beat waveform on the Monitor display.

c. **ADJUST** DL910 on A18/CH1 (A18/CH2) so the bit error (shown by fuzziness or jitter in the waveform) is at a minimum.

d. Set SAMPLE INTERVAL and Generator Frequency as shown in Table 4-6 and **CHECK** that the waveform has no bit error. If bit error is observed, **ADJUST** DL910 on A18/CH1 (A18/CH2) just slightly until the bit error disappears.

e. Disconnect the Sine Wave Generator.

Table 4-6
BEAT CHECK SETTINGS

Sample Interval	Generator Frequency
10 ns	50 MHz
10 ns	100 MHz

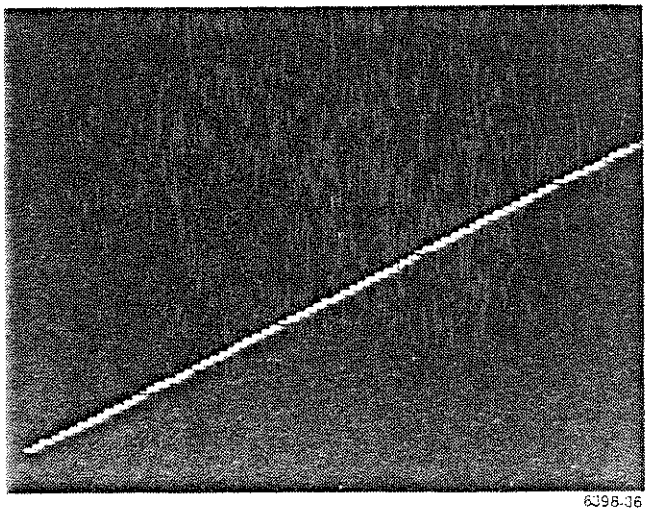
D7. CHECK/ADJUST LINEARITY OF 2ND A/D (A18)

a. Set the RTD 710A as follows:

CH1 (CH2) COUPLING:	DC
Trigger	
SLOPE:	+HYS
LEVEL1:	10%
LEVEL2:	–10%
SAMPLE INTERVAL:	100 ns
DISPLAY LOCATION:	CH1 (CH2)
VERT ZOOM:	8
HORIZ ZOOM:	4

b. Connect the Function Generator through a 50 ohm Cable and 50 ohm Termination to CH1 (CH2). Set the generator for a 1 kHz, 1.0 V (8-division Monitor display) triangle waveform.

c. Select TRIG DELAY and set it to obtain a waveform similar to Figure 4-8.



6398-36

Fig. 4-8 Waveform to adjust 2nd A/D linearity

d. **ADJUST** R650, R550, and R660 on A18/CH1 (A18/CH2) for the best linearity of the waveform.

e. Press the RESET/HOLD key to hold the RTD 710A.

f. Set TRIGGER MODE to SGL and select AVE/ENV # OF TIMES and set it to 2048.

g. Press the RESET/HOLD key to reset the RTD 710A.

h. **CHECK** that Monitor display is linear. If it isn't set TRIGGER MODE to AUTO and repeat steps d through h.

i. Turn the RTD 710A front-panel power switch to STANDBY and the rear-panel PRINCIPAL POWER SWITCH to OFF.

j. Remove the CH1 (CH2) A/D Board from the A/D Extender, remove the A/D Extender, and reinstall the A/D Board in the instrument.

k. Turn the RTD 710A rear-panel PRINCIPAL POWER SWITCH and the front-panel power switch to ON.

l. Disconnect the Function Generator.

D8. ADJUST DC LEVEL FOR BREAK POINT FUNCTION (A18)

a. Push INIT twice to initialize the RTD710A, then reset these controls:

CH1 (CH2) COUPLING:	GND
SAMPLE INTERVAL:	100 ns
VERT ZOOM:	32
DISPLAY LOCATION:	CH1 (CH2)

b. Select BREAK POINT SET and set it to 256.

c. Select SAMPLE INTERVAL and set it to 10 ns.

d. Select BREAK POINT SET and set it to 512.

e. Select SAMPLE INTERVAL and set it to 100 ns.

f. **CHECK** that the breakpoints are displayed after the trigger point on the Monitor display.

g. **ADJUST** C120 on A18/CH1 so the display baseline before and after the breakpoint is at the same level (Figure 4-9).

NOTE

The 10 ns baseline may be very noisy.

h. Change RECORD MODE to AVE and set AVE # OF TIMES to 512.

i. **CHECK** that the DC level shift is within ±6 LSBs (1.5 divisions).

j. Change SAMPLE MODE to HI SPD.

k. Clear the breakpoints as follows:

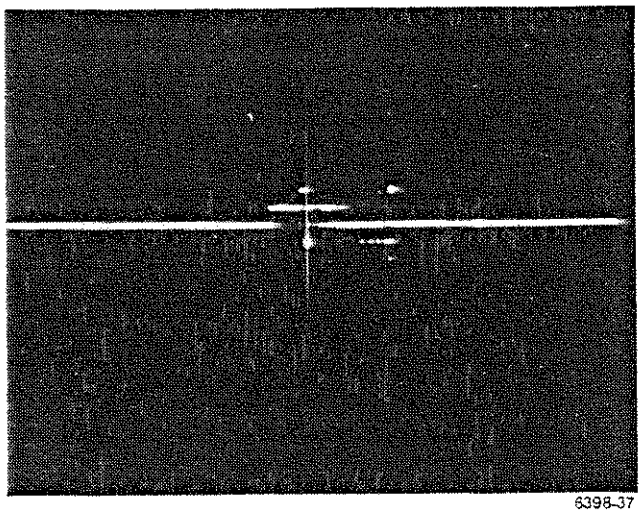
(1) Push the BREAK POINT DISPLAY key.

(2) Rotate the Parameter Entry Knob to select the highest addressed breakpoint in the RECORDING Indicator.

(3) Push BREAK POINT CLR as many times as necessary until the RECORDING Indicator reads zero (0).

l. Select BREAK POINT SET and set it to 256.

m. Select SAMPLE INTERVAL and set it to 5 ns.



6398-37

Fig. 4-9 Waveform to adjust breakpoint DC level

n. Select BREAK POINT SET and set it to 512.

o. Select SAMPLE INTERVAL and set it to 10 ns.

p. **CHECK** that the DC level shift is within ±10 LSBs (2.5 divisions) as shown in Figure 4-9, except for a bit or two at the breakpoint change point.

E. TRIGGER

Equipment Required:

- Oscilloscope
- Digital Voltmeter
- Sine Wave Generator
- Function Generator
- Calibration Generator
- Monitor
- Service Kit
- 10X Probe
- 50 ohm Cable
- 50 ohm Termination
- Dual Input Coupler
- Alignment Tool
- 40 pF Normalizer

E1. CHECK CH1 TRIGGER PATH (A22)

a. Push INIT twice to initialize the RTD 710A, then reset these controls:

CH1/CH2 RANGE:	500 mV
CH1/CH2 COUPLING:	DC
SAMPLE INTERVAL:	1 µs
TRIGGER MODE:	NORM

b. Connect the Oscilloscope through a X10 Probe to TP400-2 and its associated ground on A22 and set its vertical input for 500 mV/div.

c. Connect the Function Generator through a 50 ohm Cable and 50 ohm Termination to CH1. Set the generator for a 1 kHz, 1.0 V, triangle waveform.

d. **CHECK** that the Oscilloscope display is approximately 2 Vp-p.

e. Disconnect the X10 Probe.

E2. ADJUST CH1 TRIGGER AC COUPLING OFFSET (A22)

a. Set the RTD 710A as follows:

CH1 COUPLING:	GND
TRIGGER COUPLING:	AC

b. Connect the Digital Voltmeter between TP400-2 and its associated ground on A22.

c. **ADJUST** AC OFS, R414 on A22 to 0 V (±2 mV).

E3. ADJUST CH1 TRIGGER DC COUPLING OFFSET (A22)

a. Set TRIG COUPLING to DC.

b. Set CH1 COUPLING to DC.

c. **ADJUST** INT1 OFS, R108 on A22 so the average shift level of the trigger point on the Monitor is 0 when the TRIGGER SLOPE is switched between + and −.

d. Set CH1 COUPLING to GND.

E4. ADJUST CH1 TRIGGER HF REJ COUPLING OFFSET (A22)

a. Set TRIGGER COUPLING to HF REJ.

b. **ADJUST** HF OFS, R428 to 0 V (±2 mV). If unable to adjust within the limits, repeat procedures E2 through E4.

c. Disconnect the Digital Voltmeter and Function Generator.

E5. CHECK CH2 TRIGGER PATH (A22)

a. Change TRIG SOURCE to CH2.

b. Connect the Oscilloscope through a X10 Probe to TP400-2 and its associated ground on A22 and set its vertical input for 500 mV/div.

c. Connect the Function Generator through a 50 ohm Cable and a 50 ohm Termination to CH2 and set the generator for a 1 kHz, 1.0 V, triangle waveform.

d. **CHECK** that the Oscilloscope display is approximately 2 Vp-p.

e. Disconnect the X10 Probe.

E6. ADJUST CH2 TRIGGER DC COUPLING OFFSET (A22)

a. Set TRIGGER COUPLING to DC.

b. **ADJUST** INT2 OFS, R208 on A22 so the average shift level of the trigger point on the Monitor is 0 when the TRIGGER SLOPE is switched between + and −.

E7. CHECK EXT TRIG IN PATH (A22)

a. Set CH2 RANGE to 5 V and set the Function Generator for 10 Vp-p Monitor display. Then set CH2 RANGE to 800 mV and move the Function Generator output to EXT TRIG IN.

b. Set TRIG SOURCE to EXT.

c. Connect the X10 Probe from the Oscilloscope to TP400-2 and its associated ground on A22.

d. **CHECK** that the Oscilloscope display is approximately 1.8 Vp-p.

e. Disconnect the Function Generator and Oscilloscope.

E8. ADJUST EXTERNAL TRIGGER DC COUPLING OFFSET (A22)

a. Connect the Digital Voltmeter to TP400-2 and its associated ground on A22.

b. **ADJUST** EXT OFS, R312 on A22 to 0 V (±2 mV).

c. Disconnect the Digital Voltmeter.

E9. ADJUST TRIGGER LEVEL (A22)

a. Set the RTD 710A as follows:

CH1 COUPLING:	AC
TRIGGER SOURCE:	CH1

b. Connect the Oscilloscope through a X10 Probe to TP470 and ground (TP985) on A22.

c. **CHECK** that the Oscilloscope display has no oscillation.

d. Move the X10 Probe to TP480 and ground (TP985) on A22.

e. **CHECK** that the Oscilloscope display has no oscillation.

f. Disconnect the Oscilloscope.

g. Connect the Digital Voltmeter between TP470 and ground (TP985) on A22.

h. Select TRIG LEVEL 1 and set it to +99%.

i. **ADJUST** TL1, R478 to +0.860 V (±5 mV).

j. Select TRIG LEVEL 2 and set it to +99%.

k. Move the Digital Voltmeter to TP480 and ground (TP985) on A22.

l. **ADJUST** TL2, R480 on A22 to +1.130 V (±5 mV).

m. Set TRIG LEVEL 2 to 0%, then select TRIG LEVEL 1 and set it to 0%.

n. Disconnect the Digital Voltmeter.

E10. CHECK TRIGGER COUPLING (A22)

a. Set CH1 COUPLING to DC.

b. Connect the Oscilloscope through a X10 Probe to TP400-2 and its associated ground on A22.

c. Connect the Function Generator through a 50 ohm Cable and 50 ohm Termination to CH1 and set the generator for a 10 kHz, 5-division, negative

offset, square waveform on the Oscilloscope display.

d. **CHECK** that the waveform is a clean square waveform as shown in Figure 4-10A.

e. Select each TRIGGER COUPLING in the REJ set (HF, LF, and AC) except DC, and **CHECK** that the Oscilloscope displays are the same as those shown in Figures 4-10B through 4-10D.

f. Disconnect the Function Generator.

E11. CHECK EXT TRIGGER INPUT COMPENSATION (A22)

a. Set TRIGGER SOURCE to EXT.

b. Set the Oscilloscope vertical input to 200 mV/div and the sweep speed to 200 µs/div.

c. Connect the Calibration Generator through a 50 ohm Cable and 40 pF Normalizer to EXT TRIGGER IN. Set the generator for a 1 kHz, 5-division Oscilloscope display.

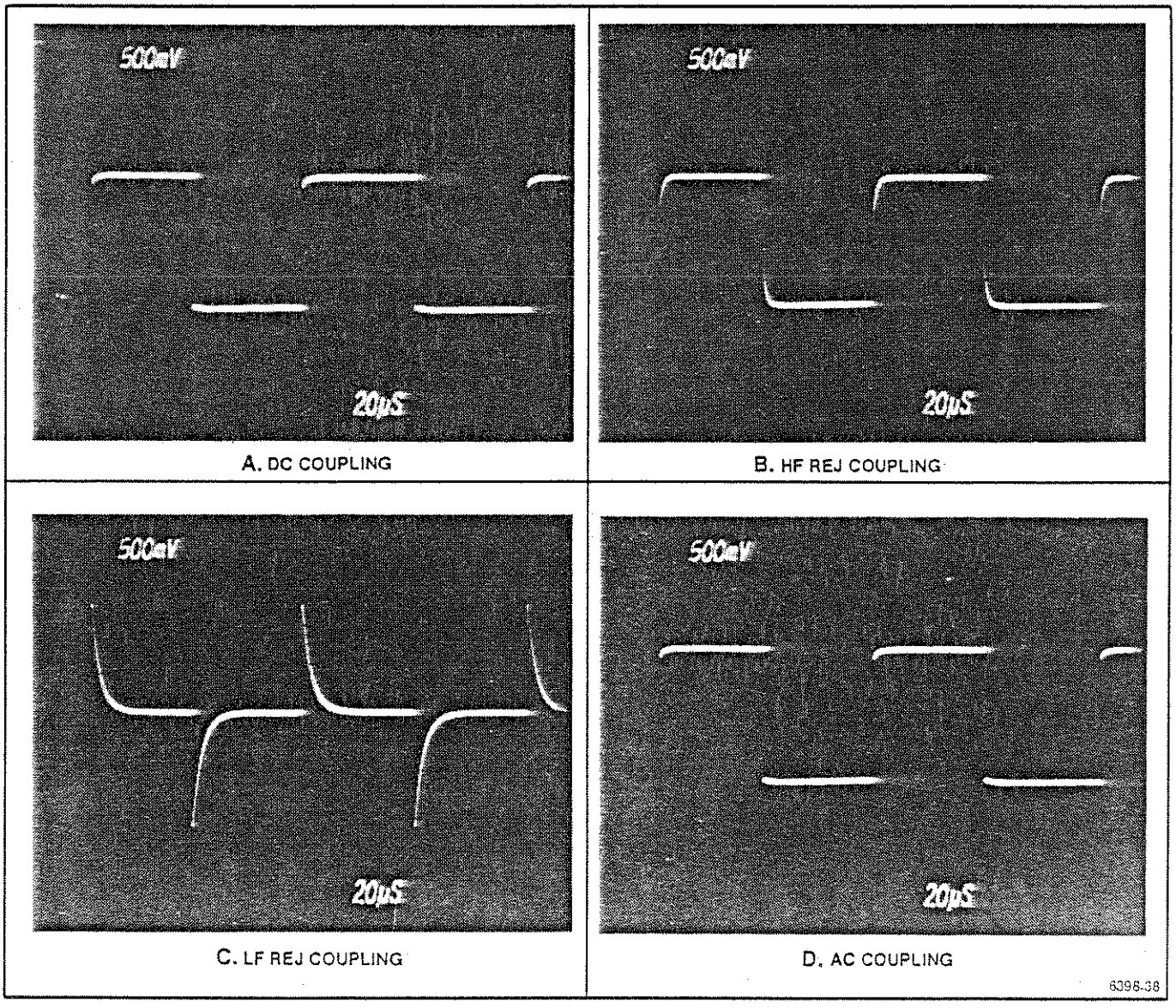


Fig. 4-10 Waveforms to check trigger coupling

d. **CHECK** that the Oscilloscope display is a clean square waveform.

e. Disconnect the Oscilloscope and Calibration Generator.

E12. CHECK TRIGGER SLOPE (A22)

a. Set the RTD 710A as follows:

SAMPLE INTERVAL:	20 ns
TRIGGER SOURCE:	CH1

b. Connect the Sine Wave Generator through a 50 ohm Cable and 50 ohm terminator to CH1 and set the generator for a 50 kHz, 800 mVp-p Monitor display (4-divisions).

c. **CHECK** that the Monitor display is stable.

d. Set TRIG SLOPE to –.

e. **CHECK** that the Monitor display is stable.

f. Set TRIG SLOPE to BI slope (both + and – indicators are illuminated) and TRIG LEVEL 2 to –20%.

g. **CHECK** that the Monitor display is unstable.

h. Set TRIGGER SLOPE to +HYS.

i. **CHECK** that the Monitor display is stable.

j. Select TRIG LEVEL 2 and set it to –60%.

k. **CHECK** that STATUS TRIG'D LED is not illuminated (not triggered).

l. Select TRIG LEVEL 2 to 0%.

m. Set TRIGGER SLOPE TO –HYS.

n. **CHECK** that the Monitor display is stable.

o. Select TRIG LEVEL 1 and set it to 60%.

p. **CHECK** that the STATUS TRIG'D LED is not illuminated (not triggered).

q. Set TRIG LEVEL 1 to 0%.

r. Disconnect the Sine Wave Generator.

E13. CHECK INTERNAL 20 MHz TRIGGERING (A22).

a. Push INIT twice to initialize the RTD 710A, then reset these controls:

CH1/CH2 RANGE:	100 mV
CH1/CH2 COUPLING:	DC
SAMPLE INTERVAL:	20 ns

b. Connect the Sine Wave Generator through a 50 ohm Cable, 50 ohm Termination, and Dual Input Coupler to CH1 and CH2. Set the generator for a 20 MHz, 78 mV (3.12 divisions) Monitor display.

c. Set CH1 RANGE to 800 mV (0.39 divisions) Monitor display.

d. Set TRIGGER MODE to NORM.

e. **CHECK** that the TRIG'D LED is illuminated at each of the TRIGGER function settings shown in Table 4-7. With some Trigger COUPLING settings, TRIG LEVEL 1 may need to be readjusted slightly.

Table 4-7
20 MHz INTERNAL TRIGGER CHECK SETTINGS

Trigger SOURCE	Trigger SLOPE	Trigger COUPLING
CH1	+	DC, LF REJ, AC
	–	
CH2	+	DC, LF REJ, AC
	–	

E14. CHECK INTERNAL 100 MHz TRIGGERING (A22)

a. Set CH1 RANGE to 100 mV and TRIGGER MODE to AUTO.

b. Set the Sine Wave Generator for a 100 MHz, 109 mV (4.36 divisions) Monitor display.

c. Set CH1 RANGE to 800 mV (0.54 divisions) Monitor display.

d. Set TRIGGER MODE to NORM.

e. **CHECK** that the TRIG'D LED is illuminated at each of the TRIGGER function settings shown in Table 4-8. With some Trigger COUPLING settings, TRIG LEVEL 1 may need to be readjusted slightly.

Table 4-8
100 MHz INTERNAL TRIGGER CHECK SETTINGS

Trigger SOURCE	Trigger SLOPE	Trigger Coupling
CH1	+	DC, LF REJ, AC
	−	
CH2	+	DC, LF REJ, AC
	−	

E15. CHECK INTERNAL 50 KHz TRIGGERING (A22)

a. Set CH1 RANGE to 100 mV and TRIGGER MODE to AUTO.

b. Set the Sine Wave Generator for a 50 kHz, 78 mV (3.12 divisions) Monitor display.

c. Set CH1 RANGE to 800 mV (0.39 division) Monitor display.

d. Set TRIGGER MODE to NORM.

e. **CHECK** that the TRIG'D LED is illuminated at each of the TRIGGER function settings shown in Table 4-9. With some Trigger COUPLING settings. TRIG LEVEL 1 may need to be readjusted slightly.

Table 4-9
50 kHz INTERNAL TRIGGER CHECK SETTINGS

Trigger SOURCE	Trigger SLOPE	Trigger Coupling
CH1	+	HF REJ, LF REJ
	−	
CH2	+	HF REJ, LF REJ
	−	

E16. CHECK INTERNAL 30 Hz TRIGGERING (A22)

a. Set the RTD 710A as follows:

CH1 RANGE:	100 mV
TRIGGER MODE:	AUTO
SAMPLING INTERVAL:	20 µs

b. Replace the Sine Wave Generator with a Function Generator and set the generator for a 30 Hz, 78 mV (3.12 divisions) Monitor display.

c. Set Ch1 RANGE to 800 mV (0.39 division) Monitor display.

d. Set TRIGGER MODE to NORM.

e. **CHECK** that the display is stable and the TRIG'D LED is illuminated at each of the TRIGGER function settings shown in Table 4-10. With some Trigger COUPLING settings, TRIG LEVEL 1 may need to be readjusted slightly.

f. Disconnect the Function Generator.

Table 4-10
30 Hz INTERNAL TRIGGER CHECK SETTINGS

Trigger SOURCE	Trigger SLOPE	Trigger Coupling
CH1	+	AC
	−	
CH2	+	AC
	−	

E17. CHECK EXTERNAL 20 MHz TRIGGERING (A22)

a. Push INIT twice to initialize the RTD 710A, then reset these controls.

CH1 RANGE:	400 mV
CH1 COUPLING:	DC
SAMPLE INTERVAL:	20 ns
TRIGGER SOURCE:	EXT

b. Connect the Sine Wave Generator through a 50 ohm Cable, 50 ohm Termination, and Dual Input Coupler to CH1 and EXT TRIG IN. Set the generator for a 20 MHz, 500 mV Monitor display.

c. Set TRIGGER MODE to NORM.

d. **CHECK** that the TRIG'D LED is illuminated at each of the TRIGGER function settings shown in Table 4-11. With some Trigger COUPLING settings, TRIG LEVEL 1 may need to be readjusted slightly.

Table 4-11
20 MHz EXTERNAL TRIGGER CHECK SETTINGS

Trigger SOURCE	Trigger SLOPE	Trigger Coupling
EXT	+	DC, LF REJ, AC
	−	

E18. CHECK EXTERNAL 100 MHz TRIGGERING (A22)

a. Set TRIGGER MODE to AUTO.

b. Set the Sine Wave Generator for a 50 kHz, 700 mV Monitor display.

c. Set TRIGGER MODE to NORM.

d. Set the Sine Wave Generator to 100 MHz.

e. **CHECK** that the TRIG'D LED is illuminated at each of the TRIGGER function settings shown in Table 4-12. With some Trigger COUPLING settings, TRIG LEVEL 1 may need to be readjusted slightly.

Table 4-12
100 MHz EXTERNAL TRIGGER CHECK SETTINGS

Trigger SOURCE	Trigger SLOPE	Trigger Coupling
EXT	+	DC, LF REJ, AC
	−	

E19. CHECK EXTERNAL 50 KHz TRIGGERING (A22)

a. Set TRIGGER MODE to AUTO.

b. Set the Sine Wave Generator for a 50 KHz, 500 mV (5-divisions) Monitor display.

c. Set TRIGGER MODE to NORM.

e. **CHECK** that the TRIG'D LED is illuminated at each of the TRIGGER function settings shown in Table 4-13. With some Trigger COUPLING settings, TRIG LEVEL 1 may need to be readjusted slightly.

Table 4-13
50 kHz EXTERNAL TRIGGER CHECK SETTINGS

Trigger SOURCE	Trigger SLOPE	Trigger Coupling
XT	+	HF, REJ, LF REJ
	−	

E20. CHECK EXTERNAL 30 Hz TRIGGERING (A22)

a. Set TRIGGER MODE to AUTO and SAMPLING INTERVAL to 20 ms.

b. Replace the Sine Wave Generator with a Function Generator and set the generator for a 30 Hz, 500 mV (5-divisions) Monitor display.

c. Set TRIGGER MODE to NORM.

e. **CHECK** that the display is stable and the TRIG'D LED is illuminated at each of the TRIGGER function settings shown in Table 4-14. With some Trigger COUPLING settings, TRIG LEVEL 1 may need to be readjusted slightly.

e. Disconnect the Function Generator.

Table 4-14
30 Hz EXTERNAL TRIGGER CHECK SETTINGS

Trigger SOURCE	Trigger SLOPE	Trigger SOURCE
EXT	+	AC
	−	

E21. ADJUST PROBE CAL SIGNAL (A22)

a. Remove the shorting strap from P800 on A22.

b. Connect the Digital Voltmeter Low lead to chassis ground and connect the Volts lead to the PROBE CAL terminal.

c. **ADJUST** R810 on A22 to 4.020 V.

d. Replace the shorting strap on P800 on A22.

e. Connect the Oscilloscope through a X10 Probe to the PROBE CAL terminal.

f. **CHECK** that the square wave on the Oscilloscope display is 4 V and approximately 1 kHz.

g. Disconnect the Digital Voltmeter and Oscilloscope.

E22. CHECK SGL (SINGLE) TRIGGER MODE

a. Push RESET/HOLD to hold the RTD 710A.

b. Set CH1 COUPLING to GND and TRIGGER MODE to SGL.

c. Push RESET/HOLD for RESET.

d. **CHECK** that the ARM'D LED is illuminated and TRIG'D LED is extinguished.

e. Push MAN TRIG.

f. **CHECK** that the TRIG'D LED is illuminated, a single acquisition has occurred, and the HOLD LED is fully illuminated (not blinking).

F. ENVELOPE

Equipment Required:

Oscilloscope	X10 Probe (2)
Sine Wave Generator	50 ohm Cable
Service Kit	50 ohm Termination

F1. ADJUST STRIG (A30)

a. Turn the front-panel power switch to STANDBY and the rear-panel PRINCIPAL POWER SWITCH to OFF.

b. Remove the Envelope Board (A30), install the Extender (670-9888-00) from the Service Kit, and reinstall the Envelope Board on the Extender.

c. Turn the rear-panel PRINCIPAL POWER SWITCH and front-panel power switch to ON.

d. Push the INIT key twice to initialize RTD 710A, then set the controls as follows:

RECORD LENGTH:	1024
SAMPLE INTERVAL:	60 ns
DISPLAY LOCATION:	0 (CH1 and CH2)

e. Connect the Oscilloscope CH1 through a X10 Probe to TP104 and its associated ground on A30, then connect the Oscilloscope CH2 through a X10 Probe to TP112 and its associated ground on A30.

f. Set the Oscilloscope as follows:

Volts/div:	500 mV
Time/div:	2 ns
Trigger:	Norm, CH1

g. Set RESET/HOLD KEY to RESET (Acquisition).

h. Move the J106 jumper on A30 to a position that obtains a T_s of 3.5 ns ±1.5 ns on the Oscilloscope display as shown in Figure 4-11.

i. Turn the front-panel power switch to STANDBY and the rear-panel PRINCIPAL POWER SWITCH to OFF.

j. Remove the Envelope Board (A30) from the Extender, remove the Extender, and reinstall the Envelope Board on the instrument.

k. Turn the rear-panel PRINCIPAL POWER SWITCH and front-panel power switch to ON.

l. Disconnect the Oscilloscope.

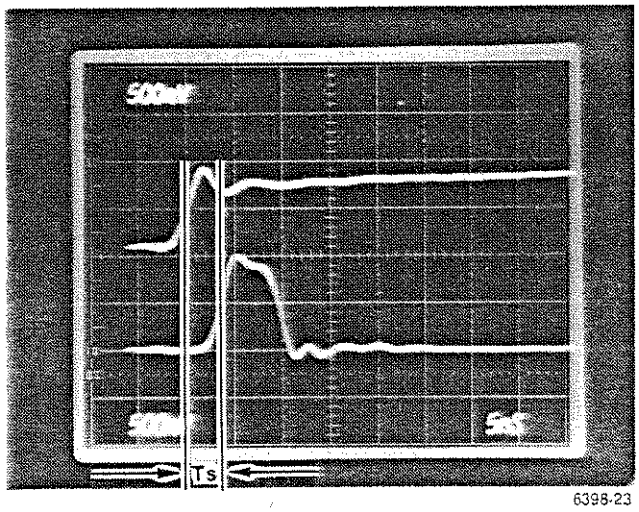


Fig. 4-11 Oscilloscope display for STRIG adjustment

G. TIME BASE

Equipment Required

Ocilloscope	10X Probe
Frequency Counter	Alignment Tool
Service Kit	

G1. CHECK ARM DELAY SOURCE CLOCK AND 200 MHz CLOCK (A32)

a. Turn the front-panel power switch to STANDBY and the rear-panel PRINCIPAL POWER SWITCH to OFF.

b. Remove the Time Base Board (A32), install the Extender (670-9888-00) from the Service Kit, and reinstall the Time Base Board on the Extender.

c. Turn the rear-panel PRINCIPAL POWER SWITCH and front-panel power switch to ON.

d. Push INIT twice to initialize the RTD 710A.

e. Connect the Frequency Counter through a X10 Probe to TP120 and a chassis ground on A32. Set the counter as follows:

TERM:	1 MΩ
COUPL:	AC
TRIG MODE:	AUTO
RESOLUTION:	10 Hz

f. **CHECK** that the frequency is 10 kHz ±500 Hz (9.500 KHz - 10.500 KHz).

g. Move the Frequency Counter X10 Probe to TP400 and its associated ground on A32.

h. **CHECK** that the frequency at TP400 is 200 MHz ±1 kHz.

i. Move P400 shorting strap to DIV position.

j. **CHECK** that the frequency at TP400 varies as the sample interval is changed and the frequency of the sample interval selected is changed.

k. Replace the P400 strap to DIRECT position.

l. Disconnect the Frequency Counter.

m. Turn the front-panel power switch to STANDBY and the rear-panel power switch to OFF.

n. Remove the Time Base Board from the Extender, remove the Extender, and reinstall the Time Base Board.

o. Turn the rear-panel PRINCIPAL POWER SWITCH and front-panel power switch to ON.

G2. ADJUST PHASE CALIBRATION (A32)

NOTE

This adjustment should not be made without first adjusting the Input Amplifiers and A/D Converters.

a. Verify that J122 and J124 on A32 are jumpered between pins 1-2.

b. Enter diagnostic mode by simultaneously pressing the MEASURE function keys V or ΔV and 1/T or 1/ΔT.

c. Set diagnostic to 70101.

d. Push BREAK POINT SET to start the diagnostic routine.

e. Select the position of S450 on A32 that minimizes the position difference between the top and bottom portions of the displayed waveform. Figure 4-12 shows a good and bad waveform.

NOTE

The monitor brightness may need to be increased to see the waveform patterns.

f. Push BREAK POINT CLR to stop the diagnostic routine.

g. Push RECALL/LOC to return to normal operation.

h. Set SAMPLE MODE to HI SPD.

i. Press AUTO CAL key.

j. **CHECK** that AUTO CAL passes without error (Error code E-350 occurs if it doesn't pass).

G3. CHECK BREAKPOINTS

a. Push the INIT key twice to initialize the RTD 710A, then set CH1 RANGE to 800 mV.

b. Set breakpoints and Sample Intervals as shown in Table 4-15.

Table 4-15
BREAK POINT SETTINGS

Break Point	Sample Interval
0	10 ns
16	100 ns
24	10 ns

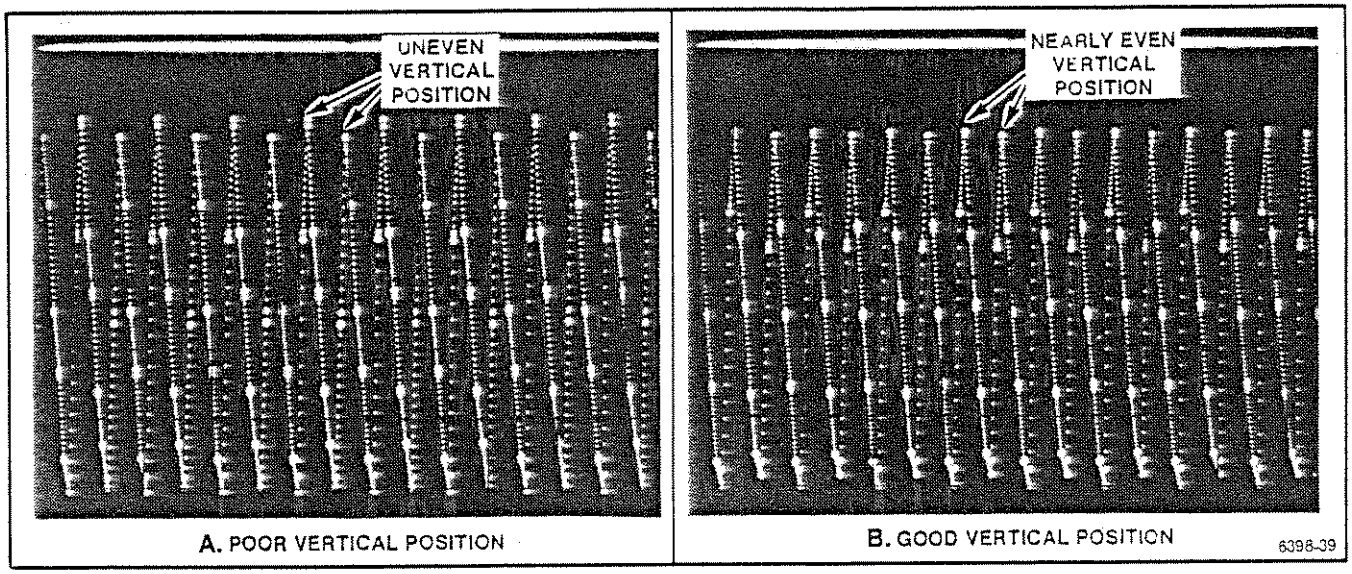


Fig. 4-12 Waveform for Phase calibration adjustment

c. Connect the Sine Wave Generator through a 50 ohm cable and 50 ohm termination to CH1 and set the generator for a 600 kHz, 1 Vp-p Monitor display.

d. Set RESET/HOLD key to RESET (Acquisition).

e. Set CURSOR1 and move it to the trigger point onthe Monitor display.

f. Set HORIZ ZOOM to 16.

g. Select CURSOR2 and move it to the first breakpoint on the Monitor display.

h. **CHECK** that the control display reads –16 and that the sample interval has not changed from 10 ns to 100 ns at the 16th sample point (not counting the trigger point).

i. Move CURSOR2 to the second breakpoint on the Monitor display.

j. **CHECK** that the CONTROL display reads –24 and that the sample interval has changed from 100 ns to 10 ns at the 24th sample point.

k. Push the INIT key twice to initialize the RTD 710A, then set the controls as follows:

CH1 RANGE:	500 mV
SAMPLE MODE:	HI SPD

l. Set breakpoints and Sample Intervals as shown in Table 4-16.

Table 4-16
BREAK POINT SETTINGS

Break Point	Sample Interval
0	5 ns
32	100 ns
48	5 ns

m. Set the Sine Wave Generator to 400 kHz.

n. Set RESET/HOLD key to RESET (Acquisition).

o. Select CURSOR1 and move it to the trigger point on the Monitor display.

p. Set HORIZ ZOOM to 16.

q. Select CURSOR2 and move it to the first breakpoint on the Monitor display.

r. **CHECK** that the CONTROL display reads –32 and the sample interval has changed from 5 ns to 100 ns at the 32nd sample point (excluding the trigger point).

s. Move CURSOR2 to the second break point on the Monitor display.

t. **CHECK** that the CONTROL display reads –48 and that the sample interval has changed from 100 ns to 5 ns at the 48th sample point.

u. Disconnect the Sine Wave Generator.

H. MPU

Equipment Required:

Frequency Counter

10X Probe

H1. CHECK MPU CLOCK (A50)

a. Push INIT twice to initialize the RTD 710A.

b. Connect the Frequency Counter through a X10 Probe to TP170 and ground on A50 and set it for 100 Hz resolution.

c. **CHECK** that the frequency is 8 MHz ±800 Hz (7.9992 MHz - 8.0008 MHz).

d. Disconnect the Frequency Counter.

I. DMA

Equipment Required:

Frequency Counter	10X Probe

I1. CHECK GPIB CLOCK (A52)

a. Push INIT twice to initialize the RTD 710A.

b. Connect the Frequency Counter through a X10 Probe to TP380 and ground on A52 and set the counter for 100 Hz resolution.

c. **CHECK** that the frequency is 5 MHz ±500 Hz (4.9995 MHz - 5.0005 MHz).

d. Disconnect the Frequency Counter.

I2. CHECK ROTARY ENDCODER CLICK (A52)

a. **CHECK** that there is a clicking sound when the Parameter Entry Knob is rotated in either direction.

b. Remove the jumper J250 on A52.

c. **CHECK** that there is no clicking sound when the Parameter Entry Knob is rotated in either direction.

d. Replace the jumper J250 on A52.

I3. CHECK NON-VOLATILE MEMORY (NVM) (A52)

a. Push INIT twice to initialize the RTD 710A.

b. **CHECK** that the default values in the 7-segment LED indicators are as follows:

INPUT (CH1)	50 V
INPUT (CH2)	50 V
TRIGGER	–400
TIME BASE	10 ns
RECORDING	2048
CONTROL	1

c. Change the values in each of the 7-segment indicators by individually selecting RANGE (CH1 and CH2), TRIG DELAY, SAMPLE INTERVAL, RECORD LENGTH, and DISPLAY LOCATION and setting a new value. Make a note of each value.

d. Cycle the front-panel power switch to STANDBY for a couple of seconds, then back to ON.

e. **CHECK** that the 7-segment indicators returned to the last values which were set for RANGE (CH1 and CH2), TRIG DELAY, SAMPLE INTERVAL, RECORD LENGTH, and DISPLAY LOCATION, which were noted.

J. DISPLAY CONTROL

Equipment Required:

Oscilloscope	10X Probe
Alignment Tool	

J1. ADJUST BETWEEN BLANKING (A54)

a. Push INIT twice to initialize the RTD 710A.

b. Set RESET/HOLD key to HOLD (Hold).

c. Connect the Oscilloscope through a X10 Probe to TP370 and ground on A54 and set the oscilloscope as follows:

Volts/div:	1 V/div
Time/div:	0.5 µs/div
Trigger Slope:	–

d. Adjust R372 for a negative pulse width of 1 µs ±0.05 µs (2 div ±0.1 div) as shown in Figure 4-13

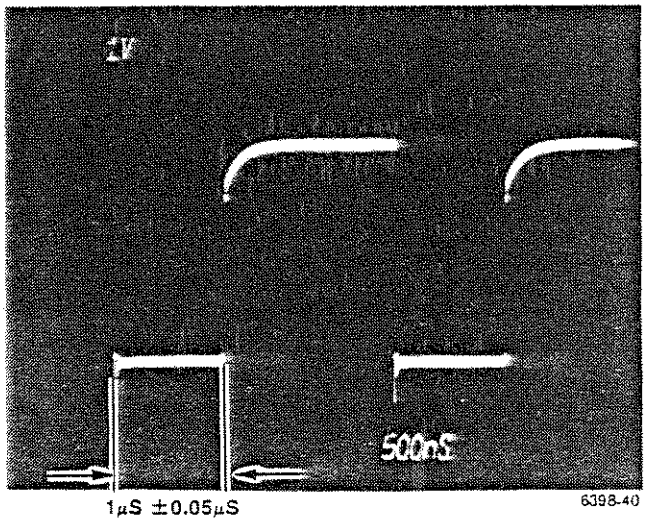


Fig. 4-13 Waveform to adjust between blanking

e. Disconnect the Oscilloscope.

J2. ADJUST RETRACE BLANKING (A54)

a. Connect the Oscilloscope through a X10 Probe to TP330 and ground on A54 and set the Oscilloscope Time/div to 10 µs.

b. **Adjust** R330 for a negative pulse width of 50 µs ±1 µs (5 div ±0.1 div) as shown in Figure 4-14.

c. Disconnect the Oscilloscope.

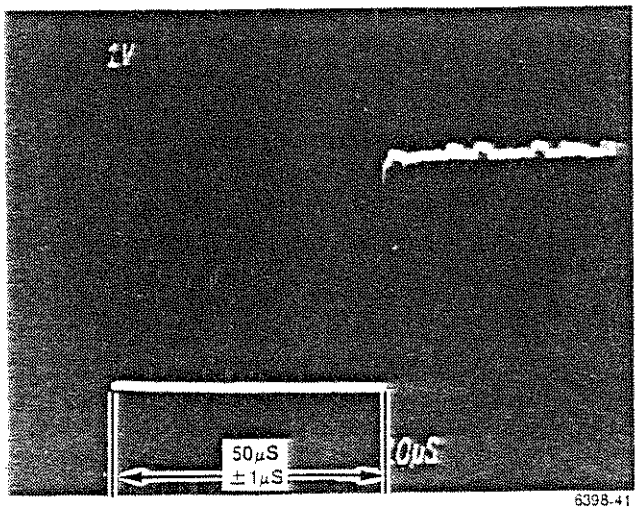


Fig. 4-14 Waveform to adjust retrace blanking

K. GPIB/MONITOR CONTROL

Equipment Required:

Oscilloscope	10X Probe
Monitor	50 ohm Cable
Service Kit	Alignment Tool

K1. ADJUST Y OUTPUT LEVEL (A56)

a. Turn the front-panel power switch to STANDBY and the rear-panel PRINCIPAL POWER SWITCH to OFF.

b. Remove the GPIB/Monitor Board (A56), install the Extender (670-9888-00) from the Service Kit, and reinstall the GPIB/Monitor on the Extender.

c. Turn the rear-panel PRINCIPAL POWER SWITCH and front-panel power switch to ON.

d. Push INIT twice to initialize the RTD 710A.

e. Connect the J430 (Y LEVEL) jumper between pins 1-2 on A56.

f. Connect the Oscilloscope through a X10 Probe to TP430 (YCRT) and its associated ground on A56 and set it as follows:

Volts/div:	1 V
Time/div:	2 ms
Trigger:	Norm, CH1

g. Enter diagnostic mode by simultaneously pressing the MEASURE FUNCTION keys V or ΔV and 1/T or 1/ Δ T.

h. Set diagnostic to 30302.

i. Push BREAK POINT SET to start the diagnostic routine.

j. **ADJUST** YFS, R412 on A56 for a 5 V ±0.1 V (5 divisions ±0.1 division) Oscilloscope display.

k. Move the J430 (Y LEVEL) jumper on A56 to pins 2-3.

l. Set the Oscilloscope to 0.2 V/div.

m. **CHECK** that the Oscilloscope display is 1 V ±0.02 V (5 divisions ±0.1 division).

n. Disconnect the Oscilloscope.

K2. ADJUST X OUTPUT LEVEL (A56)

a. Connect the J470 (X LEVEL) jumper on A56 between pins 1-2.

b. Connect the Oscilloscope Probe to TP470 (XCRT) and its associated ground on A56 and set the Oscilloscope Volts/div for 1 V.

c. **ADJUST** XFS, R420 on A56 for a 5V ±0.1 V (5 divisions ±0.1 division) Oscilloscope display.

d. Move the J470 (X LEVEL) jumper on A56 to pins 2-3.

e. Set the Oscilloscope Volts/div to 0.2 V.

f. **CHECK** that the Oscilloscope display is 1 V ±0.02 V (5 divisions ±0.1 division).

g. Disconnect the Oscilloscope.

K3. CHECK Z OUTPUT LEVEL AND POLARITY (A56)

a. Connect the J481 (Z LEVEL) jumper on A56 between pins 1-2.

b. Connect the J480 (Z POL) jumper on A56 between pins 2-3 (NEG).

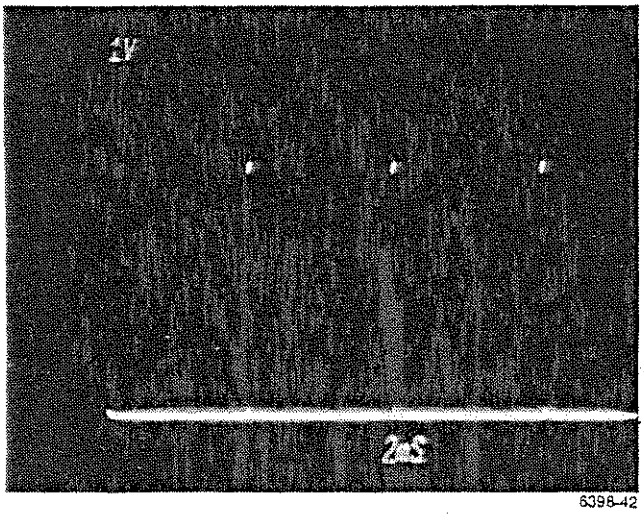


Fig. 4-15 Waveform for negative polarity Z output

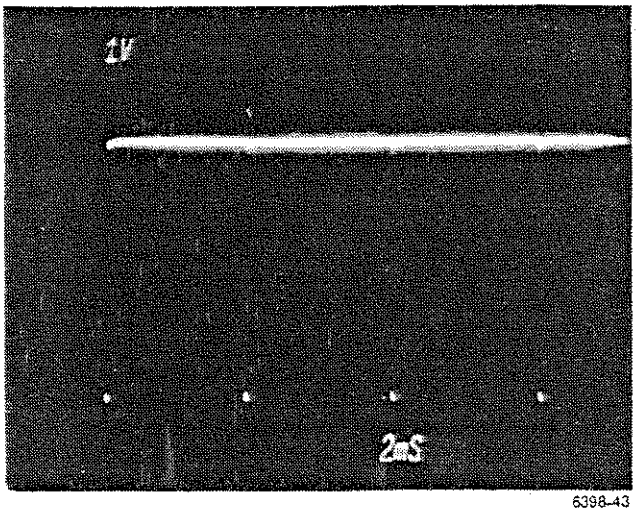


Fig 4-16 Waveform for positive polarity Z output

c. Connect the Oscilloscope Probe to TP480 (ZCRT) on A56.

d. Set the Oscilloscope Volts/div to 1 V.

e. **CHECK** that the Oscilloscope display is 5 Vp-p (+5% –15%) (4.25 –5.25 divisions) and the pulse polarity is similar to Figure 4-15.

f. Move the J481 (Z LEVEL) jumper on A56 between pins 2-3.

g. Set the Oscilloscope Volts/div to 0.2 V.

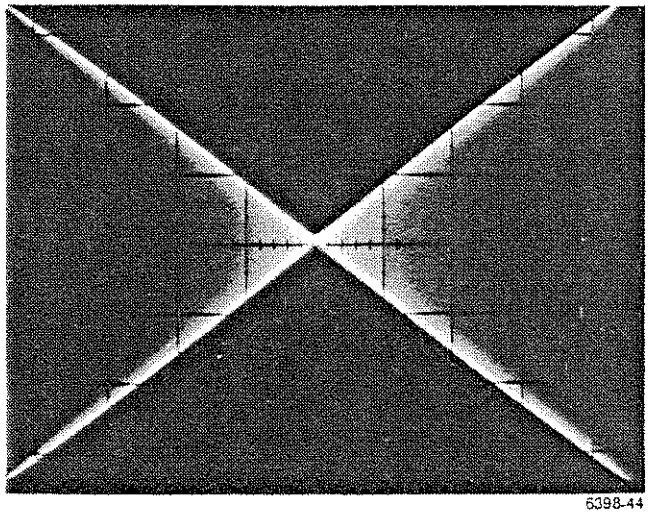
h. **CHECK** that the Oscilloscope display is 1 Vp-p (+5% –15%) (4.25 –5.25 divisions).

i. Move the J480 (ZPOL) jumper (P480) on A56 between pins 1-2 (POS).

j. **CHECK** that the pulse polarity on the Oscilloscope display is similar to Figure 4-16.

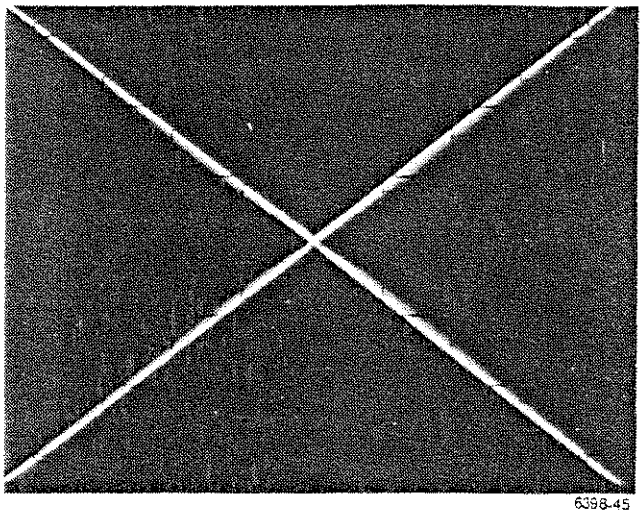
k. Push BREAK POINT CLR to stop the diagnostic routine.

l. Disconnect the Oscilloscope.



6398-44

Fig. 4-17 Line mode display



6398-45

Fig. 4-18 Dot mode display

K4. CHECK DOT/LINE DISPLAY FUNCTION

a. Push BREAK POINT SET to start the diagnostic routine.

b. **CHECK** that the Monitor display looks like Figure 4-17.

c. Push BREAK POINT CLR to stop the diagnostic routine.

d. Set diagnostic to 30301.

e. Push BREAK POINT SET to start the diagnostic routine.

f. **CHECK** that the Monitor display looks like Figure 4-18.

g. Push BREAK POINT CLR to stop the diagnostic routine.

K5. ADJUST Y BANDWIDTH (A56)

a. Set diagnostic to 30302.

b. Push BREAK POINT SET to start the diagnostic routine.

c. **ADJUST** Y BANDWIDTH, C432 on A56 for the maximum width Monitor display.

d. Push BREAK POINT CLR to stop the diagnostic routine.

K6. ADJUST Y GLITCH CANCEL (A56)

a. Disconnect the 50 ohm cable at the Monitor Y INPUT and connect it to the Oscilloscope. Set the Oscilloscope as follows:

Volts/div:	0.2 V/div
Time/div:	2 ms/div
Coupling:	DC

b. Set diagnostic to 30501.

c. Push BREAK POINT SET to start the diagnostic routine.

d. **CHECK** for an Oscilloscope display similar to Figure 4-19A.

e. Set the Oscilloscope as follows:

Volts/div:	5 mV/div
Time/div:	50 µs/div
Coupling:	AC

f. **ADJUST** Y GLITCH CANCEL, C412 on A56 so the two glitches shown in Fig 4-19B are minimized (2 mV or less).

g. Push BREAK POINT CLR to stop the diagnostic routine.

h. Disconnect the 50 ohm cable at the Oscilloscope and reconnect it to the Monitor's Y INPUT connector.

K7. ADJUST X BANDWIDTH (A56)

a. Set diagnostic to 30310.

b. Push BREAK POINT SET to start the diagnostic routine.

c. **ADJUST** X BANDWIDTH, C472 on A56 for the narrowest line width on the Monitor display (Figure 4-20A). The ideal display approaches a narrow diagonal line from top left to bottom right (Figure 4-20B).

d. Push BREAK POINT CLR to stop the diagnostic routine.

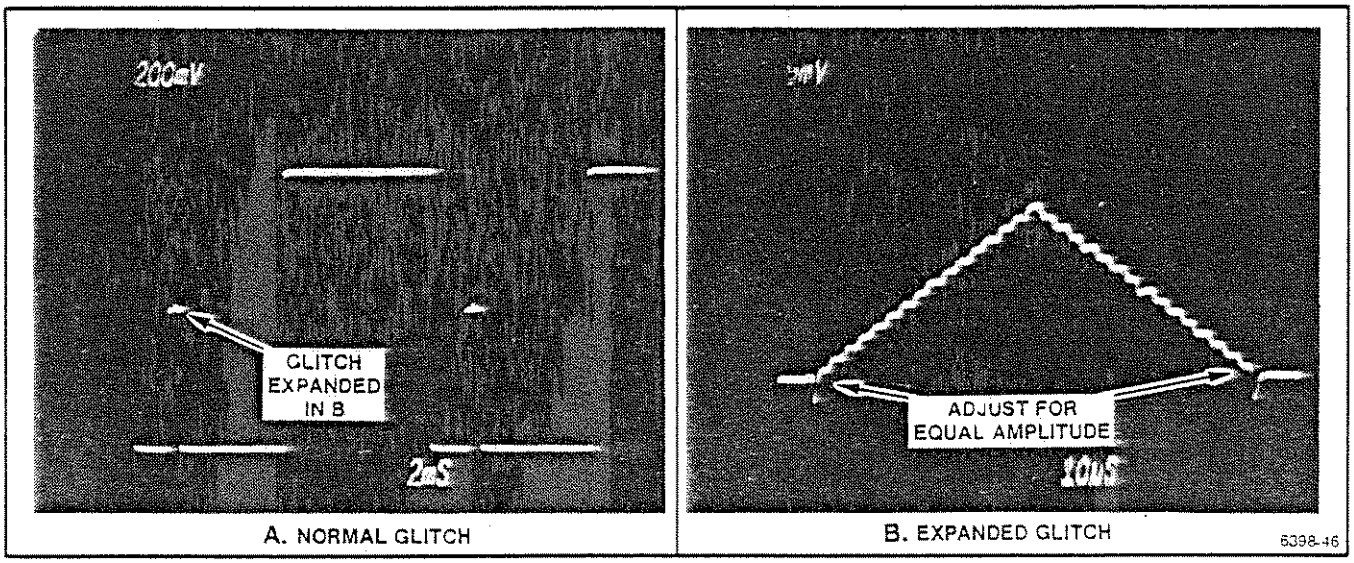


Fig. 4-19 Waveforms to adjust Y Glitch Cancel

K8. CHECK X-Y/Y-T DISPLAY FUNCTION

a. Set diagnostic to 30309.

b. Push BREAK POINT SET to start the diagnostic routine.

c. **CHECK** for the MONITOR display in Figure 4-21.

d. Push BREAK POINT CLR to stop the diagnostics routine.

e. Set diagnostic to 30301.

f. Push BREAK POINT SET to start the diagnostic routine.

g. **CHECK** for the Monitor display shown in Figure 4-22.

h. Push BREAK POINT CLR to stop the diagnostic routine.

i. Push RECALL/LOC to return to normal operation.

K9. ADJUST TRIGGER POINT INTENSITY (A56)

a. Push INIT twice to initialize RTD 710A, then set CH1 OFFSET TO 10%.

b. Set RESET/HOLD key to RESET (Acquisition).

c. **CHECK** for a trigger point (first intensified dot) on the Monitor display (Figure 4-23).

d. Set RESET/HOLD key to HOLD.

e. Connect the Oscilloscope through a X10 Probe to U150-12 and ground on A56 and set it as follows:

Volts/div	1 V
Time/div:	50 µs
Coupling:	DC
Trigger Slope:	–

f. **ADJUST** TP, R155 on A56 for a negative pulse width of 4 divisions ±0.1 divisions on the Oscilloscope display (Figure 4-24).

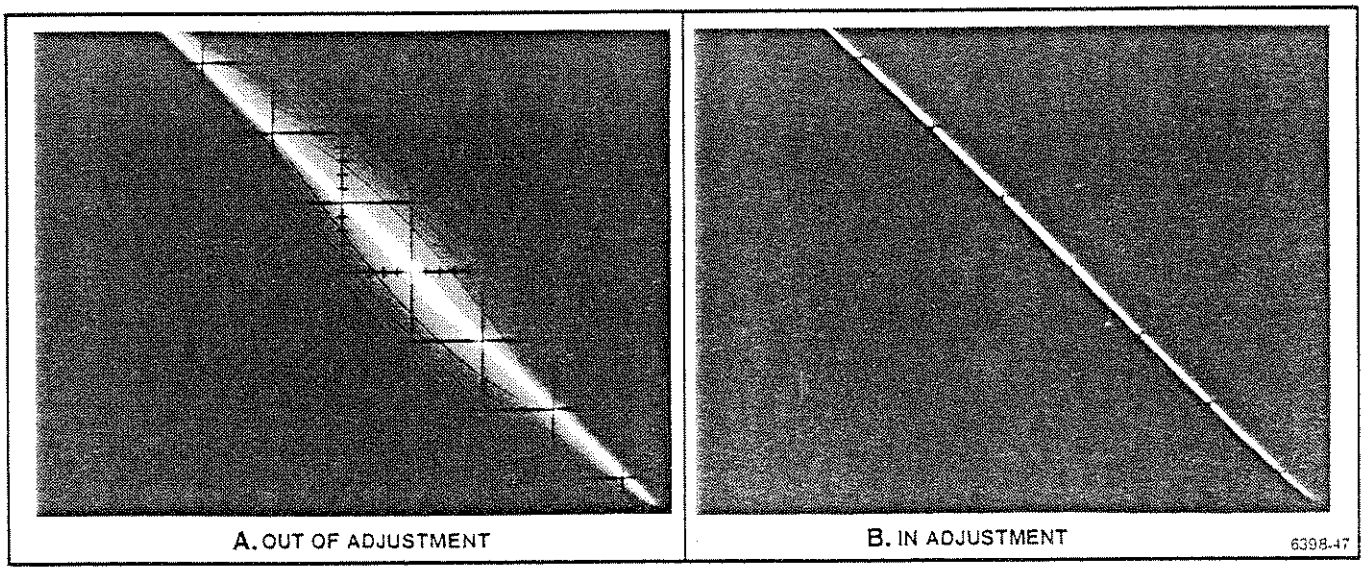


Fig. 4-20 Waveforms to adjust X BANDWIDTH

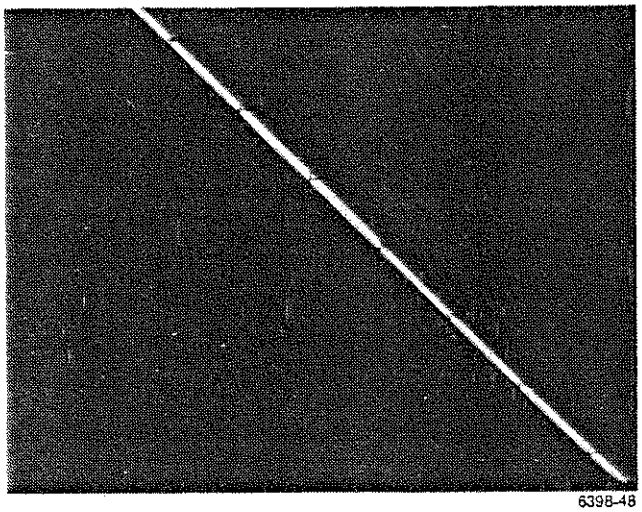


Fig. 4-21 X-Y waveform

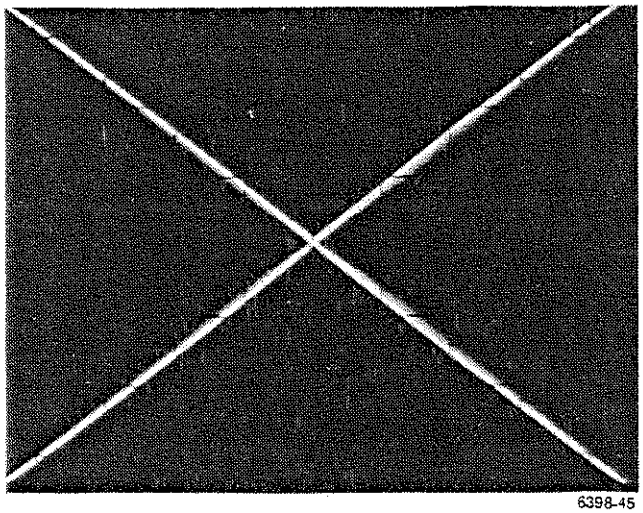


Fig. 4-22 Y-T waveform

g. Disconnect the Oscilloscope.

K10. CHECK/ADJUST CURSOR SELECTION AND INTENSITY (A56).

a. Select CURSOR1.

b. **CHECK** for CURSOR1 (intensified dot other than trigger point) on the Monitor display (Figure 4-25).

c. Connect the Oscilloscope through a X10 Probe to U150-4 and ground on A56 and set it as follows:

Volts/div:	1 V
Time/div:	100 µs

d. **ADJUST** CURSOR1, R152 on A56 for a negative pulse width of 5 divisions ±0.1 divisions on the Oscilloscope display.

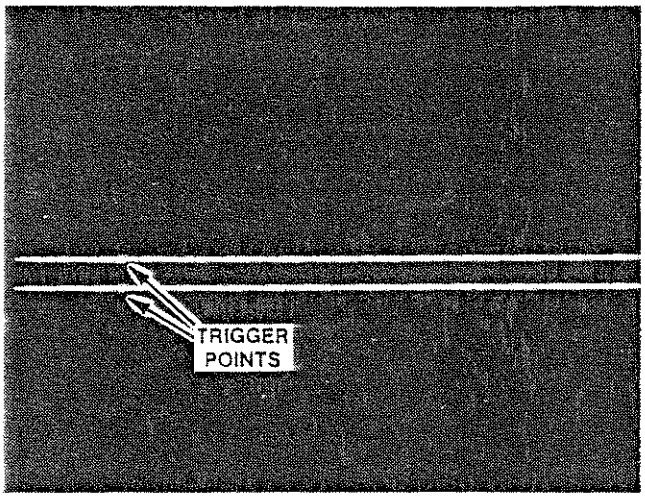
e. **CHECK** that the CURSOR1 and trigger point intensity are about equal.

f. Move the J400 (HAIR) jumper on A56 to pins 2-3.

g. **CHECK** that CURSOR1 on the Monitor display disappears.

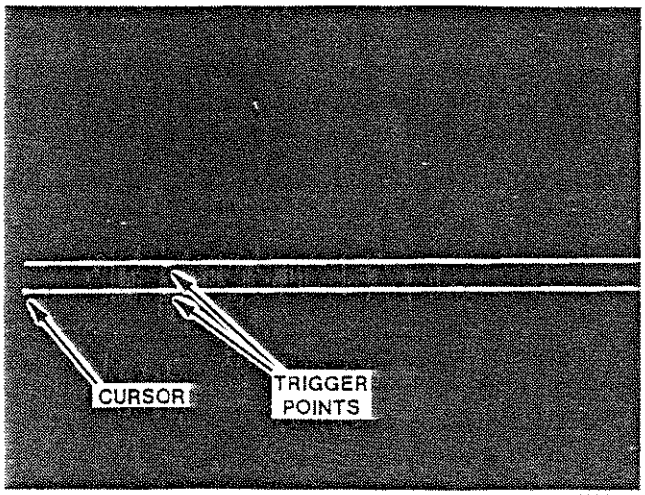
h. Return the J400 (HAIR) jumper on A56 to pins 1-2.

i. Turn the front-panel power switch to STANDBY and the rear-panel PRINCIPAL POWER SWITCH to OFF.



6398-49

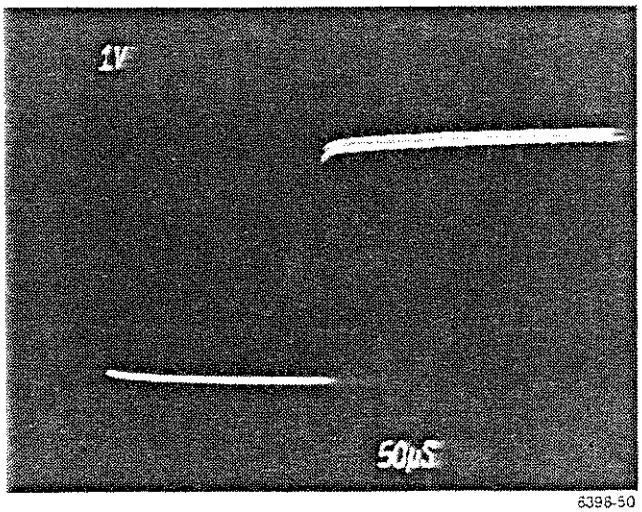
Fig 4-23 Trigger point display



6398-51

Fig. 4-25 Cursor display

j. Remove the GPIB/MONITOR BOARD from the Extender, remove the Extender, and reinstall the GPIB/MONITOR BOARD.



6398-50

Fig 4-24 Display to adjust trigger point intensity

k. Turn the rear-panel PRINCIPAL POWER SWITCH and front-panel power switch to ON.

L. PANEL CONTROL

Equipment Required:

Sine Wave Generator	50 ohm Cable
50 ohm Termination	Dual Input Coupler

L1. CHECK FRONT PANEL LEDS (A60)

a. Enter diagnostic mode by simultaneously pressing the MEASURE function keys V or ΔV and 1/T or 1/ Δ T.

b. Set diagnostic to 50200.

c. Push VERT ZOOM to select the looping diagnostic mode.

d. Push BREAK POINT SET to start the diagnostic routine.

e. **CHECK** that all LED's illuminate, except the overrange arrow LED's, 7-Segment LED's, and ARM'D/TRIG'D LED's.

f. Push BREAK POINT CLR until the diagnostic routine stops.

g. Set diagnostic to 50400.

h. Push BREAK POINT SET to start the diagnostic routine.

i. **CHECK** that all 7-Segment LED indicators are illumninated (displaying "8." in each segment).

j. Push BREAK POINT CLR to stop the diagnostic routine.

k. Push RECALL/LOC to return to normal operation.

l. Push INIT twice to initialize the RTD 710A, then set CH1 and CH2 RANGE to 800 mV.

m. Connect the Sine Wave Generator through a 50 ohm cable, 50 ohm termination, and Dual Input Coupler to CH1 and CH2. Set the generator for a 50 kHz, 2 Vp-p Monitor display.

n. Set RESET/HOLD key to RESET.

o. **CHECK** that the ARM'D/TRIG'D LEDS and CH1/CH2 overrange arrow LED's are illumninated.

p. Disconnect the Sine Wave Generator.

M. I/O

Equipment Required:

None

M1. CHECK GPIB ADDRESS (A74)

a. Set the rear panel GPIB Address Switch to 31.

b. Push the RQS ID key.

c. **CHECK** that the CONTROL Indicator displays 31.

d. Return the rear panel GPIB Address Switch to 1.

N. BLANK FRONT PANEL INDICATORS (Option 19 Only)

Equipment Required:

Sine Wave Generator	50 ohm Cable
50 ohm Termination	Dual Input Coupler

N1. CHECK LED OPERATION (A64)

a. Turn on the rear-panel PRINCIPAL POWER SWITCH and front-panel power switch.

b. **CHECK** that the power ON LED is illuminated.

c. **CHECK** that the SRQ LED illuminates after the power-up self test is completed.

O. TV TRIGGER (Option 05 Only)

Equipment Required:

Function Generator	50 ohm Cable
NTSC TV Generator	75 ohm Termination
T-Connector	Dual Input Coupler
50 ohm to 75 ohm Attenuator	75 ohm Termination

O1. CHECK LINE TRIGGER (A24)

a. Push INIT twice to initialize the RTD 710A, then reset these controls:

CH1 RANGE:	1.0 V
SAMPLE INTERVAL:	100 ns
TRIGGER:	
COUPLING:	LINES
SLOPE	–

b. Connect the TV Generator through a 75 ohm cable and 75 ohm termination to CH1. Set the generator for a normal full field NTSC composite video output.

c. **CHECK** that the trigger point (first intensified dot) on the Monitor display is in the front porch on the TV Line Sync (Figure 4-26).

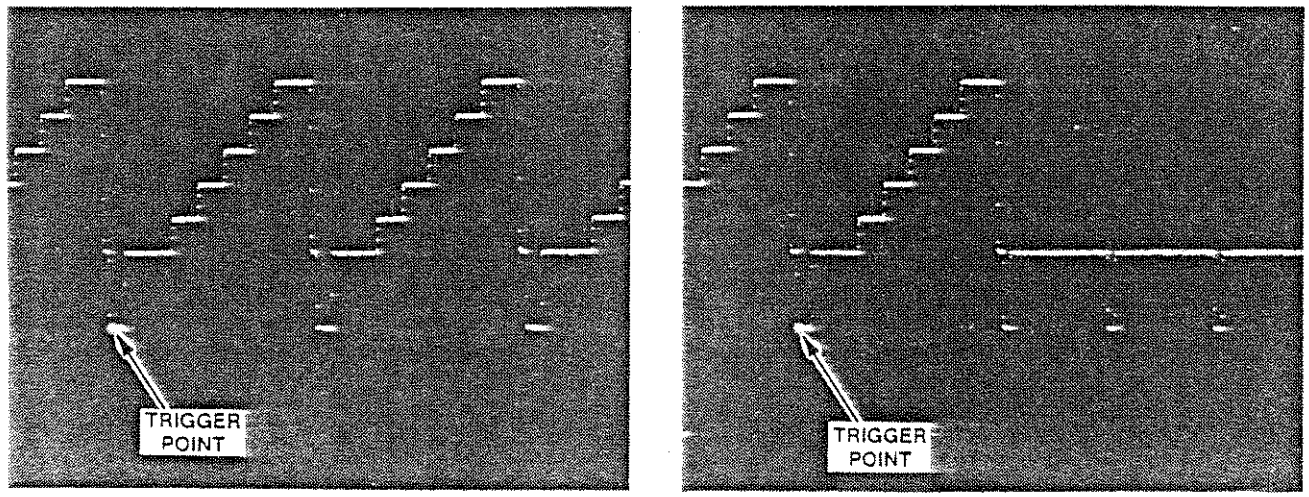


Fig. 4-26 Trigger point displays for TV trigger check

O2. CHECK TRIGGER SENSITIVITY (A24)

a. Set CH1 RANGE to 0.1 V, then 10 V and **CHECK** that the Monitor display remains triggered and stable at both RANGE settings.

b. Set CH1 RANGE to 1V.

O3. CHECK TRIGGER SLOPE

a. Set TRIGGER SLOPE to +.

b. **CHECK** that the Monitor display is unstable.

c. Set TRIGGER SLOPE to –.

O4. CHECK INPUT SELECTOR

a. Set TRIGGER SOURCE to EXT.

b. **CHECK** that the monitor display is unstable.

c. Connect the COMP SYNC or COMP VIDEO output from the TV Generator through a 75 ohm cable, 75 ohm termination, and Dual Input Coupler to CH1 and EXT TRIG IN.

d. **CHECK** that the Monitor display is triggered and stable.

e. Remove the Dual Input Coupler and reconnect TV generator through a 75 ohm cable and 75 ohm terminator to CH1.

f. Set TRIG SOURCE to INT.

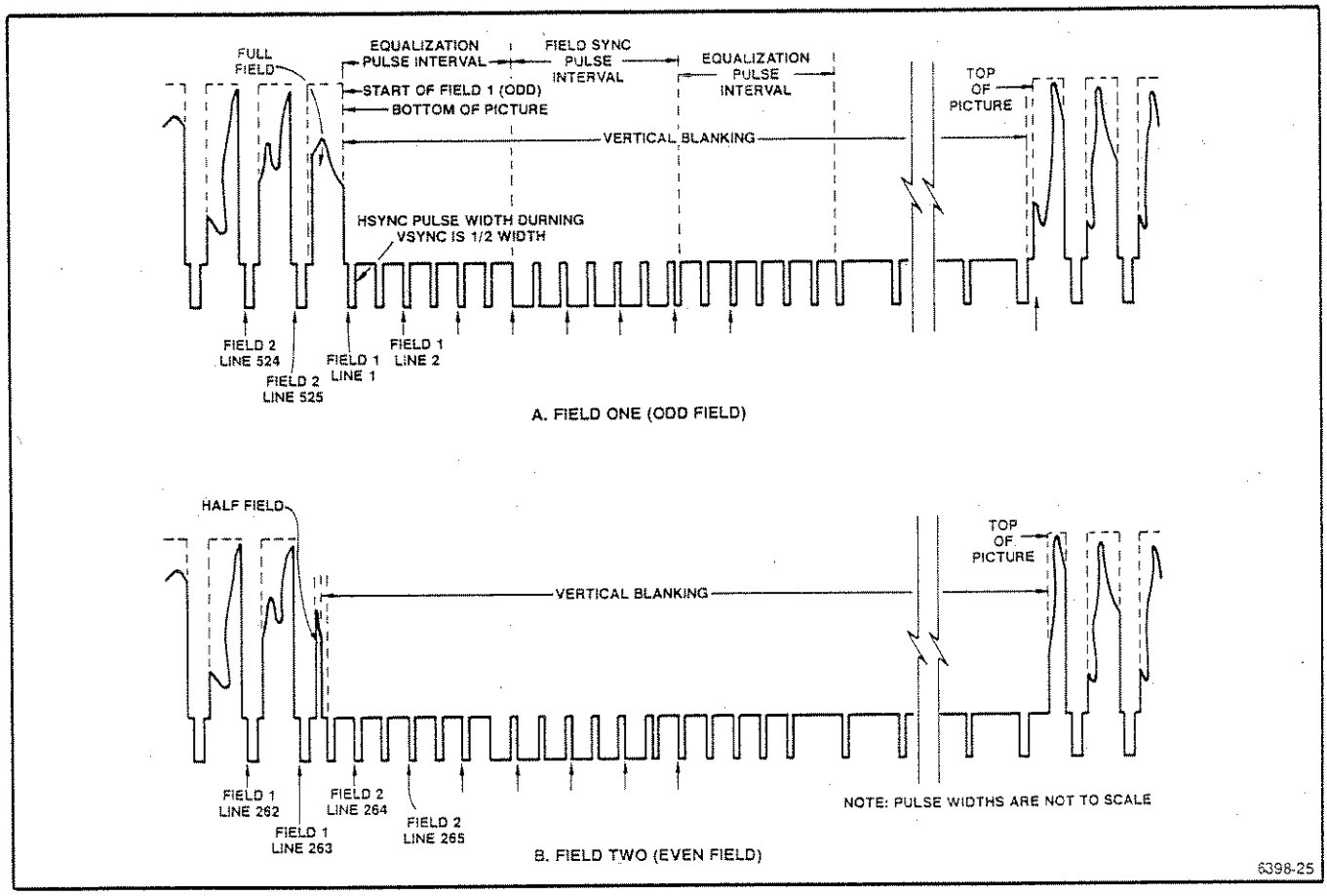
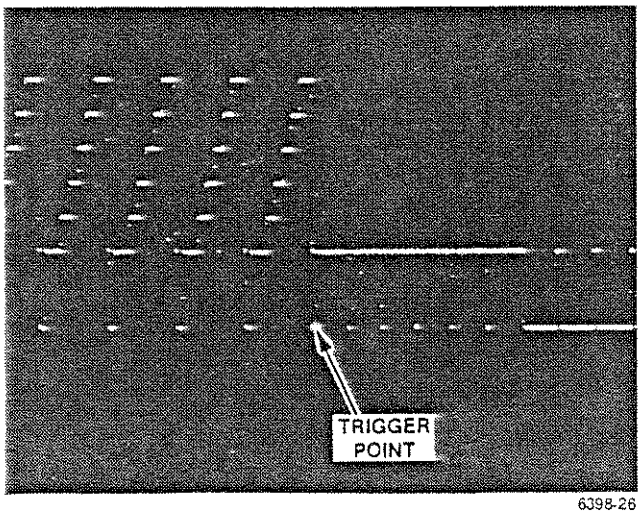
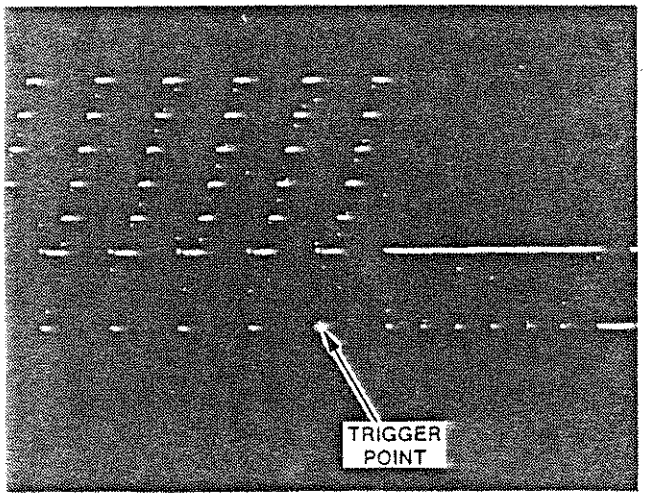


Fig. 4-27 Field 1 and Field 2 TV triggers



6398-26

Fig. 4-28 TV field 1, line 1 display



6398-27

Fig. 4-29 TV field 1, line 525 display

O5. CHECK FIELD TRIGGER (A24)

When checking TV field triggers for Field 1 and Field 2, they are recognized as shown in Figure 4-27.

a. Set the RTD 710A as follows:

TRIGGER COUPLING:	FLD1
TRIG DISPLAY:	–1000
SAMPLE INTERVAL:	300 ns

b. **CHECK** that the Monitor display is triggered and indicates the correct line signal (Field 1, Line 1) as shown in Figure 4-28.

c. Select FIELD LINE # (TRIG LEVEL 2) and set it to 525.

d. **CHECK** that the Monitor display is triggered and indicates the correct line signal (Field 1, Line 525) as shown in Figure 4-29.

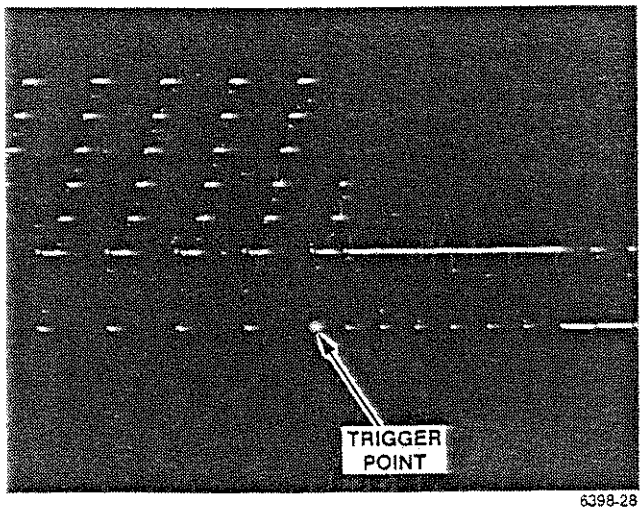


Fig. 4-30 TV field 2, line 525 display

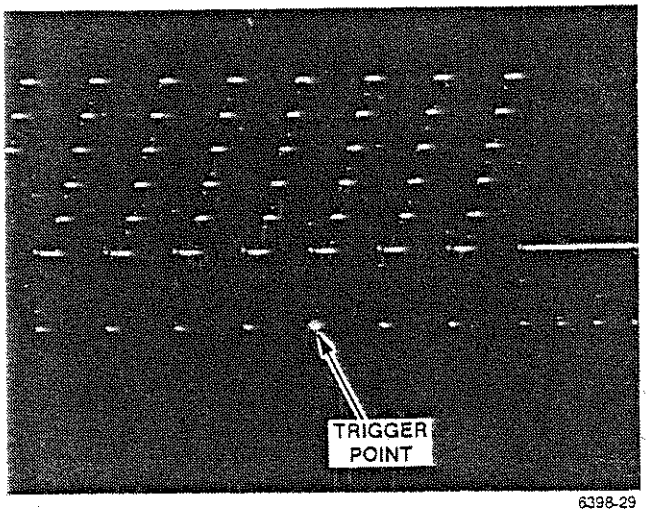


Fig. 4-31 TV PAL system trigger display

e. Set Trigger COUPLING to FLD2.

f. **CHECK** that the Monitor display is triggered and indicates the correct line (Field 2, Line 525) as shown in Figure 4-30.

NOTE

Following is the line number relationship between FLD1 and FLD2:

FIELD1	FIELD2	FIELD1	FIELD2
1	263	264	1
2	264	265	2
3	265	266	3

O6. CHECK PAL AND PAL-M TV SYSTEMS (A24)

a. Set Trigger COUPLING to FIELD1 and FIELD LINE # (TRIG LEVEL 2) to 523 as shown in Figure 4-31.

b. Push FIELD LINE # again and **CHECK** that the TRIGGER display LED's indicate a – sign.

c. **CHECK** that the trigger point shifts 3 lines to the left on the Monitor display (Figure 4-32).

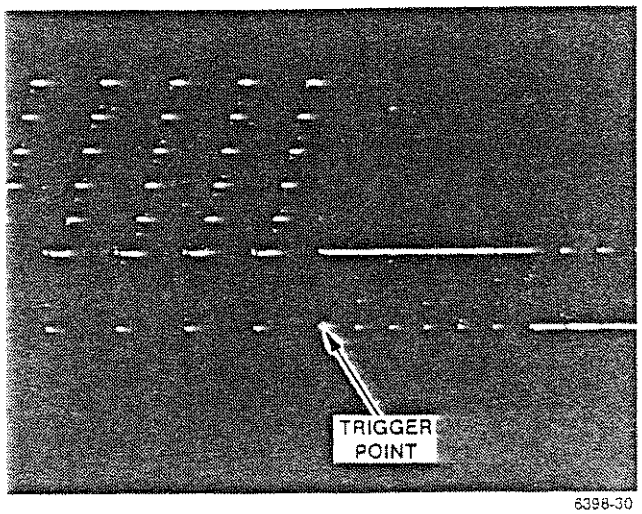
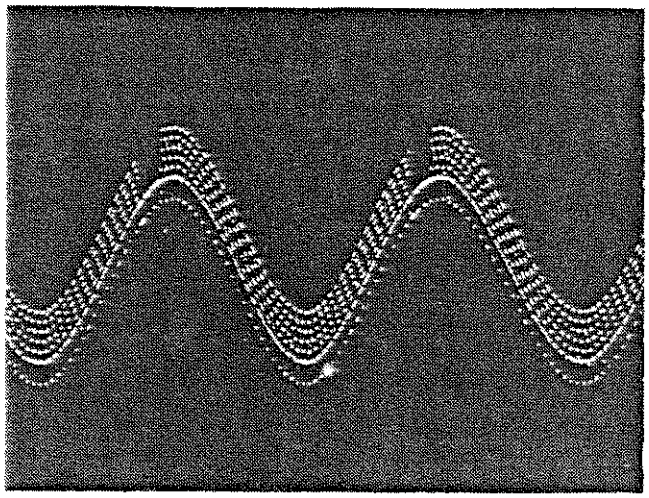
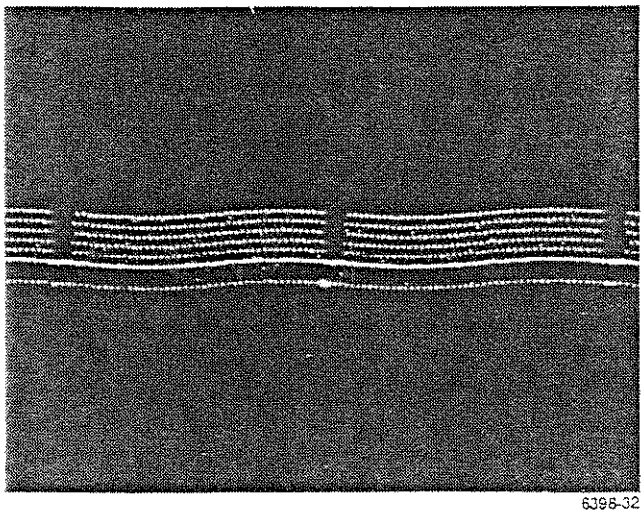


Fig. 4-32 TV PAL-M system trigger display



6398-31

Fig. 4-33 50 Hz signal for TV Clamp check



6398-32

Fig. 4-34 TV Clamp check display

O7. CHECK TV CLAMP (A24)

a. Set CH1 COUPLING to TV CLAMP and SAMPLE INTERVAL to 20 µs.

b. **CHECK** that the Back Porch Level of the Video signal is clamped to within 20% of full scale (approximately 1.6 divisions = 20% of full scale).

c. Install a T-Connector between the 75 ohm cable and 75 ohm termination.

d. Set CH1 COUPLING to AC.

e. Connect the Function Generator through a 50 ohm cable and 50-to-75 ohm Minimum Loss Attenuator to the T-Connector. Set the generator for a 60 Hz, 1 VP-p, sine wave output. Note the amplitude of the 60 Hz signal on the Monitor display (Figure 4-33).

f. Set CH1 COUPLING to TV CLAMP.

g. **CHECK** that the Monitor display amplitude of the 60 Hz signal is less than 1/10 of the noted value in step e. (Figure 4-34).

P. POST CAL OPERATIONAL CHECK

Equipment Required:

Sine Wave Generator	50 ohm Cable
Function Generator	50 ohm Termination
Dual Input Coupler	T-Connector

P1. CHECK PROBE SENSE

a. Push INIT twice to initialize the RTD 710A.

b. Short between the BNC connector and coding ring on each of the CH1 and CH2 inputs.

c. **CHECK** that INPUT Indicator reads 500 V.

P2. CHECK AVERAGE MODE

a. Set the RTD 710A as follows:

CH1/CH2 RANGE:	500 mV
CH1/CH2 COUPLING:	DC
SAMPLE INTERVAL:	100 ns

b. Install a T-Connector on CH1.

c. Connect the Sine Wave Generator through a 50 ohm cable to one side of the T-Connector on CH1. Set the generator for a 1 MHz, 0.4-division sine wave on the Monitor.

d. Connect the Function Generator through a 50 ohm cable to the other side of the T-Connector on CH1. Set the generator for a 10 kHz, 4-division square wave on the Monitor display.

e. Set RESET/HOLD key to RESET (Acquisition).

f. **CHECK** that the Monitor display is a mixed waveform similar to Figure 4-35.

g. Set RESET/HOLD key to HOLD.

h. Set RECORD MOVE key to AVE.

i. Select AVE/ENV # OF TIMES and **CHECK** that it can be set from 2 - 16384 in 2^n steps.

j. Set AVE/ENV # OF TIMES to 32 and TRIG MODE to SGL.

k. Set RESET/HOLD key to RESET (Acquisition).

l. **CHECK** that the Monitor display is an averaged wave form similar to Figure 4-36.

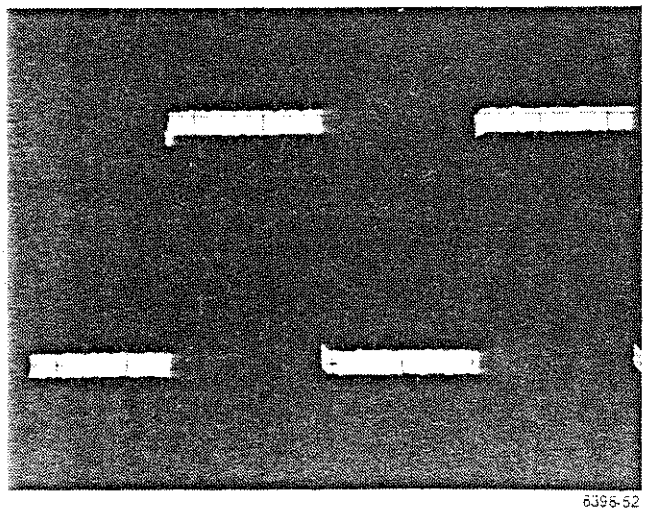
m. Move the T-Connector to CH2.

n. Set the RTD 710A as follows:

TRIGGER SOURCE:	CH2
RECORD MODE:	NORM
TRIG MODE:	AUTO

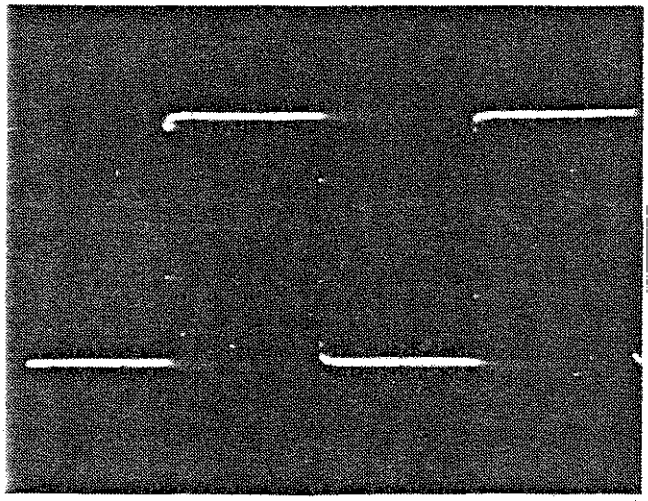
o. Repeat steps e through l.

p. Disconnect the test equipment.



6396-52

Fig. 4-35 Average mode mixed waveform



6398-53

Fig. 4-36 Averaged waveform

P3. CHECK ENVELOPE MODE

a. Push the INIT key twice to initialize the RTD 710A, then set CH1/CH2 RANGE to 500 mV.

b. Connect the Sine Wave Generator through a 50 ohm cable and 50 ohm termination to CH1. Set the generator for a 50 kHz, 4-division, sine wave on the Monitor display.

c. Set the RESET/HOLD key to RESET (Acquisition).

d. Set the RESET/HOLD key to HOLD.

e. Set RECORD MODE to ENV.

f. Select AVE/ENV # OF TIMES and **CHECK** that it can be set from 2 - 16484 in 2^n steps, and to 99999.

g. Set AVE/ENV OF TIMES to 32.

h. Set RESET/HOLD key to RESET (Acquisition).

i. Set CH1 OFFSET to 10%.

j. **CHECK** that a 2-trace envelope waveform is displayed on the Monitor until the display is automatically reset at the end of 32 sweeps.

k. Push RESET/HOLD until the RTD 710A is in HOLD.

l. Move the Sine Wave Generator to CH2.

m. Set TRIGGER SOURCE to CH2 and RECORD MODE to NORM.

n. Repeat steps c through k for CH2, except for CH2 OFFSET to 10% in step i.

o. Move the Sine Wave Generator output to CH1.

P4. CHECK AUTO ADVANCE MODE

a. Push the INIT key twice to initialize the RTD 710A.

b. Set the RTD 710A as follows:

CH1/CH2 RANGE:	500 mV
RECORD LOCATION:	16
TRIGGER MODE:	SGL
RECORD MODE:	ADV

c. Set RESET/HOLD key to RESET (Acquisition).

d. **CHECK** that the CONTROL Indicator sequences from 1 to 16 in steps of 1, then stops at 16.

e. Select DISPLAY LOCATIONs 1 through 16.

f. **CHECK** that the monitor display is the same at all 16 DISPLAY LOCATIONs.

g. Set the RTD 710A as follows:

DISPLAY:	CH2
TRIGGER SOURCE:	CH2

h. Move the Sine Wave Generator output to CH2.

i. Repeat steps c through f for CH2.

P5. CHECK TRIG DELAY

a. Move the Sine Wave Generator to CH1.

b. Push INIT twice to initialize the RTD 710A, then set CH1 RANGE to 500 mV.

c. Select TRIG DELAY and set it to its largest – (minus) value. **CHECK** that the value is –2040.

d. Set the delay value to its largest + (plus) value. **CHECK** that the value is 262136.

e. Push INIT, then TRIG DELAY to reset the value to –400.

f. Set RESET/HOLD key to RESET (Acquisition).

g. Push CURSOR1 and **CHECK** that it position is –400.

h. Move CURSOR1 to the trigger point (HORIZ ZOOM may need to be used to set the cursor directly on the trigger point), and **CHECK** that its position is 0 and that the trigger point is located at the TRIG DELAY value selected.

i. Disconnect the Sine Wave Generator.

P6. CHECK ARM DELAY

a. Push INIT twice to initialize the RTD 710A.

b. Select ARM DELAY and **CHECK** that it can be set from 0s to 10s in a 1-2-5 sequence (0s, 10ms, 20ms, etc.).

c. Push ARM DELAY key again and **CHECK** that an "E" is displayed in the TRIGGER Indicator.

P7. CHECK INTERNAL CLOCK SOURCE

a. Push INIT twice to initialize the RTD 710A.

b. Select SAMPLE INTERVAL and **CHECK** that the it can be set from 10 ns to 200 ms in a 1-2-3-4-5-6-7-8-9 sequence (10 ns, 20 ns, 30 ns, etc.).

c. Set SAMPLE MODE to HI SPD.

d. **CHECK** that SAMPLE INTERVAL can be set to 5 ns, then from 10 ns to 200 ms in a 1-2-3-4-5-6-7-8-9 sequence 10 ns, 20 ns, etc.).

P8. CHECK EXTERNAL CLOCK SOURCE

a. Push INIT twice to initialize the RTD 710A, then set CLK SOURCE to EXT.

b. Select SAMPLE INTERVAL and **CHECK** that it can be set from 1E0 (x1) to 2E7 ($X2*10^7$) in a 1-2-3-4-5-6-7-8-9 sequence (1E0, 2E0, 3E0, 4E0, 5E0, 6E0, 7E0, 8E0, 9E0, 1E1, 2E1, ... 2E7).

c. Set SAMPLE MODE to HI SPD.

d. **CHECK** that SAMPLE INTERVAL can be set from 1EO (X1) to 4E7 ($X4*10^7$) in a 1-2-4-6-8 sequence (1E0, 2E0, 4E0, 6E0, 8E0, 1E1, 2E1, ... 4E7).

P9. CHECK ROLL MODE

a. Push INIT twice to initialize the RTD 710A, then set CH1 RANGE to 800 mV.

b. Connect the Function Generator through a 50 ohm cable and 50 ohm termination to CH1. Set the generator for a 10 kHz, 5-division sine wave Monitor display.

c. Set SAMPLE INTERVAL to 100 µs.

d. Set RESET/HOLD key to RESET (Acquisition).

e. **CHECK** that the acquired waveform is completely displayed after the acquisition occurs.

f. Set SAMPLE INTERVAL to 200 µs through 200 ms and **CHECK** that the acquired waveform is displayed in ROLL mode at each interval setting.

NOTE

In ROLL mode the previous data scrolls toward the left of the monitor as each new data point is acquired, in creating a constant flow of data across the CRT screen.

g. Set SAMPLE MODE to HI SPD.

h. Repeat steps c through f.

i. Disconnect the Function Generator.

P10. CHECK RECORD LENGTH

a. Push INIT twice to initialize the RTD 710A.

b. Select RECORD LENGTH and **CHECK** that it can be set from 1024 to 131072 in X2 steps (2048, 4096, 8192, 16384, 32768, 65536, and 131072).

c. Set SAMPLE MODE TO HI SPD.

d. **CHECK** that RECORD LENGTH can be set from 1024 to 262144 in X2 steps (1024, 2048, 4096, 8192, 16384, 32768, 65536, 131072, and 262144).

P11. CHECK BREAK POINT

a. Push INIT twice to initialize the RTD 710A, then set CH1/CH2 RANGE to 500 mV.

b. Connect the Sine Wave Generator through a 50 ohm cable, 50 ohm termination, and Dual Input Coupler to CH1 and CH2. Set the generator for a 50 kHz, 3-division, sine wave Monitor display.

c. Set RESET/HOLD key to HOLD.

d. Starting with BREAK POINT SET, alternately select BREAK POINT SET and SAMPLE INTERVAL and set them as shown in Table 4-17.

Table 4-17
BREAK POINT SET/
SAMPLE INTERVAL SETTINGS

BREAK POINT SET	SAMPLE INTERVAL
0	10 ns
96	100 ns
200	1 µs
296	10 µs
400	100 µs
496	1 ms

f. Select BREAK POINT DISPLAY and verify the SAMPLE INTERVAL at each breakpoint.

g. Set RESET/HOLD key to RESET (Acquisition).

h. Set RESET/HOLD key to HOLD.

i. Set CH1 DISPLAY VERT POSN to 50.

j. Set CH2 DISPLAY VERT POSN to –50.

k. Select CURSOR 1, then move it to each breakpoint and **CHECK** the breakpoint setting. HORIZ ZOOM may need to be used to set the cursor directly on the intensified breakpoint dot.

l. Select BREAK POINT DISPLAY and display the last breakpoint setting in the RECORDING Indicator. Then push BREAK POINT CLR as many times as needed until the RECORDING Indicator reads 0 (this clears the breakpoints).

m. Disconnect the Sine Wave Generator.

P12. CHECK VERT POSITION

a. Push INIT twice to initialize the RTD 710A.

b. Select VERT ZOOM and set it as shown in Table 4-18. Then select VERT POSN and **CHECK** that the available VERT POSN range is as shown.

Table 4-18
VERT ZOOM SETTING vs VERT POSN RANGE

VERT ZOOM SETTING	VERT POSN RANGE
1-4	–2048 to 2047
1-2	–1024 to 1023
1 or greater	–512 to 511

P13. CHECK MEASURE KEYS T or ΔT, 1/T or 1/ΔT, and V or ΔV)

a. Push INIT twice to initialize the RTD 710A, then reset these controls:

CH1/CH2 RANGE:	500 mV
SAMPLE INTERVAL:	20 ns.

b. Connect the Sine Wave Generator through a 50 ohm cable, 50 ohm termination, and Dual Input Coupler to CH1 and CH2. Set the generator for a 50 kHz, 4-division, sine wave Monitor display.

c. Set RESET/HOLD key RESET (Acquisition).

d. Set RESET/HOLD key to HOLD.

e. Select CURSOR1 and move it to the first point where the positive-going waveform crosses the center horizontal graticule line. Then select CURSOR2 and move it to the point where the positive-going waveform next crosses the center horizontal graticule line.

f. **CHECK** that there is approximately 1000 points between the two cursors.

g. Select T or ΔT.

h. **CHECK** that the period between the cursors is approximately 20 μs.

i. Select 1/T or 1/ΔT.

j. **CHECK** that the frequency is approximately 50 kHz.

k. Select CURSOR1 and set it to top of the wave form. Select CURSOR2 and set it to the bottom of the waveform.

l. Select V or ΔV.

m. **CHECK** that the voltage difference is approximately 500 mv.

n. Disconnect the Sine Wave Generator.

P14. CHECK DOT/LINE and YT/XY MODE

a. Push INIT twice to initialize the RTD 710A, then reset these controls:

CH1/CH2 RANGE:	500 mV
SAMPLE INTERVAL:	20 ns

b. Connect the Sine Wave Generator through a 50 ohm cable, 50 ohm termination, and Dual Input Coupler to CH1 and CH2. Set the generator for a 1 MHz, 8-division, sine wave Monitor display.

c. Set RESET/HOLD key to RESET (Acquisition).

d. Set RESET/HOLD key to HOLD.

e. Set HORIZ ZOOM to 16.

f. Select DISPLAY LINE.

g. **CHECK** that the waveform on the Monitor display is a LINE display.

h. Select DISPLAY XY.

i. **CHECK** that the diameter of the ellipse on the Monitor display, measured vertically at the center of the graticule, is 0.7 division or less (<5 degree ellipse).

P15. CHECK BUSY INDICATOR

a. Push INIT twice to initialize the RTD 710A, then set RECORD LENGTH to 131072.

b. Set RESET/HOLD key RESET (Acquisition).

c. Set HORIZ ZOOM to 1/64.

d. Check that the BUSY indicator lights.

P16. CHECK CH1/CH2 CROSSTALK

a. Push INIT twice to initialize the RTD 710A, then set CH1 and CH2 RANGE to 500 mV.

b. Connect the Sine Wave Generator output through a 50 ohm cable and 50 ohm termination to CH1. Set the Generator for a 100 MHz full scale (1Vp-p) monitor display.

c. Set the RTD 710A as follows:

CH1 DISPLAY LOCATION:	0 (erased)
CH2 VERT ZOOM:	32

d. Adjust the Sine Wave Generator frequency for appropriate beat waveform.

e. Push RESET/HOLD to hold the RTD 710A.

f. Read amplitude of the sine wave component from CH2 display discarding the noise component.

g. **CHECK** that the amplitude is less than 15 LSB.

h. Repeat steps d through g with CH2 RANGE changed. Reset the instrument with the RESET/HOLD key.

i. Repeat above steps after exchanging the driven channel and the measured channel.

REPLACEABLE ELECTRICAL PARTS

PARTS ORDERING INFORMATION

Replacement parts are available from or through your local Tektronix, Inc. Field Office or representative.

Changes to Tektronix instruments are sometimes made to accommodate improved components as they become available, and to give you the benefit of the latest circuit improvements developed in our engineering department. It is therefore important, when ordering parts, to include the following information in your order: Part number, instrument type or number, serial number, and modification number if applicable.

If a part you have ordered has been replaced with a new or improved part, your local Tektronix, Inc. Field Office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

LIST OF ASSEMBLIES

A list of assemblies can be found at the beginning of the Electrical Parts List. The assemblies are listed in numerical order. When the complete component number of a part is known, this list will identify the assembly in which the part is located.

CROSS INDEX-MFR. CODE NUMBER TO MANUFACTURER

The Mfr. Code Number to Manufacturer index for the Electrical Parts List is located immediately after this page. The Cross Index provides codes, names and addresses of manufacturers of components listed in the Electrical Parts List.

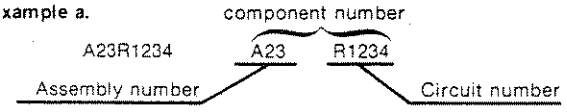
ABBREVIATIONS

Abbreviations conform to American National Standard Y1.1.

COMPONENT NUMBER (column one of the Electrical Parts List)

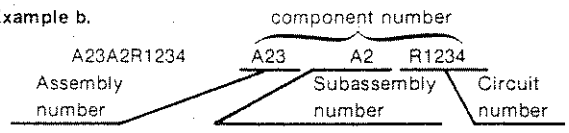
A numbering method has been used to identify assemblies, subassemblies and parts. Examples of this numbering method and typical expansions are illustrated by the following:

Example a.



Read: Resistor 1234 of Assembly 23

Example b.



Read: Resistor 1234 of Subassembly 2 of Assembly 23

Only the circuit number will appear on the diagrams and circuit board illustrations. Each diagram and circuit board illustration is clearly marked with the assembly number. Assembly numbers are also marked on the mechanical exploded views located in the Mechanical Parts List. The component number is obtained by adding the assembly number prefix to the circuit number.

The Electrical Parts List is divided and arranged by assemblies in numerical sequence (e.g., assembly A1 with its subassemblies and parts, precedes assembly A2 with its subassemblies and parts).

Chassis-mounted parts have no assembly number prefix and are located at the end of the Electrical Parts List.

TEKTRONIX PART NO. (column two of the Electrical Parts List)

Indicates part number to be used when ordering replacement part from Tektronix.

SERIAL/MODEL NO. (columns three and four of the Electrical Parts List)

Column three (3) indicates the serial number at which the part was first used. Column four (4) indicates the serial number at which the part was removed. No serial number entered indicates part is good for all serial numbers.

NAME & DESCRIPTION (column five of the Electrical Parts List)

In the Parts List, an Item Name is separated from the description by a colon (:). Because of space limitations, an Item Name may sometimes appear as incomplete. For further Item Name identification, the U.S. Federal Cataloging Handbook H6-1 can be utilized where possible.

MFR. CODE (column six of the Electrical Parts List)

Indicates the code number of the actual manufacturer of the part. (Code to name and address cross reference can be found immediately after this page.)

MFR. PART NUMBER (column seven of the Electrical Parts List)

Indicates actual manufacturers part number.

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
01121	ALLEN-BRADLEY CO	1201 S 2ND ST	MILWAUKEE WI 53204-2410
01295	TEXAS INSTRUMENTS INC SEMICONDUCTOR GROUP	13500 N CENTRAL EXPY PO BOX 655012	DALLAS TX 75265
02289	HI-G CO INC SUB OF NYTRONICS INC	101 LOCUST ST	HARTFORD CT 06114-1504
02735	RCA CORP SOLID STATE DIVISION	ROUTE 202	SOMERVILLE NJ 08876
04222	AVX CERAMICS DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
04713	MOTOROLA INC SEMICONDUCTOR PRODUCTS SECTOR	5005 E MCDOWELL RD	PHOENIX AZ 85008-4229
05397	UNION CARBIDE CORP MATERIALS SYSTEMS DIV	11901 MADISON AVE	CLEVELAND OH 44101
07263	FAIRCHILD SEMICONDUCTOR CORP NORTH AMERICAN SALES SUB OF SCHLUMBERGER LTD MS 118	10400 RIDGEVIEW CT	CUPERTINO CA 95014
07716	TRW INC TRW IRC FIXED RESISTORS/BURLINGTON	2850 MT PLEASANT AVE	BURLINGTON IA 52601
11236	CTS CORP BERNE DIV THICK FILM PRODUCTS GROUP	406 PARR ROAD	BERNE IN 46711-9506
18324	SIGNETICS CORP MILITARY PRODUCTS DIV	4130 S MARKET COURT	SACRAMENTO CA 95834-1222
19701	MEPCO/CENTRALAB A NORTH AMERICAN PHILIPS CO MINERAL WELLS AIRPORT	PO BOX 760	MINERAL WELLS TX 76067-0760
20932	KYOCERA INTERNATIONAL INC	11620 SORRENTO VALLEY RD PO BOX 81543 PLANT NO 1	SAN DIEGO CA 92121
22526	DU PONT E I DE NEMOURS AND CO INC DU PONT CONNECTOR SYSTEMS DIV MILITARY PRODUCTS GROUP	515 FISHING CREEK RD	NEW CUMBERLAND PA 17070-3007
24355	ANALOG DEVICES INC	RT 1 INDUSTRIAL PK PO BOX 9106	NORWOOD MA 02062
24546	CORNING GLASS WORKS	550 HIGH ST	BRADFORD PA 16701-3737
27014	NATIONAL SEMICONDUCTOR CORP	2900 SEMICONDUCTOR DR	SANTA CLARA CA 95051-0606
31433	KEMET ELECTRONICS CORP NATIONAL SALES HEADQUARTERS	PO BOX 5928	GREENVILLE SC 29606
32293	INTERSIL INC SUB OF GENERAL ELECTRIC CO	10600 RIDGEVIEW COURT	CUPERTINO CA 95014-0704
32997	BOURNS INC TRIMPOT DIV	1200 COLUMBIA AVE	RIVERSIDE CA 92507-2114
50434	HEWLETT-PACKARD CO OPTOELECTRONICS DIV	370 W TRIMBLE RD	SAN JOSE CA 95131
57668	ROHM CORP	8 WHATNEY PO BOX 19515	IRVINE CA 92713
59660	TUSONIX INC	7741 N BUSINESS PARK DR PO BOX 37144	TUCSON AZ 85740-7144
74970	JOHNSON E F CO	299 10TH AVE S W	WASECA MN 56093-2539
75042	IRC ELECTRONIC COMPONENTS PHILADELPHIA DIV TRW FIXED RESISTORS	401 N BROAD ST	PHILADELPHIA PA 19108-1001
75915	LITTELFUSE INC SUB TRACOR INC	800 E NORTHWEST HWY	DES PLAINES IL 60016-3049
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077-0001
91637	DALE ELECTRONICS INC	2064 12TH AVE PO BOX 609	COLUMBUS NE 68601-3632
S0167	FUJITSU LTD	2-3-13 TORANOMON MINATO-KU	TOKYO JAPAN
S4217	NIPPON CHEMI-CON CORP	1-167-1 HIGASHI-OUME OUME-CITY	TOKYO JAPAN
S4220	SOSHIN ELECTRIC CO LTD	1-18-18 NAKAMAGONE OHTA-KU	TOKYO JAPAN
S4431	MURATA MFG CO LTD	16 KAIDEN NISHIJM CHO NAGAOKAKY-CITY	KYOTO JAPAN

CROSS INDEX - MFR. CODE NUMBER TO MANUFACTURER

Mfr. Code	Manufacturer	Address	City, State, Zip Code
S5372	HITACHI LTD	1-5-1 MARUNOUCHI CHIYODA-KU	TOKYO JAPAN
S5407	SHOWA ELECTRIC WIRE & CABLE CO LTD	1-2-20 TORANOMON MINATO-KU	TOKYO JAPAN
S5518	ROHM CO LTD	21 SAIINN MIZOSAKI CHO UKYO KU	KYOTO JAPAN
TK00D	ALPHA ELECTRONICS CORP	1-10-6 KAJIMACHI CHIYODA-KU	TOKYO JAPAN
TK00I	MATSUSHITA ELECTRIC IND CO LTD	1-1-2 SHIBAKOEN MINATO-KU	TOKYO JAPAN
TK00J	NEC CORP	5-33-1 SHIBA MINATO-KU	TOKYO JAPAN
TK00L	TOSHIBA CO LTD	1-1-1 SHIBAURA MINATO-KU	TOKYO JAPAN
TK00T	LINEAR TECHNOLOGY CORP	3-1 KOSUGI-CHO NAKAHARA-KU KAWASAKI-CITY	KANAGAWA JAPAN
TK00W	RYOSAN ELEC CO LTD	2-18-22 SOTO-KANDA SHIYODA-KU	TOKYO JAPAN
TK00Y	INTERSIL INC	7-4-7 NISHI-SHINJUKU SHINJUKU-KU	TOKYO JAPAN
TK0191	SONY TEKTRONIX	PO BOX 14 HANEDA AIRPORT	TOKYO JAPAN
TK0AA	MOTOROLA INC	1-6-7 NAKAMACHI MUSASHINO-CITY	CHIBA JAPAN
TK0AC	ANALOG DEVICES INC	4-7-8 KOUJIMACHI CHIYODA-KU	TOKYO JAPAN
TK0BO	ELMEC CORP	458 OHAZASHIMOKOSAKA KAWAGOE-CITY	SAITAMA JAPAN
TK0BT	TAISEI	5-16-2 NISHI-IKEBUKURO TOSHIMA-KU	TOKYO JAPAN
TK0FB	NIHON BURNDY	3-26-33 TAKANASA MINATO-KU	TOKYO JAPAN

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10	671-0691-00			CIRCUIT BD ASSY:ATT	TK0191	ORDER BY DESCR
A12	671-0690-00			CIRCUIT BD ASSY:INPUT AMP	TK0191	ORDER BY DESCR
A14	671-0689-00			CIRCUIT BD ASSY:AUTO CAL	TK0191	ORDER BY DESCR
A18	671-0804-00			CIRCUIT BD ASSY:A/D	80009	671-0804-00
A22	670-9856-02			CIRCUIT BD ASSY:TRIGGER	80009	670-9856-02
A24	670-9857-02			CIRCUIT BD ASSY:TV TRIGGER (OPTION 05)	80009	670-9857-02
A30	670-9858-01			CIRCUIT BD ASSY:ENVELOPE	TK0191	ORDER BY DESCR
A32	671-0688-01			CIRCUIT BD ASSY:TIME BASE	80009	671-0688-01
A34	671-0361-00			CIRCUIT BD ASSY:TIME BASE CONTROL	80009	671-0361-00
A36	671-0687-00			CIRCUIT BD ASSY:MPU	TK0191	ORDER BY DESCR
A40	671-0876-00			CIRCUIT BD ASSY:ADDRESS GENERATOR	TK0191	ORDER BY DESCR
A44	670-9862-00			CIRCUIT BD ASSY:AVERAGER	80009	670-9862-00
A50	671-0686-01			CIRCUIT BD ASSY:MPU	80009	671-0686-01
A52	671-0685-00			CIRCUIT BD ASSY:DMA	TK0191	ORDER BY DESCR
A54	670-9865-00			CIRCUIT BD ASSY:DISPLAY CONTROL	80009	670-9865-00
A56	670-9866-00			CIRCUIT BD ASSY:GPIB/MONITOR	80009	670-9866-00
A60	671-0684-00			CIRCUIT BD ASSY:FRONT PANEL CONTROL	TK0191	ORDER BY DESCR
A64	670-9868-00			CIRCUIT BD ASSY:INDICATOR (OPTION 19)	80009	670-9868-00
A70	670-9869-00			CIRCUIT BD ASSY:MAIN INTERCONNECT	80009	670-9869-00
A74	670-9870-00			CIRCUIT BD ASSY:I/O	80009	670-9870-00
A76	670-9871-00			CIRCUIT BD ASSY:OSCILLATOR	80009	670-9871-00
A10	671-0691-00			CIRCUIT BD ASSY:ATT	TK0191	ORDER BY DESCR
A10AT101	307-1013-06			ATTENUATOR,FXD:10X	80009	307-1013-06
A10AT102	307-1013-06			ATTENUATOR,FXD:10X	80009	307-1013-06
A10AT201	307-1013-06			ATTENUATOR,FXD:10X	80009	307-1013-06
A10AT202	307-1013-06			ATTENUATOR,FXD:10X	80009	307-1013-06
A10C10	290-1207-00			CAP,FXD,ELCTLT:22UF,20%,25V	S4217	SXE25VB-22
A10C20	290-1207-00			CAP,FXD,ELCTLT:22UF,20%,25V	S4217	SXE25VB-22
A10C30	290-1207-00			CAP,FXD,ELCTLT:22UF,20%,25V	S4217	SXE25VB-22
A10C100	285-1132-00			CAP,FXD,PLASTIC:0.019UF,10%,600V	80009	285-1132-00
A10C104	281-0138-00			CAP,VAR,PLASTIC:0.3-1.2PF,600V	74970	273-0001-007
A10C106	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A10C108	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V	04222	MA101A101KAA
A10C115	283-0909-00			CAP,FXD,CER DI:5PF,+/-0.5PF,50V	S4431	RPE110C0G050D50
A10C120	283-1015-00			CAP,FXD,CER DI:36PF,5%,50V	80009	283-1015-00
A10C122	283-0000-00			CAP,FXD,CER DI:0.001UF,+100-0%,500V	59660	831-610-Y5U0102P
A10C124	283-0168-00			CAP,FXD,CER DI:12PF,5%,100V	05397	C315C120J1G5CA
A10C126	283-1016-00			CAP,FXD,CER DI:7PF,+/-0.5PF,50V	80009	283-1016-00
A10C130	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A10C132	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A10C134	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A10C140	283-1013-00			CAP,FXD,CER DI:0.5PF,+/-5PF,50V	80009	283-1013-00
A10C150	281-0930-00			CAP NTWK,CER DI:(7) 0.1UF,+80/-20%,25V	80009	281-0930-00
A10C162	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A10C200	285-1132-00			CAP,FXD,PLASTIC:0.019UF,10%,600V	80009	285-1132-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10C204	281-0138-00			CAP,VAR,PLASTIC:0.3-1.2PF,600V	74970	273-0001-007
A10C206	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A10C208	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V	04222	MA101A101KAA
A10C215	283-0909-00			CAP,FXD,CER DI:5PF,+/-0.5PF,50V	S4431	RPE110C0G050D50
A10C220	283-1015-00			CAP,FXD,CER DI:36PF,5%,50V	80009	283-1015-00
A10C222	283-0000-00			CAP,FXD,CER DI:0.001UF,+100-0%,500V	59660	831-610-Y5U0102P
A10C224	283-0168-00			CAP,FXD,CER DI:12PF,5%,100V	05397	C315C120J1G5CA
A10C226	283-1016-00			CAP,FXD,CER DI:7PF,+/-0.5PF,50V	80009	283-1016-00
A10C230	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A10C232	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A10C234	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A10C240	283-1013-00			CAP,FXD,CER DI:0.5PF,+/-5PF,50V	80009	283-1013-00
A10C250	281-0930-00			CAP NTWK,CER DI:(7) 0.1UF,+80/-20%,25V	80009	281-0930-00
A10C262	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A10C300	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A10C302	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A10CR100	152-0323-03			SEMICOND DVC,DI:SI,35V,0.1A	80009	152-0323-03
A10CR102	152-0323-03			SEMICOND DVC,DI:SI,35V,0.1A	80009	152-0323-03
A10CR104	152-0323-03			SEMICOND DVC,DI:SI,35V,0.1A	80009	152-0323-03
A10CR106	152-0323-03			SEMICOND DVC,DI:SI,35V,0.1A	80009	152-0323-03
A10CR110	152-0832-00			SEMICOND DVC,DI:SW,SI,50V,0.12A,DO-34	80009	152-0832-00
A10CR200	152-0323-03			SEMICOND DVC,DI:SI,35V,0.1A	80009	152-0323-03
A10CR202	152-0323-03			SEMICOND DVC,DI:SI,35V,0.1A	80009	152-0323-03
A10CR204	152-0323-03			SEMICOND DVC,DI:SI,35V,0.1A	80009	152-0323-03
A10CR206	152-0323-03			SEMICOND DVC,DI:SI,35V,0.1A	80009	152-0323-03
A10CR210	152-0832-00			SEMICOND DVC,DI:SW,SI,50V,0.12A,DO-34	80009	152-0832-00
A10F100	159-0245-00			FUSE,WIRE LEAD:1A,125V,FAST	75915	R251001T1
A10F200	159-0245-00			FUSE,WIRE LEAD:1A,125V,FAST	75915	R251001T1
A10J110	131-3849-00			CONN,RCPT,ELEC:COAX,FINGER LOCK	80009	131-3849-00
A10J112	131-3849-00			CONN,RCPT,ELEC:COAX,FINGER LOCK	80009	131-3849-00
A10J121	131-3862-00			CONN,RCPT,ELEC:DIP SKT,2 X 10,0.1 SPACING	80009	131-3862-00
A10J161	131-3862-00			CONN,RCPT,ELEC:DIP SKT,2 X 10,0.1 SPACING	80009	131-3862-00
A10K100	148-0199-02			RELAY,REED:FORM A,0.4A,250V	80009	148-0199-02
A10K102	148-0199-02			RELAY,REED:FORM A,0.4A,250V	80009	148-0199-02
A10K104	148-0199-02			RELAY,REED:FORM A,0.4A,250V	80009	148-0199-02
A10K106	148-0199-02			RELAY,REED:FORM A,0.4A,250V	80009	148-0199-02
A10K108	148-0199-02			RELAY,REED:FORM A,0.4A,250V	80009	148-0199-02
A10K110	148-0199-02			RELAY,REED:FORM A,0.4A,250V	80009	148-0199-02
A10K112	148-0199-02			RELAY,REED:FORM A,0.4A,250V	80009	148-0199-02
A10K114	148-0199-02			RELAY,REED:FORM A,0.4A,250V	80009	148-0199-02
A10K116	148-0199-02			RELAY,REED:FORM A,0.4A,250V	80009	148-0199-02
A10K118	148-0199-02			RELAY,REED:FORM A,0.4A,250V	80009	148-0199-02
A10K200	148-0199-02			RELAY,REED:FORM A,0.4A,250V	80009	148-0199-02
A10K202	148-0199-02			RELAY,REED:FORM A,0.4A,250V	80009	148-0199-02
A10K204	148-0199-02			RELAY,REED:FORM A,0.4A,250V	80009	148-0199-02
A10K206	148-0199-02			RELAY,REED:FORM A,0.4A,250V	80009	148-0199-02
A10K208	148-0199-02			RELAY,REED:FORM A,0.4A,250V	80009	148-0199-02
A10K210	148-0199-02			RELAY,REED:FORM A,0.4A,250V	80009	148-0199-02
A10K212	148-0199-02			RELAY,REED:FORM A,0.4A,250V	80009	148-0199-02
A10K214	148-0199-02			RELAY,REED:FORM A,0.4A,250V	80009	148-0199-02
A10K216	148-0199-02			RELAY,REED:FORM A,0.4A,250V	80009	148-0199-02
A10K218	148-0199-02			RELAY,REED:FORM A,0.4A,250V	80009	148-0199-02
A10Q100	151-1032-00			TRANSISTOR:FET,DUAL N-CHAN,SI,TO-78A	80009	151-1032-00
A10Q102	151-0871-00			TRANSISTOR:NPN,SI,TO-92B	TK00J	2SC2570A
A10Q200	151-1032-00			TRANSISTOR:FET,DUAL N-CHAN,SI,TO-78A	80009	151-1032-00
A10Q202	151-0871-00			TRANSISTOR:NPN,SI,TO-92B	TK00J	2SC2570A
A10R102	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A10R104	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A10R106	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A10R108	313-0510-00			RES,FXD,FILM:51 OHM,5%,0.166W	80009	313-0510-00
A10R109	313-0360-00			RES,FXD,FILM:36 OHM,5%,0.166W	80009	313-0360-00
A10R111	313-0100-00			RES,FXD,FILM:10 OHM,5%,0.166W	80009	313-0100-00
A10R113	313-0111-00			RES,FXD,FILM:110 OHM 5%,0.166W	S5518	R20T29J1100HM
A10R114	313-0300-00			RES,FXD,FILM:30 OHM,5%,0.166W	80009	313-0300-00
A10R116	313-0510-00			RES,FXD,FILM:51 OHM,5%,0.166W	80009	313-0510-00
A10R117	----- -----			RES,FXD,FILM:82 OHM		
A10R118	313-0560-00			RES,FXD,FILM:56 OHM,5%,0.166W	S5518	R20 J 56 OHM
A10R120	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A10R122	321-0481-01			RES,FXD,FILM:1M OHM,0.5%,0.125W	07716	CEAD10003D
A10R124	313-0474-00			RES,FXD,FILM:470K OHM,5%,0.166W	80009	313-0474-00
A10R126	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A10R128	326-0001-00			RES,FXD,FILM:22 OHM,1%,0.166W	80009	326-0001-00
A10R130	----- -----			RES,FXD,FILM:82 OHM		
A10R132	313-0131-00			RES,FXD,FILM:130 OHM,5%,0.166W	80009	313-0131-00
A10R134	326-0030-01			RES,FXD,FILM:20 OHM,1%,0.166W	S5518	
A10R136	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A10R138	313-0242-00			RES,FXD,FILM:2.4K OHM,5%,0.166W	80009	313-0242-00
A10R140	326-0084-00			RES,FXD,FILM:73.2 OHM,1%,0.166W	S5518	CRB20R65FY73.20H
A10R202	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A10R204	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A10R206	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A10R208	313-0510-00			RES,FXD,FILM:51 OHM,5%,0.166W	80009	313-0510-00
A10R209	313-0360-00			RES,FXD,FILM:36 OHM,5%,0.166W	80009	313-0360-00
A10R211	313-0100-00			RES,FXD,FILM:10 OHM,5%,0.166W	80009	313-0100-00
A10R213	313-0111-00			RES,FXD,FILM:110 OHM 5%,0.166W	S5518	R20T29J1100HM
A10R214	313-0300-00			RES,FXD,FILM:30 OHM,5%,0.166W	80009	313-0300-00
A10R216	313-0510-00			RES,FXD,FILM:51 OHM,5%,0.166W	80009	313-0510-00
A10R217	----- -----			RES,FXD,FILM:82 OHM		
A10R218	313-0560-00			RES,FXD,FILM:56 OHM,5%,0.166W	S5518	R20 J 56 OHM
A10R220	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A10R222	321-0481-01			RES,FXD,FILM:1M OHM,0.5%,0.125W	07716	CEAD10003D
A10R224	313-0474-00			RES,FXD,FILM:470K OHM,5%,0.166W	80009	313-0474-00
A10R226	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A10R228	326-0001-00			RES,FXD,FILM:22 OHM,1%,0.166W	80009	326-0001-00
A10R230	----- -----			RES,FXD,FILM:82 OHM		
A10R232	313-0131-00			RES,FXD,FILM:130 OHM,5%,0.166W	80009	313-0131-00
A10R234	326-0030-01			RES,FXD,FILM:20 OHM,1%,0.166W	S5518	
A10R236	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A10R238	313-0242-00			RES,FXD,FILM:2.4K OHM,5%,0.166W	80009	313-0242-00
A10R240	326-0084-00			RES,FXD,FILM:73.2 OHM,1%,0.166W	S5518	CRB20R65FY73.20H
A10R300	313-0391-00			RES,FXD,FILM:390 OHM,5%,0.166W	80009	313-0391-00
A10R302	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A10R304	313-0132-00			RES,FXD,FILM:1.3K OHM,5%,0.166W	80009	313-0132-00
A10R306	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A10T102	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A10U100	156-3587-00			MICROCKT,LINEAR:BUFFER AMP,HYBRID	80009	156-3587-00
A10U200	156-3587-00			MICROCKT,LINEAR:BUFFER AMP,HYBRID	80009	156-3587-00
A10VR10	152-0280-00			SEMICOND DVC,DI:ZEN,SI,6.2V,5%,0.4W,DO-7	04713	1N753A
A10VR20	152-1065-00			SEMICOND DVC,DI:ZENER,SI,6.2V,0.4V,0.8W	S5372	DO-41 HZ6.28P
A10XU101	136-0252-07			SOCKET,PIN CONN:W/O DIMPLE (QUANTITY OF 6)	22526	75060-012
A10XU102	136-0252-07			SOCKET,PIN CONN:W/O DIMPLE (QUANTITY OF 6)	22526	75060-012
A10XU201	136-0252-07			SOCKET,PIN CONN:W/O DIMPLE (QUANTITY OF 6)	22526	75060-012
A10XU202	136-0252-07			SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
				(QUANTITY OF 6)		
A12	671-0690-00			CIRCUIT BD ASSY:INPUT AMP	TK0191	ORDER BY DESCR
A12C10	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A12C12	290-1161-00			CAP,FXD,ELCTLT:47UF,20%,25V	80009	290-1161-00
A12C20	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A12C22	290-1161-00			CAP,FXD,ELCTLT:47UF,20%,25V	80009	290-1161-00
A12C30	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A12C32	290-1161-00			CAP,FXD,ELCTLT:47UF,20%,25V	80009	290-1161-00
A12C40	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A12C42	290-1161-00			CAP,FXD,ELCTLT:47UF,20%,25V	80009	290-1161-00
A12C50	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A12C52	290-1161-00			CAP,FXD,ELCTLT:47UF,20%,25V	80009	290-1161-00
A12C100	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A12C102	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A12C104	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A12C106	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A12C108	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A12C110	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A12C150	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A12C152	283-1014-00			CAP,FXD,CER DI:0.1UF,+/-20%,50V	80009	283-1014-00
A12C200	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C202	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C204	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C206	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C208	283-1017-00			CAP,FXD,CER DI:4700PF,5%,50V	80009	283-1017-00
A12C210	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C211	290-1214-00			CAP,FXD,ELCTLT:10UF,205,25V	80009	290-1214-00
A12C250	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C260	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C300	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C302	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C304	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C306	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C308	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C310	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A12C312	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A12C350	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C352	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C354	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C356	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C358	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C400	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C402	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C404	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C406	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C408	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C410	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C500	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A12C502	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A12C503	283-0909-00			CAP,FXD,CER DI:5PF,+/-0.5PF,50V	S4431	RPE110C0G050D50
A12C504	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A12C506	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A12C508	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A12C510	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A12C550	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A12C552	283-1014-00			CAP,FXD,CER DI:0.1UF,+/-20%,50V	80009	283-1014-00
A12C600	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C601	283-1017-00			CAP,FXD,CER DI:4700PF,5%,50V	80009	283-1017-00
A12C602	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C604	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C606	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C608	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C611	290-1214-00			CAP,FXD,ELCTLT:10UF,20S,25V	80009	290-1214-00
A12C650	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C652	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C654	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A12C656	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C700	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C702	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C704	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C706	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C708	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C710	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A12C712	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A12C750	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C752	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C754	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C756	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C758	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C800	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C810	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C812	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C814	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C816	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C818	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C820	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C822	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C910	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C916	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12C918	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A12CR100	152-0832-00			SEMICOND DVC,DI:SW,SI,50V,0.12A,DO-34	80009	152-0832-00
A12CR160	152-0832-00			SEMICOND DVC,DI:SW,SI,50V,0.12A,DO-34	80009	152-0832-00
A12CR250	152-0832-00			SEMICOND DVC,DI:SW,SI,50V,0.12A,DO-34	80009	152-0832-00
A12CR260	152-0832-00			SEMICOND DVC,DI:SW,SI,50V,0.12A,DO-34	80009	152-0832-00
A12CR300	152-1081-00			SEMICOND DVC,DI:SHOTTKY,GAAS,4V,150MA	80009	152-1081-00
A12CR700	152-1081-00			SEMICOND DVC,DI:SHOTTKY,GAAS,4V,150MA	80009	152-1081-00
A12J110	131-3849-00			CONN,RCPT,ELEC:COAX,FINGER LOCK	80009	131-3849-00
A12J112	131-3849-00			CONN,RCPT,ELEC:COAX,FINGER LOCK	80009	131-3849-00
A12J122	131-2942-01			CONN,RCPT,ELEC:HEADER,ANGLE,2 X 13	80009	131-2942-01
A12J123	131-3849-00			CONN,RCPT,ELEC:COAX,FINGER LOCK (QUANTITY OF 2)	80009	131-3849-00
A12J124	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A12J165	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A12K100	148-0215-00			RELAY,ARM:DPDT,28V,1A,12V	02289	ORDER BY DESCR
A12K160	148-0205-00			RELAY,REED:SPST,FORM A,5V,120 OHM COIL	80009	148-0205-00
A12L150	108-1432-00			COIL,RF:FXD,3.3UH,10%	S4220	AML0206N3R3M
A12L204	108-1456-00			COIL,RF:FXD,82NH,+/-5NH,AIRWOUND	80009	108-1456-00
A12L550	108-1432-00			COIL,RF:FXD,3.3UH,10%	S4220	AML0206N3R3M
A12L662	108-1456-00			COIL,RF:FXD,82NH,+/-5NH,AIRWOUND	80009	108-1456-00
A12P120	131-3137-00			CONN,PLUG,ELEC:DIN,3 X 32,MALE,0.1 SPACING	80009	131-3137-00
A12P121	131-3865-00			CONN,RCPT,ELEC:HDR,RTANG,2 X 10,0.1 SPACING	80009	131-3865-00
A12Q250	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A12Q260	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00

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A12Q400	151-0232-00			TRANSISTOR:NPN,SI,TO-78	07263	SP12141
A12Q410	151-0232-00			TRANSISTOR:NPN,SI,TO-78	07263	SP12141
A12Q650	151-1021-00			TRANSISTOR:FET,N-CHAN,SI,TO-18	80009	151-1021-00
A12Q820	151-0736-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0736-00
A12R104	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A12R108	313-0112-00			RES,FXD,FILM:1.1K OHM,5%,0.166W	S5518	R20T29J1.1KOHM
A12R110	313-0621-00			RES,FXD,FILM:620 OHM,5%,0.166W	80009	313-0621-00
A12R112	313-0162-00			RES,FXD,FILM:1.6K OHM,5%,0.166W	80009	313-0162-00
A12R114	311-2380-00			RES,VAR,NONWW:TRMR,500 OHM,20%,0.5W	80009	311-2380-00
A12R116	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A12R118	326-0003-00			RES,FXD,FILM:100 OHM,1%,0.166W	80009	326-0003-00
A12R120	326-0003-00			RES,FXD,FILM:100 OHM,1%,0.166W	80009	326-0003-00
A12R122	315-0910-00			RES,FXD,FILM:91 OHM,5%,0.25W	19701	5043CX91R00J
A12R150	313-0431-00			RES,FXD,FILM:430 OHM,5%,0.166W	80009	313-0431-00
A12R152	313-0300-00			RES,FXD,FILM:30 OHM,5%,0.166W	80009	313-0300-00
A12R161	313-0151-00			RES,FXD,FILM:150 OHM,5%,0.166W	80009	313-0151-00
A12R200	326-0085-00			RES,FXD,FILM:75 OHM,1%,0.166W	S5518	CRB20R65FY75 OHM
A12R201	326-0003-00			RES,FXD,FILM:100 OHM,1%,0.166W	80009	326-0003-00
A12R202	326-0085-00			RES,FXD,FILM:75 OHM,1%,0.166W	S5518	CRB20R65FY75 OHM
A12R203	326-0003-00			RES,FXD,FILM:100 OHM,1%,0.166W	80009	326-0003-00
A12R204	326-0005-00			RES,FXD,FILM:160 OHM,1%,0.166W	80009	326-0005-00
A12R208	326-0019-00			RES,FXD,FILM:4.7K OHM,1%,0.166W	80009	326-0019-00
A12R210	326-0020-00			RES,FXD,FILM:5.1K OHM,1%,0.166W	80009	326-0020-00
A12R212	326-0845-00			RES,FXD,FILM:2.7K OHM,1%,0.166W	80009	326-0845-00
A12R214	311-2381-00			RES,VAR,NONWW:TRMR,1K OHM,20%,0.5W	80009	311-2381-00
A12R250	313-0271-00			RES,FXD,FILM:270 OHM,5%,0.166W	80009	313-0271-00
A12R252	313-0751-00			RES,FXD,FILM:750 OHM,5%,0.166W	80009	313-0751-00
A12R254	313-0751-00			RES,FXD,FILM:750 OHM,5%,0.166W	80009	313-0751-00
A12R260	313-0751-00			RES,FXD,FILM:750 OHM,5%,0.166W	80009	313-0751-00
A12R262	313-0301-00			RES,FXD,FILM:300 OHM,5%,0.166W	80009	313-0301-00
A12R264	313-0751-00			RES,FXD,FILM:750 OHM,5%,0.166W	80009	313-0751-00
A12R300	313-0910-00			RES,FXD,FILM:91 OHM,5%,0.166W	S5518	R20 T-29J 91 OHM
A12R350	313-0910-00			RES,FXD,FILM:91 OHM,5%,0.166W	S5518	R20 T-29J 91 OHM
A12R352	326-0040-00			RES,FXD,FILM:25.5K OHM,1%,0.166W	S5518	CRB20FY25.5OHM
A12R400	313-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.166W	80009	313-0222-00
A12R402	313-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.166W	80009	313-0222-00
A12R404	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A12R406	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A12R408	326-0019-00			RES,FXD,FILM:4.7K OHM,1%,0.166W	80009	326-0019-00
A12R410	326-0019-00			RES,FXD,FILM:4.7K OHM,1%,0.166W	80009	326-0019-00
A12R412	326-0021-00			RES,FXD,FILM:10K OHM,1%,0.166W	80009	326-0021-00
A12R414	326-0021-00			RES,FXD,FILM:10K OHM,1%,0.166W	80009	326-0021-00
A12R416	326-0021-00			RES,FXD,FILM:10K OHM,1%,0.166W	80009	326-0021-00
A12R418	326-0021-00			RES,FXD,FILM:10K OHM,1%,0.166W	80009	326-0021-00
A12R420	326-0021-00			RES,FXD,FILM:10K OHM,1%,0.166W	80009	326-0021-00
A12R422	326-0021-00			RES,FXD,FILM:10K OHM,1%,0.166W	80009	326-0021-00
A12R424	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A12R426	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A12R428	313-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.166W	80009	313-0152-00
A12R430	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A12R432	313-0911-00			RES,FXD,FILM:910 OHM,5%,0.166W	80009	313-0911-00
A12R434	313-0621-00			RES,FXD,FILM:620 OHM,5%,0.166W	80009	313-0621-00
A12R436	313-0241-00			RES,FXD,FILM:240 OHM,5%,0.166W	80009	313-0241-00
A12R438	313-0681-00			RES,FXD,FILM:680 OHM,5%,0.166W	80009	313-0681-00
A12R440	313-0203-00			RES,FXD,FILM:20K OHM,5%,0.166W	80009	313-0203-00
A12R442	313-0163-00			RES,FXD,FILM:16K OHM,5%,0.166W	80009	313-0163-00
A12R444	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A12R446	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00

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A12R448	313-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.166W	80009	313-0152-00
A12R450	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A12R503	313-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.166W	80009	313-0222-00
A12R506	313-0112-00			RES,FXD,FILM:1.1K OHM,5%,0.166W	S5518	R20T29J1.1KOHM
A12R508	313-0621-00			RES,FXD,FILM:620 OHM,5%,0.166W	80009	313-0621-00
A12R550	313-0471-00			RES,FXD,FILM:470 OHM,5%,0.166W	80009	313-0471-00
A12R600	326-0085-00			RES,FXD,FILM:75 OHM,1%,0.166W	S5518	CRB20R65FY75 OHM
A12R601	326-0019-00			RES,FXD,FILM:4.7K OHM,1%,0.166W	80009	326-0019-00
A12R602	326-0085-00			RES,FXD,FILM:75 OHM,1%,0.166W	S5518	CRB20R65FY75 OHM
A12R650	326-0020-00			RES,FXD,FILM:5.1K OHM,1%,0.166W	80009	326-0020-00
A12R651	313-0104-00			RES,FXD,FILM:100K OHM,5%,0.166W	80009	313-0104-00
A12R652	326-0845-00			RES,FXD,FILM:2.7K OHM,1%,0.166W	80009	326-0845-00
A12R653	313-0104-00			RES,FXD,FILM:100K OHM,5%,0.166W	80009	313-0104-00
A12R654	311-2381-00			RES,VAR,NONWW:TRMR,1K OHM,20%,0.5W	80009	311-2381-00
A12R656	326-0028-00			RES,FXD,FILM:3.6K OHM,1%,0.166W	80009	326-0028-00
A12R658	326-0022-00			RES,FXD,FILM:18K OHM,1%,0.166W	80009	326-0022-00
A12R659	313-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.166W	80009	313-0222-00
A12R660	313-0104-00			RES,FXD,FILM:100K OHM,5%,0.166W	80009	313-0104-00
A12R662	326-0111-00			RES,FXD,FILM:140K OHM,1%,0.166W	S5518	CRB20 FY 140 OHM
A12R664	326-0002-00			RES,FXD,FILM:62 OHM,1%,0.166W	80009	326-0002-00
A12R700	313-0910-00			RES,FXD,FILM:91 OHM,5%,0.166W	S5518	R20 T-29J 91 OHM
A12R750	313-0910-00			RES,FXD,FILM:91 OHM,5%,0.166W	S5518	R20 T-29J 91 OHM
A12R752	326-0040-00			RES,FXD,FILM:25.5K OHM,1%,0.166W	S5518	CRB20FY25.50HM
A12R814	313-0561-00			RES,FXD,FILM:560 OHM,5%,0.166W	80009	313-0561-00
A12R820	313-0561-00			RES,FXD,FILM:560 OHM,5%,0.166W	80009	313-0561-00
A12R822	313-0561-00			RES,FXD,FILM:560 OHM,5%,0.166W	80009	313-0561-00
A12R824	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A12R830	307-0878-00			RES NTWK,FXD,FI:4,1K OHM,5%,0.125W	80009	307-0878-00
A12R832	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A12R834	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A12R836	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A12TP10	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A12TP20	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A12TP30	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A12TP40	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A12TP50	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A12TP100	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A12TP200	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A12TP300	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A12TP400	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A12TP410	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A12U100	165-2089-05			MICROCKT,LINEAR:VERTICAL PREAMP,100 OHM	80009	165-2089-05
A12U200	156-3588-00			MICROCKT,LINEAR:INTERFACE AMP,HYBRID	80009	156-3588-00
A12U300	156-3587-00			MICROCKT,LINEAR:BUFFER AMP,HYBRID	80009	156-3587-00
A12U350	156-3587-00			MICROCKT,LINEAR:BUFFER AMP,HYBRID	80009	156-3587-00
A12U400	156-1771-00			MICROCKT,LINEAR:DUAL OP-AMP	80009	156-1771-00
A12U410	156-0513-00			MICROCKT,DGTL:CMOS,8-CHANNEL MUX	04713	MC14051BCL
A12U450	119-1671-00			HYBRID CIRCUIT:INLINE BLOCK	80009	119-1671-00
A12U500	165-2089-05			MICROCKT,LINEAR:VERTICAL PREAMP,100 OHM	80009	165-2089-05
A12U600	156-3588-00			MICROCKT,LINEAR:INTERFACE AMP,HYBRID	80009	156-3588-00
A12U650	156-0515-00			MICROCKT,DGTL:CMOS,TRIPLE 2-CHAN MUX	02735	CD4053BF
A12U700	156-3587-00			MICROCKT,LINEAR:BUFFER AMP,HYBRID	80009	156-3587-00
A12U750	156-3587-00			MICROCKT,LINEAR:BUFFER AMP,HYBRID	80009	156-3587-00
A12U800	156-0469-00			MICROCKT,DGTL:3-LINE TO 8-LINE DECODER	01295	SN74LS138N
A12U810	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A12U812	156-0865-00			MICROCKT,DGTL:OCTAL D FF W/CLR	01295	SN74LS273 N OR J
A12U814	156-0865-00			MICROCKT,DGTL:OCTAL D FF W/CLR	01295	SN74LS273 N OR J
A12U816	160-5533-00			MICROCKT,DGTL:512 X 8 BI-PROM,PRGM	S0167	PRGMMB7124E16DIP

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A12U818	156-2903-00			MICROCKT,DGTL:8 UNIT DARLINGTON XSTR ARRAY	80009	156-2903-00
A12U820	156-0385-00			MICROCKT,DGTL:HEX INVERTER	01295	SN74LS04 N OR J
A12U822	156-0480-00			MICROCKT,DGTL:TTL,QUAD 2-INP AND GATE	01295	SN74LS08(N OR J)
A12U910	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A12U912	156-0865-00			MICROCKT,DGTL:OCTAL D FF W/CLR	01295	SN74LS273 N OR J
A12U914	156-0865-00			MICROCKT,DGTL:OCTAL D FF W/CLR	01295	SN74LS273 N OR J
A12U916	160-5533-00			MICROCKT,DGTL:512 X 8 BI-PROM,PRGM	S0167	PRGMMB7124E16DIP
A12U918	156-2903-00			MICROCKT,DGTL:8 UNIT DARLINGTON XSTR ARRAY	80009	156-2903-00
A12VR300	152-0280-00			SEMICOND DVC,DI:ZEN,SI,6.2V,5%,0.4W,DO-7	04713	1N753A
A12VR350	152-0280-00			SEMICOND DVC,DI:ZEN,SI,6.2V,5%,0.4W,DO-7	04713	1N753A
A12VR650	152-0813-00			SEMICOND DVC,DI:ZENER,SI,3.0V,5%,5W	80009	152-0813-00
A12VR700	152-0280-00			SEMICOND DVC,DI:ZEN,SI,6.2V,5%,0.4W,DO-7	04713	1N753A
A12VR750	152-0280-00			SEMICOND DVC,DI:ZEN,SI,6.2V,5%,0.4W,DO-7	04713	1N753A
A12W10	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A12W20	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A12W30	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A12W40	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A12W50	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A12XU124	136-0252-07			SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
A12XU165	136-0252-07			SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
A14	671-0689-00			CIRCUIT BD ASSY:AUTO CAL	TK0191	ORDER BY DESCR
A14C100	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C102	281-0819-00			CAP,FXD,CER DI:33 PF,5%,50V	04222	GC105A330J
A14C104	281-0819-00			CAP,FXD,CER DI:33 PF,5%,50V	04222	GC105A330J
A14C110	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C112	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C300	283-0059-00			CAP,FXD,CER DI:1UF,+80-20%,50V	31433	C330C105M5R5CA
A14C302	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C304	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C310	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V	04222	MA101A101KAA
A14C312	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C314	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C316	281-0814-00			CAP,FXD,CER DI:100 PF,10%,100V	04222	MA101A101KAA
A14C318	281-0774-00			CAP,FXD,CER DI:0.022MFD,20%,100V	04222	MA201E223MAA
A14C320	281-0774-00			CAP,FXD,CER DI:0.022MFD,20%,100V	04222	MA201E223MAA
A14C322	281-0767-00			CAP,FXD,CER DI:330PF,20%,100V	04222	MA106C331MAA
A14C324	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A14C400	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C402	281-0819-00			CAP,FXD,CER DI:33 PF,5%,50V	04222	GC105A330J
A14C404	281-0819-00			CAP,FXD,CER DI:33 PF,5%,50V	04222	GC105A330J
A14C410	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C412	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C500	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C502	281-0819-00			CAP,FXD,CER DI:33 PF,5%,50V	04222	GC105A330J
A14C504	281-0819-00			CAP,FXD,CER DI:33 PF,5%,50V	04222	GC105A330J
A14C506	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C508	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C600	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C602	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C604	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C606	281-0759-00			CAP,FXD,CER DI:22PF,10%,100V	04222	MA101A220KAA
A14C608	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C610	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C612	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C614	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A14C700	119-2534-00			FILTER,RFI:0.0022UF,20%,100V	80009	119-2534-00
A14C702	119-2534-00			FILTER,RFI:0.0022UF,20%,100V	80009	119-2534-00
A14C704	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A14C706	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A14C708	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A14C710	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A14C712	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A14C730	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C732	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C734	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C736	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C750	290-1163-00			CAP,FXD,ELCTLT:4.7UF,20%,100V	80009	290-1163-00
A14C752	290-1163-00			CAP,FXD,ELCTLT:4.7UF,20%,100V	80009	290-1163-00
A14C754	290-1161-00			CAP,FXD,ELCTLT:47UF,20%,25V	80009	290-1161-00
A14C756	290-1161-00			CAP,FXD,ELCTLT:47UF,20%,25V	80009	290-1161-00
A14C758	290-1161-00			CAP,FXD,ELCTLT:47UF,20%,25V	80009	290-1161-00
A14C760	290-1161-00			CAP,FXD,ELCTLT:47UF,20%,25V	80009	290-1161-00
A14C762	290-1161-00			CAP,FXD,ELCTLT:47UF,20%,25V	80009	290-1161-00
A14C770	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C772	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C774	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14C776	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A14CR100	152-0939-00			SEMICOND DVC,DI:DUAL,100MA,20V	80009	152-0939-00
A14CR300	152-0832-00			SEMICOND DVC,DI:SW,SI,50V,0.12A,DO-34	80009	152-0832-00
A14CR302	152-0939-00			SEMICOND DVC,DI:DUAL,100MA,20V	80009	152-0939-00
A14CR304	152-0939-00			SEMICOND DVC,DI:DUAL,100MA,20V	80009	152-0939-00
A14CR600	152-0322-00			SEMICOND DVC,DI:SCHOTTKY,SI,15V,1.2PF,DO-35	50434	5082-2672
A14DL800	119-2548-00			DELAY LINE,ELEC:60NS,SIP4	80009	119-2548-00
A14F700	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A14F702	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A14J122	131-2942-01			CONN,RCPT,ELEC:HEADER,ANGLE,2 X 13	80009	131-2942-01
A14J330	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 2)	22526	48283-029
A14J710	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 3)	22526	48283-029
A14K300	148-0157-00			RELAY,REED:500 OHM,5V	80009	148-0157-00
A14P160	131-3137-00			CONN,PLUG,ELEC:DIN,3 X 32,MALE,0.1 SPACING	80009	131-3137-00
A14P161	131-3865-00			CONN,RCPT,ELEC:HDR,RTANG,2 X 10,0.1 SPACING	80009	131-3865-00
A14P710	131-4311-00			BUS,CONDUCTOR:WHITE,SHUNT ASSY	80009	131-4311-00
A14Q300	151-0347-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7951
A14Q302	151-0350-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS6700
A14Q304	151-0350-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS6700
A14Q306	151-0347-00			TRANSISTOR:NPN,SI,TO-92	04713	SPS7951
A14Q600	151-0876-00			TRANSISTOR:NPN,SI	TK00I	2SC2636T
A14Q602	151-0876-00			TRANSISTOR:NPN,SI	TK00I	2SC2636T
A14Q604	151-0877-00			TRANSISTOR:PNP,SI	TK00I	2SA1254B
A14Q606	151-0354-00			TRANSISTOR:PNP,SI,TO-78	32293	ITS-1200-A
A14Q608	151-0876-00			TRANSISTOR:NPN,SI	TK00I	2SC2636T
A14Q800	151-0776-00			TRANSISTOR:NPN,SI	80009	151-0776-00
A14Q840	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A14R100	307-1357-00			RES,FXD,FILM:10,0K OHM X 2,0.1%,0.063W	80009	307-1357-00
A14R104	326-0877-00			RES,FXD,FILM:62K OHM,1%,0.166W	80009	326-0877-00
A14R106	326-0008-00			RES,FXD,FILM:300 OHM,1%,0.166W	80009	326-0008-00
A14R107	311-2380-00			RES,VAR,NONWW:TRMR,500 OHM,20%,0.5W	80009	311-2380-00
A14R110	307-1515-00			RES,NTWK,FXD FI:(10)180-1K OHM,0.1%,125W	80009	307-1515-00
A14R112	313-0100-00			RES,FXD,FILM:10 OHM,5%,0.166W	80009	313-0100-00
A14R114	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A14R116	313-0104-00			RES,FXD,FILM:100K OHM,5%,0.166W	80009	313-0104-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A14R118	326-0021-00			RES,FXD,FILM:10K OHM,1%,0.166W	80009	326-0021-00
A14R120	326-0021-00			RES,FXD,FILM:10K OHM,1%,0.166W	80009	326-0021-00
A14R122	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A14R130	326-0871-00			RES,FXD,FILM:6.8K OHM,1%,0.166W	80009	326-0871-00
A14R132	311-2381-00			RES,VAR,NONWW:TRMR,1K OHM,20%,0.5W	80009	311-2381-00
A14R134	326-0871-00			RES,FXD,FILM:6.8K OHM,1%,0.166W	80009	326-0871-00
A14R136	326-0027-00			RES,FXD,FILM:100K OHM,1%,0.166W	80009	326-0027-00
A14R138	326-0871-00			RES,FXD,FILM:6.8K OHM,1%,0.166W	80009	326-0871-00
A14R200	307-1357-00			RES,FXD,FILM:10,0K OHM X 2,0.1%,0.063W	80009	307-1357-00
A14R202	326-0394-00			RES,FXD,FILM:124K OHM,1%,0.166W	80009	326-0394-00
A14R204	326-0877-00			RES,FXD,FILM:62K OHM,1%,0.166W	80009	326-0877-00
A14R206	326-0008-00			RES,FXD,FILM:300 OHM,1%,0.166W	80009	326-0008-00
A14R207	311-2380-00			RES,VAR,NONWW:TRMR,500 OHM,20%,0.5W	80009	311-2380-00
A14R210	307-1515-00			RES,NTWK,FXD FI:(10)180-1K OHM,0.1%,125W	80009	307-1515-00
A14R212	313-0100-00			RES,FXD,FILM:10 OHM,5%,0.166W	80009	313-0100-00
A14R230	326-0871-00			RES,FXD,FILM:6.8K OHM,1%,0.166W	80009	326-0871-00
A14R232	311-2381-00			RES,VAR,NONWW:TRMR,1K OHM,20%,0.5W	80009	311-2381-00
A14R234	326-0871-00			RES,FXD,FILM:6.8K OHM,1%,0.166W	80009	326-0871-00
A14R236	326-0027-00			RES,FXD,FILM:100K OHM,1%,0.166W	80009	326-0027-00
A14R238	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A14R238	326-0871-00			RES,FXD,FILM:6.8K OHM,1%,0.166W	80009	326-0871-00
A14R300	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A14R302	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A14R304	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A14R306	325-0418-00			RES,FXD,FILM:9K OHM,0.05%,0.6W	TK00D	MCY9K0000A
A14R308	325-0416-00			RES,FXD,FILM:1K OHM,0.05%,0.6W	TK00D	MCY1K0000A
A14R310	326-0191-00			RES,FXD,FILM:953 OHM,1%,0.166W	S5518	CRB20R65FY953OHM
A14R312	307-1515-00			RES,NTWK,FXD FI:(10)180-1K OHM,0.1%,125W	80009	307-1515-00
A14R314	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A14R316	313-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.166W	80009	313-0682-00
A14R318	313-0682-00			RES,FXD,FILM:6.8K OHM,5%,0.166W	80009	313-0682-00
A14R320	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A14R324	313-0221-00			RES,FXD,FILM:220 OHM,5%,0.166W	80009	313-0221-00
A14R326	313-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.166W	80009	313-0222-00
A14R330	313-0271-00			RES,FXD,FILM:270 OHM,5%,0.166W	80009	313-0271-00
A14R332	313-0221-00			RES,FXD,FILM:220 OHM,5%,0.166W	80009	313-0221-00
A14R332	313-0271-00			RES,FXD,FILM:270 OHM,5%,0.166W	80009	313-0271-00
A14R334	313-0471-00			RES,FXD,FILM:470 OHM,5%,0.166W	80009	313-0471-00
A14R336	313-0223-00			RES,FXD,FILM:22K OHM,5%,0.166W	80009	313-0223-00
A14R338	325-0418-00			RES,FXD,FILM:9K OHM,0.05%,0.6W	TK00D	MCY9K0000A
A14R340	325-0416-00			RES,FXD,FILM:1K OHM,0.05%,0.6W	TK00D	MCY1K0000A
A14R342	313-0470-00			RES,FXD,FILM:47 OHM,5%,0.166W	80009	313-0470-00
A14R344	313-0221-00			RES,FXD,FILM:220 OHM,5%,0.166W	80009	313-0221-00
A14R360	321-0281-07			RES,FXD,FILM:8.25K OHM,0.1%,0.125W,TC=T9	07716	CEAE82500B
A14R362	321-0220-07			RES,FXD,FILM:1.91K OHM,0.1%,0.125W	S5518	CRB25BZ1.91KOHM
A14R364	311-2379-00			RES,VAR,NONWW:TRMR,200 OHM,20%,0.5W	80009	311-2379-00
A14R366	307-1357-00			RES,FXD,FILM:10,0K OHM X 2,0.1%,0.063W	80009	307-1357-00
A14R368	313-0105-00			RES,FXD,FILM:1M OHM,5%,0.166W	80009	313-0105-00
A14R380	326-0021-00			RES,FXD,FILM:10K OHM,1%,0.166W	80009	326-0021-00
A14R382	326-0016-00			RES,FXD,FILM:2K OHM,1%,0.166W	80009	326-0016-00
A14R400	326-0024-00			RES,FXD,FILM:22K OHM,1%,0.166W	80009	326-0024-00
A14R402	326-0406-00			RES,FXD,FILM:165K OHM,1%,0.166W	80009	326-0406-00
A14R404	326-0021-00			RES,FXD,FILM:10K OHM,1%,0.166W	80009	326-0021-00
A14R406	307-1516-00			RES,NTWK,FXD FI:(5)80-1.6K OHM,1%,0.125W	80009	307-1516-00
A14R500	326-0024-00			RES,FXD,FILM:22K OHM,1%,0.166W	80009	326-0024-00
A14R502	326-0406-00			RES,FXD,FILM:165K OHM,1%,0.166W	80009	326-0406-00
A14R504	326-0021-00			RES,FXD,FILM:10K OHM,1%,0.166W	80009	326-0021-00
A14R506	307-1516-00			RES,NTWK,FXD FI:(5)80-1.6K OHM,1%,0.125W	80009	307-1516-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A14R510	326-0017-00			RES,FXD,FILM:2.4K OHM,1%,0.166W	80009	326-0017-00
A14R512	326-0027-00			RES,FXD,FILM:100K OHM,1%,0.166W	80009	326-0027-00
A14R514	313-0914-00			RES,FXD,FILM:910K OHM,5%,0.166W	80009	313-0914-00
A14R516	311-2384-00			RES,VAR,NONWW:TRMR,20K OHM,20%,0.5W	80009	311-2384-00
A14R518	326-0314-00			RES,FXD,FILM:18.2K OHM,1%,0.166W,TC=TO	80009	326-0314-00
A14R520	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A14R522	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A14R600	313-0111-00			RES,FXD,FILM:110 OHM 5%,0.166W	S5518	R20T29J1100HM
A14R602	313-0181-00			RES,FXD,FILM:180 OHM,5%,0.166W	80009	313-0181-00
A14R604	313-0201-00			RES,FXD,FILM:200 OHM,5%,0.166W	80009	313-0201-00
A14R606	301-0102-00			RES,FXD,CMPSN:1K OHM,5%,0.50W	19701	5053CX1K000J
A14R608	313-0201-00			RES,FXD,FILM:200 OHM,5%,0.166W	80009	313-0201-00
A14R610	313-0392-00			RES,FXD,FILM:3.9K OHM,5%,0.166W	80009	313-0392-00
A14R612	313-0122-00			RES,FXD,FILM:1.2K OHM,5%,0.166W	80009	313-0122-00
A14R614	313-0100-00			RES,FXD,FILM:10 OHM,5%,0.166W	80009	313-0100-00
A14R616	313-0242-00			RES,FXD,FILM:2.4K OHM,5%,0.166W	80009	313-0242-00
A14R618	313-0272-00			RES,FXD,FILM:2.7K OHM,5%,0.166W	80009	313-0272-00
A14R620	326-0010-00			RES,FXD,FILM:470 OHM,1%,0.166W	80009	326-0010-00
A14R622	326-0010-00			RES,FXD,FILM:470 OHM,1%,0.166W	80009	326-0010-00
A14R624	326-0019-00			RES,FXD,FILM:4.7K OHM,1%,0.166W	80009	326-0019-00
A14R626	313-0391-00			RES,FXD,FILM:390 OHM,5%,0.166W	80009	313-0391-00
A14R628	301-0202-00			RES,FXD,FILM:2K OHM,5%,0.5W	19701	5053CX2K000J
A14R630	326-1121-00			RES,FXD,FILM:1800HM,1%,0.166W	80009	326-1121-00
A14R632	313-0202-00			RES,FXD,FILM:2K OHM,5%,0.166W	80009	313-0202-00
A14R700	313-0751-00			RES,FXD,FILM:750 OHM,5%,0.166W	80009	313-0751-00
A14R702	313-0751-00			RES,FXD,FILM:750 OHM,5%,0.166W	80009	313-0751-00
A14R800	307-1355-00			RES NTWK,FXD,FI:(6) 4.7K OHM,5%,0.125W	80009	307-1355-00
A14R801	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A14R802	307-1355-00			RES NTWK,FXD,FI:(6) 4.7K OHM,5%,0.125W	80009	307-1355-00
A14R804	307-1355-00			RES NTWK,FXD,FI:(6) 4.7K OHM,5%,0.125W	80009	307-1355-00
A14R806	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A14R808	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A14R812	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A14R814	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A14R816	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A14R818	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A14R820	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A14R822	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A14R826	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A14R828	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A14R830	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A14R832	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A14R834	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A14R836	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A14R838	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A14R840	313-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.166W	80009	313-0332-00
A14R844	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A14R846	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A14R848	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A14R850	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A14R852	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A14R890	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A14R892	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A14T102	326-0394-00			RES,FXD,FILM:124K OHM,1%,0.166W	80009	326-0394-00
A14TP10	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A14TP20	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A14TP30	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A14TP40	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A14TP100	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A14TP110	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A14TP120	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A14TP200	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A14TP210	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A14TP300	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A14TP330	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A14TP350	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A14TP360	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A14TP370	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A14TP400	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A14TP500	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A14TP510	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A14TP520	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A14TP600	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A14TP700	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A14TP710	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A14TP720	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A14TP730	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A14TP740	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A14TP750	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A14TP760	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A14U100	156-0515-00			MICROCKT,DGTL:CMOS,TRIPLE 2-CHAN MUX	02735	CD4053BF
A14U110	156-3036-00			MICROCKT,LINEAR:DUAL,PRECISION OP AMP	TK00T	LT1013CN8
A14U120	156-3558-00			MICROCKT,LINEAR:CMOS DUAL 12 BIT,D/A CONV	TK0AC	AD7547JN 24 DIP
A14U130	156-3036-00			MICROCKT,LINEAR:DUAL,PRECISION OP AMP	TK00T	LT1013CN8
A14U140	156-1200-01			MICROCKT,LINEAR:OPNL AMPL,QUAD BIFET	80009	156-1200-01
A14U150	156-0513-00			MICROCKT,DGTL:CMOS,8-CHANNEL MUX	04713	MC14051BCL
A14U160	156-0513-00			MICROCKT,DGTL:CMOS,8-CHANNEL MUX	04713	MC14051BCL
A14U200	156-1200-01			MICROCKT,LINEAR:OPNL AMPL,QUAD BIFET	80009	156-1200-01
A14U210	156-0513-00			MICROCKT,DGTL:CMOS,8-CHANNEL MUX	04713	MC14051BCL
A14U220	156-0513-00			MICROCKT,DGTL:CMOS,8-CHANNEL MUX	04713	MC14051BCL
A14U300	156-3559-00			MICROCKT,LINEAR:VOLTAGE REFERENCE	TK0AC	AD588AD 16 DIP
A14U310	156-0515-00			MICROCKT,DGTL:CMOS,TRIPLE 2-CHAN MUX	02735	CD4053BF
A14U320	156-3036-00			MICROCKT,LINEAR:DUAL,PRECISION OP AMP	TK00T	LT1013CN8
A14U330	156-0513-00			MICROCKT,DGTL:CMOS,8-CHANNEL MUX	04713	MC14051BCL
A14U340	156-0513-00			MICROCKT,DGTL:CMOS,8-CHANNEL MUX	04713	MC14051BCL
A14U350	156-2795-00			MICROCKT,LINEAR:OPERATIONAL PRECISION	TK0191	156-2795-00
A14U360	156-3036-00			MICROCKT,LINEAR:DUAL,PRECISION OP AMP	TK00T	LT1013CN8
A14U400	156-1815-00			MICROCKT,DGTL:DA CONVERTER DUAL	80009	156-1815-00
A14U410	156-1200-01			MICROCKT,LINEAR:OPNL AMPL,QUAD BIFET	80009	156-1200-01
A14U420	156-0513-00			MICROCKT,DGTL:CMOS,8-CHANNEL MUX	04713	MC14051BCL
A14U430	156-0513-00			MICROCKT,DGTL:CMOS,8-CHANNEL MUX	04713	MC14051BCL
A14U440	156-1200-01			MICROCKT,LINEAR:OPNL AMPL,QUAD BIFET	80009	156-1200-01
A14U500	156-1815-00			MICROCKT,DGTL:DA CONVERTER DUAL	80009	156-1815-00
A14U510	156-1200-01			MICROCKT,LINEAR:OPNL AMPL,QUAD BIFET	80009	156-1200-01
A14U520	156-0513-00			MICROCKT,DGTL:CMOS,8-CHANNEL MUX	04713	MC14051BCL
A14U530	156-0513-00			MICROCKT,DGTL:CMOS,8-CHANNEL MUX	04713	MC14051BCL
A14U800	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A14U810	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A14U820	156-0469-00			MICROCKT,DGTL:3-LINE TO 8-LINE DECODER	01295	SN74LS138N
A14U830	156-0469-00			MICROCKT,DGTL:3-LINE TO 8-LINE DECODER	01295	SN74LS138N
A14U840	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A14U850	156-0391-00			MICROCKT,DGTL:LSTTL,HEX D TYPE FF W/CLEAR	04713	74LS174(N OR J)
A14U860	156-0391-00			MICROCKT,DGTL:LSTTL,HEX D TYPE FF W/CLEAR	04713	74LS174(N OR J)
A14U870	156-0865-00			MICROCKT,DGTL:OCTAL D FF W/CLR	01295	SN74LS273 N OR J
A14U880	156-0874-00			MICROCKT,DGTL:8-BIT ADDRESSABLE LATCHES	01295	SN74LS259N
A14U890	156-0382-00			MICROCKT,DGTL:QUAD 2-INP NAND GATE	01295	SN74LS00(N OR J)

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A14U892	156-0479-00			MICROCKT,DGTL:QUAD 2-INP OR GATE	01295	SN74LS32(N OR J)
A14U910	119-1671-00			HYBRID CIRCUIT:INLINE BLOCK	80009	119-1671-00
A14VR700	152-0127-02			SEMICOND DVC,DI:ZEN,SI,7.5V,5%,0.5W	80009	152-0127-02
A14VR702	152-0127-02			SEMICOND DVC,DI:ZEN,SI,7.5V,5%,0.5W	80009	152-0127-02
A18	671-0804-00			CIRCUIT BD ASSY:A/D	80009	671-0804-00
A18C20	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A18C22	290-1084-00			CAP,FXD,ELCTLT:100UF,20%,16V	80009	290-1084-00
A18C30	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A18C32	290-1084-00			CAP,FXD,ELCTLT:100UF,20%,16V	80009	290-1084-00
A18C40	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A18C42	290-1161-00			CAP,FXD,ELCTLT:47UF,20%,25V	80009	290-1161-00
A18C50	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A18C52	290-1161-00			CAP,FXD,ELCTLT:47UF,20%,25V	80009	290-1161-00
A18C60	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A18C62	290-1084-00			CAP,FXD,ELCTLT:100UF,20%,16V	80009	290-1084-00
A18C70	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A18C72	290-1084-00			CAP,FXD,ELCTLT:100UF,20%,16V	80009	290-1084-00
A18C100	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C102	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C104	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A18C106	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C108	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C110	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C120	281-0258-00			CAP,VAR,CER DI:3.3-20.5PF,250V	80009	281-0258-00
A18C123	283-0906-00			CAP,FXD,CER DI:2PF,+/-0.25PF,50V	S4431	RPE110C0G020C50
A18C201	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C210	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C211	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C212	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C214	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C215	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C220	290-1007-00			CAP,FXD,ELCTLT:22UF,20%,16V	80009	290-1007-00
A18C230	290-1084-00			CAP,FXD,ELCTLT:100UF,20%,16V	80009	290-1084-00
A18C232	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C234	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C236	290-1007-00			CAP,FXD,ELCTLT:22UF,20%,16V	80009	290-1007-00
A18C238	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C240	290-1007-00			CAP,FXD,ELCTLT:22UF,20%,16V	80009	290-1007-00
A18C242	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C244	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C246	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C248	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C250	290-1007-00			CAP,FXD,ELCTLT:22UF,20%,16V	80009	290-1007-00
A18C251	290-1007-00			CAP,FXD,ELCTLT:22UF,20%,16V	80009	290-1007-00
A18C252	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C254	290-1007-00			CAP,FXD,ELCTLT:22UF,20%,16V	80009	290-1007-00
A18C256	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C262	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C264	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C266	290-1007-00			CAP,FXD,ELCTLT:22UF,20%,16V	80009	290-1007-00
A18C300	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A18C301	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C302	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A18C303	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C304	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A18C306	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A18C310	290-1007-00			CAP,FXD,ELCTLT:22UF,20%,16V	80009	290-1007-00
A18C354	290-1007-00			CAP,FXD,ELCTLT:22UF,20%,16V	80009	290-1007-00
A18C356	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A18C400	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A18C402	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C404	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C406	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A18C408	290-1007-00			CAP,FXD,ELCTLT:22UF,20%,16V	80009	290-1007-00
A18C450	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A18C452	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A18C454	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A18C456	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A18C458	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A18C460	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A18C462	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A18C470	283-0177-00			CAP,FXD,CER DI:1UF,+80-20%,25V	04222	SR305E105ZAA
A18C501	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C530	290-1084-00			CAP,FXD,ELCTLT:100UF,20%,16V	80009	290-1084-00
A18C532	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C534	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C536	290-1007-00			CAP,FXD,ELCTLT:22UF,20%,16V	80009	290-1007-00
A18C538	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C540	290-1007-00			CAP,FXD,ELCTLT:22UF,20%,16V	80009	290-1007-00
A18C542	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C544	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C546	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C548	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C552	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C554	290-1007-00			CAP,FXD,ELCTLT:22UF,20%,16V	80009	290-1007-00
A18C556	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C562	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C564	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C566	290-1007-00			CAP,FXD,ELCTLT:22UF,20%,16V	80009	290-1007-00
A18C601	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C630	290-1084-00			CAP,FXD,ELCTLT:100UF,20%,16V	80009	290-1084-00
A18C632	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C634	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C636	290-1007-00			CAP,FXD,ELCTLT:22UF,20%,16V	80009	290-1007-00
A18C638	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C640	290-1007-00			CAP,FXD,ELCTLT:22UF,20%,16V	80009	290-1007-00
A18C642	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C644	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C646	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C648	290-1007-00			CAP,FXD,ELCTLT:22UF,20%,16V	80009	290-1007-00
A18C650	290-1007-00			CAP,FXD,ELCTLT:22UF,20%,16V	80009	290-1007-00
A18C651	290-1007-00			CAP,FXD,ELCTLT:22UF,20%,16V	80009	290-1007-00
A18C652	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C654	290-1007-00			CAP,FXD,ELCTLT:22UF,20%,16V	80009	290-1007-00
A18C656	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C662	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C664	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C666	290-1007-00			CAP,FXD,ELCTLT:22UF,20%,16V	80009	290-1007-00
A18C700	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C701	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C702	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C703	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C704	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A18C706	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C707	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C708	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C711	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C713	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C750	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C751	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C752	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C753	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C754	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C755	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18C756	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C757	290-1007-00			CAP,FXD,ELCTLT:22UF,20%,16V	80009	290-1007-00
A18C758	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C759	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C800	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C802	290-1165-00			CAP,FXD,ELCTLT:10UF,20%,25V	80009	290-1165-00
A18C810	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C812	290-1165-00			CAP,FXD,ELCTLT:10UF,20%,25V	80009	290-1165-00
A18C820	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C822	290-1165-00			CAP,FXD,ELCTLT:10UF,20%,25V	80009	290-1165-00
A18C830	290-1165-00			CAP,FXD,ELCTLT:10UF,20%,25V	80009	290-1165-00
A18C831	290-1165-00			CAP,FXD,ELCTLT:10UF,20%,25V	80009	290-1165-00
A18C850	281-0812-00			CAP,FXD,CER DI:1000PF,10%,100V	04222	MA101C102KAA
A18C852	290-1007-00			CAP,FXD,ELCTLT:22UF,20%,16V	80009	290-1007-00
A18C854	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A18C856	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A18C860	290-1007-00			CAP,FXD,ELCTLT:22UF,20%,16V	80009	290-1007-00
A18C900	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C901	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C902	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C903	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C904	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C905	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C906	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C907	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C908	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C909	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C910	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A18C911	283-0024-00			CAP,FXD,CER DI:0.1UF,+80-20%,50V	04222	SR215C104MAA
A18CR304	152-0322-00			SEMICOND DVC,DI:SCHOTTKY,SI,15V,1.2PF,DO-35	50434	5082-2672
A18CR460	152-0832-00			SEMICOND DVC,DI:SW,SI,50V,0.12A,DO-34	80009	152-0832-00
A18CR472	152-0832-00			SEMICOND DVC,DI:SW,SI,50V,0.12A,DO-34	80009	152-0832-00
A18CR850	152-0832-00			SEMICOND DVC,DI:SW,SI,50V,0.12A,DO-34	80009	152-0832-00
A18CR852	152-0832-00			SEMICOND DVC,DI:SW,SI,50V,0.12A,DO-34	80009	152-0832-00
A18DL900	119-2535-00			DELAY LINE,ELEC:6NS,100 OHM,SIP3	80009	119-2535-00
A18DL902	119-2536-00			DELAY LINE,ELEC:7NS,100 OHM,SIP4	80009	119-2536-00
A18DL904	119-1890-00			DELAY LINE,ELEC:5NS,INPUT 50/OUTPUT	80009	119-1890-00
A18DL906	119-2640-00			DELAY LINE,ELEC:1.0NS,100 OHM,SIP3	TK0B0	FDA1010
A18DL908	119-2537-00			DELAY LINE,ELEC:6NS,100 OHM,SIP4	80009	119-2537-00
A18DL910	119-1890-00			DELAY LINE,ELEC:5NS,INPUT 50/OUTPUT	80009	119-1890-00
A18DL912	119-2536-00			DELAY LINE,ELEC:7NS,100 OHM,SIP4	80009	119-2536-00
A18DL914	119-2538-00			DELAY LINE,ELEC:8NS,100 OHM,SIP4	80009	119-2538-00
A18DL916	119-2539-00			DELAY LINE,ELEC:5NS,100 OHM,SIP4	80009	119-2539-00
A18H400	214-4013-00			HT SK,MICROCKT:DIP16,ALUMINUM	TK00W	SOH5802
A18H852	214-3729-00			HEAT SINK:	80009	214-3729-00
A18J123	131-3849-00			CONN,RCPT,ELEC:COAX,FINGER LOCK	80009	131-3849-00
A18J150	131-3848-00			CONN,RCPT,ELEC:COAX,RTANG SNAP ON	80009	131-3848-00

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A18J326	131-3849-00			CONN,RCPT,ELEC:COAX,FINGER LOCK	80009	131-3849-00
A18J400	131-3848-00			CONN,RCPT,ELEC:COAX,RTANG SNAP ON	80009	131-3848-00
A18L123	108-1458-00			COIL,RF:FXD,33NH,+/-2NH	80009	108-1458-00
A18L230	108-1012-00			COIL,RF:FIXED,4.7UH	80009	108-1012-00
A18L300	108-0538-01			COIL,RF:FIXED,2.7UH	80009	108-0538-01
A18L302	108-0538-01			COIL,RF:FIXED,2.7UH	80009	108-0538-01
A18L530	108-1012-00			COIL,RF:FIXED,4.7UH	80009	108-1012-00
A18L630	108-1012-00			COIL,RF:FIXED,4.7UH	80009	108-1012-00
A18L757	108-1012-00			COIL,RF:FIXED,4.7UH	80009	108-1012-00
A18P180	131-3137-00			CONN,PLUG,ELEC:DIN,3 X 32,MALE,0.1 SPACING	80009	131-3137-00
A18Q450	151-0871-00			TRANSISTOR:NPN,SI,TO-92B	TK00J	2SC2570A
A18Q452	151-0871-00			TRANSISTOR:NPN,SI,TO-92B	TK00J	2SC2570A
A18Q454	151-0871-00			TRANSISTOR:NPN,SI,TO-92B	TK00J	2SC2570A
A18Q460	151-0719-00			TRANSISTOR:PNP,SI,TO-92B	04713	SPS8226 (MPSH81)
A18Q462	151-0271-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8236
A18Q464	151-0271-00			TRANSISTOR:PNP,SI,TO-92	04713	SPS8236
A18Q810	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A18Q850	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A18Q852	151-0562-00			TRANSISTOR:PNP,SI,PWR	TK0191	151-0562-00
A18R100	326-0085-00			RES,FXD,FILM:75 OHM,1%,0.166W	S5518	CRB20R65FY75 OHM
A18R102	322-3083-00			RES,FXD,FILM:71.5 OHM,1%,0.2W,TC=T0	57668	CRB20 FXE 71E5
A18R110	311-2386-00			RES,VAR,NONWW:TRMR,50 OHM,20%,0.5W	S4431	3321N-1-500
A18R120	313-0100-00			RES,FXD,FILM:10 OHM,5%,0.166W	80009	313-0100-00
A18R150	321-1773-00			RES,FXD,FILM:24.9 OHM,0.1%,0.125W,TC=T9	S5518	CRB25BZ24.9OHM
A18R200	321-0097-07			RES,FXD,FILM:100 OHM,0.1%,0.125W,TC=T9	91637	CMF55116C100R0B
A18R202	321-0126-07			RES,FXD,FILM:200 OHM,0.1%,0.125W,TC=T9	19701	5033RE200R0B
A18R204	313-0510-00			RES,FXD,FILM:51 OHM,5%,0.166W	80009	313-0510-00
A18R206	313-0510-00			RES,FXD,FILM:51 OHM,5%,0.166W	80009	313-0510-00
A18R210	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A18R214	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A18R250	311-1981-01			RES,VAR,NONWW:20K OHM,20%,0.5W	80009	311-1981-01
A18R252	307-1346-00			RES NTWK,FXD,FI:(6),402K,2K,1K,240,44.8K	80009	307-1346-00
A18R260	311-1981-01			RES,VAR,NONWW:20K OHM,20%,0.5W	80009	311-1981-01
A18R262	307-1347-00			RES NTWK,FXD,FI:(6),402K,2K,240,1K,3.8K,40K	80009	307-1347-00
A18R300	307-0488-01			RES NTWK,FXD,FI:(5)100 OHM,10%,0.125W	80009	307-0488-01
A18R301	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A18R302	326-0280-00			RES,FXD,FILM:8.06K OHM,1%,0.166W	S5518	CRB20R65FY8.06K
A18R304	325-0417-00			RES,FXD,FILM:8K OHM,0.02%,0.6W	TK00D	MCY8K0000Q
A18R306	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A18R308	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A18R310	326-0003-00			RES,FXD,FILM:100 OHM,1%,0.166W	80009	326-0003-00
A18R312	325-0415-00			RES,FXD,FILM:100 OHM,0.02%,0.6W	TK00D	MCY100R00Q
A18R350	325-0418-00			RES,FXD,FILM:9K OHM,0.05%,0.6W	TK00D	MCY9K0000A
A18R352	325-0416-00			RES,FXD,FILM:1K OHM,0.05%,0.6W	TK00D	MCY1K0000A
A18R354	326-0189-00			RES,FXD,FILM:909 OHM,1%,0.166W	S5518	CRB20R65FY909OHM
A18R356	313-0201-00			RES,FXD,FILM:200 OHM,5%,0.166W	80009	313-0201-00
A18R400	321-1759-07			RES,FXD,FILM:50 OHM,0.1%,0.125W	S5518	CRB25 BZ 50 OHM
A18R402	313-0751-00			RES,FXD,FILM:750 OHM,5%,0.166W	80009	313-0751-00
A18R450	326-0005-00			RES,FXD,FILM:160 OHM,1%,0.166W	80009	326-0005-00
A18R452	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A18R454	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A18R460	313-0622-00			RES,FXD,FILM:6.2K OHM,5%,0.166W	S5518	R20T29J6.2KOHM
A18R462	313-0822-00			RES,FXD,FILM:8.2K OHM,5%,0.166W	80009	313-0822-00
A18R464	313-0510-00			RES,FXD,FILM:51 OHM,5%,0.166W	80009	313-0510-00
A18R466	313-0821-00			RES,FXD,FILM:820 OHM,5%,0.166W	80009	313-0821-00
A18R468	326-0038-00			RES,FXD,FILM:3.3 OHM,1%,0.166W	S5518	CRB20R65FY3.3OHM
A18R470	313-0822-00			RES,FXD,FILM:8.2K OHM,5%,0.166W	80009	313-0822-00
A18R472	313-0622-00			RES,FXD,FILM:6.2K OHM,5%,0.166W	S5518	R20T29J6.2KOHM

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A18R474	313-0510-00			RES,FXD,FILM:51 OHM,5%,0.166W	80009	313-0510-00
A18R476	313-0821-00			RES,FXD,FILM:820 OHM,5%,0.166W	80009	313-0821-00
A18R478	326-0038-00			RES,FXD,FILM:3.3 OHM,1%,0.166W	S5518	CRB20R65FY3.3OHM
A18R480	313-0510-00			RES,FXD,FILM:51 OHM,5%,0.166W	80009	313-0510-00
A18R482	313-0510-00			RES,FXD,FILM:51 OHM,5%,0.166W	80009	313-0510-00
A18R484	326-0039-00			RES,FXD,FILM:4.7 OHM,1%,0.166W	S5518	CRB20R65FY4.7OHM
A18R486	326-0039-00			RES,FXD,FILM:4.7 OHM,1%,0.166W	S5518	CRB20R65FY4.7OHM
A18R500	315-0360-00			RES,FXD,FILM:36 OHM,5%,0.25W	19701	5043CX36R00J
A18R502	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A18R504	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A18R506	313-0103-00			RES,FXD,FILM:10K OHM,5%,0.166W	80009	313-0103-00
A18R550	311-1981-01			RES,VAR,NONWW:20K OHM,20%,0.5W	80009	311-1981-01
A18R552	307-1348-00			RES NTWK,FXD,FI:(6),806K,2K,1K,1.3K,38K,2K	80009	307-1348-00
A18R562	307-1351-00			RES NTWK,FXD,FI:(4),2.2K,1.3K,1K,1K	80009	307-1351-00
A18R600	315-0360-00			RES,FXD,FILM:36 OHM,5%,0.25W	19701	5043CX36R00J
A18R602	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A18R604	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A18R650	311-1981-01			RES,VAR,NONWW:20K OHM,20%,0.5W	80009	311-1981-01
A18R652	307-1350-00			RES NTWK,FXD,FI:(5),806K,2K,1K,1.3K,2K	80009	307-1350-00
A18R652	311-1981-01			RES,VAR,NONWW:20K OHM,20%,0.5W	80009	311-1981-01
A18R660	311-1981-01			RES,VAR,NONWW:20K OHM,20%,0.5W	80009	311-1981-01
A18R662	307-1349-00			RES NTWK,FXD,FI:(6),806K,2K,1.3K,1K,2K,40K	80009	307-1349-00
A18R700	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A18R702	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A18R706	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A18R708	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A18R710	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A18R712	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A18R750	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A18R752	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A18R754	307-0488-01			RES NTWK,FXD,FI:(5)100 OHM,10%,0.125W	80009	307-0488-01
A18R756	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A18R800	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A18R810	326-0021-00			RES,FXD,FILM:10K OHM,1%,0.166W	80009	326-0021-00
A18R812	326-0021-00			RES,FXD,FILM:10K OHM,1%,0.166W	80009	326-0021-00
A18R814	313-0100-00			RES,FXD,FILM:10 OHM,5%,0.166W	80009	313-0100-00
A18R820	326-0021-00			RES,FXD,FILM:10K OHM,1%,0.166W	80009	326-0021-00
A18R822	326-0021-00			RES,FXD,FILM:10K OHM,1%,0.166W	80009	326-0021-00
A18R824	313-0512-00			RES,FXD,FILM:5.1K OHM,5%,0.166W	80009	313-0512-00
A18R850	321-0305-07			RES,FXD,FILM:14.7K OHM,0.1%,0.125W,TC=T9	S5518	CRB25BZ14.7KOHM
A18R852	321-0266-07			RES,FXD,FILM:5.76K OHM,0.1%,0.125W,TC=T9	80009	321-0266-07
A18R854	313-0821-00			RES,FXD,FILM:820 OHM,5%,0.166W	80009	313-0821-00
A18R856	308-0710-00			RES,FXD,WW:0.27 OHM,5%,1W	75042	BW-20-R2700J
A18R858	313-0392-00			RES,FXD,FILM:3.9K OHM,5%,0.166W	80009	313-0392-00
A18R900	313-0510-00			RES,FXD,FILM:51 OHM,5%,0.166W	80009	313-0510-00
A18R902	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A18R904	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A18R906	307-0488-01			RES NTWK,FXD,FI:(5)100 OHM,10%,0.125W	80009	307-0488-01
A18R908	307-0488-01			RES NTWK,FXD,FI:(5)100 OHM,10%,0.125W	80009	307-0488-01
A18R910	307-0488-01			RES NTWK,FXD,FI:(5)100 OHM,10%,0.125W	80009	307-0488-01
A18TP1	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A18TP2	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A18TP3	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A18TP4	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A18TP5	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A18TP6	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A18TP7	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A18TP20	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036

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A18TP30	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A18TP40	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A18TP50	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A18TP60	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A18TP70	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A18TP200	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A18TP250	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A18TP260	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A18TP300	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A18TP302	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A18TP450	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A18TP500	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A18TP550	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A18TP560	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A18TP650	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A18TP660	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A18TP810	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A18TP820	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A18TP850	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A18U100	156-2907-03			MICROCKT,LINEAR:TRACK & HOLD	80009	156-2907-03
A18U150	119-2960-00			HYBRID CIRCUIT:INLINE BLOCK	TK0BT	TB-CR-01
A18U200	155-0290-01			MICROCKT,DGTL:A-D CONVERTER,1V REF VOLTAGE	80009	155-0290-01
A18U210	156-1712-01			MICROCKT,DGTL:M/S FLIP/FLOP,HEX D	TK0AA	MC10H176L
A18U212	156-1712-01			MICROCKT,DGTL:M/S FLIP/FLOP,HEX D	TK0AA	MC10H176L
A18U214	156-1712-01			MICROCKT,DGTL:M/S FLIP/FLOP,HEX D	TK0AA	MC10H176L
A18U250	156-0158-00			MICROCKT,LINEAR:BIPOLAR,DUAL OPNL AMPL	04713	MC1458P1/MC1458U
A18U300	155-0282-00			MICROCKT,DGTL:DGTL-ANALOG CONV M219B	80009	155-0282-00
A18U350	156-2795-00			MICROCKT,LINEAR:OPERATIONAL PRECISION	TK0191	156-2795-00
A18U400	155-0277-00			MICROCKT,LINEAR:SUMMING AMPLIFIER	80009	155-0277-00
A18U450	119-2961-00			HYBRID CIRCUIT:INLINE BLOCK	TK0BT	TB-CRD-01
A18U500	155-0289-01			MICROCKT,DGTL:A-D CONV,0.25V REF VOLTAGE	80009	155-0289-01
A18U550	156-0158-00			MICROCKT,LINEAR:BIPOLAR,DUAL OPNL AMPL	04713	MC1458P1/MC1458U
A18U600	155-0289-01			MICROCKT,DGTL:A-D CONV,0.25V REF VOLTAGE	80009	155-0289-01
A18U650	156-0158-00			MICROCKT,LINEAR:BIPOLAR,DUAL OPNL AMPL	04713	MC1458P1/MC1458U
A18U700	156-1712-01			MICROCKT,DGTL:M/S FLIP/FLOP,HEX D	TK0AA	MC10H176L
A18U702	156-1712-01			MICROCKT,DGTL:M/S FLIP/FLOP,HEX D	TK0AA	MC10H176L
A18U704	156-2749-00			MICROCKT,DGTL:DUAL 3 IN 3 OUT NOR	80009	156-2749-00
A18U706	156-2749-00			MICROCKT,DGTL:DUAL 3 IN 3 OUT NOR	80009	156-2749-00
A18U708	156-1508-00			MICROCKT,DGTL:ECL,6-BIT ADDER	07263	F100180DC
A18U710	156-1512-00			MICROCKT,DGTL:ECL,HEX D FLIP-FLOP	07263	F100151DC
A18U712	156-1512-00			MICROCKT,DGTL:ECL,HEX D FLIP-FLOP	07263	F100151DC
A18U750	156-0542-00			MICROCKT,DGTL:ECL,HEX INVERTER	18324	10189N
A18U752	156-0542-00			MICROCKT,DGTL:ECL,HEX INVERTER	18324	10189N
A18U754	156-0316-00			MICROCKT,DGTL:ECL,QUAD 2-INP ECL TO TTL	04713	MC10125L
A18U756	156-0388-00			MICROCKT,DGTL:DUAL D FLIP-FLOP	01295	SN74LS74 N OR J
A18U800	156-1322-00			MICROCKT,LINEAR:VOLTAGE REF,BIPOLAR,10V	24355	AD40374
A18U810	156-0158-00			MICROCKT,LINEAR:BIPOLAR,DUAL OPNL AMPL	04713	MC1458P1/MC1458U
A18U850	156-0067-00			MICROCKT,LINEAR:BIPOLAR,OPNL AMPL	04713	MC1741CP1
A18U900	156-3291-00			MICROCKT,DGTL:PLUSE MODULATOR	S5407	MCH109
A18U902	156-1519-00			MICROCKT,DGTL:ECL,QUINT 2 OR/NOR	07263	F100102DC
A18U904	156-3040-00			MICROCKT,DGTL:PULSE DRIVER	S5407	MCH103
A18U906	156-1733-00			MICROCKT,DGTL:QUAD OR/NOR GATE	04713	MC10H101PD
A18U908	156-1733-00			MICROCKT,DGTL:QUAD OR/NOR GATE	04713	MC10H101PD
A18U910	156-1733-00			MICROCKT,DGTL:QUAD OR/NOR GATE	04713	MC10H101PD
A18VR400	152-0963-00			SEMICOND DVC,DI:ZENER,SI,2.2V,+/-0.1V,400MW	S5372	HZS2B3
A18W20	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A18W30	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A18XU200	136-0919-00			SKT,PL-IN,ELEK:CHIP CARRIER,68 CONTACT	80009	136-0919-00

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A18XU500	136-0919-00			SKT,PL-IN,ELEK:CHIP CARRIER,68 CONTACT	80009	136-0919-00
A18XU600	136-0919-00			SKT,PL-IN,ELEK:CHIP CARRIER,68 CONTACT	80009	136-0919-00
A22	670-9856-02			CIRCUIT BD ASSY:TRIGGER	80009	670-9856-02
A24	670-9857-02			CIRCUIT BD ASSY:TV TRIGGER (OPTION 05)	80009	670-9857-02
A30	670-9858-01			CIRCUIT BD ASSY:ENVELOPE	TK0191	ORDER BY DESCR
A32	671-0688-01			CIRCUIT BD ASSY:TIME BASE	80009	671-0688-01
A32C10	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A32C20	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A32C30	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A32C40	290-1084-00			CAP,FXD,ELCTLT:100UF,20%,16V	80009	290-1084-00
A32C50	290-1084-00			CAP,FXD,ELCTLT:100UF,20%,16V	80009	290-1084-00
A32C60	290-1084-00			CAP,FXD,ELCTLT:100UF,20%,16V	80009	290-1084-00
A32C116	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C117	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C118	283-0065-00			CAP,FXD,CER DI:0.001UF,5%,50V	59660	0835-591Y5E0102J
A32C120	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C134	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C136	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C137	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C140	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C143	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C144	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C145	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C306	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C310	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C311	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C312	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C313	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C314	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C316	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C317	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C320	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C322	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C324	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C326	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C327	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C328	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C332	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C334	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C341	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C342	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C343	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C344	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C345	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C347	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C400	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C401	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C402	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C403	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C404	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C405	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C406	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA

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A32C407	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C409	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C410	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C411	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C412	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C414	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C415	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C416	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C418	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C419	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C420	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C421	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C422	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C423	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C424	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C425	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C426	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C428	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C430	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C432	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C433	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C435	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C436	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C437	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C438	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C439	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C440	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C441	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C442	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C444	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C446	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C447	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C448	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C450	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C451	283-0168-00			CAP,FXD,CER DI:12PF,5%,100V	05397	C315C120J1G5CA
A32C452	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C453	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C454	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C455	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C456	283-0168-00			CAP,FXD,CER DI:12PF,5%,100V	05397	C315C120J1G5CA
A32C457	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C458	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C459	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C460	290-0536-03			CAP,FXD,ELCTLT:10UF,20%,25V	80009	290-0536-03
A32C461	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A32C462	290-0536-03			CAP,FXD,ELCTLT:10UF,20%,25V	80009	290-0536-03
A32C464	281-0773-00			CAP,FXD,CER DI:0.01UF,10%,100V	04222	MA201C103KAA
A32C465	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C466	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C468	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C470	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C471	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C472	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C473	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C474	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C476	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C478	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A32C762	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A32CR322	152-0327-00			SEMICOND DVC,DI:SIG,SI,100MA,75V,D2X5,BAX13	80009	152-0327-00
A32CR323	152-0327-00			SEMICOND DVC,DI:SIG,SI,100MA,75V,D2X5,BAX13	80009	152-0327-00
A32CR325	152-0322-00			SEMICOND DVC,DI:SCHOTTKY,SI,15V,1.2PF,DO-35	50434	5082-2672
A32CR326	152-0322-00			SEMICOND DVC,DI:SCHOTTKY,SI,15V,1.2PF,DO-35	50434	5082-2672
A32CR762	152-0322-00			SEMICOND DVC,DI:SCHOTTKY,SI,15V,1.2PF,DO-35	50434	5082-2672
A32CR763	152-0322-00			SEMICOND DVC,DI:SCHOTTKY,SI,15V,1.2PF,DO-35	50434	5082-2672
A32J122	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 3)	22526	48283-036
A32J124	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 3)	22526	48283-036
A32J322	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A32J323	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A32J324	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A32J325	131-1003-00			CONN,RCPT,ELEC:CKT BD MT,3 PRONG	80009	131-1003-00
A32J326	131-3849-00			CONN,RCPT,ELEC:COAX,FINGER LOCK (QUANTITY OF 2)	80009	131-3849-00
A32J330	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ (QUANTITY OF 2)	22526	48283-029
A32J400	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL (QUANTITY OF 3)	22526	48283-036
A32J762	131-3849-00			CONN,RCPT,ELEC:COAX,FINGER LOCK	80009	131-3849-00
A32L460	108-0538-01			COIL,RF:FIXED,2.7UH	80009	108-0538-01
A32L462	108-0538-01			COIL,RF:FIXED,2.7UH	80009	108-0538-01
A32P122	131-4311-00			BUS,CONDUCTOR:WHITE,SHUNT ASSY	80009	131-4311-00
A32P134	131-4311-00			BUS,CONDUCTOR:WHITE,SHUNT ASSY	80009	131-4311-00
A32P320	131-3137-00			CONN,PLUG,ELEC:DIN,3 X 32,MALE,0.1 SPACING	80009	131-3137-00
A32P321	131-3137-00			CONN,PLUG,ELEC:DIN,3 X 32,MALE,0.1 SPACING	80009	131-3137-00
A32P400	131-4311-00			BUS,CONDUCTOR:WHITE,SHUNT ASSY	80009	131-4311-00
A32R116	313-0363-00			RES,FXD,FILM:36K OHM,5%,0.166W	80009	313-0363-00
A32R118	313-0363-00			RES,FXD,FILM:36K OHM,5%,0.166W	80009	313-0363-00
A32R120	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A32R132	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A32R134	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A32R302	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A32R310	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A32R312	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A32R314	307-0587-00			RES NTWK,FXD,FI:(7)68 OHM,20%,0.125W	11236	750-81-R68 OHM
A32R316	307-0587-00			RES NTWK,FXD,FI:(7)68 OHM,20%,0.125W	11236	750-81-R68 OHM
A32R318	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A32R320	307-0587-00			RES NTWK,FXD,FI:(7)68 OHM,20%,0.125W	11236	750-81-R68 OHM
A32R322	313-0103-00			RES,FXD,FILM:10K OHM,5%,0.166W	80009	313-0103-00
A32R323	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A32R325	313-0510-00			RES,FXD,FILM:51 OHM,5%,0.166W	80009	313-0510-00
A32R326	307-0587-00			RES NTWK,FXD,FI:(7)68 OHM,20%,0.125W	11236	750-81-R68 OHM
A32R328	307-0587-00			RES NTWK,FXD,FI:(7)68 OHM,20%,0.125W	11236	750-81-R68 OHM
A32R332	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A32R334	307-0587-00			RES NTWK,FXD,FI:(7)68 OHM,20%,0.125W	11236	750-81-R68 OHM
A32R342	307-0594-00			RES NTWK,FXD,FI:(8)220 OHM,2%,0.125W	11236	750-81-R220
A32R344	307-0587-00			RES NTWK,FXD,FI:(7)68 OHM,20%,0.125W	11236	750-81-R68 OHM
A32R345	307-0587-00			RES NTWK,FXD,FI:(7)68 OHM,20%,0.125W	11236	750-81-R68 OHM
A32R400	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A32R401	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A32R402	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A32R403	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A32R405	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A32R406	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A32R407	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A32R408	307-0587-00			RES NTWK,FXD,FI:(7)68 OHM,20%,0.125W	11236	750-81-R68 OHM
A32R409	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A32R410	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A32R413	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A32R415	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A32R416	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A32R417	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A32R419	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A32R420	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A32R421	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A32R422	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A32R423	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A32R424	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A32R425	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A32R430	307-0587-00			RES NTWK,FXD,FI:(7)68 OHM,20%,0.125W	11236	750-81-R68 OHM
A32R431	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A32R432	307-0587-00			RES NTWK,FXD,FI:(7)68 OHM,20%,0.125W	11236	750-81-R68 OHM
A32R433	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A32R434	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A32R435	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A32R439	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A32R441	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A32R444	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A32R445	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A32R448	307-0587-00			RES NTWK,FXD,FI:(7)68 OHM,20%,0.125W	11236	750-81-R68 OHM
A32R449	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A32R451	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A32R452	313-0561-00			RES,FXD,FILM:560 OHM,5%,0.166W	80009	313-0561-00
A32R453	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A32R454	313-0271-00			RES,FXD,FILM:270 OHM,5%,0.166W	80009	313-0271-00
A32R455	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A32R456	313-0752-00			RES,FXD,FILM:7.5K OHM,5%,0.166W	80009	313-0752-00
A32R457	313-0680-00			RES,FXD,FILM:68 OHM,5%,0.166W	80009	313-0680-00
A32R458	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A32R459	313-0561-00			RES,FXD,FILM:560 OHM,5%,0.166W	80009	313-0561-00
A32R460	313-0271-00			RES,FXD,FILM:270 OHM,5%,0.166W	80009	313-0271-00
A32R462	313-0132-00			RES,FXD,FILM:1.3K OHM,5%,0.166W	80009	313-0132-00
A32R464	313-0561-00			RES,FXD,FILM:560 OHM,5%,0.166W	80009	313-0561-00
A32R466	313-0392-00			RES,FXD,FILM:3.9K OHM,5%,0.166W	80009	313-0392-00
A32R468	313-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.166W	80009	313-0332-00
A32R470	307-0587-00			RES NTWK,FXD,FI:(7)68 OHM,20%,0.125W	11236	750-81-R68 OHM
A32R471	313-0222-00			RES,FXD,FILM:2.2K OHM,5%,0.166W	80009	313-0222-00
A32R762	313-0510-00			RES,FXD,FILM:51 OHM,5%,0.166W	80009	313-0510-00
A32S450	260-2353-00			SWITCH,SLIDE:(3)SPST,25MA,25V	80009	260-2353-00
A32TP100	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A32TP102	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A32TP120	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A32TP312	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A32TP400	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A32TP450	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A32TP454	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A32TP455	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A32U116	156-0402-04			MICROCKT,LINEAR:TIMER	80009	156-0402-04
A32U120	156-1895-00			MICROCKT,DGTL:CMOS,PROGRAMMABLE DIVIDER	80009	156-1895-00
A32U134	156-0368-00			MICROCKT,DGTL:ECL,QUAD TTL TO ECL CONV	04713	MC10124L
A32U136	156-0368-00			MICROCKT,DGTL:ECL,QUAD TTL TO ECL CONV	04713	MC10124L
A32U140	156-1640-02			MICROCKT,DGTL:TRIPLE LINE RCVR	80009	156-1640-02
A32U144	156-0316-00			MICROCKT,DGTL:ECL,QUAD 2-INP ECL TO TTL	04713	MC10125L
A32U304	156-0368-00			MICROCKT,DGTL:ECL,QUAD TTL TO ECL CONV	04713	MC10124L
A32U306	156-0368-00			MICROCKT,DGTL:ECL,QUAD TTL TO ECL CONV	04713	MC10124L

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A32U308	156-0759-00			MICROCKT,DGTL:ECL,QUAD 2 INP OR GATE	04713	MC10103 L OR P
A32U310	156-0458-00			MICROCKT,DGTL:ECL,QUAD AND GATE,2-INP	04713	MC10104L
A32U312	156-1712-00			MICROCKT,DGTL:HEX D MASTER-SLAVE FF	04713	MC10H176PD
A32U314	156-1712-00			MICROCKT,DGTL:HEX D MASTER-SLAVE FF	04713	MC10H176PD
A32U316	156-0368-00			MICROCKT,DGTL:ECL,QUAD TTL TO ECL CONV	04713	MC10124L
A32U320	156-2312-00			MICROCKT,DGTL:BINARY COUNTER	80009	156-2312-00
A32U322	156-2312-00			MICROCKT,DGTL:BINARY COUNTER	80009	156-2312-00
A32U324	156-2312-00			MICROCKT,DGTL:BINARY COUNTER	80009	156-2312-00
A32U326	156-2312-00			MICROCKT,DGTL:BINARY COUNTER	80009	156-2312-00
A32U328	156-2312-00			MICROCKT,DGTL:BINARY COUNTER	80009	156-2312-00
A32U330	156-2312-00			MICROCKT,DGTL:BINARY COUNTER	80009	156-2312-00
A32U332	156-2312-00			MICROCKT,DGTL:BINARY COUNTER	80009	156-2312-00
A32U334	156-2312-00			MICROCKT,DGTL:BINARY COUNTER	80009	156-2312-00
A32U340	156-1849-00			MICROCKT,DGTL:ECL,QUAD 2 INPUT OR GATE	04713	MC10H103 PDS
A32U342	156-2740-00			MICROCKT,DGTL:DUAL 3-IN/3 OUT	80009	156-2740-00
A32U344	156-2740-00			MICROCKT,DGTL:DUAL 3-IN/3 OUT	80009	156-2740-00
A32U400	156-2749-00			MICROCKT,DGTL:DUAL 3 IN 3 OUT NOR	80009	156-2749-00
A32U402	156-1733-00			MICROCKT,DGTL:QUAD OR/NOR GATE	04713	MC10H101PD
A32U404	156-1639-02			MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	80009	156-1639-02
A32U405	156-1642-02			MICROCKT,DGTL:TRIPLE 2-3-2 IN OR/NOR GATE	80009	156-1642-02
A32U406	156-2740-00			MICROCKT,DGTL:DUAL 3-IN/3 OUT	80009	156-2740-00
A32U408	156-2749-00			MICROCKT,DGTL:DUAL 3 IN 3 OUT NOR	80009	156-2749-00
A32U410	156-1639-02			MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	80009	156-1639-02
A32U412	156-1874-00			MICROCKT,DGTL:4-BIT UNIV SHIFT REGISTER	04713	MC10H141L/P
A32U414	156-1874-00			MICROCKT,DGTL:4-BIT UNIV SHIFT REGISTER	04713	MC10H141L/P
A32U416	156-1639-02			MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	80009	156-1639-02
A32U418	156-1639-02			MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	80009	156-1639-02
A32U420	156-0182-00			MICROCKT,DGTL:ECL,TRIPLE 2-3-2 INPUT GATE	04713	MC10105P/L
A32U422	156-1674-00			MICROCKT,DGTL:ECL,QUAD 2 INP AND GATE,SCRN	04713	MC10H104LD
A32U424	156-1641-02			MICROCKT,DGTL:ECL,QUAD 2-INPUT NOR GATE	80009	156-1641-02
A32U426	156-1849-00			MICROCKT,DGTL:ECL,QUAD 2 INPUT OR GATE	04713	MC10H103 PDS
A32U428	156-1639-02			MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	80009	156-1639-02
A32U430	156-1639-02			MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	80009	156-1639-02
A32U432	156-1639-02			MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	80009	156-1639-02
A32U434	156-2740-00			MICROCKT,DGTL:DUAL 3-IN/3 OUT	80009	156-2740-00
A32U436	156-2749-00			MICROCKT,DGTL:DUAL 3 IN 3 OUT NOR	80009	156-2749-00
A32U438	156-2740-00			MICROCKT,DGTL:DUAL 3-IN/3 OUT	80009	156-2740-00
A32U440	156-1874-00			MICROCKT,DGTL:4-BIT UNIV SHIFT REGISTER	04713	MC10H141L/P
A32U442	156-1874-00			MICROCKT,DGTL:4-BIT UNIV SHIFT REGISTER	04713	MC10H141L/P
A32U444	156-1874-00			MICROCKT,DGTL:4-BIT UNIV SHIFT REGISTER	04713	MC10H141L/P
A32U446	156-1639-02			MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	80009	156-1639-02
A32U448	156-1849-00			MICROCKT,DGTL:ECL,QUAD 2 INPUT OR GATE	04713	MC10H103 PDS
A32U450	156-3043-00			MICROCKT,DGTL:MULTIPLEXER W/DELAY LINE	S5407	MSH8-005
A32U452	156-1640-02			MICROCKT,DGTL:TRIPLE LINE RCVR	80009	156-1640-02
A32U454	156-1795-00			MICROCKT,DGTL:DUAL 4 TO 1 MUX	04713	MC10H174PD
A32U456	156-1639-02			MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	80009	156-1639-02
A32U458	156-1639-02			MICROCKT,DGTL:ECL,DUAL D MA-SLAVE FF	80009	156-1639-02
A32U460	156-0509-00			MICROCKT,DGTL:8-BIT BINARY,MULT CUR	04713	MC1408L8
A32U470	156-1641-02			MICROCKT,DGTL:ECL,QUAD 2-INPUT NOR GATE	80009	156-1641-02
A32U472	156-1733-00			MICROCKT,DGTL:QUAD OR/NOR GATE	04713	MC10H101PD
A32XU322	136-0252-07			SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
A32XU323	136-0252-07			SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
A32XU324	136-0252-07			SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
A32XU325	136-0252-07			SOCKET,PIN CONN:W/O DIMPLE	22526	75060-012
A34	671-0361-00			CIRCUIT BD ASSY:TIME BASE CONTROL	80009	671-0361-00

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A36	671-0687-00			CIRCUIT BD ASSY:MPU	TK0191	ORDER BY DESCR
A36C10	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A36C20	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A36C30	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A36C40	290-1084-00			CAP,FXD,ELCTLT:100UF,20%,16V	80009	290-1084-00
A36C50	290-1084-00			CAP,FXD,ELCTLT:100UF,20%,16V	80009	290-1084-00
A36C60	290-1084-00			CAP,FXD,ELCTLT:100UF,20%,16V	80009	290-1084-00
A36C70	290-1084-00			CAP,FXD,ELCTLT:100UF,20%,16V	80009	290-1084-00
A36C80	290-1084-00			CAP,FXD,ELCTLT:100UF,20%,16V	80009	290-1084-00
A36C100	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C101	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C102	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C103	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C104	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C105	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C106	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C107	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C108	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C109	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C110	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C112	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C113	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C120	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C122	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C124	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C125	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C126	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C128	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C130	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C200	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C208	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C210	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C214	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C216	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C218	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C220	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C222	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C224	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C228	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C230	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C236	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C238	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C246	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C250	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C254	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C258	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C300	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C302	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C304	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C306	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C308	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C310	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C312	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C316	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C318	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C320	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C322	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A36C324	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C326	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C328	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C330	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C332	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C334	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C336	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C338	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C340	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C342	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C344	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C346	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C350	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C406	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C410	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C414	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C422	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C426	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C430	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C440	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C441	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C442	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36C444	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A36P360	131-3137-00			CONN,PLUG,ELEC:DIN,3 X 32,MALE,0.1 SPACING	80009	131-3137-00
A36P361	131-3137-00			CONN,PLUG,ELEC:DIN,3 X 32,MALE,0.1 SPACING	80009	131-3137-00
A36R100	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A36R102	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A36R104	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A36R106	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A36R108	307-0489-01			RES NTWK,FXD,FI:(7)100 OHM,10%,0.125W	80009	307-0489-01
A36R110	307-0587-00			RES NTWK,FXD,FI:(7)68 OHM,20%,0.125W	11236	750-81-R68 OHM
A36R200	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A36R230	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A36R350	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A36R400	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	32997	4310R-101-472
A36R402	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	32997	4310R-101-472
A36R404	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	32997	4310R-101-472
A36R406	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	32997	4310R-101-472
A36R408	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	32997	4310R-101-472
A36R410	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	32997	4310R-101-472
A36R412	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	32997	4310R-101-472
A36R414	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	32997	4310R-101-472
A36R416	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	32997	4310R-101-472
A36R418	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	32997	4310R-101-472
A36R420	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	32997	4310R-101-472
A36R422	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	32997	4310R-101-472
A36R424	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	32997	4310R-101-472
A36R426	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	32997	4310R-101-472
A36R428	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	32997	4310R-101-472
A36R430	307-0445-00			RES NTWK,FXD,FI:4.7K OHM,20%,(9)RES	32997	4310R-101-472
A36R440	307-0542-00			RES NTWK,FXD,FI:(5)10K OHM,5%,0.125W	01121	106A103OR706A103
A36R442	307-0542-00			RES NTWK,FXD,FI:(5)10K OHM,5%,0.125W	01121	106A103OR706A103
A36TP100	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A36TP102	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A36TP200	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A36TP240	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A36TP242	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A36TP304	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A36U100	156-2290-00			MICROCKT,DGTL:QUAD MECL TO TTL TRANSLATOR	04713	MC10H125P
A36U102	131-3411-00			CONN,RCPT,ELEC:LYES,FXD,OHO DUMMY	80009	131-3411-00
A36U102	156-2290-00			MICROCKT,DGTL:QUAD MECL TO TTL TRANSLATOR	04713	MC10H125P
A36U104	156-2290-00			MICROCKT,DGTL:QUAD MECL TO TTL TRANSLATOR	04713	MC10H125P
A36U106	156-2290-00			MICROCKT,DGTL:QUAD MECL TO TTL TRANSLATOR	04713	MC10H125P
A36U108	156-2290-00			MICROCKT,DGTL:QUAD MECL TO TTL TRANSLATOR	04713	MC10H125P
A36U110	156-2290-00			MICROCKT,DGTL:QUAD MECL TO TTL TRANSLATOR	04713	MC10H125P
A36U200	156-1961-00			MICROCKT,DGTL:BIDIRECTIONAL UNIV SHF RGTR	07263	74F194P
A36U202	156-1961-00			MICROCKT,DGTL:BIDIRECTIONAL UNIV SHF RGTR	07263	74F194P
A36U204	156-1961-00			MICROCKT,DGTL:BIDIRECTIONAL UNIV SHF RGTR	07263	74F194P
A36U206	156-1961-00			MICROCKT,DGTL:BIDIRECTIONAL UNIV SHF RGTR	07263	74F194P
A36U208	156-1961-00			MICROCKT,DGTL:BIDIRECTIONAL UNIV SHF RGTR	07263	74F194P
A36U210	156-1961-00			MICROCKT,DGTL:BIDIRECTIONAL UNIV SHF RGTR	07263	74F194P
A36U212	156-1961-00			MICROCKT,DGTL:BIDIRECTIONAL UNIV SHF RGTR	07263	74F194P
A36U214	156-1961-00			MICROCKT,DGTL:BIDIRECTIONAL UNIV SHF RGTR	07263	74F194P
A36U216	156-1961-00			MICROCKT,DGTL:BIDIRECTIONAL UNIV SHF RGTR	07263	74F194P
A36U218	156-1961-00			MICROCKT,DGTL:BIDIRECTIONAL UNIV SHF RGTR	07263	74F194P
A36U220	156-1961-00			MICROCKT,DGTL:BIDIRECTIONAL UNIV SHF RGTR	07263	74F194P
A36U222	156-1961-00			MICROCKT,DGTL:BIDIRECTIONAL UNIV SHF RGTR	07263	74F194P
A36U224	156-1961-00			MICROCKT,DGTL:BIDIRECTIONAL UNIV SHF RGTR	07263	74F194P
A36U226	156-1961-00			MICROCKT,DGTL:BIDIRECTIONAL UNIV SHF RGTR	07263	74F194P
A36U228	156-1961-00			MICROCKT,DGTL:BIDIRECTIONAL UNIV SHF RGTR	07263	74F194P
A36U230	156-1961-00			MICROCKT,DGTL:BIDIRECTIONAL UNIV SHF RGTR	07263	74F194P
A36U232	156-1961-00			MICROCKT,DGTL:BIDIRECTIONAL UNIV SHF RGTR	07263	74F194P
A36U234	156-1961-00			MICROCKT,DGTL:BIDIRECTIONAL UNIV SHF RGTR	07263	74F194P
A36U236	156-1961-00			MICROCKT,DGTL:BIDIRECTIONAL UNIV SHF RGTR	07263	74F194P
A36U238	156-1961-00			MICROCKT,DGTL:BIDIRECTIONAL UNIV SHF RGTR	07263	74F194P
A36U240	156-1704-00			MICROCKT,DGTL:ASTTL,OCTAL D TYPE FF	07263	74F374PCQR
A36U242	156-1704-00			MICROCKT,DGTL:ASTTL,OCTAL D TYPE FF	07263	74F374PCQR
A36U244	156-1704-00			MICROCKT,DGTL:ASTTL,OCTAL D TYPE FF	07263	74F374PCQR
A36U246	156-1704-00			MICROCKT,DGTL:ASTTL,OCTAL D TYPE FF	07263	74F374PCQR
A36U248	156-1704-00			MICROCKT,DGTL:ASTTL,OCTAL D TYPE FF	07263	74F374PCQR
A36U250	156-1704-00			MICROCKT,DGTL:ASTTL,OCTAL D TYPE FF	07263	74F374PCQR
A36U252	156-1704-00			MICROCKT,DGTL:ASTTL,OCTAL D TYPE FF	07263	74F374PCQR
A36U254	156-1704-00			MICROCKT,DGTL:ASTTL,OCTAL D TYPE FF	07263	74F374PCQR
A36U256	156-1704-00			MICROCKT,DGTL:ASTTL,OCTAL D TYPE FF	07263	74F374PCQR
A36U258	156-1704-00			MICROCKT,DGTL:ASTTL,OCTAL D TYPE FF	07263	74F374PCQR
A36U300	156-3560-00			MICROCKT,LINEAR:CMOS,16384 X 4 BIT H SP	S5372	HM6288P3522DIP
A36U302	156-3560-00			MICROCKT,LINEAR:CMOS,16384 X 4 BIT H SP	S5372	HM6288P3522DIP
A36U304	156-3560-00			MICROCKT,LINEAR:CMOS,16384 X 4 BIT H SP	S5372	HM6288P3522DIP
A36U306	156-3560-00			MICROCKT,LINEAR:CMOS,16384 X 4 BIT H SP	S5372	HM6288P3522DIP
A36U308	156-3560-00			MICROCKT,LINEAR:CMOS,16384 X 4 BIT H SP	S5372	HM6288P3522DIP
A36U310	156-3560-00			MICROCKT,LINEAR:CMOS,16384 X 4 BIT H SP	S5372	HM6288P3522DIP
A36U312	156-3560-00			MICROCKT,LINEAR:CMOS,16384 X 4 BIT H SP	S5372	HM6288P3522DIP
A36U314	156-3560-00			MICROCKT,LINEAR:CMOS,16384 X 4 BIT H SP	S5372	HM6288P3522DIP
A36U316	156-3560-00			MICROCKT,LINEAR:CMOS,16384 X 4 BIT H SP	S5372	HM6288P3522DIP
A36U318	156-3560-00			MICROCKT,LINEAR:CMOS,16384 X 4 BIT H SP	S5372	HM6288P3522DIP
A36U320	156-3560-00			MICROCKT,LINEAR:CMOS,16384 X 4 BIT H SP	S5372	HM6288P3522DIP
A36U322	156-3560-00			MICROCKT,LINEAR:CMOS,16384 X 4 BIT H SP	S5372	HM6288P3522DIP
A36U324	156-3560-00			MICROCKT,LINEAR:CMOS,16384 X 4 BIT H SP	S5372	HM6288P3522DIP
A36U326	156-3560-00			MICROCKT,LINEAR:CMOS,16384 X 4 BIT H SP	S5372	HM6288P3522DIP
A36U328	156-3560-00			MICROCKT,LINEAR:CMOS,16384 X 4 BIT H SP	S5372	HM6288P3522DIP
A36U330	156-3560-00			MICROCKT,LINEAR:CMOS,16384 X 4 BIT H SP	S5372	HM6288P3522DIP
A36U332	156-3560-00			MICROCKT,LINEAR:CMOS,16384 X 4 BIT H SP	S5372	HM6288P3522DIP
A36U334	156-3560-00			MICROCKT,LINEAR:CMOS,16384 X 4 BIT H SP	S5372	HM6288P3522DIP
A36U336	156-3560-00			MICROCKT,LINEAR:CMOS,16384 X 4 BIT H SP	S5372	HM6288P3522DIP
A36U338	156-3560-00			MICROCKT,LINEAR:CMOS,16384 X 4 BIT H SP	S5372	HM6288P3522DIP
A36U340	156-3560-00			MICROCKT,LINEAR:CMOS,16384 X 4 BIT H SP	S5372	HM6288P3522DIP

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A36U342	156-3560-00			MICROCKT,LINEAR:CMOS,16384 X 4 BIT H SP	S5372	HM6288P3522DIP
A36U344	156-3560-00			MICROCKT,LINEAR:CMOS,16384 X 4 BIT H SP	S5372	HM6288P3522DIP
A36U346	156-3560-00			MICROCKT,LINEAR:CMOS,16384 X 4 BIT H SP	S5372	HM6288P3522DIP
A36U350	156-1707-00			MICROCKT,DGTL:QUAD 2-INPUT NAND GATE,SCRN	04713	MC7400(NDORJD)
A36U400	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A36U402	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A36U404	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A36U406	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A36U408	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A36U410	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A36U412	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A36U414	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A36U416	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A36U418	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A36U420	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A36U422	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A36U424	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A36U426	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A36U428	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A36U430	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A36U440	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A36U442	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A36U444	156-0852-00			MICROCKT,DGTL:HEX DRVR W/3-STATE INPUT	01295	SN74LS367N
A36W100	131-3411-00			CONN,RCPT,ELEC:LYES,FXD,OHO DUMMY	80009	131-3411-00
A40	671-0876-00			CIRCUIT BD ASSY:ADDRESS GENERATOR	TK0191	ORDER BY DESCR
A44	670-9862-00			CIRCUIT BD ASSY:AVERAGER	80009	670-9862-00
A50	671-0686-01			CIRCUIT BD ASSY:MPU	80009	671-0686-01
A50C1	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A50C2	290-1084-00			CAP,FXD,ELCTLT:100UF,20%,16V	80009	290-1084-00
A50C110	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A50C120	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A50C130	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A50C160	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A50C170	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A50C175	290-0995-00			CAP,FXD,ELCTLT:47UF,20%,16V	80009	290-0995-00
A50C180	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A50C200	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A50C210	281-0826-00			CAP,FXD,CER DI:2200PF,10%,100V	20932	401EM100AD222K
A50C230	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A50C260	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A50C280	290-0995-00			CAP,FXD,ELCTLT:47UF,20%,16V	80009	290-0995-00
A50C290	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A50C300	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A50C330	281-0809-00			CAP,FXD,CER DI:200 PF,5%,100V	04222	MA101A201JAA
A50C331	281-0809-00			CAP,FXD,CER DI:200 PF,5%,100V	04222	MA101A201JAA
A50C360	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A50C380	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A50C390	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A50C400	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A50C470	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A50C500	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A50CR175	152-0327-00			SEMICOND DVC,DI:SIG,SI,100MA,75V,D2X5,BAX13	80009	152-0327-00
A50CR280	152-0327-00			SEMICOND DVC,DI:SIG,SI,100MA,75V,D2X5,BAX13	80009	152-0327-00
A50DL270	119-2548-00			DELAY LINE,ELEC:60NS,SIP4	80009	119-2548-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A50DS490	150-1081-00			LT EMITTING DIO:RED	80009	150-1081-00
A50DS491	150-1081-00			LT EMITTING DIO:RED	80009	150-1081-00
A50DS492	150-1081-00			LT EMITTING DIO:RED	80009	150-1081-00
A50J280	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A50P500	131-3137-00			CONN,PLUG,ELEC:DIN,3 X 32,MALE,0.1 SPACING	80009	131-3137-00
A50P501	131-3137-00			CONN,PLUG,ELEC:DIN,3 X 32,MALE,0.1 SPACING	80009	131-3137-00
A50R100	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A50R140	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A50R141	307-0502-00			RES NTWK,FXD,FI:(9) 1.8K OHM,20%,0.125W	11236	750-101-R1.8KOHM
A50R172	307-0902-00			RES NTWK,FXD,FI:(5)2.2K OHM,5%,0.125W EACH	80009	307-0902-00
A50R173	307-0902-00			RES NTWK,FXD,FI:(5)2.2K OHM,5%,0.125W EACH	80009	307-0902-00
A50R175	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A50R176	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A50R177	313-0333-00			RES,FXD,FILM:33K OHM,5%,0.166W	80009	313-0333-00
A50R210	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A50R211	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A50R212	313-0471-00			RES,FXD,FILM:470 OHM,5%,0.166W	80009	313-0471-00
A50R270	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A50R271	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A50R280	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A50R281	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A50R282	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A50R284	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A50R330	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A50R331	313-0332-00			RES,FXD,FILM:3.3K OHM,5%,0.166W	80009	313-0332-00
A50R340	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A50R341	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A50R390	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A50R470	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A50R490	313-0331-00			RES,FXD,FILM:330 OHM,5%,0.166W	80009	313-0331-00
A50R491	313-0331-00			RES,FXD,FILM:330 OHM,5%,0.166W	80009	313-0331-00
A50R492	313-0331-00			RES,FXD,FILM:330 OHM,5%,0.166W	80009	313-0331-00
A50T283	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A50TP1	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A50TP2	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A50TP170	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A50U100	156-0469-00			MICROCKT,DGTL:3-LINE TO 8-LINE DECODER	01295	SN74LS138N
A50U105	156-0465-00			MICROCKT,DGTL:8-INP NAND GATE	18324	N74LS30 (N OR F)
A50U110	156-0479-00			MICROCKT,DGTL:QUAD 2-INP OR GATE	01295	SN74LS32(N OR J)
A50U120	156-0464-00			MICROCKT,DGTL:DUAL 4-INP NAND GATE	01295	SN74LS20(N OR J)
A50U130	156-0385-00			MICROCKT,DGTL:HEX INVERTER	01295	SN74LS04 N OR J
A50U140	156-1252-00			MICROCKT,DGTL:LSTTL,8/3 LINE PRIORTY ENCDR	01295	SN74LS148N P3
A50U150	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A50U160	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A50U170	156-1445-04			MICROCKT,DGTL:NMOS,16 BIT MICROPROCESSOR	04713	MC68000P8
A50U175	156-1611-00			MICROCKT,DGTL:ASTTL,DUAL D TYPE EDGE-TRIG	80009	156-1611-00
A50U180	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A50U190	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A50U200	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A50U210	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A50U220	156-1722-00			MICROCKT,DGTL:FTTL,HEX INVERTER	04713	MC74F04ND
A50U230	156-1727-00			MICROCKT,DGTL:1 OF 8 DCDR/DEMULTIPLEXER	04713	MC74F138 N
A50U240	156-1727-00			MICROCKT,DGTL:1 OF 8 DCDR/DEMULTIPLEXER	04713	MC74F138 N
A50U250	156-1726-00			MICROCKT,DGTL:FTTL,DUAL 1 OF 4 DCDR,SCRN	04713	MC74F139 N
A50U260	156-0718-00			MICROCKT,DGTL:TRIPLE 3-INP NOR GATE	80009	156-0718-00
A50U270	156-0844-00			MICROCKT,DGTL:SYN 4-BIT BIN CNTR	01295	SN74LS161AN
A50U280	156-3032-00			MICROCKT,DGTL:QUAD 2-INP,POS NAND GATES	S5372	HD74LS01
A50U290	156-3103-00			MICROCKT,DGTL:CMOS,32768 X 8 SRAM	80009	156-3103-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A50U300	156-3103-00			MICROCKT,DGTL:CMOS,32768 X 8 SRAM	80009	156-3103-00
A50U330	156-0733-00			MICROCKT,DGTL:DUAL MONOSTABLE MV W/ST INP	01295	SN74LS221 N OR J
A50U340	156-0388-00			MICROCKT,DGTL:DUAL D FLIP-FLOP	01295	SN74LS74 N OR J
A50U350	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A50U360	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A50U365	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A50U370	156-0479-00			MICROCKT,DGTL:QUAD 2-INP OR GATE	01295	SN74LS32(N OR J)
A50U375	156-1726-00			MICROCKT,DGTL:FTTL,DUAL 1 OF 4 DCDR,SCRN	04713	MC74F139 N
A50U380	156-0383-00			MICROCKT,DGTL:QUAD 2-INP NOR GATE	01295	SN74LS02 N OR J
A50U390	160-5537-00			MICROCKT,DGTL:131082 X 8 EPROM,PRGM	S5372	HN27C101G-17
A50U400	160-5538-00			MICROCKT,DGTL:131082 X 8 EPROM,PRGM	S5372	HN27C101G-17
A50U470	156-1267-00			MICROCKT,DGTL:STTL,TRIPLE 3 INP NAND GATE	01295	SN74LS15NP3
A50U475	156-1267-00			MICROCKT,DGTL:STTL,TRIPLE 3 INP NAND GATE	01295	SN74LS15NP3
A50U480	156-0465-00			MICROCKT,DGTL:8-INP NAND GATE	18324	N74LS30 (N OR F)
A50U490	156-0865-00			MICROCKT,DGTL:OCTAL D FF W/CLR	01295	SN74LS273 N OR J
A50U500	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A50U510	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A50W1	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A50XU390	136-0973-00			SKT,PL-IN ELEK:MICROCKT,DIP32	TK0FB	DILB32P-8J
A50XU400	136-0973-00			SKT,PL-IN ELEK:MICROCKT,DIP32	TK0FB	DILB32P-8J
A50Y170	119-1408-00			OSC,XTAL CLOCK:16MHZ,0.01%	80009	119-1408-00
A52	671-0685-00			CIRCUIT BD ASSY:DMA	TK0191	ORDER BY DESCR
A52BT320	146-0061-00			BATTERY,DRY:3.6V,1.0AH,LITHIUM	80009	146-0061-00
A52BT321	146-0061-00			BATTERY,DRY:3.6V,1.0AH,LITHIUM	80009	146-0061-00
A52C1	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A52C2	290-1084-00			CAP,FXD,ELCTLT:100UF,20%,16V	80009	290-1084-00
A52C100	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C120	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C140	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C170	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C190	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C191	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C220	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C230	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C240	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C250	281-0813-00			CAP,FXD,CER DI:0.047UF,20%,50V	05397	C412C473M5V2CA
A52C251	281-0813-00			CAP,FXD,CER DI:0.047UF,20%,50V	05397	C412C473M5V2CA
A52C252	281-0813-00			CAP,FXD,CER DI:0.047UF,20%,50V	05397	C412C473M5V2CA
A52C253	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C280	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C290	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C310	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C311	290-0995-00			CAP,FXD,ELCTLT:47UF,20%,16V	80009	290-0995-00
A52C320	290-1084-00			CAP,FXD,ELCTLT:100UF,20%,16V	80009	290-1084-00
A52C330	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C331	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C335	281-0826-00			CAP,FXD,CER DI:2200PF,10%,100V	20932	401EM100AD222K
A52C350	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C360	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C370	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C380	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C410	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C420	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C440	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A52C450	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A52CR310	152-0327-00			SEMICOND DVC,DI:SIG,SI,100MA,75V,D2X5,BAX13	80009	152-0327-00
A52CR311	152-0327-00			SEMICOND DVC,DI:SIG,SI,100MA,75V,D2X5,BAX13	80009	152-0327-00
A52CR320	152-0327-00			SEMICOND DVC,DI:SIG,SI,100MA,75V,D2X5,BAX13	80009	152-0327-00
A52CR321	152-0327-00			SEMICOND DVC,DI:SIG,SI,100MA,75V,D2X5,BAX13	80009	152-0327-00
A52J250	131-0608-00			TERMINAL,PIN:0.365 L X 0.025 BRZ GLD PL	22526	48283-036
A52LS250	119-2532-00			SPEAKER:PM,CERAMIC	80009	119-2532-00
A52P250	131-4311-00			BUS,CONDUCTOR:WHITE,SHUNT ASSY	80009	131-4311-00
A52P520	131-3137-00			CONN,PLUG,ELEC:DIN,3 X 32,MALE,0.1 SPACING	80009	131-3137-00
A52P521	131-3137-00			CONN,PLUG,ELEC:DIN,3 X 32,MALE,0.1 SPACING	80009	131-3137-00
A52Q250	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A52Q310	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A52Q320	151-0188-00			TRANSISTOR:PNP,SI,TO-92	80009	151-0188-00
A52Q321	151-0190-00			TRANSISTOR:NPN,SI,TO-92	80009	151-0190-00
A52Q322	151-0873-00			TRANSISTOR:NPN,SI,TO-18	TK00J	2SC1216
A52R1	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A52R2	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A52R160	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A52R161	307-0750-00			RES NTWK,FXD,FI:(8)4.7K OHM,5%,0.125W	80009	307-0750-00
A52R170	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A52R190	307-0750-00			RES NTWK,FXD,FI:(8)4.7K OHM,5%,0.125W	80009	307-0750-00
A52R191	307-0902-00			RES NTWK,FXD,FI:(5)2.2K OHM,5%,0.125W EACH	80009	307-0902-00
A52R250	321-0305-00			RES,FXD,FILM:14.7K OHM,1%,0.125W,TC=T0	19701	5033ED14K70F
A52R251	321-0334-00			RES,FXD,FILM:29.4K OHM,1%,0.125W,TC=T0	07716	CEAD29401F
A52R252	321-0363-00			RES,FXD,FILM:59.0K OHM,1%,0.125W,TC=T0	07716	CEAD59001F
A52R253	313-0103-00			RES,FXD,FILM:10K OHM,5%,0.166W	80009	313-0103-00
A52R254	313-0513-00			RES,FXD,FILM:51K OHM,5%,0.166W	80009	313-0513-00
A52R255	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A52R256	313-0103-00			RES,FXD,FILM:10K OHM,5%,0.166W	80009	313-0103-00
A52R290	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A52R300	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A52R309	321-0225-06			RES,FXD,FILM:2.15K OHM,0.25%,0.125W,T=T9	07716	CEAE21500C
A52R310	321-0929-07			RES,FXD,FILM:2.5K OHM,0.1%,0.125W,TC=T9	19701	5033RE2K500B
A52R311	313-0151-00			RES,FXD,FILM:150 OHM,5%,0.166W	80009	313-0151-00
A52R312	313-0471-00			RES,FXD,FILM:470 OHM,5%,0.166W	80009	313-0471-00
A52R313	313-0473-00			RES,FXD,FILM:47K OHM,5%,0.166W	80009	313-0473-00
A52R314	313-0202-00			RES,FXD,FILM:2K OHM,5%,0.166W	80009	313-0202-00
A52R315	313-0511-00			RES,FXD,FILM:510 OHM,5%,0.166W	80009	313-0511-00
A52R316	313-0471-00			RES,FXD,FILM:470 OHM,5%,0.166W	80009	313-0471-00
A52R317	313-0202-00			RES,FXD,FILM:2K OHM,5%,0.166W	80009	313-0202-00
A52R318	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A52R319	313-0104-00			RES,FXD,FILM:100K OHM,5%,0.166W	80009	313-0104-00
A52R320	313-0511-00			RES,FXD,FILM:510 OHM,5%,0.166W	80009	313-0511-00
A52R321	313-0511-00			RES,FXD,FILM:510 OHM,5%,0.166W	80009	313-0511-00
A52R322	313-0622-00			RES,FXD,FILM:6.2K OHM,5%,0.166W	S5518	R20T29J6.2KOHM
A52R323	313-0152-00			RES,FXD,FILM:1.5K OHM,5%,0.166W	80009	313-0152-00
A52R324	313-0202-00			RES,FXD,FILM:2K OHM,5%,0.166W	80009	313-0202-00
A52R325	313-0392-00			RES,FXD,FILM:3.9K OHM,5%,0.166W	80009	313-0392-00
A52R326	313-0392-00			RES,FXD,FILM:3.9K OHM,5%,0.166W	80009	313-0392-00
A52R327	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A52R328	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A52R330	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A52R331	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A52R332	313-0272-00			RES,FXD,FILM:2.7K OHM,5%,0.166W	80009	313-0272-00
A52R333	313-0242-00			RES,FXD,FILM:2.4K OHM,5%,0.166W	80009	313-0242-00
A52R335	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A52R336	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A52R337	313-0471-00			RES,FXD,FILM:470 OHM,5%,0.166W	80009	313-0471-00
A52R355	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A52R390	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A52R400	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A52R410	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A52R420	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A52TP1	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A52TP2	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A52TP3	214-0579-00			TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A52U100	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A52U110	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A52U120	156-1065-00			MICROCKT,DGTL:OCTAL D TYPE TRANS LATCHES	01295	SN74LS373N
A52U130	156-1065-00			MICROCKT,DGTL:OCTAL D TYPE TRANS LATCHES	01295	SN74LS373N
A52U140	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A52U150	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A52U160	156-1252-00			MICROCKT,DGTL:LSTTL,8/3 LINE PRIORTY ENCDR	01295	SN74LS148N P3
A52U170	156-1373-00			MICROCKT,DGTL:LSTTL,QUAD BUS BFR GATES	27014	DM74LS125 N OR J
A52U180	156-1722-00			MICROCKT,DGTL:FTTL,HEX INVERTER	04713	MC74F04ND
A52U190	156-2108-00			MICROCKT,DGTL:DIRECT MEMORY ACCESS CONT	04713	MC68450L8
A52U200	156-0469-00			MICROCKT,DGTL:3-LINE TO 8-LINE DECODER	01295	SN74LS138N
A52U220	156-0469-00			MICROCKT,DGTL:3-LINE TO 8-LINE DECODER	01295	SN74LS138N
A52U230	156-0469-00			MICROCKT,DGTL:3-LINE TO 8-LINE DECODER	01295	SN74LS138N
A52U240	156-0865-00			MICROCKT,DGTL:OCTAL D FF W/CLR	01295	SN74LS273 N OR J
A52U250	156-0402-04			MICROCKT,LINEAR:TIMER	80009	156-0402-04
A52U270	156-0479-00			MICROCKT,DGTL:QUAD 2-INP OR GATE	01295	SN74LS32(N OR J)
A52U280	156-0480-00			MICROCKT,DGTL:TTL,QUAD 2-INP AND GATE	01295	SN74LS08(N OR J)
A52U290	156-0388-00			MICROCKT,DGTL:DUAL D FLIP-FLOP	01295	SN74LS74 N OR J
A52U300	156-0391-00			MICROCKT,DGTL:LSTTL,HEX D TYPE FF W/CLEAR	04713	74LS174(N OR J)
A52U310	156-1126-00			MICROCKT,LINEAR:VOLTAGE COMPARATOR	01295	LM311P
A52U315	156-1631-00			MICROCKT,LINEAR:ADJUSTABLE SHUNT REGULATOR	01295	TL431C-LP
A52U320	156-1663-00			MICROCKT,DGTL:ASTTL,TPL 3-INP & GATE	04713	MC74F11ND/JD
A52U330	156-1778-00			MICROCKT,LINEAR:DUAL COMPARATOR	TK0191	156-1778-00
A52U335	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A52U340	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A52U350	156-1111-00			MICROCKT,DGTL:OCTAL BUS TRANSCEIVERS	01295	SN74LS245N
A52U355	156-0956-00			MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A52U360	156-2483-00			MICROCKT,DGTL:CMOS,8192 X 8,150NS	80009	156-2483-00
A52U370	156-2483-00			MICROCKT,DGTL:CMOS,8192 X 8,150NS	80009	156-2483-00
A52U380	156-0323-00			MICROCKT,DGTL:HEX INVERTER	01295	SN74S04N
A52U390	156-1172-00			MICROCKT,DGTL:DUAL 4 BIT BIN CNTR	01295	SN74LS393N
A52U400	156-0910-00			MICROCKT,DGTL:DUAL DECADE COUNTER	07263	SL68104
A52U410	156-0798-00			MICROCKT,DGTL:DUAL 4-INPUT MUX W/ENABLE	18324	N74LS153(N OR F)
A52U420	156-0910-00			MICROCKT,DGTL:DUAL DECADE COUNTER	07263	SL68104
A52U430	156-0910-00			MICROCKT,DGTL:DUAL DECADE COUNTER	07263	SL68104
A52U440	156-0910-00			MICROCKT,DGTL:DUAL DECADE COUNTER	07263	SL68104
A52U450	156-1373-00			MICROCKT,DGTL:LSTTL,QUAD BUS BFR GATES	27014	DM74LS125 N OR J
A52VR250	152-0590-00			SEMICOND DVC,DI:ZEN,SI,18V,5%,400MW	80009	152-0590-00
A52W1	131-0566-00			BUS,CONDUCTOR:DUMMY RES,0.094 OD X 0.225 L	24546	OMA 07
A52Y380	119-2533-00			OSCILLATOR,RF:5MHZ	80009	119-2533-00
A54	670-9865-00			CIRCUIT BD ASSY:DISPLAY CONTROL	80009	670-9865-00
A56	670-9866-00			CIRCUIT BD ASSY:GPIB/MONITOR	80009	670-9866-00
A60	671-0684-00			CIRCUIT BD ASSY:FRONT PANEL CONTROL	TK0191	ORDER BY DESCR
A60C1	119-1762-00			FILTER,RFI:0.022UF,+50/-20%,50V	80009	119-1762-00
A60C2	290-1084-00			CAP,FXD,ELCTLT:100UF,20%,16V	80009	290-1084-00
A60C100	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A60C170	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A60C180	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A60C200	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A60C220	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A60C250	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A60C260	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A60C261	290-0995-00			CAP,FXD,ELCTLT:47UF,20%,16V	80009	290-0995-00
A60C270	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A60C271	290-0995-00			CAP,FXD,ELCTLT:47UF,20%,16V	80009	290-0995-00
A60C280	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A60C281	290-0995-00			CAP,FXD,ELCTLT:47UF,20%,16V	80009	290-0995-00
A60C290	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A60C291	290-0995-00			CAP,FXD,ELCTLT:47UF,20%,16V	80009	290-0995-00
A60C330	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A60C350	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A60C360	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A60C370	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A60C390	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A60C430	281-0775-00			CAP,FXD,CER DI:0.1UF,20%,50V	04222	MA205E104MAA
A60DS250	150-1100-00			LT EMITTING DIO:RED,700NM,10MA,1.95V	80009	150-1100-00
A60DS251	150-1100-00			LT EMITTING DIO:RED,700NM,10MA,1.95V	80009	150-1100-00
A60DS252	150-1100-00			LT EMITTING DIO:RED,700NM,10MA,1.95V	80009	150-1100-00
A60DS253	150-1100-00			LT EMITTING DIO:RED,700NM,10MA,1.95V	80009	150-1100-00
A60DS254	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS255	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS260	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS261	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS262	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS263	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS264	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS265	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS266	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS267	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS270	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS271	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS272	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS273	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS274	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS275	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS276	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS277	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS280	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS281	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS282	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS283	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS284	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS285	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS286	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS287	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS290	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS291	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS292	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS293	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS294	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS295	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS296	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS297	150-0204-01			LAMP,LED RDOUT:ORANGE,7 SEG,635NM	80009	150-0204-01
A60DS314	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS315	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A60DS350	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS351	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS352	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS353	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS354	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS355	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS356	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS360	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS361	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS362	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS363	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS364	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS370	150-0148-00			LT EMITTING DIO:RED	80009	150-0148-00
A60DS371	150-0148-00			LT EMITTING DIO:RED	80009	150-0148-00
A60DS380	150-0148-00			LT EMITTING DIO:RED	80009	150-0148-00
A60DS381	150-0148-00			LT EMITTING DIO:RED	80009	150-0148-00
A60DS390	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS391	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS392	150-1190-00			LT EMITTING DIO:RED,635NM,30MA	80009	150-1190-00
A60DS393	150-1190-00			LT EMITTING DIO:RED,635NM,30MA	80009	150-1190-00
A60DS420	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS421	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS422	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS423	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS424	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS425	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS426	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS430	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS431	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS432	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS434	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS435	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS436	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS437	150-1109-01			LT EMITTING DIO:GREEN,565NM,50MA	80009	150-1109-01
A60DS440	150-0148-00			LT EMITTING DIO:RED	80009	150-0148-00
A60DS441	150-0148-00			LT EMITTING DIO:RED	80009	150-0148-00
A60DS450	150-0148-00			LT EMITTING DIO:RED	80009	150-0148-00
A60DS451	150-0148-00			LT EMITTING DIO:RED	80009	150-0148-00
A60J250	131-0589-00			TERMINAL,PIN:0.46 L X 0.025 SQ PH BRZ	22526	48283-029
A60J700	131-3866-00			CONN,RCPT,ELEC:HEADER,2 X 25,0.1 SPACING	80009	131-3866-00
A60J846	131-0787-00			TERMINAL,PIN:0.64 L X 0.025 SQ PH BRZ	22526	47359-000
A60R1	307-0750-00			RES NTWK,FXD,FI:(8)4.7K OHM,5%,0.125W	80009	307-0750-00
A60R2	307-0750-00			RES NTWK,FXD,FI:(8)4.7K OHM,5%,0.125W	80009	307-0750-00
A60R100	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A60R101	307-0750-00			RES NTWK,FXD,FI:(8)4.7K OHM,5%,0.125W	80009	307-0750-00
A60R110	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A60R120	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A60R121	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A60R130	307-0750-00			RES NTWK,FXD,FI:(8)4.7K OHM,5%,0.125W	80009	307-0750-00
A60R140	307-0750-00			RES NTWK,FXD,FI:(8)4.7K OHM,5%,0.125W	80009	307-0750-00
A60R141	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A60R150	313-0472-00			RES,FXD,FILM:4.7K OHM,5%,0.166W	80009	313-0472-00
A60R230	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A60R240	313-0102-00			RES,FXD,FILM:1K OHM,5%,0.166W	80009	313-0102-00
A60R250	307-0793-00			RES NTWK,FXD,FI:(4)330 OHM,10%,0.125 W S/T	80009	307-0793-00
A60R251	307-0488-01			RES NTWK,FXD,FI:(5)100 OHM,10%,0.125W	80009	307-0488-01
A60R252	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A60R320	307-0939-00			RES NTWK,FXD,FI:(8)330 OHM,10%,0.125W EACH	80009	307-0939-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A60R330	307-0939-00			RES NTWK,FXD,FI:(8)330 OHM,10%,0.125W EACH	80009	307-0939-00
A60R340	307-0939-00			RES NTWK,FXD,FI:(8)330 OHM,10%,0.125W EACH	80009	307-0939-00
A60R341	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A60R350	307-0876-00			RES NTWK,FXD,FI:(8)100 OHM,10%,0.125W	80009	307-0876-00
A60R360	307-0795-00			RES NTWK,FXD,FI:(6)100 OHM,10%,0.125W	80009	307-0795-00
A60R370	307-0939-00			RES NTWK,FXD,FI:(8)330 OHM,10%,0.125W EACH	80009	307-0939-00
A60R380	307-0939-00			RES NTWK,FXD,FI:(8)330 OHM,10%,0.125W EACH	80009	307-0939-00
A60R381	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A60R390	307-0488-01			RES NTWK,FXD,FI:(5)100 OHM,10%,0.125W	80009	307-0488-01
A60R391	313-0151-00			RES,FXD,FILM:150 OHM,5%,0.166W	80009	313-0151-00
A60R392	313-0151-00			RES,FXD,FILM:150 OHM,5%,0.166W	80009	313-0151-00
A60R393	313-0151-00			RES,FXD,FILM:150 OHM,5%,0.166W	80009	313-0151-00
A60R395	307-0939-00			RES NTWK,FXD,FI:(8)330 OHM,10%,0.125W EACH	80009	307-0939-00
A60R396	313-0151-00			RES,FXD,FILM:150 OHM,5%,0.166W	80009	313-0151-00
A60R397	313-0151-00			RES,FXD,FILM:150 OHM,5%,0.166W	80009	313-0151-00
A60R398	313-0151-00			RES,FXD,FILM:150 OHM,5%,0.166W	80009	313-0151-00
A60R400	307-0939-00			RES NTWK,FXD,FI:(8)330 OHM,10%,0.125W EACH	80009	307-0939-00
A60R410	307-0939-00			RES NTWK,FXD,FI:(8)330 OHM,10%,0.125W EACH	80009	307-0939-00
A60R411	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A60R420	307-0876-00			RES NTWK,FXD,FI:(8)100 OHM,10%,0.125W	80009	307-0876-00
A60R430	307-0876-00			RES NTWK,FXD,FI:(8)100 OHM,10%,0.125W	80009	307-0876-00
A60R440	307-0939-00			RES NTWK,FXD,FI:(8)330 OHM,10%,0.125W EACH	80009	307-0939-00
A60R450	307-0939-00			RES NTWK,FXD,FI:(8)330 OHM,10%,0.125W EACH	80009	307-0939-00
A60R451	313-0101-00			RES,FXD,FILM:100 OHM,5%,0.166W	80009	313-0101-00
A60S101	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S102	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S103	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S104	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S105	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S106	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S107	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S108	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S109	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S110	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S111	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S112	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S113	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S114	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S115	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S200	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S201	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S203	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S204	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S207	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S208	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S209	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S210	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S211	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S212	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S213	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S214	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S215	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S300	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S301	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S302	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S303	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S304	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S305	260-2154-00			SWITCH,KEY:SPST W/LED RED	80009	260-2154-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective - Descnt	Name & Description	Mfr. Code	Mfr. Part No.
A60S306	260-2154-00		SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S307	260-2154-00		SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S308	260-2154-00		SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S309	260-2154-00		SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S310	260-2154-00		SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S311	260-2154-00		SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S312	260-2154-00		SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S313	260-2154-00		SWITCH,KEY:SPST W/LED RED	80009	260-2154-00
A60S400	260-2351-00		SWITCH,ROCKER:SPST,0.4VA,28V	80009	260-2351-00
A60S402	260-2351-00		SWITCH,ROCKER:SPST,0.4VA,28V	80009	260-2351-00
A60S404	260-2351-00		SWITCH,ROCKER:SPST,0.4VA,28V	80009	260-2351-00
A60S406	260-2351-00		SWITCH,ROCKER:SPST,0.4VA,28V	80009	260-2351-00
A60S408	260-2351-00		SWITCH,ROCKER:SPST,0.4VA,28V	80009	260-2351-00
A60S410	260-2351-00		SWITCH,ROCKER:SPST,0.4VA,28V	80009	260-2351-00
A60TP1	214-0579-00		TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A60TP2	214-0579-00		TERM,TEST POINT:BRS CD PL	80009	214-0579-00
A60U100	156-0956-00		MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A60U110	156-2808-00		MICROCKT,DGTL:CMOS,QUAD 2-INPUT OR	TK0191	156-2808-00
A60U120	156-3034-00		MICROCKT,DGTL:HEX BUS DRVRS,INV DATA OUT	TK00L	TC74HC368P
A60U130	156-0956-00		MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A60U140	156-0956-00		MICROCKT,DGTL:OCTAL BFR W/3 STATE OUT	18324	N74LS244(N OR F)
A60U150	156-2825-00		MICROCKT,DGTL:CMOS,DUAL 2-4 DCDR	80009	156-2825-00
A60U160	156-2808-00		MICROCKT,DGTL:CMOS,QUAD 2-INPUT OR	TK0191	156-2808-00
A60U170	156-2316-00		MICROCKT,DGTL:3/8 LINE DECODER	80009	156-2316-00
A60U180	156-0914-00		MICROCKT,DGTL:OCT ST BFR W/3-STATE OUT	18324	N74LS240(N OR F)
A60U190	156-0914-00		MICROCKT,DGTL:OCT ST BFR W/3-STATE OUT	18324	N74LS240(N OR F)
A60U200	156-0728-00		MICROCKT,DGTL:QUAD 2-INP AND GATE W/OC OUT	01295	SN74LS09(N OR J)
A60U210	156-2316-00		MICROCKT,DGTL:3/8 LINE DECODER	80009	156-2316-00
A60U220	156-2316-00		MICROCKT,DGTL:3/8 LINE DECODER	80009	156-2316-00
A60U230	156-2310-00		MICROCKT,DGTL:HEX D TYPE FF	80009	156-2310-00
A60U240	156-2301-00		MICROCKT,DGTL:QUAD BUFFER W/3 STATE	80009	156-2301-00
A60U245	156-0480-00		MICROCKT,DGTL:TTL,QUAD 2-INP AND GATE	01295	SN74LS08(N OR J)
A60U250	156-0914-00		MICROCKT,DGTL:OCT ST BFR W/3-STATE OUT	18324	N74LS240(N OR F)
A60U260	156-3035-00		MICROCKT,DGTL:UNIVERSAL 3 DIGIT LED DRIVER	TK00Y	ICM7218CIJI
A60U270	156-3035-00		MICROCKT,DGTL:UNIVERSAL 3 DIGIT LED DRIVER	TK00Y	ICM7218CIJI
A60U280	156-3035-00		MICROCKT,DGTL:UNIVERSAL 3 DIGIT LED DRIVER	TK00Y	ICM7218CIJI
A60U290	156-3035-00		MICROCKT,DGTL:UNIVERSAL 3 DIGIT LED DRIVER	TK00Y	ICM7218CIJI
A60U320	156-2315-00		MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A60U330	156-2315-00		MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A60U340	156-2315-00		MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A60U350	156-2315-00		MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A60U360	156-2315-00		MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A60U370	156-2315-00		MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A60U380	156-2315-00		MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A60U390	156-2315-00		MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A60U395	156-2315-00		MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A60U400	156-2315-00		MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A60U410	156-2315-00		MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A60U420	156-2315-00		MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A60U430	156-2315-00		MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A60U440	156-2315-00		MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A60U450	156-2315-00		MICROCKT,DGTL:3 STATE OCTAL D TYPE FF	80009	156-2315-00
A64	670-9868-00		CIRCUIT BD ASSY:INDICATOR (OPTION 19)	80009	670-9868-00
A70	670-9869-00		CIRCUIT BD ASSY:MAIN INTERCONNECT	80009	670-9869-00

Component No.	Tektronix Part No.	Serial/Assembly No. Effective	Dscont	Name & Description	Mfr. Code	Mfr. Part No.
A74	670-9870-00			CIRCUIT BD ASSY:I/O	80009	670-9870-00
A76	670-9871-00			CIRCUIT BD ASSY:OSCILLATOR	80009	670-9871-00