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SG 5010 PROGRAMMABLE 160 kHz OSCILLATOR

INSTRUCTION MANUAL

Tektronix, Inc.
P.O. Box 500
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070-4331-00
Product Group 76

Serial Number _____

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SERVICE SAFETY SUMMARY

FOR QUALIFIED SERVICE PERSONNEL ONLY

Refer also to the preceding Operators Safety Summary

Do Not Service Alone

Do not perform internal service or adjustment of this product unless another person capable of rendering first aid and resuscitation is present.

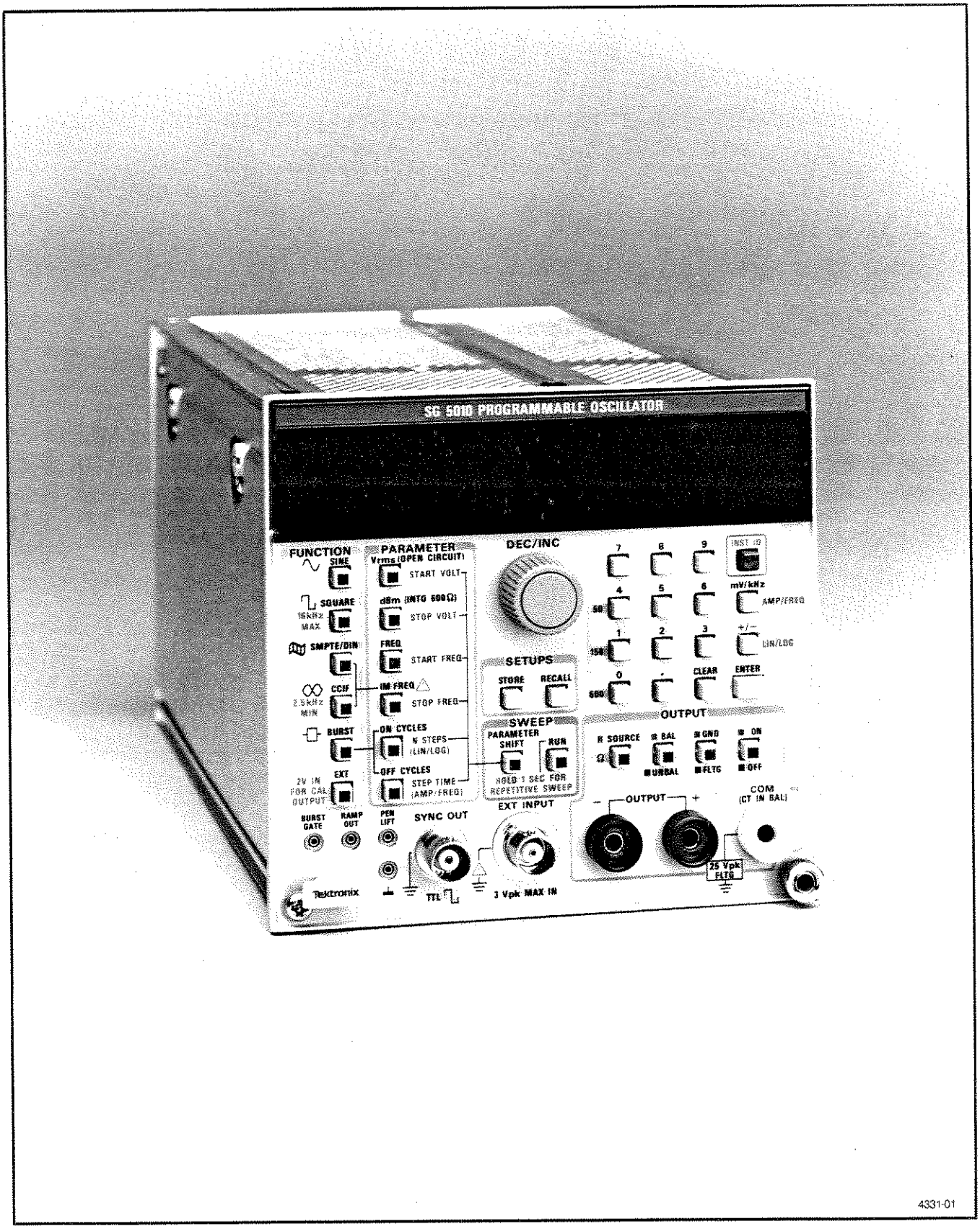
Use Care When Servicing With Power On

Dangerous voltages may exist at several points in this product. To avoid personal injury, do not touch exposed connections and components while power is on.

Disconnect power before removing protective panels, soldering, or replacing components.

Power Source

This product is intended to operate in a power module connected to a power source that will not apply more than 250 volts rms between the supply conductors or between either supply conductor and ground. A protective ground connection by way of the grounding conductor in the power cord is essential for safe operation.



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SG 5010 Programmable 160 kHz Oscillator.

SPECIFICATION

Introduction

This section of the manual contains a general description of the TEKTRONIX SG 5010 Programmable 160 kHz Oscillator and its electrical, environmental, and physical specifications. Standard accessories are also listed. Instrument option information is located in the Options section.

Instrument Description

The SG 5010 Programmable 160 kHz Oscillator is a GPIB programmable TM 5000-Series plug-in instrument designed for low-distortion audio applications. It generates five waveforms: sine wave, square wave, SMPTE/DIN intermodulation test signal, CCIF intermodulation test signal, and sine wave burst. All of these signals may be swept in frequency or amplitude. Frequency, amplitude, and burst parameters are fully programmable, as are the sweep parameters. Parameter values are displayed by 5 seven-segment LEDs in the display window. The window also indicates parameter units, remote or addressed state, and error codes. Three source impedances are selectable and the output signal can be grounded or floating, balanced or unbalanced. Output amplitude is programmable from 0.2 mV to 21.2 V peak equivalent Vrms (10.6 Vrms maximum in unbalanced mode), supplying up to 28 dBm into a 600 Ω load. An ON-OFF function turns the output signal on or off at the output connectors. Additional connectors supply a sync signal, sweep ramp and pen lift signals and accept triggering and input signals from external sources.

At power-up, the instrument performs a self-test and assumes the settings in use when previously powered-down, with the exception that the output is in the "OFF" condition and the display shows the amplitude. Instrument functions can be set to ten user-definable configurations stored in memory.

The SG 5010 is designed for remote or local operation in two compartments of any TM 5000-Series power module. It can also operate under local control only, in two compartments of a TM 500-Series power module, after minor mechanical modification (refer to qualified service personnel). Rear interface connections provide access to versions of all front panel signals except the main output.

Standard Accessories

The following items are shipped with the SG 5010.

1 Instruction Manual

1 Reference Guide

1 Instrument Interfacing Guide

1 Banana-to-bnc adapter

Optional Accessories

1 Pin plug-to-bnc cable

Refer to the Accessories page at the back of this manual for part numbers.

IEEE 488 (GPIB) Functions

The SG 5010 can be remotely programmed via the digital interface specified in IEEE Standard 488-1978, *IEEE Standard Digital Interface for Programmable Instrumentation.* In this manual, the digital interface is called the General Purpose Interface Bus (GPIB).

The IEEE standard identifies the interface function repertoire of an instrument on the GPIB in terms of interface function subsets. The subsets are defined in the standard. The subsets that apply to the SG 5010 are listed in Table 1-1.

NOTE

Refer to IEEE Standard 488-1978 for more detailed information. The standard is published by the Institute of Electrical and Electronics Engineers, Inc., 345 East 47th Street, New York, New York 10017.

Table 1-1
IEEE 488 INTERFACE FUNCTION SUBSETS

Function	Subset	Capability
Source Handshake	SH1	Complete capability.
Acceptor Handshake	AH1	Complete capability.
Basic Talker	T6	Responds to Serial Poll, Untalks if My Listen Address (MLA) is received.
Basic Listener	L4	Unlistens if My Talk Address (MTA) is received.
Service Request	SR1	Complete capability.
Remote-Local Function	RL1	Complete capability.
Parallel Poll	PP0	Does not respond to Parallel Poll.
Device Clear	DC1	Complete capability.
Device Trigger	DT1	Complete capability.
Controller Function	C0	No controller function.
Electrical Interface	E2	Tri-state drivers.

Performance Conditions

The limits stated in the Performance Requirements column of the following tables are valid with the following conditions:

1. The instruments internal adjustments are performed at an ambient temperature of +20 to +30°C.

2. The instrument must be in a non-condensing environment whose limits are described under Environmental, Table 1-4.

3. Allow twenty minutes warm-up time for operation to specified accuracy; sixty minutes after exposure to or storage in high-humidity (condensing) environment.

Items listed in the Performance Requirements column of the Electrical Characteristics are verified by completing the Performance Check in this manual. Information in the Supplemental Information and Description columns is provided for user information only and should not be interpreted to be Performance Check requirements.

Table 1-2
ELECTRICAL CHARACTERISTICS

Characteristics	Performance Requirements	Supplemental Information
	SINE FUNCTION	
FREQUENCY RANGE	10.00 Hz to 163.80 kHz	Resolution is 0.01 Hz to 163.80 Hz, 0.1 Hz to 1638.0 Hz, 1 Hz to 16.380 kHz, 10 Hz to 163.80 kHz.
Accuracy	±0.01%	Phase locked to internal crystal reference. Typical settling time to specified accuracy is less than 0.5 second for frequencies above 50 Hz, increasing to approximately 1 second at 10 Hz.
DISTORTION (RL 600 ohms maximum output)	THD, 2nd through 5th harmonics only	THD+N system spec with AA 5001 analyzer
10 Hz to 20 Hz	0.010% (−80 dB)	0.010% (−80 dB)
20 Hz to 20 kHz	0.0010% (−100 dB)	0.0032% (−90 dB)[a]
20 kHz to 50 kHz	0.0032% (−90 dB)	0.010% (−80 dB)
20 kHz to 100 kHz	0.010% (−80 dB)	0.010% (−80 dB)
100 kHz to 163.8 kHz	0.032% (−70 dB)[b]	(not applicable)
LEVEL FLATNESS (1 kHz reference)		
20 Hz to 20 kHz	±0.05 dB	
10 Hz to 163.8 kHz	±0.2 dB	
	SQUARE WAVE FUNCTION	
FREQUENCY RANGE	10.00 Hz to 16.380 kHz	Accuracy and resolution are same as sinewave function.
RISE & FALL TIME	1.5 μs ±10%	Typically less than 2% aberrations.
	SMPTE/DIN FUNCTION	
UPPER FREQUENCY RANGE	10 Hz to 163.80 kHz	Accuracy and resolution same as sinewave function.
LOWER FREQUENCY (IM frequency) RANGE	Selectable from 40 Hz, 50 Hz, 60 Hz, 80 Hz, 100 Hz, 125 Hz, 250 Hz, or 500 Hz, all ±2%	Settling time is typically less than 1 second for changes in IM frequency. Mixing ratio is selectable 4:1 or 1:1, both typically within 3%.
RESIDUAL IMD (7 kHz and 60 Hz, or 8 kHz and 250 Hz, RL ≥600 ohms)	≤0.0032% (−90 dB)	System specification with AA 5001 distortion analyzer.
	CCIF FUNCTION	
CENTER FREQUENCY RANGE	2.5 kHz to 163.80 kHz	Accuracy and resolution are same as sinewave function.
IM FREQUENCY RANGE	Selectable from 40 Hz, 50 Hz, 60 Hz, 80 Hz, 100 Hz, 125 Hz, 250 Hz, or 500 Hz, all ±2%.	Settling time is typically less than 1 second for changes in IM frequency. Output twin frequencies are fcenter ± FIM.

Table 1-2 (cont)
ELECTRICAL CHARACTERISTICS

Characteristics	Performance Requirements	Supplemental Information
	CCIF FUNCTION	
RESIDUAL IMD (14 kHz and 15 kHz, RL ≥600 ohms)	≤0.0018% (−95 dB)	System specification with AA 5001 distortion analyzer.
CENTER FREQUENCY LEAKAGE AND HARMONIC CONTENT	≤40 dB for center frequencies up to 20 kHz.	
	BURST FUNCTION	
ON CYCLES RANGE	1 to 65535	
OFF CYCLES RANGE	1 to 65535	Selecting 0 cycles enables continuous burst mode and selecting 99999 cycles enables single burst mode.
OFF AMPLITUDE		
0% Mode	≤−40 dB	
10% Mode	−20 dB ±0.5 dB	
BURST GATE INPUT		TTL compatible input with internal pullup resistor. A low input will truncate burst output at next zero crossing and reset both on and off cycle counters. A subsequent high input will enable burst output at next available zero crossing.
	EXTERNAL (AMPLIFIER) FUNCTION	
INPUT IMPEDANCE and Configuration		Balanced with approximately 15 k to 20 k ohms each side to main signal output common.
MAXIMUM INPUT VOLTAGE		3 V peak ac + dc (dc component must not exceed 50 mV for linear operation). Maximum floating voltage is 25 V peak, limited to 3 V peak between input common and main output common for linear operation. Common mode rejection is typically better than 46 dB.
GAIN ACCURACY	5.0% (0.5 dB for dBm)	Output amplitude is calibrated for 2 Vrms (5.66 Vp-p) input. Overall voltage gain is one-half of selected Vrms value.
FREQUENCY RESPONSE (1 kHz ref)	±0.1 dB, 20 Hz to 20 kHz	Risetime is typically less than 2 μs
THD+N (80 kHz bandwidth limited)	≤0.01% (−80 dB), 20 Hz to 20 kHz	

Table 1-2 (cont)
ELECTRICAL CHARACTERISTICS

Characteristics	Performance Requirements	Supplemental Information
	MAIN OUTPUT	
IMPEDANCE	Selectable 600 ohms ±1%, 150 ohms ±2%, or 50 ohms ±3%	Selectable balanced or unbalanced configuration, floating or grounded through approximately 30 ohms. In balanced configuration output impedance from each output to CT is 1/2 of selected value. Output impedance does not change with ON/OFF selection.
AMPLITUDE RANGE		
Maximum Output		
Balanced mode	21.20 Vrms open circuit or +28.05[c] dBm into 600 ohms.	Current limited for combined RS+RL below approximately 200 ohms.
Unbalanced mode	10.60 Vrms open circuit or +22.05[c] dBm into 600 ohms.	Current limited for combined RS+RL below approximately 100 ohms.
Minimum Output	0.200 mVrms open circuit or −72.45[c] dBm into 600 ohms.	
AMPLITUDE RESOLUTION		Typically better than 0.25% for Vrms or 0.05 dB.
AMPLITUDE ACCURACY (Vrms ⩾50 mV, calibrated for constant Vp-p output, sinewave equivalent Vrms or dBm.)		
Sine function		
20 Hz to 20 kHz	±2.0% (0.2 dB for dBm)	
10 Hz to 163.8 kHz	±3.0% (0.3 dB for dBm)	
Square, SMPTE/DIN, and Burst (if ⩾50 kHz) functions	±3.0% (0.3 dB for dBm)	
CCIF	±5.0% (0.5 dB for dBm)	
TYPICAL AMPLITUDE SETTLING TIME		Less than 500 ms for frequencies above 50 Hz, increasing to approximately 1 sec at 10 Hz.
DC OFFSET (Maximum Output) Balanced Unbalanced	 ⩽25 mV ⩽15 mV	
SIGNAL BALANCE RATIO (Balanced mode only)		At least 60 dB (CCITT Recommendation 0.121) from 20 Hz to 20 kHz for output levels greater than or equal to −10 dBm.
	OTHER OUTPUTS	
SYNC OUTPUT		LSTTL compatible signal designed to give stable oscilloscope display of main output signal in all internally generated modes.
Sine, Square functions	Squarewave at main output frequency.	
SMPTE/DIN function	Squarewave at lower (IM) frequency.	

Table 1-2 (cont)
ELECTRICAL CHARACTERISTICS

Characteristics	Performance Requirements	Supplemental Information
	OTHER OUTPUTS	
CCIF function	Squarewave at IM (1/2 of difference) frequency.	
Burst function	High when burst output is on, low when burst output is off.	
RAMP OUTPUT		0 to 10 V stairstep ramp enabled during sweep mode. 0 V corresponds to start parameter and 10 V to stop parameter. Number of steps equals selected N. Output impedance is approximately 1 k ohm.
PEN LIFT OUTPUT		Standard LSTTL output. Output designed to enable frequency and amplitude sweeps with no switching transients on XY recorder.
	REAR INTERFACE INPUT/OUTPUT	
SYNC OUTPUT		Pins 27B, 28B. Same as front panel sync output.
BURST GATE INPUT		Pins 24B, 24A. Same as front panel Burst Gate input.
RAMP OUTPUT		Pins 25A, 25B. Same as front panel Ramp output.
PEN LIFT OUTPUT		Pins 26A, 26B. Same as front panel Pen Lift output.
MAIN OSCILLATOR SYNC OUTPUT		Pins 15B, 14B. LSTTL level output at frequency of main oscillator.
EXTERNAL 1 MHz INPUT		Pins 14A, 15A. Buffered input for allowing external 1 MHz ±0.01% or better reference.

[a] 80 kHz bandwidth limited

[b] Any individual harmonic

[c] With 50 ohms output impedance. For other output impedance selections subtract 1.25 dB for 150 ohms, and 5.35 dB for 600 ohms.

Table 1-3
MISCELLANEOUS

Characteristics	Performance Requirements	Supplemental Information
INTERNAL POWER SUPPLIES		
Floating ±17 V		±17.0 V ±0.4 V
Floating ±15 V		±15.0 V ±0.3 V
+12.6 V		+12.6 V ±0.6 V
−12.0 V		−12.0 V ±0.6 V
+5 V		+5.15 V ±0.1 V
FUSE DATA		
F3020		0.1 A FB, 3 AG, 250 V
F4021		0.125 A FB, 3 AG, 250 V
F2022, F2020		0.6 A SB, 3 AG, 250 V
F4022		3 A FB, 3 AG, 250 V
POWER CONSUMPTION		Typically 30 to 35 W incremented line draw in TM 5000-Series power modules.
WARM-UP TIME		20 minutes. 60 minutes after storage or exposure to high humidity environments.
Recommended Calibration Interval		2000 hours or 12 months

TABLE A
DISPLAYED AND PROGRAMMED VRMS RESOLUTION

Selected Vrms Amplitude	Resolution
10.02 to 21.20 V	0.020 V or 20 mV
5.01 to 10.00 V[a]	0.010 V or 10 mV
2.005 to 5.000 V	0.005 V or 5 mV
1.002 to 2.000 V	0.002 V or 2 mV
0.501 to 1.000 V	0.001 V or 1 mV
200.5 to 500.0 mV	0.5 mV
100.2 to 200.0 mV	0.2 mV
50.1 to 100.0 mV	0.1 mV
20.05 to 50.00 mV	0.050 mV or 50 μV
10.02 to 20.00 mV	0.020 mV or 20 μV
5.01 to 10.00 mV	0.010 mV or 10 μV
2.005 to 5.000 mV	0.005 mV or 5 μV
1.002 to 2.000 mV	0.002 mV or 2 μV
0.200 to 1.000 mV	0.001 mV or 1 μV

[a]10.60 for unbalanced mode.

Table 1-4
ENVIRONMENTAL[a]

Characteristics	Description	
Temperature		Meets MIL-T-28800C, class 5.
Operating	0°C to +50°C [d]	
Non-operating	−40°C to 75°C	
Humidity	95% RH, 0°C to 30°C 75% RH, to 40°C 45% RH, to 50°C	Meets MIL-T-28800C, class 5.
Altitude		Exceeds MIL-T-28800C, class 5.
Operating	4.6 km (15,000 ft)	
Non-operating	15 km (50,000 ft)	
Vibration	0.38 mm (0.015″) peak to peak, 5 Hz to 55 Hz, 75 minutes.	Meets MIL-T-28800C, class 5, when installed in qualified power modules.[b]
Shock	30 g's (1/2 sine), 11 ms duration, 3 shocks in each direction along 3 major axes, 18 total shocks.	Meets MIL-T-28800C, class 5, when installed in qualified power modules.[b,c]
Bench Handling (Plug-in only)	12 drops from 45°, 4″ or equilibrium, whichever occurs first.	Meets MIL-T-28800C, class 5.
Packaged Product Vibration and Shock (Plug-in only)	Qualified under National Safe Transit Association Preshipment Test Procedures 1A-B-1 and 1A-B-2.	
Electromagnetic Interference	Within limits of F.C.C. Regulations, Part 15, Subpart J, Class A; and MIL-STD-461B (April 1, 1980) Class B.	
Electrostatic Immunity	At least 15 kV discharge from 500 pF in series with 100 ohms to instrument case or any front panel connector without damage or permanent performance degradation.	

[a]With TM 5000-Series power module. System performance subject to exceptions of power module or other individual plug-ins.

[b]Refer to TM 500/5000 power module specifications.

[c]Requires power module retainer bar or clip.

[d]Operation above +40°C not recommended in TM 500-Series power modules.

Table 1-5
PHYSICAL CHARACTERISTICS

FINISH	
Front Panel	Polycarbonate
Chassis	Chromate conversion-coated aluminum
NET WEIGHT (Nominal)	
Plug-in only	5.5 lbs (2.5 kg)
ENCLOSURE TYPE AND STYLE	MIL-T-28800C, type 3, style E package with power module, (Style F in rackmount power module).
OVERALL DIMENSIONS (Nominal)	
Height	126.01 mm (4.96 in.)
Width	134.47 mm (5.29 in.)
Length	288.34 mm (11.35 in.)

OPERATING INSTRUCTIONS

Introduction

This section of the manual provides installation and removal instructions and describes the functions of the SG 5010 front-panel controls and connectors. Operators familiarization information is also provided as an aid in understanding how to operate the SG 5010 under local (manual) control only.

NOTE

The information in this section assumes the instrument is not connected to the GPIB via the power module.

Complete information for programming the SG 5010 via the GPIB (General Purpose Interface Bus) is found in the Programming section of this manual.

PREPARATION FOR USE

Installation and Removal

The SG 5010 is calibrated and ready for use when received. Make certain the line selector block on the power module is positioned correctly. The SG 5010 is designed to operate in a TM 5000-Series power module. It can also operate under local (manual) control only, in a TM 500-Series power module; however, minor mechanical changes must first be made to the instrument. Refer qualified personnel to the Maintenance section of this manual for instructions on making the modifications for operation in a TM 500 Series power module.

CAUTION

To prevent damage to the SG 5010, turn off the power module before installing or removing the instrument. Do not use excessive force to install or remove.

Check to see that the plastic barriers on the interconnecting jacks of the selected power module compartments match the cutouts in the SG 5010 rear interface connectors. If they do not match, do not install the SG 5010 until the reason is investigated. When the units are properly matched, align the SG 5010 chassis with the upper and lower guides of the selected compartments (see Fig. 2-1). Push the SG 5010 chassis in and press firmly to seat the rear-interface connectors in the interconnecting jacks. Apply power to the SG 5010 by operating the power switch on the power module.

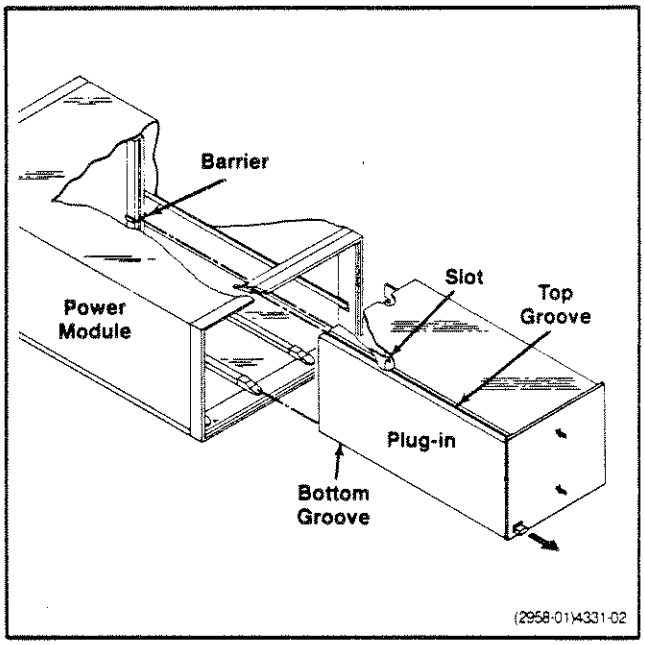


Fig. 2-1. Plug-in installation and removal.

To remove the SG 5010 from the power module, pull out on the release latch (located in the lower left corner) until the interconnecting jacks disengage and the SG 5010 slides out.

Repackaging For Shipment

If the instrument is to be shipped to a Tektronix Service Center for service or repair, attach a tag listing the owner (with address), and the name of an individual at your firm that can be contacted. Include complete instrument serial number and a description of the service required.

If the original package is unfit for use or unavailable, repackage the instrument as follows:

Surround the instrument with polyethylene sheeting or other suitable material to protect the exterior finish. Obtain a carton of corrugated cardboard of adequate strength and having inside dimensions no less than six inches more than the dimensions of the instrument.

Cushion the instrument by tightly packing dunnage or urethane foam between the carton and instrument, on all sides. Seal the carton with shipping tape or an industrial stapler.

The carton test strength for this instrument is 200 lbs.

FRONT PANEL CONTROLS, CONNECTORS AND DISPLAY

All controls necessary for local operation of the SG 5010 are located on the instrument front-panel. Many pushbuttons illuminate to provide visual indication that associated functions are active. A brief description of these controls and indicators follows. Refer to Fig. 2-2.

DISPLAY INDICATORS

The SG 5010 uses seven-segment LED's to display a numerical value of up to five digits. In addition, LED indicators in the right area of the display window illuminate, when appropriate, to indicate units of measure for parameters, GPIB operation, and error events.

PARAMETER UNITS OF MEASURE

Units for the displayed value are defined by an illuminated units indicator in the readout window. These units are:

Hz	**kHz**
dBm	**OHM**
V	**mV**
SEC	**CYC**

GPIB INDICATORS

REM—Illuminates when the instrument is operating under remote control via the GPIB.

ADRS—Illuminates when the instrument is addressed via the GPIB.

ERROR INDICATORS

ERR—Illuminates when the instrument has detected an error in keyboard entry or some other operating error. Pressing CLEAR clears the displayed operation or entry error. A three digit numerical code (300-series) displayed in the readout window indicates an internal instrument malfunction (see Table 3- , Error Codes and Events in the Programming section of this manual). Refer any error condition codes for internal errors to qualified service personnel.

ENTR—Flashes when a numerical entry is started using the front panel numerical keyboard. Stops flashing when a valid entry is accepted.

PLL—Illuminates when the frequency synthesizer unlocks.

CUR—Illuminates when the output amplifier current limits or the voltage clips.

CONTROLS AND CONNECTORS

The following list describes the SG 5010 front panel controls and connectors. Refer to Fig. 2-2. Secondary pushbutton functions (shown on the instrument front panel to the right of the associated pushbuttons) are listed in this description with their associated primary functions.

(1) FUNCTION

The pushbuttons in this group illuminate when the associated function is active. These functions are mutually exclusive. The parameter buttons set the amplitude and frequency for the selected function.

SINE

Selects the sine wave signal for output.

SQUARE

Selects the square wave signal for output.

SMPTE/DIN

Selects the SMPTE/DIN signal for output. This intermodulation test signal consists of a lower (IM) frequency sine wave mixed with the main frequency sine wave in a 4 to 1, or 1 to 1 amplitude ratio. The ratio is selected by pressing RECALL, then pressing SMPTE/DIN. The main frequency is set using the FREQ parameter and numeric buttons; the IM FREQ button sets the frequency of the lower tone.

CCIF

Selects the CCIF signal for output. This signal consists of two equal amplitude sine waves with a constant frequency offset. The FREQ parameter sets the center frequency; the IM FREQ parameter sets the upper and lower offset frequency.

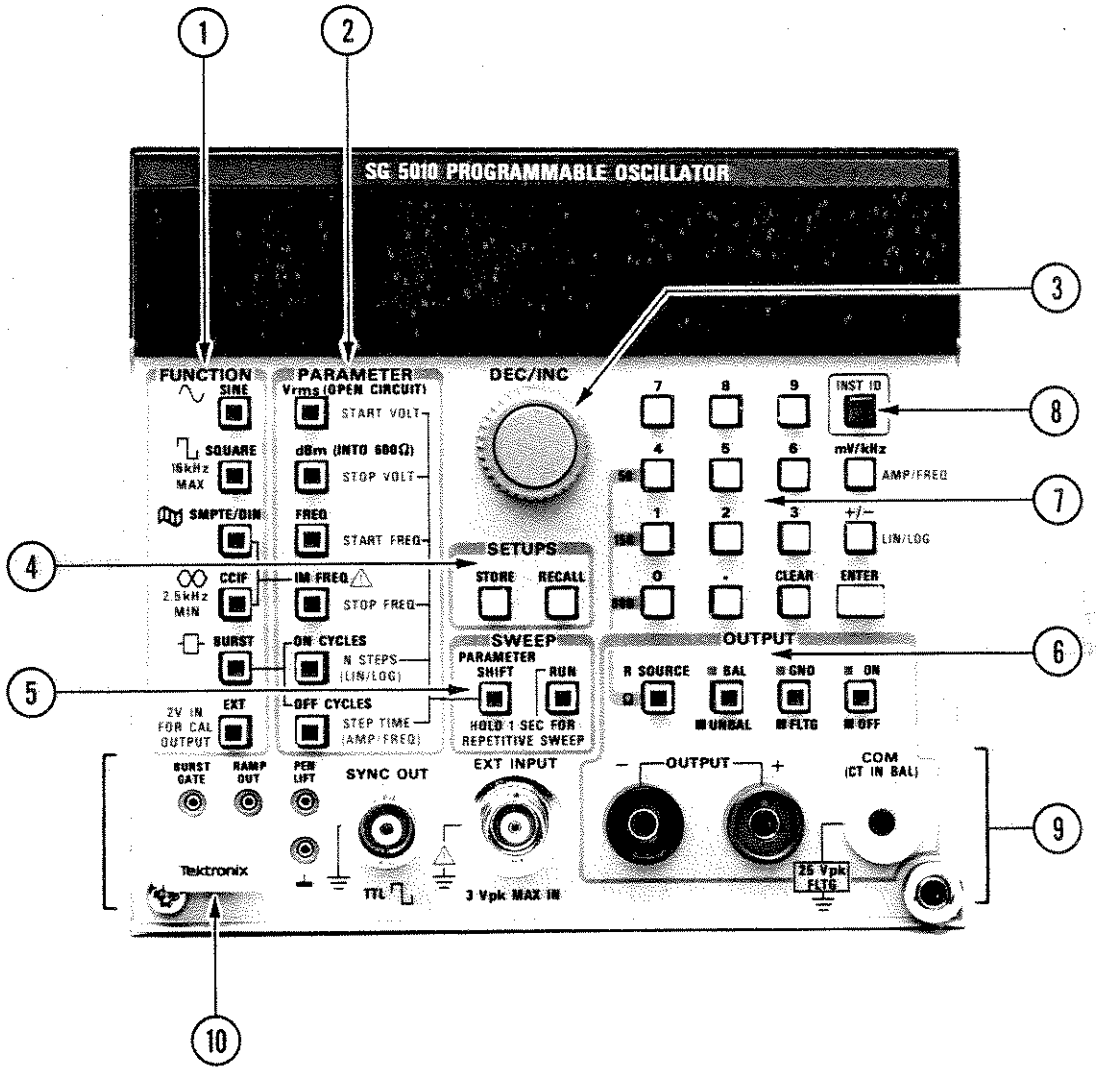


Fig. 2-2. SG 5010 front panel controls and connectors.

BURST

Selects the burst signal for output. This signal provides a sine wave during the *on* portion of the signal, at the selected frequency and amplitude. During the *off* portion of the signal, the sine wave amplitude can be set to 0 or 10% of the amplitude selected for the *on* portion. The amplitude percentage is changed by pressing RECALL, then pressing BURST.
OFFCYCLES and ONCYCLES set number of cycles; OFFCYCLES value enables gated or single burst operation.

EXT

Selects the signal applied to the EXT IN connector for output. A 2 Vrms input provides a calibrated output signal.

(2) PARAMETER

Each pushbutton in this group enables either a primary or secondary parameter; the current value and units for the selected parameter are indicated in the display window. These pushbuttons are mutually exclusive.

To enable a primary parameter (nomenclature above button), press the associated parameter button. The button for the selected primary parameter illuminates.

To enable a secondary parameter (nomenclature to the right of button), press the PARAMETER SHIFT button before pressing the desired parameter button. Both the selected parameter button and the PARAMETER SHIFT button illuminate.

The value of the selected parameter (primary or secondary) may be changed by entering a new value (using the numeric keyboard and pressing ENTER) or adjusted by rotating the DEC/INC control. The units buttons (secondary functions of some numeric buttons) alternate the units.

Vrms (START VOLT)

dBm (STOP VOLT)

Allows the operator to set the amplitude of the output signal in volts rms open circuit, or dBm into an assumed 600 Ω load. The maximum output is 10.6 Vrms (+22.05 dBm) unbalanced, and 21.2 Vrms (+28.05 dBm) balanced. The dBm display compensates for the source impedance, assuming a 600 Ω load. The voltage displayed is the open circuit voltage.

Units are volts rms or millivolts rms (mV/kHz button), or decibels, depending upon the parameter selected.

START VOLT (secondary parameter) sets the starting amplitude in Vrms for the sweep mode; STOP VOLT sets the final amplitude of the swept waveform.

FREQ (START FREQ)

Allows the operator to set the main frequency of the output signal (except EXT) using Hz or kHz units.

START FREQ (secondary parameter) sets the frequency at which the sweep begins. Units are Hz, or kHz (mV/kHz button).

IM FREQ *triangle* (STOP FREQ)

Allows the operator to set the low or offset frequency for the SMPTE/DIN and CCIF functions. In the SMPTE/DIN function, the IM FREQ is the frequency of the lower tone. In the CCIF function, the IM FREQ is one-half of the difference frequency between the two test tones. Frequency can be 40, 50, 60, 80, 100, 125, or 500 Hz. The instrument rounds off an entered frequency to the nearest legal frequency, unless the entry is beyond specified limits; the latter causes the ERR button to light and the entry is not accepted.

STOP FREQ (secondary parameter) sets the frequency at which the sweep stops.

ON CYCLES (N STEPS, LIN/LOG)

Allows the operator to set the number of *on* cycles for the BURST function. The minimum is 1; maximum is 65,535.

N STEPS (secondary parameter) sets the number of steps (1 to 99) from START FREQ to STOP FREQ. In addition, a linear or logarithmic type of sweep can be selected (LIN/LOG button). The selected sweep type is indicated by Li or Lo in the display window.

OFF CYCLES (STEPTIME, AMP/FREQ)

Allows the operator to select the number of *off* cycles for the BURST function. Minimum number is 1; maximum is 65,535. Selecting 0 enables gated burst operation using the BURST GATE input. Selecting 99999 enables triggered burst operation using the BURST GATE input.

STEPTIME (secondary parameter) sets the time (in seconds) for each SWEEP step. The minimum time is 0.1 seconds; maximum is 25.0 seconds, in increments of 0.1 seconds. The sweep mode (amplitude or frequency) is selected by pressing AMP/FREQ.

(3) DEC/INC

Varies the value of the selected parameter. Rate of change is proportional to the rate at which the control is turned. Resolution at slow rotation speeds is 100 changes per rotation.

(4) SETUPS

STORE

Stores the current settings in the user-definable storage location specified. Ten locations (0 through 9) are available. All settings are stored except DT, RQS, USEREQ, ADDRESS, PLI, and CLI (programmed internal parameter settings). Stored settings are retained in memory when the instrument is powered down.

RECALL

Recalls instrument settings from the specified storage location (0 through 9) and configures the instrument to those settings. If the recalled location is undefined (no settings stored in location specified), the following front panel settings are recalled:

FUNCTION:	SINE: on
PARAMETER:	Vrms: 1 IM FREQ: 60 Hz ON CYCLES: 10 Hz OFF CYCLES: 90 Hz FREQ: 10 kHz START VOLT: 0.1 Vrms STOP VOLT: 10.0 Vrms START FREQ: 20 Hz STOP FREQ: 20 kHz N STEPS: 30, Logarithmic sweep type STEPTIME: 1, FREQ sweep mode
SWEEP:	RUN: off
OUTPUT:	R SOURCE: 600 BAL/UNBAL: BAL on GND/FLTG: GND on ON/OFF: OFF

These settings are also recalled by pressing RECALL and then the decimal point button.

(5) SWEEP

PARAMETER SHIFT

Enables selection of one of the secondary sweep parameters: START VOLT, STOP VOLT, START FREQ, STOP FREQ, N STEPS, and STEPTIME. This button must be pressed before each press of a parameter button in order to select its secondary parameter function. The current value for the secondary parameter and its units are then displayed in the display window. The value may be changed using the numeric keyboard and pressing ENTER or by rotating the DEC/INC control.

RUN

Starts a frequency or amplitude sweep sequence. Momentarily pressing the RUN button initiates a single sweep. If held down for more than 1 second, the sweep repeats. Pressing the button during a sweep stops the sweep. The RUN button illuminates while a sweep is in progress. It blinks at the start of each sweep sequence for repetitive sweeps.

(6) OUTPUT

R SOURCE

Allows the operator to select the SG 5010 source impedance of 50, 150, or 600 Ω (numeric buttons 4, 1, and 0). The display indicates the current value. The R SOURCE button illuminates while the source impedance is displayed.

BAL/UNBAL

Selects balanced or unbalanced output. The button illuminates during balanced operation.

GND/FLTG

Selects grounded or floating output. The button illuminates during grounded operation.

ON/OFF

Turns the output signal on or off at the output connectors. The button illuminates while the output is on. The selected source impedance is maintained while the output is off. At power-up, the output is always set to the *off* state.

(7) Numeric Pushbuttons

0 through 9, Decimal Point, +/- (LIN/LOG)

Used to enter a numeric value for the selected PARAMETER, R SOURCE, or GPIB address.

While the parameter N STEPS is selected, LIN/LOG sets the sweep to the linear or logarithmic mode. Li or Lo in the LED display indicates the current sweep mode.

mV/kHz (AMP/FREQ)

Alternately sets the units of a numeric entry (before ENTER is pressed) for Vrms amplitude to V or mV; either V or

mV illuminates in the display window, indicating the selected units.

While the secondary parameter STEPTIME is selected, sets the sweep mode to sweep amplitude or frequency.

CLEAR

Used before ENTER is pressed to cancel a numeric entry and to reset the display.

After ENTER is pressed, clears a settings entry error and resets the display to the last legal value.

Also used after STORE or RECALL is pressed to cancel the STORE or RECALL operation and reset the display.

ENTER

Enters a valid numeric entry into the current operating setup. Pressing ENTER is not required when selecting a source impedance, or when STOREing or RECALLing settings.

(8) INST ID

Causes the SG 5010 to display its GPIB address, and if USER REQUEST and RQS commands are enabled, generates a Service Request (SRQ) over the GPIB. This button is also used with the RECALL button to change the GPIB address. Refer to Section 3, Programming.

(9) CONNECTORS

BURST GATE

Input connector for TTL trigger signal to initiate burst signal generation (in BURST trigger mode), or to gate the output signal (in BURST gated mode).

RAMP OUT

Provides a staircase ramp voltage that corresponds to the sweep steps. Ramp begins at 0 V for the sweep start and ends at 10 V for the sweep stop. The number of steps between 0 and 10 V equals the selected number of sweep steps.

PEN LIFT

Provides a TTL signal that goes low during frequency or amplitude transitions in a sweep. When plotting frequency response or distortion on an XY display or XY plotter, this can be used to blank the display or lift the pen, thus avoiding plotting aberrations.

SYNC OUT

Provides a TTL signal at the frequency and phase of the sine or square wave, low frequency of the IM signals, the envelope of the burst signal, or a squared version of the external input signal.

EXT INPUT *Triangle*

Differential input which is connected to internal gain and output attenuation circuits when the EXT function is selected.

+/− OUTPUT, COM

Banana jack connectors carrying the output signal. The − and + OUTPUT connectors carry the output signal in both balanced and unbalanced modes. The COM connector provides access to the CT in the balanced mode and is tied to the − OUTPUT connector in the unbalanced mode.

Chassis Ground

Chassis ground connector.

(10) Release Latch

Pull to remove plug-in.

OPERATORS FAMILIARIZATION

General Operating Information

With the SG 5010 properly installed in the power module, allow twenty minutes warmup time for operation to specified accuracy; 60 minutes after storage in or exposure to a high humidity (condensing) environment.

Power-up Sequence

When powered up, the SG 5010 performs a diagnostic self-test to check the functionality of the instrument ROM and RAM, and some hardware circuits. It also illuminates all front panel LED and indicators. If a self-test error is detected, a three digit error code appears in the readout window, indicating an internal malfunction. Should this occur, refer the condition to qualified service personnel. The SG 5010 does not respond to front panel controls until the error is cleared. Pressing the CLEAR button clears the error code from the readout window and allows the instrument to complete initialization, but does not clear the condition causing the error code.

Upon successful completion of the self-tests, the SG 5010 initializes its settings as listed below:

Setting		Description
FUNCTION:	SINE: on	Sine wave function is enabled.
PARAMETER:	Vrms: 1	Amplitude of selected function waveform,in Vrms.
	IM FREQ: 60	Frequency of the lower SMPTE/DIN tone, or one-half of the difference frequency between the two test tones for the CCIF function.
	ON CYCLES: 10	Number of *on* cycles for the BURST function.
	OFF CYCLES: 90	Number of *off* cycles for the BURST function.
	FREQ: 10 kHz	Main frequency.
	START VOLT: 0.1	Starting amplitude in Vrms for an amplitude sweep of the selected function.
	STOP VOLT: 10.0	Amplitude in Vrms at which an amplitude sweep of the selected function stops.
	START FREQ: 20	Frequency in Hz at which a frequency sweep of the selected function starts.
	STOP FREQ: 20000	Frequency in Hz at which a frequency sweep of the selected function stops.
	N STEPS: 30, Lo	Number of steps from the beginning to the end of a frequency or amplitude sweep. Sweep is logarithmic.
STEPTIME:	1, FREQ	Time in seconds for each step of a frequency sweep.
SWEEP:	RUN: off	Sweep is off.
OUTPUT:	R SOURCE: 600	Selected source impedance.
	BAL/UNBAL: BAL on	Output is balanced.
	GND/FLTG: GND on	Output is grounded.
	ON/OFF: OFF on	Output is off.

These settings can also be recalled by pressing RECALL and then the decimal point button. This feature allows the operator to quickly configure the instrument settings to a known state, and then make setting changes to produce the desired output.

Additional internal settings are also initialized; these relate to GPIB operation and are described in the programming section of this manual.

Function and Parameter Selection

The SG 5010 generates five waveforms: sine wave, square wave, SMPTE/DIN intermodulation test signal, CCIF intermodulation test signal, and sine wave burst. The frequency range for each function is specified in the Specification section of this manual.

To select a waveform for output, press the appropriate function button. Each function allows setting the value of certain primary parameters. The names of primary parameters are shown above the associated parameter button. Secondary parameters are named to the right of the parameter buttons; these parameters set values used for the sweep and burst modes. The waveform for each function (except EXT) can be swept linearly or logarithmically in frequency or amplitude.

Primary Parameters. The current value of a primary parameter can be displayed in the readout window by pressing the parameter button. Press CLEAR to reset the display.

To change the value or units of a primary parameter, press the parameter button to display the current value. Next, turn the DEC/INC control to increment or decrement the displayed value, if the parameter value can be varied, such as FREQ, Vrms, or dBm. Or press the numeric buttons representing the desired value, most significant digit first; the numbers appear in the window, as they are entered.

Next, select the units for the parameter value; then press ENTER. The readout window displays the value and units entered for the parameter, if the value is within specified limits. A value outside limits is ignored, the ERR indicator illuminates, and the last legal value is displayed. After setting a parameter, press CLEAR to reset the display.

The units for the Vrms parameter are V or mV. The units for the FREQ and IM FREQ parameters are Hz or kHz. The mV/kHz button changes the units to the alternative units used for the parameter being set.

Secondary Parameters. To display a secondary parameter value, press the PARAMETER SHIFT button, and then

the secondary parameter button. While a secondary parameter is displayed, its value or units can be changed using the procedure described for primary parameters.

Each parameter value can be entered using either of two units. The units for START VOLTS and STOP VOLTS can be set to V or mV. The units for START FREQ and STOP FREQ can be set to Hz or kHz. In addition, while N STEPS is displayed, the sweep type can be set to a linear or a logarithmic sweep, using the LIN/LOG button. Li or Lo is shown in the readout window to indicate the current sweep type. While STEPTIME is displayed, the sweep mode can be set to sweep amplitude or frequency, using the AMP/FREQ button.

Output Connections

CAUTION

To avoid damage to the SG 5010 *circuitry, do not apply a voltage exceeding ±25 V peak, with respect to chassis ground, to any front panel connector or to rear interface connector pins 14A-28A and 14B-28B.*

The SG 5010 is designed as a balanced source of audio test signals. In the BALanced mode, it is intended to be used in systems where the load is also balanced or differential. The balanced configuration is preferable in high quality audio applications because of its inherently superior rejection of common mode signals, such as induced hum or RF voltage. See Fig. 2-3A and 2-3B. The SG 5010 can also be used to drive unbalanced or single-ended loads. In this case, UNBAL mode is selected, the − OUTPUT is internally connected to COM (no need to move output cable connector), and the output voltage and the source resistance remain at the selected values. Note that the maximum output voltage in UNBAL mode is only one-half of the maximum BALanced output voltage. Driving unbalanced loads from the full balanced output is not recommended because of possible degradation due to common mode signals such as power line hum or noise spikes coupling across the output resistance. See Fig. 2-3C. Even when the SG 5010 is floating, unavoidable stray capacitances within the instrument and those associated with external cabling can cause small amounts of these common mode signals to couple to the load. This is true even though internal stray capacitances have been minimized through the use of a double-shielded power transformer and are balanced between the two outputs. The coupling magnitude is independent of the oscillator's output attenuation and will become progressively worse as output amplitude is reduced. Thus, the common mode noise may dominate any distortion products in the system, especially at lower output levels. The stray capacitance can also adversely affect high frequency flatness. If the SG 5010 GND pushbutton selects GND in this configuration, then half the output voltage is short-circuited. For these reasons, it is recommended that you select UNBAL output when driving an unbalanced load.

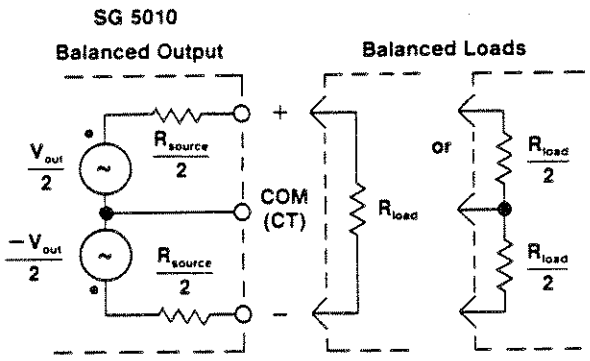
The GND-FLTG pushbutton either connects the COM connector (common or CT) to chassis ground through approximately 30 Ω or disconnects the COM from chassis ground.

Normally the SG 5010 is floated to break up any ground loops between it and the load. Standard practice is to ground all sources (microphones, etc.) at the unit under test (console, etc.). See Fig. 2-4.

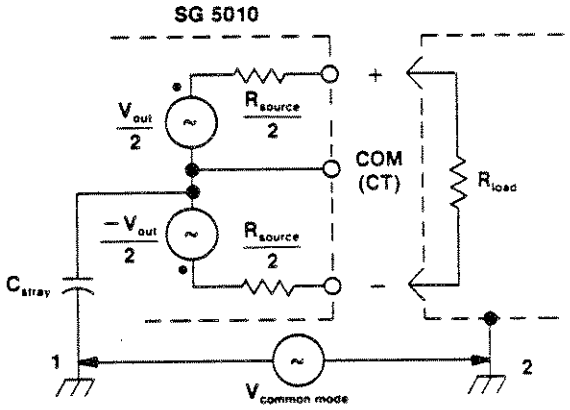
Under some conditions, it may be desirable to ground the SG 5010 CT connector. This may be true in a high RF environment to prevent the CT from floating on RF induced in the output cables. If it is of sufficient amplitude, such RF may otherwise degrade the linearity of the SG 5010 output stages. The best procedure under high RF environments is to use high-quality shielded cable. Connect the shield to the SG 5010 CT terminal with a high quality 0.01 to 0.1 μF capacitor connected between the COM terminal and the chassis ground post. The RF is effectively coupled to ground, while at low frequencies the SG 5010 still floats to break up ground loops. See Fig. 2-5. As an alternative, the GND-FLTG pushbutton can be pushed to GND with the cable's shield connected to the ground post. Double-shielded cable will improve rejection of RF interference. See Fig. 2-6. Under worst-case conditions, use three-conductor twisted, shielded cable (double-shielded is preferred) with the shield connected to the chassis ground post and the three conductors connected to the + and − OUTPUT and COM connectors. Ground the COM wire to the ground of the unit under test (console) and float the SG 5010. The popular XLR connector allows this type of connection. See Fig. 2-7.

The square wave at the SYNC OUT connector is in phase with the + OUTPUT and is designed for use as an external trigger for a counter, oscilloscope, or other device. This output has a source impedance of 1 kΩ, and is always referenced to chassis ground (even when the main OUTPUT is floating).

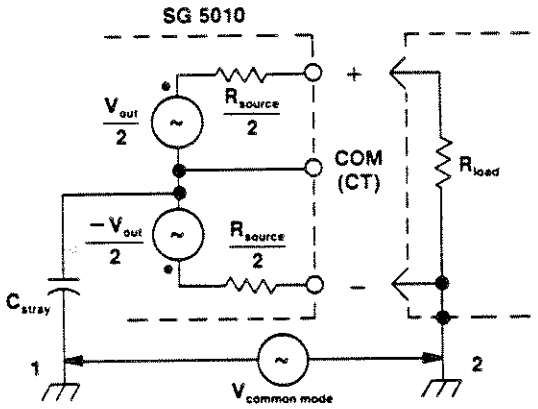
With either SMPTE/DIN or CCIF intermodulation modes selected, the signal at the SYNC OUT connector is replaced by a square wave at the selected low frequency.



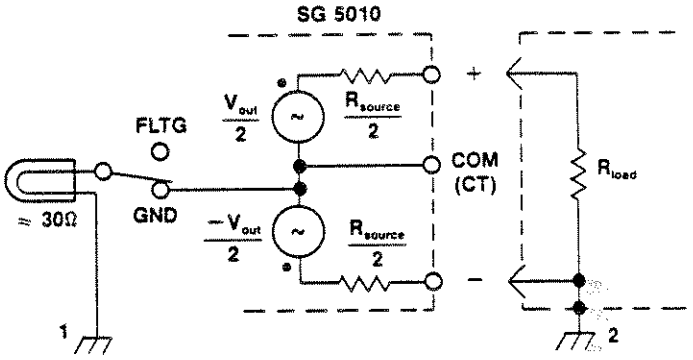
A. A balanced system = balanced source + balanced load.



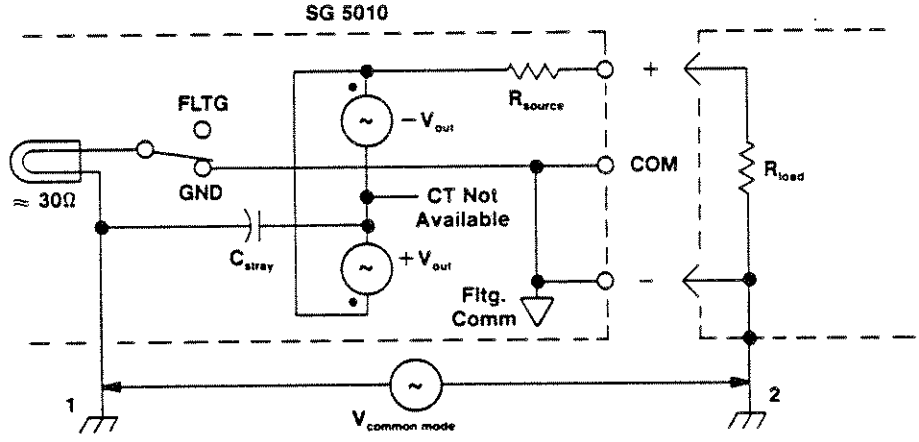
B. Common mode noise coupled in by stray capacitance; does not affect balanced load.



C. Grounded load; common mode noise appears across 1/2 R_{SOURCE}.



D. Single-ended load with GND-FLTG pushbutton activated, connecting CT to chassis ground. The − BALANCED OUTPUT is effectively short-circuited. Avoid this condition!



E. Single-ended load with single-ended source; common mode signal does not appear at load. Internal switching parallels generator halves and connects − OUTPUT to COM terminal.

4331-04

Fig. 2-3. Connection configurations.

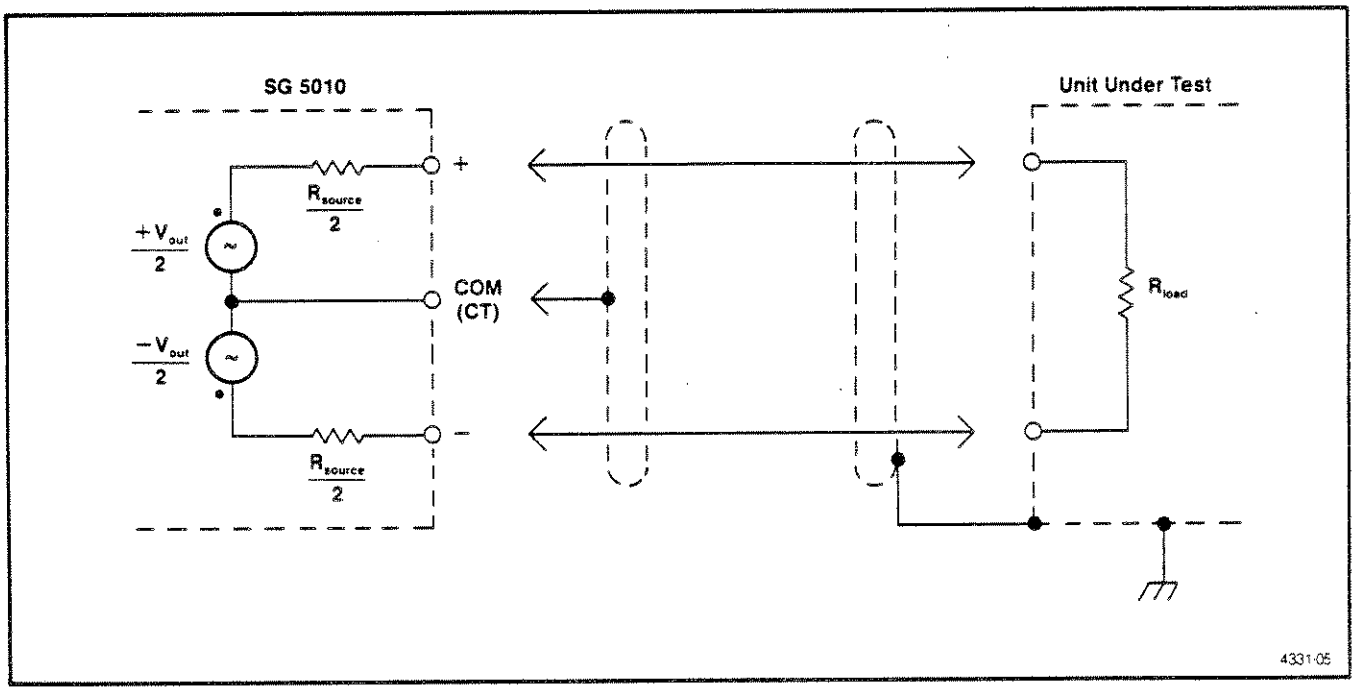


Fig. 2-4. Floating oscillator grounded to unit under test to break up ground loops.

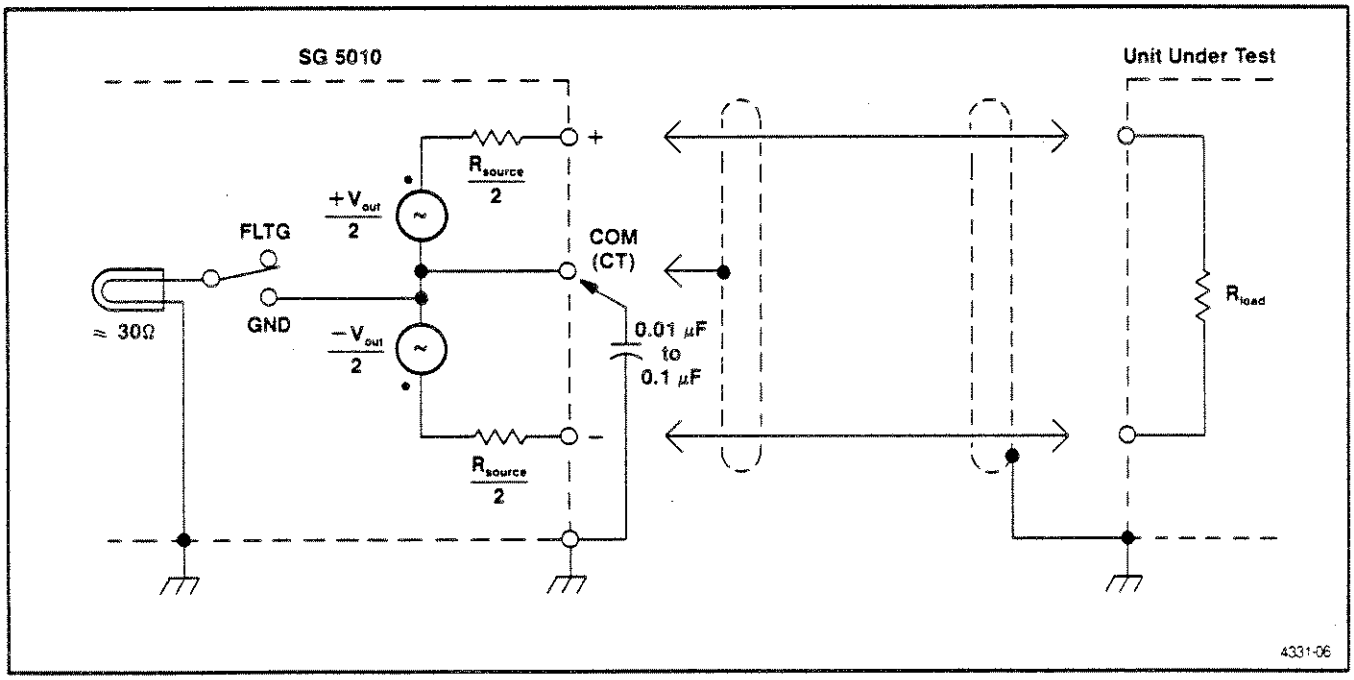


Fig. 2-5. Added capacitor between CT and chassis ground improves RFI rejection.

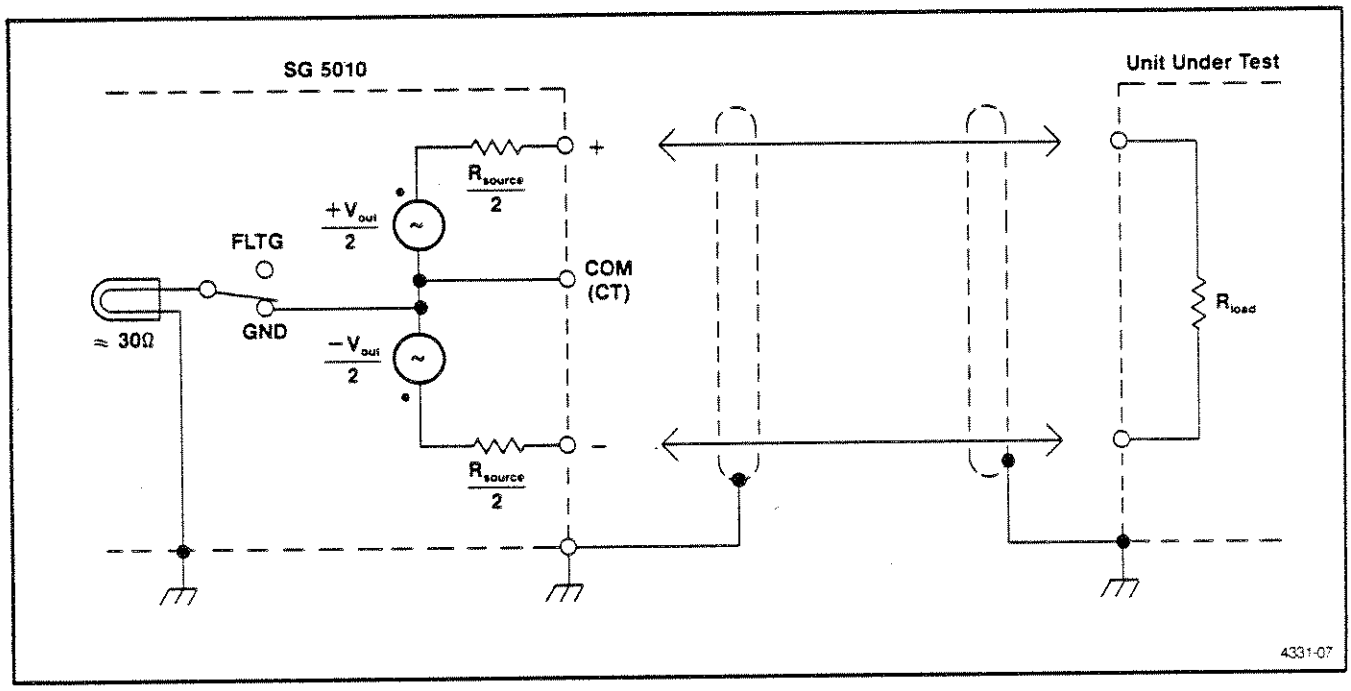


Fig. 2-6. SG 5010 COM terminal grounded and cable shield connected to ground post. Reduces RF interference but may cause low frequency ground loop.

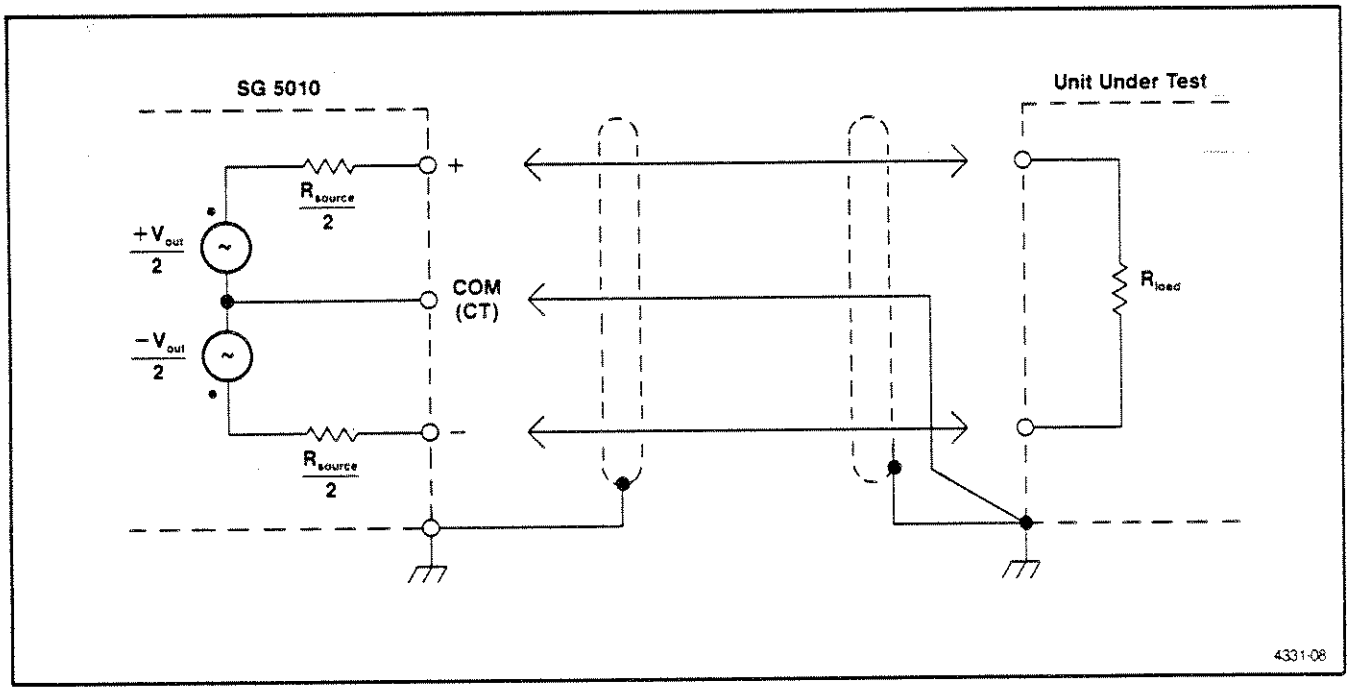


Fig. 2-7. Three conductor shielded cable allows CT to be remotely grounded while cable shield is grounded at both ends.

OPERATING PROCEDURES

1. Restoring default settings.
2. Acquiring and restoring full setup in ASCII.
3. Acquiring and restoring full setup in binary.
4. Saving and restoring front-panel settings in SG 5010 memory.
5. Output signal on/off.
6. Controlling output impedance.
7. Monitoring output overload.
8. Generating a frequency sweep.
9. Generating an amplitude sweep.
10. Generating an interrupt at end of sweep.
11. Controlling burst signals.
12. Disabling interrupts.
13. Operator (front-panel) interrupt.
14. Interrogating firmware level.

These procedures suggest how to use SG 5010 commands in a program, but do not repeat all the information about commands that are used. See the command descriptions earlier in this section for command details.

1. Restoring Default Settings

Purpose:

Restore default (preprogrammed) state of the instrument functions.

Action:

Send to the SG 5010: **INit**

Comments:

This is a simple way to restore SG 5010 settings including interrupt control to a known state (see INIT command). If most, but not all, functions are to be set to default states, add the ones to be changed. For example:

Send to the SG 5010: **INit;FReq 15.E+3**

INit settings are not restored at power-up—the SG 5010 remembers its front-panel settings at power-down.

2. Acquiring and Restoring Full Setup in ASCII

Purpose:

Acquire full SG 5010 setup so it can later be transmitted to SG 5010 to restore that setup.

Action:

Dimension string variable (280 characters min)
Send to SG 5010: **SETtings?**
Input SG 5010 response to string variable
.
.
.
Send to SG 5010: contents of string variable

Comments:

Saving SG 5010 setups allows desired known states of instrument to be restored at a later time. (This capability is implemented as INIT to restore power-up state.)

3. Acquiring and Restoring Full Setup in Binary

Purpose:

Acquire full SG 5010 setup using minimum data transfer and storage; settings are later transmitted to SG 5010 to restore the setup.

Action:

Dimension variable for at least 50 bytes
Send to SG 5010: **LLset?**
Input SG 5010 response to variable
.
.
.
Send to SG 5010: contents of variable

Comments:

The header "LLSET" is contained within the response to "LLset?", so it need not be inserted ahead of the contents of the variable sent to the SG 5010. Data bytes are 8 bit binary and must either be stored as elements of a numerical integer array or a string variable (capable of handling ASCII with Parity Bit 8).

The controller should be set to respond to EOI only so it does not terminate input if it sees the code for CR, LF or any other usual terminating character as part of the binary data.

4. Storing and Recalling Front-Panel Settings in SG 5010 Memory

Purpose:

Store SG 5010 front-panel setup in internal SG 5010 memory and later restore the setup.

Action:

Send to SG 5010: **STORe** <num>

.
.
.

Send to SG 5010: **REcall** <num>

Comments:

Sweep and output are set to off when settings are recalled, even if they were on at time the settings were stored.

5. Output Signal On/Off

Purpose:

Turn output signal on and off (SG 5010 powers on with output off).

Action:

Send to SG 5010: **OUt ON**

.
.
.

Send to SG 5010: **OUt OFF**
or
Send to SG 5010: **OUt ON**

.
.
.

Send to SG 5010: **AMp 0:Vrms**
or
Send to SG 5010: **AMp 0:Vpp**

Comments:

Setting the amplitude to zero is faster than turning off the output (opening the output relay). However, setting the amplitude to zero does not disconnect the output amplifier as does OUT OFF so the SG 5010 will attempt to hold the output at zero volts.

See also Controlling Burst Signals for how to gate the output on and off.

6. Controlling Output Impedance

Purpose:

Set the SG 5010 output impedance to 50, 150, or 600 Ω.

Action:

Send to SG 5010: **RSource** <num>

7. Monitoring Output Overload (unregulated amplitude)

Purpose:

Report unregulated output amplitude caused by overload. The first procedure uses the current-limit interrupt; an alternative does not enable the interrupt, but polls the current-limit mode.

Action:

Include SRQ handler that recognizes and handles status code 196 (out of current limit) and status code 197 (into current limit)
and
Enable and link SRQ handler
and
Send to SG 5010: **CLi ON**

Alternative (without interrupt):

Send to SG 5010: **CLi?**
Input to string variable SG 5010 response
Test for CLI ON or CLI OFF
Repeat as desired

8. Generating a Frequency Sweep

Purpose:

SG 5010 varies the output frequency incrementally from a start frequency to a stop frequency on its own (does not require controller I/O). The sweep may repeat automatically or run once when started by the controller.

Action:

Send to the SG 5010: **Mode Freq;NSteps** <num>,type;
STARTFreq <num>;**STOPFreq** <num>

Comments:

NSteps type may be either LIN or LOG.

Adding STEptime <num> causes wait (in seconds) between steps. A wait of 0.5 is usually adequate to allow for SG 5010 settling.

Adding SWeep ON starts a single sweep. (RUnn? can be used to determine if sweep has finished so it can be restarted.)

Adding SWeep Repeat causes sweep to repeat (use SWeep OFf to stop).

The above technique does not provide for synchronizing data acquistion on a point-by-point basis, which is accomplished by testing successive measurements for system settling before taking data and then incrementing the SG 5010 frequency.

9. Generating an Amplitude Sweep

Purpose:

SG 5010 varies the output amplitude incrementally from a start level to a stop level on its own (does not require controller I/O). The sweep may run once when started by the controller or repeat automatically.

Action:

Send to the SG 5010: **Mode Ampl;NSteps** <num>,type;
STARTVolts <num>;**STOPVolts** <num>

Comments:

See comments above under Generating a Frequency Sweep that relate to similar considerations when generating an amplitude sweep.

10. Generating an Interrupt at End of Sweep

Purpose:

Causes the SG 5010 to interrupt the controller when a sweep is finished.

Action:

Send to the SG 5010: **RQs ON;OPc ON**

Comments:

Interrupt control commands are switches—once set, RQS stays on and need not be set on as above unless previously turned off.

SG 5010 reports status 66 after generating SRQ.

11. Controlling Burst Signals

Purpose:

Triggering or gating the output can generate signal bursts separated by either no signal or a signal much smaller in amplitude. Software control of bursts is an alternative to automatic timing by the NBurst, ONCycles, and OFFCycles commands.

Action:

Send to SG 5010: **FUnction BUrst:**<num>;
OFFCycles <num>;**DT Gate**
Send <GET> interface message

or

Send to SG 5010: **FUnction BUrst:**<num>;
OFFCycles 99999;ONCycles <num>;**DT Trig**
Send GET interface message

Comments:

The difference in the two sequences given above under Action is:

1) DT Gate changes the state of the output—on or off.

2) DT Trig enables <GET> to trigger one burst of specified length.

The value of num in the FUnction BUrst command can be 0 or 10; it sets the output level during the "off" time as a percentage of output level during the burst.

The <GET> interface message is a software equivalent of the front-panel burst gate input. To allow control by <GET>, no signal should be applied to the front-panel input.

12. Disabling Interrupts

Purpose:

Prevent SG 5010 from asserting SRQ.

Action:

Send to SG 5010: **RQs OFf**

Comments:

RQS is like a master switch for interrupts; RQS OFF disables all interrupts except the one generated at power-on.

13. Operator (Front-Panel) Interrupt

Purpose:

Enable operator to generate an interrupt by pressing the INST ID button on SG 5010 front panel.

Action:

Send to SG 5010: **RQs ON;USerequest ON**

Comments:

USER OFF disables this interrupt.

SG 5010 reports status 67 after generating SRQ.

14. Interrogating Firmware Level

Purpose:

Check version number of firmware in SG 5010.

Action:

Dimension string variable (30 character min)
Send to SG 5010: **ID?**
Input SG 5010 response to string variable
Take string segment following "F"
(characters 22 through 24 of form "x.x")

Comments:

The ID? response also contains instrument model number and version of Tektronix Codes and Formats used in SG 5010 design. An example of the ID? response is: "ID TEK/SG5010,V81.1,F1.0;".

PROGRAMMING

INTRODUCTION

This manual section provides the information required for programming the SG 5010 Programmable Oscillator via the IEEE-488 bus. This information assumes that the reader is knowledgeable in IEEE-488 bus communication and has had some experience in programming the system that acts as the controller for the SG 5010. Communication via the IEEE-488 bus is specified and described in IEEE-Standard 488-1978, *Standard Digital Interface for Programmable Instrumentation.*[1] TM 5000 instruments are designed to communicate with any bus compatible controller that can send and receive ASCII messages (commands) over the IEEE-488 bus. These commands program the instruments or request information from the instruments.

Commands for TM 5000 programmable instruments are designed for compatibility between instrument types. The same commands are used in different instruments to control similar functions. In addition, commands are specified in mnemonics that are related to the functions implemented. For example, the INIT command initializes instrument settings to predefined default settings.

Commands are presented in this in three formats:

Command Functional Groups — A command list divided into functional groups with brief descriptions of commands.

Control/Command Descriptions — A front panel illustration showing command relationships to front panel operation and internal parameters.

Detailed Command Descriptions — An alphabetically arranged presentation of all commands with complete detailed descriptions.

[1]**Published by the Institute of Electrical and Electronics Engineers, Inc., 345 East 47th Street, New York, N.Y., 10017.**

TM 5000 programmable instruments connect to the IEEE-488 bus through a TM 5000 power module. Refer to the Operating Instructions section of this manual for information on installing the SG 5010 in the power module. Also, it is helpful to review that section to become familiar with front panel functions. The IEEE-488 bus primary address for the SG 5010 is factory set to decimal 25. Its message terminator is factory set to EOI ONLY. Both the primary address and message terminator can be changed using front panel controls. Refer to GPIB Address and Terminator Setting. (The use of message terminators is described in this section, in the portion entitled Messages and Communication Protocol.)

GPIB Address and Terminator Setting

The SG 5010 primary GPIB address is stored and maintained in memory at power-down by a backup battery. The SG 5010 responds to one of two possible message terminators (LF and EOI, or EOI ONLY) that various controllers may send on the bus. Pressing the INST ID button causes the SG 5010 to display its selected IEEE-488 bus primary address and firmware version number. The right-hand decimal point illuminates if the selected message terminator is LF/EOI. Both the message terminator and primary address are set using the front panel controls and the following sequence:

Press RECALL

Press INST ID

Press the numeric buttons to display the desired primary address, most significant digit first. To select the LF/EOI terminator, press the decimal point. EOI ONLY is assumed if the decimal point is not pressed.

Press ENTER

The primary address can be set to any number in the series 0 through 31. Address 31 effectively removes the SG 5010 from the bus. The SG 5010 is shipped with the GPIB address set to 25 and message terminator set to EOI ONLY.

The address and message terminator may be changed at any time except when the instrument is in the Local Lockout state. If the RAM checksum (part of the power-up self-test sequence) detects a memory failure, the instrument removes itself from the bus and displays a three-digit error code (340). In this event, the user should reprogram the address into memory after the cause of the failure has been resolved. Refer error code conditions to qualified service personnel. Table 3-1 lists all SG 5010 error codes and their definitions. Note that only the Internal Error codes (300-series) indicate an SG 5010 hardware malfunction.

COMMANDS

The SG 5010 is controlled either by front panel controls or through commands received from the controller. These commands are of three types:

Setting—control instrument settings.
Query/Output—request data.
Operational—cause a particular action.

When the instrument is in the remote state, it provides a response or executes all commands as appropriate. In the local state, only query/output commands are executed; setting and operational commands generate error responses, since instrument functions are under front panel control.

Command Functional Groups

The following list of commands is arranged by functional group; the instrument commands group is, in turn, divided into sub-groups.

NOTE

Brackets [ ] indicate the enclosed item is optional, and carets < > indicate a defined element. Capitalized letters are the required characters; the lower case letters may also be used.

INSTRUMENT COMMANDS

Function Commands

[FUnction] SIne – Selects the sine wave for output.

[FUnction] SQuare – Selects the square wave for output.

[FUnction] SMpte [:<ratio>] – Selects SMPTE signal for output and specifies amplitude ratio between low and high frequency tones. Valid ratios are 1:1 or 4:1 (low): (high); 4:1 is the default ratio.

[FUnction] CCif – Selects CCIF signal for output.

[FUnction] BUrst [:<percent>] – Selects sine wave burst signal for output and specifies amplitude of the *off* cycles (as a percent of the *on* cycles amplitude). Valid percent is 0 or 10; default percent is 0.

[FUnction] EXternal – Selects signal at EXT INPUT connector as the output.

FUnction? – Returns enabled function (and number indicating SMPTE ratio or burst percent, if applicable).

Amplitude Commands

AMplitude <num>[:<units>] – Sets amplitude and units of selected output signal. Valid units are VPP, VRMS, DBM, or DBU; default units are the previously specified units.

AMplitude? – Returns amplitude and units.

DBm <num> – Sets amplitude to specified dBm value.

DBm? – Returns amplitude in dBm.

DBU <num> – Sets amplitude to the equivalent Vrms value of the argument (in DBU).

DBU? – Returns amplitude in dBu.

VPp <num> – Sets amplitude to the equivalent Vrms value of the argument (Vp-p).

VPp? – Returns amplitude in V p-p units.

Vrms <num> – Sets amplitude to specified Vrms value.

Vrms? – Returns amplitude in Vrms.

Frequency Commands

FRequency <num> – Sets frequency (main frequency) for all functions except EXT.

FRequency? – Returns frequency setting (main frequency).

IMfreq <num> – Sets IM frequency for SMPTE/DIN and CCIF functions. Valid frequencies are 40, 50, 60, 80, 100, 125, 250, and 500 Hz.

IMf? – Returns IM frequency setting.

Burst Control Commands

NBurst <num> – Specifies number of *on* cycles for burst; sets number of *off* cycles to infinity (99999) for single burst mode. Valid range is 1 to 65535.

ONCycles <num> – Specifies number of *on* cycles for burst. Valid range is 1 to 65535.

ONCycles? – Returns number of *on* cycles.

OFFCycles <num> – Specifies number of *off* cycles for burst (0 for gated burst; 1 to 65535 for repetitive burst; 99999 for single burst).

OFFCycles? – Returns enabled number of *off* cycles for burst.

Sweep Control Commands

STARTFreq <num> – Sets the start frequency for sweep operation.

STARTFreq? – Returns start frequency.

STOPFreq <num> – Sets stop frequency for sweep operation.

STOPFreq? – Returns stop frequency.

STARTVolts <num> – Sets start amplitude for sweep operation in Vrms.

STARTVolts? – Returns start amplitude in Vrms.

STOPVolts <num> – Sets stop amplitude for sweep operation in Vrms.

STOPVolts? – Returns stop amplitude in Vrms.

NSteps <num>[,<type>] – Sets number of sweep steps. Valid range is 1 to 99. Type specifies linear (LIN) or logarithmic (LOG) sweep; default type is the previously specified type.

NSteps? – Returns number of sweep steps and type.

STEptime <num>[,<mode>] – Sets time per sweep step and sweep mode. Valid range for time is .1 to 25.0 seconds with .1 sec. resolution. Sweep mode is either FREQUENCY or AMPLITUDE; default mode is the previously specified mode.

STEptime? – Returns selected time per sweep step and sweep mode.

TYpe LIn – Sets sweep type to linear sweep.

TYpe LOg – Sets sweep type to logarithmic sweep.

TYpe? – Returns selected sweep type.

Mode Ampl – Sets sweep to amplitude mode.

Mode Freq – Sets sweep to frequency mode.

Mode? – Returns selected sweep mode (amplitude or frequency).

SWeep ON or **SWeep Single** – Starts a single sweep sequence.

SWeep Repeat – Starts a repetitive sweep sequence.

SWeep OFf – Stops the sweep.

RUnn? – Returns 0 (sweep not running) or 1 (sweep running).

Stored Setting Commands

STORe <num>[,<num>...] – Stores the current settings (except CLI, DT, OVER, OPC, PLI, RQS, USEREQ) in specified storage location (0 through 9).

STORe <num>:<binblk> – Stores <binblk> data in specified storage location (0 through 9).

STORe? <num>[,<num>...] – Outputs settings stored in specified location(s) 0 through 9 using the format STORE <num>:<binblk>;.

REcall <num> – Sets instrument to the settings recalled from specified storage location.

LLset <binblk> – Sets instrument to settings stored in <binblk> (except DT, CLI, OVER, OPC, PLI, RQS, USEREQ).

LLset? – Returns instrument settings in binary format.

Display Control Commands

Display Vrms – Displays amplitude setting in Vrms.

Display Dbm – Displays amplitude setting in dBm.

Display Freq – Displays frequency setting.

Display Imfreq – Displays IM frequency setting.

Display Nsteps – Displays number of steps set for sweep.

Display OFfcycles – Displays number of *off* cycles for burst.

Display ONcycles – Displays number of *on* cycles for burst.

Display RSource or **Display RSrc** – Displays source impedance setting.

Display STARTFreq – Displays sweep mode setting for start frequency.

Display STARTVolts – Displays starting sweep setting in Vrms.

Display STEptime – Displays time per sweep step.

Display STOPFreq – Displays sweep mode setting for stop frequency.

Display STOPVolts – Displays stopping sweep setting in Vrms.

OUTPUT COMMANDS

BAlance [ON] – Sets instrument to balanced output.

BAlance OFf – Sets instrument to unbalanced output.

BAl? – Response indicates the signal output is balanced or unbalanced.

UNbalance – Sets instrument to unbalanced signal output.

GRound [ON] or **GNd [ON]** – Sets instrument to grounded signal output.

GRound OFf or **GNd OFf** – Sets instrument to floating signal output.

GRound? or **GNd?** – Response indicates signal output is grounded or floating.

FLoat or **FLt** – Sets instrument to floating signal output.

RSource <num> or **RSrc <num>** – Sets source impedance. Valid impedances are 50, 150, and 600 Ω.

RSource? or **RSrc?** – Returns source impedance setting.

OUtput ON – Turns on signal output.

OUtput OFf – Turns off signal output.

OUt? – Response indicates signal output condition (on or off).

SYSTEM COMMANDS

DT Gate – A <GET> interface message toggles the burst gate, if the instrument is set to FUNC BURST, OFFCYC 0, and no external signal is connected to the BURST GATE input.

DT Set – Causes instrument to wait for <GET> interface message before updating instrument settings, except

for the SWEEP ON, SWEEP SINGLE, and SWEEP REPEAT commands which are executed when received.

DT Trig – A <GET> interface message initiates a single sweep burst, if instrument is set to FUNC BURST, OFFCYC 99999, and no external signal is connected to the BURST GATE input.

DT SWeep – A <GET> interface message initiates a single sweep sequence.

DT Off – Disables all DT (Device Trigger) functions.

DT? – Response indicates which DT function is enabled.

ERRMsg? – Returns an event code and a brief description of the event. If RQS is ON, the code indicates the most recent event. If RQS is OFF, the code indicates the highest priority event that has occurred.

ERRor? or **EVent?** – Same as ERRMSG except that the event description is eliminated.

HElp? – Returns a string list of all SG 5010 command headers.

IDentify? – Returns the instrument type, Tektronix Codes and Formats version, and the instrument firmware version.

INit – Initializes instrument to predefined (INIT command) settings.

SETtings? – Returns a string list of current instrument settings.

TEst? – Initiates instrument self test and returns 0 (no errors), or event codes of detected failures.

STATUS COMMANDS

CLi ON – Enables assertion of SRQ when instrument goes into or out of current limit.

CLi OFf – Disables assertion of SRQ when instrument goes into or out of current limit.

CLi? – Response indicates the current limit interrupt state (on or off).

CUrrent? – Returns "CURR <num>;", where <num> is 0 if instrument is not current limited; <num> is 1 if instrument is current limited.

GAte? – Returns "GATE <num>;" where <num> is 0 if BURST GATE signal is unasserted (high); <num> is 1 if BURST GATE signal is asserted (low).

LOck? – Returns "LOCK <num>;" where <num> is 1 if instrument has not been in phase lock for more than 1 ms; <num> is 0 if instrument is in phase lock.

OPc ON – Enables operation complete interrupt; instrument asserts SRQ when it completes one sweep.

OPc OFf – Disables operation complete interrupt; instrument does not assert SRQ when it completes one sweep.

OPc? – Returns "OPC ON;" or "OPC OFF;".

OVerrange ON – Enables sweep overrange interrupt; instrument asserts SRQ when the sweep exceeds a limit of the parameter being swept.

OVerrange OFf – Disables sweep overrange interrupt; instrument does not assert SRQ when the sweep exceeds a limit of the parameter being swept.

OVerrange? – Returns "OVER ON;" or "OVER OFF;".

PLi ON – Enables assertion of SRQ when instrument goes out of phase lock for more than 1 ms, or into phase lock from a reportable out-of-phase lock condition.

PLi OFf – Disables assertion of SRQ when instrument goes into of out of phase lock.

PLi? – Response indicates the phase lock interrupt state (on or off).

RQs ON – Enables service request (SRQ) interrupt.

RQs OFf – Disables service request interrupt.

RQs? – Response indicates the service request interrupt state (on or off).

USereq ON – Enables assertion of SRQ when front panel INST ID button is pressed.

USereq OFf – Disables assertion of SRQ when front panel INST ID button is pressed.

USereq? – Response indicates the user request interrupt state (on or off).

Control/Command Descriptions

Each SG 5010 command, like those in all TM 5000 instruments, begins with a header, which is a word or acronym that describes the function implemented. Following the header, many commands require an argument, which is a word or number that specifies the desired state for the function. The commands are presented alphabetically on the following pages. In this presentation, the following notations are used to represent elements of the IEEE-488 bus communications between the SG 5010 and the controller.

<GET> - The Group Execute Trigger interface message (decimal code 8, transmitted with attention asserted). Only addressed listeners respond to <GET>.

<num> - A number that can be transmitted or accepted by the SG 5010. Numbers are accepted in NR1 (integer), NR2 (decimal), and NR3 (with exponent) formats. (See ANSI Standard X3.42.)

<binblk> - A binary block of data in the format specified in Tektronix Codes and Formats (V81.1). The binary block consists of the percent sign (%, decimal 37) followed by a two-byte binary count and the data bytes, and ends with a checksum. The two-byte binary count (integer, most significant byte first) specifies the number of data bytes plus the checksum byte. The checksum is the two's complement of the modulo-256 sum of the preceding binary data bytes and the binary count bytes, but does not include the percent sign.

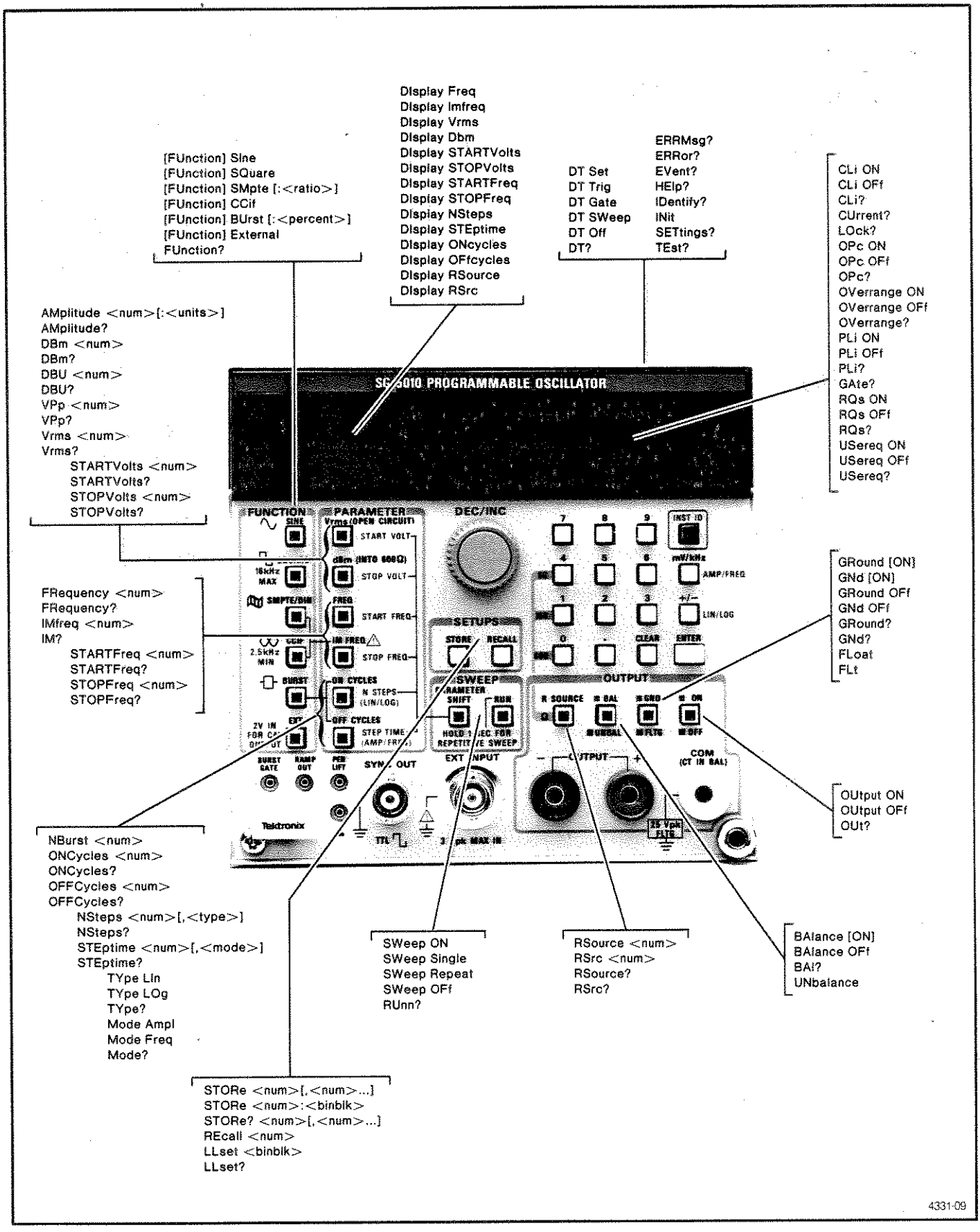


Fig. 3-1. Instrument commands and relationship to front panel controls.

DETAILED COMMAND LIST

NOTE

Brackets [ ] indicate the enclosed item is optional, and carets < > indicate a defined element. Capitalized letters are the required characters; the lower case letters may also be used.

AMPLITUDE

Type:

Setting or query

Setting syntax:

AMplitude <num>[:<units>]

where units are:

VPp - for volts peak-to-peak
Vrms - for volts rms
DBm - for dBm
DBU - for dBu

Examples:	**Amplitude selected:**
AMPLITUDE 25:VP	25 V p-p
AMPL 8.5:V	8.5 Vrms
AM 18.5:DB	18.5 dBm
AM 5:DBU	5 dBu
AMPLIT 25E-2:V	250 mV rms
AMPL 0.5	0.5 (previous units)

Query syntax:

AMplitude?

Query response syntax: (one of the following)

AMPL <num>:DBM;
AMPL <num>:VRMS;

Query response examples:

AMPL 15:DBM;
AMPL 5.5:VRMS;

Discussion:

This command sets the amplitude for the enabled function to the value specified in the numeric argument. The units portion of the argument is optional; if undefined, the units are Vrms if previously programmed in Vp-p or DBU; otherwise the units are dBm.

If VPP units are specified, the value of <num> is converted to the sine wave peak equivalent Vrms value.

The amplitude can also be set using the DBM, DBU, VPP, and VRMS commands.

Vpp and dBu units are available only under remote programming control and can not be entered from the front panel.

All parameter units except dBm define the open circuit, unloaded, output amplitude calibrated for sinewaves. The non-sinewave functions are calibrated for the same peak-to-peak output as sinewaves. The dBm unit assumes an additional 600 Ω load resistance and acknowledges SG 5010 source resistance selection.

The internal amplitude control related hardware is calibrated in Vrms. Other units are first converted into equivalent Vrms (refer to the Conversion Table) and rounded off to the closest setting (that the hardware accepts). There is little or no additional accuracy loss when using one of the alternate units, because of a closer 0.2% Vrms setting resolution (refer to the Specifications section of this manual).

CONVERSION TABLE

	Vpp	dBu	dBm
to Vrms	$\frac{Vpp}{2.8284}$	$(0.7746)10^{\left(\frac{dBu}{20}\right)}$	$(0.7746)\left(1+\frac{RS}{600}\right)10^{\left(\frac{dbm}{20}\right)}$
from Vrms	(2.8284) Vrms	$20\log_{10}\left[\frac{Vrms}{0.7746}\right]$	$20\log_{10}\left[\frac{Vrms}{0.7746}\left(\frac{600}{Rs+600}\right)\right]$

Rs = Selected source resistance

BALANCE

Type:

Setting or query

Setting syntax:

BAlance [ON]
BAlance OFf

Examples:

BALANCE ON
BALAN OF
BA OF
BA

Query syntax:

BAl?

Query response: (one of the following)

BAL ON;
BAL OFF;

Discussion:

This command sets the output to the balanced of unbalanced state, depending on the command argument.

CLI (Current Limit Interrupt)

Type:

Setting or query

Setting syntax:

CLi ON
CLi OFf

Examples:

CLI OF
CL ON
CL OFF
CL OF

Query syntax:

CLi?

Query response: (one of the following)

CLI ON;
CLI OFF;

Discussion:

This command controls the current limit interrupt. The ON argument enables the interrupt; the instrument asserts SRQ when it goes into or out of current limit. The OFF argument disables the interrupt; the instrument does not assert SRQ when a change in current limit status occurs.

Other status interrupt commands are: OPC, OVERRANGE, PLI, RQS, and USEREQ.

CURRENT?

Type:

Query

Query syntax:

CUrrent?

Query response syntax:

CURR <num>;

Discussion:

This command returns a number whose value indicates the current limit status of the instrument, as follows:

<num> = 0, if the instrument is not in current limit.

<num> = 1, if the instrument is in current limit.

The CLI command also is used to indicate current limit status.

DBM

Type:

Setting or query

Setting syntax:

DBm <num>

Examples:

DBM 3
DB 55E-2

Query syntax:

DBm?

Query response syntax:

DBM <num>;

Query response example:

DBM 3.00;

Discussion:

This command sets the amplitude to the specified dBm value. The value is rounded to the closest 0.05 dBm. It also changes the units for the AMPLITUDE command to dBm.

The following commands also set the amplitude:

AMPLITUDE
DBU
VPP
VRMS

DBU

Type:

Setting or query

Setting syntax:

DBU <num>

Examples:

DBU 2
DBU 55E-2

Query syntax:

DBU?

Query response syntax:

DBU <num>;

Discussion:

This command sets the amplitude specified in the command argument to the equivalent rms value.

The following commands also set the amplitude:

AMPLITUDE
DBM
VPP
VRMS

DISPLAY

Type:

Operational

Operational syntax:

DIsplay Freq
DIsplay Imfreq
DIsplay Vrms
DIsplay Dbm
DIsplay STARTVolts
DIsplay STOPVolts
DIsplay STARTFreq
DIsplay STOPFreq
DIsplay Nsteps
DIsplay STEptime
DIsplay ONcycles
DIsplay OFfcycles
DIsplay RSource or DIsplay RSrc

Examples:

DISPLAY FREQ
DISPL IMF
DIS STOPV
DI ONC

Discussion:

This command causes the instrument to display the current value of the specified argument. For example, DISPLAY FREQ causes the display to show the current value of the FREQ parameter; for DISPLAY VRMS, the display shows the amplitude setting in Vrms.

DT (Device Trigger)

Type:

Setting or query

Setting syntax:

DT Set
DT Trig
DT Gate
DT SWeep
DT Off

Examples:

DT SET
DT S
DT TRIG
DT T
DT GATE
DT OF
DT SW

Query syntax:

DT?

Query response: (one of the following)

DT SET;
DT TRIG;
DT GATE;
DT SWEEP;
DT OFF;

Discussion:

Each argument of the DT command enables one state of the device trigger function, as described below. The device trigger states are mutually exclusive.

DT SET – Causes the instrument to wait for the <GET> interface message before updating the instrument hardware to new settings the instrument has received, with the following exceptions: SWEEP ON, SWEEP SINGLE, and SWEEP REPEAT commands are executed when received (<GET> not required).

DT TRIG – Causes the instrument to output a single burst when it receives the <GET> interface message, if the instrument is set to FUNCTION BURST and OFFCYCLES 99999, and no external signal is applied to the BURST GATE input connector.

DT GATE – Toggles the burst gate when a <GET> interface message is received, if the instrument is set to FUNCTION BURST and OFFCYCLES 0, and no external signal is applied to the BURST GATE input connector. While burst gate is unasserted (floating high), the instrument outputs a sine wave.

DT SWEEP – Starts a single sweep sequence when a <GET> interface message is received.

DT OFF – Disables the device trigger function; the <GET> interface message is ignored.

ERRMSG?

Type:

Query

Query syntax:

ERRMsg?

Query response syntax:

ERRMSG <num>,<msg string>;

Discussion:

The ERRMSG query returns data about instrument events. If RQS is on, <num> is the event code for the last reported status byte. If RQS is off, <num> is the event code for the highest priority event that has occurred. In either case, <msg string> is a brief description of the enumerated event.

Refer to Table 3-1 for a list of event codes and status bytes.

The ERROR? and EVENT? commands and the serial poll by the controller also return instrument event information.

ERROR?
EVENT?

Type

Query

Query syntax:

ERRor?
EVent?

Query response syntax:

ERR <num>;
EVENT <num>;

Discussion:

This command returns information about instrument events. If RQS is on, <num> for both commands is the event code for the last reported status byte. If RQS is off, <num> is the event code for the highest priority event that has occurred. Refer to Status and Error Reporting for a discussion of event codes and status bytes. Table 3-1 lists all SG 5010 event codes.

The ERRMSG command also reports instrument event information.

FLOAT

Type:

Setting

Setting syntax:

FLoat or FLt

Examples:

FLOAT
FL
FLT

Discussion:

The command selects floating output.

The GROUND OFF command also selects floating output.

FREQUENCY

Type:

Setting or query

Setting syntax:

FRequency <num>

Examples:

FREQUENCY 120E3
FREQ 1.5E4
FR 5E+4

Query syntax:

FRequency?

Query response syntax:

FREQ <num>;

Query response examples:

FREQ 125E+3;
FREQ 10E+2;

Discussion:

This command sets the main frequency for the enabled function except EXT. Refer to the Specifications section for the frequency range for each function.

The command IMFREQ sets the secondary frequency for the SMPTE/DIN and CCIF functions.

FUNCTION

Type:

Setting or query

Setting syntax:

[FUnction] SIne
[FUnction] SQuare
[FUnction] SMpte[:<ratio>]
[FUnction] CCif
[FUnction] BUrst[:<percent>]
[FUnction] EXternal

Examples:

FUNCTION SINE
FUNC SIN
SI
SINE
FU SQU
FUNC SMP:1
FUNC CCIF
FUNC BUR:0
BU
EXT

Query syntax:

FUnction?

Query response: (one of the following)

FUNC SINE;
FUNC SQUARE;
FUNC SMPTE:1; or FUNC SMPTE:4;
FUNC CCIF;
FUNC BURST:0; or FUNC BURST:10;
FUNC EXTERNAL;

Discussion:

Each command enables the instrument function specified in the argument to produce a sine wave signal, square wave signal, SMPTE intermodulation test signal, CCIF intermodulation test signal, or burst signal. The command header (FUNCTION) is optional, as are the numeric arguments for the SMPTE signal ratio, and the BURST signal percent. If undefined, these numeric arguments assume the default values given below. The AMPLITUDE, DBM, DBU, VPP, or VRMS command sets the amplitude for the signal; the FREQUENCY or IMFREQ command sets the frequency. In addition, the frequency or amplitude of each function can be swept in a linear or logarithmic sweep, by using the SWEEP command.

- FUNCTION SINE enables the sine wave function for output.

- FUNCTION SQUARE enables the square wave function for output.

- FUNCTION SMPTE enables the SMPTE intermodulation test signal for output. The numeric argument sets the ratio of the low frequency tone amplitude to the high frequency tone amplitude. Valid values for <ratio> are 1 or 4. If undefined, the argument default value is 4.

- FUNCTION CCIF enables the CCIF intermodulation test signal for output.

- FUNCTION BURST enables the burst signal for output. The numeric argument specifies the amplitude of the *off* cycles as a percentage of the *on* cycles amplitude. Valid values for the argument are 0 or 10. If undefined, the argument default value is 0. Also see NBURST, ONCYCLES, and OFFCYCLES.

- FUNCTION EXTERNAL selects the signal input to the EXT INPUT connector as the output.

GATE?

Type:

Query

Query syntax:

GAte?

Query response syntax:

GATE <num>;

Discussion:

The response generated by this command indicates the status of the input signal at the BURST GATE input connector, as follows:

<num> = 0, if the BURST GATE input signal is unasserted (floating high).

<num> = 1, if the BURST GATE input signal is asserted (pulled low and then released; trigger occurs on rising edge).

GROUND

Type:

Setting or query

Setting syntax:

GRound [ON] or GNd [ON]
GRound OFf or GNd OFf

Examples:

GROUND ON
GR
GND ON
GN
GROUND OFF
GR OF
GND OFF
GN OF

Query syntax:

GRound? or GNd?

Query response: (one of the following)

GND ON;
GND OFF;

Discussion:

GROUND ON selects grounded output. GROUND OFF selects floating output. The query response indicates the state of the output: grounded or floating.

The FLOAT command also selects floating output.

WARNING

THE FOLLOWING SERVICING INSTRUCTIONS ARE FOR USE BY QUALIFIED PERSONNEL ONLY. TO AVOID PERSONAL INJURY, DO NOT PERFORM ANY SERVICING OTHER THAN THAT CONTAINED IN OPERATING INSTRUCTIONS UNLESS YOU ARE QUALIFIED TO DO SO. REFER TO OPERATORS SAFETY SUMMARY AND SERVICE SAFETY SUMMARY PRIOR TO PERFORMING ANY SERVICE.

HELP?

Type:

Query

Query syntax:

HElp?

Query response syntax:

HELP <command string>;

Query response example:

HELP AMPL, BAL, BURS, CCIF, CLI, CURR, DBU, DBM, DISP, DT, ERRMSG, ERR, EVENT, EXTE, FLOA, FLT, FREQ, FUNC, GATE, GND, GROU, HELP, ID, IMF, INIT, LLS, LOCK, MODE, NBUR, NSTEP, OFFCYC, ONCYC, OPC, OUT, OVER, PLI, RANGE, RECA, RQS, RSOU, RSRC, RUNN, SET, SINE, SMPT, SQUA, STARTF, STARTV, STEPT, STOPF, STOPV, STOR, SWEE, TEST, TYPE, UNBAL, USER, VPP, VRMS:

Discussion:

This command returns a list of all command headers available for programming the SG 5010.

IDENTIFY

Type:

Query

Query syntax:

IDentify?

Query response:

ID TEK/SG5010,V81.1,Fx.x;

Discussion:

This command returns identification information about the SG 5010, as follows:

TEK/SG5010 — identifies the instrument type.

V81.1 - identifies the version of Tektronix Codes and Formats used in the SG 5010 firmware design.

Fx.x - identifies the instruments firmware version. For example, F1.0 indicates the firmware version is 1.0.

IMFREQ (Intermodulation Frequency)

Type:

Setting or query

Setting syntax:

IMfreq <num>

Examples:

IMFREQ 40
IMF 125
IM 500

Query syntax:

IMf?

Query response syntax:

IMF <num>;

Discussion:

This command sets the secondary frequency used for the SMPTE/DIN and CCIF functions, when they are enabled. Valid secondary frequencies for both functions are:

40
50
60
80
100
125
250
500

The instrument rounds the argument to the closest valid frequency.

INIT

Type:

Operational

Syntax:

INit

Setting syntax:

INIT
IN

Discussion:

This command configures the SG 5010 settings to the predefined settings listed below:

AMPL 1:VRMS;
BAL ON;
CLI OFF;
DISP VRMS;
DT OFF;
FREQ 10000;
FUNC SINE;
GND OFF;
IMF 60;
NSTEP 30,LOG;
OFFCYC 90;
OPC OFF;
ONCYC 10;
OUT OFF;
OVER OFF;
PLI OFF;
RQS ON;
RSRC 600;
STARTF 20;
STOPF 20000;
STARTV 0.1;
STOPV 10.0;
STEPT 0.1,FREQ;
SWEEP OFF;
USER OFF;

LLSET (Low Level Settings)

Type:

Setting or query

Setting syntax:

LLset <binblk>

Examples:

LLSET <binblk>
LLS <binblk>
LL <binblk>

Query syntax:

LLset?

Query response syntax:

LLS <binblk>;

Discussion:

The setting command sets the instrument to the settings represented by the binary block data in the argument. All settings are affected except the following, since they are not stored:

CLI
DT
OVER
OPC
PLI
RQS
USEREQ

The binary block data for the current instrument settings is sent to the controller in response to the query command. The format of the binary block data is defined under the heading Control/Command Descriptions.

The STORE? command also outputs binary block settings data.

LOCK?

Type:

Query

Query syntax:

LOck?

Query response syntax:

LOCK <num>;

Discussion:

This command generates a response indicating the phase lock status, as follows:

<num> = 1, if the instrument has not been in phase lock for more than 1 ms when the query is received.

<num> = 0, if the instrument is in phase lock when queried.

The PLI command also controls phase lock status information.

MODE

Type:

Setting or query

Setting syntax:

Mode Ampl
Mode Freq

Examples:

MODE AMPL
MODE FREQ
M A
M F

Query syntax:

Mode?

Query response: (one of the following)

MODE AMPL;
MODE FREQ;

Discussion:

This command selects a frequency or amplitude sweep of the output signal. The optional argument of the STEPTIME command also selects the sweep mode.

Other sweep control commands are STARTFREQ, STOPFREQ, STARTVOLTS, STOPVOLTS, NSTEPS, TYPE, and SWEEP.

NBURST (Number of Burst)

Type:

Setting

Setting syntax:

NBurst <num>

Examples:

NBURST 10
NBUR 50E3
NB 1

Discussion:

This command sets the number of *on* cycles for the BURST function to the value specified in the argument. It also automatically sets the number of *off* cycles to infinity. The valid range for the argument is 1 to 65535. A single burst is triggered by assertion of the signal on the BURST GATE input. This input floats at a high level. To assert the signal, the high input must be pulled low and then released; triggering occurs on the rising edge.

The commands ONCYCLES and OFFCYCLES also set the number of *on* and *off* cycles for the BURST function.

NSTEPS (Number of Steps)

Type:

Setting or query

Setting syntax:

NSteps <num>[,<type>]

where <type> is one of the following:

LIn	for linear sweep
LOg	for logarithmic sweep

Examples:

NSTEPS 25,LIN
NS 75,LO
NS 10

Query syntax:

NSteps?

Query response syntax: (one of the following)

NSTEP <num>,LIN;
NSTEP <num>,LOG;

Discussion:

This command sets the number of steps from the beginning to end of a frequency or amplitude sweep. The valid range for the numeric argument is 1 to 99. The optional argument <type> selects either a linear or logarithmic type of sweep. If <type> is unspecified, the previous sweep type is assumed. The TYPE command also selects the sweep type.

Other sweep control commands are STARTFREQ, STOPFREQ, STARTVOLTS, STOPVOLTS, STEPTIME, TYPE, MODE, and SWEEP.

OFFCYCLES

Type:

Setting or query

Setting syntax:

OFFCycles <num>

Examples:

OFFCYCLES 60
OFFCYC 1E3
OFFC 99999

Query syntax:

OFFCycles?

Query response syntax:

OFFCYC <num>;

Discussion:

The argument for this command sets the number of *off* cycles for the BURST function, and enables gated, repetitive, or single burst operation. Valid arguments are:

0 - Sets the gated burst mode to output a continuous sine wave signal while the external BURST GATE signal is asserted (pulled low and then released).

1 to 65535 - Sets the number of *off* cycles for a repetitive burst output. The number of *on* cycles is set by the ONCYCLES command.

99999 - Sets the number of *off* cycles to infinity. With this argument, the instrument outputs a single burst when the BURST GATE input signal is asserted (pulled low and then released).

ONCYCLES

Type:

Setting or query

Setting syntax:

ONCycles <num>

Examples:

ONCYCLES 25
ONCYC 10
ONC 500

Query syntax:

ONCycles?

Query response syntax:

ONCYC <num>;

Discussion:

This command sets the number on *on* cycles for the BURST function. Valid range for the argument is 1 to 65535.

The commands NBURST and OFFCYCLES also set the number of burst cycles.

OPC (Operation Complete Interrupt)

Type:

Setting or query

Setting syntax:

OPc ON
OPc OFf

Examples:

OPC ON
OP ON
OPC OFF
OP OF

Query syntax:

OPc?

Query response: (one of the following)

OPC ON;
OPC OFF;

Discussion:

This command controls the operation complete interrupt. If the specified argument is ON, the interrupt is enabled; the instrument asserts SRQ when it completes one sweep. If the argument is OFF, the interrupt is disabled; no SRQ is generated for completion of one sweep.

Other status interrupt commands are CLI, OVERRANGE, PLI, RQS, and USEREQ.

OUTPUT

Type:

Setting or query

Setting syntax:

OUtput ON
OUtput OFf

Examples:

OUTPUT ON
OUT OFF
OU OF

Query syntax:

OUt?

Query response: (one of the following)

OUT ON;
OUT OFF;

Discussion:

This command turns the output on or off at the output connectors, depending on the argument specified. The source impedance is maintained when the output is off. At power-up, the output is set to the *off* state.

OVERRANGE (Sweep Overrange Interrupt)

Type:

Setting or query

Setting syntax:

OVerrange ON
OVerrange OFf

Examples:

OVERRANGE ON
OVER OFF
OV OF

Query syntax:

OVerrange?

Query response:

OVER ON;
OVER OFF;

Discussion:

This command controls the overrange interrupt. The argument ON enables the interrupt; the instrument asserts SRQ when the sweep exceeds any limit of the parameter being swept. The OFF argument disables the interrupt; an overrange does not cause SRQ to be asserted.

Other status interrupt commands are: CLI, OPC, PLI, RQS, and USEREQ.

PLI (Phase Lock Interrupt)

Type:

Setting or query

Setting syntax:

PLi ON
PLi OFf

Examples:

PLI ON
PL OF

Query syntax:

PLi?

Query response: (one of the following)

PLI ON;
PLI OFF;

Discussion:

This command controls the phase lock interrupt. The ON argument enables the interrupt; the instrument asserts SRQ when it goes out of phase lock for more than 1 ms or into phase lock after being out for more than 1 ms. The OFF argument disables the interrupt; no SRQ is asserted when the phase lock status changes.

The LOCK? command also generates phase lock status information.

Other status interrupt commands are: CLI, OPC, OVERRANGE, RQS, and USEREQ.

RECALL

Type:

Operational

Syntax:

REcall <num>

Examples:

RECALL 3
REC 2
RE 9

Discussion:

This command recalls the group of instrument settings from the location specified in the argument, and configures the instrument to the recalled settings. If no settings are stored in the specified location, the instrument assumes the INIT command settings.

RQS (Request for Service)

Type:

Setting or query

Setting syntax:

RQs ON
RQs OFf

Query syntax:

RQs?

Query response: (one of the following)

RQS ON;
RQS OFF;

Discussion:

This command provides master control over the SRQ function. If RQS is ON, the instrument asserts SRQ when an event occurs which normally initiates such action. Events that normally cause SRQ to be asserted include the power-up sequence, self-test errors, front panel operation errors, and programming errors. Other events that may cause SRQ to be asserted are the status interrupts, such as OVERRANGE, or PLI. If enabled and RQS is ON, the interrupts assert SRQ, when their specific interrupt conditions occur. However, when RQS is OFF, SRQ will be asserted only when the instrument completes the power-up sequence.

The commands that control status interrupts are the following:

CLI
OPC
OVERRANGE
PLI
USEREQ

RSOURCE

Type:

Setting or query

Setting syntax:

RSource <num> or RSrc <num>

Examples:

RSOURCE 150
RSOU 50
RS 600
RSRC 150

Query syntax:

RSource? or RSrc?

Query response syntax:

RSRC <num>;

Discussion:

This command selects the output source impedance. Valid values for <num> are 50, 150, and 600. If the instrument receives a value for <num> that is above 50 and below 600, it will round it to the nearest valid value.

RUNN?

Type:

Query

Query syntax:

RUnn?

Query response syntax:

RUNN <num>;

Discussion:

Returns RUNN <num>; where <num> is a 0 or 1 indicating the following status of the sweep:

0 - Indicates the sweep is not running.

1 - Indicates the sweep is running.

SETTINGS?

Type:

Query

Query syntax:

SETtings?

Query response example:

FUNC SINE;AMPL 1.000;VRMS;FREQ 10.000E+3;IMF 60;OFFCYC 90;ONCYC 10;
STARTV 0.100;STOPV 10.00;STARTF 20.00E+0;STOPF 20.00E+3;NSTEP 30,LOG;
STEPT 0.1,FREQ;RSRC 600;BAL ON;GND OFF;OUT OFF;CLI OFF;DT OFF;OPC OFF;OVER OFF;PLI OFF;RQS ON;USER OFF;

Discussion:

NOTE

The arguments listed in the query response example are the arguments returned when the instrument is configured to the INIT command settings.

The SETTINGS? command returns the command string in the sequence shown in the example. The arguments that are returned reflect the settings enabled at the time the instrument receives the SETTINGS? command.

STARTFREQ

Type:

Setting or query

Setting syntax:

STARTFreq <num>

Examples:

STARTFREQ 125E3
STARTF 50

Query syntax:

STARTFreq?

Query response syntax:

STARTF <num>;

Discussion:

This command sets the frequency at which a sweep of the output signal frequency begins. The frequency for the end of the frequency sweep is set using the STOPFREQ command.

The instrument does not check that the value of the argument is valid for the enabled function. While a sweep is in progress, a sweep overrange condition occurs if a sweep parameter exceeds the valid range for the selected function. If a sweep overrange condition occurs, the parameter, voltage, or frequency that is exceeded will remain at the maximum valid value for the enabled function.

Other sweep control commands are STARTVOLTS, STOPVOLTS, NSTEPS, STEPTIME, TYPE, MODE, and SWEEP.

STARTVOLTS

Type:

Setting or query

Setting syntax:

STARTVolts <num>

Examples:

STARTVOLTS 10
STARTV 5

Query syntax:

STARTVolts?

Query response syntax:

STARTV <num>;

Discussion:

This command sets the amplitude (in Vrms) at which an amplitude sweep of the output signal begins. The STOPVOLTS command sets the ending amplitude.

The instrument does not check that the value of the argument is valid for the enabled function. While a sweep is in progress, a sweep overrange condition occurs if a sweep parameter exceeds the valid range for the selected function. If a sweep overrange condition occurs, the parameter, voltage, or frequency that is exceeded will remain at the maximum valid value for the enabled function.

Other sweep control commands are STARTFREQ, STOPFREQ, NSTEPS, STEPTIME, TYPE, MODE, and SWEEP.

STEPTIME

Type:

Setting or query

Setting syntax:

STEptime <num>[,<mode>]

where <mode> is one of the following:

Freq	for a frequency sweep.
Ampl	for an amplitude sweep.

Examples:

STEPTIME 13.7,F
STEPT .5,A
STE 20.3

Query syntax:

STEptime?

Query response syntax: (one of the following)

STEPT <num>,FREQ;
STEPT <num>,AMPL;

Discussion:

This command sets the time (in seconds) for each step specified for a frequency or amplitude sweep of the output signal. The optional argument <mode> selects either a frequency or amplitude sweep. If the optional argument is unspecified, the previous sweep mode is assumed. Valid arguments are:

<num> - .1 to 25.0 seconds with 0.1 second resolution.

<mode> - Freq or Ampl.

The MODE command also selects the sweep mode.

Other sweep control commands are STARTFREQ, STOPFREQ, STARTVOLTS, STOPVOLTS, NSTEPS, TYPE, and SWEEP.

STOPFREQ

Type:

Setting or query

Setting syntax:

STOPFreq <num>

Examples:

STOPFREQ 1E3
STOPF 50

Query syntax:

STOPFreq?

Query response syntax:

STOPF <num>;

Discussion:

This command sets the frequency at which a sweep of the output signal frequency ends. The beginning sweep frequency is set using the STARTFREQ command.

The instrument does not check that the value of the argument is valid for the enabled function. While a sweep is in progress, a sweep overrange condition occurs if a sweep parameter exceeds the valid range for the selected function. If a sweep overrange condition occurs, the parameter, voltage, or frequency that is exceeded will remain at the maximum valid value for the enabled function.

Other sweep control commands are STARTVOLTS, STOPVOLTS, NSTEPS, STEPTIME, TYPE, MODE, and SWEEP.

STOPVOLTS

Type:

Setting or query

Setting syntax:

STOPVolts <num>

Examples:

STOPVOLTS 12
STOPV 1E2

Query syntax:

STOPVolts?

Query response syntax:

STOPV <num>;

Discussion:

This command sets the amplitude (in Vrms) at which an amplitude sweep of the output signal ends. The STARTVOLTS command sets the beginning amplitude.

The instrument does not check that the value of the argument is valid for the enabled function. While a sweep is in progress, a sweep overrange condition occurs if a sweep parameter exceeds the valid range for the selected function. If a sweep overrange condition occurs, the parameter, voltage, or frequency that is exceeded will remain at the maximum valid value for the enabled function.

Other sweep control commands are STARTFREQ, STOPFREQ, NSTEPS, STEPTIME, TYPE, MODE, and SWEEP.

STORE

Type:

Operational and query

Syntax:

STORe <num>[,<num>...]
STORe <num>:<binblk>

Examples:

STORE 3,6,9
STORE 1,4
STOR 8

Query syntax:

STORe? <num>[,<num>...]

Query response syntax:

STORE <num>:<binblk>;

Discussion:

This command causes the instrument to store the current settings in the user-definable location or locations specified in the argument. Ten locations are available for storing settings, and are numbered 0 through 9. All settings are stored except for the following:

CLI
DT
OVER
OPC
PLI
RQS
USEREQ

The binary block argument data is obtained using the STORE? or LLSET? commands.

The data returned by the SG 5010 represents the setting information that is stored in the location specified in the <num> argument of the STORE operational command. The format of the binary block data is defined under the heading Control/Command Descriptions.

SWEEP

Type:

Operational

Syntax:

SWeep ON or SWeep Single
SWeep Repeat
Sweep OFf

Examples:

SWEEP ON
SW ON
SWEEP SINGLE
SW S
SWEEP REPEAT
SW R
SWEEP OFF
SW OF

Discussion:

This command selects the type of sweep sequence used for the output signal, as follows:

SWEEP ON or SWEEP SINGLE — Starts a single sweep sequence of the output signal.

SWEEP REPEAT — Starts a repetitive sweep sequence of the output signal.

SWEEP OFF — Stops the sweep of the output signal.

Other sweep control commands are STARTFREQ, STOPFREQ, STARTVOLTS, STOPVOLTS, NSTEPS, STEPTIME, TYPE, and MODE.

TEST

Type:

Output

Syntax:

TEst

Response syntax:

TEST <num>,...,<num>;

Discussion:

This command causes the instrument to perform the following series of self-tests: ROM placement tests, ROM checksum tests, stored settings tests, and hardware self tests. While the tests are performed, all front panel LED's illuminate.

The response returns one or more numbers indicating the results of the tests. If no failures are detected, a single argument equal to 0 is returned. Otherwise, the decimal error code for each type of failure detected is returned. After the tests are completed, the instrument is reconfigured to the settings enabled before the TEST command was executed.

TYPE

Type:

Setting or query

Setting syntax:

TYpe LIn
TYpe LOg

Examples:

TYPE LIN
TYPE LOG
TYPE LI
TY LO

Query syntax:

TYpe?

Query response: (one of the following)

TYPE LIN;
TYPE LOG;

Discussion:

This command selects either a linear or logarithmic sweep of the frequency or amplitude of the output signal. The optional argument of the NSTEPS command also selects the sweep type.

Other sweep control commands are STARTFREQ, STOPFREQ, STARTVOLTS, STOPVOLTS, STEPTIME, MODE, and SWEEP.

UNBALANCE

Type:

Setting

Setting syntax:

UNbalance

Examples:

UNBALANCE
UNBAL
UN

Discussion:

This command sets the output to the unbalanced state.

USEREQ (User Request)

Type:

Setting or query

Setting syntax:

USereq ON
USereq OFf

Examples:

USEREQ ON
USER OFF
US OF

Query syntax:

USereq?

Query response: (one of the following)

USER ON;
USER OFF;

Discussion:

This command controls the interrupt that asserts SRQ when the front panel INST ID button is pressed. The ON argument enables the interrupt; OFF disables it.

Other status interrupt commands are: CLI, OPC, OVER-RANGE, PLI, and RQS.

VPP (Volts Peak-to-Peak)

Type:

Setting or query

Setting syntax:

VPp <num>

Examples:

VPP 6.5
VPp 355E-3

Query syntax:

VPp?

Query response syntax:

VPP <num>;

Discussion:

This command converts the p-p value specified in the argument to its equivalent rms value and sets the amplitude to the Vrms value. Also sets the units for the AMPLITUDE command to Vrms.

The query command returns the amplitude setting in Vp-p units.

The following commands also set the amplitude:

AMPLITUDE
DBM
DBU
VRMS

VRMS

Type:

Setting or query

Setting syntax:

Vrms <num>

Examples:

VRMS 8.5
VRM 6
V 455E-3

Query syntax:

Vrms?

Query response syntax:

VRMS <num>;

Query response example:

VRMS 5.50;

Discussion:

This command sets the amplitude for the enabled function to the Vrms value specified in the argument. Also sets the units for the AMPLITUDE command to Vrms.

The following commands also set the amplitude:

AMPLITUDE
DBM
DBU
VPP

MESSAGES AND COMMUNICATION PROTOCOL

Command Separator

A message consists of one command or a series of commands, followed by a message terminator. Commands in multiple command messages must be separated by semicolons. A semicolon at the end of a message is optional. For example, each line below is a message.

```
INIT
TEST;INIT;RQS ON;USER OFF;ID?;SET?
TEST;
```

Message Terminator

Messages may be terminated with EOI or the ASCII line feed (LF) character. Some controllers assert EOI concurrently with the last data byte; others use only the LF character as a terminator. The instrument can be set to accept either terminator. With EOI ONLY selected as the terminator, the instrument interprets a data byte received with EOI asserted at the end of the input message; it also asserts EOI concurrently with the last byte of the output message. With the LF/EOI setting, the instrument interprets the LF character without EOI asserted (or any data byte received with EOI asserted) as the end of an input message; it transmits carriage return (CR) followed by line feed (the LF with EOI asserted) to terminate output messages.

Formatting A Message

Commands sent to TM 5000 instruments must have the proper format (syntax) to be understood; however, this format is flexible in that many variations are acceptable. The following describes the format and the acceptable variations.

The instruments expect all commands to be encoded in ASCII, with either upper or lower case ASCII characters acceptable. All data output is in upper case.

As previously discussed, a command consists of a header, followed, if necessary, by arguments. A command with arguments must have a header delimiter, which is the space character (SP) or a comma (,) between the header and the argument. The space character (SP), carriage return (CR), and line feed (LF) are shown as subscript in the following examples.

$RQS_{SP}ON$

If extra formatting characters SP, CR, and LF (the LF cannot be used for format in the LF/EOI terminator mode) are added between the header delimiter and the argument, those characters are ignored by the instrument.

Example 1: $RQS_{SP}ON;$

Example 2: $RQS_{SP\ SP}ON;$

Example 3: $RQS_{SP\ CR\ LF}$

$_{SP\ SP}ON$

In general, these formatting characters are ignored after any delimiter and at the beginning and end of a message.

$_{SP}RQS_{SP}ON;_{CR\ LF}$
$_{SP}USER_{SP}OFF$

In the command list, some headers and arguments are listed in two forms, a full-length version and an abbreviated version. The instrument accepts any header or argument containing at least the characters listed in the short form; any characters added to the abbreviated version must be those given in the full-length version. For documentation of programs, the user may add alpha characters to the full-length version. Alpha characters may also be added to a query header, provided the question mark is at the end.

```
USER?
USERE?
USEREQ?
USEREQUEST?
```

Multiple arguments are separated by a comma; however, the instrument will also accept a space, spaces, or a colon as a delimiter.

$2,3$
$2_{SP}3$
$2_{,SP}3$

NOTE

In the last example, the space is treated as a format character because it follows the comma (the argument delimiter).

Number Formats

The instrument accepts the following kinds of numbers for any of the numeric arguments.

— Signed or unsigned integers (including +0 and -0). Unsigned integers are interpreted as positive.

Examples: +1,2,-1,-10

— Signed or unsigned decimal numbers. Unsigned decimal numbers are interpreted as positive.

Examples: -3.2,+5.0,1.2

— Floating point numbers expressed in scientific notation.

Examples: +1.0E-2,1.0E-2,1.E-2,0.01E+0

Rounding of Numeric Arguments

The instrument rounds numeric arguments to the nearest unit of resolution and then checks for out-of-range conditions.

Message Protocol

Upon receipt by the instrument, a message is stored in the Input Buffer, then processed, and executed. Processing a message consists of decoding commands, detecting delimiters, and checking syntax. For *setting commands*, the instrument then stores the indicated changes in the Pending Settings Buffer. If an error is detected during processing, the instrument asserts SRQ, ignores the remainder of the message, and resets the Pending Settings Buffer. Resetting the Pending Settings Buffer avoids undesirable states that could occur if some *setting commands* are executed while others in the same message are not.

Executing a message consists of performing the actions specified by its command(s). For *setting commands*, this involves updating the instrument settings and recording these updates in the Current Settings Buffer. The *setting commands* are executed in groups--that is, a series of *setting commands* is processed and recorded in the Pending Settings buffer before execution takes place. This allows the user ot specify a new instrument state without having to consider whether a particular sequence would be valid. Normally, execution of the settings occurs when the instrument processes the message terminator, a *query-output command*, or an *operational command* in a message. The normal executiion of settings is modified by the DT *setting commands.*

When the instrument processes a *query-output command* in a message, it executes any preceding *setting commands* to update the state of the instrument. It then executes the *query-output command* by retrieveing the appropriate information and putting it in the Output Buffer. Processing and execution then continue for the remainder of the message. The data are sent to the controller when the instrument is made a talker.

When the instrument processes an *operational command* in a message, it executes any preceding *setting commands* before executing the *operational command.*

Multiple Messages

The Input Buffer has finite capacity and thus a single message may be long enough to fill it. In this case, a portion of the message is processed before the instrument accepts additional input. During command processing, the instrument holds off additional data (by asserting NRFD) until space is available in the buffer. When space is available, the instrument can accept a second message before the first has been processed. However, it holds off additional messages with NRFD until it completes processing the first.

After the instrument executes a *query-output command* in a message, it holds the response in its Output Buffer until the controller makes the instrument a talker. If the instrument receives a new message before all of the output from the previous message is read, it clears the Output Buffer before executing the new message. This prevents the controller from getting unwanted data from old messages.

One other situation may cause the instrument to delete output. The execution of a long message might cause both the Input and Output Buffers to become full. When this occurs, the instrument cannot finish executing the message because it is waiting for the controller to read the data it has generated; but the controller cannot read the data because it is waiting to finish sending its message. Because the instrument Input Buffer is full and it is holding off the rest of the controllers message with NRFD, the system is hung up with the controller and instrument waiting for each other. When the instrument detects this condition, it generates an error, asserts SRQ and deletes the data in the Output Buffer. This action allows the controller to transmit the rest of the message, and informs the controller that the message was executed and that the output was deleted.

A TM 5000 instrument can be made a talker without having received a message that specifies the output. In this case, an acquisition instrument (a counter or a multimeter) returns a measurement if one is ready. If no measurement is ready, it returns a single byte message with all bits equal to 1 (with message terminator). Non-acquisition TM 5000 instruments will return only this message.

Instrument Response to IEEE-488 Interface Messages

Interface messages and the effects of those messages on the instrument interface functions are defined in IEEE Standard 488-1978. Abbreviations from the standard are used in this discussion, which describes the effects of interface messages on instrument operation. The character A represents the instruments listen address (the sum of its primary GPIB address plus 32); B is the instruments talk address (the sum of its primary GPIB address plus 64).

UNL—Unlisten (WBYTE @63:)
UNT—Untalk (WBYTE @95:)

When the UNL command is received, the instrument listener function goes to its idle state (unaddressed). In the idle state, the instrument will not accept instrument commands from the IEEE-488 bus.

The talker function goes to its idle state when the instrument receives the UNT command. In this state, the instrument cannot supply output data via the bus.

The ADRS indicator is off when both the talker and listener functions are idle. If the instrument is either talk-addressed or listen-addressed, the indicator is on.

IFC—Interface Clear (Bus pin 9)

This uniline message has the same effect as both the UNT and UNL messages. The front panel ADRS indicator is off.

DCL—Device Clear (WBYTE @20:)

The Device Clear message reinitializes communication between the instrument and controller. In response to DCL, the instrument clears any input and output messages and any unexecuted settings in the Pending Settings Buffer. Also cleared are any errors or events waiting to be reported, except the power-on event. If the SRQ line is asserted for any reason other than power-on when DCL is received, SRQ is unasserted.

SDC—Selected Device Clear (WBYTE @A,4:)

This message performs the same function as DCL; however, only instruments that are addressed respond to SDC.

GET—Group Execute Trigger (WBYTE @A,8:)

The instrument responds to <GET> only if it is listen-addressed and the instrument device trigger function has been enabled by the Device Trigger command (DT). The <GET> message is ignored and an SRQ generated if the DT function is disabled (DT OFF), the instrument is in the local state, or if a message is being processed when <GET> is received.

SPE—Serial Poll Enable (WBYTE @24:)

The SPE message enables the instrument to supply output serial poll status bytes when it is talk-addressed.

SPD—Serial Poll Disable (WBYTE @25:)

The SPD message switches the instrument back to its normal operation of sending the data from the Output Buffer.

MLA—My Listen Address (WBYTE @A:)
MTA—My Talk Address (WBYTE @B:)

The primary listen and talk addresses are established by the instrument IEEE-488 bus address. The current setting of the bus address is displayed on the front panel readout window when the INST ID button is pressed. When the instrument is addressed to talk or listen, the front panel ADRS indicator is lighted. (A = bus address + 32; B = bus address + 64.)

LLO—Local Lockout (WBYTE @17:)

In response to LLO, the instrument changes to a lockout state—from LOCS to LWLS or from REMS to RWLS.

REN—Remote Enable (GPIB pin 17)

If REN is true, the instrument may change to a remote state (from LOCS to REMS if the internal message return-to-local (*rtl*) is false, or from LWLS to RWLS when its listen address is received. REN false causes a transition from any state to LOCS; the instrument stays in LOCS as long as REN is false.

A REN transition may occur after message processing has begun. In this case, execution of the message being processed is not affected by a transition.

GTL—Go To Local (WBYTE @A,1:)

Only instruments that are listen-addressed respond to GTL by changing to a local state. Remote-to-local transitions caused by GTL do not affect the execution of the message being processed when GTL was received.

Remote-Local Operation

The preceding discussion of interface messages describes the state transitions caused by GTL and REN. Most front panel controls cause a transitiion from REMS to LOCS by asserting a message called return-to-local (*rtl*). This transition may occur during message execution; but, in contrast to GTL and REN transitions, a transition initiated by *rtl* does affect message execution. In this case, the instrument generates an error if there are any unexecuted *setting* or *operational commands*. Front panel controls that change only the display (such as INST ID) do not affect the remote-local states—only front panel controls that change settings assert *rtl*. The *rtl* message remains asserted while multiple keystroke settings are entered, and it is unasserted after the execution of the settings. Since *rtl* prevents transition to REMS, the instrument unasserts *rtl* if a multiple button sequence is not completed in a reasonable length of time (approximately 5 to 10 seconds).

The instrument maintains a record of its settings in the Current Settings Buffer and new settings from the front panel or the controller update these recorded settings. In additiion, the front panel is updated to reflect setting changes caused by commands. Instrument settings are unaffected by transitions between the four remote-local states. The REMOTE indicator is lighted when the instrument is in REMS or RWLS.

Local State (LOCS)

In LOCS, instrument settings are controlled by the operator via front panel pushbuttons. When in LOCS, only bus commands that do not change instrument settings are executed *(query-output commands)*. All other bus commands (*setting* and *operational*) generate an error since those functions are under front panel control.

Local Without Lockout State (LWLS)

The instrument operates the same as it does in LOCS, except that *rtl* will not inhibit a transition to remote.

Remote State (REMS)

In this state, the instrument executes all instrument commands. For commands having associated front panel indicators, the front panel is updated when the commands are executed.

Remote With Lockout State (RWLS)

Instrument operation is similar to REMS operation except that the *rtl* message is ignored. (The front panel is locked out.)

STATUS AND ERROR REPORTING

Through the Service Request function (defined in the IEEE-488 Standard), the instrument may alert the controller that it requires service. This service request is also a means of indicating that an event (a change in status or an error) has occurred. To service a request, the controller performs a Serial Poll. In response, the instrument returns a Status Byte (STB), which indicates whether it was requesting service or not. The STB can also provide a limited amount of information about the request. The format of the information encoded in the STB is given in Fig. 3-2. Note that, when data bit 8 is set, the STB conveys Device Status information, which is contained in bits 1 through 4.

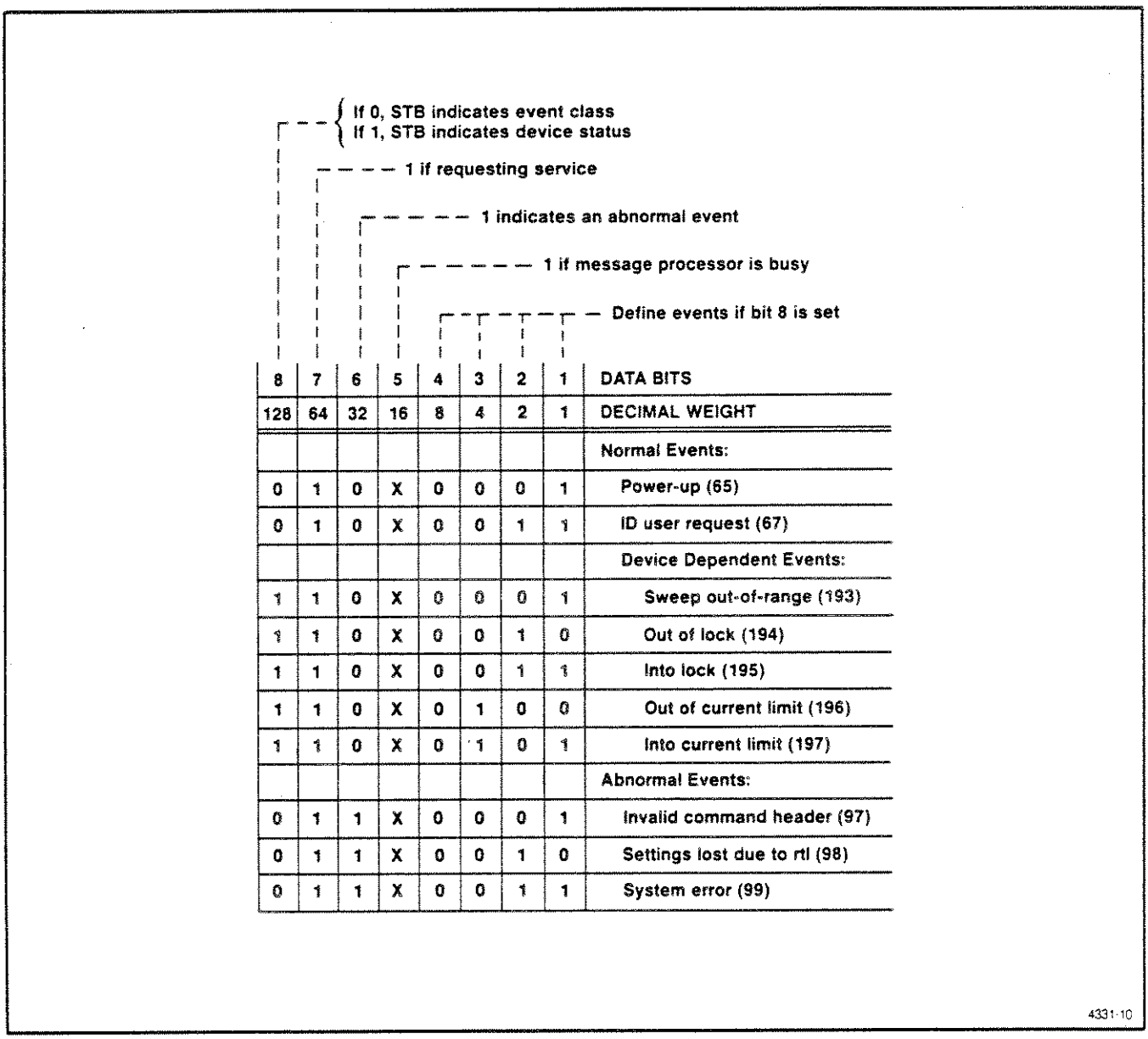
Because the STB conveys limited information about an event, the events are divided into classes; the Status Byte reports the class. The classes of events are defined as follows:

COMMAND ERROR—Indicates that the instrument has received a command that it cannot understand.

EXECUTION ERROR—Indicates that the instrument has received a command that it cannot execute. (This is causes by out-of-range arguments or settings that conflict.)

INTERNAL ERROR—Indicates that the instrument has detected a hardware condition or firmware problem that prevents operation.

SYSTEM EVENTS—Events that are common to instruments in a system (e.g., Power On, User Request, etc.).



8	7	6	5	4	3	2	1	DATA BITS
128	64	32	16	8	4	2	1	DECIMAL WEIGHT
								Normal Events:
0	1	0	X	0	0	0	1	Power-up (65)
0	1	0	X	0	0	1	1	ID user request (67)
								Device Dependent Events:
1	1	0	X	0	0	0	1	Sweep out-of-range (193)
1	1	0	X	0	0	1	0	Out of lock (194)
1	1	0	X	0	0	1	1	Into lock (195)
1	1	0	X	0	1	0	0	Out of current limit (196)
1	1	0	X	0	1	0	1	Into current limit (197)
								Abnormal Events:
0	1	1	X	0	0	0	1	Invalid command header (97)
0	1	1	X	0	0	1	0	Settings lost due to rtl (98)
0	1	1	X	0	0	1	1	System error (99)

Fig. 3-2. Definition of STB bit configuration with examples.

EXECUTION WARNING—Indicates that the instrument is operating, but that the user should be aware of potential problems.

INTERNAL WARNING—Indicates that the instrument has detected a problem (e.g., out-of-calibration). (The instrument remains operational, but the problem should be corrected.)

DEVICE STATUS—Device Dependent events.

The instrument can provide additional information about many of the events, particularly the errors reported in the Status Byte. After determining that the instrument requested service (by examining the STB), the controller may request the additional information by sending an ERR query (ERR?). In response, the instrument returns a code that defines the event. These codes are described in Table 3-1.

Table 3-1
ERROR QUERY AND STATUS INFORMATION

ABNORMAL EVENTS

Event	Priority	Error Query Response or Displayed Code	Serial Poll Response[a]
Command Errors:			
Invalid command header	2	101	97
Header delimiter error	2	102	97
Argument error	2	103	97
Argument delimiter error	2	104	97
Missing argument		106	97
Invalid message unit delimiter	2	107	97
Binary block checksum error	2	108	97
Binary block byte-count error	2	109	97
Execution Errors:			
Not executable in local mode	3	201	98
Settings lost due to rtl	3	202	98
Input and output buffers full	3	203	98
Argument out-of-range	3	205	98
Group Execute Trigger ignored	3	206	98
Amplitude/Balance conflict	3	261	98
Amplitude/RSource conflict	3	262	98
Amplitude/Function conflict	3	263	98
Frequency/Function conflict	3	264	98
Sweep Parameter conflict	3	265	98
Internal Errors:			
Interrupt fault	4	301	99
System error	4	302	99
Output overloaded[b]	5	309	99
Analog power supply error[b]	6	310	99
Phase lock error[b]	7	315	99
Current limit error[b]	8	319	99
Sine wave oscillator error[b]	9	320	99
Oscillator 1 k band error[b]	10	321	99
Oscillator 10 k band error[b]	11	322	99
Oscillator 100 k band error[b]	12	323	99
Square wave generator error[b]	13	324	99
Burst generator error[b]	14	325	99
Burst lo byte counter error[b]	15	326	99
Burst hi byte counter[b]	16	327	99
Burst gate line asserted error[b]	17	328	99
Burst gate line unasserted error[b]	18	329	99
40 Hz IM Freq error[b]	19	330	99

[a]If the GPIB message processor is busy, the number returned for a serial poll is 16 (decimal) higher than the number listed.

[b]This error is also displayed on the instrument front panel.

Table 3-1 (cont.)

ABNORMAL EVENTS

Event	Priority	Error Query Response or Displayed Code	Serial Poll Response[a]
50 Hz IM Freq error[b]	20	331	99
60 Hz IM Freq error[b]	21	332	99
80 Hz IM Freq error[b]	22	333	99
100 Hz IM Freq error[b]	23	334	99
125 Hz IM Freq error[b]	24	335	99
250 Hz IM Freq error[b]	25	336	99
500 Hz IM Freq error[b]	26	337	99
System RAM failure[c]		340	
GPIB address setting cell error[c]		348	
Power-up stored settings cell error[b]	27	349	99
Stored settings cell 0 error[b]	27	350	99
Stored settings cell 1 error[b]	27	351	99
Stored settings cell 2 error[b]	27	352	99
Stored settings cell 3 error[b]	27	353	99
Stored settings cell 4 error[b]	27	354	99
Stored settings cell 5 error[b]	27	355	99
Stored settings cell 6 error[b]	27	356	99
Stored settings cell 7 error[b]	27	357	99
Stored settings cell 8 error[b]	27	358	99
Stored settings cell 9 error[b]	27	359	99
8000 ROM placement error[c]		368	
C000 ROM placement error[c]		372	
8000 ROM checksum error[c]		388	
C000 ROM checksum error[c]		392	
Execution Warning:			
Signature analysis mode[c]		521	

NORMAL EVENTS

Event	Priority	Error Query Response or Displayed Code	Serial Poll Response[a]
System Events:			
Power-up	1	401	65
Operation complete	28	402	66
ID user request	30	403	67
No errors or events		0	128
Device Dependent Events:			
Sweep step out-of-range	29	702	193
Out of lock	29	731	194
Into lock	29	732	195
Out of current limit	29	733	196
Into current limit	29	734	197

[c]This error is only displayed on the instrument front panel.

If there is more that one event to be reported, the instrument continues to assert SRQ until it reports all events. (SRQ "stacking" consists of reporting only the latest event of each priority level.) Each event is automatically cleared when it is reported via Serial Poll. The Device Clear (DCL) interface message may be used to clear all events except Power-On.

Commands are provided to control the reporting of some individual events and to disable all service requests. For example, the User Request command (USER) provides individual control over the reporting of the user request event that occurs when the front panel INST ID button is pressed. The Request for Service command (RQS) controls whether the instrument reports any events with SRQ.

RQS OFF inhibits all SRQ's. When RQS is OFF, the ERR query allows the controller to find out about events without first performing a Serial Poll. With RQS OFF, the controller may send the ERR query at any time and the instrument will return an event waiting to be reported. The controller can clear all events by sending the ERR query until a zero (0) code is returned, or clear all events except Power-On through the DCL interface message.

With RQS OFF, the controller may perform a Serial Poll, but the Status Byte contains only Device Dependent Status information. With RQS ON, the STB contains the class of the event and a subsequent error query returns additional information about the previous event reported in the STB.

Responses to Interface Messages

Interface messages and the effects of those messages on the SG 5010 interface functions are defined in IEEE Standard 488-1978. Abbreviations from that standard are used in this description of the effects on instrument operation.

Bus interface control messages can be sent as low-level commands through the use of WBYTE controller commands. In the following list of interface control messages, A represents the instruments listen address (32 plus the instrument address), and B represents its talk address (64 plus the address).

Listen (MLA)	WBYTE @ A:
Unlisten (UNL)	WBYTE @ 63:
Talk (MTA)	WBYTE @ B:
Untalk	WBYTE @ 95:
Untalk-Unlisten	WBYTE @ 63,95:
Device Clear (DCL)	WBYTE @ 20:
Selective Device Clear (SDC)	WBYTE @ A,4:
Go To Local (GTL)	WBYTE @ A,1:
Remote with Lockout (RWLS)	WBYTE @ A,17,63:
Local Lockout (LLO)	WBYTE @ 17:
Group Execute Trigger <GET>	WBYTE @ A,8:
Serial Poll Enable (SPE)	WBYTE @ 24:
Serial Poll Disable (SPD)	WBYTE @ 25:

These commands are for TEKTRONIX 4050-Series controllers, but are representative of those for other controllers.

POWER-ON SEQUENCES AND SETTINGS

Each time power is applied to the SG 5010, the internal microprocessor performs a self-test diagnostic routine to check the instrument RAM and ROM functionality. If a RAM or ROM error is found, an error code will be displayed on the front panel readout. In this error state, the SG 5010 will not respond to input from the front panel or the IEEE-488 bus interface.

If no RAM or ROM error is found, the microprocessor performs further routines that check the functionality of other instrument hardware. Internal errors detected after the RAM and ROM tests have been completed successfully will be reported at the front panel and/or over the IEEE-488 bus. In this error state, the SG 5010 will respond to input and will attempt to operate despite the error. After successful power-on, an error code may be removed from the display by pressing the front panel CLEAR button. The ENTER button will display each accumulated error code, one at a time. The display will be filled with blanks when all error codes have been displayed.

When the self-test has been completed, the SG 5010 enters the local state (LOCS) and assumes the settings in use when previously powered down, with the following changes:

CLI OFF
DT OFF
OPC OFF
OVER OFF
PLI OFF
RQS ON
USER OFF

If a power-up stored settings error occurs, the SG 5010 assumes the following default settings:

Header	Argument
AMPL	1:VRMS;
BAL	ON;
CLI	OFF;
DISPLAY	VRMS;
DT	OFF;
FREQ	10000;
FUNC	SINE;
GND	OFF;
IMF	60;
NSTEP	30,LOG;
OFFCYC	90;
ONCYC	10;
OPC	OFF;
OUT	OFF;
OVER	OFF;
PLI	OFF;
RSRC	600;
RQS	ON;
STARTF	20;
STOPF	20000;
STARTV	0.1;
STOPV	10.0;
SWEEP	OFF;
STEPT	0.1,FREQ;
USER	OFF;

After the SG 5010 completes the power-up self test and initializes its settings, it also asserts the SRQ line on the IEEE-488 bus unless the bus address is set to 31.

Additional assistance in developing specific application oriented software is available in the following Tektronix manuals.

1. 070-3985-00 GPIB Programming Guide. This manual is specifically written for applications of this instrument in IEEE-488 systems. It contains programming instructions, tips, and some specific example programs.
2. 070-2270-00 4051 GPIB Hardware Support Manual. This manual gives an in-depth discussion of IEEE-488 bus operation, explanations of bus timing details and early bus interface circuitry.
3. 070-2058-01 Programming in BASIC.
4. 070-2059-01 Graphic programming in BASIC.
5. 062-5971-01 4050-Series programming aids, T1 (includes software).
6. 062-5972-01 4050-Series programming aids, T2 (includes software).
7. 070-2380-01 File Manager operators manual.
8. 070-2128-00 4924 Users manual.
9. 070-1940-01 4050-Series graphic system operators manual.
10. 070-2056-01 4050-Series graphic system reference manual.
11. 070-3918-00 4041 operators manual.
12. 070-3917-00 4041 Programming reference manual.

ASCII & IEEE 488 (GPIB) CODE CHART

B7 B6 B5 / BITS B4 B3 B2 B1	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
	CONTROL		NUMBERS SYMBOLS		UPPER CASE		LOWER	
0 0 0 0	0 NUL 0 (0)	20 DLE 10 (16)	40 SP 20 (32)	60 0 30 (48)	100 @ 40 (64)	120 P 50 (80)	140 ` 60 (96)	160 p 70 (112)
0 0 0 1	1 GTL SOH 1 (1)	21 LLO DC1 11 (17)	41 ! 21 (33)	61 1 31 (49)	101 A 41 (65)	121 Q 51 (81)	141 a 61 (97)	161 q 71 (113)
0 0 1 0	2 STX 2 (2)	22 DC2 12 (18)	42 " 22 (34)	62 2 32 (50)	102 B 42 (66)	122 R 52 (82)	142 b 62 (98)	162 r 72 (114)
0 0 1 1	3 ETX 3 (3)	23 DC3 13 (19)	43 # 23 (35)	63 3 33 (51)	103 C 43 (67)	123 S 53 (83)	143 c 63 (99)	163 s 73 (115)
0 1 0 0	4 SDC EOT 4 (4)	24 DCL DC4 14 (20)	44 $ 24 (36)	64 4 34 (52)	104 D 44 (68)	124 T 54 (84)	144 d 64 (100)	164 t 74 (116)
0 1 0 1	5 PPC ENQ 5 (5)	25 PPU NAK 15 (21)	45 % 25 (37)	65 5 35 (53)	105 E 45 (69)	125 U 55 (85)	145 e 65 (101)	165 u 75 (117)
0 1 1 0	6 ACK 6 (6)	26 SYN 16 (22)	46 & 26 (38)	66 6 36 (54)	106 F 46 (70)	126 V 56 (86)	146 f 66 (102)	166 v 76 (118)
0 1 1 1	7 BEL 7 (7)	27 ETB 17 (23)	47 ' 27 (39)	67 7 37 (55)	107 G 47 (71)	127 W 57 (87)	147 g 67 (103)	167 w 77 (119)
1 0 0 0	10 GET BS 8 (8)	30 SPE CAN 18 (24)	50 (28 (40)	70 8 38 (56)	110 H 48 (72)	130 X 58 (88)	150 h 68 (104)	170 x 78 (120)
1 0 0 1	11 TCT HT 9 (9)	31 SPD EM 19 (25)	51) 29 (41)	71 9 39 (57)	111 I 49 (73)	131 Y 59 (89)	151 i 69 (105)	171 y 79 (121)
1 0 1 0	12 LF A (10)	32 SUB 1A (26)	52 * 2A (42)	72 : 3A (58)	112 J 4A (74)	132 Z 5A (90)	152 j 6A (106)	172 z 7A (122)
1 0 1 1	13 VT B (11)	33 ESC 1B (27)	53 + 2B (43)	73 ; 3B (59)	113 K 4B (75)	133 [5B (91)	153 k 6B (107)	173 { 7B (123)
1 1 0 0	14 FF C (12)	34 FS 1C (28)	54 , 2C (44)	74 < 3C (60)	114 L 4C (76)	134 \ 5C (92)	154 l 6C (108)	174 | 7C (124)
1 1 0 1	15 CR D (13)	35 GS 1D (29)	55 - 2D (45)	75 = 3D (61)	115 M 4D (77)	135] 5D (93)	155 m 6D (109)	175 } 7D (125)
1 1 1 0	16 SO E (14)	36 RS 1E (30)	56 . 2E (46)	76 > 3E (62)	116 N 4E (78)	136 ^ 5E (94)	156 n 6E (110)	176 ~ 7E (126)
1 1 1 1	17 SI F (15)	37 US 1F (31)	57 / 2F (47)	77 ? UNL 3F (63)	117 O 4F (79)	137 UNT _ 5F (95)	157 o 6F (111)	177 RUBOUT (DEL) 7F (127)

ADDRESSED COMMANDS

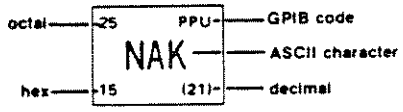
UNIVERSAL COMMANDS

LISTEN ADDRESSES

TALK ADDRESSES

SECONDARY ADDRESSES OR COMMANDS

KEY TO CHART



3391-13

Fig. 3-3. ASCII and IEEE 488 (GPIB) Code Chart.

PROGRAMMING EXAMPLES

```
100   ! ************************************************************
110   ! ******  TALKER/LISTENER PROGRAM FOR 4052A / SG 5010  ******
120   ! ************************************************************
130   !
140   ! JulY 11, 1983
150   !
160   ! PURPOSE:
170   ! Supports operator interaction with the SG 5010 over the GPIB.
180   ! The operator may enter SG 5010 commands and observe the
190   ! results.  Service requests, such as for an incorrect command,
200   ! are handled.
210   !
220   ! REQUIRED EQUIPMENT:
230   ! 4052A Controller
240   ! SG 5010 Programmable 160 kHz Oscillator
250   !
260   ! VARIABLES USED:
270   !
280   ! Sg_pri_addr -- SG 5010 primary address.  Assigned value of 25.
290   ! Change if instrument set to other address.
300   !
310   ! Spoll_stat -- Status returned by serial poll from first
320   ! instrument requesting service.
330   !
340   ! Addr_list_indx -- Address list index returned by serial poll.
350   !
360   ! Addr_list -- Array of addresses found by CONFIG routine.
370   !
380   ! Config_code -- Flag returned by config routine.
390   !
400   ! Sg_command$ -- Commands entered by the operator and directed
410   ! to the SG 5010.
420   !
430   ! SG_response$ -- Response from the SG 5010 to Sg_command$
440   ! (null if no output command contained in Sg_command$).
450   !
460   ! ROUTINE CALLED:
470   ! Serial poll subroutine handles instrument service requests
480   ! from all instruments on the bus.
490   !
500   ! POSSIBLE ERRORS:
510   ! SG 5010 primary address is set different than the number
520   ! assigned to Sg_pri_addr.
530   !
540 INIT
550 DIM Sg_response$(300),Sg_command$(100),Addr_list(15)
560 Sg_pri_addr=25
570   !
580 CALL "config",Config_code,Addr_list
590 IF Config_code THEN
600    PRINT "Configuration routine failed due to problem on GPIB."
610    STOP
620 END IF
630   !
640 ON SRQ THEN 790
650   !
660 PRINT "SG 5010 TALKER/LISTENER PROGRAM"
670   !
680 PRINT "Enter command message:  ";
690 INPUT Sg_command$
700 PRINT @Sg_pri_addr:Sg_command$
710 INPUT @Sg_pri_addr:Sg_response$
720 PRINT Sg_response$
```

4331-11

Fig. 3-4. SG 5010 Talker Listener program (4052A).

```
730 GO TO 680
740 END
750   !
760   ! Serial poll routine
770 LOCAL Sg_report$
780 DIM Sg_report$(80)
790 POLL Addr_list_indx,Spoll_stat;Addr_list
800 IF Addr_list(Addr_list_indx)=Sg_pri_addr THEN
810    PRINT @Sg_pri_addr:"id?;errmsg?"
820    INPUT @Sg_pri_addr:Sg_report$
830    PRINT "ADDRESS=";Addr_list(Addr_list_indx),"STATUS=";Spoll_stat
840    PRINT Sg_report$
850 END IF
860 RETURN   ! From service request subroutine
```

4331-12

Fig. 3-4 cont. SG 5010 Talker Listener program (4052A).

```
100   ! ***************************************************************
110   ! ********  TALKER/LISTENER PROGRAM FOR 4041 / SG 5010  *********
120   ! ***************************************************************
130   !
140   ! June 16, 1983
150   !
160   ! PURPOSE:
170   ! Supports operator interaction with the SG 5010 over the GPIB.
180   ! The operator may enter SG 5010 commands and observe the results.
190   ! Service requests, such as for an incorrect command, are handled.
200   !
210   ! REQUIRED EQUIPMENT:
220   ! 4041 Controller (V2.0)
230   ! SG 5010 Programmable 160 kHz Oscillator
240   !
250   ! VARIABLES USED:
260   !
270   ! Sg_pa --  SG 5010 primary address.  Assigned value of 25.  Change if
280   ! instrument set to other address.
290   !
300   ! Sg_port -- Port where SG 5010 connected.  Assigned value of 0.
310   ! Change if instrument is connected to GPIB1 instead of GPIB0.
320   !
330   ! Sgstrem$ -- Stream specification for SG 5010.
340   !
350   ! Spollsta -- Status returned by first instrument found requesting service.
360   !
370   ! Spolladd -- Address of first instrument found requesting service.
380   !
390   ! Command$ -- Commands entered by the operator and directed to the SG 5010.
400   !
410   ! Respons$ -- Response of the SG 5010 to command$ (null if no output
420   ! command contained in command$).
```

4331-13

Fig. 3-5. SG 5010 Talker Listener program (4041).

```
430   !
440   ! LOGICAL UNIT USED:
450   ! 100:  Assigned to SG 5010 stream spec.
460   !
470   ! ROUTINE CALLED:
480   ! Pollbus  Handles request for service from any instrument on the
490   ! bus selected by the SG 5010 stream spec.
500   !
510   ! POSSIBLE ERRORS:
520   ! Sg_pa or sg_port variables do not match the SG 5010 primary address or
530   ! port where SG 5010 is connected, respectively.
540   !
550     Dim respons$ to 300,command$ to 100,ggstrem$ to 20
560     Integer sg_pa,spollsta,spolladd,sg_port
570     Sg_pa=25
580     Sg_port=0
590   !
600     Ggstrem$="gpib"&str$(sg_port)&"(pri="&str$(sg_pa)&");"
610     Open #100:ggstrem$
620     Select ggstrem$
630     On srq then call pollbus
640     Enable srq
650   !
660 Tlk_lisn:     input prompt "Enter command message:  ":command$
670     Input #100 prompt command$:respons$
680     Print respons$ ! SG 5010 returns blank line if not queried in command$
690     Goto tlk_lisn
700     End ! Main
800 Sub pollbus local report$
810   ! PURPOSE:
820   ! Handles gpib service requests.  Polls all primary addresses until
830   ! source of srq is found.  If srq from instrument at SG 5010 primary
840   ! address, routine queries id and error message.
850   !
860   ! LOCAL VARIABLE:
870   ! Report$:  Id and event report from instrument at sg_pa if it has srq.
880   !
890     Dim report$ to 80
900     Poll spollsta,spolladd
910     If spolladd=sg_pa then input #100 prompt "id?;errmsg?":report$
920     Print report$,"STATUS=";spollsta,"ADDRESS=";spolladd,"PORT=";val(ggstrem$)
930     Resume
940     End ! Sub pollbus
```

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Fig. 3-5 cont. SG 5010 Talker Listener program (4041).

```
100   ! ***************************************************************
110   ! ********** 10 HZ TO 100 KHZ RESPONSE TO LOG SWEEP ************
120   ! ***************************************************************
130   !
140   ! For 4052A, 5/16/83
150   !
160   ! Copyright (c) 1983, Tektronix Inc.  All rights reserved.
170   ! This software is provided on an "as is" basis without warranty
180   ! of any kind.  It is not supported.
190   !
200   ! This program may be reproduced without prior permission, in
210   ! whole or in part, by the original purchaser.  Copies must
220   ! include the above copyright and warranty notice.
230   !
240   ! PURPOSE:
250   ! Records the response of a system to a leveled input signal
260   ! between 10 Hz and 100 kHz and prints the results.
270   !
280   ! REQUIRED EQUIPMENT:
290   ! SG 5010 Programmable 160 kHz Oscillator at address 25
300   ! DM 5010 Programmable Digital Multimeter at address 16
310   ! 4052A Controller
320   !
330   ! GLOBAL VARIABLES:
340   ! Addr:  Address array of instruments found by Config routine.
350   ! Coderet:  Flag set by Config routine.
360   ! E$:  Report returned by instrument that requests service.
370   ! Npoints:  Number of points in frequency sweep.
380   ! Sg_freq:  Array of frequency points in sweep.
390   ! Outamp:  Array of DM 5010 readings from each point in sweep.
400   ! Ampin:  Amplitude of SG 5010 signal.
410   ! Lim4settl:  Tolerance used to check DM readings for settling.
420   ! Freqstart:  Beginning point of sweep.
430   ! Freqstop:  Ending point of sweep.
440   ! Sg_pa:  SG 5010 primary address.
450   ! DM_pa:  DM 5010 primary address.
460   ! Lff:  Flag for state of DM 5010 low-frequency response function.
470   ! Measure:  Reading returned from DM settling routine.
480   ! Index:  Index to Addr array set by POLL.
490   ! Stabyt:  Status byte acquired by the serial poll handler.
500   !
510   ! SUBPROGRAMS CALLED:
520   !  logsweep:  Generates frequency points for sweep.
530   ! Sttldrdg:  Gets reading from DM 5010, allowing for settling.
540   !
550   ! OPERATING INSTRUCTIONS
560   ! Connect 4052A and TM 5000 power module with GPIB cable.
570   ! Set DM 5010 and SG 5010 message terminator to EOI ONLY.
580   ! Change instrument addresses or variables sg_pa and dm_pa so
590   !   the program and instruments agree.
600   ! Connect SG 5010 out to DUT in and DUT out to DM 5010 in.
610   !
620   ! ERRORS:
630   ! No GPIB error handlers are linked so program stops with default
640   ! system error message if error such as wrong address occurs.
650   !
660   ! INSTRUMENT CONTROL:
670   ! Polls all instruments on GPIB by primary address only.
680   !
690 INIT
700   !
710 DIM Addr(15)
720 CALL "config",Coderet,Addr
```

4331-15

Fig. 3-6. SG 5010 program example (4052A).

```
730 IF Coderet THEN
740    IF Coderet=1 THEN
750       PRINT "More than 15 devices connected to GPIB."
760    ELSE
770       PRINT "No one home on GPIB.  Check power to instruments and GP
          IB"
780       PRINT "cable connections."
790    END IF
800    PRINT "Fix problem and RUN the program again."
810    STOP
820 END IF
830 ON SRQ THEN 1320
840    !
850    ! Set variables
860 Npoints=41
870 DIM Ss_freq(Npoints),Outamp(Npoints),E$(35)
880 Outamp=0
890 Ampin=0.5
900 Lim4settl=0.1   ! Passed to sub sttldrdg; because DM is set
910    !              to dBr, .1 is equivalent to about 1%.
920 Freqstart=10
930 Freqstop=100000
940 Ss_pa=25
950 Dm_pa=16
960    !
970    ! Init instruments
980 PRINT @Ss_pa:"init;vrms ";Ampin;";out on"
990 PRINT @Dm_pa:"init;acv;dbr ";Ampin;";calc dBr;dis 3.5"
1000    ! dB referred to ampin; dis 3.5 is faster and loses no accuracy
1010    ! in acv compared to dis 4.5.
1020    !
1030 CALL _lossweep(Freqstart,Freqstop,Npoints,Ss_freq)
1040    !
1050    ! Log data within FOR/NEXT loop
1060 Lfr=0   ! DM if resp function was turned off above by INIT to DM
1070 FOR N=1 TO Npoints
1080    PRINT @Ss_pa: USING "faxfd.1d":"freq";Ss_freq(N)
1090    IF Ss_freq(N)<20 THEN    ! Set DM lfr function on below 20 Hz
1100       IF NOT(Lfr) THEN    ! Skip if lfr already on
1110          PRINT @Dm_pa:"lfr on"
1120          Lfr=1
1130       END IF
1140    ELSE    ! Set DM low-frequency response off for 20 Hz and above
1150       IF Lfr THEN    ! Skip if lfr already off
1160          PRINT @Dm_pa:"lfr off"
1170          Lfr=0
1180       END IF
1190    END IF
1200    CALL Sttldrdg(Dm_pa,Lim4settl,Measure)
1210    Outamp(N)=Measure   ! Can't pass by reference into array
1220 NEXT N
1230    !
1240    ! Display results
1250 PRINT USING "fa3xfa":"FREQUENCY","GAIN"
1260 FOR N=1 TO Npoints
1270    PRINT USING "2x6d11t4d.1d":Ss_freq(N),Outamp(N)
1280 NEXT N
1290    !
1300 END
1310    ! Sub to handle srqs
1320 POLL Index,Stabyt;Addr   ! Polls using array obtained by Config
1330 PRINT @Addr(Index):"id?;err?"
1340 INPUT @Addr(Index):E$
```

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Fig. 3-6 cont. SG 5010 program example (4052A).

```
1350 PRINT "ADDRESS ";Addr(Index),"STATUS ";Stabyt,E$
1360 RETURN
1370   ! ************************************************************
1380   !                    4052A  LOG Sweep Subroutine
1390   !
1400   !  PURPOSE:
1410   !  Generates an array of frequencies which are distributed
1420   !  logarithmically according to the input parameters.
1430   !
1440   !  INPUTS:
1450   !  Param1 (Fstart):  Sweep start frequency.
1460   !  Param2 (Fstop):  Sweep stop frequency.
1470   !  Param3 (_points):  Number of frequency points in sweep.
1480   !
1490   !  OUTPUT:
1500   !  Array Freqar contains the calculated discrete frequencies.
1510   ! ************************************************************
1520 SUB _logsweep(Fstart,Fstop,_points,Freqar)
1530    LOCAL Nsteps,Stsize,Index,Count
1540    Nsteps=_points-1
1550    Stsize=(LGT(Fstop)-LGT(Fstart))/Nsteps
1560    Index=0
1570    FOR Count=LGT(Fstart) TO LGT(Fstop) STEP Stsize
1580       Index=Index+1
1590       Freqar(Index)=10^Count
1600    NEXT Count
1610 END SUB
1620   ! ************************************************************
1630   !           DM 5010 SETTLING SUBROUTINE
1640   !
1650   ! PURPOSE:
1660   ! Compares successive DM readings in a circular queue.  Returns
1670   ! last reading when settling occurs or average of readings in
1680   ! the queue if settling does not occur.  DM setup is not changed.
1690   ! If dBr or dBm is used, the second parameter is effectively
1700   ! converted to a relative rather than absolute tolerance.
1710   !
1720   ! INPUTS:
1730   ! Param 1 (Pa):       DM 5010 GPIB primary address.
1740   ! Param 2 (Sttlim):   Tolerance for successive readings to
1750   !                     indicate settling.
1760   !
1770   ! OUTPUT:
1780   ! Param 3 (_reading): Settled or averaged reading.
1790   !
1800 SUB Sttldrdg(Pa,Sttlim,_reading)
1810    LOCAL Qsize,Circlq,Frontq,Tryvalue,Sttlerr,Arrptr,Match
1820    Qsize=5  ! How many to average if settling does not occur
1830    DIM Circlq(Qsize)  ! Circular queue of size n
1840    Circlq=3000  ! Prevent match on first pass to uninitialed data
1850    Match=0
1860    Frontq=0
1870    Tryvalue=0
1880    DO
1890       Frontq=Tryvalue MOD Qsize  ! Modulo n arithmetic on q 0 to n-
           1
1900       Arrptr=Frontq+1  ! Adjust pointer for array index of 1 to n
1910       PRINT @Pa:"SEND"
1920       INPUT @Pa:Circlq(Arrptr)
1930         ! Compare new value to one just ahead in circular q, e.g.,
1940         !   1 is ahead of 2, 4 ahead of 5, 5 ahead of 1, etc.
1950       Sttlerr=ABS(Circlq(Arrptr)-Circlq((Frontq+Qsize-1 MOD Qsize)+
           1))
```

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Fig. 3-6 cont. SG 5010 program example (4052A).

```
1960        IF Sttlerr<=Sttlim THEN
1970           Match=Match+1
1980        EXIT IF Match=>5  ! Success if successive readings close
1990        ELSE
2000           Match=0
2010        END IF
2020     EXIT IF Tryvalue>60  ! Allows about 3 seconds in DIG 3.5 mode
2030        Tryvalue=Tryvalue+1
2040     LOOP
2050     IF Match=>5 THEN
2060        _readings=Circle(Arrptr)
2070     ELSE
2080        _readings=SUM(Circle)/Qsize  ! If not settled, average last n
2090     END IF
2100  END SUB
```

4331-18

Fig. 3-6 cont. SG 5010 program example (4052A).

```
100   ! ************************************************************************
110   ! ************* 10 HZ TO 100 KHZ RESPONSE TO LOG SWEEP *************
120   ! ************************************************************************
130   !
140   ! For 4041, May 16, 1983
150   !
160   !
170   ! Copyright (c) 1983 Tektronix, Inc.  All rights reserved.  This
180   ! software is provided on an "as is" basis without warranty of
190   ! any kind.  It is not supported.
200   !
210   ! This program may be reproduced without prior permission, in whole
220   ! or in part, by the orisinal purchaser.  Copies must include the
230   ! above copyright and warranty notice.
240   !
250   ! PURPOSE:
260   ! Records the response of a system to a leveled input signal
270   ! between 10 Hz and 100 kHz and prints the results.
280   !
290   ! REQUIRED EQUIPMENT:
300   ! SG 5010 Programmable 160 kHz Oscillator at GPIB primary address 25.
310   ! DM 5010 Programmable Disital Multimeter at primary address 16.
320   ! 4041 Controller (V2.0 BASIC)
330   !
340   ! GLOBAL VARIABLES:
350   !
360   ! Stabyt:     Contains status byte returned by serial poll.
370   ! Addr:       Contains primary address of instrument reporting stabyt.
380   ! Nsteps:     Number of steps in sweep including end points.
390   ! Ss_pa:      SG 5010 primary address--change if SG set other than 25.
400   ! Dm_pa:      DM 5010 primary address--   "      "  DM   "    "    "  16.
410   ! Ss_lu:      SG 5010 logical unit number senerated by program.
420   ! Dm_lu:      DM 5010    "      "      "      "    "    "
430   ! Port:       Set to GPIB0, change if GPIB1 used.
440   ! Port$:      String of port number senerated by program.
450   ! Pos_pa:     Used for building logical unit numbers.
460   ! Lu$:        Used in building instrument stream specs.
```

4331-19

Fig. 3-7. SG 5010 program example (4041).

```
470   ! N:          Counter in sweep loop.
480   ! Ss_freq:    Array of frequencies passed by main program by sub logsweep.
490   ! Lfr:        State of DM 5010 low-frequency response function.
500   ! Frqstrt:    Sweep starting frequency.
510   ! Frqstop:    Sweep ending frequency.
520   ! Ampin:      Amplitude of SG 5010 stimulus in volts rms.
530   !
540   ! SUPROGRAMS CALLED:
550   ! Polibus:  Handles service requests on selected GPIB port.
560   ! Logsweep:  Generates frequency values for log sweep.
570   ! Settrdg:  Gets settled DM 5010 readings, if settling occurs soon enough.
580   !
590   ! OPERATING INSTRUCTIONS:
600   ! Connect 4041 GPIB0 (unless program changed) and TM 5000 power module.
610   ! Change ss_pa and dm_pa as needed for other primary addresses.
620   ! DM 5010 and SG 5010 message terminator should be set for EOI ONLY.
630   ! Connect SG 5010 out to DUT in and DUT out to DM 5010 in.
640   !
650   ! ERRORS:
660   ! No GPIB error handler is provided; errors such as instrument power
670   ! off will terminate the program.
680   !
690   ! INSTRUMENT CONTROL:
700   ! Selects the port where logical unit numbers for SG 5010 and DM 5010 are OPENed.
710   ! Polls all instruments by primary address only on selected port.
720   !
730   ! Set variables
740     Init var all
750     Integer stabyt,addr,nsteps,ss_pa,dm_pa,ss_lu,dm_lu,port,lfr,n,pos_pa
760     Nsteps=41
770     Dim ss_freq(nsteps),outamp(nsteps)
780     Frqstrt=10
790     Frqstop=1.0E+5
800     Ampin=0.5
810     Lim4setl=0.1 ! Passed to sub that gets settled DM readings.  Since DM is
820   !                  set to dBr, .1 is equivalent to about 1% of reading.
830   !
840   ! Open logical units
850     Port=0
860     Ss_pa=25
870     Dm_pa=16
880     Port$="gpib"&str$(port)&":"
890     Select port$
900     Ss_lu=100
910     Dm_lu=101
920     Lu$=port$
930     Rep$(lu$,6,0)="(pri="&str$(ss_pa)&")" ! Mod for SG address first
940     Open #ss_lu:lu$
950     Pos_pa=pos(lu$,"=",1)+1
960     Rep$(lu$,pos_pa,pos(lu$,")",1)-pos_pa)=str$(dm_pa) ! Mod for DM address
970     Open #dm_lu:lu$
980   !
990     On srq then call polibus
1000    Enable srq
1010  !
1020    Call logsweep(frqstrt,frqstop,nsteps,ss_freq) ! Get freq values for sweep
1030  !
1040  ! Init instruments
1050    Print #ss_lu:"init;vrms";ampin;"out on"
1060    Print #dm_lu:"init;acv;dbr";ampin;"calc dbr;dig 3.5"
1070  ! Read in dBr referred to value in ampin; dig 3.5 is faster with no loss
1080  ! in accuracy in ac volts.
1090  !
```

4331 20

Fig. 3-7 cont. SG 5010 program example (4041).

```
1100    ! Log data within for/next loop
1110      Lfr=0 ! DM 5010 low-freq response function was set off by INIT above.
1120      For n=1 to nsteps
1130        Print #sg_lu:"freq";sg_freq(n)
1140        If sg_freq(n))=20 then goto 1180 ! Use low-frequency response function
1150        If not(lfr) then print #dm_lu:"lfr on" ! in DM 5010 only below 20 Hz.
1160        Lfr=1
1170        Goto 1200
1180        If lfr then print #dm_lu:"lfr off"
1190        Lfr=0
1200        Outamp(n)=settlrdg(dm_lu,lim4set) ! Get settled readings
1210.       Next n
1220    !
1230    ! Display freq and amplitude out recorded during sweep.
1240      Print using "fa3xfa":"FREQUENCY","GAIN"
1250      For n=1 to nsteps
1260        Print using "2x6d11t5.1s":sg_freq(n),outamp(n)
1270        Next n
1280    !
1290      End
1400 Sub pollbus local e$ ! Global stabyte, addr, port
1410    !
1420    ! PURPOSE:
1430    ! Autopolls selected port; prints address and status report.
1440    ! Uses low-level i/o for id and error report so can be used for
1450    ! for either port.  Id? and err? work only with Tek C&F instruments.
1460    !
1470    ! LOCAL VARIABLE:
1480    ! e$:  Contains response to id and err queries
1490    !
1500      Dim e$ to 35
1510      Poll stabyt,addr
1520      Wbyte atn(unl,addr+32,mta),"id?;err?",eoi,atn(unl,unt,mla,addr+64)
1530      Rbyte e$
1540      Wbyte atn(unl,unt)
1550      Print e$;"Address=";addr,"Port=";port,"Status=";stabyt
1560      Resume
1570      End
1600 Sub logsweep(fstart,fstop,points var freqar) local steps,stepsize,index,count
1610    ! ********************************************************
1620    !                    4041 LOG SWEEP SUBROUTINE
1630    !
1640    ! PURPOSE:
1650    ! Generates an array of frequencies that are distributed logarithmically
1660    ! according to the input parameters.
1670    !
1680    ! INPUTS:
1690    ! Parameter 1 (fstart):  Sweep start frequency.
1700    ! Parameter 2 (fstop):   Sweep stop frequency.
1710    ! Parameter 3 (points):  Number of frequency points in sweep.
1720    !
1730    ! OUTPUT:
1740    ! Array freqar contains the calculated discrete frequencies.
1750    !
1760      Integer index,steps
1770      Steps=points-1
1780      Stepsize=(lgt(fstop)-lgt(fstart))/steps
1790      Index=0
1800      For count=lgt(fstart) to lgt(fstop) step stepsize
1810        Index=index+1
1820        Freqar(index)=10^count
1830        Next count
1840      Return
1850      End
1900 Function settlrdg(lu,settllim) local qsize,circlq,settlerr,match,frontq,tryvalue,arrptr
```

433121

Fig. 3-7 cont. SG 5010 program example (4041).

```
1910    ! ***************************************************************
1920    !              DM 5010 SETTLING SUBROUTINE
1930    !
1940    ! PURPOSE:
1950    ! Compares successive DM readings input to circular queue.  Returns
1960    ! last reading when settling occurs or average of readings in the
1970    ! queue if settling does not occur.  DM setup is not changed.
1980    ! If dBr or dBm is used, the second parameter is effectively
1990    ! converted to a relative rather than absolute tolerance.
2000    !
2010    ! INPUT:
2020    ! Parameter 1 (lu):       DM 5010 logical unit number.
2030    ! Parameter 2 (setlim):   Tolerance for successive readings to indicate
2040    !                        settling.
2050    !
2060    ! OUTPUT:
2070    ! Function name (ampread):  Settled or averaged reading.
2080    !
2090      Integer match,qsize,frontq,tryvalue,arrptr ! Automatically zeroed
2100      Qsize=5 !                    How many will be averaged if no settling
2110      Long circlq(qsize) ! Set up circular q of size n
2120      Circlq=3000 ! Improbable value for DM reading
2130      For tryvalue=0 to 60 ! Allows about 3 seconds if DM in DIG 3.5 mode
2140        Frontq=tryvalue mod qsize ! Modulo n arithmetic assumes q from 0 to n-1
2150        Arrptr=frontq+1 !  Adjust pointer because array runs from 1 to n
2160        Input #lu prompt "send":circlq(arrptr)
2170    ! Compare new value to one just ahead of it in array that holds the
2180    ! circular queue: 2 to 1, 3 to 2, 4 to 3, 5 to 4, 1 to 5, etc.
2190        Settlerr=abs(circlq(arrptr)-circlq((frontq+qsize-1 mod qsize)+1))
2200        If settlerr(=setllim then match=match+1 else match=0
2210        If match)=5 then exit to settled ! Success--successive readings close to each other
2220        Next tryvalue
2230      Settlrds=sum(circlq)/qsize ! Failed to settle--average last n readings
2240      Return ! with average reading
2250  Settled:     settlrds=circlq(arrptr)
2260      Return ! with settled reading
2270    ! Return
2280      End
```

4331-22

Fig. 3-7 cont. SG 5010 program example (4041).

```
100   ! ::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::
110   ! :::::::::::::: SG 5010 / 4052A COMMAND PROGRAM ::::::::::::::
120   ! ::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::
130   !
140   ! July 11, 1983
150   !
160   ! Copyright (c) 1983, Tektronix, Inc.  All rights reserved.
170   ! This software is provided on an "as is" basis without
180   ! warranty of any kind.  It is not supported.
190   !
200   ! This software may be reproduced without prior permission
210   ! in whole or in part.  Copies must include the above
220   ! copyright and warranty notice.
230   !
240   ! REQUIRED EQUIPMENT:
250   ! SG 5010 Programmable 160 kHz Oscillator
260   ! 4052A Controller w/ 4052R14 GPIB Enhancement Rompack, Opt 1A
270   !
280   ! PURPOSE:
290   ! Lockout SG 5010 front panel and then generate:  1) sine wave
300   ! burst 2) frequency sweep, and 3) amplitude sweep.  The
310   ! program waits after 1 and 2 for a user interrupt (ID button
320   ! press).  SG 5010 front panel control is restored after 3.
330   !
340   ! OPERATING PROCEDURE:
350   ! Connect the TM 5000 mainframe to 4052A GPIB port.  Set
360   ! the SG 5010 address to 25 (factory default).  Enter the
370   ! program and run it.  To verify operation, monitor the SG
380   ! 5010 output with an oscilloscope.  Set vertical at 1 V/div,
390   ! horizontal at 20 ms/div, and triggering to normal a little
400   ! above center screen.  Trigger adjustment or automatic
410   ! triggering may be required to view amplitude sweep.
420   !
430   ! PROGRAM VARIABLES AND LABELS:
440   !
450   ! Sg_pa -- Primary address of SG 5010.
460   !
470   ! _poll_stat -- Status returned by serial poll of GPIB.
480   !
490   ! Addr_lis_indx -- Index to Addrs_list set by serial poll.
500   !
510   ! Addr_list -- List of addresses found by CALL "config".
520   !
530   ! Stat_report$ -- Id and event message reported by SG 5010.
540   !
550   ! Conf_code -- Required by CALL "Config", not used by program.
560   ! ::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::
570 INIT
580 PRINT "SG 5010 COMMAND PROGRAM"
590   !
600 DIM Addr_list(15)
610 Sg_pa=25
620 CALL "config",Conf_code,Addr_list
630 IF Conf_code THEN
640    PRINT "Check for instruments connected and power on, then reRUN."
650    STOP
660 END IF
670 ON SRQ THEN 1010
680   !
690 CALL "llo"
700 PRINT "SG 5010 front panel locked out."
710   !
720 PRINT "Press SG 5010 ID key to step through three setups."
```

4331-23

Fig. 3-8. SG 5010 Command Program (4052A).

```
730 I=0
740 DO
750     I=I+1
760     GOSUB I OF 840,880,920
770 EXIT IF I>2
780     WAIT
790     IF NOT(_poll_stat=67 AND Addr_list(Addr_list_indx)=Sg_pa) THEN
        780
800 LOOP
810 END
820   !
830   ! Set up IHF202-like test burst
840 PRINT @Sg_pa:"INIT;FREQ 1.0E+3;FUNC BURST;10;USER ON;VRMS 2"
850 PRINT @Sg_pa:"ONCYCL 20;OFFCYCL 480;OUT ON"
860 RETURN
870   ! Set up log frequency sweep from 10 Hz to 100 kHz
880 PRINT @Sg_pa:"FUNC SINE;MODE FREQ;STARTFREQ 10;STOPFREQ 100.E+3"
890 PRINT @Sg_pa:"NSTEPS 40:LOG;STEPTIME .2;SWEEP REPEAT"
900 RETURN
910   ! Set up voltage sweep from 20 mV to 2 volts
920 PRINT @Sg_pa:"SWEEP OFF;FREQ 1.E+3;MODE AMP;STARTVOLTS .02"
930 PRINT @Sg_pa:"STOPVOLTS 2;NSTEPS 20:LOG;STEPTIME .1;SWEEP REPEAT"
940 RETURN
950   !
960 CALL "locs"  ! Unlock instrument front panels.
970 PRINT "Front panel control restored."
980 PRINT "End of program."
990 END
1000   ! Poll the bus for service request
1010 POLL Addr_list_indx,_poll_stat;Addr_list
1020 CALL "vartst",_poll_stat,239,_poll_stat  ! Mask busy bit
1030 IF Addr_list(Addr_list_indx)=Sg_pa THEN
1040    PRINT @Sg_pa:"ID?;ERRMSG?"
1050    INPUT @Sg_pa:Stat_report$
1060    PRINT Stat_report$
1070 END IF
1080 PRINT "ADDRESS=";Addr_list(Addr_list_indx),"STATUS=";_poll_stat
1090 RETURN
```

4331-24

Fig. 3-8 cont. SG 5010 Command Program (4052A).

```
100   ! ::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::
110   ! :::::::::::::: SG 5010 / 4041 COMMAND PROGRAM ::::::::::::::
120   ! ::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::
130   !
140   ! July 11, 1983
150   !
160   ! Copyright (c) 1983, Tektronix, Inc.  All rights reserved.
170   ! This software is provided on an "as is" basis without
180   ! warranty of any kind.  It is not supported.
190   !
200   ! This software may be reproduced without prior permission
210   ! in whole or in part.  Copies must include the above
220   ! copyright and warranty notice.
230   !
240   ! REQUIRED EQUIPMENT:
250   ! SG 5010 Programmable 160 kHz Oscillator
260   ! 4041 Controller (V2.0)
270   !
280   ! PURPOSE:
290   ! Program the SG 5010 to lockout the front panel and: 1) Generate
300   ! a sine wave burst, 2) frequency sweep, and 3) amplitude sweep.
310   ! The program waits after 1 and 2 for a user interrupt (ID button
320   ! press).  SG 5010 front panel control is restored after 3.
330   !
340   ! OPERATING PROCEDURE:
350   ! Connect the TM 5000 mainframe to 4041 GPIB port 0.
360   ! Set the SG 5010 address to 25 (factory default).
370   ! Enter the program and run it.  To verify operation, monitor
380   ! the SG 5010 output with an oscilloscope.  Set vertical at 1 V/div,
390   ! horizontal at 20 ms/div, and triggering to normal a little
400   ! above center screen.  Trigger level adjustment or automatic
410   ! trigger may be required to view amplitude sweep.
420   !
430   ! PROGRAM VARIABLES and LABELS:
440   !
450   ! Sg_lu -- Logical unit number of SG 5010.
460   !
470   ! I -- Counter for waveform types (seem comments under PURPOSE).
480   !
490   ! Poll_sta -- Status returned by serial poll on the GPIB.
500   !
510   ! Poll_add -- Address of instrument reporting poll_sta.
520   !
530   ! Sta_rpt$ -- Id and event code reported by SG 5010.
540   !
550   ! Address -- Line where SG 5010 logical unit variable is assigned.
560   ! Burst --  Beginning line for block that generates a signal burst.
570   ! Frq_swp       "        "    "    "      "       "     " frequency sweep.
580   ! Amp_swp       "        "    "    "      "       "     an amplitude sweep.
590   ! Poll_bus      "        "    "    "      "  handles serial poll.
600   !
610   ! Finish -- Where program goes to end.
620   ! ::::::::::::::::::::::::::::::::::::::::::::::::::::::::::::
630     Init var all
640     Print "SG 5010 COMMAND PROGRAM"
650     Dim sta_rpt$ to 80
660     Integer sg_lu,poll_sta,poll_add,i
670 Address:     sg_lu=25 ! Default lu equal to GPIB primary address
680     On srq then gosub poll_bus
690     Enable srq
700   !
710   !Wbyte llo !    Lockout front panel of instruments on bus.
720     Print "Front panel locked out."
```

4331 25

Fig. 3-9. SG 5010 Command Program (4041).

```
730   !
740     Print "Press SG 5010 ID key to step through three setups."
750     For i=1 to 3
760       Gosub i of burst,frq_swp,amp_swp
770       If i>2 then exit to finish
780       Wait
790       If poll_sta<>67 or poll_add<>ss_lu then goto 780 ! Check for ID key press
800       Next i
810   !
820   ! Set up IHF A202-like test burst
830 Burst:      print #ss_lu:"INIT;FREQ 1.0E+3;FUNC BURST;10;USER ON;VRMS 2"
840     Print #ss_lu:"ONCYCL 20;OFFCYCL 480;OUT ON"
850     Return
860 Frq_swp:      print #ss_lu:"FUNC SINE;MODE FREQ;STARTFREQ 10;STOPFREQ 100.E+3"
870     Print #ss_lu:"NSTEPS 40;LOG;STEPTIME .1;SWEEP REPEAT"
880     Return
890 Amp_swp:      print #ss_lu:"SWEEP OFF;FREQ 1.E+3;MODE AMP;STARTVOLTS .02"
900     Print #ss_lu:"STOPVOLTS 2;NSTEPS 20;LOG;STEPTIME .1;SWEEP REPEAT"
910     Return
920   !
930 Poll_bus:      poll poll_sta,poll_add
940     Poll_sta=poll_sta band [11101111b] ! Mask busy bit
950     If poll_add<>ss_lu then goto 980
960     Input #ss_lu prompt "id?;errmsg?":sta_rpt$
970     Print sta_rpt$
980     Print "ADDRESS=";poll_add,"STATUS=";poll_sta
990     Resume
1000  !
1010 Finish:      wbyte ren(0),ren(1) ! Unlock instrument front panels
1020    Print "Front panel control restored."
1030    Print "End of program."
1040    End
```

4331-26

Fig. 3-9 cont. SG 5010 Command Program (4041).

DELETED

Table 10-13
COMPONENT REFERENCE CHART

P/O A13 ASSY — LOGIC INTERFACE 13

CIRCUIT NUMBER	SCHEMATIC LOCATION	BOARD LOCATION
C1020	F6	B1
C1021	C8	C1
C2060	G4	G2
CR1011	E6	A1
CR1013	G6	A2
CR1021	E8	B2
CR2011	H8	A3
CR2021	I6	B3
CR2060	G2	F2
CR2061	F2	F2
CR3011	L7	A4
CR3012	M8	A4
CR3021	J7	B3
CR4011	I8	A4
J1051	B1	F1
J1051	B3	F1
J1051	M1	F1
J1051	M6	F1
J2051	B1	F3
J2051	M1	F3
J2051	M3	F3
K1011	E7	A1
K1013	G7	A2
K1021	E8	B1
K2021	I6	B3
K3011	L7	A3
K3012	H8	A3
K3031	J7	C4
K4011	M8	A4
K4021	I8	B5
P1051	B1	F1
P1051	B3	F1
P1051	M1	F1
P1051	M6	F1
P2051	B1	F3
P2051	M1	F3
P2051	M3	F3
Q1011	E7	A1
Q1021	E8	B2
Q1052	G5	F2
Q1053	E3	F1
Q1062	H6	F2
Q1063	D3	G1
Q2011	G7	A2
Q2012	H8	A2
Q2020A	D6	B2
Q2020B	G8	B2
Q2020C	L8	B2
Q2020D	K7	B2
Q2020E	I6	B2
Q2020F	E8	B2
Q2020G	G6	B2
Q2021	L6	B2
Q2051	H5	E2
Q2060	F4	F2
Q2061	F4	G2
Q2062	H1	F2
Q2063	G2	G2
Q3011	I7	B3
Q3012	J7	B3
Q3013	M9	A4
Q3014	L7	A4
Q4011	I8	B4
R2013A	D7	A2
R2013B	G8	A2
R2013C	G7	A2
R2013D	E8	A2
R2013E	I7	A2
R2013F	I7	A2
R2013G	L8	A2
R2013H	K7	A2
R2014A	K8	B2
R2014B	L9	B2
R2014C	I7	B2
R2014D	E8	B2
R2014E	F7	B2
R2014F	G8	B2
R2014G	D7	B2
R2051	I1	F2
R2055	C6	F2
R2060	I2	F2
R2061A	H5	F2
R2061B	F4	F2
R2061C	D2	F2
R2061D	F3	F2
R2061E	E3	F2
R2061F	H5	F2
R2061G	G4	F2
R3021	L6	B3
R4022	I8	B4
U2022	C9	B2
VR2051	C2	F3
VR3024	L6	B3
W530	B1	CHASSIS
W530	M1	CHASSIS
W530	M3	CHASSIS
W540	B1	CHASSIS
W540	B3	CHASSIS
W540	B7	CHASSIS
W540	B9	CHASSIS
W540	M1	CHASSIS
W540	M6	CHASSIS

P/O A13 ASSY also shown on 14 15 16

THEORY OF OPERATION

Reference Oscillator ◇2◇ (A12)

The 4 Mhz reference oscillator sets the timing for the CPU and the phase lock loops. The oscillator circuitry is composed of Q4030, Q3041, Y4040, C4032, and other components. The crystal Y4040 sets the frequency for the oscillator. The output at the collector of Q4030 passes through C4041 which ac couples the elevated voltage to the base of Q3041, a TTL buffer. This signal then goes into U3050C and outputs to the microprocessor and the phase lock loop board (diagram 6).

+12 V Supply ◇2◇

The +33 V (+25 V) from rear edge connector J3010, pins 12A and 12B passes through fuse F4021 and light bulb DS3030. DS3030 provides current limiting for the +12 V supply and relieves some of the power requirements of Q3040, the +12 V regulator. The zener diode, VR3040 sets the reference voltage for Q3040 at approximately +12.6 V which is decoupled by C3043. This voltage also supplies the reference for the +5 V (set by zener diode VR3033 with R3032 as a current source) and is used by other circuits in the SG 5010.

+5 V Supply ◇2◇

Operational Amplifier U3030B is the control element for the +5 V supply and provides approximately +5.1 V output. This voltage drives the NPN transistor which drives the PNP transistor (both located in the power module). The NPN transistor emitter connects to the PNP transistor collector at R3023 (current sense for the +5 V supply). Transistor Q3030 is the current limit set transistor and shorts out the NPN transistor base when current limit occurs.

The 5.6 V zener diode, VR4021 with R4023, C4021, and Q4031, comprise an overvoltage protect circuit that triggers Q4031 and opens the 8 V line fuse, F4022, if the voltage at the top of R3023 exceeds 6.2 V. Components C4021, R4023, and R4030 comprise damping elements that protect Q4031 from voltage transients.

Transistor Q3080 with CR3041 and R3037 form a saturating switch. When the +8 V is higher than the +5 V supply, this switch turns on RPWR line (at Q3080 emitter) shorting the line to the +5 V rail. Resistor R4080 maintains the chip select for the RAM ($\overline{\text{RON}}$ line) at a high level when power is off. Capacitor C3090 provides some decoupling and CR5080 keeps the lithium battery (BT5060) from being charged. Resistor R5080 provides short circuit protection to the battery. The battery has a built in resistor for additional protection.

The reset power-on, power-off detect circuit works primarily as follows. In a TM 5000-Series power module, the power-on signal comes in the rear edge connector and passes through diode CR4022. It is held low during the power-on reset interval (approximately 100 ms) which forces the output of U3030C low, the output of Q3081 high, and the $\overline{\text{RON}}$ line high. The RAM is, therefore, disabled and running at a very low current. This action also pulls down on Q2032 emitter voltage which holds C2032 at a low voltage. This keeps the output of U3030D low which keeps the microprocessor reset. When the power-on signal from the power module goes high, the output of U3030C goes high which enables the memory (the chip select goes low). Through R2041 and CR2041, capacitor C2032 slowly charges until the voltage exceeds the +5 V threshold, at which point the output of U3030D goes high. Components R2033 and C2031, and R3041 and C3041 supply hysteresis and some amount of noise reduction to U3030D and U3030C. Since both operational amplifiers use +12 V as a rail, CR2031 keeps the voltage on the reset line from exceeding +5 V and R2032 ensures the voltage goes up to +5 V. Also, R2035 assures that the reset line is pulled down hard enough to drive everything on the line. Diode CR2032 assures that this voltage doesn't go much below ground (about 0.3 V).

The TM 500-Series power module does not provide a power-on signal to the SG 5010. Resistors R4024 and R3042 are a devider network that set the +5.5 V, in absence of the power-on signal. When the +8 V supply reaches approximately +5.5 V, the same actions occur as described above for the power module power-on line going high. The RAM is protected when this +5.5 V point is detected, if the power supply voltage drops.

−12 V Supply ◇2◇

The −33 V comes in the rear edge connector and passes through fuse F3020 and light bulb DS3020. As with the +12 V supply, DS3032 provides current limiting for the supply and relieves some of the power requirements of Q3021. Zener diode VR3021 sets the −12 V reference voltage for Q3021 and C3021 decouples the −12 V output.

25 Vac Supply ◇2◇

The 25 Vac power input from the power module connects to the primary winding of transformer T300 (diagram 16) through plug P1023 and fuses F2020 and F2022.

Microprocessor ◇3◇ A12

NOTE

For more detailed information on the internal operation of a microprocessor, refer to the manufacturers data sheet.

Integrated circuit U5040 is an 8-bit microprocessor containing an internal 1 MHz clock.

The internal, single phase, 1 MHz TTL clock output (E) on pin 37 is derived from the 4 MHz crystal controlled oscillator (diagram 2). This oscillator provides a stable and accurate timing element for the microprocessor's internal clock oscillator. The $\overline{\text{RESET}}$ signal starts the microprocessor from a power down condition (power failure or initial start up) and does not generate this signal until the power on signal from the TM 5000 power module is received. In a TM 500 power module, the reset circuitry generates its own delay. When a high level is detected on pin 40, the microprocessor begins the restart sequence.

Normal low level TTL interrupt request signals to U5040 occur on pin 4 ($\overline{\text{IRQ}}$) through on-board jumper, J2070. The microprocessor may or may not recognize this interrupt signal, depending on the operating conditions when the signal occurs. When recognized, the microprocessor completes its current instruction before servicing the current interrupt condition. The jumper (J2070) is used to disconnect the IRQ line for troubleshooting the microprocessor. This jumper may be removed when running forced instruction mode. Refer to the Maintenance section for details. Another on-board jumper, J3050, in the MR (Memory Ready) line performs the same function as J2070.

The microprocessor uses two output control lines, VMA (Valid Memory Access) pin 5 and R/$\overline{\text{W}}$ (Read/Write) pin 34 to read and write data over the peripheral devices. The R/$\overline{\text{W}}$ signal goes low to write data or goes high to read data from the data buses.

The VMA line goes low to indicate the 16-bit code on the address bus is not a valid memory address. VMA does not go low between machine instructions unless the microprocessor is using the address register for some operation other than accessing a valid location in memory or input/output peripherals. VMA is not gated by or necessarily related to the clock (E) in any way.

The data lines, D0 through D7 enter the octal latch, U5021 which drives the Digital-To-Analog Converter (DAC), U5020. The DAC output drives the amplifier, U3030A. Zener diode, VR3022 holds U3030A output between +12 V and ground. The feedback network composed of C3031, C3022, R3024, and R3031 comprises a two-pole filter for the RAMP OUT signal.

Resistor pack, R4040 is removed when in the non-operating forced instruction mode. The data lines, D1 through D7 go to ground through resistor pack, R5021. Data line D0 goes to +5 V through resistor, R4031. This allows a non-operating forced instruction mode, and much of the microprocessor kernel may be exercised and verified apart from devices that may be malfunctioning on the Data Bus. The microprocessor sequentially increments through its entire address field, exercising many devices connected to the address bus in a repeatable and predictable fashion. This allows for verification of the kernel and may be used as an aid in distinguishing data-related problems from hardware problems when troubleshooting.

The address lines, A0 through A13 from the microprocessor, drive the two ROM's (U4050 and U4060). These ROMs contain the operational firmware for the SG 5010. Data is read from the ROM stage one byte at a time from any of 16k locations as addressed by the microprocessor. Each ROM contains 16k bytes of memory. The address lines A0 through A10 drive the RAM, U4080 (consisting of one 2k X 8-bit RAM) and a small amount of enable logic. The primary chip select IC, U2052 is a dual 1 of 4 decoder. Address lines A14 and A15 are decoded into four lines. Two lines, the most significant and second most significant bits, C, D, E, F (U2052 pin 9) and 89AB (U2052 pin 10) respectively, feed into the two ROMs (U4050 and U4060). Addresses C000 through FFFF access U4050 which contains all reset factors and IRQs (Interrupt Request). Addresses 8000 through BFFF access U4060 which contains some of the operating code.

When on-board jumper is in the SATEST (Signature Analysis Test) position, the driven address range (4, 5, 6, and 7) from 1Y1 (pin 11) causes D0 (J2071 pin 3) to be pulled down ; otherwise D0 remains high.

The signal from 2Y1 (U2052 pin 5) to the Address Decoder, U2060 (G2B) and U3052C, when low with $\overline{\text{E}}$ line low enables the Octal Buffer, U4082 (diagram 4). If pin 5 or $\overline{\text{E}}$ line is high, this buffer passes data in either direction. U2060 receives the address lines A10, A11, A12, and U2052 outputs and decodes this information. The decoded sequence

is 2000, 2400, 2800, 2C0, 3000, 3400, 3800, and 3C00 for the Y1 through Y7 outputs respectively. Output Y6 (U2060 pin 9) drives the 1 shot device, U3062A and its output (pin 7) drives back the MR (Memory Ready) line through J3050 to the MR on U5040, pin 3. Output Y6 also goes to the chip enable on the Display Driver (diagram 4). Driving the MR line causes the microprocessor to wait in order to meet the timing requirements of the Display Driver.

The other 1 shot device, U3062B receives the 1 MHz clock ($\overline{BE}$) and turns on, clocking the JK flip-flop, U2080B. The output Q (pin 9) pulls the $\overline{IRQ}$ line down, via Q2070. This causes the microprocessor to reset U2080B through the 3C00 decode line (U2060, pin 7). This signal is used to set a 1 ms timing for scanning through various operating modes of the instrument. Note that U3062B is held-off internally (pin 10 to pin 12) while on.

Another line INT coming from the GPIB (diagram 6) U2081 is also detected by the microprocessor, PIN 4 (IRQ line).

The output clock E is inverted by U3060B ($\overline{E}$) and buffered by U3052B ($\overline{BE}$) driving both ROMS and the 1 shot (U3062B). E clock also goes to U3060C and, in conjunction with U2052 and U3050D sets up the chip select for the RAM.

The R/$\overline{W}$ (Read/Write) signal is sent to the RAM and also to the Phase Lock Loop board (diagram 6).

The RAM also receives RPWR (RAM Power Line) signal from Q3080 (diagram 2) and the $\overline{RON}$ line on CE2 (Chip Enable Line 2), pin 18 indicating memory access.

Address lines A0 through A10 go to ground through resistor pack R4050. These lines to U4080 must connect to a power supply through a resistor. When the instrument is battery powered, the current through U4080 must be minimal. Minimum current flows when all the lines are at a legal voltage (either 0.8 V or above 2.4 V) and R4050 causes approximately 0 V on these lines.

CPU I/O ◇4◇ A12

The CPU I/O circuitry consists of the bi-directional buffer for the microprocessor and also has address buffering, display driver, and a keyboard sensor.

The purpose of the bi-directional buffer, U4082 is to assure the microprocessor isn't over loaded from input/output data over the bus. A resistor pack, R4090 provides U4082 CMOS voltage because U3090, the display driver is a CMOS chip and has different level requirements than the TTL components. The display driver is a multiplexer having internal display drivers and needs little circuitry for the displays. It receives buffered data lines (0 through 7), a write line (the display), and a mode line which is an address line from the microprocessor. The buffered address 1 (complement of address 1) and display generate the mode line. The mode line and buffered data lines access memory locations, inside the chip, which are scanned for driving the display. D1 through D8 are the main driver lines, from U3090, for groups of displays used on the front panel.

U3082 is an input buffer. It is driven with the LOCK DETECT line (from diagram 7) which also drives the out-of-lock LED on the front panel. The trigger in (BURST TRIG IN) and SYNC IN are signals from the CPU ISOLATORS (diagram 5).

The OVLOAD (Overload) line, from the output board (diagram 15) detects clipping or excessive current from the output amplifiers. This is sensed by the microprocessor through U3082 and drives the current limit LED on the front panel through Q5080.

The pot chip select, $\overline{POT}$ line from the address decoder, U2060 (diagram 3) when received, allows the microprocessor to enable data transfer from the inputs to the data lines.

The PEN LIFT line at U3082, pin 17 is the sense point for the GATE line from U2050 (diagram 5). This line also receives the AA 5001/SG 5010 INTERFACE signal which is enabled via jumper, P3071 (diagram 6).

Pins 6 and 13 of U3082 are the front panel digital knob detection lines from the two comparators, U3080A and U3080B. They detect the digital pot input voltage swing of approximately 2.5 V from the threshold voltage set by R3073 and R3070D. The pullup resistors (R2080 and R2082) and a low pass filter (R3072, C3072 and R3071, C3071) help to reduce the noise.

The LED DRIVER, U1101 drives the front panel LEDs for RUN, PARAMETER, NOT ENTERED, ERROR, ADDRESS, REMOTE, and outputs the phase lock reset line. It also transmits the main trigger (being optically coupled to the Burst circuitry board).

The BUFFERS, U3050A, U3050E, and U3050F receive address lines from the CPU board (diagram 3) and output

these lines (BA0 through BA2) to U1101. Pin 13 (U1101) is the data line, BD6 from U4090. This line, in conjunction with the reset line is write selected through the LED line and clears itself on power up.

The KEYBOARD ENCODER circuitry permits the use of forty front panel keyboard function keys with a chip (U4090) that is limited to 20 keys operation. Using U4092, U3092, and U3070B with U4090 allows an additional 20 user function keys. The keyboard scanner, U4092 communicates with the front panel keyboard (diagram 1) and operates using a set of keyboard drive lines, X1 through X4 and senses a set of switched lines, Y1 through Y5. Lines Z1 through Z5 are diode coupled to drive lines Y1 through Y5, also from the front panel keys.

If a front panel key intersecting an X-line and a Y-line is pressed, the Y-line is detected but the corresponding Z-line remains high. This causes a low on U3092 output, placing a low on U3070B pin 9 (latch) after receiving a clock signal from the DA (Data Available) line of U4092. If the front panel key intersecting an X-line and a Z-line is pressed, it drives U3092 output high and also pulls down on the Y-line.

U4092 scans the X-lines to determine if the Y-line was active and debounces the appropriate key. When the key is debounced, U4092 puts this data on the DOA through DOE lines and sets DA (pin 13) which latches U3070B as described previously.

U4090 buffers the data sent by U4092 and U3070B and outputs it to the data lines, BD0 through BD7.

CPU ISOLATORS ⟨5⟩ A12

The CPU Isolators circuitry couples the CPU and the floating secton of the instrument.

U2050 is an addressable latch. It drives the GATE line that is protected from going above +5 V or below ground by clamping diodes, CR1080 and CR2044. This line (PEN LIFT) drives U3082, pin 17 (as previously described, diagram 4), and connects to the power module and front panel.

The remaining output lines from U2050 supply the serial write signals to the oscillator for programming the hardware. Common data and latch lines are used for all serial information. The five clock outputs: IM CK, BURST CK, AMP CK, FREQ CLOCK, and the ATTENUATOR CK send information to the five shift registers (diagram 13). One data bit is placed on the data line, then clocked into the appropriate shift register by pulsing the appropriate clock line. This process is repeated until the shift register is full. The LATCH line (pin 12, U2050) is strobed to transfer this data to the outputs. The number of bits required varies from 8, for the IM and Attenuator data words; 16 bits, for the Frequency and Amplitude words; to 32 bits, for the Burst data word. The BURST GATE (Burst Trigger Detector) from the front panel or power module is protected from going above +5 V by diode CR2042. An internal diode in U3050B protects it from going below ground. The inverter, U3050B output drives the BURST TRIG IN and a set of latches (U3082, diagram 4). The MAIN TRIG and the BURST GATE (through U3050B) are OR'ed through U3052A. This output (high) resets U3070A which resets U2080A. This causes the opto-coupler, U2040 to turn off and outputs the trigger to the output board (diagram 13). The FL PHASELOCK DRIVE (Phase Lock Loop Drive) is optically coupled through U1030 and, as the trigger stops (the next V2 after that), the next arriving enable signal clocks U2080A. This output (pin 13) resets and the next phase lock loop drive pulse edge clocks U2080A. This operation allows the MAIN TRIG or BURST GATE pulses to elongate to the required length to trigger U2080A by U3070A. U2080A assures this pulse is long enough so it can be detected by the Burst circuitry.

The FL SYNC (Phase Lock Sync Line) from the output board (diagram 13) is ground isolated by opto-coupler, U1020. The couplers output is protected from going above +5 V and below ground by diodes CR1020 and CR1010, and goes through series resistors to the power module and to the front panel.

GPIB ⟨6⟩ A11

The GPIB interface circuits consist of the GPIB Interface, U2081 and two GPIB Drivers, U2051 and U2071. U2051 is used to transfer data and U2071 is used for handshake and management lines. U2081 sends and receives data over the IEEE-488 data bus via the GPIB driver, U2051 and communicates with the microprocessor via the bi-directional buffer, U4082 (diagram 4). Data transfer is under the control of commands from the IEEE-488 bus and control signals from various circuits within the SG 5010.

Phase Lock Loop ⟨7⟩ A11

The phase lock loop circuitry fine tunes the frequency of the main oscillator. It does this by phase locking the oscillator to a square wave of the desired frequency. This square wave is generated by another phase lock circuit which references itself to the CPU crystal oscillator. There are, as a result, two phase lock loops on the phase lock loop circuit board. The first generates the accurate frequency, the second locks the low distortion sine wave to this frequency.

Both the phase lock loop board and the main oscillator receive the same frequency information from the CPU. This consists of a 16-bit serial word having a 14-bit mantissa and a 2-bit exponent. The 14-bit mantissa has a maximum value of 16,383. This is used directly as the full scale value in each frequency band. The 2-bit exponent selects one of the following decade bands: 10 to 163.80 Hz, 163.9 Hz to 1.6380 kHz, 1.639 kHz to 16.380 kHz, and 16.39 kHz to 163.80 kHz. All bands represent a 10 to 1 range in frequency except the bottom band which ranges 16 to 1. Each binary value in the mantissa corresponds directly to the displayed frequency of the instrument. The diagram in Fig. 4-1 shows the bit order and gives a few examples.

U5151A and U5151D convert the 1 MHz microprocessor clock to a 1 MHz reference suitable for use by the phase lock loop circuitry. If an external 1 MHz is used, it is buffered by Q6171 and associated circuitry. Jumper P6161 selects one of these two signals which is fed to a divider chain composed of U5151B, U5151C, and U5071A. The output of this chain is an 8 kHz signal which is available at TP6061. This signal is further divided by a counter chain in phase lock loop IC U5061. This is a commercial "all in one" IC which is used for the bulk of the accurate frequency generation task. A block diagram from the manufacturers data sheet is shown in Fig. 4-2. The internal reference counter chain is set to divide by 16, this setting being accomplished by logic zeroes on pins 1, 2, and 18 of U5061. The resulting reference is 500 Hz, which is fed to one input of the phase detector internal to the IC.

The other input of the phase detector is fed from a 4-bit programmable counter. This counter divides the frequency of its input by any binary number up to 16383 (2 to the 14th power). A shift register and latch inside the IC accept the serial frequency information from the CPU and convert this to a 16-bit parallel word. The bottom 14 bits (the mantissa) are used as the preload information for the counter while the top two bits are available as open drain outputs on pins 13 and 14 of the phase lock loop IC, U5061. These are pulled and used to drive the range changing circuits on the board. The serial frequency information is input to the IC on the CLOCK, DATA, and ENABLE pins from the FREQUENCY CLOCK, DATA, and LATCH lines. The clock line is filtered to prevent false triggering of the IC by glitches from the CPU.

Frequency	MSB	Exponent x100	Exponent x10	8192	4096	2048	1024	512	256	128	64	32	16	8	4	2	1	LSB
163.80 kHz		1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	
16.380 kHz		1	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	
1.6380 kHz		0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	
163.80 Hz		0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	
4.096 kHz		1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	
4.099 kHz		1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	1	
2.000 kHz		1	0	0	0	0	1	1	1	1	1	0	1	0	0	0	0	
100.00 Hz		0	0	1	0	0	1	1	1	0	0	0	1	0	0	0	0	
10.00 Hz		0	0	0	0	0	0	1	1	1	1	1	0	1	0	0	0	

4331-60

Fig. 4-1. Frequency word bit patterns.

U5041, Q5033, Q5031 and associated components form a voltage controlled oscillator which spans the range of 500 kHz to 8 MHz. Q5031 is used as a current source. Its output charges C6031 forming a ramp which is seen by U5041A. When the voltage on the capacitor reaches the input threshold of the inverter, the inverter output goes low. This is inverted and buffered by three more gates from the same IC, and used to drive Q5033 which discharges the capacitor. When this happens the voltage on the capacitor drops below the threshold of the inverter, turning off the discharge transistor, causing the cycle to repeat. There is enough delay in the four gates to insure that the capacitor is fully discharged before the cycle repeats itself. CR5031, CR5041, R4041, and R4043 linearize the voltage to frequency characteristics of the VCO maintaining near constant gain for the complete loop. U5041C and U5041D buffer the discharge pulse from the VCO. This pulse signal drives the input of the programmable counter in the phase lock loop IC and drives a divider chain for later lockup with the main oscillator. The frequency of this oscillator will be 500 times the mantissa of the frequency word when the loop is locked.

The output of the phase detector on pin 6 of U5061 is a series of pulses whose width and polarity vary with the direction and magnitude of the phase error between the divided-down VCO and the 500 Hz reference. These pulses are converted to a dc voltage by the loop filter consisting of U6061A and its associated parts. This voltage drives the input of the VCO, forming a complete loop. The VCO drive voltage is available on TP6041 and ranges from −8 V at the highest frequencies to +2 V at the bottom frequency of the instrument. This voltage is also connected to U6061B which is used as a comparator. This senses when the frequency of the oscillator is programmed below approximately 4000 in any of the decade bands and goes low. In other words, the output of U6061B is low from 10 Hz to approximately 40 Hz, 164 Hz to 400 Hz, etc. This information is used to change loop filter time constants in the second phase lock loop.

The lock detect output of U5061 is a series of pulses at the reference frequency of 500 Hz. When the loop is locked, the pulses are a few nanoseconds wide. When the loop is unlocked, the pulses become much wider. This output, on pin 8 of U5061, is fed to a pulse width detector consisting of U5091B, R5101, and C5101. When the pulses get wider, approximately 1 μs, the output of U5091B goes high. This drives the lock detect line and resets the phase comparator circuitry of the second phase lock loop. The reset input of

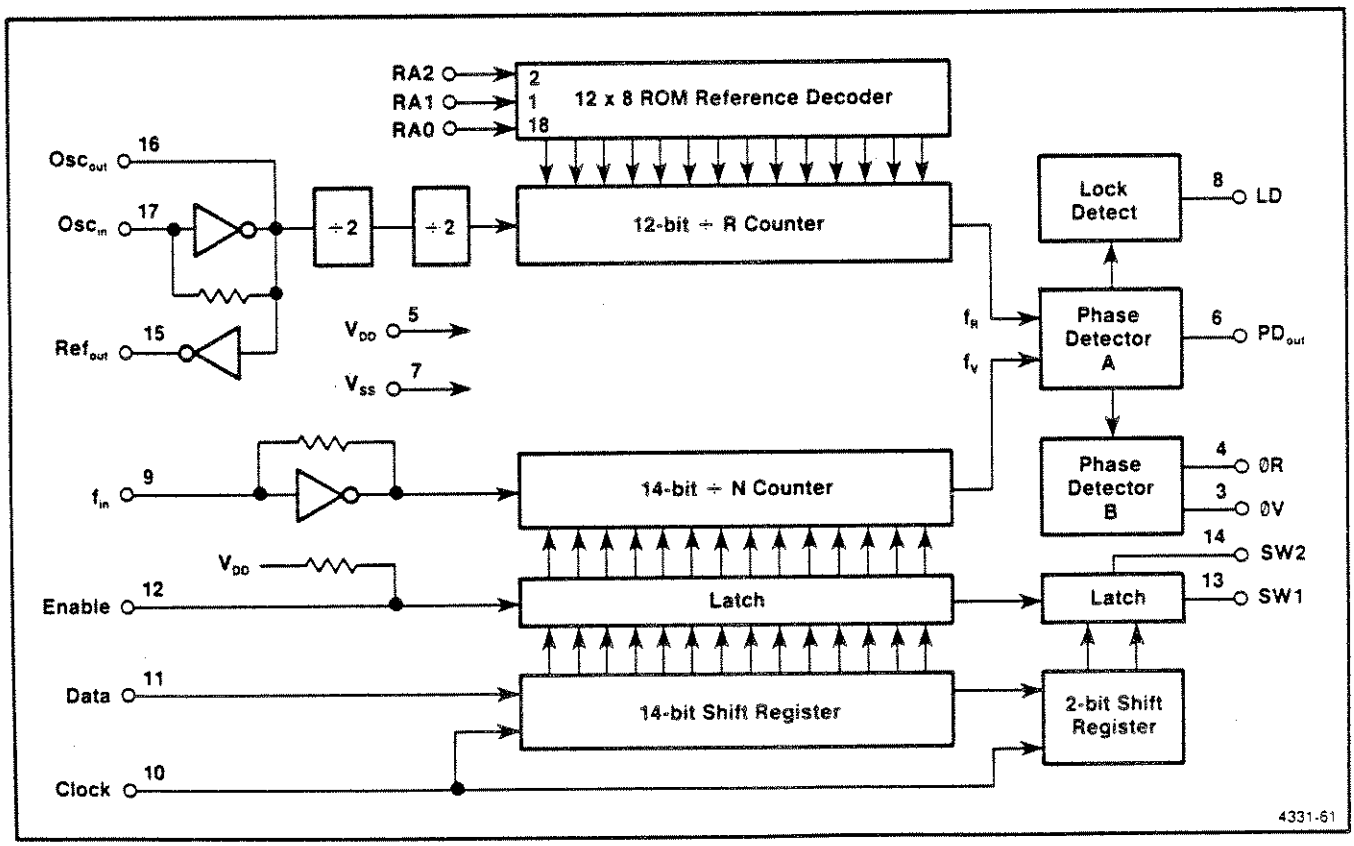


Fig. 4-2. Manufacturers block diagram.

this flipflop is connected to the CPU, enabling the second phase lock loop to be shut down under microprocessor control.

The output of the first phase lock loop is divided down and used as the reference in the second phase lock loop. U5071B and U6091 form the reference divider chain for the second phase lock loop. U5071B divides the VCO by 5, providing a signal that is always 100 times the mantissa of the frequency word. This is available on TP6101 for use in verifying the operation of the first phase lock loop. When connected to a counter it should read the same as the programmed frequency, ignoring the decimal point and exponents. U6091 divides this frequency by powers of ten to produce a square wave at the same frequency as the programmed frequency. The divider ratio is selected by the logic levels on pins 1 and 2 as shown in Table 4-1.

Table 4-1
Divider Select Inputs

Select 2 (pin 2)	Select 1 (pin 1)	Output Division
0	0	10,000
0	1	1,000
1	0	100
1	1	10

The output of this divider chain is fed to a discrete phase detector consisting of dual flipflop U5121, quad nand gate U5111 and diodes CR5101 and CR5103. The other input of this phase detector is a ground referenced version of the main oscillator output. The two inputs are the clock inputs of the dual flipflop. When one input has a rising edge, a high is clocked into the respective flipflop output. When both outputs are high, the output of nand gate U5111A goes low causing the output of nand gate U5111D to go high, resetting the flipflops. If the reference has a positive clock edge first, the Q outputs of U5121A and U5121B will both be low, causing a net negative output from the phase detector. If the two rising edges are in phase, the output of the phase detector will not go high or low (the diodes will always be reverse biased). U5111C acts as a lock detector by comparing the two $\overline{Q}$ outputs of the dual flipflop. If the input signals are always in phase (the loop is locked), the two $\overline{Q}$ outputs are always high. The output of U5111C will then be low, indicating a locked loop.

U6121, U5131, and associated resistors and capacitors form the loop filter for the second phase lock loop. Its function is to smooth the pulses from the phase detector into a dc voltage which will fine tune the main oscillator to the correct frequency. The CMOS switch U5131 changes the time constants of the filter to optimize the stability, frequency settling time, and distortion of the overall loop. Because of the wide frequency range (10 Hz to 163 kHz) of the second loop, the time constants of the filter are changed every half decade as shown in Table 4-2. The three control bits to run the CMOS switch come from the exponent bits of the frequency word and the output of U6061B. CR6123, CR6125, and R6125 clamp the free end of C5141 providing a two pole system response for large perturbations to the loop. VR6161 provides level shifting to optimize the useful range of the operational amplifier output. Q5161 and Q4161 linearize the voltage-to-frequency characteristics of the main oscillator fine tuning. The TUNE- signal is connected to the anode end of an LED in an optically isolated photoresistor fine-tune circuit in the main oscillator. As more current flows through the LED, the frequency of the oscillator goes up. This corresponds to a more negative voltage at the output of U6121A. As the output of U6121A goes more positive, the oscillator frequency goes down.

Table 4-2
Loop Filter Selection

FREQUENCY RANGE*	SELECT BITS (U5131) Pin 9	Pin 10	Pin 11	U5131 FILTER NETWORK (Pin Number)
10 Hz—40 Hz	L	L	L	13
40 Hz—163.8 Hz	L	L	H	14
163.9 Hz—400 Hz	L	H	L	15
400 Hz—1.638 kHz	L	H	H	12
1.639 kHz—4 kHz	H	L	L	1
4 kHz—16.38 kHz	H	L	H	5
16.39 kHz—40 kHz	H	H	L	2
40 kHz—163.8 kHz	H	H	H	4

*40 Hz, 400 Hz, 4 kHz, and 40 kHz switch frequencies are approximate. The exact point will vary with VCO tuning characteristics and has a tolerance of 25%.

When a new frequency is programmed or when the first phase lock loop becomes unlocked, the flipflop U5091A is set. This shuts down the phase detector and resets the reference divider of the second loop. At the next positive edge of the oscillator clock, the reset will be released, causing the reference divider and the oscillator to start in phase. Any phase error at the end of the cycle will be due only to a frequency difference between the two and will not depend on the initial conditions of the circuitry. This substantially reduces the settling time of the loop at very low frequencies.

Main Oscillator ◈8◈ A14

The main oscillator is a state-variable type, using three operational amplifiers. Two amplifiers are used as integrators while the third is used as an inverter. When the overall loop gain of this circuit is unity, the loop will oscillate. The frequency of this oscillation will be the frequency at which the gain through both integrators and the inverter add up to unity. This is determined by the resistors and capacitors around the integrator operational amplifiers and the input and feedback resistors around the inverter operational amplifier. The integrator components are tuned by JFET switches switching binarily weighted resistors and decade weighted capacitors. The fine frequency adjustment is accomplished by varying the input resistor of the inverter while the initial frequency setting is done by adjusting the feedback resistor of the inverter. Switching of all resistors and capacitors is done in pairs (with two exceptions) to maintain balanced levels in the integrators.

Both the phase lock loop board and the main oscillator receive the same frequency information from the CPU. This consists of a 16-bit serial word having a 14-bit mantissa and a 2-bit exponent. The 14-bit mantissa has a maximum value of 16,383. This is used directly as the full scale value in each frequency band. The 2-bit exponent selects one of the following decade bands:10 to 163.80 Hz, 163.9 Hz to 1.6380 kHz, 1.639 kHz to 16.380 kHz, and 16.39 kHz to 163.80 kHz. All bands represent a 10 to 1 range in frequency except the bottom band which ranges 16 to 1. Each binary value in the mantissa corresponds directly to the displayed frequency of the instrument. The diagram in Fig. 4-1 shows the bit order and gives a few examples.

The two shift registers U8081 and U8071 convert the 16-bit serial word to a parallel word. These shift registers, like all shift registers in the floating portion of the instrument, operate on −15 V and ground. This makes direct connection to the JFET switches possible, significantly reducing the circuitry. The two most significant bits, the decade exponent, are decoded by U8061C, U8061E and U8061F into the format necessary to drive the JFET switches selecting the capacitors. As with the shift registers, this gate package operates from −15 V and ground. When both bits are low (the 10 Hz to 163 Hz band) the outputs of all three gates are high (0 V), causing all three pairs of capacitors to be switched in. The JFETs which do the switching need to be very low resistance for low distortion operation, so two devices are used in parallel. When the least significant decade bit is high (the 163 Hz to 1.63 kHz frequency band), the output of U8061C goes low, taking the 0.5 μF capacitor out of the circuit. Resistors R2081, R3081, and R4081 precharge the capacitors to the correct potential to start the oscillator when they are switched in again. When the most significant bit is high (the 1.63 Hz to 16.3 kHz band), the outputs of both U8061E and U8061C are low, causing both the 0.5 μF and 0.05 μF capacitors to be switched out of the circuit. If both bits are high (the 16.3 kHz to 163 kHz band), the outputs of all three gates are low, removing all three capacitors from the circuit.

Frequency selection within a decade band is done by switching resistors in parallel, raising the frequency as more resistors are switched in. The MSB of the mantissa is 5 kΩ, including the JFET resistance. This corresponds to 8192 counts in the mantissa, meaning that at a frequency of 81.92 Hz only this bit will be high. The next most significant bit is 10 kΩ corresponding to a count of 4096. The third bit is 20 kΩ resulting in a value of 2048 counts, etc. When more than one bit is on, the counts add linearly to produce the final frequency value. All resistors are switched in pairs of binarily increasing value except the last two. The imbalance in levels caused by adjusting only one integrator is insignificant for these very small bits. Only twelve of the fourteen mantissa bits are used for oscillator tuning. The last two are accomplished through the phase lock loop circuitry. The resistor and capacitor tolerances as well as component drift are also taken up by the phase lock loop.

U4121 and associated resistors form the inverter stage. At nominal tuning, this stage has a gain of approximately 2.1. This results in 4.2 Vrms at the operational amplifier output for an oscillator output of 2.0 Vrms. Fine tuning of the oscillator by the phase lock loop is accomplished by adjustment of the gain of this stage using U1121. Driving more current through the LED of the opto-isolator decreases the resistance of the opto-isolator, raising the gain and the frequency. When the current decreases through the LED, the opto-isolator resistance goes up, lowering the gain and decreasing the frequency of the oscillator. The resistors around the opto-isolator decrease its tuning range to ±2%, and reduce the sensitivity of oscillator amplitude to changes in the opto-isolator.

The non-ideal characteristics of operational amplifiers and capacitors make the oscillator level inherently unstable and unpredictable. It is therefore necessary to provide some means of stabilizing the oscillator amplitude. This may be accomplished by providing a slight amount of the 90° phase sine wave signal to the integrator stage and regulating the amplitude and polarity of this feedback to keep the oscillator amplitude at the correct value. This feedback path is provided by R2123, R2125, and R4117. JFET Q5121 normally provides control of the amount of this feedback by acting as a voltage variable resistor working against R4117. The leveler circuit of diagram 9 produces the control signal for this JFET by looking at the oscillator output and comparing it to

a reference. When the gate of the JFET is pulled to ground the FET turns on and increases the oscillator amplitude. Driving the gate with a negative voltage will decrease the oscillator amplitude. Once the correct oscillator level is established, the JFET will be driven to a resistance that maintains this amplitude constant. For large changes in oscillator level, there is another pair of FETs (Q3121 and Q5123) which are used as switches to drastically change the amount of feedback and rapidly bring the oscillator close to the correct level. These FETs are fed from another control signal called SPEED-UP.

Q2051, Q2053 and associated components provide a clamp circuit to prevent the output from ever increasing more then one dB above the correct level before it is clamped. This improves amplitude leveling time and prevents the device under test from seeing too great an amplitude. R5082 provides bias current compensation for U5091 since the leveling circuit is sensitive to the changing dc offsets it would otherwise produce. R3121 allows adjustment for initial capacitor set nominal value. Although they are matched very closely, they do not have a very tight initial tolerance.

Leveler ◇9◇ A14

The leveler circuit has the job of maintaining the oscillator amplitude constant at 2 V, independent of changes in frequency and component value. It looks at the amplitude of the oscillator output and adjusts the gain of the 90° feedback to maintain the amplitude constant. The leveler has two paths, a high accuracy medium speed path which establishes exactly 2 V and a fast leveling path to quickly restore proper amplitude when severe transients occur such as changing decade capacitors.

The two integrators in the state variable oscillator provide sine waves which are 90° out of phase. If the output of the oscillator is taken as the 0° reference, the signal labeled "90°" leads this sine wave by one quarter cycle. When the oscillator output is at a positive peak, the 90° signal will be crossing zero in the negative direction. At negative peaks, the reverse is true. These two signals are both used in the leveler to provide information about the amplitude of the oscillation at any given time.

The high accuracy leveler path uses a sample and hold circuit to measure the peak amplitude of the sine wave and maintain this at 2.828 V. The 90° signal is fed to a comparator (U2171A) which senses its zero crossings. As the signal goes below zero, the output of U2171A goes high. Buffering and inversion is provided by U2181B which, in turn, drives a sample and hold IC U1151, placing it in the hold mode. Since the oscillator output is now at a positive peak, the sample and hold output is a voltage which can be used as a measure of the sine wave amplitude. This output is sampled by another IC U1141 which provides a long hold-time capability and eliminates ripple at its output when the first IC goes into the sample mode again. U2181A, R2173, C1173, and CR2173 form a one shot which places the second sample and hold in the sample mode for only a short time during the hold time of the first sample and hold.

The sample and hold output is now a dc voltage equal to the peak value of the previous cycle of the sine wave. This voltage is compared against a reference derived from the negative supply in integrator U5131A. When the oscillator output is greater than 2.828 V, the operational amplifier output will go more negative. When the output is too small, the operational amplifier will go more positive. The resulting voltage drives the level control FET Q5121 in the main oscillator. This serves to maintain the oscillator amplitude at the correct value. This voltage is available at TP5111 and should be twice (approximately −6 V) the pinch-off voltage of the FET when the oscillator is leveled.

RT1141, R3141, and R1135 provide compensation for bias current in U1141-6. Q2150 and R2150 provide filtering of the sample and hold signal below 1.63 kHz to reduce the effects of noise on the output amplitude. Q3141 and Q4133 change the time constants of integrator U5131A to optimize the settling time of the circuit at different frequencies.

Quad-comparator U5151 and associated components provide fast amplitude information to the speedup circuit FETs Q3121 and Q5123. At any instant in the cycle of a correctly leveled oscillator, the amplitude of at least one of the two signal phases will be within 0.707 of the peak amplitude. By comparing these two signals against both positive and negative references slightly less than 0.707 times the 2.828 V peak value (1.9 V) we can detect if the amplitude is low. The outputs of these four open collector comparators are "wire-ANDed" together to provide a signal which goes low if at least one phase is at a sufficient amplitude. If all four phases are low in amplitude, this signal goes high, turning on the speedup FETs and very quickly raising the level to the correct value. R3157 and C3151 provide filtering of this output to reduce high frequency distortion from power supply noise. Since the normal operating voltage at the output of U5091 (the 90° signal) is 1.43 (the square root of the inverter gain) times higher than the 0° amplitude, R3177 and R4171 attenuate the signal down to the same amplitude.

IM Oscillator and CCIF/SMPTE Circuits ◇10◇ A14

The IM oscillator is a simplified version of the main oscillator. It is a state-variable design with only eight discrete frequency selections. U7011B and U7051A are the two integrator operational amplifiers, while U7011A is the inverter operational amplifier. Only resistors are switched to affect selection between the eight frequencies. The eight frequencies are decoded from a 3-bit binary word as shown in the table on diagram 10. The inverter stage operates with a nominal gain of unity making all levels within the loop the same. Initial calibration of frequency is accomplished by adjusting the gain of the inverter stage.

Frequency selection is achieved by decoding two of the three frequency bits to four frequency states and using the last bit to shift these by a factor of two. All JFETs are selected in pairs, maintaining balance between the integrators. With all frequency control bits low (−15 V) all JFETs are off. This sets the oscillator to 80 Hz. When the LSB F0 is high, Q8023 and Q9041 turn on, reducing the tuning resistors and raising the frequency to 100 Hz. When only bit F1 is high (0 V), Q8021 and Q8031 turn on raising the frequency to 125 Hz. Driving both bits high turns on not only the two pairs of JFETs described above, but through CR9033, CR9031, and R9031 turns on Q9021 and Q9043. This switches in three pairs of resistors in parallel, raising the frequency to 500 Hz. The third frequency control bit operates Q7021 and Q7031, lowering each of the frequencies by a factor of two by attenuating the input to the tuning resistors by a factor of two. Resistors R8021 and R9059 compensate for the source resistance of the resistor divider network. R8023 and R9057 adjust the frequency ratio in the 125-60 Hz selection to be slightly off of 2 to 1.

The leveling circuit for the IM oscillator rectifies the output signal with CR6023. This current is compared against a reference developed by R6031 in the integrator Q6033. The output of this stage adjusts a peak detector formed by Q6031, C7031, and C5023. Signal peaks are captured and used as a fast indication of oscillator amplitude but the dc path formed by the rectifier and integrator supplies the high accuracy leveling. Resistor R6021 provides a ripple current cancelation to reduce distortion generated by ripple on the leveling FET (Q5011) gate voltage. Operation of this JFET is identical to Q5121 in the main oscillator.

A −15 V/0 V sync signal is generated by Q7051 and Q7151. They compare the inverter output to ground, supplying a sync signal in phase with the oscillator output.

CCIF signals are generated by multiplying the main oscillator output by the IM oscillator output. The output of the multiplier is then filtered to remove any residual low frequency energy which would show up as CCIF difference tone distortion. The heart of the multiplier is a dual JFET which is used as a voltage variable resistor. The IM oscillator signal is applied through R4045 to the drains of the two FETs. This attenuates the amplitude down to approximately 100 mV to maintain linear operation of the FETs. The sources of the FETs are connected to the summing junctions of two operational amplifiers (U4011 and U3041) wired to difference the currents coming out of the FETs. When no signal is applied to the gates, the currents from the FETs cancel, giving no output. Adjustment of the gain through U3041 is accomplished by R4033 allowing for slight mismatch of FET characteristics. The main oscillator signal is applied differentially to the gates of the FETs by U4051. This gives a balanced modulator effect, canceling even order nonlinearities in the process. Gain of the entire multiplier is adjusted by R4031 and compensates mainly for variations in the pinch-off voltage of the JFETs. When the CCIF signal is not selected, Q4023 shorts it out to prevent interference with other modes of the generator. The output signal from the multiplier is amplified and filtered by a six-pole quasi-elliptic highpass filter. This has a cutoff frequency of 2 kHz with a notch in its response at 500 Hz. Resistors R2011, R3011, R3031, and R3033 provide the gain while R2021 introduces the 500 Hz notch.

External Input/Output Selector ◇11◇ A14

U8091 is an 8-bit shift register which accepts a serial word from the CPU and latches it to supply control signals for the IM oscillator, burst circuits, and output selector. The three least significant bits of the register output are routed to the IM oscillator for frequency control. The next two bits are used to control the burst generator and enable the various modes. The three most significant bits of the word are used to select the desired output waveform. Table 4-3 gives the bit patterns for the eight output functions. These three bits drive a one of eight decoder U8181, which enables and disables the various circuitry for the generation of each signal. This IC is a CMOS analog switch whose input is tied to −15 V and whose outputs are all pulled high (0 V) by resistors. As each function is selected, the corresponding output is pulled low and the others are pulled high.

Table 4-3
Function Selection

FUNCTION	U8091 OUTPUTS (Pin)13	12	11	U8111 INPUT (Pin No.)	U8181 OUTPUT (Pin No.)
SINE	L	L	L	4	13
SQUARE	H	L	L	12	1
SMPTE 4:1	L	L	H	5	14
SMPTE 1:1	L	H	H	7	12
CCIF	L	H	L	6	15
BURST 0	H	H	L	10	6
BURST 10	H	L	H	11	5
EXTERNAL	H	H	H	9	4

These three bits are also used to control two analog switches U8111 and U8171 which select the signal output and sync output respectively. The sync output selector U8171 is a CMOS selector which also runs on −15 V and ground. Its inputs are the sync signals SIN2, IM SYNC, SQR SYNC, and BURST SYNC generated by their respective circuits. There is no EXTERNAL sync. These three bits are also level-shifted to interface to JFETs Q8101 and Q9101. These are driven from transistors Q8122 and Q8102 respectively. The $\overline{\text{CCIF}}$ signal is also needed in the CCIF multiplier, so it is buffered by U8061A and U8061D to prevent interaction.

The SMPTE/DIN signals are generated by mixing resistors R7065, R7067, and R7069. When the SMPTE/DIN mode is not selected, the signals are shorted out by Q8051.

The EXT INPUT connector on the front panel is connected to J5141 by a two conductor shielded cable. This signal is buffered by a differential input amplifier consisting of U5131B and associated resistors. C5131 and C5133 provide bandwidth limiting. Q6141 and Q6131 short the external input when it is not selected, reducing interference from signals which may be present. The control signal for the FETs goes low when the EXT INPUT is selected.

Square Wave Generator and Burst Circuitry ◇12◇ A14

The 0° sine wave signal is converted to a square wave by comparator U2171B and nand gate U2181C. Positive feedback is added to provide hysteresis. The 0 V/+15 V output of this circuit is level shifted by VR5171 to −15 V/0 V. This is fed to decade divider U9151 and some of the burst circuitry. The buffer output of the divider (non-divided) drives the remaining portions of the burst circuits, the phase lock loop, and the sync output.

The divided output of U9151, wired as a divide-by-10, is used as the square wave output signal. It is level shifted by R9135 and R9137 to center it about ground. R9133 and R8143 attenuate the square wave to match the peak amplitude of the other waveforms (2.828 V). C8131, R9131, and C9141 limit the risetime of the square wave to prevent slew rate limiting of any succeeding stages. The square wave sync is also derived from the output of the divider.

The burst circuitry is designed to provide up to 65535 cycles of burst **on** and 65535 cycles of burst **off**. The same 16-bit counter is used for both **on** and **off** cycle counting. The CPU sends a 32-bit serial word representing the on and off cycle information. This is stored in shift registers U5171, U5181, U7171, and U7181 which have tri-state outputs. The **on** and **off** cycle registers have their outputs tied together, and the output enable pins are used to select one or the other. The burst counting is done by a pair of 8-bit presettable down counters U7161 and U5161 which are loaded with the appropriate value from the shift registers. When the counters finish a count cycle they pull their $\overline{\text{ZD}}$ (Zero Detect) pin low. Since this is connected to the $\overline{\text{SPE}}$ (Synchronous Preset Enable) pin, the counters load themselves at the next clock edge. The $\overline{\text{ZD}}$ output also drives the J and K inputs of a JK flipflop U8161B wired to toggle on the next clock edge it sees. The outputs of the flipflop drive the OE (Output Enable) pins of the shift registers causing the correct count value to be loaded into the counters for the next count cycle. This creates a burst of **on** cycles or **off** cycles one longer than the count stored in the shift registers. The difference is corrected by the microprocessor when it writes the value into the registers. One output of the flipflop is fed through U7151F to a JFET, Q8121, which gates the burst signal on or off. When the gate is high (0 V) the burst is off, while when it is low (−15 V) the output is on. A resistor divider formed by R9123 and R9121 creates the 10% burst signal while the signal on the drain of Q8121 is the 0% burst. U7151F and C9121 compensate for the charge injection from the gate of Q8121.

When the FL BURST GATE line is low, the circuit works normally. When this line is high the burst signal is truncated, the output is turned off, and the counters are reset to the start of an **on** count. This line is a floating version of the burst gate input on the front panel ORed with a signal from the CPU. Flipflop U8161A insures that this always occurs at the zero crossing of the signal. U7151D, U7151C, and U7151F enable two additional modes of burst operation. When the COUNTED/$\overline{\text{GATED}}$ line and the $\overline{\text{CT INH}}$ (Count Inhibit) are both high (0 V) the circuit works as described above. When the $\overline{\text{CT INH}}$ line is low, the counters are held in the clear condition preventing any counting and maintaining the output on. The FL BURST GATE line may then be used as a gate line without interference from the counters. When the $\overline{\text{CT INH}}$ line is high and the COUNTED/$\overline{\text{GATED}}$ line is low, the counters will be stopped at the end of an **on** count by U7151C. The counters may then be reset to the beginning of an **on** count by pulling the FL BURST GATE line high momentarily. One complete **on** count will then occur before the output is turned off, and the line counters stopped. In this mode, the **on** cycles count will be the same as the value stored in the **on** cycles shift register. The CPU makes the necessary one count adjustment when modes are changed.

Amplitude DAC ◇14◇ A13

In the SINE mode, the amplitude DAC takes the constant 2 Vrms signal (or equivalent peak-to-peak voltage in modes other than SINE) provided by the Oscillator board and changes its amplitude to provide 20 dB of variable amplitude to the output amplifiers. The DAC has two stages; the first stage has a "fine tune" range of 2 to 1 (or 2.5 to 1 in the 2 to 5 ranges), accomplished with ten bits of modified binary steps. The second DAC stage performs a coarser "range switch" at the 1-2-5 amplitude points (front panel reference), or the 2-5-10 amplitude points in the UNBALanced mode. It also performs two additional gain reductions—one to provide 20 dB of attenuation for the lowest output voltage scale

(+0.2 mV to 2 mV, BALanced mode), and the other to redistribute the DAC gain to reduce noise in the lowest 8 dB (BALanced) or 6 dB (UNBALanced) of any 20 dB range (2.005 to 5.000, BALanced). These gain changes are accomplished by using FETs to switch resistors to the summing node of operational amplifiers. When the FET gates are high (0 V), the FETs conduct and connect the resistors at the drain leads to the summing node. The FETs are turned off by −15 V at the gates. In order to reduce high frequency distortion caused by the nonlinear off-capacitance of the FETs, resistors such as R3056A-G are connected to common from some FET drains. In lower impedance branches, the FET drains are connected to common through PNP transistors such as Q4056 to prevent nonlinear feedthrough when the FETs are off. The binary scheme of the DAC is modified in the most significant bits to reduce distortion due to current through the nonlinear FET on-resistance. By splitting the two most significant bits and turning both on to obtain the MSB, the current through any one FET is reduced, reducing the accompanying distortion. The network consisting of C4051, C4061, R4056, and R4059 controls the rise time and slew rate of the square wave signal and also helps determine high frequency amplitude flatness in sine wave mode. Capacitor C4065 reduces distortion above about 50 kHz by feeding a slight amount of the signal around the input stage of U4060. Resistors R4061 and R4062 provide a "ground sense" back to the Oscillator board to reduce common mode signals between the oscillator and the DAC commons. Table 4-4 shows certain "key" voltages at which only one FET is on (high) and should aid in troubleshooting the first stage of the DAC.

At the given SG 5010 voltage setting, check that only the indicated FET is on by measuring its gate voltage. *Hi = 0 V; Lo (or off) = −15 V.*

The second stage of the DAC is U4032 with gain-switching FETs Q3033, Q3044, Q4031, Q4033, Q4042, and Q4043. The latter four FETs change the gain in a 1-2-5 sequence by various parallel combinations. The four PNP transistors on the FET drains serve the same purpose as those in DAC1—they reduce high-frequency distortion caused by nonlinear FET off-capacitance. Q4031 turns on to reduce the gain by 20 dB in the lowest voltage ranges of the SG 5010 (0.2 mV to 2 mV, BALanced), and Q3033 changes the gain distribution by 6 dB (with a concurrent change in input FETs) in the lowest 6 dB (UNBALanced) or 8 dB (BALanced) of each 20 dB voltage range to reduce noise. R4030, R4020, and C4020 help reduce high frequency distortion. This stage is two-pole compensated by C4032, C4031, and R4031 to improve high frequency performance. Table 4-5 shows which DAC2 FETs are on for any desired output voltage and should aid in troubleshooting the DAC2.

The signal from U4032-6 feeds both power amplifiers in the UNBALanced mode, or is inverted by precision inverter U4031 to provide a 180 degree phase-shifted signal to one power amplifier in the BALanced mode. U4031 is feed forward compensated by C4034 and R4032 for best square wave performance. R4028 permits the inverter gain to be precisely set to provide equal amplitude out-of-phase signals at the + and − output connectors (referenced to common).

The data ("amplitude word") that programs the DAC comes from the CPU by way of the Oscillator board. This 16-bit word is shifted into registers U4041 and U3061 which store it to control the DAC FETs. The data logic is high = 0 V, low = −15 V.

OUTPUT AMPLIFIERS ◇15◇ A13

Since the two output amplifiers shown on diagram 15 are identical, only the top amplifier in the drawing will be discussed. The only difference between the amplifiers is that the lower amplifier has its input switched between U4032 (BAL) or the inverter U4031 (UNBAL) by K3031-S1. The two amplifiers are driven in phase and connected in parallel after the attenuators for UNBALanced operation (the − output is switched to common), or they are driven 180° out of phase (U4031 provides the phase inversion) and feed the + and − OUTPUT connectors respectively, in BALanced mode. This connection provides twice the output voltage between + and − OUTPUT connectors (with common half-way between the outputs but able to float above chassis ground) because the one amplifier swings positive to "+V" volts peak, the other amplifier swings negative to "−V" volts peak.

The amplifier consists of a differential input stage followed by a voltage gain stage and then a high-current output stage. This topology is very similar to high-quality audio power amplifiers. The differential input stage is formed by Q3031 and Q2036. Resistor R3033 supplies about 1 mA of emitter current to the differential pair which split it equally under quiescent conditions. A current mirror image consisting of diode-connected Q3032 and Q2037 is the load for the differential amplifier. The output of this first stage is buffered by emitter follower Q2034 and fed to voltage gain stage Q2035. Diodes CR3031 and CR2031 control the clipping characteristics of the amplifier by preventing saturation of individual stages. The voltage gain transistor Q2035 has a very small emitter resistor (R2037) but its load is the current source consisting of Q2033 and R2033, so its gain is very high. Q2033 and R2033 form a quasi-current source because Q2033's Vbe is relatively constant with signal, so the current through R2033 is relatively constant. Q2033 also serves as an emitter-follower buffer to the output transistors, as does Q2038. The emitter resistors of these followers are split. Boot-strap capacitors C2032 and C1031 are connected from the split points to the amplifier output to increase signal swing capability. The output stage consists of two parallel-connected transistors from each buffer (one pair for each signal polarity) with separate emitter degeneration resistors to force equal current sharing. The output transistors are Q2031 in parallel with Q1031, and Q1032 in parallel with Q2032. C2022 increases the collector to base capacitance of the NPN transistors to match that of the somewhat slower PNP's, creating a symmetrical load on the

Table 4-4
FINE AMPLITUDE DAC TROUBLESHOOTING
Hi = 0 V, Lo = -15 V

Ampl. Word Bit #	[a]U4041 Pin #	[a]U3061 Pin #	[a]FET (gate) Q #	SG 5010 Voltage Setting (BAL Mode)
6 LSB	12	—	Q4052	2.005
7	11	—	Q4053	2.010
8	—	4	Q3051	2.020
9	—	5	Q3052	2.040
10	—	6	Q3055	2.080
11	—	7	Q4051	2.160
12	—	14	Q4054	2.320
13	—	13	Q3053	2.640
14	—	12	Q3054	3.280
15 MSB	—	11	Q4055	4.305[b]

[a]Check for approximately 0 V.

[b]Q4055 turns on at this voltage; however other FETs remain on.

Table 4-5
COARSE AMPLITUDE RANGES
Hi = 0 V, Lo = -15 V

			Ampl MODE Word			UNBAL		BAL	
Bit #	U4041 Pin #	FET Q #	1.002-2.000	2.005-5.000	5.010-10.00 (10.60)	2.005-5.000	5.010-10.00	10.02-20.00 (21.2)	OFF (BAL & UNBAL)
			Except 0.2-1.000 mV range			Except 0.2-2.000 mV range			
0	4	Q4031	Lo	Lo	Lo	Lo	Lo	Lo	Hi
1	5	Q3033	Hi	Lo	Lo	Hi	Lo	Lo	Hi
2	6	Q4043	Hi	Lo	Hi	Lo	Lo	Hi	Lo
3	7	Q4033	Lo	Lo	Hi	Lo	Lo	Hi	Lo
4	14	Q3044	Lo	Hi	Hi	Hi	Hi	Hi	Lo
5	13	Q4042	Lo	Hi	Hi	Hi	Hi	Hi	Lo
		(mV) (mV)	0.1-0.2	0.200-0.500	0.501-1.000	0.200-0.500	0.501-1.000	1.002-2.000	
0	4	Q4031	NA	Hi	Hi	Hi	Hi	Hi	
1	5	Q3033	NA	Lo	Lo	Lo	Lo	Lo	
2	6	Q4043	NA	Lo	Hi	Lo	Lo	Hi	
3	7	Q4033	NA	Lo	Hi	Lo	Lo	Hi	
4	14	Q3044	NA	Hi	Hi	Lo	Hi	Hi	
5	13	Q4042	NA	Hi	Hi	Hi	Hi	Hi	

buffers for improved high frequency distortion. Diodes CR1033 and CR1034 act against the voltage drop across the emitter ballast resistors to provide output current limiting for the amplifier. When the voltage across the 4.7 Ω resistors exceeds two diode drops, these diodes turn on and divert base current from the drivers. Resistor R2032 sets the voltage difference between the bases of the driver transistors, thereby establishing the quiescent current in the output stage. Any dc offset appearing at the amplifier output is integrated by servo-amplifier U3031B and associated components, which drives the base of Q2036 to reduce output offset to 0 ±10 mV. Capacitor C2033 provides dominant pole compensation for the amplifier while C3041 and R3040 provide feed forward compensation for best square wave response. Diodes CR1031 and CR1032 protect the amplifier from signals sourced back into the SG 5010 output connectors. The gain of the amplifier is fixed at 2.57 by R3034 and R3036. TP1012 (TP1011 for the other amplifier) provides a convenient point at which to test amplifier operation (before any relays or output attenuation). Operational amplifier U3031A monitors the summing node of the output amplifier to provide an indication of clipping or overload. Threshold detectors U3032A-D detect when the summing node moves away from 0 V and inform the CPU via optoisolator U1022 and the $\overline{\text{OVLD}}$ line (J1051-19). This line is normally high (+5 V) and goes low (about chassis ground) when overload occurs.

OUTPUT ATTENUATORS AND SWITCHING 

The amplifier outputs as measured at TP1012 or TP1011 are designed to run between 1 Vrms and 10 Vrms (2 to 20 Vrms into a balanced load). Full +28 dBm output (21.2 V, open-circuit, BAL) is generated by programming the DAC to maximum gain. To obtain lower output voltages, attenuators having 20 dB per step (R2011 and R2012) and an impedance of 25 Ω are used to divide the output voltage to lower levels. Relays K1021, K1013, and K3012 select progressively lower voltage taps on the attenuators. (The lowest 20 dB voltage range is provided in the second stage of the DAC, as discussed earlier.) For the highest output voltages (2 V to 21.2 Vrms), relay K1011 switches the amplifier outputs to fixed 25 Ω resistors and removes the rest of the attenuator networks to minimize loading. These resistors (or the attenuator impedance) provide the 50 Ω source resistance of the SG 5010. This resistance can be increased to 150 Ω or 600 Ω by switching in additional series resistance contained in the attenuator hybrids. K3011, when open, inserts an additional 275 Ω in each attenuator, which, when added to the 25 Ω attenuator impedance, gives 300 Ω per side, balanced (600 Ω total). Relay K4011 closes to put 61.11 Ω in parallel with this 275 Ω resistor, giving 50 Ω plus 25 Ω, or 75 Ω per side (150 Ω total balanced R).

In the UNBALanced mode, K3031 connects the outputs of the two amplifiers together after the attenuators, making twice the current available to the load. The second section of K3031 bypasses the precision inverter so the amplifiers have in-phase signals. To keep the source resistance constant, R3011 is inserted to raise the 12.5 Ω resistance of the paralleled attenuators back to approximately 50 Ω, and both sections of additional output resistors are used in series. K2021 accomplishes the switching necessary to connect these "build-out" resistors in series and connects the − OUTPUT connector to common. Thus, it is not necessary to move the output connectors and cable when the operator desires an UNBALanced connection. When the GND button is activated, K4021 connects the floating common to chassis ground through lamp DS4021. This lamp, which has 25 Ω to 30 Ω of resistance when cold, provides protection in case the GND button is pushed while the common is connected to an external voltage. The lamp limits the current flowing between the external voltage and chassis ground and, under extreme conditions, acts as a fuse to prevent damage to the external circuitry.

Attenuator and Switching Register and Drivers 

The data word ("attenuator word") which programs the attenuator and output switching comes from the CPU via P1040. U2022 stores this data on the Output board and uses it to turn the appropriate relays on or off. The attenuator word and the relay power are chassis-referenced +5 V. The relay drivers, shown on diagram 13, are sections of a transistor array, Q2020A-F, which buffer the CMOS output of U2022, followed by higher-current transistors such as Q1011. The format of the attenuator word is given in Table 4-6.

Temperature compensated zener diode VR4060 provides a stable reference for the supplies. The +17 V rail is divided down by R4060, R4083, and R4082 and the resultant is compared to the 6.2 V reference voltage. U1060B amplifies any error and drives the base of series-pass transistor Q106 to reduce the error. For example, if the output voltage exceeds the desired value, U1060-5 is more positive than U1060-6. Then U1060-7 increases in voltage, reducing the Vbe of Q106 and causing more voltage to be dropped across the collector to emitter of Q106. This action reduces the output voltage of the supply. FET Q1061 supplies about 5 mA to guarantee that Q106 always turns on and the supply always "starts up". Diodes CR1071 and CR1072 establish the threshold for supply current limiting. As the load current increases, the voltage drop across the parallel combination of R1056 and R1060 increases. When this drop plus the Vbe of Q106 equals two diode drops (approximately 0.7 V across the resistors), the two diodes turn on, and, acting against R1062, take base drive from Q106, limiting the supply current to about 350 mA. The output voltage reduces to keep the output current at the limit value.

The operation of the −17 V supply is identical to that of the +17 V supply except that it is referenced to +17 V. This is because its output is added to the +17 V supply via R1054 and R1055 before being compared to 0 V. U1060A is the error amplifier and Q107 is the series-pass device for the −17 V supply. The ±17 V supplies power the dual output amplifiers to allow outputs of +28 dBm into 600 Ω from 50 Ω.

Table 4-6
Attenuator Word Format

MSB U2022-	11	12	13	14	7	6	5	4	LSB
Driver		Q1011	Q1021	Q2011	Q2012	Q3011, Q3012	Q4011	Q3014	Q3013
Function		Atten. top tap	Atten. 2nd tap	Atten. 3rd tap	Atten. bottom tap	BAL/UNBAL	GND/FLT	50 Ω	150 Ω
BAL V or logic 1		2.005-21.2	200.5 mV-2.000 V	20.05-200.0 mV	2.005-20.00 mV	1=UNBAL	1=GND	1=50 Ω	1=150 Ω
		Logic 1 = Hi (≈5 volts)							

±15 V Power Supplies (16)

The +17 V is converted to +15 V by R4080, R4070, Q4071, and Q4081. The resistors divide the voltage down, and Q4081 (a high-gain transistor) buffers the voltage to the base of Q4071. The Vbe drops and the associated temperature coefficients of the two transistors approximately cancel, and the current through the collector of Q4081 returns to the +15 V line. Resistor R4073 supplies part of the base current for Q4071, guaranteeing start up. Operation of the −15 V supply is identical to the +15 V supply operation, using transistors Q1080 and Q4070.

Zener diodes VR3022 and VR3021 provide over-voltage protection by turning on if either 15 V supply exceeds 18 V. In this case, the zeners place the 15 V and 17 V supplies into current limit to keep the 15 V supplies below 18 V, and their high power rating enables them to maintain this condition indefinitely. Note that if the +17 V or +15 V supplies are current limited so that the +17 V is reduced in amplitude, then the −17 V and −15 V supplies track this reduction. However, current-limiting the −17 V and −15 V supplies does not cause the +17 V and +15 V supplies to track the reduction in the −17 V and −15 V supplies.

Capacitors C4031 and C4041, located at the output terminals, help prevent any RF that may be picked up by long cables connected to the output terminals from interfering with the SG 5010 operation. VR4051 eliminate any undesired effects (such as false programming) by static discharges to common or the output cables.

Also shown on diagram 13 are the buffers for the opto-isolators which convert the chassis-referenced 5 V digital lines from the CPU to floating common-referenced 15 V digital signals. The floating data lines are distinguished from the ground-referenced data lines (from which they are derived) by adding "FL" to their names; e.g., AMP CLK becomes FL AMP CLK. Transistors Q2062 and Q2063, used to drive the LED section of the opto-isolators for the phase lock drive and sync drive, are also shown on diagram 13. A power supply sense circuit consisting of Q2021 and VR3023 signals the CPU when the sum of the two 15 V supplies drops below approximately 24 V. This indicates that one or both of the supplies is in current limit or that a failure has occurred in the power supply or fuse. Q2021 then turns off, causing opto-isolator U2046 on diagram 4 (CPU board) to interrupt the CPU which puts an error message in the display and on the GPIB.

±17 V Power Supplies (13)

Power in the form of 25 Vac from the power module connects to the primary of transformer T300 (mounted on the bulkhead) through P1023 and fuses F2020 and F2022 on the CPU board. The two secondaries of T300 are each fullwave bridge- rectified and filtered by 1000 μF capacitors C1070 and C1071. The transformer has separate internal shields for the primary (chassis-referenced) and the secondaries (common-referenced) to help reduce power-line noise coupling to the SG 5010 floating ground or common. Capacitors C1072 and C1080 prevent high frequency interference caused by commutation of the bridge rectifier diodes.

The regulator scheme used on the + and −17 V supplies is a series-pass type with the regulator in the common path rather than the supply path. This scheme permits higher open loop gain for improved ripple reduction and maintains low output impedance up to relatively high frequencies.

PERFORMANCE CHECK

Introduction

This procedure checks the electrical performance requirements as listed in the Specifications section of this manual and may used in an incoming inspection facility to determine acceptability of performance. If the instrument fails to meet the requirements given in this Performance Check section, the Adjustments Procedure section should be performed. Refer to the Parts Location Grid in the pull-out pages for the following Checks and Procedures. This procedure can be performed at any ambient temperature between 0°C to 50°C.

Performance Check Interval

The performance check should be performed at the following intervals:

- At incoming inspection
- After 2000 hours of operation or every 12 months, if used infrequently.
- After repair or accidental abuse.

Services Available

Tektronix, Inc. provides complete instrument repair facilities at local field service centers and at the factory service center. Contact your local Tektronix Field Office or representative for more information.

Test Equipment Required

The test equipment, or equivalent (except as noted) listed in Table 4-1 is suggested to perform the Performance Check and the Adjustment Procedure in this manual.

LIST OF TEST EQUIPMENT REQUIREMENTS

Description	Minimum Requirements	Perf Chk	Adj Chk	Example
TM 500 Series Power Module	3 compartments			TEKTRONIX TM 503
TM 5000 Series Power Module	6 compartments			TEKTRONIX TM 5006
Digital Freq Counter	0.001% Accuracy; 0.0001 Hz Resol at 10 Hz; 0.01 Hz Resol at 160 kHz			TEKTRONIX DC 509
Wide Band Rms Voltmeter	0.5% from 10 Hz to 160 kHz			Hewlett Packard 3403C True Rms Voltmeter or Fluke 8502 (Opt. 09A)[a]
Distortation Analyzer	10 Hz to 100 kHz, THD 0.0032%; both SMPTE/DIN and CCIF Distortion Meas. Capability			TEKTRONIX AA 5001 (no equivalent)
Oscilloscope System				TEKTRONIX 7704A
Vertical	Dual Channel			TEKTRONIX 7A18
Time Base				TEKTRONIX 7B80
Spectrum Anal.	20 Hz-1 MHz; 10 Hz resol; 80 dB dynamic range			TEKTRONIX 7L5/L3
Gen. Purpose Digital Multimeter	0.2%, DC Volts 0.2%, Ohms			TEKTRONIX DM 501A
Low Dist. Sineware Generator	20 Hz to 20 kHz, THD 0.0010%			TEKTRONIX SG 505
Controller	GPIB Compatible			TEKTRONIX 4052A or 4041
Notch Filter Cal Fixture				Tektronix 067-0938-00
Load Resistor	600 Ω, 1%, 3W (two 300 Ω, 1%, 3W, in series)			Tektronix Part No. 308-0299-00 (2)
Bnc T Adaptor (2)				Tektronix Part No. 103-0030-00
Coaxial Cables (2)	50 Ω, Precision 36"			Tektronix Part No. 012-0482-00
Coaxial Cables (4)	50 Ω, 18"			Tektronix Part No. 012-0076-00

[a]Note specified accuracy of Fluke 8502-09A is 1.0% at 10 Hz and 100 kHz and 2.0% at 160 kHz. Calibration should be verified before checking SG 5010.

PERFORMANCE CHECK PROCEDURES

1. Check Basic Functional Operation and Sync Output

Connect equipment as shown in Fig. 5-1. Check setup 1.

SG 5010 CONTROL SETTINGS

FUNCTION	SINE
Vrms	1.000
FREQ	5.000 kHz
R SOURCE	50 ohms
GND-FLTG	FLTG
BAL-UNBAL	UNBAL
ON-OFF	ON

OSCILLOSCOPE SETTINGS

Vertical Mode	Left
Horizontal Mode	B
B Trig Source	Left

VERTICAL PLUG-IN SETTINGS

Display Mode	ALT
Trigger Source	CH 2

a. Turn on the TM 5006 and TM 503 power.

b. Turn on the oscilloscope.

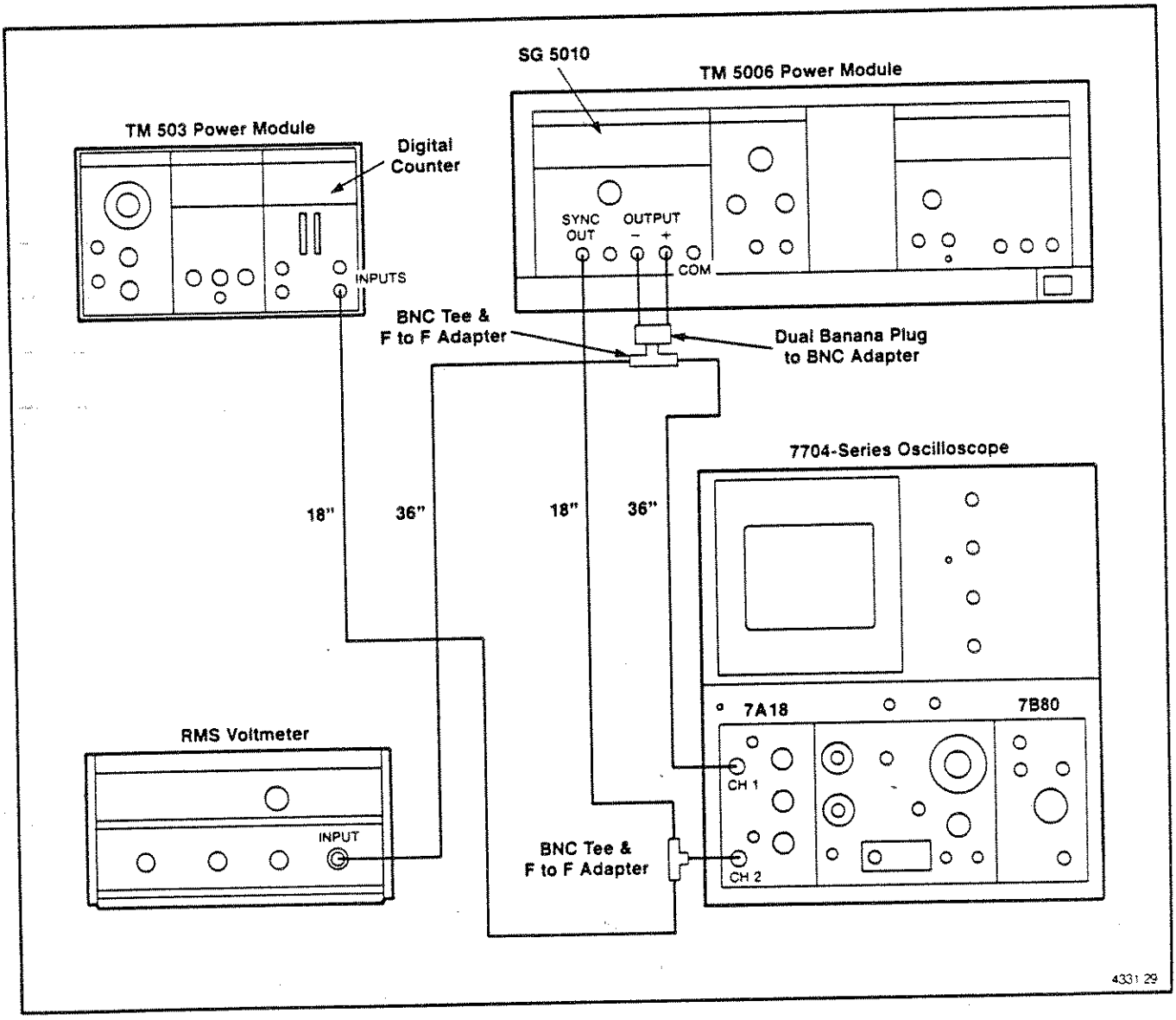


Fig. 5-1. SG 5010 check setup 1.

c. Observe the SG 5010 Main output and Sync output signals (make certain the trigger source is derived from the SG 5010 Sync output signal). Adjust oscilloscope triggering for a stable display.

d. CHECK—that the Sync output signal is a 5 kHz squarewave with the same frequency and polarity as the Main output signal.

e. Set the SG 5010 FUNCTION button to SQUARE.

f. CHECK—for Sync output signal as shown in step e.

g. Change the SG 5010 FUNCTION to SMPTE/DIN and the IM FREQ to 100 Hz.

h. CHECK—that the SG 5010 Sync Output signal is approximately 100 Hz squarewave and the SMPTE/DIN IM Output signal is a stable display.

i. Change the SG 5010 FUNCTION to CCIF and the IM FREQ to 250 Hz.

j. CHECK—that the SG 5010 Sync Output signal is approximately 250 Hz squarewave and the CCIF IM Output signal is a stable display.

k. Change the SG 5010 FUNCTION to BURST; ON CYCLES to 10; and OFF CYCLES to 90.

l. CHECK—that the SG 5010 Sync Output signal is a 50 Hz repetitive pulse with the displayed waveform high state corresponding to the burst with a duration of 2 ms.

2. Check Frequency Accuracy

Refer to Fig. 5-1. Check setup 1 for the following check.

SG 5010 CONTROL SETTINGS

FUNCTION	SINE
Vrms	100.0 mV
FREQ	1.000 kHz
R SOURCE	50 ohms
GND-FLTG	FLTG
ON-OFF	ON

a. Adjust the counter for a stable display readout.

b. CHECK—for a counter displayed readout of 999.90 Hz to 1000.10 Hz.

c. Change the SG 5010 FUNCTION to SQUARE.

d. CHECK—for a counter displayed readout of 999.90 Hz to 1000.10 Hz.

e. Change the SG 5010 FUNCTION to SINE and set the FREQ button for 10.00 Hz.

f. CHECK—for a counter displayed readout of 9.9990 Hz to 10.0010 Hz.

g. Change the SG 5010 FREQ to 163.8 kHz.

h. CHECK—for a counter displayed readout of 163.7836 kHz to 163.8164 kHz.

3. Check Sine Amplitude Accuracy

Refer to Fig. 5-1. Check setup 1 for the following check.

a. Set the SG 5010 FREQ for 10.00 Hz.

b. Set the wideband true rms voltmeter range to 100 mV (200 mV range on some voltmeters).

c. CHECK—that the voltmeter readings are within the limits as shown in the following table for the frequencies specified. check for bal and unbal

SG 5010 FREQ	Voltmeter Reading (limits)
10 Hz	97.0 to 103.0 mV
20 Hz	98.0 to 102.0 mV
1.00 kHz	98.0 to 102.0 mV
20 kHz	98.0 to 102.0 mV
100 kHz	97.0 to 103.0 mV
163.8 kHz	97.0 to 103.0 mV

d. Change the SG 5010 UNBAL to BAL.

e. CHECK—(repeat step 3c).

f. Change the SG 5010 BAL to UNBAL and set the Vrms for 10.60.

g. Change the wideband voltmeter range to 10 V (20 V range on some voltmeters).

h. CHECK—that the voltmeter readings are within the limits as shown in the following table for the frequencies specified.

SG 5010 FREQ	Voltmeter Reading (limits)
10 Hz	10.28 to 10.92 V
20 Hz	10.39 to 10.81 V
20 kHz	10.39 to 10.81 V
163.8 kHz	10.28 to 10.92 V

i. Change the SG 5010 UNBAL to BAL and set the Vrms for 1.400.

j. Change the wideband voltmeter range to 1 V (2 V range on some voltmeters).

k. CHECK—that the voltmeter readings are within the limits as shown in the following table for the frequencies specified.

SG 5010 FREQ	Voltmeter Reading (limits)
10 Hz	1.358 to 1.442 V
20 Hz	1.372 to 1.428 V
20 kHz	1.372 to 1.428 V
163.8 kHz	1.358 to 1.442 V

4. Check Sine Level Flatness

Refer to Fig. 5-1. Check setup 1 for the following check.

a. Change the SG 5010 FREQ for 1.000 kHz.

b. Adjust the SG 5010 Vrms using the DEC/INC control, until the wideband voltmeter indicates a reading of 1.400 V.

NOTE

If unable to obtain this 1.400 V reading, note the closest setting and refer this difference (error) to correct all subsequent readings in this check. For example: if reading is 1.401 V, correct all subsequent readings by subtracting 0.001 V.

c. CHECK—that the voltmeter readings are within the limits as shown in the following table for the frequencies specified.

SG 5010 FREQ	Corrected (if necessary) Voltmeter Reading (limits)
10 Hz	1.368 to 1.432 V
20 Hz	1.392 to 1.408 V
20 kHz	1.392 to 1.408 V
100 kHz	1.368 to 1.432 V
163.8 kHz	1.368 to 1.432 V

5. Check Squarewave Risetime

Refer to Fig. 5-1. Check setup 1 for the following check.

SG 5010 CONTROL SETTINGS

FREQ	10.00 kHz
FUNCTION	SQUARE
Vrms	1.000 V

VERTICAL PLUG-IN SETTINGS

Display Mode	CH 1
Trigger Source	CH 1

a. Adjust the oscilloscope vertical and horizontal scale factors as necessary to make the following risetime and falltime measurements.

b. CHECK—that the risetime and falltime (10% to 90%) oscilloscope crt waveform indicates between 1.35 and 1.65 μseconds.

6. Check Squarewave Amplitude Accuracy

Refer to Fig. 5-1. Check setup 1 for the following check.

NOTE

The SG 5010 is calibrated for constant peak-to-peak output voltage (sinewave equivalent) Vrms thus, a direct true rms voltage measurement will be in error by a factor of 1.4142 for squarewaves. There will be an additional error because of the finite bandwidth limitation of the squarewave signal. For frequencies to approximately 400 Hz, this effect of non-zero risetime and falltime is negligible. Above 400 Hz, a true rms voltage measurement should be corrected by multiplying by a factor of (1+ frequency X risetime) ***FROM STEP 5.***

a. Set the SG 5010 FREQ to any frequency between 10 Hz and 16.38 kHz; e.g.,400 Hz and 1.00 Vrms.

b. CHECK—that the corrected (if necessary) voltmeter reading indicates between 1.372 and 1.457 V.

7. Check IM Frequency Accuracy

Refer to Fig. 5-1. Check setup 1 for the following check.

NOTE

The same internal low frequency source is used by both SMPTE/DIN and CCIF intermodulation test signal generators. It is sufficient to verify accuracy with only one IM test signal function selection.

SG 5010 CONTROL SETTINGS

FUNCTION	SMPTE/DIN or CCIF
FREQ	5.000 kHz
IM FREQ	40 Hz

a. Adjust the digital counter triggering controls for a stable readout.

b. CHECK—that the displayed counter readings are within limits as shown in the following table for the IM frequencies specified.

SG 5010 IM FREQ	Counter Reading (limits)
40 Hz	39.20 to 40.80 Hz
50 Hz	49.0 to 51.0 Hz
60 Hz	58.8 to 61.20 Hz
80 Hz	78.4 to 81.60 Hz
100 Hz	98.0 to 102.0 Hz
125 Hz	122.5 to 127.5 Hz
250 Hz	245.0 to 255.0 Hz
500 Hz	490.0 to 510.0 Hz

8. Check SMPTE/DIN Amplitude Accuracy

Refer to Fig. 5-1. Check setup 1 for the following check.

NOTE

The SG 5010 is calibrated for constant peak-to-peak output voltage (sinewave equivalent) Vrms, thus a direct true rms voltage measurement will be in error by a factor of 0.8246 for the 4:1 ratio IM test signal or 0.7071 for the 1:1 ratio signal.

SG 5010 CONTROL SETTINGS

FUNCTION	SMPTE/DIN
FREQ	7.000 kHz
IM FREQ	any valid IM frequency; e.g., 60 Hz.
Vrms	1.000 V

a. CHECK—that the wideband voltmeter reading indicates between 0.800 to 0.849 V.

b. Press the SG 5010 RECALL button and the SMPTE/DIN button to select the 1:1 ratio mode.

c. CHECK—that the voltmeter reading indicates between 0.686 and 0.728 V.

9. Check CCIF Amplitude Accuracy

Refer to Fig. 5-1. Check setup 1 for the following check.

NOTE

The SG 5010 is calibrated for constant peak-to-peak output voltage (sinewave equivalent) Vrms, thus a direct true rms voltage measurement will be in error by a factor of 0.7071 for the CCIF IM test signal.

SG 5010 CONTROL SETTINGS

FUNCTION	CCIF
FREQ	any frequency between 2.5 kHz and 163.8 kHz (e.g. 14.5 kHz).
IM FREQ	500 Hz
Vrms	1.000 V

a. CHECK—that the wideband voltmeter indicates a reading between 0.672 and 0.742 V.

10. Check Burst ON/OFF Amplitude Accuracy

Refer to Fig. 5-1. Check setup 1 for the following check.

SG 5010 CONTROL SETTINGS

FUNCTION	BURST
FREQ	any frequency between 10 Hz and 50 kHz (e.g., 10 kHz).
Vrms	1.000 V
ON CYCLES	10
OFF CYCLES	0

a. CHECK—that the wideband voltmeter indicates a reading between 0.970 to 1.030 V.

b. Change the SG 5010 OFF CYCLES to 99999.

c. CHECK—that the voltmeter indicates a reading less than 10 mV (the voltmeter range may have to be adjusted for this reading).

d. Press the SG 5010 RECALL and BURST buttons to select the 10% Burst-off mode.

e. CHECK—that the voltmeter reading indicates between 0.094 and 0.106 V (the voltmeter range may have to be adjusted for this reading).

11. Check DC Offset

Refer to Fig. 5-2. Check setup 2 for the following check.

SG 5010 CONTROL SETTINGS

FUNCTION	EXT
Vrms	10.60 V
UNBAL-BAL	UNBAL
ON-OFF	ON

DIGITAL MULTIMETER SETTINGS

Volts	DC
Range	2 V

a. CHECK—that the digital multimeter readout indicates between −15.0 mV and +15.0 mV.

b. Change the SG 5010 UNBAL to BAL and the Vrms to 21.2 V.

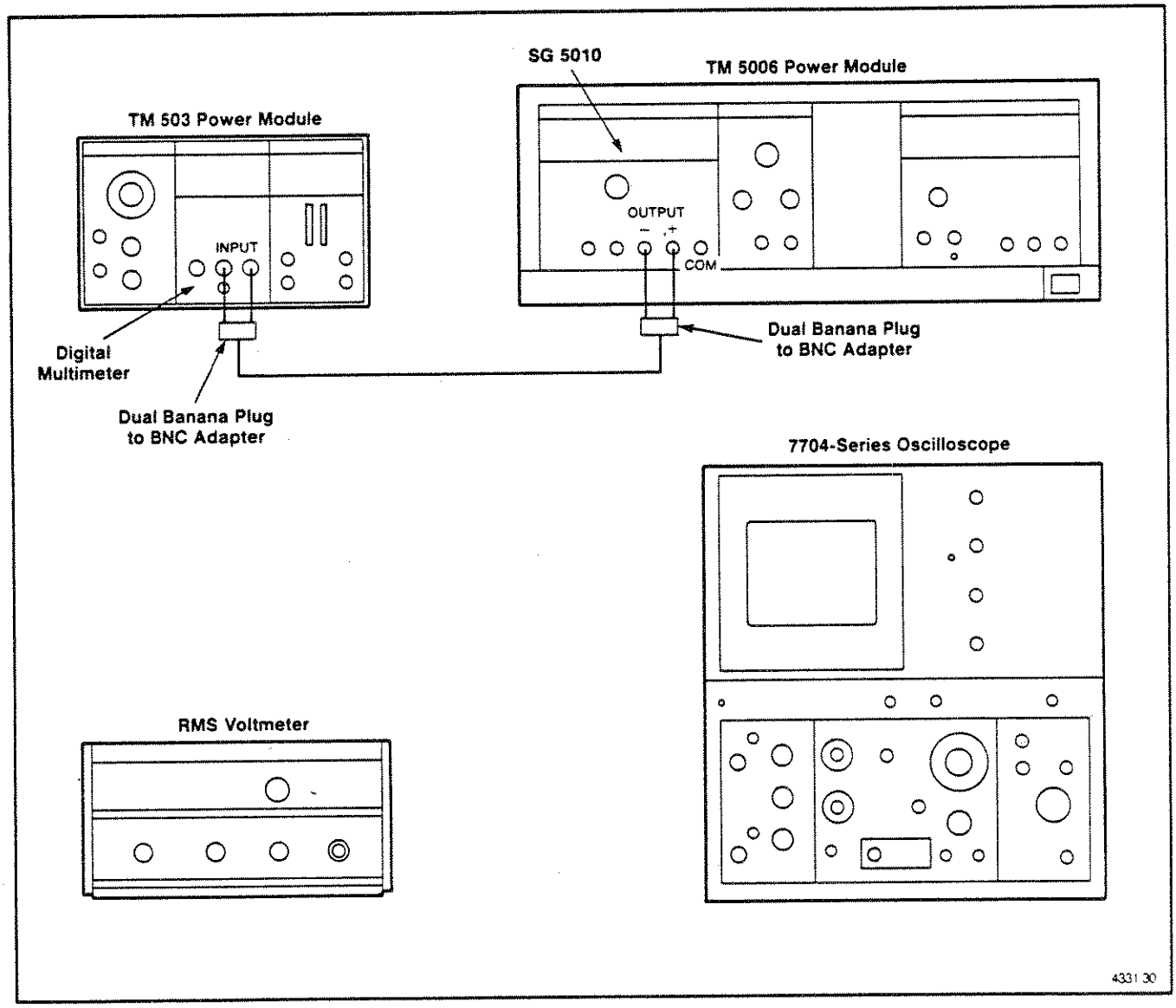


Fig. 5-2. SG 5010 check setup 2.

c. CHECK—that the multimeter readout indicates between −25.0 mV and +25.0 mV.

12. Check Output Impedance (SOURCE R) Accuracy

Refer to Fig. 5-2. Check setup 2 for the following check.

SG 5010 CONTROL SETTINGS

ON-OFF	OFF

DIGITAL MULTIMETER SETTINGS

Mode	Ω

a. Set the multimeter range to 200 Ω.

b. CHECK—that the multimeter readout indicates between 48.5 and 51.5 when SG 5010 R SOURCE is selected for 50 Ω. When R SOURCE is 150 Ω, the reading indicates between 147.0 and 153.0 Ω.

c. Change the multimeter Range to 2 k .

d. Change the SG 5010 R SOURCE for 600 Ω.

e. CHECK—that the multimeter readout indicates between 594.0 and 606.0 Ω.

f. Change the SG 5010 UNBAL-BAL to BAL.

g. Repeat steps 12a through 12f.

13. Check Sinewave Distortion

Refer to Fig. 5-3. Check setup 3 for the following check.

NOTE

A complex and lengthy procedure is required to verify the SG 5010 ultra-low distortion. Unless there is reason to suspect the SG 5010 may not meet its distortion specification because of recent repair to the SINE section or accidental abuse, it is suggested that this step be omitted. Step 14 verifies system distortion and noise performance with the AA 5001 Distortion Analyzer which will include the effects of SG 5010 distortion.

The following procedure checks THD in the UNBAL mode only. If desired, the THD in the BAL mode may be checked; however each output should be referenced to Common Terminal (CT) and tested individually with the results averaged. An additional 600 Ω resistor should be paralleled with the output to create a 300 Ω effective load to CT. A 300 Ω resistor should be placed from the unused output to CT to provide maximum output load.

SG 5010 CONTROL SETTINGS

FUNCTION	SINE
Vrms	2.000 V
FREQ	10 Hz
R SOURCE	50 Ω
ON-OFF	ON
GND-FLTG	GND
UNBAL-BAL	UNBAL

Calibration Fixture CONTROL SETTINGS

NOTCH FREQUENCY	10 Hz
MODE	Flat (out)
ATTEN	−60 dB (in)

7L5 CONTROL SETTINGS

FREQUENCY	50 Hz/div
RESOLUTION	10 Hz
TIME/DIV	10 sec/div
LOG	10 dB/div
SOURCE MODE	FREE RUN,NORMAL

Set the L3 controls to 1 MΩ ,dBv.

Distortion Analyzer Settings

INPUT RANGE	20 mV/div
FUNCTION LEVEL	FILTERS (OFF)

a. Set the 7L5 A & B to off and manual sweep.

Adjust the 7L5 manual sweep dial to position the dot horizontally in line with the 10 Hz graticule mark (see Fig. 5-4).

Adjust the 7L5 Reference level control to position the dot vertically on the top graticule line (this line is the −60 dB reference level).

NOTE

The 1 dB/Step Reference Level control should be used to set the −60 dB reference rather than the Variable control to avoid increasing the amplitude of the 0 Hz displayed spur.

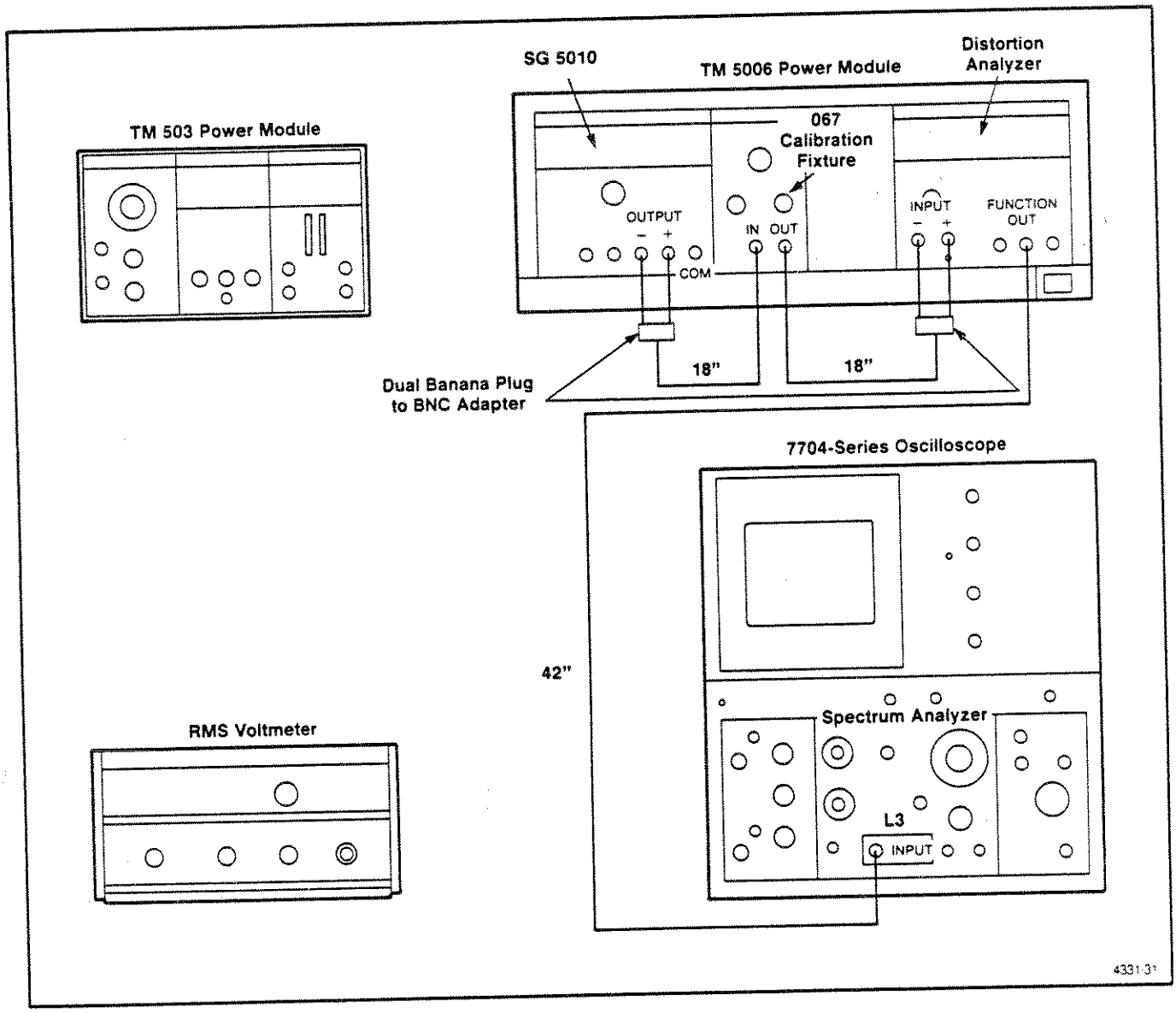


Fig. 5-3. SG 5010 check setup 3.

b. Set the calibration fixture Mode to Notch (in) position and the Atten to 0 dB (out). Adjust the SG 5010 FREQ and the calibration fixture Adj for Null controls to position the dot vertical to the most stable point below the −80 dB level on the display. (See Fig. 5-4.)

c. Change the distortion analyzer RANGE control to 2 mV (this adds 20 dB more gain to the display).

Re-adjust the SG 5010 FREQ and the calibration fixture ADJ and Null controls for minimum displayed amplitude.

d. Set the 7L5 A & B to the on position and normal sweep mode.

e. Note the 2nd, 3rd, 4th, and 5th harmonics on the displayed waveform (see Fig. 5-5). If the harmonic amplitudes on either side of the 0 Hz are slightly different, average the two readings for each harmonic.

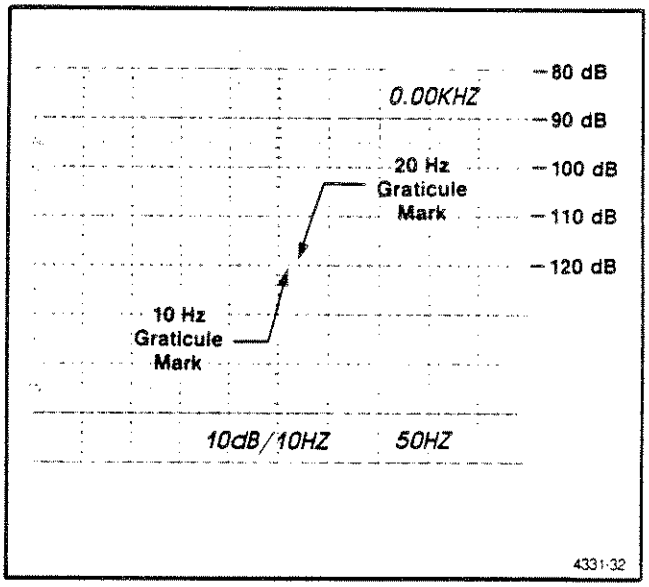


Fig. 5-4. 10 Hz null adjustment.

NOTE

Due to the purely passive nature of the 067-0938-00 Calibration Fixture, the losses at the various harmonics must be taken into account to correct the harmonic values noted on the spectrum analyzer display. The following loss (correction) factors must be added to the displayed values to obtain corrected values

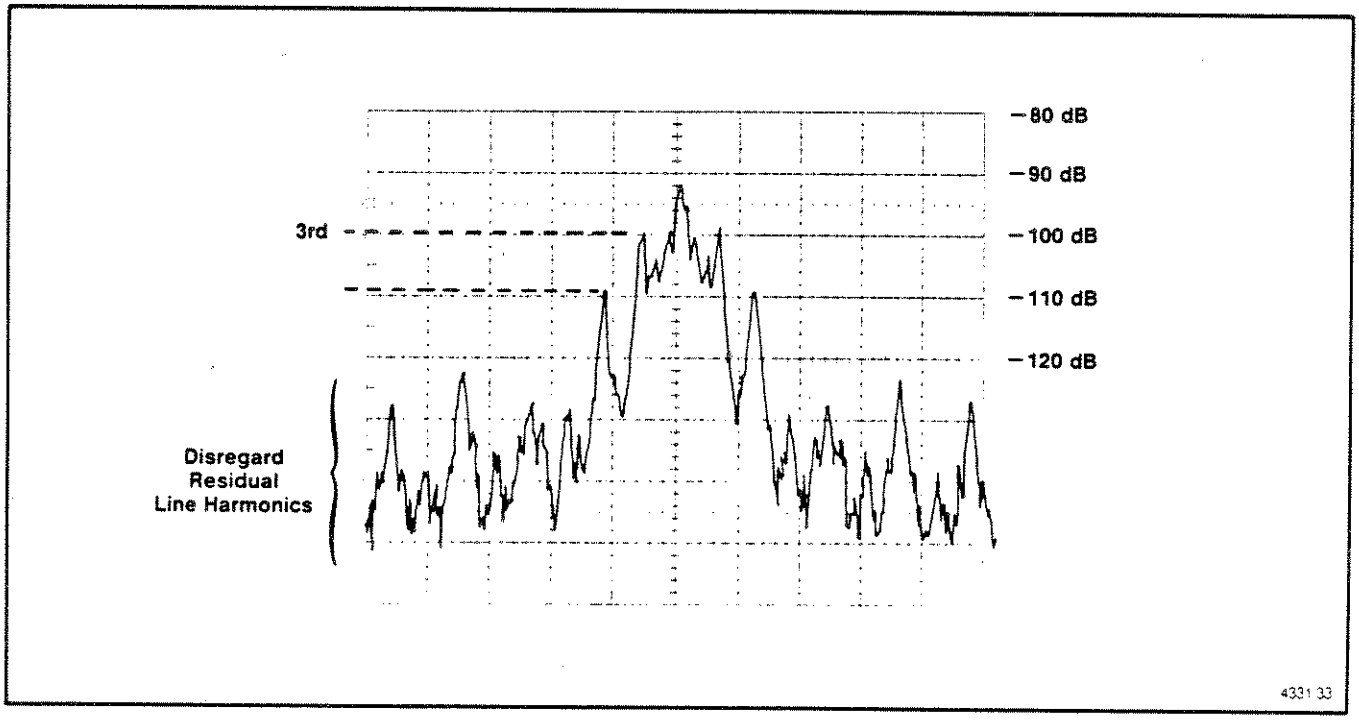


Fig. 5-5. 10 Hz harmonic distortion display.

TABLE 5-1
HARMONIC CORRECTION FACTORS

Harmonic	Notch Frequency Setting		
	10 Hz to 20 kHz	50 kHz	100 kHz
2nd	9.5	10	10.5
3rd	6.0	6.5	7
4th	4.5	5	5.5
5th	3.5	4	4.5

e. Compute the harmonic distortion (thd) using the harmonic values noted and either of the two following methods.

Formula Method for Computing thd:

Substitute the harmonic values (in dB), noted in step 13-d, in the following formula:

The numbers added to the harmonic values in the formula are correction factors for the calibration fixture at 10 Hz Notch Frequency.

Example:

Using the harmonic distortion levels in Table 5-1 and the corrections factors in the previous formula.

2nd harmonic = − 110 dB + 9.5 = − 100.5
3rd harmonic = − 107 dB + 6 = − 101
4th harmonic = − 115 dB + 4.5 = − 110.5
5th harmonic = − 121 dB + 3.5 = − 117.5

Dividing by 10 and raising 10 to this power gives:

$$\begin{aligned} -100.5 \div 10 &= -10.05 \quad 10^{-10.05} = 89.12 \times 10^{-12} \\ -101 \div 10 &= -10.1 \quad 10^{-10.1} = 79.43 \times 10^{-12} \\ -110.5 \div 10 &= -11.05 \quad 10^{-11.05} = 8.91 \times 10^{-12} \\ -117.5 \div 10 &= -11.75 \quad 10^{-11.75} = 1.77 \times 10^{-12} \\ & \qquad\qquad\qquad\qquad 179.2 \times 10^{-12} \end{aligned}$$

Taking the square root results in:

$$\sqrt{179.2 \times 10^{-12}} = 1.34 \times 10^{-5}$$

Taking the log:

$$\text{Log}_{10}\, 1.34 \times 10^{-5} = -4.87$$

Multiplying by 20:

$$-4.87 \times 20 = -97.46 \text{ dB thd}$$

Table Method for Computing thd:

Add the calibration fixture correction factors to the harmonic distortion levels noted in step 14-d. For example, using the harmonic distortion levels in Table 5-1 and the calibration fixture correction factors for 10 Hz Notch Frequency:

2nd harmonic = − 110 dB + 9.5 = − 100.5
3rd harmonic = − 107 dB + 6 = − 101
4th harmonic = − 115 dB + 4.5 = − 110.5
5th harmonic = − 121 dB + 3.5 = − 117.5

Compute the arithmetic difference between the two numerically lower dB values - in this case, −100.5 and −101. Locate this difference value (0.5) in Table 5-2. If the difference value falls between two of the difference values in the table, interpolate the corresponding value in the Additive Factor column. Algebraically add the number in the Additive Factor column (2.77) to the numerically lower dB value:

$$\begin{array}{r} -100.50 \\ 2.77 \\ \hline -\ 97.73 \end{array}$$

Now repeat the process (find the arithmetic difference) using the resulting number (−97.73) and the next numerically lower dB value:

$$\begin{array}{r} -110.50 \\ -\ 97.73 \\ \hline 12.77 \end{array}$$

The value opposite 12.77 in Table 5-2 is approximately 0.23. Algebraically adding 0.23 to −97.73 = −97.50. Repeat the process using −97.50 and the remaining dB value to the combined, −117.5:

$$\begin{array}{r} -117.5 \\ -\ 97.50 \\ \hline -\ 20.00 \end{array}$$

The value opposite 20.00 in the table is approximately 0.04.

$$\begin{array}{r} -97.50 \\ 0.04 \\ \hline -97.46 = \text{thd} \end{array}$$

Table 5-2
FACTORS FOR THD COMPUTATION

Difference Value	Additive Factor
0.0	3.01
0.5	2.77
1.0	2.54
2.0	2.12
3.0	1.76
4.0	1.46
5.0	1.19
6.0	0.97
7.0	0.79
8.0	0.64
9.0	0.51
10.0	0.41
11.0	0.33
12.0	0.27
13.0	0.21
14.0	0.17
15.0	0.14
16.0	0.11
17.0	0.09
18.0	0.07
19.0	0.05
20.0	0.04

f. CHECK—that the calculated thd is less than −95 dB.

g. Change the SG 5010 FREQ to 20 Hz.

Change the calibration fixture Notch Frequency to 20 Hz.

h. Repeat steps 13-b through 13-e using the 20 Hz graticule mark on the display for step 13-b (see Fig. 5-6).

i. CHECK—that the calculated thd is less than −102 dB (see Fig. 5-6 for harmonics at 20 Hz).

Refer to Fig. 5-7. Check setup 4 for the following check.

j. Change the SG 5010 FREQ to 20 kHz.

Change the calibration fixture Notch Frequency to 20 kHz.

k. Set the calibration fixture Mode to Flat (out) and the Atten to −60 dB (in) position.

Change the 7L5 to 10 kHz/div and 0.1 sec/div.

l. Adjust the 7L5 reference level control to position the 20 kHz peak on the top horizontal graticule line. This line is the −60 dB reference level.

m. Set the calibration fixture Mode to Notch (in) and Atten to 0 dB (out).

Adjust the SG 5010 FREQ and the two calibration fixture Adjust For Null controls to position the 20 kHz peak below the top horizontal graticule line.

n. Note the 2nd, 3rd, 4th, and 5th harmonics on the waveform, or as many of these harmonics as are visible. See Fig. 5-4 and compute the thd using the formula in step 13-e.

o. CHECK—that the calculated thd is less than −102 dB.

p. Change the SG 5010 FREQ to 50 kHz.

Change the calibration fixture Notch Frequency to 50 kHz.

q. Repeat steps 13-k through 13-m, except position the 50 kHz peak (2nd peak) of the waveform.

NOTE

The loss (correction) factors for the 067-0938-00 Calibration Fixture at the 50 kHz and 100 kHz frequencies are slightly different from the correction factors for the lower frequencies (see Table 5-1).

r. CHECK—that the calculated thd is less than −95 dB.

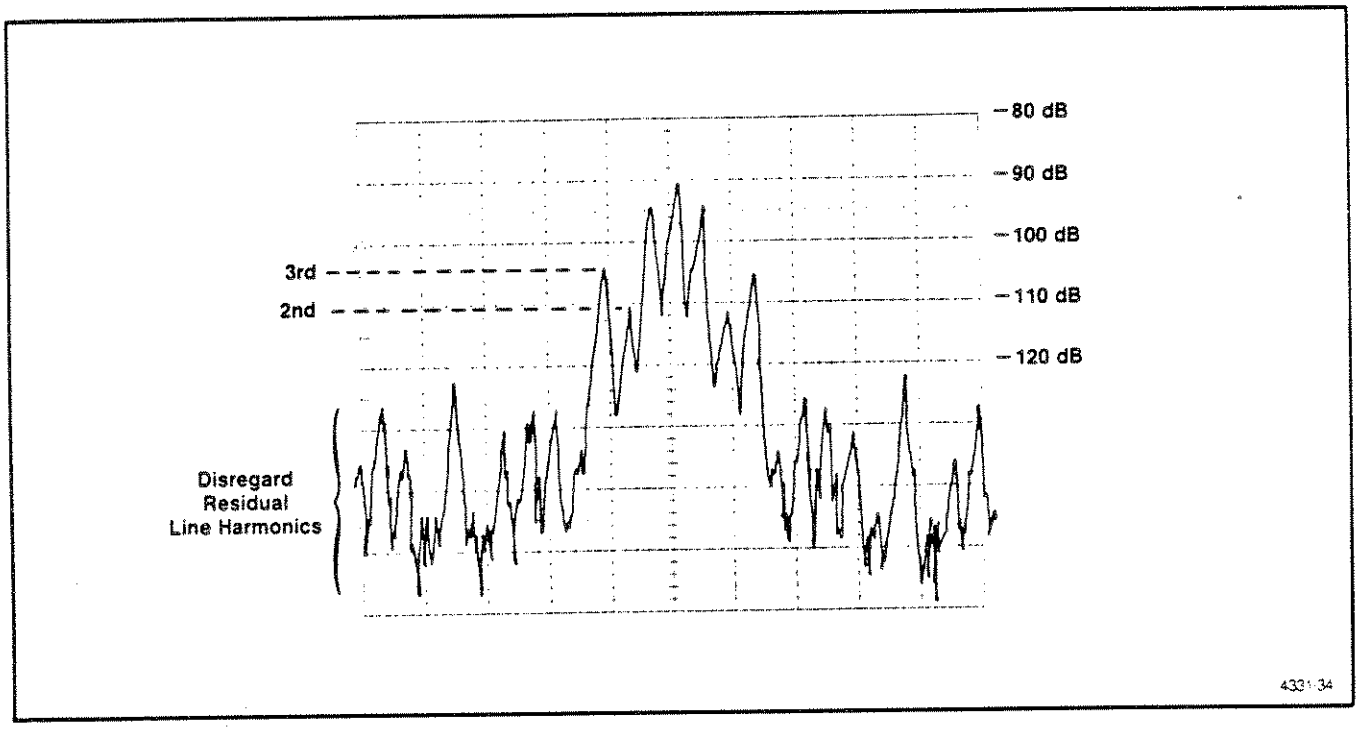


Fig. 5-6. 20 Hz harmonic distortion display.

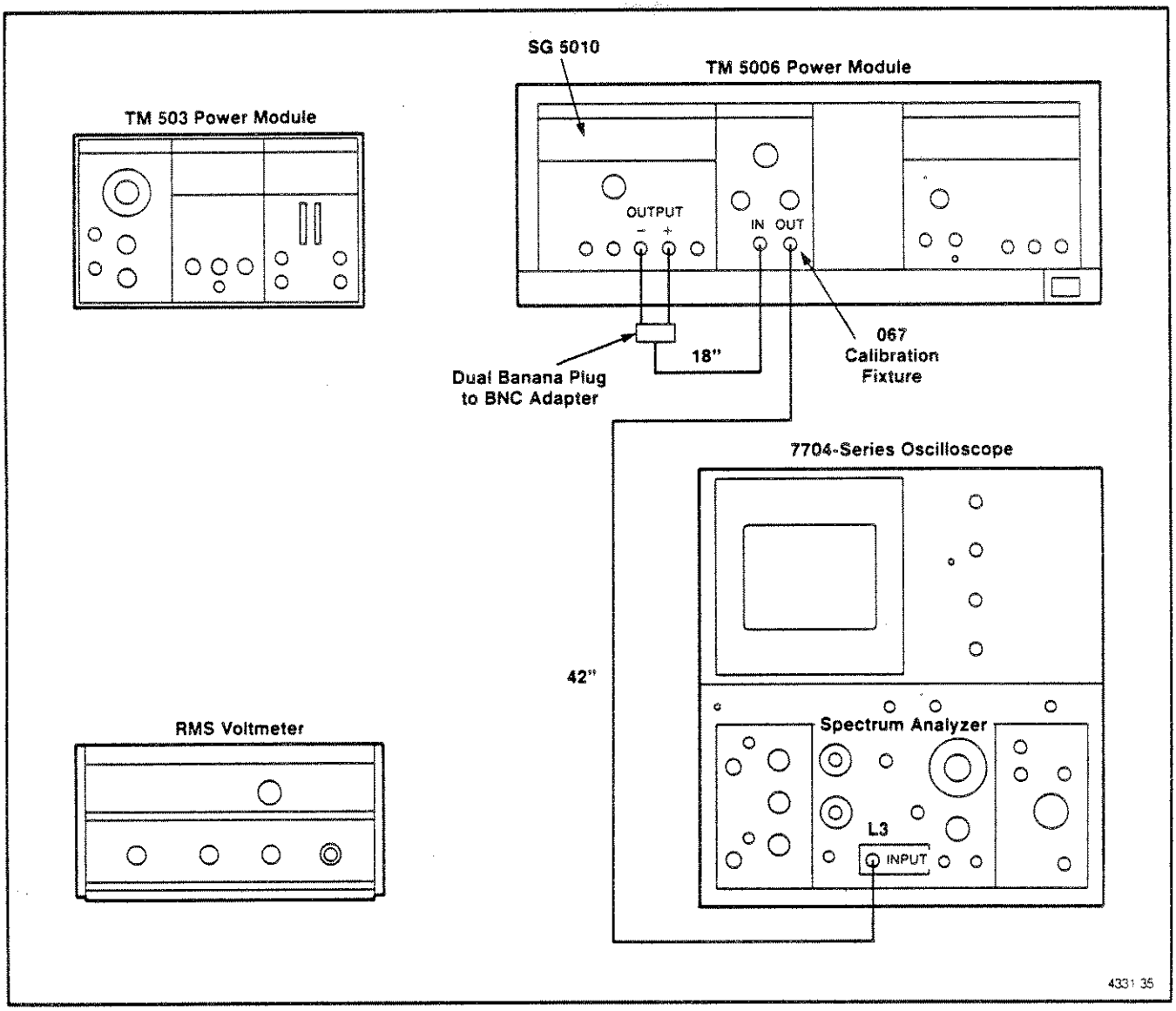


Fig. 5-7. SG 5010 check setup 4.

s. Change the SG 5010 FREQ to 100 kHz.

Change the calibration fixture Notch Frequency to 100 kHz.

t. Repeat steps 13-k through 13-m, except position the 100 kHz peak (2nd peak) of the waveform.

u. CHECK—that the calculated thd is less than −90 dB.

v. Change the SG 5010 FREQ to 163.8 kHz.

Set the calibration fixture Mode switch to FLAT and 7L5 to 100 kHz/div.

Adjust the 7L5 Reference Level to position the peak at the top of the screen (see Fig. 5-8).

w. CHECK—that all harmonics are below −70 dB.

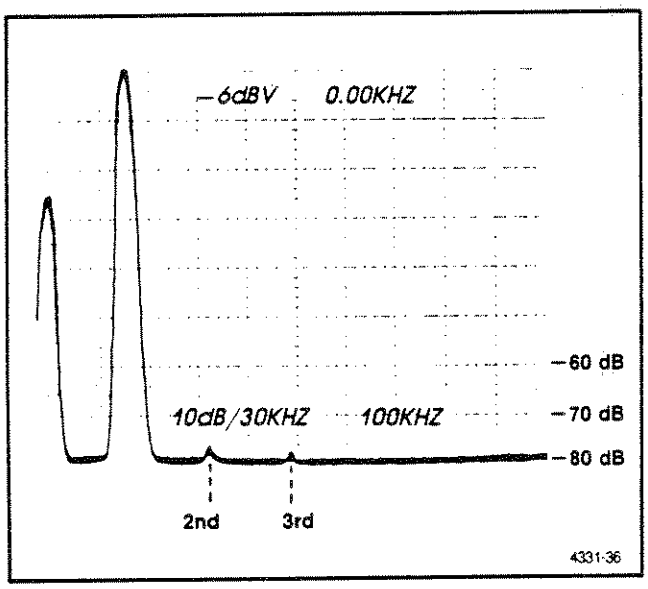


Fig. 5-8. 163 kHz THD display.

14. Check Residual THD+N (System Specification with AA 5001, Distortion Analyzer)

Refer to Fig. 5-9. Check setup 5 for the following check.

SG 5010 CONTROL SETTINGS

FUNCTION	SINE
Vrms	any setting>250 mV, e.g. 3.00 V
UNBAL-BAL	UNBAL
ON-OFF	ON

AA 5001 CONTROL SETTINGS

Input	Autorange
Function	THD+N
%	Autorange

a. CHECK—that the displayed AA 5001 readings do not exceed the limits as shown in the following table for the frequencies specified and for the AA 5001 filter specified.

SG 5010 Freq	AA 5001 FILTER AA	AA 5001 THD+N (limits)
10 Hz	none	0.010 %
20 Hz	80 kHz	0.0032 %
1 kHz	80 kHz	0.0032 %
20 kHz	80 kHz	0.0032 %
50 kHz	none	0.010 %
100 kHz	none	0.010 %

b. Change the SG 5010 UNBAL to BAL.

c. CHECK—repeat step 14a.

15. Check Residual SMPTE/DIN IMD (System Specification with AA 5001, Distortion Analyzer)

Refer to Fig. 5-9. Check setup 5 for the following check.

SG 5010 CONTROL SETTINGS

FUNCTION	SMPTE/DIN
Vrms	any setting >250 mV, e.g. 3.00 V
UNBAL-BAL	UNBAL
FREQ	7 kHz or 8 kHz
IM FREQ	60 Hz or 250 Hz

a. Change the AA 5001 Function to IMD and turn off any selected filters.

b. CHECK—that the displayed AA 5001 reading does not exceed 0.0032 %.

c. Change the SG 5010 UNBAL to BAL.

d. CHECK—repeat step 15b.

e. Press the SG 5010 RECALL button and SMPTE/DIN button to select the special function 1:1 ratio test signal.

f. CHECK—repeat step 15b.

g. Change the SG 5010 BAL to UNBAL.

h. CHECK—repeat step 15b.

16. Check Residual CCIF IMD (System Specification with AA 5001, Distortion Analyzer)

Refer to Fig. 5-9. Check setup 5 for the following check.

SG 5010 CONTROL SETTINGS

FUNCTION	CCIF
Vrms	any setting >250 mV, e.g. 3.00 V
FREQ	14.5 kHz
IM FREQ	500 Hz

a. CHECK—that the displayed AA 5001 reading does not exceed 0.0018 %.

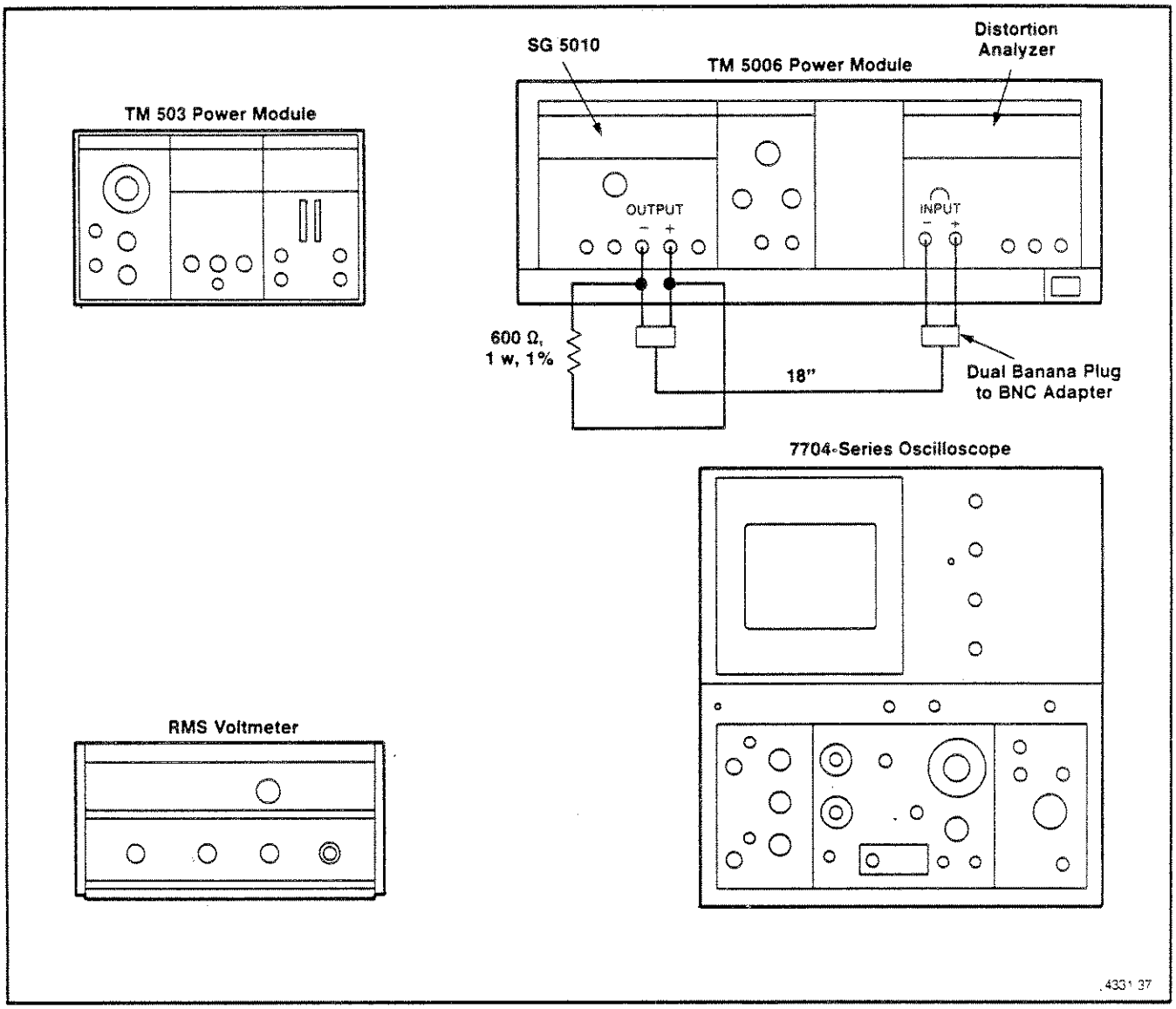


Fig. 5-9. SG 5010 check setup 5.

b. Change the SG 5010 UNBAL to BAL.

c. CHECK—repeat step 16a.

17. Check CCIF Center Frequency Leakage and Harmonic Content

Refer to Fig. 5-7. Check setup 4 for the following check.

SG 5010 CONTROL SETTINGS

FREQ	20 kHz
Vrms	1.000 V
UNBAL-BAL	UNBAL
GND-FLTG	FLTG
ON-OFF	ON

Spectrum Analyzer SETTINGS

Frequency	200 Hz/div
Resolution	30 Hz
Time/Div	2 Sec/div
Log	10 dB/div
Source Mode	Free Run, Normal

a. Adjust the spectrum analyzer for a center frequency of 20 kHz (refer to Fig. 5-10). Rotate the Reference Level control to line up the displayed twin tones at 19.5 kHz and 20.5 kHz with the top graticule line (0 dB reference level).

b. CHECK—that the displayed center frequency leakage (at 20 kHz) is at least 40 dB below the reference level.

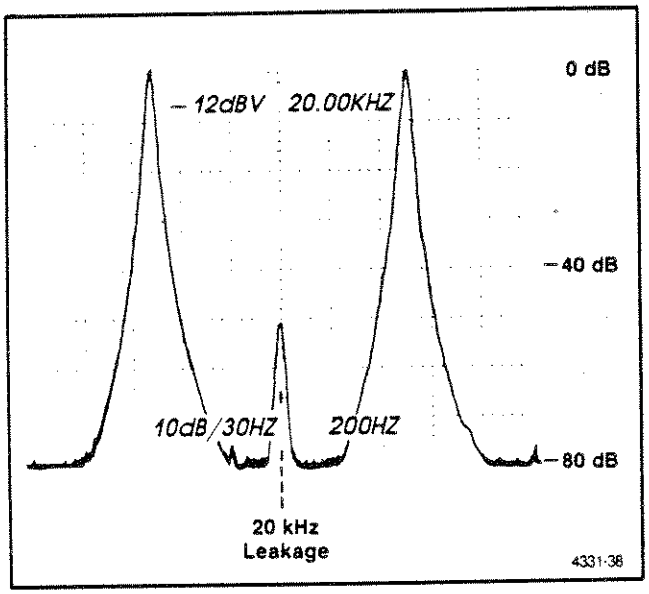


Fig 5-10. CCIF center frequency leakage.

c. Adjust the spectrum analyzer for a center frequency of 40 kHz with a 500 Hz/div span and 100 Hz resolution setting.

d. CHECK—That the displayed waveform has no frequency components greater than —40 dB, with respect to the reference shown in step 17a.

e. Adjust the spectrum analyzer for a center frequency of 60 kHz and repeat step 17d.

18. Check External Input Gain Accuracy

Refer to Fig. 5-11. Check setup 6 for the following check.

SG 5010 CONTROL SETTINGS

FUNCTION	EXT
Vrms	1.400 V
R SOURCE	50
UNBAL-BAL	UNBAL
GND-FLTG	GND
ON-OFF	ON

a. Set the SG 5010 for a 1 kHz frequency and 2.000 V rms using the wideband voltmeter.

b. Disconnect the voltmeter (from the tee connector) and re-attach this cable to the SG 5010 OUTPUT connectors.

c. CHECK—that the voltmeter indicates a reading between 1.330 and 1.470 V.

19. Check External Input Frequency Response

Refer to Fig. 5-11. Check setup 6 for the following check.

a. Adjust the SG 5010 Vrms using the DEC/INC control for 1.400 V readout on the wideband voltmeter.

NOTE

If unable to obtain this 1.400 V reading, note the closest setting and refer this difference (error) to correct all subsequent readings in this check. for example: if reading is 1.401 V, correct all subsequent readings by subtracting 0.001 V.

b. Connect the wideband voltmeter to the bnc tee connector and note the reading.

c. Set the SG 5010 Frequency to 20 Hz.

d. Re-adjust the sinewave generator Output control (vernier) to display the reading from step 19b (3 mV ,or less, errors may be ignored).

e. Re-connect the wideband voltmeter to the SG 5010 OUTPUT.

f. CHECK—that the voltmeter reading indicates between 1.384 and 1.416 V.

g. Set the sinewave generator Frequency to 20 kHz.

h. Re-adjust the sinewave generator Output vernier control to display the reading from step 19b (3 mV,or less, errors may be ignored).

i. Re-connect the wideband voltmeter to the SG 5010 OUTPUT.

j. CHECK—that the voltmeter reading indicates between 1.384 and 1.416 V.

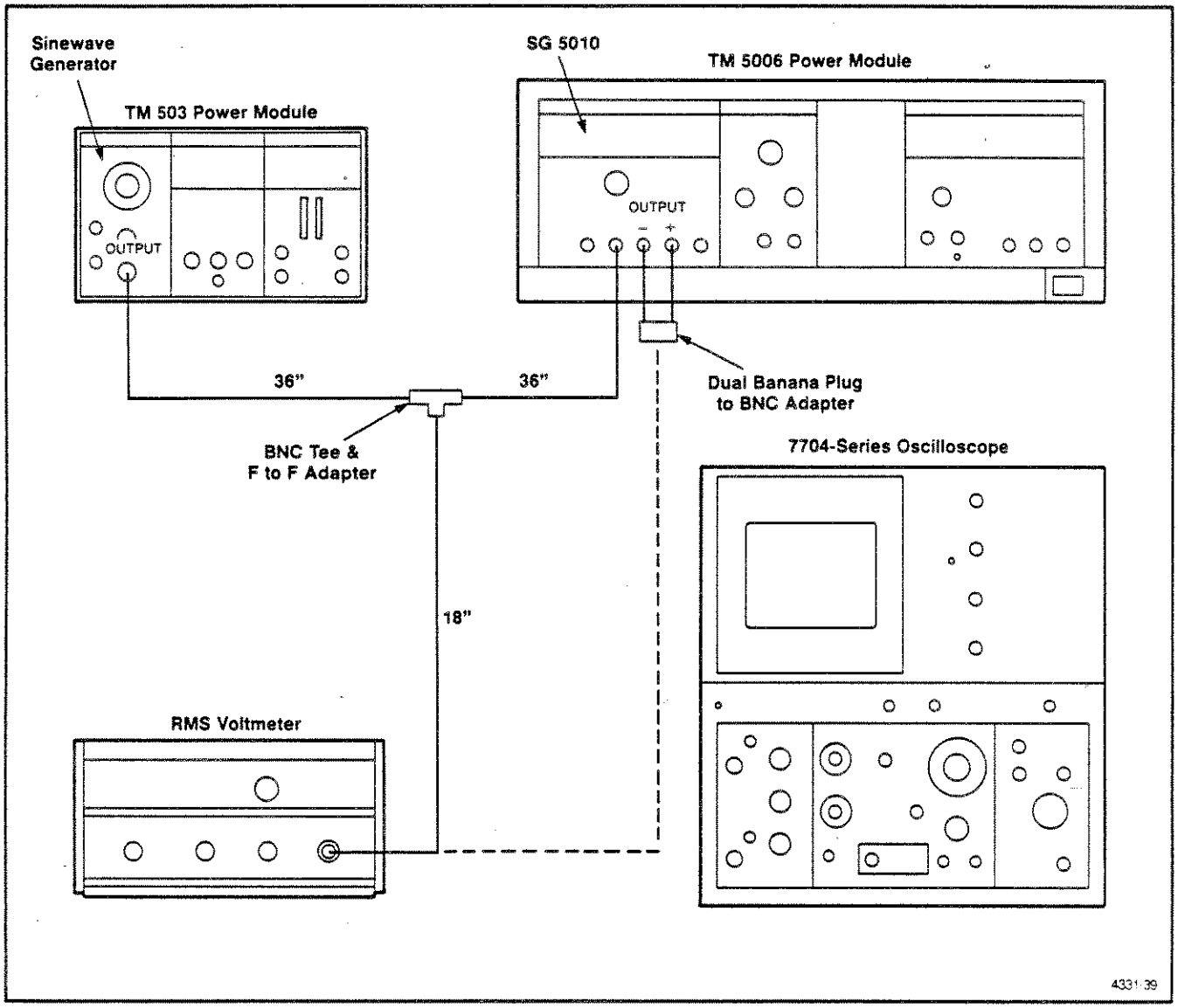


Fig. 5-11. SG 5010 check setup 6.

20. Check External Input THD+N

Refer to Fig. 5-11. Check setup 6 for the following check.

SG 5010 CONTROL SETTINGS

FUNCTION	EXT
Vrms	any setting >250 mV, e.g. 1.400 V
GND/FLTG	GND

a. Set the AA 5001 for Input Autoranging, THD+N Function, % Autorange, and 80 kHz Filter.

b. CHECK—that the AA 5001 reading does not exceed 0.010 % for the SG 5010 20 Hz, 1 kHz, and 20 kHz Frequency settings.

21. Check The GPIB Through Controller.

Refer to the Talker/Listener sample programs in the Programming Section of this manual.

a. Connect the controller to the TM5000 Series power module.

b. RUN the sample program for your selected controller using settings and queries commands.

c. CHECK—the SG5010 display readout and front panel lighted buttons for returned query data.

This completes the Performance Check.

USERS CHECK LIST

STEP	CHARACTERISTIC	ALLOWABLE LIMITS	ACTUAL VALUE
2	Freq. Accuracy		
	1 kHz Sine	999.90 to 1000.10 Hz	
	1 kHz Square	999.90 to 1000.10 Hz	
	10 Hz Sine	9.9990 to 10.0010 Hz	
	163.8 kHz Sine	163.7863 to 163.8164 kHz	
3	Sine Ampl Accuracy		
	100 mV,Unbal		
	10 Hz	97.0 to 103.0 mV	
	20 Hz	98.0 to 102.0 mV	
	1 kHz	98.0 to 102.0 mV	
	100 mV, Balanced		
	10 Hz	97.0 to 103.0 mV	
	20 Hz	98.0 to 102.0 mV	
	1 kHz	98.0 to 102.0 mV	
	20 kHz	98.0 to 102.0 mV	
	100 kHz	97.0 to 103.0 mV	
	163.8 kHz	97.0 to 103.0 mV	
	10.6 V, Unbalanced		
	10 Hz	10.28 to 10.92 V	
	20 Hz	10.39 to 10.81 V	
	20 kHz	10.39 to 10.81 V	
	163.8 kHz	10.28 to 10.92 V	
	1.40 V, Balanced		
	10 Hz	1.358 to 1.442 V	
	20 Hz	1.372 to 1.428 V	
	20 kHz	1.372 to 1.428 V	
	163.8 kHz	1.358 to 1.442 V	
4	Sine Level Flatness		
	(1.400 V, 1 kHz refer)		
	10 Hz	1.368 to 1.432 V	
	20 Hz	1.392 to 1.408 V	
	20 kHz	1.392 to 1.408 V	
	100 kHz	1.368 to 1.432 V	

USERS CHECK LIST (cont)

STEP	CHARACTERISTIC	ALLOWABLE LIMITS	ACTUAL VALUE
	163.8 kHz	1.368 to 1.432 V	
5	Square Wave		
	Rise Time	1.35 to 1.65 μs	
	Fall Time	1.35 to 1.65 μs	
6	1 V Rms Square		
	Ampl Accuracy	1.372 to 1.457 V	
7	IM Freq Accuracy		
	40 Hz	39.2 to 40.8 Hz	
	50 Hz	49.0 to 51.0 Hz	
	60 Hz	58.8 to 61.2 Hz	
	80 Hz	78.4 to 81.6 Hz	
	100 Hz	98.0 to 102.0 Hz	
	125 Hz	122.5 to 127.5 Hz	
	250 Hz	245.0 to 255.0 Hz	
	500 Hz	490.0 to 510.0 Hz	
8	1 V Rms SMPTE/DIN Ampl Accuracy		
	4:1 Ratio	0.800 to 0.849 V	
	1:1 Ratio	0.686 to 0.728 V	
9	1 V Rms CCIF		
	Ampl Accuracy	0.672 to 0.742 V	
10	1 V Rms Burst Ampl Accuracy		
	ON	0.970 to 1.030 V	
	0% OFF	≤10 mV	
	10% OFF	94.0 to 106.0 mV	
11	DC Offset		
	Unbalanced	−15.0 to +15.0 mV	
	Balanced	−25.0 to +25.0 mV	
12	Output Impedance Accuracy Unbalanced		
	50 ohms	48.5 to 51.5 ohms	
	150 ohms	147.0 to 153.0 ohms	
	600 ohms	594.0 to 606.0 ohms	
	Balanced		
	50 ohms	48.5 to 51.5 ohms	
	150 ohms	147.0 to 153.0 ohms	

USERS CHECK LIST (cont)

STEP	CHARACTERISTIC	ALLOWABLE LIMITS	ACTUAL VALUE
	600 ohms	594.0 to 606.0 ohms	
13	Sine Distortion (2nd through 5th thd)		
	10 Hz	0.010% (−80 dB)	
	20 Hz	0.0010% (−100 dB)	
	1 kHz	0.0010% (−100 dB)	
	20 kHz	0.0010% (−100 dB)	
	50 kHz	0.0032% (−90 dB)	
	100 kHz	0.010% (−80 dB)	
	163.8 kHz	0.032% (−70 dB)	
14	System Residual THD+N (with AA 5001) Unbalanced		
	10 Hz	0.010% (−80 dB)	
	20 Hz	0.0032% (−90 dB)	
	1 kHz	0.0032% (−90 dB)	
	20 kHz	0.0032% (−90 dB)	
	50 kHz	0.010% (−80 dB)	
	100 kHz	0.010% (−80 dB)	
	Balanced		
	10 Hz	0.010% (−80 dB)	
	20 Hz	0.0032% (−90 dB)	
	1 kHz	0.0032% (−90 dB)	
	20 kHz	0.0032% (−90 dB)	
	50 kHz	0.010% (−80 dB)	
	100 kHz	0.010% (−80 dB)	
15	System Residual SMPTE/DIN IMD (with AA 5001) 4:1 Ratio		
	Unbalanced	0.0032% (−90 dB)	
	Balanced	0.0032% (−90 dB)	
	1:1 Ratio		
	Unbalanced	0.0032% (−90 dB)	
	Balanced	0.0032% (−90 dB)	
16	System Residual CCIF IMD (with AA 5001)		
	Unbalanced	0.0018% (−95 dB)	
	Balanced	0.0018% (−95 dB)	

USERS CHECK LIST (cont)

STEP	CHARACTERISTIC	ALLOWABLE LIMITS	ACTUAL VALUE
17	CCIF Center Freq Leakage & Harmonic Content		
	20 kHz	−40 dB	
	37.5 to 42.5 kHz	−40 dB	
	57.5 to 62.5 kHz	−40 dB	
18	Ext Input Gain		
	Accuracy	1.330 to 1.470 V	
19	Ext Input Freq Response (1.400 V, 1 kHz reference)		
	20 Hz	1.384 to 1.416 V	
	20 kHz	1.384 to 1.416 V	
20	Ext Input THD+N		
	20 Hz	0.010% (−80 dB)	
	1 kHz	0.010% (−80 dB)	
	20 kHz	0.010% (−80 dB)	

ADJUSTMENT PROCEDURE

Introduction

This procedure need not be performed unless the instrument fails to meet the performance requirements of the electrical characteristics listed in the Specification section of this manual. To ensure instrument accuracy, perform the adjustment of the instrument every 2000 hours of operation or every twelve months if used infrequently. Adjustment may be required after a repair has been made. If adjustment of internal controls does not bring the instrument performance within the limits listed in the Specification section, troubleshooting is indicated. Adjustments should be made with the instrument operating at an ambient temperature of 20°C to 30°C.

Test Equipment Required

Test equipment used for adjustment of the SG 5010 is listed at the beginning of the Performance Check section of this manual.

Preparation

To gain access to the test points and adjustable components, remove the instrument side covers (refer to the Maintenance section for instructions). The adjustment locations are also shown in the illustration located in the pull-out pages in the rear of this manual.

Connect the SG 5010 to the power module via the extender cable. Connect the test equipment and the power module to a suitable line voltage source.

Turn on the power module and test equipment; allow at least 30 minutes warm-up time for the SG 5010.

PROCEDURE

1. SINE Adjust

Refer to Adjustment setup in Fig. 6-1.

SG 5010 Control Settings

FREQ	1 kHz
FUNCTION	SINE
BAL-UNBAL	BAL
Vrms	2.000 V
R SOURCE	50
GND/FLTG	GND
ON/OFF	ON

Rms Voltmeter Settings

VOLTS	2 V

a. Connect the test cable from the SG 5010 front panel + OUTPUT and COM connectors to the rms voltmeter input connectors (observe proper lead polarities).

b. Locate the SINE control that is accessed through the SG 5010 bottom cover (rear of instrument).

c. ADJUST—the SINE control (R4083) for a digital readout of 1.000 Vac.

2. BAL Adjust

Refer to Adjustment setup in Fig. 6-1.

Use the same control settings from Step 1.

a. Locate the BAL control that is accessed through the SG 5010 bottom cover (front of the instrument).

b. ADJUST—the BAL control (R4028) for a digital readout of 1.000 Vac.

3. MAIN OSC FREQ Adjust

Refer to Adjustment setup in Fig. 6-2.

Use the same control settings from Step 1.

a. Disconnect the rms voltmeter Input test cable and connect to the digital multimeter Input connectors.

b. Connect the + test lead to testpoint, TP3183 (located on the Oscillator board) and the - test lead to test point, TP6161 (located on the Phase Lock Loop board, A11).

c. ADJUST—the MAIN OSC FREQ control (R3121), located on the Oscillator board, for a digital readout of −4.00 Vdc.

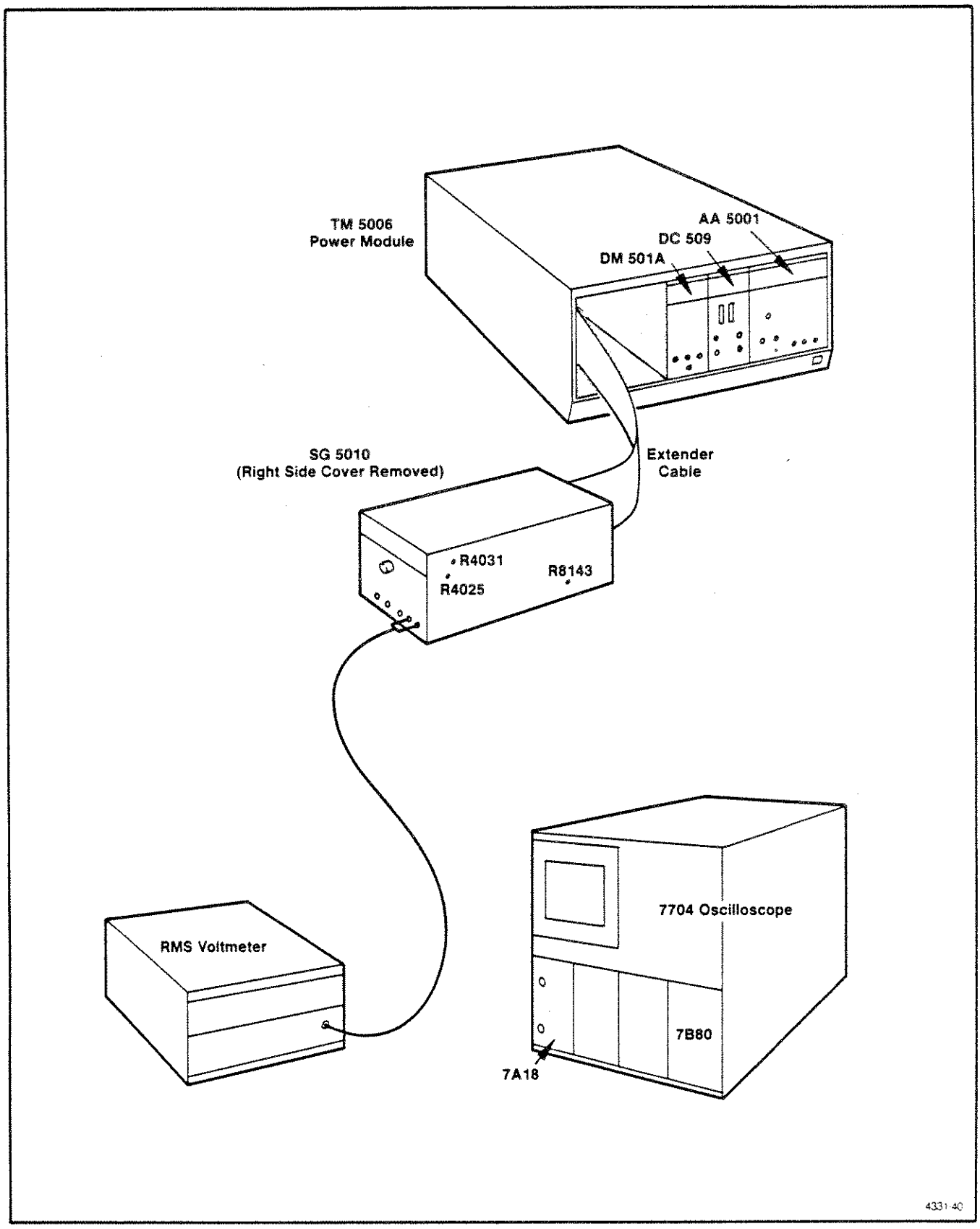


Fig. 6-1. Adjustment setup for SINE, BAL, SIMPTE CAL, SQ WAVE CAL, and CCIF CAL control adjustments.

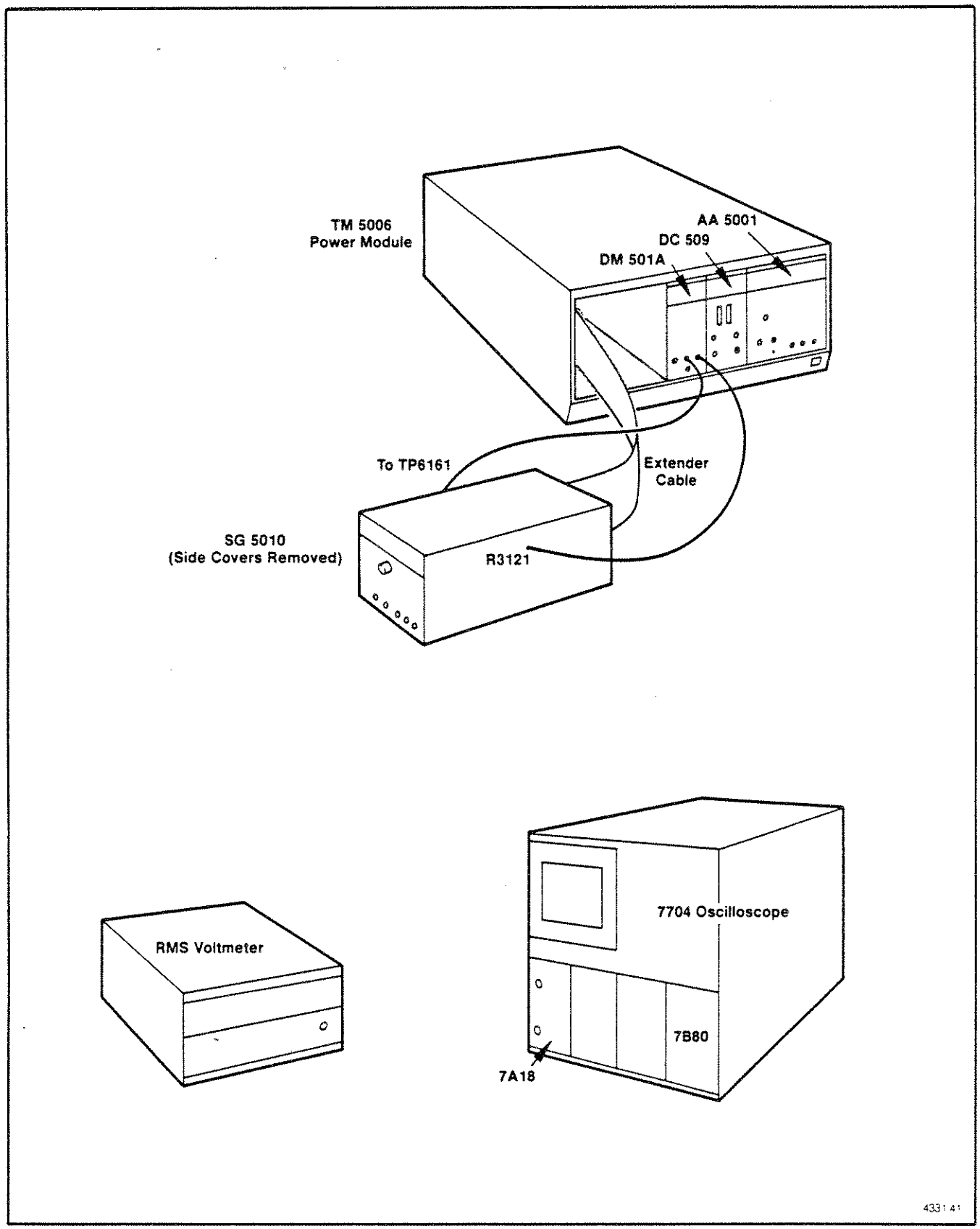


Fig. 6-2. Adjustment setup for MAIN OSC FREQ control.

d. Remove all cable connections.

4. IM OSC FREQ Adjust

Refer to Adjustment setup in Fig. 6-3.

Change the SG 5010 FUNCTION to SIMPTE/DIN and set the IM FREQ to 50 Hz.

Digital Counter Settings

FREQ	A
COUPL	DC
AVGS	AUTO

a. Connect the test cable from the SG 5010 SYNC OUT connector to the digital counter Input connectors.

b. ADJUST—the IM OSC FREQ control (R7021), located on the Oscillator board, for a counter reading of 50 Hz.

c. Disconnect all cable connections.

5. SMPTE CAL Adjust

Refer to Adjustment setup in Fig. 6-1.

a. Connect the test cable from the SG 5010 OUTPUT connectors to the rms voltmeter Input.

b. ADJUST—the SMPTE CAL control (R4025), located on the Oscillator board, for a voltmeter reading of 0.7071 V.

6. SQ WAVE CAL Adjust

Refer to Adjustment setup in Fig. 6-1.

a. ADJUST—the SQ WAVE CAL control (R8143), located on the Oscillator board, for a voltmeter reading of 1.4142 V.

7. CCIF CAL Adjust

Refer to Adjustment setup in Fig. 6-1.

a. Change the SG 5010 IM FREQ to 10 kHz.

b. ADJUST—the CCIF CAL control (R4031), located on the Oscillator board, for a voltmeter reading of 0.7071 V.

c. Remove all cable connections.

8. CCIF DISTO Adjust

Refer to Adjustment setup in Fig. 6-4.

Distortion Analyzer Settings

INPUT RANGE	AUTO RANGE
FUNCTION	IMD
DISTORTION RANGE	AUTO RANGE
RESPONSE	RMS
FILTERS	400 Hz

a. Change the SG 5010 IM FREQ to 500 Hz; FREQ to 10 kHz; and the FUNCTION to CCIF.

b. Connect the test cable from the SG 5010 OUTPUT (− and +) connectors to the distortion analyzer Input.

c. ADJUST—the CCIF DISTO control (R4033), located on the Oscillator board for minimum displayed readout on the distortion analyzer.

d. Disconnect all cable connections.

9. 10 Hz THD Adjust

Refer to Adjustment setup in Fig. 6-5.

a. Change the SG 5010 FREQ to 10 Hz and set the FUNCTION to SINE.

b. Set the oscilloscope system for 5 mv/div period and AC coupled.

c. Connect a test cable with X1 probe from the oscilloscope vertical plug-in Input connector.

On the Oscillator board, connect the + probe lead to test point TP5111 and the probe ground lead to COM testpoint, TP3183.

d. ADJUST—the 10 Hz THD control (R3141), located on the Oscillator board, for minimum ripple on the crt display. (This adjustment will be at the end of the potentiometer rotation, in most instruments.)

e. Remove all connections.

This completes the Adjustment Procedure.

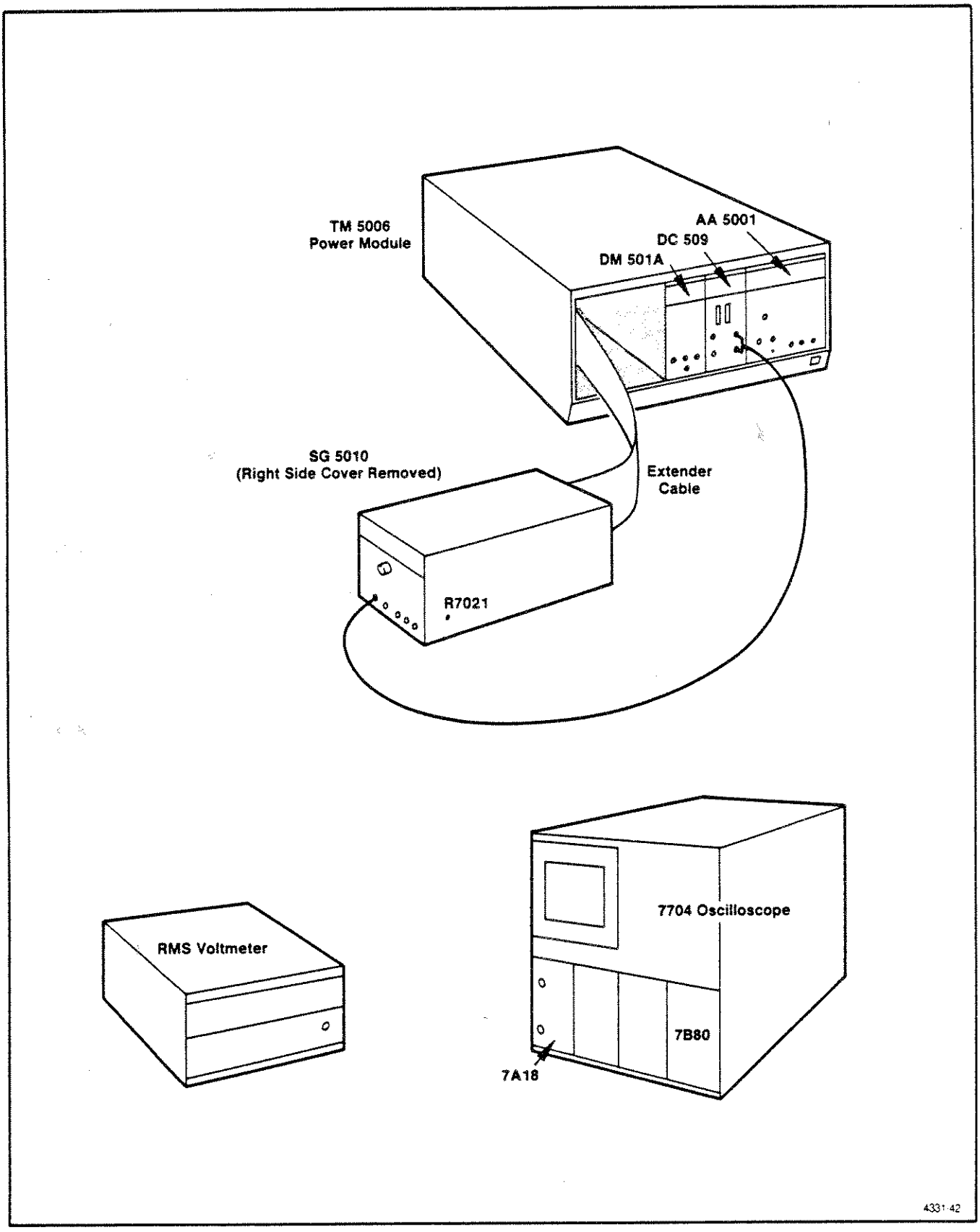


Fig. 6-3. Adjustment setup for IM OSC FREQ control.

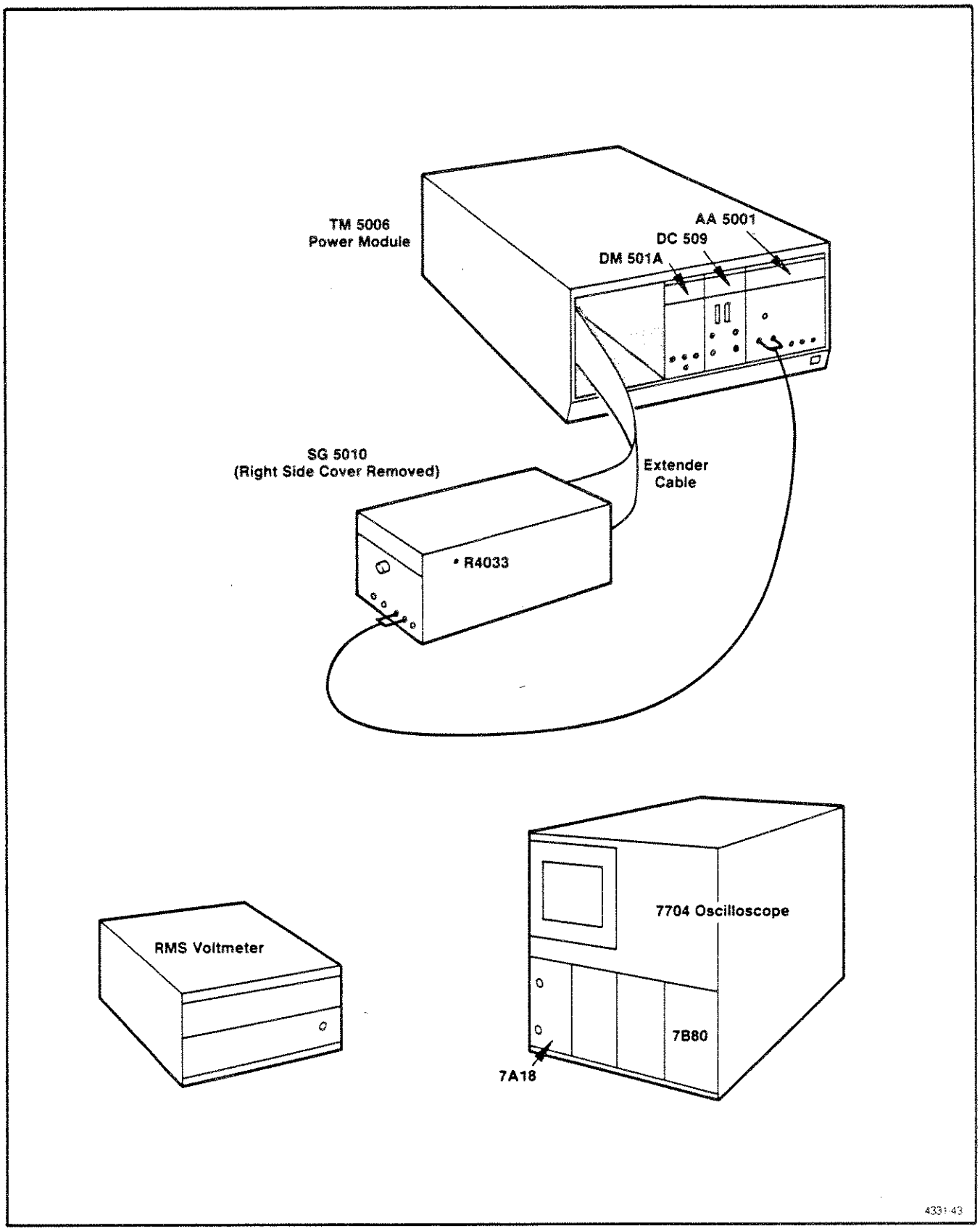


Fig. 6-4. Adjustment setup for CCIF DISTO control.

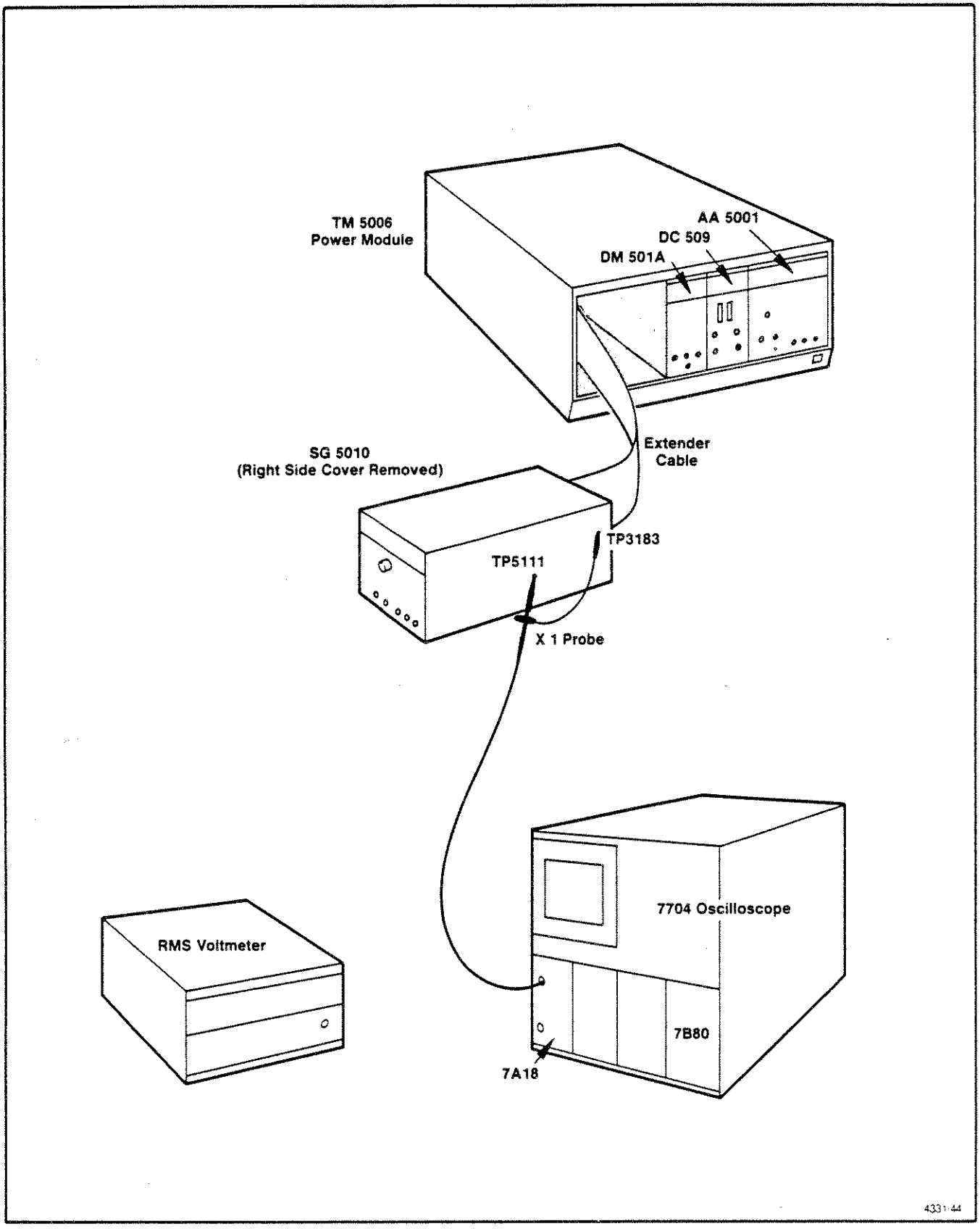
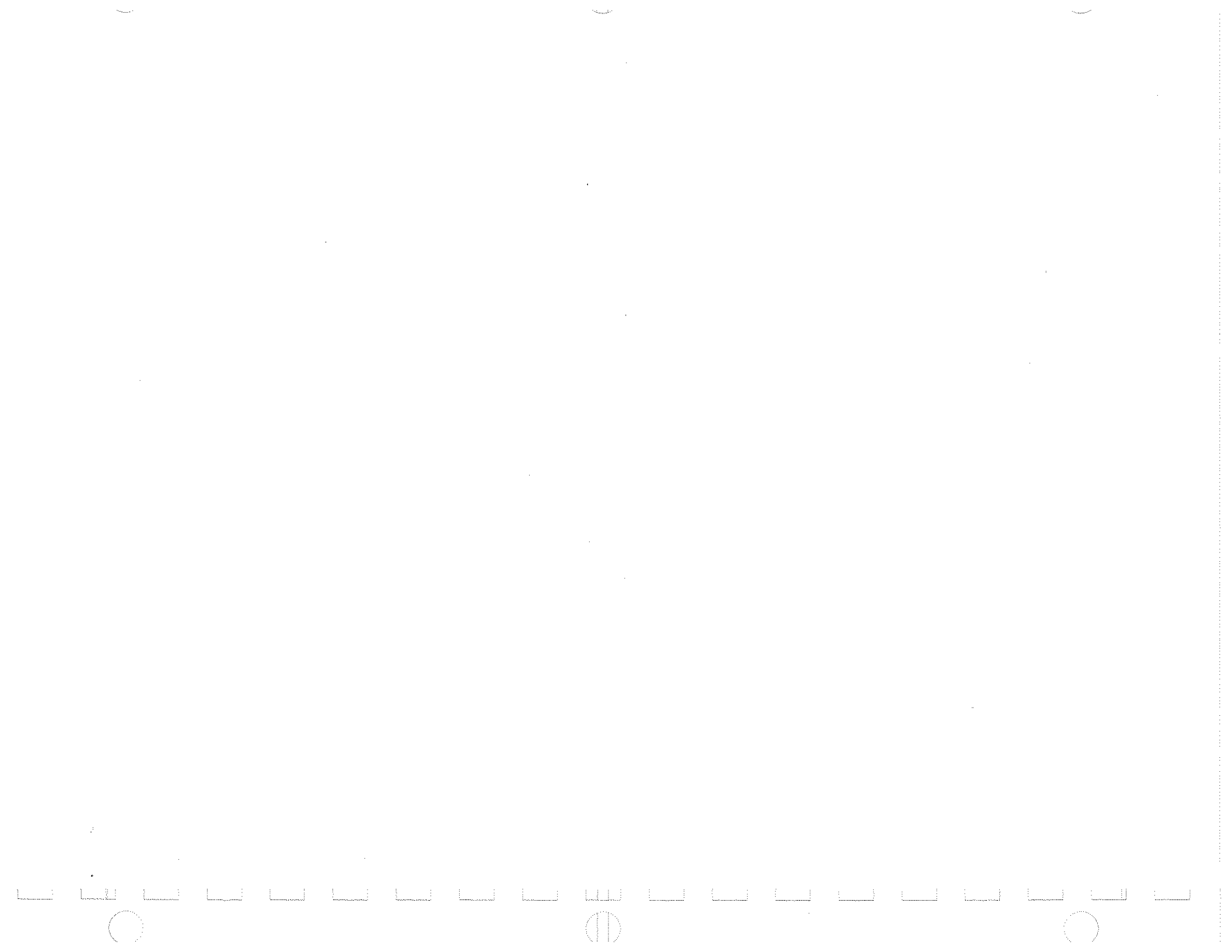


Fig. 6-5. Adjustment setup for 10 Hz THD control.



MAINTENANCE

Introduction

This section of the manual describes on-board jumpers and rear interface information and provides general maintenance and troubleshooting information.

CAUTION

To prevent damage to the SG 5010, turn off the power module before installing or removing the instrument. Do not use excessive force to install or remove.

Preparation for Use

On-board Jumpers

Refer to the Parts Location Grids located in the pull-out pages of this manual.

Front Panel board:

J3050 Self Test—Used to place SG 5010 into continuous self test mode.

Phase Lock Loop board:

J3071 μCom—AA 5001/SG 5010 serial interface. Used to enable or disable communication between the SG 5010 and AA 5001 during sweep mode.

J6161 Internal/External Reference—Used to select between internal and external 1 MHz reference frequencies.

CPU board:

J2070 1 ms Timer Disconnect—Used to disable 1 ms timer during signature analysis and forced instruction mode test.

J2071 SA/NORM—Used to enable signature analysis routines internal to SG 5010 in conjunction with J2070 and J3050.

J3050 Memory Ready Disconnect—Used to disconnect display driver memory stretch during signature analysis and forced instruction mode test.

R4040 Forced Instruction Mode Test—Used to initiate forced instruction mode test in conjunction with J3050 and J2070.

Output board:

J4022 SA/NORM—Used to translate floating circuitry to appropriate voltage level for the signature analyzer input.

Operation In TM 500-Series Power Module

Refer to CIRCUIT BOARD REMOVAL in this section, for the following. To operate the SG 5010 in a TM 500-Series Power Module, it is necessary to make the following modifications:

1. Remove the instrument left side cover.
2. Remove the four screws retaining the phase lock loop board.
3. Move the phase lock loop board until the second set of mounting holes lines up with the stand-off hex screws.
4. Replace the phase lock loop board screws (4).
5. Remove the back cover.
6. Remove the two mechanical lock-outs from the top and bottom rails.
7. Replace the back cover.
8. Replace the left side cover.

NOTE

The maximum operating temperature in TM 500-Series Power Modules should be restricted to +40° C.

REAR INTERFACE INFORMATION

Refer to Fig. 7-1 for the CPU board assignments and Fig. 7-2 for the GPIB assignments.

MAIN OUT HI (pin 28A); MAIN OUT LO (pin 27A)—The Optional Rear Output on-board pin locations (located on the CPU and Output boards) allow qualified technical personnel to connect the analog + (**HI**) and the − (**LO**) output signals to the rear interface connector as follows.

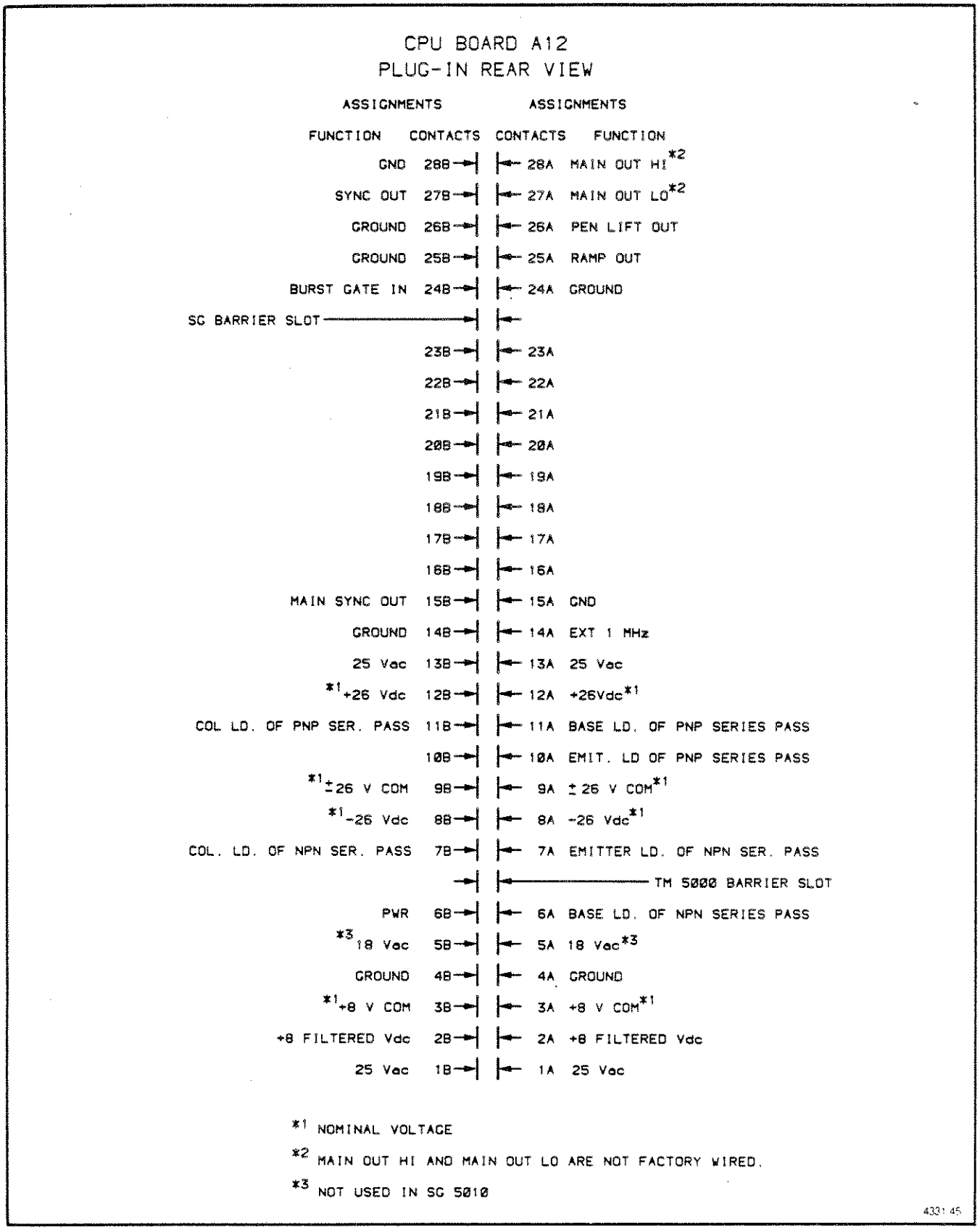


Fig. 7-1. CPU board rear interface connector assignments.

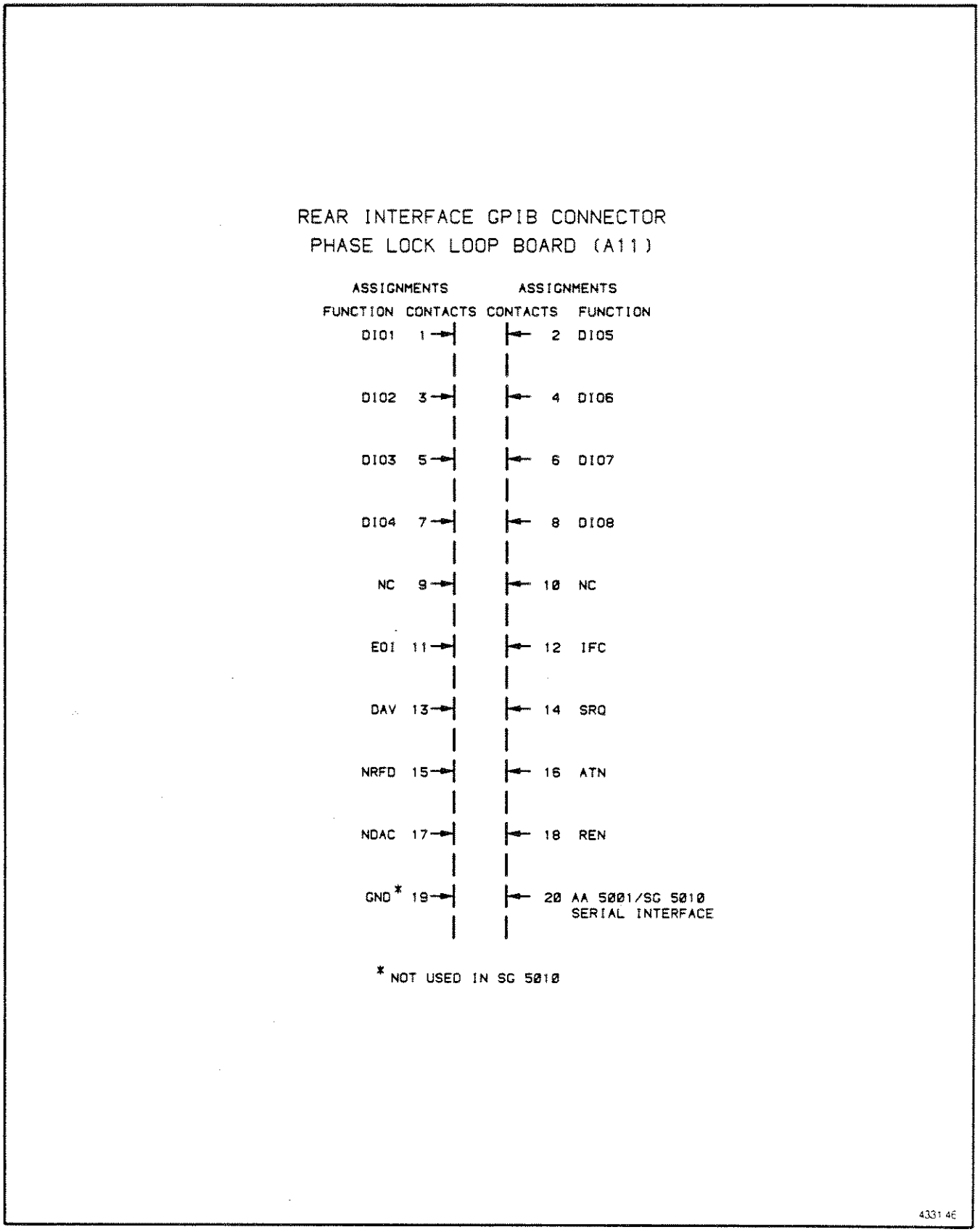


Fig. 7-2. GPIB board rear interface connector assignments.

NOTE

Refer to the Circuit Board Removal instructions in this section, and the Parts Location Grids, located in the pullout pages of this manual.

a. Solder three connector pins (Tektronix Part No. 131-1426-00) to the three circuit board holes (J1020) located on the non-component side of the CPU board, facing the pins *DOWN*.

b. Solder three connector pins (same part as above) to the three circuit board holes (J4012) located on the non-component side of the Output board, facing the pins *UP*.

c. Attach the cable assembly (Tektronix Part No. 175-7848-00) to these pins (J1020 and J4012), routing this cable between the transformer and circuit board.

NOTE

These rear interface connected signals may cause distortion or noise due to crosstalk with existing signals.

SYNC OUT (Pin 27B)—This output signal pin wired in parallel with the front panel SYNC OUT connector is used as an external trigger for a counter, oscilloscope, or other device. With a source impedance of 1 kΩ, this signal is referenced to chassis ground.

PEN LIFT OUT (pin 26A)—This TTL output signal pin is wired parallel with the front panel PEN LIFT connector. It can be used to blank the display or lift the pen.

RAMP OUT (pin 25A)—This staircase ramp output voltage pin is wired in parallel with the front panel RAMP OUT connector.

BURST GATE IN (pin 24B)—A TTL trigger input signal pin that is wired in parallel with the front panel BURST GATE connector.

MAIN OSC SYNC OUT (pin 15B)—A user option TTL sync output signal (from the internal phaselock drive circuit).

EXT 1 MHz (pin 14A)—This input signal pin can be used in conjunction with on-board jumper P6161 (located on the Phaselock Loop board). An external 1 MHz signal can be connected to the internal phaselock circuit when the jumper is set (by qualified technical personnel) to the E (external) position.

GENERAL MAINTENANCE

Battery Replacement

Stored setups and the current contents of the SG 5010 front panel buffer will be lost when the battery is removed. To avoid this, copy the contents of the stored setup and reenter them into the instrument upon completion of the replacement.

Battery Handling and Disposal

WARNING

To avoid personal injury, observe proper procedures for handling and disposal of lithium battery. Improper handling may cause fire, explosion, or severe burns. Do not recharge, crush, disassemble, heat above 212° F (100° C), incinerate, or expose contents of battery to water. Dispose of battery in accordance with local, regional, and national regulations.

Crystal

CAUTION

When replacing the crystal, note solder point on crystal can. Do not solder on narrow side of crystal. Solder only on the wide side of the can, to avoid damaging the soldered vacuum seal of the crystal.

Troubleshooting Aids

Diagrams. Complete circuit diagrams are located in the pullout pages in the Diagrams and Circuit Board Illustrations Section of this manual. The portions of the circuit mounted on the circuit boards is enclosed by a solid line. The circuit number of each component in this instrument is shown on a diagram. See the first page of the Diagrams and Circuit Board Illustrations section for definitions of the symbols and reference designators used on the diagrams.

Circuit Board Illustrations. Circuit board illustrations are provided in conjunction with the circuit diagrams. Each board-mounted component shown on a diagram is also identified on the circuit board illustration by circuit number. A table is provided with each diagram, listing components by assembly and circuit number. The table also lists the component grid locations on both the associated diagram and the circuit board illustration.

Calibration Fixtures

Several calibration fixtures are available from Tektronix, Inc. that are helpful in troubleshooting the SG 5010.

067-0938-00 Notch Filter
067-0645-02 Plug-in Extender
067-0996-00 GPIB Extender

Contact your nearest Tektronix, Inc. Field Office or representative for ordering information.

Troubleshooting Equipment

Before using any test equipment to make measurements on static-sensitive components or assemblies, be certain that any voltage or current supplied by the test equipment does not exceed the limits of the component to be tested.

Static-Sensitive Components

CAUTION

Static discharge can damage any semiconductor component in this instrument.

This instrument contains electrical components that are susceptible to damage from static discharge. See Table 7-1 for relative susceptibility of various classes of semiconductors. Static voltages of 1 kV to 30 kV are common in unprotected environments.

Observe the following precautions to avoid damage:

1. Minimize handling of static-sensitive components.

2. Transport and store static-sensitive components or assemblies in their original containers, on a metal rail, or on conductive foam. Label any package that contains static-sensitive assemblies or components.

3. Discharge the static voltage from your body by wearing a wrist strap while handling these components. Servicing static-sensitive assemblies or components should be performed only at a static-free work station by qualified service personnel.

4. Nothing capable of generating or holding a static charge should be allowed on the work station surface.

5. Keep the component leads shorted together whenever possible.

6. Pick up components by the body, never by the leads.

7. Do not slide the components over any surface.

8. Avoid handling components in areas that have a floor or work surface covering capable of generating a static charge.

9. Use a soldering iron that is connected to earth ground.

10. Use only special antistatic suction type or wick type desoldering tools.

Table 7-1
RELATIVE SUSCEPTIBILITY TO STATIC DISCHARGE DAMAGE

Semiconductor Classes	Relative Susceptibility Levels*
MOS or CMOS microcircuits or discretes, or linear microcircuits with MOS inputs. (Most Sensitive)	1
ECL	2
Schottky signal diodes	3
Schottky TTL	4
High-frequency bipolar transistors	5
JFETs	6
Linear microcircuits	7
Low-power Schottky TTL	8
TTL (Least Sensitive)	9

***Voltage equivalent for levels:**

1 = 100 to 500 V 4 = 500 V 7 = 400 to 1000 V(est.)
2 = 200 to 500 V 5 = 400 to 600 V 8 = 900 V
3 = 250 V 6 = 600 to 800 V 9 = 1200 V

(Voltage discharged from a 100 pF capacitor through a resistance of 100 Ω.)

Obtaining Replacement Parts

Electrical and mechanical parts can be obtained through your local Tektronix Field Office or representative. However, it may be possible to obtain many of the standard electronic components from a local commercial source. Before purchasing or ordering a part from a source other than Tektronix, Inc., check the Replaceable Electrical Parts list for the proper value, rating, tolerance, and description.

NOTE

When selecting replacement parts, remember that the physical size and shape of a component may affect its performance in the instrument.

Some parts are manufactured or selected by Tektronix, Inc. to satisfy particular requirements or are manufactured for Tektronix, Inc., to our specifications. Most of the mechanical parts used in this instrument have been manufactured by Tektronix, Inc. To determine the manufacturer, refer to the replaceable parts lists and the Cross Reference Index, Mfr. Code Number to Manufacturer.

When ordering replacement parts from Tektronix, Inc., include the following information:

1. Instrument type (include modification or option number).

2. Instrument serial number.

3. A description of the part (if electrical, include complete circuit number).

4. Tektronix part number.

CIRCUIT BOARD REMOVAL

Qualified service personnel will find the SG 5010 instrument cover and board removal quite simple using the following procedure. Refer to Fig. 7-3.

1. Side, Top, and Back Covers Removal

a. Remove the two side covers (four 1/4 turn fasteners).

NOTE

Top and Back Covers are removed as a single unit.

b. Remove the top cover screws (5).

c. Remove the back cover 3/16″ hex. bullet connectors (2).

d. Carefully pull the covers up and back to remove.

2. Phaselock Loop Board (A11) Removal.

a. Remove the side, top, and back covers.

b. Remove the screws (4) that secure the Phaselock Loop board to the CPU board (A12).

c. Disconnect the ribbon connector, J2100 and remove board.

NOTE

For troubleshooting purposes, do not remove this connector. The board can swing back (towards the front panel), for servicing.

3. Oscillator Board (A14) Removal

a. Remove the side, top, and back covers.

b. Remove the screws (4) that connect to the Output board (A13).

c. Disconnect the on-board ribbon connector, J7121 that attaches to the Output board and the coax cable harmonic connector, J5141 and remove the Oscillator board.

NOTE

For troubleshooting purposes, the ribbon cable attaching the two boards can be reversed end-for-end (noting the pin number configuration), and the board can be positioned on its side. Be sure to return the cable to its original connections, upon re-assembly.

d. The oscillator board shield can be detached by removing the screws (3), as shown in Fig. 7-4.

4. Output Board (A13) Removal

a. Remove the side, top, and back covers.

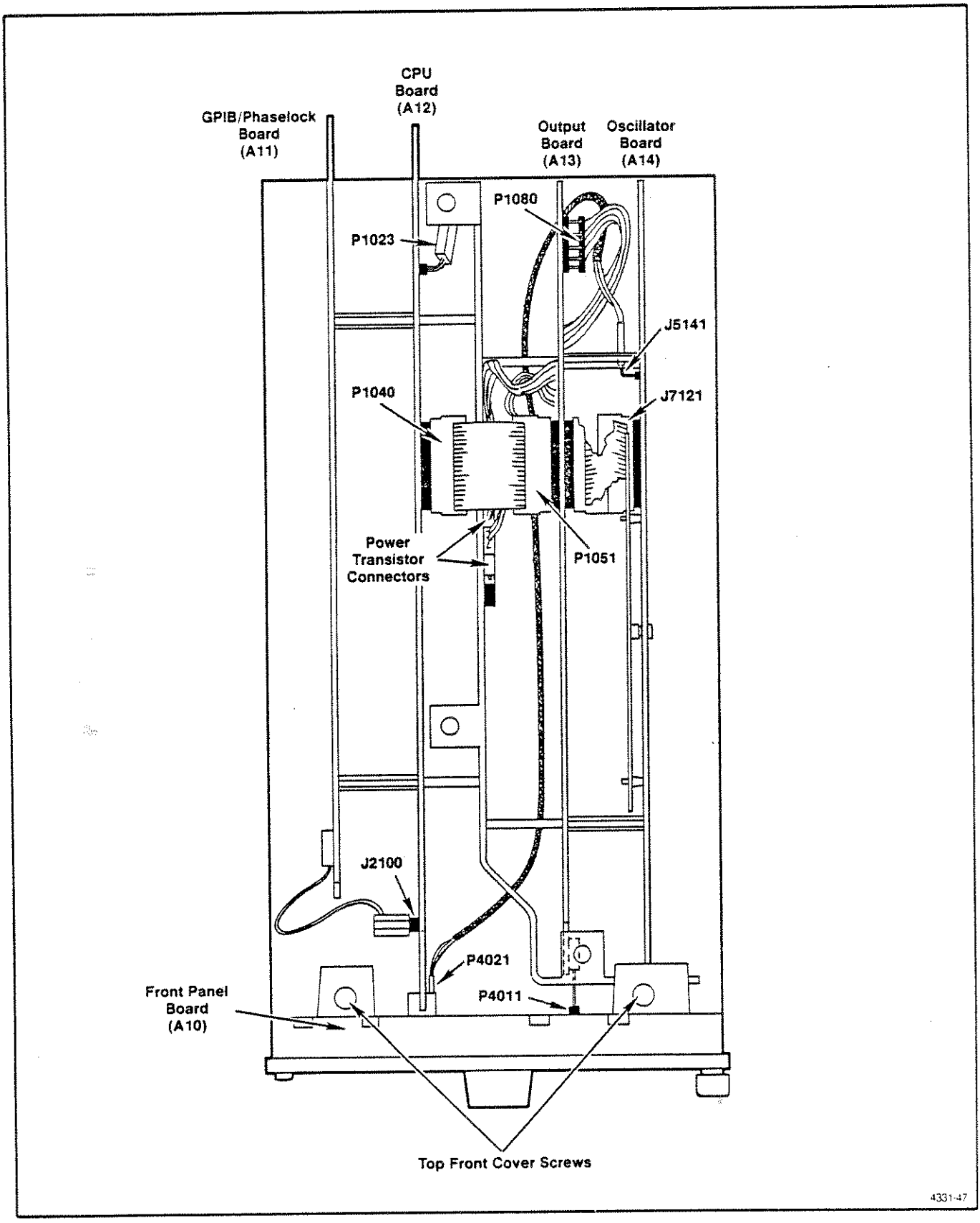


Fig. 7-3. Circuit board and connectors pictorial (top view).

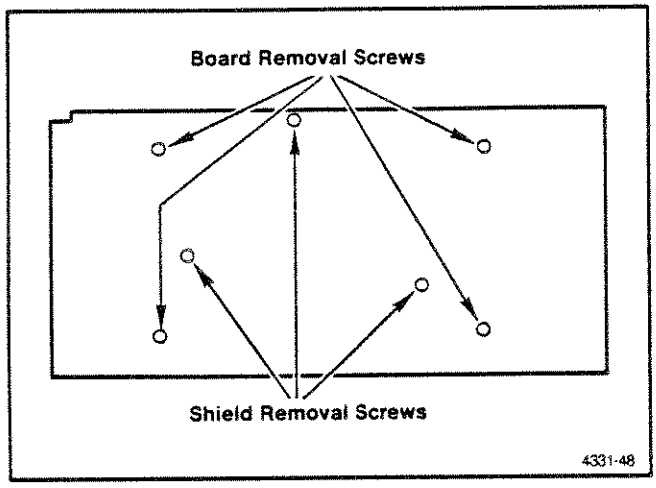


Fig. 7-4. Oscillator board pictorial (right side view).

b. Remove the Oscillator board.

c. Remove the stand-off hex screws (4).

d. Disconnect the transformer connector, P1080.

e. Disconnect the interconnect plug, P1051.

f. Remove the power transistor connectors (2). Note their locations, for re-assembly; the front cable connects to the front transistor.

g. Carefully slide the board back, making certain not to stress or bend the interconnecting pins (P4011) that attach to the front panel board.

5. Transformer Removal

a. Remove the side, top, and back covers.

b. Remove the Oscillator board.

c. Remove the transformer connector (P1080) from the Output board.

d. Disconnect the 3-pin harmonic connector (P1023), from the CPU board.

e. Remove the transformer bracket screws (4), as shown in Fig. 7-5.

f. Carefully pull out the transformer.

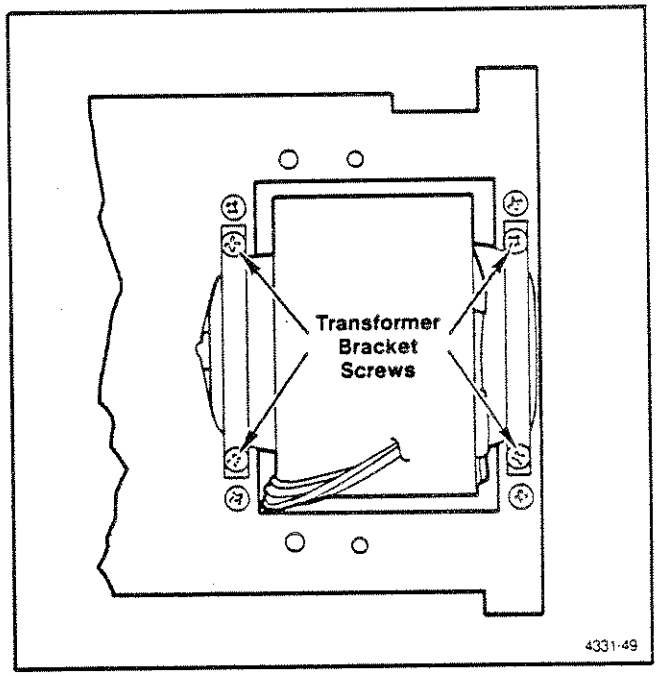


Fig. 7-5. Transformer and bracket (partial pictorial).

6. CPU Board (A12) Removal

a. Remove the side, top, and back covers.

b. Remove the Phaselock Loop board.

c. Remove the stand-off hex screws (4).

d. Remove the 3-pin harmonic connector (P1023).

e. Disconnect the 20-pin ribbon interconnect cable (P1040).

f. Slide board back for removal.

7. Front Panel Assembly Removal

a. Remove side covers (not necessary to remove the top and back covers).

b. Remove the front cover screws (2).

c. Remove the latch assembly using the following procedure (refer to Fig. 7-6):

Use a small screwdriver to push forward slightly on the rear latch (1) just in front of the spring. Press down on the latch knob to raise the latch knob extension at the point where the two latch pieces engage. While holding the latch knob down, push up on the front panel latch piece at the point of engagement (2) to disengage the two pieces. Then, pull the latch knob out.

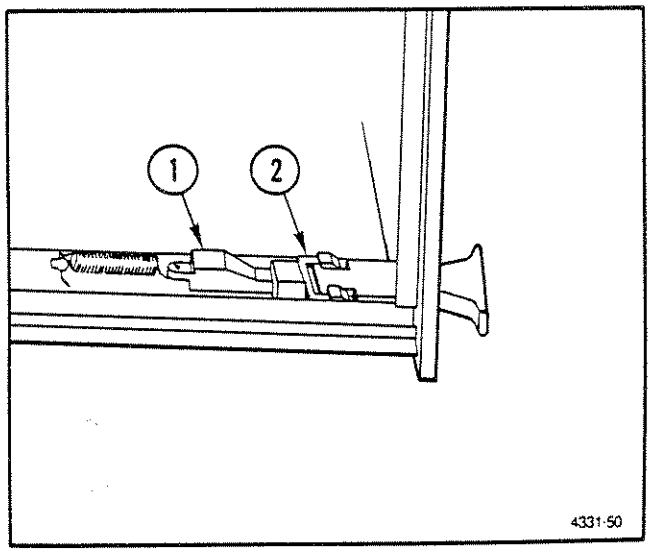


Fig. 7-6. Latch assembly pictorial.

CAUTION

Do not install the plug-in in the power module while the latch is disassembled. Removal of the plug-in without use of the latch can be extremely difficult.

d. Remove the bottom front panel screws (one being the ground lug).

e. Carefully pull front panel away from frame being certain to disconnect the 3-pin harmonic connector (P4021) from the board.

8. Front Panel Board (A10) Removal

Refer to Fig. 7-7 for the following:

a. Remove front panel board assembly.

b. Remove the front panel control knob.

c. Remove the board screws (6).

d. Unsolder the five solder points.

e. Unsolder the coax connector wires.

f. Remove the front panel banana jacks (3).

g. Carefully lift out board.

Soldering Techniques

WARNING

To avoid electric-shock hazard, disconnect the instrument from the power source before soldering.

The reliability and accuracy of this instrument can be maintained only if proper soldering techniques are used when repairing or replacing parts. General soldering techniques, which apply to maintenance of any precision electronic equipment, should be used when working on this instrument. Use only 60/40 rosin-core, electronic grade solder. The choice of soldering iron is determined by the repair to be made.

CAUTION

The Oscillator, Output, and CPU boards are multilayer-type boards with a conductive path laminated between the top and bottom board layers. All soldering on these boards should be done with extreme care to prevent breaking the connections to this conductive path.

Do not allow solder or solder flux to flow under printed circuit board switches. The printed circuit board is part of the switch contacts; intermittent switch operation can occur if the contacts are contaminated.

When soldering on circuit boards or small wiring, use only a 15 watt, pencil-type soldering iron. A high wattage soldering iron can cause the etched circuit wiring to separate from the board base material and melt the insulation from small wiring. Always keep the soldering iron tip prop-

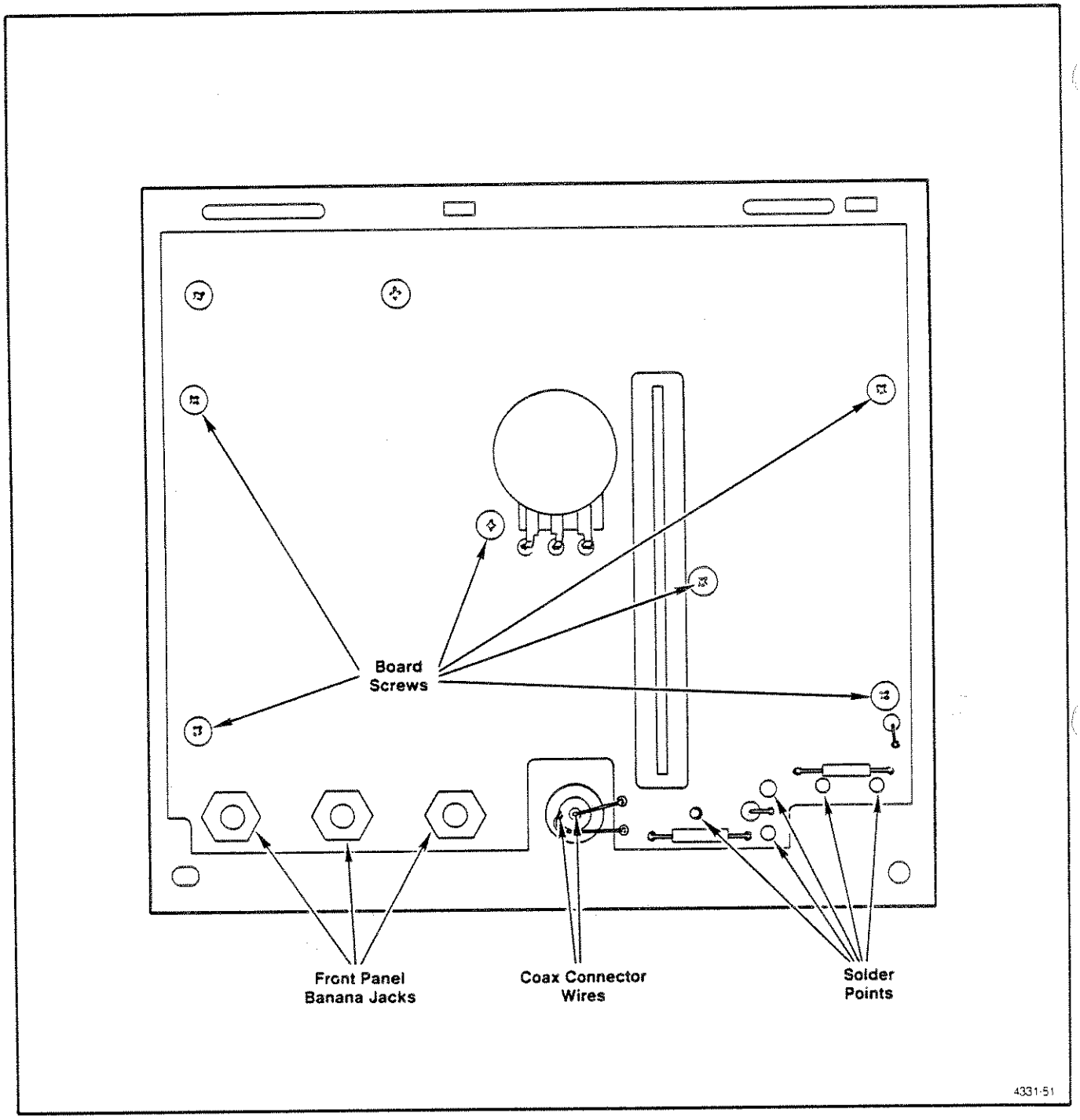


Fig. 7-7. Front panel board pictorial (rear view).

erly tinned to ensure the best heat transfer to the solder joint. Apply only enough heat to remove the component or to make a good solder joint. To protect heat-sensitive components, hold the component lead with a pair of long-nose pliers between the component body and the solder joint. Use a solder removing wick to remove excess solder from connections or to clean circuit board pads.

Semiconductors

To remove in-line integrated circuits mounted in sockets, use an extracting tool. This tool is available from Tektronix, Inc.; order Tektronix Part No. 003-0619-00. If an extracting tool is not available, use care to avoid damaging the pins. Pull slowly and evenly on both ends of the integrated circuit. Try to avoid disengaging one end before the other end.

Exterior Cleaning

Chassis. Accumulated dust on the instrument chassis can be removed with a soft cloth or small brush. Remove dirt that remains with a soft cloth dampened in a mild detergent and water solution; then remove the detergent with a cloth dampened in clean water. Do not use abrasive cleaners.

Front Panel. Use only a cotton swab or soft cloth, dampened in isopropyl alcohol or water.

CAUTION

To avoid damage, use only isopropyl alcohol or water. Do not use petroleum based agents. Before using a cleaner other than isopropyl alcohol, consult your Tektronix Service Center or representative for information.

Interior Cleaning

Clean circuit boards only when required for operation to specified performance. Dust in the interior of the instrument should be removed occasionally due to its electrical conductivity under high humidity conditions. The best way to clean the interior is to blow off the accumulated dust with dry, low pressure air. Then use a soft brush.

Isopropyl alcohol can be used to clean major repairs to the circuit board; however, flush the board well with clean, isopropyl alcohol. Make certain that resin or dirt is carefully removed from board areas of high impedance circuitry.

TROUBLESHOOTING INFORMATION

Introduction

Troubleshooting information for the SG 5010 includes hardware tests, troubleshooting flow charts, and signature analysis for selected digital circuits. This information is located in the pullout pages of this manual.

If an error code is either displayed on the instrument front panel or returned to the controller in response to an ERR? query, refer to the error code definitions in the Programming section of this manual. The only error codes that indicates instrument malfunction are those classified as Internal Errors in the error code list. The displayed error code 521 indicates that one of the signature analysis jumpers is enabled.

HARDWARE TESTS

The hardware is tested by the SG 5010 firmware in two ways:

1. The Power-on Self Tests
2. The Test Query

These methods use the same set of basic hardware tests. The hardware tested and the specific tests are briefly described under "SG 5010 Self Tests".

Power-on Self Tests

The power-on self tests run each hardware test once. If an error occurs, the corresponding position in the error histogram (see Fig. 7-8) is set to one. After all tests are completed and one or more tests have failed, the SG 5010 display is set to the code of the first error detected. To display additional error codes, if any, the ENTER button is pressed. If the last code generated is in the display and the ENTER button is pressed, the display fills with blanks. This feature indicates all errors have been displayed. To display the error codes again, the ENTER button is pressed.

The CLEAR key is pressed to continue the power-on sequence. After the CLEAR key is pressed, the SG 5010 completes its initialization, then reports any errors that occurred over the GPIB. The power-on sequence takes approximately three seconds.

The flow diagram (error histogram) in Fig. 7-8 illustrates the power-on error reporting procedure.

The Test Query

The second test method is the TEST? (TEST query). TEST? is sent to the SG 5010 over the GPIB. When received, the SG 5010 will:

1. Save the current state of the machine.
2. Turn on all front panel LEDs.
3. Set up and commence self testing.
4. Create a histogram of error codes from the self tests.
5. Report the errors, if any, in the form:

   TEST <num>,<num>,...,<num>;

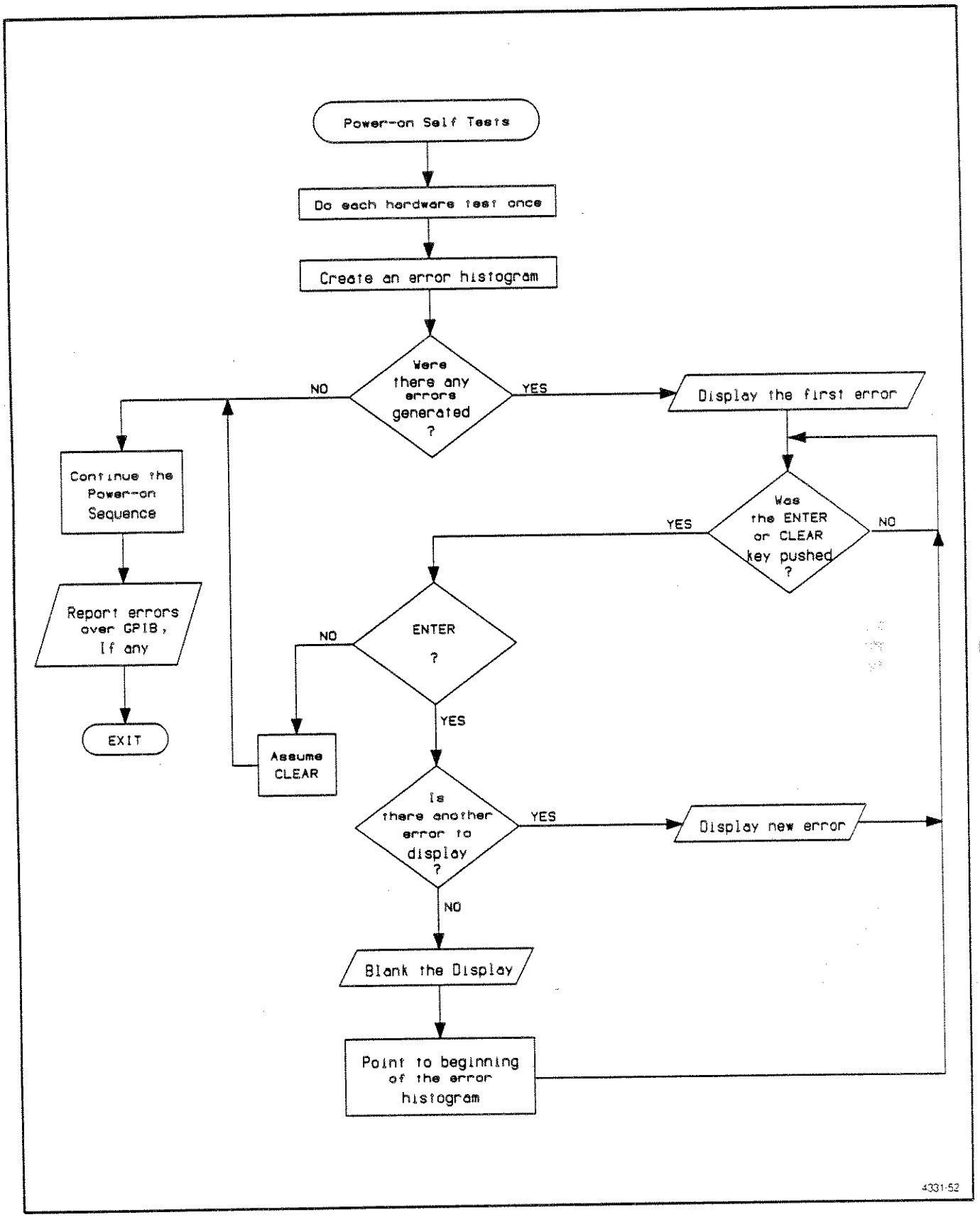


Fig. 7-8. Power-on Self Test flow diagram.

where each <num> is an error code corresponding to an error condition detected by the self tests. If no errors are detected, the response is:

TEST 0

6. The error histogram is reset.

7. The SG 5010 is returned to its settings prior to the TEST? execution.

SG 5010 SELF TESTS

Introduction

Two signals are the primary tools used to test the hardware. These signals are the Timer Interrupt signal occurring once every 1 ms, and the Sync Wave signal which differs for the various function modes. Also, the current limit, phase lock loop, and analog power supply each have accessible test points in the microprocessor section of the SG 5010.

The Basic Algorithm

The SG 5010 is set to the desired test parameters and the hardware is allowed time to settle. Since the sync wave will run at different frequencies for the various tests, a new sync wave count (for timing purposes) will be calculated for each test. The test lasts approximately 100 ms, so that the timer interrupts can be counted effectively. After the new sync count is set, the actual test begins. On the next positive transition of the sync pulse, the timer interrupt bit is reset. Then, two nested loops are entered. The outer loop counts the preset number of sync pulses and the inner loop counts timer interrupts. After the preset number of sync pulses have passed, the next part of the test is entered. The timer interrupt count, which is approximately 100, is compared with 100. If the two numbers are within 20% of each other, the test passes and the next test begins.

Error Handling

Each segment of hardware to be tested has its own error code. In the SG 5010 RAM space, there is an array that is used by the self test as a histogram of error occurrances. One location in the array is used for each self test error code. If a specific test fails, the proper location corresponding to that test's error code (in the histogram) will be incremented by one. The hardware test errors are divided into two types, fatal and non-fatal. When a fatal type test fails, the proper histogram location is incremented and the remaining hardware tests stop (self test sequence aborted). If an error is generated by a non-fatal type test, the histogram increments and the self test procedure continues.

Reporting the data from the error histogram will be different for each of the parent routines that uses the hardware self tests. The parent routines are Power-on Self Tests, and TEST?.

Error Codes (Internal) and Definitions

301	Interrupt fault
302	System error
309	Output overloaded
310	Analog power supply error
315	Phase lock error
319	Current limit error
320	Sine wave oscillator error
321	Oscillator 1 k band error
322	Oscillator 10 k band error
323	Oscillator 100 k band error
324	Square wave generator error
325	Burst generator error
326	Burst LO byte counter error
327	Burst HI byte counter error
328	Burst gate line asserted error
329	Burst gate line unasserted error
330	40 Hz IM Freq error
331	50 Hz IM Freq error
332	60 Hz IM Freq error
333	80 Hz IM Freq error
334	100 Hz IM Freq error
335	125 Hz IM Freq error
336	250 Hz IM Freq error
337	500 Hz IM Freq error
340	System RAM failure
348	GPIB address setting cell error
349	Power-up stored settings cell error
350	Stored settings cell 0 error
351	Stored settings cell 1 error
352	Stored settings cell 2 error
353	Stored settings cell 3 error
354	Stored settings cell 4 error
355	Stored settings cell 5 error
356	Stored settings cell 6 error
357	Stored settings cell 7 error
358	Stored settings cell 8 error
359	Stored settings cell 9 error
368	8000 ROM placement error
372	C000 ROM placement error
388	8000 ROM checksum error
392	C000 ROM checksum error

Hardware Tested (with error code returns):

1. Analog Power Supply
2. Sine Wave and 100 Hz Oscillator Frequency
3. Oscillator at 1000 Hz
4. Oscillator at 10 kHz
5. Square Wave Generator
6. Burst Mode, Continuous
7. Low Burst Counter
8. 100 kHz Oscillator Band
9. High Burst Counter
10. Burst Gate—Line Test
11. Current Limit Test
12. All 8 IM frequencies
13. Phase Lock Loop

Analog Power Supply

The analog power supply is checked 10 times, using a hard-wired test line. This test takes 10 ms; one check of the power every 1 ms. If no analog power is present during any two or more of the ten checks, the test fails. This test failure causes instrument failure. This is a fatal error.

Displayed error code, ERR 310

CHECK:

- Fuses—F2020 and F2022, located on the CPU board (A12)
- Transformer, T300 and connections
- U1060, located on the Output board, A13
- Q106, Q107, and wiring located on the chassis
- U2046, located on the CPU board

Sine Wave Oscillator at 100 Hz, 1000 Hz, and 10 kHz

The basic algorithm, outlined earlier, is used to test each of the lower oscillator frequency bands. It is a fatal error, if any of the oscillator frequency bands fail to operate. The sync wave and the oscillator are at the same frequency while the SG 5010 is in sine mode.

The following checks are on the Oscillator board, A14 (main oscillator circuit), unless otherwise noted.

Displayed error code, ERR 320 (100 Hz)

CHECK:

- U4121, U5091, U5081, U8081, U8071, and U8061
- U5151, speedup circuit
- U2171 and U2181
- FETs—Q4093, Q4091, Q4073, and Q4081
- U3062B, 1 ms timer located on the CPU board (A12)
- Capacitors—C2091 and C2081

Displayed error code ERR 321 (1000 Hz)

CHECK:

- FETs—Q4093, Q4091, Q4073, Q4081, Q4101, Q3091, Q3075, Q3073, and ICs—U8071 and U8061
- Capacitors—C2071 and C2093

Displayed error code, ERR 322 (10 kHz)

CHECK:

- FETs—Q3103, Q3101, Q3071, Q3061, Q4101, and Q3091
- U8071 and U8061
- Capacitors—C2101 and C2063

Square Wave Generator

The test algorithm is used to check the square wave. The sync wave is 1/10th or 0.1 times the frequency of the oscillator. This test uses the 10 kHz frequency band which must be operational for this test to be valid.

Displayed error code, ERR 324

CHECK:

- U9151, located on the Oscillator board

Continuous Burst Mode

When setting the instrument to continuous burst mode, the function is set to burst and on and off cycles set to one (the low burst counter is not used during this test). The 10 kHz frequency band should be fully operational before this test is valid. The sync wave is equal to half the specified frequency, or 5000 Hz. In burst mode, the sync frequency is equal to one complete burst cycle (one time through the on and off cycles). A non-fatal error is generated if this test fails.

Displayed error code, ERR 325

CHECK:

- U8161 and U7151, located on the Oscillator board

Low Burst Counter

While the SG 5010 is in burst mode, the on and off cycles are each set to 5. The oscillator is still at 10 kHz, but the sync wave is now at 1000 Hz, because of the longer burst cycle. The basic algorithm is used. This test depends on the 10 kHz frequency band and the burst function being fully operational. A non-fatal error is generated, if the low counter develops operational problems.

Displayed error code, ERR 326

CHECK:

- U5161, U5171, and U5181 located on the Oscillator board

Oscillator 100 kHz Frequency Band

The SG 5010 function is set to squarewave (the square wave generator must be fully operational). The frequency is set to 100 kHz, but the square wave generator divides this frequency by 10 so the sync wave runs at 10 kHz, which can be tested. The general algorithm is used to check the sync wave. If any of the oscillator frequency ranges fail, it is treated as a fatal error.

Displayed error code, ERR 323

CHECK:

- Q3103, Q3101, Q3061, Q3071, C2111, C2061, and U8061 located on the Oscillator board

High Burst Counter

The on and off cycles are both set to 500. The frequency remains at 100 kHz, producing a 100 Hz sync wave. This test depends on the 100 kHz frequency band working properly. If this test fails, a non-fatal error occurs.

Displayed error code, ERR 327

CHECK:

- U7161, U7171, and U7181 located on the Oscillator board

Burst Gate-Line Test

The burst is put into trigger mode, and an external trigger is needed to drive the burst signal. The sync wave presence is checked. If there is a sync wave (should be none at this time) the burst gate-line failed. Next, the burst is put into continuous mode and the sync wave is checked again. This time, if the sync wave is not on (it should be), the test fails.

Displayed error code, ERR 328 or ERR 329

CHECK:

- U8161A and U7151 located on the Oscillator board
- U1030, U3070, U3050, U3052, U2080, and U2040 located on the CPU board

Current Limit

The current limit indicator LED is on when the SG 5010 is in sine wave function, 0 Hz frequency (dc), and Vrms is at maximum. The routine then enters a wait state (for 50 ms), so the hardware has time to settle. Then the current limit indicator is observed. If it is in current limit, the test has passed. If this test fails, a non-fatal error is generated.

Displayed error code, ERR 309

CHECK:

- U3031, U3051, U3032, U1022, and Q3022 located on the Output board

Phase Lock Loop

The SG 5010 function is changed to sine wave and the frequency is set to 100 Hz. This is the worst case for the phase lock loop. The IM frequencies are tested, then the phase lock loop line is checked to see if it locked. If not locked, the non-fatal error occurs.

Displayed error code, ERR 315

CHECK:

- U1121 located on the Oscillator board
- U5061, U5041, and U5131 located on the Phaselock Loop board

IM Frequencies

All of the IM frequencies are tested. The SG 5010 is put in CCIF mode, so the IM waves are accessible. Next, the routine steps through each IM frequency and tests them, with the basic algorithm. During this test, the sync wave is at the same frequency as the IM waveform. Each IM frequency has its own non-fatal error code.

Displayed error codes, ERR 330 through ERR 337

CHECK:

- IM Oscillator, located on the Oscillator board
- FETs in IM Oscillator
- Q7021 and Q7031 (ERR 330, ERR 331, and ERR 332)
- Q7021, Q7031, Q9021, and Q9043 (ERR 336)
- Q9021 and Q9043 (ERR 337)

Signature Analysis

To enable the signature analysis mode:

Remove the SG 5010 left panel and the phaselock loop board, leaving the ribbon connector intact (refer to the Circuit Board Removal instructions in this section).

Locate the CPU board jumper, J2071 (refer to the Parts Location Grid located in the pullout pages) and connect it to the SA position. Remove the on-board jumpers, J2070 and J3050.

Insert the SG 5010 into a TM 5000-Series Power Module, using an extender cable, and turn on the power module. The SG 5010 display readout should be 521.

NOTE

The SG 5010 will not perform other functions while in the signature analysis mode.

Signature analysis information for troubleshooting some SG 5010 digital circuitry is provided in the pullout pages pages in the back of this manual. To determine the applicable signature version for your instrument, compare the board assembly (670-) and firmware (160-) numbers in the SG 5010 Signature Versions Table (at the back of this section) with those on the instrument boards. Use the signature analysis information in the pullout pages for the signature version indicated in the table for your instrument board and firmware configuration.

NOTE

After repositioning the jumpers to enable or disable the signature analysis mode (as indicated in the signature analysis tables in the pullout pages), turn the power module off and then back on to re-initialize the SG 5010 microprocessor.

Table 7-2
SG 5010 SIGNATURE VERSIONS

Assembly ROM	1.0
A12, CPU	670-7723-01
U4050	160-1803-00
U4060	160-1802-00

Table 7-3
List of Troubleshooting Accessories

Notch Filter Calibration Fixture	067-0938-00
Plug-in Extender	067-0645-02
GPIB Extender	067-0996-00
Signature Analyzer	067-1090-00