Service Manual

Tektronix

TLA7PG2
Pattern Generator and Probes

071-0714-01

This document applies to firmware version 1.00 and above.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

www.tektronix.com

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WARRANTY

Tektronix warrants that this product will be free from defects in materials and workmanship for a period of one (1) year from the date of shipment. If any such product proves defective during this warranty period, Tektronix, at its option, either will repair the defective product without charge for parts and labor, or will provide a replacement in exchange for the defective product.

In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period and make suitable arrangements for the performance of service. Customer shall be responsible for packaging and shipping the defective product to the service center designated by Tektronix, with shipping charges prepaid. Tektronix shall pay for the return of the product to Customer if the shipment is to a location within the country in which the Tektronix service center is located. Customer shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other locations.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Ground the Product. These products (P6470, P6471, P6472, P6473, and P6474) are indirectly grounded through the grounding conductor of the mainframe power cord. The P6475 is directly grounded through the grounding conductor of the probe power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

CAUTION
Refer to Manual

Protective Ground
(Earth) Terminal

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, switch off the instrument power, then disconnect the power cord from the mains power.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface

This is the service manual for the TLA7PG2 Pattern Generator. The manual contains information needed to service the pattern generator to the module level.

Manual Structure

The following lists contains a brief description of each manual section.

- The *Specifications* contains a description and a list of the characteristics of the pattern generator and pattern generator probes.
- The *Operating Information* includes general information and operating instructions at the level needed to safely power on and service the pattern generator.
- The *Theory of Operation* contains circuit descriptions that support general service to the module level.
- The *Performance Verification* contains procedures to verify the functional operation of the pattern generator and modules as well as procedures to verify the performance to advertised specifications.
- The *Adjustment Procedures* normally lists procedures to adjust the instrument to meet advertised specifications. At this printing, there are no adjustment procedures required for the pattern generator module.
- The *Maintenance* contains information and procedures for performing preventive and corrective maintenance of the pattern generator module. These instructions include cleaning and fault isolation to the module.
- The *Options* contains information about options and accessories that are available for the instrument.
- The *Replaceable Electrical Parts* contains a statement referring you to the Mechanical Parts List, where both electrical and mechanical parts are listed.
- The *Diagrams* contains block diagrams and cabling diagrams that are useful in isolating failed components.
- The *Replaceable Mechanical Parts* includes a table of all replaceable parts, their descriptions, and their Tektronix part numbers.

Manual Conventions

This manual uses certain conventions that you should become familiar with before doing service.

Some sections of the manual contain procedures for you to perform. To keep these instructions clear and consistent, this manual uses the following conventions:

- Names of front-panel controls and menus appear in the same case (initial capitals, all uppercase, and so on.) in the manual as they appear on the TLA7PG2 Pattern Generator front panel and menus.
- Instruction steps are numbered, unless there is only one step.
- An arrow placed after a menu title directs you to access the indicated submenu. For example, System → System Configuration is directing you to select the System menu and then select the submenu named System Configuration.

Related Manuals

Other documentation for the TLA7PG2 Pattern Generator include:

- The *Tektronix Logic Analyzer Family User Manual* contains specifications and information on how to use the TLA7PG2 Pattern Generator.
- A series of probe manuals that provide information for using the probes the the TLA7PG2 Pattern Generator.

Contacting Tektronix

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Service support	1-800-833-9200, select option 2*
Technical support	Email: techsupport@tektronix.com 1-800-833-9200, select option 3* 1-503-627-2400 6:00 a.m. – 5:00 p.m. Pacific time

*** This phone number is toll free in North America. After office hours, please leave a voice mail message.**
Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices.

Introduction

This manual contains information needed to service the TLA7PG2 Pattern Generator, as well as general information critical to safe and effective servicing.

To prevent personal injury or damage to the pattern generator, consider the following before attempting service:

- The procedures in this manual should be performed only by a qualified service person.
- Read the *General Safety Summary* and the *Service Safety Summary*, near the beginning of this manual.
- Read *Preparation for Use* in the *Operating Instructions* section.

Strategy for Servicing

To isolate a failure to a module, use the fault isolation procedures found in *Troubleshooting* in the *Maintenance* chapter of this manual. To move and replace any failed module, follow the instructions in *Removal and Installation Procedures*, also part of the *Maintenance* chapter of this manual. After isolating a faulty module, replace it with a fully-tested module obtained from the factory. The *Replaceable Mechanical Parts* section contains part number and ordering information for all replaceable modules.

Tektronix Service Offerings

Tektronix provides service to cover repair under warranty as well as other services that may provide a cost-effective answer to your service needs.

Whether providing warranty repair service or any of the other services listed below, Tektronix service technicians are well equipped to service the TLA7PG2 Pattern Generator. Tektronix technicians train on Tektronix products; they have access to the latest information on improvements to the TLA7PG2 Pattern Generator as well as the latest new options.

Warranty Repair Service

Tektronix warrants this product for one year from the date of purchase. (The warranty is listed in the front of this manual.) Tektronix technicians provide warranty service at most Tektronix service locations worldwide. The Tektronix product catalog lists all service locations worldwide.

Self Service

Tektronix supports repair to the module level by providing Module Exchange.

Module Exchange. This service reduces down-time for repair by allowing you to exchange most modules for remanufactured ones. Tektronix ships an updated tested exchange module from the Beaverton, Oregon service center, typically within 24 hours. Each module comes with a 90-day service warranty.

Specifications

This chapter provides a high-level description of the TLA7PG2 Pattern Generator module and the associated pattern generator probes. It also lists the specifications for the modules and probes.

Product Description

The TLA7PG2 Pattern Generator is a 64-channel, programmable pattern generator module with sequential control that plugs into the TLA700 series mainframes, and is intended for use as an integral component of the Tektronix Logic Analyzer Family series of products.

The pattern generator module provides multichannel signals for use in applications, such as simulation of missing system elements, erroneous signals for stress testing, or extended analysis for simulating a device under test.

You can put circuits in a desired state and operate the pattern generator at full speed or single step it through a series of states. The TLA7PG2 Pattern Generator can also generate infrequently encountered test conditions to test a hardware design or software program for robustness.

The TLA7PG2 Pattern Generator supports the following probes:

- P6470 TTL/CMOS
- P6471 ECL
- P6472 PECL/LVPECL
- P6473 LVDS
- P6474 LVCMOS
- P6475 Variable

You can have up to four probes on each pattern generator.

Following are some of the key features of the TLA7PG2 Pattern Generator:

- Provides up to 64 channels
- Offers a Jump If condition for all data blocks (maximum of 4000) up to clock rates of 268 MHz

The TLA7PG2 Pattern Generator can fully test circuits at real clock speeds, without having to use improvised setups.

Pattern Generator Module Characteristics

All specifications are guaranteed unless noted *Typical*. Typical characteristics describe typical or average performance and provide useful reference information.

Specifications that are marked with the ✓ symbol are checked directly (or indirectly) in the *Performance Verifications* chapter of this manual.

The specifications apply to all versions of the pattern generator unless otherwise noted.

The performance limits in this specification are valid with these conditions:

- The modules must be installed in a Tektronix Logic Analyzer Mainframe.
- The module must have had at least a 30 minute warm-up period.

Table 1-1: PG module electrical characteristics, operational mode

Characteristic	Description
Normal	Pattern data output is synchronized by the internal/external clock input
Step	Pattern data output is synchronized by the software command

Table 1-2: PG module electrical characteristics, output pattern

Characteristic	Description	
✓ Maximum Operating Clock Frequency	134 MHz in Full Channel Mode 268 MHz in Half Channel Mode	
Pattern length	40 to 262,140 (2^{18} - 4) in Full Channel Mode (standard) 80 to 524,280 (2^{19} - 8) in Half Channel Mode (standard) 40 to 1,048,572 (2^{20} - 4) in Full Channel Mode (option 1M or PowerFlex upgrade) 80 to 2,097,144 (2^{21} - 8) in Half Channel Mode (option1M or PowerFlex upgrade)	
Number of channels	64 channels in Full Channel Mode 32 channels in Half Channel Mode The pattern memory for the following data channel will be shared with strobe control/internal inhibit control	
	Probe D data output channel	*Control*
	D0:0	STRB0
	D0:1	STRB1
	D0:2	STRB2
	D0:3	STRB3
	D0:4	Inhibit probe A

Table 1-2: PG module electrical characteristics, output pattern (Cont.)

Characteristic	Description	
	D0:5	Inhibit probe B
	D0:6	Inhibit probe C
	D0:7	Inhibit probe D
Sequences	Maximum 4,000	
Number of Blocks	Maximum 4,000	
Number of Sub-Sequences	Maximum 50	
Sub-Sequences	Maximum 256 steps	
Repeat Count	1 to 65,536 or infinite	

Table 1-3: PG module, internal clock

Characteristic	Description
Clock Period	2.0000000 s to 7.4626865 ns in Full Channel Mode 1.0000000 s to 3.7313432 ns in Half Channel Mode
Period Resolution	8 digits

Table 1-4: PG module, external clock input

Characteristic	Description
Clock Rate	DC to 134 MHz in Full Channel Mode DC to 268 MHz in Half Channel Mode
Polarity	Normal or Invert
Threshold	
Range	-2.56 V to +2.54 V
Resolution	20 mV
Input Impedance	1 kΩ terminated to GND
Sensitivity	500 mV_{p-p}

Table 1-5: PG module, event processing

Characteristic	Description
Event Action	Advance, Jump and Inhibit
Number of Event Inputs	8 External Event Inputs (2 per each probe)

Table 1-5: PG module, event processing (Cont.)

Characteristic	Description
Number of Event Definitions	8 (A maximum of 256 event input patterns can be OR'd to define an event)
Event Mode	
for Advance	Edge or Level
for Jump	Edge or Level
Event Filter	None or 50 ns

Table 1-6: PG module, intermodule interactions

Characteristic	Description
Signal Input	Input from backplane Selectable from Signal 1, 2, 3, and 4 Used to define the Event
Signal Output	Output to backplane Selectable from Signal 1, 2, 3, and 4 Specified as High or Low in each Sequence line

Table 1-7: PG module, merged PG modules

Characteristic	Description
Number of modules that can be merged together	5
External Event Input for merged module	For Jump and Advance, only the External Event Input of the leftmost module is used; for Inhibit, each module uses its own External Event Input as a source

Table 1-8: PG module, mechanical

Characteristic	Description
Slot width	Requires 2 mainframe slots
Weight (Typical)	2.5 kg (5 lbs 4 oz)
Overall dimensions (excluding connectors)	
Height	10.32 in (262 mm)
Width	2.39 in (61 mm)

Table 1-8: PG module, mechanical (Cont.)

Characteristic	Description
Depth	14.7 in (373 mm)
Mainframe interlock	1.4 ECI keying is implemented

Probe Characteristics

All specifications are guaranteed unless noted *Typical*. Typical characteristics describe typical or average performance and provide useful reference information.

Specifications that are marked with the ✓ symbol are checked directly (or indirectly) in the *Performance Verifications* chapter of this manual.

The specifications apply to all versions of the pattern generator probes unless otherwise noted.

The performance limits in this specification are valid with these conditions:

- The probes must be installed in a TLA7PG2 Pattern Generator.
- The probes must have had at least a 30 minute warm-up period.

Table 1-9: P6470 TTL/CMOS probe

All timing values are specified at the probe connector under the conditions listed below, unless otherwise noted:
Output Voltage setting: +5 V
Series Termination Resistor: 75 Ω
Load: 510 Ω + 50 pF

Characteristic	Description		
Maximum Clock Frequency (with series termination resistor: 75 Ω)	Output Level (V_{cc})	Full Channel mode	Half Channel mode
	Vcc ≤ 3.3 V	134 MHz	268 MHz
	3.3 V < Vcc ≤ 5 V	62.5 MHz	125 MHz
	Vcc > 5 V	52.5 MHz	105 MHz
Maximum Clock Frequency (with series termination resistor: 75 Ω, load: 10 kΩ + 15 pf, sample output pattern: 8 bit counter) *Typical*	Output Level (V_{cc})	Full Channel mode	Half Channel mode
	Vcc ≤ 5.5 V	134 MHz	268 MHz
Output Level (V_{CC})	2.0 V to 5.5 V, 25 mV step, into 1 MΩ		
Maximum Resistive Load	220 Ω		
Maximum Capacitive Load	50 pF		
Output Type	74LVC541A for Data Output 74LVC244A for Clock/Strobe Output		
Series Termination Resistor	75 Ω standard. 43, 100 and 150 Ω as optional accessories (18 pin DIP socket)		
Supported Channel Mode	Half and Full		
Number of External Inhibit Inputs	1		

Table 1-9: P6470 TTL/CMOS probe (Cont.)

All timing values are specified at the probe connector under the conditions listed below, unless otherwise noted:
Output Voltage setting: +5 V
Series Termination Resistor: 75 Ω
Load: 510 Ω + 50 pF

Characteristic	Description
Rise/Fall Time (20% to 80% load: 1 MΩ +< 1 pF) *Typical*	Clock/Strobe Output Rise 640 ps Fall 1.1 ns Data Output Rise 680 ps Fall 2.9 ns
Rise/Fall Time (20% to 80% load: 510 Ω + 51 pF) *Typical*	Clock/Strobe Output Rise 6.5 ns Fall 6.3 ns Data Output Rise 5.2 ns Fall 4.5 ns
Data Output Skew *Typical*	< 570 ps between all data output pins of all modules in the mainframe after intermodule skew is adjusted manually < 480 ps between all data output pins of all probes of single module < 440 ps between all data output pins of single probe
Data Output to Strobe Output Delay *Typical*	+ 1.7 ns when strobe delay set to zero. (Td3 in Figure 1-1 on page 1-25)
Data Output to Clock Output Delay *Typical*	+2.4 ns (Td2 in Figure 1-1 on page 1-25)
External Clock Input to Clock Output Delay *Typical*	61 ns (Td1 in Figure 1-1 on page 1-25)
External Inhibit Input to Output Enable Delay *Typical*	34 ns for Data Output (Td4 in Figure 1-2 on page 1-25)
External Inhibit Input to Output Disable Delay *Typical*	86 ns for Data Output (Td5 in Figure 1-2 on page 1-25)
Probe D Data Output to Output Enable Delay (for Internal Inhibit) *Typical*	7 ns for Data Output (Td4 in Figure 1-2 on page 1-25)
Probe D Data Output to Output Disable Delay (for Internal Inhibit) *Typical*	8 ns for Data Output (Td5 in Figure 1-2 on page 1-25)
External Event Input to Clock Output Setup (for inhibit) (event-filter: off) *Typical*	Full channel mode: 1.5 clocks + 240 ns (Td6 in Figure 1-3 on page 1-25) Half channel mode: 2 clocks + 240 ns
External Event Input and Inhibit Input Input Type Minimum Pulse Width	 74LVC14A, Positive True, 1 kΩ to GND 200 ns (event filter: off)

Table 1-9: P6470 TTL/CMOS probe (Cont.)

All timing values are specified at the probe connector under the conditions listed below, unless otherwise noted:
Output Voltage setting: +5 V
Series Termination Resistor: 75 Ω
Load: 510 Ω + 50 pF

Characteristic	Description
External Event Input Delay to Data Output for Advance	230 ns to 330 ns + 1.5 to 2.5 CLK2 (Td12 in Figure 1-7 on page 1-27) (CLK2 is from 2.5 ns to 5 ns when Internal Clock is used. It is the same as one clock period when the External Clock is used.)
External Event Input Number of Inputs Setup Time of Event *Typical* Input for Event Jump	 2 Half Channel Mode 54 to 61 clocks + 240 ns before the next block Full Channel Mode 27.5 to 31 clocks + 240 ns before the next block (Td9 in Figure 1-4 on page 1-26)
Setup Time of Event Input for Event Advance *Typical*	In Half Channel Mode, 240 ns before the rising edge of 5th clock output pulse from the last of the previous block (Td10 in Figure 1-5 on page 1-26) In Full Channel Mode, 240 ns before the rising edge of 3rd clock output pulse from the last of the previous block (Td11 in Figure 1-6 on page 1-27)
Mainframe External Signal Input to PG Probe data output for Advance via Signal 1, 2 *Typical* via Signal 3, 4 *Typical*	 200 ns to 300 ns + 1.5 to 2.5 CLK2 230 ns to 330 ns + 1.5 to 2.5 CLK2 (CLK2 is from 2.5 ns to 5 ns when the Internal Clock is used. It is the same as one clock period when the External Clock is used)
for Inhibit via Signal 1, 2 *Typical* via Signal 3, 4 *Typical*	 100 ns to 200 ns + 2 to 3 CLK (Half Channel Mode) 100 ns to 200 ns + 1.5 to 2.5 CLK (Full Channel Mode) 130 ns to 230 ns+ 2 to 3 CLK (Half Channel Mode) 130 ns to 230 ns + 1.5 to 2.5 CLK (Full Channel Mode)
PG Probe Clock Output to Mainframe External Signal Output via Signal 1, 2 *Typical* via Signal 3, 4 *Typical*	 18 ns - 5 CLK (Half Channel Mode) 18 ns - 3 CLK (Full Channel Mode) 29 ns - 5 CLK (Half Channel Mode) 29 ns - 3 CLK (Full Channel Mode)
Number of Data Outputs	16 in Full Channel Mode 8 in Half Channel Mode
Number of Clock Outputs	1
Number of Strobe Outputs	1 (Only one Clock Output or Strobe Output can be enabled at one time per probe)
Number of External Event Inputs	2

Table 1-9: P6470 TTL/CMOS probe (Cont.)

All timing values are specified at the probe connector under the conditions listed below, unless otherwise noted:
Output Voltage setting: +5 V
Series Termination Resistor: 75 Ω
Load: 510 Ω + 50 pF

Characteristic	Description
Clock Output Polarity	Positive
Strobe Type	RZ only

Table 1-10: P6471 ECL probe

All timing values are specified at the probe connector under the condition listed below, unless otherwise noted:
Load: 51 Ω terminated to -2 V

Characteristic	Description
Maximum Clock Frequency	134 MHz in Full Channel mode 268 MHz in Half Channel mode
Output Level	ECL
Output Type	100E151 for data output 100EL16 for strobe output 100EL04 for clock output outputs are unterminated
Supported Channel Mode	Half and Full
Rise/Fall Time (20% to 80%) *Typical*	Clock Output Rise 320 ps Fall 330 ps Data Output Rise 1,200 ps Fall 710 ps Strobe Output Rise 290 ps Fall 270 ps
Data Output Skew *Typical*	< 255 ps between all data output pins of all modules in the mainframe after intermodule skew is adjusted manually < 240 ps between all data output pins of all probes of single module < 210 ps between all data output pins of a single probe
Data Output to Strobe Output Delay *Typical*	+2.94 ns when strobe delay set to zero (Td3 in Figure 1-1 on page 1-25)
Data Output to Clock Output Delay *Typical*	+780 ps (Td2 in Figure 1-1 on page 1-25)
External Clock Input to Clock Output Delay *Typical*	50 ns (Td1 in Figure 1-1 on page 1-25)

Table 1-10: P6471 ECL probe (Cont.)

All timing values are specified at the probe connector under the condition listed below, unless otherwise noted:
Load: 51 Ω terminated to -2 V

Characteristic	Description
External Event Input Delay to Data Output for Advance	170 ns to 270 ns + 1.5 to 2.5 CLK2 (Td12 in Figure 1-7 on page 1-27) (CLK2 is from 2.5 ns to 5 ns when Internal Clock is used. It is the same as one clock period when the External Clock is used.)
External Event Input Input Level Input Type Minimum Pulse Width	 ECL 10H116 with 75 kΩ to -2 V 150 ns (Event filter: off)
External Event Input Number of Inputs Setup Time of Event Input for Event Jump *Typical*	 2 Half Channel Mode, 54 to 61 clocks + 180 ns before the next block Full Channel Mode, 27.5 to 31 clocks + 180 ns before the next block (Td9 in Figure 1-4 on page 1-26)
Setup Time of Event Input for Event Advance *Typical*	Half Channel Mode: 80 ns before the rising edge of 5th clock output pulse from the last of the previous block (Td10 in Figure 1-5 on page 1-26) Full Channel Mode 80 ns before the rising edge of 3rd clock output pulse from the last of the previous block (Td11 in Figure 1-6 on page 1-27)
Mainframe External Signal Input to PG Probe data output for Advance via Signal 1, 2 *Typical* via Signal 3, 4 *Typical*	 200 ns to 300 ns + 1.5 to 2.5 CLK2 230 ns to 330 ns + 1.5 to 2.5 CLK2 (CLK2 from 2.5 ns to 5 ns when Internal Clock is used. It is same as one clock period when External Clock is used.)
PG Probe Clock Output to Mainframe External Signal Output via Signal 1, 2 *Typical* via Signal 3, 4 *Typical*	 28 ns - 5 CLK (Half Channel Mode) 28 ns - 3 CLK (Full Channel Mode) 38 ns - 5 CLK (Half Channel Mode) 38 ns - 3 CLK (Full Channel Mode)
Number of Data Outputs	16 in Full Channel Mode 8 in Half Channel Mode
Number of Clock Outputs	1
Number of Strobe Outputs	1 (Only one Clock Output or one Strobe Output can be enabled at one time per probe)
Number of External Event Inputs	2
Clock Output Polarity	Positive
Strobe Type	RZ only

Table 1-11: P6472 PECL/LVPECL probe

All timing values are specified with a load condition of 1 M Ω + ≤ 1 pF with PECL mode.

Characteristic	Description	
Maximum Clock Frequency	Full Channel Mode	Half Channel Mode
	134 MHz	268 MHz
Number of Data Outputs	8 Full Channel 8 Half Channel	
Number of Clock Outputs	1 differential	
Number of Strobe Outputs	1 differential (Only one Clock Output or one Strobe Output can be enabled at one time per probe)	
Number of External Event Inputs	2	
Clock Output Polarity	Positive	
Strobe Type	RZ (return to zero) only	
Strobe Delay	Zero or Trailing Edge	
Output Level	PECL, LVPECL (selectable by moving a jumper in the probe)	
Output Type	100EL90 (all outputs are terminated)	
Supported Channel Mode	Half and Full	
Rise/Fall Time (20% to 80%)	Rise 430 ps Fall 970 ps	
Data Output Skew	< 385 ps between all data output pins of all modules in the mainframe after intermodule skew is adjusted manually < 370 ps between all data output pins of all probes of single module < 340 ps between all data output pins of a single probe	
Data Output to Strobe Output Delay	+ 2.93 ns when strobe delay is set to zero (See Td3 in Figure 1-1 on page 1-25)	
Data Output to Clock Output Delay	+ 1.12 ns (Td2 in Figure 1-1 on page 1-25)	
External Clock Input to Clock Output Delay	50 ns (See Td1 in Figure 1-1 on page 1-25)	
External Event Input Delay to Data Output for Advance	170 ns to 270 ns + 1.5 to 2.5 CLK2 (Td12 in Figure 1-7 on page 1-27) (CLK2 is from 2.5 ns to 5 ns when Internal Clock is used. It is the same as one clock period when the External Clock is used.)	
External Event Input		
Input Level	PECL, LVPECL (selectable by moving a jumper in the probe)	
Input Type	100EL91, unterminated	
Minimum Pulse Width (event filter: off)	150 ns	

Table 1-11: P6472 PECL/LVPECL probe (Cont.)

All timing values are specified with a load condition of 1 M Ω + ≤ 1 pF with PECL mode.

Characteristic	Description
External Event Input	
Setup Time of Event Input for Event Jump	Half Channel Mode: 54 to 61 Clocks + 180 ns before the next block Full Channel Mode: 27.5 to 31 Clocks + 180 ns before the next block (see Td9 in Figure 1-4 on page 1-26)
Setup Time of Event Input for Event Advance	Half Channel Mode: 180 ns before the rising edge of the 5th clock output pulse from the last of the previous block (See Td10 in Figure 1-5 on page 1-26) Full Channel Mode: 180 ns before the rising edge of the 3rd clock output pulse from the last of the previous block (see Td11 in Figure 1-6 on page 1-27)
Mainframe External Signal Input to PG Probe Data Output	
For Advance:	
Using signal 1 or 2	200 ns to 300 ns + 1.5 to 2.5 CLK2
Using signal 3 or 4	230 ns to 330 ns + 1.5 to 2.5 CLK2
	(CLK2 is from 2.5 ns to 5 ns when Internal Clock is used. It is the same as one clock period when the External Clock is used.)
PG Probe Clock Output to Mainframe External Signal Output	
Using signal 1 or 2	31 ns -5 CLK (Half Channel Mode) 31 ns -3 CLK (Full Channel Mode)
Using signal 3 or 4	40 ns -5 CLK (Half Channel Mode) 40 ns -3 CLK (Full Channel Mode)

Table 1-12: P6473 LVDS probe

All timing values are specified at the probe connector under the condition listed below, unless otherwise noted:
Load: 100 Ω + < 1 pF

Characteristic	Description	
Maximum Clock Frequency	Full Channel Mode	Half Channel Mode
	134 MHz	268 MHz
Number of Data Outputs	16 Full Channel 8 Half Channel	

Table 1-12: P6473 LVDS probe (Cont.)

All timing values are specified at the probe connector under the condition listed below, unless otherwise noted:
Load: 100 Ω + < 1 pF

Characteristic	Description
Number of Clock Outputs	1 (Only one Clock Output or One Strobe Output can be enabled at one time per probe.)
Number of Strobe Outputs	1 (Only one Clock Output or One Strobe Output can be enabled at one time per probe.)
Number of External Event Inputs	1
Number of External Inhibit Inputs	1
Clock Output Polarity	Positive
Strobe Type	RZ (return to zero) only
Strobe Delay	Zero or Trailing Edge
Maximum Capacitive Load	10 pF
Output Type	LVDS (TIA/EIA-644 compatible)
Supported Channel Mode	Half and Full
Rise/Fall Time (20% to 80%)	Rise: 910 ps Fall: 750 ps
Data Output Skew	< 365 ps between all data output pins of all modules in the mainframe after intermodule skew is adjusted manually < 350 ps between all data output pins of all probes of single module < 320 ps between all data output pins of a single probe
Data Output to Strobe Output Delay	-280 ns when strobe delay is set to zero (See Td3 in Figure 1-1 on page 1-25)
Data Output to Clock Output Delay	1.2 ns (Td2 in Figure 1-1 on page 1-25)
External Clock Input to Clock Output Delay	55 ns (See Td1 in Figure 1-1 on page 1-25)
External Inhibit Input to Output Enable Delay	9 ns for Data Output (See Td4 in Figure 1-2 on page 1-25)
External Inhibit Input to Output Disable Delay	12 ns for Data Output (See Td5 in Figure 1-2 on page 1-25)
Probe D Data Output to Output Enable Delay (for Internal Inhibit)	2 ns for Data Output (See Td4 in Figure 1-2 on page 1-25)
Probe D Data Output to Output Disable Delay (for Internal Inhibit)	5 ns for Data Output (See Td5 in Figure 1-2 on page 1-25)
External Event Input to Clock Output Setup (for inhibit) event-filter: off	Full Channel mode: 1.5 Clocks + 180 ns Half Channel mode: 2 Clocks + 180 ns (See Td6 in Figure 1-3 on page 1-26)
External Event Input Delay to Data Output for Advance	170 ns to 270 ns + 1.5 to 2.5 CLK2 (Td12 in Figure 1-7 on page 1-27) (CLK2 is from 2.5 ns to 5 ns when Internal Clock is used. It is the same as one clock period when the External Clock is used.)

Table 1-12: P6473 LVDS probe (Cont.)

All timing values are specified at the probe connector under the condition listed below, unless otherwise noted:
Load: 100 Ω + < 1 pF

Characteristic	Description
External Event Input and Inhibit Input	
Input Type	LVDS (TIA/EIA-644 compatible), positive true
Minimum Pulse Width (event filter: off)	150 ns
External Event Input Setup Time of Event Input for Event Jump	Half Channel Mode: 54 to 61 Clocks + 180 ns before the next block Full Channel Mode: 27.5 to 31 Clocks + 180 ns before the next block (See Td9 in Figure 1-4 on page 1-26)
External Event Input Setup Time for Event Advance	Half Channel Mode: 180 ns before the rising edge of the 5th clock output pulse from the last of the previous block (See Td10 in Figure 1-5 on page 1-26) Full Channel Mode: 180 ns before the rising edge of the 3rd clock output pulse from the last of the previous block (See Td11 in Figure 1-6 on page 1-27)
Mainframe External Signal Input to PG Probe Data Output	
For Advance:	
Using signal 1 or 2	200 ns to 300 ns + 1.5 to 2.5 CLK2
Using signal 3 or 4	230 ns to 330 ns + 1.5 to 2.5 CLK2
	(CLK2 is from 2.5 ns to 5 ns when Internal Clock is used. It is the same as one clock period when the External Clock is used.)
For Inhibit:	
Using signal 1 or 2	100 ns to 200 ns + 2 to 3 CLK (Half Channel Mode)
	100 ns to 200 ns +1.5 to 2.5 CLK (Full Channel Mode)
Using signal 3 or 4	130 ns 230 ns + 2 to 3 CLK (Half Channel Mode)
	130 ns to 230 ns + 1.5 to 2.5 CLK (Full Channel Mode)
PG Probe Clock Output to Mainframe External Signal Output	
Using signal 1 or 2	26 ns -5 CLK (Half Channel Mode)
	26 ns -3 CLK (Full Channel Mode)
Using signal 3 or 4	35 ns -5 CLK (Half Channel Mode)
	35 ns -3 CLK (Full Channel Mode)

Table 1-13: P6474 LVCMOS probe

All timing values are specified at the probe connector under the conditions listed below, unless otherwise noted:

Output Voltage setting: +3.3 V

Series Termination Resistor: 75 Ω

Load: 510 Ω + 20 pF

Characteristic	Description	
Maximum Clock Frequency	Full Channel Mode	Half Channel Mode
	134 MHz	268 MHz
Number of Data Outputs	16 Full Channel 8 Half Channel	
Number of Clock Outputs	1 (Only one Clock Output or One Strobe Output can be enabled at one time per probe.)	
Number of Strobe Outputs	1 (Only one Clock Output or One Strobe Output can be enabled at one time per probe.)	
Number of External Event Inputs	2	
Number of External Inhibit Inputs	1	
Clock Output Polarity	Positive	
Strobe Type	RZ (return to zero) only	
Strobe Delay	Zero or Trailing Edge	
Output Level (V_{cc})	1.2 V to 3.3 V, 25 mV step, into 1 M Ω	
Maximum Resistive Load	510 Ω	
Maximum Capacitive Load	20 pF	
Output Type	74AVC16244	
Series Termination Resistor	75 Ω standard. 43, 100 and 150 Ω as optional accessories (18 pin DIP socket)	
Supported Channel Mode	Half and Full	
Rise/Fall Time (20 % to 80 %, load: 1M Ω + < 1 pF)	Rise 1200 ps Fall 610 ps	
Rise/Fall Time (20 % to 80 %, load: 510 Ω + 50 pF)	Rise 3.4 ns Fall 3.2 ns	
Data Output Skew	< 590 ps between all data output pins of all modules in the mainframe after intermodule skew is adjusted manually < 500 ps between all data output pins of all probes of single module < 460 ps between all data output pins of a single probe	
Data Output to Strobe Output Delay	460 ps when strobe delay is set to zero (See Td3 in Figure 1-1 on page 1-25)	
Data Output to Clock Output Delay	1.84 ns (Td2 in Figure 1-1 on page 1-25)	
External Clock Input to Clock Output Delay	55 ns (See Td1 in Figure 1-1 on page 1-25)	

Table 1-13: P6474 LVCMOS probe (Cont.)

All timing values are specified at the probe connector under the conditions listed below, unless otherwise noted:

Output Voltage setting: +3.3 V

Series Termination Resistor: 75 Ω

Load: 510 Ω + 20 pF

Characteristic	Description
External Inhibit Input to Output Enable Delay	36 ns for Data Output (See Td4 in Figure 1-2 on page 1-25)
External Inhibit Input to Output Disable Delay	18 ns for Data Output (See Td5 in Figure 1-2 on page 1-25)
Probe D Data Output to Output Enable Delay (for Internal Inhibit)	6 ns for Data Output (See Td4 in Figure 1-2 on page 1-25)
Probe D Data Output to Output Disable Delay (for Internal Inhibit)	7 ns for Data Output (See Td5 in Figure 1-2 on page 1-25)
External Event Input to Clock Output Setup (for inhibit) event-filter: off	Full Channel mode: 1.5 Clocks + 180 ns Half Channel mode: 2 Clocks + 180 ns (See Td6 in Figure 1-3 on page 1-26)
External Event Input Delay to Data Output for Advance	170 ns to 270 ns + 1.5 to 2.5 CLK2 (Td12 in Figure 1-7 on page 1-27) (CLK2 is from 2.5 ns to 5 ns when Internal Clock is used. It is the same as one clock period when the External Clock is used.)
External Event Input and Inhibit Input	
Input Type	74AVC16244, Positive True, 1 k Ω to GND The V_{cc} of the input receiver is variable and the same as the V_{cc} of the output driver.
Minimum Pulse Width	150 ns (event filter: off)
External Event Input	
Setup Time of Event	Half Channel Mode: 54 to 61 Clocks + 180 ns before the next block
Input for Event Jump	Full Channel Mode: 27.5 to 31 Clocks + 180 ns before the next block (See Td9 in Figure 1-4 on page 1-26)
External Event Input Setup Time for Event Advance	Half Channel Mode: 180 ns before the rising edge of the 5th clock output pulse from the last of the previous block (See Td10 in Figure 1-5 o n page 1-26) Full Channel Mode: 180 ns before the rising edge of the 3rd clock output pulse from the last of the previous block (See Td11 in Figure 1-6 on page 1-27)

Table 1-13: P6474 LVCMOS probe (Cont.)

All timing values are specified at the probe connector under the conditions listed below, unless otherwise noted:

Output Voltage setting: +3.3 V

Series Termination Resistor: 75 Ω

Load: 510 Ω + 20 pF

Characteristic	Description
Mainframe External Signal Input to PG Probe Data Output	
For Advance:	
Using signal 1 or 2	200 ns to 300 ns + 1 to 2 CLK2
Using signal 3 or 4	230 ns to 330 ns + 1 to 2 CLK2
	(CLK2 is from 2.5 ns to 5 ns when the Internal Clock is used. It is the same as one clock period when the External Clock is used.)
For Inhibit:	
Using signal 1 or 2	100 ns to 200 ns + 2 to 3 CLK (Half Channel Mode)
	100 ns to 200 ns + 1.5 to 2.5 CLK (Full Channel Mode)
Using signal 3 or 4	130 ns to 230 ns + 2 to 3 CLK (Half Channel Mode)
	130 ns to 230 ns + 1.5 to 2.5 CLK (Full Channel Mode)
PG Probe Clock Output to Mainframe External Signal Output	
Using signal 1 or 2	25 ns -5 CLK (Half Channel Mode)
	25 ns -3 CLK (Full Channel Mode)
Using signal 3 or 4	34 ns -5 CLK (Half Channel Mode)
	34 ns -3 CLK (Full Channel Mode)

Table 1-14: P6475 Variable probe

All timing values are specified at the probe connector under the conditions listed below, unless otherwise noted:

Output Voltage setting: Voh +2 V, Vol 0 V

Slew Rate: 2.5 V/ns

Delay Range: 0

Delay Time: 0 ns

Load: 50 Ω

Characteristic	Description		
Maximum Clock Frequency		**Full CH Mode**	**Half CH Mode**
	Delay Range: 0 Delay ≤ 10 ns	134 MHz	268 MHz
	Delay Range: 0 Delay ≥ 10 ns	134 MHz	268 MHz
	Delay Range: 1,2,3	30 MHz	30 MHz
Number of Data Outputs	8 (CH0 to CH7)		
Number of Clock Outputs	1		
Number of Strobe Outputs	0		
Number of External Event Inputs	2		
Number of External Inhibit Inputs	1		
Clock Output Polarity	Positive or Negative		
Data Format	CH0 to CH5: NRZ CH6 and CH7: NRZ, R1 or RZ (independent)		
Output Impedance	50 Ω		
Output Level			
Vol	-3 V to +6.75, 10 mV step, into 1 M Ω		
Voh	-2.75 V to +7 V, 10 mV step, into 1 M Ω		
Voltage Swing	250 mV_{p-p} to 9 V_{p-p}		
Control	CH0 to CH5: Common CH6, CH7, CLK: Independent		
Accuracy	± 3% of value ± 0.1 V		
Output Current			
Sink	<-30 mA		
Source	<+30 mA		
Supported Channel Mode	Half and Full		

Table 1-14: P6475 Variable probe (Cont.)

All timing values are specified at the probe connector under the conditions listed below, unless otherwise noted:

Output Voltage setting: Voh +2 V, Vol 0 V

Slew Rate: 2.5 V/ns

Delay Range: 0

Delay Time: 0 ns

Load: 50 Ω

Characteristic	Description		
Delay Channel	CH6 and CH7 (Independent)		
Delay Time	**Delay Range**	**Minimum Delay**	**Maximum Delay**
	0	0 ns	20 ns
	1	15 ns	30 ns
	2	25 ns	40 ns
	3	35 ns	50 ns
	With reference to CH0, CH6, CH7 independent.		
Delay Resolution	10 ps		
Delay Accuracy	± (3% of Delay Time) ± 0.8 ns (to CH0) (For delay range of 1, 2, and 3 this is only for rising edge. The falling edge will be delayed approximately 4 ns from the setting value.)		
CH6 Output Mode	The following five modes are available: Normal CH6 or CH7 CH6 and CH7 CH6 or (not CH7) CH6 and (not CH7)		
Slew Rate Control	0.5 V/ns to 2.5 V/ns, 100 mV step		
Rise/Fall Time 20 % to 80 % at maximum slew rate, load: 1 M Ω + < 10 pF	Rise 550 ps Fall 640 ps		
Rise/Fall Time 20 % to 80 % at maximum slew rate, load: 50 Ω	Rise 430 ps Fall 510 ps		

Table 1-14: P6475 Variable probe (Cont.)

All timing values are specified at the probe connector under the conditions listed below, unless otherwise noted:

Output Voltage setting: Voh +2 V, Vol 0 V

Slew Rate: 2.5 V/ns

Delay Range: 0

Delay Time: 0 ns

Load: 50 Ω

Characteristic	Description
Data Output Skew	< 295 ps between all data output pins of all modules in the mainframe after intermodule skew is adjusted manually < 280 ps between all data output pins of all probes of single module < 250 ps between all data output pins of a single probe
Data Output to Clock Output Delay	940 ps (See Td2 in Figure 1-1 on page 1-25)
External Clock Input to Clock Output Delay	62 ns (See Td1 in Figure 1-1 on page 1-25)
External Inhibit Input to Output Enable Delay	30 ns for Data Output (See Td4 in Figure 1-2 on page 1-25)
External Inhibit Input to Output Disable Delay	28 ns for Data Output (See Td5 in Figure 1-1 on page)
Probe D Data Output to Output Enable Delay (for Internal Inhibit)	-100 ps for Data Output (See Td4 in Figure 1-2 on page 1-25)
Probe D Data Output to Output Disable Delay (for Internal Inhibit)	-4.4 ns for Data Output (See Td5 in Figure 1-2 on page 1-25)
External Event Input to Clock Output Setup (for inhibit) event-filter: off	Full Channel mode: 1.5 Clocks +180 ns Half Channel mode: 2 Clocks + 180 ns (See Td6 in Figure 1-3 on page 1-26)
External Event Input Delay to Data Output for Advance	170 ns to 270 ns + 1.5 to 2.5 CLK2 (Td12 in Figure 1-7 on page 1-27) (CLK2 is from 2.5 ns to 5 ns when Internal Clock is used. It is the same as one clock period when the External Clock is used.)
External Event Input and Inhibit Input	
Polarity	Positive True
Impedance	1 k Ω to GND
Threshold:	
Level	-2.5 V to +2.5 V Event and Inhibit are independent
Resolution	20 mV
Minimum Pulse Width	150 ns (event filter: off)

Table 1-14: P6475 Variable probe (Cont.)

All timing values are specified at the probe connector under the conditions listed below, unless otherwise noted:

Output Voltage setting: Voh +2 V, Vol 0 V

Slew Rate: 2.5 V/ns

Delay Range: 0

Delay Time: 0 ns

Load: 50 Ω

Characteristic	Description
External Event Input	
Setup Time of Event Input for Event Jump	Half Channel Mode: 54 to 61 Clocks + 180 ns before the next block Full Channel Mode: 27.5 to 31 Clocks + 180 ns before the next block (See Td9 in Figure 1-4 on page 1-26)
Setup Time of Event Input for Event Advance	Half Channel Mode: 180 ns before the rising edge of the 5th clock output pulse from the last of the previous block (See Td10 in Figure 1-5 on page 1-26) Full Channel Mode: 180 ns before the rising edge of the 3rd clock output pulse from the last of the previous block (See Td11 in Figure 1-6 on page 1-27)

Table 1-14: P6475 Variable probe (Cont.)

All timing values are specified at the probe connector under the conditions listed below, unless otherwise noted:

Output Voltage setting: Voh +2 V, Vol 0 V

Slew Rate: 2.5 V/ns

Delay Range: 0

Delay Time: 0 ns

Load: 50 Ω

Characteristic	Description
Mainframe External Signal Input to PG Probe Data Output	
For Advance:	
Using signal 1 or 2	200 to 300 ns + 1.5 to 2.5 CLK2
Using signal 3 or 4	230 to 330 ns + 1.5 to 2.5 CLK2
	(CLK2 is from 2.5 ns to 5 ns when the Internal Clock is used. It is the same as one clock period when the External Clock is used.)
For Inhibit: (Output Enable)	
Using signal 1 or 2	100 to 200 ns + 2 to 3 CLK (Half Channel Mode)
	100 to 200 ns +1.5 to 2.5 CLK (Full Channel Mode)
Using signal 3 or 4	130 to 230 ns + 2 to 3 CLK (Half Channel Mode)
	130 to 230 ns + 1.5 to 2.5 CLK (Full Channel Mode)
For Inhibit: (Output Disable)	
Using signal 1 or 2	100 to 200 ns + 2 to 3 CLK (Half Channel Mode)
	100 to 200 ns +1.5 to 2.5 CLK (Full Channel Mode)
Using signal 3 or 4	130 to 230 ns + 2 to 3 CLK (Half Channel Mode)
	130 to 230 ns + 1.5 to 2.5 CLK (Full Channel Mode)
PG Probe Clock Output to Mainframe External Signal Output Delay	
Using signal 1 or 2	19 ns -5 CLK (Half Channel Mode)
	19 ns -3 CLK (Full Channel Mode)
Using signal 3 or 4	28 ns -5 CLK (Half Channel Mode)
	28 ns -3 CLK (Full Channel Mode)

Table 1-15: Power Supply (P6475 only)

Characteristic	Description
AC Line Power	
Voltage rating	100 - 240 V AC
Voltage range	90 - 250 V AC
Frequency range	50 to 60 Hz
Maximum power	35 W
Maximum current	2 A

Table 1-16: Atmospherics

Characteristic	Description
Temperature	
Operating:	+0°C to + 50°C
Nonoperating:	-20°C to + 60°C
Relative Humidity	
Operating:	20% to 80% (No condensation)
	Maximum wet-bulb temperature 29.4°C
Nonoperating:	5% to 90% (No condensation)
	Maximum wet-bulb temperature 40.0°C
Altitude	
Operating:	Up to 4.5 km (15,000 ft)
	Maximum operating temperature decreases 1°C
Nonoperating:	Up to 15 km (50,000 ft)

Table 1-17: Dynamics characteristics (P6470, P6471, P6472, P6473, and P6474)

Characteristic	Description
Vibration	
Operating:	3.038 m/s^2 (0.31 G_{rms}), 5 Hz to 500 Hz
Nonoperating:	24.108 m/s^2 (2.46 G_{rms}), 5 Hz to 500 Hz

Table 1-17: Dynamics characteristics (P6470, P6471, P6472, P6473, and P6474) (Cont.)

Characteristic	Description
Shock	
Nonoperating:	294 m/s^2 (30G), half-sine, 11 ms duration, 3 shocks per axis in each direction (18 shocks total)

Table 1-18: Dynamics characteristics (P6475)

Characteristic	Description
Vibration	
Operating:	3.038 m/s^2 (0.31 $G_{rms)}$, 5 Hz to 500 Hz
Nonoperating:	24.108 m/s^2 (2.46 G_{rms}) , 5 Hz to 500 Hz
Shock (P6475 only)	
Nonoperating:	588 m/s^2 (60G), half-sine, 11 ms duration, 3 shocks per axis in each direction (18 shocks total)

Table 1-19: Probe cables

Characteristic	Description
Dimensions Length	1.5 m (5 ft) Standard probe cable
Length	3.3 m (10.83 ft) Time alignment cable

Table 1-20: Twisted lead set

Characteristic	Description
Dimensions Length	25.4 cm (10 in)

Table 1-21: Certifications and compliances for P6475

Category	Standards or description
Safety	
Third party certification	UL 3111-1
	CSA C22.2 No.1010.1
Self-Declaration	EN61010-1 with second amendment

Pattern Generator Module Timing Diagrams

Figures 1-1 through 1-6 show the pattern generator timing diagrams. The diagrams apply to all probes unless otherwise stated.

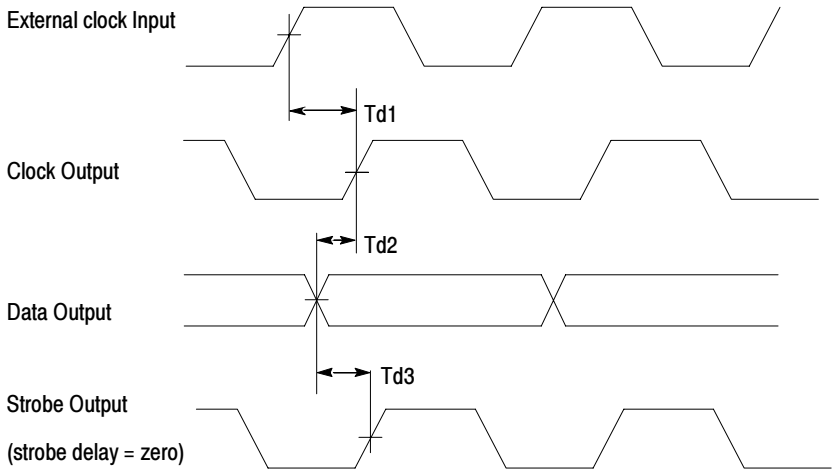


Figure 1-1: Clock and strobe timing diagram

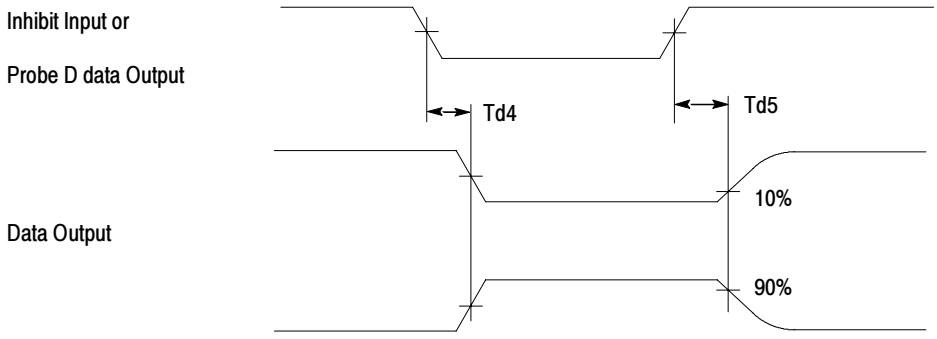


Figure 1-2: P6470, P6472, P6473, and P6474 inhibit timing diagram

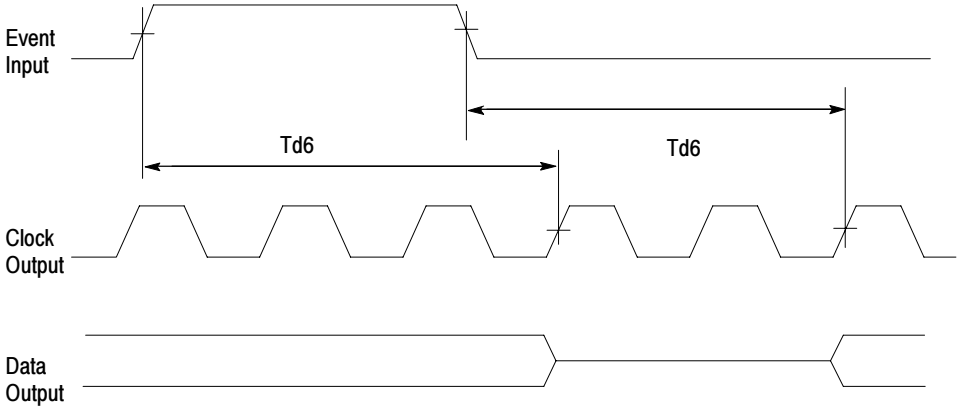


Figure 1-3: P6470, P6472, P6473, and P6474 external event for inhibit timing diagram

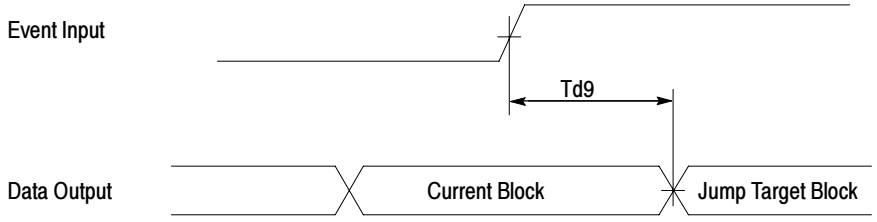


Figure 1-4: External event for jump timing diagram

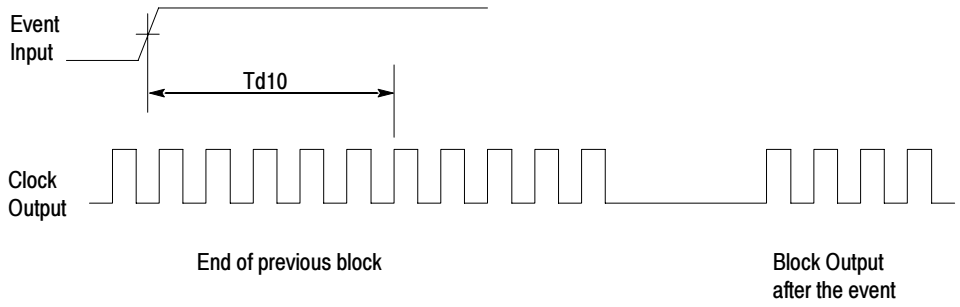


Figure 1-5: External event for half channel advance timing diagram

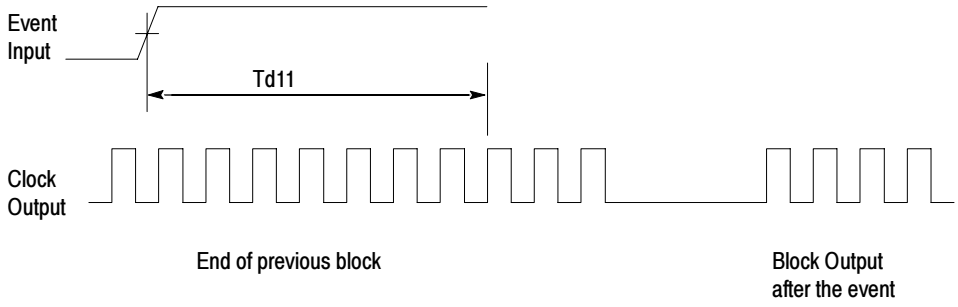


Figure 1-6: External event for full channel advance timing diagram

Figure 1-7: External event for delay to data output for advance diagram

P6470 and P6471 Probe Environmental Characteristics

Table 1-22: P6470 TTL/CMOS probe and P6471 ECL probe

Characteristic	Description
Vibration	
Operating:	0.31 G_{rms}, 5 to 500 Hz
Nonoperating:	2.46 G_{rms}, 5 Hz to 500 Hz
Shock	
Nonoperating:	294 m/s^2 (30G), half-sine, 11 ms duration, 3 shocks per axis in each direction (18 shocks total)

Certifications

Table 1-23: Certifications and compliances

Category	Standards or description
EC Declaration of Conformity - EMC	Meets intent of Directive 89/336/EEC, amended by 93/68/EEC for Electromagnetic Compatibility when configured with sampling head modules designed for use with this instrument as identified in this manual. Compliance was demonstrated to the following specifications as listed in the Official Journal of the European Union: EN 61326 EMC Requirements for Electrical Equipment for Measurement, Control and Laboratory use. Class A Radiated and Conducted Emissions IEC 61000-4-2 Performance Criterion B IEC 61000-4-3 Performance Criterion A IEC 61000-4-4 Performance Criterion B IEC 61000-4-5 Performance Criterion B IEC 61000-4-6 Performance Criterion A IEC 61000-4-11 Performance Criterion B EN 61000-3-2 AC Power Harmonic Current Emissions Radiated emissions may exceed the levels specified in EN 61326 when this instrument is connected to a test object.
Australia/New Zealand Declaration of Conformity - EMC	Complies with EMC Framework per the following standard: AS/NZS 2064.1/2 Class A Radiated and Conducted Emissions
General EMC	To ensure compliance with EMC requirements, only high quality shielded cables having a reliable, continuous outer shield (braid & foil) with full coverage, low impedance connections to shielded connector housings at both ends should be connected to this product.

Operating Information

This section contains basic information about your pattern generator. Refer to your *Tektronix Logic Analyzer Family User Manual* and the TLA7PG2 on-line help for more information on how to use your pattern generator.

Before servicing the TLA7PG2, read the operating instructions. These instructions are at the level appropriate for servicing the pattern generator.

Installation

Hardware installation procedures are described in the *Tektronix Logic Analyzer Family User Manual*. Refer to that document for installing the TLA7PG2 modules in a mainframe. All software required to operate the instrument (except the performance verification software) is already installed on the instrument. The following installation instructions only apply to the TLA7PG2 performance verification software.

It is recommended you have ≥10 MB of free space on the hard drive before installing the software. The Performance Verification software is located on Disc 1 of the Tektronix Logic Analyzer Family Application Software CD.

NOTE. *This installation program uses parameters you supply to create a custom start-up file in your hard disk directory.*

The batch file enables the software to configure your instrument properly before it runs the program.

---

1. Power on the instrument.
2. Exit the Logic Analyzer or Pattern Generator application.

Verify PV/Adjust Software Version

If your instrument already has PV/Adjust software loaded on it, you must verify that the version is the same as the version printed on Disc 1 of the Tektronix Logic Analyzer Family Application Software CD.

If the version of the PV/Adjust software loaded on your instrument is an earlier version, you must delete the earlier version before you can load the newer version.

Install the PV/Adjust Software

Follow these instructions to install the pattern generator setup files.

1. Close all open windows on the desktop.
2. Insert Disc 1 of the Tektronix Logic Analyzer Family Application Software CD in the CD-ROM drive.
3. Click the My Computer Icon and double-click the CD-ROM drive.
4. Double-click the TLA Performance Verification folder.
5. Double-click on the Pattern Generator PV folder and then double-click the Disk1 folder.
6. Double-click the Setup.exe icon to begin the installation program.
7. Follow the on-screen instructions to install the pattern generator setup files on the hard disk.

Operating Environment

The pattern generator operates in an environment with an ambient air temperature between +0° C and +50° C. The pattern generator storage temperature ranges from –20° C and +60° C. After storage at temperatures outside the operating limits, allow the pattern generator chassis to stabilize at a safe operating temperature before applying power.

Applying and Interrupting Power

Consider the following when you power on or power off the TLA7PG2 Pattern Generator:

CAUTION. *To prevent damage to the pattern generator module or probe, do not connect or disconnect the pattern generator cables to or from the pattern generator module or probe while the logic analyzer is on.*

The pattern generator probe cable is not compatible with a SCSI cable, do not use a SCSI cable with the pattern generator module or use the pattern generator probe cable with a SCSI instrument.

The probe is fragile, handle carefully.

Power-On Cycle

The power-on diagnostics run when you first power on, the logic analyzer or when you first start the TLA application or the pattern generator application.

The Power-On window displays the results of the power-on diagnostics in a List Box. These diagnostics only run at power on so there are no controls to execute them.

Power-Off Cycle

Wait for the TLA7PG2 to finish the operation when saving data files. Improper power off or unexpected loss of power to the pattern generator can result in the corruption of data stored in nonvolatile memory.

Diagnostics

Following are two levels of diagnostics programs provided with the pattern generator.

Power-On Diagnostics

The power-on diagnostics run when you first power on the pattern generator or when you first start the TLA application or the pattern generator application.

The Power-On window displays the results of the power-on diagnostics in a List Box. These diagnostics only run at power on, so there are no controls to execute them.

If any test failed, this page opens as the first active window, and all failed tests are highlighted. If a test fails, you can select the Extended Diagnostics property page and rerun the test or dismiss this property page. If you dismiss the page, the application finishes loading.

The Test Name column lists the mainframe, slot number, and name of installed modules. This column also lists specific tests. If a module is not recognized, the module type area is filled in with any available information or the word Unknown is displayed.

Extended Diagnostics

The extended diagnostics test the pattern generator more thoroughly than the power-on diagnostics. The extended diagnostics test the modules in the benchtop mainframe as well as the modules in the expansion mainframe(s). You can use the extended diagnostics to isolate problems to an individual module.

Disconnect any attached probes prior to running the extended diagnostics.

To run the extended diagnostics, select System → System Diagnostics → Extended Diagnostics.

The extended diagnostics window allows you to select and run the extended diagnostics using a hierarchical selection mechanism. You can select one of the following:

- All modules, all tests
- All tests for the system or for one module
- A group of tests for the system or for one module
- A single test for the system or for one module

You can select the run mode: One Time Continuous, or Until Fail. The tests can be stopped using the Stop or Abort buttons.

Run the extended diagnostics for the following:

- Incoming inspection. Run these diagnostics when you first receive this instrument.
- Functional procedure. Run these diagnostics after the instrument or module has been repaired.
- Suspected problem. Run these diagnostics if you think your instrument is not performing correctly.

Test Name. The Test Name column has an indented hierarchical structure.

- All Modules, All Tests. This selection runs all tests in the list.
- Module name. Selects all tests associated with the named module; for example, 1:TLA7PG1.
- Subsystem tests. Selects a set of tests covering a portion of the mainframe or module.
- Item test. A single diagnostic test for a module.
- Last Result. The Last Result column shows the pass or fail result of the most recent test.

When a test is running, the word Running displays until the test is complete and results show. When a series of tests is running and an individual test is complete, results are displayed and the next test is executed. The result Unknown indicates that a particular test is in question. Run the diagnostic again. Contact your local Tektronix service representative if problems persist.

Fail Count. The Fail Count column shows the number of times a test has failed since the Run button on this page was clicked. This count is mainly used when

the run mode is set to Continuous. One Time and Until Fail run modes always display a count of one. All values are cleared when you click the RUN button.

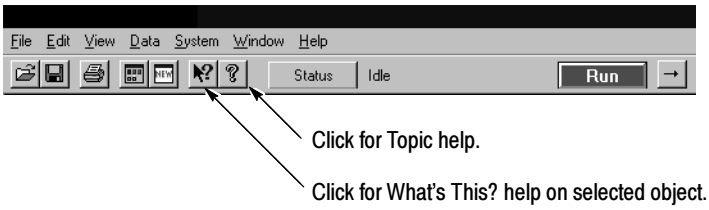
Menus

The TLA7PG2 Pattern Generator is primarily controlled by means of the Application menus. The SYSTEM menu opens when the application is started and provides access to SETUP and PROGRAM functions. The main menu toolbar provides functions for manipulating the basic instrument settings. Refer to the *Tektronix Logic Analyzer Family User Manual* or the TLA7PG2 Pattern Generator online help for more information concerning these menus.

Online Help

The online help gives detailed information about the pattern generator and its probes. Look in the online help for details about user interface selections that are not described in this manual. The online help also has basic operating information for microprocessor support products.

To access the online help system, go to the Help menu, or click the toolbar buttons shown:



Help Topics. Help topics tell you how to perform tasks and describe software features and selections shown on the screen. There are two types of help topics: overview topics and task topics.

Overview topics describe application features, such as the different application windows. Overview topics also describe concepts. Overview topics are available through the Help menu and through Help buttons in dialog boxes. From the Help menu, click Help Topics, and locate the topic using the Contents or Index tab. The Help on Window selection in the Help menu provides overview help for the currently-selected window.

Task topics provide procedure information about how to perform specific tasks. Task topics are available through the Help menu. From the Help menu, click Help Topics, and locate the topic using the Contents or Index tab.

What's This? Help. What's This? help provides a short description of the control or screen feature selected. First click the What's This? button on the toolbar, and then click the item of interest. For further information about the item, go to the Topic help.

PPI Online Help. Select Help for the pattern generator Programmatic Interface (PPI) from the drop-down help menu.

Pattern Generator Online Help. Select Help for the pattern generator help topics from the drop-down help menu.

Windows Online Help. Information about Windows features is available through the Windows help system. Access Windows help as you would with any Windows application.

Setups

The following steps provide information on using the TLA7PG2 application.

Setting Up the Pattern Generator

Follow the steps below to set up the module program:

1. Power off the mainframe.
2. Install the pattern generator module in the mainframe.
3. Connect the probe to the pattern generator module. The probe cable is reversible so that you can connect the cable in either direction.
4. Apply power to the mainframe.
5. Open the pattern generator application window.
6. Power on the pattern generator by clicking on the ON/Off button in the pattern generator module icon.
7. Click on the Setup button to open the Setup window.

CAUTION. *Damage to the instrument can occur if you connect or disconnect the probes from the module while the mainframe is powered on.*

Setting Up the Module Setup Parameters

Follow the steps below to set up the module setup parameters:

1. Select the Module Setup parameters from the Setup window.
2. Click the Channel Setup tab.
3. Define the logical groups of channels and the channel names.
4. Click the Probe Setup tab.
5. Specify the probe details corresponding to the module.
6. Click Signals Setup.
7. Specify the backplane signals to be used for Signal Input and Signal Output.
8. Close the Setup window.
9. Click the Program icon in the System window.

Setting Up the Module Program

Follow the steps below to set up the module program:

1. Select the Block tab.
2. Define the pattern data for each block.
3. Click the Sequence tab.
4. Define the main pattern generator sequence program (series of blocks to be output by the pattern generator).
5. Click the Subsequence tab.
6. Define the nest of sequence definition.
7. Click the Event tab.
8. Define up to 8 events used by the sequencer and the probe inhibit control.
9. Close the Program window.

Connecting the Probes

Follow the steps below to connect the probes:

1. Ensure that the mainframe is powered off.
2. Install the pattern generator module in the mainframe.
3. Connect the probe to the pattern generator module. The probe cable is reversible so that you can connect the cable in either direction.

CAUTION. *To prevent damage to the pattern generator module or probe, do not connect or disconnect the pattern generator cables to or from the pattern generator module or probe while the logic analyzer is powered on. The recommended DUT (Device Under Test) and pattern generator power on/off sequence is as follows:*

Power on the DUT first, then power on the pattern generator. Power off the pattern generator and then power off the DUT.

Although the pattern generator probe cable appears to be a SCSI cable, it is not compatible with a SCSI cable; do not use a SCSI cable with the pattern generator module, or use the pattern generator probe cable with a SCSI instrument.

The probe is fragile; handle it carefully.

P6475 Power On/Off Procedure

The following procedures provide information to power on and power off the probes.

Standard Probes

Follow the procedures below to power on and power off the standard probes:

1. Power on the DUT
2. Power on the TLA

1. Power off the TLA
2. Power off the DUT

P6475

Follow the procedures below to power on and power off the P6475 variable probe:

1. Power on the DUT
2. Power on the P6475 (power switch on rear of probe)
3. Power on the TLA

1. Power off the TLA
2. Power off the P6475
3. Power off the TLA

Loading a Saved System

Follow the steps below to load a saved system:

1. Go to the File menu and select Load System.
2. Navigate to the directory where you saved your system.
3. Select the file and click Open.

***NOTE**. The saved system must exactly match the current system for all parts of the system to load.*

Loading Data

The Load Data application dialog box is accessible from a drop down menu when you click on File from the main toolbar.

This dialog box allows you to load the contents of the pattern generator system file. When you select the pattern generator system file, the modules that are saved in that file will be listed, and you can select a particular module.

When you click the OK button, the dialog loads the contents of that module in a new Program window. When you name the program window, a Name Window dialog box opens to allow you to specify a new name. If you do not specify a name, the operation is aborted.

Loading a Saved System File

The Load System application dialog box is accessible from a drop down menu when you click on File from the main toolbar.

This dialog box allows you to load a saved pattern generator system file. You can click on the Options button to open the Load System Options dialog box and indicate which modules to load from the saved system to the current system.

When you click Open, the application will bring up the Yes/No/Cancel prompt message.

- If you click Yes, the application will load the saved system without saving the current system.
- If you click No, the application will bring up the Save System As dialog if the current system is not associated with a saved system file. Or, for example, if the current system has been initially loaded from a Saved System File, the application will save the current system onto the associated file and then continue with the load operation.

***NOTE**. The default file name extension for the pattern generator system files will be <filename>.tpg.*

Merging Pattern Generator Modules

This section describes how to merge up to five pattern generator modules to form a wider, channel-width module.

Pattern Generator Merged Modules

A merged pattern generator module set consists of a master-pattern generator module and up to four slave-pattern generator modules. You merge the pattern generator modules in software. You do not need to physically connect them.

Rules for Merging Pattern Generator Modules

The following pattern generator module merging rules must be followed:

- The pattern generator modules are merged through software.
- The pattern generator modules must be physically adjacent.
- The pattern generator modules may not be merged across mainframes.
- Merged pattern generator modules of unequal memory depths will assume the depth of the shallowest pattern generator module.
- The pattern generator modules must have the same firmware version.
- When merged, the pattern generator module to the left is the master.

Refer to the pattern generator online help for additional help in merging pattern generator modules.

Importing and Exporting Data

The pattern generator export/import feature is available from the file menu when a block listing is the active view. The vector data for that block can be exported and imported. The possible formats for export and import are listed below.

Exporting/importing to or from a spreadsheet format enables the user to create and/or manipulate the pattern data in any of the various standard simulators and other tools supported by the Synapticad Waveformer. (Synapticad Waveformer is a third party tool that outputs waveforms in specific simulator tool format.)

Export

The pattern generator will export block data to:

- TLA text files (*.txt)
- Synapticad Spreadsheet files (*.txt)

Import

The pattern generator will import block data from:

- TLA text files (*.txt)
- Synapticad Spreadsheet files (*.txt)
- HP pattern generator (disk) files (*.hpd)

All of the data is assumed to be in hexadecimal radix.

If a data field has more data than the corresponding group width indicates, only the least significant bits of the data field will be used.

The block will be resized to reflect the data size in the file.

The pattern generator application will automatically create the channel grouping. Automatic channel grouping will delete the existing grouping. Channels are assigned to a group from most significant bit (MSB) to least significant bit (LSB), starting from the highest required channel and working down to 0. For example, for a 16 bit group, the channels would be assigned as A1(7), A1(6) … A0(0).

Importing TLA Text Files. In the TLA text format, the separator should be Tab. The Header and TimeStamp must be present.

Importing from HP Pattern Generator Files. In the HP-ASCII format, there can be data for up to 2 blocks in a single file, an Initialization block and a Main block. Initialization block is optional. All the data is assumed to be in hexadecimal radix.

The Main block data will be loaded into the active block and the initialization block data, if any will be loaded into a new block. The name of the new block will be the main block name suffixed with “init”.

If a block with this name already exists, then the new name is suffixed with #<number>. Starting from zero, the <number>is incremented, until the name becomes unique.

Pattern Editing

The Listing window in the pattern generator application allows the vector data to be edited by block, in numeric format.

You can open multiple pattern editing windows to allow selected data to be easily moved from one block to another using copy/paste.

The Listing window allows the vector data to be edited by block, in numeric format.

You can open multiple pattern editing windows to allow selected data to be easily moved from one block to another using copy and paste functions.

Columns

The Listing window allows the vector data to be edited by block, in numeric format.

You can open multiple pattern editing windows to allow selected data to be easily moved from one block to another using copy/paste.

References

References will help you find the time difference between two vectors. References are similar to cursors in the TLA series logic analyzers.

You can move the reference by clicking the right mouse button on the listing window and selecting the option Move Reference1 here or Move Reference2 here. You can also move References by highlighting the edit box present in the Reference bar and using the Spin button.

Data Area

The data area can by split vertically by dragging the split box from the left end of the horizontal scroll bar. This allows you to compare columns.

Clicking the right mouse button in the columns will display a pop-up menu containing items to manage the column display.

Clicking the right mouse button in the pattern data area will display a pop-up menu containing items to manage various items present in the listing window. This menu will have some of the frequently used items present in the menu bar.

You can select multiple rows by clicking on the first column using mouse and then dragging the selection. Please note that, if you don’t click on the first column and then copy the selection, only one cell will be copied.

Theory of Operation

This chapter describes the general operation of the pattern generator (PG) module and probe.

Module Overview

The module overview describes the basic operation of each functional circuit block.

The basic pattern generator module consists of the A20 Clock and VXI I/F board and the A50 PG board.

The *Diagram* section of this manual includes a block diagram and an interconnect diagram. The block diagram shows the functional blocks of the pattern generator and the probes. The interconnect diagram shows how the modules connect.

A20 Clock and VXI I/F Board

The A20 Clock and VXI I/F board contains the following circuits:

- Processor circuit
- VXI I/F circuit
- Clock circuit
- Power supply circuit

Processor circuit. The Processor circuit contains a 68340 microprocessor that controls the entire pattern generator. Commands and data that are sent to the pattern generator through the mainframe, pass through the VXI I/F, which resides on the 68340 bus. The 68340 bus also routes data between the Processor circuit and the PG board.

The Processor circuit also contains the instrument firmware. Upgrades to the firmware are made to the Flash ROM.

VXI I/F circuit. The VXI I/F circuit transfers commands and data between the module and the Slot 0 controller.

Clock circuit. The Direct Digital Synthesizer (DDS) uses a 10 MHz Clock signal from the VXI Bus as the reference signal for the phase lock loop (PLL) circuit.

A50 PG Board

The A50 PG board contains the following circuits:

- Sequencer Field Programmable Gate Array (FPGA) circuit
- Sequence RAM circuit
- Sequence Address Counter FPGA circuit
- Pattern Address Counter FPGA circuit
- Pattern RAM circuit
- ASIC Silver circuit
- Output Latch circuit
- Clock Control circuit
- VXI Local Bus Signal circuit
- CPU I/F FPGA circuit
- Power supply circuit

Sequencer FPGA. The Sequence RAM outputs a Sequence OP Code to the Sequencer FPGA circuit. This causes the Sequencer FPGA to generate the load and enable timing signals for the register and count of the SEQuence Address Counter FPGA and the Pattern Address Counter FPGA. The Sequencer FPGA also controls the jump sequence for events.

Sequence RAM. The Sequence RAM stores the Sequence OP Code and Sequence Data and consists of three SRAMs that have a 12 ns high-speed access time.

Sequence Address Counter FPGA. The Sequence Address Counter FPGA includes two registers (A and B). Each counter circuit stores data for the corresponding counter. Usually, one of two registers is used except in the case of an event jump. For an event jump, banks of two registers are swapped to load the jump sequence to the corresponding counter. Although the A register is used for the first time, they are swapped with the other registers at every jump process.

Pattern Address Counter FPGA. This circuit operates the same as the Sequence Address Counter FPGA above.

Pattern RAM. The Pattern RAM stores pattern data. Each Pattern Ram stores data for two channels. The Silver circuit has the capability of changing the dividing ratio of the Pattern RAM. A second Pattern RAM is reserved for storing the control data. This controls the dividing ratio of the divider.

X7 or X8 Shift SILVER ASIC. The Silver ASIC circuit is a high speed shift register that shifts data from the Pattern RAM. The circuit includes a divider that has the capability to change its dividing ratio. The dividing ratio is controlled by the data.

There are four dedicated SILVER ASICs for each probe (Probe A, Probe B, Probe C, and Probe D.)

Output Latch. The Output Latch circuit latches the output of the X7 or X8 Shift Silver ASIC for speed-up purposes. The probe derived data, which will be used to generate the Inhibit and the strobe signal, is also latched. The clock signals are supplied to the respective probe through the buffer.

Clock Control. The Clock Control Circuit generates clock signals for various circuits to operate synchronously with the clock signal from the A20 Clock and VXI I/F board.

The clock signal to the Clock Distributor circuit is supplied through the delay line for deskew purposes and to the buffer circuit through a 50 Ω coaxial cable. The output of the Clock Distributor circuit is supplied directly to the SILVER ASIC circuit. Also the Clock Distributor circuit is supplied to the module Output Latch circuit through the delay line to adjust the timing. The divider divides the clock signal by two. Either the original clock signal or the divided clock signal is selected by the selector circuit depending on the channel mode selection (half or full). The signal is supplied to the probe through the delay line to adjust the timing.

VXI Local Bus Signal. When the board is used as the Master Module, the clock signal is selected from the A20 Clock and VXI I/F board. When the board is used as the Slave1 through Slave4 module, the clock signal is selected from the Master Module through the VXI local bus. Jump-related signals are also switched between self-generated signals and signals from the Master Module, depending on the board usage of the Master or Slave.

CPU I/F FPGA. The CPU I/F FPGA circuit is configured by the EPROM at the system start up. This circuit decodes the address data from the CPU and establishes various board settings. The CPU also monitors various board circuits.

Power Supplies. The power supplies receive power from the VXI bus backplane. Power is supplied to corresponding circuits through the Filter circuit. The A20 Clock and VXI I/F board also supply power to these power supplies through the power connector that compensates in case of a shortage of power from a single slot of the VXI bus.

A relay is provided to detect overheating of a probe. The relay will shut off power to the probe if overheating is detected.

Probe Overview

The probe overview describes the basic operation of each functional circuit block. There are five standard probes and one variable probe available for use with the TLA7PG2 pattern generator.

The *Diagram* section of this manual includes block diagrams for the standard probes and the variable probe. These diagrams show the functional blocks of the probes.

Standard Probes

The following standard probes are available for use with the pattern generator:

- The P6470 TTL/CMOS probe includes the A95 board
- The P6471 ECL probe includes the A90 board
- The P6472 PECL/LVPECL includes the A83 board
- The P6473 LVCMOS includes the A81 board
- The P6474 LVDS includes the A82 board

The standard probes contains the following circuits:

Input Latch. The Input Latch circuit latches the channel data through the probe cable from the A50 board. At the rising edge of the clock signal, data is latched into Bank-A. At the falling edge of the clock signal, data is latched into Bank-B. When the channel is in the half channel mode, only Bank-A is used.

Output Latch. The Output Latch circuit latches the data from the input circuit to achieve simultaneous output of all data from every probe channel, regardless of what channel mode is used.

Output Driver. The Output Driver (Buffer) circuit translates the signal level and drives the DUT.

Event Input. The Event Input circuit routes the external event input signal from the probe output connector to the A50 PG board.

Sensor. The Sensor circuit senses the inner temperature of the probe to detect overheating and then reports the findings to the CPU.

Variable Probe

The P6475 variable probe is available for use with the pattern generator. The variable probe includes the A80 Variable board.

The Variable probe contains the following circuits:

Input Latch,The Input Latch circuit latches the channel data through the probe cable from the A50 board. At the rising edge of the clock signal, data is latched into Bank-A. Bank-B is not available for the A80 Variable board.

Output Latch. The Output Latch circuit latches the data from the input circuit to achieve simultaneous output of all data from every probe channel, regardless of what channel mode is used.

Delay . The Delay circuit supports variable delay for CH6 and CH7.

CH6, 7 Mix. The CH6,7 Mix circuit supports logical function between CH6 and CH7.

Pin Driver. The Pin Driver circuit supports variable output voltage and drives the DUT.

Event Input. The Event Input circuit routes the external event input signal from the probe output connector to the A50 PG board.

Sensor. The Sensor circuit senses the inner temperature of the probe to detect overheating and then reports the findings to the CPU.

Performance Verification

This chapter contains procedures for performing the functional verification procedures and performance verification procedures for the TLA7PG2 Pattern Generator module and the pattern generator probes. You should perform the performance verification procedures once per year or following repairs that affect certification.

Refer to the *Install the PV/Adjust Software* section on page 2–2 to load the PV setup files.

Verification Summary

Functional verification procedures verify the basic functionality of the instrument inputs, outputs, and basic instrument actions. These procedures include power-on diagnostics, extended diagnostics, manual check procedures and they can be used for incoming inspection purposes.

The tests are grouped by instrument, however some preliminary setups are at the beginning of this section.

Functional Verification. Refer to the following pages for functional verification procedures:

TLA7PG2 Procedures	Page 4–14
P6470 Procedures	Page 4–40
P6471 Procedures	Page 4–51
P6472 Procedures	Page 4–58
P6473 Procedures	Page 4–66
P6474 Procedures	Page 4–76
P6475 Procedures	Page 4–88

Performance Verification. Refer to the following pages for probe tests for the performance verification portion of the section.

TLA7PG2 Maximum Operating Frequency	Page 4–106
P6475 Delay Accuracy Check	Page 4–112

Certification procedures certify the accuracy of an instrument and provide a traceability path to national standards. The P6475 Delay Accuracy procedure provides the only certifiable parameter.

Performance verification procedures confirm that a product meets or exceeds the performance requirements for the published specifications documented in the *Specifications* section of this manual.

Table 4–1 lists the various probes available for use with the TLA7PG2 Pattern Generator, the verifications tests, the setup file names and Termination board requirements. A check mark in the probe column means that you can use that particular probe to send signals to the Termination board. Testing with a particular probe does not necessarily verify the functionality of the the probe. A probe must be attached to the pattern generator for all tests except for the extended diagnostics.

Table can be used to quickly select the functional verification test, the probe that you are using, and the setup file that is required. Table 4–1 also notes if a Termination board is required for the test. The Termination board is not used with the P6475.

Table 4-1: Pattern generator module verification procedures

Test	Setup file name	Termination board required	TLA7PG2	P6470	P6471	P6472	P6473	P6474	P6475
Module self tests and power-on diagnostics	NA								
Extended diagnostics	NA								
External clock input (Half, Normal)	TP2EXCLK.TPG		√						
External clock input (Half, Invert)	TP3EXCLK.TPG		√						
External clock input (Full)	TP4EXCLK.TPG		√						
Merge operation	TP9PG.TPG		√						
Deskew function	TP10DSKW.TPG		√						

Table 4-1: Pattern generator module verification procedures (Cont.)

Test	Setup file name	Termination board required	TLA7PG2	P6470	P6471	P6472	P6473	P6474	P6475
Internal clock frequency	TP1CLK.TPG	√	√	√	√	√	√	√	√
Sequence and data output (probe A)	TP5PG0.TPG	√	√	√	√	√		√	
	TP5PG1.TPG	√	√				√		√
	TP5PG2.TPG		√						√
Sequence and data output (probe B)	TP6PG0.TPG	√	√	√	√	√		√	
	TP6PG1.TPG	√	√				√		√
Sequence and data output (probe C)	TP7PG0.TPG	√	√	√	√	√		√	
	TP7PG1.TPG	√	√				√		√
Sequence and data output (probe D)	TP8PG0.TPG	√	√	√	√	√		√	
	TP8PG1.TPG	√	√				√		√
Inhibit function (by data)	TP14INH.TPG	√	√						
Inhibit function (by event using Signal1 Output and Signal1 Input)	TP12INH.TPG	√	√	√			√	√	√
Inhibit function (by external inhibit input)	TP13INH.TPG		√	√			√	√	√
P6475 Data format and CH6 output mode test	TP19V.TPG	√							√

Table 4-1: Pattern generator module verification procedures (Cont.)

Test	Setup file name	Termination board required	TLA7PG2	P6470	P6471	P6472	P6473	P6474	P6475
TLA7PG2 Maximum Operating Frequency (probe A)	TP15PV0.TPG	√	√	√	√	√		√	
	TP15PV1.TPG	√	√				√		√
TLA7PG2 Maximum Operating Frequency (probe B)	TP16PV0.TPG	√	√	√	√	√		√	
	TP16PV1.TPG	√	√				√		√
TLA7PG2 Maximum Operating Frequency (probe C)	TP17PV0.TPG	√	√	√	√	√		√	
	TP17PV1.TPG	√	√				√		√
TLA7PG2 Maximum Operating Frequency (probe D)	TP18PV0.TPG	√	√	√	√	√		√	
	TP18PV1.TPG	√	√				√		√
P6475 Delay Accuracy Check	TP19V.TPG		√						√

Equipment Required

These procedures use external, traceable signal sources to directly test characteristics that are designated as checked (✓) in the *Specifications* chapter of this manual. Table 4–2 on page 4–5 shows the required equipment list. Always warm up the equipment for 30 minutes before beginning the procedures.

Table 4-2: Test equipment

Item number and description	Minimum requirements	Example
1. Mainframe	TLA715 Portable mainframe or TLA721 Benchtop mainframe with a TLA7PG2 Pattern Generator module installed	
2. Oscilloscope	1 GHz bandwidth Delay time accuracy ±25 ppm over any ≥ 1 ms interval	Tektronix TDS7104
3. DSO probes (not used with P6475)	Three required, with < one-inch ground leads	Tektronix P6243 or P6245 probe, with std. accessories
4. Termination board (not used with P6475)	Two required	Tektronix part number: 067-A018-00
5. Function generator	Amplitude: 4 V Offset: 2 V (50 Ω termination) Frequency: 1 MHz or higher	Tektronix AFG310, AWG2005, or AWG2021
6. Power supply	Voltage: +5 V Current: 1 A	CPS250, 5V fixed output
7. BNC Cable	Impedance: 50 Ω, Length: 24 in (two required)	Tektronix part number: 012-1342-XX
8. T-Connector	One required	Tektronix part number: 103-0030-XX
9. BNC to SMB cable	Four required	Tektronix part number: 012-1459-00

P6475 Variable Probe Test Record

Photocopy this test record and use to record the performance test results for your P6475 Variable probe.

P6475 Variable Probe Test Record

Date of Test: _____ Technician: _____

Serial Number: _____

Function tested	Delay Range	Delay	Minimum	Test Data	Maximum
Delay Accuracy					
CH6 and CH7	0 - 20 ns	0 ns	-0.80 ns	_	0.80 ns
		10 ns	8.90 ns	_	11.10 ns
		20 ns	18.60 ns	_	21.40 ns
	15 - 30 ns	15 ns	13.75 ns	_	16.25 ns
		30 ns	28.30 ns	_	31.70 ns
	25 - 40 ns	25 ns	23.45 ns	_	26.55 ns
		40 ns	38.00 ns	_	42.00 ns
	35 - 50 ns	35 ns	33.15 ns	_	36.85 ns
		50 ns	47.70 ns	_	52.30 ns

Setup Procedures

This subsection provides setup procedures to that must be completed prior to running the function and performance procedures.

Power On/Off Procedures

Follow the procedures below to power on and power off the instruments. Refer to page 4–88 for *P6475 Power On/Off* procedures.

1. Power on the DUT
2. Power on the TLA

1. Power off the TLA
2. Power off the DUT

Install the Pattern Generator Module

Install the pattern generator module in the TLA700 mainframe and complete the following steps in this subsection:

CAUTION. *Power off the TLA700 mainframe before removing or installing the pattern generator module. Power off the mainframe while connecting or disconnecting the probes to the pattern generator module. You can damage the pattern generator if you connect or disconnect the probe while the mainframe is powered on.*

1. Power off the TLA700 mainframe.
2. Install the pattern generator module in the TLA700 mainframe.
   a. If you are testing a single module, install the module in any slot.
   b. If you are testing multiple modules, install one pattern generator module in the lower-numbered slot. Install the pattern generator module to be tested in the adjacent higher-numbered slot.
3. Connect the probe to the Probe-A connector of the pattern generator module using the probe cable. Connect four sets of the same probe to the pattern generator module.
4. Power on the mainframe and test equipment and allow a 30-minute warm up before continuing with any procedures in this section.

Pattern Generator Setup Files

The PV/Adjust software used to verify the pattern generator modules consists of setup files rather than executable software. To use the pattern generator setup files complete the following steps:

1. Verify that your module configuration matches the setup as called for in the written procedure (for some of the setups you will need to merge or unmerge modules).
2. Select Load Module from the File menu; the Load Module dialog box appears.
3. Click the Browse button and navigate to the C:\Program Files\Tektronix Pattern Generator\PV folder.
4. Double-click on the file name; the Load Module dialog box reappears with the file name and module name under the Module list.
5. Click OK to load the module setup. A dialog box may appear reminding you that the current module settings and data will be lost.
6. Click Yes to confirm your choice.
7. Follow the remaining written procedures.

Complete each of the following procedures in sequence. Use the external test equipment together with the tables and illustrations in this section to verify the functionality of the pattern generator modules and probes as indicated.

Module Self Tests and Power-On Diagnostics

During power-on, the installed modules perform an internal self test to verify basic functionality. No external test equipment is required. The self tests require only a few seconds for each module. The front-panel indicators may blink during the self test. Table 4–3 summarizes the function of each indicator.

Table 4-3: Front panel indicators

Function	Description
Ready LED (green)	The Ready LED illuminates when the module is ready for operation.
Accessed LED (amber)	The Accessed LED illuminates each time the mainframe communicates with the pattern generator module.
Output LED (amber)	The Output LED illuminates while the probe is asserting a high or low level at the output pins. It will not illuminate while the output pins are in the high impedance state when the HI-Z on Stop function is active. If you have a P6471 ECL probe, the LED will always be illuminated because the probe does not support Hi-Z on Stop.

Table 4-3: Front panel indicators (Cont.)

Function	Description
Started LED (green)	The Started LED illuminates while the pattern generator runs or is waiting for an event.
Waiting LED (green)	The Waiting LED illuminates while the pattern generator is waiting for an event.

Next, the power-on diagnostics are run. If any self tests or power-on diagnostics fail, the instrument displays the Diagnostics property sheet. If any diagnostics fail, run the extended diagnostics to help isolate the problem.

Extended Diagnostics

The following procedure checks the basic functionality of the pattern generator module using the extended diagnostics. Before beginning this procedure, be sure that no active signals are applied to the instrument. Certain diagnostic tests may fail if signals are applied to the probe during the test.

1. In the pattern generator application, go to the System menu and select System Diagnostics.
2. Click the Extended Diagnostics tab.
3. Select the top level test of the pattern generator module and then click the Run button.

   The diagnostics will perform each one of the tests listed in the menu under the module selection. All tests that displayed an Unknown status will change to a Pass or Fail status depending on the outcome of the tests.
4. Scroll through the test results and verify all tests pass. If any tests fail, refer to Table 4–4 to identify the fault.

Table 4- 4: Extended Diagnostic test Items and faulty component

Test item	Faulty component
ROM Test	A20 CLOCK and VXI I/F board
RAM Test	A20 CLOCK and VXI I/F board
Register Read Test	A20 CLOCK and VXI I/F board A50 PG board A90 ECL board A95 TTL/CMOS board A80 Variable probe board A81 LVCMOS board A82 LVDS board A83 PECL/LVPECL
PLL Lock Test	A20 CLOCK and VXI I/F board
Pattern Memory Test	A50 PG board
Sequence Memory Test	A50 PG board
Event Memory Test	A50 PG board
Signal Test	A50 PG board

In Case of Problems

If any tests fail, use the following steps to troubleshoot problems:

1. Check all test equipment for improper or loose connections.
2. Check that all test equipment is powered on and has the proper warm-up time.
3. Rerun mainframe or module diagnostics.
4. Run the tests a second time to verify the failure.
5. If tests continue to fail, refer to *Troubleshooting* in the *Maintenance* section of this manual for corrective action or contact your local Tektronix representative.

Common Setups for the Function Generator

These function generator setups are the same for all tests. Set up CH1 of the function generator as follows:

Amplitude:		
	P6470	2 V_{p-p} (50 Ω termination)
	P6471, P6472, P6475	505 mV_{p-p} (50 Ω termination)
	P6473, P6474	1.5 V_{p-p} (50 Ω termination)
Offset:		
	P6470	1 V (50 Ω termination)
	P6471	-650 mV (50 Ω termination)
	P6472 PECL mode	3.5 V (50 Ω termination)
	P6472 LVPECL mode	1 V (50 Ω termination)
	P6473, P6474	750 mV (50 Ω termination)
	P6475	1.25 V (50 Ω termination)
Waveform		Square wave

Connect the DSO Probe to the Oscilloscope

Connect the DSO probe to the oscilloscope inputs. Refer to Figure 4–1 for termination board pin identification.

- Use J110, J160, or J210 GND pins (2 through 36) for GND test points.
- Use J110, J160, or J210 (D0 through D15, STB, CLK) for termination board signal connection oscilloscope probing.

Connect the TLA7PG2 Probes to the Termination Board

Connect the pattern generator probe to the Termination board so that the probe labels are on top. Check individual procedures list for required equipment.

You can connect or disconnect the probes to or from the termination board while the power is on.

Connect the Power Supply

Check individual procedures list for required equipment. Follow the steps below to connect the termination board to an external power supply:

1. Connect the +5, V output of the power supply to J365 on the Termination board.
2. Connect the power supply ground to J350 on the Termination board.

Termination Board

The Termination board is required for testing the P6470, P6471, P6472, P6473, and P6474 probes. Refer to Figure 4–1 for connector locations.

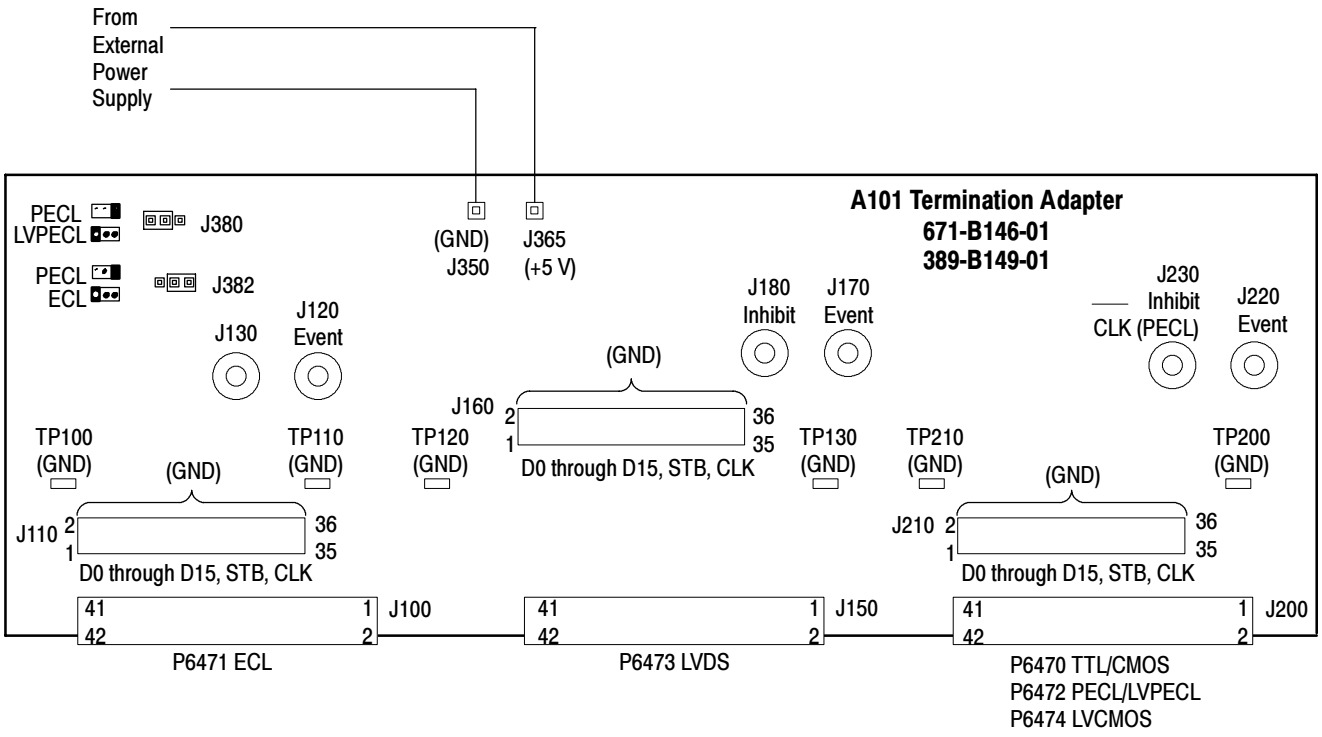


Figure 4- 1: Termination Board

Functional Verification Procedures

The tests in this section confirmation the functionality of these products when the following requirements are met:

- The PV/Adjust software must be loaded on the hard disk drive.
- The pattern generator module must be installed in a mainframe, operating for at least 30 minutes, and operating at an ambient temperature between +20° C and +30° C.
- The instrument must be in an operating environment within the limits described in the *Specifications* section of the *Tektronix Logic Analyzer Family User Manual*.

TLA7PG2 Functional Verification Procedures

The following procedures verifies that the TLA7PG2 module is operating correctly.

TLA7PG2 External Clock Input Test

The External Clock Input test confirms the external clock input operation of the pattern generator module.

Setup files	TP2EXCLK.TPG, TP3EXCLK.TPG, TP4EXCLK.TPG
Equipment	Termination board (item 4) (not used with P6475) TDS7104 Digitizing Oscilloscope (item 2) P6245 1 MΩ 10X Oscilloscope probe (Item 3) (not used with P6475) CPS250 Power supply (item 6) (not used with P6475) AFG310 Function generator (item 5) Two BNC cables (item 7) T-connector (item 8) (not used with P6475)
Prerequisites	Connected Pattern generator probe Test equipment connected as shown in Figure 4-2 or Figure 4-3 Diagnostics pass

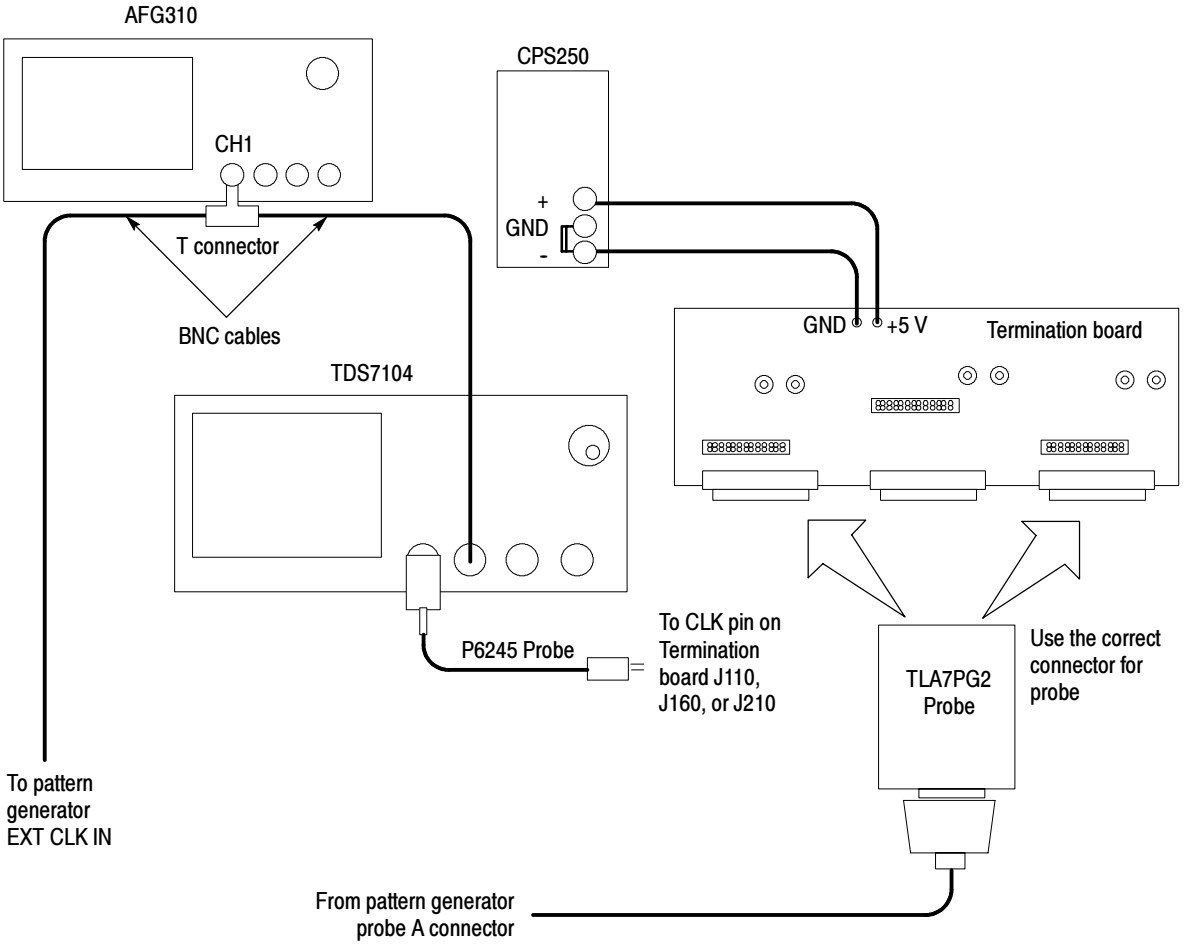


Figure 4-2: External Clock Input connections using a P6470, P6471, P6472, P6473, or P6474

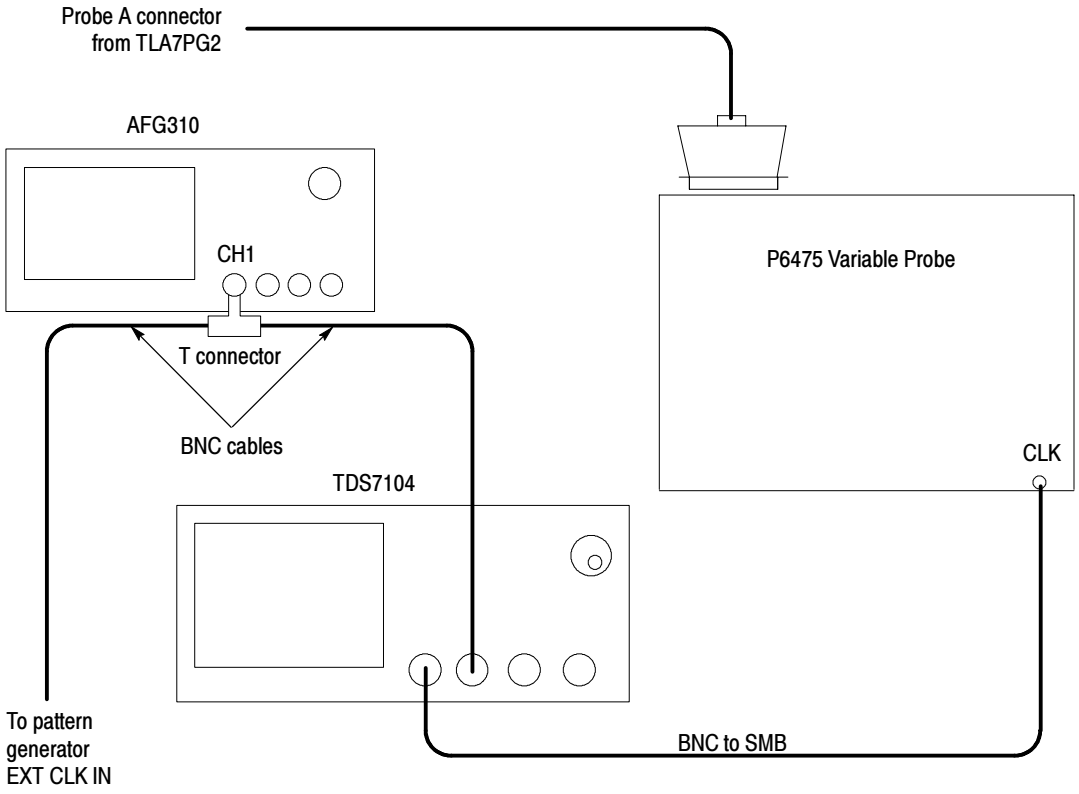


Figure 4-3: External Clock Input connections using a P6475

1. Connect all equipment as shown in Figure 4–2 or Figure 4–3.
2. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
3. Set the oscilloscope controls as follows:

Displayed channel:	CH1, CH2
Vertical axis (CH1):	
P6470, P6473, P6474	2 V/div
P6471, P6472, P6475	500 mV/div
Vertical axis (CH2):	
P6470, P6473, P6474	2 V/div
P6471, P6472, P6475	500 mV/div
Vertical position (CH1):	
P6470, P6473, P6474, P6475	-2.00 div
P6471, P6472	1.00 div

Vertical position (CH2):	
P6470, P6473, P6474, P6475	-2.00 div
P6471, P6472	1.00 div
Vertical offset (CHx):	
P6472 PECL mode	5 V
P6472 LVPECL mode	3.3 V
P6470, P6471, P6473, P6474, P6475	0.0 V
Bandwidth:	Full
Input coupling (CH1, CH2):	DC
Input impedance (CH1, CH2):	50 Ω
Horizontal axis:	200 ns/div
Record length:	5000
Trigger mode:	NORM
Trigger slope:	Rise
Trigger source:	CH2
Trigger level:	
P6472 PECL mode	3.7 V
P6470, P6472 LVPECL mode	2 V
P6471	-1.3 V
P6473, P6474	1.65 V
P6475	0.5 V
Trigger coupling:	DC
Trigger position:	50%

4. Set up CH1 on the function generator as follows:

Amplitude	1 V_{p-p} (50 Ω termination)
Offset	500 mV (50 Ω termination)
Frequency	1 MHz
CH1	ON

Half, Normal. Use the TP2EXCLK.TPG module setup file.

5. Load the TP2EXCLK.TPG module setup file.

6. Start the pattern generator.

7. Verify that the leading edge of the 1 MHz clock signal is synchronized with the leading edge of the CH2 waveform.
8. Stop the pattern generator.

Half, Invert. Use the TP3EXCLK.TPG module setup file.

9. Load the TP3EXCLK.TPG module setup file.
10. Start the pattern generator.
11. Verify that the trailing edge of the 1 MHz clock signal is synchronized with the leading edge of the CH2 waveform.
12. Stop the pattern generator.

Full. Use the TP4EXCLK.TPG module setup file.

13. Load the TP4EXCLK.TPG module setup file.
14. Start the pattern generator.
15. Verify that the leading edge of the 1 MHz clock signal is synchronized with the leading edge of the CH2 waveform.
16. Stop the pattern generator.

TLA7PG2 Internal Clock Frequency Test

The Internal Clock Frequency test confirms the frequency of the pattern generator module internal clock with the probe.

Setup files:	TP1CLK.TPG
Equipment	Termination board (item 4) (not used with P6475) TDS7104 Digitizing Oscilloscope (item 2) P6245 1 MΩ 10X Oscilloscope probe (Item 3) (not used with P6475) CPS250 Power supply (item 6) (not used with P6475) BNC to SMB cable (item 9)
Prerequisites	Connected pattern generator probe Connect the test equipment as shown in Figure 4-16 Diagnostics pass

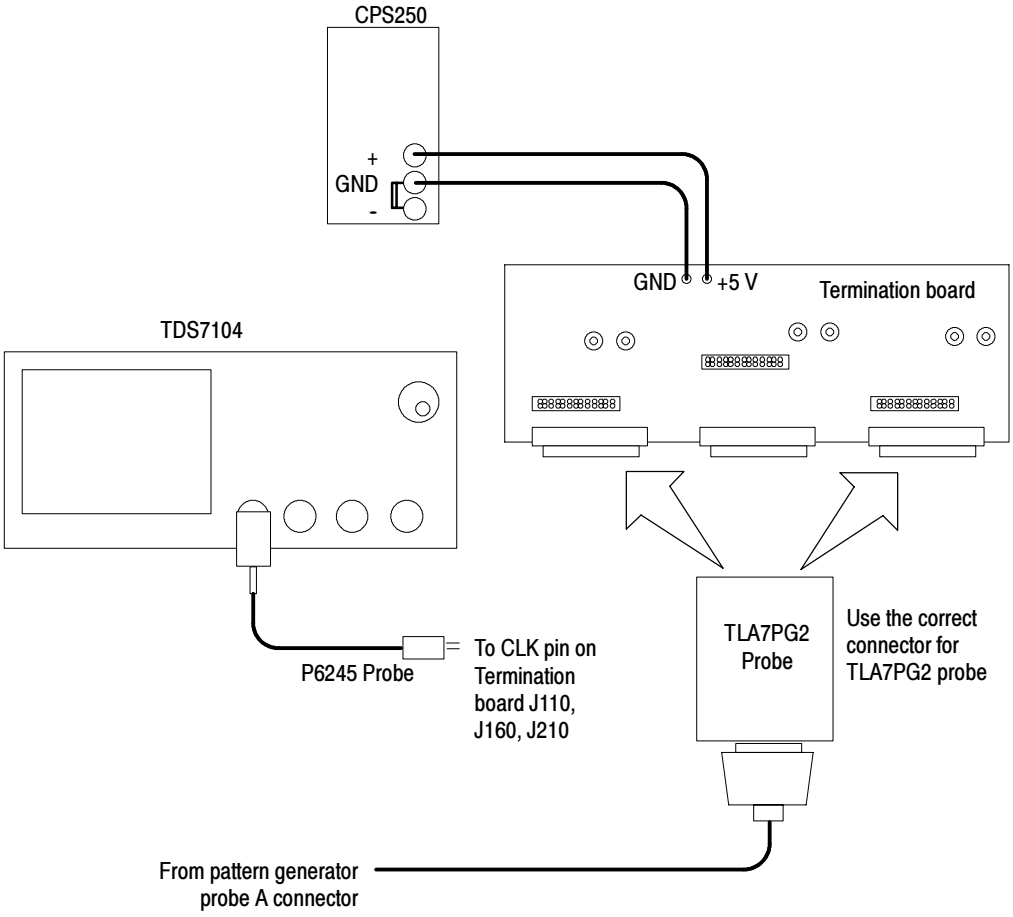


Figure 4- 4: Internal Clock Frequency connections using a P6470, P6471, P6472, P6473, or P6474

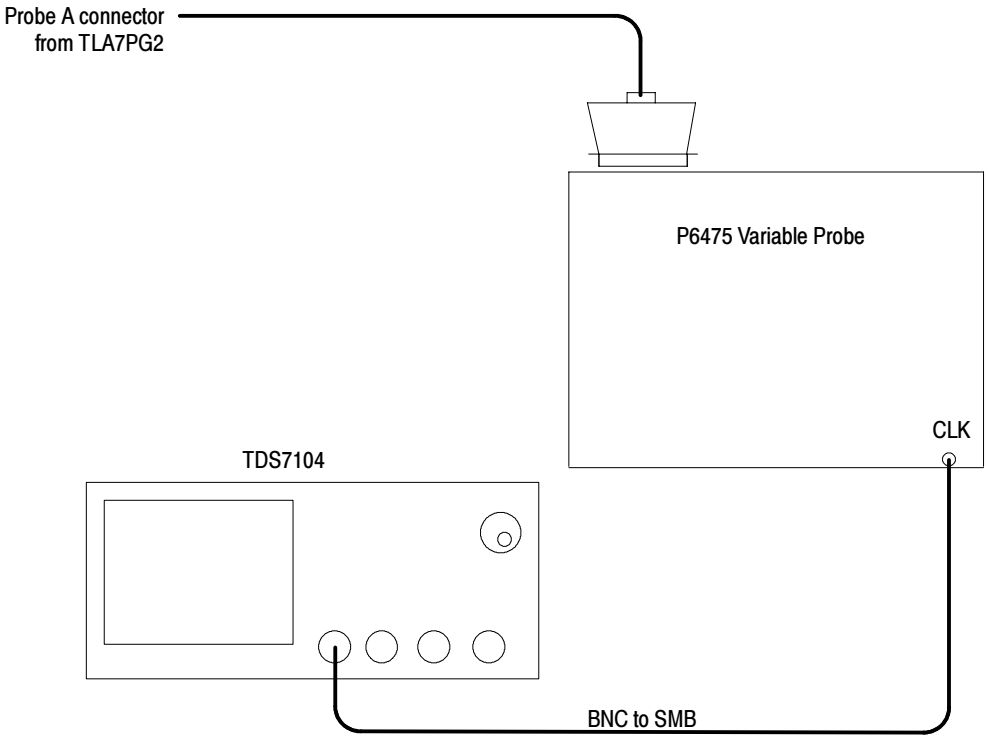


Figure 4- 5: Internal Clock Frequency connection using a P6475

1. Connect all equipment as shown in Figure 4–4 or Figure 4–5.
2. Set up the oscilloscope by pressing Setup, Factory, and then press OK Confirm Factory Init to return the oscilloscope to the default condition.
3. Set the oscilloscope controls as follows:

Displayed channel:	CH1
Vertical axis (CH1):	
P6470, P6473, P6474	1 V/div
P6471, P6472, P6475	500 mV/div
Vertical position (CH1):	
P6470, P6473, P6474, P6475	-2.00 div
P6471, P6472	1.00 div
Vertical offset (CHx):	
P6470, P6471, P6473, P6474, P6475	0.0 V
P6472 PECL mode	5 V
P6472 LVPECL mode	3.3 V
Bandwidth:	Full
Input coupling:	DC
Input impedance:	50 Ω
Horizontal axis:	1 ns/div
Record length:	5000
Trigger mode:	NORM
Trigger source:	CH1
Trigger slope::	Rise
Trigger level:	
P6470	2 V
P6471	-1.3 V
P6472 PECL mode	3.7 V
P6472 LVPECL mode	2 V
P6473	1.65 V
P6474	1.65 V
P6475	0.5 V
Trigger coupling:	DC
Trigger position:	50%

4. Load the TP1CLK.TPG module setup file. When the file is loaded, the pattern generator clock period will be set to 3.7313 ns internally.
5. Click the Setup icon in the pattern generator application window and change the internal clock period to 9.99 ns.
6. Start the pattern generator.
7. Verify that the frequency of the pattern generator output signal is 100.1 MHz.
8. Stop the pattern generator.
9. Set the pattern generator clock period to 5.0000 μs.
10. Start the pattern generator.
11. Set the oscilloscope Horizontal axis setting to 1.00 μs/div.
12. Verify that the frequency of the pattern generator output signal is 200 kHz.
13. Stop the pattern generator.
14. Set the pattern generator clock period to 1.0000 s.
15. Start the pattern generator.
16. Set the oscilloscope Horizontal axis setting to 200 ms/div.
17. Verify that the frequency of the pattern generator output signal is about 1 Hz.
18. Stop the pattern generator.

TLA7PG2 Merge Operation Test

This procedure confirms that the pattern generator merges properly.

Setup files:	TP9PG.TPG
Equipment	Two termination boards (item 4) (not used with P6475) TDS7104 Digitizing Oscilloscope (item 2) Two P6245 1 MΩ 10X Oscilloscope probes (Item 3) (for P6470, P6471, P6472, P6473, P6474) Three BNC to SMB cables (item 9) (for P6475 only) CPS250 Power supply (item 6) (not used with P6475) AFG310 Function generator (item 5) One BNC cable (item 7) (not used with P6475)
Prerequisites	Pattern generator modules merged, module under test in the higher-numbered slot Connected pattern generator probe Test equipment connected as shown in Figure 4-6 for standard probes or Figure 4-7 for variable probe. Diagnostics pass

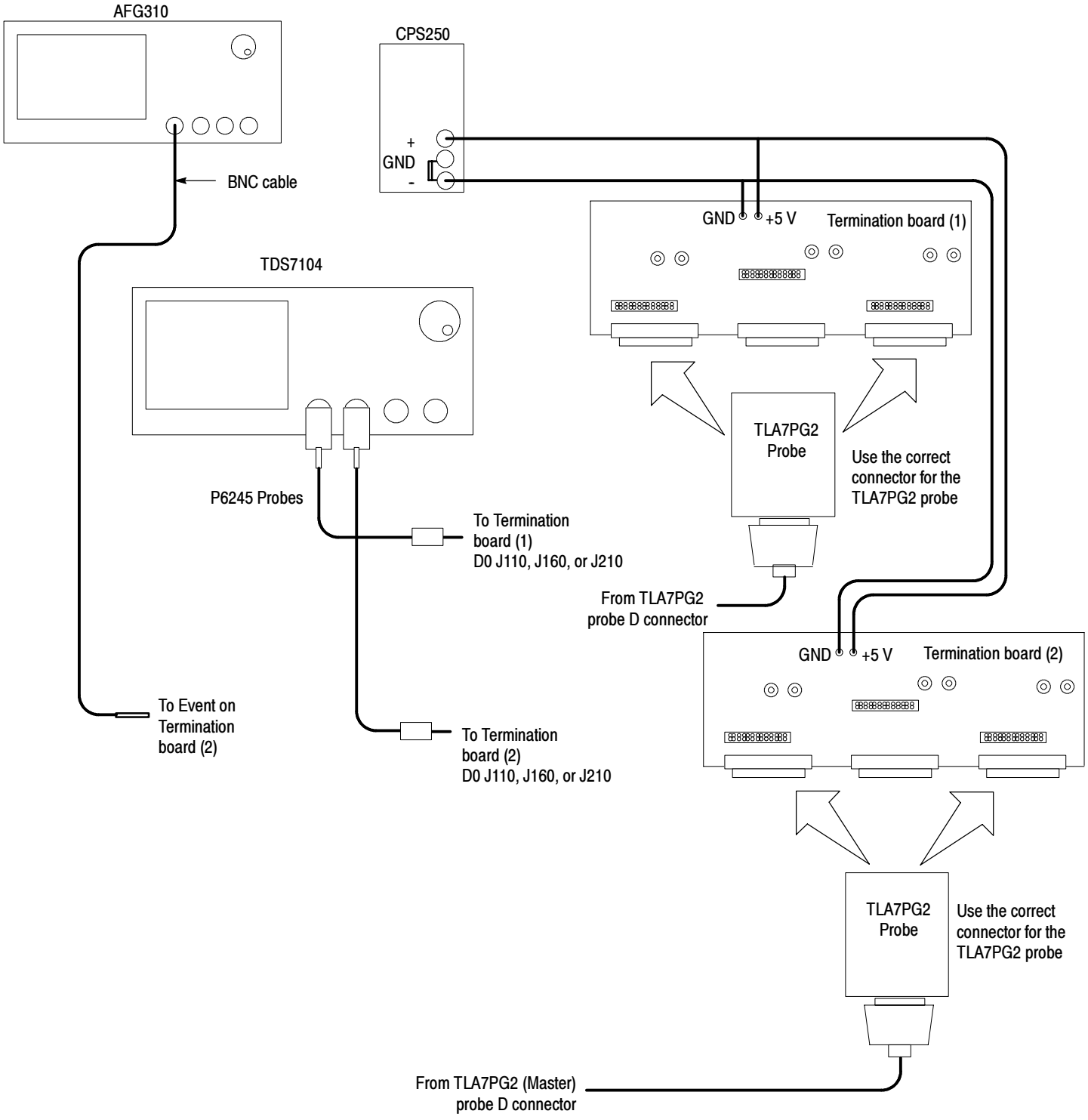


Figure 4- 6: Merge operation connections using P6470, P6471, P6472, P6473, or P6474 probes

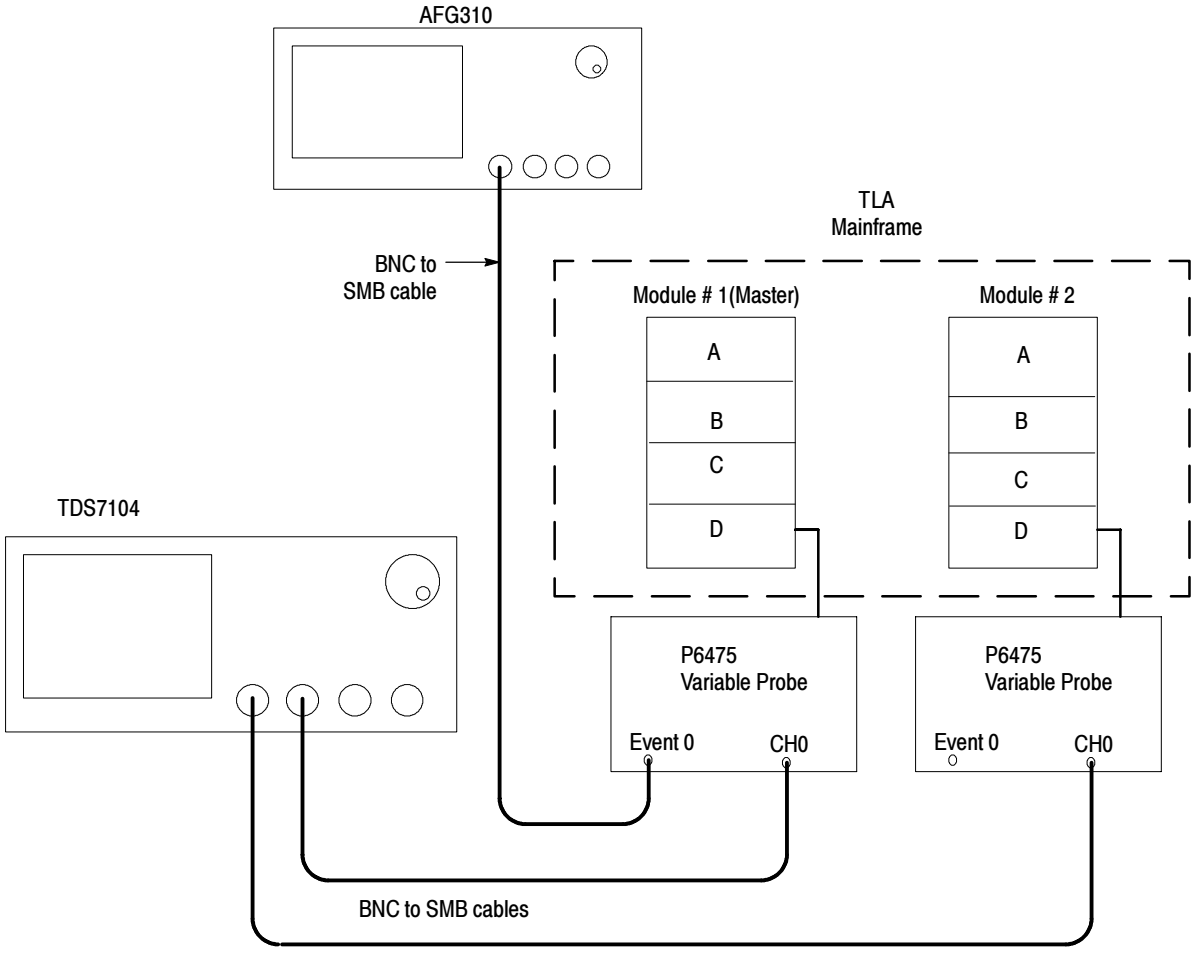


Figure 4-7: Merge operation connections using P6475 probe

1. Connect all equipment as shown in Figure 4–6 or Figure 4–7.
2. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
3. Set the oscilloscope controls as follows:

Displayed channel:	CH1, CH2
Vertical axis (CH1, CH2):	
P6470, P6473, P6474	5 V/div
P6471, P6472, P6475	1 V/div
Vertical position (CH1):	
P6470, P6473, P6474, P6475	2.50 div
P6471, P6472	4.00 div

Vertical position (CH2):	
P6470, P6473, P6474, P6475	0.50 div
P6471, P6472	2.00 div
Vertical offset (CHx):	
P6472 PECL mode	5 V
P6472 LVPECL mode	3.3 V
P6470, P6471, P6473, P6474, P6475	0.0 V
Bandwidth:	Full
Input coupling (CH1, CH2):	DC
Input impedance (CH1, CH2):	50 Ω
Horizontal axis:	1 μs/div
Record length:	5000
Trigger mode:	AUTO
Trigger slope:	Rise
Trigger source:	CH1
Trigger level:	
P6472 PECL mode	3.7 V
P6470, P6472 LVPECL mode	2 V
P6471	-1.3 V
P6473, P6474	1.65 V
P6475	0.5 V
Trigger coupling:	DC
Trigger position:	50%

4. Set up CH 1 of the function generator as follows:
   - Frequency 200 kHz
   - CH1 ON
5. If you have not already done so, complete the following steps to merge the pattern generator module under test to the reference module:
   a. Select System Configuration from the System menu in the pattern generator application.
   b. Click the Merge button between the reference module and the module under test to merge the two modules. (Figure 4–8 shows an example where PG6 consists of two merged modules, while PG3, PG4, and PG5 are unmerged modules as; note the merge buttons.)

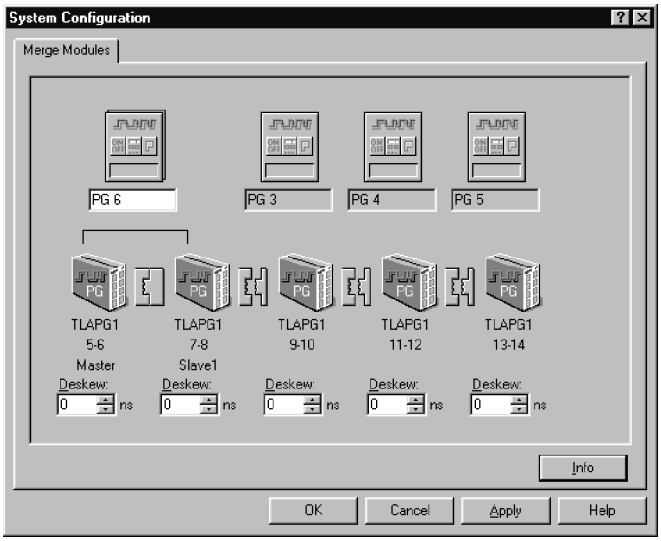


Figure 4-8: Merged and unmerged modules in the Merge Modules window

   c. Click OK to save the changes.
6. Load the TP9PG.TPG module setup file.
7. For P6473 and P6475:
   a. Open the Program window and select the Event tab.
   b. Change the event definition of EVENT1, EVENT2, EVENT3, and EVENT4 from 000000011 to 000000001.
8. Start the pattern generator.

9. Verify that the CH1 waveforms are similar to the waveforms shown in Figure 4-9. Notice the position of the strobe pulse in the figure.

10. Connect the CH2 oscilloscope probe to the D0 connector on the termination Board. Verify that the output signal data pattern is similar to the waveform shown in Figure 4-9.

11. Stop the pattern generator.

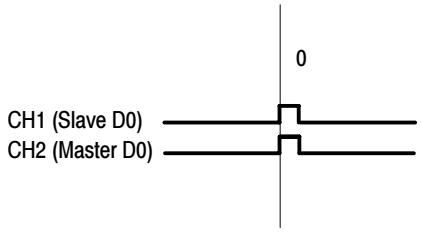


Figure 4-9: Timing Chart

TLA7PG2 Deskew Function Test

This procedure confirms the deskew function of the pattern generator module.

Setup files:	TP10DSKW.TPG
Equipment	Two termination boards (item 4) (not used with P6475) TDS7104 Digitizing Oscilloscope (item 2) Two P6245 1 MΩ 10X Oscilloscope probe (Item 3) (use with P6470, P6471, P6472, P6473, P6474 probes) Two BNC to SMB cables (item 9) (for P6475 only) CPS250 Power supply (item 6) (not used with P6475)
Prerequisites	Pattern generator modules merged, module under test in the higher-numbered slot Connected pattern generator probe Test equipment connected as shown in Figure 4-10 or Figure 4-11 Diagnostics pass

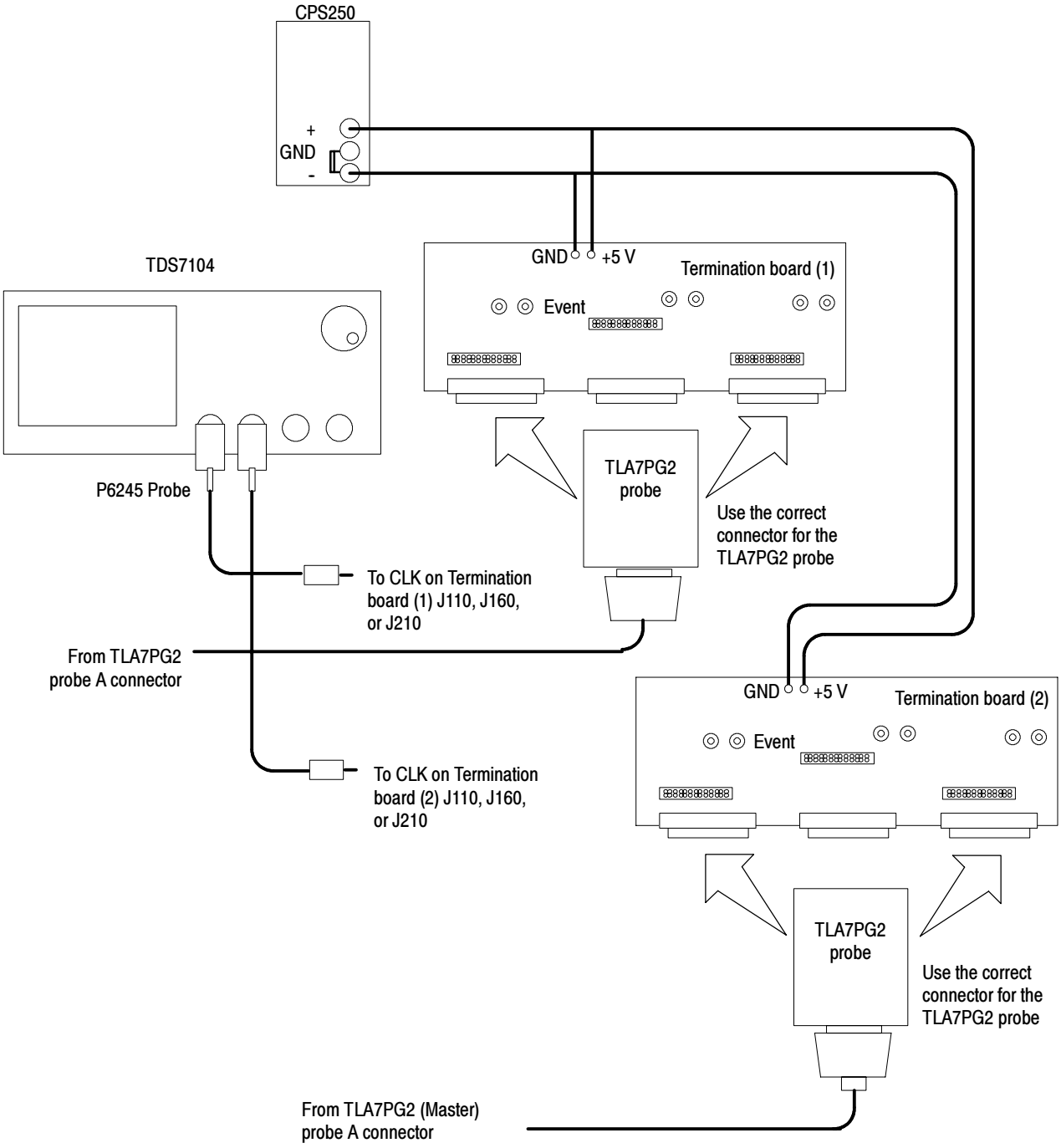


Figure 4-10: TLA7PG2 Deskew function connections using a P6470, P6471, P6472. P6473, or P6474

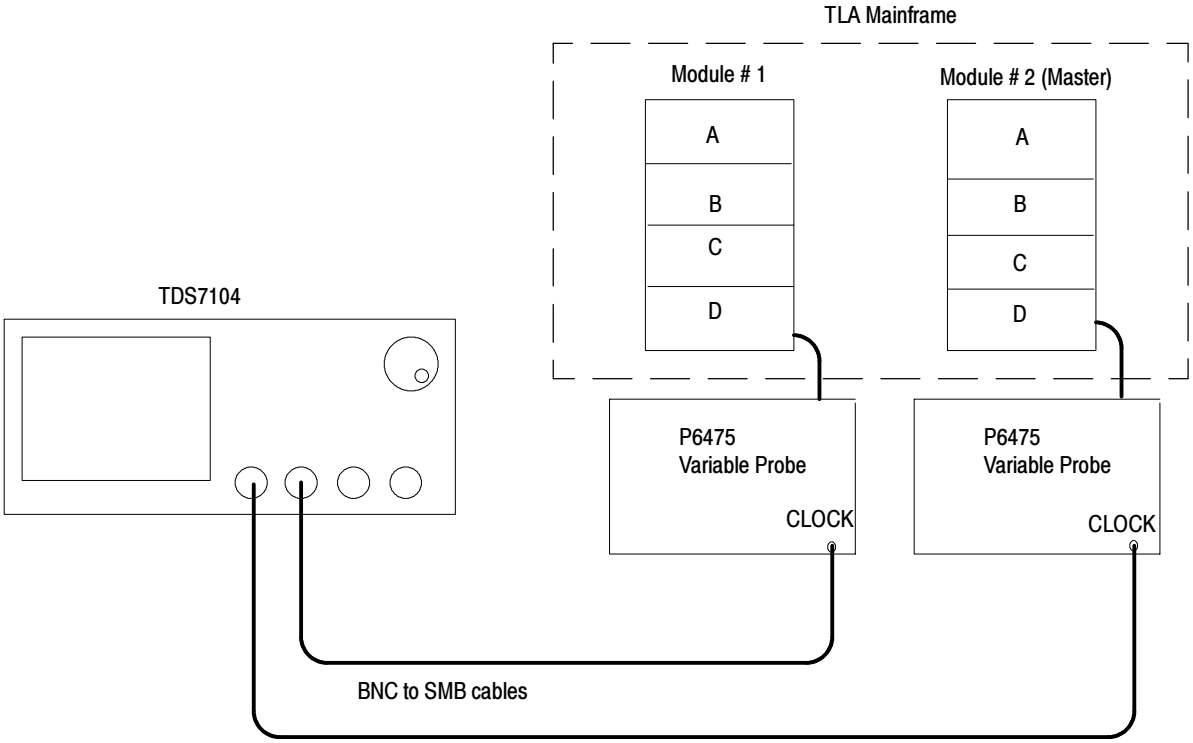


Figure 4- 11: TLA7PG2 Deskew function connections using a P6475 probe

1. Connect all equipment as shown in Figure 4–10 or Figure 4–11.
2. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
3. Set the oscilloscope controls as follows:

Displayed channel:	CH1, CH2
Vertical axis (CH1, CH2):	
P6470, P6474	2 V/div
P6471, P6472	500 mV/div
Vertical position (CH1):	
P6470, P6474	-1.00 div
P6471, P6472	4.00 div
Vertical position (CH2):	
P6470, P6474	-1.00 div
P6471, P6472	2.00 div
Vertical offset (CHx):	

P6472 PECL mode	5 V
P6472 LVPECL mode	3.3 V
P6470, P6471,P6474	0.0 V
Bandwidth:	Full
Input coupling (CH1, CH2):	DC
Input impedance (CH1, CH2):	50 Ω
Horizontal axis:	1 μs/div
Record length:	5000
Trigger mode:	NORM
Trigger slope:	Rise
Trigger source:	CH2
Trigger level:	
P6472 PECL mode	3.7 V
P6470, P6472 LVPECL mode	2 V
P6471	-1.3 V
P6474	1.65 V
Trigger coupling:	DC
Trigger position:	50%

4. Load the TP10DSKW.TPG module setup file.
5. Select System Configuration in the pattern generator application to display the Merge Modules window.
6. Set the Deskew setting for Slave1 module to 1.5 ns.
7. Click OK to save the changes and to close the window.
8. Start the pattern generator.
9. Record the delay time from the leading edge of the CH1 waveform to the leading edge of the CH2 waveform (T1).
10. Stop the pattern generator.
11. Select System Configuration in the pattern generator application to display the Merge Modules window.
12. Set the deskew value of the Slave1 module to –1.5 ns.
13. Click OK to save the changes and to close the window.
14. Start the pattern generator.

15. Write down the delay time from the leading edge of the CH1 waveform to the leading edge of the CH2 waveform (T2).
16. Stop the pattern generator.
17. Verify that T1 minus T2 is approximately 2 ns.

TLA7PG2 Inhibit Function (by data)

This check confirms the Inhibit function (by data) of the pattern generator module.

Setup files:	TP14INH.TPG
Equipment	Termination board (item 4) TDS7104 Digitizing Oscilloscope (item 2) One P6245 1 MΩ 10X Oscilloscope probe (Item 3) (use with P6470, P6473, P6474 probes) Two BNC to SMB cables (item 9) (for P6475 only) CPS250 Power supply (item 6)
Prerequisites	Pattern generator modules *not* merged Connected pattern generator probe Test equipment connected as shown in Figure 4-12 or Figure 4-13 Diagnostics pass

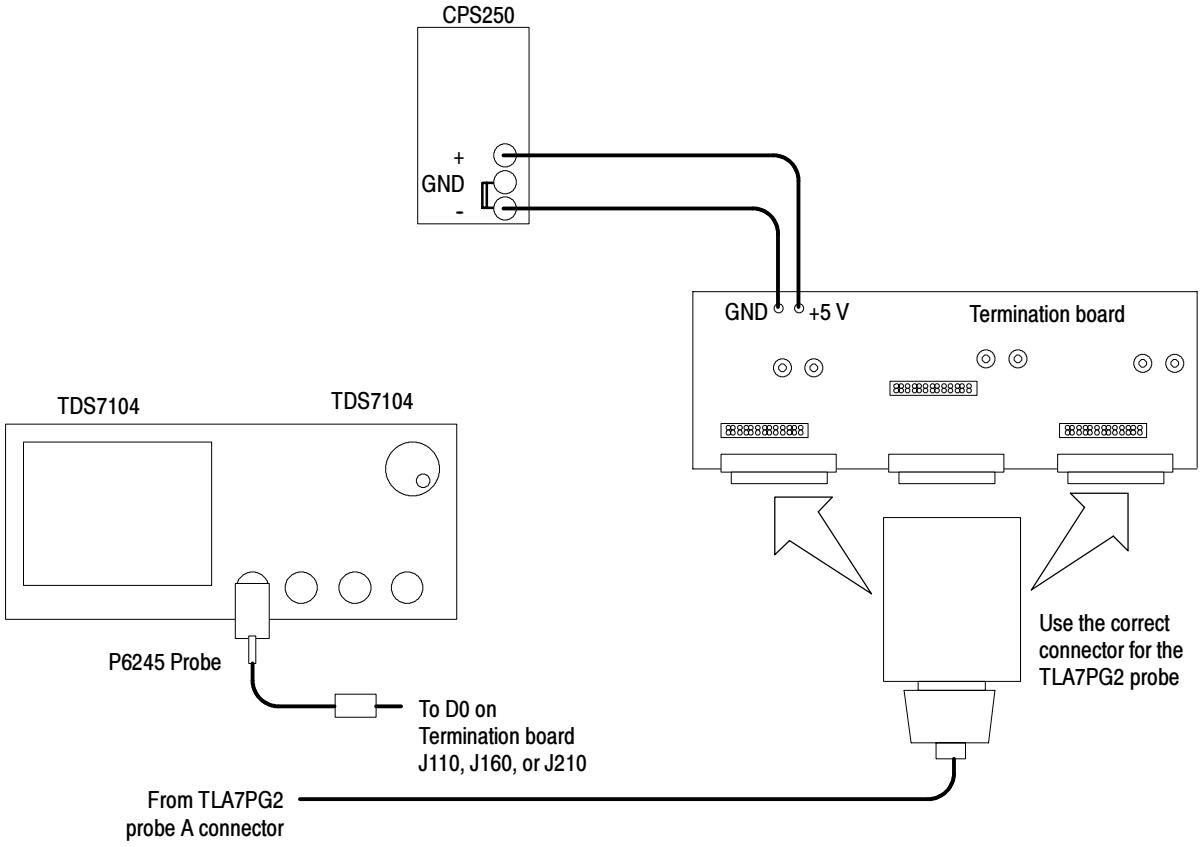


Figure 4-12: TLA7PG2 Inhibit function (by data) connections using a P6470, P6473, or P6474 probe

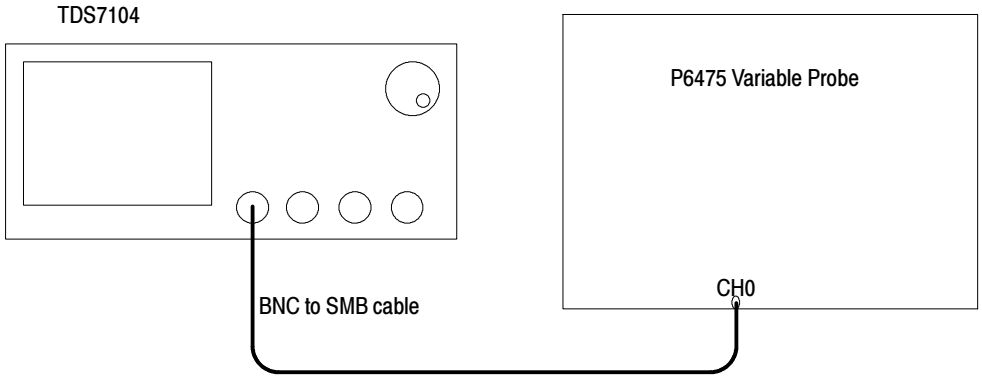


Figure 4-13: TLA7PG2 Inhibit function (by data) connections using a P6475 probe

1. Connect all equipment as shown in Figure 4–12 or Figure 4–13.
2. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
3. Set the oscilloscope controls as follows:

Displayed channel:	CH1
Vertical axis (CH1):	
P6470, P6473, P6474	2 V/div
P6475	500 mV/div
Vertical position (CH1):	1.00 div
Vertical offset (CHx):	0.0 V
Bandwidth:	Full
Input coupling (CH1):	DC
Input impedance (CH1):	50 Ω
Horizontal axis:	1 ms/div
Record length:	5000
Trigger mode:	NORM
Trigger slope:	Rise
Trigger source:	CH1
Trigger level:	2 V
P6470	2 V
P6473, P6474	1.65 V
P6475	0.5 V
Trigger coupling:	DC
Trigger position:	50%

4. If you have not already done so, complete the following steps to unmerge the pattern generator modules:
   a. Select System Configuration from the System menu in the pattern generator application.
   b. Click the Merge button between the merged modules to unmerge the two modules.
   c. Click the OK button.
5. Connect Probe A to the termination Board.
6. Load the TP14INH.TPG module setup file.

Do the following substeps if you are using a P6474; otherwise continue with Step 7:

a. Open the Program window and select the Block tab.

b. Select Block7.

c. Select Edit→ Pattern → Listing to open the Listing window.

d. Select all of the Group1 column by clicking the Group1 label cell.

e. Select Edit → Invert to fill the lines with 0000.

f. Repeat step a through step e for Group2, Group3, and Group4.

7. Start the pattern generator.

8. Verify that the output signal on CH1 has a 500 Hz clock pattern.

9. Repeat step 6 for Probe B, Probe C, and Probe D.

10. Stop the pattern generator.

This completes the functional verification for the TLA7PG2.

TLA7PG2 Inhibit Function (by Event) Test

This check confirms the Inhibit function (by event) for the pattern generator module.

Setup files:	TP12INH.TPG
Equipment	TDS7104 Digitizing Oscilloscope (item 2) P6245 1 MΩ 10X Oscilloscope probe (Item 3) (not used with P6475) CPS250 Power supply (item 6) (not used with P6475) One BNC cable (item 7)
Prerequisites	Pattern generator modules *not* merged Pattern generator probe connected Test equipment connected as shown in Figure 4-14 or 4-15 Diagnostics pass

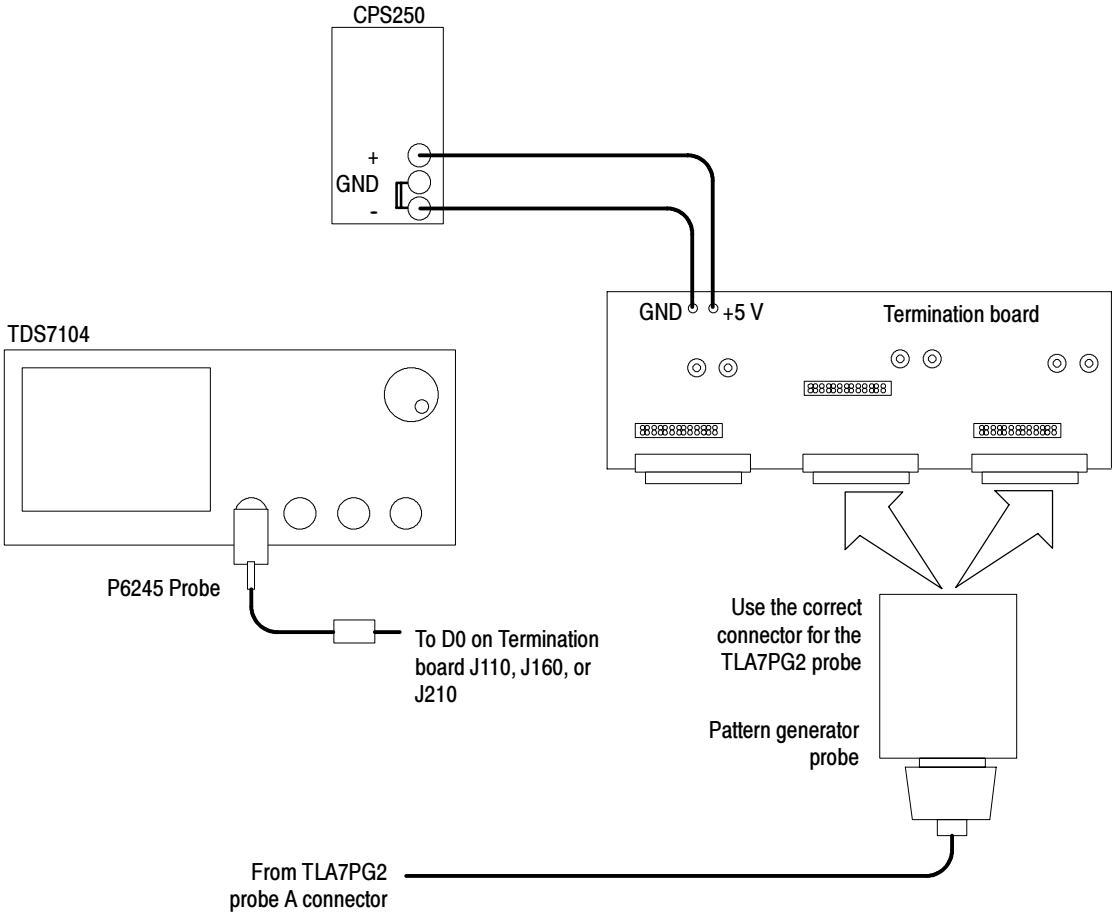


Figure 4- 14: Inhibit function (by Event) connections using a P6470, P6473, or P6474

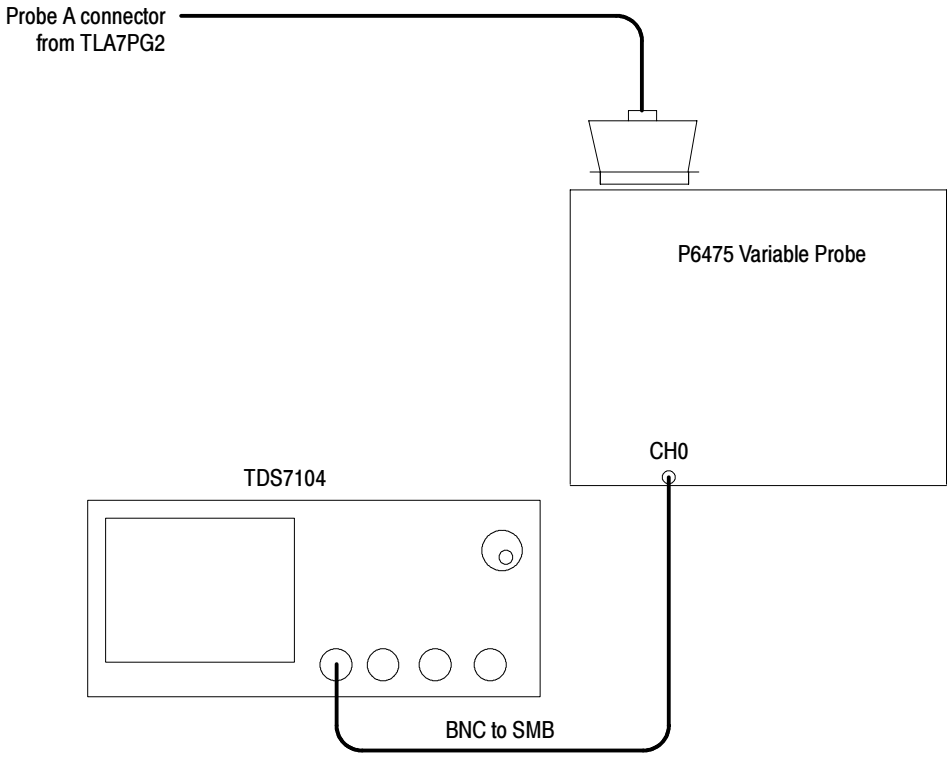


Figure 4- 15: Inhibit function (by Event) connections using a P6475

Follow the steps below to complete the functional verification:

1. Connect all equipment as shown in Figure 4–20.
2. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
3. Set the oscilloscope controls as follows:

Displayed channel:	CH1
Vertical axis (CH1):	
P6470, P6473, P6474	2 V/div
P6475	500 mV/div
Vertical position (CH1):	1.00 div
Vertical offset (CHx):	0.0 V
Bandwidth:	Full
Input coupling (CH1):	DC
Input impedance (CH1):	50 Ω
Horizontal axis:	1 ms/div
Record length:	5000
Trigger mode:	NORM
Trigger slope:	Rise
Trigger source:	CH1
Trigger level:	2 V
P6470	2 V
P6473, P6474	1.65 V
P6475	0.5 V
Trigger coupling:	DC
Trigger position:	50%

4. If you have not already done so, complete the following steps to unmerge the pattern generator modules:
   a. Select System Configuration from the System menu in the pattern generator application.
   b. Click the Merge button between the merged modules to unmerge the two modules.
   c. Click the OK button.
5. Load the TP12INH.TPG module setup file.

Do the following substeps if you are using a P6474; otherwise continue with Step 7:

a. Open the Program window and select the Block tab.

b. Select Block7.

c. Select Edit→ Pattern → Listing to open the Listing window.

d. Select all of the Group1 column by clicking the Group1 label cell.

e. Select Edit → Invert to fill the lines with 0000.

f. Repeat step a through step e for Group2, Group3, and Group4.

6. Start the pattern generator.

7. Verify that the CH1 output signal has a 500 Hz clock pattern.

8. Stop the pattern generator.

9. Repeat step 7 for Probe B, Probe C, and Probe D.

10. Stop the pattern generator.

TLA7PG2 Sequence and Data Output Test

The Sequence and Data Output test confirms that the pattern generator sends the proper sequences and data to the probes. This check also verifies the probe operation.

Use the following probe Sequence and Data Output Tests to test the TLA7PG2.

P6470 page 4–43

P6471 page 4–53

P6472 page 4–61

P6473 page 4–68

P6474 page 4–79

P6475 page 4–90

P6470 Functional Verification Procedures

The Probe Verification Procedures contains procedures to verify certain functions for the P6470, P6471, P6472, P6473, P6474, and P6475 pattern generator probes. Refer to the TLA7PG2 Setup Procedures on page 4–7 and complete all TLA7PG2 tests prior to verifying the functions for the pattern generator probes.

Internal Clock Frequency Test for P6470

The Internal Clock Frequency test confirms the frequency of the pattern generator module internal clock with the probe.

Setup files:	TP1CLK.TPG
Equipment	Termination board (item 4)
	TDS7104 Digitizing Oscilloscope (item 2)
	P6245 1 MΩ 10X Oscilloscope probe (Item 3)
	CPS250 Power supply (item 6)
Prerequisites	P6470 probe connected
	Connect the test equipment as shown in Figure 4-16
	Diagnostics pass

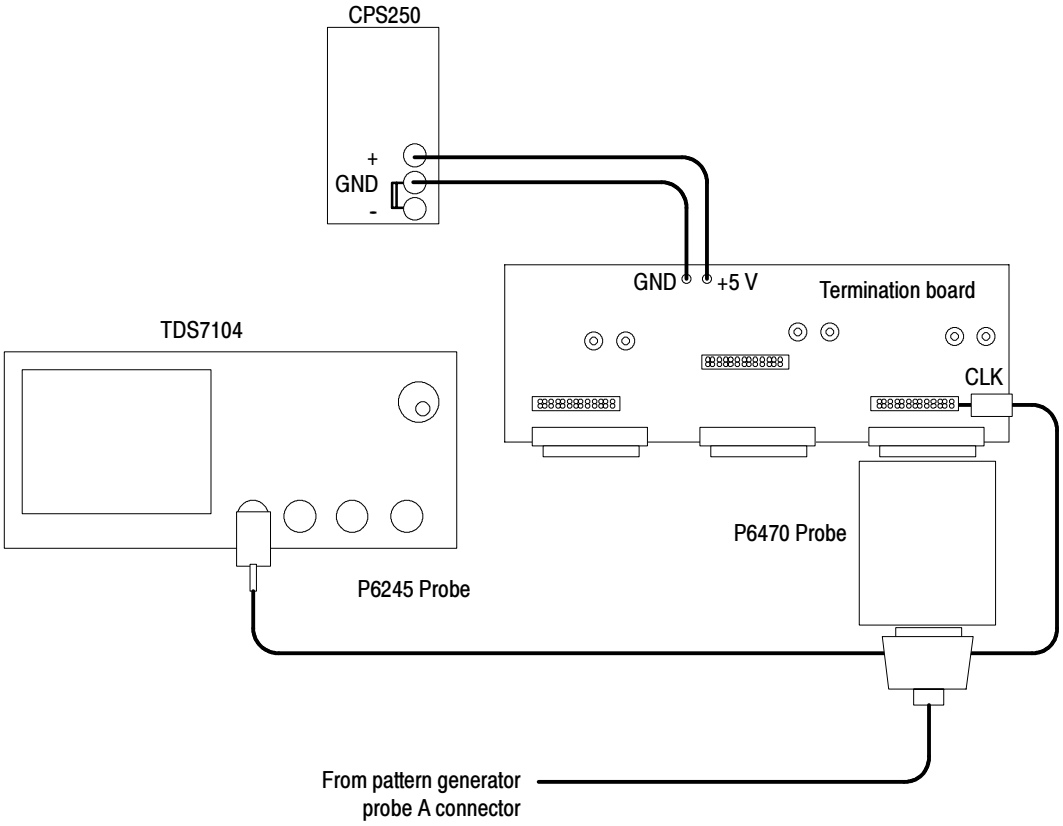


Figure 4- 16: Internal Clock Frequency connections

Follow the steps below to complete the functional verification:

1. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
2. Set the oscilloscope controls as follows:

Displayed channel:	CH1
Vertical axis (CH1):	1 V/div
Vertical position (CH1):	-2.00 div
Vertical offset (CHx):	0.0 V
Bandwidth:	Full
Input coupling:	DC
Input impedance:	50 Ω
Horizontal axis:	1 ns/div
Record length:	5000
Trigger mode:	NORM
Trigger source:	CH1
Trigger slope::	Rise
Trigger level:	2 V
Trigger coupling:	DC
Trigger position:	50%

3. Load the TP1CLK.TPG module setup file. When the file is loaded, the pattern generator clock period will be set to 3.7313 ns internally.
4. Click the Setup icon in the pattern generator application window and change the internal clock period to 9.99 ns.
5. Start the pattern generator.
6. Verify that the frequency of the pattern generator output signal is 100.1 MHz.
7. Stop the pattern generator.
8. Set the pattern generator clock period to 5.0000 μs.
9. Start the pattern generator.
10. Set the oscilloscope Horizontal axis setting to 1.00 μs/div.
11. Verify that the frequency of the pattern generator output signal is 200 kHz.
12. Stop the pattern generator.

13. Set the pattern generator clock period to 1.0000 s.
14. Start the pattern generator.
15. Set the oscilloscope Horizontal axis setting to 200 ms/div.
16. Verify that the frequency of the pattern generator output signal is about 1 Hz.
17. Stop the pattern generator.

Sequence and Data Output Test for P6470

The Sequence and Data Output test confirms that the pattern generator sends the proper sequences and data to the probes. This check also verifies the probe operation.

Setup files: TP5PG0.TPG, TP6PG0.TPG, TP7PG0.TPG, TP8PG0.TPG	
Equipment	Termination board (item 4)
	TDS7104 Digitizing Oscilloscope (item 2)
	Two P6245 1 MΩ 10X Oscilloscope probes (Item 3)
	CPS250 Power supply (item 6)
	AFG310 Function generator (item 5)
	One BNC cable (item 7)
Prerequisites	Connected P6470 probe
	Test equipment connected as shown in Figure 4-17
	Diagnostics pass

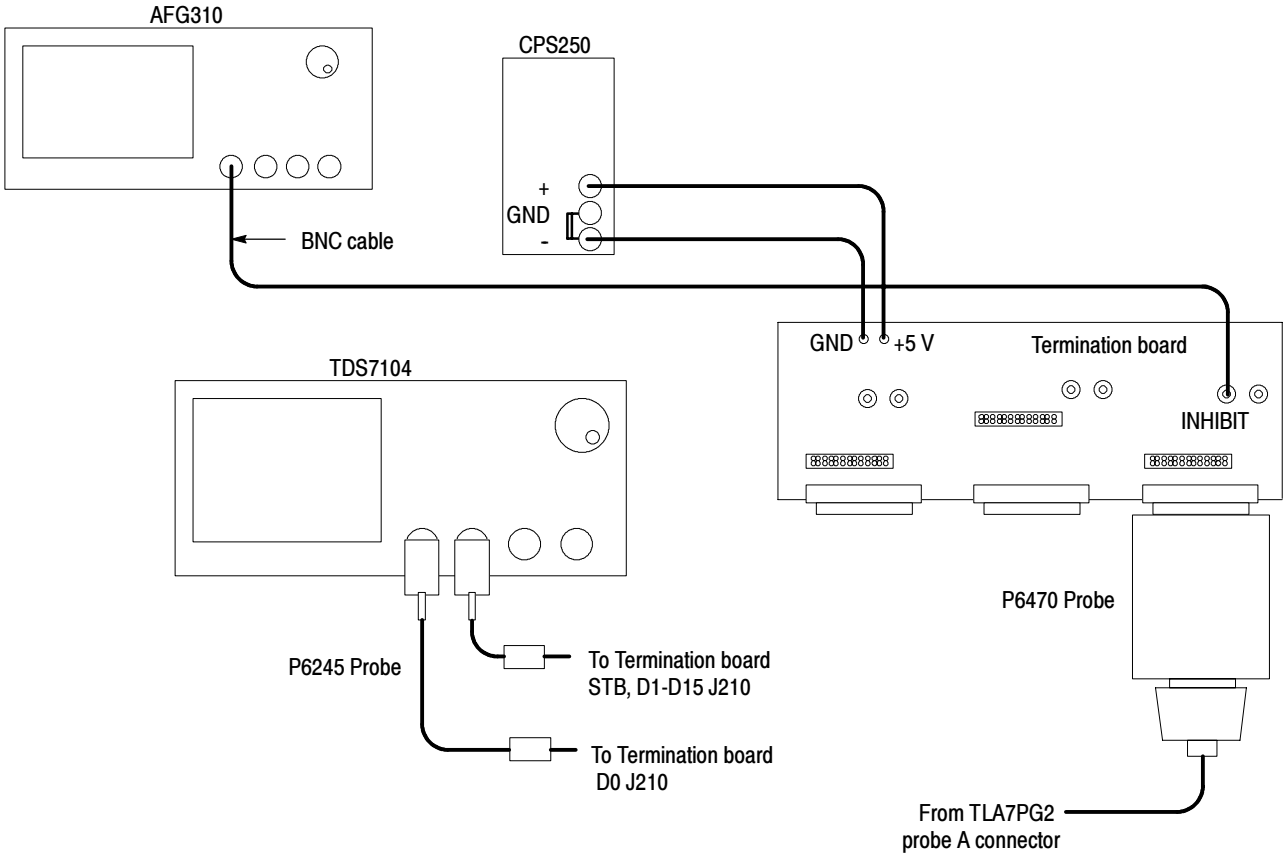


Figure 4- 17: Sequence and Data Output connections

Follow the steps below to complete the functional verification:

1. Connect all equipment as shown in Figure 4–17.
2. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
3. Set the oscilloscope controls as follows:

Displayed channel:	CH1, CH2
Vertical axis (CH1, CH2):	5 V/div
Vertical position (CH1):	2.00 div
Vertical position (CH2):	0.00 div
Vertical offset (CHx):	0.0 V
Bandwidth:	Full
Input coupling (CH1, CH2):	DC
Input impedance (CH1, CH2):	50 Ω
Horizontal axis:	1 μs/div
Record length:	5000
Trigger mode:	AUTO
Trigger slope:	Fall
Trigger source:	CH1
Trigger level:	2 V
Trigger coupling:	DC
Trigger position:	10%

4. Set up CH 1 of the function generator as follows:
   - Frequency 200 kHz
   - CH1 ON
5. Load the TP5PG0.TPG module setup
6. Verify that the front panel Accessed Indicator blinks on the pattern generator module.
7. Start the pattern generator.
8. Verify that the CH1 waveforms are similar to the waveforms shown in Figure 4–18.
9. Connect the CH2 Probe on the oscilloscope to the STB connector on the termination Board. Verify that the output signal data pattern is similar to the

waveform shown in Figure 4–18. Repeat this procedure on the output signals from D1 through the D15 connector.

10. Stop the pattern generator.

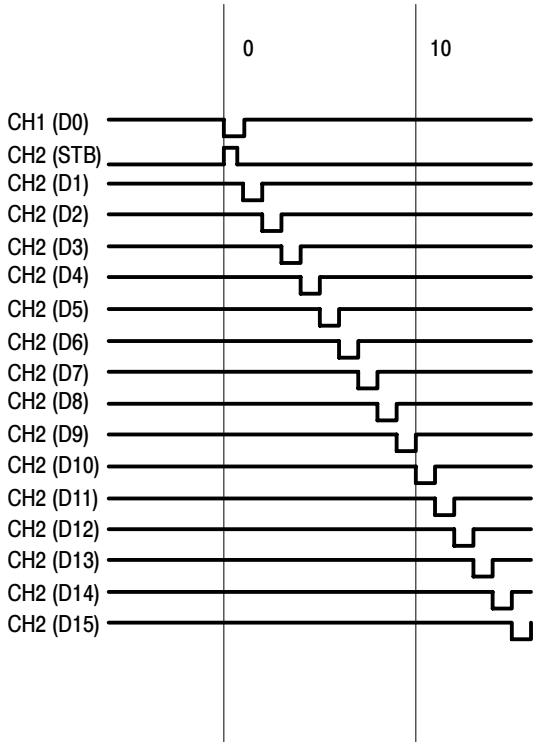


Figure 4- 18: P6470 Sequence and Data sample waveforms

11. Connect Probe B to the termination board.

12. Load the TP6PG0.TPG module setup file.

13. Repeat steps 7 through 10.

14. Connect Probe C to the termination board.

15. Load the TP7PG0.TPG module setup file.

16. Repeat steps 7 through 10.

17. Connect Probe D to the termination board.

18. Load the TP8PG0.TPG module setup file.

19. Start the pattern generator.

20. Verify that the CH1 waveforms are similar to the waveforms shown in Figure 4-19.

21. Connect the CH2 Probe of the oscilloscope to the STB connector on the termination Board. Verify that the output signal data pattern is similar to the waveform shown in Figure 4-19. Repeat this procedure on the output signals from the D1 through the D15 connector.

22. Verify that the Ready, Output**,** and Started front panel indicators are illuminated and the Waiting front panel indicator blinks while the system is operating.

23. Stop the pattern generator.

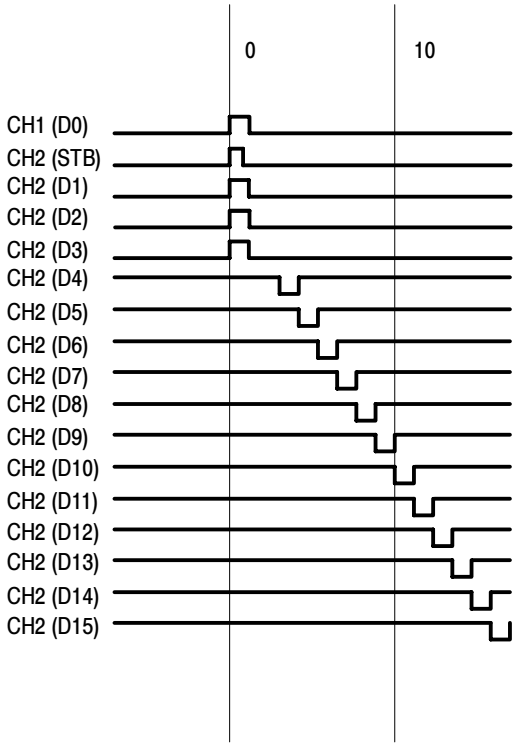


Figure 4-19: P6470 Sequence and Data strobed sample waveforms

Inhibit Function Test for P6470

This check confirms the Inhibit function of the pattern generator module and the P6470 pattern generator probes.

Setup files:	TP12INH.TPG, TP13INH.TPG
Equipment	TDS7104 Digitizing Oscilloscope (item 2) P6245 1 MΩ 10X Oscilloscope probe (Item 3) AFG310 Function generator (item 5) (used for test by Inhibit External Inhibit input only) CPS250 Power supply (item 6) One BNC cable (item 7) (used for test by External Inhibit only)
Prerequisites	Pattern generator modules *not* merged P6470 probe connected Test equipment connected as shown in Figure 4-20 Diagnostics pass

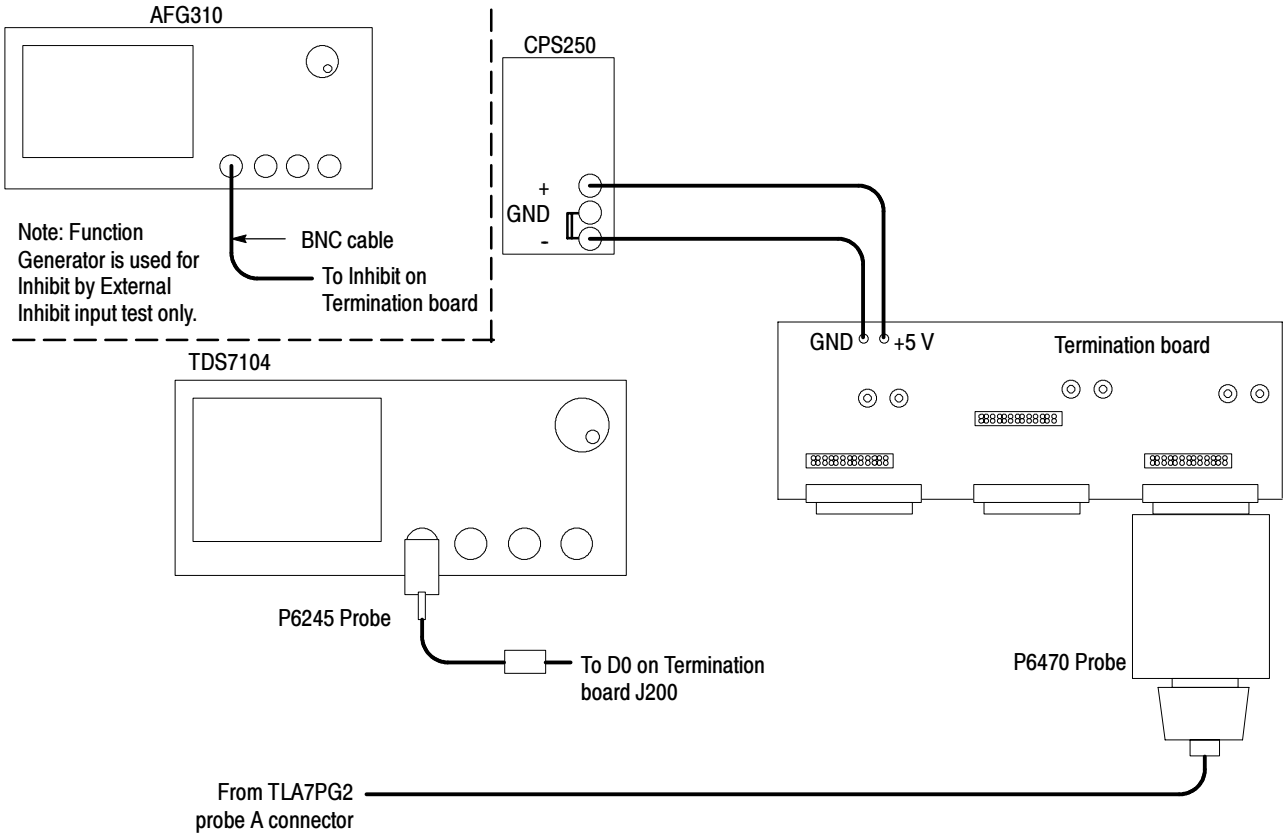


Figure 4-20: Inhibit function connections

Follow the steps below to complete the functional verification:

1. Connect all equipment as shown in Figure 4–20. (Do not connect the function generator.)
2. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
3. Set the oscilloscope controls as follows:

Displayed channel::	CH1
Vertical axis (CH1):	500 mV/div
Vertical position (CH1):	–2.00 div
Vertical offset (CHx):	0.0 V
Bandwidth:	Full
Input coupling (CH1):	DC
Input impedance (CH1):	50 Ω
Horizontal axis:	1 ms/div
Record length:	5000
Trigger mode:	NORM
Trigger slope:	Rise
Trigger source:	CH1
Trigger level:	2 V
Trigger coupling:	DC
Trigger position:	50%

4. If you have not already done so, complete the following steps to unmerge the pattern generator modules:
   a. Select System Configuration from the System menu in the pattern generator application.
   b. Click the Merge button between the merged modules to unmerge the two modules.
   c. Click the OK button.

Inhibit by Event. Use the TP12INH.TPG module setup file.

5. Load the TP12INH.TPG module setup file.
6. Start the pattern generator.
7. Verify that the CH1 output signal has a 500 Hz clock pattern.
8. Repeat step 7 for Probe B, Probe C, and Probe D.
9. Stop the pattern generator.

Inhibit by External Inhibit input. Use the TP13INH.TPG module setup file.

10. Connect a BNC Cable from the function generator to J230 (Inhibit) on the termination board.
11. Connect Probe A to the termination Board.
12. Set up CH 1 of the function generator as follows:
    - Frequency 500 Hz
    - CH1 ON
13. Load the TP13INH.TPG module setup file.
14. Start the pattern generator.
15. Verify that a 500 Hz clock pattern appears on CH1.
16. Repeat step 15 for Probe B, Probe C, and Probe D.
17. Stop the pattern generator.

P6471 Functional Verification Procedures

The following tests and information verify the operation of the P6471 probe.

Internal Clock Frequency Test for P6471

The Internal Clock Frequency test confirms the frequency of the pattern generator module internal clock with the probe.

Setup files:	TP1CLK.TPG
Equipment	Termination board (item 4) TDS7104 Digitizing Oscilloscope (item 2) P6245 1 MΩ 10X Oscilloscope probe (Item 3) CPS250 Power supply (item 6)
Prerequisites	Connected P6471 probe Connect the test equipment as shown in Figure 4-21 Diagnostics pass

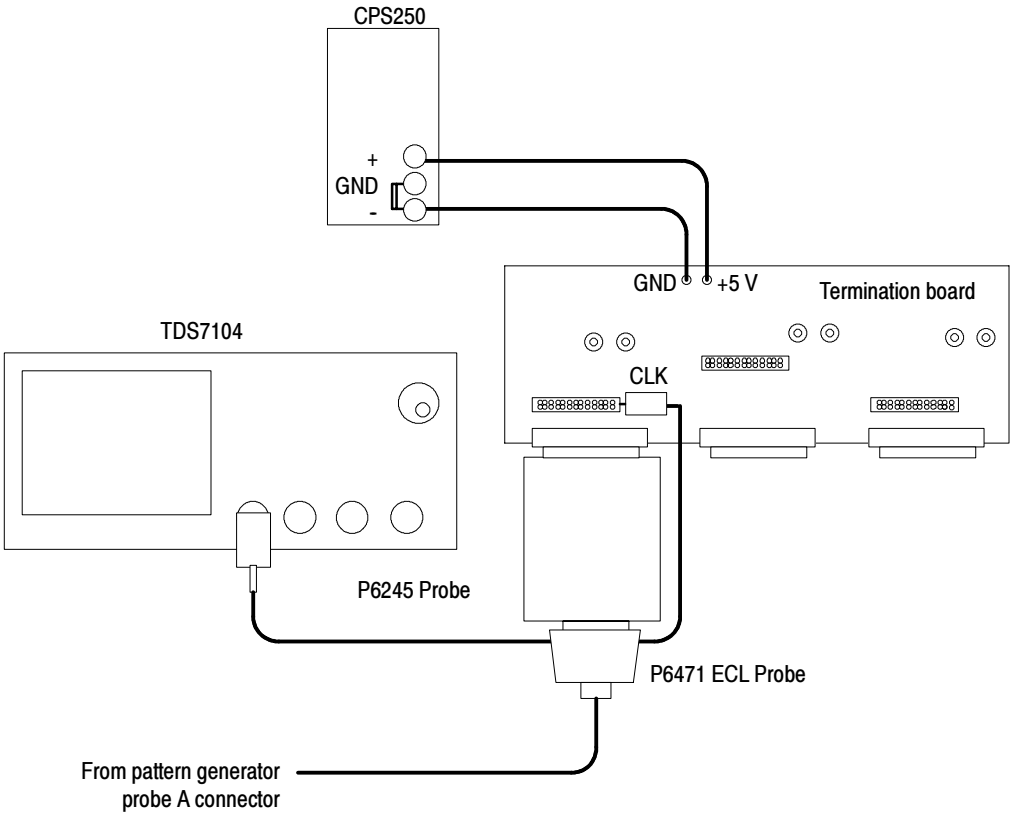


Figure 4-21: Internal Clock Frequency connections

Follow the steps below to complete the functional verification:

1. Connect all equipment as shown in Figure 4–21.
2. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
3. Set the oscilloscope controls as follows:

Displayed channel:	CH1
Vertical axis (CH1):	500 mV/div
Vertical position (CH1):	1.00 div
Vertical offset (CHx):	0.0 V
Bandwidth:	Full
Input coupling:	DC
Input impedance:	50 Ω
Horizontal axis:	1 ns/div
Record length:	5000
Trigger mode:	NORM
Trigger source:	CH1
Trigger slope::	Rise
Trigger level:	-1.3 V
Trigger coupling:	DC
Trigger position:	50%

4. Load the TP1CLK.TPG module setup file. When the file is loaded, the pattern generator clock period will be set to 3.7313 ns internally.
5. Start the pattern generator.
6. Use the frequency measurement function of the oscilloscope to verify that the frequency of the pattern generator output signal is about 268 MHz.
7. Stop the pattern generator.
8. Click the Setup icon in the pattern generator application window and change the internal clock period to 9.99 ns.
9. Start the pattern generator.
10. Verify that the frequency of the pattern generator output signal is 100.1 MHz.
11. Stop the pattern generator.

12. Set the pattern generator clock period to 5.0000 µs.

13. Start the pattern generator.

14. Set the oscilloscope Horizontal axis setting to 1.00 µs/div.

15. Verify that the frequency of the pattern generator output signal is 200 kHz.

16. Stop the pattern generator.

17. Set the pattern generator clock period to 1.0000 s.

18. Start the pattern generator.

19. Set the oscilloscope Horizontal axis setting to 200 ms/div.

20. Verify that the frequency of the pattern generator output signal is about 1 Hz.

21. Stop the pattern generator.

Sequence and Data Output Test for P6471

The Sequence and Data Output test confirms that the pattern generator sends the proper sequences and data to the probes. This check also verifies the probe operation.

Setup files: TP5PG0.TPG, TP6PG0.TPG, TP7PG0.TPG, TP8PG0.TPG	
Equipment	Termination board (item 4) TDS7104 Digitizing Oscilloscope (item 2) Three P6245 1 MΩ 10X Oscilloscope probes (Item 3) CPS250 Power supply (item 6) AFG310 Function generator (item 5) One BNC cable (item 7)
Prerequisites	Connected P6471 probe Test equipment connected as shown in Figure 4-22 Diagnostics pass

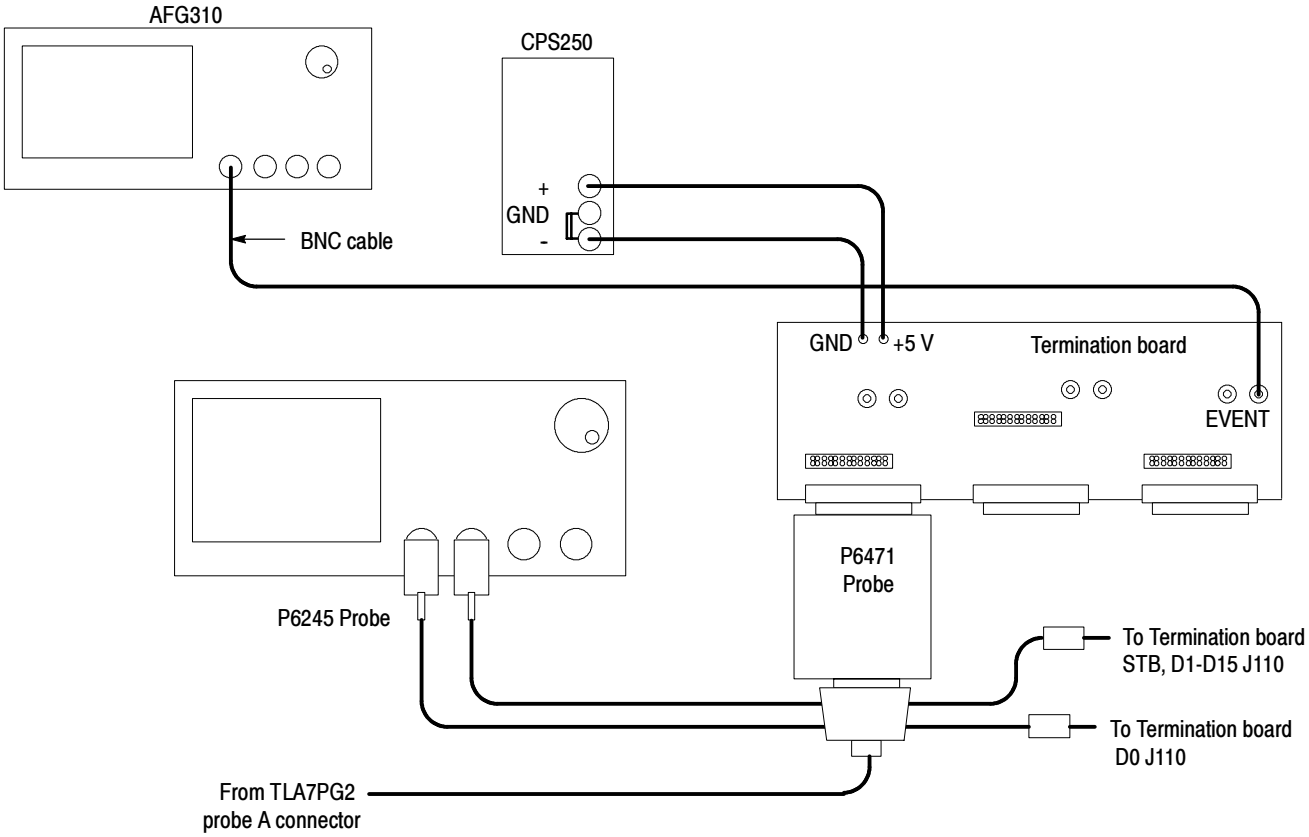


Figure 4- 22: Sequence and Data Output connections

Follow the steps below to complete the functional verification:

1. Connect all equipment as shown in Figure 4–22.
2. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
3. Set the oscilloscope controls as follows:

Displayed channel:	CH1, CH2
Vertical axis (CH1, CH2):	500 mV/div
Vertical position (CH1):	5.00 div
Vertical position (CH2):	3.00 div
Vertical offset (CHx):	0.0 V
Bandwidth:	Full
Input coupling (CH1, CH2):	DC
Input impedance (CH1, CH2):	50 Ω
Horizontal axis:	1 μs/div
Record length:	5000
Trigger mode:	AUTO
Trigger slope:	Fall
Trigger source:	CH1
Trigger level:	-1.3 V
Trigger coupling:	DC
Trigger position:	10%

4. Set up CH 1 of the function generator as follows:
   - Frequency 200 kHz
   - CH1 ON
5. Load the TP5PG0.TPG module setup
6. Verify that the front panel Accessed indicator blinks on the pattern generator module.
7. Start the pattern generator.
8. Verify that the CH1 waveforms are similar to the waveforms shown in Figure 4–18.
9. Connect the CH2 Probe on the oscilloscope to the STB connector on the termination Board. Verify that the output signal data pattern is similar to the

waveform shown in Figure 4–23. Repeat this procedure on the output signals from D1 through the D15 connector.

10. Stop the pattern generator.

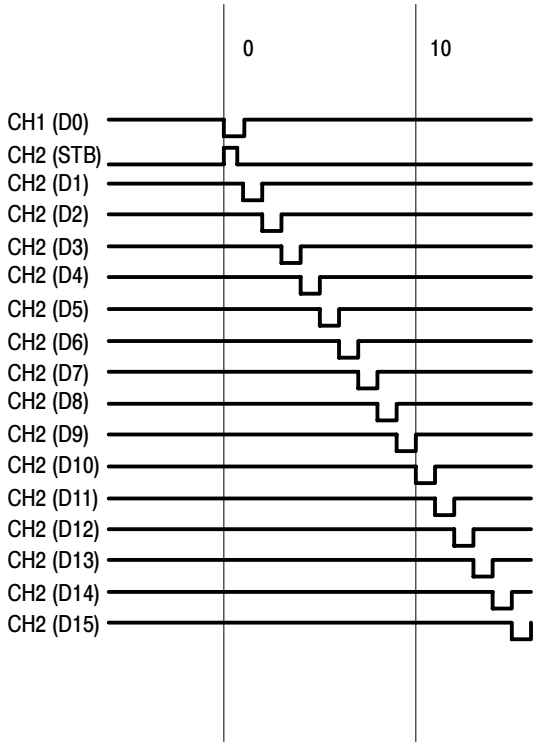


Figure 4- 23: P6471 Sequence and Data sample waveforms

11. Connect Probe B to the termination board.

12. Load the TP6PG0.TPG module setup file.

13. Repeat steps 7 through 10.

14. Connect Probe C to the termination board.

15. Load the TP7PG0.TPG module setup file.

16. Repeat steps 7 through 10.

17. Connect Probe D to the termination board.

18. Load the TP8PG0.TPG module setup file.

19. Start the pattern generator.

20. Verify that the CH1 waveforms are similar to the waveforms shown in Figure 4-24.

21. Connect the CH2 Probe of the oscilloscope to the STB connector on the termination Board. Verify that the output signal data pattern is similar to the waveform shown in Figure 4-24. Repeat this procedure on the output signals from the D1 through the D15 connector.

22. Verify that the Ready, Output**,** and Started front panel indicators are illuminated and the Waiting front panel indicator blinks while the system is operating.

23. Stop the pattern generator.

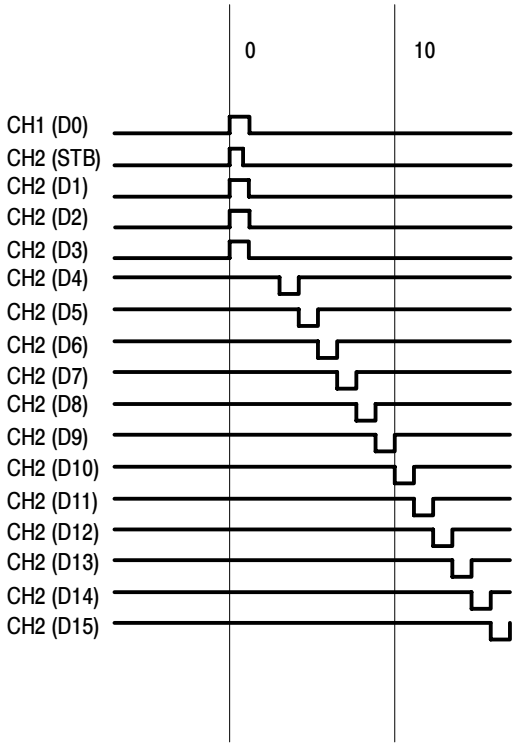


Figure 4-24: P6471 Sequence and Data strobed sample waveforms

P6472 Functional Verification Procedures

The following tests and information verify the operation of the P6472 probe.

Internal Clock Frequency Test for P6472

The Internal Clock Frequency test confirms the frequency of the pattern generator module internal clock with the probe.

Setup files:	TP1CLK.TPG
Equipment	Termination board (item 4) TDS7104 Digitizing Oscilloscope (item 2) P6245 1 MΩ 10X Oscilloscope probe (Item 3) CPS250 Power supply (item 6)
Prerequisites	Connect probe as shown in Figure NO TAG Connect the test equipment as shown in Figure NO TAG Diagnostics pass

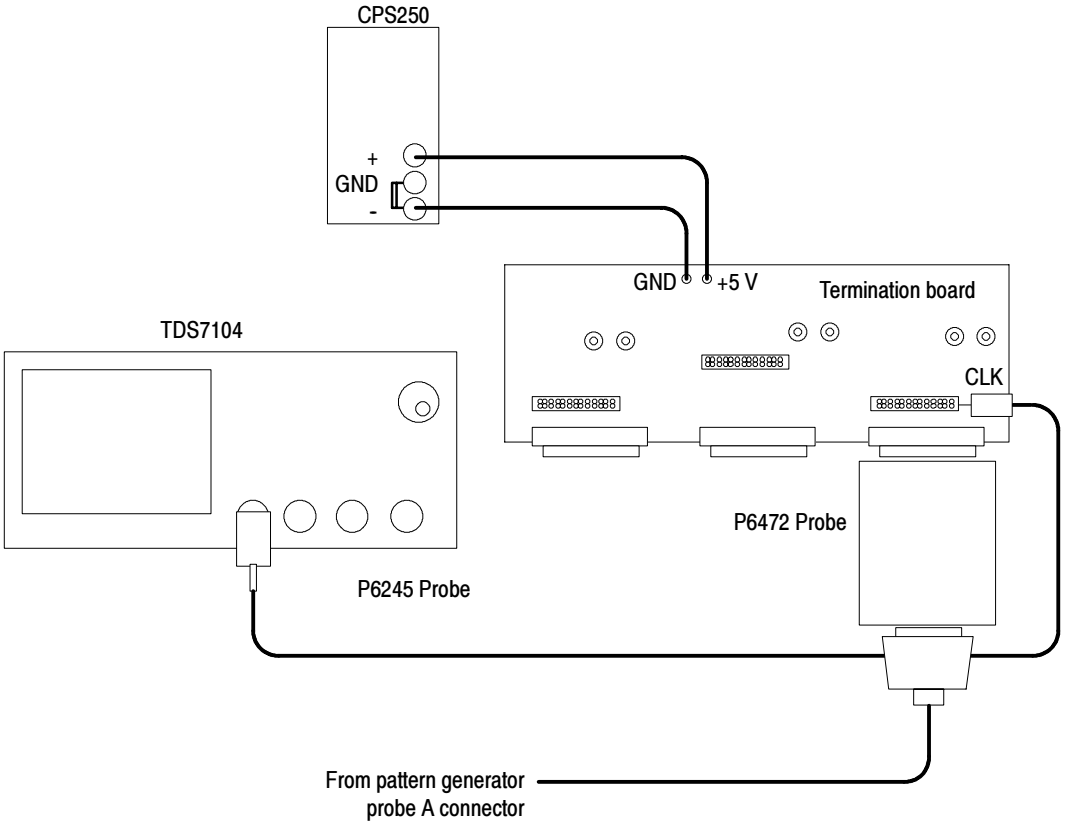


Figure 4- 25: Internal Clock Frequency connections

Follow the steps below to complete the functional verification:

1. Connect all equipment as shown in Figure NO TAG.
2. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
3. Set the oscilloscope controls as follows:

Displayed channel:	CH1
Vertical axis (CH1):	500 mV/div
Vertical position (CH1):	1.00 div
Vertical offset (CHx):	
P6472 PECL mode	5 V
P6472 LVPECL mode	3.3 V
Bandwidth:	Full
Input coupling:	DC
Input impedance:	50 Ω
Horizontal axis:	1 ns/div
Record length:	5000
Trigger mode:	NORM
Trigger source:	CH1
Trigger slope::	Rise
Trigger level:	
P6472 PECL mode	3.7 V
P6472 LVPECL mode	2 V
Trigger coupling:	DC
Trigger position:	50%

4. Load the TP1CLK.TPG module setup file. When the file is loaded, the pattern generator clock period will be set to 3.7313 ns internally.
5. Start the pattern generator.
6. Use the frequency measurement function of the oscilloscope to verify that the frequency of the pattern generator output signal is about 268 MHz.
7. Stop the pattern generator.
8. Click the Setup icon in the pattern generator application window and change the internal clock period to 9.99 ns.
9. Start the pattern generator.

10. Verify that the frequency of the pattern generator output signal is 100.1 MHz.
11. Stop the pattern generator.
12. Set the pattern generator clock period to 5.0000 μs.
13. Start the pattern generator.
14. Set the oscilloscope Horizontal axis setting to 1.00 μs/div.
15. Verify that the frequency of the pattern generator output signal is 200 kHz.
16. Stop the pattern generator.
17. Set the pattern generator clock period to 1.0000 s.
18. Start the pattern generator.
19. Set the oscilloscope Horizontal axis setting to 200 ms/div.
20. Verify that the frequency of the pattern generator output signal is about 1 Hz.
21. Stop the pattern generator.

Sequence and Data Output Test for P6472

The Sequence and Data Output test confirms that the pattern generator sends the proper sequences and data to the probes. This check also verifies the probe operation.

Setup files: TP5PG0.TPG, TP6PG0.TPG, TP7PG0.TPG, TP8PG0.TPG	
Equipment	Termination board (item 4) TDS7104 Digitizing Oscilloscope (item 2) Two P6245 1 MΩ 10X Oscilloscope probes (Item 3) CPS250 Power supply (item 6) AFG310 Function generator (item 5) One BNC cable (item 7)
Prerequisites	Connected P6472 probe Test equipment connected as shown in Figure 4-26 Diagnostics pass

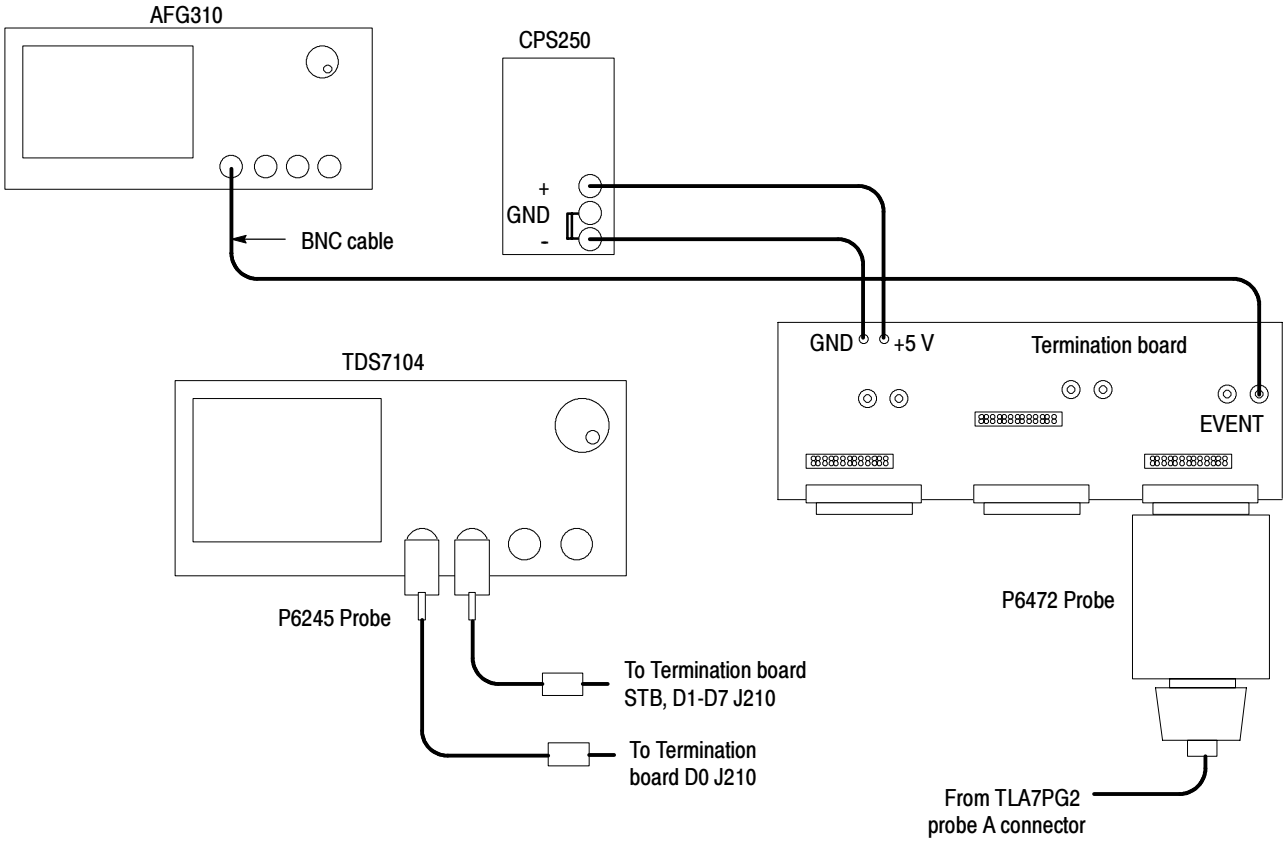


Figure 4- 26: Sequence and Data Output connections

Follow the steps below to complete the functional verification:

1. Connect all equipment as shown in Figure 4–26.
2. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
3. Set the oscilloscope controls as follows:

Displayed channel:	CH1, CH2
Vertical axis (CH1, CH2):	500 mV/div
Vertical position (CH1):	5.00 div
Vertical position (CH2):	3.00 div
Vertical offset (CHx):	
P6472 PECL mode	5 V
P6472 LVPECL mode	3.3 V
Bandwidth:	Full
Input coupling (CH1, CH2):	DC
Input impedance (CH1, CH2):	50 Ω
Horizontal axis:	1 μs/div
Record length:	5000
Trigger mode:	AUTO
Trigger slope:	Fall
Trigger source:	CH1
Trigger level:	
P6472 PECL mode	3.7 V
P6472 LVPECL mode	2 V
Trigger coupling:	DC
Trigger position:	10%

4. Set up CH1 of the function generator as follows:
   - Frequency 200 kHz
   - CH1 ON
5. Load the TP5PG0.TPG module setup.
6. Verify that the front panel Accessed indicator blinks on the pattern generator module.
7. Start the pattern generator.

8. Verify that the CH1 waveforms are similar to the waveforms shown in Figure 4–27.
9. Connect the CH2 Probe on the oscilloscope to the STB connector on the termination Board. Verify that the output signal data pattern is similar to the waveform shown in Figure 4–27. Repeat this procedure on the output signals from D1 through the D7 connector.
10. Stop the pattern generator.

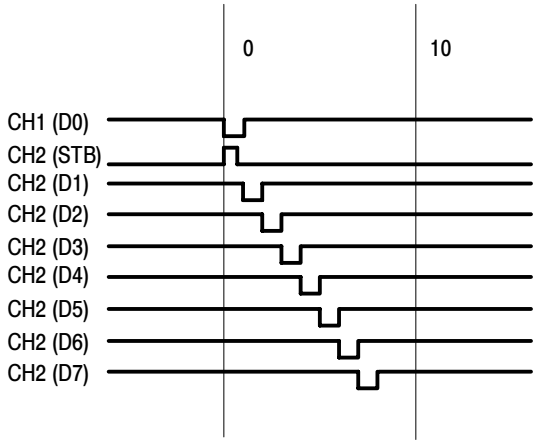


Figure 4-27: P6472 Sequence and Data sample waveforms

11. Connect Probe B to the termination board.
12. Load the TP6PG0.TPG module setup file.
13. Repeat steps 7 through 10.
14. Connect Probe C to the termination board.
15. Load the TP7PG0.TPG module setup file.
16. Repeat steps 7 through 10.
17. Connect Probe D to the termination board.
18. Load the TP8PG0.TPG module setup file.
19. Start the pattern generator.
20. Verify that the CH1 waveforms are similar to the waveforms shown in Figure 4–28.
21. Connect the CH2 Probe of the oscilloscope to the STB connector on the termination Board. Verify that the output signal data pattern is similar to the

waveform shown in Figure 4–28. Repeat this procedure on the output signals from the D1 through the D7 connector.

22. Verify that the Ready, Output**,** and Started front panel indicators are illuminated and the Waiting front panel indicator blinks while the system is operating.

23. Stop the pattern generator.

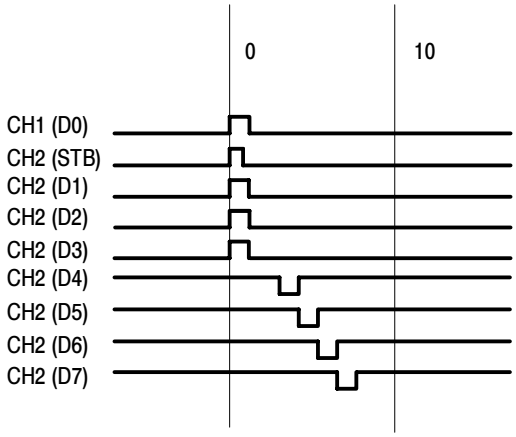


Figure 4- 28: P6472 Sequence and Data strobed sample waveforms

P6473 Functional Verification Procedures

The following tests and information verify the operation of the P6473 probe.

Internal Clock Frequency Test for P6473

The Internal Clock Frequency test confirms the frequency of the pattern generator module internal clock with the probe.

Setup files:	TP1CLK.TPG
Equipment	Termination board (item 4) TDS7104 Digitizing Oscilloscope (item 2) P6245 1 MΩ 10X Oscilloscope probe (Item 3) CPS250 Power supply (item 6)
Prerequisites	Connected P6473 probe Connect the test equipment as shown in Figure 4-29 Diagnostics pass

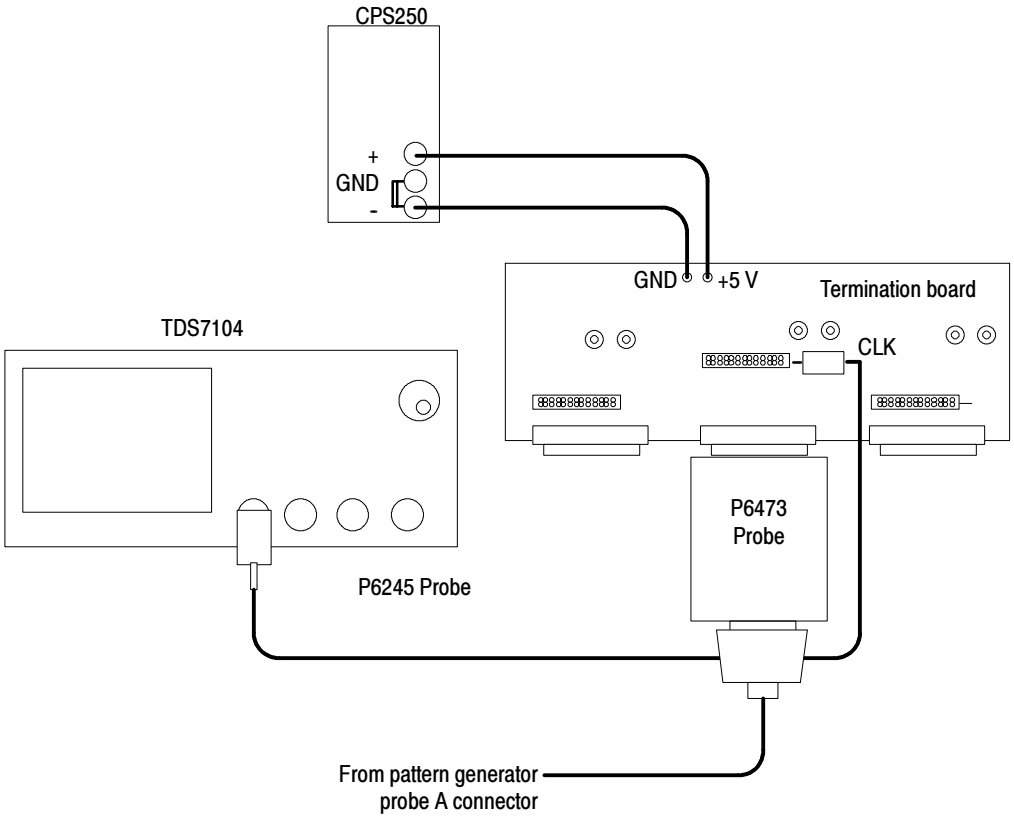


Figure 4-29: Internal Clock Frequency connections

Follow the steps below to complete the functional verification:

1. Connect all equipment as shown in Figure 4–29.
2. Set up the oscilloscope by pressing Default Setup then Factory Init to return the oscilloscope to the default condition.
3. Set the oscilloscope controls as follows:

Displayed channel:	CH1
Vertical axis (CH1):	1 V/div
Vertical position (CH1):	-2.00 div
Vertical offset (CHx):	0.0 V
Bandwidth:	Full
Input coupling:	DC
Input impedance:	50 Ω
Horizontal axis:	1 ns/div
Record length:	5000
Trigger mode:	NORM
Trigger source:	CH1
Trigger slope::	Rise
Trigger level:	1.65 V
Trigger coupling:	DC
Trigger position:	50%

4. Load the TP1CLK.TPG module setup file. When the file is loaded, the pattern generator clock period will be set to 3.7313 ns internally.
5. Start the pattern generator.
6. Use the frequency measurement function of the oscilloscope to verify that the frequency of the pattern generator output signal is about 268 MHz.
7. Stop the pattern generator.
8. Click the Setup icon in the pattern generator application window and change the internal clock period to 9.99 ns.
9. Start the pattern generator.
10. Verify that the frequency of the pattern generator output signal is 100.1 MHz.
11. Stop the pattern generator.

12. Set the pattern generator clock period to 5.0000 µs.

13. Start the pattern generator.

14. Set the oscilloscope Horizontal axis setting to 1.00 µs/div.

15. Verify that the frequency of the pattern generator output signal is 200 kHz.

16. Stop the pattern generator.

17. Set the pattern generator clock period to 1.0000 s.

18. Start the pattern generator.

19. Set the oscilloscope Horizontal axis setting to 200 ms/div.

20. Verify that the frequency of the pattern generator output signal is about 1 Hz.

21. Stop the pattern generator.

Sequence and Data Output Test for P6473

The Sequence and Data Output test confirms that the pattern generator sends the proper sequences and data to the P6473. This check also verifies the probe operation.

Setup files: TP5PG1.TPG, TP6PG1.TPG, TP7PG1.TPG, TP8PG1.TPG	
Equipment	Termination board (item 4) TDS7104 Digitizing Oscilloscope (item 2) Two P6245 1 MΩ 10X Oscilloscope probes (Item 3) CPS250 Power supply (item 6) AFG310 Function generator (item 5) One BNC cable (item 7)
Prerequisites	Connected P6473 probe Test equipment connected as shown in Figure 4-30 Diagnostics pass

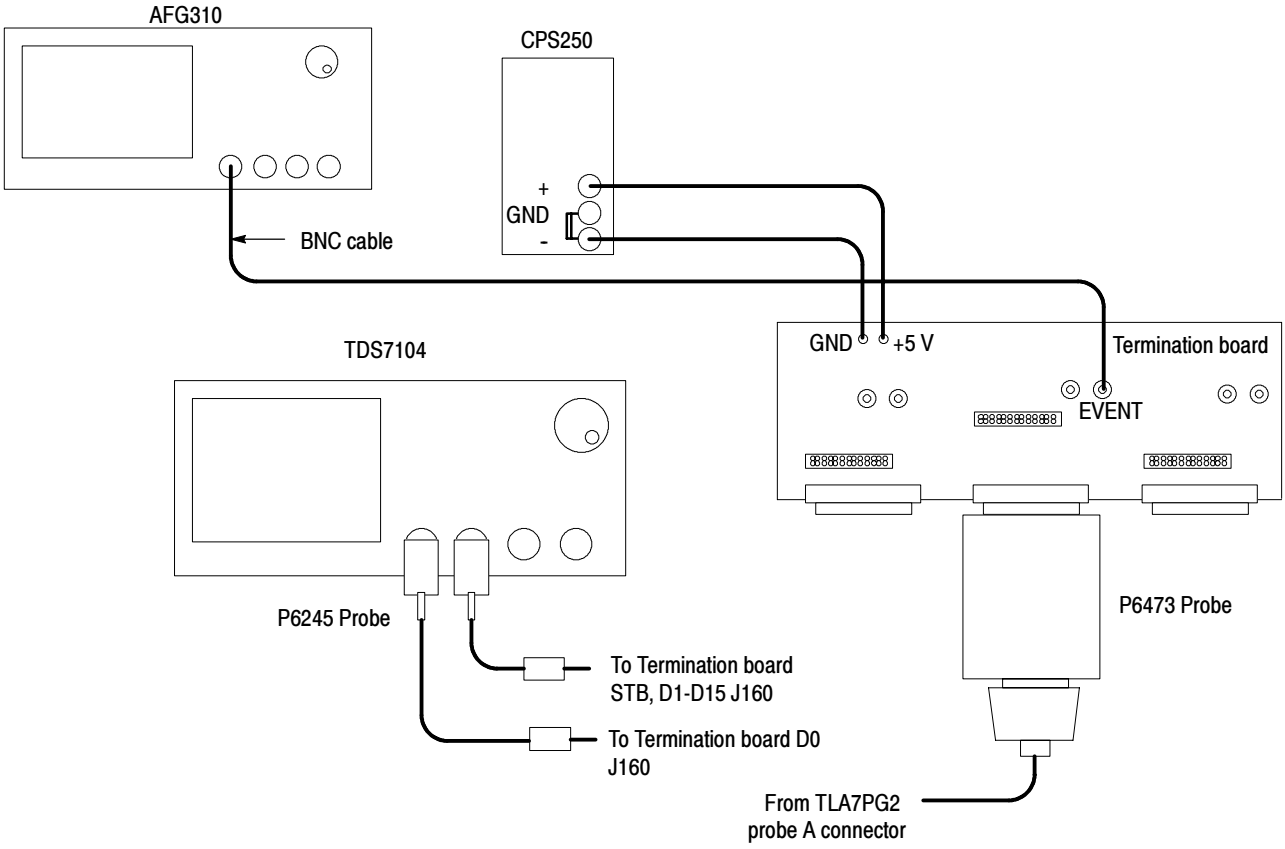


Figure 4- 30: Sequence and Data Output connections

Follow the steps below to complete the functional verification:

1. Connect all equipment as shown in Figure 4–30.
2. Set up the oscilloscope by pressing Default Setup then Factory Init to return the oscilloscope to the default condition.
3. Set the oscilloscope controls as follows:

Displayed channel:	CH1, CH2
Vertical axis (CH1):	5 V/div
Vertical position (CH1):	2.00 div
Vertical position (CH2):	0.00 div
Vertical offset (CHx):	0.0 V
Bandwidth:	Full
Input coupling (CH1, CH2):	DC
Input impedance (CH1, CH2):	50 Ω
Horizontal axis:	1 μs/div
Record length:	5000
Trigger mode:	AUTO
Trigger slope:	Fall
Trigger source:	CH1
Trigger level:	1.65 V
Trigger coupling:	DC
Trigger position:	10%

4. Set up CH1 of the function generator as follows:
   - Frequency 200 kHz
   - CH1 ON
5. Load the TP5PG1.TPG module setup file.
6. Verify that the front panel Accessed indicator blinks on the pattern generator module.
7. Start the pattern generator.
8. Verify that the CH1 waveforms are similar to the waveforms shown in Figure 4–31.
9. Connect the CH2 Probe on the oscilloscope to the STB connector on the termination Board. Verify that the output signal data pattern is similar to the

waveform shown in Figure 4–31. Repeat this procedure on the output signals from D1 through the D15 connector.

10. Stop the pattern generator.

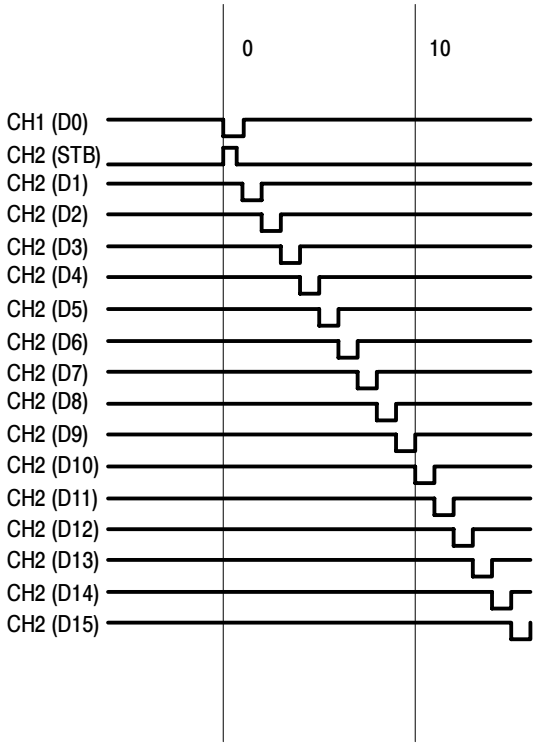


Figure 4- 31: P6473 Sequence and Data sample waveforms

11. Connect Probe B to the termination board.

12. Load the TP6PG1.TPG module setup file.

13. Repeat steps 7 through 10.

14. Connect Probe C to the termination board.

15. Load the TP7PG1.TPG module setup file.

16. Repeat steps 7 through 10.

17. Connect Probe D to the termination board.

18. Load the TP8PG1.TPG module setup file.

19. Start the pattern generator.

20. Verify that the CH1 waveforms are similar to the waveforms shown in Figure 4–32.

21. Connect the CH2 Probe of the oscilloscope to the STB connector on the termination Board. Verify that the output signal data pattern is similar to the waveform shown in Figure 4–32. Repeat this procedure on the output signals from the D1 through the D15 connector.

22. Verify that the Ready, Output**,** and Started front panel indicators are illuminated and the Waiting front panel indicator blinks while the system is operating.

23. Stop the pattern generator.

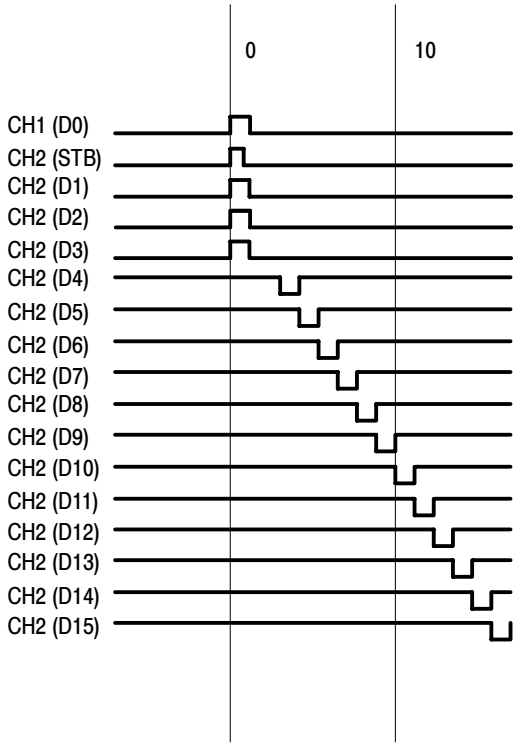


Figure 4- 32: P6473 Sequence and Data strobed sample waveforms

Inhibit Function Test for P6473

This check confirms the Inhibit function of the pattern generator module and the P6473 pattern generator probe.

Setup files:	TP12INH.TPG, TP13INH.TPG
Equipment	Termination board (item 4) TDS7104 Digitizing Oscilloscope (item 2) P6245 1 MΩ 10X Oscilloscope probe (Item 3) AFG310 Function generator (item 5) (used for test by Inhibit External Inhibit input only) CPS250 Power supply (item 6) One BNC cable (item 7) (used for test by Inhibit External Inhibit input only)
Prerequisites	Pattern generator modules *not* merged Connected P6473 probe Test equipment connected as shown in Figure 4-33 Diagnostics pass

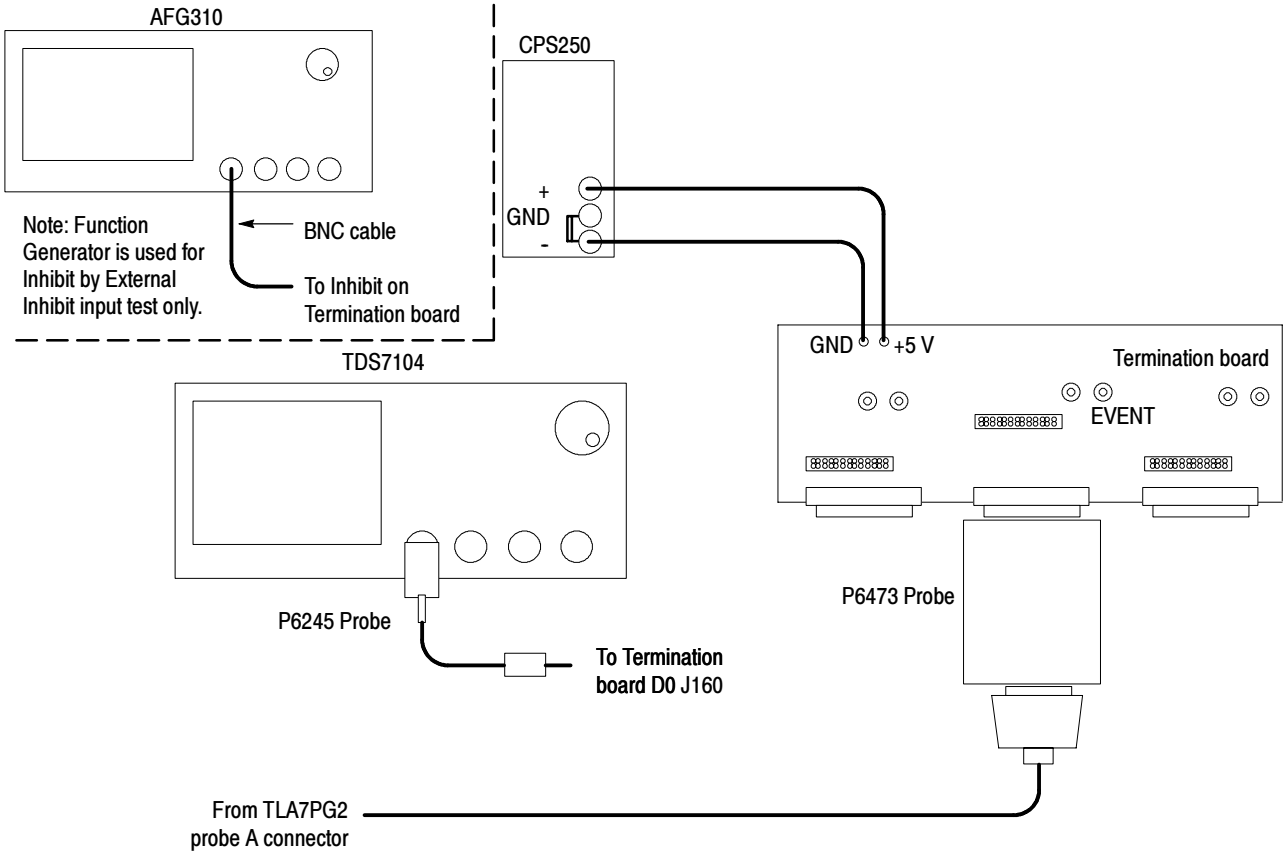


Figure 4- 33: Inhibit function connections

Follow the steps below to complete the functional verification:

1. Connect all equipment as shown in Figure 4–33.(Do not connect the function generator.)
2. Set up the oscilloscope by pressing Default Setup then Factory Init to return the oscilloscope to the default condition.
3. Set the oscilloscope controls as follows:

Displayed channel:	CH1
Vertical axis (CH1, CH2):	2 V/div
Vertical position (CH1):	1.00 div
Vertical offset (CHx):	0.0 V
Bandwidth:	Full
Input coupling (CH1):	DC
Input impedance (CH1):	50 Ω

Horizontal axis:	1 ms/div
Record length:	5000
Trigger mode:	NORM
Trigger slope:	Rise
Trigger source:	CH1
Trigger level:	1.65 V
Trigger coupling:	DC
Trigger position:	50%

4. If you have not already done so, complete the following steps to unmerge the pattern generator modules:
   a. Select System Configuration from the System menu in the pattern generator application.
   b. Click the Merge button between the merged modules to unmerge the two modules.
   c. Click the OK button.

The following procedures must be done sequentially.

Inhibit by Event. This procedure uses the TP12INH.TPG module setup file.

1. Load the TP12INH.TPG module setup file.
2. Open the Program window and select the Block tab.
3. Select Block7.
4. Select Edit→Pattern→Listing to open the Listing window.
5. Select all of the Group1 column by clicking the Group1 label cell.
6. Select Edit→Invert to fill the lines with 0000.
7. Repeat step 2 through step 6 for Group2 Group3, and Group4.
8. Start the pattern generator.
9. Verify that the CH1 output signal has a 500 Hz clock pattern.
10. Stop the pattern generator.

Inhibit by External Inhibit Input. This procedure uses the TP13INH.TPG module setup file.

11. Set up CH 1 of the function generator as follows:

- Frequency 500 Hz
- CH1 ON

12. Connect a BNC Cable from the function generator to J180 (Inhibit) on the termination board.

13. Connect Probe A to the termination Board.

14. Load the TP13INH.TPG module setup file.

15. Open the Program window and select the Block tab.

16. Select Block7.

17. Select Edit→Pattern→Listing to open the Listing window.

18. Select all of the Group1 column by clicking the Group1 label cell.

19. Select Edit→Invert to fill the lines with 0000.

20. Repeat step 15 through step 19 for Group2, Group3, and Group4.

21. Start the pattern generator.

22. Verify that a 500 Hz clock pattern appears on CH1.

23. Repeat step 22 for Probe B, Probe C, and Probe D.

24. Stop the pattern generator.

25. Disconnect Probe D from the termination board.

This completes the functional verification of the P6473 probe.

P6474 Functional Verification Procedures

The following tests and information verify the operation of the P6474 probe.

Internal Clock Frequency Test for P6474

The Internal Clock Frequency test confirms the frequency of the pattern generator module internal clock with the probe.

Setup files:	TP1CLK.TPG
Equipment	Termination board (item 4) TDS7104 Digitizing Oscilloscope (item 2) P6245 1 MΩ 10X Oscilloscope probe (Item 3) CPS250 Power supply (item 6)
Prerequisites	Connected P6474 probe Connect the test equipment as shown in Figure 4-34 Diagnostics pass

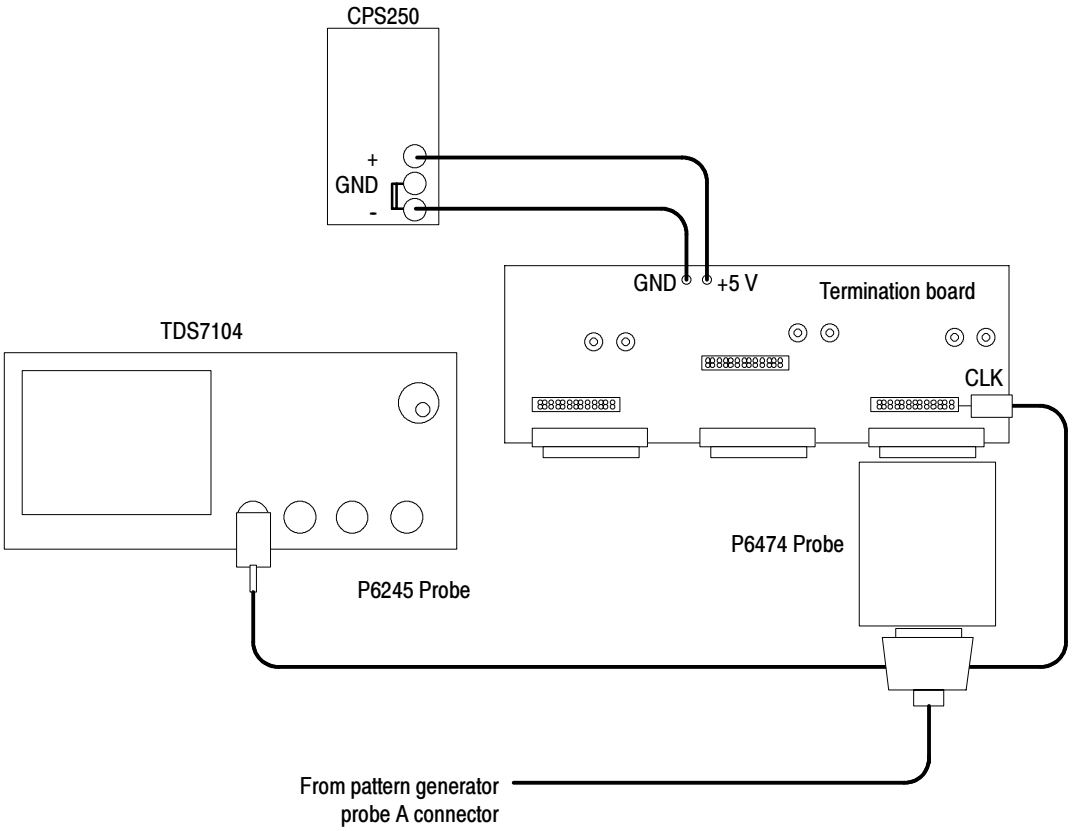


Figure 4-34: Internal Clock Frequency connections

Follow the steps below to complete the functional verification:

1. Connect all equipment as shown in Figure 4–34.
2. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
3. Set the oscilloscope controls as follows:

Displayed channel:	CH1
Vertical axis (CH1):	1 V/div
Vertical position (CH1):	-2.00 div
Vertical offset (CHx):	0.0 V
Bandwidth:	Full
Input coupling:	DC
Input impedance:	50 Ω
Horizontal axis:	1 ns/div
Record length:	5000
Trigger mode:	NORM
Trigger source:	CH1
Trigger slope::	Rise
Trigger level:	1.65 V
Trigger coupling:	DC
Trigger position:	50%

4. Load the TP1CLK.TPG module setup file. When the file is loaded, the pattern generator clock period will be set to 3.7313 ns internally.
5. Start the pattern generator.
6. Use the frequency measurement function of the oscilloscope to verify that the frequency of the pattern generator output signal is about 268 MHz.
7. Stop the pattern generator.
8. Click the Setup icon in the pattern generator application window and change the internal clock period to 9.99 ns.
9. Start the pattern generator.
10. Verify that the frequency of the pattern generator output signal is 100.1 MHz.
11. Stop the pattern generator.

12. Set the pattern generator clock period to 5.0000 µs.

13. Start the pattern generator.

14. Set the oscilloscope Horizontal axis setting to 1.00 µs/div.

15. Verify that the frequency of the pattern generator output signal is 200 kHz.

16. Stop the pattern generator.

17. Set the pattern generator clock period to 1.0000 s.

18. Start the pattern generator.

19. Set the oscilloscope Horizontal axis setting to 200 ms/div.

20. Verify that the frequency of the pattern generator output signal is about 1 Hz.

21. Stop the pattern generator.

Sequence and Data Output Test for P6474

The Sequence and Data Output test confirms that the pattern generator sends the proper sequences and data to the probes. This check also verifies the probe operation.

Setup files: TP5PG0.TPG, TP6PG0.TPG, TP7PG0.TPG, TP8PG0.TPG	
Equipment	Termination board (item 4) TDS7104 Digitizing Oscilloscope (item 2) Two P6245 1 MΩ 10X Oscilloscope probes (Item 3) CPS250 Power supply (item 6) AFG310 Function generator (item 5) One BNC cable (item 7)
Prerequisites	Connected P6474 probe Test equipment connected as shown in Figure 4-35 Diagnostics pass

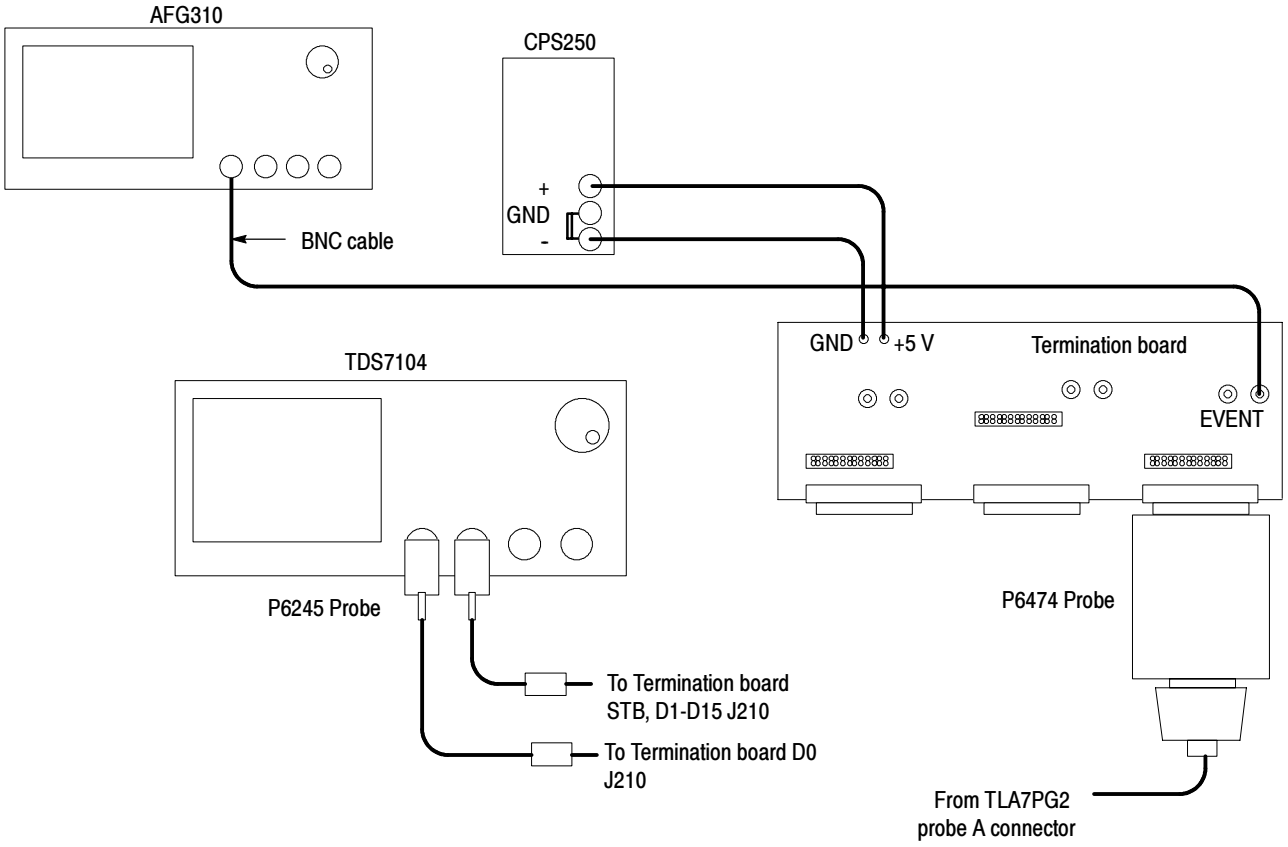


Figure 4- 35: Sequence and Data Output connections

Follow the steps below to complete the functional verification:

1. Connect all equipment as shown in Figure 4–35.
2. Set up the oscilloscope by pressing Default Setup then Factory Init to return the oscilloscope to the default condition.
3. Set the oscilloscope controls as follows:

Displayed channel:	CH1, CH2
Vertical axis (CH1, CH2):	5 V/div
Vertical position (CH1):	2.00 div
Vertical position (CH2):	0.00 div
Vertical offset (CHx):	0.0 V
Bandwidth:	Full
Input coupling (CH1, CH2):	DC
Input impedance (CH1, CH2):	50 Ω
Horizontal axis:	1 μs/div
Record length:	5000
Trigger mode:	AUTO
Trigger slope:	Fall
Trigger source:	CH1
Trigger level:	1.65 V
Trigger coupling:	DC
Trigger position:	10%

4. Set up CH 1 of the function generator as follows:
   - Frequency 200 kHz
   - CH1 ON
5. Load the TP5PG0.TPG module setup.
6. Verify that the front panel Accessed indicator blinks on the pattern generator module.
7. Start the pattern generator.
8. Verify that the CH1 waveforms are similar to the waveforms shown in Figure 4–36.
9. Connect the CH2 Probe on the oscilloscope to the STB connector on the termination Board. Verify that the output signal data pattern is similar to the

waveform shown in Figure 4–36. Repeat this procedure on the output signals from D1 through the D15 connector.

10. Stop the pattern generator.

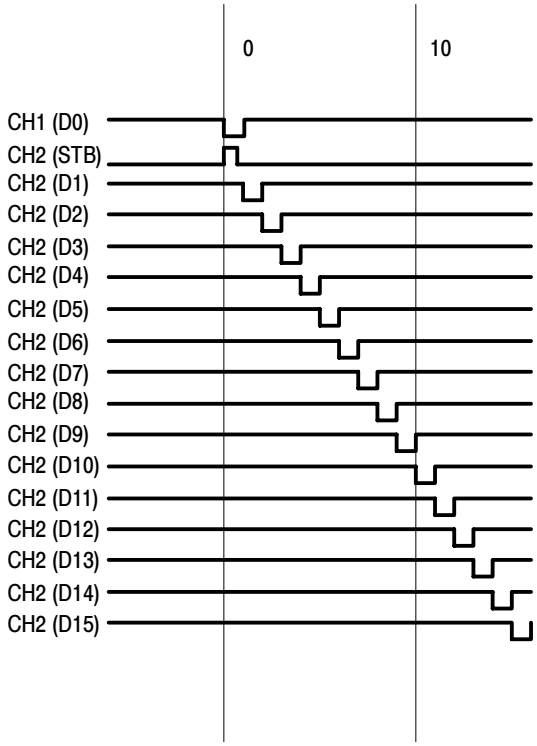


Figure 4- 36: P6474 Sequence and Data sample waveforms

11. Connect Probe B to the termination board.

12. Load the TP6PG0.TPG module setup file.

13. Repeat steps 7 through 10.

14. Connect Probe C to the termination board.

15. Load the TP7PG0.TPG module setup file.

16. Repeat steps 7 through 10.

17. Connect Probe D to the termination board.

18. Load the TP8PG0.TPG module setup file.

19. Start the pattern generator.

20. Verify that the CH1 waveforms are similar to the waveforms shown in Figure 4–37.

21. Connect the CH2 Probe of the oscilloscope to the STB connector on the termination Board. Verify that the output signal data pattern is similar to the waveform shown in Figure 4–37. Repeat this procedure on the output signals from the D1 through the D15 connector.

22. Verify that the Ready, Output**,** and Started front panel indicators are illuminated and the Waiting front panel indicator blinks while the system is operating.

23. Stop the pattern generator.

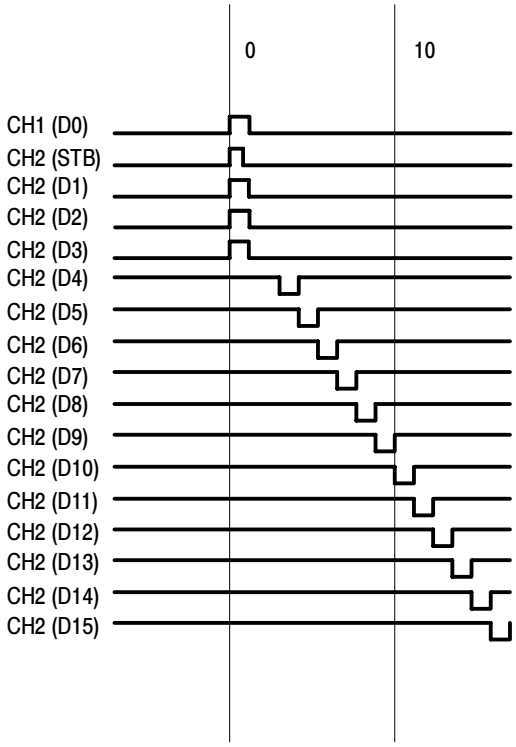


Figure 4-37: P6474 Sequence and Data strobed sample waveforms

Inhibit Function Test for P6474

This check confirms the Inhibit function of the pattern generator module and the P6474 pattern generator probes.

Setup files:	TP12INH.TPG, TP13INH.TPG
Equipment	TDS7104 Digitizing Oscilloscope (item 2) P6245 1 MΩ 10X Oscilloscope probe (Item 3) AFG310 Function generator (item 5) (used for test by Inhibit External Inhibit input only) CPS250 Power supply (item 6) One BNC cable (item 7) (used for test by Inhibit External Inhibit input only)
Prerequisites	Pattern generator modules *not* merged P6474 probe connected Test equipment connected as shown in Figure 4-38 Diagnostics pass

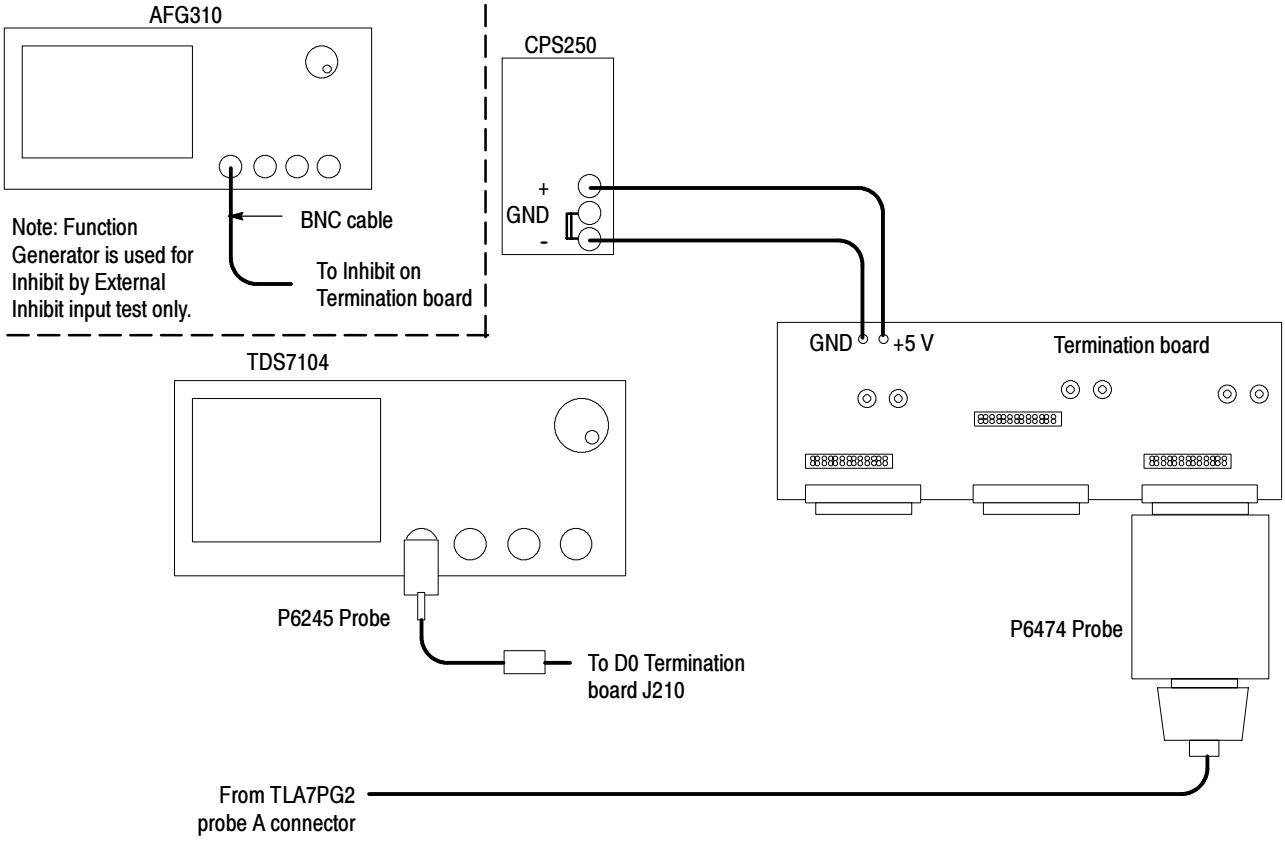


Figure 4-38: Inhibit function connections

Follow the steps below to complete the functional verification:

1. Connect all equipment as shown in Figure 4–38. (Do not connect the function generator.)
2. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
3. Set the oscilloscope controls as follows:

Displayed channel:	CH1
Vertical axis (CH1):	500 mV/div
Vertical position (CH1):	-2.00 div
Vertical offset (CHx):	0.0 V
Bandwidth:	Full
Input coupling (CH1):	DC
Input impedance (CH1):	50 Ω
Horizontal axis:	1.0 ms/div
Record length:	5000
Trigger mode:	NORM
Trigger slope:	Rise
Trigger source:	CH1
Trigger level:	2 V
Trigger coupling:	DC
Trigger position:	50%

4. If you have not already done so, complete the following steps to unmerge the pattern generator modules:
   a. Select System Configuration from the System menu in the pattern generator application.
   b. Click the Merge button between the merged modules to unmerge the two modules.
   c. Click the OK button.

The following tests must be done sequentially:

Inhibit by by Event. Use the TP12INH.TPG module setup file.

5. Load the TP12INH.TPG module setup file.
6. Open the Program window and select the Block tab.

a. Select Block7.

b. Select Edit→ Pattern → Listing to open the Listing window.

c. Select all of the Group1 column by clicking the Group1 label cell.

d. Select Edit → Invert to fill the lines with 0000.

e. Repeat step a through step e for Group2, Group3, and Group4.

7. Start the pattern generator.

8. Verify that the CH1 output signal has a 500 Hz clock pattern.

9. Repeat step 7 for Probe B, Probe C, and Probe D.

10. Stop the pattern generator.

Inhibit by External Inhibit Input. Use the TP13INH.TPG module setup file.

11. Set up CH 1 of the function generator as follows:

- Frequency 500 Hz
- CH1 ON

12. Connect a BNC Cable from the function generator to J230 (Inhibit) on the termination board.

13. Connect Probe A to the termination Board.

14. Load the TP13INH.TPG module setup file.

15. Open the Program window and select the Block tab.

a. Select Block7.

b. Select Edit→ Pattern → Listing to open the Listing window.

c. Select all of the Group1 column by clicking the Group1 label cell.

d. Select Edit → Invert to fill the lines with 0000.

e. Repeat step a through step e for Group2, Group3, and Group4.

16. Start the pattern generator.

17. Verify that a 500 Hz clock pattern appears on CH1.

18. Repeat step 15 for Probe B, Probe C, and Probe D.

19. Stop the pattern generator.

P6475 Functional Verification Procedures

The following tests and information verify the operation of the P6475 probe.

P6475 Power On/Off

Follow the procedures below to power on and power off the P6475 variable probe:

1. Power on the P6475
2. Power on the TLA

1. Power off the TLA
2. Power off the P6475

Connect the P6475 to the Oscilloscope

Connect CH1 on the oscilloscope to the Clock output connector on the P6475.

Internal Clock Frequency Test for P6475

The Internal Clock Frequency test confirms the frequency of the pattern generator module internal clock with the probe.

Setup files:	TP1CLK.TPG
Equipment	TDS7104 Digitizing Oscilloscope (item 2) One BNC to SMB cable (item 9)
Prerequisites	Connect probe as shown in Figure 4-39 Connect the test equipment as shown in Figure 4-39 Diagnostics pass

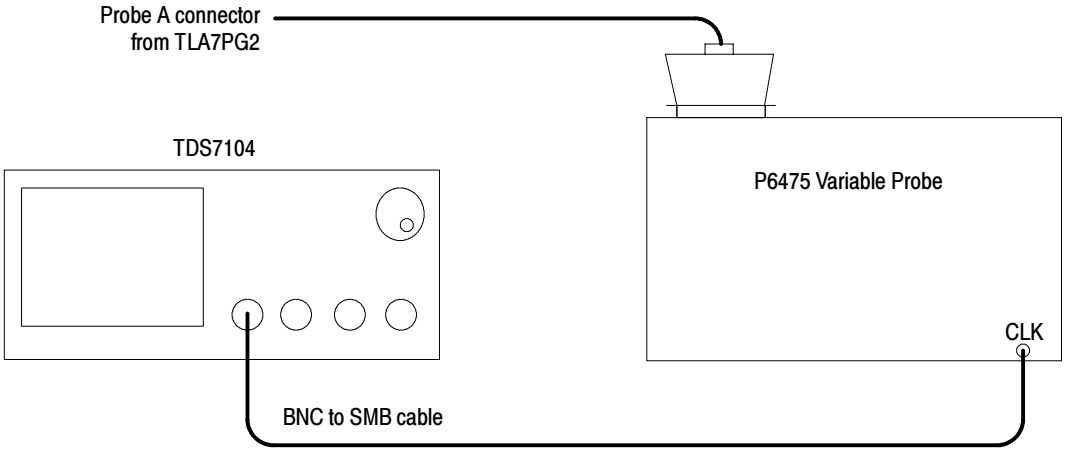


Figure 4-39: Internal Clock Frequency connections

Follow the steps below to complete the functional verification:

1. Connect all equipment as shown in Figure 4–39.
2. Set up the oscilloscope by pressing Default Setup then Factory Init to return the oscilloscope to the default condition.
3. Set the oscilloscope controls as follows:

Displayed channel:	CH1
Vertical axis (CH1):	500 mV/div
Vertical position (CH1):	-2.00 div
Vertical offset (CHx):	0.0 V
Bandwidth:	Full
Input coupling:	DC
Input impedance:	50 Ω
Horizontal axis:	1 ns/div
Record length:	5000
Trigger mode:	NORM
Trigger source:	CH1
Trigger slope::	Rise
Trigger level:	0.5 V
Trigger coupling:	DC
Trigger position:	50%

4. Load the TP1CLK.TPG module setup file. When the file is loaded, the pattern generator clock period will be set to 3.7313 ns internally.
5. Start the pattern generator.
6. Use the frequency measurement function of the oscilloscope to verify that the frequency of the pattern generator output signal is about 268 MHz.
7. Stop the pattern generator.
8. Click the Setup icon in the pattern generator application window and change the internal clock period to 9.99 ns.
9. Start the pattern generator.
10. Verify that the frequency of the pattern generator output signal is 100.1 MHz.
11. Stop the pattern generator.
12. Set the pattern generator clock period to 5.0000 μs.
13. Start the pattern generator.
14. Set the oscilloscope Horizontal axis setting to 1.00 μs/div.
15. Verify that the frequency of the pattern generator output signal is 200 kHz.
16. Stop the pattern generator.
17. Set the pattern generator clock period to 1.0000 s.
18. Start the pattern generator.
19. Set the oscilloscope Horizontal axis setting to 200 ms/div.
20. Verify that the frequency of the pattern generator output signal is about 1 Hz.
21. Stop the pattern generator.

Sequence and Data Output Test for P6475

The Sequence and Data Output test confirms that the pattern generator sends the proper sequences and data to the P6475. This check also verifies the probe operation.

You must have four P6475 probes to complete this procedure or power down the TLA mainframe and move the P6475 connection from Probe A to B to C to D.

Setup files: TP5PG1.TPG, TP6PG1.TPG, TP7PG1.TPG, TP8PG1.TPG	
Equipment	TDS7104 Digitizing Oscilloscope (item 2) AFG310 Function generator (item 5) Three BNC to SMB cables (item 9)
Prerequisites	Connect the probe Test equipment connected as shown in Figure 4-40 Diagnostics pass

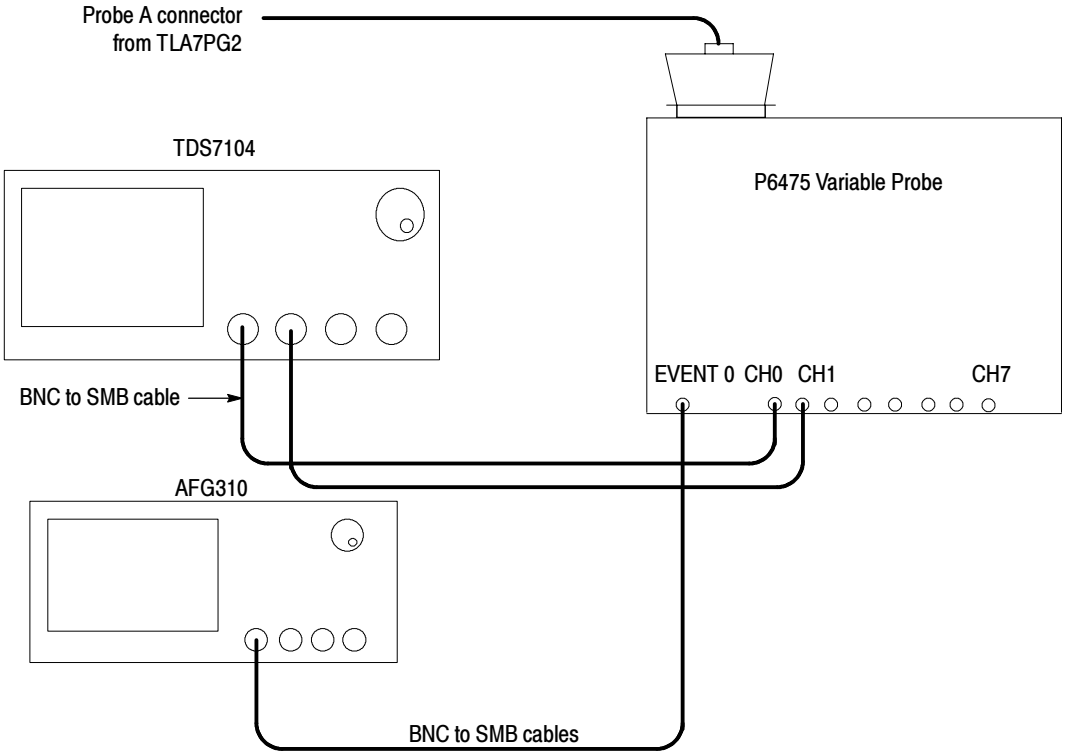


Figure 4-40: Sequence and Data Output connections

Follow the steps below to complete the functional verification:

1. Connect all equipment as shown in Figure 4–40.
2. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
3. Set the oscilloscope controls as follows:

Displayed channel::	CH1, CH2
Vertical axis (CH1, CH2):	500 mV/div
Vertical position (CH1):	2.00 div
Vertical position (CH2):	0.00 div
Vertical offset (CHx)	0.0 V
Bandwidth:	Full
Input coupling (CH1, CH2):	DC
Input impedance (CH1, CH2):	50 Ω
Horizontal axis:	1 μs/div
Record length:	5000
Trigger mode:	AUTO
Trigger slope::	Fall
Trigger source:	CH1
Trigger level:	0.5 V
Trigger coupling:	DC
Trigger position:	10%

4. Set up CH1 of the function generator as follows:

- Frequency 200 kHz
- CH1 ON

5. Connect the Probe A connector on the TLA7PG2 to the P6475.

6. Load the TP5PG1.TPG module setup file.

7. Verify that the front panel Accessed indicator blinks on the pattern generator module.

8. Start the pattern generator.

9. Verify that the CH1 waveform is similar to the waveforms shown in Figure 4–41.

10. Connect the CH2 BNC to SMB cable on the oscilloscope to the CH1 connector on the P6475.

11. Verify that the output signal data pattern is similar to the waveform shown in Figure 4–41.

12. Repeat steps 10 and 11 for CH2 through CH7 on the P6475.

13. Stop the pattern generator.

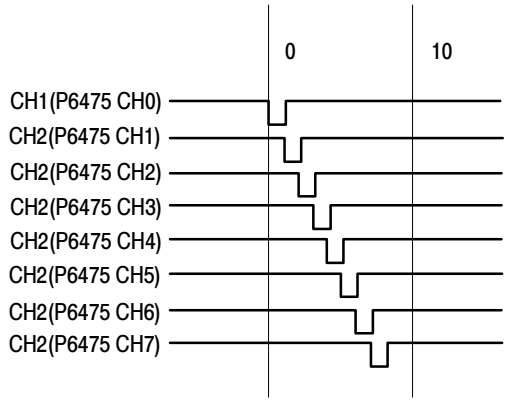


Figure 4-41: P6475 Sequence and Data sample waveforms

14. Connect the Probe B connector on the TLA7PG2 to the P6475.

15. Load the TP6PG1.TPG module setup file.

16. Repeat steps 7 through 10.

17. Connect the Probe C connector on the TLA7PG2 to the P6475.

18. Load the TP7PG1.TPG module setup file.

19. Repeat steps 7 through 10.

20. Connect the Probe D connector on the TLA7PG2 to the P6475.

21. Load the TP8PG1.TPG module setup file.

22. Start the pattern generator.

23. Verify that the CH1 waveform is similar to the waveforms shown in Figure 4-42.

24. Connect the CH2 BNC to SMB cable on the oscilloscope to the CH1 connector on the P6475.

25. Verify that the output signal data pattern is similar to the waveform shown in Figure 4-42.

26. Repeat steps 24 and 25 for CH2 through CH7 on the P6475.

27. Verify that the CH0 through CH7 waveforms are similar to the waveforms shown in Figure 4-42.

28. Verify that the Ready, Output**,** and Started front panel indicators are illuminated and the Waiting front panel indicator blinks while the system is operating.

29. Stop the pattern generator.

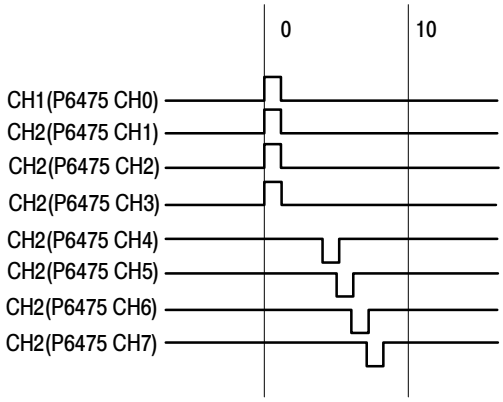


Figure 4-42: P6475 Sequence and Data strobed sample waveforms

Inhibit Function Test for P6475

This test confirms the Inhibit function of the pattern generator module and the P6475 pattern generator probes.

Setup files:	TP12INH.TPG, TP13INH.TPG
Equipment	TDS7104 Digitizing Oscilloscope (item 2) AFG310 Function generator (item 5) (used for test by Inhibit External Inhibit input only) Two BNC to SMB cable (item 9)
Prerequisites	Pattern generator modules *not* merged P6475 probe connected Test equipment connected as shown in Figure 4-43 Diagnostics pass

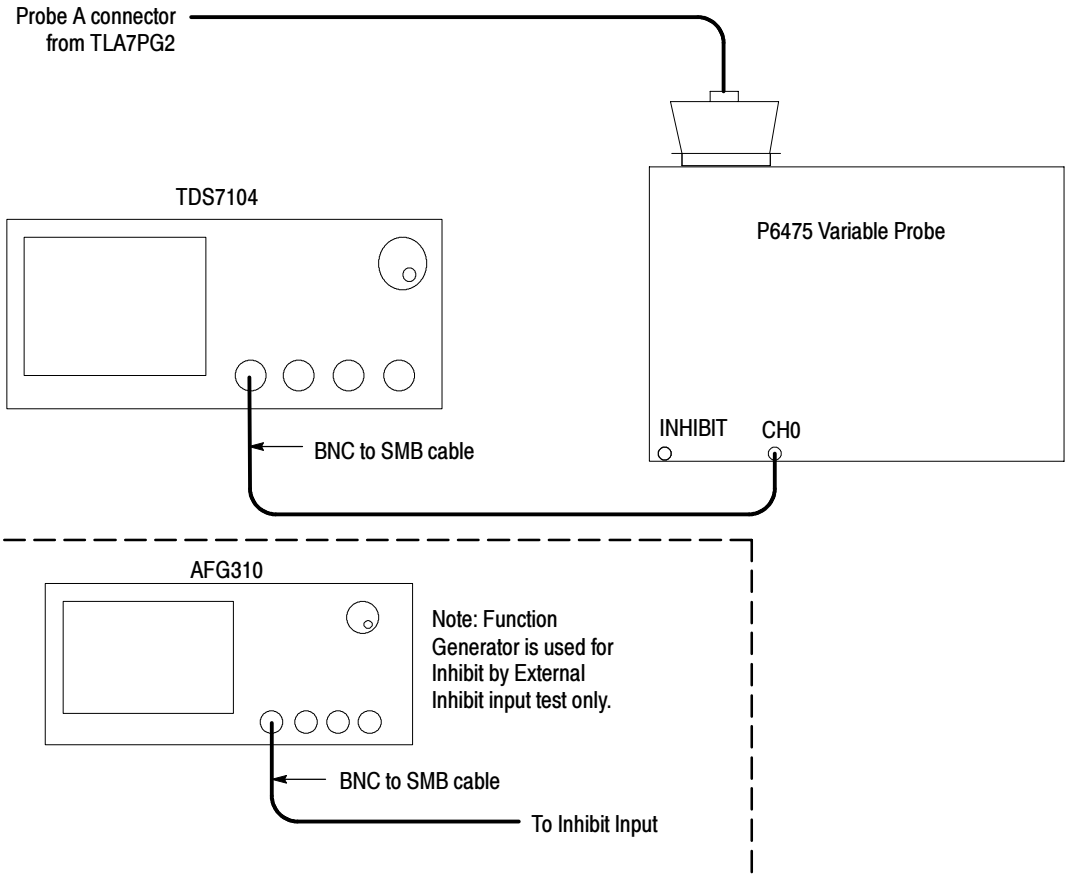


Figure 4- 43: Inhibit function connections

Follow the steps below to complete the functional verification:

1. Connect all equipment as shown in Figure 4–43. (Do not connect the function generator.)
2. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
3. Set the oscilloscope controls as follows:

Displayed channel:	CH1
Vertical axis (CH1):	500 mV/div
Vertical position (CH1):	-2.00 div
Vertical offset (CHx):	0.0 V
Bandwidth:	Full
Input coupling (CH1):	DC

Input impedance (CH1):	50 Ω
Horizontal axis:	1 ms/div
Record length:	5000
Trigger mode:	NORM
Trigger slope:	Rise
Trigger source:	CH1
Trigger level:	2 V
Trigger coupling:	DC
Trigger position:	50%

4. If you have not already done so, complete the following steps to unmerge the pattern generator modules:
   a. Select System Configuration from the System menu in the pattern generator application.
   b. Click the Merge button between the merged modules to unmerge the two modules.
   c. Click the OK button.

The following tests must be done sequentially:

Inhibit by Event. Use the TP12INH.TPG module setup file.

5. Load the TP12INH.TPG module setup file.
6. Start the pattern generator.
7. Verify that the CH1 output signal has a 500 Hz clock pattern.
8. Repeat step 7 for Probe B, Probe C, and Probe D.
9. Stop the pattern generator.

Inhibit by External Inhibit Input. Use the TP13INH.TPG module setup file.

10. Set up CH 1 of the function generator as follows:
    - Frequency 500 Hz
    - CH1 ON
11. Connect a BNC to SMB cable from the function generator to the INHIBIT connector on the P6475.
12. Connect the Probe A connector on the TLA7PG2 to the P6475.

13. Load the TP13INH.TPG module setup file.

14. Start the pattern generator.

15. Verify that a 500 Hz clock pattern appears on CH1.

16. Repeat step 15 for Probe B, Probe C, and Probe D.

17. Stop the pattern generator.

18. Disconnect the BNC to SMB cable from the INHIBIT connector on the P6475.

19. Stop the pattern generator.

P6475 Data Format and CH6 Output Mode Test

The following procedures verifies the data formats and CH6 output modes for the P6475.

Setup files:	TP19V.TPG
Equipment	TDS7104 Digitizing Oscilloscope (item 2) 4 BNC to SMB cables (item 9)
Prerequisites	P6475 probe connected Test equipment connected as shown in Figure 4-44 Diagnostics pass

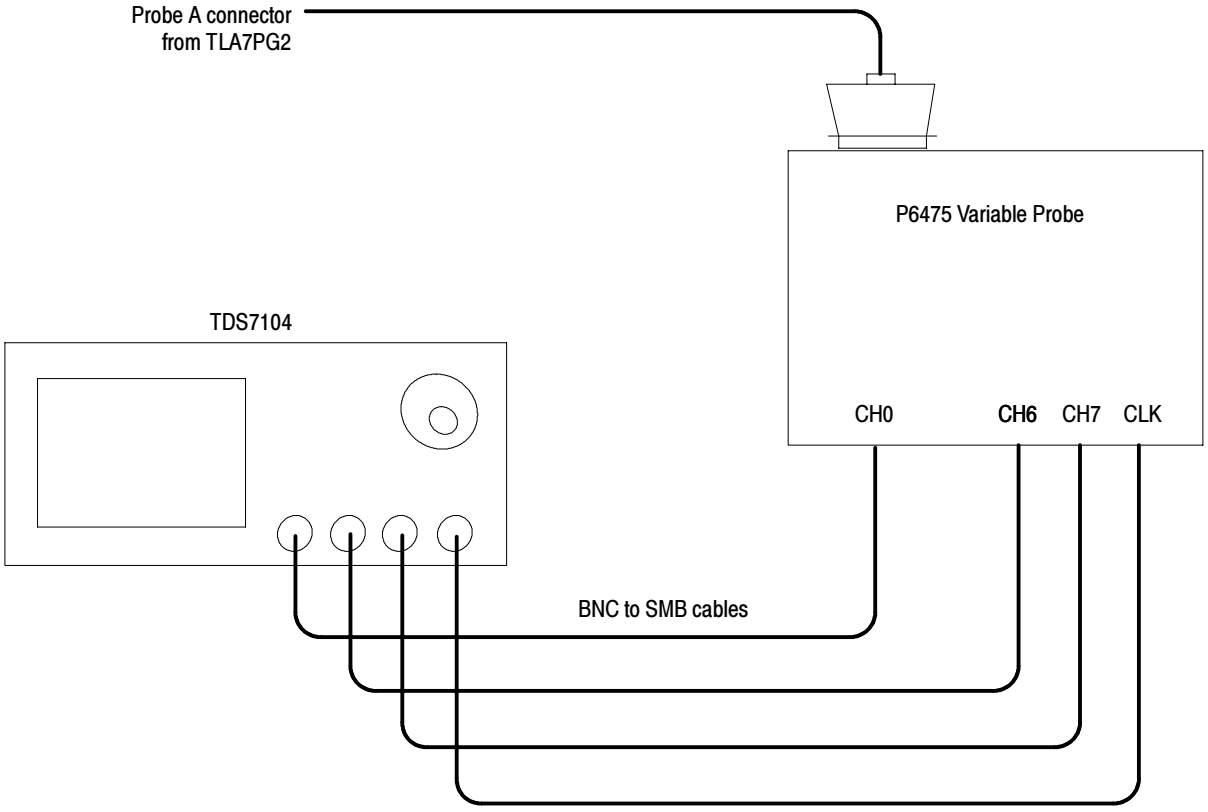


Figure 4-44: P6475 Data Output and CH6 Output Mode connections

Follow the steps below to complete the functional verification:

1. Connect all equipment as shown in Figure 4-44.
2. Set up the oscilloscope by pressing Default Setup then Factory Init to return the oscilloscope to the default condition.

3. Set the oscilloscope controls as follows:

Displayed channel:	CH1, CH2, CH3, CH4
Vertical axis (all channels):	1.0 V/div
Vertical position (all channels):	-1.00 div
Vertical offset (all channels):	0.0 V
Bandwidth (all channels):	Full
Input coupling (all channels):	DC
Input impedance (all channels):	50 Ω
Repetitive Signal::	On (Enable ET)
Horizontal axis:	40 ns/div
Record length:	500
Trigger mode:	AUTO
Trigger slope:	Rise
Trigger source:	CH1
Trigger level:	500 mV
Trigger coupling:	DC
Trigger position:	10%

4. Load the TP19V.TPG module setup file.
5. Start the pattern generator.
6. Verify that the low level is approximately -0.5 V and the high level is approximately 1.5 V for all of the traces.
7. Open the Probe Setup window and change the slew rate for all channels to 0.5 V/ns.
8. Verify that all of the traces have a longer rise time.
9. Set the Trigger Position of the oscilloscope to 10%.
10. Deselect CH4 of the oscilloscope.
11. Set the vertical scale to 2 V/div for CH1, CH2, and CH3 on the oscilloscope.
12. Set the oscilloscope vertical position as follows:
    - CH1 2 div
    - CH2 0 div
    - CH3 -2 div

13. Set the oscilloscope horizontal axis to 20 ns/div.

14. Change the slew rate to 2.5 V/ns.

15. Verify that the waveforms are similar to those shown in Figure 4–45.

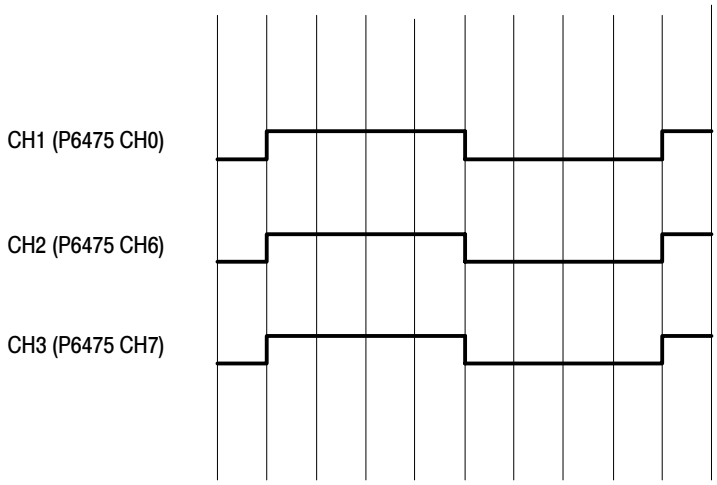


Figure 4-45: NRZ data format

16. Select the Probe Setup window and change the data format of P6475 CH6 and CH7 to RZ.

17. Verify that the waveforms are similar to those shown in Figure 4–46.

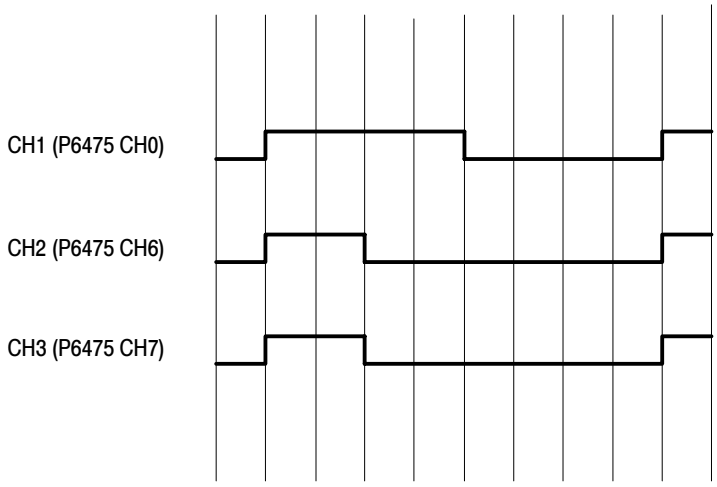


Figure 4-46: RZ data format

18. Select the Probe Setup window and change the data format of CH6 and CH7 to R1.

19. Verify that the waveforms are similar to those shown in Figure 4–47.

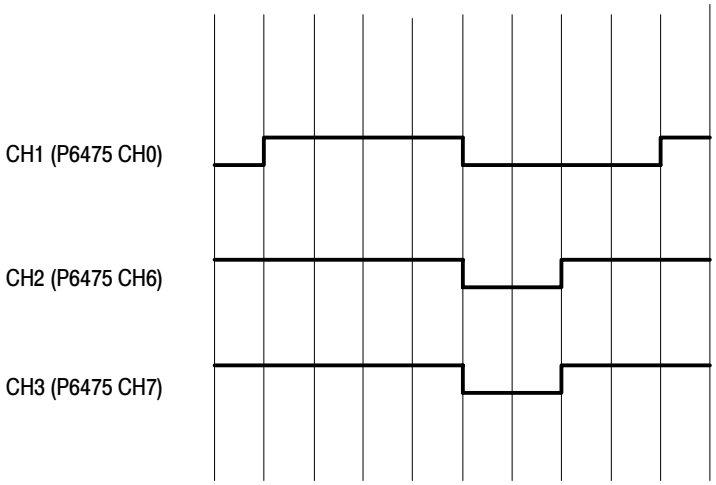


Figure 4-47: R1 data format

20. Select the Probe Setup window and change the data format of CH6 and CH7 to NRZ.

21. Set the delay of CH7 to 50 ns.

22. Stop the pattern generator.

23. Select the Probe Setup window and set the CH6 output mode to CH6 OR CH7.

24. Start the pattern generator.

25. Verify that the waveforms are similar to those shown in Figure 4–48.

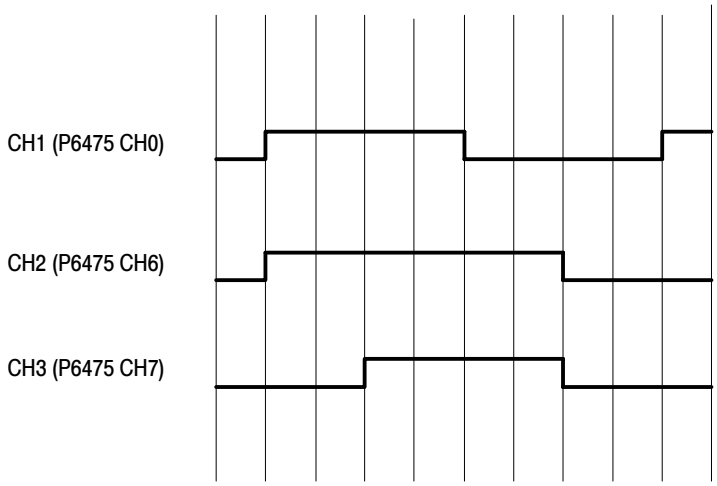


Figure 4- 48: OR logic

26. Stop the pattern generator.

27. Select the Probe Setup window and set the CH6 output mode to CH6 AND CH7.

28. Start the pattern generator.

29. Verify that the waveforms are similar to what are shown in Figure 4–49.

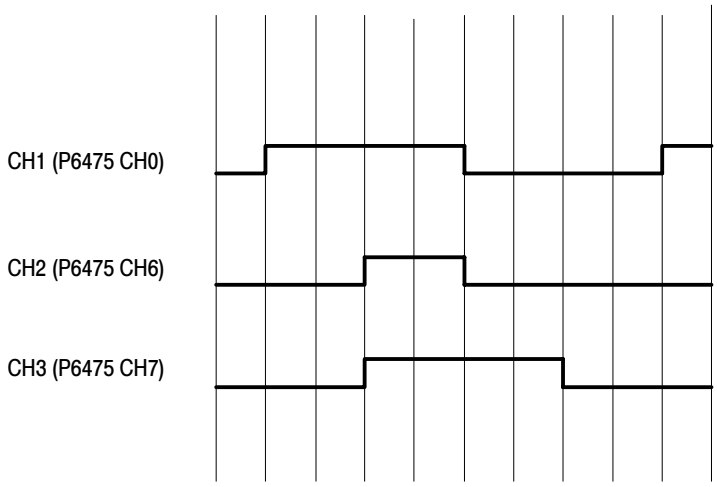


Figure 4- 49: AND logic

30. Stop the pattern generator.

31. Select the Probe Setup window and set the CH6 output mode to CH6 AND (NOT CH7).

32. Start the pattern generator.

33. Verify that the waveforms are similar to those shown in Figure 4–50.

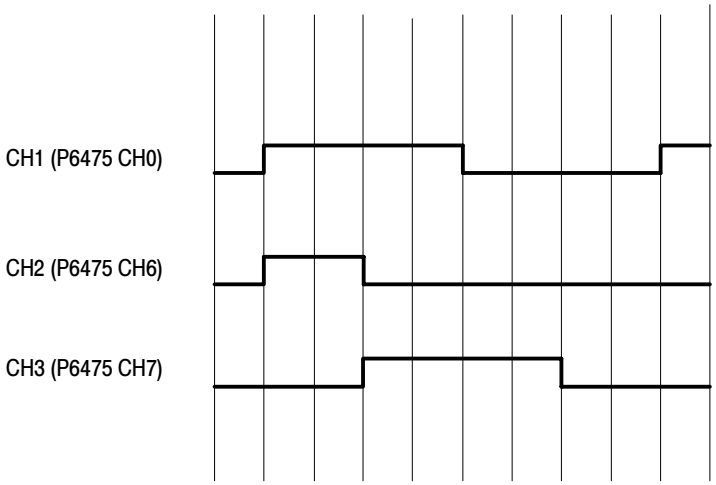


Figure 4-50: CH6 AND (NOT CH7)

34. Stop the pattern generator.

35. Select the Probe Setup window and set the CH6 output mode to CH6 OR (NOT CH7).

36. Start the pattern generator.

37. Verify that the waveforms are similar to those shown in Figure 4–51.

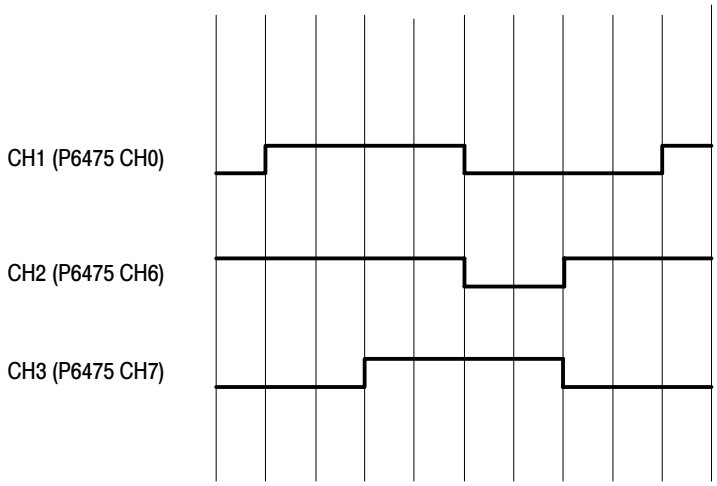


Figure 4- 51: CH6 OR (NOT CH7)

38. Stop the pattern generator.

This completes the functional verification of the P6475 probe.

Performance Verification Procedures

The tests in this section comprise an extensive, valid confirmation of performance and functionality when the following requirements are met:

- The pattern generator module and probes pass all of the functional tests in the *Pattern Generator Module Functional Verification* section.
- The PV/Adjust software must be loaded on the hard disk drive.
- The pattern generator module must be installed in a mainframe, operating for at least 30 minutes, and operating at an ambient temperature between +20° C and +30° C.
- The instrument must be in an operating environment within the limits described in the *Specifications* section of the *Tektronix Logic Analyzer Family User Manual*.

These procedures use external, traceable signal sources to directly test the characteristics that are designated as checked (✓) in the *Specifications* chapter of this manual. In addition to the basic setup, you will need some of the equipment shown in Table 4–2 on page 4–5 to complete the performance verification procedures. Use Table 4–2 for equipment specifications. If you substitute equipment, always choose instruments that meet or exceed the minimum requirements specified.

There are no certifiable parameters for the pattern generator module.

The Delay Accuracy test is a certifiable parameter for the P6475.

TLA7PG2 Maximum Operating Frequency

This procedure verifies the maximum operating frequency of the pattern generator module. The procedure uses four separate test files, one for each probe connector as indicated below.

Setup files:	For P6470, P6471, P6472, and P6474: TP15PVP0.TPG (Performance check using probe A) TP16PVP0.TPG (Performance check using probe B) TP17PVP0.TPG (Performance check using probe C) TP18PVP0.TPG (Performance check using probe D) For P6473 and P6475: TP15PVP1.TPG (Performance check using probe A) TP16PVP1.TPG (Performance check using probe B) TP17PVP1.TPG (Performance check using probe C) TP18PVP1.TPG (Performance check using probe D)
Equipment	Termination board (item 4) (not used with P6475) TDS7104 Digitizing Oscilloscope (item 2) Two P6245 1 MΩ 10X Oscilloscope probe (Item 3) AFG310 Function generator (item 5) CPS250 Power supply (item 6) (not used with P6475) One BNC cable (item 7) (not used with P6475) 3 BNC to SMB cables (item 9)
Prerequisites	Probes connected Test equipment connected as shown in Figure 4-52 or Figure 4-53 Functional Verifications pass Diagnostics pass

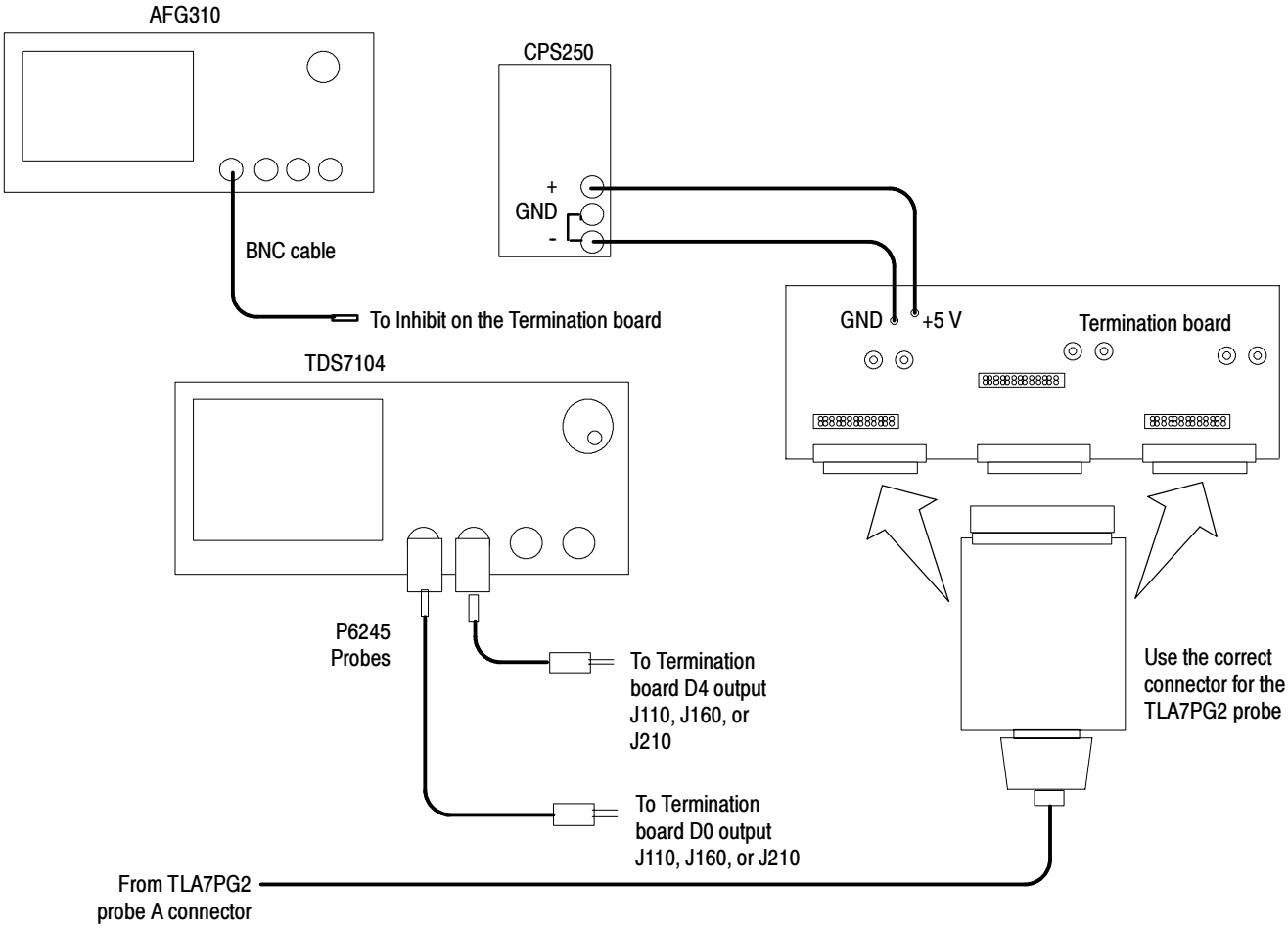


Figure 4- 52: Maximum Operating Frequency Connections using P6470, P6471, P6472, P6473, or P6474 (Example)

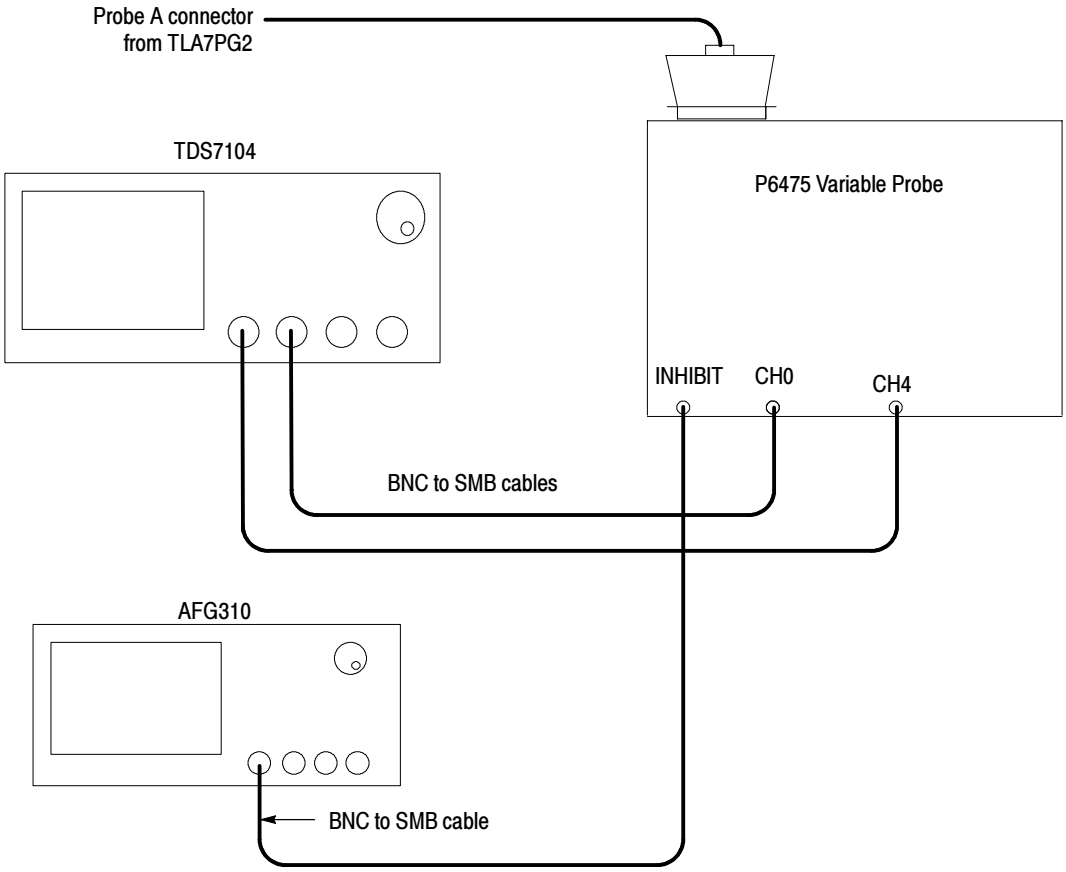


Figure 4-53: Maximum Operating Frequency Connections using a P6475 probe

Follow the steps below to complete the functional verification:

1. Connect all equipment as shown in Figure 4-52 or Figure 4-53.
2. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
3. Set the oscilloscope controls as follows:

Displayed channel:	CH1, CH2
Vertical axis (CH1, CH2):	
P6470, P6473, P6474	5 V/div
P6471, P6472, P6475	1 V/div
Vertical position (CH1):	
P6470, P6473, P6474, P6475	2.00 div
P6471, P6472	4.00 div

Vertical position (CH2):	
P6470, P6473, P6474, P6475	0.0 div
P6471, P6472	2.00 div
Vertical offset (CHx):	
P6472 PECL mode	5 V
P6472 LVPECL mode	3.3 V
P6470, P6471, P6473, P6474, P6475	0.0 V
Bandwidth:	Full
Input coupling (CH1, CH2):	DC
Input impedance (CH1, CH2):	50 Ω
Horizontal axis:	12.5 ns/div
Record length:	5000
Trigger mode:	AUTO
Trigger slope:	Rise
Trigger source:	CH1
Trigger level:	
P6472 PECL mode	3.7 V
P6470, P6472 LVPECL mode	2 V
P6471	-1.3 V
P6473, P6474	1.65 V
P6475	0.5 V
Trigger coupling:	DC
Trigger position:	50%

4. Set up CH 1 of the function generator as follows:
   - Frequency 500 kHz
   - CH1 ON
5. Load the module setup file:
   - TP15PVP0.TPG for P6470, P6471, P6472, or P6474
   - TP15PVP1.TPG for P6473 or P6475

   After the file is loaded, the TLA7PG2 clock period is set to 7.4627 ns.
6. Start the pattern generator.

7. Verify that the data pattern output from the pattern generator probes is similar to the waveform in Figure 4–54 (ignore the small amount of timing skew between the channels).

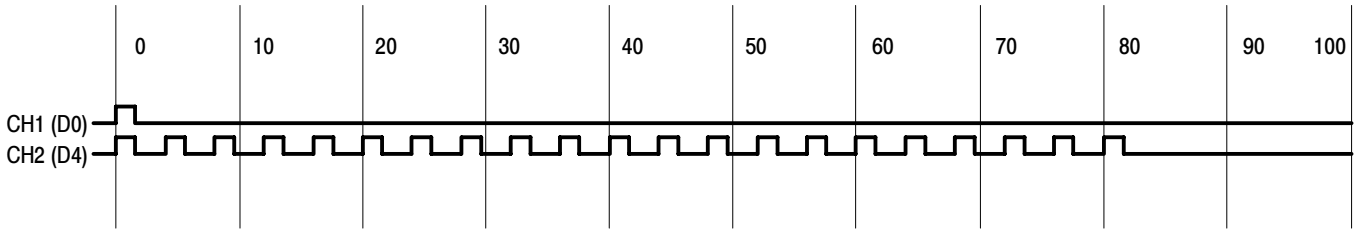


Figure 4- 54: Timing chart for the Maximum Operating Frequency check

8. Stop the pattern generator.
9. Connect the Probe B connector from the TLA7PG2 to the Termination board or to the P6475.
10. Load the module setup file:
    - TP16PVP0.TPG for P6470, P6471, P6472, or P6474
    - TP16PVP1.TPG for P6473 or P6475
11. Repeat steps 6 through 8.
12. Connect the Probe C connector from the TLA7PG2 to the Termination board or to the P6475.

13. Load the module setup file:
    - TP17PVP0.TPG for P6470, P6471, P6472, or P6474
    - TP17PVP1.TPG for P6473 or P6475
14. Repeat steps 6 through 8.
15. Connect the Probe D connector from the TLA7PG2 to the Termination board or to the P6475.
16. Load the module setup file:
    - TP18PVP0.TPG for P6470, P6471, P6472, or P6474
    - TP18PVP1.TPG for P6473 or P6475
17. Repeat steps 6 through 8.

P6475 Delay Accuracy Check

The following procedure verifies the Delay Accuracy.

Setup files:	TP19V.TPG
Equipment	TDS7104 Digitizing Oscilloscope (item 2) 3 BNC to SMB cables (item 9)
Prerequisites	P6475 probe connected Test equipment connected as shown in Figure 4-55 Diagnostics pass

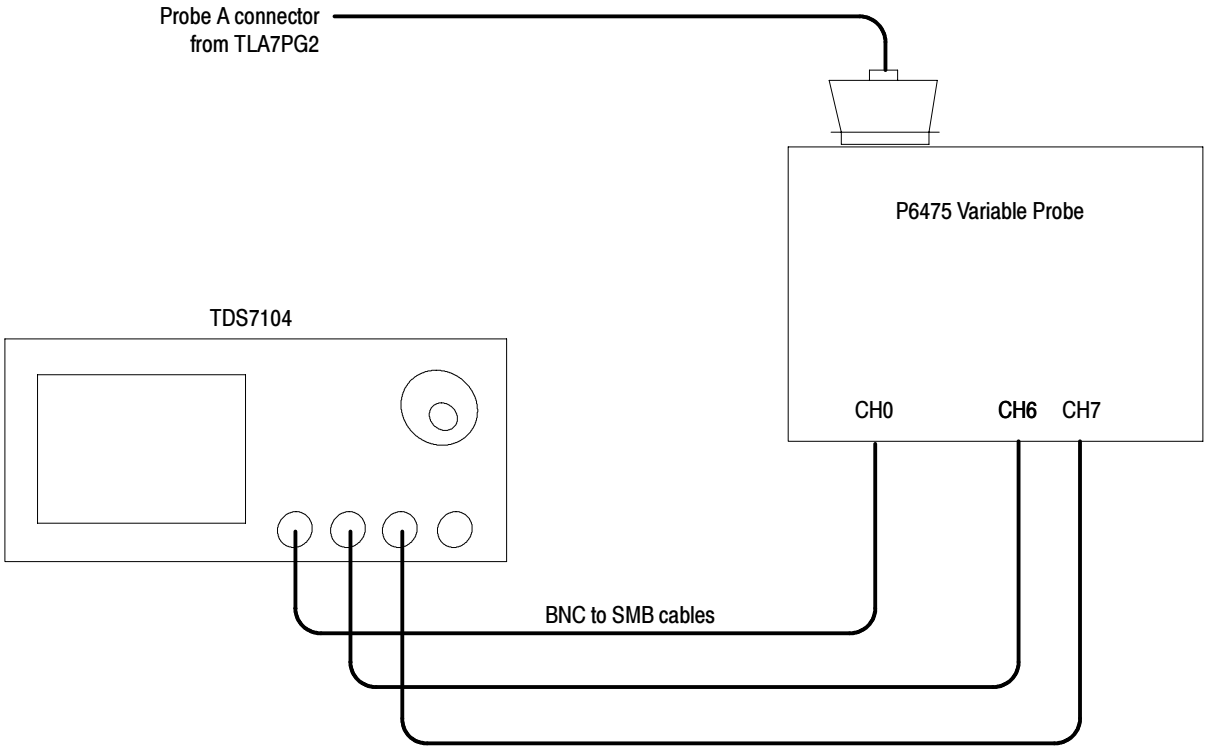


Figure 4-55: Delay Accuracy connections

1. Set up the oscilloscope by pressing Setup, Factory, and then OK Confirm Factory Init to return the oscilloscope to the default condition.
2. Set the oscilloscope controls as follows:

Displayed channel:	CH1, CH2, CH3
Vertical axis (CH1, CH2, CH3):	500 mV/div
Vertical position (CH1, CH2, CH3):	-1.00 div
Vertical offset (CH1, CH2, CH3):	0.0 V
Bandwidth (CH1, CH2, CH3):	Full
Input coupling (CH1, CH2, CH3):	DC
Input impedance (CH1, CH2, CH3):	50 Ω
Horizontal axis:	12.5 ns/div
Repetitive Signal:	ON (Enable ET)
Record length:	500
Trigger mode:	AUTO
Trigger slope:	Rise
Trigger source:	CH1
Trigger level:	500 mV
Trigger coupling:	DC
Trigger position:	10%
Acquisition mode:	Average
Average count:	16

3. Load the TP19V.TPG module setup file.
4. Change the Delay Range and Delay of CH6 and CH7 to the value listed in Table 4–5.
5. Verify that the delay time measured is within the tolerance.

Table 4-5: Delay

Delay range	Delay	Minimum	Maximum
0 - 20 ns	0 ns	-0.80 ns	0.80 ns
	10 ns	8.90 ns	11.10 ns
	20 ns	18.60 ns	21.40 ns
15 - 30 ns	15 ns	13.75 ns	16.25 ns
	30 ns	28.30 ns	31.70 ns

Table 4-5: Delay (Cont.)

Delay range	Delay	Minimum	Maximum
25 - 40 ns	25 ns	23.45 ns	26.55 ns
	40 ns	38.00 ns	42.00 ns
35 - 50 ns	35 ns	33.15 ns	36.85 ns
	50 ns	47.70 ns	52.30 ns

Photocopy the P6475 Variable Probe Test Record on page 4–6 and add the test data that you acquire from this test.

This completes the performance verification tests for the pattern generator probes.

Adjustment Procedures

There are no adjustment procedures for the TLA7PG2 Pattern Generator module or for the pattern generator probes.

Maintenance

This chapter provides procedures for inspecting and cleaning the pattern generator, removing and replacing internal chassis components, and isolating problems to the board or replacement module level.

To repair, you must exchange or replace the failed part; this manual does not provide component-level procedures for isolating components on the failed part.

Preparation

The information in this section is designed for use by qualified service personnel. Read the *General Safety Summary* and the *Service Safety Summary* at the front of this manual before attempting any procedures in this chapter. Refer to the *Operating Instructions* section for information on the location of controls, indicators, and connectors used with the chassis.

Preventing ESD

When performing any service which requires internal access to the pattern generator, adhere to the following precautions to avoid damaging internal circuit boards and their components due to electrostatic discharge (ESD).

CAUTION. *Many components within the chassis are susceptible to static-discharge damage. Service the chassis only in a static-free environment.*

Observe standard handling precautions for static-sensitive devices while servicing the chassis.

Always wear a grounded wrist strap, or equivalent, while servicing the chassis.

1. Minimize handling of static-sensitive circuit boards.
2. Transport and store static-sensitive circuit boards in their static protected containers or on a metal rail. Label any package that contains static-sensitive boards.
3. Discharge the static voltage from your body by wearing a grounded antistatic wrist strap while handling these circuit boards. Do service of static-sensitive circuit boards only at a static-free work station.
4. Nothing capable of generating or holding a static charge should be allowed on the work station surface.

5. Handle circuit boards by the edges when possible.
6. Do not slide the circuit boards over any surface.
7. Avoid handling circuit boards in areas that have a floor or work-surface covering capable of generating a static charge.

WARNING. *To avoid electric shock, always power off the chassis and disconnect the power cord before cleaning or servicing the chassis.*

Inspection and Cleaning

The pattern generator is inspected mechanically and electrically before shipment. It should be free of marks or scratches and should meet or exceed all electrical specifications. To confirm this, inspect the chassis for physical damage incurred during transit. Retain the chassis packaging in case shipment for repair is necessary. If there is damage or deficiency, contact your local Tektronix representative.

Cleaning procedures consist of exterior and interior cleaning of the chassis. Clean the chassis as needed, based on the operating environment.

Interior Cleaning

Use a dry, low-velocity stream of air to clean the interior of the chassis. Use a soft-bristle, nonstatic brush for cleaning around components. If you must use a liquid for minor interior cleaning, use a 75% isopropyl alcohol solution and rinse with deionized water.

Exterior Cleaning

Clean the exterior surfaces of the chassis with a dry, lint-free cloth or a soft-bristle brush. If any dirt remains, use a cloth or swab dipped in a 75% isopropyl alcohol solution. Use a swab to clean narrow spaces around controls and connectors. Do not use abrasive compounds on any part of the chassis.

CAUTION. *To avoid damage do not allow moisture inside the chassis during exterior cleaning; use just enough moisture to dampen the cloth or swab.*

Do not wash the front-panel On/Standby switch. Cover the switch while washing the chassis.

Use only deionized or distilled water when cleaning. Use a 75% isopropyl alcohol solution as a cleanser and rinse with deionized or distilled water.

Do not use chemical cleaning agents; they may damage the chassis. Avoid using benzene, toluene, xylene, acetone, or similar solvents.

Removal and Installation Procedures

This section contains procedures for removal and installation of field replaceable parts.

Preparation

WARNING. *To prevent injury, read the Safety Summary found at the beginning of this manual before doing this or any other procedure in this manual, Also, to prevent possible injury to service personnel or damage to this instrument's components, read the* Installation *section and* Preventing ESD *in this section.*

This subsection contains the following items:

- This preparatory information that you need to properly do the procedures that follow.
- A list of tools that are required to remove and disassemble all modules.
- Procedures for removal and reinstallation of the electrical and mechanical modules.
- A disassembly procedure for removal of all the major modules from the instrument at one time and for reassembly of those modules into the instrument. Instructions for cleaning are found under *Maintenance* in the previous section.

WARNING. *To prevent serious injury or death, disconnect the power cord from the line voltage source before doing any procedure in this subsection.*

General Instructions

STOP. READ THESE GENERAL INSTRUCTIONS BEFORE REMOVING A MODULE.

Read Equipment Required *for a list of the tools needed to remove and install modules in this instrument.*

Read the cleaning procedure before disassembling the instrument for cleaning.

Equipment Required. Most module parts can be removed with a driver using a Phillips #0 or a #1 tip. Use this tool with the appropriate tip whenever a procedure step instructs you to remove or install a screw. Use a $^{7}/_{32}$ inch nut driver to remove the circuit board standoffs.

Table 6-1: Tools required for part removal

Item No.	Name	Description
1	Driver with a #0 tip and a #1 tip	Screwdriver for removing small phillips screws
2	Nutdriver, $^{7}/_{32}$ inch	Standard tool
3	Nutdriver, $^{1}/_{2}$ inch	Standard tool
4	Solder Iron	Standard tool
5	Small flat-blade screwdriver	Standard tool

Removal Procedures for the Pattern Generator

Right Cover

Follow the steps below to remove the right cover:

1. Remove the eight Phillips-drive screws and the one pan-head screw and washer that secures the right cover.
2. Lift the cover off of the chassis. See Figure 6–1

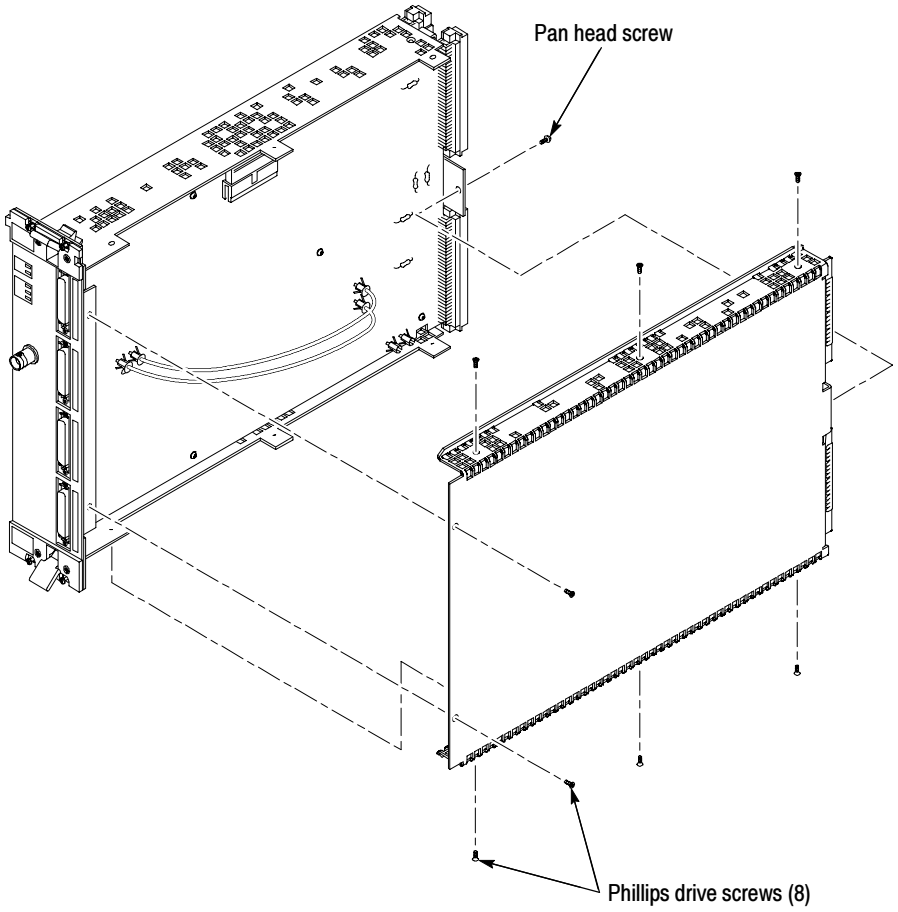


Figure 6-1: Right cover

A50 PG Board

Follow the steps below to remove the A50 PG board:

1. Remove the five screws securing the A50 PG board. See Figure 6–2
2. Use a driver with a #0 Phillips tip to remove the eight screws securing the board mounted connectors to the front panel.

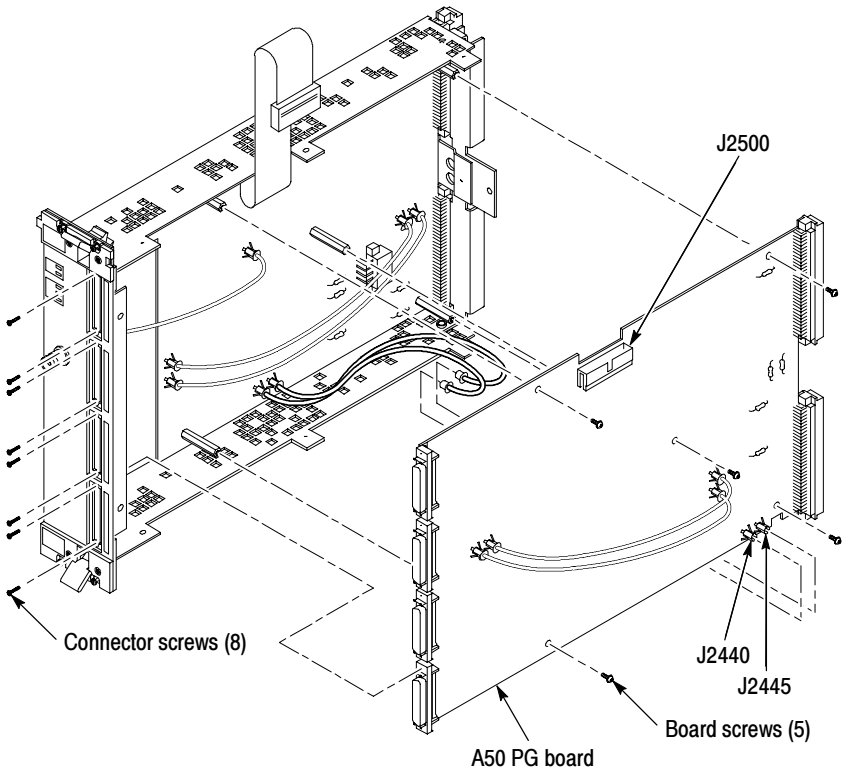


Figure 6- 2: A50 PG board

3. Carefully lift the A50 PG board to allow access to the cable connections.
4. Disconnect the cables from the following connections:
   - J2440
   - J2445
   - J2500

   See Figure 6–2 for cable locations.
   - J1960 cable housing on the A20 Clock and VXI board (Push the cable housing tab to release the cable latch.) See Figure 6–3.
5. Lift the A50 PG board out of the chassis.

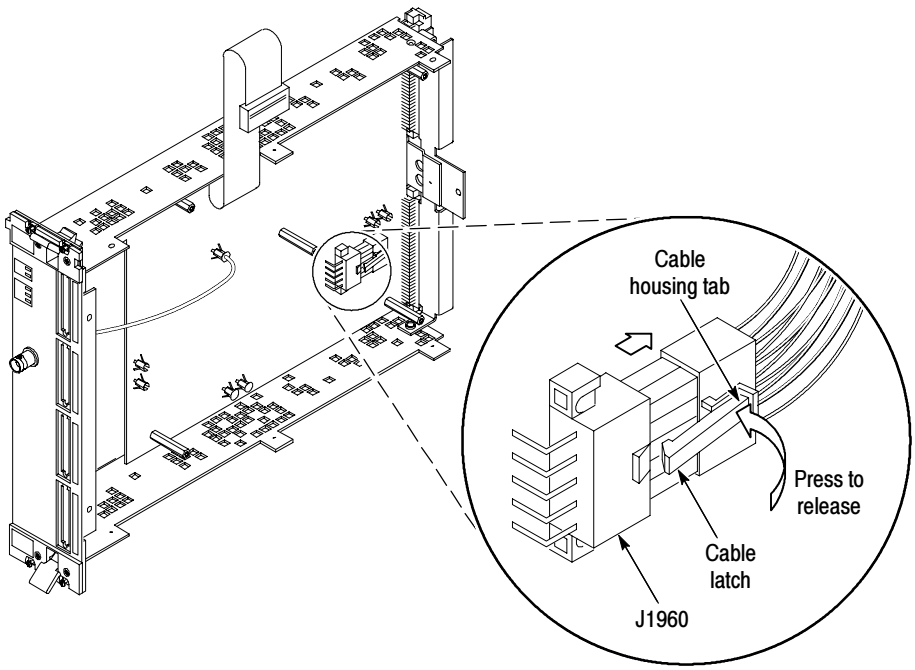


Figure 6-3: J1960 cable housing latch

A20 Clock and VXI I/F Board

Follow the steps below to remove the A20 Clock and VXI board:

1. Disconnect the cable from J200, located on the A20 Clock and VXI board.
2. Use a $^{7}/_{32}$ inch nut driver to remove the five spacer posts securing the A20 board to the chassis.
3. Remove the screw in the upper left section of the A20 board.
4. Remove the three screws securing the Rear End Cap to the chassis.
5. Carefully lift the A20 board out of the chassis.

Fuses

Follow the steps below to remove one or more fuses from the A20 or A50 board. See Figure 6–4.

1. Carefully unsolder the fuse that needs to be replaced.
2. Solder the new fuse into the board.
3. Clip the fuse leads on the backside of the A20 if necessary.

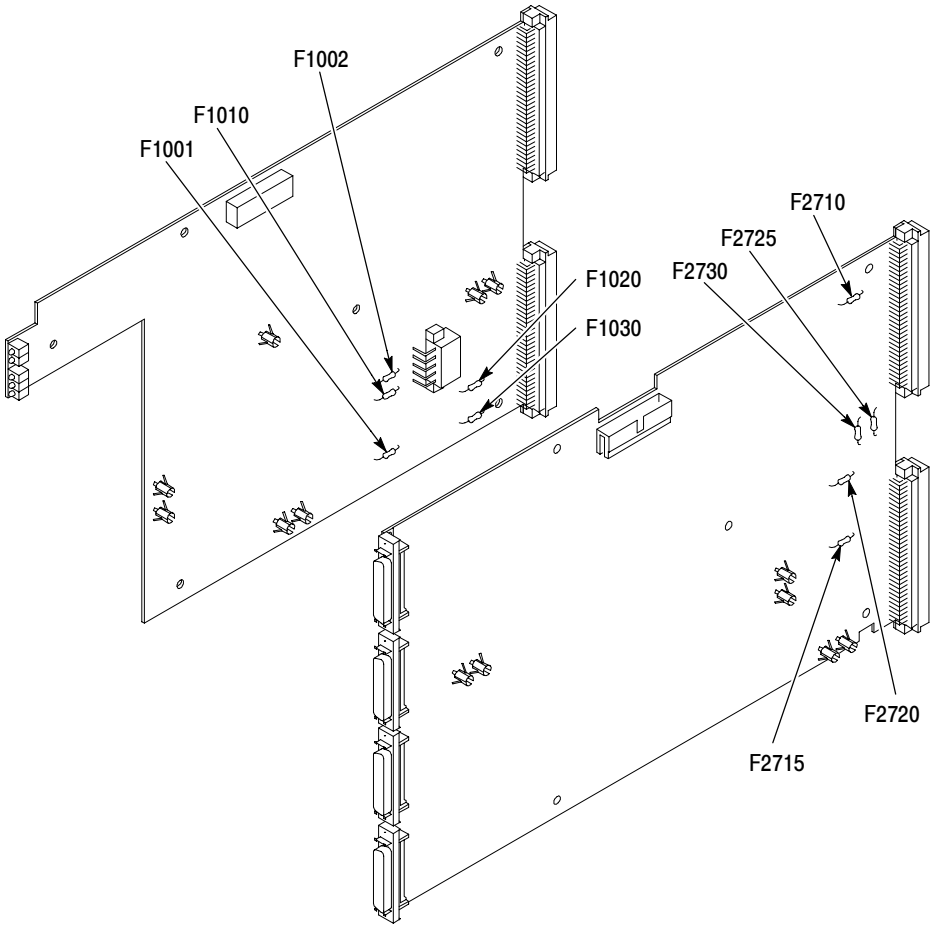


Figure 6- 4: A20 and A50 fuse locations

BNC Connector

Follow the steps below to remove the BNC connector from the front panel:

1. Use a $^1/_2$ inch nut driver to remove the nut from the BNC connector.
2. Remove the BNC connector from the front panel.

Ejector Assemblies

Follow the steps below to remove the ejector assemblies:

***NOTE**. The top and bottom ejector assemblies have different part numbers.*

1. Remove the two screws that secure the ejector assembly.
2. Remove the ejector assembly by tipping the ejector away from the chassis.

See Figure 6–5.

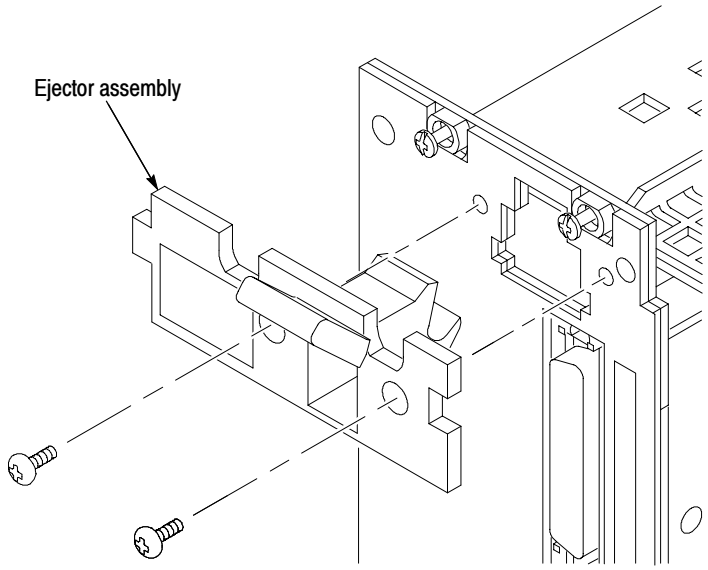


Figure 6-5: Ejector assembly

Cushioning Pad

The pad is used for heat dissipation and cushioning between the side cover and A50 board components. Peel off the self-adhesive backing and affix the pads as shown in Figure 6–6.

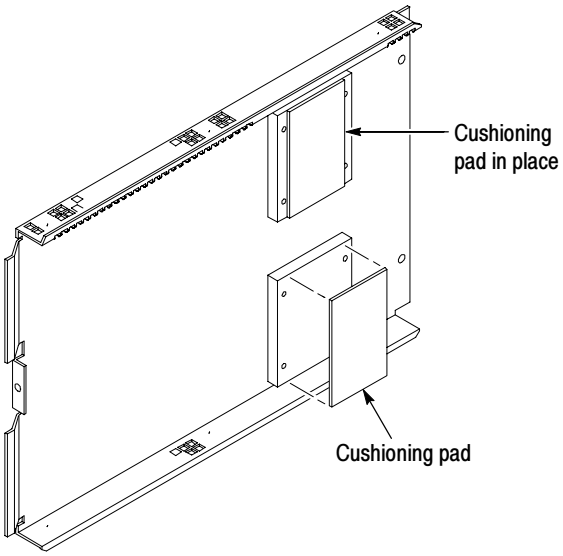


Figure 6- 6: Cushioning pad

Installation Procedures for Pattern Generator

Do the *Removal Procedures for the Pattern Generator* in reverse order.

Removal Procedures for Standard Probes

The following procedures provide instructions for removing and replacing standard probe parts.

Removing the Standard Probe Cover

Follow the steps below to remove the probe cover. See Figure 6–7.

1. Remove the four screws securing the probe cover.
2. Release the cover latches by pushing the tip of a small flat-blade screwdriver into the cutouts on each side of the probe. Do not pry.
3. Remove the top cover.

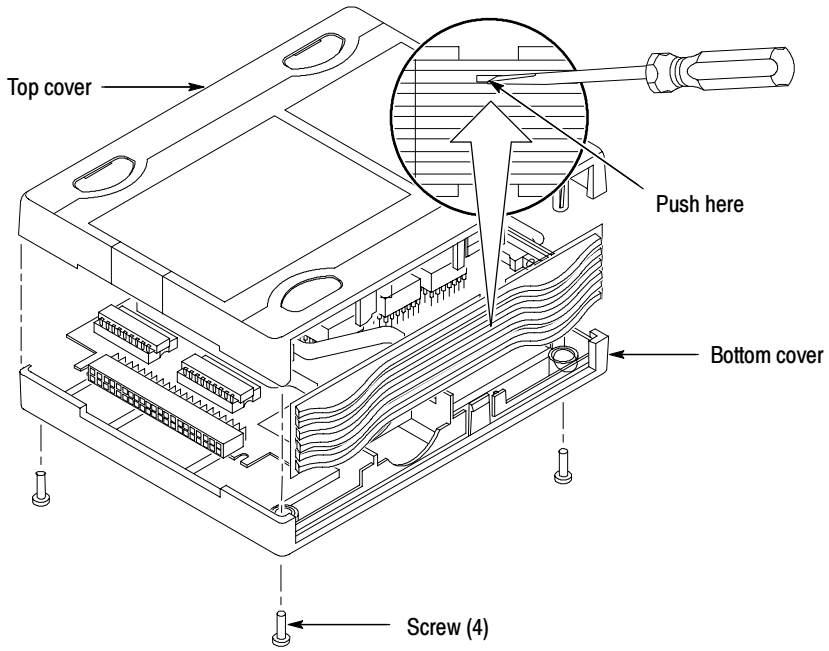


Figure 6-7: Removing the standard probe cover

Changing the Series Termination Resistors (P6470 and P6474 only)

Table 6–2 lists the various resistor packs available for the P6470 and P6474 probes (see Figure 6–8 for the P6470 and Figure 6–9 for the P6474). These resistor packs are a subpart of the 015-A095-00 kit.

Table 6-2: P6470 series termination resistors

Part number	Value
307-1683-00	43 Ω
307-1684-00	75 Ω
307-1686-00	100 Ω
307-1687-00	150 Ω

***NOTE**. Be careful not to bend the resistor pack pins when installing the replacement resistors in sockets.*

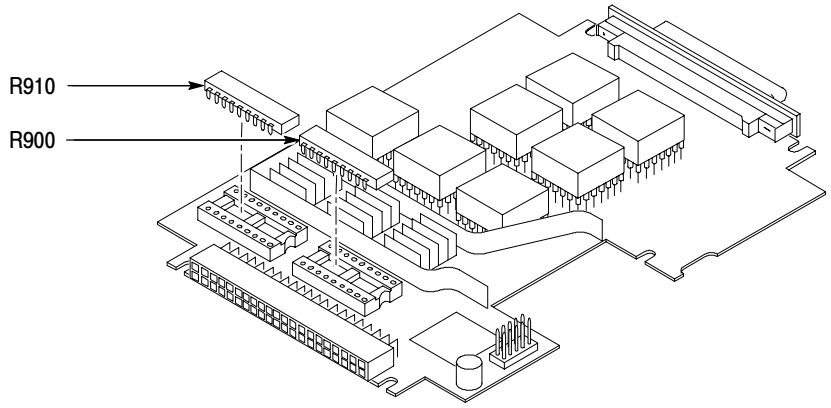


Figure 6-8: P6470 series termination resistors

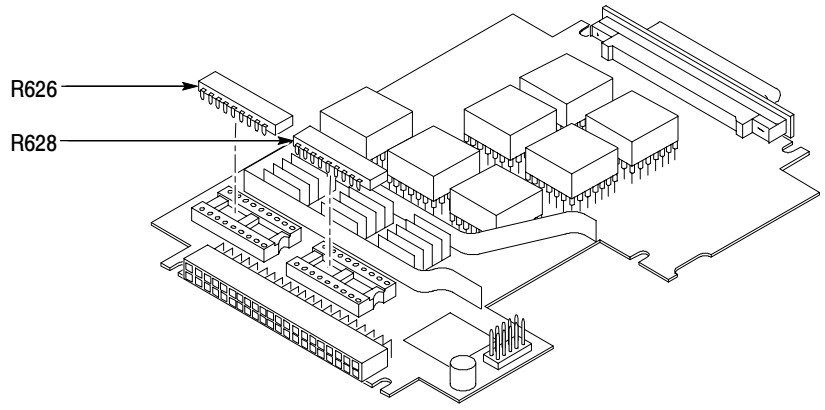


Figure 6-9: P6474 series termination resistors

Configuring the P6472 for PECL or LVPECL

You can select the PECL or LVPECL circuit by moving the P300 jumper inside the probe to the J300 pin locations as shown in Figure 6–10.

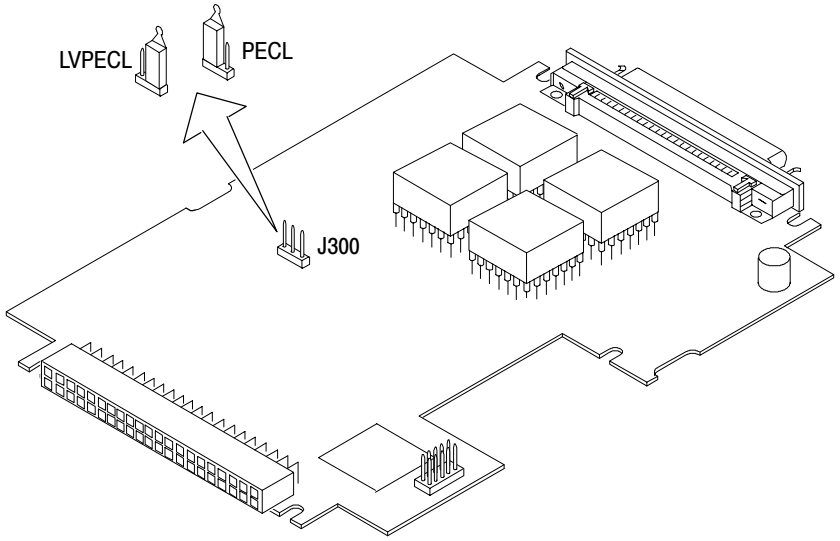


Figure 6-10: P6472 PECL and LVPECL jumper position

P6472, P6473, P6474, P6475 Fuse Replacement

The P6472, P6473, P6474, and P6475 have surface mount fuses that are not replaceable.

***NOTE**. Replacing surface mount fuses could cause damage to the circuit board. Contact your local Tektronix service center for replacement information.*

Table 6-3: P6472, P6473, P6474, and P6475 fuse descriptions

Probe	Qty	Description	Circuit location
P6472	4	FUSE, CARTRIDGE:1A, 125V, FAST, SMD, T/R	A83F110, A83F120, A83F130, A83F140
	1	FUSE, CARTRIDGE:2A, 125V, FAST, SMD, T/R	A83F100
P6473	4	FUSE, CARTRIDGE:1A, 125V, FAST, SMD, T/R	A82F110, A82F120, A82F130, A82F140
	1	FUSE, CARTRIDGE:2A, 125V, FAST, SMD, T/R	A82F100
P6474	4	FUSE, CARTRIDGE:1A, 125V, FAST, SMD, T/R	A81F110, A81F120, A81F130, A81F140
	1	FUSE, CARTRIDGE:2A, 125V, FAST, SMD, T/R	A81F100
P6475	3	FUSE, CARTRIDGE:1A, 125V, FAST, SMD, T/R	A80F1500, A80F1510, A80F1530
	1	FUSE, CARTRIDGE:2A, 125V, FAST, SMD, T/R	A80F1520

P6470 and P6471 Fuse Replacement

Figure 6–11 shows the fuse location for the P6470 and P6471 fuses. Refer to Table 6–4 for the fuse descriptions and the circuit locations.

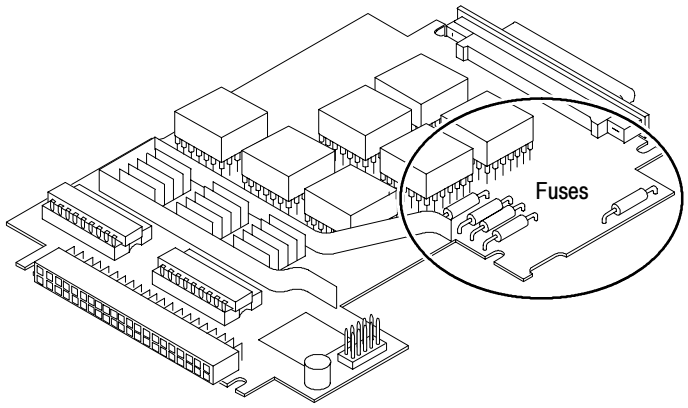


Figure 6-11: Fuse location for the P6470 and P6471

***NOTE**. Clip replacement fuse leads if needed.*

Table 6-4: P6470 and P6471 fuse descriptions

Probe	Tektronix part number	Qty	Description	Circuit location
P6470	159-0335-00	4	FUSE,WIRE LEAD:1A,125V,FAST BLOW,AXIAL LEADS	A95F380, A95F390, A95F392, A95F395
	159-A025-00	1	FUSE:WIRE-LEAD,AXI,2A,125V,FAST	A95F385
P6471	159-0335-00	3	FUSE,WIRE LEAD:1A,125V,FAST BLOW,AXIAL LEADS	A90F380, A90F392, A90F395
	159-A025-00	1	FUSE:WIRE-LEAD,AXI,2A,125V,FAST	A90F385

Removing the Standard Probe Fan

Follow the steps below to remove the fan (See Figure 6–12):

1. Disconnect the cable from J810.
2. Remove the fan from the probe.

Replace the fan by reversing this procedure.

***NOTE**. Position the fan so that the label is facing towards the circuit board.*

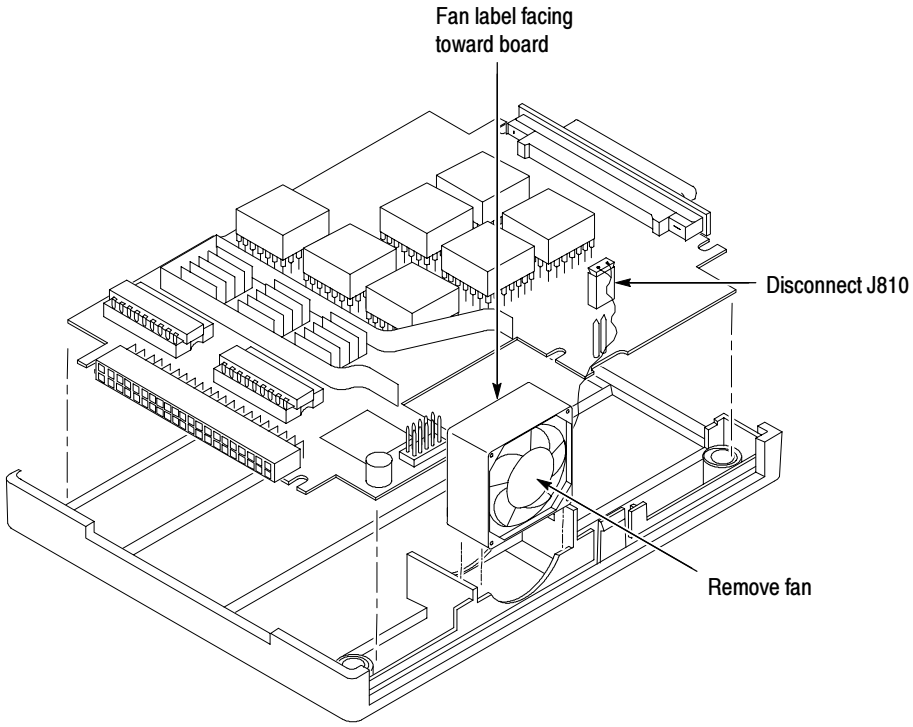


Figure 6-12: Removing the standard probe fan

Removal Procedures for P6475 Variable Probe

The following procedures provide instructions for removing and replacing P6475 probe parts.

Removing the P6475 Cover

Follow the steps below to remove the P6475 cover. See Figure 6–13.

1. Remove the 4 screws securing the probe cover.
2. Lift the probe cover off of the probe chassis.

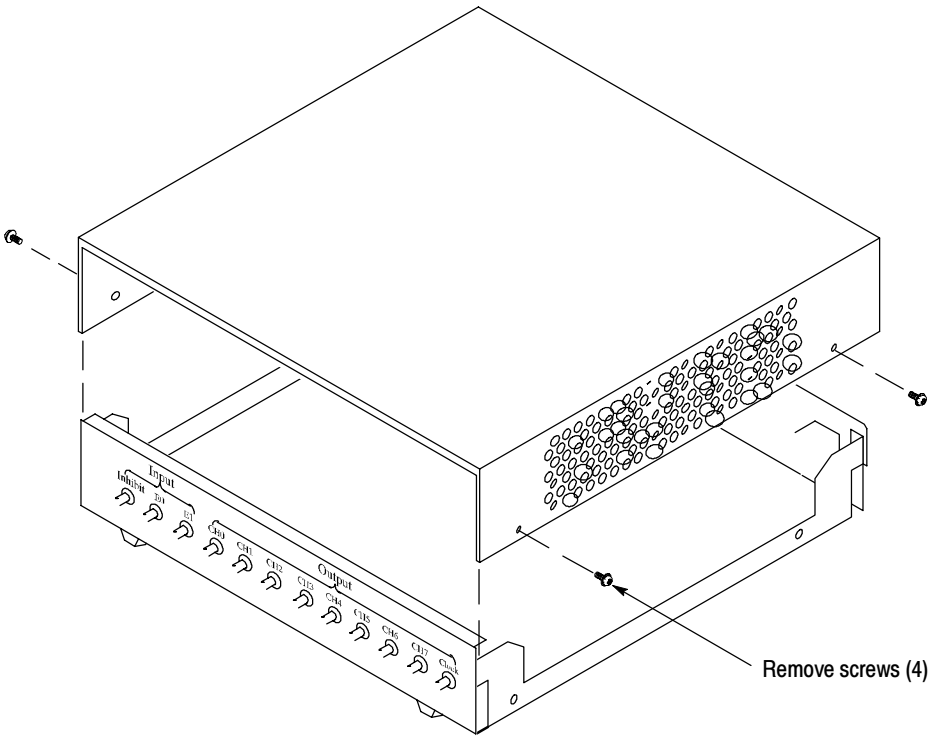


Figure 6-13: Removing the P6475 cover

Removing the P6475 Fan

Follow the steps below to remove and replace the P6475 fan (See Figure 6–14):

1. Disconnect the fan cable (J1510 or J1520).
2. Remove the 4 screws securing the fan that you are replacing.
3. Remove the fan from the probe chassis.

Replace the fan by reversing this procedure. Be sure the fan is reinstalled so that the airflow is directed inside of the chassis.

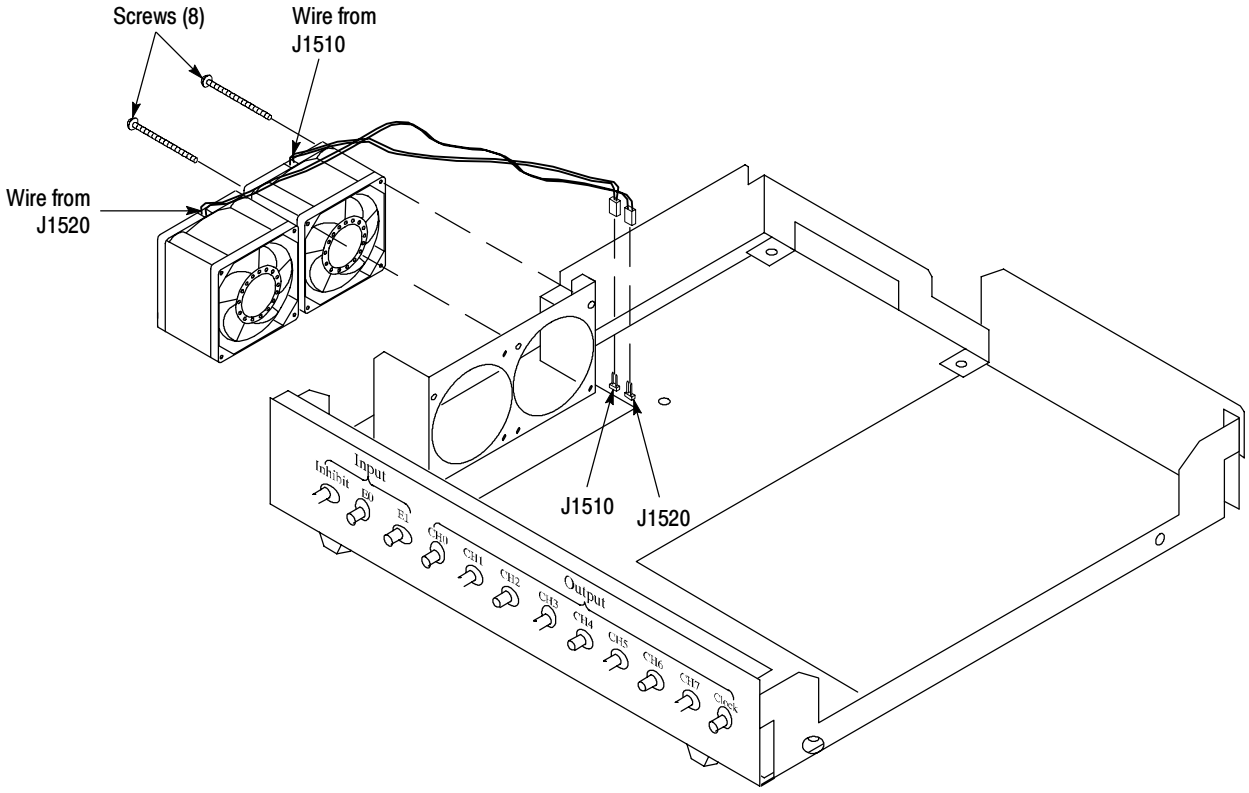


Figure 6- 14: Removing the P6475 fans

Removing the P6475 Power Supply

Follow the steps below to remove the P6475 power supply:

1. Disconnect the power switch cables from CN1 and CN2 locations on the power supply board. See Figure 6–15.
2. Remove the 2 phillips screws that are securing the board. See Figure 6–16.
3. Remove the board by lifting the board up and towards the front of the chassis.

Replace the board by reversing this procedures.

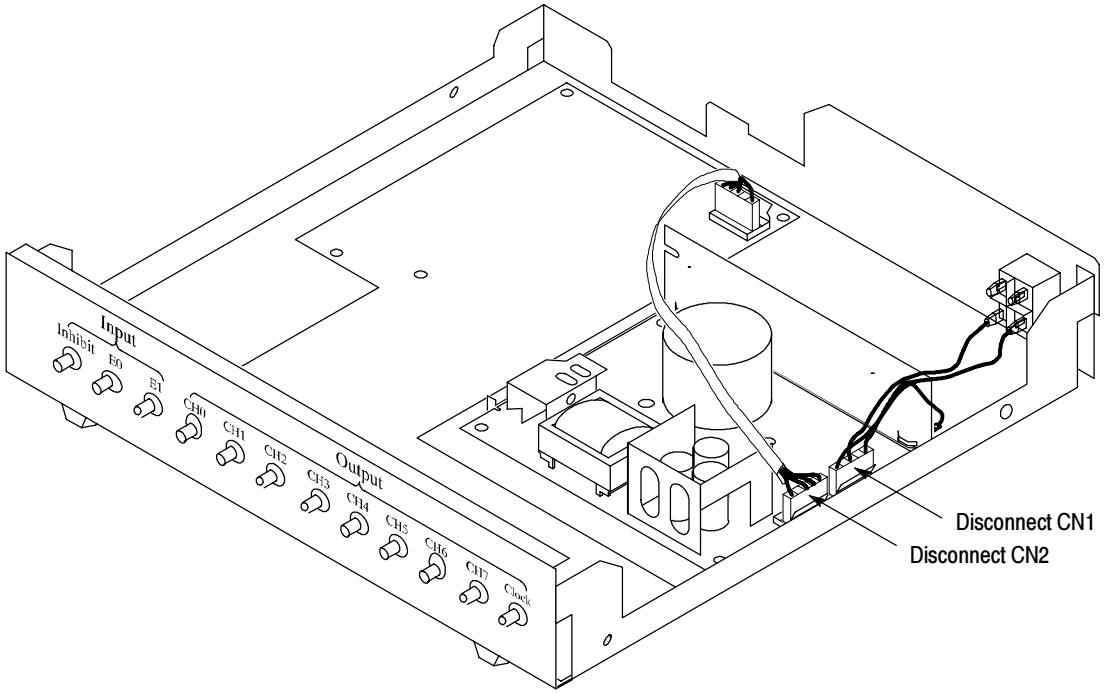


Figure 6-15: Disconnect power supply cables

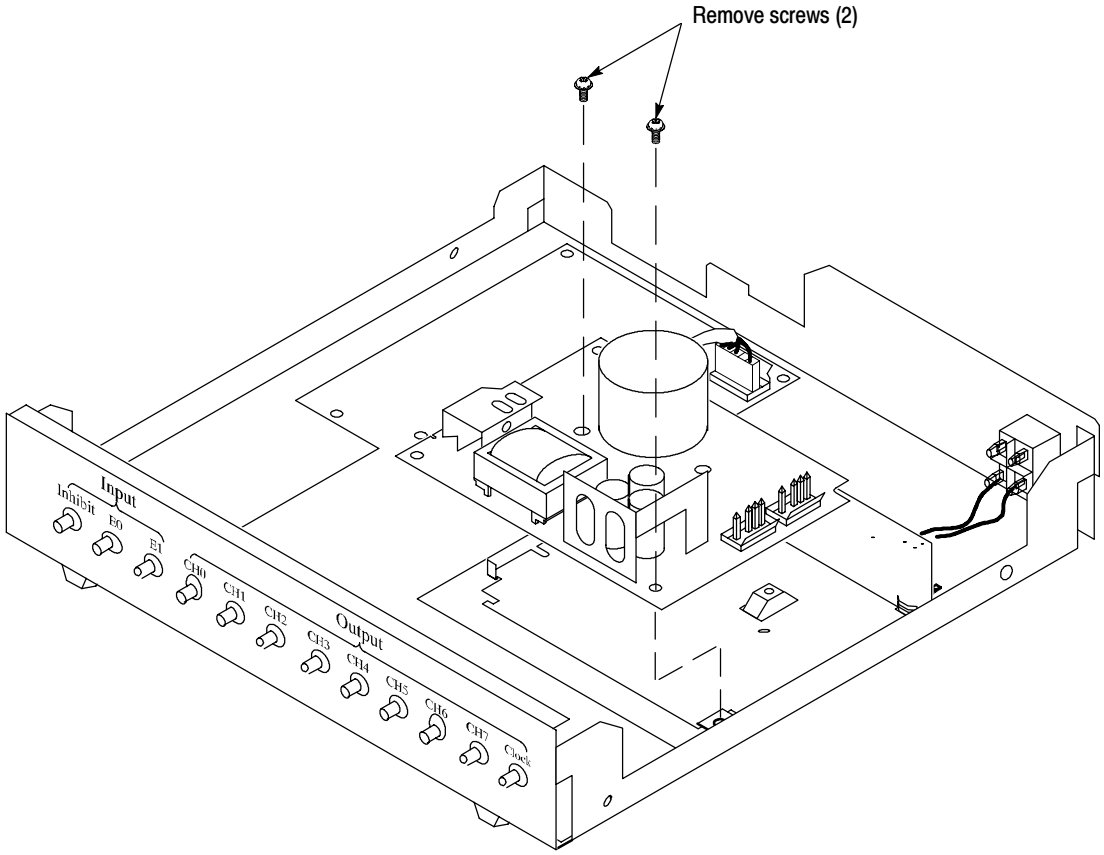


Figure 6- 16: Remove the power supply board

Troubleshooting

This section contains information and procedures designed to isolate faulty modules in the TLA7PG2 Pattern Generator. If these procedures indicate that a module needs to be replaced, follow the *Removal and Installation Procedures* in the preceding section.

LEDs

The TLA7PG2 has five front-panel LEDs that indicate whether a particular function of the pattern generator is in operation. The following table provides a description of each function:

Table 6-5: LEDs

Function	Description
Ready LED (green)	The Ready LED illuminates when the module is ready for operation.
Accessed LED (amber)	The Accessed LED will briefly illuminate each time communication to the Tektronix pattern generator module occurs.
Output LED (amber)	The Output LED will illuminate while the probe is asserting high or low level at the output pins. It will not illuminate while the output pins are high impedance when the HI-Z on Stop function is active. The P6471 ECL probe does not support Hi-Z on Stop so the LED will always be illuminated if that probe is used.
Started LED (green)	The Started LED will illuminate while the pattern generator is running or waiting for an event.
Waiting LED (green)	The Waiting LED will illuminate while the pattern generator is waiting for an event.

Troubleshooting Procedures

The troubleshooting procedure in this subsection consists of the flowchart in Figure 6–17.

Use this procedure to check the various functions, and then follow the recommendations indicated in the chart.

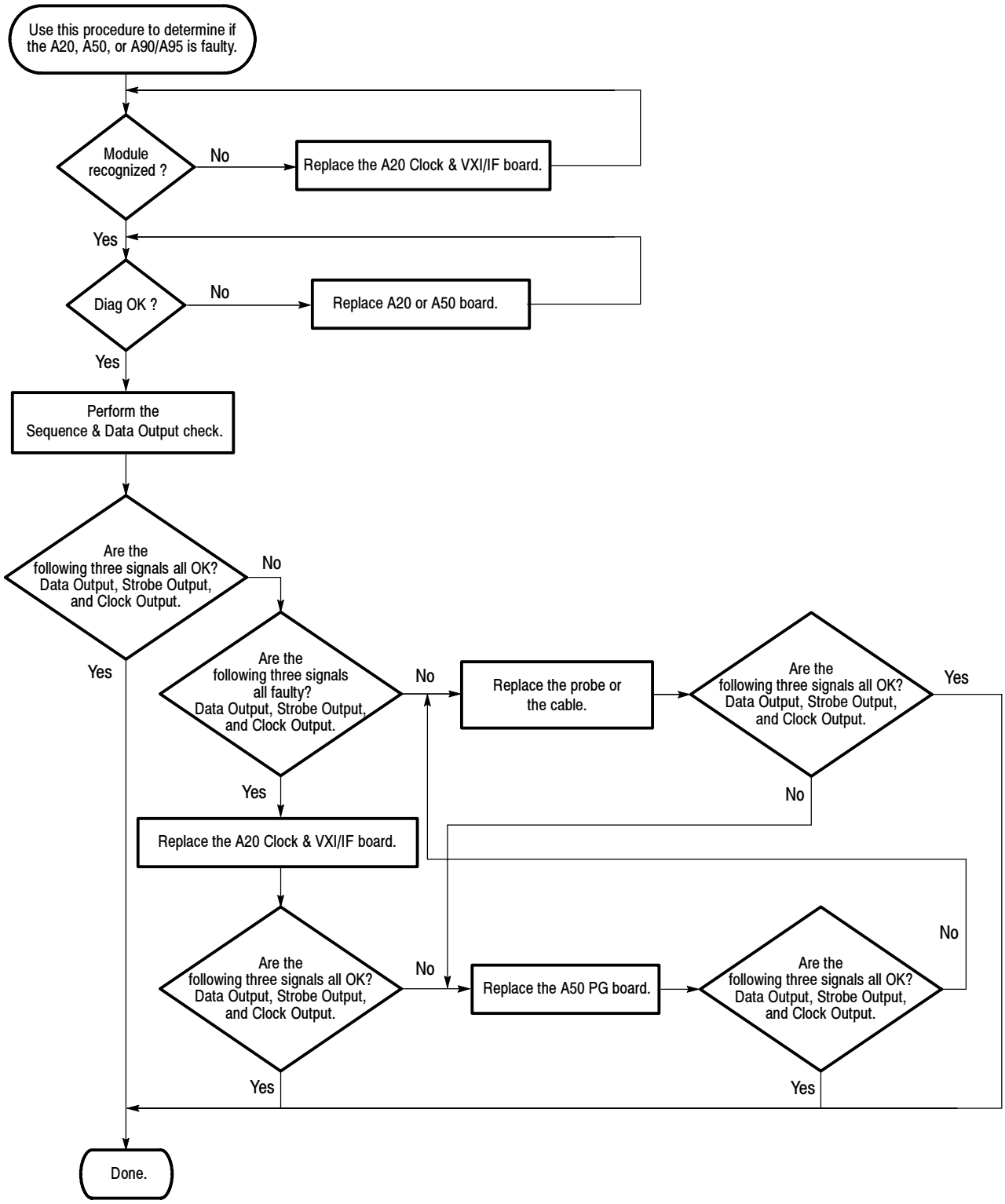


Figure 6-17: Troubleshooting procedure

Diagnostics

The pattern generator has internal diagnostics that verify circuit functionality.

The power-on diagnostics only run at power on so there are no controls to execute them. The extended diagnostics test provides a more thorough test than the power-on diagnostics.

Disconnect any attached probes prior to running the extended diagnostics.

For more information on diagnostics, see the *Operating Instructions* section of this manual.

***NOTE**. Some items in the pattern generator extended diagnostics menu will fail if a logic analyzer or DSO is running. Stop all LA and DSO modules before performing the extended pattern generator diagnostics.*

Restoring and Reinstalling Software

This section describes procedures for restoring or reinstalling your pattern generator software or firmware.

Restoring Software

This section provides information for restoring software in your pattern generator. In addition to the pattern generator software, there are other software programs that are installed separately. Table 6–6 lists some of the software and installation information. Note that the version of the Microsoft Windows operating system depends on the systems software version installed on the mainframe. Version 4.0 and above come with Microsoft Windows 2000 Professional while Version 3.2 and below come with Microsoft Windows 98.

Refer to your *Tektronix Logic Analyzer Family User Manual* for detailed software installation procedures or the The *TLA7UP Upgrade Instructions* for upgrading the system software.

Table 6-6: Restoring software

Software	Installation information
Microsoft Windows OS[1]	Refer to the Microsoft Windows documentation or contact your local Microsoft representative.
Other Software	Refer to the instructions that come with your software.

[1] **For information on installing Microsoft Windows software not available on the Windows backup floppy disks, refer to the MS Web Site at: www.microsoft.com**

Reinstalling Pattern Generator Application Software

You can reinstall the pattern generator software by performing the following steps.

***NOTE**. The following instructions assume that you are reinstalling the Pattern Generator application software only.*

1. If the Pattern Generator application is running, exit the application before continuing.

***CAUTION.** Do not install the software from the TLA700 Hard Disk Image CD. Using this CD will erase the entire contents of your hard disk drive.*

2. Insert the Disk 1 *(Logic Analyzer Software)* in the CD ROM drive.
3. Click **Start → Settings → Control Panel**.
4. In the Control Panel window, double-click **Add/Remove Programs**.

***NOTE**. Depending on the Windows operating system, the Add/Remove Programs dialog may vary.*

5. Locate the software and follow the instructions on the screen for installing the application software.

   The application software is located on the CD in the following directory:

   \Pattern Generator Application SW\Disk1

When executed, the setup program will replace old versions of the software after you have confirmed your choice. The program also offers to delete shared files which appear to be no longer needed by any application. The program will not remove saved PG files.

Uninstalling Pattern Generator Application Software

You can remove the Pattern Generator (PG) software using the Uninstall program. Use the Add/Remove Programs tool under the Control Panel to uninstall software.

Updating Module Firmware

Perform the following steps if you need to reinstall or update the flash ROM-based firmware on your modules. You can update multiple modules and module types during a single firmware update session.

1. Turn off the instrument.
2. Disconnect the power cord.
3. Disconnect any probes on the modules that you want to upgrade.
4. Remove the module from the mainframe.
5. Refer to Figure 6–18 and locate the flash programming pins on the rear of the module.

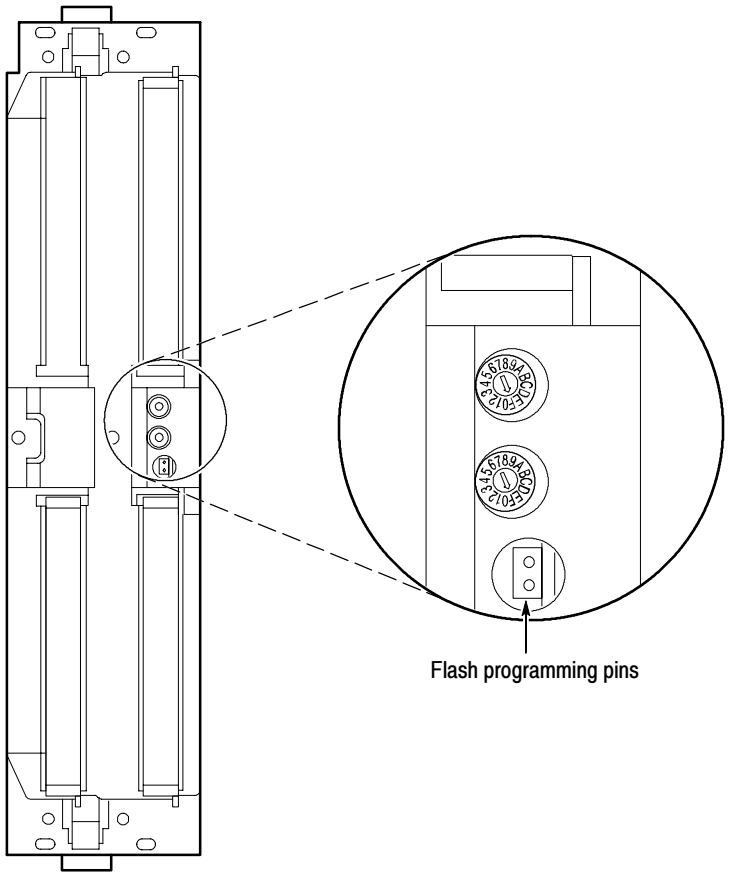


Figure 6-18: Flash programming pins

6. Install a jumper on the flash programming pins (use one of the spare jumpers that came with your logic analyzer software).
7. Reinstall the module(s) in the mainframe.
8. Reconnect the power cord and turn on the mainframe.

***NOTE**. Any modules with the flash programming jumper installed will not display in the System window.*

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9. Exit the pattern generator or logic analyzer application.
10. Click **Start → Programs → Tektronix Logic Analyzer**, and click **TLA Firmware Loader**.
11. Select the modules that you want to update from the list of modules displayed in the Supported list box near the top of the menu. If you are updating more than one module at a time, note the slot location of the module in the selection box.
12. Select Load Firmware from the Execute menu.
13. Click the proper .LOD file for the PG module in the C:\Program Files\ Tektronix Pattern Generator\ Firmware directory. If you are updating more than one module, make sure that you select the proper firmware file for the module in the listed slot number.
14. Click OK. You will be asked to confirm your action; click Yes when prompted.

***NOTE**. The program will not allow you to load firmware to an incompatible module. For example, the program will not load DSO firmware to a pattern generator module.*

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15. If you are updating another module, select the proper .LOD file for the module.
16. Click OK. You will be asked to confirm your action; click Yes when prompted.

    The program will load the firmware for each module one at a time. The process takes approximately five minutes per module.
17. When the load operation is complete, select each of the modules in the Supported list and then select Checksum from the Execute menu.
18. If each module passes the checksum test, exit the program.

19. Turn off the mainframe and disconnect the power cord.

20. Remove the module from the mainframe and remove the jumper from the Flash programming pins on the rear of the module. Keep the jumper for future updates.

21. Attach a new label with the new firmware version to the module.

22. Reinstall the module in the mainframe and reconnect the probes.

23. Reconnect the power cord and turn on the mainframe.

24. Verify that the power-on diagnostics pass.

Repackaging

This subsection contains information about repackaging the TLA7PG2 Pattern Generator for shipment.

Repackaging Instructions

Use a corrugated cardboard shipping carton having a test strength of at least 275 pounds and with an inside dimension at least six inches greater than the pattern generator dimensions. (If available, use the original shipping carton, which meets these requirements.)

If the TLA7PG2 is shipped to a Tektronix Service Center, enclose the following information:

- The owner's name
- The name and phone number of a contact person
- The type and serial number of the TLA7PG2 Pattern Generator
- Reason for returning
- A complete description of the service required

Seal the shipping carton with an industrial stapler or strapping tape.

Mark the address of the Tektronix Service Center and your own return address on the shipping carton in two prominent locations.

Options and Accessories

This section describes the various options as well as the standard and optional accessories that are available for the TLA7PG2 Pattern Generator module.

Pattern Generator Options

The following options are available for the pattern generator:

- Option R3 — Repair warranty; extended to cover 3 years
- Option C3 — 3 Year calibration services (functional only)
- Option IN — Add on-site installation service (excludes network integration)
- TLA7F70 — TLA 7PG2 module powerflex kit
- Opt 1M — Increases memory depth from 256/512 to 1M/2M
- Option 1F — Add return-to-Tektronix installation service

P6475 Options

The following options are available for the P6475

- TLAPG2 6P — 120 V US Standard Power Cord
- TLAPG2 7P — 220 V Euro Power Cord
- TLAPG2 8P — 240 V UK Power Cord
- TLAPG2 8P — 240 V Australian Power Cord
- TLAPG2 AP — 240 V North. American Power Cord
- TLAPG2 BP — 220 V Swiss Power Cord
- TLAPG2 CP — No Power Cord

Pattern Generator and Probe Optional Accessories

Table 7–1 lists the optional accessories that are recommended for use with the pattern generator.

Table 7-1: Optional accessories

Optional accessory	Tektronix part number
TLA7PG2 Pattern Generator and Probes Service Manual (this manual)	071-0714-XX
P6470, P6471, P6472, P6473, and P6474 probes only	
Option 1C, Grabber tips (bag of 42)	020-2336-00
Termination board (order quantity of 2)	067-A018-00
Tip, Probe Microckt test, 0.05 ctr.	206-0364-00
P6470 and P6474 probes only	
Series termination resistor kit	015-A095-00
P6475 used with a P6470, P6473, or P6474	
Time Alignment cable, 3.3 m (10,83 ft)	012-A224-00

Pattern Generator Standard Accessories

Table 7–2 standard accessories are provided with each pattern generator:

Table 7-2: Pattern generator standard accessories

Standard accessory	Tektronix part number
TLA 700 Application CD ROM	063-3487-XX
Tektronix Series Logic Analyzer Family User Manual	071-0863-XX
Probe cables (Quantity 4)	012-1570-00

Probe Options

There are no options are available for the probes.

Probe Standard Accessories

The following standard accessories are provided with each probe unless stated otherwise:

Table 7-3: Probe standard accessories

Standard accessory	Tektronix part number
TLA7PG2 Pattern Generator Probes Instruction Manual	071-1017-XX
Standard lead set kit: for P6470, P6471, P6472, P6473, and P6474 probes only. Probe lead sets 10-VON twisted pair (quantity 1) Probe lead sets; 16-VON twisted pair (quantity 2)	020-2338-00
SMB to Header coax cable set for P6475 probe only 50.8 cm (20 in)	012-1504-00
Power cable for P6475 probe only	Refer to Power Cord Options, Table

Replaceable Electrical Parts

The pattern generator and probes included in this service manual are a combination of mechanical and electrical subparts. All replaceable modules are listed in the *Replaceable Mechanical Parts* chapter. Refer to that chapter for part numbers when using this manual.

Diagrams

This section contains the following diagrams:

- Function block diagram for the TLA7PG2 Pattern Generator
- Function block diagram for P6470, P6471, P6472, P6473, and P6474 probes
- Function block diagram for the P6475 probe
- Cable diagram for the TLA7PG2 pattern generator
- Cable diagram for the P6475 probe

The block diagrams show the modules, probes, and the functional blocks. The cable diagram shows how the pattern generator, probes and mainframe connect together.

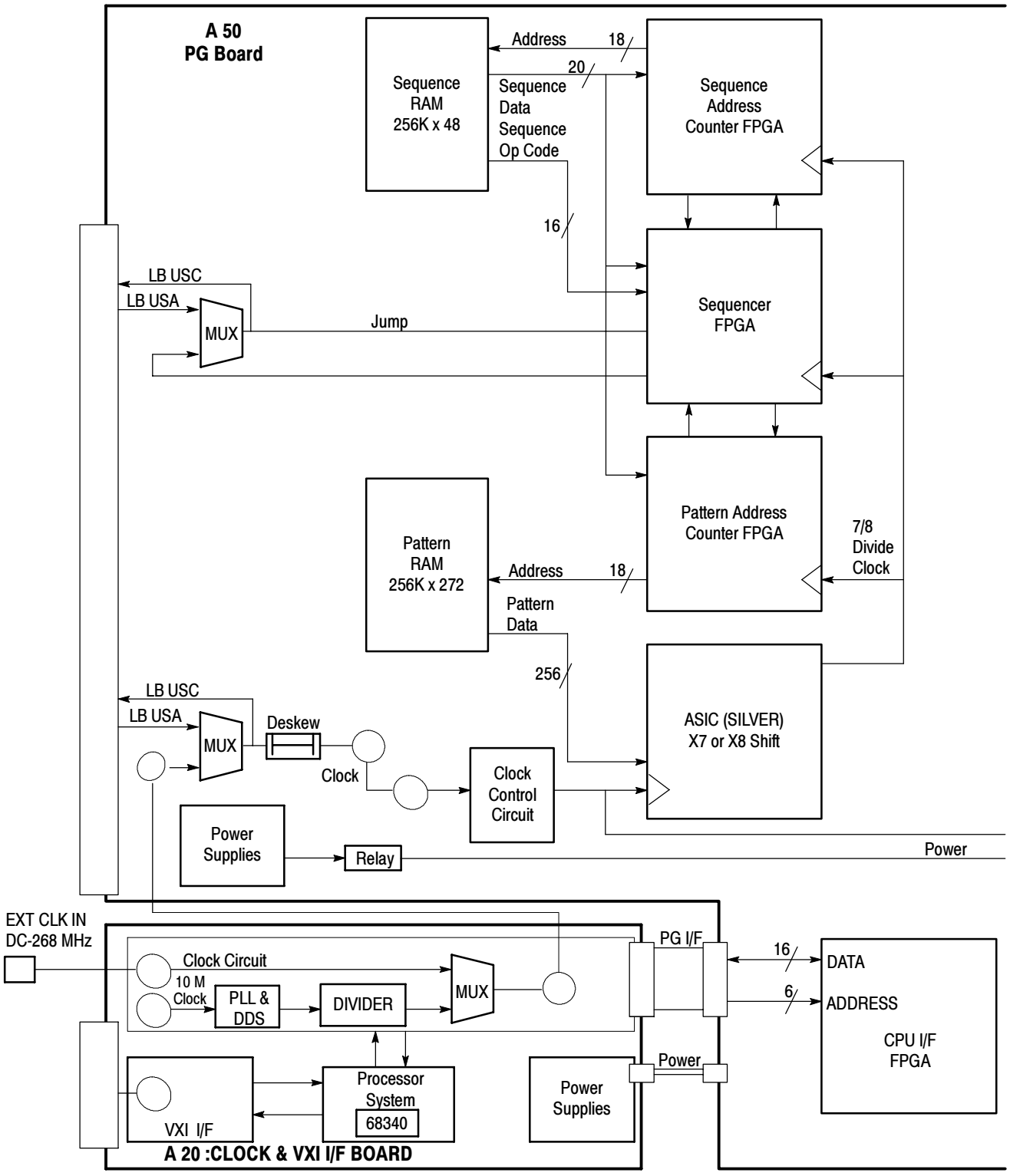

Figure 9- 1: Function block diagram for the TLA7PG2 Pattern Generator

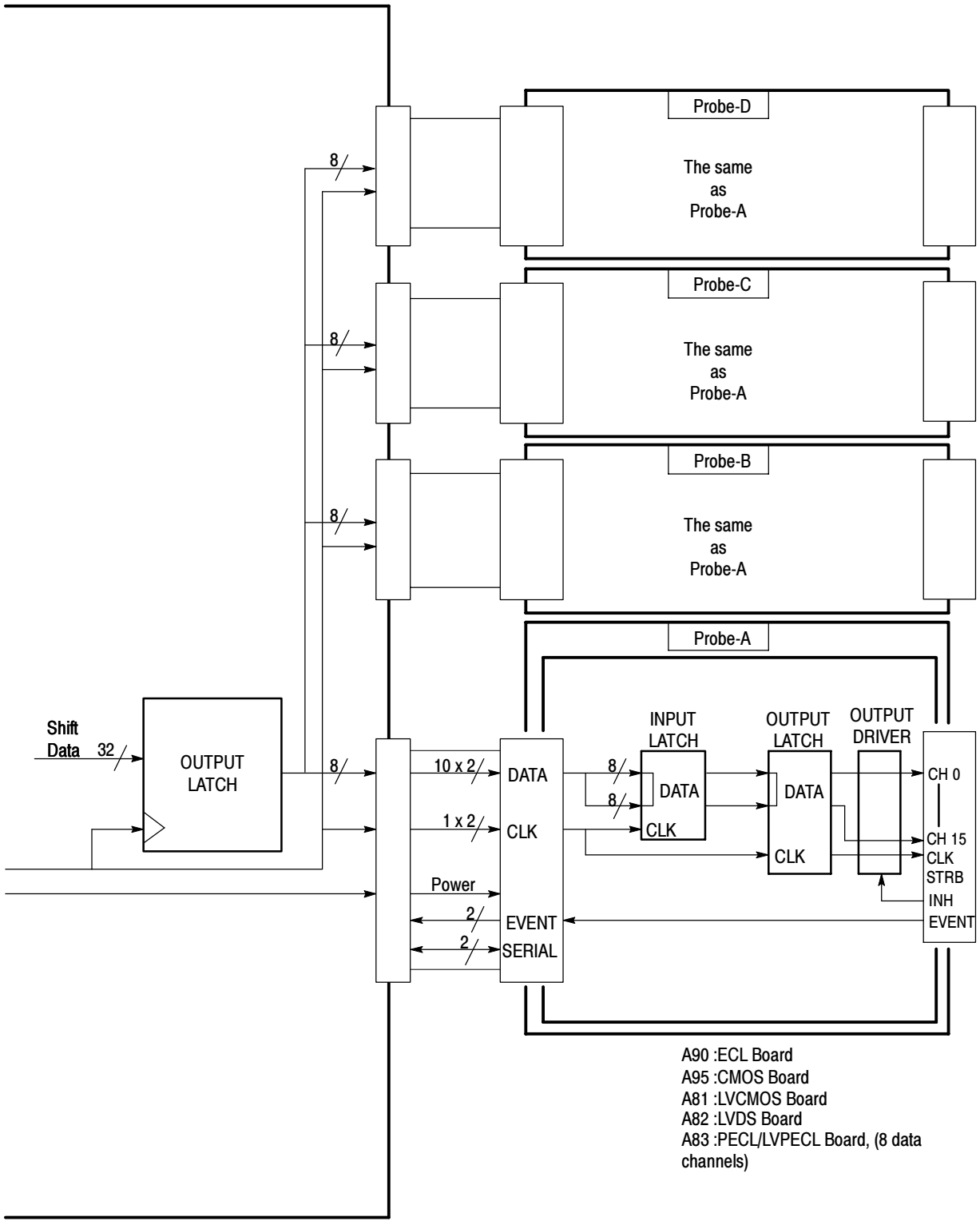

Figure 9-2: Function block diagram for P6470, P6471, P6472, P6473, and P6474 probes

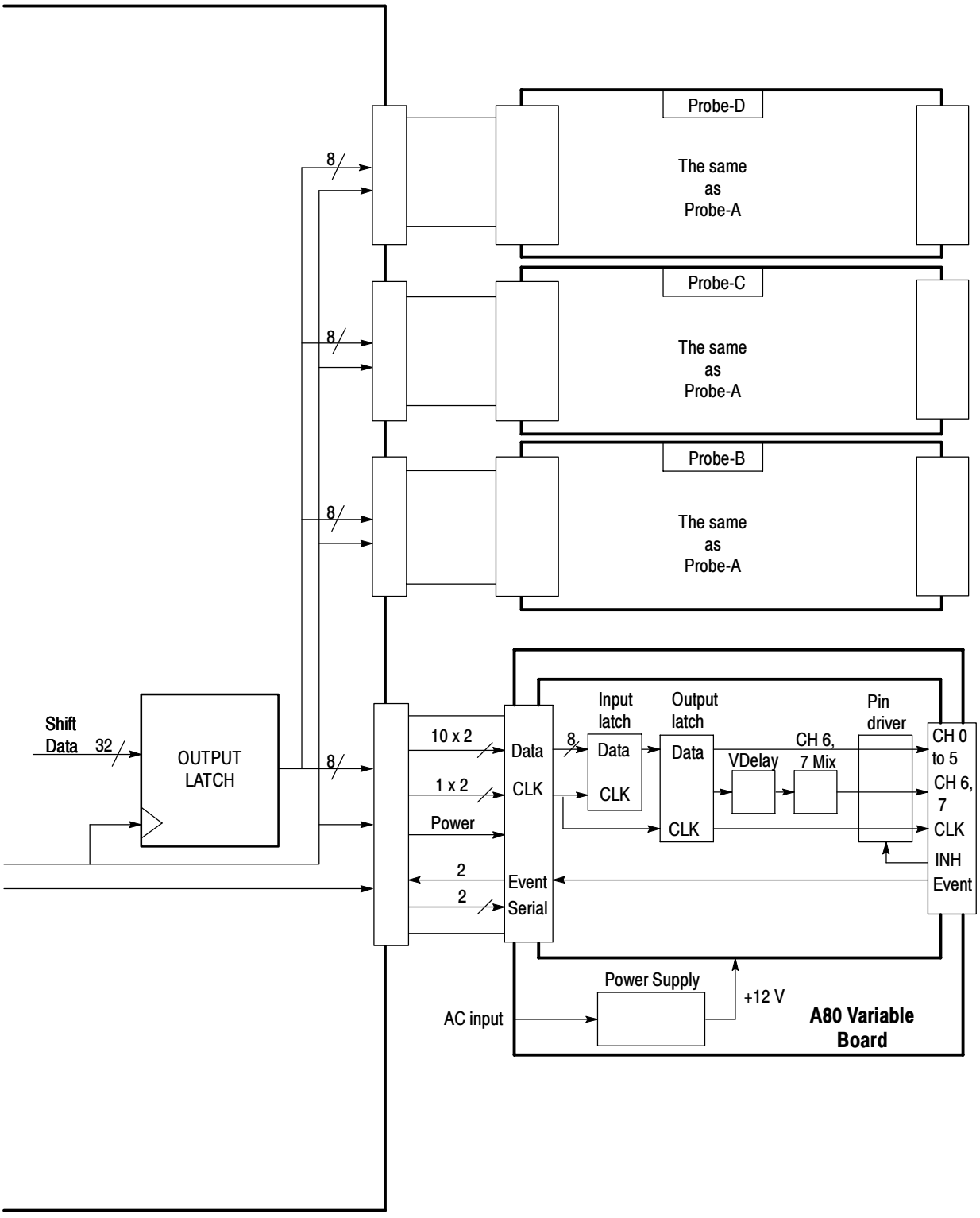

Figure 9- 3: Function block diagram for P6475 Probe

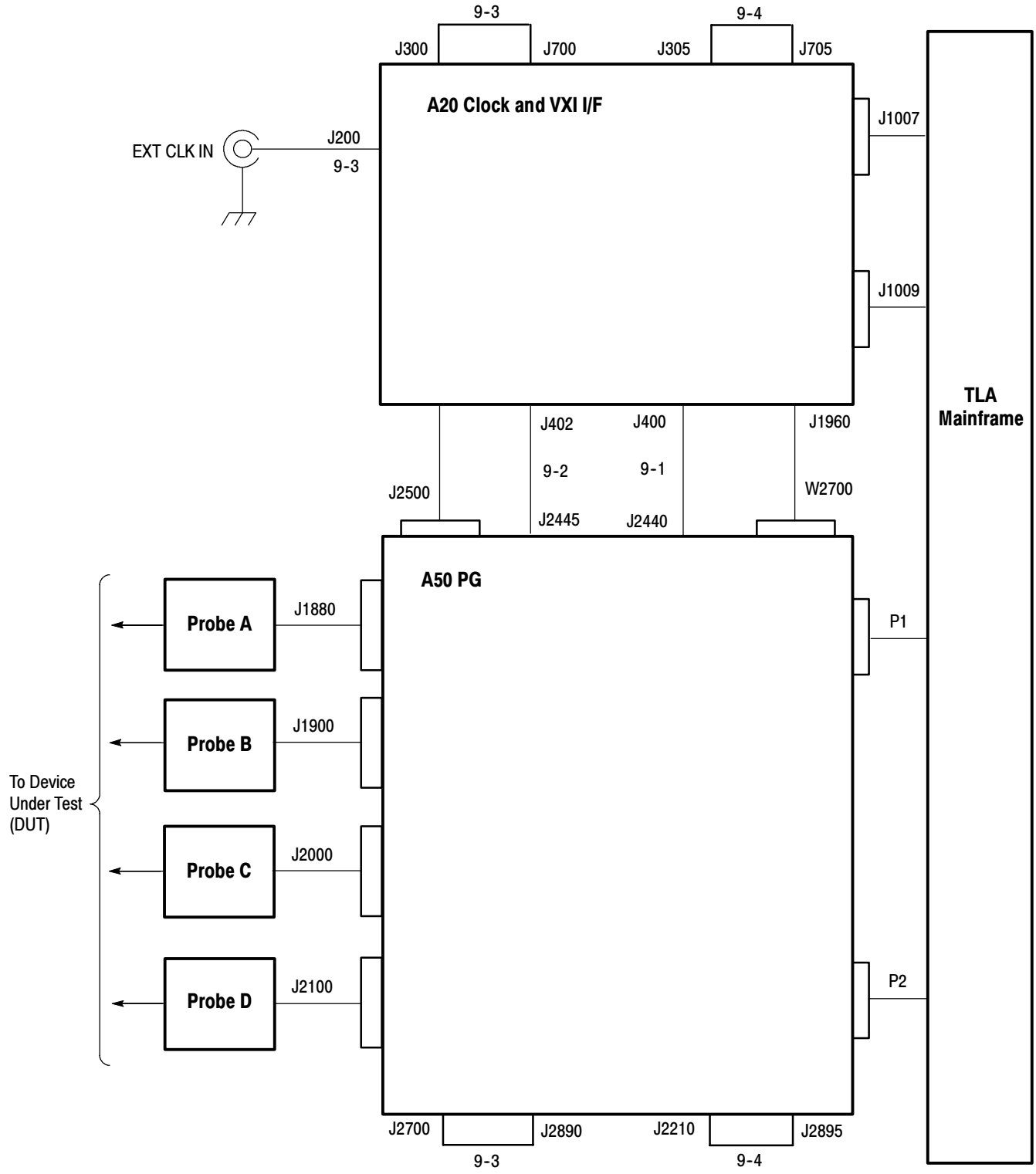

Figure 9-4: Cable diagram for the TLA7PG2 pattern generator

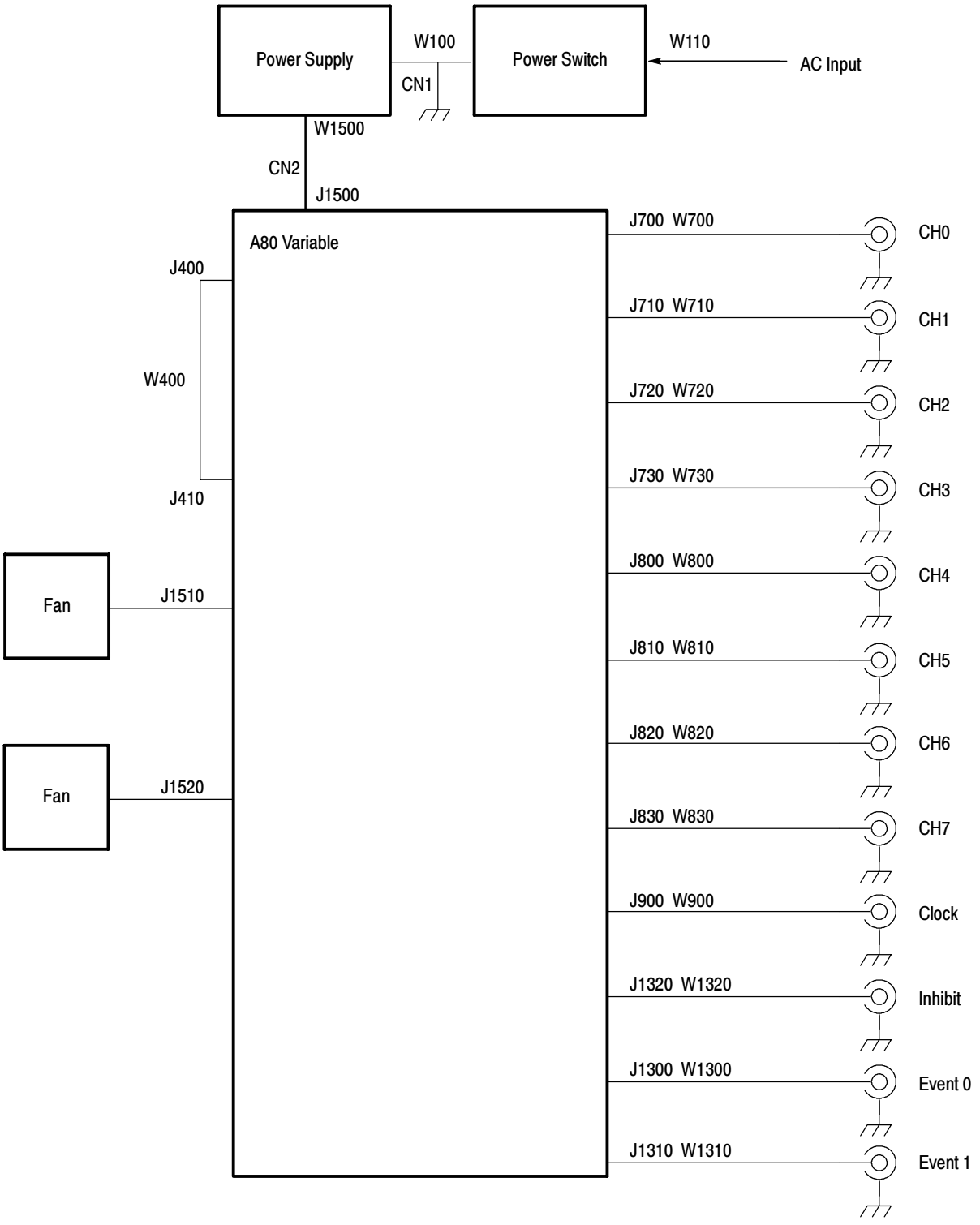

Figure 9- 5: Cable diagram for the P6475 probe

Replaceable Mechanical Parts

This section contains a list of the replaceable modules for the TLA7PG2 Pattern Generator. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Module Servicing

Modules can be serviced by selecting one of the following three options. Contact your local Tektronix service center or representative for repair assistance.

Module Exchange. In some cases you may exchange your module for a remanufactured module. These modules cost significantly less than new modules and meet the same factory specifications. For more information about the module exchange program, call 1-800-TEK-WIDE, extension 6630.

Module Repair and Return. You may ship your module to us for repair, after which we will return it to you.

New Modules. You may purchase replacement modules in the same way as other replacement parts.

Using the Replaceable Parts List

This section contains a list of the mechanical and/or electrical components that are replaceable for the TLA7PG2 Pattern Generator. Use this list to identify and order replacement parts. The following table describes each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
24931	FCI/BERG ELECTRONICS INC	RF/COAXIAL DIV 2100 EARLYWOOD DR PO BOX 547	FRANKLIN, IN 46131
7X318	KASO PLASTICS INC	5720-C NE 121ST AVE, STE 110	VANCOUVER, WA 98682
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077-0001
85480	BRADY USA	NAMEPLATE DIVISION P O BOX 571 346 ELIZABETH BRADY RD	HILLSBOROUGH, NC 27278
TK00U	LITTELFUSE	4-4-5 AOBADAI MEGURO-KU	TOKYO JAPAN,
TK0191	SONY/TEKTRONIX	PO BOX 5209 TOKYO INTERNATIONAL	TOKYO, JP 100-31
TK0AL	ONODERA MFG CO LTD	3-1-2 KAMIYOHGA SETAGAYA-KU	TOKYO JAPAN,
TK2565	VISION PLASTICS INC	26000 SW PARKWAY CENTER DRIVE	WILSONVILLE, OR 97070
TK2548	XEROX CORPORATION	14181 SW MILLIKAN WAY	BEAVERTON, OR 97005

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
1-1	063-3022-XX			1	SOFTWARE PKG:APPLICATION,CD ROM,TLA7PG2	TK0191	063-3381-00
	071-0729-XX			1	MANUAL,TECH:USER,TLA SERIES	TK2548	071-0729-00
-1	334-4565-00			1	MARKER,IDENT:BLANK	85480	ORDER BY DESCRIPTION
-2	335-0097-00			1	MARKER,IDENT:LABEL,FIRMWARE VERSION & OPTION,135 X135 MM.POLYESTER	TK0191	335-0097-00
-3	348-1662-00			1	SHLD,GSKT,ELEC:SYMETRICAL SLOTTED FINGER,11.4 MM W X 114 MM L, (FRONT)	TK0191	348-1662-00
-4	441-2213-00			1	CHASSIS ASSY:TLA7PG2,AL	TK0191	441-2213-00
-5	348-1663-00			2.76 in. (70 mm.)	GASKET,EMI:CLIP-ON,BE CU, (REAR CHASSIS)	TK0191	348-1663-00
-6	671-5063-XX			1	CIRCUIT BD ASSY:A20 CLOCK & VXI I/F	TK0191	671-5063-XX
-7	129-1247-00			5	SPACER,POST:28.8MM L,BRASS	TK0AL	ORDER BY DESCRIPTION
-8	386-7217-00			1	PANEL,END CAP:VXI TWO WIDE,AL	TK0191	386-7217-00
-9	211-0871-00			7	SCREW,MACHINE:M3 X 6MM L,PNH STL,ZN PL,CROSS REC,W/FLAT & LOCK WASHER	TK0191	211-0871-00
-10	200-4594-02			1	COVER:RIGHT,AL	TK0191	200-4594-02
-11	211-0941-00			10	SCREW MACHINE:M3 X 6MM L,FLH,BRS NI PL,CROSS REC,WFM1125	TK0191	211-0941-00
-12	348-1332-00			1	PAD,CUSHIONING:12.7MM SQ X 3.0MM H,POLYURETHAN W/ADHESIVE	80009	348-1332-00
-13	671-4859-XX			1	CIRCUIT BD ASSY:A50 PG	TK0191	671-4859-XX
-14	214-4946-00			4	SPRING:CONICAL,VXI MOUNTING SCREW,0.26 MM SUS304,5.4 MML	TK0191	214-4946-00
-15	211-1022-00			8	SCREW,MACHINE:M2.5 X 8MM L,PNH,STL,NI PL,CROSS REC	TK0191	211-1022-00
-16	213-1129-00			4	SCREW,MACHINE:M2.5 X 11MM L,PAN HD,STL, NI PL,CROSS REC & SLOTTED	TK0191	213-1129-00
-17	333-4348-00			1	PANEL,FRONT:TLA 7PG2	TK0191	333-4348-00
-18	367-0484-00			1	HANDLE,EJECTOR:INJECTOR/EJECTOR ASSEMBLY,TWO WIDE VXI,W/OUT KEYING,SPRING LOADED,PLASTIC,20% GL	7X318	1462
-19	335-0096-00			1	MARKER,IDENT:MKD TLA700,EJECTOR LABEL,BOTTOM	TK0191	335-0096-00
-20	131-1315-01			1	CONN,RFJACK:BNC,50 OHM, FEMALE,STR,PELTOLA/PANEL MOUNT	24931	28JR306-1
-21	211-A137-00			4	SCREW,MACHINE:M3 X 6MML,TRUSS HD,STL, NI PL,CROSS REC	TK0191	211-A137-00

Replaceable parts list (cont.)

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
-22	335-0095-00			1	MARKER,IDENT:MKD SONY/TEK,TOP INJECTOR/EJECTOR LABEL,(TLA PG ONLY)	TK0191	335-0095-00
-23	367-0483-00			1	HANDLE:INJECTOR/EJECTOR ASSEMBLY, TWO WIDE VXI,W/KEYING, SPRING LOADED,PLASTIC	7X318	2TEK 1461

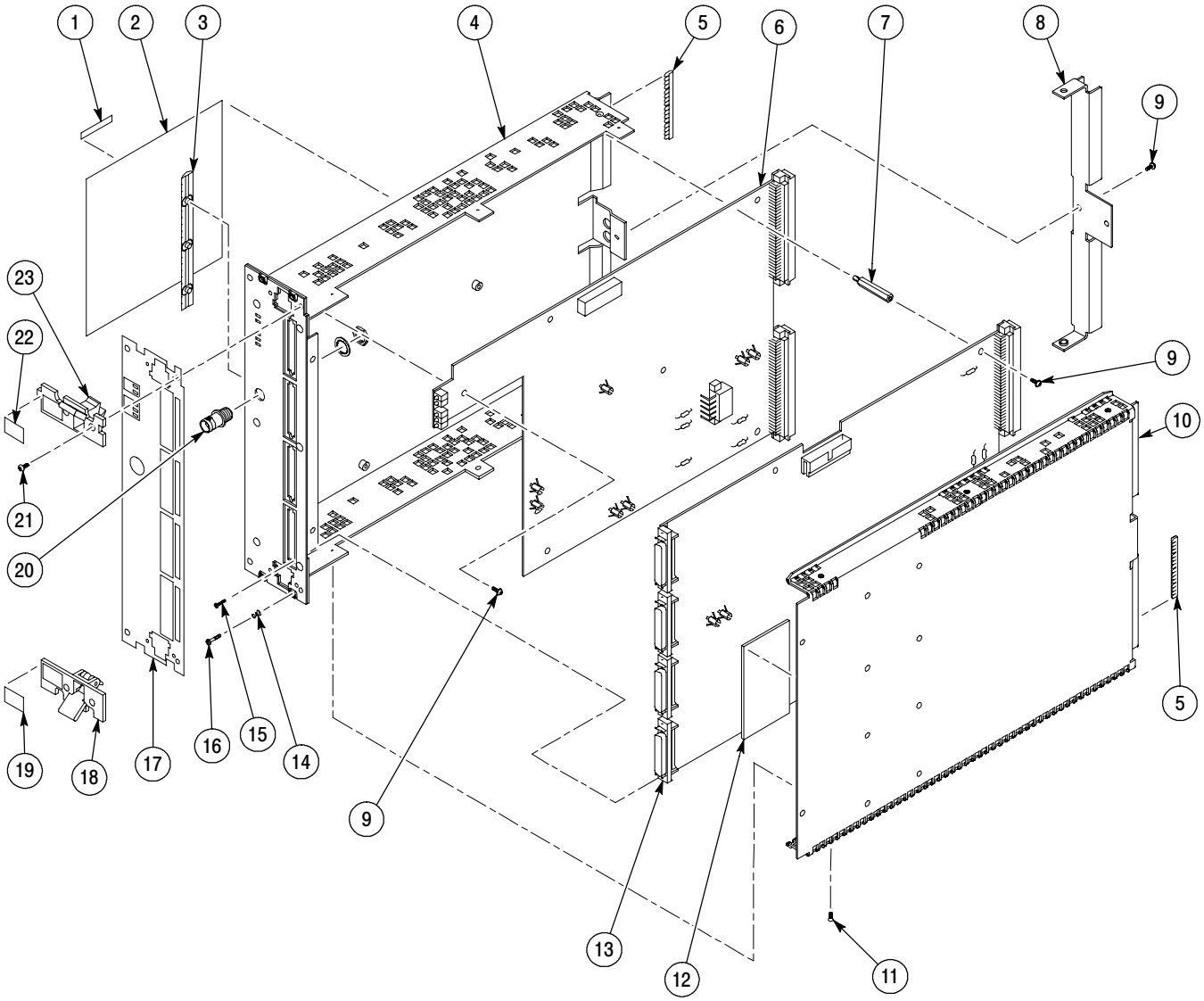

Figure 10- 1: TLA7PG2 chassis

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
2-1	174-3205-00			1	CA ASSY,RF:50 OHM COAX,20CM L,9-5,W/PELTOLA BOTH ENDS,AWG2005, (W200; EXT. CLOCK, A20J200 TO FRONT PANEL BNC)	TK0191	174-3205-00
-2	159-0347-00			3	FUSE,WIRE LEAD:3A,125V,FAST, (A20F1001, A20F1002, A20F1030)	80009	159-0347-00
-3	159-A014-00			2	FUSE:WIRE-LEAD,AXI,15A,32V,FAST, (A20F1010, A50F2715)	TK0191	159-A014-00
-4	159-0236-01			2	FUSE,WIRE LEAD:10A,125V,FAST, (A20F1020, A50F2710)	TK00U	251010
-5	174-B693-00			1	CA ASSY,RF:50 OHM COAX,30 CM L,9-2,W/PELTOLA BOTH-ENDS, (W402; A20J402 TO A50J2445)	TK0191	174-B693-00
-6	174-3200-00			1	CA ASSY,RF:50 OHM COAX,26CM L,9-1,W/PELTOLA BOTH ENDS,AWG2005, (W400; A20J400 TO A50J2440)	TK0191	174-3200-00
-7	159-A054-00			2	FUSE:WIRE-LEAD,AXI,4A,125V,FAST, (A50F2725, A50F2730)	TK0191	159-A054-00
-8	159-0344-00			1	FUSE,CARTRIDGE:AXAL,5A,125V,FAST, (A50F2720)	80009	159-0344-00
-9	174-A609-00			2	CA ASSY,RF:50 OHM COAX,30 CM L,9-3,W/PELTOLA, (W700, A20J700 TO A20J300), (W2890, A50J2890 TO A50J2200)	TK0191	174-A609-00
-10	174-2808-00			2	CABLE ASSY,RF:50 OHM COAX,25CM L,9-4,W/PELTOLA,AFG2020, (W705, A20J705 TO A20J305), (W2895, A50J2895 TO A50J2210)	80009	174-2808-00
-11	015-1570-00			4	CABLE,SP,ELEC:11 PAIR SHIELDED TWIST + 10 SINGLE LINE W/CONNECTOR,100OHM,150CM, WITH LABEL	TK0191	012-A212-00

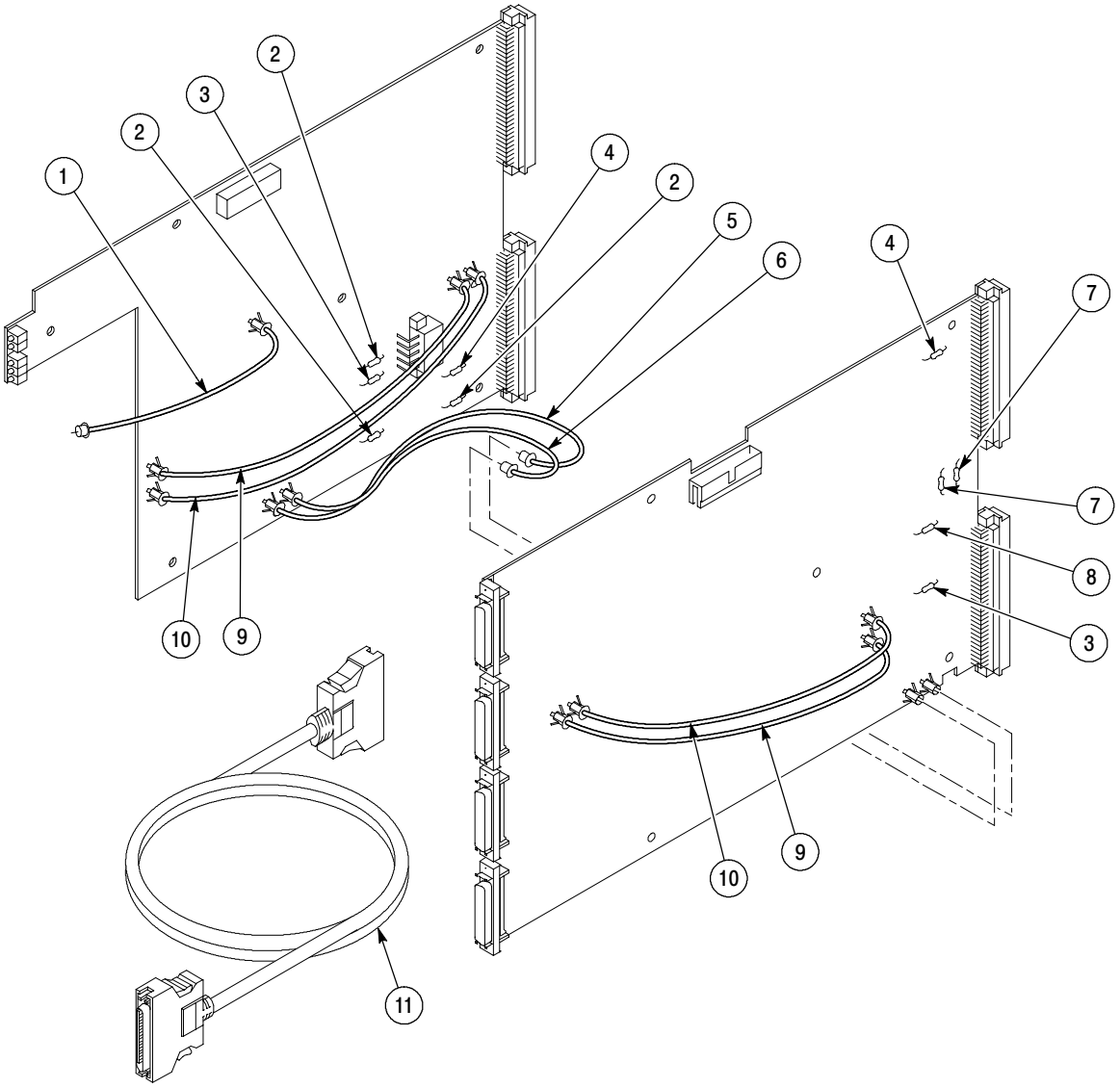

Figure 10-2: TLA7PG2 cables and fuses

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					P6470 TTL/CMOS PROBE		
	650-A793-00			1	REPL PART:P6470	TK0191	650-A793-00
10-3-1	390-1204-01			1	CABINET ASSY:PROBE,PC/ABS ALLOY	TK0191	390-1204-01
-2	335-0206-00			1	MARKER,IDENT:MKD P6470 AND PIN ASSIGN,POLYESTER	TK0191	335-0206-00
-3	159-0335-00			4	FUSE,WIRE LEAD:1A,125V,FAST BLOW,AXIAL LEADS (A95F380, A95F390. A95F392, A95F395)	80009	159-0335-00
-4	159-A025-00			1	FUSE:WIRE-LEAD,AXI,2A,125V,FAST, (A95F385)	TK0191	159-A025-00
-5	119-A698-00			1	FAN,TUBEAXIAL:12VDC,0.06A,9000RPM,BRUSHLESS,25 X 25 10,L=15CM W/CONN		119-A698-00
-6	348-A127-00			1	CUSHION,FAN:RUBBER,W/ADHESIVE TAPE		348-A127-00
-7	213-1127-00			4	SCREW,TPG:M3 8MM L,PNH,STL, BLK ZN PL,CROSS REC	TK0191	213-1127-00
-8	015-A095-00			1	ACCESSORY KIT:TERMINATOR RESISTOR NETWORK,2 EA,43 OHM,75 OHM,100 OHM, 150 OHM		015-A095-00
	307-1683-00			2	RES,NTWK,FXD,FI:(9),43 OHM,2%,0.45W (SUBPART OF 015-A095-00)	TK0191	307-1683-00
	307-1684-00			2	RES,NTWK,FXD,FI:(9),75 OHM,2%,0.45W (SUBPART OF 015-A095-00)	TK0191	307-1684-00
	307-1686-00			2	RES,NTWK,FXD,FI:(9),100 OHM,2%,0.45W (SUBPART OF 015-A095-00)	TK0191	307-1686-00
	307-1687-00			2	RES,NTWK,FXD,FI:(9),150 OHM,2%,0.45W (SUBPART OF 015-A095-00)	TK0191	307-1687-00

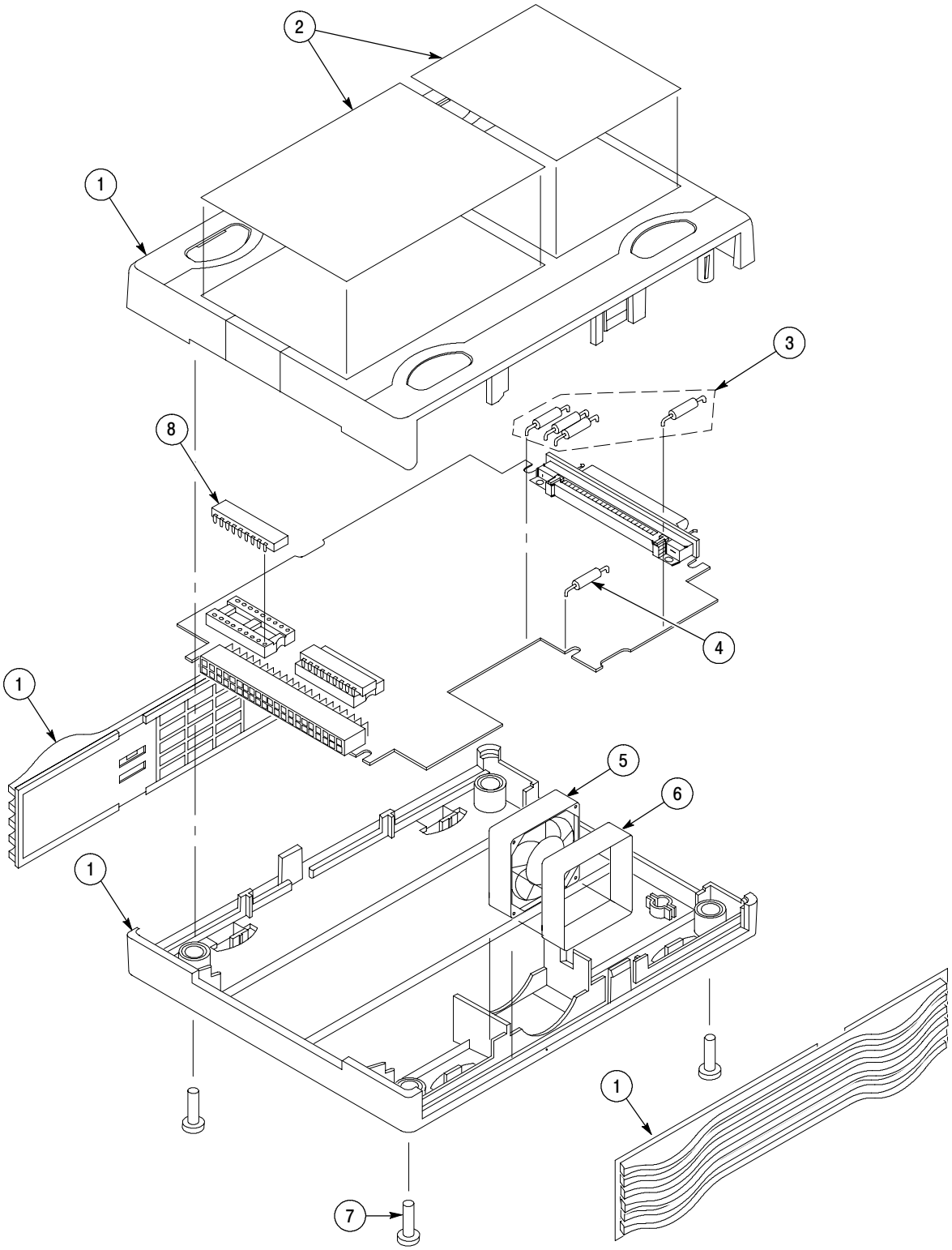

Figure 10-3: P6470 probe chassis

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					P6471 ECL PROBE		
	650-A794-00			1	REPL PART:P6471	TK0191	650-A794-00
10-4-1	390-1204-01			1	CABINET ASSY:PROBE,PC/ABS ALLOY	TK0191	390-1204-01
-2	335-0207-01			1	MARKER,IDENT:MKD P6471 AND PIN ASSIGN,POLYESTER	TK0191	335-0207-01
-3	159-0335-00			3	FUSE,WIRE LEAD:1A,125V,FAST BLOW,AXIAL LEADS, (A90F380, A90F392, A90F395)	80009	159-0335-00
-4	159-A025-00			1	FUSE:WIRE-LEAD,AXI,2A,125V,FAST, (A90F385)	TK0191	159-A025-00
-5	119-A698-00			1	FAN,TUBEAXIAL:12VDC,0.06A,9000RPM,BRUSHLESS,25 X 25 10,L=15CM W/CONN		119-A698-00
-6	348-A127-00			1	CUSHION,FAN:RUBBER,W/ADHESIVE TAPE		348-A127-00
-7	213-1127-00			4	SCREW,TPG:M3 8MM L,PNH,STL,BLK ZN PL,CROSS REC	TK0191	213-1127-00

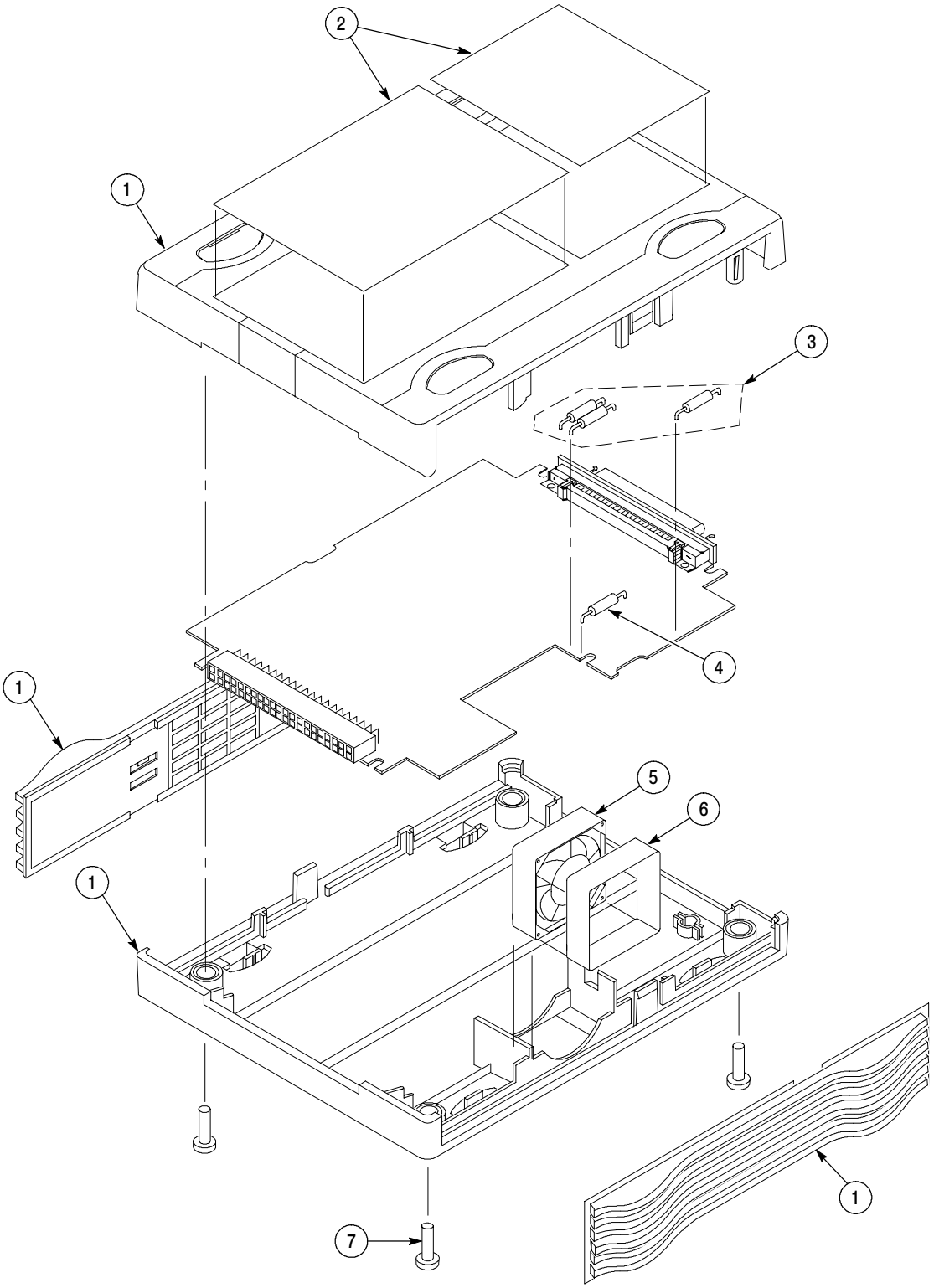

Figure 10-4: P6471 probe chassis

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					P6472 TTL/CMOS, P6473 LVDS, and P6474 LVCMOS		
	650-A874-00			1	EXCHANGE MODULE:P6472	TK0191	650-A874-00
	650-A875-00			1	EXCHANGE MODULE:P6473	TK0191	650-A875-00
	650-A876-00			1	EXCHANGE MODULE:P6474	TK0191	650-A876-00
10-5-1	390-1204-01			1	CABINET ASSY:PROBE,PC/ABS ALLOY	TK0191	390-1204-01
-2	334-A571-00			1	MARKER,IDENT:MKD P6472 AND PIN ASSIGN,POLYESTER	TK0191	334-A571-00
-2	334-A571-00			1	MARKER,IDENT:MKD P6473 AND PIN ASSIGN,POLYESTER	TK0191	334-A571-00
-2	334-A571-00			1	MARKER,IDENT:MKD P6474 AND PIN ASSIGN,POLYESTER	TK0191	334-A571-00
-3	119-A698-00			1	FAN,TUBEAXIAL:12VDC,0.06A,9000RPM,BRUSHLES S,25 X 25 10,L=15CM W/CONN		119-A698-00
-4	348-A127-00			1	CUSHION,FAN:RUBBER,W/ADHESIVE TAPE		348-A127-00
-5	213-1127-00			4	SCREW,TPG:M3 8MM L,PNH,STL, BLK ZN PL,CROSS REC	TK0191	213-1127-00
					P6474 LVCMOS ONLY		
-6	015-A095-00			1	ACCESSORY KIT:TERMINATOR RESISTOR NETWORK,2 EA,43 OHM,75 OHM,100 OHM, 150 OHM		015-A095-00
	307-1683-00			2	RES,NTWK,FXD,FI:(9),43 OHM,2%,0.45W (SUBPART OF 015-A095-00)	TK0191	307-1683-00
	307-1684-00			2	RES,NTWK,FXD,FI:(9),75 OHM,2%,0.45W (SUBPART OF 015-A095-00)	TK0191	307-1684-00
	307-1686-00			2	RES,NTWK,FXD,FI:(9),100 OHM,2%,0.45W (SUBPART OF 015-A095-00)	TK0191	307-1686-00
	307-1687-00			2	RES,NTWK,FXD,FI:(9),150 OHM,2%,0.45W (SUBPART OF 015-A095-00)	TK0191	307-1687-00

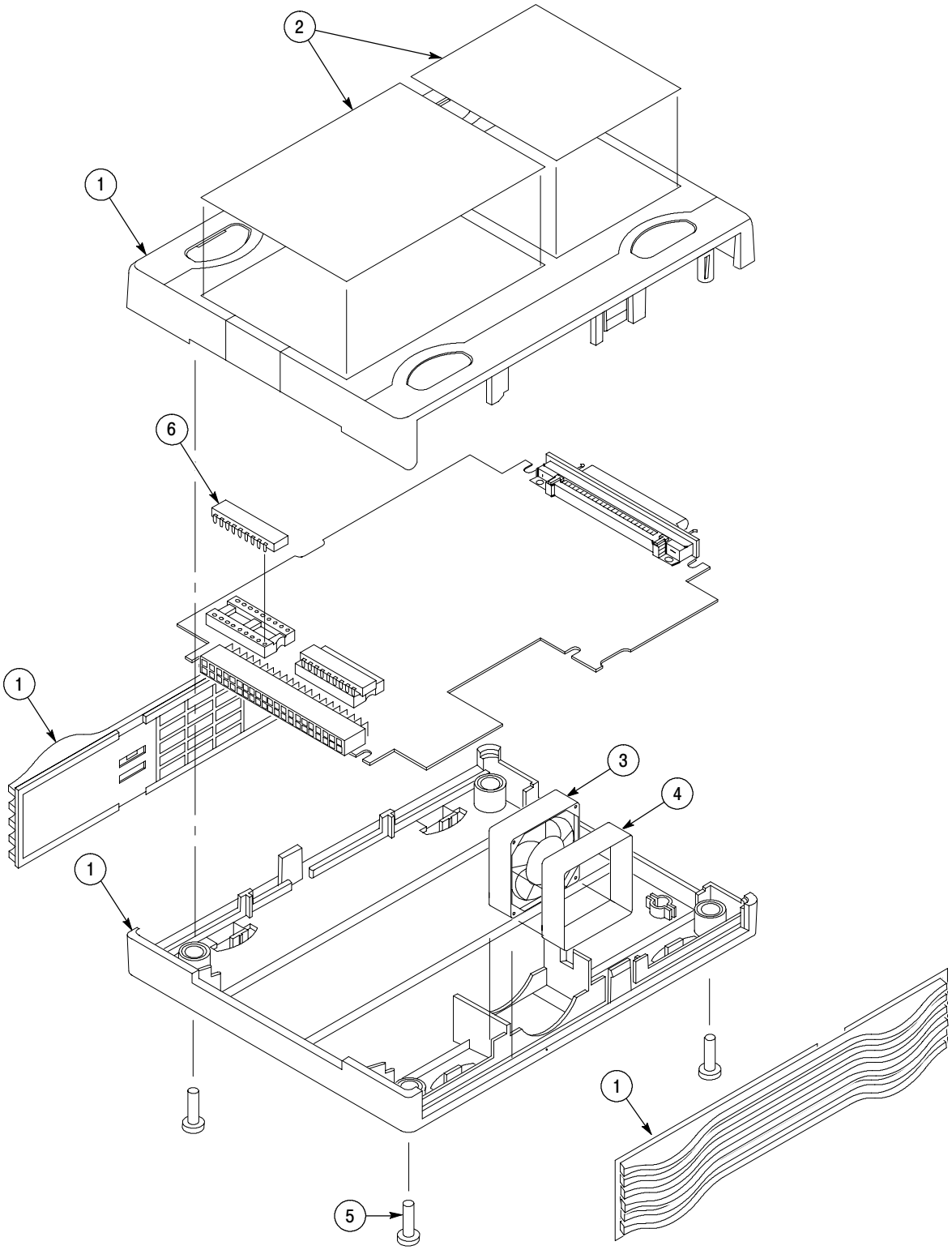

Figure 10-5: P6472, P6473, and P6474 probe chassis

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					P6475 VARIABLE PROBE		
	650-A877-00			1	EXCHANGE MODULE:P6475	TK0191	650-A877-00
	071-1017-01			1	MANUAL,TECH:INSTRUCTION,PATTERN GEN PROBE,P6470,P6471,P6472,P6473,P6474,P6475	TK2548	071-1017-01
10-6-1	211-A234-00			8	SCREWS: FAN	TK0191	211-A234-00
-2	119-B118-00			2	FAN,TUBEAXIAL:119-B055-00 W/CONN,13CM L	TK0191	119-B118-00
-3	211-A148-00			6	SCREWS: BOARD, CHASSIS		211-A148-00
-4	119-B112-00			1	POWER SUPPLY:INPUT 85-265VAC,47-440HZ,OUT+12V/2.5	TK0191	119-B112-00

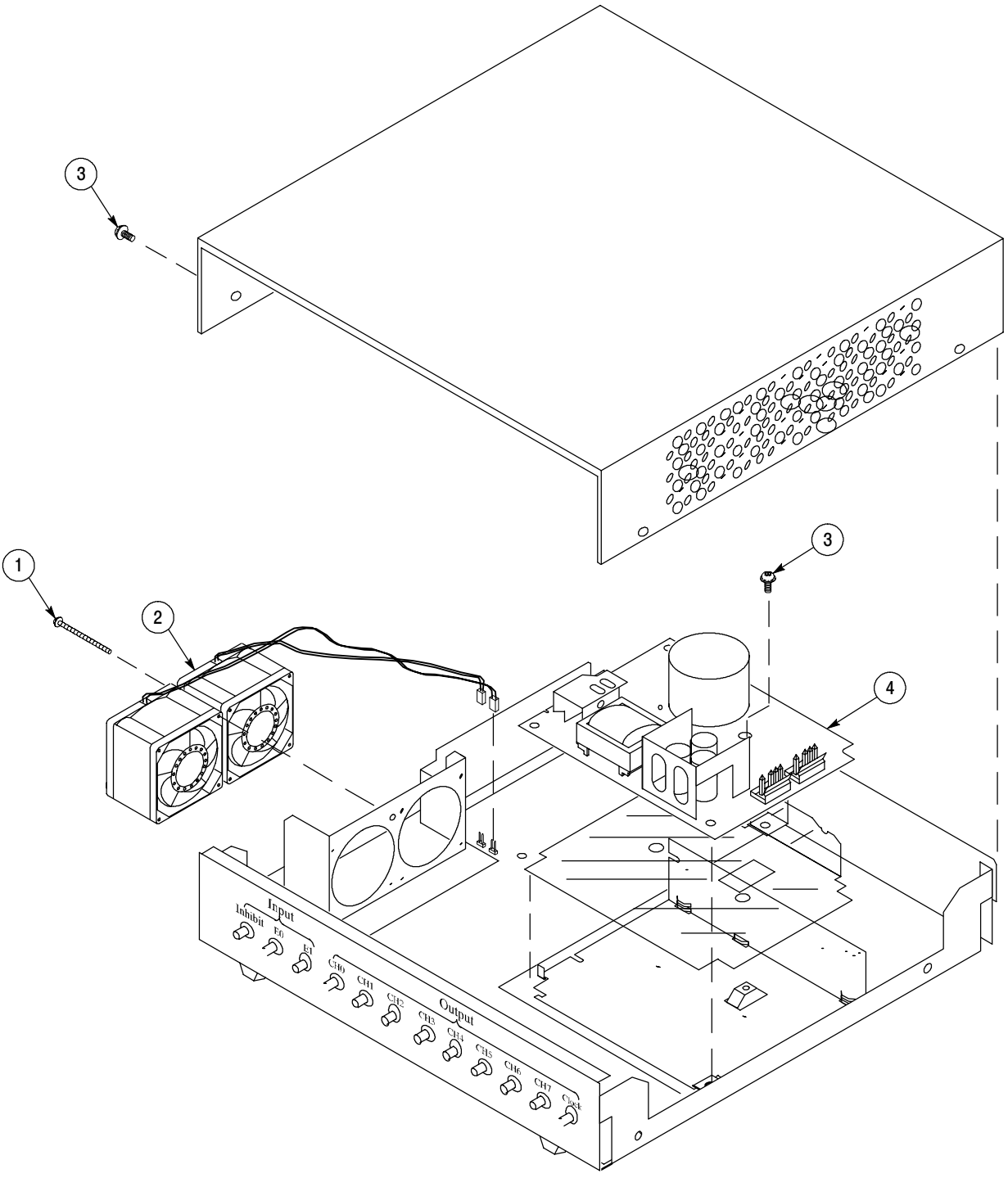

Figure 10- 6: P6475 variable probe chassis

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					CABLES FOR STANDARD PROBES ONLY		
10-71-1	020-2338-00			1	Kit: CABLE,INTCON:10-VON,TWISTED PAIR,127 MM L, 2 EACH. CABLE,INTCON:16-VON,TWISTED PAIR,127 MM L, 1 EACH	TK0191	012-2338-00

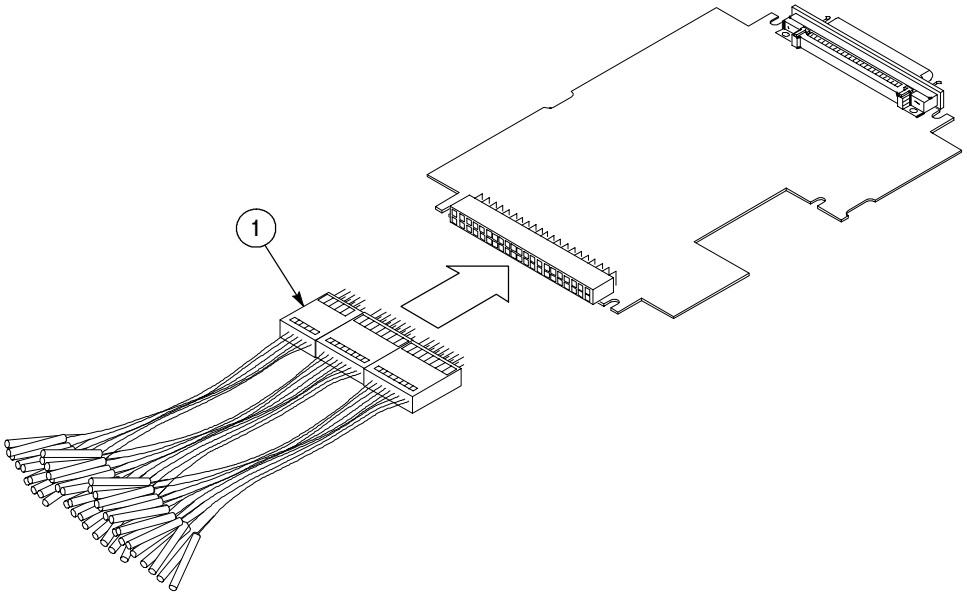

Figure 10-7: Cables for standard probes

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					CABLE FOR P6475 ONLY		
10-8-1	012-1504-00			12	CABLE ASSY, RF:50 OHM COAX, RFD,50CM L,W/SMB & HEADER,P3410	80009	012-1503-00
-2	131-5919-00			1	CONN,CARRIER:P3410, MALE & FEMALE, STR, 2X13,0.1CTR,PLZ CTR,SCI	80009	131-5919-00

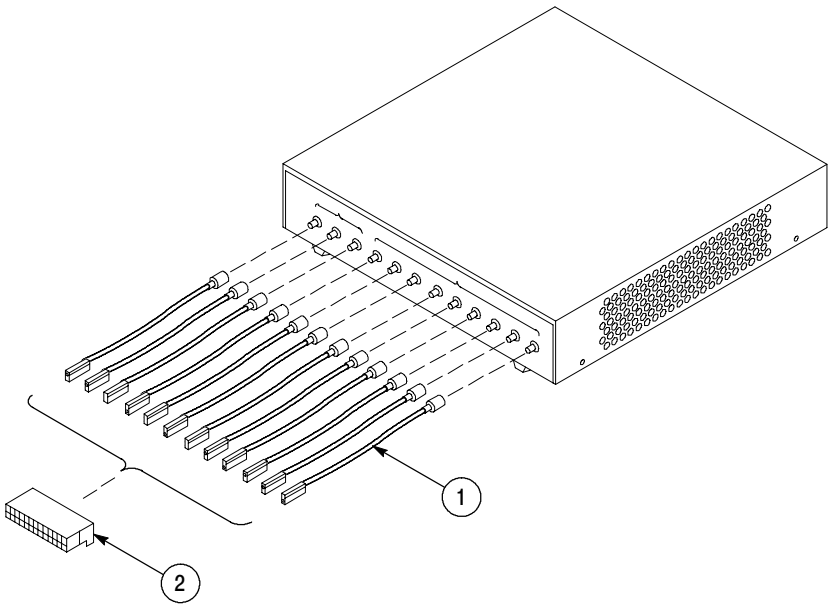

Figure 10-8: Cables for P6475 variable probe

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					OPTIONAL ACCESSORIES		
	071-0714-XX			1	TLA7PG2 PATTERN GENERATOR	80009	071-0714-XX
	020-2336-00			Bag of 42	FOR P6470, P6471, P6472, P6473, and P6475 ONLY: OPTION 1C, GRABBER TIPS	80009	020-2336-00
	067-A108-00			2	FOR P6470, P6471, P6472, P6473, and P6475 ONLY: FIXTURE, CAL: TERMINATION	80009	067-A108-00
	015-A095-00			1	FOR P6470 AND P6474 ONLY: ACCESSORY KIT: TERMINATION RESISTOR NETWORK, 2 EA, 43 OHM, 75 OHM, 100 OHM, 150 OHM	80009	015-A095-00
	206-0364-00			1	FOR P6470, P6471, P6472, P6473, and P6475 ONLY: TIP, PROBE: MICROCKT TEST, 0.05 CTR	80009	206-0364-00
	012-A224-00			1	FOR USE WITH P6475 WHEN USING A P6470, P6473 OR P6474. CABLE ASSY, SP: TIME ALIGNMENT CABLE, 3.3M (10.83 FT),	80009	012-A224-00