Tektronix Logic Protocol Analyzer Solutions for PCI Express 3.0

Instruction Manual

Tektronix Logic Protocol Analyzer Solutions for PCI Express 3.0
TLA7012/16 Mainframes
TLA Application Software V6.1+
TLA7SAxx Logic Protocol Analyzer Modules
P67SAxxx Serial Analyzer Probes
www.tektronix.com

077-0400-04

Tektronix

October 25, 2011

Contacting Tektronix

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USA

For product information, sales, service, and technical support:
- In North America, call 1-800-833-9200.
- Worldwide, visit www.tektronix.com to find contacts in your area.

Warranty

Tektronix warrants that this product will be free from defects in materials and workmanship for a period of one (1) year from the date of shipment. If any such product proves defective during this warranty period, Tektronix, at its option, either will repair the defective product without charge for parts and labor, or will provide a replacement in exchange for the defective product. Parts, modules and replacement products used by Tektronix for warranty work may be new or reconditioned to like new performance. All replaced parts, modules and products become the property of Tektronix.

In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period and make suitable arrangements for the performance of service. Customer shall be responsible for packaging and shipping the defective product to the service center designated by Tektronix, with shipping charges prepaid. Tektronix shall pay for the return of the product to Customer if the shipment is to a location within the country in which the Tektronix service center is located. Customer shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other locations.

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[W2 – 15AUG04]

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[W9b – 15AUG04]

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General safety summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it.

To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of a larger system. Read the safety sections of the other component manuals for warnings and cautions related to operating the system.

To avoid fire or personal injury

Use proper power cord. Use only the power cord specified for this product and certified for the country of use.

Use proper voltage setting. Before applying power, ensure that the line selector is in the proper position for the source being used.

Connect and disconnect properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Ground the product. This product is grounded through the grounding conductor of the power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe all terminal ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

The inputs are not rated for connection to mains or Category II, III, or IV circuits.

Connect the probe reference lead to earth ground only.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Power disconnect. The power cord disconnects the product from the power source. Do not block the power cord; it must remain accessible to the user at all times.

Do not operate without covers. Do not operate this product with covers or panels removed.

Do not operate with suspected failures. If you suspect that there is damage to this product, have it inspected by qualified service personnel.

Avoid exposed circuitry. Do not touch exposed connections and components when power is present.

Do not operate in wet/damp conditions.

Do not operate in an explosive atmosphere.

Keep product surfaces clean and dry.

Provide proper ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Terms in this manual

These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

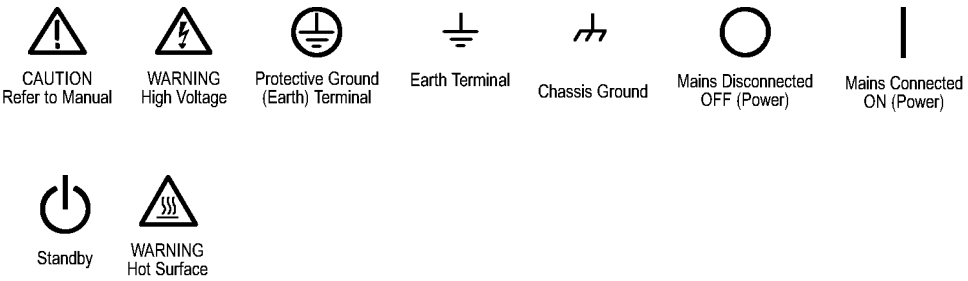
CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Symbols and terms on the product

These terms may appear on the product:

- DANGER indicates an injury hazard immediately accessible as you read the marking.
- WARNING indicates an injury hazard not immediately accessible as you read the marking.
- CAUTION indicates a hazard to property including the product.

The following symbol(s) may appear on the product:



Service safety summary

Only qualified personnel should perform service procedures. Read this *Service safety summary* and the *General safety summary* before performing any service procedures.

Do not service alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect power. To avoid electric shock, switch off the instrument power, then disconnect the power cord from the mains power.

Use care when servicing with power on. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Compliance information

This section lists the EMC (electromagnetic compliance), safety, and environmental standards with which the instrument complies.

EMC compliance

EMC compliance

Meets the intent of Directive 2004/108/EC for Electromagnetic Compatibility when it is used with the product(s) stated in the specifications table. Refer to the EMC specification published for the stated products. May not meet the intent of the directive if used with other products.

European contact.

Tektronix UK, Ltd.
Western Peninsula
Western Road
Bracknell, RG12 1RF
United Kingdom

Australia / New Zealand Declaration of Conformity – EMC

Complies with the EMC provision of the Radiocommunications Act per the following standard, in accordance with ACMA:

- CISPR 11:2003. Radiated and Conducted Emissions, Group 1, Class A, in accordance with EN 61326-1:2006.

Safety compliance

Equipment type

Test and measuring equipment.

Safety class

Class 1 – grounded product.

Pollution degree description

A measure of the contaminants that could occur in the environment around and within a product. Typically the internal environment inside a product is considered to be the same as the external. Products should be used only in the environment for which they are rated.

- Pollution Degree 1. No pollution or only dry, nonconductive pollution occurs. Products in this category are generally encapsulated, hermetically sealed, or located in clean rooms.
- Pollution Degree 2. Normally only dry, nonconductive pollution occurs. Occasionally a temporary conductivity that is caused by condensation must be expected. This location is a typical office/home environment. Temporary condensation occurs only when the product is out of service.

- Pollution Degree 3. Conductive pollution, or dry, nonconductive pollution that becomes conductive due to condensation. These are sheltered locations where neither temperature nor humidity is controlled. The area is protected from direct sunshine, rain, or direct wind.
- Pollution Degree 4. Pollution that generates persistent conductivity through conductive dust, rain, or snow. Typical outdoor locations.

Pollution degree

Pollution Degree 2 (as defined in IEC 61010-1). Note: Rated for indoor use only.

Installation (Overvoltage) category descriptions

Terminals on this product may have different installation (overvoltage) category designations. The installation categories are:

- Measurement Category IV. For measurements performed at the source of low-voltage installation.
- Measurement Category III. For measurements performed in the building installation.
- Measurement Category II. For measurements performed on circuits directly connected to the low-voltage installation.
- Measurement Category I. For measurements performed on circuits not directly connected to MAINS.

Overvoltage category

Overvoltage Category I (as defined in IEC 61010-1)

Environmental considerations

This section provides information about the environmental impact of the product.

Product end-of-life handling

Observe the following guidelines when recycling an instrument or component:

Equipment recycling. Production of this equipment required the extraction and use of natural resources. The equipment may contain substances that could be harmful to the environment or human health if improperly handled at the product's end of life. In order to avoid release of such substances into the environment and to reduce the use of natural resources, we encourage you to recycle this product in an appropriate system that will ensure that most of the materials are reused or recycled appropriately.

This symbol indicates that this product complies with the applicable European Union requirements according to Directives 2002/96/EC and 2006/66/EC on waste electrical and electronic equipment (WEEE) and batteries. For information about recycling options, check the Support/Service section of the Tektronix Web site (www.tektronix.com).

Restriction of hazardous substances

This product is classified as an industrial monitoring and control instrument, and is not required to comply with the substance restrictions of the recast RoHS Directive 2011/65/EU until July 22, 2017.

Preface

This manual describes how to install and use a TLA7SA16 or TLA7SA08 Logic Protocol Analyzer, probes, and software with your PCI Express 3 system.

Related documentation

The following table lists related documentation, available from the Tektronix Web site (www.tektonix.com/manuals).

- The *TLA7SA08 & TLA7SA16 PCIe3 Product Specifications and Performance Verification Technical Reference Manual* (Tektronix part number 077-0402-xx) lists the product specifications and high-level functional check procedures for your TLA7SA16 or TLA7SA08 Logic Protocol Analyzer Module and probes.

Related documentation

Item	Purpose
TLA Quick Start User Manuals	High-level operational overview
Online Help	In-depth operation and UI help
Installation Reference Sheets	High-level installation information
Installation Manuals	Detailed first-time installation information
XYZs of Logic Analyzers	Logic analyzer basics
Declassification and Securities instructions	Data security concerns specific to sanitizing or removing memory devices from Tektronix products
Application notes	Collection of logic analyzer application specific notes
Product Specifications & Performance Verification Procedures	TLA Product specifications and performance verification procedures
TPI.NET Documentation	Detailed information for controlling the logic analyzer using .NET
Field upgrade kits	Upgrade information for your logic analyzer
Optional Service Manuals	Self-service documentation for modules and mainframes

Product description

Tektronix provides two different logic protocol analyzer modules and probes. The logic protocol analyzer modules have acquisition rates of 8.0 GT/s, 5.0 GT/s, and 2.5 GT/s to acquire PCIe3, PCIe2, and PCIe1 data. They provide packet-level triggering, sequence triggering, and error triggering. The modules acquire up to 160 million 8b/10b symbols or bytes-per-lane. The main difference between the modules are the number of inputs.

The modules can be installed in either the TLA7012 portable mainframe or TLA7016 benchtop mainframe, depending on your application.

TLA7SA16 x8 Logic Protocol Analyzer module

The TLA7SA16 Logic Protocol Analyzer Module has 16 differential inputs and supports x1, x2, x4, and x8 links.

TLA7SA08 x4 Logic Protocol Analyzer module

The TLA7SA08 Logic Protocol Analyzer Module has 8 differential inputs and supports x1, x2, and x4 links.

Midbus probes

A midbus probe connects to a retention mechanism installed on your circuit board. To install the retention mechanism to either a PCI Express Gen3, Gen2, or Gen 1 footprint on your circuit board, refer to the instructions in Appendix C. (See page 145, *Installing the midbus retention mechanism*.) Tektronix offers the following midbus probes:

- P67SA16 x8 Midbus probe
- P67SA08 x4 Midbus probe
- P67SA16G2 x8 Midbus probe
- P67SA08G2 x4 Midbus probe

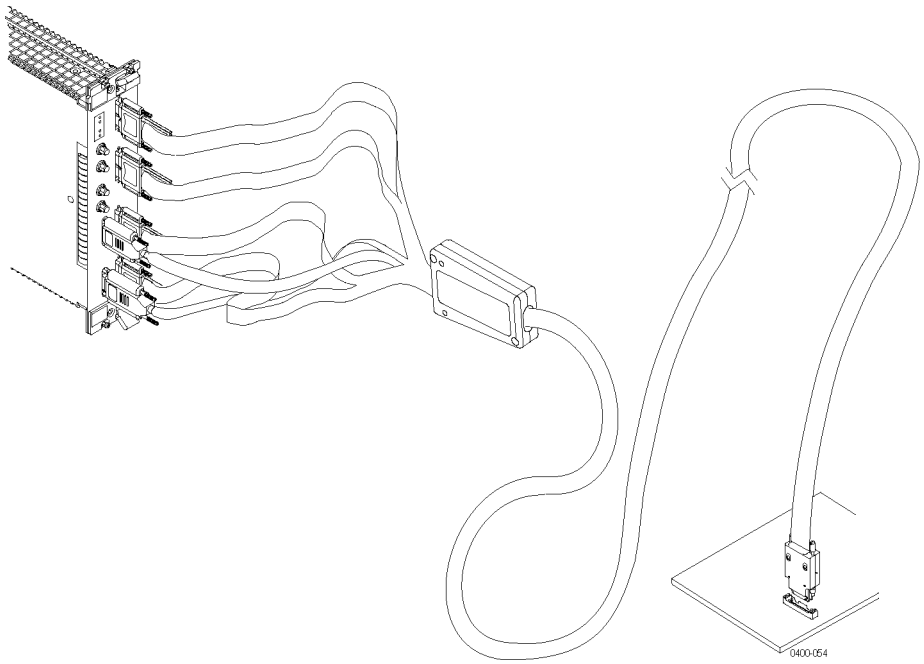


Figure 1: P67SA16 x8 midbus probe

Slot interposer probes

A slot interposer probe connects to a PCI Express slot on your SUT. Tektronix offers the following slot interposer probes:

- P67SA16S PCI Express x16 slot interposer probe
- P67SA08S PCI Express x8 slot interposer probe
- P67SA04S PCI Express x4 slot interposer probe
- P67SA01S PCI Express x1 slot interposer probe

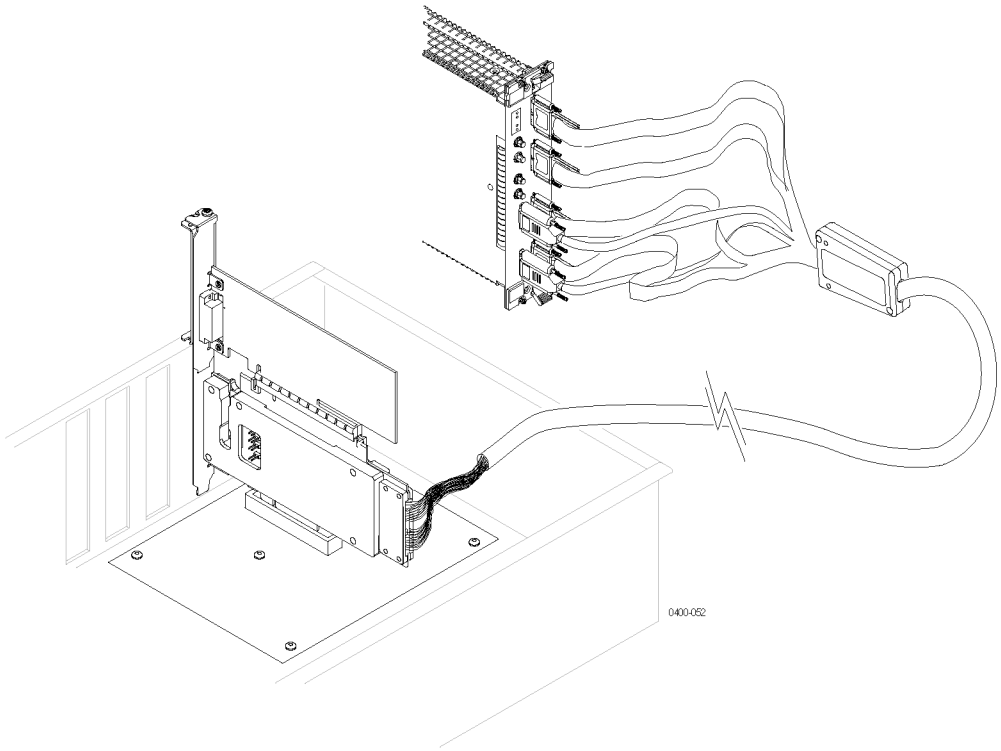


Figure 2: P67SA08S x8 Slot interposer probe

Solder-down probe

The P67SA01SD probe connects to your SUT through the differential solder-down tip (P75TLRST). Up to four probes (one differential pair each) can be installed in each signal connector to the logic protocol module. (See page 159, *Adding probes to the P67SA01SD probe connector*.)

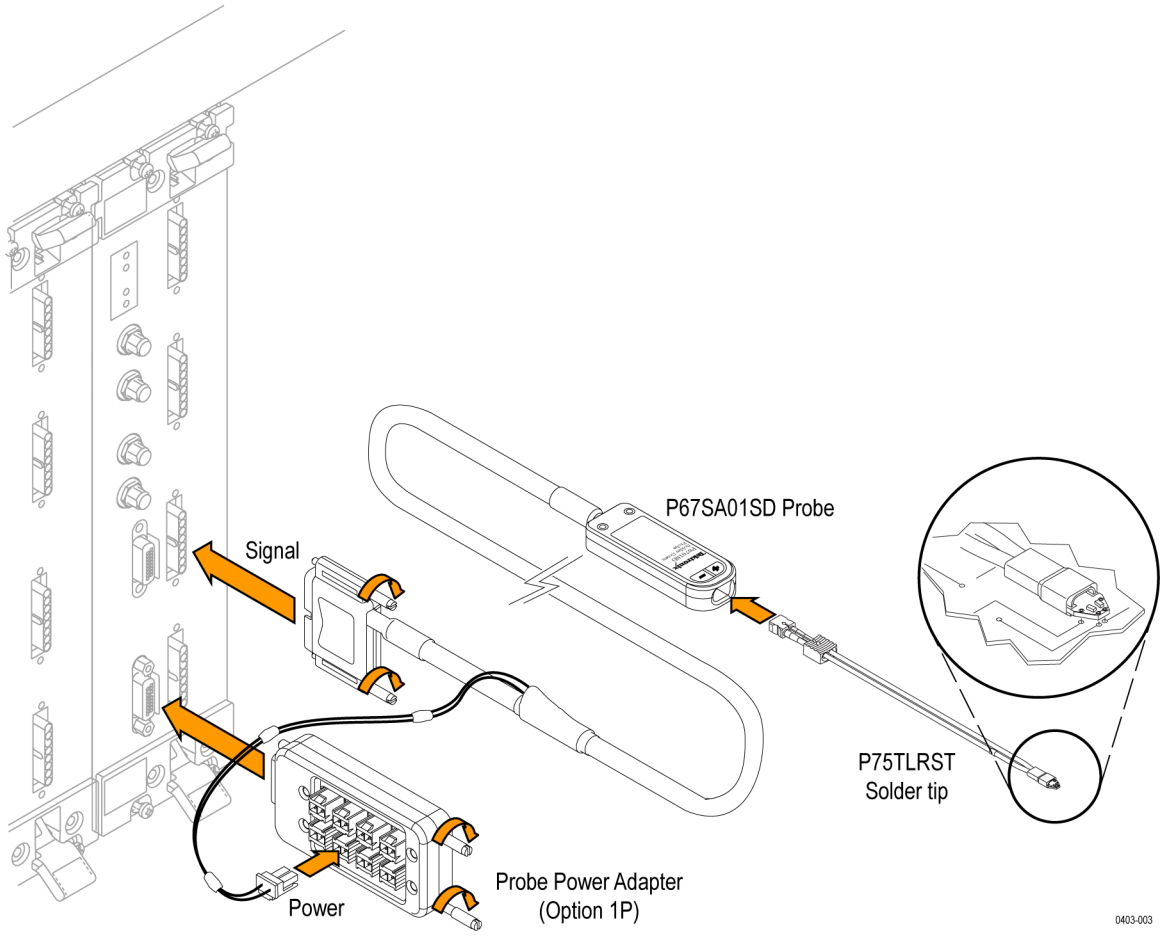


Figure 3: P67SA01SD Solder-Down probe

Logic protocol analyzer module controls and connectors

This section briefly describes the logic protocol analyzer controls and connectors.

Front panel

The front panel provides indicators for checking the status of the logic protocol analyzer. It includes probe connectors, two probe power connectors, and four connectors for a reference clock. The TLA7SA08 has two probe connectors. (See Figure 4.) The TLA7SA16 has four probe connectors. (See Figure 5.) A description of the indicators and connectors is provided. The functions of the indicators and connectors are the same for both modules except where noted. (See Table 1 on page 7.)

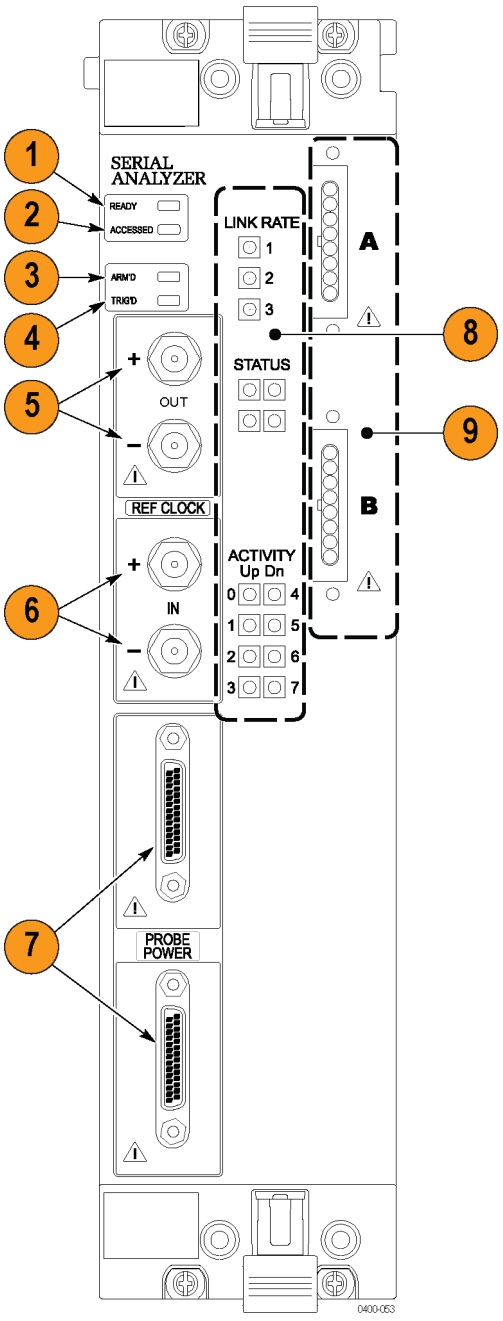


Figure 4: TLA7SA08 logic protocol analyzer front panel

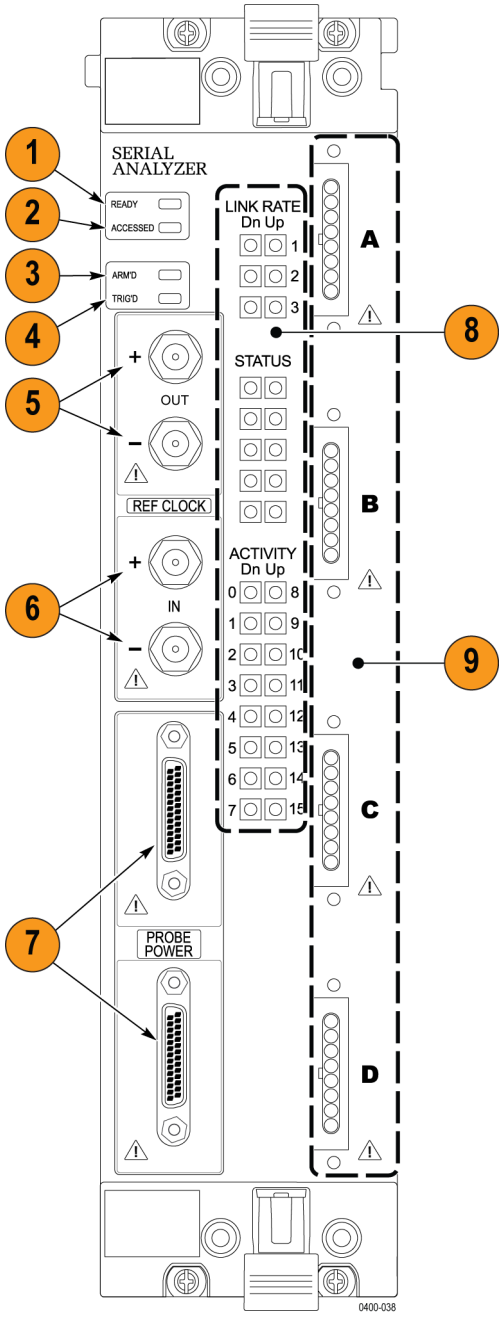


Figure 5: TLA7SA16 logic protocol analyzer front panel

Table 1: Front panel indicators and connectors

Item number	Indicator or connector	Description
1	READY indicator	The READY indicator lights continuously after the logic protocol analyzer module successfully completes the power-on process. If the indicator fails to light within five seconds of power-on, an internal module failure may be present.
2	ACCESSED indicator	The ACCESSED indicator lights anytime the controller accesses the logic protocol analyzer module.
3	ARM'D indicator	The ARM'D indicator lights when the logic protocol analyzer module is armed during an acquisition.
4	TRIG'D indicator	The TRIG'D indicator lights when the logic protocol analyzer module triggers and stays on until the module finishes acquiring data.
5	Reference Clock Output connectors	The Reference Clock Output SMA connectors (labeled + and –) provide a means of passing the differential clock signal from the Reference Clock Input connectors to another external module.
6	Reference Clock Input connectors	Two SMA connectors (labeled + and –) provide differential clock input connections from the SUT or from another module.
7	Probe Power connectors	The probe power connectors provide power to the probes.
8	LED indicators	Three groups of LED indicators provide different information. (See page 7, *LED indicators*.)
9	Probe connectors	Four connectors for the TLA7SA16 module (two for the TLA7SA08 module) provide the probe connections for the module. Each connector is labeled with a letter A, B, C, or D for the TLA7SA16 module (A or B for the TLA7SA08 module). The letters correspond to the graphic display in the Setup window.

LED indicators

The TLA7SA16 x8 modules have 32 front panel LEDs that provide information on the status of the SUT. The TLA7SA08 x4 modules have 15 LEDs.

Link rate LEDs. The top set of LEDs are the Link Rate LEDs. They monitor the current rate of the SUT and indicate the most-recent rate detected by the module. The TLA7SA16 x8 module has two columns of LEDs; the TLA7SA08 x4 module has one.

- The top LEDs (Row 1) show that the SUT is operating at 2.5 GT/s.
- The center LEDs (Row 2) show that the SUT is operating at 5.0 GT/s.
- The bottom LEDs (Row 3) show that the SUT is operating at 8.0 GT/s.

The LEDs help identify problems on the link. The link might not be operating at the highest-reported rate detected by the module on at least one direction of the link. The rate of each link is determined from Lane 0; there is no indication if other lanes are running at different rates. For the x8 modules, the two columns indicate the rate in each direction – the system tracks the current rate indicated by the direction of each link.

Status LEDs. The Status LEDs provide an indication that the system is operating as expected after the first turn-on. If the top two LEDs are turned on, the system is working as expected.

Table 2: Status LEDs

Row / LED	Description
TLA7SA16 and TLA7SA08	
Top row	
Diagnostics passed	The left LED is on when the module has passed the diagnostics. If the LED is off, check the Module diagnostics to determine which diagnostics have failed. If the Power On diagnostics fail, the Power On Diagnostics dialog box appears on the screen. If it does not, select **Calibration and Diagnostics** from the System menu to display the dialog box.
Reference Clock found	The right LED turns on when the module has locked onto a reference clock. The clock can be internal or external. This LED should always be on unless an external reference clock is selected and is not present.
Second row	
Link Locked Down	This LED monitors the Serdes status of all lanes of the Down link. The LED is on when all lanes are symbol locked or in the EIDLE state. If the link is in the EIDLE state, the LED blinks at a steady rate.
Link Locked Up	This LED monitors the Serdes status of all lanes of the Up link. The LED is on when all lanes are symbol locked or in the EIDLE state. If the link is in the EIDLE state, the LED blinks at a steady rate.
TLA7SA16 only	
Third, fourth, and fifth rows	
Acquisition progress	These LEDs progressively light in a downward direction after an acquisition has started (the RUN button was pressed or clicked). The fifth row indicates that the link is aligned (deskewed).

Activity LEDs. The lower set of LEDs show the current Serdes status of each lane. The LEDs track the status of the Dn/Up settings in the Setup window. An LED is on when the corresponding lane is symbol locked. The LEDs are on when the lane is in the EIDLE state (and the EIDLE timeout counter has not expired). The lanes are logically numbered to indicate their position in the link.

If there is a problem, you can quickly see which logical lane has the problem. A blinking LED indicates an invalid condition, such as the lane not achieving a symbol lock. For another example, if a problem occurs that causes the link to downgrade to a x4 link, LEDs 4 through 7 will turn off. Refer to the Setup window to determine which physical lane is associated with the logical lane.

NOTE. *The Up and Dn indications on the front panel do not apply when all lanes are capturing a single unidirectional link.*

Logic protocol analyzer and logic analyzer compatibility

Install the TLA7SA08 & TLA7SA16 Logic Protocol Analyzer modules in either a TLA7012 portable mainframe logic analyzer, or a TLA7016 benchtop mainframe logic analyzer. The logic analyzer must have TLA Software V6.1 or higher installed.

Options and accessories

The following table lists the accessories for the TLA7SA08 Logic Protocol Analyzer Modules and TLA7SA16 Logic Protocol Analyzer Modules.

Table 3: TLA7SAxx logic protocol analyzer module standard accessories

Accessory	Tektronix part number
Reference clock cable, SMA-to-3 pin header	872-0594-xx
Cable assembly, reference clock jumper	174-5392-xx

The following tables list the accessories for the P67SA16 and P67SA08 Midbus probes. For descriptions of the bolster assembly kits and retention mechanisms refer to the information in Appendix C. (See page 145, *Installing the midbus retention mechanism*.)

Table 4: P67SA16 and P67SA08 Midbus probes standard accessories

Accessory	Tektronix part number
Probe case	016-1994-xx
x8 Bolster assembly kit (includes $^{1}/_{16}$-inch hex wrench)	020-3056-xx
x8 Retention mechanism	131-8616-xx
x4 Bolster assembly kit (includes $^{1}/_{16}$-inch hex wrench)	020-3057-xx
x4 Retention mechanism	131-8617-xx
Probe head jack screw adjustment tool	003-1890-xx
Probe cable straps (two straps)	346-0300-xx

Table 5: P67SA16 and P67SA08 Midbus probes optional accessories

Accessory	Tektronix part number
x8 Retention assembly kit, P67SA16 Consisting of the x8 retention mechanism (Tektronix part number, 131-8616-xx) and the bolster assembly kit (Tektronix part number, 020-3056-xx)	020-4016-xx
x4 Retention assembly kit, P67SA08 Consisting of the x4 retention mechanism (Tektronix part number, 131-8617-xx) and the bolster assembly kit (Tektronix part number, 020-3057-xx)	020-4008-xx

The following tables list the accessories for the P67SAxxS slot probes.

Table 6: P67SAxxS slot probes standard accessories

Accessory	Tektronix part number
Probe case, P67SA16S	016-2002-xx
Probe case, P67SA08S, P67SA04S, P67SA01S	016-1994-xx
Probe cable straps (two straps)	346-0300-xx
Tall support bracket, P67SA16S	407-5559-xx
Short support bracket, P67SA08S, P67SA04S	407-5560-xx

Table 7: P67SAxxS slot probes optional accessories

Accessory	Tektronix part number
PCI Express x16 to x8 adapter, P67SA16S	013-0392-xx
PCI Express x16 to x4 adapter, P67SA16S, P67SA08S	013-0391-xx
PCI Express x16 to x1 adapter, P67SA16S, P67SA08S, P67SA04S	013-0375-xx

The following tables list the accessories for the P67SA01SD Solder-Down probe.

Table 8: P67SA01SD Solder-Down probe standard accessories

Accessory	Tektronix part number
Probe case	016-2009-xx
Solder kit, ROHS-compliant (two spools wire, one spool solder)	020-2754-xx
G3PO bullet removal tool	003-1896-xx
Bullet contacts (QTY 4)	013-0359-xx
Solder tip	P75TLRST
Probe cable straps (package of 2 straps)	016-1953-xx

Table 9: P67SA01SD Solder-Down probe optional accessories

Accessory	Tektronix part number
Probe power adapter (one required to power up to eight P67SA01SD probes)	P67SA01SD Option 1P
Solder tip tape (strip of 10)	066-8237-xx
Solder kit, ROHS-compliant (two spools wire, one spool solder)	020-2754-xx
Probe cable straps (package of 2 straps)	016-1953-xx
G3PO bullet removal tool	003-1896-xx
Bullet contacts (QTY 4)	013-0359-xx
Probe power adapter	878-0509-xx
Solder tip	P75TLRST
Trimode resistor solder tip, with resistor leads	020-2936-xx
Resistor conversion kit to add resistor leads to P75TLRST trimode solder tip	020-2937-xx

The following tables list the accessories for the P67SA16G2 x8 Midbus probe and the P67SA08G2 x4 Midbus probe.

Table 10: P67SA16G2 x8 Midbus probe standard accessories

Accessory	Tektronix part number
Probe case	016-1994-xx
Retention assemblies, full-width (50 contacts), long wires with integrated CLGA contacts (two sets)	131-7941-xx
Jewel case (used to hold retention mechanism)	006-8173-xx
Probe head jack screw adjustment tool	003-1890-xx
Probe cable straps (four straps)	346-0300-xx

Table 11: P67SA08G2 x4 Midbus probe standard accessories

Accessory	Tektronix part number
Probe case	016-1994-xx
Retention assemblies, half-width (26 contacts), long wires with integrated CLGA contacts (two sets)	131-7951-xx
Jewel case (used to hold retention mechanism)	006-8173-xx
Probe head jack screw adjustment tool	003-1890-xx
Probe cable straps (four straps)	346-0300-xx

Table 12: P67SA16G2 and P67SA08G2 Midbus probes optional accessories

Accessory	Tektronix part number
x8 Retention assembly kit, P67SA16G2 Consisting of the full-width (50 contacts) retention assemblies (Tektronix part number, 131-7941-xx) and the jewel case (Tektronix part number, 006-8173-xx)	020-2784-xx
x4 Retention assembly kit, P67SA08G2 Consisting of the half-width (26 contacts) retention assemblies (Tektronix part number, 131-7951-xx) and the jewel case (Tektronix part number, 006-8173-xx)	020-2785-xx

The following table lists the service options for the modules and probes.

Table 13: TLA7SAxx logic protocol analyzer module and P67SAxxx probes service options

Service Offerings	Option number
Repair warranty extended to cover three years (including warranty)	R3
Repair warranty extended to cover five years (including warranty)	R5
Calibration services extended to cover three years	C3
Calibration services extended to cover five years	C5

The following table lists the accessories for the P67UHDSMA four-differential inputs, x2, UHD-to-SMA probe leadset for use with the P67xx and P67SAxx series probes.

Table 14: P67UHDSMA standard accessories

Accessory	Tektronix part number
50 Ω SMA terminator (QTY 8)	015-1022-xx
SMA connector, female-to-female (QTY 8)	015-1012-xx

Operation overview

The following information provides a high-level overview of using the Tektronix logic protocol analyzer to set up and capture PCI Express data.

Configure the instrument

- Install modules in the mainframes. (See page 17, *Install common hardware*.)
- Download the latest TLA application software (go to www.tek.com to download the latest software).
- Connect the probes to the modules.

Connect the system to the SUT

- Connect the system to the SUT. (See page 18, *Connecting the instrument to the SUT*.)
- If your system uses two modules, connect the clock reference cable (Tektronix part number, 872-0594-xx) to one module and connect a clock jumper cable (Tektronix part number, 174-5392-xx) between the two modules. (See page 20, *Clock cable*.)

NOTE. *Tektronix recommends connecting the clock reference cable and enable it in the SUT, especially if Spread Spectrum or Active State Power Management (ASPM) is enabled. IF using the clock reference cable with two TLA7SA08/SA16 modules, use the SMA-to-SMA clock jumper cable.*

If your SUT does not have a 100 MHz reference clock, connect the clock reference cable directly to your slot interposer probe.

Calibrate the system

- Power on the instrument.
- Launch the TLA application and connect the system to the desired TLA instrument.
- Configure the Setup window. (See page 38, *Setup window*.)
- Calibrate the probes. (See page 48, *Probe calibration*.)

Acquire data

- Click the Run button begin acquiring data.
- Click the Status button to monitor the acquisition status.

Analyze the acquired data

- After the acquisition is complete, click the View Summary button in the Setup window to confirm that the calibration was successful and to get an overview of the PCIe protocol elements acquired.

Install common hardware

This manual is written assuming that your logic analyzer mainframe is already installed properly. However, a high-level module installation overview is provided. If you need additional help installing your mainframe, refer to the *TLA7000 Series Logic Analyzers Installation Manual.*

CAUTION. *To avoid damaging the mainframe, do not install or remove any modules while the mainframe is powered on. Always power off the instrument before installing or removing modules.*

Cover any empty module slots with a blank cover (Tektronix part number, 333-4206-xx).

Install the modules in the mainframe. (See Figure 6.) Use a screwdriver to tighten the retaining screws to 2.5 in-lbs after seating the modules in place.

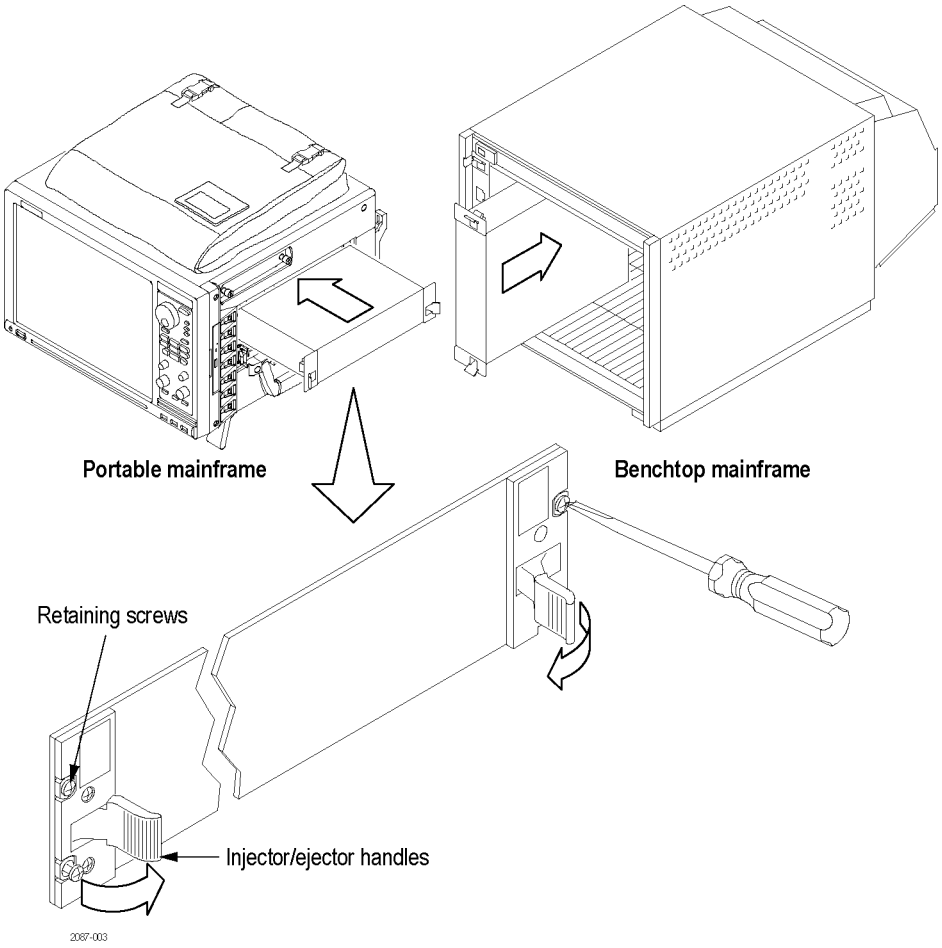


Figure 6: Installing a module

Connecting the instrument to the SUT

The probes connect your logic protocol analyzer module to the SUT. The following illustration shows possible connections to your SUT. Choose the probing scheme that works for your application.

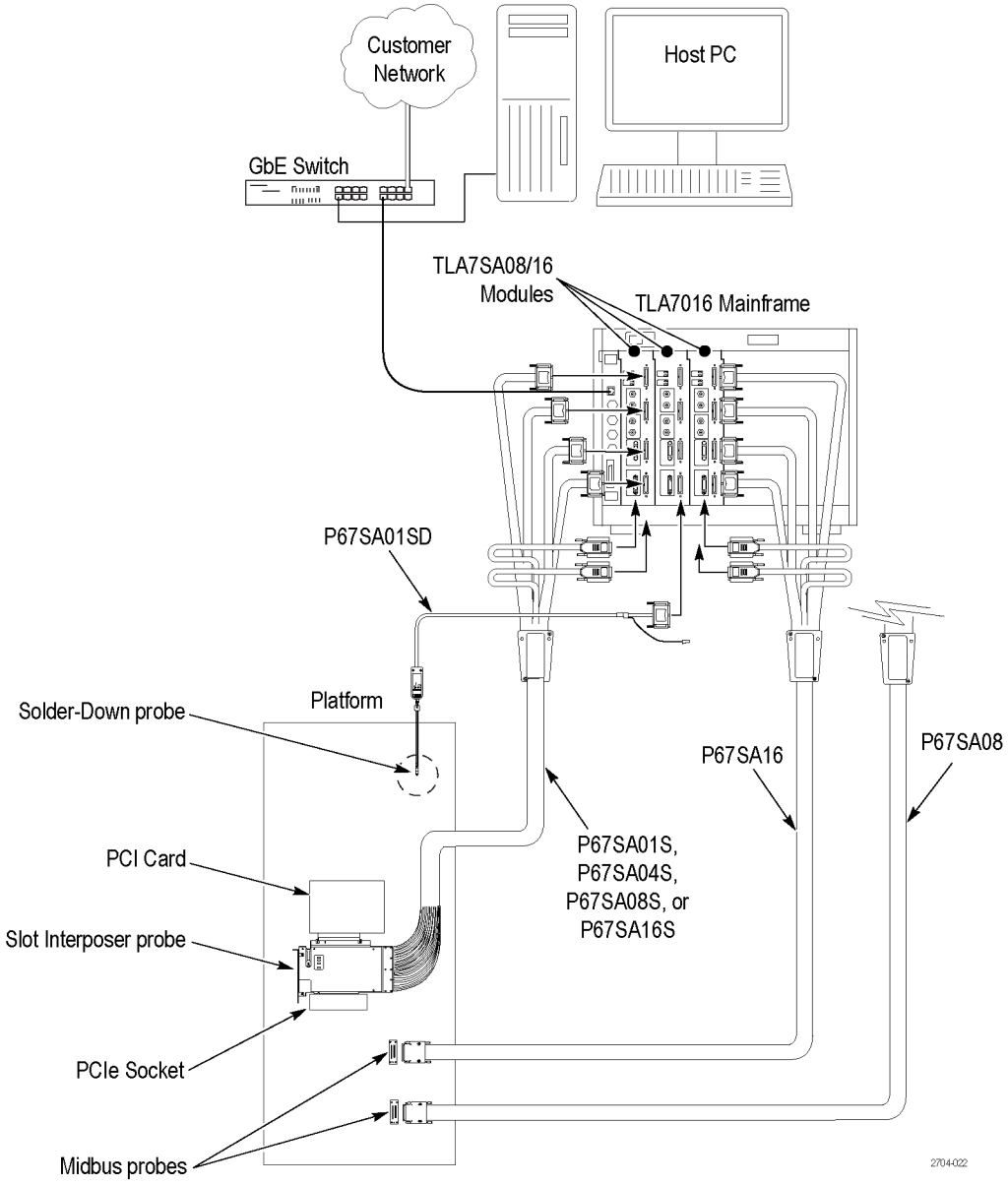


Figure 7: Installation overview

The following tables list the number of probes needed per module to connect to a link. Refer to the previous illustration for an overview of the connections to the logic analyzer and SUT. (See Figure 7 on page 18.)

Additional probe connection information is provided later in this document; refer to those sections for additional information.

Table 15: TLA Modules and midbus probes per link

Link	TLA Modules	Probes
x16	2 TLA7SA16	2 P67SA16
x8	1 TLA7SA16	1 P67SA16
x4, x2, or x1	1 TLA7SA16 or 1 TLA7SA08	1 P67SA16 or P67SA08

Table 16: TLA Modules and slot interposer probes per link

Link	TLA Modules	Probes
x16	2 TLA7SA16	1 P67SA16S
x8	1 TLA7SA16	1 P67SA08S
x4, or x2	1 TLA7SA16 or 1 TLA7SA08	1 P67SA04S
x1	1 TLA7SA16 or 1 TLA7SA08	1 P67SA01S

Table 17: TLA Modules and solder down probes per link

Link	TLA Modules	Probes
x16	2TLA7SA16	32 P67SA01SD
x8	1 TLA7SA16	16 P67SA01SD
x4	1 TLA7SA16 or 1 TLA7SA08	8 P67SA01SD
x1	1 TLA7SA16 or 1 TLA7SA08	2 P67SA01SD

Clock cable

Two clock connection cables are included with your logic protocol analyzer module. One is for connecting the reference clock input of the module to the SUT or slot interposer probe, and the other is a jumper cable for connecting one module to another.

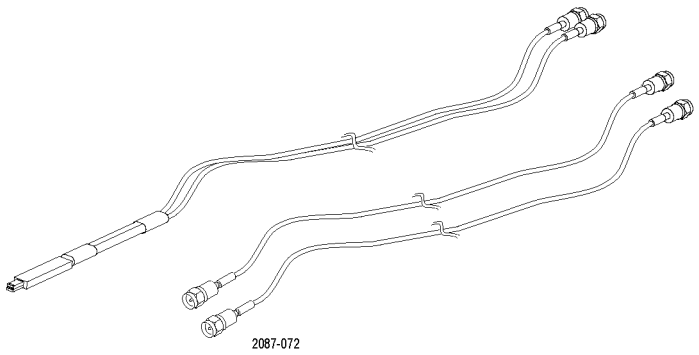


Figure 8: Clock cable and clock jumper cable

Connect the clock cable

Connect a clock cable by following these steps:

1. Connect one end of the cable to the Ref Clock input connectors (+ and –) on the logic protocol analyzer module; screw the SMA connectors down until they are snug.
2. Connect the other end of the correct cable to the SUT three-pin connector or the slot interposer probe three-pin connector.

Connect the clock jumper cable

1. Connect one end of the cable to the Ref Clock input connectors (+ and –) on the logic protocol analyzer module; screw the SMA connectors down until they are snug.
2. Connect the other end of the cable to the Ref Clock output connectors (+ and –) on another module.

NOTE. *Clock Reference Source must be set to SUT if either clock cable is used.* *(See page 44, SUT Reference clock.)*

Connect a probe to the logic protocol analyzer module

Follow these steps to connect a probe to the logic protocol analyzer:

1. Note the label on the module-end of the probe connector and connect the probe to the appropriate connector on the logic protocol analyzer (for example connect the probe with the A connector label to the A connector on the logic protocol analyzer).

NOTE. *If you have a multi-module system, make sure that you connect the probe power connectors to the same module as the respective data probe connectors. Connecting the probe power connectors to the wrong module will prevent the probes from being calibrated correctly and the probes will not acquire the correct data. Pay attention to the probe power connector labels when connecting the probes to the modules.*

2. Note the labels on the probe power connectors and connect the power connectors to the same module as the data probe connectors.
3. Tighten the connector screws using the adjustment tool included with your probe.

Connect the midbus probe

The P67SA08 and P67SA16 Midbus probes are designed for use with the TLA7SA08 and TLA7SA16 Logic Protocol Analyzer modules to capture PCIe3, PCIe2, and PCIe1 data from PCIe3 footprints. The P67SA16G2 x8 Midbus and the P67SA08G2 x4 Midbus probes are designed to connect the TLA7SA08 and TLA7SA16 Logic Protocol Analyzer modules to signals using PCIe2 footprints. The general probe connection procedures are the same for all the midbus probes; however the P67SA16G2 x8 Midbus and the P67SA08G2 x4 Midbus probes require a different type of retention mechanism.

Connect the midbus probe from the logic protocol analyzer to a retention mechanism on your circuit board. Instructions for installing a retention mechanism are provided in Appendix B. (See page 145, *Installing the midbus retention mechanism*.)

Handling the probe head

Handle the probe head with care. Keep the following points in mind:

- Handle the probe head by the outer casing. Do not touch the contacts in the center with fingers, tools, wipes, or any other devices.
- Do not expose the connector to liquids or dry chemicals.

NOTE. *Be careful when handling the probe head while the midbus probe is connected to a powered module. The probe head may become warm to the touch; the probe is operating normally.*

- When connecting the probe, be careful not to touch the probe head contacts to any other surfaces or components on your circuit board.

CAUTION. *Static discharge can damage the probe head. Always wear a grounded antistatic wrist strap whenever handling the probe head. Also verify that anything to which the probe head is connected does not carry a static charge.*

Connect the probe

Follow these steps to connect a midbus probe to the retention mechanism on your circuit board:

1. Locate the correct retention mechanism. If you intend to use multiple probes, your PCB has multiple retention mechanisms. Be careful to select the correct one.
2. Align the probe head with the retention mechanism. Both are keyed so that the probe can only be inserted one way.
3. Press the probe head into the retention mechanism.

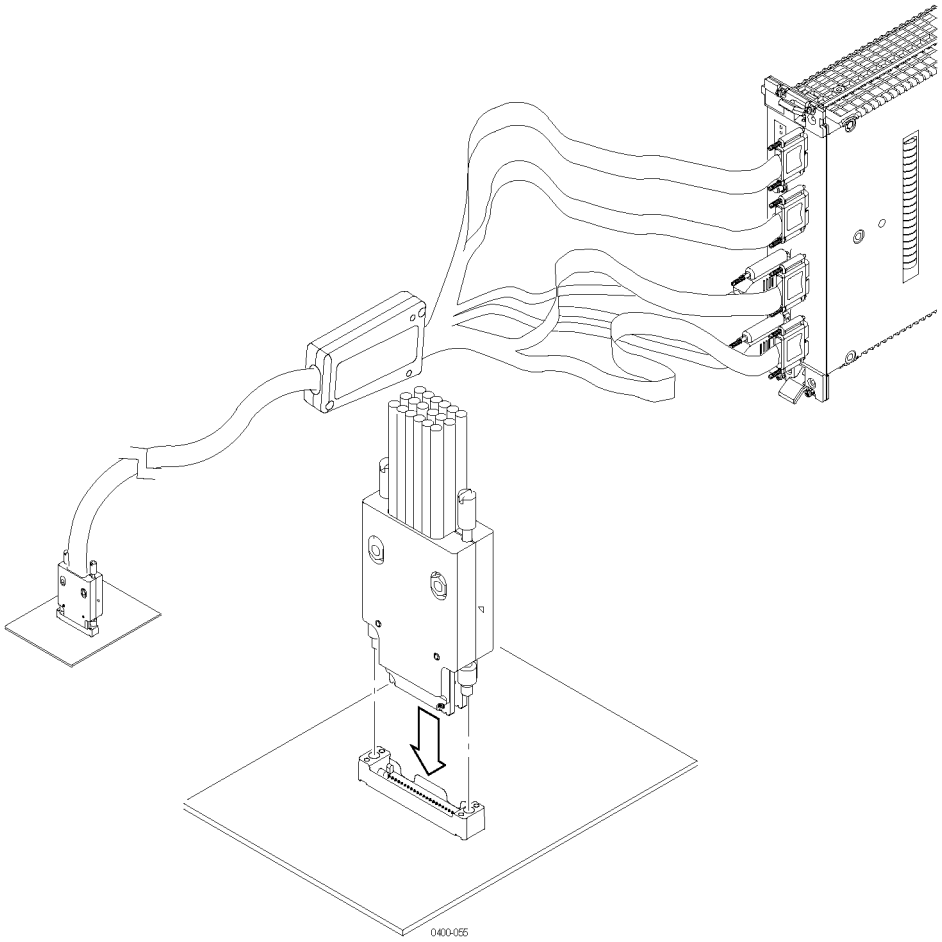


Figure 9: Connecting a probe to the retention mechanism

4. Start both mounting screws in the posts, and tighten them evenly to ensure that the probe approaches and mates squarely to the PCB. Use the adjustment tool included with your probe. Proper installation torque is 1 in-lb.

Arrange the midbus probe cables

Hang the probe cables so that the probe head is perpendicular to the circuit board, and tension on the retention mechanism is minimized. Route the cables as straight as possible, maximizing the bend radius, and making sure that a 90 degree bend does not occur within three inches of the circuit board surface. (See Figure 10.)

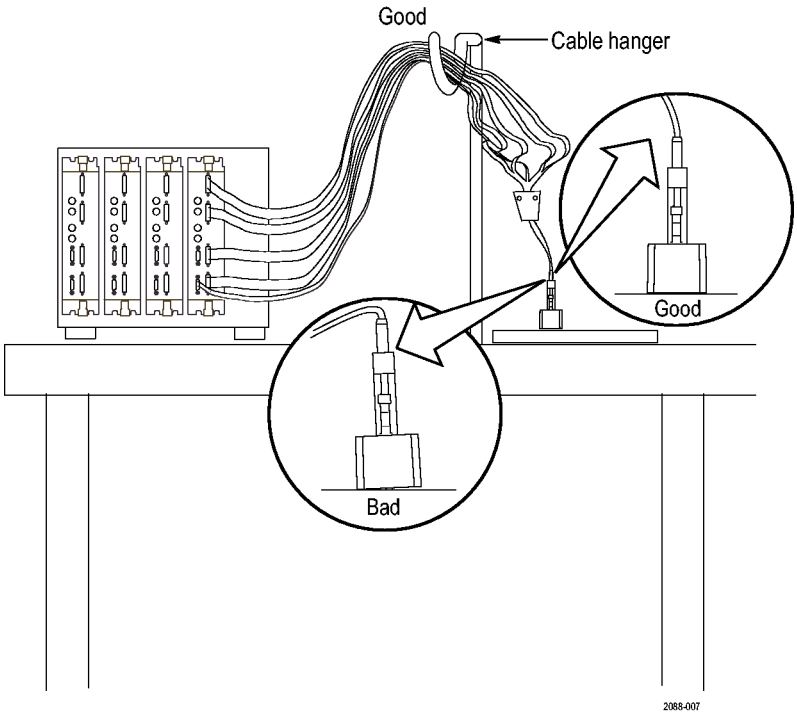


Figure 10: Arranging the midbus probe cables

Connect the slot interposer probe

Connect the slot interposer probe to a PCI Express slot on your SUT.

Handling the Probe Head

Handle the probe head with care. Keep the following points in mind:

- Handle the probe head by the outer casing. Do not touch the contacts with fingers, tools, wipes, or any other devices.
- Do not expose the connector to liquids or dry chemicals.
- When connecting the probe, be careful not to touch the probe head contacts to any other surfaces or components on your circuit board.

CAUTION. *Static discharge can damage the probe head. Always wear a grounded antistatic wrist strap whenever handling the probe head. Also verify that anything to which the probe head is connected does not carry a static charge.*

NOTE. *If your system requires a slot probe adapter, install the adapter before you install the slot interposer probe. (See page 29, Optional lane adapters installation overview.)*

Connect the probe

Connect a slot interposer probe to a PCI Express slot on your SUT by following these steps:

CAUTION. *Connecting the slot probe head to a powered SUT can damage the slot probe. Do not hot-plug the slot interposer probe head into a powered SUT. Always power off the SUT before installing the slot probe head into the SUT.*

1. Disconnect the power supply to your SUT. Disconnect the PC power supply if your SUT is connected to one.

NOTE. *To provide additional mechanical support for the PCI Express card when it connected to the slot probe, install the slot probe bracket. (See page 30, Install the slot SUT card support bracket.)*

2. Locate the correct PCI Express slot.
3. Remove the PCI Express card that is in the PCI Express slot of the SUT.
4. Align the probe head with the slot.

5. Press the probe head into the slot.

NOTE. *Remove the slot probe bracket if it interferes with the add-in PCI Express card.*

6. Position the mounting bracket and attach the screws.
7. Press your PCI Express card device into the probe.

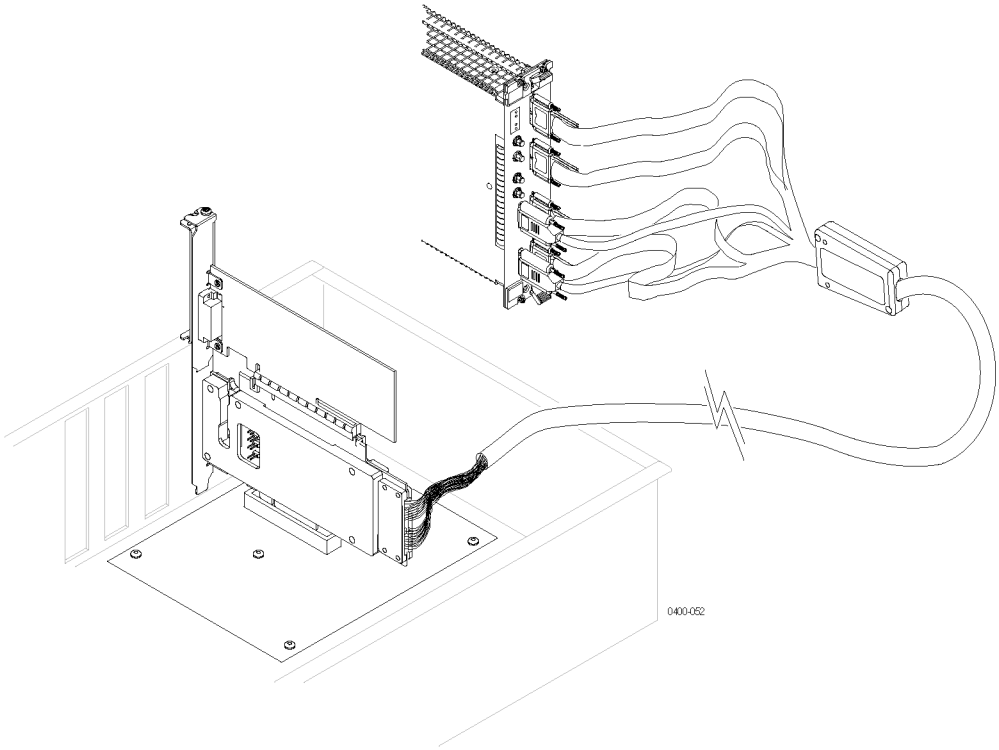


Figure 11: Connecting a slot interposer probe

NOTE. *When the slot interposer is installed, connect the power connector to the module. The module must be powered on whenever the SUT is powered on for the PCI Express signals to reach the PCI Express card connected to the probe.*

NOTE. *Unlike the bottom edge connector on the slot interposer probe, you can hot plug your PCI Express card (if hot plugging is supported) into the top edge connector of the slot interposer probe without powering down the SUT.*

Connect a probe to a x16 link

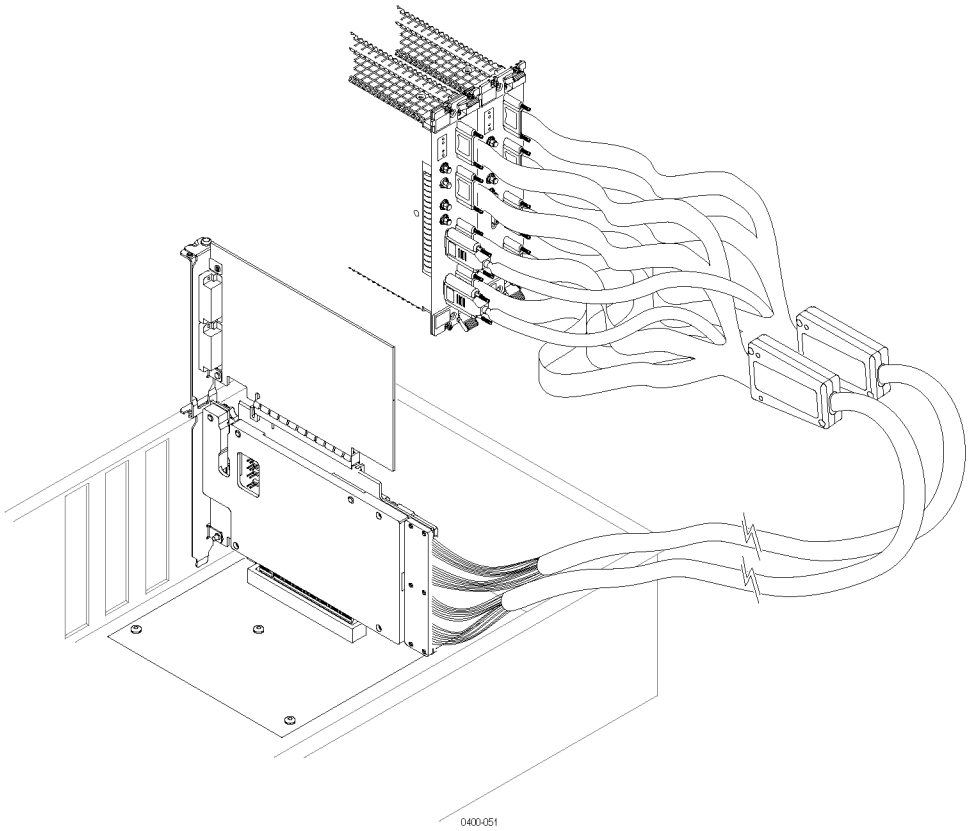
To capture signals from a x16 link you need to connect two modules to a single slot interposer probe. Connect the probe by following these steps:

NOTE. *To provide additional mechanical support for the PCI Express card when it connected to the slot probe, install the slot probe bracket. (See page 30, Install the slot SUT card support bracket.)*

CAUTION. *Connecting the slot probe head to a powered SUT can damage the slot probe. Do not hot-plug the slot interposer probe head into a powered SUT. Always power off the SUT before installing the slot probe head into the SUT.*

1. Disconnect the power supply to your SUT. If your SUT is connected to a PC power supply, disconnect the power supply.
2. Locate the correct PCI Express slot.
3. Remove the PCI Express card that is in the PCI Express slot of the SUT.
4. Align the probe head with the slot.
5. Press the probe head into the slot.

NOTE. *Remove the slot probe bracket if it interferes with the add-in PCI Express card.*



6. Position the mounting bracket and attach the screws.
7. Press your PCI Express card device into the probe.
8. Connect the probe to the two modules and connect the probe power connector to both modules.

NOTE. *The slot probes have two power connectors. Connect the power connectors to the same module as the respective data connectors. Pay attention to labels on the probe power connectors when connecting them to the module. The modules must be powered on whenever the SUT is powered on for the PCI Express signals to reach the PCI Express card connected to the probe.*

NOTE. *Unlike the bottom edge connector on the slot interposer probe, you can hot plug your PCI Express card (if hot plugging is supported) into the top edge connector of the slot interposer probe without powering down the SUT.*

Optional lane adapters installation overview

Tektronix provides a series of optional lane adapters for systems that do not have x16 sockets on the SUT. The following adapters are available:

- PCI Express x16 to x8 adapters for use with the P67SA16S slot probes
- PCI Express x16 to x4 adapters for use with the P67SA16S and P67SA08S slot probes
- PCI Express x16 to x1 adapters for use with the P67SA16S, P67SA08S, and P67SA04S slot probes

The part numbers for the adapters are listed with the P67SAxxS optional accessories. (See Table 7 on page 11.)

The adapters have minimal impact on system performance, typically increasing the measured jitter by less than 6 ps on the probe and SUT. Added jitter depends on a number of factors in the system configuration, including the output impedance match of the source and distance of the source from the add-in card.

The following illustrations shows how to install a x16-to-x8 adapter with a slot probe. (See Figure 12.)

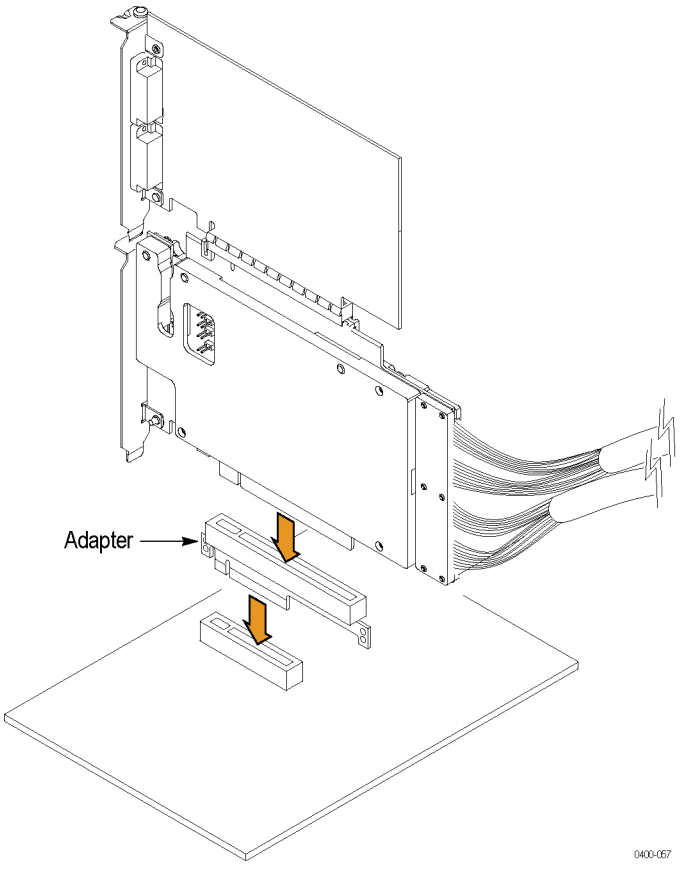


Figure 12: Installing an optional slot probe adapter

Install the slot SUT card support bracket

Use the slot SUT card support bracket to provide additional mechanical support for your PCI Express card when connecting to the slot probe. The following orientations are available; use the orientation that meets your needs. (See Figure 13 on page 31.) The illustration shows the support bracket connected to a x16 slot probe; connections to the x8, x4, and x1 probes are similar.

NOTE. *The Slot SUT card support brackets cannot be used when your system includes the optional slot probe adapters, due to the additional height added by the adapters.*

- Install the support bracket parallel with the existing PCI Express bracket (Option A).
- Install the support bracket parallel with the existing PCI Express bracket in an adjacent card slot (Option B).
- Install the support bracket perpendicular to the existing PCI Express bracket (Option C).

Use either the supplied screws or existing screws to connect the support bracket to the slot probe.

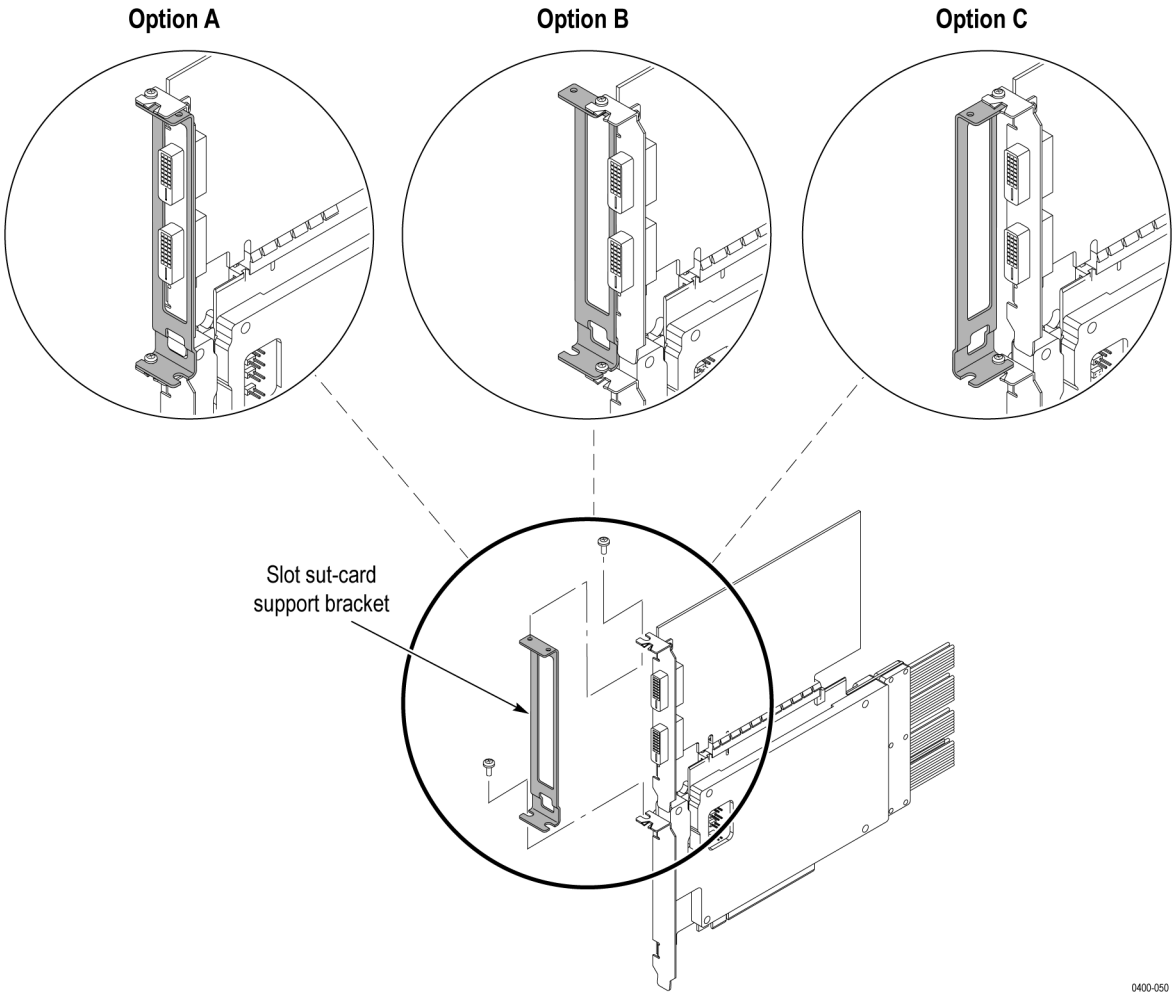


Figure 13: Slot SUT card support bracket configurations

Connect the solder down probe

The probe connects to the module and to the probe tip, and the probe tip is soldered to the circuit. Install the probe by following these steps.

Connect to the logic protocol analyzer module

1. Plug the signal connector into the module and tighten the hold-down screws.
2. Plug the probe power adapter into the module and tighten the hold-down screws.

NOTE. *The probe power adapter can be ordered as an option for the solder-down probe (P67SA01SD Option IP). (See Table 9 on page 12.)*

3. Plug the power connector into any one of the receptacles on the probe power adapter.
4. Plug the solder tip into the solder-down probe.

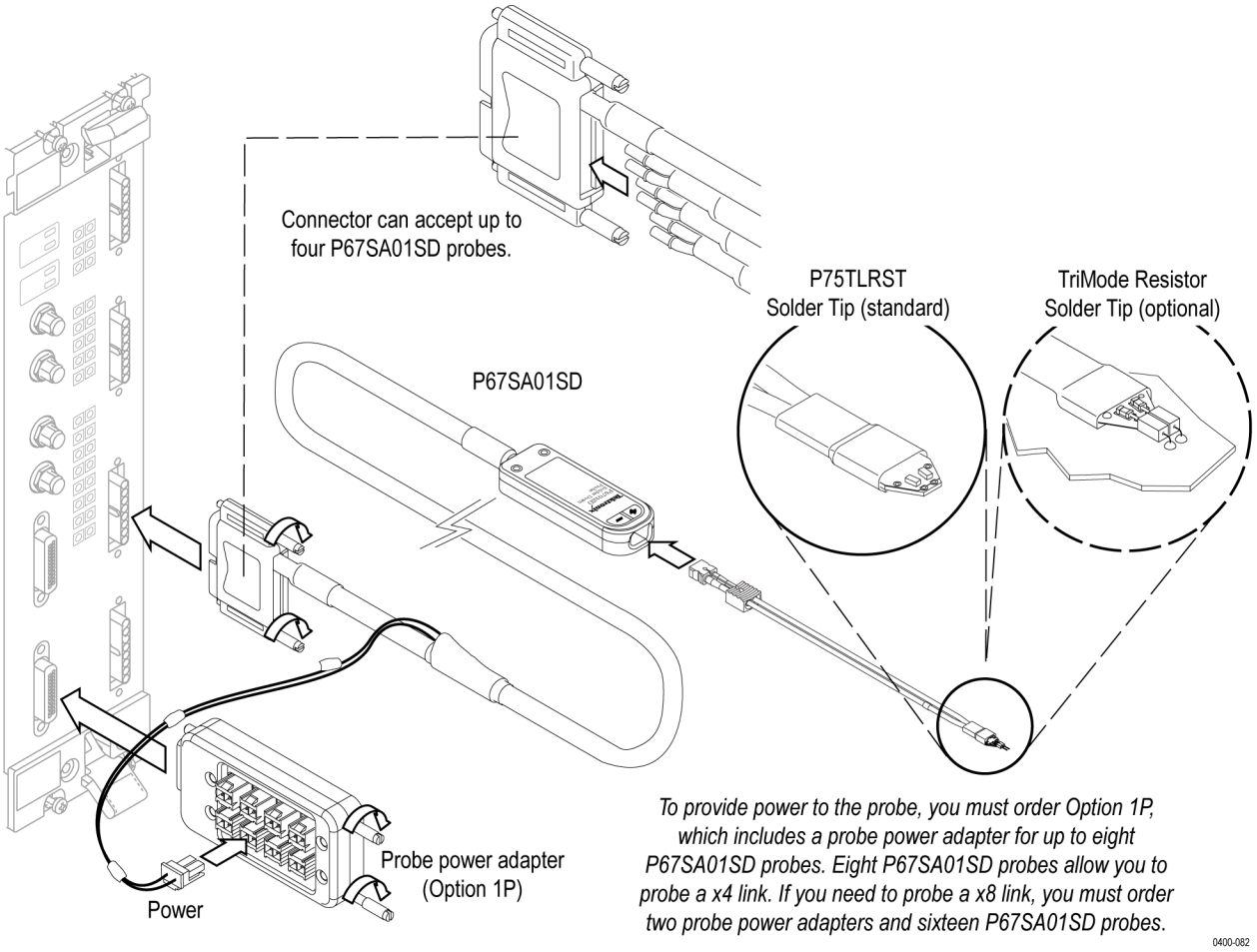


Figure 14: Installing the P67SA01SD probe

P75TLRST solder tip

Install the probe tip by following these steps:

NOTE. *This tip is very small and must be handled carefully. The following procedures describe the proper techniques for using the tip.*

Connect to the probe head. The probe body and tip cable ends are keyed to ensure correct installation.

1. Orient the probe body with the + and – inputs on top.
2. Align the tip cable lead with the red band to the + input.

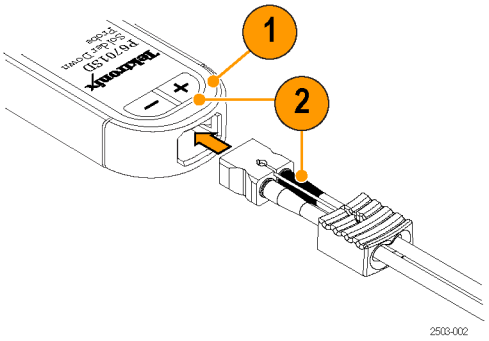


Figure 15: Connecting the P75TLRST tip to the probe head

3. Hold the cable connector by hand and push the cable into the probe body until you feel a click. The cable housing is fully seated when it is flush with the edge of the probe body.
4. To remove the tip, pull the cable tab straight out from the probe body.

CAUTION. *Pulling the cables when removing the probe tip can damage the tip or the probe. To avoid this, pull only on the cable tab when removing the tip.*

Connect to the circuit. The dimensions of the solder tip connections are provided in this manual for reference. (See Figure 55 on page 91.) Design the tip footprint into your circuit board layout for easier test connections.

To connect the probe tip to your circuit, use the wire and solder that are provided in the wire replacement kit. The kit includes:

- 0.004 in (0.1016 mm) wire
- 0.008 in (0.2032 mm) wire
- SAC305 solder (RoHS compliant)

1. Identify a location where the tip can be placed, soldered, and attached to your circuit. When working with long wires (~1 inch), keep the finished wire lengths of the signal and ground connections as short as possible.
2. Lay the wires against a circuit board pad, trace, or other conductive feature. (If vias or through-holes are very close, thread the wires through them.)
3. Solder the wires to your circuit.

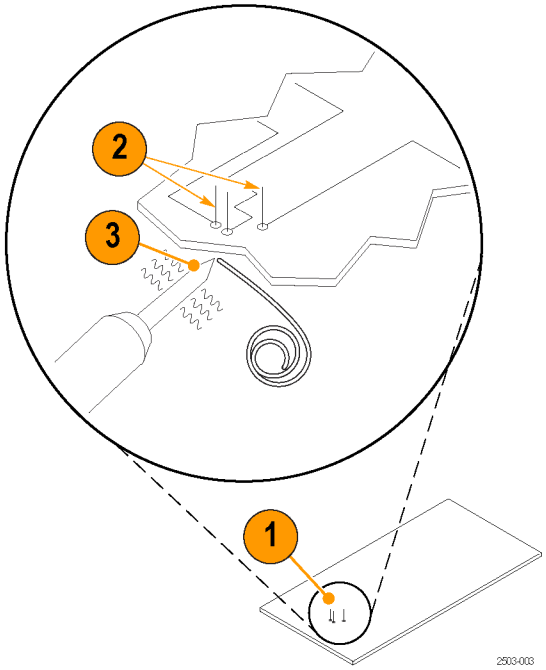


Figure 16: Connecting wires to the circuit

4. Attach tip tape to the bottom of the tip.
5. Clean out the tip vias with a solder-wick material if you are reusing the tip. Thread the wires through the tip.
6. Press the tip to the circuit board and quickly solder the wires to the tip. Keep all finished wire lengths as short as possible.
7. Clip off the excess wire from all of the solder joints.
8. Push the end of the tip into the probe head until it seats in the probe head.

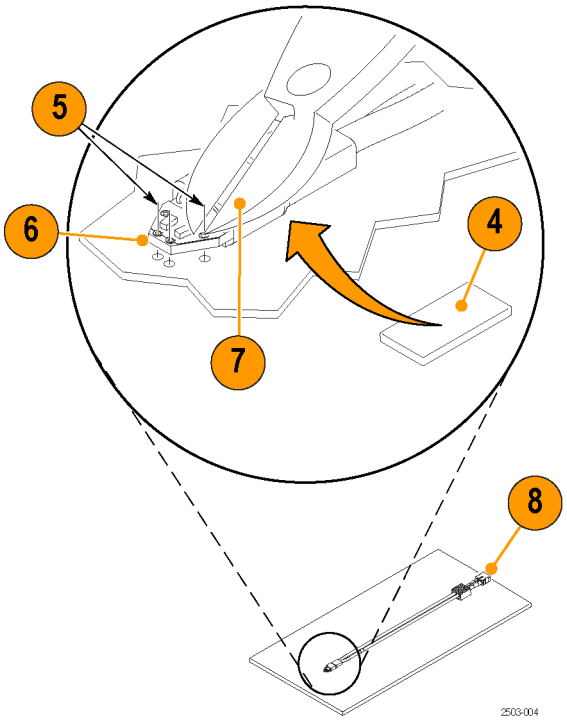


Figure 17: Connecting the tip to the circuit

9. Secure the probe to the circuit board with tape or with the hook-and-loop strips and dots that are included with the probe.

Applying and removing power

After you have connected all probes to the SUT, you are ready to apply power to the SUT and the logic protocol analyzer.

NOTE. *When using slot interposer probes power on the logic protocol analyzer before applying power to the SUT.*

NOTE. *Unlike the bottom edge connector on the slot interposer probe, you can hot plug your PCI Express card (if hot plugging is supported) into the top edge connector of the slot interposer probe without powering down the SUT.*

Set up the logic protocol analyzer module

NOTE. *Refer to the information earlier in this document for installing common hardware, connecting the instrument to the SUT, and connecting probes to the SUT and to the logic protocol analyzer.*

The logic protocol analyzer can automatically configure the Setup window based on characteristics of the link. For the auto configuration to function properly, the logic protocol analyzer must sense Gen 1 or Gen 2 training sets. To ensure that the logic protocol analyzer senses the training sequences, perform the following steps.

1. Start the TLA application and wait for the Setup window to appear.
2. Start or restart the SUT so that the logic protocol analyzer can sense the training sequences on the bus.

NOTE. *If this is a first-time setup, the Setup window will display status messages and indications in the Calibration dashboard that probe calibration is required. Calibrate the probes before continuing this procedure. (See page 49, Calibrate the probes.)*

3. Use the Setup window to view signal activity. Adjust the link characteristics as needed to conform to your specific SUT behavior (such as, polarity, width, and rate).
4. If this is the first-time setup, use the default trigger settings in the Trigger window to acquire some data to see if the instrument behaves as expected.
5. Click **Run** to acquire and validate initial data in the Transaction and Listing display windows.

NOTE. *The Transaction and Listing windows appear automatically to display data from the SUT to help you validate that the system is set up correctly.*

6. Use the Summary Profile window together with the Transaction and Listing windows to analyze high-level transaction information linked to lowest-level physical layer symbols across the entire acquisition.

Setup window

The Setup window is the default window when you start the TLA application or default the system. If your system includes more than one logic protocol analyzer module, the system displays the Setup window for the module in the lowest-numbered slot. By default, he Setup window automatically configures the logic protocol analyzer based on the characteristics of the link.

NOTE. *After starting the TLA application, start or restart the SUT so that the logic protocol analyzer senses the Gen 1 or Gen 2 training sequences.*

The Setup window provides easy access to a variety of configuration options to do the following:

- Acquire bidirectional data
- Calibrate probes attached to the module and to the SUT
- Specify the link width and transfer rate
- Use a clock embedded in the data stream or use an external clock connected to the front panel
- Establish storage conditions such as hardware filtering, link scrambling and deskewing, specifying the storage length, and specifying the trigger position
- Establish which modules are associated to links

Open the Setup window

The Setup window is the default window when you start the TLA application. If the Setup window does not display, open the window using one of the following methods:

- Click the Setup Icon in the TLA Explorer.

  By default the first logic protocol analyzer is identified as SA 1.

- Click the Setup button in the System Navigation toolbar.

  If your system has more than one module, select the appropriate module from the Setup button.

- Click the Setup button on the Logic Protocol Analyzer icon in the System window.

- Click **Next Setup** in the Window menu or press the F10 key.

The default Setup window is shown below. (See Figure 18.) The color of the status indicators near the center of the window will vary depending on the signal activity at the probe tip.

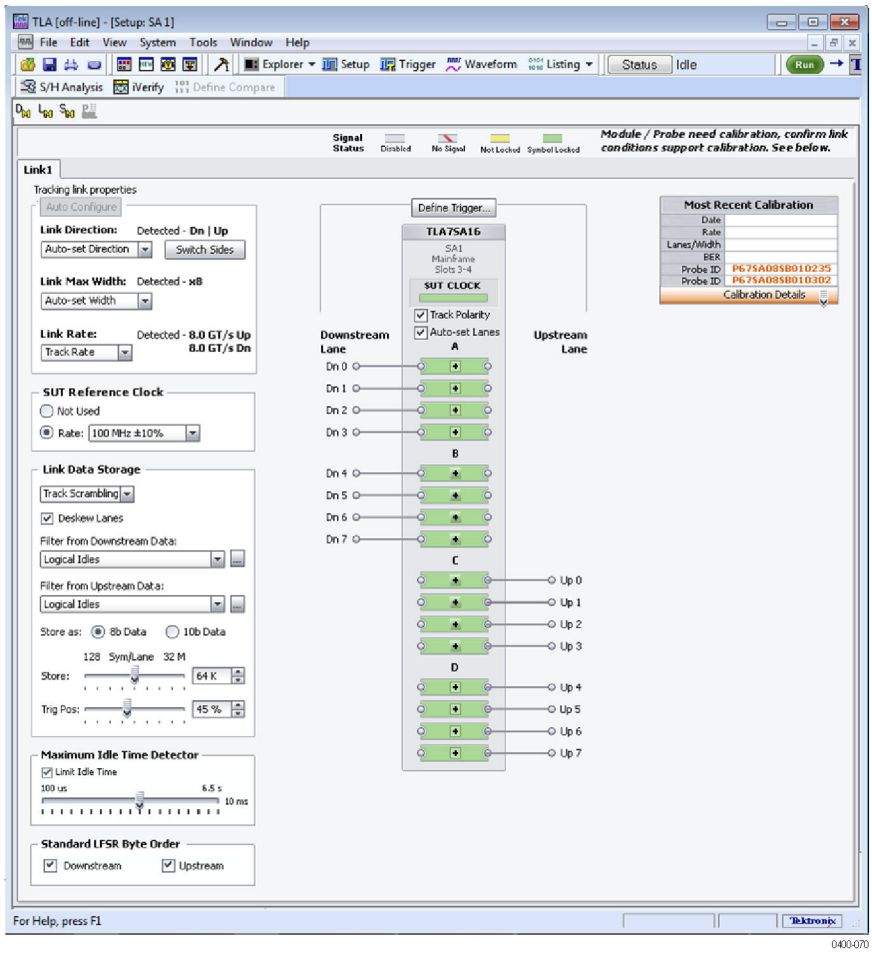


Figure 18: Default Setup window

Monitoring signal activity

After you have connected the probes and installed the software and firmware, monitor the signal activity on each of the lanes to make sure that your system is operating correctly and that the probes are connected properly. A graphic representation of the logic protocol analyzer module shows a status indicator for each lane. Use the status indicators to determine if the SUT produces the signals that the module can recognize. The logic protocol analyzer constantly monitors the status of each lane, even when data is not being acquired. The status of each lane is mirrored by the front-panel LEDs.

A description of each status indicator is listed below.

Table 18: Status indicators in the Setup window

Indicator	Description
	No signal (gray). A signal has not been assigned to a lane. (See page 45, *Assigning lanes*.)
	Signal missing. The signal is assigned to a lane, but it is not recognized. This symbol appears when a lane is inactive.
	Signal (yellow). A signal is detected, but not locked. The data is not recognized.
	Data signal (green). A signal is detected and recognized as data.
	Clock signal. A clock signal is detected via the clock cable connected to the SUT or slot interposer probe. The colors and patterns of the clock signal indicator function similar to those of the other status indicators. This indicator is gray if the SUT Reference Clock selection is set to Not Used. (See page 44, *SUT Reference clock*.)

Auto configuration

The logic protocol analyzer automatically configures the link direction, maximum link width, link rate, and other settings that the system senses through the setup and the SUT. This allows the module and software to track the state of the link and reduces the time required to make an initial acquisition. All of the controls that the system tracks use a "Track" prefix, such as Track Direction, Track Training, or Track Rate. The system tracks the configuration settings until you manually make a change in the setup.

When you manually change any of the configuration settings, the system displays a list of the changed settings at the top of the window. For example in the following illustration, the left side shows the system operating in the auto-configuration mode. The right side of the illustration shows a manually-configured system, in which the Link Direction, Width, and Lanes are not being automatically configured. (See Figure 19.)

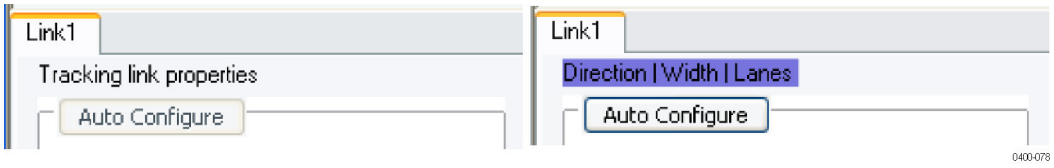


Figure 19: Changes identified in the Setup window

In addition to providing indications of which link characteristics are manually tracked, the system also provides indications in the Setup window where it sensed discrepancies between the manual settings and the automatically-detected settings. For example, in the following illustration, the Link Direction has been set to only acquire downstream data. (See Figure 20 on page 43.) Next to its setting, the system provides the indication that it has detected traffic in both directions.

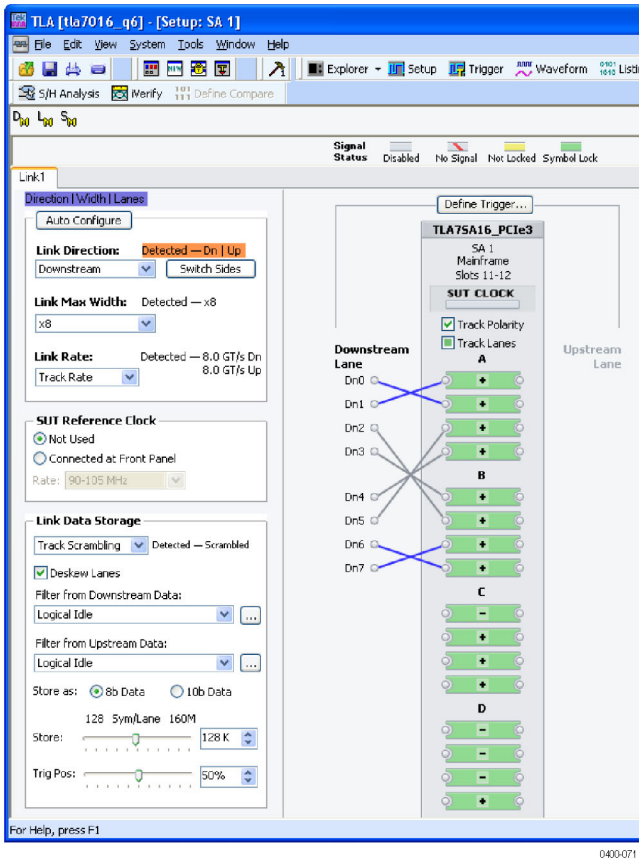


Figure 20: Setup window with changes from auto configuration

Any change from the auto configuration activates the Auto Configure button. To return the system to the auto-configured state, click the Auto Configure button or manually change the controls to their auto-configured states.

Link Rate controls

By default, when the TLA application starts, or when you reset the Auto Configuration (by clicking the Auto Configure button), the Link Rate selection is set to Track Rate. The actual detected rate is displayed adjacent to the Link Rate drop-down list. The detected rate may show rates in both the up and down direction.

If you select a specific link rate, the system displays the detected values. If the detected values differ from the selected link rate, the detected values are highlighted.

If the Link Rate is set to Track Rate, the system can report back a mixed value for one or both of the link directions. This is an error condition and the detected link rate values are highlighted.

NOTE. *If the Link Rate is set to Track Rate and the link trains down from 8.0 GT/s to a slower rate, the logic protocol module returns to the last known rate. For example, a rate change from 5.0 GT/s to 8.0 GT/s and back to 5.0 GT/s operates correctly. However, a change from 5.0 GT/s to 8.0 GTS/s and then down to 2.5 GT/s will fail.*

NOTE. *The TLA7SA08 & TLA7SA16 Logic Protocol Analyzers do not support the capture of Compliance State when using the 8.0 GT/s rate.*

SUT Reference clock

In Auto Configuration, the logic protocol analyzer can recognize a clock signal by recovering the clock signal embedded in the data. The SUT Reference clock is set to **Not Used**. A stable reference signal is generated by the logic protocol analyzer and synchronizes with the embedded clock signal. A clock cable connection is not required, since the logic protocol analyzer recognizes the embedded signal from the probe.

To use an external clock signal, Tektronix recommends connecting a clock cable to make sure that data is accurately synchronized with the clock signal. Select an approximate frequency for your application. Make sure the reference clock cable is connected correctly. (See page 20, *Connect the clock cable*.)

Descramble and deskew

In the Auto Configuration mode, the logic protocol analyzer tracks the scrambling setting of the link. To change the scrambling, select one of the other entries; the instrument senses the change and highlights the changed area. The following guidelines provide information when you should select items in the Link Data Storage area:

- Select **Descramble** to store data in a descrambled format.
- Select **Store as 10b Data** to store data in 10b format.
- Select **Store as 8b Data** to store data in the more conventional 8b data format.
- Select **Deskew Lanes** to view time-aligned lane data in the listing window.

Defining a data filter

The Setup window provides a means of filtering data to focus on the data you are interested in. Select a predefined data filter from the list, or click  (Define Filter button) and select what you want to filter from the data stream. Click OK when done.

Maximum Idle Time detector

When the logic protocol analyzer is auto configured and an electrical idle occurs longer than the specified timeout, the instrument switches the acquisition rate to 2.5 GT/s.

Some applications return to an electrical idle after a preset time period. The circuits should have returned from an L1 state within that time-out period. However, some tests might require a longer time-out setting. You may want to limit the idle time by checking the Limit Idle Time check box and by specifying a set time.

Assigning lanes

In the center of the Setup window, the graphic representation of the logic protocol analyzer module shows the channel-lane connectors (lines drawn between numbered lanes and channels depending on the number of lanes in use). A line connects each signal to a lane so that data will be recorded and displayed properly in the data windows. Unless all connected indicators are green, the logic protocol analyzer will not be able to identify packet structures correctly.

When you first open the Setup window, or default the module, the channels and lanes are already connected to support the default settings for the attached probes. The instrument is auto configured and automatically tracks the status of the lanes (as indicated by the Track Lanes drop-down box). As soon as the system senses any training sequences, it updates the lines (if necessary) to match the mapping reported by the probe. The lines in the Setup window appear as gray lines (system assigned).

To manually change the channel-lane indicators, click and drag the lines so that the signals are connected to the lanes as your design dictates. The Track Lanes check box changes its state depending on connections (mixed connections or all manual connections).

If you decide to manually configure the module, the color of the lines appear in a different color to indicate the change. The following table shows the different color possibilities.

Table 19: Channel-lane connector colors

Channel-lane connector	Description
	System assigned channel-lane connectors
	Manually assigned lines channel-lane connectors

In the following illustration, the connections are limited to the downstream direction. (See Figure 21 on page 46.) In this example the lines from Dn 2, Dn 3, Dn 4, and Dn 5 are system assigned, indicated by the gray lines. The lines from Dn 0, Dn 1, Dn 6, and Dn 7 are were manually drawn as indicated by the darker colored lines.

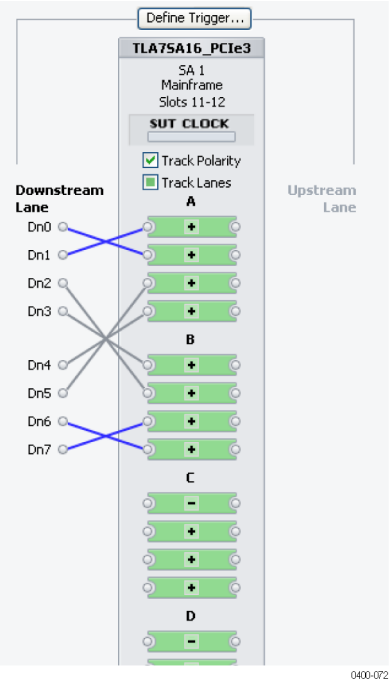


Figure 21: Changes from the default channel-lane connections

Multimodule configurations

If your system has two logic protocol analyzer modules, each set up as unidirectional modules, the system automatically establishes them as a bidirectional pair. If your system contains more than two logic protocol analyzer modules and all are set up as unidirectional modules, additional controls appear in the Setup window to allow you manually assign the pairs of modules comprising the bidirectional link. (See Figure 22.)

Select **Track Rate** to allow the two unidirectional modules to track the rates and widths together.

Select the module from the drop-down list. For convenience, click **Setup** to open the Setup window associated with the selected module.

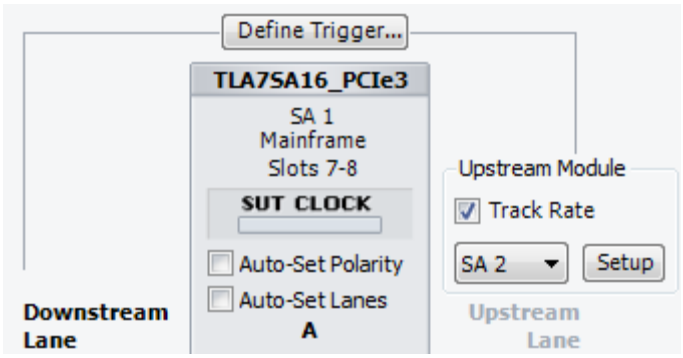


Figure 22: Setup window with multimodule configuration

Probe calibration

When working with high-speed serial analysis, probes attached to the instrument should be calibrated to the logic protocol analyzer and to the SUT. The Setup window includes a Calibration Dashboard on the right side of window to quickly show the status of the probe calibration.

For systems operating with PCI Express 3 rates, a partially filled-in dashboard or a dashboard with highlighted information indicates that calibration is required. A common example showing when calibration is required is during an initial setup.

NOTE. *Systems operating with PCI Express 1 or PCI Express 2 rates will not require calibration.*

The following illustration shows an example of the dashboard for a PCI Express 3 system with an initial setup. Note the missing information in the dashboard.

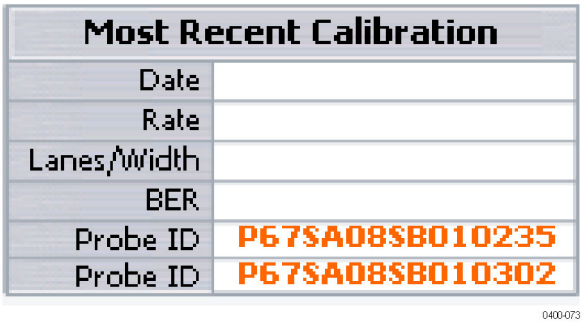


Figure 23: Calibration dashboard, initial setup

When the dashboard displays the calibration information without any highlighting, the probes are calibrated. (See Figure 24 on page 48.)

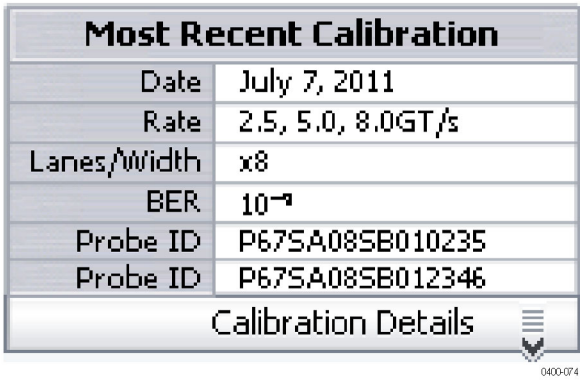


Figure 24: Calibration dashboard, calibrated system

When the system detects information in the dashboard that is different from the previous setup, the dashboard uses highlighting to show that calibration is needed.

Reasons for calibrating or recalibrating the probes include the following:

- The initial use of the system. Calibration is needed because the dashboard contains missing information.
- The instrument detects a rate different than the most recent calibration value. The rate information is highlighted in the dashboard.
- The instrument detects a width or series of widths wider than the most recent calibration value. If the current lane mapping differs from the prior calibration, the information is highlighted in the dashboard..
- Improving the calibration to achieve a lower bit error rate (BER). A highlighted BER indicates that either the calibration was stopped before reaching the desired target BER, of that the system could not achieve the desired BER. The initial calibration might be good enough to start; but further debugging may require a better error rate.
- Adding a new probe (one or two entries in the dashboard). The Probe ID information is highlighted when the instrument detects a different probe ID than the ID than the most recent calibration value.
- Returning to an existing setup with a new SUT. Relocating the instrument and probes from one location to another will require confirming that the module and probes are calibrated to the new SUT.

Calibrate the probes

When the instrument senses any changes from the most recent values used for calibration, the dashboard highlights the changed elements.

Perform the following steps to calibrate the probes:

1. Click **Calibration Details** at the bottom of the dashboard to view and access the calibration options.

   A drawer opens showing the status of the current probe calibration. A status message at the top of the drawer provides an estimate of the time required to calibrate the probes. Other information includes the Gain setting of each probe and a list of the calibration results for each lane.

   The Calibrate button is labeled **Calibrate** whenever a calibration is required. The label changes to **Recalibrate** after a successful calibration.

2. Click **Calibrate** to begin the probe calibration. The probe calibration may take several minutes to complete.

During the calibration process, status messages and a progress bar shows the progress of the calibration. When the calibration is complete, the results are updated in the Calibration Results table.

3. If necessary, click **Cancel** to terminate the calibration.

   If the system has completed part of the calibration process, the button label displays **Stop**. Stopping the calibration will not remove any of the calibration that has been successfully completed. Clicking **Cancel** returns the calibration process to the same state as when the calibration started.

Calibration Results table overview

The Calibration Results table provides a summary of the probe calibration status. The probe calibration process includes the following stages:

- The initial determination stage
- One or more refinement stages

The system displays a progress bar at the top of the Probe Calibration Results table showing the progress of the calibration.

The Calibration Results table displays a row for each lane associated with a probe channel. For example, a x4 system will only display four lanes in each direction; the remaining rows will be blank. The table includes the following columns:

- Selection check boxes. These check boxes allow you to calibrate or recalibrate individual lanes. This is helpful to achieve a better error rate for specific lanes.
- Lane label. The Lane label defines the lane number and the direction (Up or Down).
- Equalization value. This value will most likely vary from lane to lane to achieve the lowest possible error rate.
- Bit Error Rate (~BER). The table lists the BER value achieved during the calibration. A value of **?** indicates that a BER has not yet been calculated. During the calibration, the BER value displays as **- -**. The dashes are replaced by an actual value when the calibration has been completed. If the BER is not sufficient, it might be possible to recalibrate the lane to achieve a better value. Select the lanes to be calibrated and confirm that the Target BER has been set to the desired value. Click **Calibrate** to adjust the EQ only for the selected lanes.

Probe recalibration information

Under certain situations, you might have to recalibrate the probes due to changes to the lane mapping.

Reasons for recalibrating probes are listed below:

- The module has been defaulted. The system might be able to restore the lane mapping associated with the defaulted module. However, if the lane mapping cannot be restored, calibration is required.
- A saved system has been loaded. If the saved system configuration is different from the current probe or module lane mapping, calibration might be required. The system offers a choice of waiting to see if the system can update the lane mapping (based on the observed training set) or overwriting the current lane mapping with the lane mapping saved with the calibration. In the latter case, the system displays a Map Lanes button in the Calibration Status area. Click **Map Lanes** to use the lanes saved with the calibration.
- Lane mapping has changed. When the lane mapping changes to use a new probe channel, the system will need to be recalibrated. (If the lanes are remapped to probe channels that had already been calibrated, recalibration will not be required.) If the SUT has changed its lane mapping since the logic protocol analyzer was calibrated, such that new probe channels are needed, recalibration is required. The system senses the change and displays a message that recalibration is required.

Trigger window

After defining parameters in the Setup window, define a trigger that tells the logic protocol analyzer when to begin recording data. The logic protocol analyzer provides powerful triggering capabilities including predefined trigger templates to specify trigger conditions on any field within a packet.

Open the Trigger window

NOTE. *The instrument has a separate Trigger window for each installed module. Make sure that you select the Trigger window that applies to your module.*

Open the Trigger window by doing one of the following:

- Click the Trigger icon in the TLA Explorer.

  By default the first logic protocol analyzer is identified as SA 1.

- Select the Logic Protocol Analyzer from the Trigger button in the TLA toolbar.
- Click the Trigger button on the Logic Protocol Analyzer icon in the System window.
- Click **Trigger: SA 1** in the Window menu.
- Click **Define Trigger** in the Setup window.

The default Trigger window is shown below. (See Figure 25.)

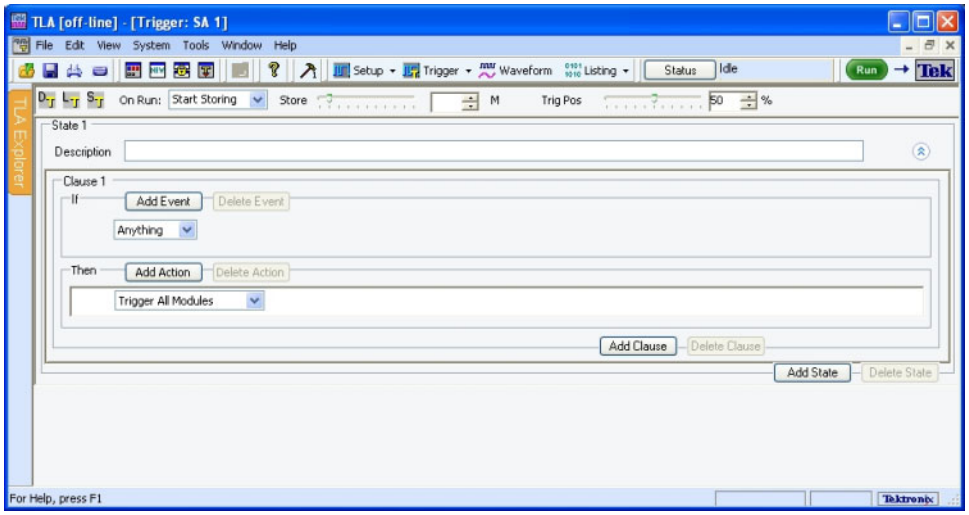


Figure 25: Default Trigger window

Quick tips

- Click to collapse the current trigger state to provide more room on the screen.
- Click to expand the current trigger state.
- Look for the or to expand or collapse information in the current Clause. They are indicators that there may be more or less information to display on screen.
- Click one of the three icons at the top of the Trigger window to open the default trigger window, load a trigger, or save a trigger.
- The Store and Trigger Position controls are identical to those in the Setup window.

Add States, Clauses, Events, and Actions to the Trigger window

A trigger definition is a logical expression consisting of events and actions within clauses, within states. The default Trigger window starts with one state (State 1). and one clause (Clause 1). A trigger definition can have up to eight trigger states with eight trigger clauses per state. To work with states, clauses, events, and actions, do the following:

1. Begin editing the clause by selecting Events (IF) and Actions (THEN).
2. To add additional events or actions to the clause, click Add Event or Add Action.
3. Multiple events can be joined by a logical AND or an OR. Click AND to change it to an OR. Actions can only be joined by an AND.
4. To add another clause or state, click Add Clause or Add State.
5. Add states, clauses, events, and actions by right-clicking and selecting from the context menu.

Delete States, Clauses, Events, and Actions from the Trigger window

Delete states, clauses, events, and actions by clicking the appropriate button in the Trigger window, selecting from the Edit menu, or by right-clicking and selecting from the context menu.

Trigger events

Trigger events are listed in the following table.

Table 20: Trigger events

Event	Description
Anything	Recognizes any data.
TLP	Recognizes the presence or absence of a specific TLP. Choose the TLP from a list, or define a TLP.
DLLP	Recognizes the presence or absence of a specific DLLP. Choose the DLLP from a list, or define a DLLP.
Sequence	Recognizes a specific ordered set or symbol sequence. Choose the Sequence from a list, or define a Sequence.
Link Event	Recognizes link events and link errors. Choose the Link Event from a list, or define a Link Event and specify which lanes to monitor.
Timer	Recognizes a specified timer value.
Counter	Recognizes a specified counter value.
Signal In	Recognizes a signal from another module.

The following table provides additional information about the event recognizer resources. You may need to be aware of these when setting up the Trigger window.

Table 21: Trigger event recognizer resources

Event recognizer	Description
DLLP packet recognizers	4 per link direction
TLP packet recognizers	4 per link direction
Symbol sequence recognizers	4 shared between link directions
Link event recognizers	4 per link direction

Create a TLP event

1. Select **TLP** from the list and specify your TLP.

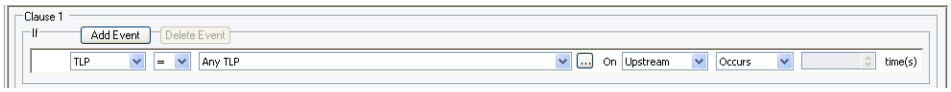


Figure 26: Specifying a TLP event

2. Click the ellipsis to define a more detailed TLP.

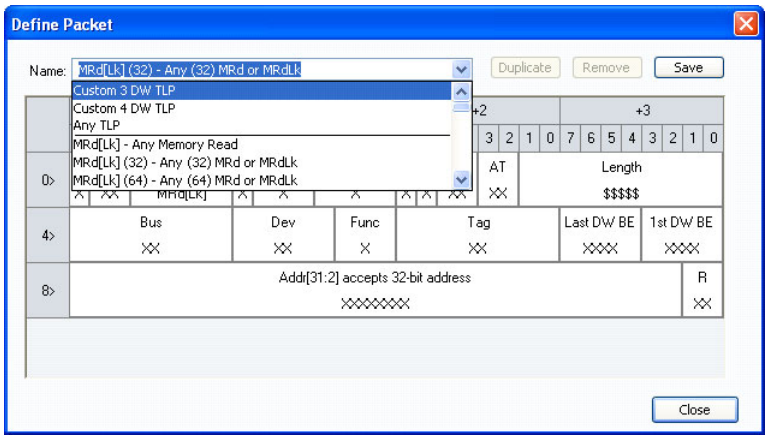


Figure 27: Defining a TLP

3. Enter a meaningful name for the TLP or select one from the list and a copy will be created. To change the radix, right-click and select from the list. Edit the TLP definition and click Close when you are finished. The new TLP will now appear in the list.

Create a DLLP event

1. Select DLLP from the list and specify your DLLP.

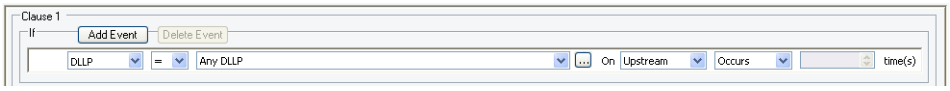


Figure 28: Specifying a DLLP event

2. Click the ellipsis to define a more detailed DLLP.

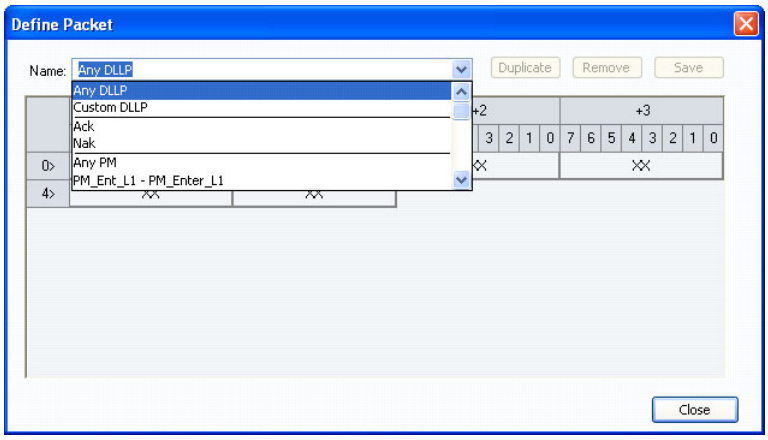


Figure 29: Defining a DLLP

3. Enter a meaningful name for the DLLP or select one from the list and a copy will be created. To change the radix, right-click and select from the list. Edit the DLLP definition and click Close when you are done. The new DLLP will now appear in the list.

Create a Link event

1. Select Link Event from the list and specify your Link event.

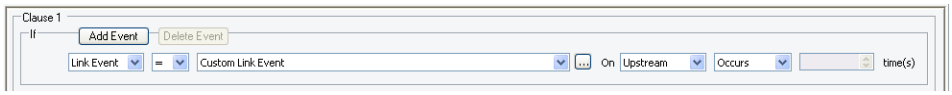


Figure 30: Specifying a Link event

2. Click the ellipsis to define a more detailed Link event.

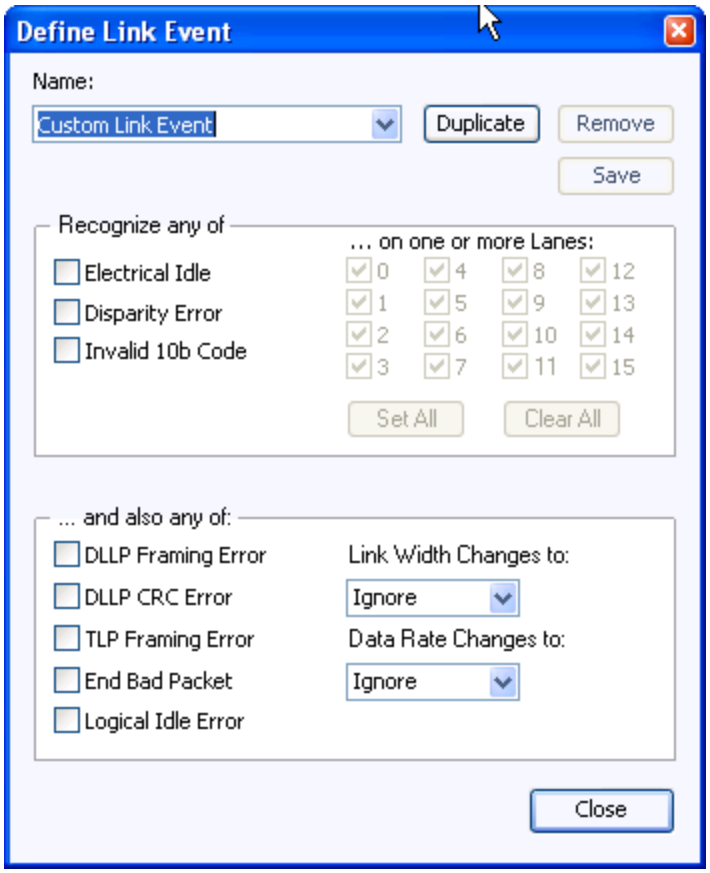


Figure 31: Defining a Link event

3. Enter a meaningful name for the Link event or select one from the list and a copy will be created. Edit the Link event definition and click Close when you are done. The new event will now appear in the list.

Create a Sequence event

1. Select Sequence from the list and specify your symbol sequence or ordered set.

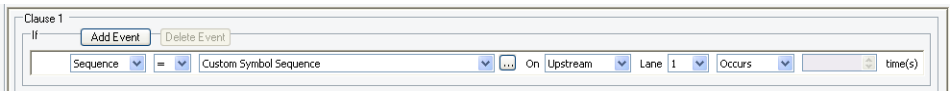


Figure 32: Specifying a symbol sequence

2. Click the ellipsis to define a more detailed symbol sequence.

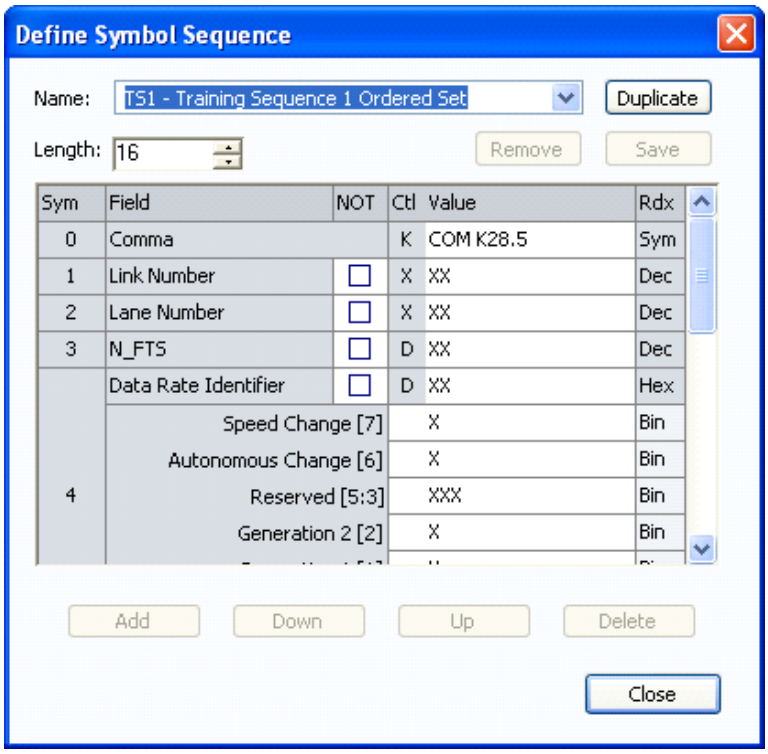


Figure 33: Defining a symbol sequence

3. Enter a meaningful name for the symbol sequence or select one from the list and a copy will be created. Define a symbol sequence with a maximum of 16 symbols per lane. Click the K to change it to a D or an X. An X indicates that the trigger will recognize either a K or a D control bit. To change the radix, right-click and select from the list, or just click the radix text. Edit the symbol sequence definition and click Close when you are done. The new symbol sequence will now appear in the list.

Event Counter, Global Counter, and Timer overview

Four types of events have counters associated with them. The counter will increment every time the event occurs (or does not occur). These counters are called event counters and are associated with the following events:

- TLP
- DLLP
- Sequence
- Link Event

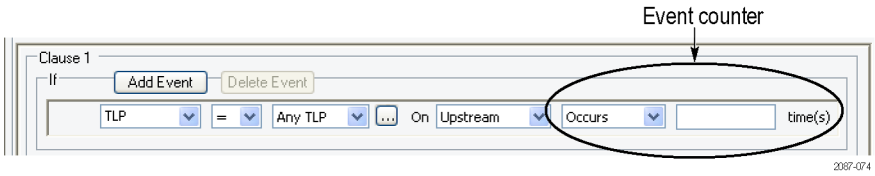


Figure 34: Event counter

There are two event counters in every state. Event counters are limited to counting only the event they are associated with. To create a counter that can be incremented, decremented, and reset by any clause in any state, select Counter from the event list. This type of counter is called a global counter.

There are four counter/timers that may be used as either Global Counters, or Global Timers. A counter/timer can not be used as both a Global Counter and a Global Timer in the same trigger program. Each individual counter timers are independently enabled to be a Global Counter or a Global Timer.

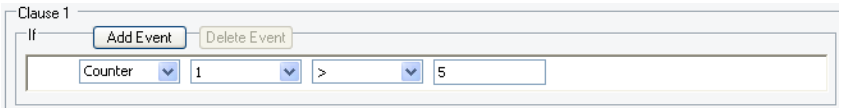


Figure 35: Specifying a global counter

Global counters are usually combined with another clause or state that increments, decrements, or resets the counter with an action. *See Actions.*

Timers are also global, meaning that they can be started, stopped and reset by any clause in any state. Select Timer from the event list and specify your timer.

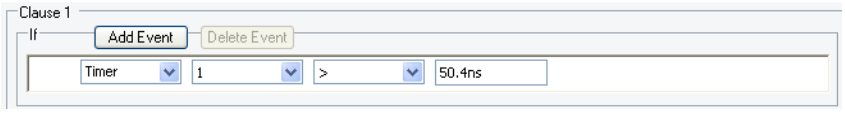


Figure 36: Specifying a timer

Timers are usually combined with another clause or state that starts, stops, or resets the timer with an action. (See page 60, *Trigger actions*.) A maximum of four global counters or timers are available.

Create a Signal-In event

Select Signal In from the event list and specify a signal number.

There are four global signals that can be used for triggering by any module installed in the logic analyzer mainframe.

Trigger actions

When an event (IF) in a clause becomes TRUE, the associated action (THEN) is taken. Click Add Action to join multiple actions with a logical AND.

Trigger Actions are listed in the following table.

Table 22: Trigger actions

Action	Description	Interactions
Trigger	Triggers the current module and causes acquisition memory postfill to begin.	When Trigger is used in the trigger program, Trigger All Modules cannot be used.
Trigger All Modules	Also known as a System trigger. This signal is also available at the System Trigger Out connector.	When Trigger All Modules is used in the trigger program, Trigger cannot be used.
Wait for System Trigger	Used for a module that does not trigger itself or any other module, but waits to be triggered by another module.	Capable of receiving the following three (mutually exclusive) trigger actions: Trigger, Trigger all Modules, or Wait for System Trigger.
Go To	Causes a change to a different trigger state.	Use only one in clause definition.
Counter actions	Increments, decrements, or resets counters.	Counter 1, 2, 3, and 4 actions conflict with Timer 1, 2, 3, and 4 actions respectively. The actions also conflict with their respective events.
Timer actions	Starts, stops, or resets timers.	Counter 1, 2, 3, and 4 actions conflict with Timer 1, 2, 3, and 4 actions respectively. The actions also conflict with their respective events.
Set and Clear Signal	Sets or clears one of the four internal system signals.	Use only one in a trigger program. Mutually exclusive with Arm Module action.
Arm Module	Sends an Arm signal to another module. The other module begins running its trigger program.	Can only arm one module in a trigger program, but actions can be taken throughout the trigger program.
Start and Stop Storing	Begins or ends storing of samples.	
Do Nothing	Used as a placeholder when defining a complicated trigger program.	Does not override other actions specified in a clause.

Acquiring and viewing data

The TLA application software provides predefined setups for the data windows. When you first acquire data, the logic protocol analyzer displays the Transaction window and the Listing window. Based on the Setup window information, all modules with the supported software loaded are identified as participating links.

- Use the Transaction window to locate transactions of interest and to help understand the detailed sequence of the transactions. After locating a transaction of interest, use the Transaction window to further examine the packet sequence, timing, and internal content to confirm any suspected problems.
- Use the Bird's Eye View (BEV) with the Transaction window for a high-level view of the overall acquisition. Configure the BEV to display a visualization for flow control credits and then use the Packet view to identify possible credit overflows.
- Use the Summary Profile window to view a summary statistical analysis of protocol elements within a region and across the entire acquisition.
- Use the Listing window to display columns of disassembled PCI Express symbol data (ordered sets, DLLPs, and TLPs). Each column represents a lane of PCI Express data with a disassembled view of the packet data. This allows you to quickly view symbol data as it flows across the link.
- Use the Waveform window to display rows of symbol data. Each row represents a lane of PCI Express data. Use iView to correlated data from an external Tektronix oscilloscope in the same waveform window.

Use the New Data Window wizard to select and set up other data windows as needed for your application.

NOTE. *If your logic protocol analyzer is configured to acquire multiple protocols, or if the system does not detect any protocols in the setup, the Components and Links dialog box appears on the screen when you attempt to create a new Transaction window. Fill out the necessary fields in the dialog box to associate the links captured by the logic protocol analyzer to the Transaction window.*

Transaction window

The Transaction window provides a display of packet information, colored by packet type, to view transactions and overall packet flow, interspersed with physical layer activity (such as ordered sets) to gain an understanding of traffic flows within your system.

The Transaction window has elements similar to other data windows such as the toolbar to search data, apply filters, and manage other aspects of the display. The following illustration shows some of the key elements in the Transaction window.

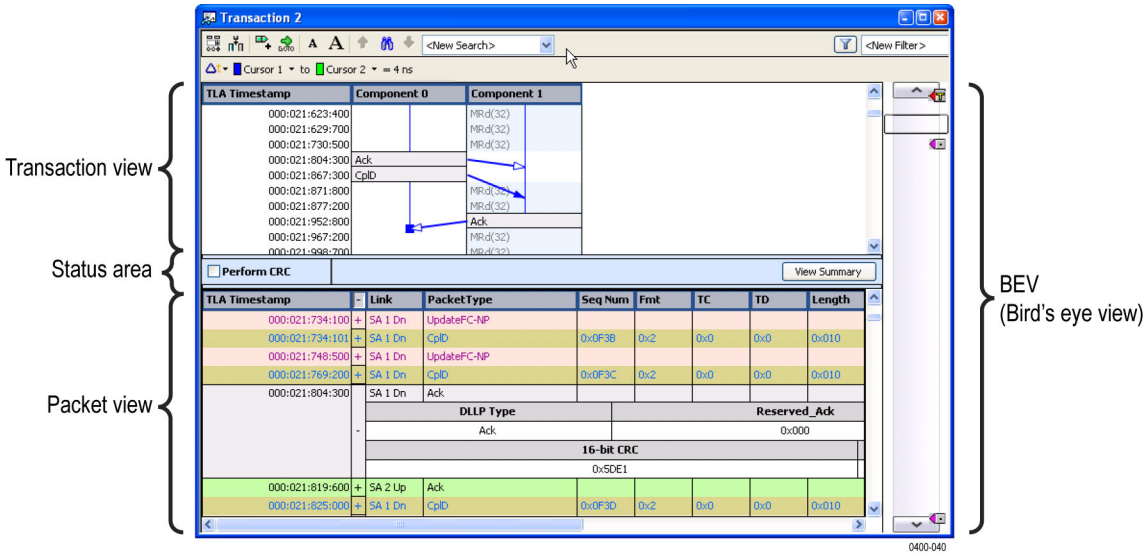


Figure 37: Transaction window

Transaction view

Links are represented as relationships between the end point columns.

Click a transaction to show the link relationship by displaying a Feynman diagram. (See page 64, *Examining transactions*.)

Quick tip

- Use the mouse with rollover messages to show the amount of time required for the transaction or to identify errors in the transaction.

Status area

The status area separates the Transaction and Packet views in the Transaction window. It provides additional information about the status of the Transaction window including the following items:

- Status messages and error messages as they occur
- A progress bar showing the status of searches and filtering taking longer than two seconds
- A statistics panel showing the statistics from the BEV Viewfinder.
- Access to the Summary Profile window through the Display Summary button. (See page 71, *Summary Statistics Tab Notebook information*.)

Packet view

The Packet view shows the primary source of information in the Transaction window. All acquired packets are interleaved in the timestamp followed by the source (transmitter) ID. Packets come in different sizes and transmit in varying amounts of time.

The columns in the Packet view show information from the fields available to the packet. To add or remove columns, right-click the mouse and select **Add/Remove Columns** from the context menu; add or delete columns from the Field Chooser menu.

Each major row in the Packet view represents a packet. Click the + sign to expand the fields to see more packet information. Minor rows in the Packet view show low-level information such as ordered sets and error conditions. A special type of row is associated with Training Sets. Neither a packet, nor a single phy-layer indication, Training Set rows show information about the current state of the link.

Coloring provides a way to differentiate packets, such as Memory Reads, Memory Writes, ACK, NACK, message types and special events (ordered sets with data, symbolic ordered sets, and errors.

Quick tips

- Position the mouse over special events to display rollover messages with additional information about the event.
- Position the mouse over Training Set fields to display rollover messages with additional information about the field value.
- Reduce the packet rows to a few pixels high to only display the color bands without the detailed text labels by continuing to select **Smaller Text** from the right-click menu. This provides an easy way view more data in the window.

Examining transactions

Click a transaction to see the packets that make up the transaction. Other packets involved in the transaction are added to the appropriate columns and are highlighted. Click the transaction a second time to remove the highlighting.

All packets related by the transaction are highlighted and have arrows drawn from them to their ultimate delivery time; all other packets are attenuated with grayed-out text. Ends of the arrows indicate when a packet has fully arrived; position the mouse on the arrow to show amount of time between packets.

NOTE. *Because packets do not flow across links instantly, abnormally long or short transmission times can indicate the source of a problem. Use the timestamp to indicate when the packet left the sending component.*

If the target row does not display (is filtered out) the arrow is drawn to the top of the nearest visible and appropriate timestamp row. The arrowhead is rendered with a colored border with a white fill. The last line for the last packet to complete is shown by a square-end cap; it indicates there are no more packets in the current transaction.

A vertical line indicates how long the component was involved with the transaction after it received the first packet.

Physical Layer view

The Packet view shows Physical layer information in addition to the packet information. Use the Packet view to look for errors and gaps due to hardware filtering or to identify other problems in the Physical layer. The interleaving of the physical information with the packet information can help in identifying elements of interest.

Special events are identified as information events, ordered sets, or error messages. These events may be displayed as horizontal lines starting in the left side of the Packet view. Each line has a different appearance; use the rollover messages with the mouse to provide more information about the special events.

Using the Transaction window with the Listing window

Use the Transaction window and Listing window together to trace problems from the Transaction window by locking cursor 1 to the same data in the Listing window. By default, the system positions the windows side-by-side to view activity in both windows at the same time.

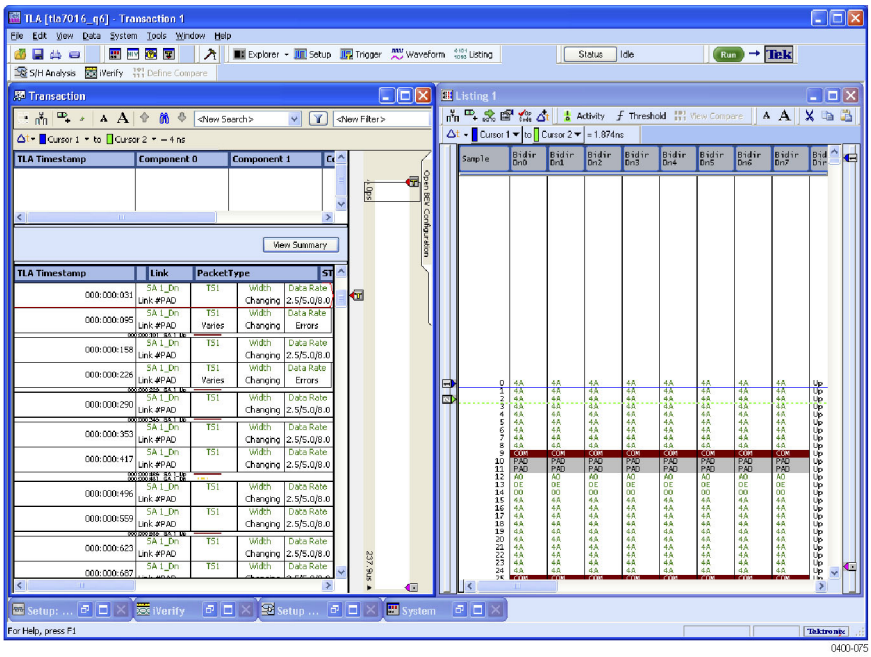


Figure 38: Side-by-side Transaction window and Listing window

Find a link rate change because of new sets of training information (moving from TS1 to TS2). Look for the relative lane data in the Listing window to identify the rate change. Then look for additional information in the Listing window to see the lane data to identify what is going on.

Bird’s Eye view

The Bird’s Eye View (BEV) displays Flow Control across the entire acquisition. When you identify an area of interest, such as a possible buffer overflow, use the BEV to navigate to the data and view the details of the transactions in the Transaction window. (See Figure 39.)

Updating information in the BEV might take a few moments or longer, depending on the amount of data that needs to be updated.

Use the BEV Configuration panel to configure the properties of the Flow Control visualization. (See page 69, *Configure the Flow Control visualization*.)

Viewfinder

Use the Viewfinder to move to areas of interest within the BEV. The system updates statistics about the data within the Viewfinder region and displays them in the Status area of the Transaction window. The displayed statistics depend on the visualizations displayed in the BEV.

NOTE. *Changing the position or the size of the Viewfinder in the Transaction window changes the position and size of the Viewfinder in the Summary Profile window.*

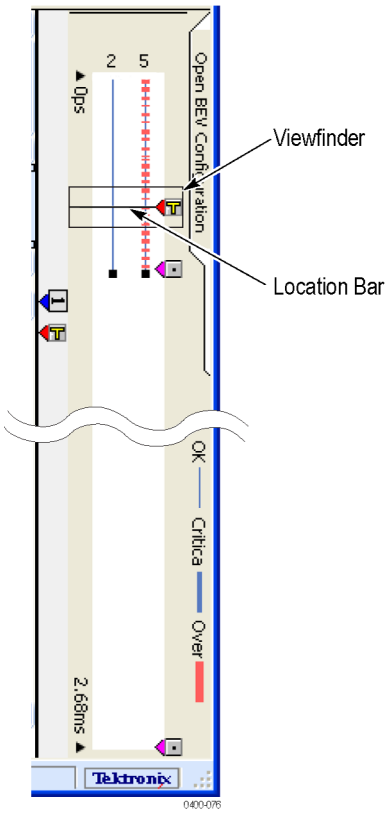


Figure 39: BEV with viewfinder and location bar

Location bar

The Location bar represents the current location of the first packet in the Packet view. Change the position of the Location bar in the BEV using one of the following methods:

- Drag the Location bar to a new location within the BEV. The Packet and Transaction views are updated with new data for that position.
- Click on any location within the BEV. The Packet and Transaction view positions are updated to show the first element associated with the Location bar position.
- Scroll the data in the Packet or Transaction views. The Location bar moves to the new location in the BEV.

The Location Bar and the Viewfinder operate independently– moving the Location Bar does not impact the position of the Viewfinder. To move both the Location Bar and the Viewfinder simultaneously, use the Alt key with the mouse as described in the on-screen rollover messages.

Flow Control visualization overview

The Flow Control visualization displays a graphical representation of Flow Control Credits. The BEV displays up to six Flow Control graphs where each is a vertical line showing the Flow Control activity.

Use the BEV Configuration panel to define the credit values to display with each line. For a given time slice, the line displays the absolute maximum value for the union of elements as specified in the configuration panel. For example, if you specified all data values in the up direction, the line would identify the absolute maximum value of all data values within the time slice. The line represents the following ranges of values:

- Okay. The Okay range is any range of values below the Critical threshold value.
- Critical. The Critical range is arbitrarily set by the application to be 80% of the Overflow threshold.
- Overflow. The Overflow range is determined by the threshold value that you set in the BEV Configuration panel. Setting the Overflow threshold adjusts the sensitivity of the visualization to errors. Setting the threshold to a low value will render errors more frequently. Setting the thresholds to a value greater than 100% decreases the potential for showing errors.

When you notice an area of interest in the visualization, move the Location bar to that location and see the resultant data in the Packet and Transaction views.

Quick Tip

- Move the mouse over one of the Overflow ranges in the BEV to display a rollover message that provides information for the highest three overflow values.

Configure the Flow Control visualization

1. Click the Configure BEV tab at the top-right side of the BEV to open the BEV Configuration panel. The panel shows the options for the Flow Control visualization. (See Figure 40.)

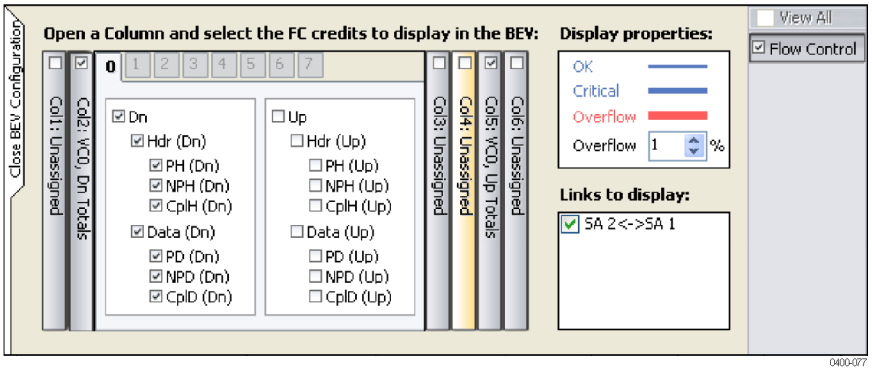


Figure 40: BEV Configuration panel with Flow Control selected

2. Select the links to display by clicking the check box under the Links to Display area; clear the check box for any links that you do not want to display.

NOTE. *Any unidirectional links are disabled and cannot be displayed in the BEV.*

Each differential in the BEV is represented by a Column button in the BEV Configuration panel. Rearrange the Column buttons by clicking and dragging the column to the desired position.

3. Determine the differentials to display in the BEV by clicking the check box at the top of the column.
4. Click a Column button to open a drawer showing the virtual channels and credits to display in the BEV.

   Tabs within each column allow you to select the virtual channels to display.
5. Select a Virtual Channel tab and then select the individual credits to display by clicking the check boxes in the panel.

   The label on the Column button summarizes the credits for that column.

Flow Control statistics

Move the Viewfinder to any data of interest. The Statistics panel in the Status area of the Transaction window shows the minimum values for the differential within the bounds of the Viewfinder. Values are hyperlinks; click a hyperlink to go to the first instance of that value in the Transaction window.

Summary Profile window

Use the Summary Profile window to view a summary statistical analysis of protocol elements within a region and across the entire acquisition. The window provides real-time statistics without the need to take a separate acquisition to view the overall health of your system. Summary information includes statistical analysis of the trace elements such as:

- TLPs
- DLLPs
- Ordered sets
- Errors
- Custom

A Summary Profile window is associated with one or more Transaction widows for any one protocol. To view the Summary Profile window, click the **Display Summary** button on the status bar of the Transaction window.

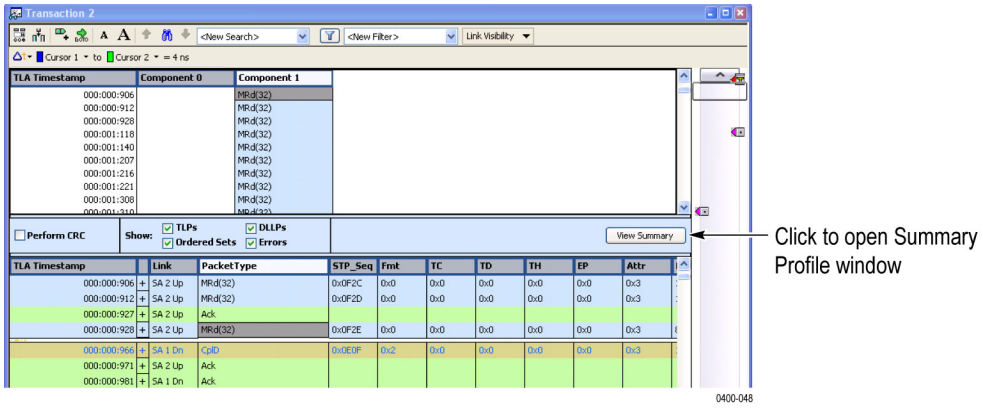


Figure 41: Opening the Summary Profile window

The following illustration shows the major components of the Summary Profile window.

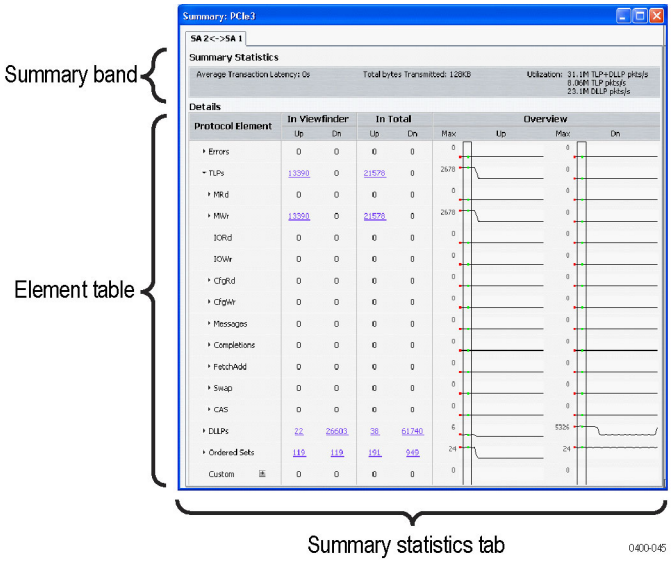


Figure 42: Summary Profile window

Summary Statistics Tab Notebook information

The Summary Statistics Tab Notebook contains a collection of the summary statistics. The tabs identify the individual links or copies of the links with an associated Transaction window instance. Each tab contains a list of protocol elements and a list of the totals of elements in the Viewfinder regions in the overall acquisition.

The summary band at the top of each tab provides a brief summary of the statistics for the selected link including the average transaction latency, the total bytes transmitted, and the total bandwidth utilization.

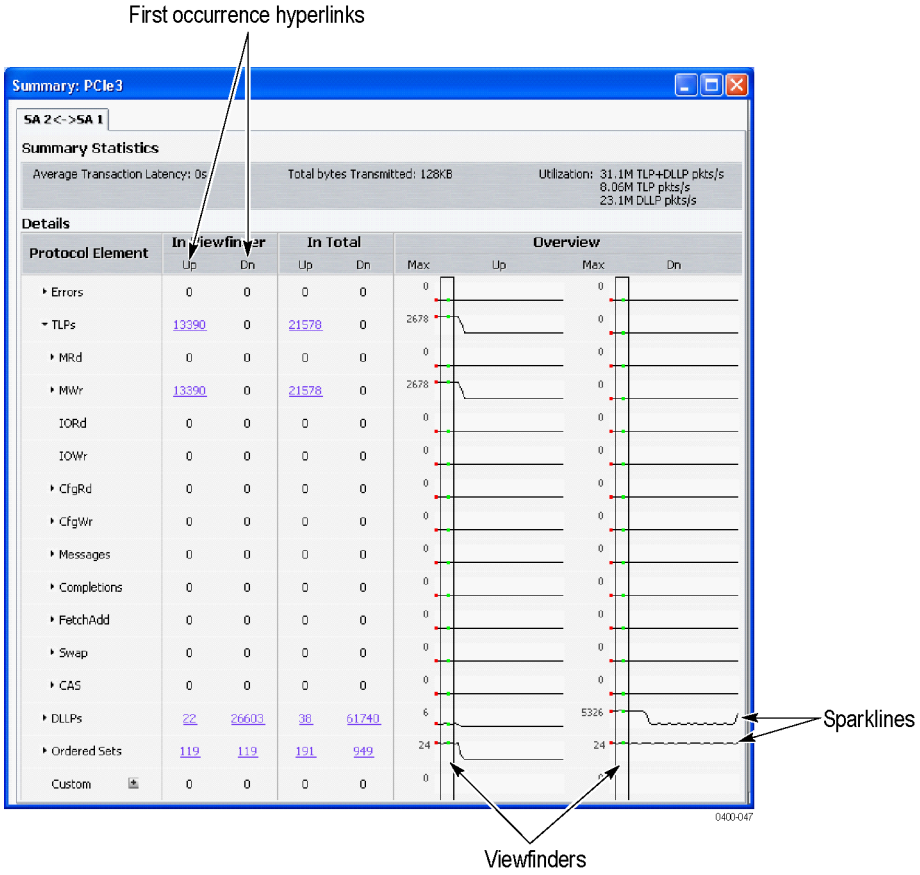


Figure 43: Summary Profile window (Summary Statistics Tab Notebook)

Element Table information

The Element table contains the following items:

- Protocol Element. This column lists the hierarchy of the elements in the protocol. Click the arrow to display any sub-elements and the details for those elements. The column may contain filtered items (in italics) that represent items not displayed in the Transaction window because of post-processing filtering. Click elements with hyperlinks to scroll the associated Transaction window to the first instance of the element.
- The In Viewfinder columns list the totals of each element within the Viewfinder regions. Click an item a Viewfinder column to scroll to the first occurrence of the corresponding item in the Transaction window. (See Figure 43.)

- The In Total column lists the grand totals of each element in the entire acquisition. Click an item in the column to scroll to the first occurrence of the corresponding item in the Transaction window.
- The Overview column contains a summary of each element in the acquisition including the following items:
  - Viewfinder. The Viewfinder specifies an area within the sparklines that looks interesting. This is the same area displayed by the Viewfinder in the BEV in the Transaction window. Changing the Viewfinder updates the statistics under In Viewfinder columns. Click the updated hyperlink to go to the first instance (in the Transaction window) on an element in the Viewfinder region.

NOTE. *Changing the position or the size of the Viewfinder in the Summary Profile window changes the position and size of the Viewfinder in the BEV.*

  - Sparklines, a summary of the entire trace data for each element broken into segments (approximately 40 discrete sections over the entire trace). The horizontal (X) dimension is each segment; the vertical (Y) dimension depends on the maximum value of the element and which root element the sparkline is part of.

Create a Custom element

Use the Custom element to establish user-defined protocol elements for which the Summary Profile window will provide appropriate statistics. The Custom element does not create a new packet type, but provides a means to specify a set of values for the fields of a packet that may or may not correspond to an existing packet definition.

1. Click the button next to the Custom element to open the Define Packet window.
2. Select one of the default packet types from the Name list. (See Figure 44.)

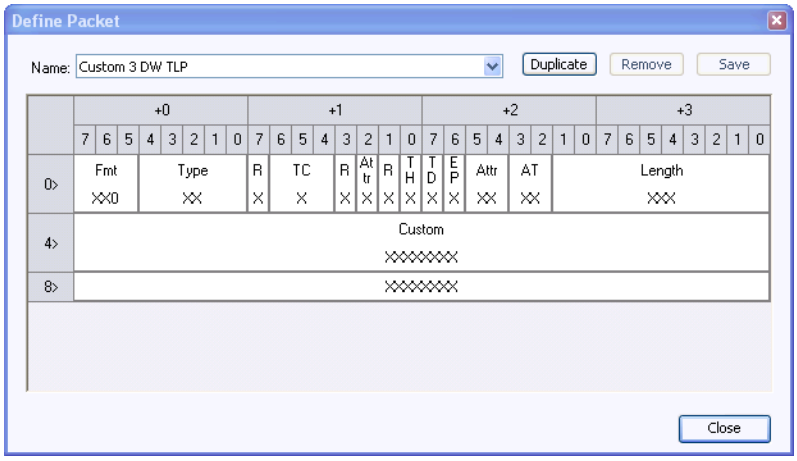


Figure 44: Define Packet window for a Custom element in the Summary Profile window

3. Enter a name for the packet and then change the values of the fields for your needs.
4. Save the Custom element by clicking **Save**. The new element is added to the Protocol Element list.

Guidelines for using Custom elements are listed below:

- DLLPs start with an SDP and complete with an End or EDB with mod4 lane starts and a maximum of two SDP per symbol times.
- TLPs start with SDP and finish with an End or EDB with mod4 lane starts and a maximum of one STP per symbol time.
- The maximum packet sizes are defined by Max_Payload_Size.

Listing window

Use the Listing window with the Transaction window and Summary Profile window to display disassembled data in a list format; packets appear in searchable columns.

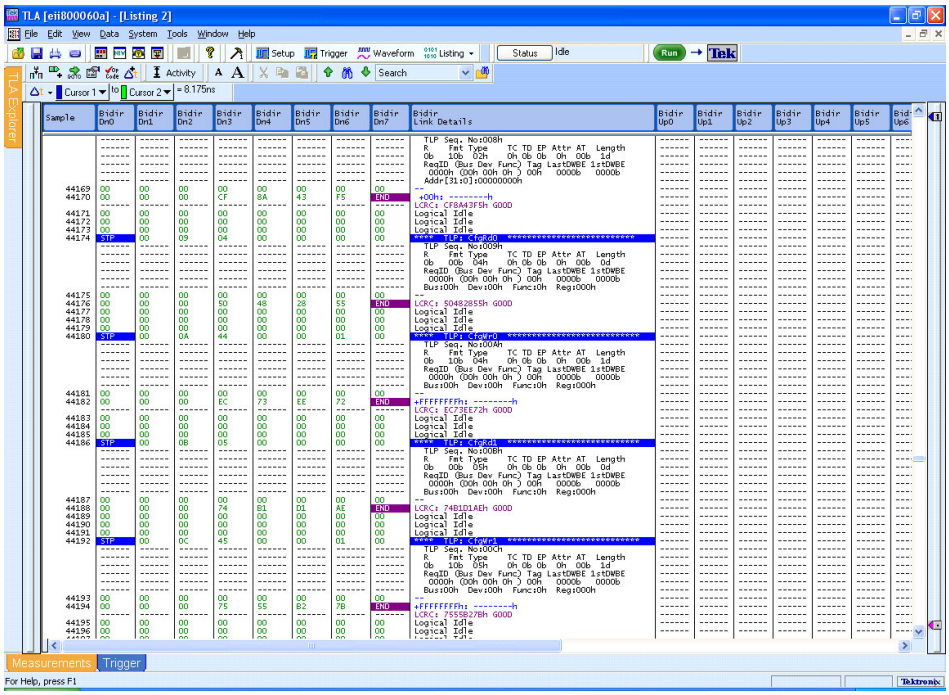


Figure 45: Data displayed in the Listing window

The Listing window displays special characters and strings to indicate significant events. (See Table 23.) The columns that display in the Listing window depend on the Acquire settings in the Setup window.

Table 23: Special characters in the Listing window

Character or string	Description
>	Insufficient room on the screen to show all available data
- -	Invalid data or group, including read data

Add two sides of a link to a single Listing window

If you are using two logic protocol analyzer modules and one is connected to the upstream side of a link and the other module is connected to the downstream side, display both sides of the link in a single listing window. To do this, complete the following steps:

1. Select New Data Window from the Window menu to start the New Data Window wizard.
2. Click Listing and then Click OK.
3. Press the Ctrl key on your keyboard and select the two modules from the Data from list.

   Both modules should be selected in the wizard.
4. Click Next >.
5. Enter a name for the new Listing window and then click Finish.

   The wizard will close and display the data from both modules in the new listing window.
6. If necessary, edit the window by adding or moving columns to display the data that you are interested in.

Change the data display in the listing or Waveform windows

The logic protocol analyzer provides different ways for viewing data in Listing and Waveform windows. Change the display settings in the properties pages of either display window:

1. Click the Properties icon  in either display window to open the property pages for the respective display.
2. Click the Disassembly tab to select the Disassembly property page.
3. Change the display items as needed.

The following table lists some of the display settings that you can change in the Listing window.

Table 24: Logic protocol analyzer disassembly display options

Disassembly property page selections	Settings	Description
Show	All (default)	All required data is disassembled and shown including logical idle samples
	Non-Idle Samples	Logical idle samples are hidden
	TLP/DLLPs Only	Only samples containing TLPs and DLLPs are shown
	TLPs Only	Only samples containing TLPs are shown
	TLP Headers Only	Only samples containing TLP headers are shown
Highlight	None (default)	Nothing is highlighted
Disassemble Across Gaps	Yes or No (default)	General listing window setting. (not recommended for PCI Express data)

Any errors in link traffic detected by the disassembler are displayed regardless of the display option that you selected.

Bus-specific fields

In the Controls area of the Disassembly property page, select any of the following controls to change the way data is displayed.

Disassemble and display

When working with bidirectional data with a single module, the data window can only disassemble and display either upstream or downstream data. Select the data that you want to view in the Listing window.

Extended Link details

Set the Extended Link Details mode to ON or OFF to show or hide extended packet information in the Listing window. If you set it to OFF, the Link_Details column displays general packet information on a single line. If you set it to ON, the Link_Details column displays extended packet information on multiple lines. All packet fields are decoded and displayed in the Link_Details column. TLP payload data is displayed double word aligned along with the lower word address starting with the address acquired in the TLP header.

Calculate CRC

The disassembler calculates the CRCs for all packets when Calculate CRS is set to ON. If the calculated value differs from the value acquired from the link, an error message is displayed in the Link_Details column. The default setting is OFF.

By default, the field values are aligned with the sample containing the STP if it is a TLP, or with the sample containing the SDP if it is a DLLP. By setting this property to ON, the packet field values are displayed on the same line as the TLP_fmttype and DLLP_type group values.

10-bit mode acquisition

When the logic protocol analyzer is configured to acquire the link in 10-bit mode, the Listing window displays the symbol encoding in the individual lane columns. No further link analysis is performed.

Change from binary listing symbol tables to 10-bit mode

To change the radix of a binary listing symbol table to radix in 10-bit mode acquisition, perform the following steps:

1. Select a column and right-click.
2. Select one of the symbol files from the list, or click **Other** and then navigate to the location of the symbol file.

Disassembler special messages

The disassembler uses special messages to indicate significant events. These messages are highlighted in red in the Link Details column of the listing window. The following tables list the messages and their descriptions.

The special messages are in addition to the errors detected by the logic protocol analyzer hardware listed in the PCIEx_RuleViol.tsf file. The file is located in the C:\Program Files\TLA 700\\Serial\PCIe folder under the Bidir, Uni_Up, or Uni_Dn subfolders.

Table 25: Training sequence messages

Message	Description
Error - Duplicate Lane Number Assignment in Lanes:	More than one lane is assigned the lane number. The lane numbers are listed below the message.
Error - Lanes That Exceed Maximum Link Width:	The lane number as acquired in the training sequence is higher than the link width. The lane numbers are listed below the message.
Lane??: Lane Polarity In	The lane is inverted. Click the center of the polarity indicator (+ or -) in the graphical display in the Setup window to fix the polarity problem.

Table 26: Packet framing messages

Message	Description
Error: Abnormal packet termination	The packet was interrupted and terminated by a skip ordered set, training sequence, or FTS, TLP, DLLP.
Non-Idle Bus	The link is supposed to be in logical idle at this sample, but a nonzero value is found in one or more lanes.

Table 27: DLLP messages

Message	Description
Error reading DLLP	A general error occurred while trying to decode the DLLP. This was possibly caused by a gap/suppression of data.

Table 28: TLP header messages

Message	Description
Error reading TLP	A general error occurred while trying to decode the TLP header, possibly caused by a gap/suppression of data.
Error Forwarding/Poisoned TLP	The EP field of TLP header is HIGH.
Error: Invalid 1stDWBE/Length values for Req TLP	The TLP length field > 1 and First DWBE field is 0 for request TLPs.
Error: Invalid LastDWBE/Length values for Req TLP	The TLP length field is 1 and Last DWBE field is not 0, or TLP length field > 1 and Last DWBE field is 0 for request TLPs.
Zero Length Read Request - Possible Flush	The TLP length field is 1, Last DWBE is 0, First DWBE is 0, for Memory Read Request.

Table 28: TLP header messages (cont.)

Message	Description
Error: Invalid Traffic Class for Message TLP	The TC field was not zero.
Completion Status: + `Unsupported Request', `Config Req Rtry Stat', or `Completer Abort'	A completion status other than `Successful Completion'.
TLP: Msg - + `ERR_COR', `ERR_NONFATAL', or `ERR_FATAL'	An error message TLP was acquired.

Table 29: CRC checking messages

Message	Description
Error: ECRC mismatch	The ECRC value acquired in the TLP digest field does not match the ECRC value calculated by applying the ECRC algorithm to the acquired data. Possible causes include incorrect ECRC at the transmitter, poor signal quality at probe head, different algorithm used between transmitter and software, incorrect polarity or ordering of cables at the input of the logic protocol analyzer, problem with the cables or connection to the logic protocol analyzer.
Error: CRC mismatch	The TLP or DLLP CRC acquired does not match the CRC value calculated by applying the CRC algorithm to the acquired data.

Table 30: General acquisition messages

Message	Description
Error: Missing Data - Gap in TLP header	Complete decode of TLP header was not possible due to a gap or suppression of data
Error: Missing Data - Gap in DLLP	Complete decode of DLLP was not possible due to a gap or suppression of data
Error: Missing Data - Gap in Training Sequence	Complete decode of Training Sequence ordered set was not possible due to a gap or suppression of data
Error: Missing Data - Gap in packet	Complete decode of Training Sequence ordered set was not possible due to a gap or suppression of data
Lane-to-Lane Deskew Error	The link was not properly deskewed by the logic protocol analyzer. Also displayed when the sample contains SKP (K28.0) symbols in one or more lanes but not all lanes of the link. This error message is displayed until a sample containing all SKP (K28.0) symbols is found. No further post processing of packets is performed when the link is not deskewed.

Vendor Defined Message (VDM) support

The TLA7SA08 and TLA7SA16 Logic Protocol Analyzers provide Vendor Defined Message (VDM) support to define and decode vendor-defined packets and fields. Tektronix provides information about VDM support in a file that you use to configure the VDM decoder (PacketFormats_VDM.xml).

Modify the decoder file with the VDM information specific to your system.

The decoder file is available in the following location on your TLA system:

```
C:\Program Files\TLA 700\System\CommonAssemblies\
PacketFormats_VDM.xml
```

Probe dimensions

This section provides information on the dimensions of the P67SAxx probes.

Midbus probe cable dimensions

The following figure shows dimensions of the midbus probe cables. All midbus probes have the same cable lengths. (See Figure 46.)

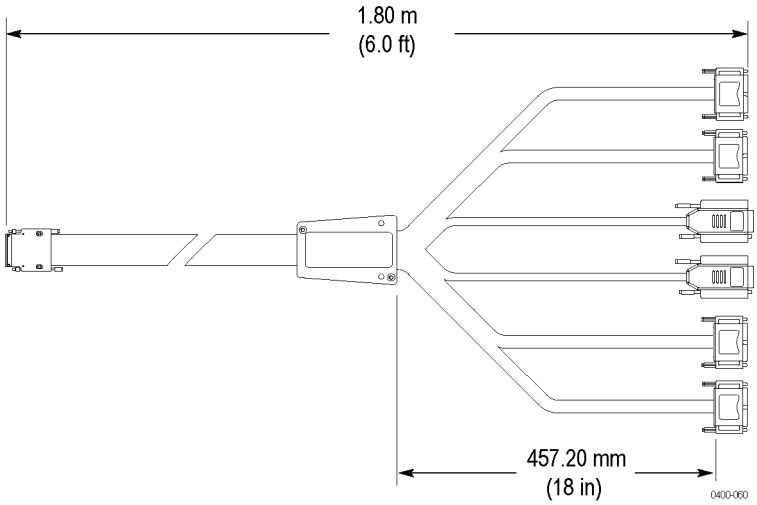


Figure 46: P67SA08, P67SA08G2, P67SA16, and P67SA16G2 cable length dimensions

P67SA08 Midbus probe head dimensions

The following figure shows the dimensions of the P67SA08 midbus probe head. (See Figure 47.) A 3D CAD solid model (pcie_gen3_x4_probe.stp file is attached to the PDF version of this document. (See page 143, *Midbus probe 3D CAD models*.)

NOTE. *3D CAD solid models are included in the electronic files that are attached to the PDF file of this document. To access the attached files, open the PDF file and click on the paperclip icon on the lower-left side of the document viewer.*

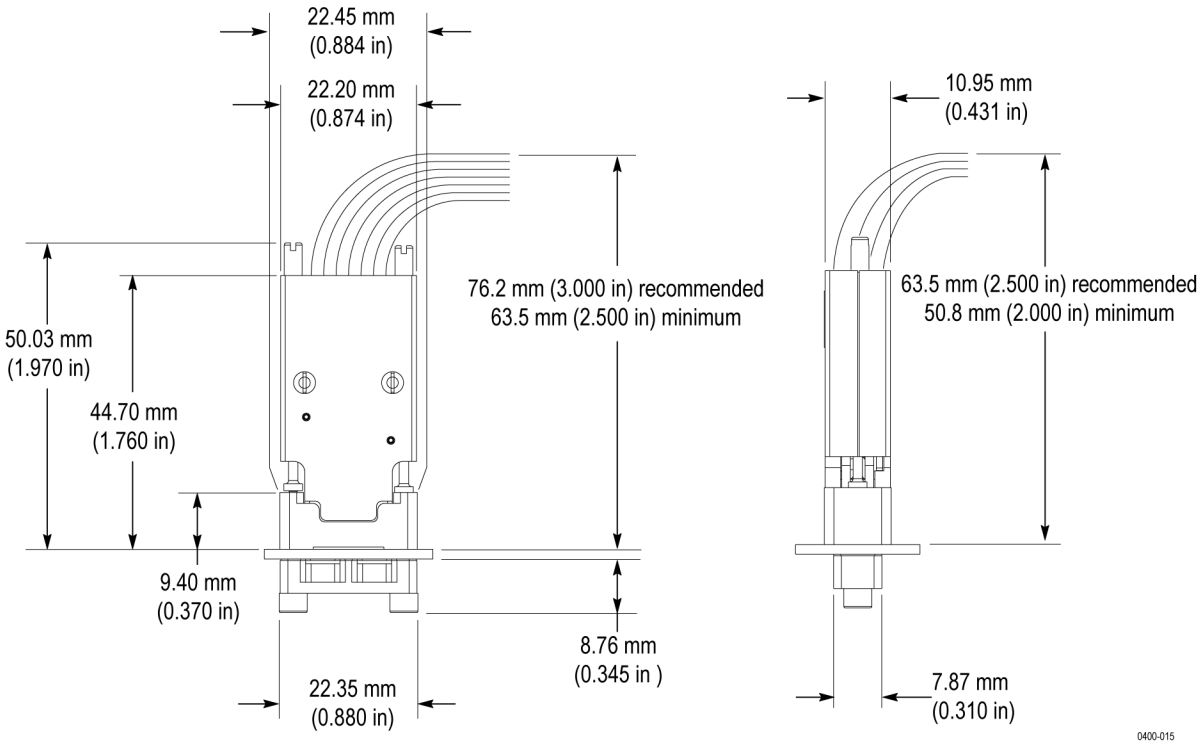


Figure 47: P67SA08 midbus probe head dimensions

P67SA08G2 Midbus probe head dimensions

The following figure shows the dimensions of the P67SA08G2 midbus probe head. (See Figure 48.) A 3D CAD solid model (pcie_p67sa08g2_x4_probe.stp file is attached to the PDF version of this document. (See page 143, *Midbus probe 3D CAD models*.)

NOTE. *3D CAD solid models are included in the electronic files that are attached to the PDF file of this document. To access the attached files, open the PDF file and click on the paperclip icon on the lower-left side of the document viewer.*

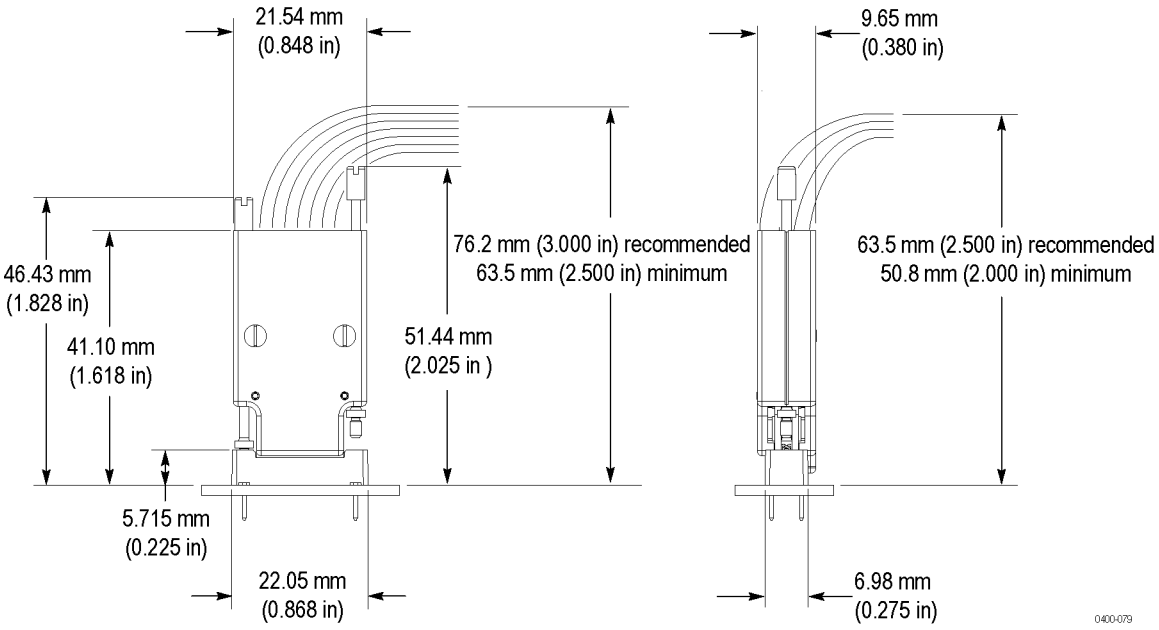


Figure 48: P67SA08G2 midbus probe head dimensions

P67SA16 Midbus probe head dimensions

The following figure shows the dimensions of the P67SA16 midbus probe head. (See Figure 49.) A 3D CAD solid model (pcie_gen3_x8_probe.stp file is attached to the PDF version of this document. (See page 143, *Midbus probe 3D CAD models*.)

NOTE. *3D CAD solid models are included in the electronic files that are attached to the PDF file of this document. To access the attached files, open the PDF file and click on the paperclip icon on the lower-left side of the document viewer.*

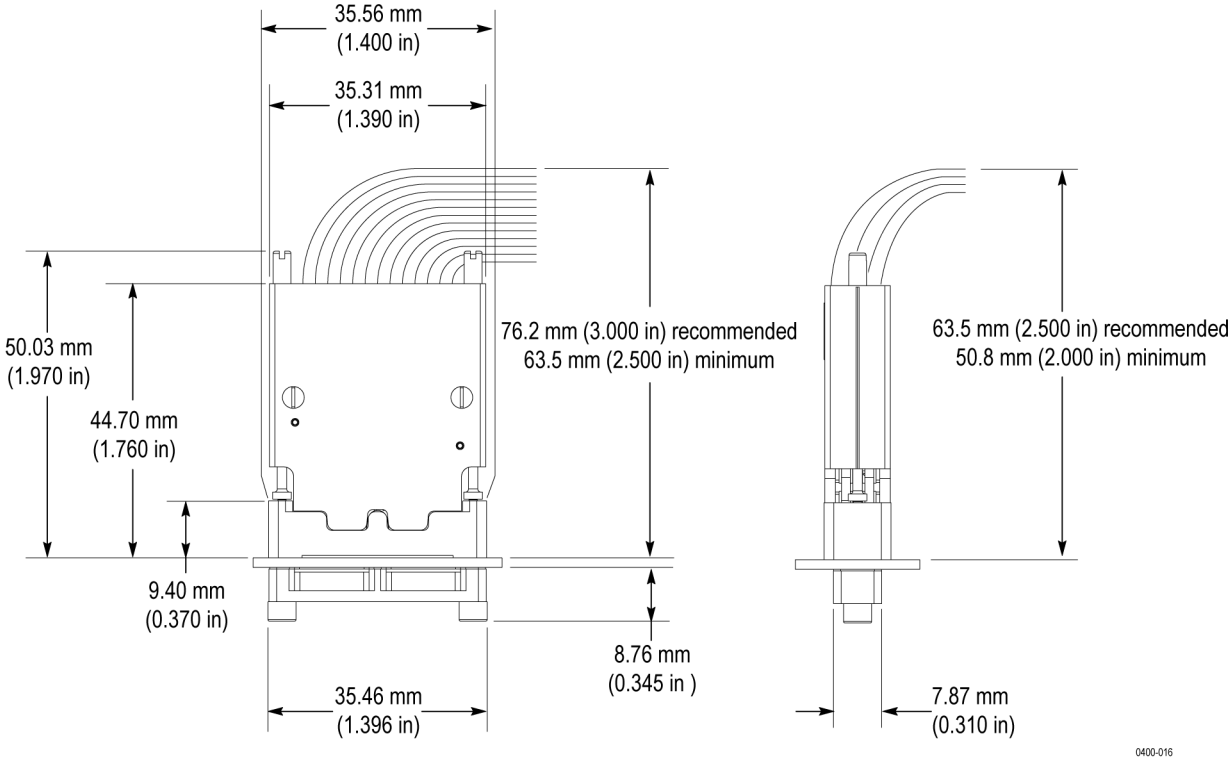


Figure 49: P67SA16 midbus probe head dimensions

P67SA16G2 Midbus probe head dimensions

The following figure shows the dimensions of the P67SA16G2 midbus probe head. (See Figure 50.) A 3D CAD solid model (pcie_p67sa16g2_x8_probe.stp file is attached to the PDF version of this document. (See page 143, *Midbus probe 3D CAD models*.)

NOTE. *3D CAD solid models are included in the electronic files that are attached to the PDF file of this document. To access the attached files, open the PDF file and click on the paperclip icon on the lower-left side of the document viewer.*

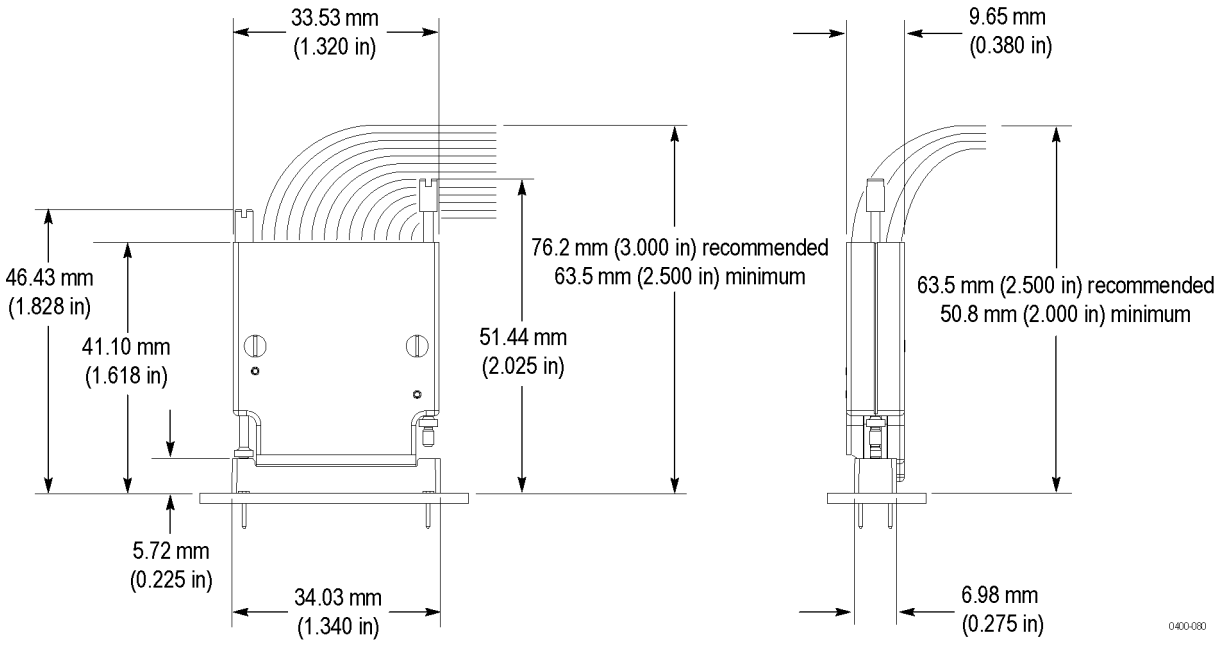


Figure 50: P67SA16G2 midbus probe head dimensions

Slot interposer probe cable dimensions

The following figure shows the dimensions of the P67SAxxS slot interposer probes; all slot probes have the same cable lengths.

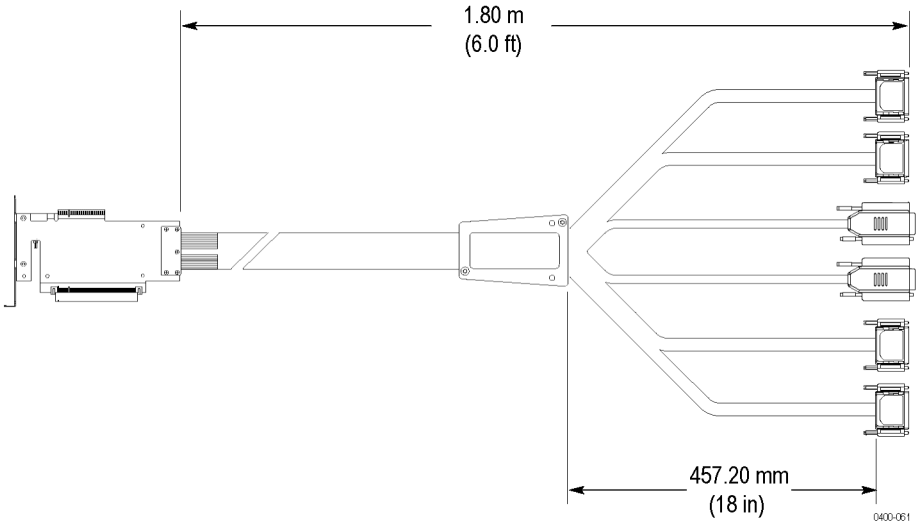


Figure 51: P67SA16S, P67SA08S, P67SA04S and P67SA01S Slot Interposer probe cable lengths

P67SA16 Slot Interposer Probe dimensions

The following figure shows the dimensions of the P67SA16S Slot Interposer Probe head. (See Figure 52 on page 89.) A 3D CAD solid model, pcie_x16_slot_probe.stp file, is attached to the PDF version of this document. (See page 144, *Slot interposer probe 3D CAD models*.)

NOTE. *3D CAD solid models are included in the electronic files that are attached to the PDF file of this document. To access the attached files, open the PDF file and click on the paperclip icon on the lower-left side of the document viewer.*

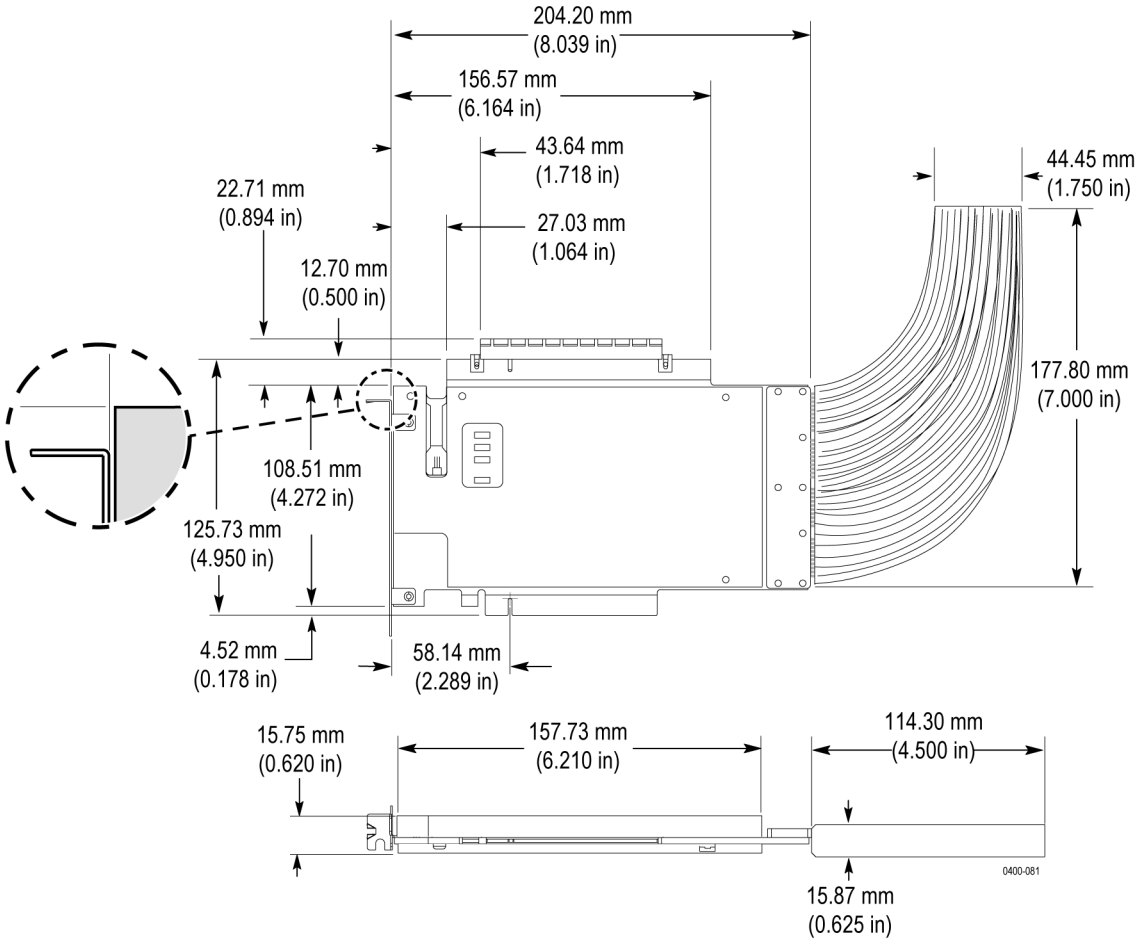


Figure 52: P67SA16S Slot Interposer Probe dimensions

P67SA08S, P67SA04S, and P67SA01S Slot Interposer Probe dimensions

The following figure shows the dimensions of the P67SA08S, P67SA04S, and P67SA01S Slot Interposer Probe heads. (See Figure 53 on page 90.) A 3D CAD solid model, pcie_x8-x4-x1_slot_probe.stp file, is attached to the PDF version of this document. (See page 144, *Slot interposer probe 3D CAD models*.)

NOTE. *3D CAD solid models are included in the electronic files that are attached to the PDF file of this document. To access the attached files, open the PDF file and click on the paperclip icon on the lower-left side of the document viewer.*

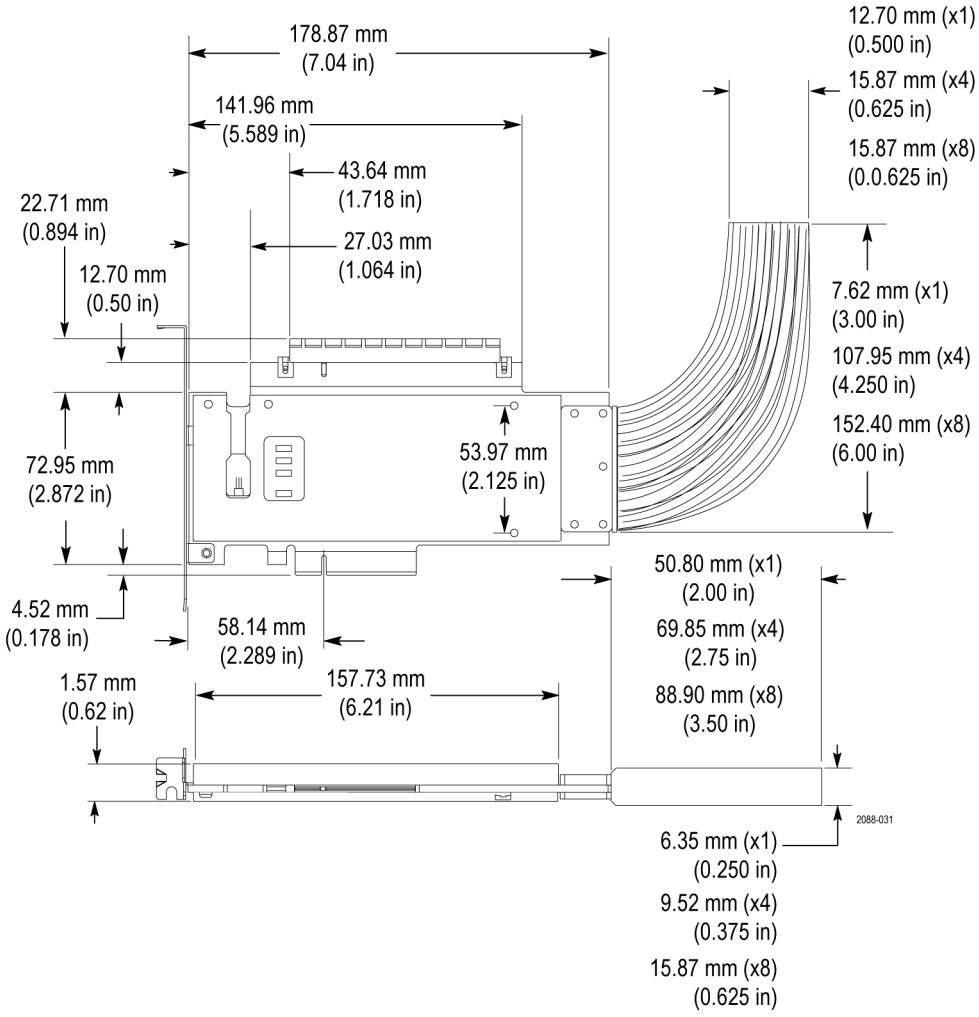


Figure 53: P67SA08S, P67SA04S, and P67SA01S Slot Interposer probe dimensions

NOTE. *The TLA7SAxx modules support capturing unidirectional traffic such as compliance mode. If only one agent is present on the bus then the system must provide termination of the bus that meets the PCIe receiver specifications. This can be implemented as on board termination or using a slot termination board such as the PCI Express Compliance Load Board (CLB1). (See Figure 54.)*

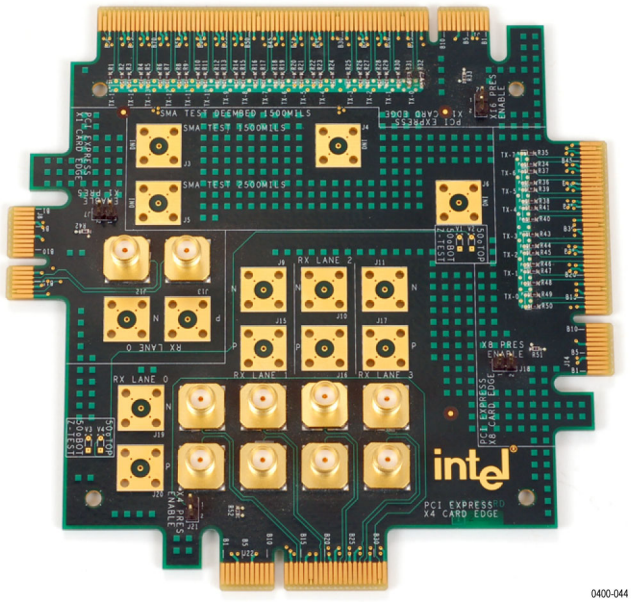


Figure 54: PCI Express Compliance Load Board (CLB1)

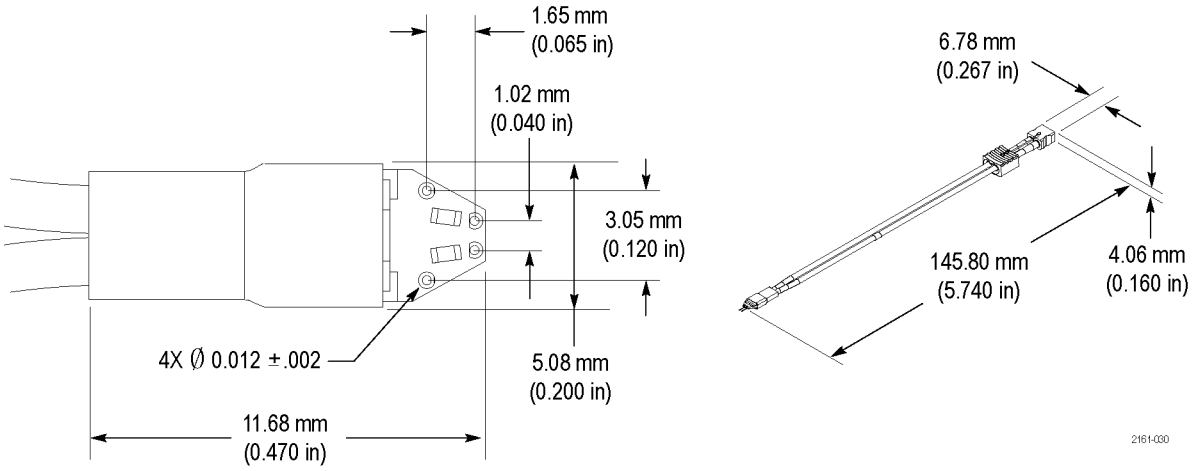


Figure 55: P75TLRST solder tip dimensions

The following figure shows the dimensions of the optional TriMode resistor solder tip.

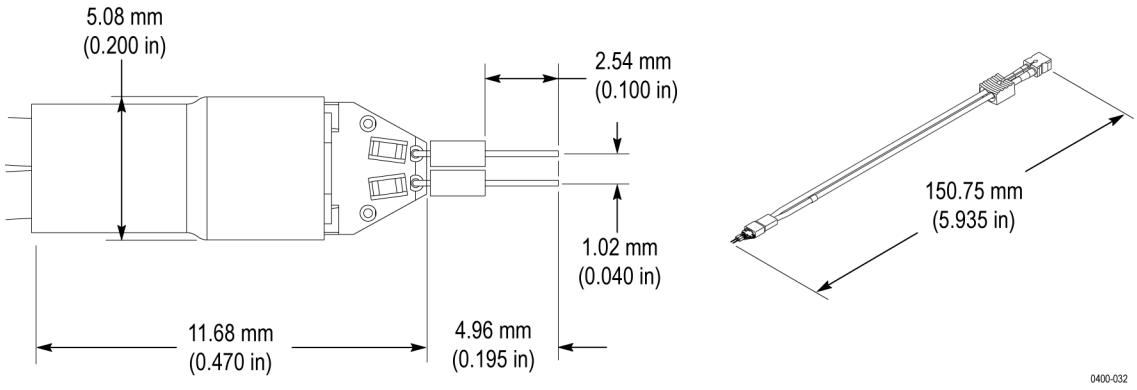


Figure 56: TriMode resistor solder tip dimensions

The following figure provides a graphical overview of how to connect the P67SA01SD Solder-Down probe to the logic protocol analyzer module, including the power connections. (See Figure 57.) Tektronix provides a means to add additional solder-down probes to the probe connector. (See page 159, *Adding probes to the P67SA01SD probe connector*.)

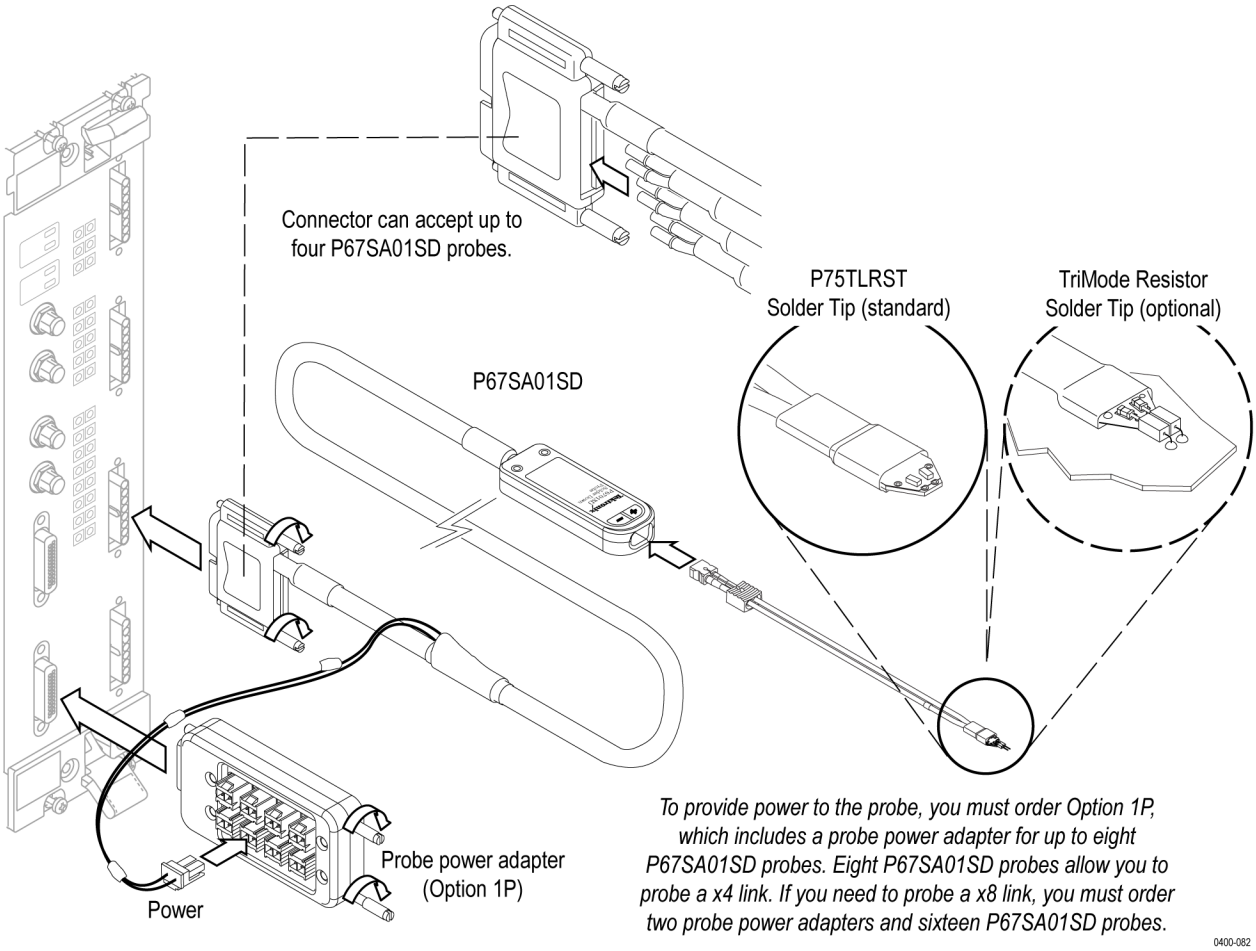


Figure 57: Connecting the P67SA01SD Solder-Down probe

Circuit board design

Use the following mechanical and electrical guidelines when designing your system.

Mechanical design

This section provides mechanical design details for the midbus probe, including footprint dimensions, footprint keep-out areas, trace and via size, and routing requirements.

NOTE. *The footprints described in this section are intended for use with the TLA7SAxx logic protocol analyzer module and the P67SAxx midbus probes. This hardware supports PCIe3 including support for PCIe2 and PCIe1. These footprints are NOT compatible with the TLA7Sxx logic protocol analyzer modules and P67xx midbus probes. If your design requires interoperability with the TLA7Sxx logic protocol analyzer modules and P67xx midbus probes, please contact your local Tektronix representative for assistance.*

Table 31: Recommended circuit board design criteria

Parameter	Description
Circuit board thickness	0.79 mm (0.031 in) minimum 6.35 mm (0.250 in) maximum
Footprint type	PCI Express Gen3
Pad finish	3 to 7 microinches of immersion gold over 50 to 150 microinches of electroless nickel. Protect the pads from solder during assembly operations to maintain the gold finish.
Solder mask coverage	At a minimum, solder mask must be present in the region specified, but should not cover the midbus pads.

Footprint dimensions and keep-out area

Design your circuit board layout using the footprint dimensions in the following figures so that a probe retention mechanism will fit properly and make good electrical contact with your system. The space around the footprint (keep-out area) represents the area that will be covered by the retention mechanism.

The following figures show the x8 midbus probe footprint and keepout areas for the top or front side of the circuit board and for the bottom or back side of the circuit board. (See Figure 58 on page 95.) (See Figure 59 on page 96.)

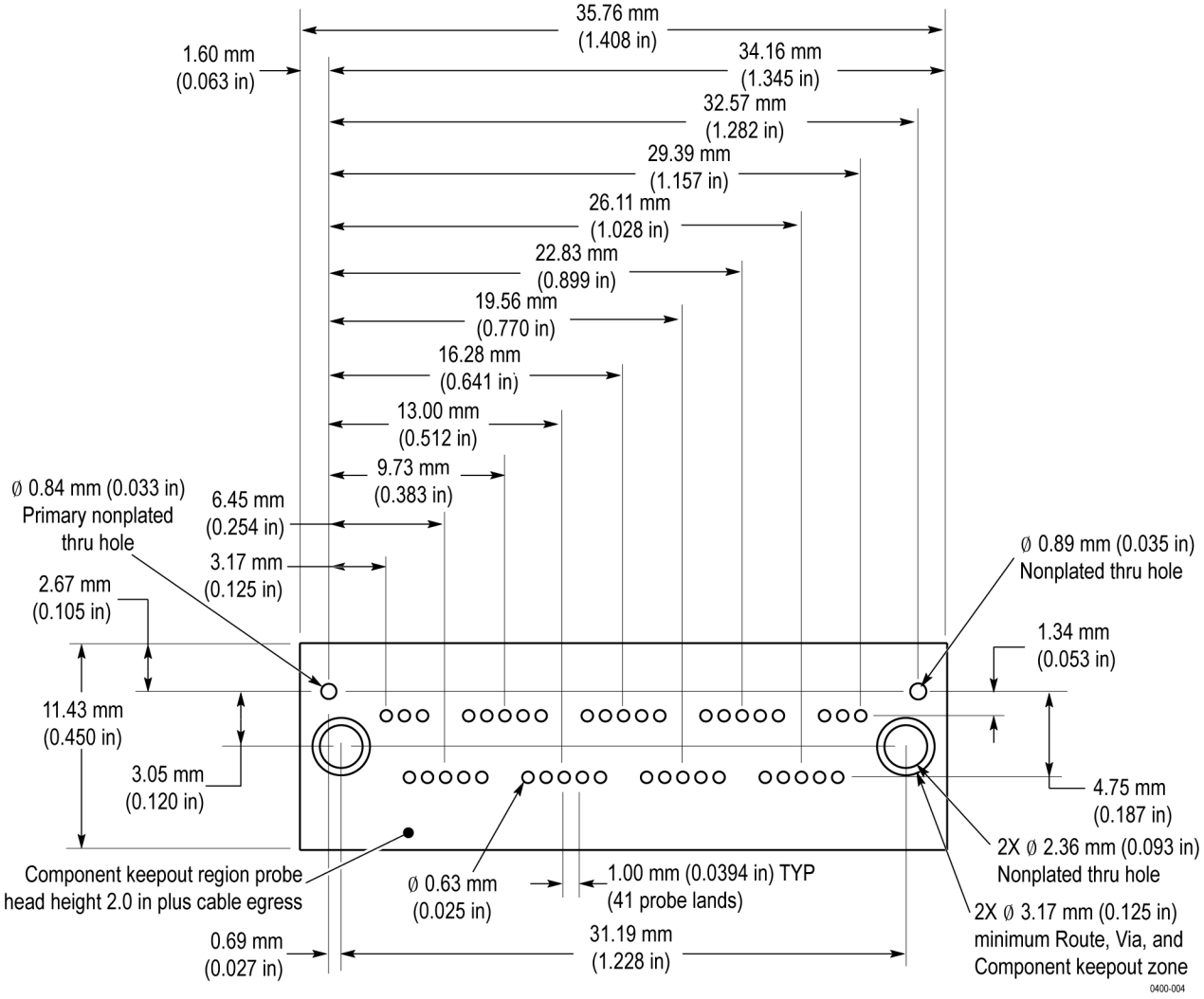


Figure 58: x8 midbus footprint dimensions and keep-out area (front side of circuit board)

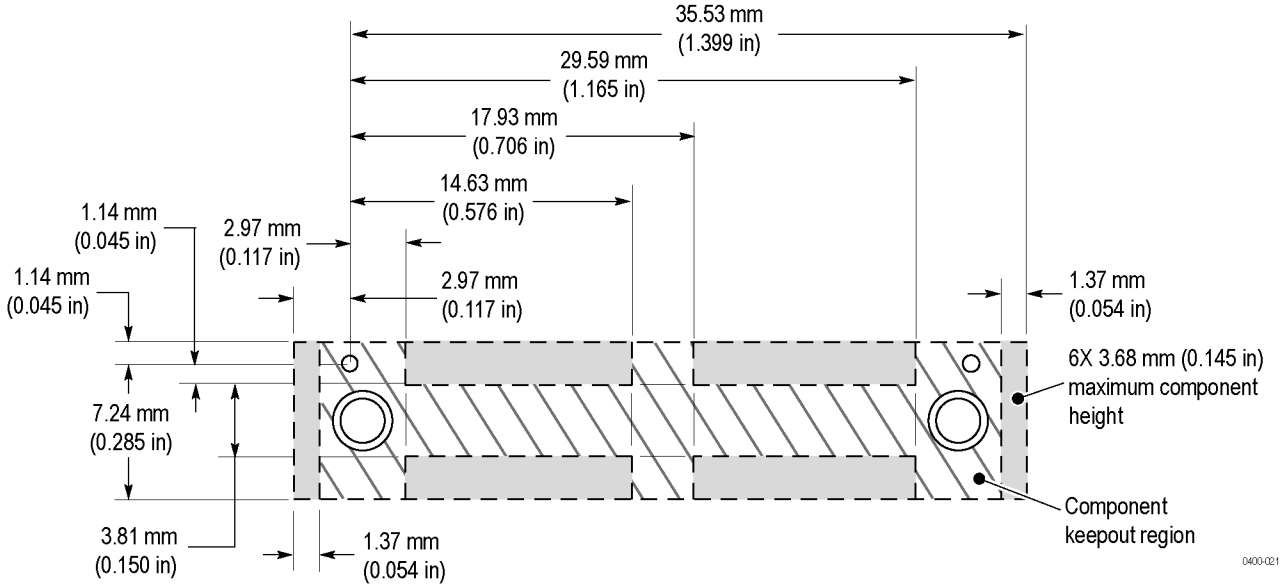


Figure 59: x8 midbus footprint dimension and keep-out area (back side of circuit board)

The following figure shows the footprint pad details of the x8 and x4 midbus probes. (See Figure 60.)

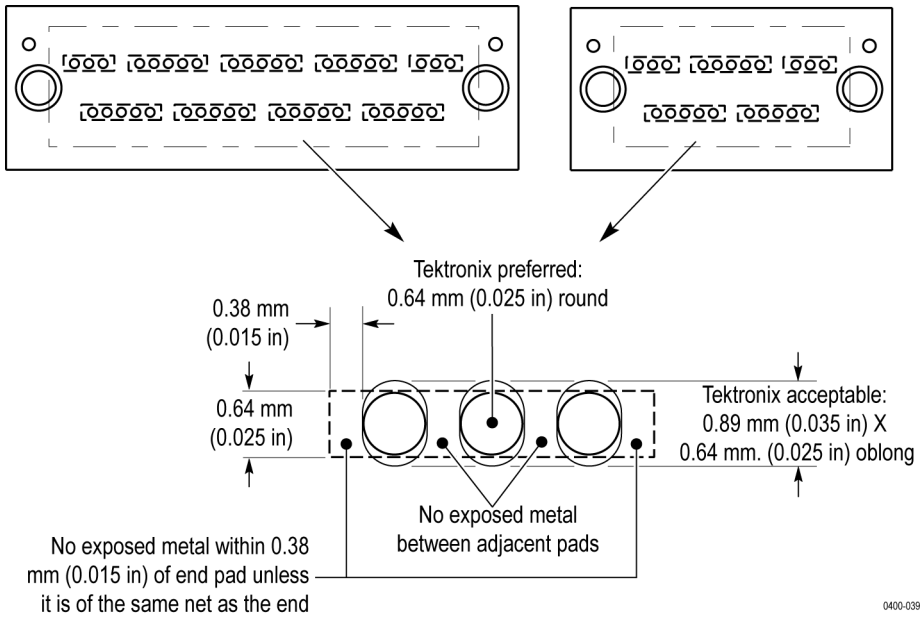


Figure 60: Footprint pad details for x8 and x4 midbus probes

The following figures show the x4 midbus probe footprint and keepout areas for the top or front side of the circuit board and for the bottom or back side of the circuit board. (See Figure 61.) (See Figure 62 on page 98.)

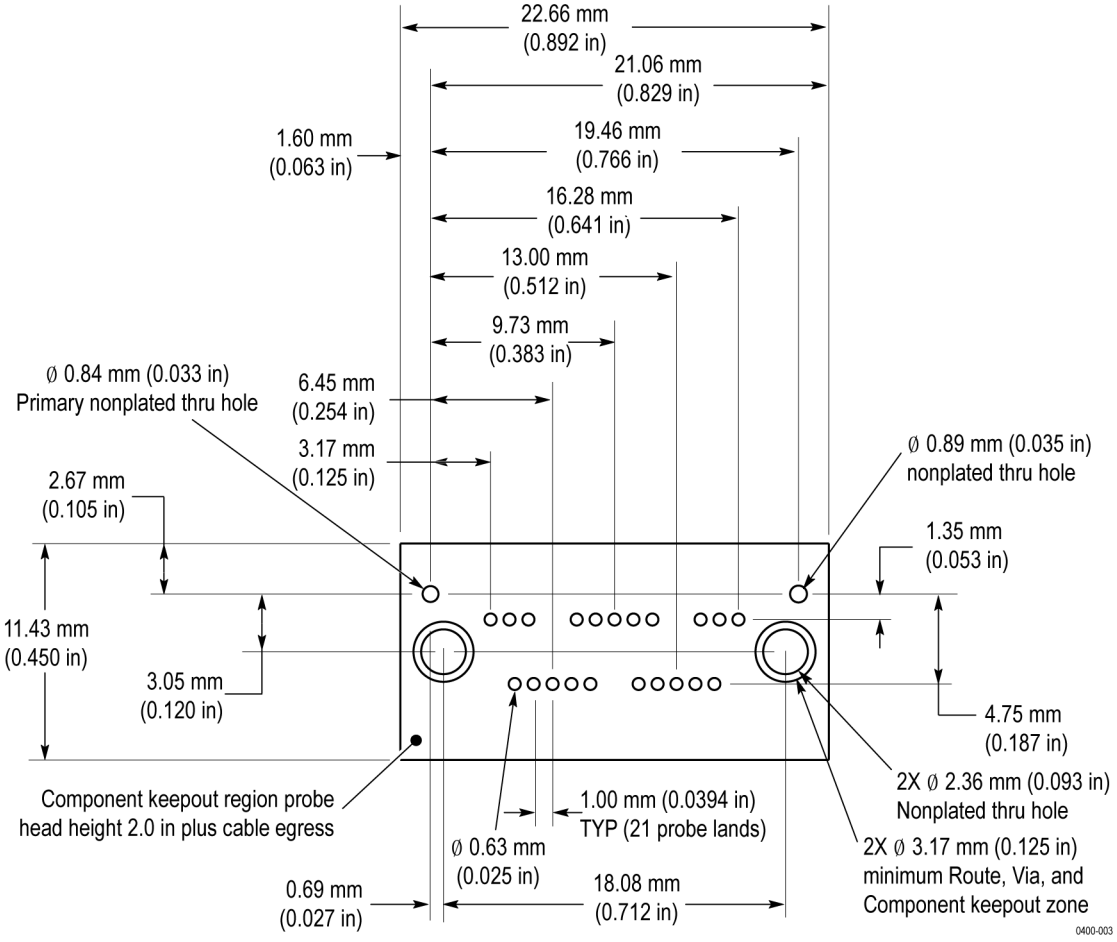


Figure 61: x4 midbus footprint dimensions and keep-out area (front side of circuit board)

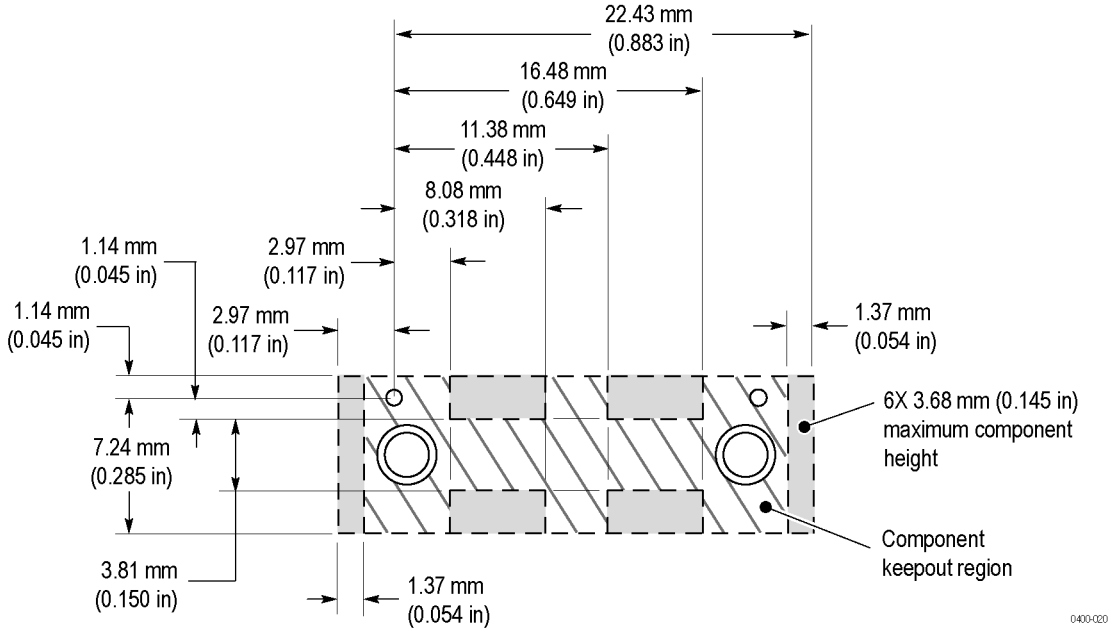


Figure 62: x4 midbus footprint dimension and keep-out area (back side of circuit board)

The following illustration shows the P67SA16G2 x8 Midbus probe footprint and keepout areas of the top or front side of the circuit board.

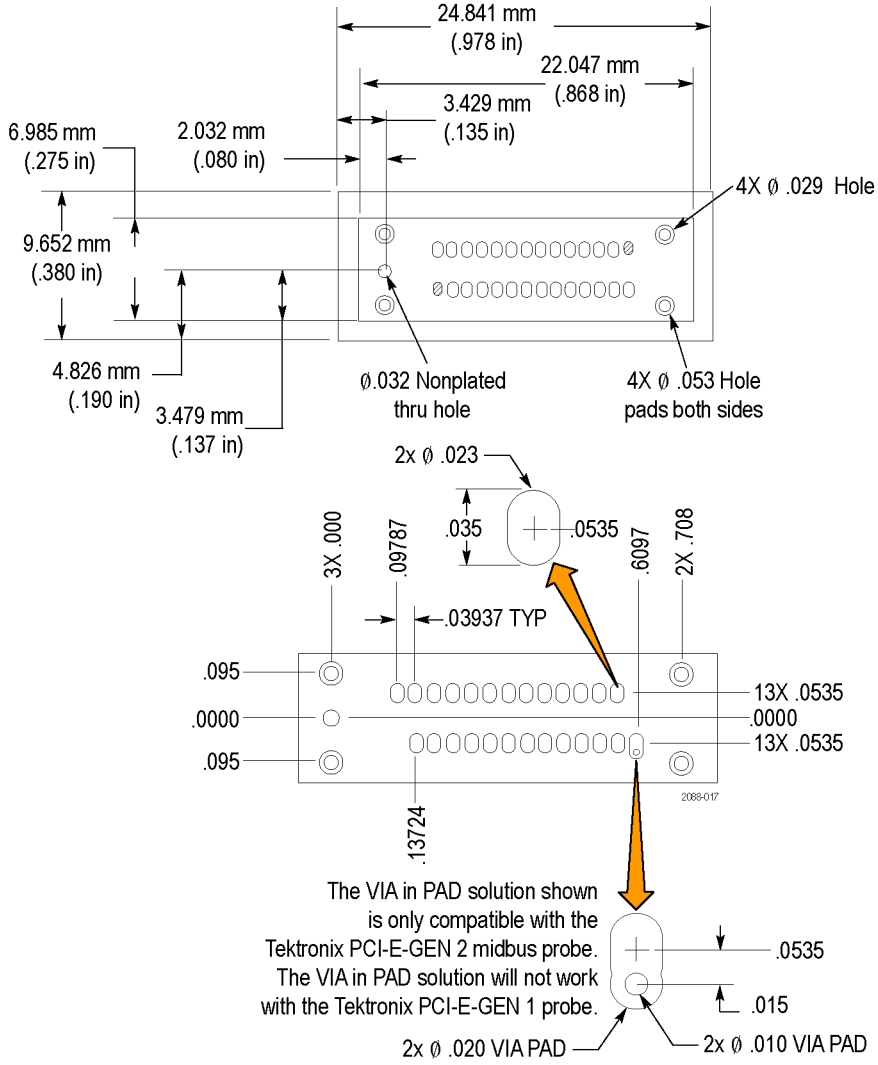


Figure 63: P67SA16G2 x8 Midbus footprint dimensions and keep-out area

The following illustration shows the P67SA08G2 x4 Midbus probe footprint and keepout areas of the top or front side of the circuit board.

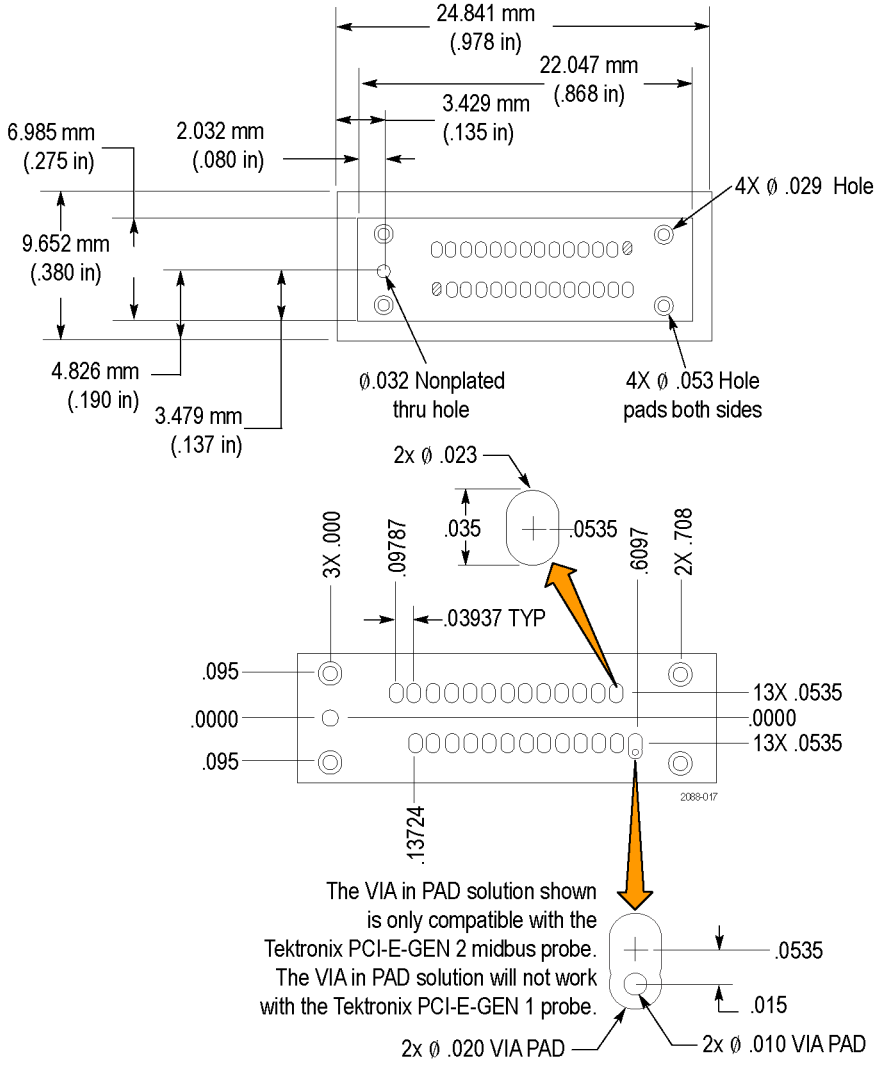


Figure 64: P67SA08G2 x4 Midbus footprint dimensions and keep-out area

Routing considerations for the midbus probe footprint

Routing and simulation studies have been performed near and through the PCI Express midbus footprint to determine a best-known method for maintaining integrity of the system, as well as provide an adequate signal to the logic protocol analyzer. However, the following information does not imply that superior routing techniques do not exist. Every stackup will drive differences in layout. Use the recommended routing below as an example to start from. It is mandatory that you closely monitor and simulate the routing near and through the midbus probe to ensure that integrity of the system and midbus signal eye are maximized. Some dimensional details concluded from these simulations and studies are provided in the following table.

Table 32: Trace characterisitics

Parameter	Size
Trace width	7.5 mil
Trace spacing	8.0 mil
Necked-down trace width	5.5 mil
Necked-down trace spacing	4.0 mil
Space between differential pairs	15.0 mil

The following figure shows the routing through the footprint, assuming the footprint is on the same layer as the bus. (See Figure 65.) If the bus is on an inner layer or on the opposite side of the circuit board, the traces will need vias up to the surface layer before the footprint and down after the footprint.

NOTE. *Adding vias to traces to connect to the probe footprint while keeping the traces on inner layers has a large impact on the signal integrity.*

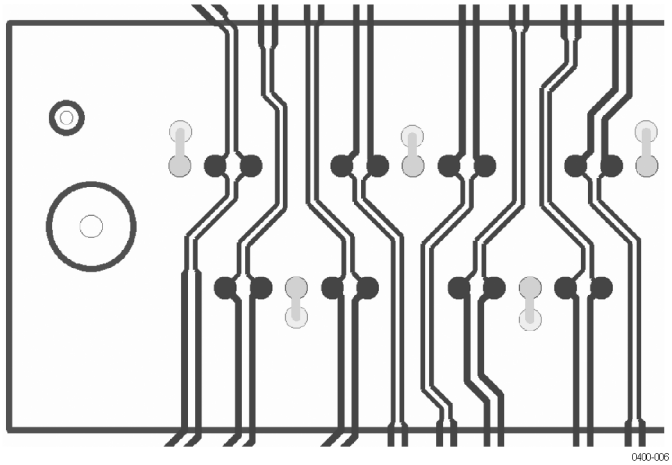


Figure 65: Recommended trace routing on the primary surface layer

Midbus probe CAD symbols for PCB layout

Tektronix has provided CAD symbols for the P67SA08 x4 midbus probes and for the P67SA16 x8 midbus probes for your use when placing midbus probe footprints on your circuit board. The following figures show the CAD symbols (the files are attached to the PDF copy of this document). (See Figure 66.) (See Figure 67.)

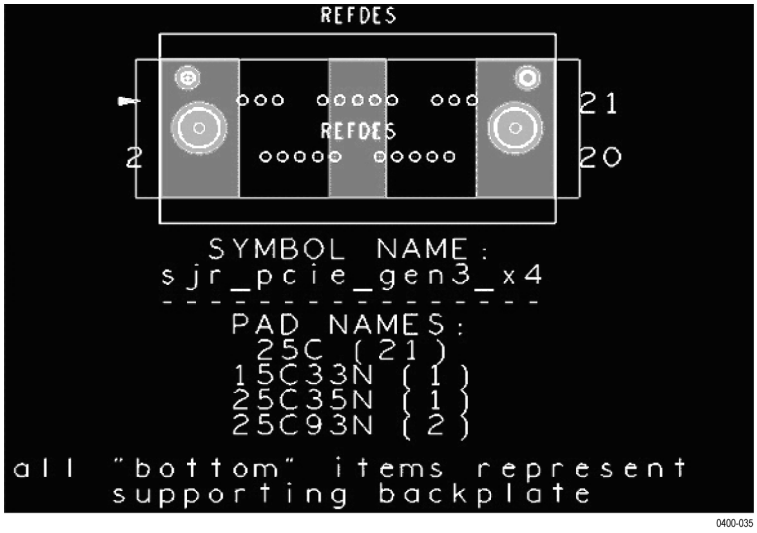


Figure 66: P67SA08 x4 midbus probe CAD symbol

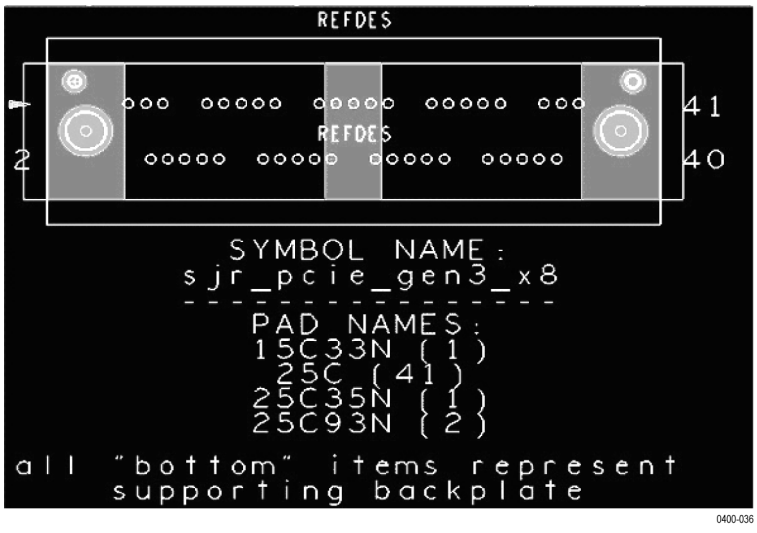


Figure 67: P67SA16 x8 midbus probe CAD symbol

NOTE. *File attachments are identified by a paperclip icon in the PDF file window. To access the attached files, open the PDF file and click on the paperclip icon on the lower-left side of the document viewer.*

There are two types of PCB layout CAD symbol files attached to the PDF version of this document:

- Files with .dra or .psm file extensions–for Cadence® Allegro® Version 16.01 or greater
- Files with .dxf or .igs file extensions–for other PCB layout programs that support the import of CAD symbols in these file formats

Additional information is available in Appendix A. (See page 142, *Midbus probe CAD symbols for PCB layout*.)

P67SA01SD Probe solder tips

The P67SA01SD Solder-Down Probe includes a P75TLRST probe tip which is designed for solder-down probing applications. It is composed of a small form factor interconnect circuit board with SMD0402 damping resistors and a set of vias for wire attachment to the SUT. The probe tip dimensions are shown in the *Probe Dimensions* section. (See Figure 55 on page 91.)

The P75TLRST probe tip circuit board vias are designed for both 4 mil and 8 mil wire and a special high tensile strength wire is supplied as part of the wire accessory kit. The expanded view of the probe tip shows the location of the + and – signal inputs as well as the two ground reference connections. (See Figure 68.)

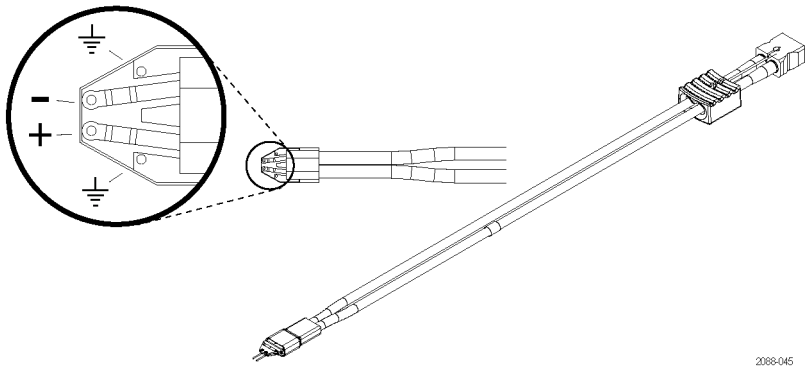


Figure 68: P75TLRST TriMode Long Reach Solder Tip

TriMode resistor solder tip

An optional solder tip is also available that includes axial-lead damping resistors between it and the solder connections to your circuit. (See Figure 69.) Order the TriMode Resistor solder tip, Tektronix part number 020-2936-XX. For more information, refer to the *P7500 Series TriMode Probe Technical Reference*, Tektronix part number 077-2161-XX, available on the Tektronix Web site, www.tektronix.com.

The probe tip dimensions are shown in the *Probe Dimensions* section. (See Figure 56 on page 92.)

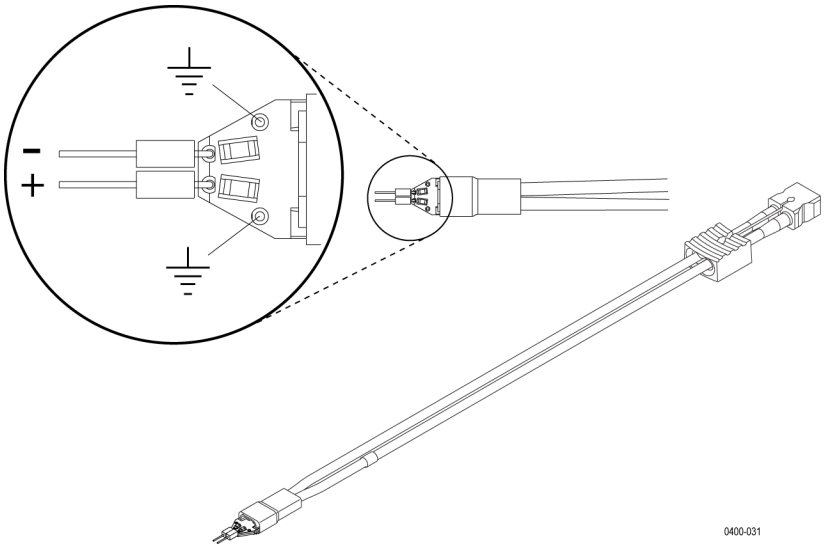


Figure 69: TriMode Resistor Solder Tip

Tip topology

Attached to the circuit board are a pair of very low skew (<1 ps) coaxial cables and a polarized G3PO dual connector block. The G3PO connectors use a miniature, high frequency design that enables quick and easy installation of the solder tip. The G3PO connector block of the probe tip is inserted into the input nose piece on the end of the P67SA01SD Logic Protocol Analyzer probe body. The probe body contains a mating, polarized G3PO connector block with attached G3PO connector bullets.

The connector bullets are a part of the G3PO connector design, providing a self-aligning interconnect mechanism between G3PO connectors. The G3PO connector in the probe body is designed to have higher detent force than the probe tip connectors, which is intended to ensure that the G3PO bullets remain in the probe body connector when disconnected.

The probe body nose piece, with its integral spring mechanism, helps to provide a self-aligning mechanism for hand insertion of the probe tip. The probe body nose springs also give a secure capture of the probe tip connector after insertion.

Release of the probe tip is assisted by using the wire-connected cable release holder on the probe tip connector. This probe tip release holder should always be used rather than pulling on the probe tip cables, which may cause tip cable damage.

Soldering the tips

The recommended wire attachment method for the P75TLRST tip is to first solder the wires to the SUT, being careful to minimize the wire length of the signal connections. This is followed by threading the wires through the probe tip board vias, being careful to achieve as symmetrical a wire pattern as possible between the two signal inputs. For the TriMode Resistor solder tip, you only need to solder the resistor leads to the SUT, keeping the resistor leads as short as possible. No further soldering is necessary when using this optional tip.

Finally, the attachment is completed by soldering the wires on top of the probe tip circuit board. Any excess wire lead length extending through the probe tip board should be removed to minimize possible signal reflection problems. Because of the limited mechanical strength of the wire interconnect and probe tip circuit board, the solder-down probe tip should be taped down at the SUT for strain relief. Although the accessory kit includes adhesive strips that can be used for the strain relief of the probe tip, the use of mylar tape will generally provide stronger attachment if room is available at the SUT.

The lead length of the connection wires between the probe tip board and the SUT must be kept as short as possible to preserve the integrity of the measured signal. Typical wire lengths range from 0.010 in. to 0.100 in. (See Figure 70.)

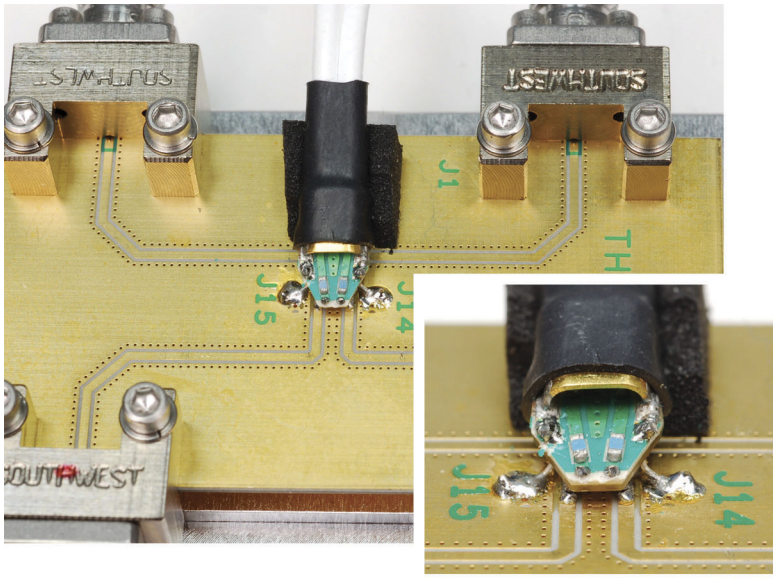


Figure 70: Typical wire length from probe tip to circuit

The following four figures illustrate the signal integrity effect on the P75TLRST solder tip when used with different lengths of tip wire. Signal fidelity is best when the wire length is kept as short as possible. The step generator that was used as a signal source for these screen shots has a 30 ps 10-90% rise time. The table in each figure contains data for two rise time measurements (10-90% and 20-80%).

These screen shots can be used as a guide to gauge the effects of wire length, but actual results may vary depending on the other factors like characteristics of the device under test (for example, rise time and impedance), and the precision of the solder connection.

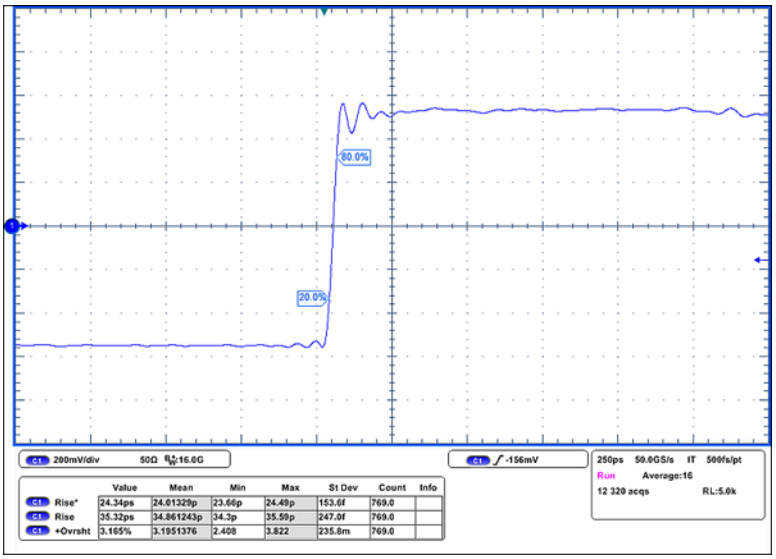


Figure 71: P75TLRST solder tip with 0.010 inch of tip wire

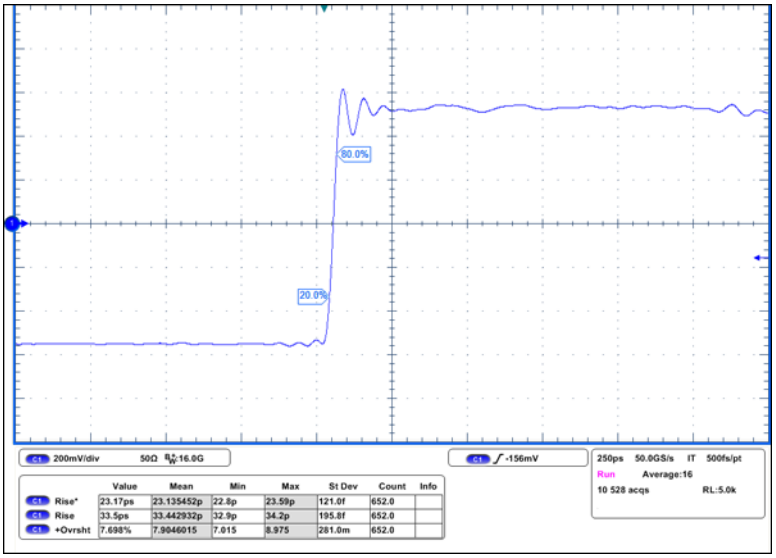


Figure 72: P75TLRST solder tip with 0.050 inch of tip wire

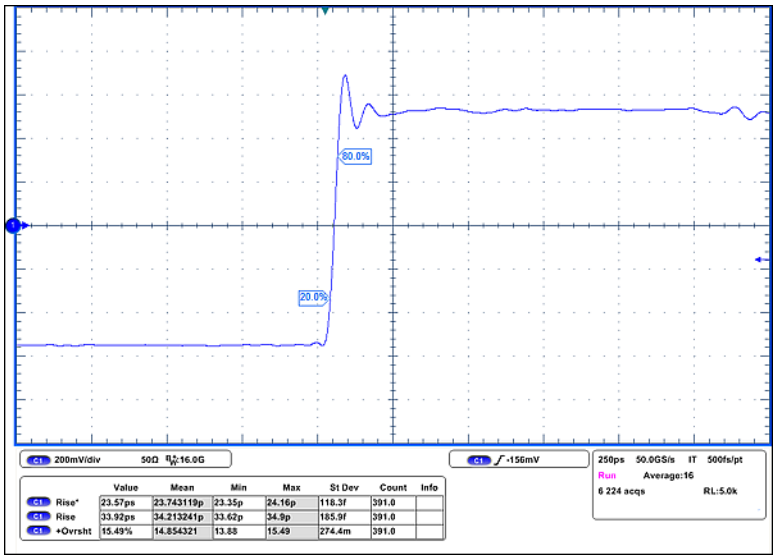


Figure 73: P75TLRST solder tip with 0.100 inch of tip wire

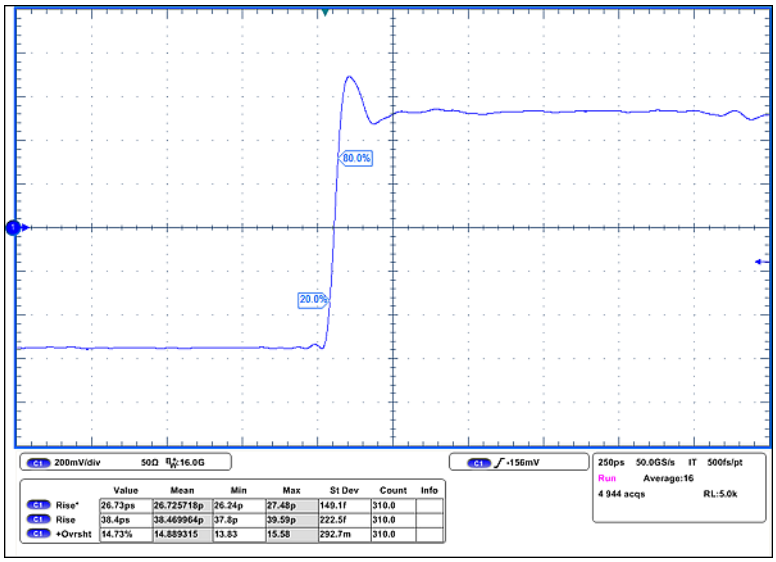


Figure 74: P75TLRST solder tip with 0.200 inch of tip wire

Reference clock cable three-pin connector

If SSC (spread-spectrum clocking) is enabled, and your PCI Express link uses ASPM (Active State Power Management) protocol, you must connect a reference clock cable to the SUT and set the SUT Reference Clock selection (in the Setup window) to **Connected at Front Panel** so that the module will capture data reliably.

NOTE. *While your application might not use either the SSC or ASPM protocol, Tektronix recommends that you include this three-pin connector if you plan to use a midbus or solder-down probe (the three-pin connector is already included on the slot interposer probes. For more information, refer to the discussion on under Reference Clock Signal.* *(See page 117, Reference clock signal.)*

If you intend to use either a midbus probe or a solder-down probe with a reference clock cable, you must install a three-pin micro-terminal strip connector on your SUT. A non-intrusive clock cable (Tektronix part number 872-0594-00) has two SMA connectors on one end (+ and –), and a small circuit board with a mating three-pin connector on the other. Only one connector is needed, even if more than one TLA7SA16 module is used. In this case, a "jumper" clock cable with SMA connectors on each end (+ and –) can connect the two modules and share the clock signal.

Tektronix suggests installing the following three-pin connector (or similar):

- Through hole: Samtec® TMS 103-02-S-S

  (1 x 3, 0.05 in. center spacing)

- Surface mount: Samtec® FTR 103-02-S-S

  (1 x 3, 0.05 in. center spacing)

Table 33: Reference clock cable three-pin connector pin assignments

Signal	Pin number
REFCLKp	1 (or 3) [1]
GND	2
REFCLKn	3 (or 1) [1]

[1] The logic protocol module is not sensitive to the polarity of the reference clock signal. The clock cable connector can be attached in either orientation.

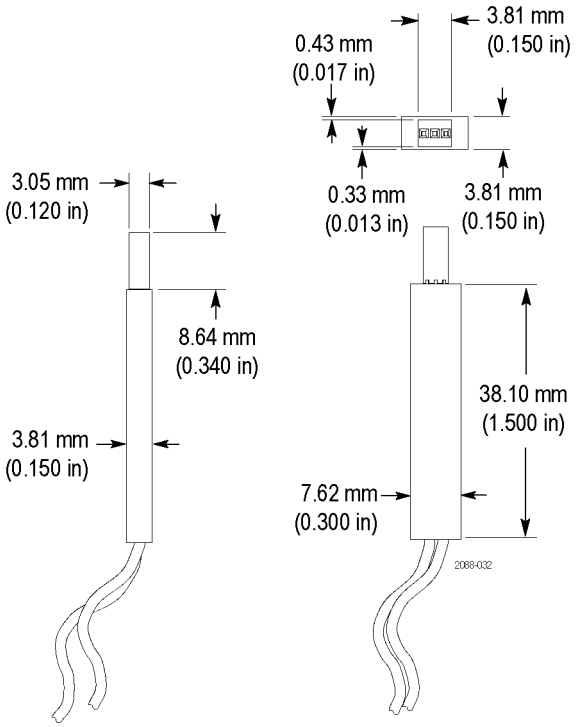


Figure 75: Reference clock cable connector dimensions

For more specific information on keep-out volumes for particular system configurations, contact your local Tektronix representative.

Electrical design

For the logic protocol analyzer module to reliably capture logical transactions on the bus, the bus must have adequate signal integrity at the point of probing while the probe is connected. This can be verified by electrical simulation using the probe models for your P67SAxx series probe.

The P67SAxx series probes can probe a signal that has an eye closed due to losses in boards or cables. Eye requirements are defined at the point of probing with an equalization function applied (midbus footprint, solder tip input for the solder-down probe, or the slot connector for the slot interposer probe), and are measured by eye height and eye width, forming a diamond shape. The equalization function is included in the probe model. Simulation and measurement methodologies for verifying the eye are in the following sections.

The eye specification formula includes some jitter components from the system under test. The $S_{J\,SYS}$ component should only include Sinusoidal jitter from the transmitter above 20 MHz. The $R_{J\,SYS}$ number should include all Gaussian jitter from the transmitter.

The eye height (labeled X in the diagram) must have an amplitude of at least 5 mV. (See Figure 76 on page 111.) The eye width (labeled Y) must satisfy the following formula. The eye is measured or simulated in the system and then the appropriate equalization model from this document is applied. The Y_{EYE} and the X_{EYE} are determined from the equalized eye.

$$Y_{EYE} \geq 28.12\,ps + S_{JSYS} + 14.07\sqrt{1.44 \times 10^{-24} + R_{J\,SYS}}^{\,2}$$

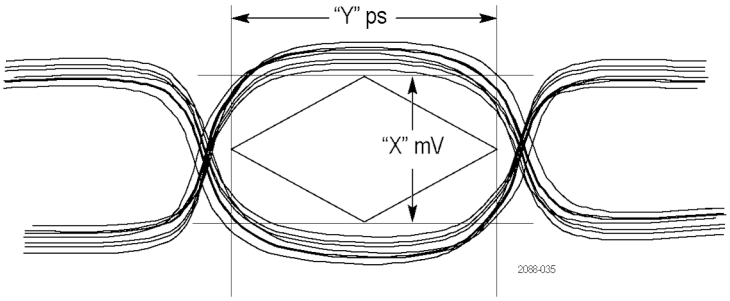


Figure 76: Signal eye measurements (time versus voltage)

Measuring signal eye

Tektronix recommends using a Tektronix DPO70000 series or DSA70000 series oscilloscope, with a P7500 series probe with solder-down tips to achieve the most accurate results. If your system does not allow you to use solder-down tips, use the handheld Precision Differential Probing Module (Tektronix part number P75PDPM). Tektronix recommends using DPOJET application to take signal eye measurements. Tektronix RT-Eye software is also acceptable. For instructions on using DPOJET and RT Eye software, go to Tektronix.com/manuals, or contact your local Tektronix representative.

P67SAxx midbus probe circuit impact

The probe models for the P67SAxx midbus probes are six-port Touchstone® models attached to the PDF version of this document.

NOTE. *File attachments are identified by a paperclip icon in the PDF file window. To access the attached files, open the PDF file and click on the paperclip icon on the lower-left side of the document viewer.*

There are two models to choose from.

- Use the P67SAxx_Short_Channel_Model.s6p Touchstone® data file for most PCIe signals.
- Use the P67SAxx_Long_Channel_Model.s6p Touchstone® data file for signals where the midbus probe is over 18 inches from the transmitter.

Insert the probe model into the system simulation at the point where the midbus probe will be placed:

- Connect Port 1 to the positive side of the upstream driver.
- Connect Port 2 to the negative side of the upstream driver.
- Connect Port 3 to the positive side of the downstream receiver.
- Connect Port 4 to the negative side of the downstream receiver.
- Ports 5 and 6 are the differential outputs of the probe after equalization. Connect these ports to a clean 50 Ω termination. The differential eye at Ports 5 and 6 must meet the eye specification listed earlier in this section.

The following illustration shows the system impact of the P67SAxx midbus probe.

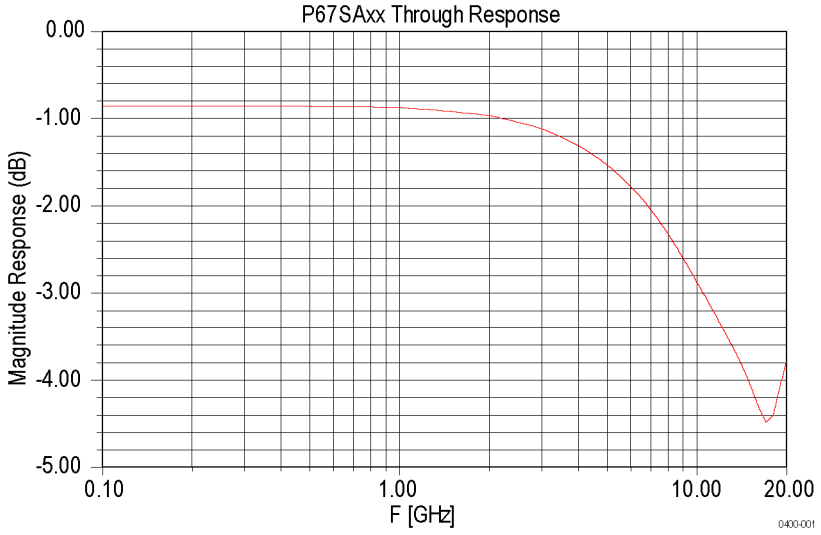


Figure 77: Probe impact of the P67SAxx midbus probe

P67SA16G2 x8 or P67SA08G2 x4 Midbus probe circuit impact

Tektronix has provided two Touchstone® models (P67xx_wop.s2p and P67xx_wp.s2p). (See page 141, *File attachments*.) These models simulate the impact of the P67SA16G2 x8 or P67SA08G2 x4 Midbus probe retention mechanisms with and without the probe installed. This is actual S-parameter measured data using real probes and retentions. Graphical representation of the data is provided in the next two graphs.

The first graph shows the frequency response of a transmission line loaded with a P67SA16G2 x8 or a P67SA08G2 x4 Midbus probe retention. (See Figure 78 on page 113.)

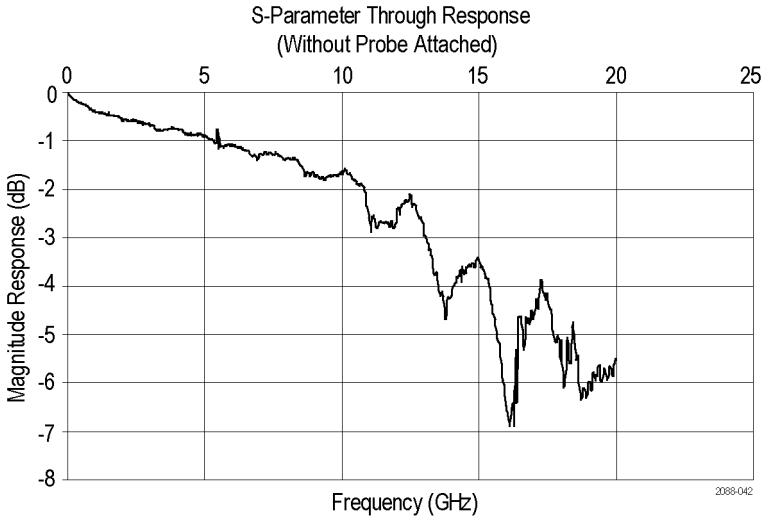


Figure 78: S-parameter data of retention mechanism only

The following graph shows the frequency response of a transmission line loaded with a P67SA16G2 x8 or a P67SA08G2 x4 Midbus probe retention and a probe.

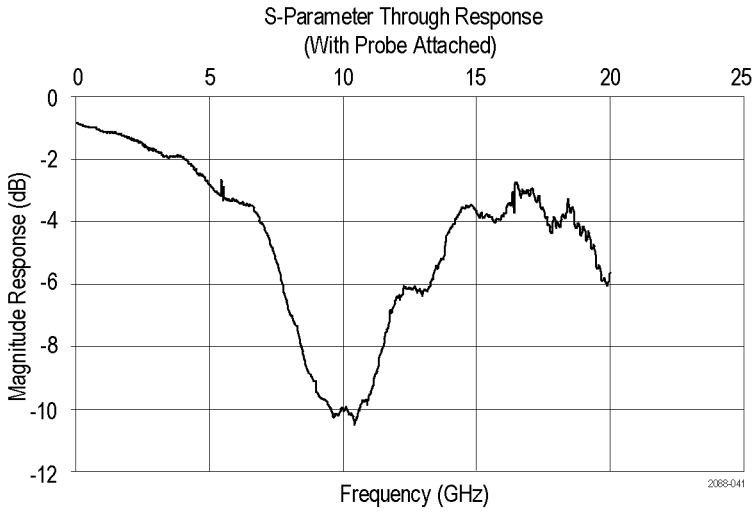


Figure 79: S-parameter data of retention mechanism plus P67SA16G2 x8 or P67SA08G2 x4 Midbus probe

P67SAxx slot interposer probe circuit impact

The probe models for the P67SAxx slot interposer probes are six port Touchstone® models attached to this document.

NOTE. *File attachments are identified by a paperclip icon in the PDF file window. To access the attached files, open the PDF file and click on the paperclip icon on the lower-left side of the document viewer.*

There are two models to choose from.

- Use the P67SAxxS_Short_Channel.s6p Touchstone® data file for most PCIe signals.
- Use the P67SAxxS_Long_Channel.s6p Touchstone® data file for signals where the slot probe is over 18 inches from the transmitter.

Insert the probe model into the system simulation at the point where the slot probe will be placed:

- Connect Port 1 to the positive side of the upstream driver.
- Connect Port 2 to the negative side of the upstream driver.
- Connect Port 3 to the positive side of the downstream receiver.

- Connect Port 4 to the negative side of the downstream receiver.
- Ports 5 and 6 are the differential outputs of the probe after equalization. Connect these ports to a clean 50 Ω termination. The differential eye at Ports 5 and 6 must meet the eye specification listed earlier in this section.

The following illustration shows the system impact of the P67SAxxS slot probe.

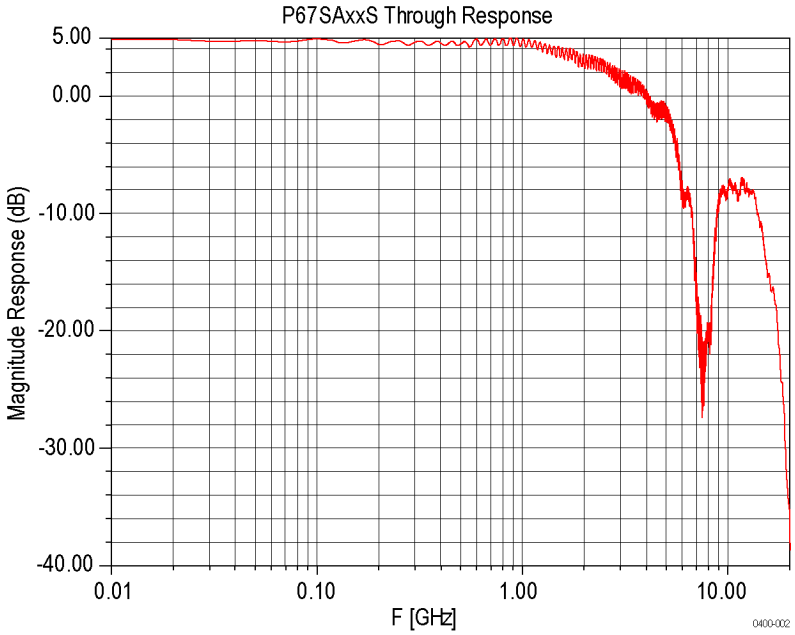


Figure 80: Probe impact of the P67SAxxS slot probe

P67SA01SD Solder-Down Probe circuit impact

Tektronix has provided a Touchstone® model (P67SA01SD.s4p) to simulate the impact of a P67SA01SD solder-down probe and P75TLRST solder tip. This is actual S-parameter measured data using a P67SA01SD solder-down probe. Graphical representation of the data is provided in the following graph. It shows the frequency response of a transmission line loaded with a P67SA01SD solder-down probe and P75TLRST solder tip.

NOTE. *S-parameter and load model data are included in the electronic files that are attached to the PDF file of this document. To access the attached files, open the PDF file and click on the paperclip icon on the lower-left side of the document viewer.*

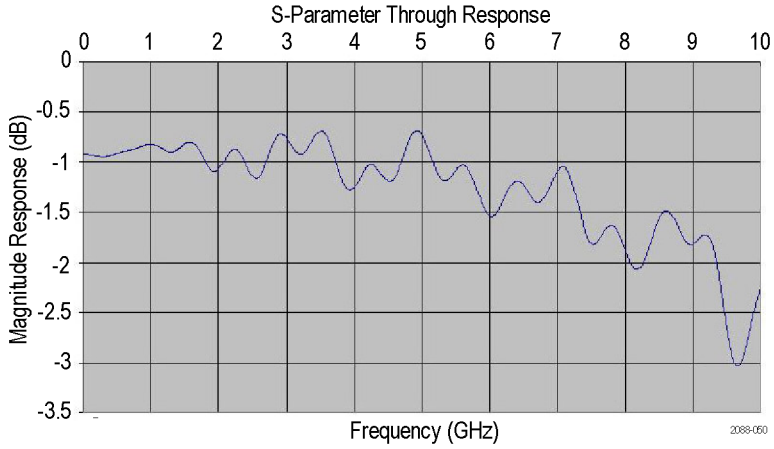


Figure 81: S-parameter data of P67SA01SD Solder-Down probe

NOTE. *When not connected to an oscilloscope or an LPA probe, the P75TLRST can cause additional loading on the bus beyond that is specified in this document. In a marginal system, do not leave the P75TLRST soldered into the platform without a probe attached.*

Reference clock signal

The TLA7SA16 Logic Protocol Analyzer modules can recognize a clock signal from a cable connection to the SUT, or by recovering the clock signal embedded in the data.

NOTE. *While your application might not use either the SSC or ASPM protocol, Tektronix recommends that you include this three-pin connector if you plan to use a midbus or solder-down probe (the three-pin connector is already included on the slot interposer probes.*

Recognize the reference clock signal by connecting to the SUT with a clock cable

Connect the external reference clock cable to the three-pin connector on the SUT (slot interposer probes already have this connector installed on the probe). Make sure that you set the SUT Reference Clock selection (in the Setup window) to **Connected at Front Panel** so that the module will capture data reliably.

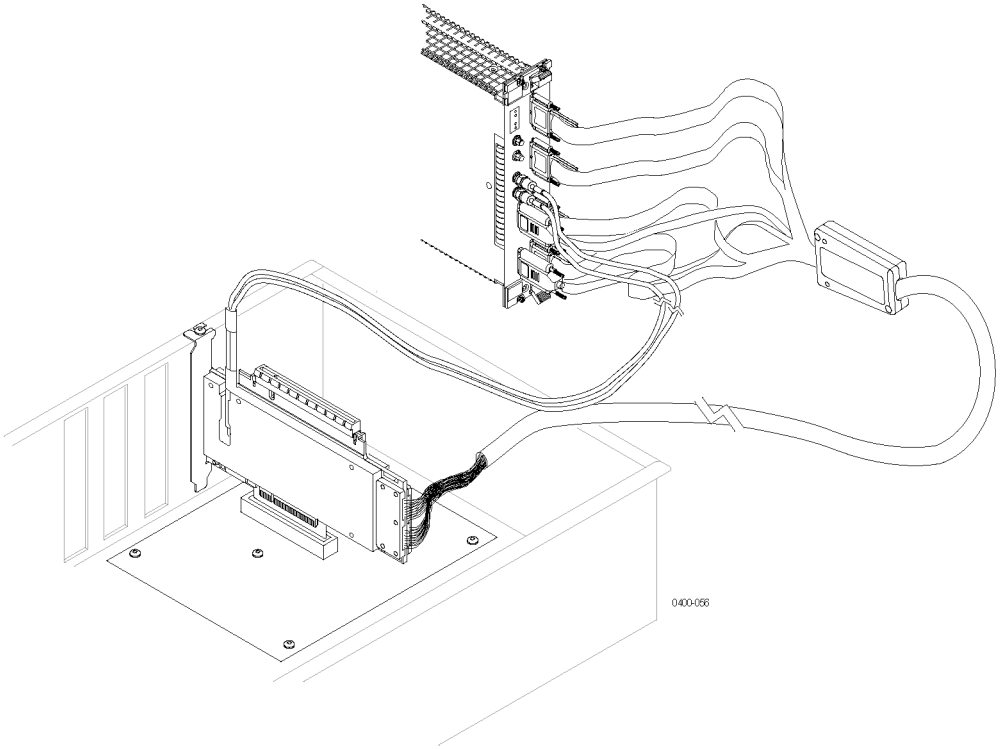


Figure 82: Slot interposer probe with a reference clock cable connected

Recognize the clock signal embedded in the data stream

A stable reference signal is generated by the logic protocol analyzer and synchronized with the embedded clock signal. A reference clock cable connection is not required, since the logic analyzer recognizes the embedded signal from the probe.

The transfer rate of the serial link must be 2.5 GT/s ±300 ppm (PCI Express Gen 1) or 5.0 GT/s ±300 ppm (PCI Express Gen 2) or 8.0 GT/s ±300 ppm (PCI Express Gen 3). If the transfer rate is not within this range, the module will not capture the data reliably.

Table 34: Reference clock electrical requirements

Module requirement	Symbol	Minimum	Typical	Maximum
Differential Voltage at Ref Clock Attach Point	Vdiff [2]	0.8 V	-	2.0 V
Absolute Voltage Limit at Ref Clock Attach Point	Vabs	0 V	-	3.3 V
Reference Clock Frequency –100 MHz	Freq100	-	100 MHz ±300 ppm	-
Reference Clock Frequency –100 MHz + 10% [1]	Freq100 +10%	-	110 MHz ±300 ppm	-
Reference Clock Frequency –100 MHz - 10% [1]	Freq100 -10%	-	90 MHz ±300 ppm	-
Reference Clock Total Jitter	RefClkJitter	- -	<1 MHz: 25 ps p-p >1 MHz: 200 ps p-p	- -

1 With SSC (spread-spectrum clocking) enabled or disabled

2 Vdiff= |2*(Vrefclockp - Vrefclockn)|

Midbus footprint pin and probe input assignments

The following figure shows the standard pin assignments for a PCIe3 x8 midbus footprint.

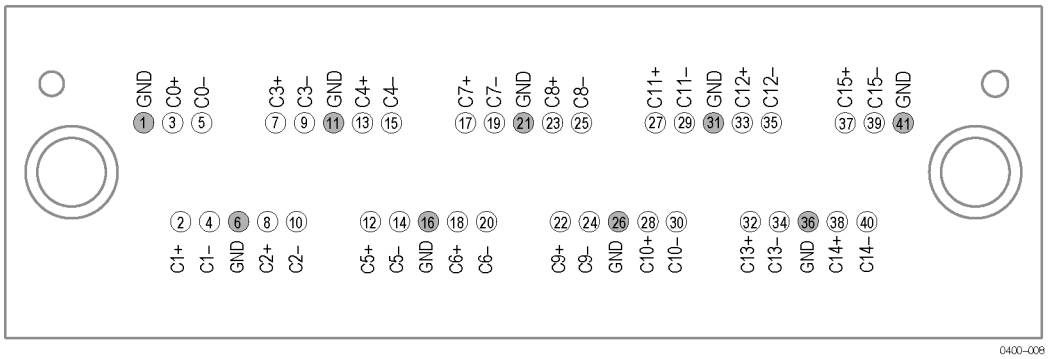


Figure 83: P67SA16 x8 midbus probe footprint pin assignments

The following figure shows the standard pin assignments for a PCIe3 x4 midbus footprint.

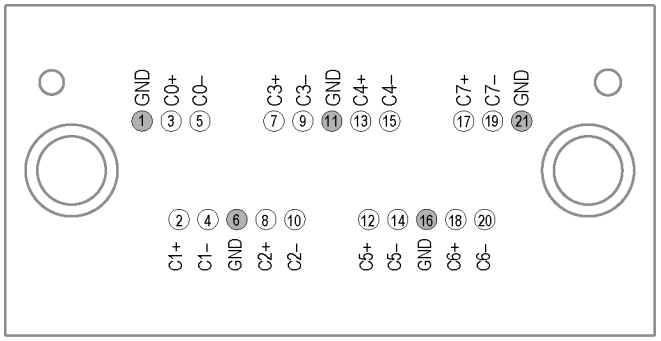


Figure 84: P67SA08 x4 midbus probe footprint pin assignments

General guidelines for lane mapping

Tektronix recommends that you design your system so that pins are assigned to lanes according to the following guidelines and formats listed in the following paragraphs and illustrations. The formats listed in the illustrations were created so that each module-end probe connector contains the wires connected to adjacent differential pairs from the same link on the footprint. A footprint should only contain signals from one or two links; a module-end probe connector should only contain signals from one link.

The logic protocol analyzer software is designed to be easily configured, based on these standard formats. If your system design does not allow you to follow these guidelines, or if a footprint is incorrectly wired, you may have to disassemble and rewire the connector at the module end of the probe. (See page 155, *Rearranging wires in the probe connector*.)

- The differential pairs that make up a PCI Express link must be connected to specific pads (pins) on the footprint.
- The polarity of the differential pairs can be swapped, if required, for routing.
- Upstream and downstream signals can be swapped on a footprint, if required, for routing.
- Entire links can be reversed, compared to the suggested routing.
- All lanes of a link must route to the same probe connector or group of probe connectors (for example, A-B-C-D), so that they connect to the same logic protocol analyzer module.
- Avoid routing more than one link to a given probe connector.
- The logic protocol analyzer modules have two probe power connectors and can provide power for 8 lanes (16 differential inputs). While it is possible to use multiple probes with one module, the system must still have enough power connectors and power for all probes.

x8 PCI Express midbus pin assignments

The following figure shows an example of footprints and pin assignments for the x8 midbus probes when used in an upstream *or* downstream configuration. (See Figure 85.)

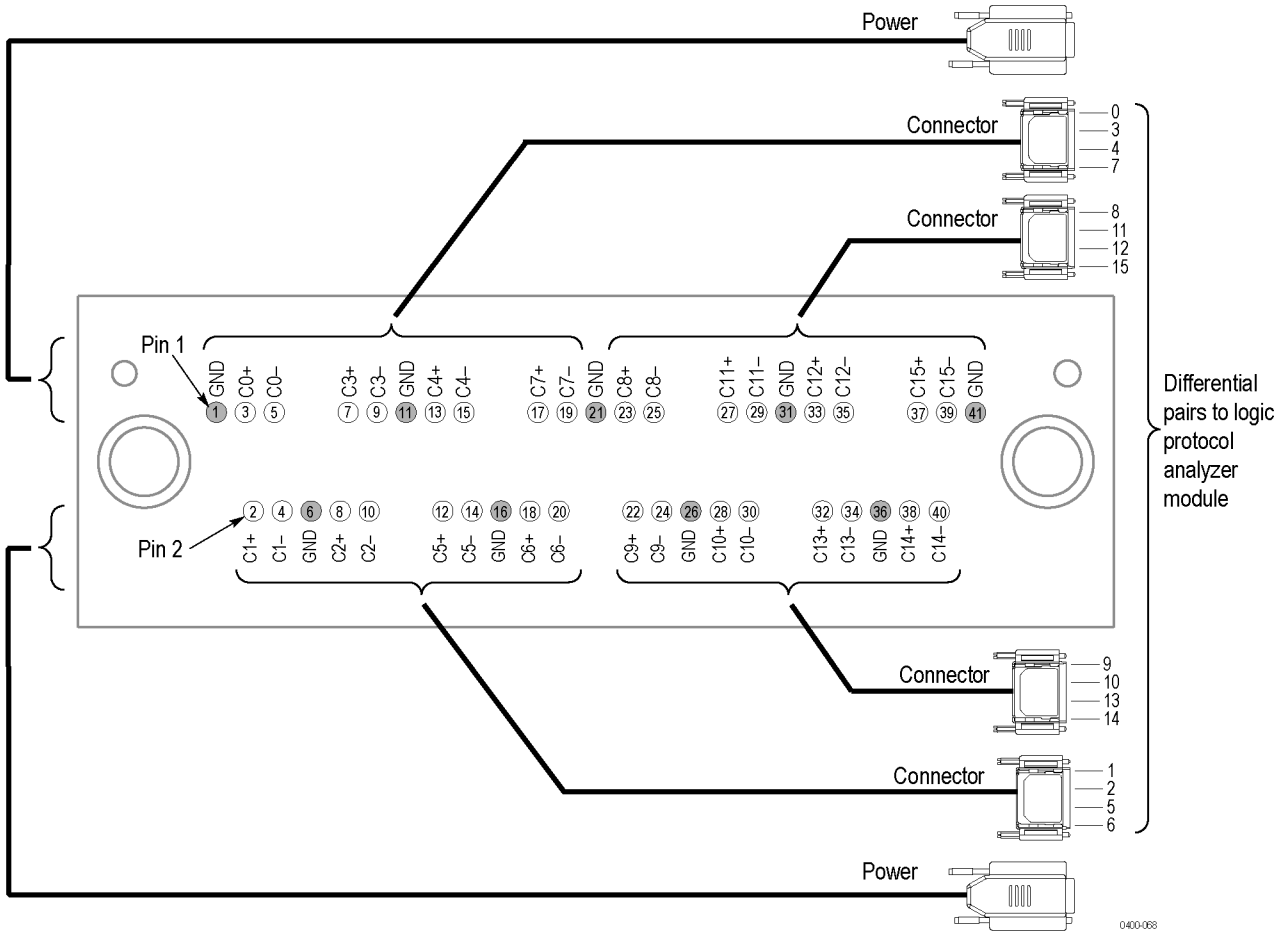


Figure 85: x8 midbus footprint connections for an upstream or downstream configuration

The following figure shows an example of footprints and pin assignments for the x8 midbus probes when used in an upstream *and* downstream configuration. (See Figure 86.)

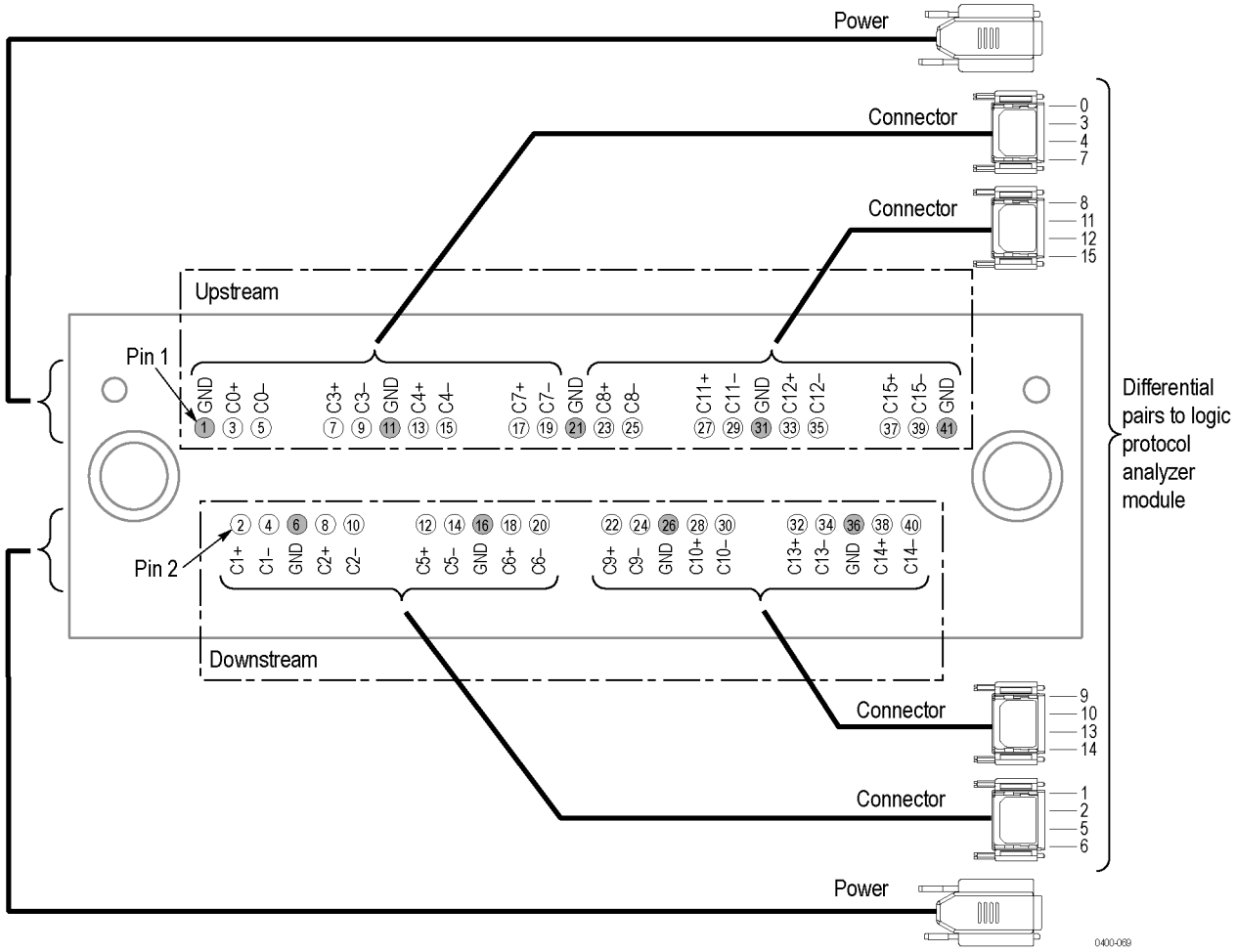


Figure 86: x8 midbus footprint connections in an upstream and downstream configuration

The following figure shows another example of footprints and pin assignments for the x8 midbus probes when used in an upstream *and* downstream configuration. (See Figure 87.)

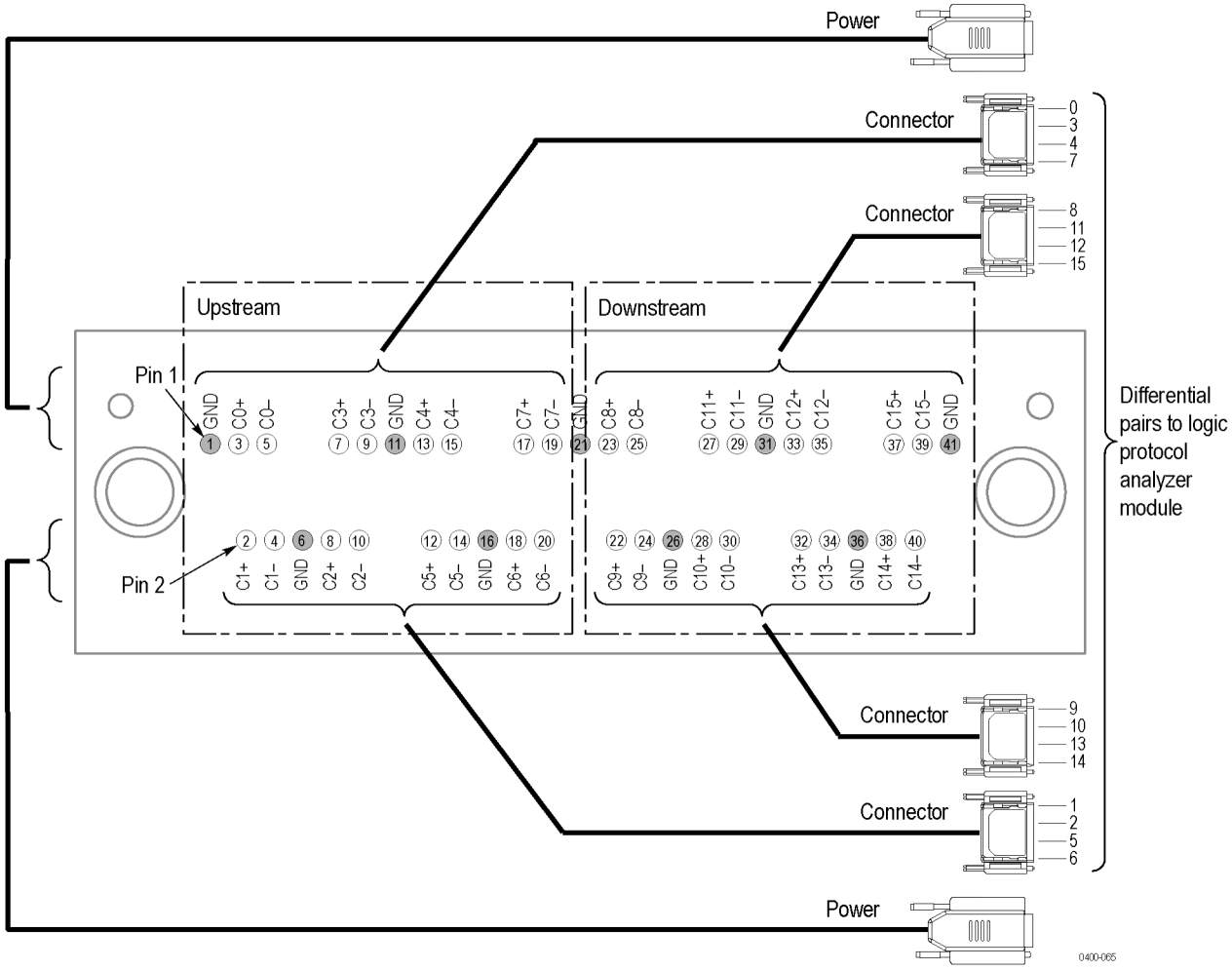


Figure 87: x8 midbus footprint connections for an upstream and downstream configuration

x4 PCI Express midbus pin assignments

The following figure shows an example of footprints and pin assignments for the x4 midbus probes when used in an upstream *or* downstream configuration. (See Figure 88.)

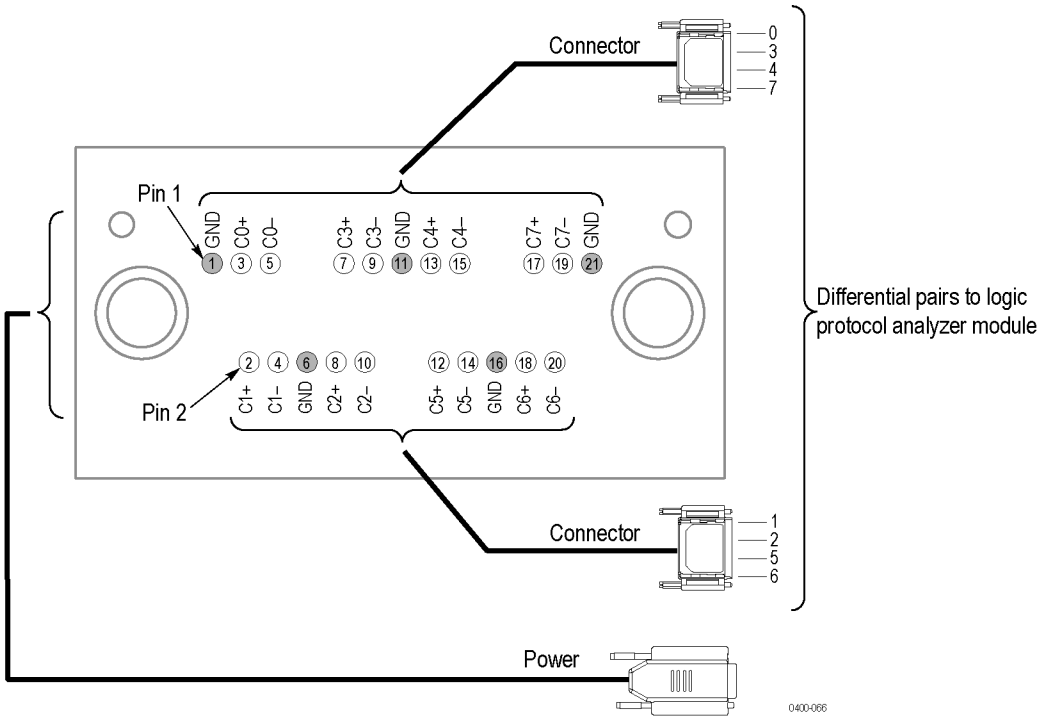


Figure 88: x4 midbus footprint connections for an upstream or downstream configuration

The following figure shows an example of footprints and pin assignments for the x4 midbus probes when used in an upstream *and* downstream configuration. (See Figure 89.)

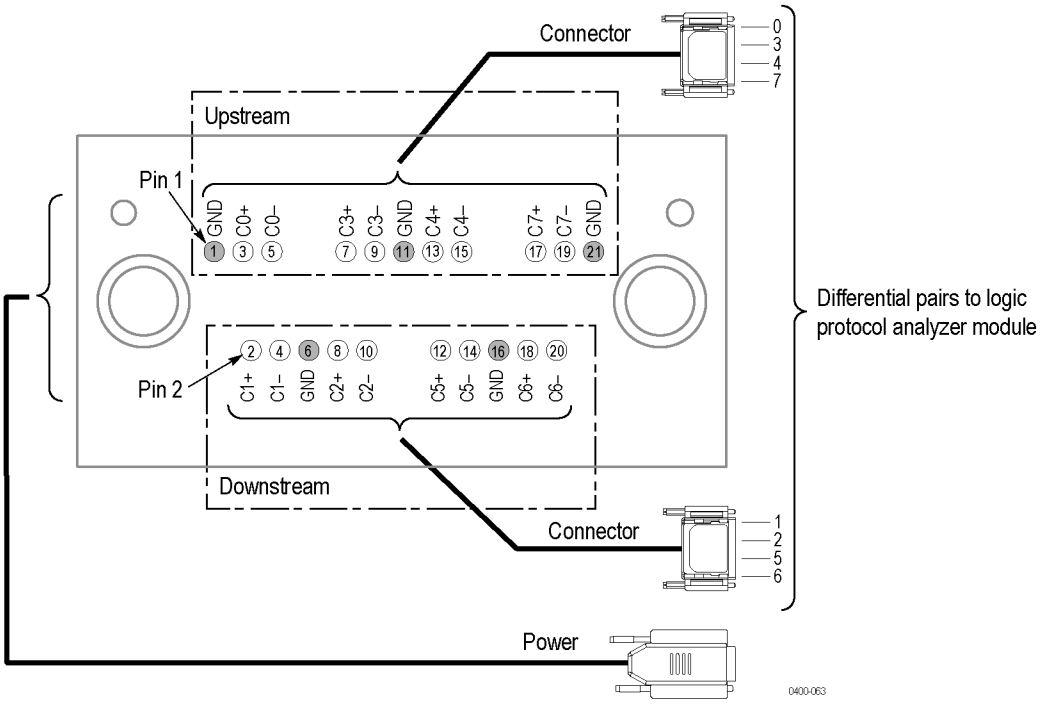


Figure 89: x4 midbus footprint connections for an upstream and downstream configuration

The following figure shows another example of footprints and pin assignments for the x4 midbus probes when used in an upstream *and* downstream configuration. (See Figure 90.)

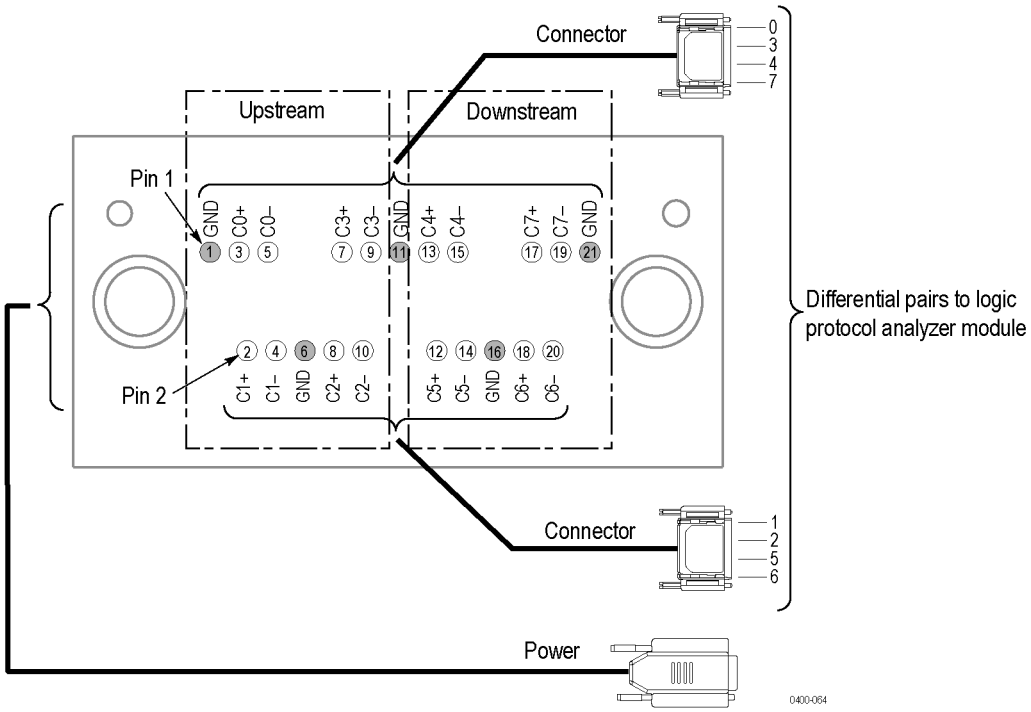


Figure 90: x4 midbus footprint connections for an upstream and downstream configuration.

P67SA16G2 x8 midbus probe pin assignments

The following figure shows the standard pin assignments for a PCIe2 x8-midbus footprint for use with the P67SA16G2 x8 Midbus probe. (See Figure 91.)

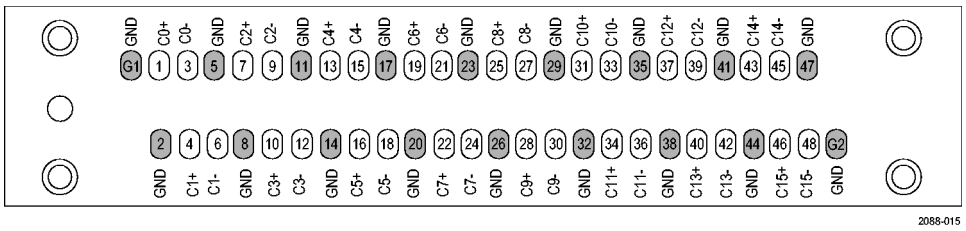


Figure 91: P67SA16G2 Midbus probe footprint pin assignments

The following figure shows the footprint connections from the probe head to the front panel probe connectors.

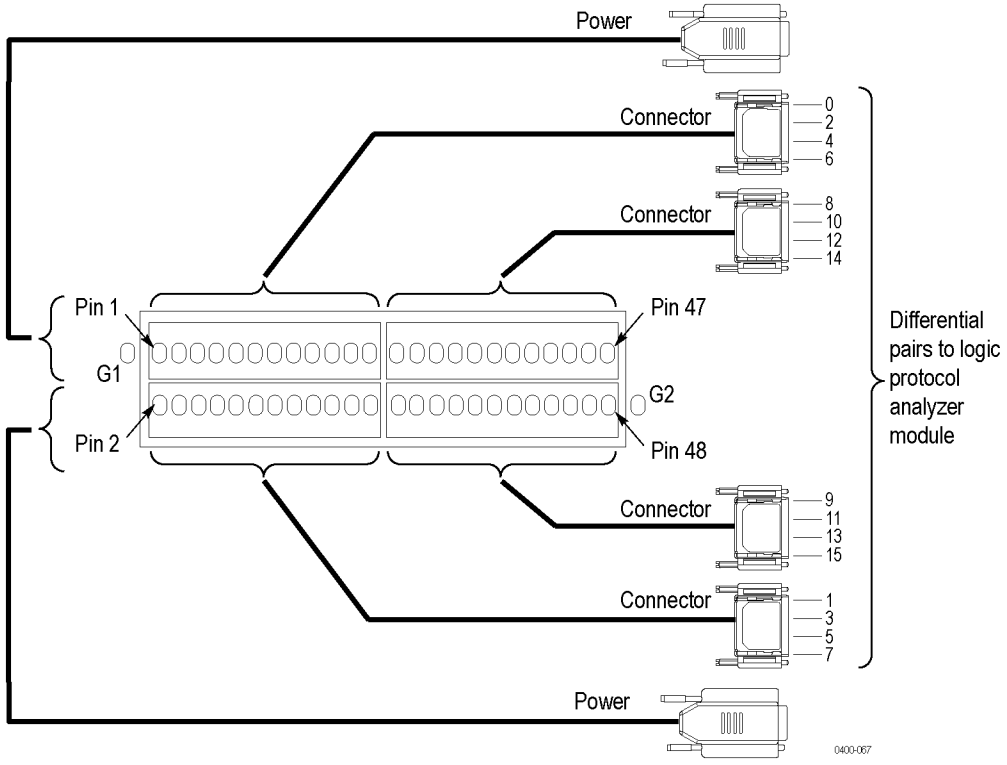


Figure 92: P67SA16G2 x8 Midbus footprint connections to module connectors

P67SA08G2 x4 midbus probe pin assignments

The following figure shows the standard pin assignments for a PCIe2 x4-Midbus footprint for use with the P67SA08G2 x4 Midbus probe. (See Figure 93.)

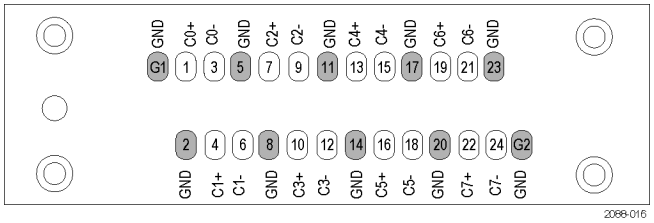


Figure 93: P67SA08 x4 midbus probe footprint pin assignments

The following figure shows the footprint connections from the probe head to the front panel probe connectors. (See Figure 94.)

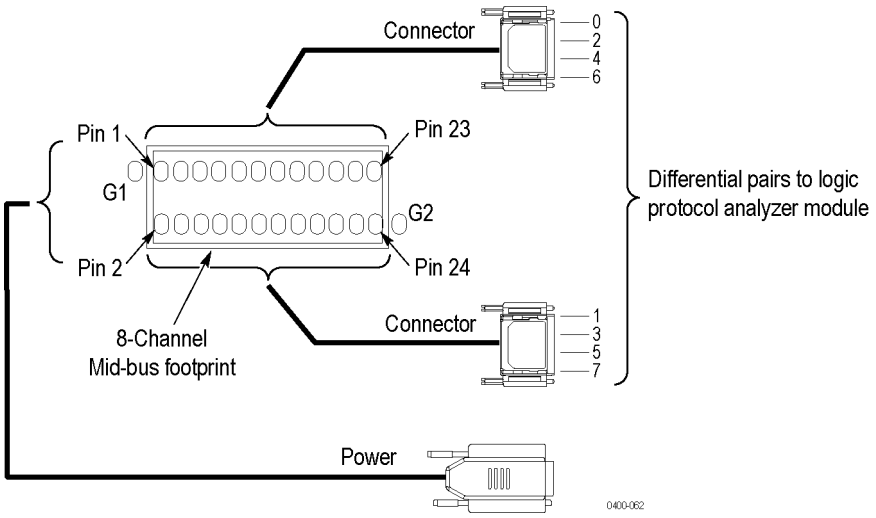


Figure 94: P67SA08G2 x4 midbus footprint connections to module connectors

Diagnostics

The logic protocol analyzer module performs power-on diagnostics each time you power on the mainframe. The Calibration and Diagnostics property sheet appears at power-on if one or more of the diagnostics fail.

Power-on diagnostics

Power-on diagnostics check basic functionality of the logic protocol analyzer at every power on. If any failures occur at power on, the screen displays the calibration and diagnostics property sheet.

NOTE. *When operating the TLA7000 Series mainframe from a remote location, the power-on diagnostics can be disabled in the TLA Connection dialog box. To run the power-on diagnostics, be sure to clear the Run Power-on Diagnostics check box in the dialog box before connecting to the TLA instrument.*

If there are no diagnostic failures when you power on the mainframe, display and run the calibration and diagnostics property sheet by selecting Calibration and Diagnostics from the System menu.

Extended diagnostics

The extended diagnostics execute more thorough tests than the power-on diagnostics. Using the extended diagnostics, do the following tasks:

- Run tests individually or as a group
- Run tests once or continuously
- Run tests until failures occur

To run the extended diagnostics, do the following steps:

1. Start the TLA application if it is not already running.
2. From the System menu, select Calibration and Diagnostics.
3. Select the Extended Diagnostics property page.
4. Select the individual tests, group of tests, or all tests.
5. Click Run to start the extended diagnostics.

While the tests are executing, the word Running displays adjacent to the tests. When the tests are complete, either a Pass or Fail indication displays adjacent to each test.

Troubleshooting

This section describes some high-level procedures to perform to isolate common problems with your logic protocol analyzer or probes.

General troubleshooting

The following table lists some common problems and possible causes. Contact your local Tektronix representative for additional help in resolving problems and, if necessary, repairing the module or probes.

CAUTION. *To avoid damaging the logic protocol analyzer module or the mainframe, be sure to power off the mainframe before removing or reinstalling any modules.*

Table 35: Failure symptoms and possible causes

Symptom	Possible cause(s)
Modules not recognized in the mainframe	■ Modules not fully inserted in the mainframe. Turn off the mainframe and make sure that the module is flush with the front panel of the mainframe. ■ Mainframe power supply failure. Contact your local Tektronix service center. ■ Corrupted module firmware or incorrect module firmware. Reinstall the module firmware. (See page 139, *Updating the logic protocol analyzer module firmware*.) ■ Module logical address switches on the rear of the module set to 00. Turn off the mainframe, remove the module and reset the switches to FF.
Module does not pass the normal power on diagnostics (READY indicator not green)	■ Modules not fully inserted in the mainframe. Turn off the mainframe and make sure that the module is flush with the front panel of the mainframe. ■ Module failure; contact your local Tektronix service center.

Table 35: Failure symptoms and possible causes (cont.)

Symptom	Possible cause(s)
Module loses settings when power is turned off	■ Module failure; contact your local Tektronix service center.
Module will not acquire data or the acquired data is incorrect	■ Faulty probe connections. Check the probe connections at the front of the module and at the SUT. ■ Incorrect probe calibration or incorrect AutoSample setting. Recalibrate the probes or check the AutoSample setting in the Setup window. ■ Faulty probe. See *Probe Troubleshooting*. ■ Module failure; contact your local Tektronix service center.

Probe troubleshooting

If the logic protocol analyzer module acquires no data or faulty data, the probes may be at fault. Perform the following procedure to isolate faults to a probe or to the module.

NOTE. *The following procedure requires that the mainframe is functional and operates normally when modules are installed.*

1. Verify that the probe is correctly connected to the module and to the SUT.
2. Move the suspected probe to another probe connection on the SUT and observe if the problem follows the probe. If the problem does not follow the probe, the module may be faulty.
3. Substitute the suspected probe with a known good probe and observe if the problem is still present. If the problem still occurs, the module may be faulty.

Using the P67UHDSMA Probe

The P67UHDSMA probe is available to help isolate problems to a probe or to your system. The probe allows you to quickly connect any of the probe connector outputs to an oscilloscope. It supports any of the P67SAxx series probes (midbus, slot interposer, or solder-down). Use the probe to do the following tasks:

- Verify the P67SAxx series probe functions properly and delivers the PCIe3 signals to the logic protocol analyzer module.
- Verify the PCIe3 signal meets the P67SAxx series probe input requirements.
- Verify the P67SAxx series probe is properly connected to the SUT.

NOTE. *File attachments are identified by a paperclip icon in the PDF file window. To access the attached files, open the PDF file and click on the paperclip icon on the lower-left side of the document viewer.*

Tektronix has provided DSP filter files (Midbus_UHDSMA_Fs50GHz.flt, Slot_UHDSMA_Fs50GHz.flt, and SolderDown_UHDSMA_Fs50GHz.flt) to help you troubleshoot possible probe problems. (See page 144, *DSP filter files for probe troubleshooting*.) Use the Tektronix-supplied DSP filter for your probe and module to configure the software filters of a Tektronix oscilloscope (DPO/DSA/MSO7000 20 GHz Analog Bandwidth, 50 GS/s Oscilloscope) to show the PCIe3 eye data. You can also use the Tektronix DPOJET application to provide advanced measurement and filter analysis of your PCIe3 waveforms.

Additionally, use the Tektronix SDLA (Serial Data Link Analysis) application to emulate your PCIe3 serial data channel, de-embed the PCIe3 probe, a fixture, or other network, and add or remove transmitter equalization.

The following illustrations show examples of the P67UHDSMA probe connected to two logic protocol analyzer modules in a TLA7012 Portable Mainframe through a P67SAxx series probe. The other end of the P67UHDSMA probe connect to the inputs of a Tektronix oscilloscope. The other end of the P67SAxx series probe is connected to the SUT.

There are eight leads from the P67UHDSMA probe, comprising of four differential connections. If you have access to four differential SMA probes (such as the Tektronix, P7313SMA probe), connect all four pairs to the oscilloscope. (See Figure 95 on page 133.) If you use single-ended oscilloscope inputs (such as the Tektronix TCA-SMA or the Tektronix TCA-292MM), connect up to two pairs to the oscilloscope at one time. (See Figure 96 on page 134.)

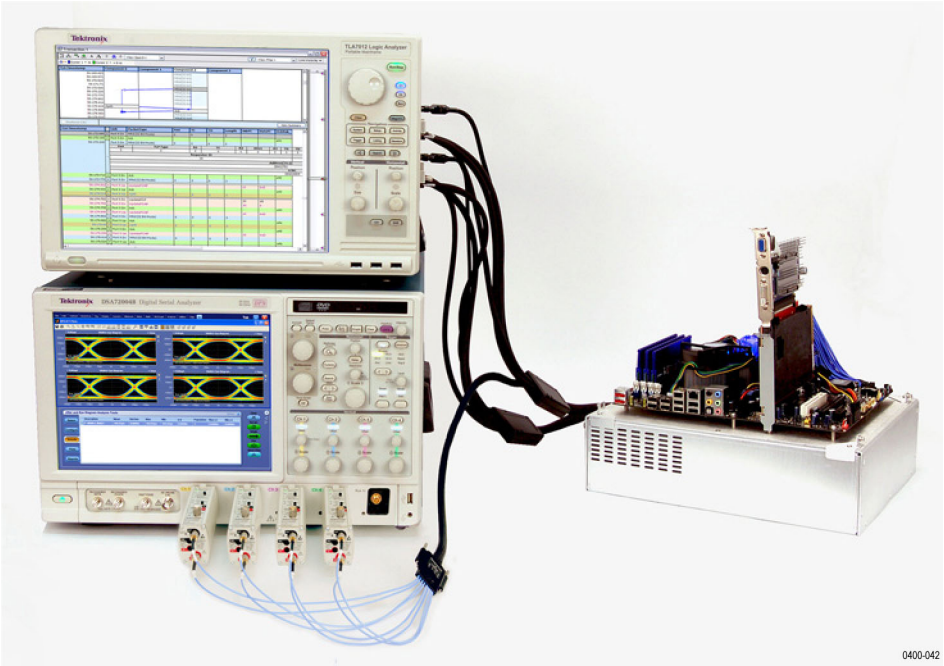


Figure 95: P67UHDSMA probe connected to the inputs of a Tektronix oscilloscope (example 1)

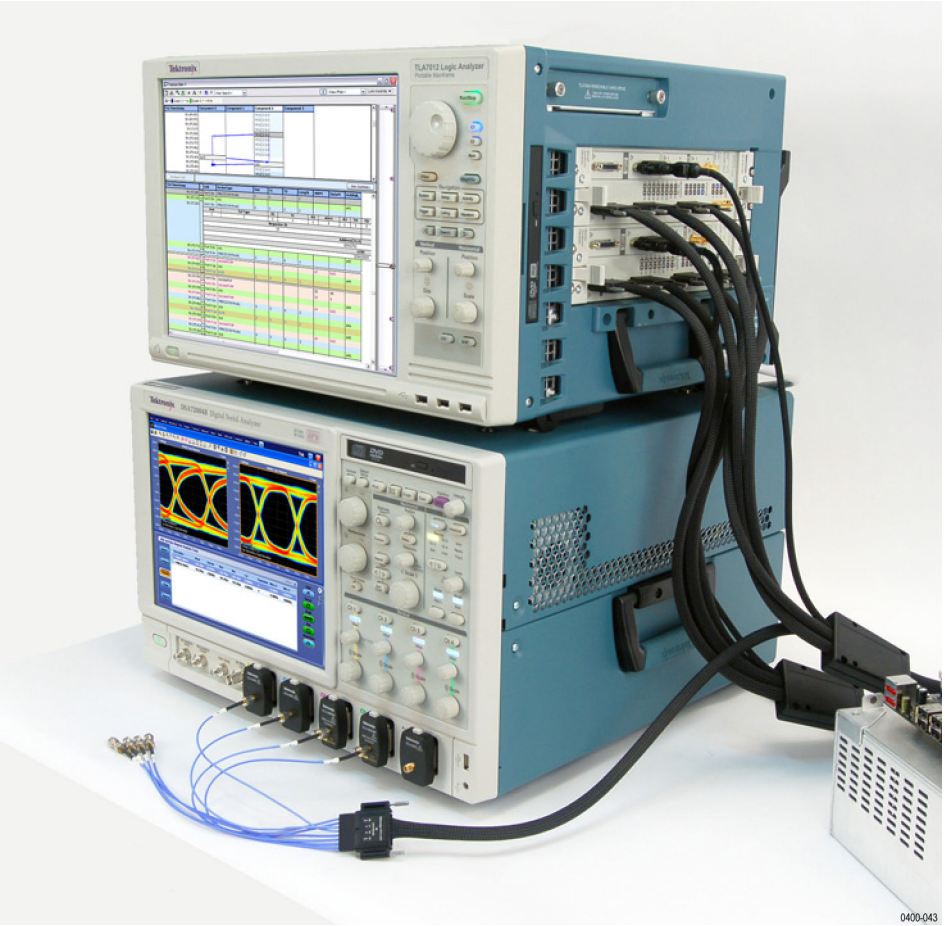


Figure 96: P67UHDSMA probe connected to the inputs of a Tektronix oscilloscope (example 2)

The following procedure describes how to use the P67UHDSMA probe with a P67SAxx series probe and a Tektronix oscilloscope.

NOTE. *Terminate all unused P67UHDSMA probe outputs to 50Ω; use the 50Ω terminators supplied with the P67UHDSMA probe.*

1. Disconnect the probe from the logic protocol analyzer inputs but leave the other end connected to the SUT. Do not disconnect the probe power connections from the logic protocol analyzer.
2. If you use the single-ended inputs, deskew the inputs following the standard procedure as described in your oscilloscope documentation.

   The output of each pair of inputs will be a math function defined by the difference of the two input channels (for example, Math1 = CH1 – Ch2).

3. Apply the DSP filter to the differential input waveform:

   a. Save the DSP filter file to a location to access with the oscilloscope (the default location for DSP filters on the Tektronix oscilloscope is: C:\TekScope\Math Arbitrary Filters).

   b. Start the Equation editor on the oscilloscope: Select **Math** > **Math Setup** and then click **Editor**.

   c. Use the drop-down menu at the left of the equation line to determine the math waveform that will contain the filtered waveform.

   d. Click the Filter tab and then click **Load** next the FLT1 button.

   e. Browse to the location of the DSP filter file and click **Open**.

      The selected filter will now be associated with the FLT1 button.

4. Click the FLT1 button to define a new waveform in the edit line using the active waveform. For example, use ArbFlt1(CH1) if Ch1 was the active waveform when you clicked the FLT1 button.

5. Edit the new line as appropriate. For example, the waveform to be filtered is on a different channel or the input waveform is the difference of two input channels Math1 = ArbFlt1(Ch1 – Ch2).

6. Click **Apply**.

   The new waveform should appear on the oscilloscope.

The DSP filters are only valid for waveforms sampled at 50 Gs/s and greater than 1000 samples in length. If either of these two conditions are not met, the waveform will be defined, but will not appear on the oscilloscope.

To ensure that the above two conditions are met, set the Horizontal mode of the oscilloscope to Manual, the Sample Rate to 50 Gs/s, and the Record Length to 10 k or greater. Use the Windowing function of the oscilloscope to view a shorter duration section of the filtered waveform.

Care and maintenance

Inspection and cleaning are done as preventive maintenance. Preventive maintenance, when done regularly, may prevent malfunctions and enhance reliability.

Preventive maintenance consists of visually inspecting and cleaning the instrument, and using general care when operating it. How often to perform maintenance depends on the severity of the environment in which the instrument is used. A proper time to perform preventive maintenance is during an incoming inspection.

Exterior inspection

Inspect the outside of the instrument for damage, wear, and missing parts. (See Table 36.) Instruments that appear to have been dropped or otherwise abused should be checked thoroughly to verify correct operation and performance.

Contact your local Tektronix representative to repair any defects. In particular, immediately repair any defects that can cause personal injury or lead to further damage to the logic protocol analyzer module or mainframe where it is used.

Table 36: Internal inspection checklist

Item	Inspect for
Front panel and side cover	Cracks, scratches, deformations, missing or damaged retainer screws, ejector handles, or EMI shields.
Front panel connectors	Broken shells, cracked insulation, and deformed contacts. Dirt in connectors.
Rear connectors	Cracked or broken shells, damaged or missing contacts. Dirt in connectors.
Accessories	Missing items or parts of items, bent pins, broken or frayed cables, and damaged connectors.

Inspection and cleaning

Inspect and clean the instrument as often as operating conditions require. Collection of dirt on internal components can cause them to overheat and breakdown. Dirt acts as an insulating blanket, preventing efficient heat dissipation. Dirt also provides an electrical conduction path that can cause failures, especially under high-humidity conditions.

CAUTION. *Avoid using chemical cleaning agents that might damage the plastics and external labels used in the instrument.*

Use a cloth dampened with water to clean external surfaces. To prevent damage to electrical components from moisture during external cleaning, use only enough liquid to dampen the cloth or applicator.

Keep the probes free of dirt, dust, and contaminants to maintain a reliable electrical probe connection.

Clean the exterior module

To clean the exterior of the module, perform the following steps:

1. Remove loose dust on the outside of the module with a lint free cloth.
2. Remove remaining dirt with a lint-free cloth or applicator and water, using only enough liquid to dampen the cloth or applicator. Do not use abrasive cleaners.

CAUTION. *To avoid electrical damage, always power off your SUT before cleaning the retention mechanism.*

Clean the probe retention mechanism

If the retention mechanism appears to be dirty, remove any lint using a nitrogen air gun or clean, oil-free dry air.

Clean the probes

To clean the exterior surfaces of the probes, remove dirt and dust with a soft brush. For more extensive cleaning, use only a damp cloth. Never use abrasive cleaners or organic solvents.

CAUTION. *Static discharge can damage any semiconductor component in the probe head. Always wear a grounded antistatic wrist strap whenever handling the probe head. Also verify that anything to which the probe head is connected does not carry a static charge.*

Clean the probe head

Remove any lint using a nitrogen air gun or clean, oil-free dry air. Avoid brushing or rubbing the contacts. Never use abrasive cleaners or organic solvents.

Store the probe

When not in use, store the probes in the Tektronix-supplied transport case.

Repackage the probe

Use the original packaging, if possible, to return or store the probe. If the original packaging is not available, use a corrugated cardboard shipping carton. Add cushioning material to prevent the probe from moving inside the shipping container.

Enclose the following information when shipping the probe to a Tektronix Service Center:

- Owner's address
- Name and phone number of a contact person
- Type of probe
- Reason for return
- Full description of the service required

Appendix A: TLA application software

The TLA application software is available on the CDs that get shipped from the factory. You can also download the latest version of the software from the Tektronix Web site (www.tektronix.com/software). The logic protocol analyzer requires TLA application Software V6.1 or higher.

To install the software from the Tektronix Web site:

1. Go to the Tektronix Web site at www.tektronix.com/software and search for your software.
2. Follow the on-screen instructions.

Updating the logic protocol analyzer module firmware

After you install the software and restart the instrument, a message may appear on the screen indicating that your current module firmware is unsupported by the currently installed logic protocol analyzer software. A new of the firmware must be installed on the instrument so that it will work with the latest TLA PCI Express Support software.

1. If you have not already done so, exit the TLA application.
2. Click Start >All Programs > Tektronix Logic Analyzer > TLA Firmware Loader.
3. Select your mainframe instrument from the TLA Connection dialog box.

   You are given a choice to load Mainframe or Instrument Module Firmware. Click the Load button in the Instrument Module Firmware section (bottom part of the dialog box).
4. You may be prompted about cycling the power on the mainframe after completing the upgrade operation. Click Yes to continue.

   The instrument will scan the mainframe to detect all installed modules, and to determine which modules have firmware that needs to be upgraded.
5. Select your module(s) from the list displayed in the Supported list box near the top of the window. If you are updating the firmware for more than one module, note the locations of the modules in the mainframe and select them from the list.
6. Select Load Firmware from the Execute menu.
7. Navigate to C:\Program Files\TLA 700\Firmware and select the TLA7SAxx.lod file.

NOTE. *Be sure to correctly associate your module with this file. Note the slot number in the title bar so that you select the correct module.*

8. Click OK. You will be prompted to confirm your action; click Yes.

   The program will begin to load the firmware. The process may take several minutes.

9. When the process is complete, the firmware is loaded for the module. Exit the firmware loader program and power off the instrument. You must power off the instrument to allow the software application to start up properly.

Appendix B: File attachments

This appendix provides information on the file attachments available for your use. The files are attached to the PDF version of this document. To access the attached files, open the PDF file and click on the paperclip icon on the lower-left side of the document.

Probe electrical simulation models

The following table lists probes and the associated S-parameter and load model files that are attached to the PDF file of this document.

NOTE. *Use the Short_Channel.s6p Touchstone® data files for most PCIe signals. Use the Long_Channel.s6p Touchstone® data files for signals where the midbus or slot interposer probe is over 18 inches from the transmitter.*

Table 37: Probes and related electrical simulation models

Probes	Simulation models
P67SA08, P67SA16 Midbus probes	P67SAxx_Short_Channel_Model.s6p
	P67SAxx_Long_Channel_Model.s6p
P67SA16G2 x8 Midbus probe	P67xx_wop.s2p (simulation without the probe)
P67SA08G2 x4 Midbus probe	P67xx_2wp.s2p (simulation with the probe)
P67SA01S, P67SA04S, P67SA08S, P67SA16S Slot Interposer probes	P67SAxxS_Short_Channel.s6p
	P67SAxxS_Long_Channel.s6p
P67SA01SD Solder Down probe	P67SA01SD.s4p

For additional information on using the simulation models, refer to the following sections in this document:

- (See page 112, *P67SAxx midbus probe circuit impact*.)
- (See page 113, *P67SA16G2 x8 or P67SA08G2 x4 Midbus probe circuit impact*.)
- (See page 114, *P67SAxx slot interposer probe circuit impact*.)
- (See page 115, *P67SA01SD Solder-Down Probe circuit impact*.)

NOTE. *Contact your local Tektronix Representative for additional information on the file attachments.*

Midbus probe CAD symbols for PCB layout

The following table lists the PCB layout programs and the compatible CAD symbols to use when designing layouts for the P67SA08 x4 Midbus probes and P67SA16 x8 Midbus probes.

Table 38: Midbus probe CAD symbols for PCB layout

PCB layout programs	CAD symbols
Cadence® Allegro® Version 16.01 or greater [1]	sjr_pcie_gen3_x4.dra
	sjr_pcie_gen3_x4.psm
	sjr_pcie_gen3_x8.dra
	sjr_pcie_gen3_x8.psm
	15c33n.pad
	25c.pad
	25c35n.pad
	25c93n.pad
Other PCB layout programs that support import of CAD symbols in either .dxf or .igs format	pcie_gen3_x4_footprint.dxf
	pcie_gen3_x4_footprint.igs
	pcie_gen3_x8_footprint.dxf
	pcie_gen3_x8_footprint.igs

[1] Each probe has a land pattern that consists of the .dra and .psm files with respective x4 and x8 file names. They both use the same pad stacks (.pad files).

Midbus probe 3D CAD models

The following table lists the 3D CAD solid models to use when designing layouts for the P67SA08 x4 Midbus probes, P67SA08G2 x4 Midbus probes, P67SA16 x8 Midbus probes, and P67SA16G2 x8 Midbus probes. The files are step (.stp) files available for use with most 3D design programs.

Table 39: Midbus probe 3D CAD models

PCB layout programs	CAD symbols
Bolster plate models	pcie_gen3_x4_bolster.stp
	pcie_gen3_x8_bolster.stp
Retention mechanism models	pcie_gen3_x4_retention.stp
	pcie_gen3_x8_retention.stp
	pcie_gen2_x4_retention.stp [1]
	pcie_gen2_x8_retention.stp [1]
Probe models	pcie_gen3_x4_probe.stp
	pcie_gen3_x8_probe.stp
	pcie_p67sa08_x4_probe.stp
	pcie_p67sa16_x8_probe.stp

[1] The pcie_gen2_x4_retention.stp and pcie_gen2_x8_retention.stp files support the geometry of the PCIe2 (CLGA) sockets to go with the P67SA08G2 and P67SA16G2 midbus probes.

For additional information on using the 3D CAD solid models, refer to the following sections in this document:

- (See page 84, *P67SA08 Midbus probe head dimensions*.)
- (See page 85, *P67SA08G2 Midbus probe head dimensions*.)
- (See page 86, *P67SA16 Midbus probe head dimensions*.)
- (See page 87, *P67SA16G2 Midbus probe head dimensions*.)

NOTE. *Contact your local Tektronix Representative for additional information on the file attachments.*

Slot interposer probe 3D CAD models

The following table lists the 3D CAD solid models to use when designing layouts for the P67SxxS slot interposer probes. The files are setp (.stp) files available for use with most 3D design programs.

Table 40: Slot interposer probe 3D CAD models

PCB layout programs	CAD symbols
Probe models	pcie_x16_slot_probe.stp
	pcie_x8-x4-x1_slot_probe.stp

For additional information on using the 3D CAD solid models, refer to the following sections in this document:

- (See page 88, *P67SA16 Slot Interposer Probe dimensions*.)
- (See page 89, *P67SA08S, P67SA04S, and P67SA01S Slot Interposer Probe dimensions*.)

NOTE. *Contact your local Tektronix Representative for additional information on the file attachments.*

DSP filter files for probe troubleshooting

The following table lists the probes and the associated DSP filter file for each probe type that are attached to the PDF file of this document. Use these files with an external Tektronix oscilloscope to troubleshoot possible probe problems.

Table 41: Probes and related DSP filter files

Probes	Filter files
P67SA08, P67SA16 Midbus probes	Midbus_UHDSMA_Fs50GHz.flt
P67SA01S, P67SA04S, P67SA018S, P67SA16S Slot Interposer probes	Slot_UHDSMA_Fs50GHz.flt
P67SA01SD Solder Down probe	SolderDown_UHDSMA_Fs50GHz.flt

For information on using the DSP filter files, refer to the following sections in this document:

- (See page 131, *Using the P67UHDSMA Probe*.)

Appendix C: Installing the midbus retention mechanism

Cleaning the footprint

Inspect the footprint for lint, oil, or fingerprints. If the footprint is dirty, clean it by following these steps:

CAUTION. *To avoid electrical damage, always power off your system under test before cleaning the footprint.*

1. Use a lint-free, clean-room cloth lightly moistened with electronic/reagent grade isopropyl alcohol, and gently wipe the surface of the footprint.
2. Remove any remaining lint using a nitrogen air gun or clean, oil-free dry air.

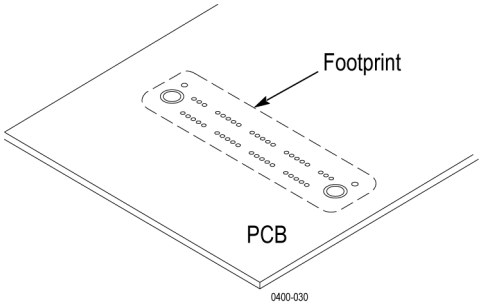


Figure 97: x8 footprint

Installing the midbus retention mechanism

Before connecting a midbus probe, you must install the retention mechanism on the circuit board. The retention mechanism connects the probe head to your circuit board. The installation procedures differ depending on your midbus probe; use the correct procedure for your probe type.

Installing the retention mechanism for the P67SA08 or P67SA16 Midbus probes

To install the retention mechanism for the P67SA08 or P67SA16 Midbus probes, complete the following steps. Refer to the illustrations as necessary. (See Figure 98 on page 147.) (See Figure 99 on page 148.)

1. Locate the correct footprint. If you intend to use multiple probes, your PCB has multiple footprints. Be careful to select the correct one.
2. Align the retention housing over the footprint so that the keying pins on the retention mechanism line up with the keying pin holes on the footprint.
3. Insert the retention housing into the holes in the footprint on the PCB.
4. Install the bolster plate on the bottom side of the PCB so that it aligns with the footprint and the retention housing.
5. Note the circuit board thickness. If the thickness is greater than 3.56 mm (0.140 in), use the longer, black screws provided in the kit.
6. Tighten the screws on the bolster plate to secure the retention mechanism in place. Use the provided hex key in the low-torque orientation. Proper installation torque is 1.5 in-lbs.

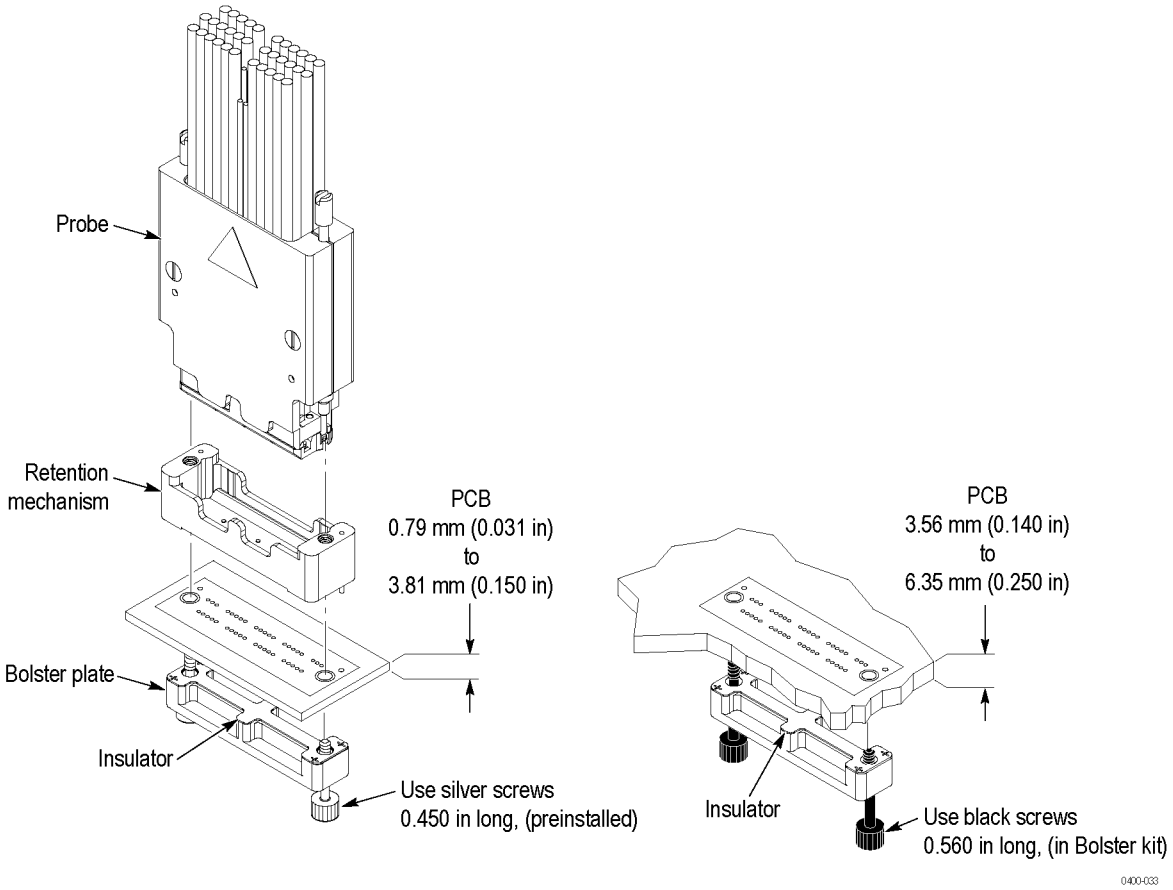


Figure 98: Connecting the P67SA16 midbus probe to the retention mechanism on the circuit board

Table 42: P67SA16 x8 Midbus probe retention assembly kit

Tektronix part number	Description
020-4016-00	x8 Retention assembly consisting of:
131-8616-00	x8 Retention Module
020-3056-00	x8 Bolster Assembly, consisting of: 386-7581-00, 1 x8 Bolster plate, black anodized aluminum 342-1209-00, 1 x8 Bolster plate insulator, Lexan 211-1332-00, 2 silver screws for PCBs 0.031 in to 0.150 in 211-1332-00, 2 black screws for PCBs 0.140 in to 0.250 in 1 wrench, L-Key, $^{1}/_{16}$ Hex

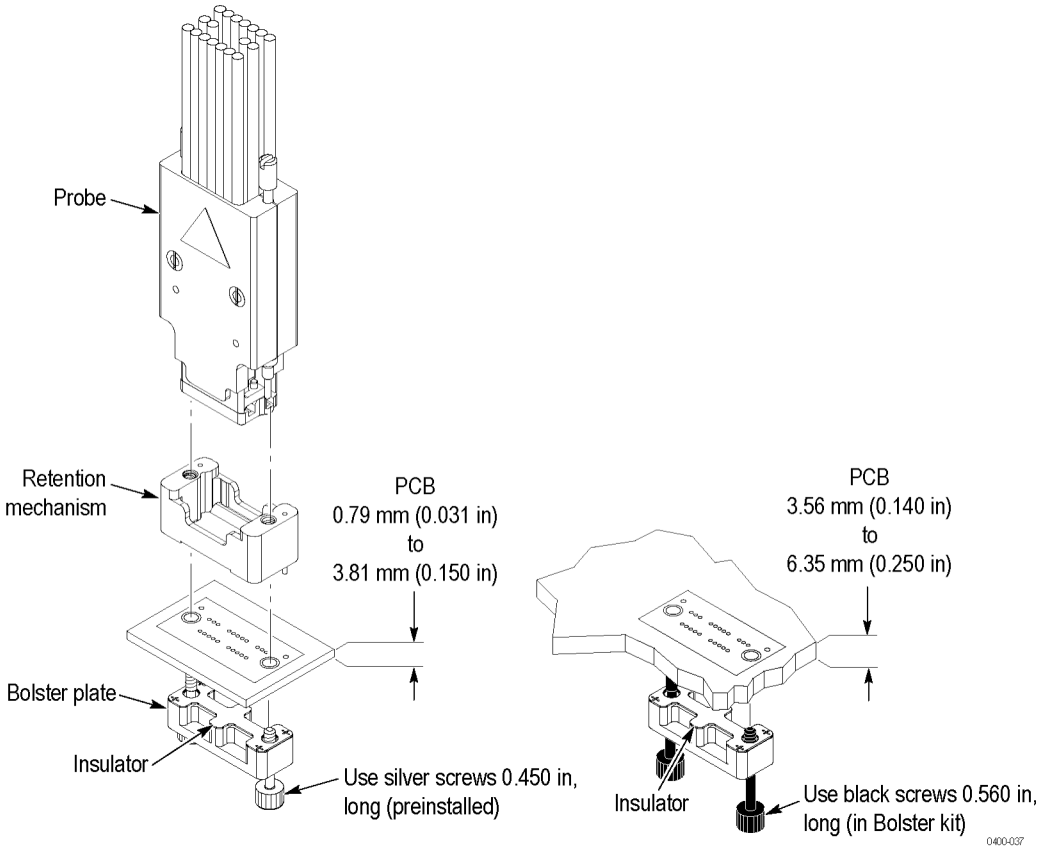


Figure 99: Connecting the P67SA08 midbus probe to the retention mechanism on the circuit board

Table 43: P67SA08 x4 Midbus probe retention assembly kit

Tektronix part number	Description
020-4008-00	x4 Retention assembly consisting of:
131-8617-00	x4 Retention Module
020-3057-00	x4 Bolster Assembly, consisting of: 386-7582-00, 1 x4 Bolster plate, black anodized aluminum 342-1210-00, 1 x4 Bolster plate insulator, Lexan 211-1332-00, 2 silver screws for PCBs 0.031 in to 0.150 in 211-1332-00, 2 black screws for PCBs 0.140 in to 0.250 in 1 wrench, L-Key, $^{1}/_{16}$ Hex

Installing the retention mechanism for the P67SA16G2 x8 or P67SA08G2 x4 Midbus probes

The retention mechanism for the P67SA16G2 x8 Midbus probe or the P67SA08G2 x4 Midbus probe fits on the PCIe2 footprint and must be soldered to the circuit board. To install the retention mechanism on the circuit board, do the following steps:

1. Locate the correct footprint. If you intend to use multiple probes, your PCB has multiple footprints. Be careful to select the correct one.
2. Align the retention mechanism over the footprint so that the keying pin on the retention mechanism lines up with the keying pin hole on the footprint. (See Figure 100.)
3. Insert the retention mechanism into the holes in the footprint on the circuit board.

NOTE. *The following two steps are important to ensure that the retention mechanism is correctly mounted and that the probe makes proper contact with the circuit board.*

4. Hold the retention mechanism so that it is firmly flush with the surface of the footprint, and the four anchoring posts extend through the circuit board to the opposite side.
5. Using a pair of needle-nose pliers, grasp one of the posts. Using the circuit board hole as a fulcrum, bend the post outward so that it secures the mechanism to the circuit board. Bend the other three posts in the same manner.

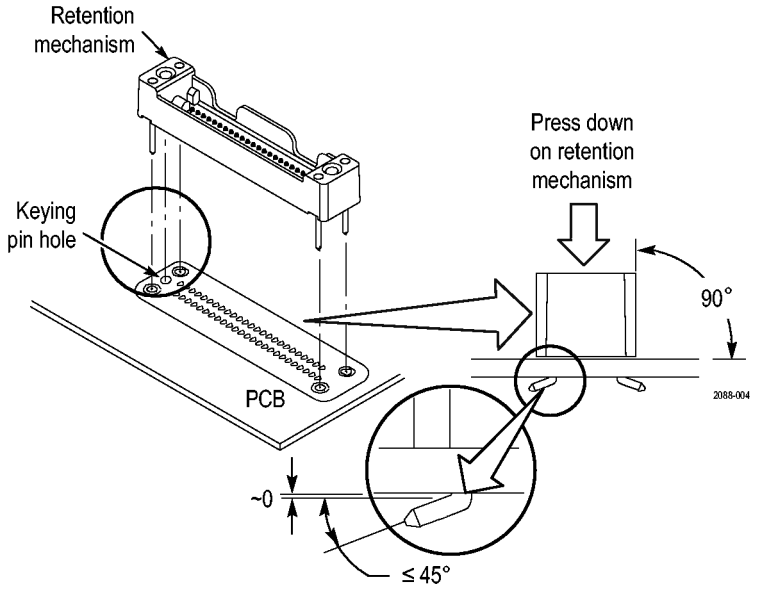


Figure 100: Installing the retention mechanism

6. Solder the anchoring posts to the circuit board.

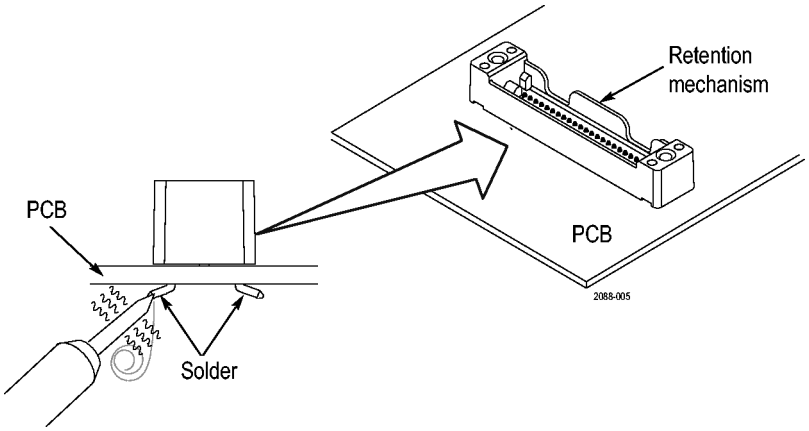


Figure 101: Soldering the anchoring posts to the circuit board (PCB)

Table 44: P67SA16G2 x8 Midbus probe retention assembly kit

Tektronix part number	Description
020-2784-00	P67SA16G2 x8 Midbus probe retention assembly kit, full width (50 contacts)
131-7941-00	Retention assembly, full width (50 contacts), long wires with integrated CLGA contact

Table 45: P67SA08G2 x4 Midbus probe retention assembly kit

Tektronix part number	Description
020-2785-00	P67SA08G2 x4 Midbus probe retention assembly kit, half-width (26 contacts)
131-7951-00	Retention assembly, half-width (26 contacts), long wires with integrated CLGA contact

Appendix D: System design review checklist

Use the following tables as a guide to review your system design.

General considerations

Your system design must allow you to physically connect a midbus, slot interposer, or solder-down probe to each of the links in the system. If this seems impossible, contact your local Tektronix representative for an alternative solution.

Midbus probe configuration

Table 46: Midbus probe configuration

Pass	Fail	N/A	Description
☐	☐	☐	Each midbus footprint is configured according to one of the pin assignment formats recommended in this manual. [1]
☐	☐	☐	A reference clock cable connector (if required) is provided for each PCI Express reference clock domain. [2]
☐	☐	☐	All reference clocks are properly terminated in the system.

1 If your design requires you to use a pin assignment that is not recommended, please contact your local Tektronix representative for help.

2 A reference clock connector is required if SSC (spread-spectrum clocking) is enabled or can not be disabled. A reference clock connector is also required if the link frequency is intentionally margin tested outside the standard +/-150 ppm tolerance, or the link reference operates outside the +/-150 ppm tolerance imposed by the current tools.

Mechanical considerations

Table 47: Midbus probe

Pass	Fail	N/A	Description
☐	☐	☐	Each midbus footprint is designed according to the specifications provided in this document, including:
☐	☐	☐	Pad size, spacing, arrangement
☐	☐	☐	Hole sizes, locations, tolerance, plating
☐	☐	☐	Solder mask requirements
☐	☐	☐	Pad plating requirements
☐	☐	☐	Pin numbering

Table 47: Midbus probe (cont.)

Pass	Fail	N/A	Description
☐	☐	☐	Footprint keep-out requirements
☐	☐	☐	Probe keep-out requirements
☐	☐	☐	Egress for probe cables is provided.

Table 48: Slot interposer probe

Pass	Fail	N/A	Description
☐	☐	☐	System design provides the physical space needed for the probe and the PCI Express add-in card that plugs into the probe, including:
☐	☐	☐	Probe keep-out requirements
☐	☐	☐	Egress for probe cables is provided.
☐	☐	☐	Any special requirements (cables, add-ons) for the PCI Express card have been met.
☐	☐	☐	The thermal requirements of the PCI Express card have been met. (The card will be out of its normal position when the interposer probe is installed.)
☐	☐	☐	If a reference clock is provided on the PCI Express card, verify that it meets the reference clock probe keep-out requirements while connected to the probe.

Table 49: Reference clock connector

Pass	Fail	N/A	Description
☐	☐	☐	Each reference clock connector matches the specifications in this manual, including:
☐	☐	☐	Verify that the dimensions are equivalent to the suggested part specification for either the SMT connector (Samtec FTR-103-02-S-S) or the through-hole connector (Samtec TMS-103-02-S-S). Check pad and hole size, spacing, arrangement, etc.
☐	☐	☐	Verify pin assignment (Pin 1 = REFCLKp or REFCLKn, Pin 2 =GND, Pin3 = REFCLKn or REFCLKp.)
☐	☐	☐	Verify that adequate space exists on the board. Review the reference clock keep-out requirements in this manual.
☐	☐	☐	Verify that egress for reference clock cables is provided.

Electrical considerations

Table 50: Midbus probe

Pass	Fail	N/A	Description
☐	☐	☐	System loss and jitter due to the footprint has been calculated and the values meet the requirements for the TLA7SA08 and TLA7SA16 Logic Protocol Analyzer modules.
☐	☐	☐	The requirements for AC coupling capacitor location have been met. (Each pair of capacitors may be placed on either side of the midbus footprint for each differential signal pair, but the location relationship can be varied for different differential pairs in the link.)
☐	☐	☐	For each link probed, system simulations have been performed with load models included in order to verify that the system will work with midbus probes attached. Verify that the loss and jitter at the system receivers is within specifications when the probe load is present.
☐	☐	☐	For each link probed using a midbus footprint, system simulations have been performed with the footprint load model included in order to verify that the system will work with the footprint *without* the probe attached
☐	☐	☐	The end of the PCIe link is terminated with an active or passive PCIe card. If the link does not end at a PCIe slot, use on-board termination resistors to provided the correct termination.
☐	☐	☐	The system layout follows the guidelines in this manual, including:
☐	☐	☐	Via and trace requirements
☐	☐	☐	Differential pair routing (matched length, identical paths/vias, etc.)
☐	☐	☐	Pin assignment of each midbus footprint matches a suggested format provided in this manual:
☐	☐	☐	All signals of a single direction of a link connect to the same footprint. It is preferable (but not required) that both directions of a link connect to the same footprint.

Table 51: Slot interposer probe

Pass	Fail	N/A	Description
☐	☐	☐	For each PCI Express slot that supports the use of an interposer, loss and jitter at the card connector has been calculated and the values meet the requirements for the TLA7SA08 and TLA7SA16 Logic Protocol Analyzer modules.
☐	☐	☐	For each PCI Express slot probed, system simulations have been performed with slot interposer probe load models included in order to verify that the system will work with a slot interposer probe connected.
☐	☐	☐	Loss and jitter at the system receivers is within spec when the slot interposer probe load is included.
☐	☐	☐	The end of the PCIe link is terminated with an active or passive PCIe card. If the link does not end at a PCIe slot, use on-board termination resistors to provided the correct termination.

Table 52: Reference clock connector

Pass	Fail	N/A	Description
☐	☐	☐	Reference clock electrical requirements have been met, including:
☐	☐	☐	Differential voltage requirements
☐	☐	☐	Absolute voltage requirements
☐	☐	☐	Frequency requirements
☐	☐	☐	Simulations of the reference clock network(s) have been performed using load models for the reference clock connector to ensure good signal integrity to the logic protocol module.

Appendix E: Rearranging wires in the probe connector

If your design is not consistent with the previous link configuration recommendations, you must disassemble and rewire the connectors at the module end of the probe.

The wires can be rearranged in any way as long as you observe the following guidelines:

- x16 links require two x8 modules, and each side of the link must have all of the lanes grouped together on the module end connectors (upstream with upstream and downstream with downstream).
- The midbus footprint can have multiple links on it, but the module end connectors must have less than x16 links.

A module can handle a single link of x8, x4, x2, or x1 with no routing restrictions to the module end connectors.

If you have questions or concerns about reordering the wires in the probe, please contact a Tektronix support representative.

NOTE. *You can only rearrange wires in the connector at the module end of the probe, not in the probe head.*

1. Press gently on either side of the connector to snap off the cover. You will see that each of the wires is labeled. Identify the wire you want to remove from the connector.

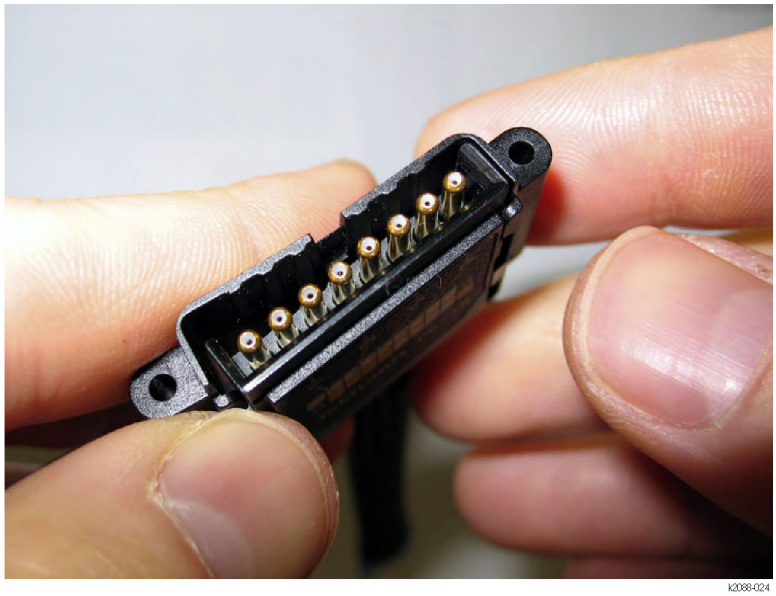


Figure 102: Opening the probe connector

2. Remove the probe sleeve anchor from the connector, and pull the sleeve away from the connector so that the wire labels are exposed.

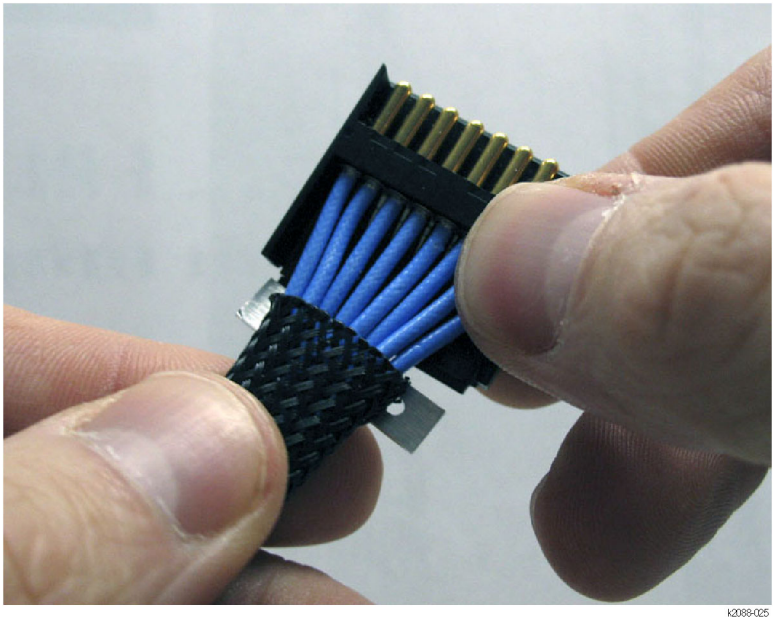


Figure 103: Removing the probe sleeve

3. Use the labels on the wires to determine the new order for the wires in the connector.

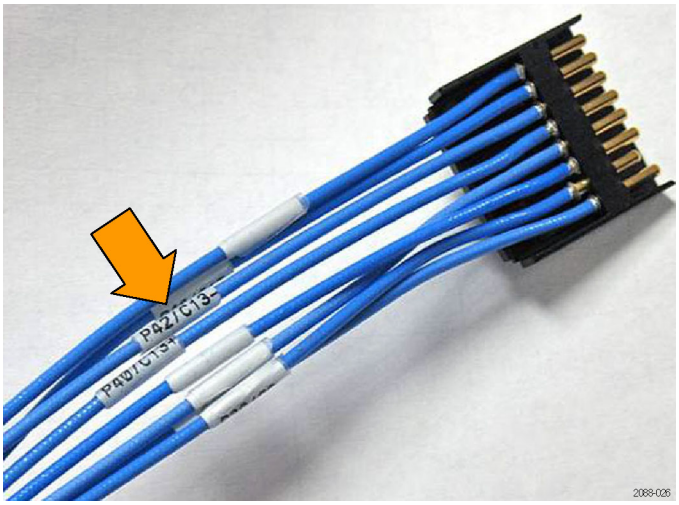


Figure 104: Probe labels

4. Use a bent paper clip (or similar tool) to press downward on the plastic retainer in the connector until the wire slides out. Repeat for the second wire.

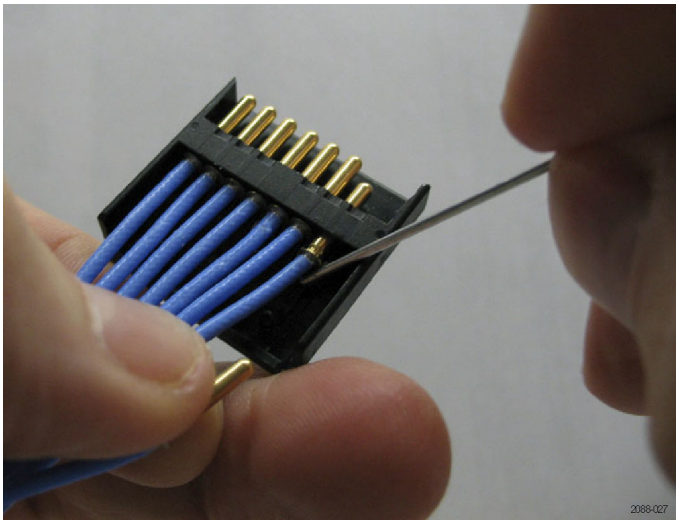


Figure 105: Removing individual wires

5. Repeat step 3 for the wire that you want to put in its place.
6. Insert the replacement wire, making sure the plastic retainer holds it securely. You will feel and hear the connector snap in place.
7. Replace the probe sleeve and the connector cover.

Appendix F: Adding probes to the P67SA01SD probe connector

The P67SA01SD probe ships with two signal wires (one differential pair) in the 8-pin signal connector that connects to the logic protocol analyzer module. The 8-pin connector can accommodate up to three additional probes, for a total of four probes per connector.

To add, remove, or rearrange probes in the connector, refer to the illustrations in the previous section and perform the following procedure. (See page 155, *Rearranging wires in the probe connector*.)

1. Press gently on either side of the connector to snap off the cover.
2. Remove the probe sleeve anchor from the connector, and pull the sleeve away from the connector.
3. Use a bent paper clip (or similar tool) to press downward on the plastic retainer in the connector until the cable slides out. Repeat for the second cable.
4. Insert the wires from the additional probe into the connector, making sure the plastic retainer holds it securely. You will feel and hear the connector snap in place.

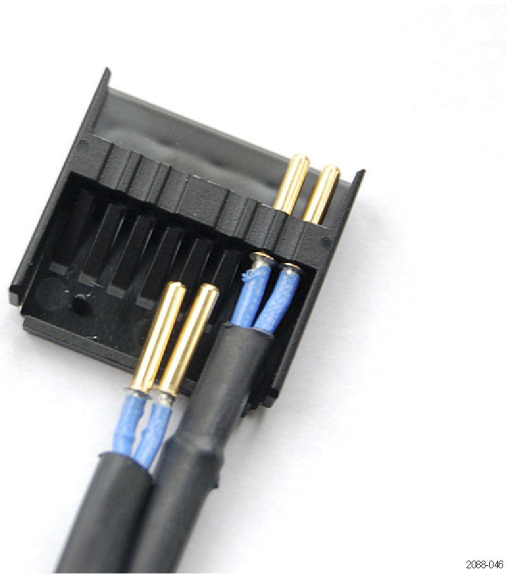


Figure 106: Inserting additional probe wires

5. Repeat step 4 for additional probes as needed.
6. Replace the probe sleeve and the connector cover.

Appendix G: Solder-down probe bullets

The P67SA01SD solder-down probe contains replaceable bullet contacts in the probe head. This appendix describes instructions for replacing the contacts.

The input sockets in the probe body assembly are protected by preinstalled, replaceable bullet contacts. The bullet contacts protect the input sockets by absorbing the wear from repeated connect/disconnect cycles of the accessory tips. The bullet contacts are rated for 100 connect/disconnect cycles. Exceeding this number may degrade the performance of the probe.

An optional bullet tool is used to replace the bullet contacts from the probe body assembly. A kit of four replacement bullets is available as an optional accessory for the probe. See the *P67SA01SD Solder-Down Logic Analyzer Probe Installation Manual* for replacement part numbers.

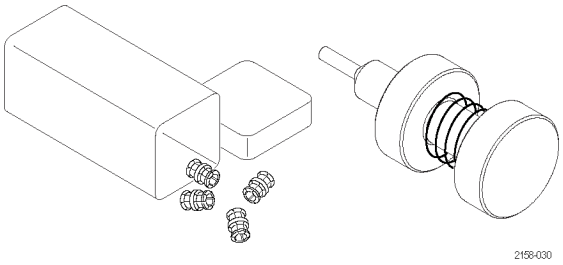


Figure 107: Replaceable bullets and tool

CAUTION. *To prevent wear to the probe housing, use only the bullet tool to remove and install the bullets from the probe body assembly. To prevent damage to the probe, before you connect accessories to the probe body, always check that the contacts are located in the probe body only.*

Removing the bullets

Follow these steps to remove the bullets by using the removal tool:

1. Squeeze the tool plunger to extend the holder tangs.
2. Insert the tool into the probe body so that the holder tangs surround one of the bullets.

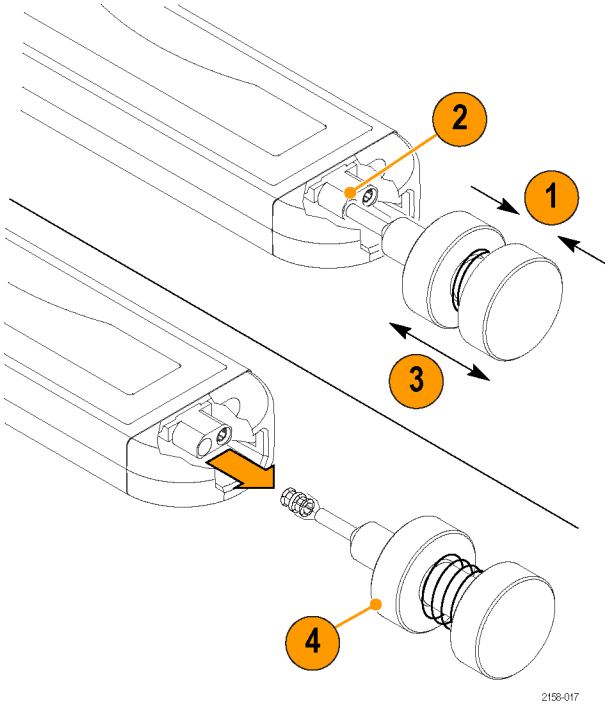


Figure 108: Removing the bullet contacts

3. Release the plunger to secure the holder tangs on the bullet.
4. Gently pull the tool outward to remove the bullet.
5. Repeat for the other bullet.

Inspecting the bullets and connectors

Use a microscope to closely examine the bullets and connectors. Use the illustrations to determine if the contacts appear worn or broken, and always replace them in pairs.

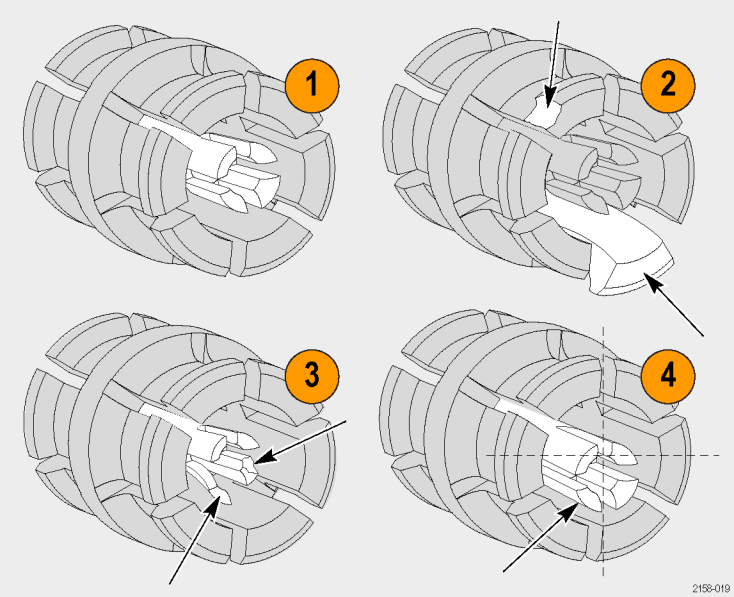


Figure 109: Inspect the bullet contacts

1. Good
2. Chipped or bent ground contacts (outer conductor)
3. Chipped or bent signal contacts (inner conductor)
4. Inner contacts misaligned to outer conductor

Installing the bullets

1. Squeeze the tool plunger to extend the holder tangs.
2. Insert a new bullet into the tool so that the holder tangs surround the bullet.
3. Release the plunger to secure the holder tangs on the bullet.
4. Insert the tool into the probe body and seat the bullet in the recess.

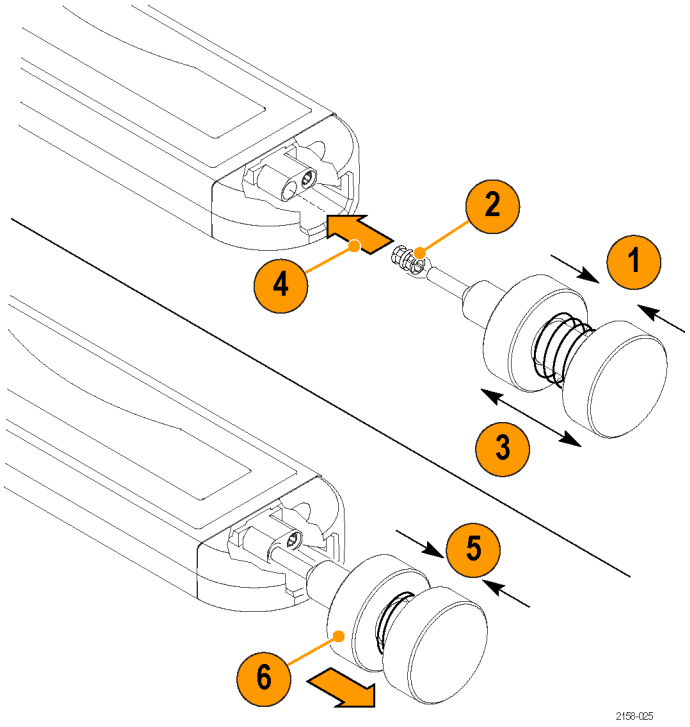


Figure 110: Installing the bullet contacts

5. Squeeze the tool plunger to release the bullet.
6. Gently pull the tool out of the probe body.
7. Repeat for the other bullet.
8. Test that the bullets are installed correctly by connecting and then removing the solder tip to the probe head. Inspect the probe head and verify that the bullets remain seated in the probe head.

Glossary

The following is a list of terms that appear in this manual. You may want to review this list if you are unfamiliar with some of the terms. For a list of PCI Express®-specific terms, refer to the PCI Express Base Specification.

differential pair

A set of two signals, positive and negative, transmitting data from one device to another.

downstream: relative device location

The relative position of a device (or other element) in a system where the device is farther (topologically) from the root complex. Examples: The port on a switch that is farther from the root complex is the downstream port. The upstream component on a link is the component closer to the root complex.

downstream: relative direction of data flow

The direction of data flow where data is flowing away from the root complex.

feynman diagram

A directed graph consisting of packets connected by arrows showing how a transaction evolved.

field

A subunit of a packet defined by the protocol to contain a range of values. Fields can contain data, define the packet itself, and can be reserved, among other possibilities.

footprint

An arrangement of pads built into the board as specified in the PCI Express Base Specification. It is the contact point for the retention mechanism.

lane

A group of two differential pairs (four signals) that transmit data in a PCI Express Link.

link

A connection between two PCI Express devices. A link is described by the number (N) of lanes it contains, as by-N (or xN). For example, a x4 link contains 4 lanes, with each lane having two differential signal pairs, for a total of 16 wires excluding any grounds.

packet

A discrete unit of information used in various serial protocols, often composed of subunits called fields, and constructed from more primitive units called symbols. Packets come in a variety of types and sizes defined by the protocol.

PCB

Printed circuit board

probe head

The end of the probe that connects to the retention mechanism on the circuit board.

retention mechanism

The mechanism that connects the probe head to the circuit board. It fits on the footprint and must be mechanically attached to top and bottom (or front and back) of the circuit board.

root complex

A device (or other element, typically a controller hub) that is located closest to the connection between the I/O system, the CPU and memory.

SUT

System under test. This is the system/circuit board(s) you intend to test with the logic protocol analyzer.

upstream: relative device location

The relative position of a device (or other element) in a system where the device is closer (topologically) to the root complex. Examples: The port on a switch that is closest to the root complex is the upstream port. The port on an endpoint or bridge component is an upstream port. The upstream component on a link is the component closer to the root complex.

upstream: relative direction of data flow

The direction of data flow where data is flowing towards the root complex.

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