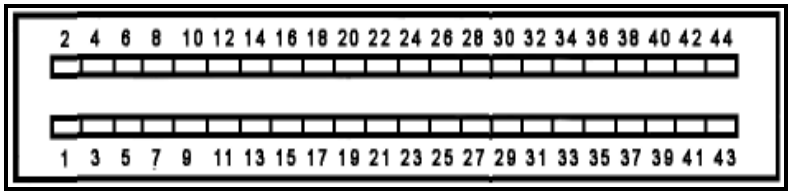
THE MIRAGE EXPANSION PORT

The following describes the lines to be found on the Expansion Port on the rear of the Mirage.
Extreme care must be exercised when connecting anything to these lines. Most of them are static-sensitive. Most of the signal and supply voltage lines aren't buffered or current-limited and can be overloaded - so watch It!

Ensonlq will not perform any warranty repairs on instruments that have had non-approved devices attached to the Expansion Port. Right now. the only approved devices are the Sequencer Expander and the Input Sampling Filter.
Also, note that the pin numbering scheme Is a little different than most edge connectors.



NOTES:

1. **Early Mirages (before Serial Number 11250) used a -12 V supply instead of -8 V.**
2. **The Address Bus and Data Bus are shared by the microprocessor and the Q-Chip resulting in an effective bus speed of 2 MHz. The processor is active when the E clock is high, while the Q-chlp is active when the E clock is low.**
3. **The R/W output is gated with the E clock. A write can occur only when the E clock is high.**
4. **The RES signal is an output. Do not pull this line low.**
5. **When pulled low, the HALT line will tri-state the Address Bus, Data Bus, and R/W line. Pull-up resistors will cause the Address Bus and R/W lines to float to a high state.**
6. **A15 is a special control signal output and is treated differently than the other address lines. A15 reflects the state of Internal bank-switching circuitry and Is not a direct connection to the microprocessor.**
7. **The IRQ input is a common connection for many internal devices that generate interrupts. If an external interrupt is generated, the standard Mirage operating system will ignore it. If an external device holds this line low, the Mlrage will lock up.**
8. **The CART output is gated with the E clock; therefore, a chip select can only occur when the E clock is high.**
9. **TXD and RXD are direct connections to the ACIA and operate at LSTTL levels. The serial data that appears here is the same as on the MIDI port. The baud rate can be set for MIDI rate (31.25 Kbaud) or 4800 baud. When using these pins, the MIDI port should be left unconnected to avoid a conflict.**
10. **If CART Is not used and additional chip selects are decoded off the Address Bus, these chip selects should be gated with the E clock to ensure that they can only be valid during the E clock high time.**
11. **The E clock has a 60% low, 40% high duty cycle.**

Pin#	Name	Description	Pin#	Name	Description
1	GND	System Ground Reference	2	GND	System Ground Reference
3	–8V	Regulated -8 V (100 mA MAX)	4	A0	Address Bus Bit 0 from Microprocessor. (Unbuffered. 3.3k-ohm pull-up, one LSTTL-load MAX.)
5	+12V	Regulated +12 V (100 mA MAX)			
7	R/$\overline{W}$	Read/Write Control line from Microprocessor. (Unbuffered MOS output with 510-ohm pull-up. One LSTTL-load MAX.)	6	A1	Address Bus Bit 1. (See A0.)
			8	A2	Address Bus Bit 2. (See A0.)
			10	A3	Address Bus Bit 3. (See A0.)
9	$\overline{RES}$	Negative-Active Power-on reset. output. (Unbuffered bipolar output One LSTTL-load MAX.)	12	A4	Address Bus Bit 4. (See A0.)
			14	A5	Address Bus Bit 5. (See A0.)
11	NC	No connection.	16	A6	Address Bus Bit 6. (See A0.)
13	NC	No connection.	18	A7	Address Bus Bit 7. (See A0.)
15	NC	No connection.	20	GND	System Ground Reference
17	NC	No connection.	22	A15	Address Bus Bit 15. (See A0.)
19	GND	System Ground Reference	24	A14	Address Bus Bit 14. (See A0.)
21	$\overline{IRQ}$	Negative-Active Interrupt Input to Microprocessor. (Unbuffered MOS Input with 2.4k-ohm pull-up.)	26	A13	Address Bus Bit 13. (See A0.)
			28	A12	Address Bus Bit 12. (See A0.)
23	$\overline{HALT}$	Negative-Active Halt Input to Microprocessor. (Unbuffered MOS input with 2.4k-ohm pull-up.)	30	A11	Address Bus Bit 11. (See A0.)
			32	A10	Address Bus Bit 10. (See A0.)
25	D0	Data Bus Bit 0 from Microprocessor. (Unbuffered, one LSTTL-load MAX.)	34	A9	Address Bus Bit 9. (See A0.)
27	D1	Data Bus Bit 1 from Microprocessor. (Unbuffered, one LSTTL-load MAX.)	36	A8	Address Bus Bit 8. (See A0.)
29	D2	Data Bus Bit 2 from Microprocessor. (Unbuffered, one LSTTL-load MAX.)	38	$\overline{CART}$	Negative-Active Chip-Select for Cartridges. Decode address range $C000 to $DFFF. (Buffered TTL output. One TTL-load MAX.)
31	D3	Data Bus Bit 3 from Microprocessor. (Unbuffered, one LSTTL-load MAX.)	40	E	1.0 MHz Master Bus Clock of Microprocessor. (LSTTL output with 1k- ohm pull-up. One LSTTL-load MAX.)
33	D4	Data Bus Bit 4 from Microprocessor. (Unbuffered, one LSTTL-load MAX.)	42	RXD	Serial Data Input to ACIA. (Unbuffered MOS input with 200-ohm pull-up.)
35	D5	Data Bus Bit 5 from Microprocessor. (Unbuffered, one LSTTL-load MAX.)	44	+5V	Regulated +5 V supply. (Combined output of pins 43 and 44 is 250 mA MAX.)
37	D6	Data Bus Bit 6 from Microprocessor. (Unbuffered, one LSTTL-load MAX.)			
39	D7	Data Bus Bit 7 from Microprocessor. (Unbuffered, one LSTTL-load MAX.)			**Formatted for the Mirage E-Group**
41	TXD	Serial Data Output from ACIA. (Unbuffered. ONE LSTTL-load MAX.)			**by Phoenix Audio - Anaheim**
43	+5V	Regulated + 5 V supply. (See pin 44.)			**Email:** caithleann@gmail dot.com

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