ENSONIQ
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5503 DIGITAL OSCILLATOR CHIP

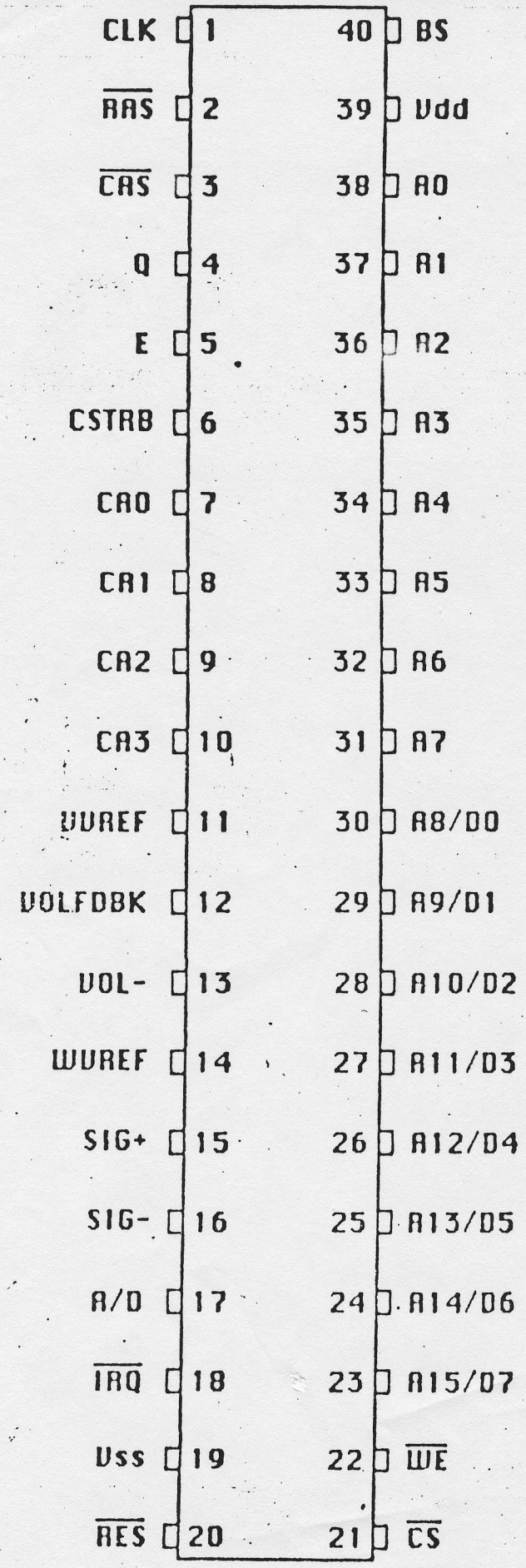
GENERAL DESCRIPTION

The 5503 digital oscillator chip was designed to provide high quality electronic music synthesis capabilities for any music related applications. These applications range from professional music products (synthesizer's etc.) to arcade or home video games. The 5503 chip contains 32 digital oscillators, various control registers and an A/D converter.

FEATURES

- Directly addresses 64k bytes of memory
- Bank select output expands addressing to 128k bytes of memory
- Allows waveform output to be assigned to different channels (voices)
- Generates clock signals compatible with the Motorola 6809e microprocessor (E & Q clock inputs)
- Generates the row and column address strobes used by dynamic memories (RAS & CAS)
- Automatically refreshes 64k x 1 compatible dynamic memories
- On chip 8 bit linear Analog to digital converter
- Compatible with 6800/6500 family microprocessors

5503 PIN DESCRIPTION



5503 PIN DESCRIPTION

PIN NUMBER	SIGNAL NAME	FUNCTION
1	CLK	CLOCK INPUT - Master clock for the 5503 chip. Must be 50% duty cycle. It is internally divided by 8 to get the basic cycle time.
2	$\overline{RAS}$	ROW ADDRESS STROBE OUTPUT - Strobe for accessing dynamic memory.
3	$\overline{CAS}$	COLUMN ADDRESS STROBE OUTPUT - Strobe for accessing dynamic memory.
4	Q	Q CLOCK OUTPUT - Compatible with the M6809E microprocessor Q clock. This clock leads the E clock (pin 5) by 1/4 cycle and has a 50% duty cycle.
5	E	E CLOCK OUTPUT - Compatible with the M6809E microprocessor E clock. This clock also has a 50% duty cycle.
6	$\overline{CSTRB}$	CHANNEL STROBE OUTPUT - Low active signal indicates when the channel assign outputs (CA0 - CA3) are valid.
7 - 10	CA0 - CA3	CHANNEL ASSIGN OUTPUTS - Allows the outputs of the oscillators (SIG+ & SIG-) to be directed to different channels.
11	VVREF	VOLUME VOLTAGE REFERENCE INPUT - Reference voltage for the internal volume D/A converter. Must be -5v + or - 5%.
12	VOLFDBK	VOLUME FEEDBACK INPUT - This signal is the output of the VOL- output after it has been converted to a voltage

5503 PIN DESCRIPTION (CONT.)

PIN NUMBER	SIGNAL NAME	FUNCTION
13	VOL-	VOLUME OUTPUT - This signal is a current output which should be converted to a voltage , the output of which is fed into the WVREF input (pin 14). This voltage will be used as the reference voltage for the internal D/A converter for the SIG+ AND SIG- outputs. It must also be fed back into the volfdbk input (pin 12).
14	WVREF	WAVEFORM VOLTAGE REFERENCE INPUT - This input will provide the reference voltage for the internal D/A converter for the SIG+ AND SIG- outputs (pins 15 & 16).
15 - 16	SIG+ & SIG-	WAVEFORM SIGNAL + AND - OUTPUTS - These two outputs are differential currents representing the final waveform output value (sample).
17	A/D	ANALOG/DIGITAL CONVERTER INPUT - This is the input for the analog to digital converter on the 5503 chip. The conversion time is 30 usec and the input range is 0v to 2.5v. The linearity error is + or - 1/2 LSB.
18	$\overline{IRQ}$	INTERRUPT REQUEST OUTPUT - This low active signal indicates that one or more oscillators have completed their cycle. This output can be disabled through the individual oscillators control registers. It is an open collector output.

5503 PIN DESCRIPTION (CONT.)

PIN NUMBER	SIGNAL NAME	FUNCTION
19	Vss	VOLTAGE INPUT - This is the ground reference for the 5503 chip.
20	RES	RESET INPUT - This pin when low will internally reset the 5503's registers.
21	$\overline{CS}$	CHIP SELECT INPUT - This pin when low will enable the 5503 to communicate with a microprocessor or other controlling device.
22	$\overline{WE}$	WRITE ENABLE INPUT - This pin is the read/write signal for the 5503. A high signal on this pin initiates a read cycle and a low signal on this pin initiates a write cycle.
23 - 30	A15/D7 - A8/D0	ADDRESS/DATA LINES INPUT/OUTPUT - These pins are address lines A8 - A15 and data lines D0 - D7 when the 5503 is accessing waveform data (E clock output is low) and they are data lines D0 - D7 when the 5503 is being accessed by an external controlling device (E clock output is high).
31 - 38	A0 - A7	ADDRESS LINES INPUT/OUTPUT - These pins are address lines A0 - A7 out when the 5503 is accessing waveform data and are address lines A0 - A7 in when the 5503 is being accessed by an external controlling device.
39	Vdd	VOLTAGE INPUT - This is the positive power supply pin - +5v + or - 5%.
40	BS	BANK SELECT OUTPUT - This output pin is essentially address line A16.

5503 ELECTRICAL SPECIFICATION

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	-10 to 80 degrees C
Storage Temperature	-65 to 150 degrees C
Voltage on any Pin	-0.3v to +7 v

D.C. CHARACTERISTICS

Ta = 0 to 50 degrees C, Vdd = 5v +/- 5%

CHARACTERISTIC	MIN.	MAX.	TYP.	UNITS
R/W, CS, A0 - A7,				
A8/ D0 - A15/D7, RES				
Vil	0.0	0.4	-	Volts
Vih	2.4	5.0	-	Volts
CSTRB, CA0 - CA3,				
VSTRB, WSTRB, BS				
A0 - A7, A8/D0 - A15/D7.				
Vol	-	0.8	-	Volts
Voh	2.4	-	-	Volts
Iol - Sink Current, Vol = 0.4	-	2.0	-	mA
Ioh - Source Current, Voh = 2.4	-	1100	-	uA
CLOCK INPUT (CLK)				
Frequency	-	16	8	Mhz
Vil	0.0	0.4	-	Volts
Vih	4.5	-	-	Volts
CLOCK OUTPUTS (RAS, CAS, E Q)				
Frequency (RAS, CAS)	-	-	2	Mhz
Frequency (E, Q)	-	-	1	Mhz
Vol	-	0.8	-	Volts
Voh	2.4	-	-	Volts
Iol - Sink Current, Vol = 0.4	-	2.0	-	mA
Ioh - Source Current, Voh = 2.4	-	100	-	uA

DIGITAL OSCILLATOR CHIP SPECIFICATION

There are 32 oscillators in the chip. Each oscillator is controlled by a set of seven registers:

1. Frequency Low
2. Frequency High
3. Volume
4. Data Sample
5. Address Pointer
6. Control Register
7. Resolution/Table Size Registers

In addition to these 224 oscillator control registers, there are three other registers:

1. Oscillator IRQ
2. Oscillator Enable
3. Analog to Digital Converter

The seven oscillator control registers are grouped as a set of 32 registers. In other words, all 32 frequency low control registers are grouped together and addresses consecutively, e.g., frequency low for oscillator 0 is address at location $00, OSC 1 frequency low is at $01. Frequency High Control for OSC is at $20, which is 32 locations above frequency low control. The register map for each of the seven oscillator control groups is as follows:

Address	Register Function Description
00-1F	Frequency low for OSC0 thru OSC31
20-3F	Frequency high for OSC0 thru OSC31
40-5F	Volume
60-7F	Waveform Data Sample
80-9F	Address Pointer
A0-BF	Control Register
C0-DF	Resolution/Table Size
E0	Oscillator Interrupt Register
E1	Oscillator Enable Register
E2	Analog to Digital COnverter

Note that the oscillators are also grouped into 8 "voices". Each voice consists of four oscillators, e.g., OSC0, OSC1, OSC2 and OSC3 are referred to as Voice 0; OSC4, OSC5, OSC6, and Osc7 are Voice 1.

CONTROL REGISTER (A0-BF)

The following chart indicates the decomposition of the control register into its bit definitions:

D7	D6	D5	D4	D3	D2	D1	D0
CA3	CA2	CA1	CA0	IE	M2	M1	H

For each OSC the control register is used to control three functions.

1. Channel Assignment (CA3-CA0)
   Bits 7 thru 4 of the control register are defined as CA3 thru CA0. These four bits are used to control the final voice multiplexor. Sixteen different channel assignments are possible; only eight are normally used. Channel assignment is usually synonomous with voice assignment.

2. Interrupt Assignment (IE)
   Bit 3 of the control register is used to stop an interrupt from being passed to the Oscillaor Interrupr Register (OIR). If IE is set, then the oscillator will cause an interrupt to be passed to the OIR when it completes a cycle, which n turn will interrupt the processor. If IE is clear, then the interrupt will be put into the oscillator interrupt table, but not passed to the OIR. When more than one oscillator interrupt occurs, the interrupt stack will retain the status and pass interrupts to the OIR as they are serviced by the processor. If the interrupt has been stored into the interrupt table while IE = 0 , when IE is changed to a 1 the IRQ will be passed to the OIR.

Oscillator Mode (M2, M1, H)

Bits 2,1, 0 control the functional mode of each oscillator.

The following chart describes these modes:

M2	M1	Oscillator Mode
0	0	Free run
0	1	Address one cycle, reset OSC accumulator to zero, and set halt bit.
1	0	Sync OSC2 to OSC1 or amplitude modulate OSC1 by OSC0. If set for an Even voice then the Odd voice will sync to the Even voice. It will reset the accumulators for both the Even and Odd voices to zero and the cycle will start again. If set for an Odd voice then the Odd voice envelopes the next Even voice. Note: voice 0 has no modulation source.
1	1	Address one cycle, reset OSC accumulator to zero, and set halt bit then reset halt bit of associated oscillator (togle mode)

Whenever the halt bit is set by DOC or the processor and M1 is set, the OSC will be reset to zero.

M1 * H = 1 causes oscillator to be reset

Sync will cause OSC2 to sync to OSC1 in each voice group. (OSC6 syncs to OSC5 for voice 1 etc.)

Amplitude mosulation will cause OSC0 to be used as an envelope for OSC1 in each voice group. (OSC4 modulates OSC5 in voice 3 etc.) Volume for OSC0 and OSC1 is ignored.

DATA SAMPLE (60-7F)

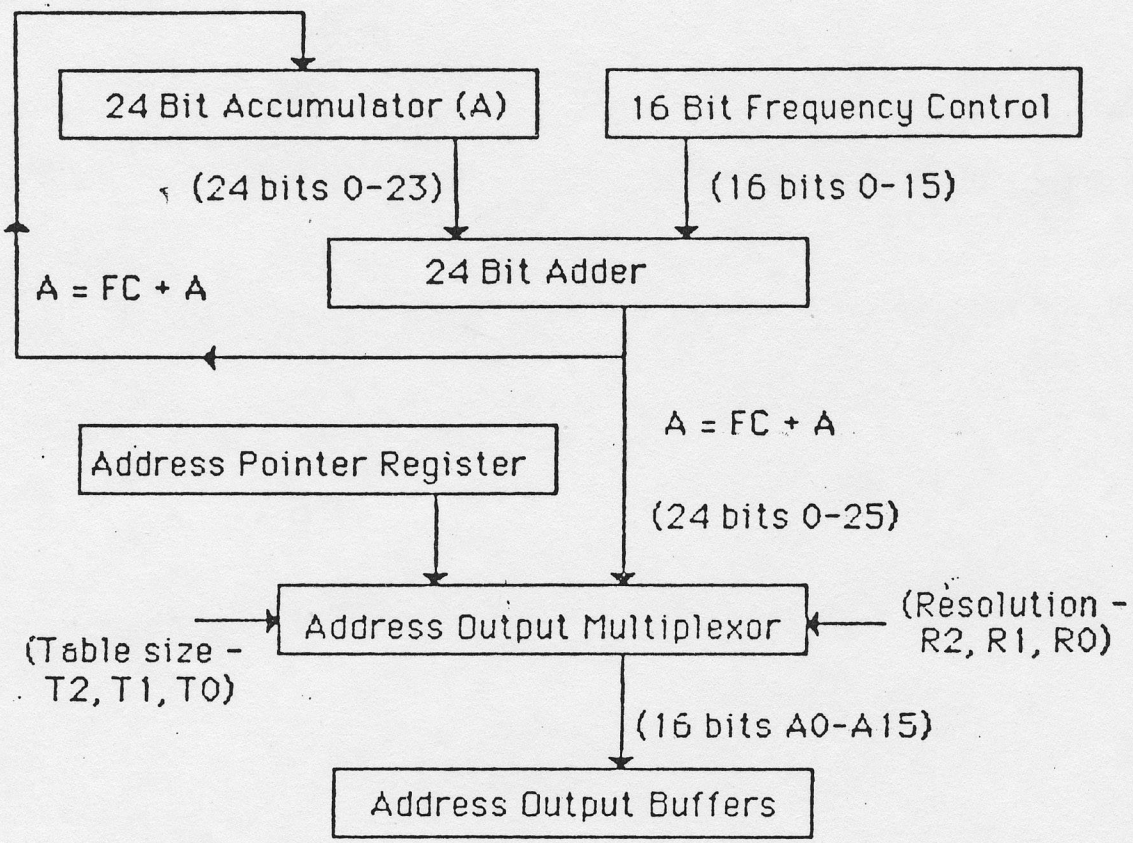
This set of registers is used to indicate the current 8-bit value of the waveform sample. This value will be fed to the DOC for that particularoscillator. This function is useful for LFO or modulation applications where the DOC oscillators are used to fetch sine wave samples that can be read by the processor for additional processing. These registers are read only.

VOLUME (40-5F)

This set of registers is used to control the volume level of the waveform data. The 9-bit volume level is multiplied by the 8-bit waveform value to form the final analog output for each oscillator.

FREQUENCY CONTROL HIGH AND LOW (00-3F)

This group of registers is the 16-bit value which defines in part the actual frequency of the oscillator. These tworegisters are concatonated and become the incremental value for the linear accumulating oscillators. THe oscillator block diagram is indicated below:


24 Bit Accumulator (A)
16 Bit Frequency Control
(24 bits 0-23)
(16 bits 0-15)
24 Bit Adder
A = FC + A
A = FC + A
Address Pointer Register
(24 bits 0-25)
Address Output Multiplexor
(Resolution - R2, R1, R0)
(Table size - T2, T1, T0)
(16 bits A0-A15)
Address Output Buffers

ADDRESS POINTER (80-9F)

This is an 8-bit register which defines the strarting base address of the waveform table. The number of address pointer bits actually used in the final address depends on the size of the waveform table specified. The following chart indicates the use of the pointer bits:

WAVEFORM TABLE SIZE	A15	A14	A13	A12	A11	A10	A9	A8
256	P7	P6	P5	P4	P3	P2	P1	P0
512	P7	P6	P5	P4	P3	P2	P1	-
1024	P7	P6	P5	P4	P3	P2	-	
2048	P7	P6	P5	P4	P3	-		
4096	P7	P6	P5	P4	-			
8192	P7	P6	P5	-				
16384	P7	P6	-					
32768	P7							

WAVEFORM TABLE SIZE/RESOLUTION/BANK SELECT (C0-DF)

This rgister controls three oscillator functions. The following chart indicates the bit positions within the register to control the three functions.

D7	D6	D5	D4	D3	D2	D1	D0
N.U.	B.S.	T2	T1	T0	R2	R1	R0

1. Bank Select Bit (B.S. = bit 6)
   This bit is used to extend the addressing range of the DOC from 64K to 128K.

2. Table Size (T = b5, b4, b3)
   These 3-bits are used to specify the size of the waveform table addressed by the oscillator.

T2	T1	T0	Table Size
0	0	0	256
0	0	1	512
0	1	0	1024
0	1	1	2048
1	0	0	4096
1	0	1	8192
1	1	0	16384
1	1	1	32768

3. Resolution

These three bits determine which set of 16 bits, of the 24 in the oscillator accumulator, are used to address the waveform table. The purpose of this accumulator bit selection is to allow the frequency resolution to be adjusted to the waveform table size. For example, when using a 32K waveform table, accumulator bits 8 thru 23would normally be used, but in a 256 byte table a lower resolution setting would be used to step through the table faster.

There are eight accumulator address bit selections available.

R2	R1	R0	Accumulator Bits Used as Addresses
0	0	0	1 through 16
0	0	1	2 through 17
0	1	0	3 through 18
0	1	1	4 through 19
1	0	0	5 through 20
1	0	1	6 through 21
1	1	0	7 through 22
1	1	1	8 through 23

ADDRESS CALCULATION

The final address that is used to access a waveform table is a function of the address pointervalue, the table size, and the resolution. The following table indicates the various address possibilities for the DOC.

Table Size	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	R2	R1	R0
									A23	A	A	A	A	A	A	A16	1	1	1
256	P7	P6	P5	P4	P3	P2	P1	P0	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕
									A16	A	A	A	A	A	A	A9	0	0	0
								A23	A	A	A	A	A	A	A	A15			
512	P7						P1	↕	↕	↕	↕	↕	↕	↕	↕	↕			
								A16	A	A	A	A	A	A	A	A8			
							A23	A	A	A	A	A	A	A	A	A14			
1024	P7					P2	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕			
							A16	A	A	A	A	A	A	A	A	A7			
						A23	A	A	A	A	A	A	A	A	A	A13			
2048	P7				P3	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕			
						A16	A	A	A	A	A	A	A	A	A	A6			
					A23	A	A	A	A	A	A	A	A	A	A	A12			
4096	P7			P4	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕			
					A16	A	A	A	A	A	A	A	A	A	A	A5			
				A23	A	A	A	A	A	A	A	A	A	A	A	A11			
8192	P7		P5	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕			
				A16	A	A	A	A	A	A	A	A	A	A	A	A4			
			A23	A	A	A	A	A	A	A	A	A	A	A	A	A10			
16384	P7	P6	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕			
			A16	A	A	A	A	A	A	A	A	A	A	A	A	A3			
		A23	A	A	A	A	A	A	A	A	A	A	A	A	A	A9			
32768	P7	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕	↕			
		A16	A	A	A	A	A	A	A	A	A	A	A	A	A	A2			

OSCILLATOR INTERRUPT REGISTER

The OIR is used to inform the processor which oscillator has caused an interrupt request to occur. When an oscillator completes a waveorm table an interrupt is generated. THis interrupt will be passed to the OIR if IE = 1. The OIR will thenissue an IRQ to the processor. Upon recognizing th IRQ, the processor reads the oIR to determine which oscillator issued the IRQ. The OIR is an 8-bit register where Bit 7 indicates the state of the IRQ line. (bit 7 = 0 for valid IRQ). Bits 5 through1 contain the oscillator number 0through 31. Bits 6 and 0 are always 1.

D7	D6	D5	D4	D3	D2	D1	D0
IR	1	04	03	02	01	00	1

After the processor reads the OIR, the DOC will clear the appropriate oscillator interrupr request, e.g., if oscillator 4 causes an IRQ, then the processor will read: OIR = 65 + 4.

OSCILLATOR ENABLE REGISTER (E1)

This register determines the number of active oscillators on the DOC. Load the register with the number of oscillators to be enabled, multiplied by 2, e.g., to enable all oscillators, load register with a 62.

Note: There are 32 oscillators on DOC plus 2 additional time slots for RAM refresh. Therefore, 34 actual oscillator time slots are used. If the number of oscillators is halved to 16 the frequency is not doubled since the two refresh time slots still exist. To halve the frequency, the number of enabled oscillators should be 15. Oscillators which are disabled will not hold their associated register data since they are not refreshed.

5503 REGISTER MAP SUMMARY

ADDRESS (HEX)	FUNCTION	D7	D6	D5	D4	D3	D2	D1	D0
00 - 1F	FREQUENCY LOW	FL7	FL6	FL5	FL4	FL3	FL2	FL1	FL0
20 - 3F	FREQUENCY HIGH	FH7	FH6	FH5	FH4	FH3	FH2	FH1	FH0
40 - 5F	VOLUME	V7	V6	V5	V4	V3	V2	V1	V0
60 - 7F	WAVEFORM DATA SAMPLE	W7	W6	W5	W4	W3	W2	W1	W0
80 - 9F	WAVEFORM TABLE POINTER	P7	P6	P5	P4	P3	P2	P1	P0
A0 - BF	CONTROL	CA3	CA2	CA1	CA0	IE	M2	M1	H
C0 - DF	BANK SELECT/ TABLE SIZE/ RESOLUTION	H	BS	T2	T1	T0	R2	R1	R0
E0	OSCILLATOR INTERRUPT	IRQ	1	04	03	02	01	00	1
E1	OSCILLATOR ENABLE	H	H	E4	E3	E2	E1	E0	H
E2	A/D CONVERTER	S7	S6	S5	S4	S3	S2	S1	S0

NOTES: 1) BITS LABELED 1 ARE NOT USED AND ALWAYS READ BACK AS A 1.

2) BITS LABELED H ARE NOT USED AND ALWAYS READ BACK AS A 1.

5503 SYSTEM TIMING

INPUT CLOCK TIMING

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS
Input Clock Cycle Time	Tcyc1	100	-	125	ns
Clock High	Tpwh	50	-	-	ns
Clock Low	Tpwl	50	-	-	ns
Rise and Fall Times	Tr, Tf	-	-	10	ns

OUTPUT CLOCK TIMING

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS
Two MHz Clock Cycle Time	Tcyc2	480	-	500	ns
RAS/CAS Clock Output High	Toh1	270	-	290	ns
RAS/CAS Clock Output Low	Tol1	190	-	210	ns
RAS High after E Low	Trd	-	-	40	ns
CAS High after RAS High	Tcd	40	-	70	ns
1MHz uProcessor Clocks Cycle Times	Tcyc3	980		1000	ns
E/Q Clock Output High	Toh2	480	-	500	ns
E/Q Clock Output Low	Tol2	480	-	500	ns
E High from Q High (Q leads E)	Tqd	240	-	250	ns
Rise and Fall Times (E, Q, RAS, CAS)	Tr, Tf	-	-	10	ns

MICROPROCESSOR READ/WRITE TIMING TO 5503

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS
Address Setup Time	Tas	350	-	-	ns
Address Hold Time	Tah	0	-	100	ns
R/W Signal Delay From E Low	Trs	-	-	-	ns
R/W Signal Valid for Read	Trw	350	-	-	ns
Chip Select Hold From E Low	Th	0	-	-	ns
Data In Setup Time	Tds	150	-	-	ns
Data In Hold Time	Tdh	30	-	-	ns
R/W Signal Valid for Write	Tww	350	-	-	ns
Data Out Hold Time	Tdh	30	-	-	ns

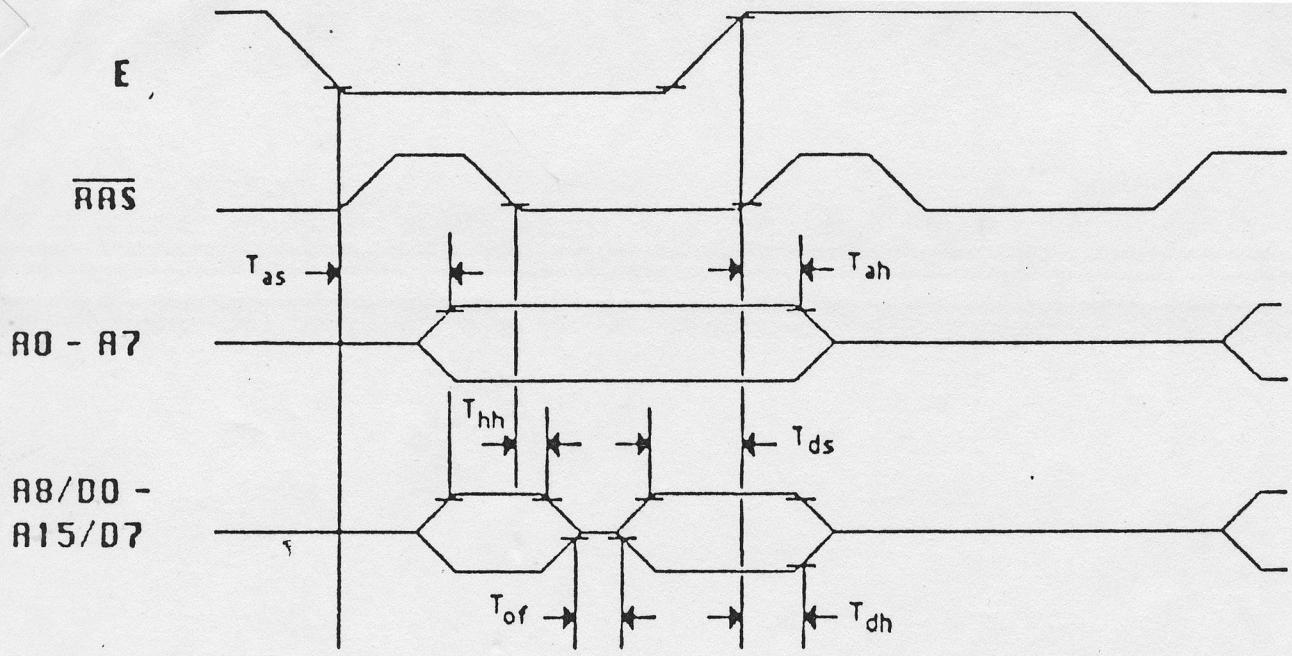
5503 READ FROM MEMORY

CHARACTERISTIC	SYMBOL	MIN.	TYP.	MAX.	UNITS
Time to Valid Address From E	Tas	-	-	50	ns
Address Hold Time (A0 - A7)	Tah	0	-	10	ns
A8 - A15 Hold Time From RAS Fall	Thh	-	-	30	ns
A8/D0 - A15/D7 Lines Switching Time	Tof	30	-	-	ns
Data In Setup Time	Tds	100	-	-	ns
Data In Hold Time	Tdh	20	-	-	ns

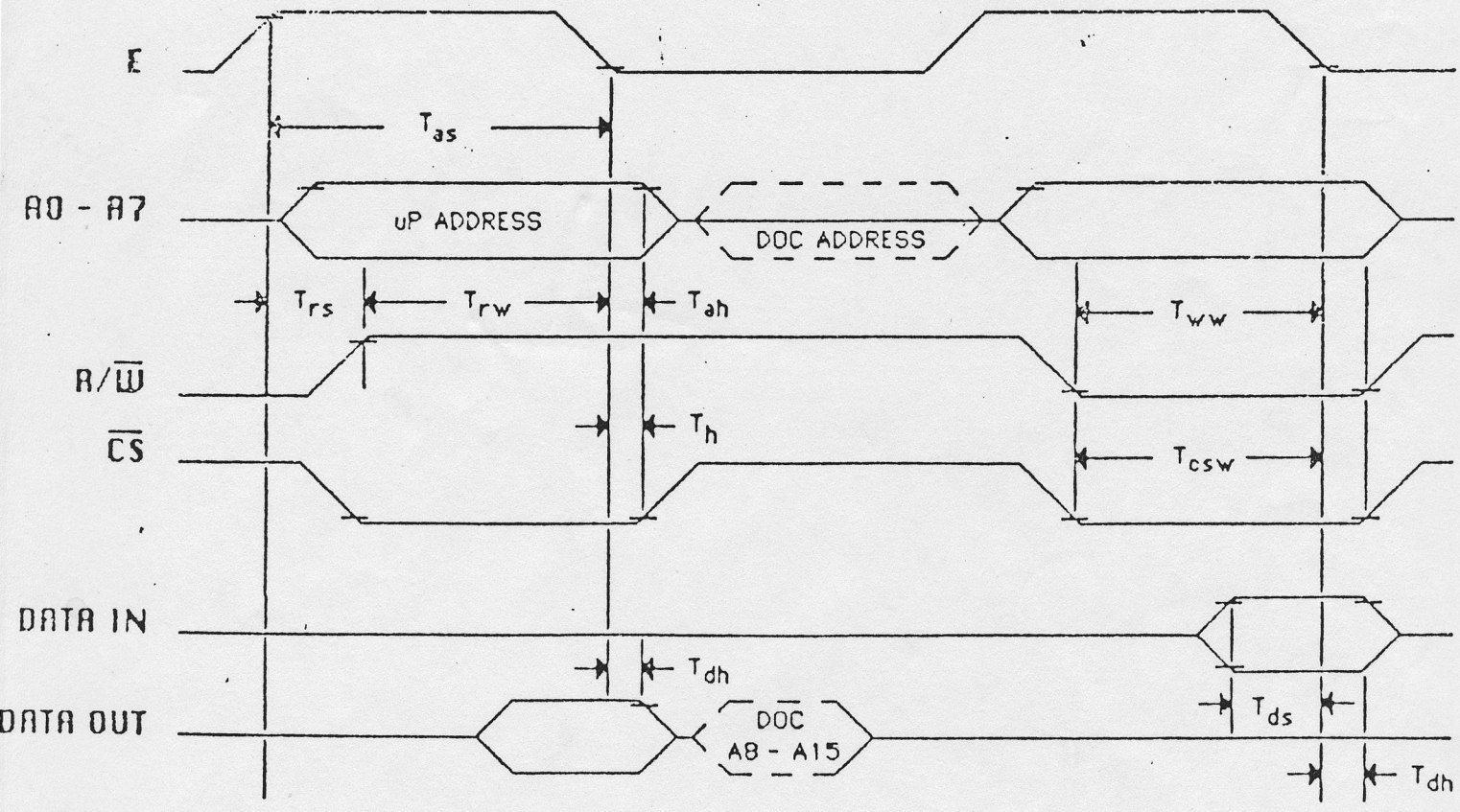
250 - TCAC

150 TDS

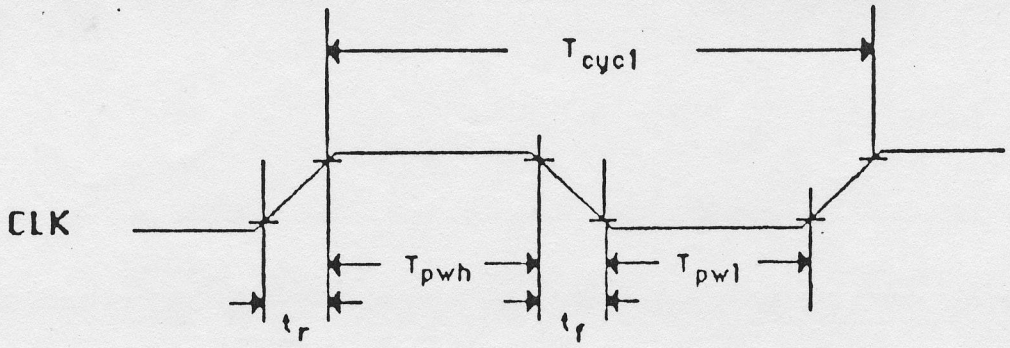
100 ?



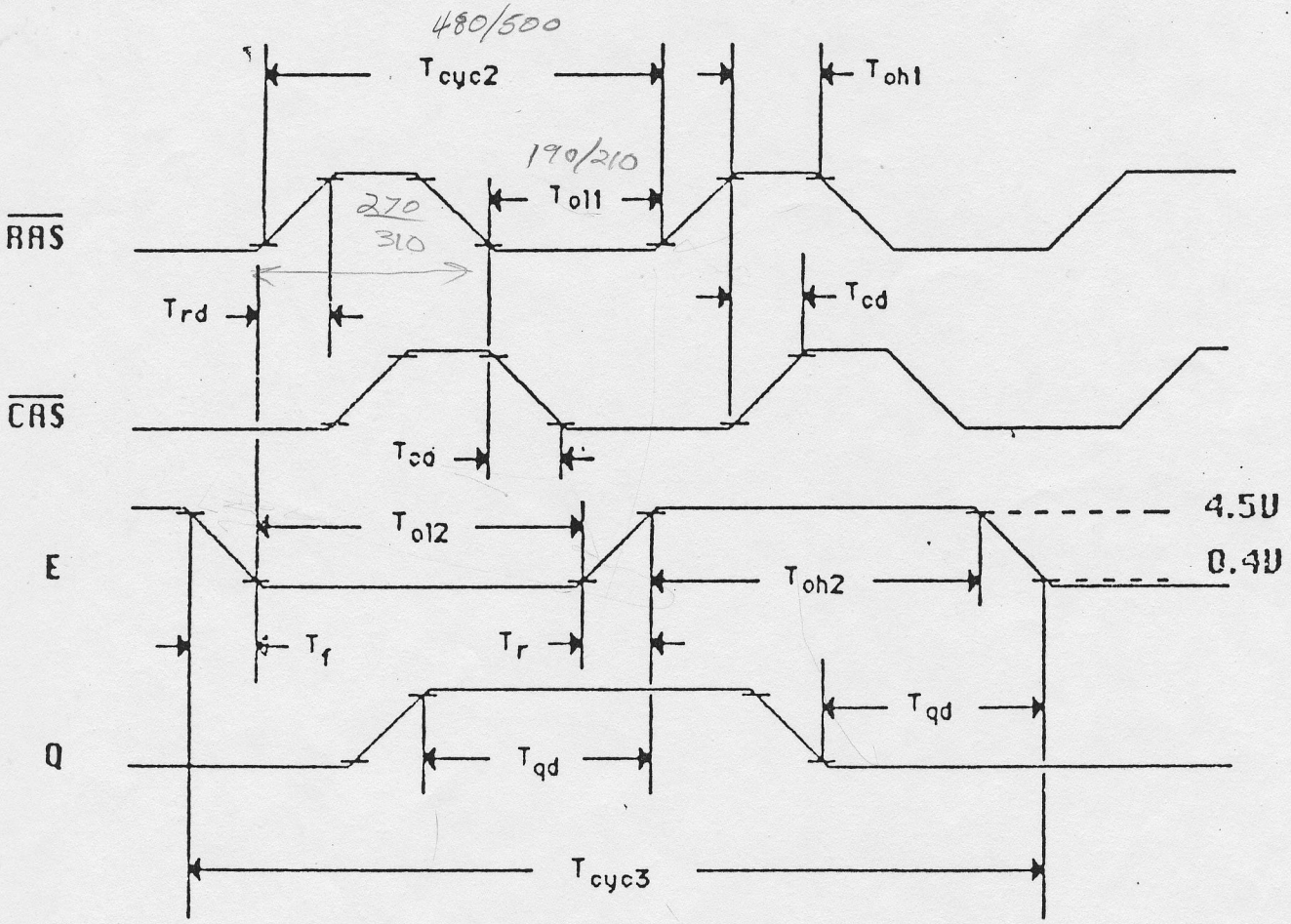
5503 READ FROM MEMORY



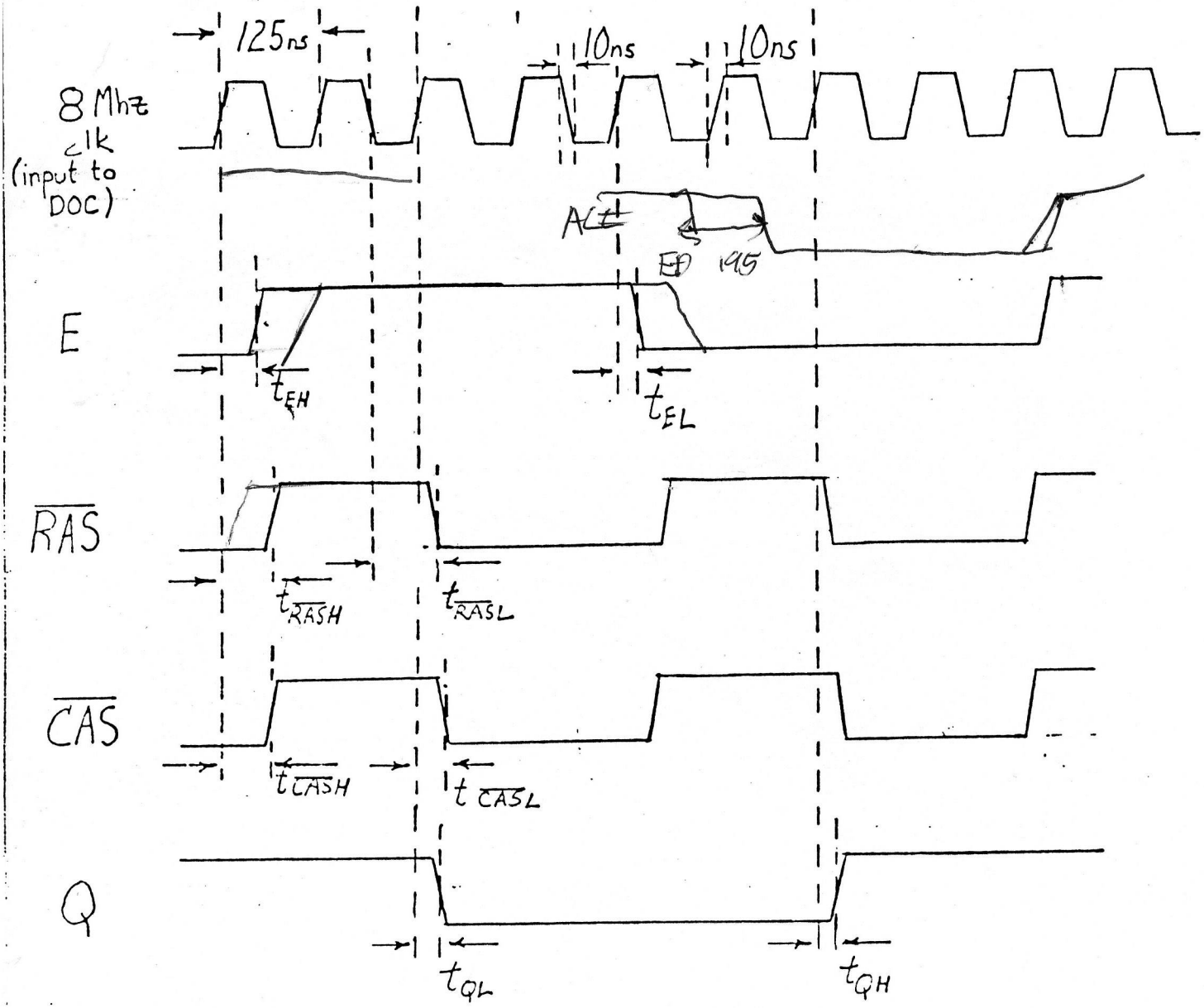
MICROPROCESSOR READ/WRITE TIMING TO 5503



INPUT CLOCK



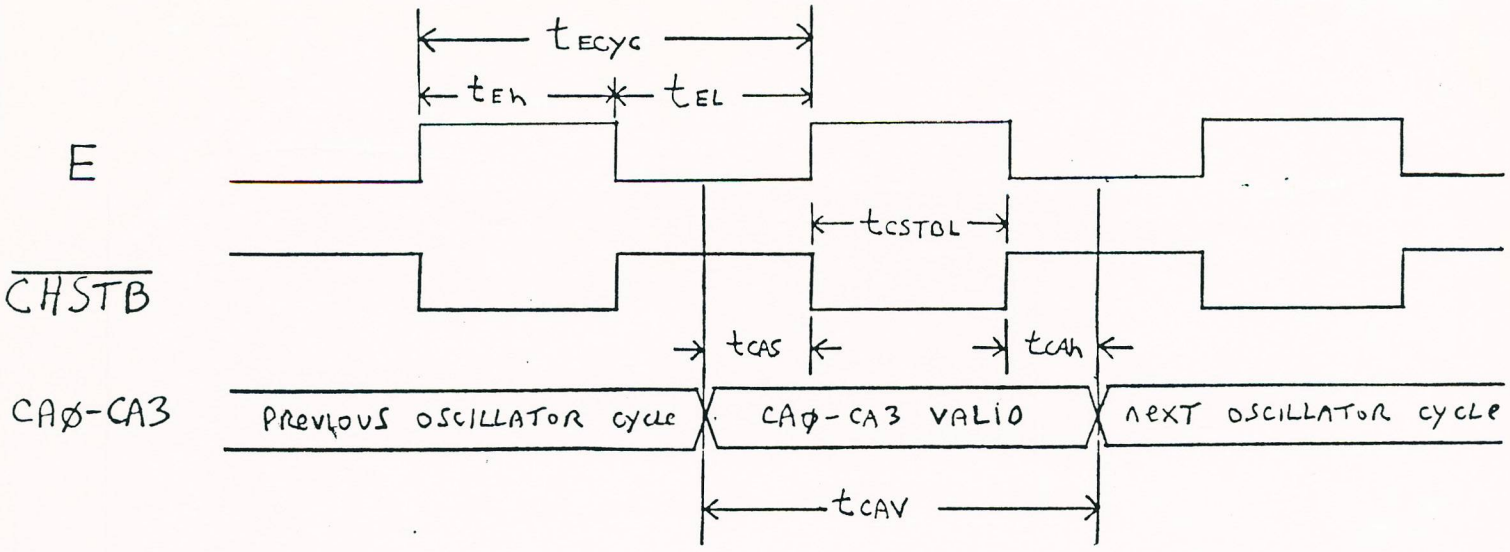
OUTPUT CLOCKS



Symbol	Parameter	MIN	TYP	MAX
t_{EH}	time to E high ①	40	50	60 ns
t_{EL}	time to E Low	50	63	80 ns
$t_{\overline{RASH}}$	time to $\overline{RAS}$ high	50	60	80 ns
$t_{\overline{RASL}}$	time to $\overline{RAS}$ Low	60	82	97 ns
$t_{\overline{CASH}}$	time to $\overline{CAS}$ high	60	65	80 ns
$t_{\overline{CASL}}$	time to $\overline{CAS}$ Low	50	60	70 ns
t_{QL}	time to Q low	50	55	70 ns
t_{QH}	time to Q high	50	60	70 ns

① Referenced to the rising edge of the indicated cycle of the 8 Mhz input clock

DOC CHIP CHANNEL STROBE AND CAØ-CA3 TIMING



SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
tECYC	E CLOCK CYCLE TIME		1000		NS
tEH	E CLOCK HIGH TIME		500		NS
tEL	E CLOCK LOW TIME		500		NS
tCSTBL	CHANNEL STROBE LOW TIME		500		NS
tCAV	CAØ-CA3 VALID TIME		1000		NS
tCAS	CAØ-CA3 SETUP TIME TO CHANNEL STROBE LOW		250		NS
tCAH	CAØ-CA3 HOLD TIME FROM CHANNEL STROBE HIGH		250		NS

NOTES 1) ALL TIMMING IS BASED ON 8MHZ CLOCK INPUT

2) CHANNEL STROBE AND CAØ-CA3 ARE ALWAYS HIGH DURING THE TWO REFRESH CYCLES

CLK -1 Q-4

NUMBERS ARE AS MEASURED