FIELD MANUAL FOR 68302 SUPPORT

NNC302

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***** DRAFT *****

Contents

This manual contains the following sections:

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Product description

The 68302 microprocessor support product disassembles data from systems that are based on the Motorola 68302 and 68LC302 processors. The 68302 support runs on a TLA logic analyzer equipped with one 68-channel Jupiter Data Acquisition Module.

The NNC 302 software is loaded to an acquisition module as application software. The acquisition module's setup menu is then used to set up trigger specifications and acquire 68302 or the 68LC302 (depending which option is selected in the AMS) bus cycles using general purpose Jupiter probes. The acquired bus cycles are then disassembled and displayed in the TLA 700 Listing Disassembly display.

The support provides the highest level of disassembly support, including mnemonic and operand decoding, branch detection, and flushing.

The NNC 302 disassembler requires Custom clocking to function properly. Other clocking selections (Internal & External) may cause improper disassembly.

The 68302 product decodes and displays bus cycle types including

- (RESET) -- system reset
- (READ) -- data read
- (WRITE) -- data write
- (HALT/RETRY) – Halt cycle or Retry cycle
- (ALTERNATE MASTER) – Alternate Bus Master cycles. When a processor other than the processor connected to the Logic Analyzer owns the Bus.
- (UNKNOWN) -- The combination of control bits is unexpected and/or unrecognized.

Can find more details in the Control Symbol Table detailed in this manual.

The application decodes all 68302 instructions, marks invalid bytes on the data bus, and decodes and labels all exception vector reads.

The external address has 20 lines for 68LC302 and 24 lines for 68302. However, the address group in the disassembly listing display will be displayed to represent the maximum address space of 24-bits for both the processors.

The address display for 68LC302 uses the Chip selects to calculate the 24-bit address. Note 68LC302 has only 20 Address lines.

Product Limitations

Processor 68LC302 does not have any indications to differentiate fetch and read cycle types. 68302 does have indication for fetch but this support does not use it. Therefore the support uses a Fetch/Read Algorithm to determine if a certain read cycle sequence is a fetch cycle type or read cycle type.

Details of the algorithm: In 16-bit mode there should be three read cycle type sequences with addresses of N, N+2 and N+4, to determine that sequence with address N is a fetch cycle. Similarly in 8-bit mode there should be six read cycle type sequences with addresses N, N+1, N+2, N+3, N+4 and N+5 to determine that sequence with address N is a fetch cycle. Besides this control flow instructions are also analyzed to anticipate the target address. Some instructions like MOVEM alter the search length for the fetch/read algorithm. There is one exception to the above mentioned details. To determine the first fetch sequence, after an RTE instruction has been disassembled, the algorithm looks for one more (in 16-bit, and two more in 8-bit) read sequence(s) than otherwise. Once a fetch has been identified, the algorithm reverts to the original method.

The limitation is that if the read sequences do not match the above requirement the FETCH cycles will be decoded as READ cycles. This could also result in incorrect disassembly during backtracking when there are **many consecutive** MOVEM <ea>, <list> type instructions. These type of instructions could initiate upto 32 consecutive READ cycles in 16-bit mode and upto 64 consecutive READ cycles in 8-bit mode, depending on the Register list mentioned in the instruction. In such circumstances if in the Listing window we move up by doing “Page Up”, there could be incorrect disassembly display. The user could use Marking feature or see the disassembly of the required sequence by starting from the beginning of the Reference Memory and do “Page Down” to the required sequence.

Channel Assignments Tables

Channel assignments shown in Table 3-1 through Table 3-6 use the following conventions:

- All signals are required for disassembly unless indicated otherwise
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB)
- A tilde (~) following a signal name indicates an active low signal

The NNC 302 will support the Address, Data, and Control channel groups, in addition to other channel groups. In the following tables, channel is the TLA 700 "section: channel" number, and signal name is the 68302/68LC302 signal name. Channel groups will be displayed on the screen in the order shown below.

Group Name	Display Radix
Address	HEX
Data	HEX
Mnemonic	-NONE- <-- Disassembly text generated by PDL
Control	SYM
ChipSelect	OFF
Intr	OFF
Misc	OFF
Timestamp	

Channel Groups Needed for Disassembly

The channel groups listed in this part of the section are needed by the disassembler software. So these channel groups must not be deleted, renamed, or rearranged if you want to disassemble the data samples.

If any of the channel groups Address, Data, or Control was changed, you will have to reload the support.

Table 3-1 shows the probe section and channel assignments for the Address group, and the microprocessor signal to which each channel connects. Refer to How data is acquired in this section for information on sample points. The default display radix for the Address group is HEX

Table 3-1 Address Group Channel Assignments

Acquisition Module		68302 device	68LC302 device
Bit No.	Section:Channel	Signal Name	Signal Name
23	A2:7	A23	GND *

22	A2:6	A22	GND *
21	A2:5	A21	GND *
20	A2:4	A20	GND *
19	A2:3	A19	A19
18	A2:2	A18	A18
17	A2:1	A17	A17
16	A2:0	A16	A16
15	A1:7	A15	A15
14	A1:6	A14	A14
13	A1:5	A13	A13
12	A1:4	A12	A12
11	A1:3	A11	A11
10	A1:2	A10	A10
9	A1:1	A9	A9
8	A1:0	A8	A8
7	A0:7	A7	A7
6	A0:6	A6	A6
5	A0:5	A5	A5
4	A0:4	A4	A4
3	A0:3	A3	A3
2	A0:2	A2	A2
1	A0:1	A1	A1
0	A0:0	UDS~/A0	WEH~/UDS~/A0

Note: Channel A2: 7- 4 indicated by * should be connect to Ground for 68LC302 Device.

Table 3-2 shows the probe section and channel assignments for the Data group, and the microprocessor signal to which each channel connects. The default display radix is HEX.

Table 3-2 Data Group Channel Assignments

Acquisition Module		68302 device	68LC302 device
Bit No.	**Section:Channel**	**Signal Name**	**Signal Name**
15	D1:7	D15	D15
14	D1:6	D14	D14
13	D1:5	D13	D13
12	D1:4	D12	D12
11	D1:3	D11	D11
10	D1:2	D10	D10
9	D1:1	D9	D9
8	D1:0	D8	D8
7	D0:7	D7	D7

6	D0:6	D6	D6
5	D0:5	D5	D5
4	D0:4	D4	D4
3	D0:3	D3	D3
2	D0:2	D2	D2
1	D0:1	D1	D1
0	D0:0	D0	D0

Table 3-3 shows the probe section and channel assignments for the Control group, and the microprocessor signal to which each channel connects. By default this channel group is displayed symbolically. The Symbol file is 68302_Ctrl.ast.

Table 3-3 Control Group Channel Assignments

Acquisition Module		68302 device	68LC302 device
Bit No.	**Section:Channel**	**Signal Name**	**Signal Name**
8	C2:3	RESET~	RESET~
7	C2:5	HALT~	HALT~
6	C2:2	DISCPU	DISCPU
5	C2:0	BGACK~	IPL1~/BGACK~
4	C2:1	AS~	AS~
3	CLK:1	UDS~/A0	WEH~/UDS~/AO
2	CLK:2	LDS~/DS~	WEL~/LDS~/DS~
1	CLK:3	R/W~	OE~/R/W~

Table 3-4 shows the probe section and channel assignments for the ChipSelect group and the microprocessor signal to which each channel connects. The default display radix is OFF.

Table 3-4 ChipSelect Group Channel Assignments

Acquisition Module		68302 device	68LC302 device
Bit No.	**Section:Channel**	**Signal Name**	**Signal Name**
3	C3:3	CS3~	CS3~
2	C3:2	CS2~	CS2~
1	C3:1	CS1~	CS1~
0	C3:0	CS0~/IOUT2~	CS0~/IOUT2~

Table 3-5 shows the probe section and channel assignments for the Interrupt group and the microprocessor signal to which each channel connects. The default display radix is OFF.

Table 3-5 Interrupt Group Channel Assignments

Acquisition Module		68302 device	68LC302 device
Bit No.	**Section:Channel**	**Signal Name**	**Signal Name**
7	C2:7	IPL2~/IRQ7~	IPL2~/BG~
6	C2:0	NC	IPL1~/BGACK~
5	C3:5	IPL1~/IRQ6~	NC
4	C2:6	IPL0~/IRQ1~	IPL0~/BR~
3	A3:3	PB11	PB11
2	A3:2	PB10	PB10
1	A3:1	PB9	PB9
0	A3:0	PB8	PB8

Channel Groups not Needed for Disassembly

The channel groups listed in this part of the section are extra channel groups not needed by the disassembler software. So these channel groups can be deleted, renamed, or rearranged as it is up to your needs.

Table 3-6 shows the probe section and channel assignments for the Misc group and the microprocessor signal to which each channel connects. The default display radix is OFF.

Table 3-6 Misc Group Channel Assignments

Acquisition Module		68302 device	68LC302 device
Bit No.	**Section:Channel**	**Signal Name**	**Signal Name**
3	C2:4	BUSW	BUSW
2	C3:4	DTACK~	DTACK~
1	C3:7	BR~	NC
0	C3:6	BG~	NC

Control Symbol Table

SYMBOL	BINARY PATTERN	DEFINITION
	+--------------	RESET~
	| +------------	HALT~
	| |+-----------	DISCPU
	| || +---------	IPL1~/BGACK~
	| || |+--------	AS~
	| || ||+-------	WEH~/UDS~/A0
	| || ||| +-----	WEL~/LDS~/DS~
	| || ||| |+----	OE~/R/W~
	| || ||| ||	
(SYSTEM RESET)	0 0X XXX XX	
(RESET)	0 1X XXX XX	
(HALT/RETRY)	1 0X XXX XX	
(RD_LC302)	1 10 X01 10	
(WR_302/RD_LC302)	1 10 10X X0	
(RD_302/WR_LC302)	1 10 10X X1	
(RD_LC302/ALTM_WR_302)	1 10 X0X X0	
(WR_LC302/ALTM_RD_302)	1 10 X0X X1	
(ALT_MASTER_RD)	1 11 00X X1	
(ALT_MASTER_WR)	1 11 00X X0	
(ALT_MASTER)	1 11 00X XX	
(UNKNOWN)	X XX XXX XX	

How Data is Acquired

This part explains how the acquisition module acquires 68302/68LC302 device signals using the TLA_68302 support.

A special clocking program is provided every time the TLA_68302 support is loaded into the acquisition module. When selecting Custom Clocking the module logs in signals from multiple groups of channels at same times when they are valid on the 68302/68LC302 bus. The module then sends all the logged-in signals to the trigger machine and to the acquisition memory of the module for storage.

In Custom clocking the module's clocking state machine (CSM) generates one master sample for each bus cycle, no matter how many sample points are defined for that cycle.

When loading the TLA_68302 support, there is one sample point defined, plus the master sample point. The sample point acquires all signals of the microprocessor. The master sample occurs at the end of the cycle.

Figure 3-1 shows Read cycle type, the sample point and master sample point for acquiring the cycle for both 68302 and 68LC302 Signal OE~ is valid for 68LC302 and LDS~-UDS~ are valid for 68302.

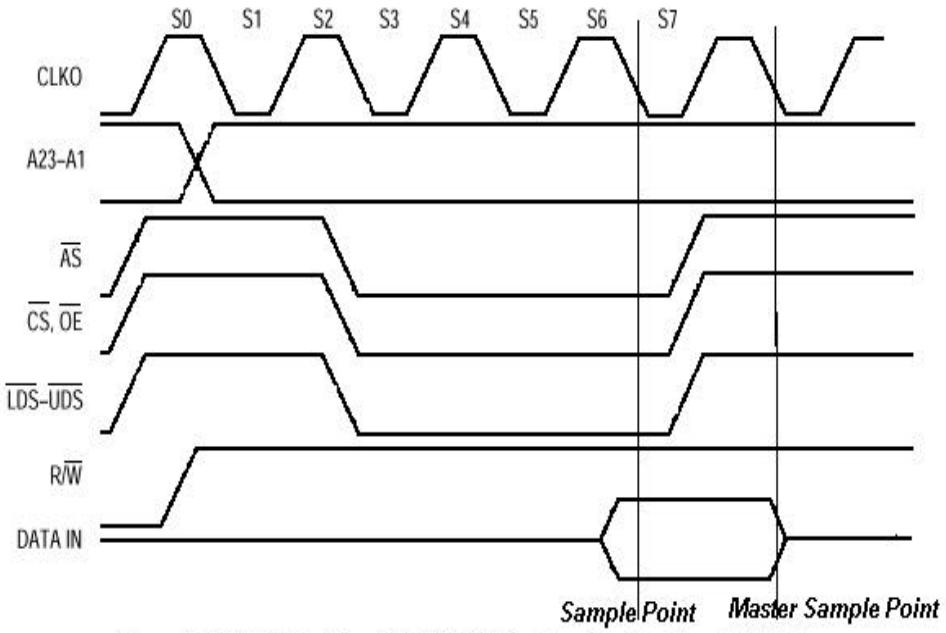

Figure 3-1: 68302 Bus *Read* Timing and Custom Clocking Sample Points

Figure 3-2 shows the Write cycle type with sample point information for both 68302 and 68LC302. LDS~-UDS~ are valid for 68302 and WEH~-WEL~ are valid for 68LC302.

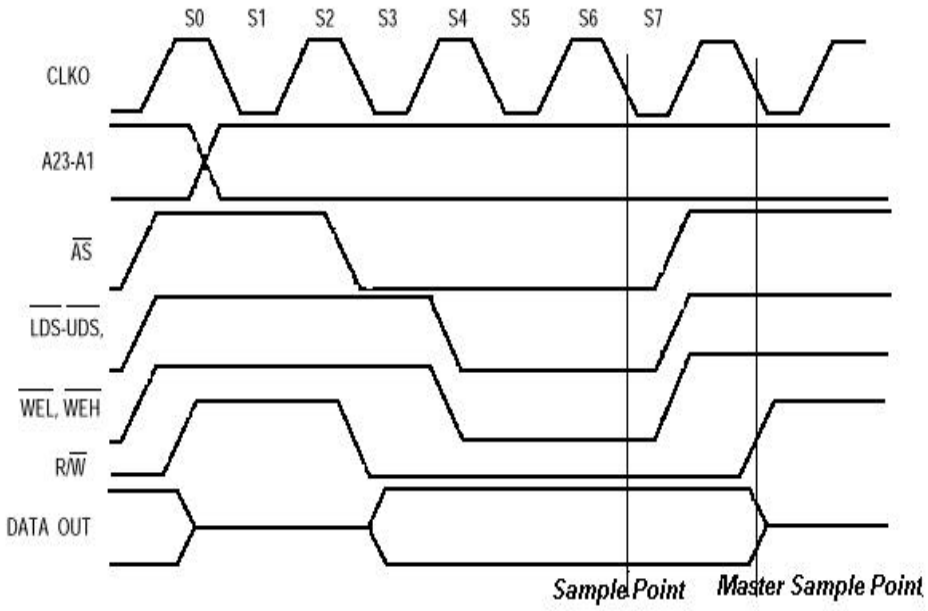

Figure 3-2 : 68302 Bus *Write* Timing and Custom Clocking Sample Points

Custom Fields in the disassembler

This appendix describes disassembly problems that you may encounter while acquiring data.

This sub-menu will have the title: “68302 Controls”.

PROCESSOR

Here is a choice of two processors. Choice is between “68302” and “68LC302”. This Disassembler supports for both of the processors. There is a difference in the number of Address pins and the control signals. Default value is “68302”.

BUSW

Here is a choice between Buswidth-8 and Buswidth-16. It is possible in 68LC302 to change the bus width through software. This does not affect the Logic level of the BUSW pin externally. Default value is Buswidth-16. This selection IS VALID for both processor selections.

BAR

This custom field is required only for 68LC302. The SUPPORT will use this information to display the 24 bit address, when access is made to the Internal memory. This is a 4-digit (hex) fill-in field, to inform the disassembler the value in the BAR, by entering the relevant 16-bit value. Default value is 0x0000.

BR0

This custom field is required only for 68LC302. This input will be used to display 24 bit address when CS0 (chip select 0) is asserted. User will have to enter the relevant 16-bit value. This is a 4-digit (hex) fill-in field, to inform the disassembler the value in the BR0, by entering the relevant 16-bit value. Default value is 0x0000.

BR1

This custom field is required only for 68LC302. This input will be used to display 24 bit address when CS1 (chip select 1) is asserted. User will have to enter the relevant 16-bit value. This is a 4-digit (hex) fill-in field, to inform the disassembler the value in the BR1, by entering the relevant 16-bit value. Default value is 0x0000.

BR2

This custom field is required only for 68LC302. This input will be used to display 24 bit address when CS2 (chip select 2) is asserted. User will have to enter the relevant 16-bit value. This is a 4-digit (hex) fill-in field, to inform the disassembler the value in the BR2, by entering the relevant 16-bit value. Default value is 0x0000.

BR3

This custom field is required only for 68LC302. This input will be used to display 24 bit address when CS3 (chip select 3) is asserted. User will have to enter the relevant 16-bit value. This is a 4-digit (hex) fill-in field, to inform the disassembler the value in the BR3, by entering the relevant 16-bit value. Default value is 0x0000.

Appendix A: Disassembly Problems

This appendix describes disassembly problems that you may encounter while acquiring data.

Disassembly Problems

There may be problems with disassembly for which no error messages are displayed. Some of these problems and their recommended solutions follow.

Check the Disassembly Properties. An incorrect entry in the Disassembly Properties can result in Incorrect Disassembly.

Incorrect Data

If the data acquired is obviously incorrect, check the following:

1. 68302 support is loaded.
2. The Clocking selection is Custom and the correct Processor option is selected.
3. The connections between the acquisition module and the SUT are correct.
   - The clock and 8-channel probe connections are properly oriented (GND connects to ground), the single channel probes are in the right order, and are fully engaged.
   - The probe cables have matched color labels, matched slot numbers, and are properly keyed.

Incorrect Disassembly

If the disassembly is obviously incorrect, check the following:

1. If lots of "- ? -" are displayed in the mnemonics column, check whether the bus mode is setup correctly in the Disassembly Format Definition overlay.
2. Any marks placed by using the F4: MARK DATA key are correct or use the key to correct other errors in the disassembly.

If you are not sure which bus mode is used in your SUT select the default display options for Bus Mode:

- Bus Mode: 16 bit

With this setup the Data column represents 16-bit data .The Address column should show consecutive address values now. Change your Bus Mode setting to ”8 bit, ...” if consecutive address values differ by 1.

Other Suggestions

If the previous suggestions do not fix the problem with acquiring data, disassembled bus cycles, or instruction mnemonics reload the support to restore the system to a known state.

If the logic analyzer still is not acquiring data after trying these solutions, there may be a problem with your 68302 system. Try performing hardware analysis with your logic analyzer to ensure that the signals are valid at the time they are sampled.

Refer to information on basic operations on sampling data using either the Internal or External clocking selections. Also refer to *How Data is Acquired* in the *Specifications* section to see when the disassembler software samples the signals of your SUT.