Instruction Manual

Tektronix

TMS 101
8086 & 8088 Microprocessor Support

070-9804-00

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

Printed in the U.S.A.

Tektronix, Inc., P.O. Box 1000, Wilsonville, OR 97070–1000

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In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period and make suitable arrangements for the performance of service. Customer shall be responsible for packaging and shipping the defective product to the service center designated by Tektronix, with shipping charges prepaid. Tektronix shall pay for the return of the product to Customer if the shipment is to a location within the country in which the Tektronix service center is located. Customer shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other locations.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface: Microprocessor Support Documentation

This instruction manual contains specific information about the TMS 101 8086/8088 microprocessor support and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor supports on the logic analyzer for which the TMS 101 8086/8088 support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor supports, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor supports is included with each product. Each logic analyzer has basic information that describes how to perform tasks common to supports on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing disassembled data
- Using the probe adapter

Manual Conventions

This manual uses the following conventions:

- The term disassembler refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to online help, an installation manual, or a basic operations of microprocessor supports user manual.
- In the information on basic operations, the term XXX or P54C used in field selections and file names can be replaced with 8086/88. This is the name of the microprocessor in field selections and file names you must use to operate the 8086/8088 support.
- The term System Under Test (SUT) refers to the microprocessor-based system from which data will be acquired.

- The term logic analyzer refers to the Tektronix logic analyzer for which this support was purchased.
- The term module refers to a 102/136-channel or a 96-channel module.
- 8086/88 refers to all supported variations of the 8086/8088 microprocessor unless otherwise noted.
- A tilde (~) following a signal name indicates an active low signal.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The manual set provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or, contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Contact your local Tektronix distributor or sales office. Or, visit our web site for a listing of worldwide service locations. http://www.tek.com
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000

Getting Started

Getting Started

This chapter provides information on the following topics:

- A description of the TMS 101 microprocessor support
- Logic analyzer software compatibility
- Your system under test requirements
- Support restrictions
- How to configure the probe adapter
- How to connect to a System Under Test (SUT)

Support Description

The TMS 101 microprocessor support disassembles data from systems that are based on the Intel 8086/8088 microprocessor. The support runs on a compatible Tektronix logic analyzer equipped with a 102/136-channel module or a 96-channel module.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 101 microprocessor support.

Table 1–1 shows the microprocessors and packages from which the TMS 101 support can acquire and disassemble data.

Table 1–1: Supported microprocessors

Name	Package
8086	DIP
8088	DIP
80C86	DIP
80C88	DIP

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Mechanical Parts* chapter.

To use this support efficiently, you need to have the items listed in the information on basic operations as well as the *8086/8088 Microprocessor User's Manual*, Intel, 1994.

Information on basic operations also contains a general description of supports.

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

To use the 8086/8088 support, the Tektronix logic analyzer must be equipped with either a 102/136-channel module, or a 96-channel module at a minimum. The module must be equipped with enough probes to acquire clock and channel data from signals in your 8086/8088-based system.

Refer to information on basic operations to determine how many modules and probes the logic analyzer needs to meet the channel requirements.

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor supports in the information on basic operations as they pertain to your SUT.

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other 8086/8088 support requirements and restrictions.

System Clock Rate. The TMS 101 support can acquire data from the 8086/8088 microprocessor at speeds of up to 16 MHz[1].

Configuring the Probe Adapter

The probe adapter does not require any configuration.

Connecting to a System Under Test

Before you connect to the SUT, you must connect the probes to the module. Your SUT must also have a minimum amount of clear space surrounding the

[1] **Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest devices supported.**

microprocessor to accommodate the probe adapter. Refer to the *Specifications* chapter in this manual for the required clearances.

The channel and clock probes shown in this chapter are for a 102/136-channel module. The probes will look different if you are using a 96-channel module.

The general requirements and restrictions of microprocessor supports in the information on basic operations shows the vertical dimensions of a channel or clock probe connected to square pins on a circuit board.

DIP Probe Adapter

To connect the logic analyzer to a SUT using a DIP probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probe adapter, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. Discharge your stored static electricity by touching the ground connector located on the back of the logic analyzer. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.
3. Place the probe adapter onto the antistatic shipping foam to support the probe as shown Figure 1–1. This prevents the circuit board from flexing and the socket pins from bending.
4. Remove the microprocessor from your SUT.
5. Line up pin 1 on the microprocessor with the pin 1 indicator on the probe adapter board.

CAUTION. *Failure to correctly place the microprocessor into the probe adapter might permanently damage all electrical components once power is applied.*

6. Place the microprocessor into the probe adapter as shown in Figure 1–1.

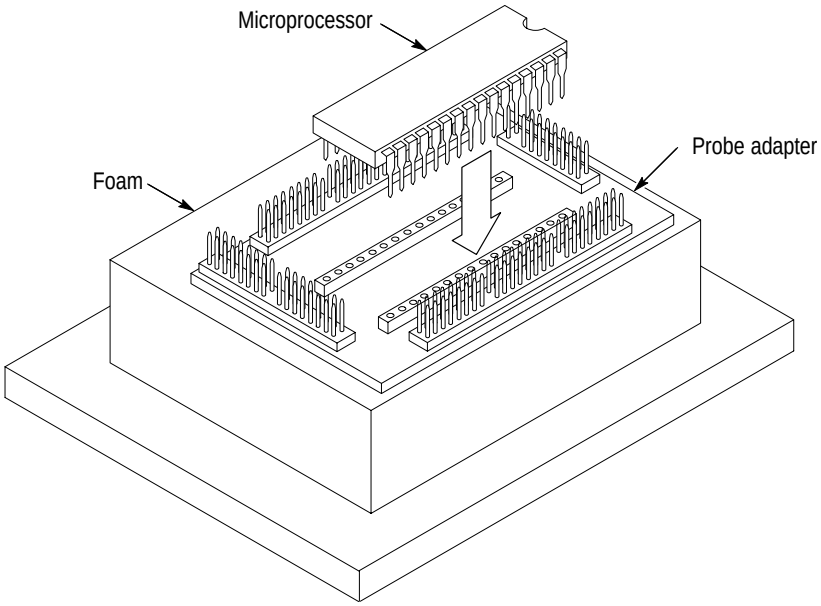


Figure 1–1: Placing a microprocessor into a DIP probe adapter

7. Connect the channel and clock probes to the probe adapter as shown in Figure 1–2. Match the channel groups and numbers on the probe labels to the corresponding pins on the probe adapter. Match the ground pins on the probes to the corresponding pins on the probe adapter.

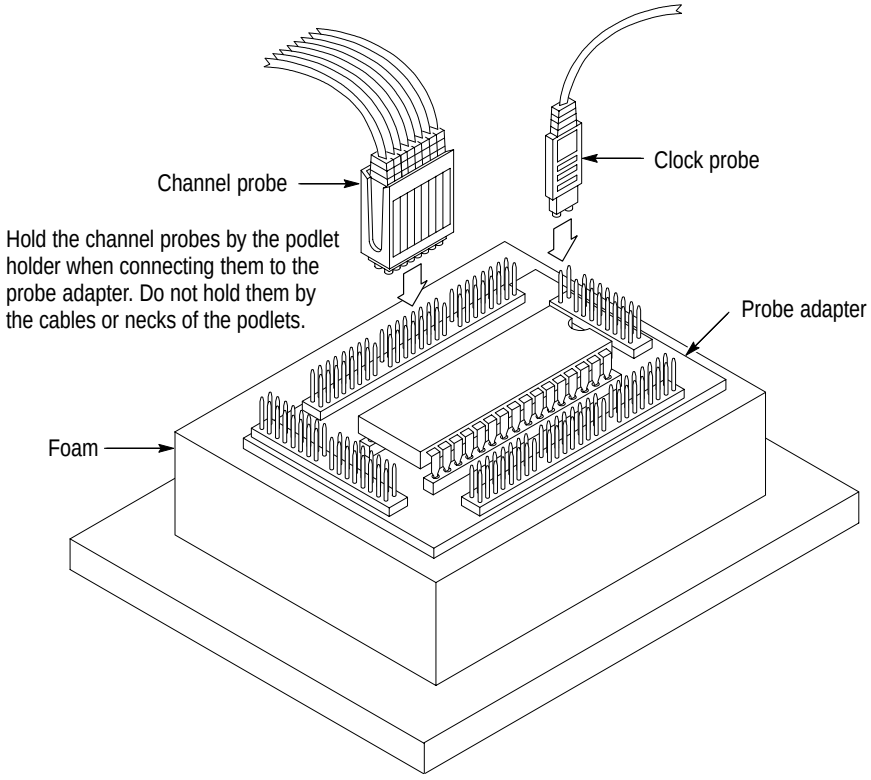


Figure 1–2: Connecting probes to a DIP probe adapter

8. Place the probe adapter onto the SUT as shown in Figure 1–3.

NOTE. *You might need to stack one or more replacement sockets between the SUT and the probe adapter to provide sufficient vertical clearance from adjacent components. However, keep in mind that this might increase loading, which can reduce the electrical performance of your probe adapter.*

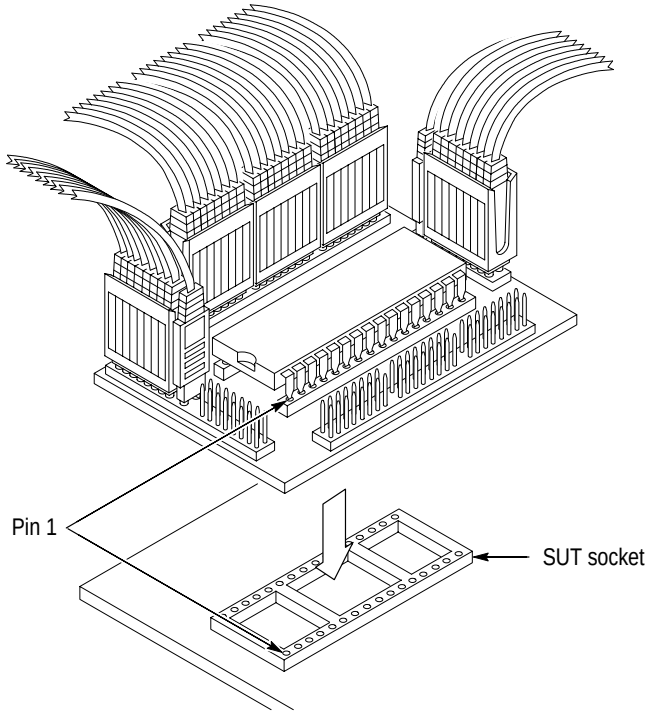


Figure 1–3: Placing a DIP probe adapter onto the SUT

DIP Probe Adapter with a DIP Clip

If your microprocessor is soldered to a circuit board and the probe adapter provides pins to which you can connect a DIP clip, you will need to use the DIP converter clip with the probe adapter.

One end of the converter clip connects to square pins on the probe adapter. The other end connects to the microprocessor in your SUT. To connect the logic analyzer to your SUT using a DIP probe adapter with a clip, refer to Figure 1–4 and follow these steps:

1. Follow steps 1, 2, and 3 in the previous procedure.
2. Line up the colored stripe on the side of the ribbon cable with the pin-1 indicator on the probe adaptor.

NOTE. *The colored stripe along the side of the cable indicates that it connects to pin 1 on the probe adapter and pin 1 of the microprocessor.*

3. Connect the cable end to the square pins on the probe adapter.
4. Follow step 7 in the previous procedure.
5. Connect the clip end to the microprocessor.

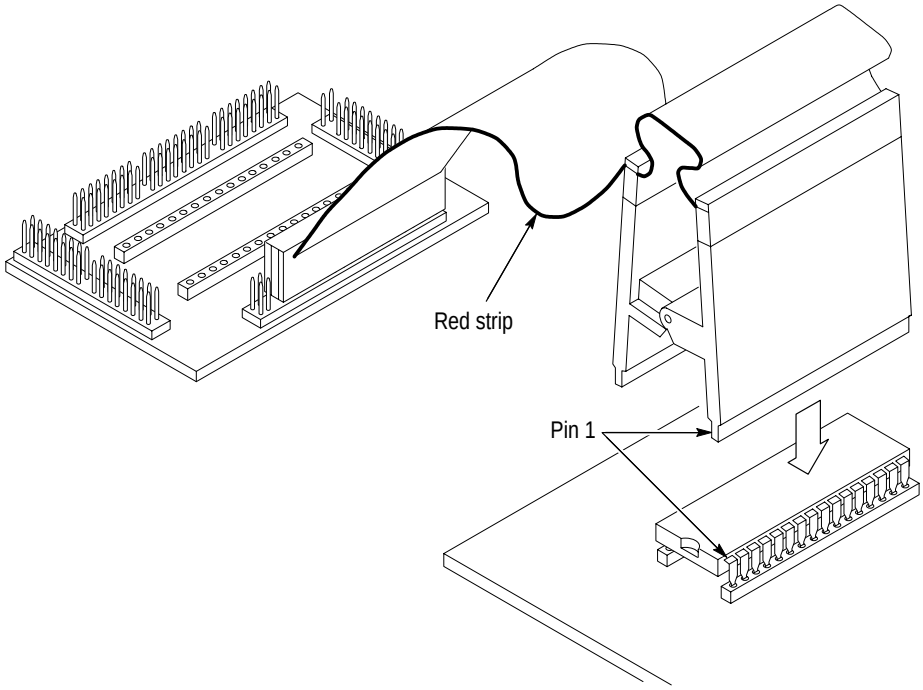


Figure 1–4: Connecting to the SUT using a DIP converter clip

Without a Probe Adapter

You can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your SUT.

To connect the probes to 8086/8088 signals in the SUT using a test clip, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from it.

CAUTION. *Failure to place the SUT on a horizontal surface before connecting the test clip might permanently damage the pins on the microprocessor.*

3. Place the SUT on a horizontal static-free surface.
4. Use Table 1–2 to connect the channel probes to 8086/8088 signal pins on the test clip or in the SUT.

   Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip.
5. Align pin 1 or A1 of your test clip with the corresponding pin 1 or A1 of the 8086/8088 microprocessor in your SUT and attach the clip.

Table 1–2: 8086/8088 signal connections for channel probes

Selection: Channel	8086 signal name: MIN mode	8086 signal name: MAX mode	8088 signal name: MIN mode	8088 signal name: MAX mode
A3:7				
A3:6				
A3:5				
A3:4				
A3:3				
A3:2				
A3:1				
A3:0				
A2:7	IO_M~_T*	S2~	IO_M~_T*	S2~
A2:6	DT_R~_T*	S1~	DT_R~_T*	S1~
A2:5	DEN~_T*	S0~	DEN~_T*	S0~
A2:4	BHE~	BHE~	SS0~	SS0
A2:3	A19	A19	A19	A19
A2:2	A18	A18	A18	A18
A2:1	A17	A17	A17	A17
A2:0	A16	A16	A16	A16
A1:7	A15	A15	A15	A15
A1:6	A14	A14	A14	A14
A1:5	A13	A13	A13	A13
A1:4	A12	A12	A12	A12
A1:3	A11	A11	A11	A11
A1:2	A10	A10	A10	A10
A1:1	A9	A9	A9	A9

Table 1–2: 8086/8088 signal connections for channel probes (cont.)

Selection: Channel	8086 signal name: MIN mode	8086 signal name: MAX mode	8088 signal name: MIN mode	8088 signal name: MAX mode
A1:0	A8	A8	A8	A8
A0:7	A7	A7	A7	A7
A0:6	A6	A6	A6	A6
A0:5	A5	A5	A5	A5
A0:4	A4	A4	A4	A4
A0:3	A3	A3	A3	A3
A0:2	A2	A2	A2	A2
A0:1	A1	A1	A1	A1
A0:0	A0	A0	A0	A0
D3:7				
D3:6				
D3:5				
D3:4				
D3:3				
D3:2				
D3:1				
D3:0				
D2:7	M/IO~		M/IO~	
D2:6	DT/R~		DT/R~	
D2:5	DEN~		DEN~	
D2:4	S7	S7	S7	S7
D2:3	S6	S6	S6	S6
D2:2	S5	S5	S5	S5
D2:1	S4	S4	S4	S4
D2:0	S3	S3	S3	S3
D1:7	D15	D15		
D1:6	D14	D14		
D1:5	D13	D13		
D1:4	D12	D12		
D1:3	D11	D11		
D1:2	D10	D10		
D1:1	D9	D9		
D1:0	D8	D8		
D0:7	D7	D7	D7	D7
D0:6	D6	D6	D6	D6

Table 1–2: 8086/8088 signal connections for channel probes (cont.)

Selection: Channel	8086 signal name: MIN mode	8086 signal name: MAX mode	8088 signal name: MIN mode	8088 signal name: MAX mode
D0:5	D5	D5	D5	D5
D0:4	D4	D4	D4	D4
D0:3	D3	D3	D3	D3
D0:2	D2	D2	D2	D2
D0:1	D1	D1	D1	D1
D0:0	D0	D0	D0	D0
C3:7				
C3:6	CLK_B *	CLK_B * †	CLK_B *	CLK_B * †
C3:5	TEST~	TEST~ †	TEST~	TEST~ †
C3:4	READY	READY †	READY	READY †
C3:3	INTR	INTR †	INTR	INTR †
C3:2	NMI	NMI †	NMI	NMI †
C3:1	HLDA †	RQ~/GT1~ †	HLDA †	RQ~/GT1~ †
C3:0	HOLD †	RQ~/GT0~ †	HOLD †	RQ~/GT0~ †
C2:7	RD~	RD~	RD~	RD~
C2:6	WR~	LOCK~	WR~	LOCK~
C2:5	INTA~	QS1	INTA~	QS1
C2:4	ALE	QS0	ALE	QS0
C2:3	MN/MX~	MN/MX~	MN/MX~	MN/MX~
C2:2	EOC_D *	EOC_D *	EOC_D *	EOC_D *
C2:1	HLDA_D *	HLDA_D *	HLDA_D *	HLDA_D *
C2:0	RESET	RESET	RESET	RESET
C1:7				
C1:6				
C1:5				
C1:4				
C1:3				
C1:2				
C1:1				
C1:0				
C0:7				
C0:6				
C0:5				
C0:4				
C0:3				

Table 1–2: 8086/8088 signal connections for channel probes (cont.)

Selection: Channel	8086 signal name: MIN mode	8086 signal name: MAX mode	8088 signal name: MIN mode	8088 signal name: MAX mode
C0:2				
C0:1				
C0:0				

***** **Derived signal**
† **Signal not required for disassembly**

Table 1–3 shows the clock probes and the 8086/8088 signals to which they must connect for disassembly to be correct.

Table 1–3: 8086/8088 signal connections for clock probes

Section:channel	8086/8088 signal
CK:3	CLK
CK:2	STATUS_D
CK:1	ALE_L

Operating Basics

Setting Up the Support

This section provides information on how to set up the support. Information in this section covers the following topics:

- Channel group definitions
- Clocking options
- Symbol table files

Remember that the information in this section is specific to the operations and functions of the TMS 101 8086/8088 support on any Tektronix logic analyzer for which it can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and disassemble data, you need to load the support and specify setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The disassembler software automatically defines channel groups for the support. The channel groups for the 8086/8088 support are Address, Data, Control, and Misc.

Clocking Options

The TMS 101 support offers a microprocessor-specific clocking mode for the 8086/8088 microprocessor. This clocking mode is the default selection whenever you load the 8086/88 support.

A description of how cycles are sampled by the module using the support and probe adapter is found in the *Specifications* chapter.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

The clocking option for the TMS 101 support is DMA Cycles.

DMA Cycles A DMA cycle is defined as the cycle in which the 8086/8088 microprocessor gives up the bus to an alternate device (a DMA device or another microprocessor). These types of cycles are acquired when you select Included.

Symbols

The TMS 101 support supplies four symbol table files:

- 8086MN_Ctrl for the 8086 in MIN mode
- 8086MX_Ctrl for the 8086 in MAX mode
- 8088MN_Ctrl for the 8088 in MIN mode
- 8088MX_Ctrl for the 8088 in MAX mode

These files replaces specific Control channel group values with symbolic values when Symbolic is the radix for the channel group.

Table 2–1 shows the name, bit pattern, and meaning for the symbols in the file 8086MX_Ctrl, the Control channel group symbol table.

Table 2–1: Control group symbol table for the 8086 in MAX Mode

Symbol	Control group value RD~ BHE~ LOCK~ S7	S6 S5 S4 S3	MIN/MAX~ QS1 QS0 S2~	S1~ S0~ HLDA_D RESET	Meaning
RESET	X X X X	X X X X	0 X X X	X X X 1	RESET signal asserted
DMA_READ	X X X X	X X X X	0 X X X	0 1 1 0	DMA read
DMA_WRITE	X X X X	X X X X	0 X X X	1 0 1 0	DMA write
DMA	X X X X	X X X X	0 X X X	X X 1 0*	Any DMA
FETCH	X X X X	X X X X	0 X X 1	0 0 0 0	Memory code read (opcode fetch)
HALT	X X X X	X X X X	0 X X 0	1 1 0 0	Processor halted
MEM_READ	X X 1 X	X X X X	0 X X 1	0 1 0 0	Data read cycle (opcode fetch)
MEM_WRITE	X X 1 X	X X X X	0 X X 1	1 0 0 0	Any memory write
I/O_READ	X X 1 X	X X X X	0 X X 0	0 1 0 0	Read from I/O space
I/O_WRITE	X X 1 X	X X X X	0 X X 0	1 0 0 0	Write to I/O space
INT_ACK	X X X X	X X X X	0 X X 0	0 0 0 0	Responding to an interrupt
LKD_M_RD	X X 0 X	X X X X	0 X X 1	0 1 0 0	Locked data read cycle (nonopcode fetch)
LKD_M_WR	X X 0 X	X X X X	0 X X 1	1 0 0 0	Locked memory write cycle
LKD_IO_RD	X X 0 X	X X X X	0 X X 0	0 1 0 0	Locked read from I/O space

Table 2–1: Control group symbol table for the 8086 in MAX Mode (cont.)

Symbol	Control group value RD~ BHE~ LOCK~ S7 / S6 S5 S4 S3 / MIN/MAX~ QS1 QS0 S2~ / S1~ S0~ HLDA_D RESET	Meaning
LKD_IO_WR	X X 0 X / X X X X / 0 X X 0 / 1 0 0 0	Locked write to I/O space
LOCKED	X X 0 X / X X X X / 0 X X X / X X 0 0*	Inseparable back-to-back cycles
READ	X X X X / X X X X / 0 X X X / 0 1 0 0*	Any memory or I/O read cycles except an Opcode Fetch
WRITE	X X X X / X X X X / 0 X X X / 1 0 0 0*	Any memory or I/O write
WRONGMODE	X X X X / X X X X / 1 X X X / X X X X	The processor is not in MAX mode

***** **Symbols used only for triggering, they are not displayed.**

Table 2–2 shows the name, bit pattern, and meaning for the symbols in the file 8088MX_Ctrl, the Control channel group symbol table.

Table 2–2: Control group symbol table for the 8088 in MAX Mode

Symbol	Control group value RD~ SSO~ LOCK~ S7 / S6 S5 S4 S3 / MIN/MAX~ QS1 QS0 S2~ / S1~ S0~ HLDA_D RESET	Meaning
RESET	X X X X / X X X X / 0 X X X / X X X 1	RESET signal asserted
DMA_READ	X X X X / X X X X / 0 X X 1 / 0 1 1 0	DMA read
DMA_WRITE	X X X X / X X X X / 0 X X 1 / 1 0 1 0	DMA write
DMA	X X X X / X X X X / 0 X X 1 / X X 1 0*	Any DMA
FETCH	X X X X / X X X X / 0 X X 1 / 0 0 0 0	Memory code read (opcode fetch)
HALT	X X X X / X X X X / 0 X X 0 / 1 1 0 0	Processor halted
MEM_READ	X X 1 X / X X X X / 0 X X 1 / 0 1 0 0	Data read cycle (opcode fetch)
MEM_WRITE	X X 1 X / X X X X / 0 X X 1 / 1 0 0 0	Any memory write
I/O_READ	X X 1 X / X X X X / 0 X X 0 / 0 1 0 0	Read from I/O space
I/O_WRITE	X X 1 X / X X X X / 0 X X 0 / 1 0 0 0	Write to I/O space
INT_ACK	X X X X / X X X X / 0 X X 0 / 0 0 0 0	Responding to an interrupt
LKD_M_RD	X X 0 X / X X X X / 0 X X 1 / 0 1 0 0	Locked data read cycle (nonopcode fetch)
LKD_M_WR	X X 0 X / X X X X / 0 X X 1 / 1 0 0 0	Locked memory write cycle
LKD_IO_RD	X X 0 X / X X X X / 0 X X 0 / 0 1 0 0	Locked read from I/O space
LKD_IO_WR	X X 0 X / X X X X / 0 X X 0 / 1 0 0 0	Locked write to I/O space
LOCKED	X X 0 X / X X X X / 0 X X X / X X 0 0*	Inseparable back-to-back cycles

Table 2–2: Control group symbol table for the 8088 in MAX Mode (cont.)

Symbol	Control group value RD~ SSO~ LOCK~ S7 / S6 S5 S4 S3 / MIN/MAX~ QS1 QS0 S2~ / S1~ S0~ HLDA_D RESET	Meaning
READ	X X X X / X X X X / 0 X X X / 0 1 0 0*	Any memory or I/O read cycles except an Opcode Fetch
WRITE	X X X X / X X X X / 0 X X X / 1 0 0 0*	Any memory or I/O write
WRONGMODE	X X X X / X X X X / 1 X X X / X X X X	The processor is not in MAX mode

* **Symbols used only for triggering, they are not displayed.**

Table 2–3 shows the name, bit pattern, and meaning for the symbols in the file 8086MN_Ctrl, the Control group symbol table for the 8086 in MIN mode.

Table 2–3: Control group symbol table for the 8086 in MIN Mode

Symbol	Control group value RD~ BHE~ WR~ S7 / S6 S5 S4 S3 / MIN/MAX~ INTA~ ALE M/IO~ / DT/R~ DEN~ HLDA_D RESET	Meaning
RESET	X X X X / X X X X / 1 X X X / X X X 1	RESET signal asserted
DMA_READ	X X X X / X X X X / 1 1 X 1 / 0 X 1 0	DMA read
DMA_WRITE	X X X X / X X X X / 1 1 X 1 / 1 X 1 0	DMA write
DMA	X X X X / X X X X / 1 1 X 1 / X X 1 0*	Any DMA
FETCH_CS	X X X X / X X 1 0 / 1 1 X 1 / 0 X 0 0	Memory code read (opcode fetch)
MEM_READ	X X X X / X X X X / 1 1 X 1 / 0 X 0 0	Data read cycle (opcode fetch)
MEM_WRITE	X X X X / X X X X / 1 1 X 1 / 1 X 0 0	Any memory write
I/O_READ	X X X X / X X X X / 1 1 X 0 / 0 X 0 0	Read from I/O space
I/O_WRITE	X X X X / X X X X / 1 1 X 0 / 1 X 0 0	Write to I/O space
READ	X X X X / X X X X / 1 1 X X / 0 X 0 0*	Any memory or I/O read cycles except an Opcode Fetch
WRITE	X X X X / X X X X / 1 1 X X / 1 X 0 0*	Any memory or I/O write
INT_ACK	X X X X / X X X X / 1 0 X X / X X X 0	Responding to an interrupt
WRONGMODE	X X X X / X X X X / 0 X X X / X X X X	The processor is not in MAX mode

* **Symbols used only for triggering, they are not displayed.**

Table 2–4 shows the name, bit pattern, and meaning for the symbols in the file 8086MN_Ctrl, the Control group symbol table for the 8088 in MIN mode.

Table 2–4: Control group symbol table for the 8088 in MIN Mode

Symbol	Control group value RD~ sso~ WR~ S7 / S6 S5 S4 S3 / MIN/MAX~ INTA~ ALE IO/M~ / DT/R~ DEN~ HLDA_D RESET	Meaning
RESET	X X X X / X X X X / 1 X X X / X X X 1	RESET signal asserted
DMA_READ	X 1 X X / X X X X / 1 1 X 0 / 0 X 1 0	DMA read
DMA_WRITE	X 0 X X / X X X X / 1 1 X 0 / 1 X 1 0	DMA write
DMA	X X X X / X X X X / 1 1 X 0 / X X 1 0*	Any DMA
FETCH	X 0 X X / X X X X / 1 1 X 0 / 0 X 0 0	Memory code read (opcode fetch)
HALT	X 1 X X / X X X X / 1 X X 1 / 1 X 0 0	Processor halted
MEM_READ	X 1 X X / X X X X / 1 1 X 0 / 0 X 0 0	Data read cycle (opcode fetch)
MEM_WRITE	X 0 X X / X X X X / 1 1 X 0 / 1 X 0 0	Any memory write
I/O_READ	X 1 X X / X X X X / 1 1 X 1 / 0 X 0 0	Read from I/O space
I/O_WRITE	X 0 X X / X X X X / 1 1 X 1 / 1 X 0 0	Write to I/O space
READ	X X X X / X X X X / 1 1 X X / 0 X 0 0*	Any memory or I/O read cycles except an Opcode Fetch
WRITE	X X X X / X X X X / 1 1 X X / 1 X 0 0*	Any memory or I/O write
INT_ACK	X X X X / X X X X / 1 0 X X / X X X 0	Responding to an interrupt
WRONGMODE	X X X X / X X X X / 0 X X X / X X X X	The processor is not in MAX mode

*** Symbols used only for triggering, they are not displayed.**

Information on basic operations describes how to use symbolic values for triggering and for displaying other channel groups symbolically, such as the Address channel group.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. Information covers the following topics:

- Acquiring data
- Viewing disassembled data in various display formats
- Cycle type labels
- How to change the way data is displayed
- How to change disassembled cycles with the mark cycles function

Acquiring Data

Once you load the 8086/88 support, choose a clocking mode and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual.

Viewing Disassembled Data

You can view disassembled data in four different display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE. *Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–10.*

The default display format shows the Address, Data, and Control channel group values for each sample of acquired data.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–5 shows these special characters and strings, and gives a definition of what they represent.

Table 2–5: Meaning of special characters in the display

Character or string displayed	Meaning
>>	The instruction was manually marked.
****	Indicates there is insufficient data available for complete disassembly of the instruction; the number of asterisks will indicate the width of the data that is unavailable. Each two asterisks represent a byte.

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–6 shows these cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled with the vector name.

Table 2–6: Cycle type definitions

Cycle Type	Definition
(RESET)	The RESET signal is asserted
(DMA READ)	A DMA read cycle
(DMA WRITE)	A DMA write cycle
(HALT)	The processor is halted
(INT ACK)	An interrupt acknowledge cycle
(I/O READ)	A read from I/O space
(I/O WRITE)	A write to I/O space
(MEM READ)	A read from memory that is not an opcode fetch
(MEM WRITE)	Any write to memory
(NO DATA)	Invalid data
(LOCKED MEM READ)	A locked read from memory
(LOCKED MEM WRITE)	A locked write to memory
(LOCKED I/O READ)	A locked read from I/O space
(LOCKED I/O WRITE)	A locked write to I/O space
(FLUSH)	A fetch cycle computed to be an opcode flush
(EXTENSION)	A fetch cycle computed to be an opcode extension
(WRONG MODE : MIN)	Disassembler is in MAX mode and MN/MX~ is high

Table 2–6: Cycle type definitions (cont.)

Cycle Type	Definition
(WRONG MODE : MAX)	Disassembler is in MIN mode and MN/MX~ is low
(UNKNOWN)	An unexpected or unrecognized Control channel group value

Figure 2–1 shows an example of the Hardware display.

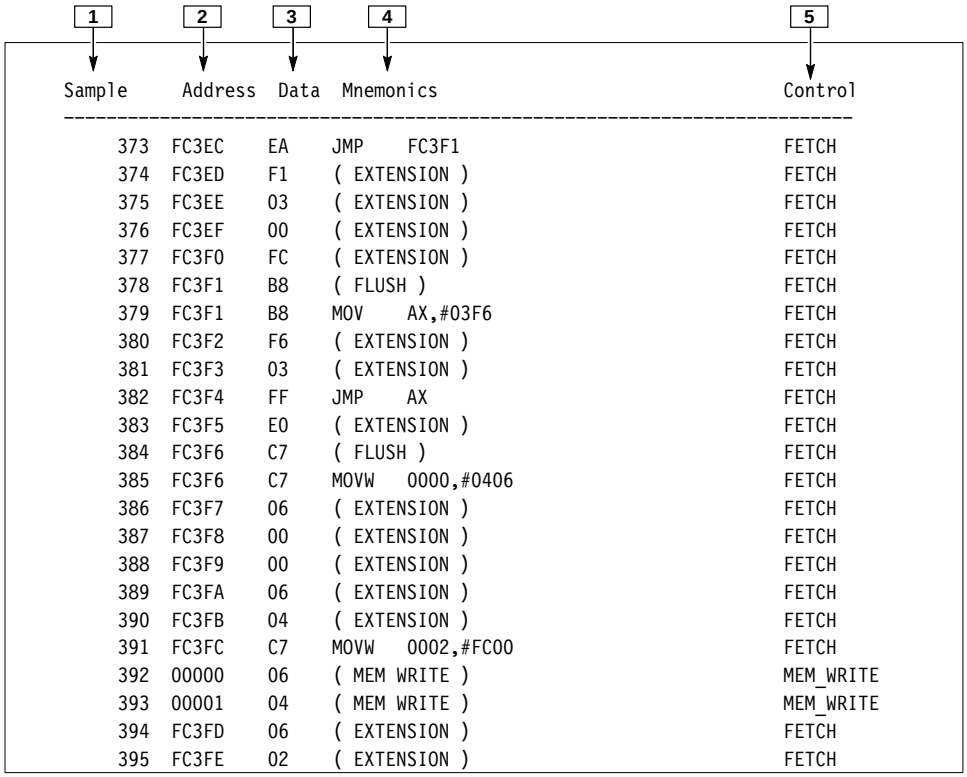


Figure 2–1: Hardware display format

1 **Sample Column.** Lists the memory locations for the acquired data.

2 **Address Group.** Lists data from channels connected to the 8086/8088 Address bus.

3 **Data Group.** Lists data from channels connected to the 8086/8088 Data bus.

4 **Mnemonic Column.** Lists the disassembled instructions and cycle types.

5 **Control Group Column.** Lists data from channels connected to the 8086/8088 Control bus.

6 **Timestamp.** Lists the timestamp values when a timestamp selection is made. Information on basic operations describes how you can select a timestamp.

Control Flow Display Format

The Control Flow display format shows only the first fetch of instructions that change the flow of control.

Instructions that generate a change in the flow of control in the 8086/8088 microprocessor are as follows:

CALL	JLE	JNS
INTO	JMP	JO
INTX	JNB	JP
IRET	JNBE	JS
JB	JNE	LOOP
JCXZ	JNL	LOOPNZ
JE	JNLE	LOOPZ
JL	JNO	RET

Subroutine Display Format

The Subroutine display format shows only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

Instructions that generate a subroutine call or a return in the 8086/8088 microprocessor are as follows:

CALL	INTX	RET
INTO	IRET	

Changing How Data is Displayed

There are fields and features that allow you to further modify displayed data to suit your needs. You can make selections unique to the 8086/8088 support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception vectors

There are no new fields for this support product. Refer to the information on basic operations for descriptions of common fields.

Optional Display Selections

You can make optional display selections for disassembled data to help you analyze the data. You can make these selections in the Disassembly property page (the Disassembly Format Definition overlay).

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it to one of the following cycle types:

- Opcode (the first word of an instruction)
- Extension (a subsequent word of an instruction)
- Flush (an opcode or extension that is fetched but not executed)
- Anything (any valid opcode, extension or flush)
- Read (marks a memory reference read as data)

Information on basic operations contains more details on marking cycles.

Mark selections for an 8-bit bus are listed in Table 2–7.

Table 2–7: Prefetch cycles for 8-bit bus

Program Fetch Cycle	Description
Opcode	The one-byte cycle will be disassembled as the beginning of an instruction
Extension	The one-byte cycle is treated as an extension of the previous instruction
Flush	The one-byte cycle is not disassembled
Undo Mark	Remove all marks from the current sequence

Mark selections for a 16-bit bus are listed in Table 2–8.

Table 2–8: Prefetch cycles for 16-bit bus

Program Fetch Cycle	Description
Any Opcode	The low byte of the cycle will be disassembled as the beginning of an instruction. The high byte is not marked.
Opcode Extension	The low byte of the cycle is treated as an instruction extension. The high byte is not marked.
Opcode Flush	The low byte of the cycle is not disassembled and the high byte of the cycle is not marked.
Flush Extension	The high byte of the cycle is not disassembled and the low byte of the cycle is treated as an instruction extension.
Flush Flush	The cycle is not disassembled.
Extension Extension	Both bytes are treated as extensions.
Read (8086MN Mode only)	The cycle is treated as a read.
Undo Mark	Remove all marks from the current sequence.

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your 8086/8088 microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your SUT.

Information on basic operations describes how to view the file.

Specifications

Specifications

This chapter contains the following information:

- Probe adapter description
- Specification tables
- Dimensions of the probe adapter
- Channel assignment tables
- Description of how the module acquires 8086/8088 signals
- List of other accessible microprocessor signals and extra acquisition channels

Probe Adapter Description

The probe adapter is nonintrusive hardware that allows the logic analyzer to acquire data from a microprocessor in its own operating environment with little effect, if any, on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and a socket for an 8086/8088 microprocessor. The probe adapter connects to the microprocessor in the SUT. Signals from the microprocessor-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

All circuitry on the probe adapter is powered from the SUT.

If you are using the optional DIP clip, the circuit board contains a 3 Amp fuse in series with the 5 Volt power plane. The fuse can be replaced with a discrete part if it opens. The 3 Amp fuse does not protect the circuitry when the power is supplied from a source other then the DIP clip.

The probe adapter accommodates the Intel 8086/8088 microprocessor in a 40-pin DIP package.

Configuration

The probe adapter does not require any configuration.

Specifications

These specifications are for a probe adapter connected between a compatible Tektronix logic analyzer and a SUT. Table 3–1 shows the electrical requirements the SUT must produce for the support to acquire correct data.

In Table 3–1, for the 102/136-channel module, one podlet load is 20 kΩ in parallel with 2 pF. For the 96-channel module, one podlet load is 100 kΩ in parallel with 10 pF.

Table 3–1: Electrical specifications

Characteristics	Requirements
SUT DC Power Requirements	
Voltage	4.75-5.25 VDC
Current	I max (calculated) 200 mA I typ (measured) 130 mA
SUT Clock	
Clock Rate	Min. DC Max. 16 MHz
Minimum Setup Time Required	
Address, Data, Control	5 ns
Relative to CLK rising edge:	
S0~-S2~ inactive to active (MAX Mode only)	3.6 ns
RQ~/GTx~ (MAX Mode only)	3.6 ns
ALE (MIN Mode only)	3.6 ns
Relative to CLK falling edge:	
S0~-S2~ active to inactive (MAX Mode only)	15 ns *
HLDA (MIN Mode only)	16.5 ns *
RD~, WR~, INTA~ (MIN Mode only)	16.5 ns *
All Other Signals	5 ns
Minimum Hold Time Required	
All Signals	0 ns

Table 3–1: Electrical specifications (cont.)

Characteristics	Requirements	
	Specification	
	AC Load	DC Load
Measured Typical SUT Signal Loading		
CLK, S0~-S2~, MIN/MAX~, HOLD, HLDA, RD~, ALE	17 pf + 1 podlet	1, 22V10C + 1 podlet
LOCK~, INTA~	17 pf + 1 podlet	same as above
RESET	17 pf + 1 podlet	same as above
Other Signals	6 pf + 1 podlet	1 podlet

*** 10 ns worst case PAL propagation delay and 5 ns logic analyzer setup time. The 8086/8088 microprocessors must meet this specification with plenty of margin.**

Table 3–2 shows the environmental specifications.

Table 3–2: Environmental specification*

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F)†
Minimum operating	0° C (+32° F)
Non-operating	–55° C to +75° C (–67° to +167° F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

*** Designed to meet Tektronix standard 062-2847-00 class 5.**

† **Not to exceed 8086/8088 microprocessor thermal considerations. Forced air cooling might be required across the CPU.**

Table 3–3 shows the certifications and compliances that apply to the probe adapter.

Table 3–3: Certifications and compliances

There are no applicable directives that apply to this product.

Figure 3–1 shows the dimensions of the probe adapter. Information on basic operations shows the vertical clearance of the channel and clock probes when connected to a probe adapter in the description of general requirements and restrictions.

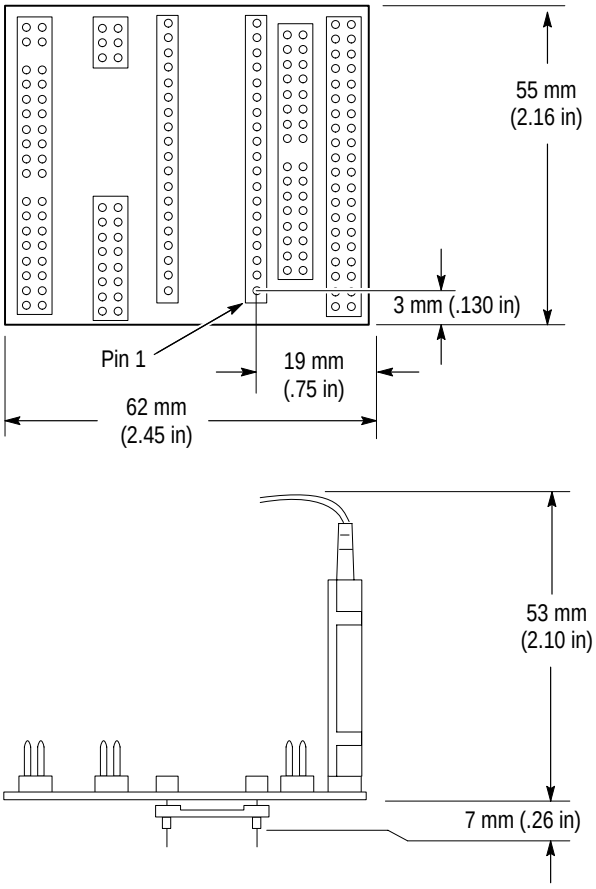


Figure 3–1: Dimensions of the probe adapter

Channel Assignments

Channel assignments shown in Table 3–4 through Table 3–8 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the Most Significant Bit (MSB) descending to the Least Significant Bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- A tilde (~) following a signal name indicates an active low signal
- An equals sign (=) following a signal name indicates that it is double probed.

Table 3–4 shows the probe section and channel assignments for the Address group and the microprocessor signal to which each channel connects. By default this channel group is displayed in hexadecimal.

Table 3–4: Address group channel assignments

Bit order	Section: channel	8086/8088 signal name
19	A2:3	A19/S6
18	A2:2	A18/S5
17	A2:1	A17/S4
16	A2:0	A16/S3
15	A1:7	AD15
14	A1:6	AD14
13	A1:5	AD13
12	A1:4	AD12
11	A1:3	AD11
10	A1:2	AD10
9	A1:1	AD9
8	A1:0	AD8
7	A0:7	AD7
6	A0:6	AD6
5	A0:5	AD5
4	A0:4	AD4
3	A0:3	AD3
2	A0:2	AD2
1	A0:1	AD1
0	A0:0	AD0

Table 3–5 shows the probe section and channel assignments for the Data group and the microprocessor signal to which each channel connects. By default this channel group is displayed in hexadecimal.

Table 3–5: Data group channel assignments

Bit order	Section: channel	8086/8088 signal name
15	A1:7	AD15
14	A1:6	AD14
13	A1:5	AD13
12	A1:4	AD12
11	A1:3	AD11
10	A1:2	AD10
9	A1:1	AD9
8	A1:0	AD8
7	A0:7	AD7
6	A0:6	AD6
5	A0:5	AD5
4	A0:4	AD4
3	A0:3	AD3
2	A0:2	AD2
1	A0:1	AD1
0	A0:0	AD0

Table 3–6 shows the probe section and channel assignments for the Control group and the microprocessor signal to which each channel connects. By default this channel group is displayed symbolically.

Table 3–6: Control group channel assignments

Bit order	Channel	8086 MAX signal name	8086 MIN signal name	8088 MAX signal name	8088 MIN signal name
15	C2:7	RD~	RD~	RD~	RD~
14	A2:4	BHE~	BHE~	SS0	SS0~
13	C2:6	LOCK~	WR~	LOCK~	WR~
12	D2:4	S7	S7	S7	S7
11	D2:3	S6	S6	S6	S6
10	D2:2	S5	S5	S5	S5
9	D2:1	S4	S4	S4	S4
8	D2:0	S3	S3	S3	S3
7	C2:3	MN/MX~	MN/MX~	MN/MX~	MN/MX~
6	C2:5	QS1	INTA~	QS1	INTA~
5	C2:4	QS0	ALE	QS0	ALE
4	A2:7	S2~	M/IO~	S2~	IO/M~
3	A2:6	S1~	DT/R~	S1~	DT/R~
2	A2:5	S0~	DEN~	S0~	DEN~
1	C2:1	HLDA_D	HLDA_D	HLDA_D	HLDA_D
0	C2:0	RESET	RESET	RESET	RESET

Table 3–7 shows the probe section and channel assignments for the Misc group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–7: Misc group channel assignments

Bit Order	Channel	8086/8088 signal name: MAX mode	8086/8088 signal same: MIN mode
6	C3:6	CLK_B*	CLK_B*
5	C3:5	TEST~*	TEST~*
4	C3:4	READY*	READY*
3	C3:3	INTR*	INTR*
2	C3:2	NMI*	NMI*
1	C3:1	RQ~/GT1~*	HOLDA
0	C3:0	RQ~/GT0~*	HOLD

* Signals not required for disasembly.

Table 3–8 shows the probe section and channel assignments for the clock probes (not part of any group) and the 8086/8088 signal to which each channel connects.

Table 3–8: Clock channel assignments

Channel	CLK or QUAL	8086/8088 signal name
CK:3	CLK	CLK
CK:2	QUAL	STATUS_D*
CK:1	QUAL	ALE_L
C2:3	QUAL	MIN/MAX~
C2:2	QUAL	EOC_D*
C2:1	QUAL	HLDA_D*
C2:0	QUAL	RESET

* Derived signals.

These channels are used only to clock in data; they are not acquired or displayed. To acquire data from any of the signals shown in Table 3–8, you must connect another channel probe to the signal, a technique called double probing. An equals sign (=) following a signal name indicates that it is already double probed.

How Data is Acquired

This part of this chapter explains how the module acquires 8086/8088 signals using the TMS 101 software and probe adapter. This part of this chapter also provides additional information on microprocessor signals accessible on or not accessible on the probe adapter, and on extra acquisition channels available for you to use for additional connections.

Custom Clocking

A special clocking program is loaded to the module every time you load the 8086/88 support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple groups of channels at different times as they become valid on the 8086/8088 bus. The module then sends all the logged-in signals to the trigger machine and to the acquisition memory of the module for storage.

In Custom clocking, the module Clocking State Machine (CSM) generates one master sample for each microprocessor bus cycle, no matter how many clock cycles are contained in the bus cycle.

Figures 3–2 and 3–3 show sample points AC (Address sample point) and DC (Data sample point), in addition to MC (Master Clock sample point).

The TMS 101 uses a PAL (22V10C) on the probe adapter to decode the status lines and determine the sample points for the disassembler. The PAL decodes the 8086/8088 signals differently depending on the mode used (MAX or MIN):

- In MAX mode, the status lines become valid after the rising edge of CLK, and become invalid several cycles later after the falling edge of CLK to indicate the end of a bus cycle (see Figure 3–2). The PAL uses the S0~–S2~ lines to synthesize an output signal, STATUS, which allows the CSM to decode the cycles correctly. STATUS is only valid in MAX mode, and is sensed by the MIN/MAX~ line from the 8086/8088.

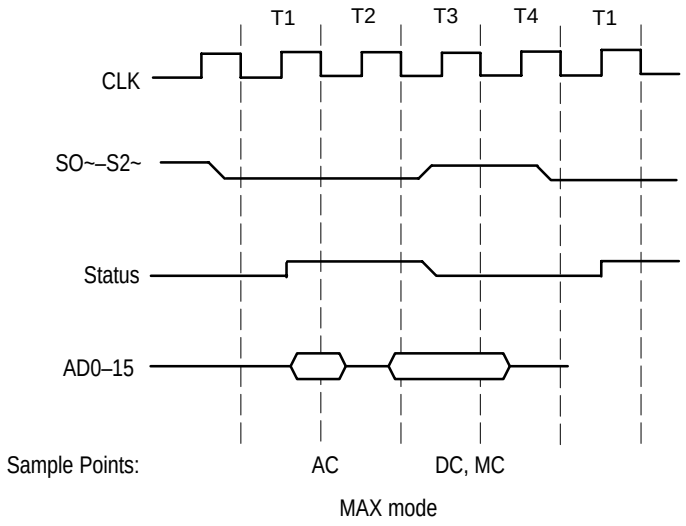


Figure 3–2: 8086/8088 Clocking in MAX Mode

- In MIN mode, the ALE line is latched on the rising edge of CLK. (See Figure 3–3.) This keeps it valid so the falling edge of CLK, which is used in the CSM, can read it and log in the address. This signal is ALE_L. A second signal, EOC_D, is generated by logically ORing the RD~, WR~, and INTA~ signals.

Figure 3–3 also shows when the various sample points are asserted. Sample points DC and MC occur at the end of a bus cycle, the only time the data is valid.

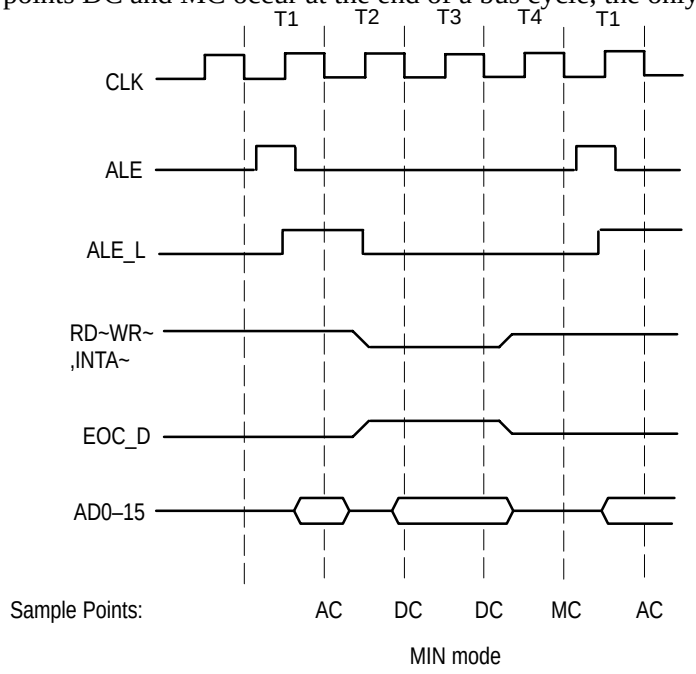


Figure 3–3: 8086/8088 Clocking in MIN Mode

Another signal generated by the PAL, HLDA_D, is also used differently depending on the mode. In MIN mode, HLDA passes straight through to the HLDA_D output. In MAX mode, HLDA is derived by tracking the pulses on the RQ~/GT0~ and RQ~/GT1~ lines.

DMA Cycles. DMA cycles may be observed only as seen by the 8086/8088 microprocessor. System buffering of the address, data, and control lines must be organized so they point to the 8086/8088, and enabled so the DMA cycles are visible to the probe adapter at the 8086/8088 socket. You may need to modify the SUT to meet these requirements if you want to monitor DMA cycles.

When DMA cycles are included, the HLDA signal is given special attention, and DMA cycles are distinguished from other ordinary 8086/8088 cycles. DMA cycles are included along with other 8086/8088-initiated cycles if the 8086/8088 bus transfer protocol is followed and if the SUT bus buffering topology provides adequate data visibility at the 8086/8088 socket. If these conditions are not met, a special sample is forced to record a transfer of bus mastership.

When DMA cycles are excluded, the CSM goes to an idle state whenever HLDA is asserted. The CSM does not log or store data while in this state, and remains in this state until HLDA is negated. Once HLDA is negated, the CSM resumes normal logging and data storage.

Clocking Options

The clocking algorithm for the 8086/8088 support has two variations: DMA Cycles Excluded and DMA Cycles Included.

Alternate Microprocessor Connections

You can connect to microprocessor signals that are not required by the support so that you can do more advanced timing analysis. These signals might or might not be accessible on the probe adapter board. The following paragraphs and tables list signals that are or are not accessible on the probe adapter board.

For a list of signals required or not required for disassembly, refer to the channel assignment tables beginning on page 3–5. Remember that these channels are already included in a channel group. If you do connect these channels to other signals, you should set up another channel group for them.

Signals On the Probe Adapter

All 8086/8088 microprocessor signals are accessible on the probe adapter. In addition to the 8086/8088 socket, all 8086/8088 signals are also routed to a 40-pin square pin header (J900). This is provided so you can connect to soldered in 8086/8088 microprocessors (using optional cable) or to extra podlets. These signals can be useful for general purpose analysis. Remember that all signals are already assigned to channel groups and cannot be assigned to another channel group.

Table 3–9 shows the microprocessor signals available on J900 of the probe adapter.

Table 3–9: 8086/8088 signals on J900

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	GND	15	AD8	28	S1~_DIR~
2	+5V	16	MIN_MAX~	29	AD1
3	AD14	17	AD7	30	S0~_DIR~
4	AD15	18	RD~	31	AD0
5	AD13	19	AD6	32	QS0_ALE
6	A16_S3	20	RQ0_HOLD	33	NMI
7	AD12	21	AD5	34	QS1_INTA~
8	A17_S4	22	RQ1_HLDA	35	INTR

Table 3–9: 8086/8088 signals on J900 (cont.)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
9	AD11	23	AD4	36	TEST~
10	A18_S5	24	LOCK~_WR~	37	CLK
11	AD10	25	AD3	38	READY
12	A19_S6	26	RS _MIO~	39	GND
13	AD9	27	AD2	40	RESET
14	BHE~_S7				

Extra Channels

Table 3–10 lists extra sections and channels that are left after you have connected all the probes used by the support. You can use these extra channels to make alternate SUT connections.

Table 3–10: Extra module sections and channels

Module	Section: channels
102-channels	C1:7-0, C0:7-0, D3:7-0, D2:7-0, Qual:1, Qual:0
136-channels	C1:7-0, C0:7-0, D3:7-0, D2:7-0, E3:7-0, E2:7-0, E1:7-0, E0:7-0, Qual:3-0
96-channels	C1:7-0, C0:7-0, D3:7-0, D2:7-0

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Maintenance

Maintenance

This section contains information on the following topics:

- Probe adapter circuit description

Probe Adapter Circuit Description

The TMS 101 uses a 22V10C PAL to decode the status lines and determine the sample points for the disassembler. How signals are decoded depends on whether the processor is in MIN or MAX mode.

In MAX mode, the status lines become valid after the rising edge of the CLK, and become invalid after the falling edge of the CLK (which indicates the end of a bus cycle). The PAL synthesizes an output signal called STATUS which allows the Clock State Machine (CSM) to decode the cycles correctly. STATUS is only valid in MAX mode, and is sensed by the MIN/MAX~ line from the 8086/88.

In MIN mode, the ALE line is latched on the rising edge of CLK to form a signal called ALE_L. This ensures that it will remain valid during the falling edge of CLK so that the CSM can recognize it and log in the address bits. EOC_D identifies the end of the cycle and logs the data. The EOC_D signal is generated by logically ORing the RD~, WR~, and INTA~ signals.

The HLDA_D signal, also generated by the PAL, is used differently depending on the mode. In MIN mode, this signal is passed straight through to become HLDA_D. In MAX mode, HLDA_D is generated by tracking the pulses on the RQ/GT0~ and RQ/GT1~ lines.

Replacing Signal Leads

Information on basic operations describes how to replace signal leads (individual channel and clock probes).

Replacing Protective Sockets

Information on basic operations describes how to replace protective sockets.

Replacing the Fuse

There is a fuse on the 40-pin dip clip. Refer to the Replaceable Electrical Part list for ordering information.

Replaceable Electrical Parts

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 101 8086/8088 microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

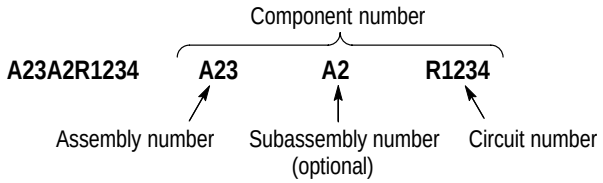
Parts list column descriptions

Column	Column name	Description
1	Component number	The component number appears on diagrams and circuit board illustrations, located in the diagrams section. Assembly numbers are clearly marked on each diagram and circuit board illustration in the *Diagrams* section, and on the mechanical exploded views in the *Replaceable Mechanical Parts* list section. The component number is obtained by adding the assembly number prefix to the circuit number (see Component Number illustration following this table). The electrical parts list is arranged by assemblies in numerical sequence (A1, with its subassemblies and parts, precedes A2, with its subassemblies and parts). Chassis-mounted parts have no assembly number prefix, and they are located at the end of the electrical parts list.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
6	Mfr. code	This indicates the code number of the actual manufacturer of the part.
7	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Component Number



Read: Resistor 1234 (of Subassembly 2) of Assembly 23

List of Assemblies

A list of assemblies is located at the beginning of the electrical parts list. The assemblies are listed in numerical order. When a part's complete component number is known, this list will identify the assembly in which the part is located.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
04222	AVX CERAMICS DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
TK0875	MATSUO ELECTRONICS INC	831 S DOUBLAS ST	EL SEGUNDO CA 92641
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A1	671–2444–00			CIRCUIT BD ASSY:8086/88 DIP40 SOCKETED, PROBE ADAPTER(LASI III);	80009	671244400
A1C340	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	04222	12063C104KAT3A
A1C630	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	04222	12063C104KAT3A
A1C650	290–5005–00			CAP,FXD,TANT:47UF,10%,10V,SMD,T&R	TK0875	267M–1002–476–K
A1F800	—— ——			FUSE, WIRE LEAD, 3.0A, 125V, 5 SECONDS, (See Replaceable Mechanical Part List)		
A1J190	—— ——			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (See Replaceable Mechanical Parts List)		
A1J330	—— ——			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (See MPL)		
A1J390	—— ——			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (See Replaceable Mechanical Parts List)		
A1J890	—— ——			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (See Replaceable Mechanical Parts List)		
A1J900	—— ——			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (See Replaceable Mechanical Parts List)		
A1U360	160–8963–00			IC,DIGITAL:CMOS,PLD;PAL,22V10,10NS,180MA STATUS B DMA	80009	160–8963–00
A1U600	—— ——			SOCKET,DIP:PCB,;FEMALE,STR,2 X 20,0.1 X 0.6 AME (See Replaceable Mechanical Parts List)		

Replaceable Mechanical Parts

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 101 8086/8088 microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
53387	MINNESOTA MINING MFG CO	PO BOX 2963	AUSTIN TX 78769–2963
63058	MCKENZIE TECHNOLOGY	44370 OLD WARMS SPRINGS BLVD	FREMONT CA 94538
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
1–0	010–0547–00			1	PROBE ADAPTER: 8086/88, DIP40 SOCKETED	80009	010054700
–1	131–5267–00			2	CONN, HDR:PCB, MALE, STR, 2 X 40, 0.1 CTR, 0.235 MLG X 0.110 TAIL,30GOLD (J190,J330,J390,J890,J900)	80009	131526700
–2	671–2444–00			1	CIRCUIT BD ASSY: 8086/88 DIP40 SOCKETED, PROBE ADAPTER (LASI III);	80009	671244400
–3	136–0916–00			2	SOCKET, DIP: PCB, FEMALE, STR, 2 X 20, 0.1 X 0.6 CTR, 0.173 H X 0.183 TAIL, GOLD, OPEN FRAME (U600)	63058	DIP–640–101B
					STANDARD ACCESSORIES		
	070–9804–00			1	MANUAL, TECH: INSTRUCTION, 8086/8088, DISSASEMBLER, TMS 101	80009	070–9804–00
	070–9803–00			1	MANUAL, TECH: TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070–9803–00
					OPTIONAL ACCESSORIES		
–4	015–0646–00			1	TEST CLIP ASSY: RIBBON, 40, 28 AWG, 4.0 L, 40 POS DIP CLIP X 2X20 0.1 CTR RCPT W/CTR PLZ	53387	015–0646–00
	159–0204–00			1	FUSE, WIRE LEAD 3.0A, 125V, 5 SECONDS (F800)	61857	ORDER BY DESC
	070–9802–00			1	MANUAL, TECH: BASIC OPS MICRO SUPPORT ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070–9802–00

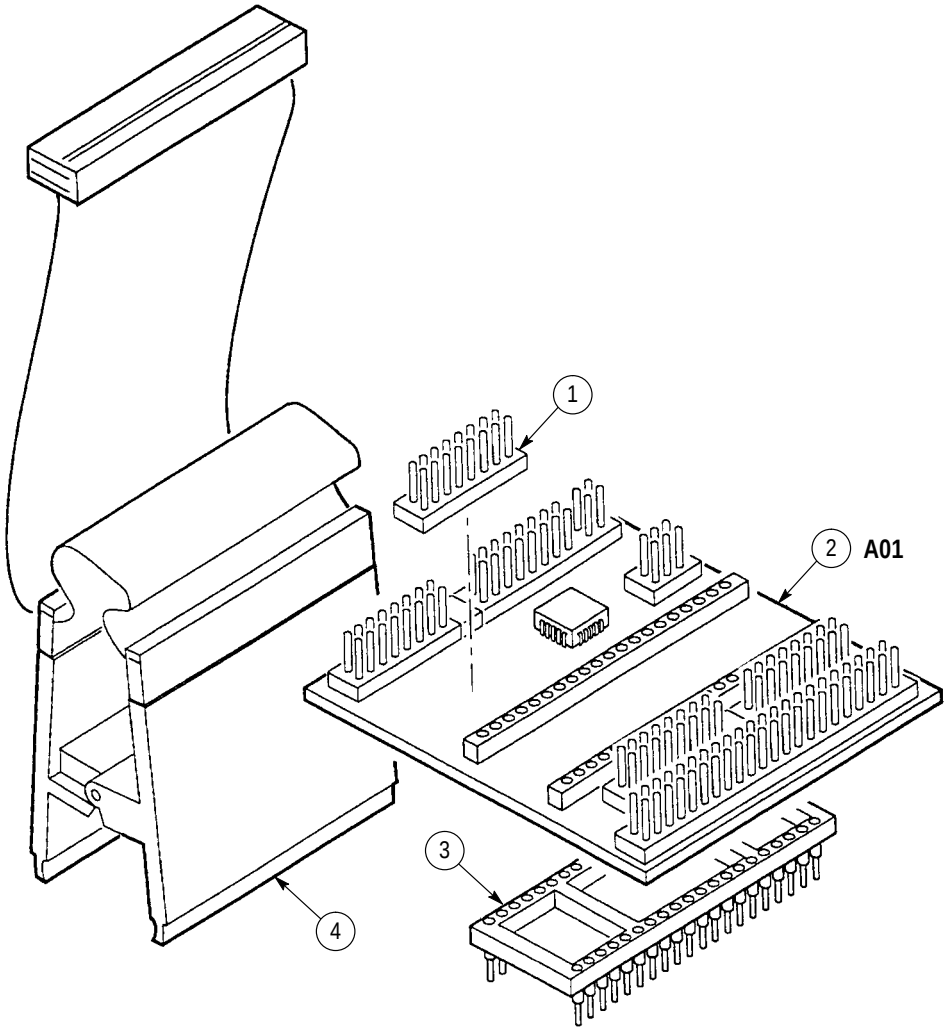


Figure 1: 8086/8088 probe adapter exploded view

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