Instruction Manual

Tektronix

TMS 103
80286 Microprocessor Support

070-9806-00

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it.

To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

Injury Precautions

Avoid Electric Overload. To avoid electric shock or fire hazard, do not apply a voltage to a terminal that is outside the range specified for that terminal.

Avoid Electric Shock. To avoid injury or loss of life, do not connect or disconnect probes or test leads while they are connected to a voltage source.

Do Not Operate Without Covers. To avoid electric shock or fire hazard, do not operate this product with covers or panels removed.

Do Not Operate in Wet/Damp Conditions. To avoid electric shock, do not operate this product in wet or damp conditions.

Do Not Operate in an Explosive Atmosphere. To avoid injury or fire hazard, do not operate this product in an explosive atmosphere.

Avoid Exposed Circuitry. To avoid injury, remove jewelry such as rings, watches, and other metallic objects. Do not touch exposed connections and components when power is present.

Product Damage Precautions

Provide Proper Ventilation. To prevent product overheating, provide proper ventilation.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

DANGER
High Voltage

Protective Ground
(Earth) Terminal

ATTENTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface: Microprocessor Support Documentation

This instruction manual contains specific information about the TMS 103 80286 microprocessor support and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor supports on the logic analyzer for which the TMS 103 80286 support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor supports, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor supports is included with each product. Each logic analyzer has basic information that describes how to perform tasks common to supports on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing disassembled data
- The TMS 103 80286 probe adapter

Manual Conventions

This manual uses the following conventions:

- The term disassembler refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to online help, an installation manual, or a basic operations of microprocessor supports user manual.
- The term System Under Test (SUT) refers to the microprocessor-based system from which data will be acquired.
- The term logic analyzer refers to the Tektronix logic analyzer for which this product was purchased.

- The term module refers to a 102-channel, 96-channel, or module. Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the channel requirements for this support.
- The term XXX or 68340 used in field selections and file names in the information on basic operations can be replaced with 286. This is the name of the microprocessor in field selections and file names you must use to operate the support.
- 286 refers to all supported variations of the 80286 microprocessor unless otherwise noted.
- A tilde (~) following a signal name indicates an active low signal.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The user manual provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or, contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Contact your local Tektronix distributor or sales office. Or, visit our web site for a listing of worldwide service locations. http://www.tek.com
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000

Getting Started

Getting Started

This chapter provides information on the following topics:

- The TMS 103 80286 microprocessor support
- Logic analyzer software compatibility
- Your 80286 system requirements
- 80286 support restrictions
- How to configure the probe adapter
- How to connect to the System Under Test (SUT)

Support Description

The TMS 103 microprocessor support disassembles data from systems that are based on the Intel 80286 microprocessor. The support runs on a compatible Tektronix logic analyzer equipped with a 102-channel module, or a 96-channel module.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 103 microprocessor support.

Table 1–1 shows the microprocessors and packages from which the TMS 103 support can acquire and disassemble data.

Table 1–1: Supported microprocessors

Microprocessor	Package
AMD 80286	PGA and PLCC
Harris 80286	PGA and PLCC
Intel 80286	PGA, PLCC and LCC
Siemens 80286	PGA, PLCC and LCC

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Mechanical Parts* chapter.

To use this support efficiently, you need to have the items listed in the information on basic operations as well as the *80286 Microprocessor User's Manual*, Intel.

Information on basic operations also contains a general description of supports.

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

To use the 80286 support, the Tektronix logic analyzer must be equipped with at least a 102-channel module, a 96-channel module. The module must be equipped with enough probes to acquire channel and clock data from signals in your 80286-based system.

Refer to information on basic operations to determine how many modules and probes the logic analyzer needs to meet the channel requirements.

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor supports in the information on basic operations as they pertain to your SUT.

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other 80286 support requirements and restrictions.

System Clock Rate. The microprocessor support product supports the 80286 microprocessor at speeds shown in Table 1–2, with a maximum speed of 25 MHz[1].

Table 1–2: Microprocessor Speed Supported

Microprocessor	Package	Speed Supported
AMD 80286	PGA PLCC LCC	12 MHz 16/20 MHz 16/20 MHz
Harris 80286	PGA PLCC	20 MHz 25 MHz

1 **Specification at time of printing. Contact your logic analyzer sales representative for current information on the fastest devices supported.**

Table 1–2: Microprocessor Speed Supported (cont.)

Microprocessor	Package	Speed Supported
Intel 80286	PGA, PLCC and LCC	12.5 MHz
Siemens 80286	PGA, PLCC and LCC	10 MHz

SUT Power. Whenever the SUT is powered off, be sure to remove power from the probe adapter. Refer to *Applying and Removing Power* at the end of this chapter for information on how to remove power from the probe adapter.

Configuring the Probe Adapter

The probe adapter does not require any configuration.

Connecting to a System Under Test

Before you connect to the SUT, you must connect the probes to the module. Your SUT must also have a minimum amount of clear space surrounding the microprocessor to accommodate the probe adapter. Refer to the *Specifications* chapter in this manual for the required clearances.

The channel and clock probes shown in this chapter are for a 102-channel module. Your probes will look different if you are using a 96-channel module.

The general requirements and restrictions of microprocessor supports in the information on basic operations shows the vertical dimensions of a channel or clock probe connected to square pins on a circuit board.

PGA Probe Adapter

To connect the logic analyzer to a SUT using a PGA probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probe adapter, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.
3. Place the probe adapter onto the antistatic shipping foam to support the probe as shown in Figure 1–1. This prevents the circuit board from flexing and the socket pins from bending.
4. Remove the microprocessor from your SUT.
5. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on the microprocessor.

CAUTION. *Failure to correctly place the microprocessor into the probe adapter might permanently damage the microprocessor once power is applied.*

6. Place the microprocessor into the probe adapter as shown in Figure 1–1.

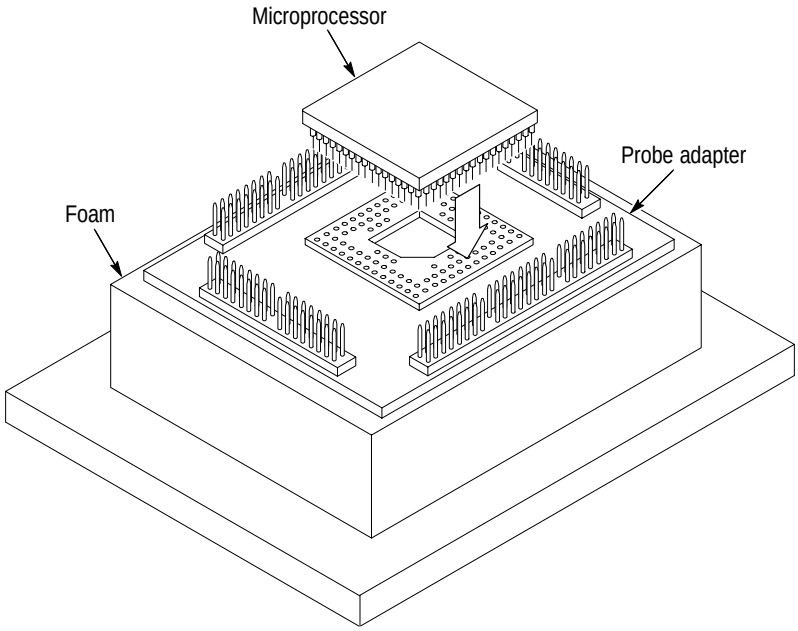


Figure 1–1: Placing a microprocessor into a PGA probe adapter

7. Connect the channel and clock probes to the probe adapter as shown in Figure 1–2. Match the channel groups and numbers on the probe labels to the corresponding pins on the probe adapter. Match the ground pins on the probes to the corresponding pins on the probe adapter.

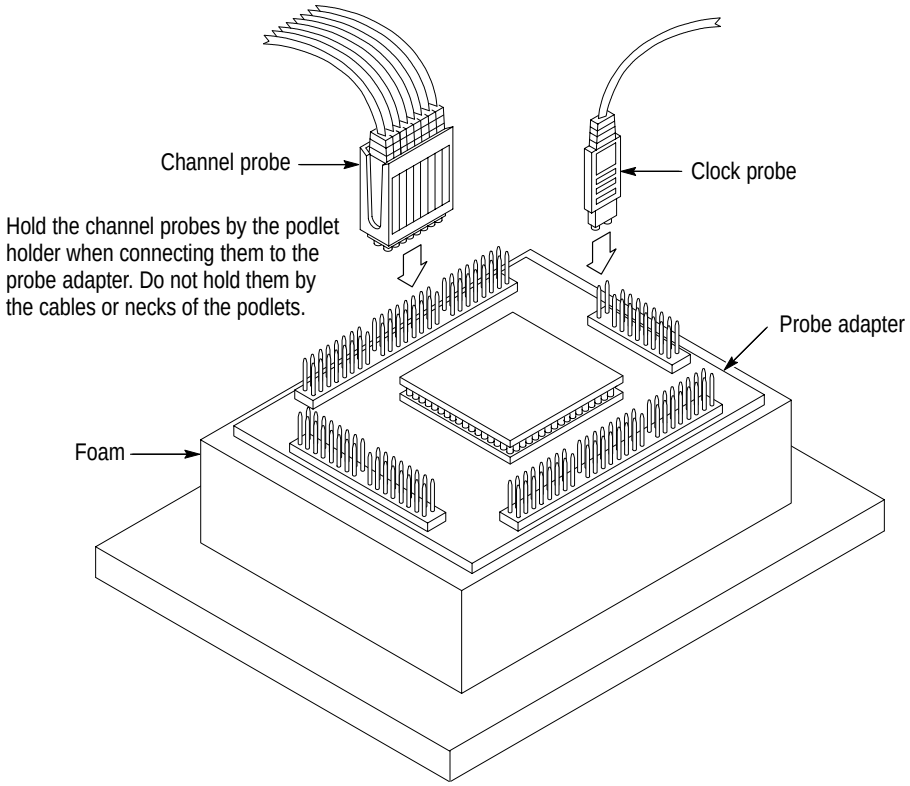


Figure 1–2: Connecting probes to a PGA probe adapter

8. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on your SUT.

9. Place the probe adapter onto the SUT as shown in Figure 1–3.

NOTE. *You might need to stack one or more replacement sockets between the SUT and the probe adapter to provide sufficient vertical clearance from adjacent components. However, keep in mind that this might increase loading, which can reduce the electrical performance of your probe adapter.*

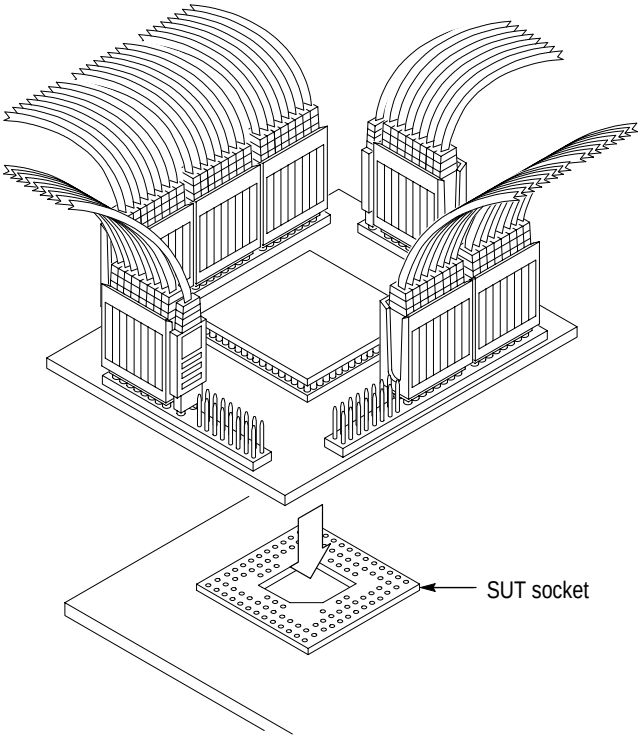


Figure 1–3: Placing a PGA probe adapter onto the SUT

PLCC Probe Adapter

To connect the logic analyzer to a SUT using a PLCC probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probe adapter, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.
3. Place the probe adapter onto the antistatic shipping foam to support the probe as shown in Figure 1–4. This prevents the circuit board from flexing.
4. Remove the microprocessor from your SUT.

5. Line up the pin 1 indicator on the microprocessor with pin 1 of the PLCC socket on the probe adapter.

CAUTION. *Failure to correctly place the microprocessor into the probe adapter might permanently damage all electrical components once power is applied.*

6. Place the microprocessor into the probe adapter as shown in Figure 1–4.

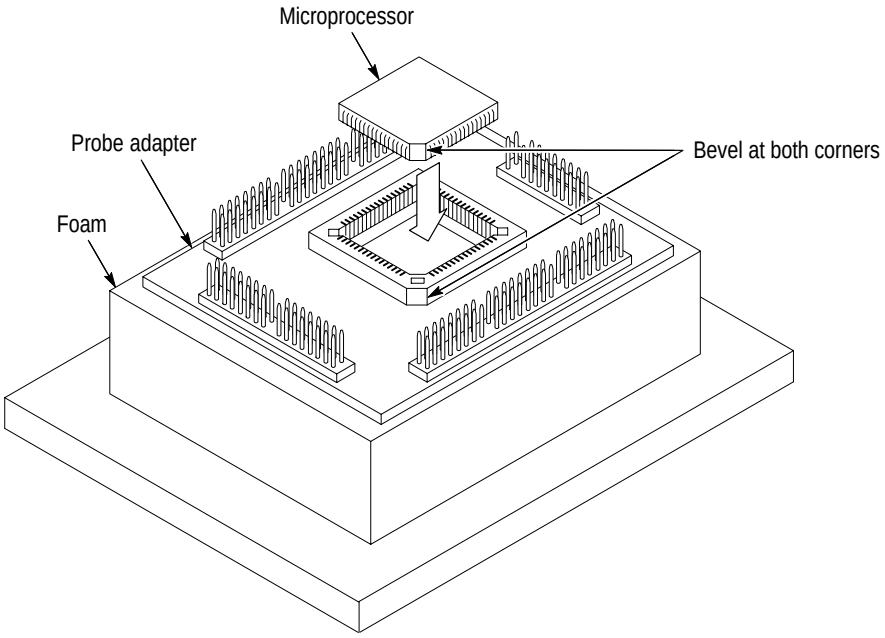


Figure 1–4: Placing a microprocessor into a PLCC probe adapter

7. Connect the channel and clock probes to the probe adapter as shown in Figure 1–5. Match the channel groups and numbers on the probe labels to the corresponding pins on the probe adapter. Match the ground pins on the probes to the corresponding pins on the probe adapter.

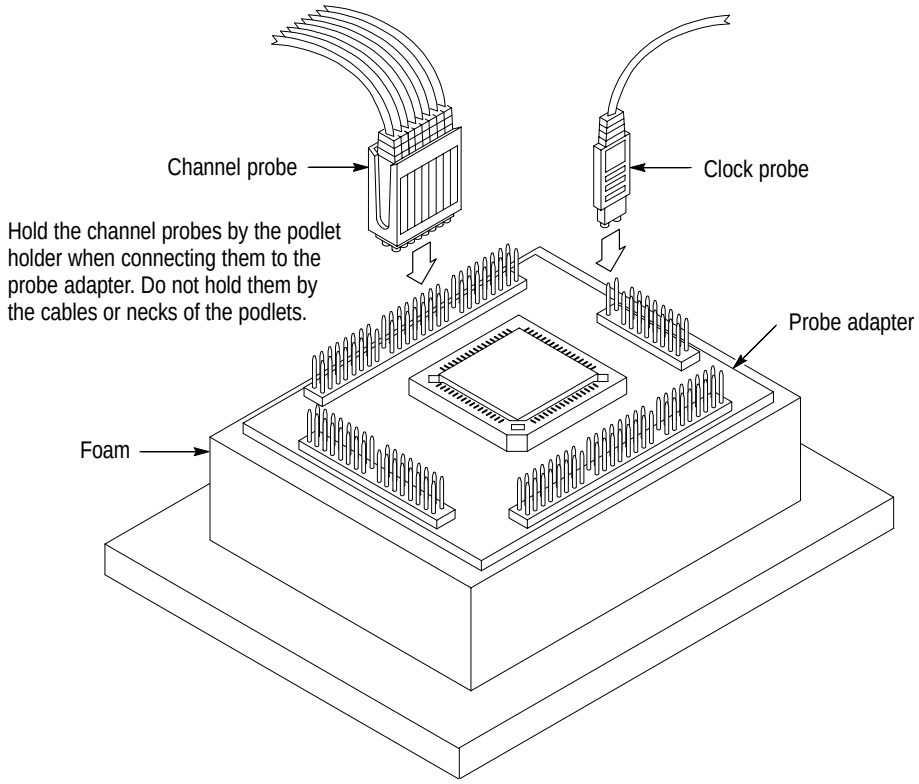


Figure 1–5: Connecting probes to a PLCC probe adapter

8. Place the probe adapter onto the SUT as shown in Figure 1–6.

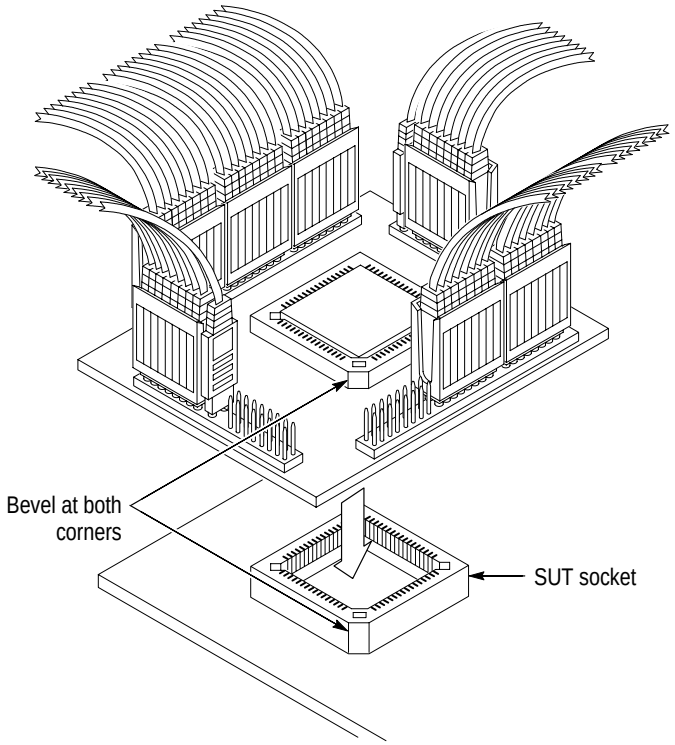


Figure 1–6: Placing a PLCC probe adapter onto the SUT

Without a Probe Adapter

You can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your SUT.

To connect the probes to 80286 signals in the SUT using a test clip, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from it.

CAUTION. *Failure to place the SUT on a horizontal surface before connecting the test clip might permanently damage the pins on the microprocessor.*

3. Place the SUT on a horizontal static-free surface.

4. Use Table 1–3 to connect the channel probes to 80286 signal pins on the test clip or in the SUT.

   Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip.

Table 1–3: 80286 signal connections for channel probes

Section:channel	80286 signal	Section:channel	80286 signal
A3:7	COD/INTA~	D3:7	
A3:6	HLDA	D3:6	
A3:5	READY~*	D3:5	
A3:4	M/IO~	D3:4	
A3:3	PEREQ*	D3:3	
A3:2	HOLD*	D3:2	
A3:1	NMI*	D3:1	
A3:0	INTR*	D3:0	
A2:7	A23	D2:7	
A2:6	A22	D2:6	
A2:5	A21	D2:5	
A2:4	A20	D2:4	
A2:3	A19	D2:3	
A2:2	A18	D2:2	
A2:1	A17	D2:1	
A2:0	A16	D2:0	
A1:7	A15	D1:7	D15
A1:6	A14	D1:6	D14
A1:5	A13	D1:5	D13
A1:4	A12	D1:4	D12
A1:3	A11	D1:3	D11

Table 1–3: 80286 signal connections for channel probes (cont.)

Section:channel	80286 signal	Section:channel	80286 signal
A1:2	A10	D1:2	D10
A1:1	A9	D1:1	D9
A1:0	A8	D1:0	D8
A0:7	A7	D0:7	D7
A0:6	A6	D0:6	D6
A0:5	A5	D0:5	D5
A0:4	A4	D0:4	D4
A0:3	A3	D0:3	D3
A0:2	A2	D0:2	D2
A0:1	A1	D0:1	D1
A0:0	A0	D0:0	D0
C3:7	BUSY~*	C2:7	BHE~
C3:6	ERROR~*	C2:6	LOCK~
C3:5	RESET*	C2:5	PEACK~
C3:4		C2:4	CLK_B*
C3:3		C2:3	S1~
C3:2		C2:2	S0~
C3:1		C2:1	READY_L~
C3:0		C2:0	HLDA_L

*** Signal not required for disassembly.**

Table 1–4 shows the clock probes, and the 80286 signal to which they must connect for disassembly to be correct.

Table 1–4: 80286 signal connections for clock probes

Section:channel	80286 signal
CK:2	M/IO_L~*
CK:1	COD/INTA_L~*
CK:0	CLK

*** These channels are used as qualifiers**

5. Align pin 1 or A1 of your test clip with the corresponding pin 1 or A1 of the 80286 microprocessor in your SUT and attach the clip to the microprocessor.
6. Use the channel assignment tables in the *Specifications* chapter to connect channel and clock probes to your test clip.
7. Use the channel assignment tables in the *Specifications* chapter to connect channel and clock probes to the module probe cables.
8. You must connect at least one ground podlet (lead) from each channel probe and the ground from each clock probe to ground pins on your test clip.
9. Align pin 1 or A1 of your test clip with the corresponding pin 1 or A1 of the microprocessor in your SUT and attach it to the microprocessor.

Operating Basics

Setting Up the Support

This section provides information on how to set up the support. Information covers the following topics:

- Channel group definitions
- Clocking options
- Symbol table files

Remember that the information in this section is specific to the operations and functions of the TMS 103 80286 support on any Tektronix logic analyzer for which it can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and disassemble data, you need to load the support and specify setups for clocking, and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the 80286 support are Address, Data, Control, Intr, Copr and Misc. If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 3–5.

Clocking Options

The TMS 103 support offers a microprocessor-specific clocking mode for the 80286 microprocessor. This clocking mode is the default selection whenever you select the 286 support.

(For the 102-channel module, from the File menu, select Load Support Package, and 286. For the 96-channel module, select 286 Support in the Configuration menu.)

The clocking options for the TMS 103 support is DMA Cycles.

A description of how cycles are sampled by the module using the support and probe adapter is found in the *Specifications* chapter.

For the 102-channel module, disassembly will not be correct with any type of Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

For the 96-channel module, disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

DMA Cycles

A DMA cycle is defined as the 80286 giving up the bus to an alternate device (a DMA device or another microprocessor). All bus cycles, including visible DMA cycles, are acquired when you select Included.

Symbols

The TMS 103 support supplies one symbol table file. The 286_Ctrl file replaces specific Control channel group values with symbolic values when Symbolic is the radix for the channel group.

Table 2–1 shows the name, bit pattern, and meaning for the symbols in the file 286_Ctrl, the Control group symbol table.

Table 2–1: Control Group Symbol Table Definitions

Symbol	Control Group Value PEACK~ HLDA COD/INTA~ M/IO~ S1~ S0~ LOCK~ BHE~	Meaning
FETCH	X 0 1 1 0 1 X X	Memory code read that may be flushed (an Opcode Fetch)
INT_ACK	X 0 0 0 0 0 X X	Responding to an interrupt
I/O_READ	X 0 1 0 0 1 1 X	A read from an I/O port
I/O_WRITE	X 0 1 0 1 0 1 X	A write to an I/O port
HALT/SHUT	X 0 0 1 0 0 X X	Enter the HALT or SHUTDOWN state
MEM_READ	X 0 0 1 0 1 1 X	A memory read cycle (not an Opcode Fetch)
MEM_WRITE	X 0 0 1 1 0 1 X	A memory write cycle
DMA_M_R	X 1 X 1 0 1 X X	A direct memory access read from memory space
DMA_M_W	X 1 X 1 1 0 X X	A direct memory access write to memory space
DMA	X 1 X X X X X X	Any direct memory access
LKD_M_RD	X 0 0 1 0 1 0 X	A locked data read from memory (not an Opcode Fetch)

Table 2–1: Control Group Symbol Table Definitions (cont.)

Symbol	Control Group Value PEACK~ HLDA COD/INTA~ M/IO~ S1~ S0~ LOCK~ BHE~	Meaning
LKD_M_WR	X 0 0 1 1 0 0 X	A locked data write to memory
LKD_IO_RD	X 0 1 0 0 1 0 X	A locked data read from an I/O port
LKD_IO_WR	X 0 1 0 1 0 0 X	A locked data write to an I/O port
READ*	X X X X 0 1 X X	A read cycle
WRITE*	X X X X 1 0 X X	A write cycle
LOCKED*	X X X X X X 0 X	A locked bus operation

* **Symbols used only for triggering; they do not appear in the Disassembly or State displays.**

Information on basic operations describes how to use symbolic values for triggering, and displaying other channel groups symbolically, such as the Address channel group.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. Information covers the following topics:

- Acquiring data
- Viewing disassembled data in various display formats
- Cycle type labels
- How to change the way data is displayed
- How to change disassembled cycles with the mark cycles function

Acquiring Data

Once you load the 80286 support, choose a clocking mode and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual, whichever is available.

Viewing Disassembled Data

You can view disassembled data in four different display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE. *Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–9.*

The default display format shows the Address, Data, and Control channel group values for each sample of acquired data.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–2 shows the special characters and strings displayed by the 80286 disassembler and gives a definition of what they represent.

Table 2–2: Special characters in the display and meaning

Character or string displayed	Meaning
m	The instruction was manually marked as a program fetch
****	Indicates there is insufficient data available for complete disassembly of the instruction; the number of asterisks will indicate the width of the data that is unavailable. Each two asterisks represent a byte.
#	Indicates an immediate value
t	Indicates the number shown is in decimal, such as #12t
* ILLEGAL INSTRUCTION *	Decoded as an illegal instruction
A-LINE OPCODE	Displayed for an A-Line trap instruction
F-LINE OPCODE	Displayed for an F-Line trap instruction

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–3 shows these cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled with the vector name.

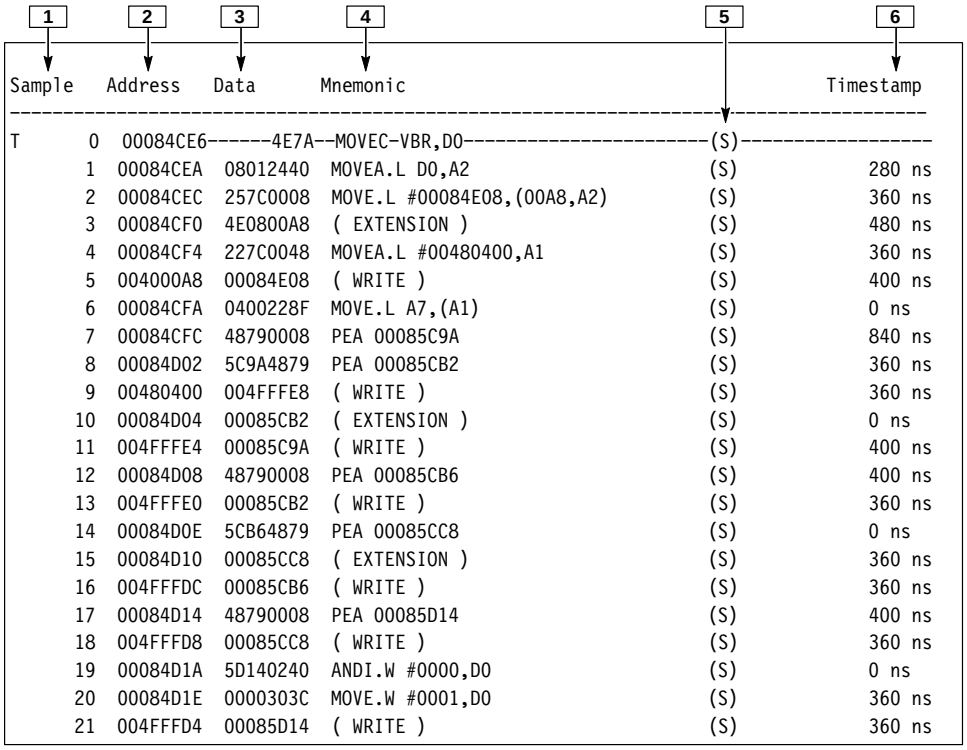
Table 2–3: Cycle Type Definitions

Cycle type	Definition
(COP I/O READ)	A coprocessor data read from an I/O port (a computed cycle type)
(COP I/O WRITE)	A coprocessor data write to an I/O port (a computed cycle type)
(COP MEM READ)	Data read from memory done by Processor for coprocessor (a computed cycle type)
(COP MEM WRITE)	Data write to memory done by Processor for coprocessor (a computed cycle type)
(DMA READ)	A direct memory read cycle
(DMA WRITE)	A direct memory access write cycle
(FLUSH)	A fetch cycle computed to be an opcode flush; the fetched cycle was not executed (a computed cycle type)
(HALT)	A microprocessor halt cycle (a computed cycle type)
(SHUTDOWN)	A microprocessor shutdown cycle (a computed cycle type)
(UNKNOWN)	An unknown cycle type
(INT ACK)	An interrupt acknowledge cycle

Table 2–3: Cycle Type Definitions (cont.)

Cycle type	Definition
(I/O READ)	A read from an I/O port
(I/O WRITE)	A write to an I/O port
(MEM READ)	A read from memory that is not an opcode fetch
(MEM WRITE)	Any write to memory
(LOCKED I/O READ)	A locked data read from an I/O port
(LOCKED I/O WRITE)	A locked data write to an I/O port
(LOCKED MEM READ)	A locked data read from memory
(LOCKED MEM WRITE)	A locked data write to memory
(EXTENSION)	A word read from program space to complete opcode fetch sequence (a computed cycle type)
* ILLEGAL INSTRUCTION *	An illegal cycle; an unrecognized combination of control channel values. This may indicate a faulty connection or a defective probe adaptor, a setup that was modified from the original one created by 92DM08A, a problem with your prototype or a cycle reserved for Intel's use

Figure 2–1 shows an example of the Hardware display.




```
T       0  00084CE6------4E7A--MOVEC-VBR,D0----------------------(S)------------------
        1  00084CEA  08012440  MOVEA.L D0,A2                     (S)           280 ns
        2  00084CEC  257C0008  MOVE.L #00084E08,(00A8,A2)        (S)           360 ns
        3  00084CF0  4E0800A8  ( EXTENSION )                     (S)           480 ns
        4  00084CF4  227C0048  MOVEA.L #00480400,A1              (S)           360 ns
        5  004000A8  00084E08  ( WRITE )                         (S)           400 ns
        6  00084CFA  0400228F  MOVE.L A7,(A1)                    (S)           0 ns
        7  00084CFC  48790008  PEA 00085C9A                      (S)           840 ns
        8  00084D02  5C9A4879  PEA 00085CB2                      (S)           360 ns
        9  00480400  004FFFE8  ( WRITE )                         (S)           360 ns
       10  00084D04  00085CB2  ( EXTENSION )                     (S)           0 ns
       11  004FFFE4  00085C9A  ( WRITE )                         (S)           400 ns
       12  00084D08  48790008  PEA 00085CB6                      (S)           400 ns
       13  004FFFE0  00085CB2  ( WRITE )                         (S)           360 ns
       14  00084D0E  5CB64879  PEA 00085CC8                      (S)           0 ns
       15  00084D10  00085CC8  ( EXTENSION )                     (S)           360 ns
       16  004FFFDC  00085CB6  ( WRITE )                         (S)           360 ns
       17  00084D14  48790008  PEA 00085D14                      (S)           400 ns
       18  004FFFD8  00085CC8  ( WRITE )                         (S)           360 ns
       19  00084D1A  5D140240  ANDI.W #0000,D0                   (S)           0 ns
       20  00084D1E  0000303C  MOVE.W #0001,D0                   (S)           360 ns
       21  004FFFD4  00085D14  ( WRITE )                         (S)           360 ns
```

Figure 2–1: Hardware display format

1 **Sample Column.** Lists the memory locations for the acquired data.

2 **Address Group.** Lists data from channels connected to the 80286 Address bus.

3 **Data Group.** Lists data from channels connected to the 80286 Data bus.

4 **Mnemonic Column.** Lists the disassembled instructions and cycle types.

5 The disassembler displays an (S) or (U) in the mnemonic column to indicate the mode in which the microprocessor is operating, S for Supervisor, or U for User.

6 **Timestamp.** Lists the timestamp values when a timestamp selection is made. Information on basic operations describes how you can select a timestamp.

Software Display Format

The Software display format shows only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Read extensions will be used to disassemble the instruction, but will not be displayed as a separate cycle in the Software display format. Data reads and writes are not displayed.

Control Flow Display Format

The Control Flow display format shows only the first fetch of instructions that change the flow of control.

Instructions that generate a change in the flow of control in the 80286 microprocessor are as follows:

BOUND	JLE	JO
CALL	JMP	JP
INT3	JNB	JS
INTO	JNBE	LOOP
INTx	JNE	LOOPE
IRET	JNL	LOOPNE
JB	JNLE	LOOPNZ
JCXZ	JNO	LOOPZ
JE	JNP	RET
JL	JNS	

Subroutine Display Format

The Subroutine display format shows only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

Instructions that generate a subroutine call or a return in the 80286 microprocessor are as follows:

BOUND	INTO	IRET
CALL	INTX	RET
INT3		

Changing How Data is Displayed

There are fields and features that allow you to further modify displayed data to suit your needs. You can make selections unique to the 80286 support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception vectors

Optional Display Selections

You can make optional display selections for disassembled data to help you analyze the data. You can make these selections in the Disassembly property page (the Disassembly Format Definition overlay).

In addition to the common display options (described in the information on basic operations), you can change the displayed data in the following ways:

- Choose process mode
- Specify the starting address of the interrupt table
- Specify the size of the interrupt table

The 80286 support has three additional fields: Processor Mode, Interrupt Table Address, and Interrupt Table Size. These fields appear in the area indicated in the information on basic operations.

Processor Mode. You can specify if the mode of operation for the 80286 microprocessor is Real or Protected. The default is Real.

Interrupt Table Address. You can specify the starting address of the interrupt table in hexadecimal. The default starting address is 0x000000.

Interrupt Table Size. You can specify the size of the interrupt table in hexadecimal. The default size is 400.

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it to one of the following cycle types:

- Opcode (the first word of an instruction)
- Extension (a subsequent word of an instruction)
- Flush (an opcode or extension that is fetched but not executed)

Mark selections for an 8-bit acquisitions (single byte fetch) are as follows:

```
Opcode
Extension
Flush
Undo Mark
```

Mark selections for a 16-bit acquisition (double byte fetch) are as follows:

```
Any          Opcode
Opcode       Extension
Opcode       Flush
Flush        Extension
Extension    Extension
Flush        Flush
Undo Mark
```

Table 2–4: Mark selection descriptions

Mark selection	Description
Opcode	The one-byte cycle is disassembled as the beginning of an instruction.
Extension	The one-byte cycle is treated as an extension of the previous instruction.
Flush	The one-byte cycle is not disassembled.
Any Opcode	The low byte of the cycle is disassembled as the beginning of an instruction. The high byte is not marked.
Opcode Extension	The low byte of the cycle is treated as an instruction extension. The high byte is not marked.
Opcode Flush	The low byte of the cycle is not disassembled. The high byte of the cycle is not marked.
Extension Extension	Both the high byte and low byte of the cycle are treated as instruction extensions.
Flush Extension	The high byte of the cycle is not disassembled. The low byte is treated as an instruction extension.
Flush Flush	The cycle is not disassembled.
Undo Mark	Marks are removed from the cycle and the disassembly reverts to the premark state.
Default	Opcode

Information on basic operations contains more details on marking cycles.

Displaying Exception Vectors

The disassembler can display 80286 exception vectors. You can select to display the interrupt vectors for Real or Protected mode in the Processor Mode field.

You can relocate the table by entering the starting address in the Interrupt Table Address field. The Interrupt Table Address field provides the disassembler with the offset address; enter an eight-digit hexadecimal value corresponding to the offset of the base address of the exception table. The Interrupt Table Size field lets you specify a three-digit hexadecimal size for the table.

You can make these selections in the Disassembly property page (the Disassembly Format Definition overlay).

Table 2–5 lists the 80286 exception vectors for the Real Addressing mode.

Table 2–5: 8XC196NP exception vectors for Interrupt Controller Service

Exception number	Location in IV* table (in hexadecimal)	Displayed exception name
0	0000	DIVIDE ERROR
1	0004	DEBUG EXCEPTIONS
2	0008	NMI INTERRUPT
3	000C	BREAKPOINT INTERRUPT
4	0010	INTO DETECTED OVERFLOW
5	0014	BOUND RANGE EXCEEDED
6	0018	INVALID OPCODE
7	001C	COPROCESSOR NOT AVAILABLE
8	0020	INTERESTED TABLE LIMIT TOO SMALL
9-11	0024-002C	RESERVED
12	0030	STACK EXCEPTION
13	0034	SEGMENT OVERRUN
14-15	0038-003C	RESERVED
16	0040	COPROCESSOR MODE
17-31	0044-007C	RESERVED
32-255	0080-03FC	USER DEFINED

*** IV means interrupt vector.**

Table 2–6 lists the 80286 exception vectors for the Protected Addressing mode.

Table 2–6: Exception vectors for Protected Addressing mode

Exception number	Location in IDT* (in hexadecimal)	Displayed exception name
0	0000	DIVIDE ERROR
1	0008	DEBUG EXCEPTIONS
2	0010	NMI INTERRUPT
3	0018	BREAKPOINT INTERRUPT
4	0020	INTO DETECTED OVERFLOW
5	0028	BOUND RANGE EXCEEDED
6	0030	INVALID OPCODE
7	0038	DEVICE NOT AVAILABLE

Table 2–6: Exception vectors for Protected Addressing mode (cont.)

Exception number	Location in IDT* (in hexadecimal)	Displayed exception name
8	0040	DOUBLE FAULT
9	0048	RESERVED
10	0050	INVALID TSS
11	0058	SEGMENT NOT PRESENT
12	0060	STACK EXCEPTION
13	0068	GENERAL PROTECTION
14	0070	PAGE FAULT
15	0078	RESERVED
16	0080	COPROCESSOR MODE
17	0088	ALIGNMENT CHECK
18-31	0090-00F8	RESERVED
32-255	0100-07F8	USER DEFINED

*** IDT means interrupt descriptor table.**

Viewing a System File

A demonstration system file is provided so you can see an example of how your 80286 microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use. You can view the system file without connecting the logic analyzer to your SUT.

Information on basic operations describes how to view the 286 Demonstration System file.

Specifications

Specifications

This chapter contains the following information:

- Probe adapter description
- Specification tables
- Dimensions of the probe adapter
- Channel assignment tables
- Description of how the module acquires 80286 signals
- List of other accessible 80286 signals and extra acquisition channels

Probe Adapter Description

The probe adapter is a nonintrusive piece of hardware that allows the acquisition module to acquire data from a 80286 microprocessor in its own operating environment with little affect, if any, on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and a socket for a 80286 microprocessor. The probe adapter connects to the microprocessor in the SUT. Signals from the microprocessor-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

All circuitry on the probe adapter is powered from the SUT.

The PGA probe adapter accommodates the 80286 microprocessor in a 68-pin PGA package. The PLCC probe adapter accommodates the 80286 microprocessor in a 68-pin PLCC package.

Configuration

The probe adapter does not require any configuration.

Specifications

These specifications are for a probe adapter connected to a compatible Tektronix logic analyzer, and the SUT. Table 3–1 shows the electrical requirements the SUT must produce for the support to acquire correct data.

In Table 3–1, for the 102/136-module, one podlet load is 20 kΩ in parallel with 2 pF. For the 96-channel module, one podlet load is 100 kΩ in parallel with10 pF. For the 80-channel module, one podlet load is 100 kΩ in parallel with 5 pF.

Table 3–1: Electrical specifications

Characteristics	Requirements	
SUT DC power requirements		
Voltage	4.75-5.25 VDC	
Current	I max (calculated) 210 mA I typ (measured) 140 mA	
SUT clock		
Clock rate	Min. DC Max. 25 MHz	
	Specification	
	Probe Adapter	**80286 @ 25 MHz**
Minimum setup time required		
D15-D0	5 ns	3 ns
READY~	3.5 ns	9 ns
All other signals	5 ns	——
Minimum hold time required		
D15-D0	0 ns	2 ns
READY~	5 ns	3 ns
All other signals	0 ns	——
	Specification	
	AC Load	**DC Load**
Measured typical SUT signal loading		
CLK, READY~, HLDA, M/IO~, COD/INTA~	13 pF + 1 podlet	1 20R6-5 in parallel with 1 podlet
NMI, RESET	10 pF + 1 podlet	1 podlet
A23-A0	6 pF + 1 podlet	1 podlet
D15-D0	5 pF + 1 podlet	1 podlet
All Other Signals	5 pF + 1 podlet	1 podlet

Table 3–2 shows the environmental specifications.

Table 3–2: Environmental specification*

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F)†
Minimum operating	0° C (+32° F)
Non-operating	–55° C to +75° C (–67° to +167° F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

*** Designed to meet Tektronix standard 062-2847-00 class 5.**

† **Not to exceed 80286 microprocessor thermal considerations. Forced air cooling might be required across the CPU.**

Table 3–3 shows the certifications and compliances that apply to the probe adapter.

Table 3–3: Certifications and compliances

There are no applicable directives that apply to this product.

Figure 3–1 shows the dimensions of the PGA probe adapter. Information on basic operations shows the vertical clearance of the channel and clock probes when connected to a probe adapter in the description of general requirements and restrictions.

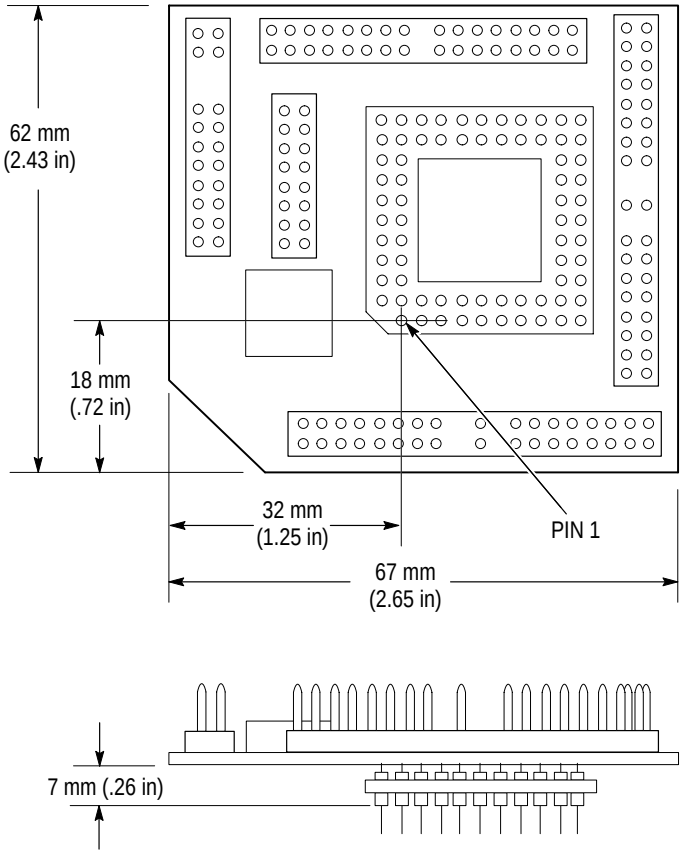


Figure 3–1: Dimensions of the PGA probe adapter

Figure 3–2 shows the dimensions of the PLCC probe adapter. Information on basic operations shows the vertical clearance of the channel and clock probes when connected to a probe adapter in the description of general requirements and restrictions.

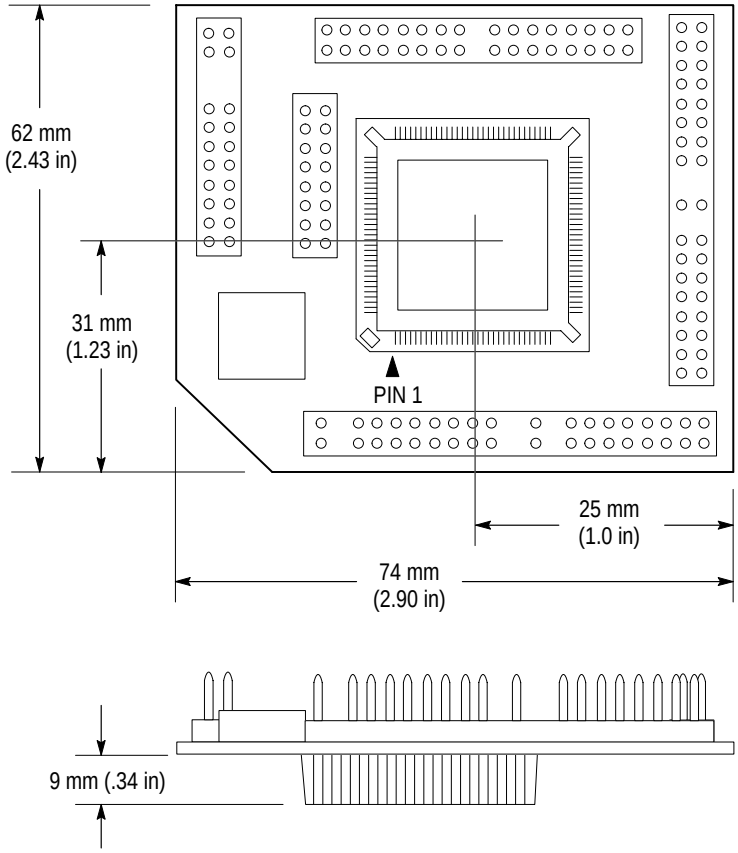


Figure 3–2: Dimensions of the PLCC probe adapter

Channel Assignments

Channel assignments shown in Table 3–4 through Table 3–10 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- A tilde (~) following a signal name indicates an active low signal.
- An equals sign (=) following a signal name indicates that it is double probed.

Table 3–4 shows the probe section and channel assignments for the Address group, and the microprocessor signal to which each channel connects. By default the display radix is hexadecimal.

Table 3–4: Address group channel assignments

Bit order	Section:channel	80286 signal name
23	A2:7	A23
22	A2:6	A22
21	A2:5	A21
20	A2:4	A20
19	A2:3	A19
18	A2:2	A18
17	A2:1	A17
16	A2:0	A16
15	A1:7	A15
14	A1:6	A14
13	A1:5	A13
12	A1:4	A12
11	A1:3	A11
10	A1:2	A10
9	A1:1	A9
8	A1:0	A8
7	A0:7	A7
6	A0:6	A6
5	A0:5	A5
4	A0:4	A4
3	A0:3	A3
2	A0:2	A2
1	A0:1	A1
0	A0:0	A0

Table 3–5 shows the probe section and channel assignments for the Data group, and the microprocessor signal to which each channel connects. By default the display radix is hexadecimal.

Table 3–5: Data group channel assignments

Bit order	Section:channel	80286 signal name
15	D1:7	D15
14	D1:6	D14
13	D1:5	D13
12	D1:4	D12
11	D1:3	D11
10	D1:2	D10
9	D1:1	D9
8	D1:0	D8
7	D0:7	D7
6	D0:6	D6
5	D0:5	D5
4	D0:4	D4
3	D0:3	D3
2	D0:2	D2
1	D0:1	D1
0	D0:0	D0

Table 3–6 shows the probe section and channel assignments for the Control group, and the microprocessor signal to which each channel connects. By default the display radix is symbolic.

Table 3–6: Control group channel assignments

Bit order	Section:channel	80286 signal name
7	C2:5	PEACK~
6	A3:6	HLDA
5	A3:7	COD/INTA~
4	A3:4	M/IO~
3	C2:3	S1~
2	C2:2	S0~
1	C2:6	LOCK~
0	C2:7	BHE~

Table 3–7 shows the probe section and channel assignments for the Intr group, and the microprocessor signal to which each channel connects. By default the display radix is symbolic.

Table 3–7: TMS 103 Intr group channel assignments

Bit order	Section:channel	80286 signal name
1	A3:1	NMI*
0	A3:0	INTR*

*** Signal not required for disassembly.**

Table 3–8 shows the probe section and channel assignments for the Copr group, and the microprocessor signal to which each channel connects. By default, Show Column is not selected for the 102-channel module. The default display radix is OFF for the 96-channel module.

Table 3–8: TMS 103 Copr group channel assignments

Bit order	Section:channel	80286 signal name
2	C3:7	BUSY~*
1	C3:6	ERROR~*
0	A3:3	PEREQ*

*** Signal not required for disassembly.**

Table 3–8 shows the probe section and channel assignments for the Misc group, and the microprocessor signal to which each channel connects. By default, Show Column is not selected for the 102-channel module. The default display radix is OFF for the 96-channel module.

Table 3–9: TMS 103 Misc group channel assignments

Bit order	96-channel section/probe	80286 signal name
3	A3:2	HOLD*
2	A3:5	READY~*
1	C2:4	CLK_B*
0	C3:5	RESET*

*** Signal not required for disassembly.**

Table 3–10 shows the probe section and channel assignments for the clock probes (not part of any group), and the 80286 signal to which each channel connects.

Table 3–10: TMS 103 clock channel assignments

Section:channel	Clk/Qual	80286 signal name
CK:0	Clk	CLK
CK:1	Clk*	COD/INTA_L~*
CK:2	Clk*	M/IO_L~*
C2:3	Qual	S1~
C2:2	Qual	S0~
C2:1	Qual	READY_L~
C2:0	Qual	HLDA_L

* **These channels are actually used as qualifiers.**

These channels are used only to clock in data; they are not acquired or displayed. To acquire data from any of the signals shown in Table 3–10, you must connect another channel probe to the signal, called double probing. An equals sign (=) following a signal name indicates that it is already double probed.

How Data is Acquired

This part of this chapter explains how the module acquires 80286 signals using the TMS 103 support and probe adapter. This part also provides additional information on microprocessor signals accessible on or not accessible on the probe adapter, and on extra acquisition channels available for you to use for additional connections

80286 Clocking

A special clocking program is loaded to the module every time you select the microprocessor support. This special clocking is called Custom for the 102-channel module or 96-channel module.

With this clocking, the module logs in signals from multiple groups of channels at different times when they are valid on the 80286 bus. The module then sends all the logged-in signals to the trigger machine and to the acquisition memory of the module for storage.

In Custom clocking for the 102-channel module or the 96-channel module, the module clocking state machine (CSM) generates one master sample for each 80286 bus cycle, no matter how many clock cycles are contained in the bus cycle.

Figure 3–3 shows the sample points and the master sample point.

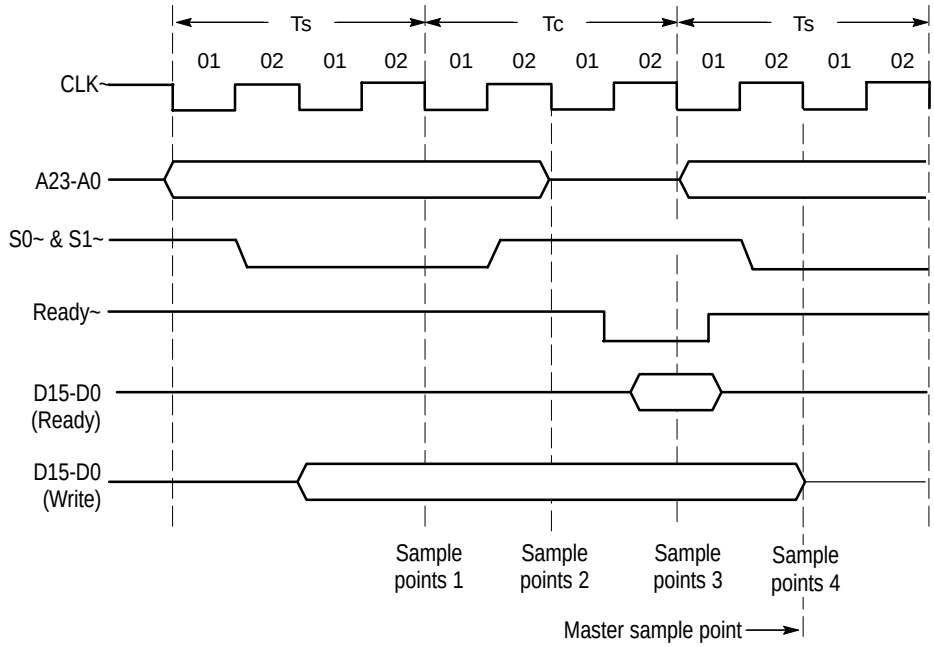


Figure 3–3: 80286 bus timing

Sample point AC includes A23-A0, some synchronous control signals (BHE~, BUSY~, COD/INTA~, ERROR~, HLDA, LOCK~, M/IO~, PEACK~, S1~, S0~), RESET, and CLK_B. If you use extra channels from C3:4-C3:0, D2:7-D2:0 or D3:7-D3:0, they are logged in on this sample point.

Sample point ASY includes the HOLD, INTR, NMI, and PEREQ asynchronous control signals.

Sample point D includes D15-D0.

Sample point M is the master sample point where data from sample points AC, Asy, and D is logged in.

Clocking Options

The clocking algorithm for the 80286 support is DMA Cycles.

DMA Cycles Excluded. Whenever the HLDA signal is high, no bus cycles are logged in. If either S1~ or S0~ become asserted while HLDA is high, a bus cycle has started and will continue until READY~ becomes asserted. Only bus cycles driven by the 80286 microprocessor (HLDA low) will be logged in.

DMA Cycles Included. All bus cycles, including DMA cycles, are logged in.

When the HLDA signal is high, the 80286 microprocessor has given up the bus to an alternate device. The design of the 80286 system affects what data will be logged in. The support only samples the data at the pins of the 80286 microprocessor. To properly log in bus activity, any buffers between the 80286 microprocessor and the alternate bus master must be enabled and pointing at the 80286 microprocessor.

There are three possible 80286 system designs and clocking interactions when an alternate bus master has control of the bus. The three different possibilities are listed below (in each case, the HLDA signal is logged in as a high level):

- If the alternate bus master drives the same control lines as the 80286 microprocessor, and the 80286 microprocessor “sees” these signals, the bus activity is logged in like normal bus cycles except that the HLDA signal is high.
- If HLDA and S0~ or S1~ become active, then the current bus cycle will be logged in as a DMA cycle.
- If HLDA becomes active and then inactive without either S0~ or S1~ becoming active, then the bus cycle will be logged in with the current bus cycles Address and Controls and the previous bus cycles Data.

When logging in DMA cycles, the data bus and control signals are logged in on the falling clock edge.

Alternate Microprocessor Connections

You can connect to microprocessor signals that are not required by the support so you can do more advanced timing analysis. These signals might or might not be accessible on the probe adapter board. The following paragraphs and tables list signals that are or are not accessible on the probe adapter board.

For a list of signals required or not required for disassembly, refer to the channel assignment tables beginning on page 3–5.

Signals On the Probe Adapter

All 80286 microprocessor signals are accessible on the probe adapter.

Extra Channels

Table 3–11 lists extra channels that are left after you have connected all the channels used by the support. You can use these extra channels to make alternate SUT connections. You can also disconnect channels not required by the support to make alternate connections. The channel assignment tables in this chapter indicate channels not required by the support for disassembly.

Table 3–11: Extra module sections and channels

Section	Channels
D3	7-0
D2	7-0
C3	4-0

For the 102-channel module, these channels (and signals you connect them to) are not defined as a channel group in the Channel Grouping Table of the LA Setup window. You need to access the Channel Grouping Table and define a channel group based on the extra channels.

For the 96-channel module, these channels (and signals you connect them to) are not defined as a channel group in the Channel Setup menu. You need to access the Channel Setup menu and define a channel group based on the extra channels.

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Maintenance

Maintenance

This section contains information on the probe adapter circuit description.

Probe Adapter Circuit Description

The TMS 103 probe adapter uses a 20R6 PAL (U1000) configured to act as a negative-edge triggered D flip-flop. This circuitry acts to latch the necessary control lines, ensuring the state of READY~, HLDA, M/IO~, and COD/INTA~. READY~ is the user-generated signal that ends the current bus cycle and is latched to meet the minimum setup time as a qualifier. HLDA is also latched to meet the minimum setup time as a qualifier. M/IO~ and COD/INTA~ are both latched to avoid uncertainty in the CPU idle cycle.

The clocking state machine uses the falling edge of CLK to determine when to log the necessary signals.

Replaceable Electrical Parts

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 103 80286 microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order.

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

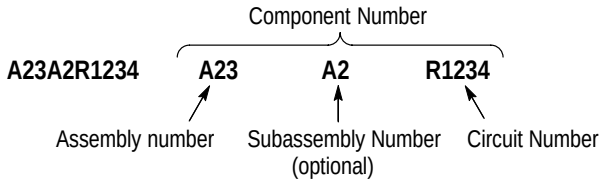
Parts list column descriptions

Column	Column name	Description
1	Component number	The component number appears on diagrams and circuit board illustrations, located in the diagrams section. Assembly numbers are clearly marked on each diagram and circuit board illustration in the *Diagrams* section, and on the mechanical exploded views in the *Replaceable Mechanical Parts* list section. The component number is obtained by adding the assembly number prefix to the circuit number (see Component Number illustration following this table). The electrical parts list is arranged by assemblies in numerical sequence (A1, with its subassemblies and parts, precedes A2, with its subassemblies and parts). Chassis-mounted parts have no assembly number prefix, and they are located at the end of the electrical parts list.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
6	Mfr. code	This indicates the code number of the actual manufacturer of the part.
7	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Component Number



Read: Resistor 1234 (of Subassembly 2) of Assembly 23

List of Assemblies

A list of assemblies is located at the beginning of the electrical parts list. The assemblies are listed in numerical order. When a part's complete component number is known, this list will identify the assembly in which the part is located.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
TK0875	MATSUO ELECTRONICS INC	831 S DOUBLAS ST	EL SEGUNDO CA 92641
01295	TEXAS INSTRUMENTS INC SEMICONDUCTOR GROUP	13500 N CENTRAL EXPY PO BOX 655303	DALLAS TX 75262–5303
04222	AVX CERAMICS DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
22526	BERG ELECTRONICS INC (DUPONT)	857 OLD TRAIL RD	ETTERS PA 17319
53387	MINNESOTA MINING MFG CO	PO BOX 2963	AUSTIN TX 78769–2963
63058	MCKENZIE TECHNOLOGY	910 PAGE AVENUE	FREMONT CA 94538
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A1	671–2387–00			CIRCUIT BD ASSY: 80286, PROBE ADAPTER, LASI III	80009	671238700
A2	671–2486–00			CIRCUIT BD ASSY: 80286 PROBE ADAPTER, PLCC68, SOCKETED;	80009	671248600
A1C245	283–5004–00			CAP, FXD, CERAMIC: MLC; 0.1UF, 10%, 25V, X7R, 1206	04222	12063C104KAT3A
A1C340	283–5004–00			CAP, FXD, CERAMIC: MLC; 0.1UF, 10%, 25V, X7R, 1206	04222	12063C104KAT3A
A1C345	290–5005–00			CAP, FXD, TANT: 47UF, 10%, 10V, 5.8MM X 4.6MM	TK0875	267M–1002–476–K
A1C400	283–5004–00			CAP, FXD, CERAMIC: MLC; 0.1UF, 10%, 25V, X7R, 1206	04222	12063C104KAT3A
A1C420	283–5004–00			CAP, FXD, CERAMIC: MLC; 0.1UF, 10%, 25V, X7R, 1206	04222	12063C104KAT3A
A1J130	131–5267–00			CONN, HDR: PCB, MALE, STR, 2 X 40, 0.1 CTR, 0.235	53387	N–2480–6122–TB
A1J300	131–5267–00			CONN, HDR: PCB, MALE, STR, 2 X 40, 0.1 CTR, 0.235	53387	N–2480–6122–TB
A1J310	131–5267–00			CONN, HDR: PCB, MALE, STR, 2 X 40, 0.1 CTR, 0.235	53387	N–2480–6122–TB
A1J350	131–5267–00			CONN, HDR: PCB, MALE, STR, 2 X 40, 0.1 CTR, 0.235	53387	N–2480–6122–TB
A1J530	131–5267–00			CONN, HDR: PCB, MALE, STR, 2 X 40, 0.1 CTR, 0.235	53387	N–2480–6122–TB
A1U410	160–8830–00			IC, DIGITAL: STTL, PLD; PAL, 20R6, 125MHZ, 210MA, PRGM 156–6381–00	80009	160–8830–00
A1U430	136–0921–00			SOCKET, PGA: PCB, 68 POS, 11 X 11, 0.1 CTR, 0.170 H X 0.183 TAIL, OPEN CTR, SYMMETRICAL, PAT1132	63058	PGA 68H101B1–11

Replaceable electrical parts list (cont.)

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A2	671–2486–00			CIRCUIT BD ASSY: 80286 PROBE ADAPTER, PLCC68, SOCKETED	80009	671248600
A2C1240	290–5005–00			CAP, FXD, TANT: 47UF,10%, 10V, 5.8MM X 4.6MM	TK0875	267M–1002–476–K
A2C1330	283–5004–00			CAP, FXD, CERAMIC: MLC; 0.1UF, 10%, 25V, X7R, 1206	04222	12063C104KAT3A
A2C1400	283–5004–00			CAP, FXD, CERAMIC: MLC; 0.1UF, 10%, 25V, X7R, 1206	04222	12063C104KAT3A
A2C1420	283–5004–00			CAP, FXD, CERAMIC: MLC; 0.1UF, 10%, 25V, X7R, 1206	04222	12063C104KAT3A
A2C1430	283–5004–00			CAP, FXD, CERAMIC: MLC; 0.1UF, 10%, 25V, X7R, 1206	04222	12063C104KAT3A
A2J1100	131–5267–00			CONN, HDR: PCB, MALE, STR, 2 X 40, 0.1 CTR, 0.235	53387	N–2480–6122–TB
A2J1130	131–5267–00			CONN, HDR: PCB, MALE, STR, 2 X 40, 0.1 CTR, 0.235	53387	N–2480–6122–TB
A2J1220	131–5267–00			CONN, HDR: PCB, MALE, STR, 2 X 40, 0.1 CTR, 0.235	53387	N–2480–6122–TB
A2J1350	131–5267–00			CONN, HDR: PCB, MALE, STR, 2 X 40, 0.1 CTR, 0.235	53387	N–2480–6122–TB
A2J1530	131–5267–00			CONN, HDR: PCB, MALE, STR, 2 X 40, 0.1 CTR, 0.235	53387	N–2480–6122–TB
A2P2330	—— ——			CONN, ADPT: SMD, PLCC; MALE, STR, 68 POS, 0.05 CTR, 0.268H, PLCC MALE TOSMD PADS (SEE RMPL)		
A2U1330	—— ——			SOCKET,PLCC: SMD, 68 POS, 0.05 CTR, 0.200 H, TIN, ACCOM 0.055–0.095 (SEE RMPL)		
A2U1420	156–6381–00			IC, DIGITAL: STTL, PLD; PAL, 20R6, 125MHZ, 210MA	01295	TIBPAL20R6–5CFN
A2U1420	160–8830–00			IC, DIGITAL: STTL, PLD; PAL, 20R6, 125MHZ, 210MA, PRGM 156–6381–00	80009	160–8830–00

Replaceable Mechanical Parts

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 103 80286 microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order.

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
TK2358	EMULATION TECHNOLOGY INC	2368B WALSH AVE, BLDG D	SANTA CLARA CA 95051
TK2548	XEROX BUSINESS SERVICES DIV OF XEROX CORPORATION	14181 SW MILLIKAN WAY	BEAVERTON OR 97077
05276	ITT POMONA ELECTRONICS DIV	1500 E 9TH ST PO BOX 2767	POMONA CA 91766–3835
53387	MINNESOTA MINING MFG CO	PO BOX 2963	AUSTIN TX 78769–2963
63058	MCKENZIE TECHNOLOGY	910 PAGE AVENUE	FREMONT CA 94538
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
1–0	010–0538–00			1	PROBE ADAPTER: 80286, PGA68, SOCKETED	80009	010053800
1–2	131–5267–00			2	CONN, HDR: PCB, MALE, STR, 2 X 40, 0.1 CTR, 0.235 MLG X 0.110 TAIL, 30GOLD (SEE A01 REPL J130, J300, J310, J350, J530)		
1–3	136–0921–00			1	SOCKET, PGA: PCB, 68 POS, 11 X 11, 0.1 CTR, 0.170 H X 0.183 TAIL, OPEN CTR, SYMMETRICAL, PAT 1132 (USED WITH 136–1023–00 TO FORM AN LCC–TO–PGA TEST CLIP)	63058	PGA 68H101B1–11
1–4	671–2387–00			1	CIRCUIT BD ASSY: 80286, PROBE ADAPTER, LASI III	80009	671238700
					STANDARD ACCESSORIES		
	070–9806–00			1	MANUAL, TECHNICAL: TMS 103, 80286 MICROPROCESSOR SUPPORT INSTRUCTION MANUAL	80009	070–9806–00
	070–9803–00			1	MANUAL, TECHNICAL: TLA 700 SERIES MICROPROCESSOR SUPPORT INSTALLATION	80009	070–9803–00
					OPTIONAL ACCESSORIES		
1–1	136–0921–00			2	SOCKET, PGA: PCB, 68 POS, 11 X 11, 0.1 CTR, 0.170 H X 0.183 TAIL, OPEN CTR, SYMMETRICAL, PAT 1132 (U430)	63058	AP3–68–PGA–G
1–5	103–0294–00			1	ADAPTER, CONN: 80186/80188 68 PIN LCC TO 68 PIN PGA (USED WITH 013–0250–00 TO FORM A LCC–TO PGA TESTCLIP)	TK2358	AP3–68–PGA–G
1–6	013–0250–00			1	ADAPTER, TEST: 68 PIN PLCC (USED WITH 1030311–00 TO FORM A LCC–TO–PGA TEST CLIP)	05276	E11886
1–7	103–0311–00			2	ADAPTER, CONN: 68186/8088 68 PIN PGA TO PLCC (USED WITH 013–0250–00 TO FORM AN LCC–TO PGA TESTCLIP)	TK2358	AC–PGA–PCC–8018
1–8	136–1023–00			1	SKT, PL–IN ELEK: MICROCKT, 68 CONTACT, LCC (USED WITH 136–0921–00 T0 FORM AN LCC–TO PGA TESTCLIP)	53387	2–0068–05400–08
	070–9802–00			1	MANUAL, TECH: BASIC OPS MICROPROCESSOR SUPPPORT ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070–9802–00

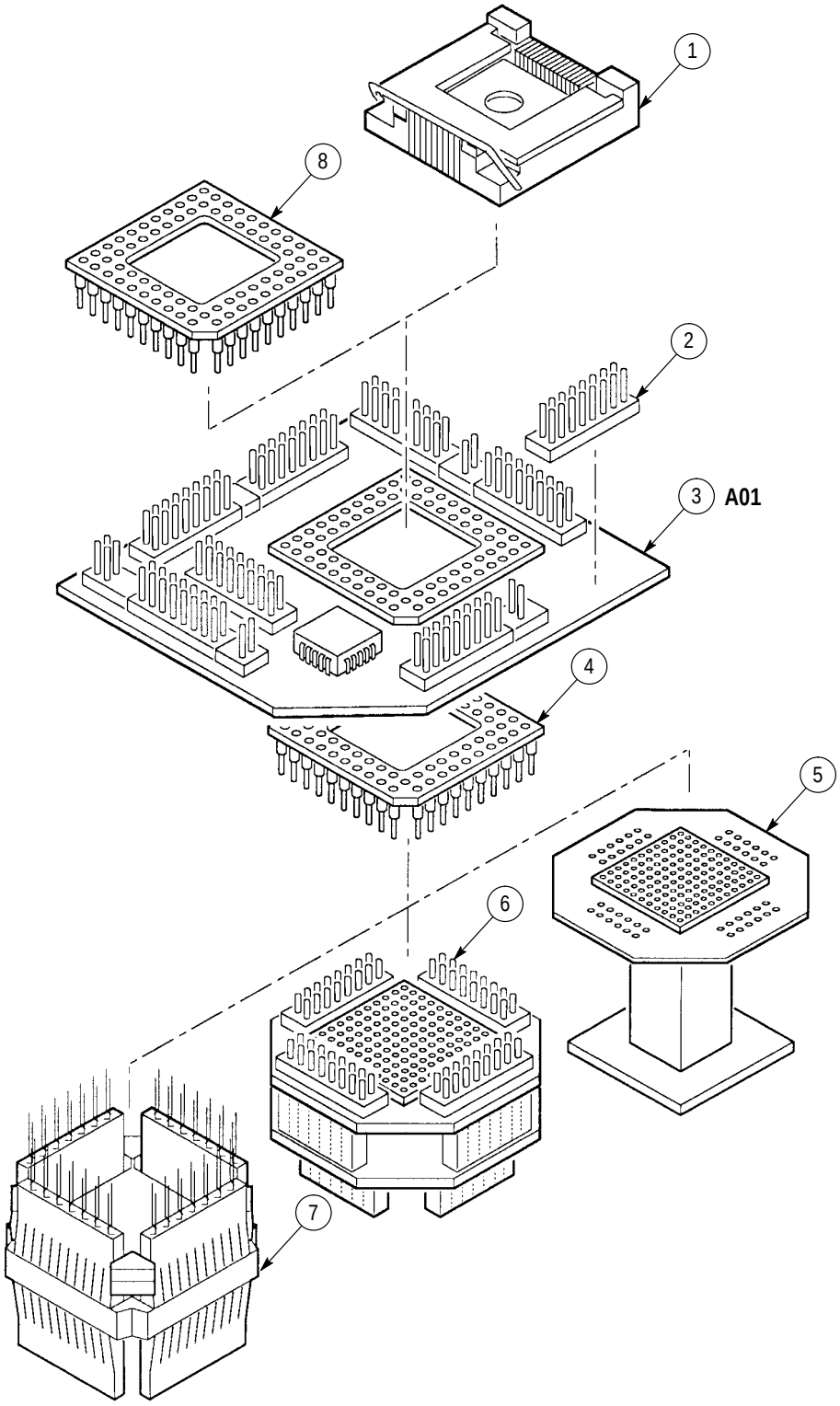


Figure 1: PGA probe adapter exploded view

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
2–1	131–5267–00			2	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD (SEE A02 REPL J1100,J1130,J1220,J1350,J1530)		
2–2	671–2486–00			1	CIRCUIT BD ASSY:80286 PROBE ADAPTER, PLCC68,SOCKETED	80009	671248600
					STANDARD ACCESSORIES		
	070–9806–00				MANUAL,TECH:TMS 103, INSTRUCTION, 80286, DISASSEMBLER	80009	070980600
	070–9803–00			1	MANUAL, TECH:TLA 700 SERIES MICROPROCESSOR SUPPORT INSTALLATION	80009	070–9803–00
					OPTIONAL ACCESSORIES		
	070–9802–00			1	MANUAL, TECH:BASIC OPS MICRO SUP ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070–9802–00

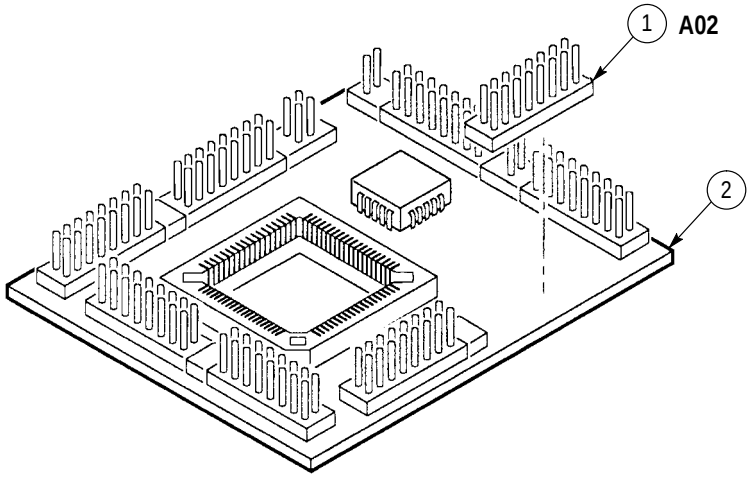


Figure 2: PLCC probe adapter exploded view

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