Instruction Manual

Tektronix

TMS 107
i486 Microprocessor Support

070-9810-00

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

Printed in the U.S.A.

Tektronix, Inc., P.O. Box 1000, Wilsonville, OR 97070–1000

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Use Proper Voltage Setting. Before applying power, ensure that the line selector is in the proper position for the power source being used.

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

The common terminal is at ground potential. Do not connect the common terminal to elevated voltages.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Replace Batteries Properly. Replace batteries only with the proper type and rating specified.

Recharge Batteries Properly. Recharge batteries for the recommended charge cycle only.

Use Proper AC Adapter. Use only the AC adapter specified for this product.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Wear Eye Protection. Wear eye protection if exposure to high-intensity rays or laser radiation exists.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface: Microprocessor Support Documentation

This instruction manual contains specific information about the TMS 107 i486 microprocessor support and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor supports on the logic analyzer for which the TMS 107 i486 support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor supports, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor supports is included with each product. Each logic analyzer has basic information that describes how to perform tasks common to supports on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing disassembled data
- The TMS 107 i486 probe adapter

Manual Conventions

This manual uses the following conventions:

- The term disassembler refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to online help, an installation manual, or a basic operations of microprocessor supports user manual.
- In the information on basic operations, the term XXX or P54C used in field selections and file names can be replaced with 486. This is the name of the microprocessor in field selections and file names you must use to operate the i486 support.
- The term system under test (SUT) refers to the microprocessor-based system from which data will be acquired.

- The term logic analyzer refers to the Tektronix logic analyzer for which this product was purchased.
- The term module refers to a 102/136-channel or a 96-channel module.
- 486 refers to all supported variations of the i486 microprocessor unless otherwise noted.
- A pound sign (#) following a signal name indicates an active low signal.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The user manual provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or, contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Contact your local Tektronix distributor or sales office. Or, visit our web site for a listing of worldwide service locations. http://www.tek.com
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000

Getting Started

Getting Started

This chapter provides information on the following topics:

- The TMS 107 i486 microprocessor support
- Logic analyzer software compatibility
- Your i486 system requirements
- i486 support restrictions
- How to configure the probe adapter
- How to connect to the system under test (SUT)
- How to apply power to and remove power from the probe adapter

Support Description

The TMS 107 microprocessor support disassembles data from systems that are based on the Intel i486 microprocessor, including SL-enhanced versions. The support runs on a compatible Tektronix logic analyzer equipped with a 102/136-channel module, or a 96-channel module.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 107 microprocessor support.

Table 1–1 shows which microprocessors and their packages the TMS 107 supports.

Table 1–1: Supported microprocessors

Microprocessor*	Package
i486DX2	PGA
i486DX	PGA
i486DX-50	PGA
i486SX	PGA
i486SX	PGA

*** Includes SL-enhanced variations.**

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Mechanical Parts* chapter.

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Parts* chapter.

To use this support efficiently, you need to have the items listed in the information on basic operations, as well as the following items:

- The *i486 DX Microprocessor Data Book*, Intel, Inc. 1991 (240440-004)
- The *i486 Microprocessor Programmer's References Manual*, Intel, Inc., 1990 (240486-001)
- The *i486 Microprocessor,* Intel, Inc., 1989 (240440-002)
- The *i486 SX Microprocessor/487 SX Math Coprocessor,*Intel, Inc., 1991 (240950-001)
- The *i486 DX CPU-Cache Chip Set,Microprocessor,*Intel, Inc., 1991 (241084-001)
- The *S-Series i486 CPU External Design,*Intel, Inc., revision 1.0
- The *80486 Microprocessor User's Manual,*Intel, Inc., 1993 (ISBN 1-55512-170-5)

Information on basic operations also contains a general description of supports.

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

To use the i486 support, the Tektronix logic analyzer must be equipped with at least a 102/136-channel module, or a 96-channel module. The module must be equipped with enough probes to acquire channel and clock data from signals in your i486-based system.

Refer to information on basic operations to determine how many modules and probes the logic analyzer needs to meet the channel requirements.

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor supports in the information on basic operations as they pertain to your SUT.

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other i486 support requirements and restrictions.

System Clock Rate. The TMS 107 support can acquire data from the i486 microprocessor at speeds of up to 50 MHz[1].

Hardware Reset. If a hardware rest occurs in your i486 system during an acquisition, the disassembler may acquire an invalid sample.

Cache Invalidation. Correct disassembly is not guaranteed for microprocessor systems that run cache invalidations concurrent with burst cycles. Data for these cycles will not be disassembled and will be labeled as Cache Invalidation cycles.

Disabling the Instruction Cache. To disassemble acquired data, you must disable the internal instruction cache. Disabling the caches makes all instruction prefetches visible on the bus so they can be acquired and disassembled.

Dynamic Bus Sizing. When the Bus Size Control signals (BS16# or BS8#) are asserted, the i486 microprocessor allows the bus width to be changed for extra cycles (when more than one cycle is required for a transaction). The disassembler does not support changing the bus size for extra cycles. To keep the disassembler synchronized, you can use the Mark Opcode function as described in *Marking Cycles* in the *Operating Basics* chapter.

Little-Endian Byte Ordering. The disassembler always uses Little-Endian byte ordering for instruction disassembly. Little-Endian byte ordering is when the least significant data byte is located at the lowest address.

Data Reads and Writes. The disassembler will not link data reads and writes with the instructions which cause them.

Locked Bus Cycles. The disassembler will not identify locked bus cycles.

1 **Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest devices supported.**

Disabling the Instruction Cache

To disassemble acquired data, you must disable the i486 instruction cache. Disabling the cache makes all instruction prefetches visible on the bus so they can be acquired and disassembled.

If you cannot disable the cache through software or some other means on your SUT, you can disable it on the i486 probe adapter. To disable the cache on the i486 probe adapter, you can cut pin F15 (KEN# signal) on the sacrificial socket on the underside of the probe adapter board. If you want to acquire timing data for general purpose analysis from the KEN# signal, you can replace the damaged sacrificial socket.

CAUTION. *To prevent permanent damage to the i486 probe adapter, do not cut pin F15 on the socket soldered to the topside of the probe adapter. If you do cut F15 on the soldered socket, the KEN# signal can never be acquired again using that probe adapter.*

When you cut pin F15 on the sacrificial socket of the probe adapter, the KEN# signal does not connect to your SUT from the i486 microprocessor in the probe adapter. A pullup resistor on the probe adapter pulls KEN# into the inactive state which stops anything from being cached.

Configuring the Probe Adapter

There are six jumpers on the probe adapter. One is set to power the PAL on the TMS 107 probe adapter from the system under test (SUT) or an external source. Another is used to set the PAL to synthesize A1 and A0 for display purposes. The remaining four jumpers are used to connect the FERR#, BRDYC#, NMI, and IGNNE# signals to the correct pins on the microprocessor socket of the probe adapter.

Power Source Jumper

The Power Source jumper (J420) should be positioned on pins 1 and 2 if you have a +5 V i486 microprocessor and the probe adapter will be powered from the SUT. If the probe adapter will be powered by an external source, position this jumper on pins 2 and 3.

For more information on using an alternate power source, refer to *Applying and Removing Power* later in this section.

Figure 1–1 shows the location of J420 on the probe adapter.

Address Synthesis Jumper

Address signals A1 and A0 are not available on the i486 microprocessor. The PAL (U410) on the probe adapter can synthesize signals A1 and A0 for display and triggering purposes. To synthesize addresses A1 and A0, position J421 on pins 2 and 3. If you do not want to synthesize these signals, position J421 on pins 1 and 2; in this position, both A1 and A0 connect to ground.

***NOTE**. Due to limitations of the probe adapter, you should not synthesize A1 and A0 on a i486 system operating at or above 50 MHz.*

Figure 1–1 shows the location of J421 on the probe adapter.

FERR#, BRDYC#, NMI and IGNNE# Signal Jumpers

The FERR#, BRDYC#, NMI and IGNNE# signal jumpers should be set in the correct position for the microprocessor from which you are acquiring data. Table 1–2 shows how to position these jumpers for i486 microprocessors, including SL-enhanced variations.

Table 1–2: Microprocessor configuration jumper positions

	Jumper position			
Microprocessor	**J422, FERR#**	**J423, BRDYC#**	**J430, NMI**	**J431, IGNNE#**
i486SX (P23)	pins 2, 3	pins 1, 2	pins 2, 3	pins 2, 3
i487SX	pins 2, 3	pins 1, 2	pins 1, 2	pins 1, 2
i486DX (P4)	pins 1, 2	pins 1, 2	pins 1, 2	pins 1, 2
i486DX-50 (Normal Mode)	pins 1, 2	pins 1, 2	pins 1, 2	pins 1, 2
i486DX-50 (Chipset Mode)	pins 1, 2	pins 2, 3	pins 1, 2	pins 1, 2
i486DX2 (P24)	pins 1, 2	pins 1, 2	pins 1, 2	pins 1, 2
SL-Enhanced i486SX	pins 2, 3	pins 1, 2	pins 2, 3	pins 2, 3
SL-Enhanced i486DX	pins 1, 2	pins 1, 2	pins 1, 2	pins 1, 2
SL-Enhanced i486DX2	pins 1, 2	pins 1, 2	pins 1, 2	pins 1, 2
i486 Overdrive (+5 V)	pins 2, 3	pins 1, 2	pins 1, 2	pins 1, 2
i486 Overdrive (+3 V)	pins 2, 3	pins 1, 2	pins 1, 2	pins 1, 2

You can contact your Tektronix representative for pin compatibility of future 486 microprocessor variations.

Figure 1–2 shows the location of J422, J423, J430 and J431 on the probe adapter.

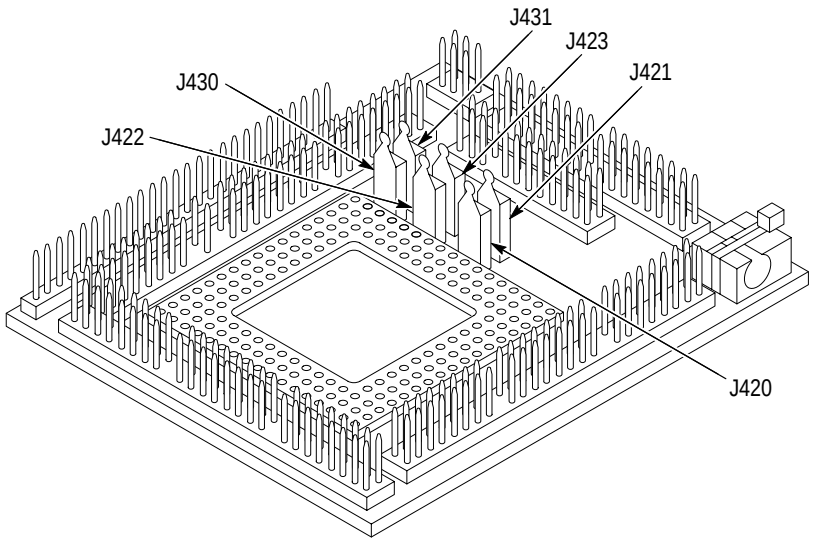

Figure 1–1: Jumper locations on the probe adapter

Connecting to the System Under Test

Before you connect to the SUT, you must connect the probes to the module. Your SUT must also have a minimum amount of clear space surrounding the microprocessor to accommodate the probe adapter. Refer to the *Specifications* chapter in this manual for the required clearances.

The channel and clock probes shown in this chapter are for a 102/136-channel module. Your probes will look different if you are using a 96-channel module.

The general requirements and restrictions of microprocessor supports in the information on basic operations shows the vertical dimensions of a channel or clock probe connected to square pins on a circuit board.

PGA Probe Adapter

To connect the logic analyzer to a SUT using a PGA probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probe adapter, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.

3. Place the probe adapter onto the antistatic shipping foam to support the probe as shown in Figure 1–2. This prevents the circuit board from flexing and the socket pins from bending.

4. Remove the microprocessor from your SUT.

5. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on the microprocessor.

CAUTION. *Failure to correctly place the microprocessor into the probe adapter might permanently damage the microprocessor once power is applied.*

6. Place the microprocessor into the probe adapter as shown in Figure 1–2.

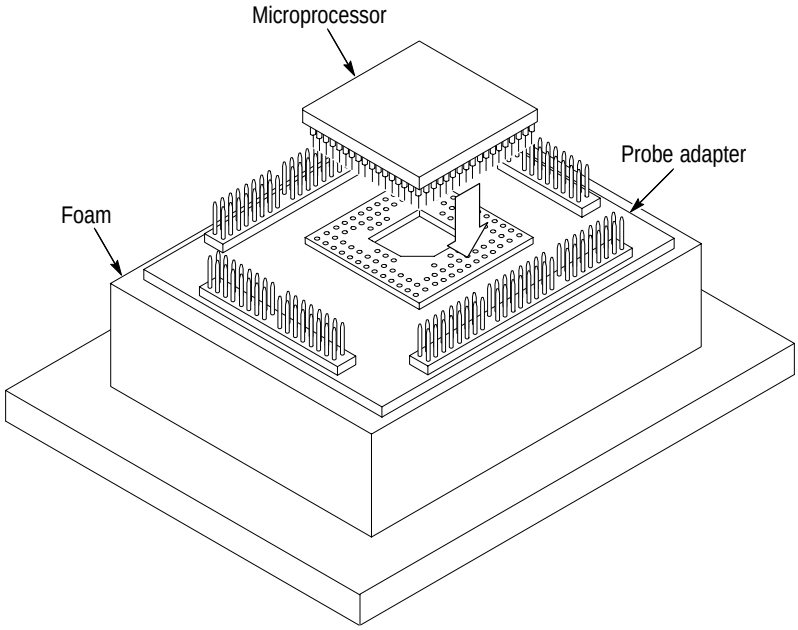

Figure 1–2: Placing a microprocessor into a PGA probe adapter

7. Connect the channel and clock probes to the probe adapter as shown in Figure 1–3. Match the channel groups and numbers on the probe labels to the corresponding pins on the probe adapter. Match the ground pins on the probes to the corresponding pins on the probe adapter.

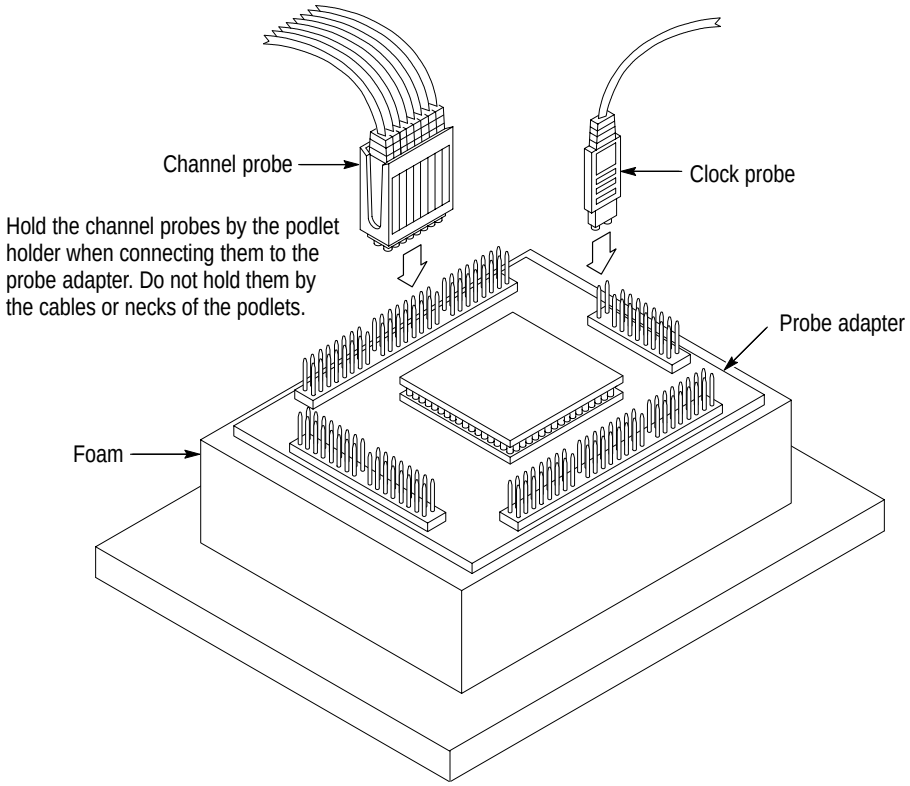

Figure 1–3: Connecting probes to a PGA probe adapter

8. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on your SUT.

9. Place the probe adapter onto the SUT as shown in Figure 1–4.

NOTE. *You might need to stack one or more replacement sockets between the SUT and the probe adapter to provide sufficient vertical clearance from adjacent components. However, keep in mind that this might increase loading, which can reduce the electrical performance of your probe adapter.*

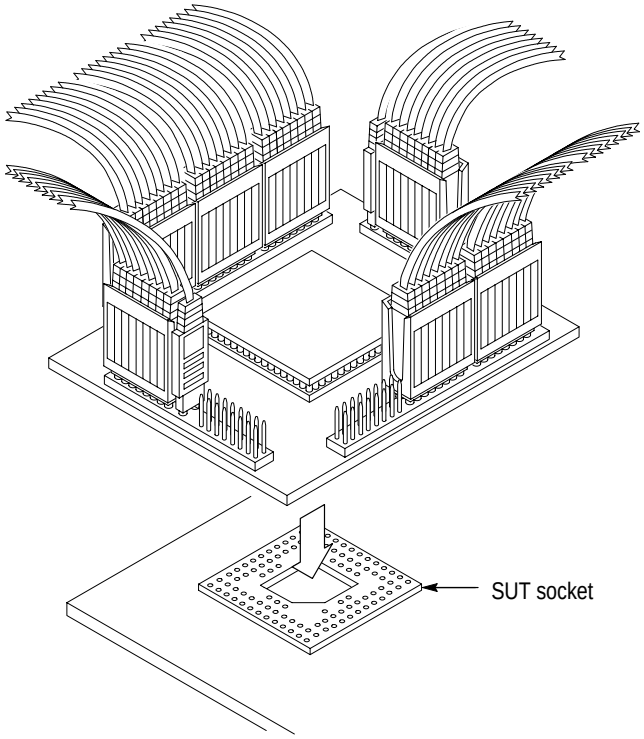

Figure 1–4: Placing a PGA probe adapter onto the SUT

Without a Probe Adapter

You can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your SUT.

To connect the probes to i486 signals in the SUT using a test clip, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor.

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2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from it.

CAUTION. *Failure to place the SUT on a horizontal surface before connecting the test clip might permanently damage the pins on the microprocessor.*

3. Place the SUT on a horizontal static-free surface.

4. Use Table 1–3 to connect the channel probes to i486 signal pins on the test clip or in the SUT.

Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip.

Table 1–3: i486 signal connections for channel probes

Section:channel	i486 signal	Section:channel	i486 signal
A3:7	A31	D3:7	D31
A3:6	A30	D3:6	D30
A3:5	A29	D3:5	D29
A3:4	A28	D3:4	D28
A3:3	A27	D3:3	D27
A3:2	A26	D3:2	D26
A3:1	A25	D3:1	D25
A3:0	A24	D3:0	D24
A2:7	A23	D2:7	D23
A2:6	A22	D2:6	D22
A2:5	A21	D2:5	D21
A2:4	A20	D2:4	D20
A2:3	A19	D2:3	D19
A2:2	A18	D2:2	D18
A2:1	A17	D2:1	D17
A2:0	A16	D2:0	D16
A1:7	A15	D1:7	D15
A1:6	A14	D1:6	D14
A1:5	A13	D1:5	D13
A1:4	A12	D1:4	D12
A1:3	A11	D1:3	D11
A1:2	A10	D1:2	D10
A1:1	A9	D1:1	D9
A1:0	A8	D1:0	D8
A0:7	A7	D0:7	D7
A0:6	A6	D0:6	D6

Table 1–3: i486 signal connections for channel probes (cont.)

Section:channel	i486 signal	Section:channel	i486 signal
A0:5	A5	D0:5	D5
A0:4	A4	D0:4	D4
A0:3	A3	D0:3	D3
A0:2	A2	D0:2	D2
A0:1	A1	D0:1	D1
A0:0	A0	D0:0	D0
C3:7	CLK=*	C2:7	AHOLD
C3:6	BE2#	C2:6	BEO#
C3:5	D/C#	C2:5	W/R#
C3:4	BS8#	C2:4	SMIACT#
C3:3	BE1#	C2:3	HLDA
C3:2	BE3#	C2:2	BLAST#
C3:1	M/IO#	C2:1	ADS#
C3:0	BS16#	C2:0	BOFF#
C1:7	RESET#*	C0:7	NMI*
C1:6	FLUSH#*	C0:6	IGNNE#*
C1:5	PLOCK#*	C0:5	EADS#*
C1:4	BREQ#*	C0:4	SRESET#*
C1:3	INTR#*	C0:3	HOLD*
C1:2	FERR#*	C0:2	KEN#*
C1:1	BRDY#=*	C0:1	LOCK#*
C1:0	BRDYC#=*	C0:0	RDY#=*

*** Signal not required for disassembly.**

Table 1–4 shows the clock probes, and the i486 signal to which they must connect for disassembly to be correct.

Table 1–4: i486 signal connections for clock probes

Section:channel	i486 signal
CK:3	CLK
CK:2	RDY#
CK:1	BRDY#
CK:0	BRDYC#

5. Align pin 1 or A1 of your test clip with the corresponding pin 1 or A1 of the i486 microprocessor in your SUT and attach the clip to the microprocessor.

Applying and Removing Power

If your microprocessor system cannot supply power to the i486 probe adapter or your system has a +3.3 V i486 microprocessor (probe adapters need +5 V), you must use an alternate power source. A +5 V power supply for the i486 probe adapter is available as an optional accessory. Refer to the *Replaceable Mechanical Parts* chapter for information on how to order a power supply.

The alternate power supply provides +5 volts to the i486 probe adapter. The center connector of the power jack connects to Vcc.

To use the power supply, the Power Source jumper (J420) on the probe adapter must be positioned on pins 2 and 3.

NOTE. *Whenever the SUT is powered off, be sure to remove power from the probe adapter.*

To apply power to the i486 probe adapter and SUT, follow these steps:

CAUTION. *Failure to use the +5 V power supply provided by Tektronix might permanently damage the probe adapter and i486 microprocessor. Do not mistake another power supply that looks similar for the +5 V power supply.*

1. Connect the +5 V power supply to the jack on the probe adapter. Figure 1–5 shows the location of the jack on the adapter board.

CAUTION. *Failure to apply power to the probe adapter before applying power to your SUT might permanently damage the i486 microprocessor and SUT.*

2. Plug the power supply for the probe adapter into an electrical outlet.
3. Power on the SUT.

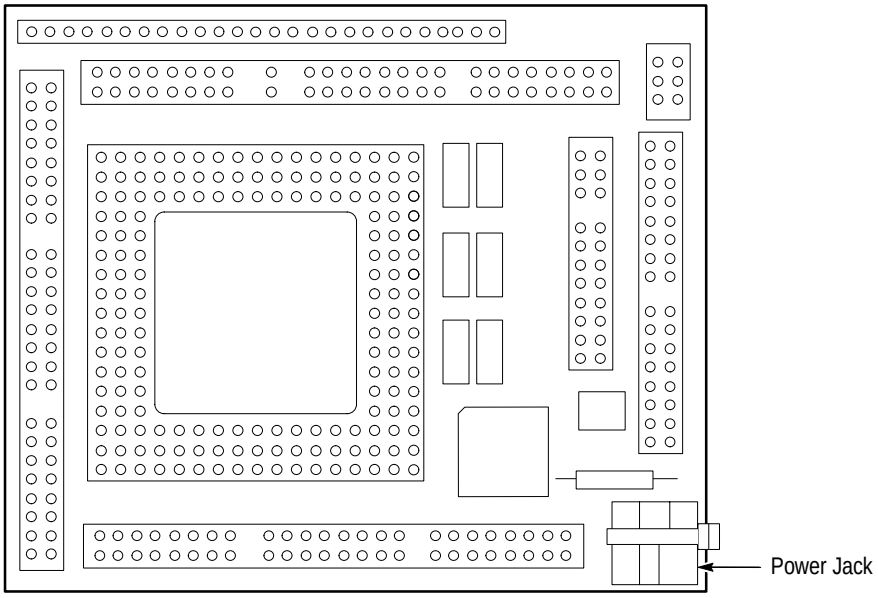


Figure 1–5: Location of the power jack

To remove power from the SUT and i486 probe adapter, follow these steps:

CAUTION. *Failure to power down your SUT before removing the power from the probe adapter might permanently damage the i486 microprocessor and SUT.*

1. Power down the SUT.
2. Unplug the power supply for the probe adapter from the electrical outlet.

Operating Basics

Setting Up the Support

This section provides information on how to set up the support. Information covers the following topics:

- Channel group definitions
- Clocking options
- Symbol table files

Remember that the information in this section is specific to the operations and functions of the TMS 107 i486 support on any Tektronix logic analyzer for which it can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and disassemble data, you need to load the support and specify setups for clocking, and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Groups and Assignments

The disassembler software automatically defines the channel groups for the microprocessor. The channel groups for the i486 microprocessor are Address, Data, Control, DataSize, Misc, Cache, and Misc2.

Clocking Options

The TMS 107 support offers a microprocessor-specific clocking mode for the i486 microprocessor. This clocking mode is the default selection whenever you select the 486 support.

A description of how cycles are sampled by the module using the support and probe adapter is found in the *Specifications* chapter.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

The clocking option for the TMS 107 support is Alternate Bus Master Cycles.

Alternate Bus Master Cycles

An alternate bus master cycle is defined as the i486 microprocessor giving up the bus to an alternate device (a DMA device or another microprocessor). These types of cycles are acquired when you select Included.

Symbols

The TMS 107 support supplies one symbol table file. The 486_Ctrl file replaces specific Control channel group values with symbolic values when Symbolic is the radix for the channel group.

Table 2–1 shows the name, bit pattern, and meaning for the symbols in the file 486_Ctrl, the Control channel group symbol table.

Table 2–1: Control group symbol table definitions

Symbol	Control group value BLAST# AHOLD HLDA BOFF# M/IO# D/C# W/R# SMIACT#	Meaning
SMM_FETCH	X X 0 1 1 0 0 0	Opcode Fetch from SM space/Opcode Fetch from SMRAM space
SMM_M_RD	X X 0 1 1 1 0 0	A memory read cycle from SM space
SMM_M_WR	X X 0 1 1 1 1 0	A memory write cycle to SM space
SMM_IO_RD	X X 0 1 0 1 0 0	An I/O read cycle from SM space
SMM_IO_WR	X X 0 1 0 1 1 0	An I/O write cycle to SM space
RVP_FETCH	X X 0 1 1 0 0 1	Fetch from Real, Virtual86 or Protected space
RVP_M_RD	X X 0 1 1 1 0 1	A memory read cycle from Real, Virtual86 or Protected space
RVP_M_WR	X X 0 1 1 1 1 1	A memory write cycle to Real, Virtual86 or Protected space
RVP_IO_RD	X X 0 1 0 1 0 1	An I/O read cycle from Real, Virtual86 or Protected space
RVP_IO_WR	X X 0 1 0 1 1 1	An I/O write cycle to Real, Virtual86 or Protected space
INT_ACK	X X 0 1 0 0 0 X	Responding to an interrupt to or from any memory space
SPECIAL	X X 0 1 0 0 1 X	A Shutdown, Cacheflush, Halt, Writeback cycle, and so on
RESERVED	X X 0 1 1 0 1 X	Reserved
ALT_B_MTR	X X 1 X X X X 1	Bus released to another bus master
BACK_OFF	X X X 0 X X X X	A Backoff cycle
BG_AHOLD*	X 1 0 1 X X X X	An Address Hold in the background of any cycle
FETCH*	X X 0 1 1 0 0 X	Opcode Fetch from any memory space
MEM_READ*	X X 0 1 1 1 0 X	Non-opcode memory read from any memory space
MEM_WRITE*	X X 0 1 1 1 1 X	Any memory write to any memory space
IO_READ*	X X 0 1 0 1 0 X	An I/O data read cycle from any memory space
IO_WRITE*	X X 0 1 0 1 1 X	An I/O data write cycle to any memory space

Table 2–1: Control group symbol table definitions (cont.)

Symbol	Control group value BLAST# M/IO# AHOLD D/C# HLDA W/R# BOFF# SMIACT#	Meaning
SMM_M_R/W*	X X 0 1 1 1 X 0	A memory read or write cycle to or from SM space
SMMIO_R/W*	X X 0 1 0 1 X 0	An I/O read or write cycle to or from SM space
RVP_M_R/W*	X X 0 1 1 1X 1	A memory read or write cycle in R, V, or P space
RVPIO_R/W*	X X 0 1 0 1 X 1	An I/O read or write cycle in R, V, or P space
MEM_R/W*	X X 0 1 1 1 X X	Nonopcode read or write, to or from any memory space
IO_R/W*	X X 0 1 0 1 X X	Any I/O read or write, to or from any memory space
SMM_RD*	X X 0 1 X 1 0 0	Any read cycle from SM space
SMM_WR*	X X 0 1 X 1 1 0	Any write cycle to SM space
RVP_RD*	X X 0 1 X 1 0 1	Any read cycle from R, V, or P space
RVP_WR*	X X 0 1 X 1 1 1	Any write cycle to R, V, or P space
READ*	X X 0 1 X 1 0 X	Any read, except fetch and int ack, from any memory space
WRITE*	X X 0 1 X 1 1 X	Any memory or I/O write to any memory space
SMM_R/W*	X X 0 1 X 1 X 0	Any nonopcode access to or from SM space
RVP_R/W*	X X 0 1 X 1 X 1	Any nonopcode access to or from R, V, or P space
R/W*	X X 0 1 X 1 X X	Any nonopcode access to or from any memory space
SMM*	X X 0 1 X X X 0	Any access to or from SM space
RVP*	X X 0 1 X X X 1	Any access to or from Real, Virtual86, or Protected space

*** Symbols used only for triggering; they are not displayed.**

Information on basic operations describes how to use symbolic values for triggering, and displaying other channel groups symbolically, such as the Address channel group.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. Information covers the following topics:

- Acquiring data
- Viewing disassembled data in various display formats
- Cycle type labels
- How to change the way data is displayed
- How to change disassembled cycles with the mark cycles function

Acquiring Data

Once you load the 486 support, choose a clocking mode and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual, whichever is available.

Viewing Disassembled Data

You can view disassembled data in four different display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE. *Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2-8.*

The default display format shows the Address, Data, and Control channel group values for each sample of acquired data.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–2 shows the special characters and strings displayed by the i486 disassembler and gives a definition of what they represent.

Table 2–2: Special characters in the display and meaning

Character or string displayed	Meaning
m	The instruction was manually marked as a program fetch
****	Indicates there is insufficient data available for complete disassembly of the instruction; the number of asterisks will indicate the width of the data that is unavailable. Each two asterisks represent a byte.
#	Indicates an immediate value
c	Indicates a Cache Invalidation cycle
SMM	Indicates the microprocessor is operating in System Management Mode

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–3 shows these cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled with the vector name.

Table 2–3: Cycle type definitions

Cycle type	Definition
(MEM_READ)	A read from memory that is not an opcode fetch
(MEM_WRITE)	Any write to memory
(I/O_READ)	A read from an I/O port
(I/O_WRITE)	A write to an I/O port
(INT_ACK)	An Interrupt Acknowledge cycle
(SHUTDOWN)	A Shutdown cycle; the cycle type is HALT/SPECIAL and the address is 0H (BE3#-BE0# = 1110)
(CACHE FLUSH)	A Cache Flush cycle; the cycle type is HALT/SPECIAL and the address is 01H (BE3#-BE0# = 1101)

Table 2–3: Cycle type definitions (cont.)

Cycle type	Definition
(HALT)	A Halt cycle; the cycle type is HALT/SPECIAL and the address is 02H (BE3#-BE0# = 1011)
(WRITE-BACK)	A Write Back cycle; the cycle type is HALT/SPECIAL and the address is 03H (BE3#-BE0# = 0111)
(FIRST FLUSH ACK)	A First Flush Ack cycle; the cycle type is HALT/SPECIAL and the address is 07H (BE3#-BE0# = 0111)
(SECOND FLUSH ACK)	A Second Flush Ack cycle; the cycle type is HALT/SPECIAL and the address is 05H (BE3#-BE0# = 1101)
(STOP GRANT ACK)	A Stop Grant Ack cycle; the cycle type is HALT/SPECIAL and the address is 012H (BE3#-BE0# = 1011)
(RESERVED)	Reserved
(BACK OFF)	A Back Off bus cycle
(ALTERNATE BUS MASTER)	The bus is released to an alternate bus master
(UNKNOWN)	The combination of bits in the Control channel group is either unexpected or unrecoginzed.
(EXTENSION) *	A fetch cycle computed to be an opcode extension
(FLUSH)	A fetch cycle computed to be flushed
(CACHE/BURST FILL)	A fetch cycle computed to be a burst fill; the data is fetched but not executed because it is part of a 16-byte fetch; the cycle may be stored in cache

* **Computed cycle types.**

Figure 2–1 shows an example of the Hardware display.

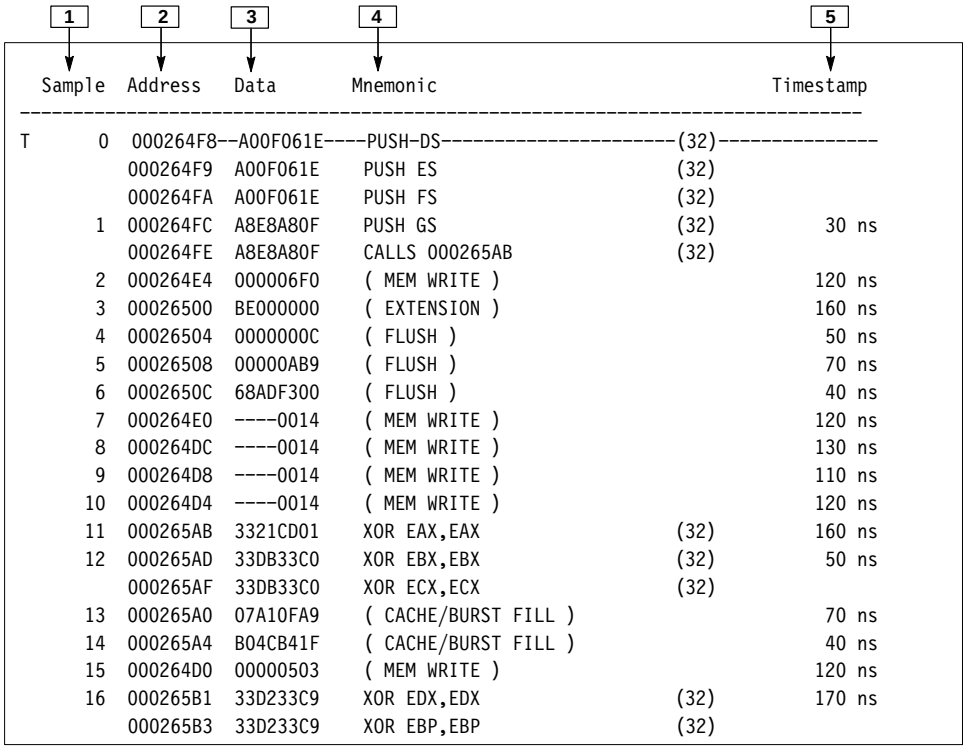


Figure 2–1: Hardware display format

1 **Sample Column.** Lists the memory locations for the acquired data.

2 **Address Group.** Lists data from channels connected to the i486 Address bus.

3 **Data Group.** Lists data from channels connected to the i486 Data bus.

4 **Mnemonic Column.** Lists the disassembled instructions and cycle types.

5 **Timestamp.** Lists the timestamp values when a timestamp selection is made. Information on basic operations describes how you can select a timestamp.

Software Display Format

The Software display format shows only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction.

Control Flow Display Format

The Control Flow display format shows only the first fetch of instructions that change the flow of control.

Instructions that generate a change in the flow of control in the i486 microprocessor are as follows:

CALL	IRET	RET
INT	JMP	RSM

Instructions that might generate a change in the flow of control in the i486 microprocessor are as follows:

BOUND	JLE/JNG*	JP/JPE*
DIV	JNB/JAE/JNC*	JNS
IDIV	JNBE/JA*	JS
INTO	JNE/JNZ*	LOOP
JB/JNAE/JC*	JNL/JGE*	LOOPNZ/LOOPNE*
JBE/JNA*	JNLE/JG*	LOOPZ/LOOPE*
JCXZ/JECXZ*	JNO	RET
JE/JZ	JNP/JPO*	RSM
JL/JNGE*	JO	

Subroutine Display Format

The Subroutine display format shows the first fetch of subroutine calls, traps, interrupts, exception vector reads, and return instructions. It will display conditional subroutine calls if they are considered to be taken.

Instructions that generate a subroutine call or a return in the i486 microprocessor are as follows:

CALL	INT	IRET	RET

Instructions that might generate a subroutine call or a return in the i486 microprocessor are as follows:

BOUND	IDIV	RSM
DIV	INTO	

Changing How Data is Displayed

There are fields and features that allow you to further modify displayed data to suit your needs. You can make selections unique to the i486 support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception vectors

*** The disassembler recognizes all the instructions in this group, but only displays the first one shown.**

Optional Display Selections

You can make optional display selections for disassembled data to help you analyze the data. You can make optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

In addition to the common display options (described in the information on basic operations), you can change the displayed data in the following ways:

- Specify the code segment size
- Choose an interrupt table
- Specify the starting address of the interrupt table
- Specify the size of the interrupt table

The i486 support has four additional fields: Code Segment Size, Interrupt Table, Interrupt Table Address, and Interrupt Table Size. These fields appear in the area indicated in the information on basic operations.

Code Segment Size. You can select the default code size: 32-bit or 16-bit. The default code size is 16 bit.

Interrupt Table. You can specify if the interrupt table is Real, Virtual, or Protected. (Selecting Virtual is equivalent to selecting Protected.) The default is Real.

Interrupt Table Address. You can specify the starting address of the interrupt table in hexadecimal. The default starting address is 0x00000000.

Interrupt Table Size. You can specify the size of the interrupt table in hexadecimal. The default size is 0x400.

Out-Of-Order Fetches

The i486 microprocessor can prefetch cycles out of ascending order. For example, a branch to address 1004 could cause the following sample of addresses across the bus: 1004, 1000, 100C, and 1008. The data at address 1004 is executed, but the data at address 1000 is not; it just fills the cache. The data at addresses 100C and 1008 are executed, but the data at address 1008 is executed before the data at 100C. The fetched order versus the executed order of this example is as follows:

Fetched Order	Executed Order
1004	1004
1000	1008
100C	100C
1008	

In the Hardware display format, the out-of-order fetches are displayed in the order they are fetched. They will be properly disassembled and identified by an asterisk to the left of the instruction.

In the Hardware display format, you can determine the executed order of the out-of-order fetches by looking at the address of the out-of-order cycles and subsequent cycles. Fetch cycles always have the sample number displayed.

Figure 2–2 shows an example of out-of-order fetches in the Hardware display format.

Sample	Address	Data	Mnemonic		Timestamp
223	0002605C	40E00000	(MEM READ)		240 ns
224	000264B0	00000010	(MEM READ)		490 ns
225	00026671	83FF33F6	XOR EDI,EDI	(32)	150 ns
	00026673	83FF33F6	ADD EDX,#04	(32)	
226	00026676	CDFE04C2	DECB CH	(32)	40 ns
227	00026678	5D03CB75	JNE 00026645	(32)	80 ns
228	0002667C	18558B08	(FLUSH)		50 ns
229	00026008	------00	(MEM READ)		150 ns
230	0002606C	41880000	(MEM WRITE)		320 ns
231	00026645	204D8A10	MOV CL,20[EBP]	(32)	200 ns
232	00026640	6D8A0000	(CACHE/BURST FILL)		50 ns
233	0002664C	00000004	*(EXTENSION)		70 ns
234	00026648	1D89EED9	FLDZ	(32)	40 ns
	0002664A	1D89EED9	MOV 00000004,EBX	(32)	
235	00026650	D83304D9	FLD [EBX][ESI]	(32)	160 ns
	00026653	D83304D9	FMUL [EDX][EDI]	(32)	
236	00026656	C1DE3A0C	FADDP ST(1),ST	(32)	50 ns
237	00026658	0304C683	ADD ESI,#04	(32)	70 ns
	0002665B	0304C683	ADD EDI,04[EBP]	(32)	
238	0002665E	C9FE047D	DECB CL	(32)	40 ns
239	000264CC	------02	(MEM READ)		160 ns
240	00026004	00000034	(MEM WRITE)		250 ns

Figure 2–2: Hardware display format with out-of-order fetches

In the Software display format, out-of-order fetches are displayed in the order they were executed. If the previous executed instruction had a larger sample number than the out-of-order fetch, the sample number will not be displayed. If the previous sample number is smaller than the out-of-order fetch, the sample number will be displayed. To mark an instruction without a sample number, you will have to change to the Hardware display format.

Figure 2–3 shows an example of out-of-order fetches in the Software display format.

Sample	Address	Data	Mnemonic		Timestamp
218	00026660	00080D02	ADD CL,00000008	(32)	160 ns
219	00026666	E8750000	JNE 00026650	(32)	40 ns
220	00026668	040518D9	FSTP [EAX]	(32)	90 ns
	0002666A	040518D9	ADD EAX,#00000004	(32)	
221	0002666F	33000000	XOR ESI,ESI	(32)	30 ns
225	00026671	83FF33F6	XOR EDI,EDI	(32)	1.040 us
	00026673	83FF33F6	ADD EDX,#04	(32)	
226	00026676	CDFE04C2	DECB CH	(32)	40 ns
227	00026678	5D03CB75	JNE 00026645	(32)	80 ns
231	00026645	204D8A10	MOV CL,20[EBP]	(32)	720 ns
234	00026648	1D89EED9	FLDZ	(32)	160 ns
	0002664A	1D89EED9	MOV 00000004,EBX	(32)	
235	00026650	D83304D9	FLD [EBX][ESI]	(32)	160 ns
	00026653	D83304D9	FMUL [EDX][EDI]	(32)	
236	00026656	C1DE3A0C	FADDP ST(1),ST	(32)	50 ns
237	00026658	0304C683	ADD ESI,#04	(32)	70 ns
	0002665B	0304C683	ADD EDI,04[EBP]	(32)	
238	0002665E	C9FE047D	DECB CL	(32)	40 ns
242	00026660	00080D02	ADD CL,00000008	(32)	720 ns
243	00026666	E8750000	JNE 00026650	(32)	40 ns
253	00026650	D83304D9	FLD [EBX][ESI]	(32)	1.440 us
	00026653	D83304D9	FMUL [EDX][EDI]	(32)	

Figure 2–3: Software display format with out-of-order fetches

Cache Invalidation Cycles

Cache Invalidation cycles are needed to keep the microprocessor's cache contents consistent with external memory. On a nonburst cycle that is also a Cache Invalidation cycle, the data and address will be valid as probed. On a burst cycle that is also a Cache Invalidation cycle, the data and the first address will be valid. In the remaining cycles of the burst, the data will be valid, but the address will not be valid as probed and the software will try to calculate the address from the surrounding cycles. A letter "c" to the left of the mnemonic indicates a Cache Invalidation cycle.

The disassembler assumes that the AHOLD signal is always used in cache invalidation protocol. If you use AHOLD to avoid contention on the address bus, then associated cycles may be mislabeled as Cache Invalidation cycles.

System Management Mode (SMM)

Some variations of the i486 microprocessor provide System Management Mode. This is a special mode where the CPU executes code from a separate, alternate memory space called SMRAM. The disassembler uses information from the SMIACT# signal to determine when the microprocessor is operating in SMM. When the disassembler detects that the microprocessor is operating in this mode, it displays an "SMM" to the right of the mnemonic.

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it to one of the following cycle types:

- Opcode (the first byte of an instruction)
- Extension (a subsequent byte of an instruction)
- Flush (an opcode or extension that is fetched but not executed)
- Any (any valid opcode, extension, or flush)
- 16-bit or 32-bit default segment size

Mark selections for a 32-bit bus are as follows:

```
Any          Any          Any          OPCODE
Any          Any          OPCODE       Any
Any          OPCODE       Any          Any
OPCODE       Any          Any          Any
Ext          Ext          Ext          Ext
Flush        Flush        Flush        Flush

16-bit Default Segment Size
32-bit Default Segment Size

Undo marks on this cycle
```

Mark selections for a 16-bit bus are as follows:

```
Any          OPCODE
OPCODE       Any
Ext          Ext
Flush        Flush

16-bit Default Segment Size
32-bit Default Segment Size

Undo marks on this cycle
```

Mark selections for an 8-bit bus are as follows:

```
OPCODE
Ext
Flush

16-bit Default Segment Size
32-bit Default Segment Size

Undo marks on this cycle
```

You can also use the F4: Mark Cycle key to specify the default segment size mode (16-bit or 32-bit) for the cycle. The segment size selection changes the cycle the cursor is on and the remaining cycles to the end of memory or to the next mark.

The default segment size of a cycle is independent of any prefix override bytes in that particular fetch. For example, if you mark a cycle with a default size of 32 bits, but there are address/operand override prefixes in the instruction, the default size will be 32-bits but the size of the instruction will be 16 bits.

If the Disassembly menu is set up for Software format, and an out-of-order fetch does not have a sample number, you must change to the Hardware format to mark that sample.

You can only make one selection at a time. If you decide to mark an opcode and the default size of a cycle, you must do them in separate steps.

Displaying Exception Vectors

The disassembler can display i486 exception vectors. You can select to display the interrupt vectors for Real, Virtual, or Protected mode in the Interrupt Table field. (Selecting Virtual is equivalent to selecting Protected.)

You can relocate the table by entering the starting address in the Interrupt Table Address field. The Interrupt Table Address field provides the disassembler with the offset address; enter an eight-digit hexadecimal value corresponding to the offset of the base address of the exception table. The Interrupt Table Size field lets you specify a three-digit hexadecimal size for the table.

You can make these selections in the Disassembly property page (the Disassembly Format Definition overlay).

Interrupt cycle types are computed and cannot be used to control triggering. When the i486 microprocessor processes an interrupt, the disassembler software displays the type of interrupt, if known.

Table 2–4 lists the i486 exception vectors for the Real Addressing mode.

Table 2–4: Interrupt vectors for Real Addressing mode

Exception number	Location in IV* table (in hexadecimal)	Displayed interrupt name
0	0000	DIVIDE ERROR
1	0004	DEBUG EXCEPTIONS
2	0008	NMI INTERRUPT
3	000C	BREAKPOINT INTERRUPT
4	0010	INTO DETECTED OVERFLOW
5	0014	BOUND RANGE EXCEEDED
6	0018	INVALID OPCODE
7	001C	COPROCESSOR NOT AVAILABLE
8	0020	INTERRUPT TABLE LIMIT TOO SMALL
9-11	0024-002C	RESERVED
12	0030	STACK EXCEPTION
13	0034	SEGMENT OVERRUN
14-15	0038-003C	RESERVED
16	0040	COPROCESSOR MODE ERROR
17-31	0044-007C	RESERVED
32-255	0080-03FC	USER DEFINED

*** IV means interrupt vector.**

Table 2–5 lists the i486 exception vectors for the Protected Addressing mode.

Table 2–5: Interrupt vectors for Protected Addressing mode

Exception number	Location in IDT* (in hexadecimal)	Displayed interrupt name
0	0000	DIVIDE ERROR
1	0008	DEBUG EXCEPTIONS
2	0010	NMI INTERRUPT
3	0018	BREAKPOINT INTERRUPT
4	0020	INTO DETECTED OVERFLOW
5	0028	BOUND RANGE EXCEEDED
6	0030	INVALID OPCODE
7	0038	DEVICE NOT AVAILBLE
8	0040	DOUBLE FAULT
9	0048	RESERVED

Table 2–5: Interrupt vectors for Protected Addressing mode (cont.)

Exception number	Location in IDT* (in hexadecimal)	Displayed interrupt name
10	0050	INVALID TSS
11	0058	SEGMENT NOT PRESENT
12	0060	STACK EXCEPTION
13	0068	GENERAL PROTECTION
14	0070	PAGE FAULT
15	0078	RESERVED
16	0080	COPROCESSOR MODE
17	0088	ALIGNMENT CHECK
18-31	0090-00F8	RESERVED
32-255	0100-07F8	USER DEFINED

*** IDT means interrupt descriptor table.**

Figure 2–4 shows the display of an interrupt mnemonic. Sample 849 shows an INT 33 instruction. Samples 867 and 868 show the associated table read. All INT # instructions are displayed with decimal numbers as indicated by a following `t`.

```
  Sample  Address   Data        Mnemonic                                Timestamp
-------------------------------------------------------------------------------
     849  000265A9  3321CD01    INT 33t                    (32)          80 ns
     850  000265AC  33DB33C0    ( FLUSH )                                40 ns
     851  000264D4  ----0014    ( MEM READ )                          1.000 us
     852  000265B0  33D233C9    ( FLUSH )                               160 ns
     853  000265B4  33F633ED    ( FLUSH )                                40 ns
     854  000265B8  0000C3FF    ( FLUSH )                                80 ns
     855  000265BC  00000000    ( FLUSH )                                40 ns
     856  0001D930  00469310    ( MEM READ )                            320 ns
     857  0001D92C  00008FFF    ( MEM READ )                            200 ns
     858  000264D8  ----0014    ( MEM READ )                            440 ns
     859  0001D930  00469310    ( MEM READ )                            440 ns
     860  0001D92C  00008FFF    ( MEM READ )                            200 ns
     861  000264DC  ----0014    ( MEM READ )                            440 ns
     862  0001D930  00469310    ( MEM READ )                            440 ns
     863  0001D92C  00008FFF    ( MEM READ )                            200 ns
     864  000264E0  ----0014    ( MEM READ )                            440 ns
     865  0001D930  00469310    ( MEM READ )                            440 ns
     866  0001D92C  00008FFF    ( MEM READ )                            200 ns
     867  0001D030  00008E00    ( USER DEFINED ) (33)                   720 ns
     868  0001D02C  000813E0    ( USER DEFINED)  (33)                    200 ns
     869  0001D7D0  00409B00    ( MEM READ )                            520 ns
```

Figure 2–4: Display of an INT 33 instruction

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your i486 microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your SUT.

Information on basic operations describes how to view the file.

Specifications

Specifications

This chapter contains the following information:

- Probe adapter description
- Specification tables
- Dimensions of the probe adapter
- Channel assignment tables
- Description of how the module acquires i486 signals
- List of other accessible i486 signals and extra acquisition channels

Probe Adapter Description

The probe adapter is a nonintrusive piece of hardware that allows the acquisition module to acquire data from a i486 microprocessor in its own operating environment with little affect, if any, on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and a socket for a i486 microprocessor. The probe adapter connects to the microprocessor in the SUT. Signals from the microprocessor-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

Circuitry on the probe adapter can be powered from the SUT or an external power source. Refer to *Applying and Removing Power* in the *Getting Started* chapter for information on using an external power source.

The probe adapter accommodates the Intel i486 microprocessor in a 168-pin PGA package.

Configuring the Probe Adapter

Refer to *Configuring the Probe Adapter* in the *Getting Started* section for information on jumpers and settings.

Specifications

In Table 3–1, for the 102/136-channel module, one podlet load is 20 kΩ in parallel with 2 pF. For the 96-channel module, one podlet load is 100 kΩ in parallel with 10 pF.

Table 3–1: Electrical specifications

Characteristics	Requirements	
SUT DC power requirements		
Voltage	4.75-5.25 VDC	
Current	I max (calculated) 210 mA I typ (measured) 140 mA	
Probe adapter power supply requirements*		
Voltage	90-265 VAC	
Current	1.1 A maximum at 100 VAC	
Frequency	47-63 Hz	
Power	25 W maximum	
SUT clock		
Clock rate	Min. DC Max. 50 MHz	
Minimum setup time required		
D31-D0	5 ns†	
BOFF#	6.5 ns†	
All other signals	5 ns	
Minimum hold time required		
All signals	0 ns	
	Specification	
	AC load	**DC load**
Measured typical SUT signal loading		
CLK	21 pF + 2 podlets	21 pF + 100 Ω + 2 podlets
A31-A0	6 pF + 1 podlet	1 podlet
BE3#-BE0#	13 pF + 1 podlet	1 podlet
RDY#, BRDY#‡	6 pF + 1 podlet	1 podlet
NC/BRDYC#‡	8 pF + 1 podlet	1 podlet
D31-D0, AHOLD, HLDA, BLAST#, D/C#, M/IO#, W/R#, ADS#, BS8#, BS16#, BOFF#	5 pF + 1 podlet	1 podlet
SMIACT#	6 pF	1 podlet + 10 K

Table 3–1: Electrical specifications (cont.)

Characteristics	Requirements	
KEN#‡	6 pF	10 K
RESET, NMI, SRESET, HOLD, FLUSH#, IGNNE#, PLOCK#_LEN, EADS#, LOCK#, BREQ#, INTR‡	6 pF	
PCHK#, A20M#, DP3-DP0, TD1, TD0, TMS, TCK§	6 pF	

*** A power supply is available and can be used as an alternate power source. Refer to *Applying and Removing Power* in the *Getting Started* chapter for more information.**

† **This requirement is greater than that of the i486 microprocessor.**

‡ **Signals will have an additional podlet load if you connect probes to the C0 or C1 square pins on the i486 probe adapter.**

§ **Connected to J370; loading is the run capacitance on the i486 probe adapter board.**

Table 3–2: Environmental specification*

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F)†
Minimum operating	0° C (+32° F)
Non-operating	–55° C to +75° C (–67° to +167° F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

*** Designed to meet Tektronix standard 062-2847-00 class 5.**

† **Not to exceed i486 microprocessor thermal considerations. Forced air cooling might be required across the CPU.**

Table 3–3: Certifications and compliances

EC Compliance	There are no current European Directives that apply to this product.
Pollution Degree 2	Do not operate in environments where conductive pollutants might be present.

Figure 3–1 shows the dimensions of the probe adapter. Information on basic operations shows the vertical clearance of the channel and clock probes when connected to a probe adapter in the description of general requirements and restrictions.

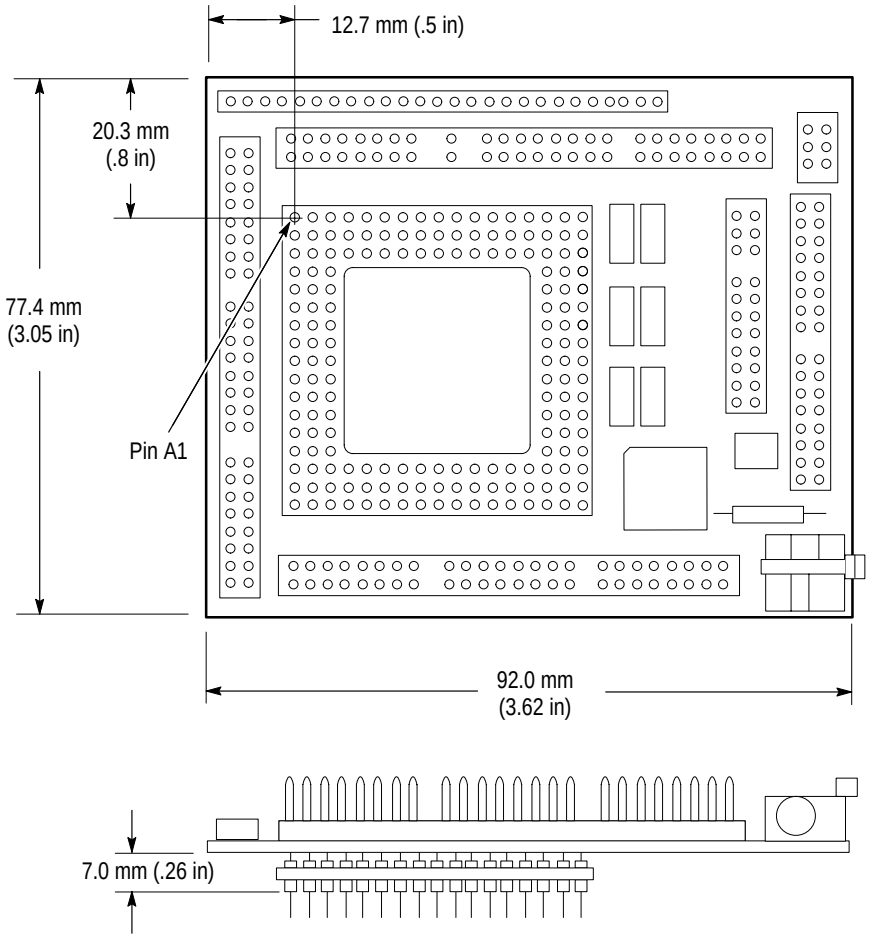


Figure 3–1: Minimum clearance of the probe adapter

Channel Assignments

Channel assignments shown in Table 3–4 through Table 3–11 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for the 102/136-channel, and 96-channel unless otherwise noted.
- A pound sign (#) following a signal name indicates an active low signal.
- An equals sign (=) following a signal name indicates that it is double probed.

Table 3–4 shows the probe section and channel assignments for the Address group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–4: Address group channel assignments

Bit order	Section:channel	i486 signal name
31	A3:7	A31
30	A3:6	A30
29	A3:5	A29
28	A3:4	A28
27	A3:3	A27
26	A3:2	A26
25	A3:1	A25
24	A3:0	A24
23	A2:7	A23
22	A2:6	A22
21	A2:5	A21
20	A2:4	A20
19	A2:3	A19
18	A2:2	A18
17	A2:1	A17
16	A2:0	A16
15	A1:7	A15
14	A1:6	A14
13	A1:5	A13
12	A1:4	A12
11	A1:3	A11
10	A1:2	A10
9	A1:1	A9
8	A1:0	A8
7	A0:7	A7
6	A0:6	A6
5	A0:5	A5
4	A0:4	A4
3	A0:3	A3
2	A0:2	A2
1	A0:1	A1*
0	A0:0	A0*

*** Signals synthesized depending on jumper position of J421; refer to *Configuring the Probe Adapter* in the *Getting Started* chapter for more information; signals are not required for disassembly.**

Table 3–5 shows the probe section and channel assignments for the Data group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–5: Data group channel assignments

Bit order	Section:channel	i486 signal name
31	D3:7	D31
30	D3:6	D30
29	D3:5	D29
28	D3:4	D28
27	D3:3	D27
26	D3:2	D26
25	D3:1	D25
24	D3:0	D24
23	D2:7	D23
22	D2:6	D22
21	D2:5	D21
20	D2:4	D20
19	D2:3	D19
18	D2:2	D18
17	D2:1	D17
16	D2:0	D16
15	D1:7	D15
14	D1:6	D14
13	D1:5	D13
12	D1:4	D12
11	D1:3	D11
10	D1:2	D10
9	D1:1	D9
8	D1:0	D8
7	D0:7	D7
6	D0:6	D6
5	D0:5	D5
4	D0:4	D4
3	D0:3	D3
2	D0:2	D2
1	D0:1	D1
0	D0:0	D0

Table 3–6 shows the probe section and channel assignments for the Control group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–6: Control group channel assignments

Bit order	Section:channel	i486 signal name
7	C2:2	BLAST#
6	C2:7	AHOLD
5	C2:3	HLDA
4	C2:0	BOFF#
3	C3:1	M/IO#
2	C3:5	D/C#
1	C2:5	W/R#
0	C2:4	SMIACT#

Table 3–7 shows the probe section and channel assignments for the DataSize group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–7: DataSize group channel assignments

Bit order	Section:channel	i486 signal name
5	C3:4	BS8#
4	C3:0	BS16#
3	C3:2	BE3#
2	C3:6	BE2#
1	C3:3	BE1#
0	C2:6	BE0#

Table 3–8 shows the probe section and channel assignments for the Misc group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–8: Misc group channel assignments

Bit order	Section:channel	i486 signal name
1	C3:7	CLK=*
0	C2:1	ADS#

*** Signal not required for disassembly.**

Table 3–9 shows the probe section and channel assignments for the Cache group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–9: Cache group channel assignments

Bit order	Section:channel	i486 signal name
2	C0:2	KEN#*
1	C0;5	EADS#*
0	C1:6	FLUSH#*

*** Signal not required for disassembly.**

Table 3–10 shows the probe section and channel assignments for the Misc2 group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–10: Misc2 group channel assignments

Bit order	Section:channel	i486 signal name
12	C1:4	BREQ#*
11	C1:3	INTR#*
10	C0:1	LOCK#*
9	C1:5	PLOCK#*
8	C0:0	RDY#=*
7	C1:1	BRDY#=*
6	C1:0	BRDYC#=*
5	C0:3	HOLD*

Table 3–10: Misc2 group channel assignments (cont.)

Bit order	Section:channel	i486 signal name
4	C0:6	IGNNE#*
3	C1:2	FERR#*
2	C1:7	RESET#*
1	C0:4	SRESET#*
0	C0:7	NMI*

*** Signal not required for disassembly.**

Table 3–11 shows the probe section and channel assignments for the clock probes (not part of any group), and the i486 signal to which each channel connects.

Table 3–11: Clock channel assignments

Section:channel	CLK or QUAL	i486 signal name
CLK:3	CLK	CLK=
CLK:2	QUAL	RDY#
CLK:1	QUAL	BRDY#
CLK:0	QUAL	BRDYC#

These channels are used only to clock in data; they are not acquired or displayed. To acquire data from any of the signals shown in Table 3–11, you must connect another channel probe to the signal, called double probing. An equals sign (=) following a signal name indicates that it is already double probed.

How Data is Acquired

This part of this chapter explains how the module acquires i486 signals using the TMS 107 support and probe adapter. This part also provides additional information on microprocessor signals accessible on or not accessible on the probe adapter, and on extra acquisition channels available for you to use for additional connections.

Custom Clocking

A special clocking program is loaded to the module every time you select the microprocessor support. This special clocking is called Custom.

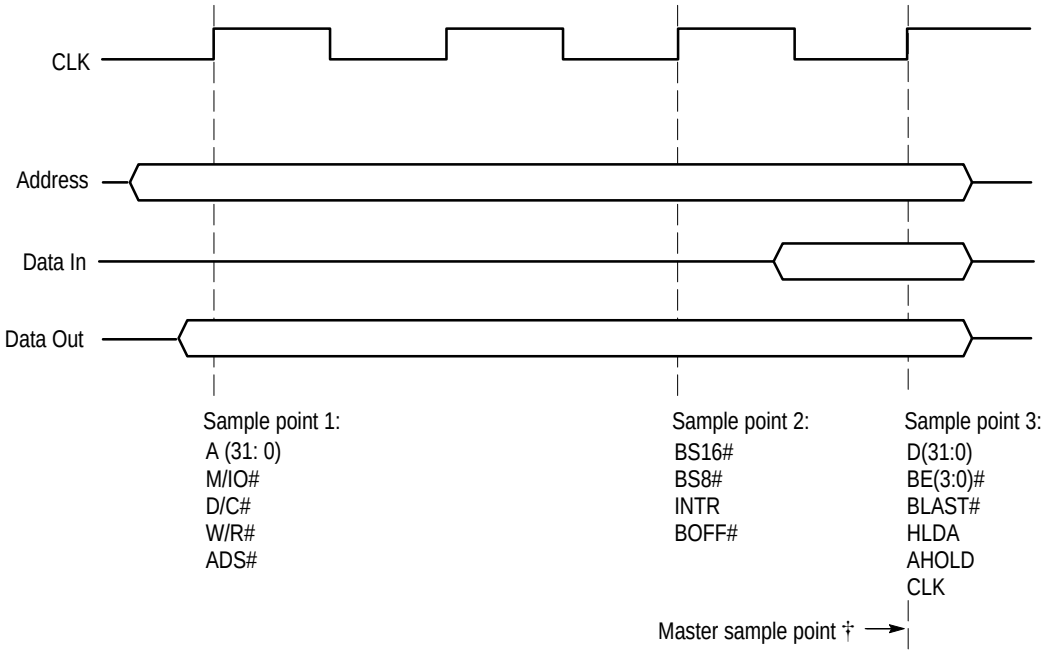
(For the 102/136-channel module, from the File menu, select Load Support Package, and 486. For the 96-channel module, select 486 Support in the Configuration menu.)

With Custom clocking, the module logs in signals from multiple groups of channels at different times when they are valid on the i486 bus. The module then sends all the logged-in signals to the trigger machine and to the acquisition memory of the module for storage.

In Custom clocking, the module clocking state machine (CSM) generates one master sample for each i486 bus cycle, no matter how many clock cycles are contained in the bus cycle.

Figure 3–2 shows the sample points and the master sample point.

The disassembler waits for the ADS# signal to be asserted. When asserted, the address value and some control signals are logged in. The disassembler then waits for any RDY# signal to be asserted. When one of the three RDY# signals is asserted, the data and some control signals are logged in, and the disassembler waits for the ADS# signal to be asserted again.



† Channels not set up in a channel group by the TMS 107 software are logged with the Master sample.

Figure 3–2: i486 Bus Timing

Clocking Options

The clocking algorithm for the i486 support has two variations: Alternate Bus Master Cycles Excluded, and Alternate Bus Master Cycles Included.

Alternate Bus Master Cycles Excluded. Whenever the HLDA signal is high, no bus cycles are logged in. Only bus cycles initiated by the i486 microprocessor (HLDA low) will be logged in. Backoff cycles (caused by the BOFF# signal) are stored.

Alternate Bus Master Cycles Included. All bus cycles, including Alternate Bus Master cycles and Backoff cycles, are logged in.

When the HLDA signal is high, the i486 microprocessor has given up the bus to an alternate device. The design of the i486 system affects what data will be logged in. The module only samples the data at the pins of the i486 microprocessor. To properly log in bus activity, any buffers between the i486 microprocessor and the alternate bus master must be enabled and pointing at the i486 microprocessor.

There are three possible i486 system designs and clocking interactions when an alternate bus master has control of the bus. The three different possibilities are listed below (in each case, the HLDA signal is logged in as a high level):

- If the alternate bus master drives the same control lines as the i486 microprocessor, and the i486 microprocessor “sees” these signals, the bus activity is logged in like normal bus cycles except that the HLDA signal is high.
- If none of the control lines are driven or if the i486 microprocessor can not see them, the module will still clock in an alternate bus master cycle. The information on the bus, one clock prior to the HLDA signal going low, is logged in. If the ADS# signal goes low on the same clock when the HLDA signal goes low, the address that gets logged in will be the “next address,” not the address that occurred one clock before the HLDA signal went low.
- If some of the i486 microprocessor control lines are visible (but not all), the module logs in what it determines is valid from the control signals and logs in the remaining bus signals one clock cycle prior to the HLDA signal going low. If the ADS# signal goes low on the same clock that the HLDA signal goes low, the “next address” will be logged in instead of the previously saved address.

When the BOFF# signal goes low (active), a backoff cycle has been requested, and the i486 microprocessor gives up the bus on the next clock cycle. The module aborts the bus cycle that it is currently logging in (the i486 microprocessor will restart this cycle once the BOFF# signal goes high). A backoff cycle will be logged in using one of the three interactions described for the HLDA signal (except that the BOFF# signal is stored as a low-level signal in each of the cases).

Alternate Microprocessor Connections

You can connect to microprocessor signals that are not required by the support so you can do more advanced timing analysis. These signals might or might not be accessible on the probe adapter board. The following paragraphs and tables list signals that are or are not accessible on the probe adapter board.

For a list of signals required or not required for disassembly, refer to the channel assignment tables beginning on page 3–5. Remember that these channels are already included in a channel group. If you do connect these channels to other signals, you should set up another channel group for them.

Signals On the Probe Adapter

The probe adapter board contains pins for microprocessor signals that are not acquired by the TMS 107 support. You can connect extra channels to these pins, because they can be useful for general purpose analysis.

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.

Table 3–12 shows the microprocessor signals available on J335 of the probe adapter.

Table 3–12: i486 signals on J335

Pin no.	Signal name	Pin no.	Signal name
1	GND	12	B13
2	BHE#*	13	A12
3	PCD	14	B12
4	PWT	15	A10
5	A20M#	16	GND
6	GND	17	NC_SMI#
7	PCHK#	18	NC_STPCLK#
8	NC_TDO	19	NC_UP#
9	NC_TD1	20	NC_TCK
10	NC_MP#_UP#_TMS	21	GND
11	GND	22	DP3

*** Signal generated on the probe adapter.**

Table 3–13 shows the microprocessor signals available on J130 of the probe adapter.

Table 3–13: i486 Signals on J130

Pin No.	Signal Name	Pin No.	Signal Name
1	DP2	3	DP0
2	DP1	4	GND

Extra Channels

Table 3–14 lists extra sections and channels that are left after you have connected all the probes used by the support. You can use these extra channels to make alternate SUT connections.

Table 3–14: Extra module sections and channels

Module	Section: channels
102-channels	C1:7-0, C0:7-0, D3:7-0, D2:7-0
136-channels	C1:7-0, C0:7-0, D3:7-0, D2:7-0, E3:7-0, E2:7-0, E1:7-0, E0:7-0
96-channels	C1:7-0, C0:7-0, D3:7-0, D2:7-0

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Maintenance

Maintenance

This section contains information on the following topics:

- Probe adapter circuit description
- How to replace a fuse

Probe Adapter Circuit Description

The probe adapter has a PAL (U420) that synthesizes the A0, A1, and BHE# signals. A jumper on the probe adapter, J421, can be used to disable the synthesis of these signals. When disabled, both signals connect to ground and will always have the value of 00. You should not synthesize these signals if your SUT operates at or above 50 MHz.

If your SUT operates at or above 50 MHz, the TMS 107 probe adapter does not have enough time to synthesize A1 and A0 before the entire address is logged in by the logic analyzer. In this case, the value of A1 and A0 is unpredictable. To make the value predictable, you should disable the synthesis of A1 and A0. To do this, position J421 on pins 1 and 2.

Replacing Signal Leads

Information on basic operations describes how to replace signal leads (individual channel and clock probes).

Replacing Protective Sockets

Information on basic operations describes how to replace protective sockets.

Replacing the Fuse

If the fuse on the i486 probe adapter board burns out, you can replace it with a 1.5 Amp, 125 V fuse. Figure 4–1 shows the location of the fuse on the probe adapter board.

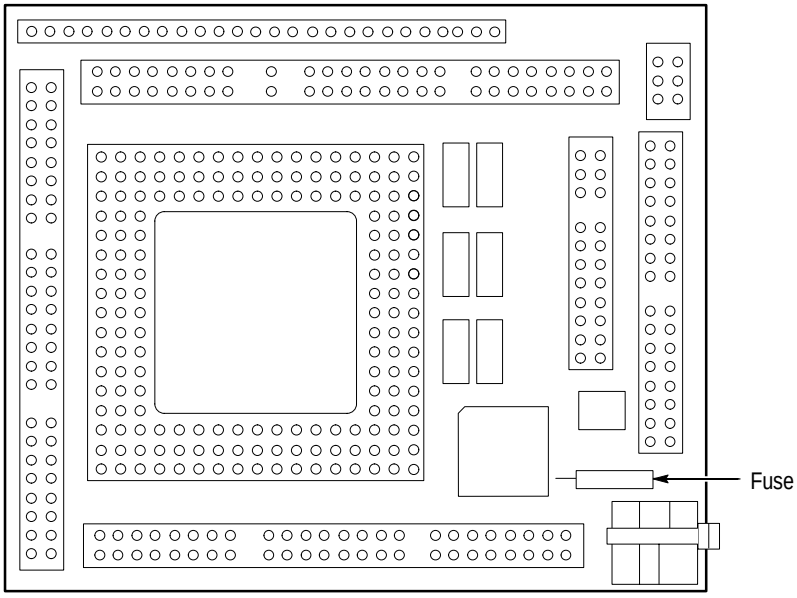


Figure 4–1: Location of the fuse

Replaceable Electrical Parts

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 107 i486 microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

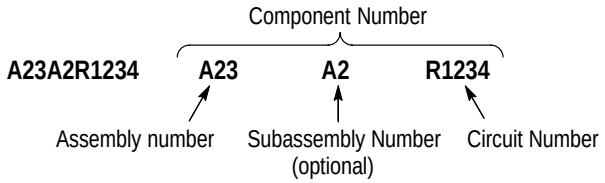
Parts list column descriptions

Column	Column name	Description
1	Component number	The component number appears on diagrams and circuit board illustrations, located in the diagrams section. Assembly numbers are clearly marked on each diagram and circuit board illustration in the *Diagrams* section, and on the mechanical exploded views in the *Replaceable Mechanical Parts* list section. The component number is obtained by adding the assembly number prefix to the circuit number (see Component Number illustration following this table). The electrical parts list is arranged by assemblies in numerical sequence (A1, with its subassemblies and parts, precedes A2, with its subassemblies and parts). Chassis-mounted parts have no assembly number prefix, and they are located at the end of the electrical parts list.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
6	Mfr. code	This indicates the code number of the actual manufacturer of the part.
7	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Component Number



Read: Resistor 1234 (of Subassembly 2) of Assembly 23

List of Assemblies

A list of assemblies is located at the beginning of the electrical parts list. The assemblies are listed in numerical order. When a part's complete component number is known, this list will identify the assembly in which the part is located.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
TK0875	MATSUO ELECTRONICS INC	831 S DOUBLAS ST	EL SEGUNDO CA 92641
TK2427	A/D ELECTRONIC	2121 17TH AVE SE	BOTHELL WA 97021
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
04222	AVX CERAMICS DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
26742	METHODE ELECTRONICS INC	7447 W WILSON AVE	CHICAGO IL 60656–4548
50139	ALLEN–BRADLEY CO ELECTRONIC COMPONENTS	1414 ALLEN BRADLEY DR	EL PASO TX 79936
50434	HEWLETT–PACKARD CO OPTOELECTRONICS DIV	370 W TRIMBLE RD	SAN JOSE CA 95131–1008
53387	MINNESOTA MINING MFG CO	PO BOX 2963	AUSTIN TX 78769–2963
58050	TEKA PRODUCTS INC	45 SALEM ST	PROVIDENCE RI 02907
61857	SAN–0 INDUSTRIAL CORP	91–3 COLIN DRIVE	HOLBROOK NY 11741
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A01	671–3013–00			CIRCUIT BD ASSY:80486,PROBE ADAPTER	80009	671301300
A01C130	283–5003–00			CAP,FXD,CERAMIC:MLC;0.01UF,10%,50V,X7R,1206	04222	12065C103KAT1A
A01C200	283–5003–00			CAP,FXD,CERAMIC:MLC;0.01UF,10%,50V,X7R,1206	04222	12065C103KAT1A
A01C201	283–5003–00			CAP,FXD,CERAMIC:MLC;0.01UF,10%,50V,X7R,1206	04222	12065C103KAT1A
A01C230	283–5003–00			CAP,FXD,CERAMIC:MLC;0.01UF,10%,50V,X7R,1206	04222	12065C103KAT1A
A01C300	283–5003–00			CAP,FXD,CERAMIC:MLC;0.01UF,10%,50V,X7R,1206	04222	12065C103KAT1A
A01C330	283–5187–00			CAP,FXD,CERAMIC:MLC;15PF,5%,100V,NPO,1206	04222	12061A0150JAT1A
A01C331	283–5003–00			CAP,FXD,CERAMIC:MLC;0.01UF,10%,50V,X7R,1206	04222	12065C103KAT1A
A01C400	283–5003–00			CAP,FXD,CERAMIC:MLC;0.01UF,10%,50V,X7R,1206	04222	12065C103KAT1A
A01C410	283–5003–00			CAP,FXD,CERAMIC:MLC;0.01UF,10%,50V,X7R,1206	04222	12065C103KAT1A
A01C415	283–5003–00			CAP,FXD,CERAMIC:MLC;0.01UF,10%,50V,X7R,1206	04222	12065C103KAT1A
A01C510	290–5005–00			CAP,FXD,TANT:47UF,10%,10V,SMD,T&R	TK0875	267M–1002–476–K
A01CR415	152–5045–00			DIODE,SIG:SCHTKY,;20V,1.2PF,24 OHM	50434	HSMS–2810–T31
A01CR510	152–5045–00			DIODE,SIG:SCHTKY,;20V,1.2PF,24 OHM	50434	HSMS–2810–T31

Replaceable electrical parts list (cont.)

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A01F500	159–0153–00			FUSE,WIRE LEAD:1.5A,125V,FAST BLOW,	61857	SP5–1.5A DI
A01J120	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	N–2480–6122–TB
A01J130	131–1857–00			CONN,HDR:PCB,;MALE,STR,1 X 36,0.1 CTR,0.230	58050	082–3644–SS10
A01J200	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	N–2480–6122–TB
A01J330	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	N–2480–6122–TB
A01J335	131–1857–00			CONN,HDR:PCB,;MALE,STR,1 X 36,0.1 CTR,0.230	58050	082–3644–SS10
A01J420	131–4530–00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION	00779	104344–1
A01J421	131–4530–00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION	00779	104344–1
A01J422	131–4530–00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION	00779	104344–1
A01J423	131–4530–00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION	00779	104344–1
A01J430	131–4530–00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION	00779	104344–1
A01J431	131–4530–00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION	00779	104344–1
A01J520	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	N–2480–6122–TB
A01J530	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	N–2480–6122–TB
A01J650	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	N–2480–6122–TB
A01JR500	—— ——			JACK,POWER DC:PCB,;MALE,RTANG,2.0 MM DIA PIN,7 MM H X 3.3 MM TAIL,3 COND,W/SWITCH, MTGPOST,DC PWR JACK,1 AMP@12V (SEE FIQURE1 MPL)		
A01P420	—— ——			CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X 2,0.1 (SEE FIGURE 1 MPL)		
A01P421	—— ——			CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X 2,0.1 (SEE FIGURE 1 MPL)		
A01P422	—— ——			CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X 2,0.1 (SEE FIGURE 1 MPL)		
A01P423	—— ——			CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X 2,0.1 (SEE FIGURE 1 MPL)		
A01P430	—— ——			CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X 2,0.1 (SEE FIGURE1 MPL)		
A01P431	—— ——			CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X 2,0.1 (SEE FIGURE1 MPL)		
A01R330	321–5006–00			RES,FXD:THICK FILM;100 OHM,1%,0.125W,TC=100	50139	BCK1000FT
A01R420	321–5030–00			RES,FXD:THICK FILM;10.0K OHM,1%,0.125W, TC=100 PPM	50139	BCK1002FT

Replaceable electrical parts list (cont.)

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A01R421	321–5030–00			RES,FXD:THICK FILM;10.0K OHM,1%,0.125W, TC=100 PPM	50139	BCK1002FT
A01R422	321–5030–00			RES,FXD:THICK FILM;10.0K OHM,1%,0.125W, TC=100 PPM	50139	BCK1002FT
A01R423	321–5030–00			RES,FXD:THICK FILM;10.0K OHM,1%,0.125W, TC=100 PPM	50139	BCK1002FT
A01R430	321–5030–00			RES,FXD:THICK FILM;10.0K OHM,1%,0.125W, TC=100 PPM	50139	BCK1002FT
A01U410	160–9734–00			IC,DIGITAL:STTL,PLD;PAL,16L8,4.5NS,210MA,PRGM	80009	160–9734–00

Replaceable Mechanical Parts

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 107 i486 microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order.

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
TK2427	A/D ELECTRONIC	2121 17TH AVE SE	BOTHELL WA 97021
OB445	ELECTRI–CORD MFG CO INC	312 EAST MAIN ST	WESTFIELD PA 16950
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
14310	AULT INC	7300 BOONE AVENUE NORTH	MINNEAPOLIS MN 55428
26742	METHODE ELECTRONICS INC	7447 W WILSON AVE	CHICAGO IL 60656–4548
53387	MINNESOTA MINING MFG CO	PO BOX 2963	AUSTIN TX 78769–2963
58050	TEKA PRODUCTS INC	45 SALEM ST	PROVIDENCE RI 02907
61857	SAN–0 INDUSTRIAL CORP	91–3 COLIN DRIVE	HOLBROOK NY 11741
63058	MCKENZIE TECHNOLOGY	910 PAGE AVENUE	FREMONT CA 94538
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
1–0	010–0571–00			1	PROBE ADAPTER:80486,PGA168,SOCKETED;	80009	010057100
–1	——— ———			1	CONN,HDR PCB,:MAILE, STR, 1 X 36, 0.1 CTR,O.230 MLG X 0.100 TAIL, GOLD (SEE EPL J130,J335)	58050	082–3644–SS10
–2	131–4530–00			6	CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION (SEE EPL J420,J421,J422,J423,J430,J431)	00779	104344–1
–3	131–4356–00			6	CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X 2,0.1CTR, 0.630 H,BLK,W/HANDLE,JUMPER (P420,P421,P422,P423,P430,P431)	26742	9618–302–50
–4	343–0549–00			1	STRAP,TIEDOWN,E0.098 W X 4.0L,ZXTEL	06383	PLT1M
–5	——— ———			1	FUSE,WIRE LEAD:1.5A,125V,FAST BLOW, (SEE EPL F500)	61857	SP5–1.5A DI
–6	131–5148–00			1	JACK,POWER DC:PCB,;MALE,RTANG,2.0 MM DIA PIN,7 MM H X 3.3 MM TAIL,3 COND,W/SWITCH, MTGPOST,DC PWR JACK,1 AMP@12V (JR500)	TK2427	SCD–016
–7	671–3013–00			1	CIRCUIT BD ASSY:80846,PROBE ADAPTER, PGA168SOCKETED	80009	671301300
–8	136–1250–00			2	SOCKET,PGA:PCB;168 POS,17 X 17 MATRIX,0.1 CTR,0.173 H X 0.183 TAIL,GOLD,PHOS BRZ,PAT 1706 W/O CHAMFER,PAT 1769 (U320)	63058	PGA–168H–101B–1
–9	131–5267–00			3	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD (SEE EPL J120,J200,J330,J520,J530,J650)	53387	N–2480–6122–TB
					STANDARD ACCESSORIES		
	070–9810–00			1	MANUAL,TECH:INSTRUCTION,486,DISSASEMBLER,TMS107	80009	070–9810–00
	070–9803–00			1	MANUAL, TECH:TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070–9803–00
	119–5061–01			1	POWER SUPPLY:25W,5V 5A,CONCENTRIC 2MM,90–265V,47–63HZ (NOT SHOWN)	14310	SW106KA002F01
	161–0104–00			1	CA ASSY,PWR:3,18 AWG,98 L,250V/10AMP,98 INCH, RTANG,IEC320,RCPT X STR,NEMA 15–5P,W/CORD GRIP	S3109	ORDER BY DESCRIPTION

Replaceable mechanical parts list (cont.)

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					OPTIONAL ACCESSORIES		
	070–9802–00			1	MANUAL, TECH:BASIC OPS MICRO SUP ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070–9802–00
	161–0104–06			1	CA ASSY,PWR:3,1.0MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, EUROPEAN,SAFETY CONTROLLED (OPT A1)	S3109	ORDER BY DESCRIPTION
	161–0104–07			1	CA ASSY,PWR:3,1.0MM SQ,240V/10AMP,2.5 METER, RTANG,IEC320,RCPT X 13A, FUSED, UK PLUG, (13A FUSE), UNITED KINGDOM,SAFETY CONTROL (OPT A2)	S3109	ORDER BY DESCRIPTION
	161–0104–05			1	CA ASSY,PWR:3,1.0MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, AUSTRALIA,SAFETY CONTROLLED (OPT A3)	S3109	ORDER BY DESCRIPTION
	161–0167–00			1	CA ASSY,PWR:3,0.75MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, SWISS,NO CORD GRIP, SAFETY CONTROLLED (OPT A5)	S3109	ORDER BY DESCRIPTION

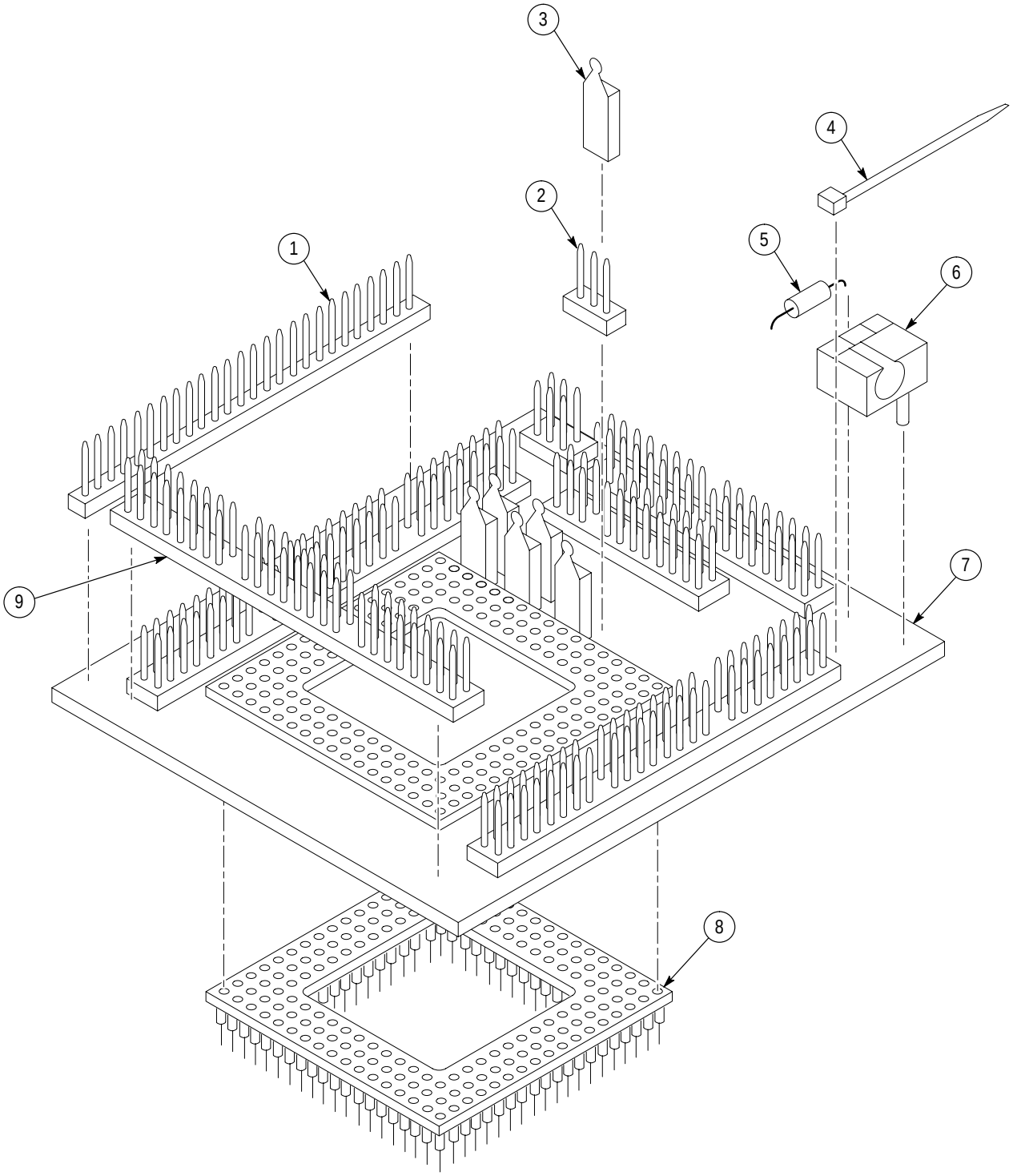


Figure 1: 486 probe adapter exploded view

Appendix

Appendix A: 486 Variations

486DX Chip-Set Mode

The 486DX microprocessor, 82495DX cache controller, and the 82490DX SRAM can be combined to form a chip set or enhanced design. The behavior of the 486DX microprocessor is affected when operating in Chip-Set mode. The TMS 107 software and probe adapter supports the 486DX in this mode.

In Chip-Set mode, there are two new signals: BRDYC# and LEN#.

In normal mode, BRDYC# is seen as a “no connect” pin. The TMS 107 probe adapter uses the BRDYC# signal for clocking when it is active. The probe adapter has a pullup resistor on this line to hold it inactive when the 486DX is in Chip-Set mode. The BRDYC# signal can be probes on C1:0.

The PLOCK# signal is renamed LEN in Chip-Set mode. LEN is not used for clocking by the TMS 107 or for disassembly. You should also be aware that the trace in the Timing menu will always be labeled PLOCK#. The PLOCK# (LEN) signal can be probed on C1:5.

486DX2

The 486DX2 microprocessor is basically a 486DX core which runs at twice the frequency of the input clock. It also has a System Management Mode (SMM) and an Upgrade Power Down mode.

Signal differences between the 486DX and 486DX2 microprocessors are:

486DX	486DX2	Pin Number
NC	SMI#	B10
NC	SMIACT#	C12
NC	UP#	C11

These signals are not used for clocking or disassembly. When the probe adapter is connected using the procedure in this manual, the software disassembles correctly. The SMIACT# signal is probed on C2:4.

486SX

Signal differences between the 486DX and 486SX microprocessors are:

486DX	486SX	Pin Number
FERR#	NC	C14
NMI	NC	B15
IGNNE#	NMI	A15

These signals are not used for clocking or disassembly. When the probe adapter is connected using the procedure in this manual, the software disassembles correctly and the signal definitions change for auxiliary channels C1:2, C0:7, and C0:6.

487SX

Signal differences between the 486DX and 487SX microprocessors are:

486DX	487SX	Pin Number
FERR#	NC	C14
NC	MP#	B14
NC	FERR#	A13
	KEY	D4

These signals are not used for clocking or disassembly. When the probe adapter is connected using the procedure in this manual, the software disassembles correctly and the signal definitions change for auxiliary channel C1:2.

J422 connects to FERR#.

The MP# signal is not acquired; it is kept asserted by the 487SX microprocessor.

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