Instruction Manual

Tektronix

**TMS 109
P54 & P55 Microprocessor Support**

070-9811-00

There are no current European directives that
apply to this product. This product provides
cable and test lead connections to a test object of
electronic measuring and test equipment.

Warning
The servicing instructions are for use by
qualified personnel only. To avoid personal
injury, do not perform any servicing unless you
are qualified to do so. Refer to all safety
summaries prior to performing service.

SOFTWARE WARRANTY

Tektronix warrants that the media on which this software product is furnished and the encoding of the programs on the media will be free from defects in materials and workmanship for a period of three (3) months from the date of shipment. If a medium or encoding proves defective during the warranty period, Tektronix will provide a replacement in exchange for the defective medium. Except as to the media on which this software product is furnished, this software product is provided "as is" without warranty of any kind, either express or implied. Tektronix does not warrant that the functions contained in this software product will meet Customer's requirements or that the operation of the programs will be uninterrupted or error-free.

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In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period and make suitable arrangements for the performance of service. Customer shall be responsible for packaging and shipping the defective product to the service center designated by Tektronix, with shipping charges prepaid. Tektronix shall pay for the return of the product to Customer if the shipment is to a location within the country in which the Tektronix service center is located. Customer shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other locations.

This warranty shall not apply to any defect, failure or damage caused by improper use or improper or inadequate maintenance and care. Tektronix shall not be obligated to furnish service under this warranty a) to repair damage resulting from attempts by personnel other than Tektronix representatives to install, repair or service the product; b) to repair damage resulting from improper use or connection to incompatible equipment; c) to repair any damage or malfunction caused by the use of non-Tektronix supplies; or d) to service a product that has been modified or integrated with other products when the effect of such modification or integration increases the time or difficulty of servicing the product.

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Table of Contents

Getting Started

Operating Basics

Specifications

Maintenance

Replaceable Electrical Parts

Replaceable Mechanical Parts

Index

List of Figures

List of Tables

General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Use Proper AC Adapter. Use only the AC adapter specified for this product.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. Warning statements identify conditions or practices that could result in injury or loss of life.

CAUTION. Caution statements identify conditions or practices that could result in damage to this product or other property.

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING High Voltage	Protective Ground (Earth) Terminal	CAUTION Refer to Manual	Double Insulated

TMS 109 P54 & P55 Microprocessor Support Instruction Manual

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface: Microprocessor Support Documentation

This instruction manual contains specific information about the TMS 109 P54/P55 microprocessor support and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor supports on the logic analyzer for which the TMS 109 P54/P55 support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor supports, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor supports is included with each product. Each logic analyzer has basic information that describes how to perform tasks common to supports on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test

- Setting up the logic analyzer to acquire data from the system under test

- Acquiring and viewing disassembled data

- Using the probe adapter

Manual Conventions

This manual uses the following conventions:

- The term disassembler refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.

- The phrase "information on basic operations" refers to online help, an installation manual, or a basic operations of microprocessor supports user manual.

- In the information on basic operations, the term XXX used in field selections and file names must be replaced with P54C. This is the name of the microprocessor in field selections and file names you must use to operate the P54/P55 support.

- The term system under test (SUT) refers to the microprocessor-based system from which data will be acquired.

- The term logic analyzer refers to the Tektronix logic analyzer for which this product was purchased.

- The term module refers to a 136-channel or a 192-channel module.

- P54/P55 refers to all supported variations of the P54 and P55 microprocessors unless otherwise noted.

- A pound sign (#) following a signal name indicates an active low signal.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The manual set provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time
	Or, contact us by e-mail: tm_app_supp@tek.com
	For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Contact your local Tektronix distributor or sales office. Or, visit our web site for a listing of worldwide service locations.
	http://www.tek.com
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000

Getting Started

Getting Started

This chapter provides information on the following topics and tasks:

- A description of the TMS 109 microprocessor support package

- Logic analyzer software compatibility

- Your system under test requirements

- Support restrictions

- How to configure the probe adapter

- How to connect to the system under test (SUT)

- How to apply power to and remove power from the probe adapter

Support Description

The TMS 109 microprocessor support package disassembles data from systems that are based on the Intel P54C, P54CM, P55C, and P55CM microprocessors. The support runs on a compatible Tektronix logic analyzer equipped with a 136-channel module or a 192-channel module.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 109 microprocessor support.

The TMS 109 supports the P54C, P54CM, P55C, and P55CM microprocessors in a 296-pin PGA package.

The low-profile probe adapter requires a 192-Channel High-Density Probe to make connections from the logic analyzer to your SUT.

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Mechanical Parts* chapter.

To use this support efficiently, you need to have the items listed in the information on basic operations as well as the *P54/P55 Microprocessor User's Manual,* Intel, 1997.

Information on basic operations also contains a general description of supports.

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

To use the TMS 109 support, the Tektronix logic analyzer must be equipped with either a 136-channel module or a 192-channel module at a minimum. The module must be equipped with enough probes to acquire clock and channel data from signals in your P54/P55-based system.

Refer to information on basic operations to determine how many modules and probes the logic analyzer needs to meet the channel requirements.

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor supports in the information on basic operations as they pertain to your SUT.

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other P54/P55 support requirements and restrictions.

System Clock Rate. The TMS 109 support can acquire data from the P54/P55 microprocessor at speeds of up to 66.66 MHz[1].

SUT Power. Whenever the SUT is powered off, be sure to remove power from the probe adapter. Refer to *Applying and Removing Power* at the end of this chapter for information on how to remove power from the probe adapter.

Disabling the Instruction Cache. To disassemble acquired data, you must disable the internal instruction cache. Disabling the cache makes all instruction prefetches visible on the bus so they can be acquired and disassembled.

Cache Invalidation Cycles. Cache Invalidation addresses are not acquired.

Bus Hold Cycles. Bus Hold cycles are not acquired while the RESET signal is active.

[1] Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest devices supported.

AHOLD Signal. If the AHOLD signal is active (high) during a Writeback cycle (a four cycle Burst Write), the acquired address is undefined.

Burst Cycles. The P54/P55 microprocessor expects the memory system to increment addresses during a Burst cycle. When viewing disassembled data, the disassembler synthesizes the addresses. When viewing state data, the addresses appear to be identical.

Probe Mode Cycles. Probe Mode cycles are not identified.

Directory Table and Descriptor Table Reads and Writes. These reads and writes are not disassembled.

Bus Anomalies. Some combinations of instructions and operating modes of the microprocessor can cause additional cycles to be fetched. This behavior is unpredicatable, not documented, and can cause the disassembler to misinterpret if fetched cycles were or were not executed. This is most likely to occur during Floating Point operations.

Configuring the Probe Adapter

There are five jumpers on each probe adapter. Table 1–1 lists the jumper positions and functions.

Table 1–1: Jumper positions and function

Conventional probe adapter	Low-profile probe adapter	Position	Function
J1155	J1501	1–2	Match the P54/P55 microprocessor system speed at 40–80 MHz
		2–3	Match the P54/P55 microprocessor system speed at 25–50 MHz
J1160	J1500	1–2	Configure probe adapter for Custom clocking (disassembly)
		2–3	Configure probe adapter for timing analysis
J1165	J1401	1–2	Enable tracking of burst and pipelined cycles while BOFF# and HLDA are asserted
		2–3	Disable tracking of burst and pipelined cycles while BOFF# and HLDA are asserted. This setting can be used if an external master's signal timing is different from that of the P54C.

Table 1–1: Jumper positions and function (cont.)

Conventional probe adapter	Low-profile probe adapter	Position	Function
J1170	J1400	1–2	Enable Address Synthesis (A(2:0) are derived from BE(7:0)#)
		2–3	Disable Address Synthesis (A(2:0)=0)
J1340	J1404	1–2	Acquire the D/P# signal from pin AE35 of the socket being probed
		OPEN	Acquire the D/P# signal from an external source. If this jumper is left open, you must route the D/P# signal to pin 1 of this jumper from an external source. This allows you to probe your system from the Dual socket as long as the D/P# signal is accessible on the system board.

CLK Jumper

The CLK jumper (J1155 on the conventional probe adapter or J1501 on the low-profile probe adapter) should be placed in the $\geq$45 position to acquire data from a system running at or faster than 45 MHz. The jumper should be placed in the <45 position to acquire data from a system running slower than 45 MHz.

Figure 1–1 shows the location of J1155 on the conventional probe adapter; Figure 1–2 shows the location of J1501 on the low-profile probe adapter.

Disassembly/Timing Jumper

The Disassembly/Timing jumper (J1160 on the conventional probe adapter or J1500 on the low-profile probe adapter) should be placed in the D position to acquire disassembled data and in the T position to acquire timing data.

Table 1–2 shows how to position this jumper depending on the type of clocking you are using and the type of display you want to view.

Table 1–2: Disassembly/Timing jumper information

J1160/J1500 position	Clocking	Data window
D (Disassembly)	Custom	Listing window, Disassembly, State, or Graph displays
T (Timing)	Internal	Waveform window, or Timing display
	External	Waveform window, Listing window, or Timing display

Figure 1–1 shows the location of J1160 on the conventional probe adapter; Figure 1–2 shows the location of J1500 on the low-profile probe adapter.
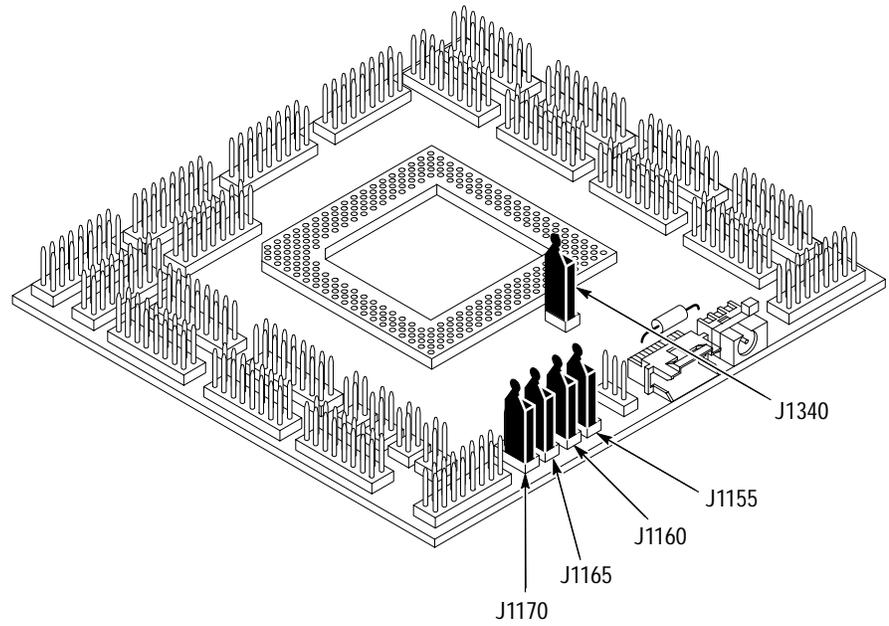
Figure 1–1: Jumper locations on the conventional probe adapter
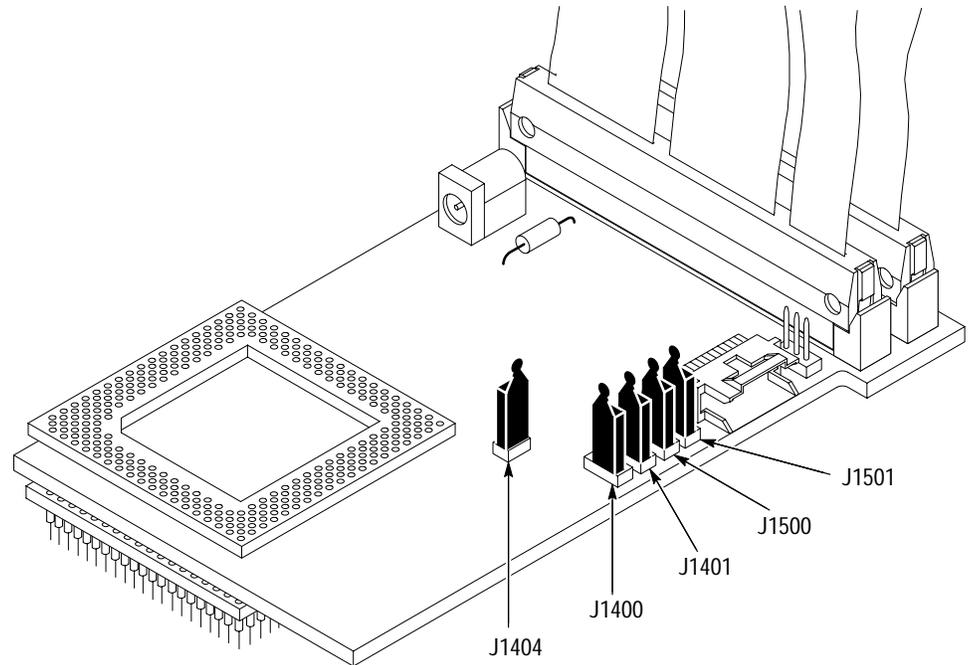
Figure 1–2: Jumper locations on the low-profile probe adapter

Tracking Jumper

The Tracking jumper (J1165 on the conventional probe adapter or J1401 on the low-profile probe adapter) should not need to be moved from the default position (pins 1 and 2 connected).

The only time this jumper should be moved is when the tracking circuitry malfunctions. An indication of such a malfunction is when you see activity on the bus during a BOFF or HLDA cycle that is uncharacteristic of the P54/P55 microprocessor. When the jumper is in the 2, 3 position, the circuitry on the probe adapter does not track BOFF and HLDA cycles. A data sample will show that such a cycle occurred but it will not contain meaningful information.

This jumper only affects the probe adapter when the Disassembly/Timing jumper (J1160 on the conventional probe adapter or J1500 on the low-profile probe adapter) is in the D position.

Figure 1–1 shows the location of J1165 on the conventional probe adapter; Figure 1–2 shows the location of J1401 on the low-profile probe adapter.

Address Synthesis Jumper

When the Address Synthesis jumper (J1170 on the conventional probe adapter or J1400 on the low-profile probe adapter) is in position 1, 2, A(2:0) are derived from the BE(7:0)# signals and stored in the acquisition memory with the rest of the address.

When the jumper is in position 2, 3, it disables address synthesis, A(2:0)=0.

Figure 1–1 shows the location of J1170 on the conventional probe adapter; Figure 1–2 shows the location of J1400 on the low-profile probe adapter.

D/P# Signal Jumper

When the D/P# signal jumper (J1340 on the conventional probe adapter or J1404 on the low-profile probe adapter) is in the 1, 2 position, the D/P# signal is acquired from pin AE35 of the socket being probed.

When the jumper is open (not connected), it acquires the D/P# signal from an external source, and you will have to route the D/P# signal to pin 1 of this jumper externally. This allows you to probe your system from the dual socket as long as the D/P# signal is accessible on the SUT.

Figure 1–1 shows the location of J1340 on the conventional probe adapter; Figure 1–2 shows the location of J1404 on the low-profile probe adapter.

Connecting to a System Under Test

Before you connect to the SUT, you must connect the probes to the module. Your SUT must also have a minimum amount of clear space surrounding the microprocessor to accommodate the probe adapter. Refer to the *Specifications* chapter in this manual for the required clearances.

The channel and clock probes shown in this chapter are for a 136-channel module. The probes will look different if you are using a 192-channel module.

The general requirements and restrictions of microprocessor supports in the information on basic operations shows the vertical dimensions of a channel or clock probe connected to square pins on a circuit board.

Conventional Probe Adapter

To connect the logic analyzer to a SUT using a conventional PGA probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

⚠ *CAUTION. Static discharge can damage the microprocessor, the probe adapter, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.

3. Place the probe adapter onto the antistatic shipping foam to support the probe as shown in Figure 1–3. This prevents the circuit board from flexing and the socket pins from bending.

4. Remove the microprocessor from your SUT.

5. Line up the pin 2B indicator on the probe adapter board with the pin 2B indicator on the microprocessor.

⚠ *CAUTION. Failure to correctly place the microprocessor into the probe adapter might permanently damage the microprocessor once power is applied.*

6. Place the microprocessor into the probe adapter as shown in Figure 1–3.
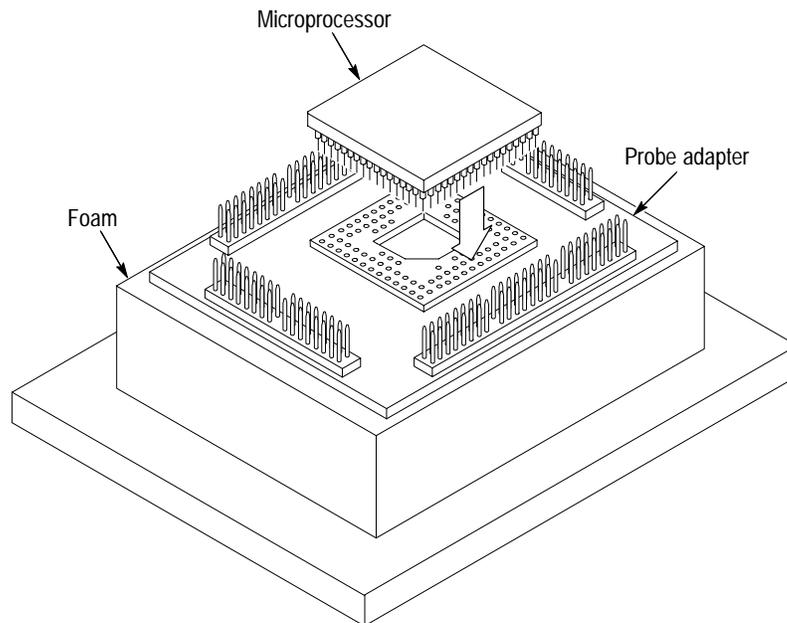
Figure 1–3: Placing a microprocessor into the conventional probe adapter

7. Connect the channel and clock probes to the probe adapter as shown in Figure 1–4. For the 192-channel module, match the channel groups and numbers on the probe labels to the corresponding HI_ and LO_pins on the probe adapter. Match the ground pins on the probes to the corresponding pins on the probe adapter.

For the 136-channel module, match the channel groups and numbers on the probe labels to the corresponding LO_ pins on the probe apapter. There are some exceptions; they are shown in Table 1–3.

Table 1–3: Probe adapter exceptions for the 136-channel module

Section	Connect to probe adapter pins
E3, E2, E1, E0	HI_A3, HI_A2, HI_A1, HI_A0
C1, C0	HI_C3, HI_C2

TMS 109 P54 & P55 Microprocessor Support Instruction Manual
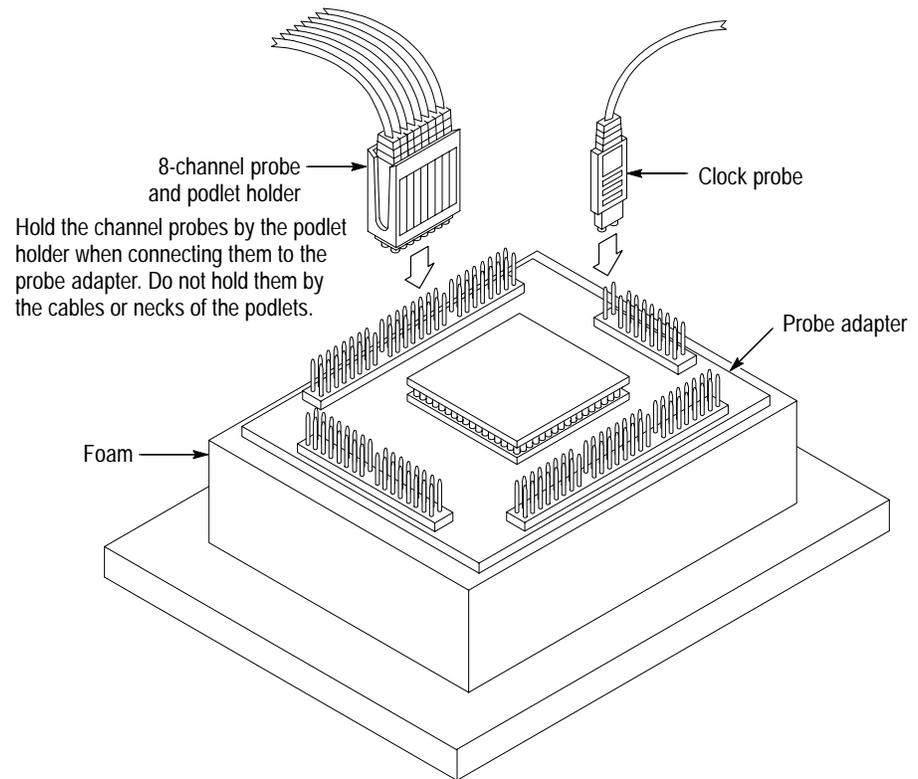
Figure 1–4: Connecting probes to the conventional probe adapter

8. Line up the pin 2B indicator on the probe adapter board with the pin 2B indicator on your SUT.

9. Place the probe adapter onto the SUT as shown in Figure 1–5.

NOTE. You might need to stack one or more replacement sockets between the SUT and the probe adapter to provide sufficient vertical clearance from adjacent components. However, keep in mind that this might increase loading, which can reduce the electrical performance of your probe adapter.
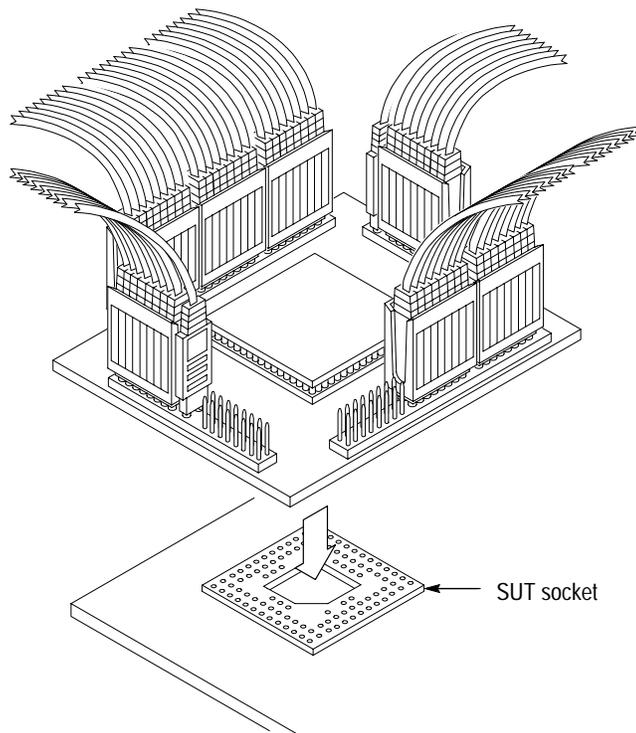
Figure 1–5: Placing the conventional probe adapter onto the SUT

Low-Profile Probe Adapter with a High-Density Probe

If a probe adapter has one or two high-density cables (probe adapter does not have pins to which the channel and clock probes connect), the probe adapter requires a high-density probe to make connections between the logic analyzer and a SUT.

To connect the logic analyzer to a SUT using the low-profile PGA probe adapter and a high-density probe, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

⚠️ *CAUTION. Static discharge can damage the microprocessor, the low-profile probe adapter, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and low-profile probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch the black foam on the underside of the probe adapter to discharge stored static electricity from the probe adapter.

3. Remove the microprocessor from the SUT.

4. Line up the pin 2B indicator on the probe adapter board with the pin 2B indicator on the microprocessor.

⚠ **CAUTION.** *Failure to correctly place the microprocessor into the probe adapter might permanently damage the microprocessor once power is applied.*

5. Place the microprocessor into the probe adapter as shown in Figure 1–6.
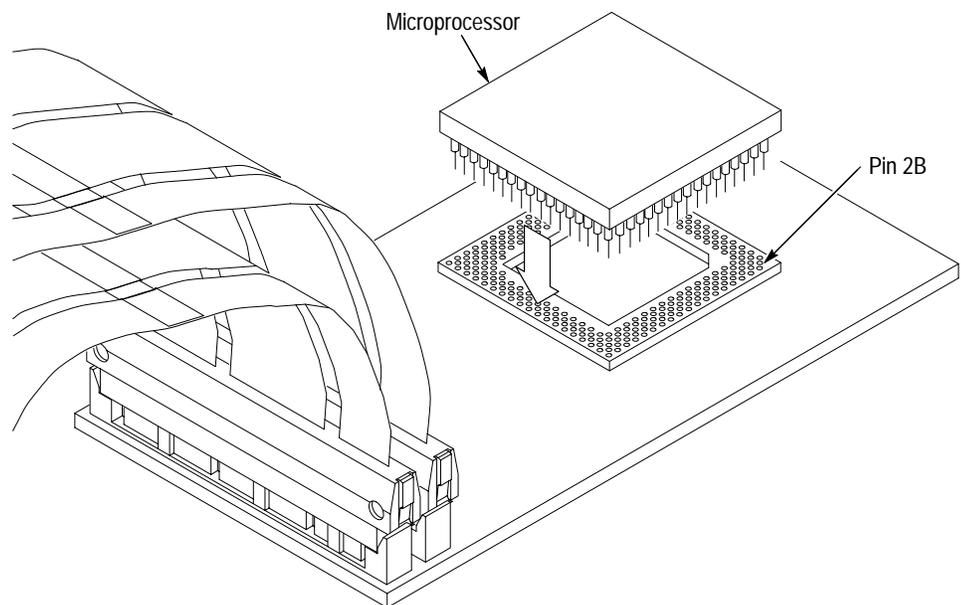
Figure 1–6: Placing a microprocessor into the low-profile probe adapter

6. Remove the black foam from the underside of the probe adapter.

7. Line up the pin 2B indicator on the probe adapter board with the pin 2B indicator on the SUT.

8. Place the probe adapter onto the SUT as shown in Figure 1–7.

NOTE. *You might need to stack one or more replacement sockets between the SUT and the probe adapter to provide sufficient vertical clearance from adjacent components. However, keep in mind this might increase loading, which can reduce the electrical performance of the probe adapter.*

SUT socket

Pin 2B
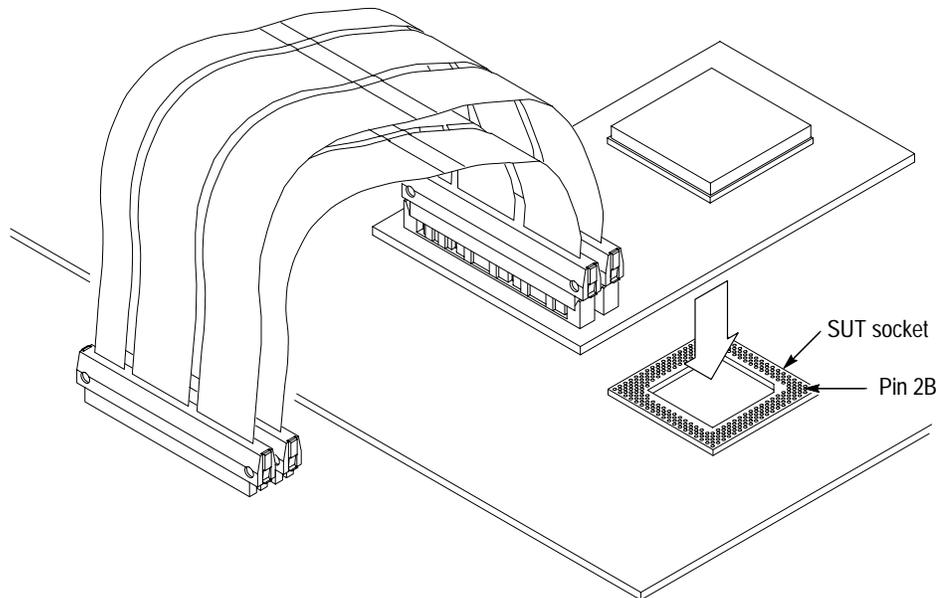
Figure 1–7: Placing the low-profile probe adapter onto the SUT

9. Connect the clock and channel probes to the high-density probe as shown in Figure 1–8. For the 192-channel module, match the channel groups and numbers on the probe labels to the corresponding HI_ and LO_pins on the high-density probe. Match the ground pins on the probes to the corresponding pins on the probe adapter.

For the 136-channel module, match the channel groups and numbers on the probe labels to the corresponding LO_ pins on the high-density probe. There are some exceptions; they are shown in Table 1–4.

Table 1–4: High-density probe exceptions for the 136-channel module

Section	Connect to high-density probe pins
E3, E2, E1, E0	HI_A3, HI_A2, HI_A1, HI_A0
C1, C0	HI_C3, HI_C2

Match the ground pins on the probes to the corresponding pins on the probe adapter.
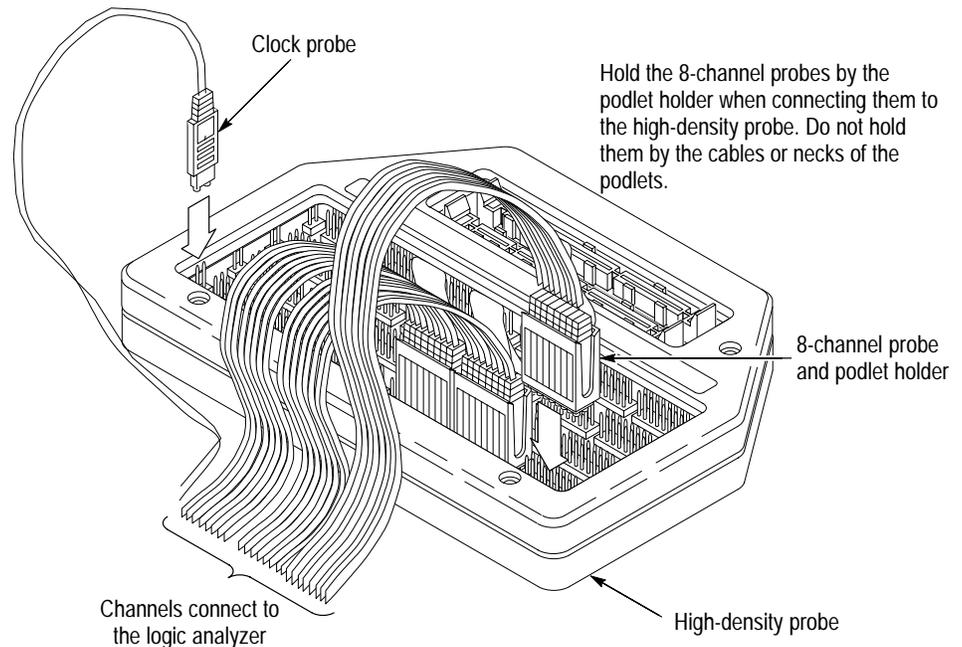
Figure 1–8: Connecting clock and channel probes to a high-density probe

10. Align pin 1 on the LO cable connector, the end on the narrowest cable strip of the cable, with pin 1 on the LO connector on the high-density probe. Connect the cable to the connector as shown in Figure 1–9.

NOTE. The LO cable is 12 inches long; the HI cable is 13 inches long.

11. Align pin 1 on the HI cable connector, the end on the narrowest cable strip of the cable, with pin 1 on the HI connector on the high-density probe. Connect the cable to the connector as shown in Figure 1–9.
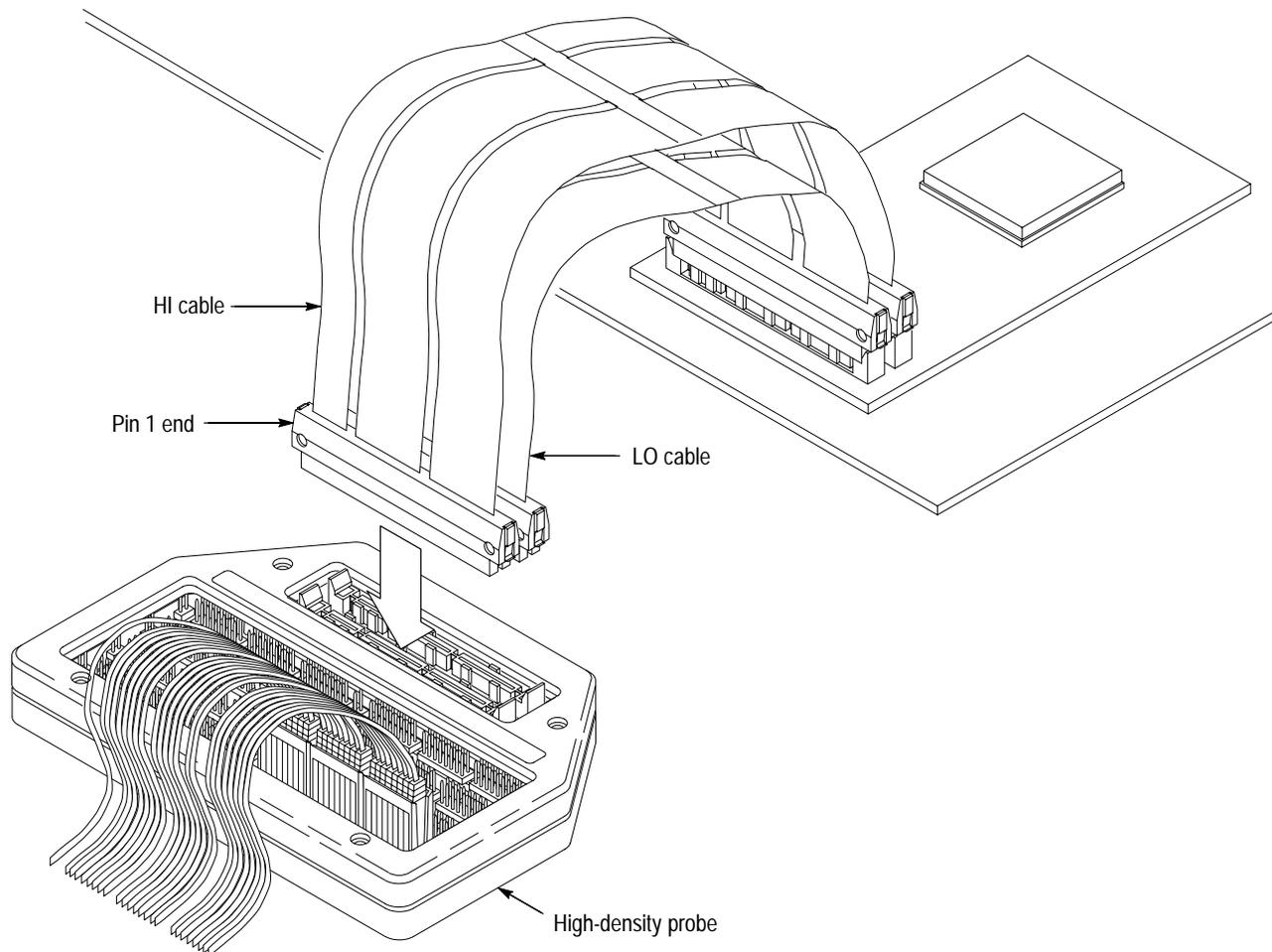
Figure 1–9: Connecting LO and HI cables to a high-density probe

Applying and Removing Power

A power supply for the P54/P55 probe adapter is included with the support. The power supply provides +5 volts power to the probe adapter. The center connector of the power jack connects to Vcc.

NOTE. Whenever the SUT is powered off, be sure to remove power from the probe adapter.

To apply power to the P54/P55 probe adapter and SUT, follow these steps:

⚠ **CAUTION.** *Failure to use the +5 V power supply provided by Tektronix might permanently damage the probe adapter and P54/P55 microprocessor. Do not mistake another power supply that looks similar for the +5 V power supply.*

1. Connect the +5 V power supply to the jack on the probe adapter. Figure 1–10 shows the location of the jack on the conventional probe adapter. Figure 1–11 shows the location of the jack on the low-profile probe adapter.

⚠ **CAUTION.** *Failure to apply power to the probe adapter before applying power to your SUT might permanently damage the P54/P55 microprocessor and SUT.*

2. Plug the power supply for the probe adapter into an electrical outlet.

3. Power on the SUT.
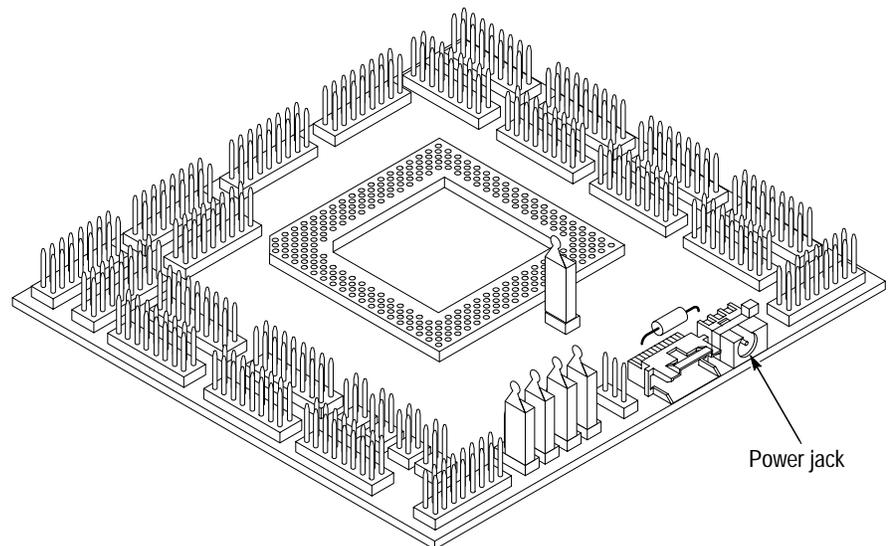
Figure 1–10: Power jack location on the conventional probe adapter
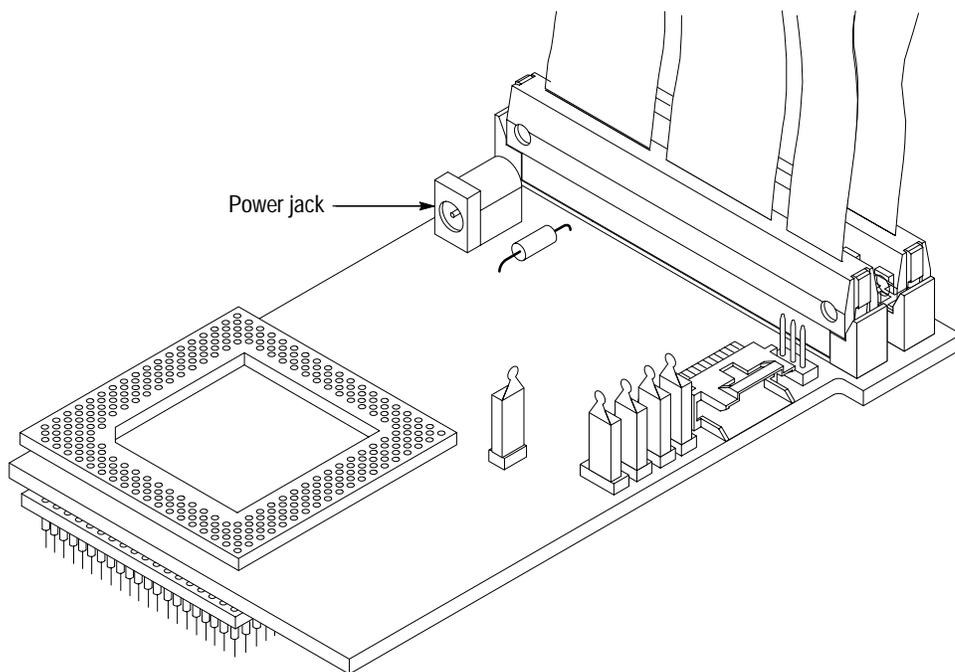
Power jack

Figure 1–11: Power jack location on the low-profile probe adapter

To remove power from the SUT and P54/P55 probe adapter, follow these steps:

⚠️ *CAUTION. Failure to power down your SUT before removing the power from the probe adapter might permanently damage the P54/P55 microprocessor and SUT.*

1. Power off the SUT.

2. Unplug the power supply for the probe adapter from the electrical outlet.

Operating Basics

Setting Up the Support

This section provides information on how to set up the support. Information covers the following topics:

■ Channel group definitions

■ Clocking options

■ Symbol table files

Remember that the information in this section is specific to the operations and functions of the TMS 109 P54/P55 support on any Tektronix logic analyzer for which it can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and disassemble data, you need to load the support and specify setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The software automatically defines channel groups for the support. For the 136-channel module, the channel groups for the P54/P55 support are Address, Data, Data_Lo, Control, DataSize, Cache, and Misc. For the 192-channel module, the channel groups for the P54/P55 support are Address, Data, Data_Lo, Control, DataSize, Cache, Debug, APIC, Priv_Bus, Parity, and Misc. If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 3–7.

Clocking Options

The TMS 109 support offers a microprocessor-specific clocking mode for the P54/P55 microprocessors. This clocking mode is the default selection whenever you load the P54C support.

A description of how cycles are sampled by the module using the TMS 109 support and probe adapter is found in the *Specifications* chapter.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

The clocking option for the TMS 109 support is Alternate Bus Master Cycles.

An alternate bus master cycle is defined as the cycle in which the P54/P55 microprocessor gives up the bus to an alternate device (a DMA device or another microprocessor). These types of cycles are acquired when you select Included.

Backoff cycles will always be acquired regardless of the Alternate Bus Master Cycles selection.

Symbols

The TMS 109 support supplies one symbol table file. The P54C_Ctrl file replaces specific Control channel group values with symbolic values when Symbolic is the radix for the channel group.

Table 2–1 shows the name, bit pattern, and meaning for the symbols in the file P54C_Ctrl, the Control channel group symbol table.

Table 2–1: Control group symbol table definitions

Symbol	D/P#	INIT	IRESET_L	PRDY	BUSCHK#	SMIACT#	LOCK#	SCYC	LAST_D	AHOLD	HLDA	BOFF#	M/IO#	D/C#	W/R#	Meaning
RESET	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	Reset
P_FETCH	0	X	0	X	X	X	1	X	X	X	0	1	1	0	0	Primary processor opcode read
D_FETCH	1	X	0	X	X	X	1	X	X	X	0	1	1	0	0	Dual processor opcode read
FETCH*	X	X	0	X	X	X	1	X	X	X	0	1	1	0	0	Opcode read
P_LOCK_RD	0	X	0	X	X	X	0	X	X	X	0	1	X	1	0	Primary processor locked read cycle
D_LOCK_RD	1	X	0	X	X	X	0	X	X	X	0	1	X	1	0	Dual processor locked read cycle
LOCK_RD*	X	X	0	X	X	X	0	X	X	X	0	1	X	1	0	Locked read cycle
P_LOCK_WR	0	X	0	X	X	X	0	X	X	X	0	1	X	1	1	Primary processor locked write cycle
D_LOCK_WR	1	X	0	X	X	X	0	X	X	X	0	1	X	1	1	Dual processor locked write cycle
LOCK_WR*	X	X	0	X	X	X	0	X	X	X	0	1	X	1	1	Locked write cycle
P_MEM_RD	0	X	0	X	X	X	X	X	X	X	0	1	1	1	0	Primary processor nonopcode read
D_MEM_RD	1	X	0	X	X	X	X	X	X	X	0	1	1	1	0	Dual processor nonopcode read
MEM_RD*	X	X	0	X	X	X	X	X	X	X	0	1	1	1	0	Read from memory, nonopcode
P_MEM_WR	0	X	0	X	X	X	X	X	X	X	0	1	1	1	1	Primary processor write to memory
D_MEM_WR	1	X	0	X	X	X	X	X	X	X	0	1	1	1	1	Dual processor write to memory
MEM_WR*	X	X	0	X	X	X	X	X	X	X	0	1	1	1	1	Write to memory

Table 2–1: Control group symbol table definitions (cont.)

Symbol	D/P#	INIT	IRESET_L	PRDY	BUSCHK#	SMIACT#	LOCK#	SCYC	LAST_D	AHOLD	HLDA	BOFF#	M/IO#	D/C#	W/R#	Meaning
P_I/O_RD	0	X	0	X	X	X	X	X	X	X	0	1	0	1	0	Primary processor I/O read cycle
D_I/O_RD	1	X	0	X	X	X	X	X	X	X	0	1	0	1	0	Dual processor I/O read cycle
I/O_RD*	X	X	0	X	X	X	X	X	X	X	0	1	0	1	0	I/O read cycle
P_I/O_WR	0	X	0	X	X	X	X	X	X	X	0	1	0	1	1	Primary processor I/O write cycle
D_I/O_WR	1	X	0	X	X	X	X	X	X	X	0	1	0	1	1	Dual processor I/O write cycle
I/O_WR*	X	X	0	X	X	X	X	X	X	X	0	1	0	1	1	I/O write cycle
P_MEM_R/W*	0	X	0	X	X	X	X	X	X	X	0	1	1	1	X	Any primary processor read or write
D_MEM_R/W*	1	X	0	X	X	X	X	X	X	X	0	1	1	1	X	Any dual processor read or write
MEM_R/W*	X	X	0	X	X	X	X	X	X	X	0	1	1	1	X	Any memory read or write cycle
P_I/O_R/W*	0	X	0	X	X	X	X	X	X	X	0	1	0	1	X	Any primary processor I/O cycle
D_I/O_R/W*	1	X	0	X	X	X	X	X	X	X	0	1	0	1	X	Any dual processor I/O cycle
I/O_R/W*	X	X	0	X	X	X	X	X	X	X	0	1	0	1	X	Any I/O read or write cycle
P_READ*	0	X	0	X	X	X	X	X	X	X	0	1	X	1	0	Any primary processor read cycle
D_READ*	1	X	0	X	X	X	X	X	X	X	0	1	X	1	0	Any dual processor read cycle
READ*	X	X	0	X	X	X	X	X	X	X	0	1	X	1	0	Any read cycle
P_WRITE*	0	X	0	X	X	X	X	X	X	X	0	1	X	1	1	Any primary processor write cycle
D_WRITE*	1	X	0	X	X	X	X	X	X	X	0	1	X	1	1	Any dual processor write cycle
WRITE*	X	X	0	X	X	X	X	X	X	X	0	1	X	1	1	Any write cycle
P_INT_ACK	0	X	0	X	X	X	X	X	X	X	0	1	0	0	0	Primary processor int. acknowledge
D_INT_ACK	1	X	0	X	X	X	X	X	X	X	0	1	0	0	0	Dual processor int. acknowledge
INT_ACK*	X	X	0	X	X	X	X	X	X	X	0	1	0	0	0	Interrupt acknowledge cycle
P_SPECIAL	0	X	0	X	X	X	X	X	X	X	0	1	0	0	1	Primary processor special cycle
D_SPECIAL	1	X	0	X	X	X	X	X	X	X	0	1	0	0	1	Dual processor special cycle
SPECIAL*	X	X	0	X	X	X	X	X	X	X	0	1	0	0	1	Special cycle
P_RESERVE	0	X	0	X	X	X	X	X	X	X	0	1	1	0	1	Primary processor reserved
D_RESERVE	1	X	0	X	X	X	X	X	X	X	0	1	1	0	1	Dual processor reserved
RESERVE*	X	X	0	X	X	X	X	X	X	X	0	1	1	0	1	Reserved
ALT_B_MTR	X	X	0	X	X	X	X	X	X	X	1	X	X	X	X	Alternate bus master cycle
BOFF	X	X	0	X	X	X	X	X	X	X	X	0	X	X	X	Backoff cycle

Table 2–1: Control group symbol table definitions (cont.)

Symbol	D/P#	INIT	IRESET_L	PRDY	BUSCHK#	SMIACT#	LOCK#	SCYC	LAST_D	AHOLD	HLDA	BOFF#	M/IO#	D/C#	W/R#	Meaning
P_BUSCHCK	0	X	0	X	0	X	X	X	X	X	0	1	X	X	X	Primary processor buscheck
D_BUSCHCK	1	X	0	X	0	X	X	X	X	X	0	1	X	X	X	Dual processor buscheck
BUSCHCK*	X	X	0	X	0	X	X	X	X	X	0	1	X	X	X	Buscheck
P_LOCKED	0	X	0	X	1	X	0	X	X	X	X	X	X	X	X	Any primary processor locked cycle
D_LOCKED	1	X	0	X	1	X	0	X	X	X	X	X	X	X	X	Any dual processor locked cycle
LOCKED*	X	X	0	X	1	X	0	X	X	X	X	X	X	X	X	Any locked cycle
P_SPLTCYC*	0	X	0	X	1	X	0	1	X	X	X	X	X	X	X	Primary processor split cycle
D_SPLTCYC*	1	X	0	X	1	X	0	1	X	X	X	X	X	X	X	Dual processor split cycle
SPLTCYC*	X	X	0	X	1	X	0	1	X	X	X	X	X	X	X	Split cycle
P_SMM*	0	X	0	X	X	0	X	X	X	X	X	X	X	X	X	The primary processor is in smm
D_SMM*	1	X	0	X	X	0	X	X	X	X	X	X	X	X	X	The dual processor is in smm
SMM*	X	X	0	X	X	0	X	X	X	X	X	X	X	X	X	Either processor is in smm
PRIMARY*	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Any primary processor cycle
DUAL*	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Any dual processor cycle

* **Symbols used only for triggering; they are not displayed.**

Information on basic operations describes how to use symbolic values for triggering and for displaying other channel groups symbolically, such as the Address channel group.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. Information covers the following topics and tasks:

- Acquiring data

- Viewing disassembled data in various display formats

- Cycle type labels

- Changing the way data is displayed

- Changing disassembled cycles with the mark cycles function

Acquiring Data

Once you load the P54C support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual.

Viewing Disassembled Data

You can view disassembled data in four display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE. Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to Changing How Data is Displayed *on page 2–10.*

The default display format shows the Address, Data, Data_Lo, and Control channel groups for each sample of acquired data. The Data and Data_Lo groups are shown in one column.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–2 shows these special characters and strings, and gives a definition of what they represent.

Table 2–2: Meaning of special characters in the display

Character or string displayed	Meaning
≫ or m	The instruction was manually marked as a program fetch
****	Indicates there is insufficient data available for complete disassembly of the instruction; the number of asterisks indicates the width of the data that is unavailable. Each two asterisks represent one byte.
#	Indicates an immediate value
(16) or (32)	Indicates that the fetch is from a 16- or 32-bit code segment size and disassembled accordingly. If the mnemonic fills the entire column width, the (16) or (32) will not be displayed.
SMM	Indicates a System management mode cycle.
(MMX)	Indicates an MMX instruction; appears at the end of the mnemonic
––	Hyphens (–) in the Data column indicate invalid bytes as determined by the BE7#-BE0# signals. When one of the two data groups does not contain valid bytes for a nonfetch cycle, the line for the group with the invalid bytes is not displayed. When neither data group contains valid bytes, both lines are displayed; this is an unexpected condition.
–	A hyphen in front of a cycle type label indicates a bus cycle from the microprocessor not being traced.
* ILLEGAL INSTRUCTION *	Decoded as an illegal instruction

Logic analyzer software does not allow more than 32 channels in each channel group. Therefore, two channel groups are used to acquire 64-bit wide P54/P55 microprocessor data: Data (D63-D32) and Data_Lo (D31-D0).

To handle the display of disassembled data from both data groups, the disassembler may display more than one line for each data sample. For samples with two display lines, data displayed under the Data column of the first line is from the Data_Lo group (D31-0); data displayed under the Data column of the second line is from the Data group (D63-32). Figure 2–1 on page 2–8 shows examples of multiple display lines used to display Data_Lo and Data group information.

The disassembler synthesizes the A2-A0 signals.

Aborting Lengthy Disassembly. When acquiring data from two microprocessors, the disassembler might take a long time to display disassembled data. This could be caused by the combination of selections in the Trace Processor and Other Processor fields in the Disassembly property page (Disassembly Format Definition overlay).

An example where this might occur is when the Trace Processor field is set to DUAL, and the Other Processor field is set to Suppress. If the acquisition data only contains data from the Primary microprocessor, then the disassembler might take a long time to display disassembled cycle types or instruction mnemonics. You can interrupt the disassembler by hitting the **Break Key**. If the disassembler does not find any displayable data, it will revert back to the Hardware display format with default settings.

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–3 shows these cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled with the vector name.

The disassembler always displays at least one line of information. Because fetches should have valid data for the Data and Data_Lo groups, most fetches should use at least two display lines. For example, a fetch cycle can show both an instruction, and a READ EXTENSION or FLUSH (or both).

Table 2–3: Cycle type definitions

Label	Description
(RESET)	A reset cycle
(MEM READ)	A nonlocked memory read cycle that is not an opcode fetch
(LOCKED MEM READ)	A locked memory read cycle that is not an opcode fetch
(MEM WRITE)	Any nonlocked memory write
(LOCKED MEM WRITE)	Any locked memory write
(IO READ)	Read from an I/O port
(IO WRITE)	Write to an I/O port
(INT ACK)	Interrupt acknowledge cycle
(SHUTDOWN)	Shutdown/special bus cycle; BE7:BE0 = 11111110
(CACHE FLUSH)	Cache flush/special bus cycle; BE7:BE0 = 11111101
(HALT)	Halt/special bus cycle; BE7:BE0 = 11111011
(WRITE–BACK)	Write back/special bus cycle; BE7:BE0 = 11110111
(FLUSH ACK)	Flush Ack/special bus cycle; BE7:BE0 = 11101111
(BRANCH TRACE: TARGET)	Branch Trace Message/special bus cycle; BE7:BE0 = 11011111
(BRANCH TRACE: SOURCE)	Branch Trace Message/special bus cycle; BE7:BE0 = 11011111
(STOP GRANT ACK)	Stop Grant cycle; cycle type is HALT/SPECIAL; BE7:BE0 = 11111011
(RESERVED)	Reserved
(ALTERNATE BUS MASTER)	Bus is released to an Alternate Bus Master

Table 2–3: Cycle type definitions (Cont.)

Label	Description
(BACK OFF)	Back Off bus cycle
(UNKNOWN)	An invalid/unknown bus cycle
(BURST LINE FILL)*	Fetch cycle computed to be a burst fill. The data is fetched but will not be executed, it is part of a 32 byte fetch. It will possibly be stored in cache.
(BACKOFF/BURST FLUSH)*	Burst/Fetch cycle computed to be flushed due to a back off
(EXTENSION)*	Fetch cycle computed to be an opcode extension
(FLUSH)*	Fetch cycle computed to be flushed
(DUAL FETCH)	Nondisassembled fetch cycle from the Dual processor
(PRIMARY FETCH)	Nondisassembled fetch cycle from the Primary processor

* Computed cycle types.	* Computed cycle types.

Figure 2–1 shows an example of the Hardware display.

Figure 2–1: Hardware display format

1 **Sample Column.** Lists the memory locations for the acquired data.

2 **Address Group.** Lists data from channels connected to the P54/P55 address bus.

3 **Data Column.** Lists data from channels connected to D63-D32 and/or D31-D0 of the P54/P55 microprocessor data bus. Refer to the general description of viewing disassembled data for information on how the disassembler determines when to display information for the Data group.

4 This part of the sample is displaying data from channels connected to D31-D0 of the P54/P55 microprocessor data bus.

5 This part of the sample is displaying data from channels connected to D63-D32 of the P54/P55 microprocessor data bus.

6 **Mnemonic Column.** Lists the disassembled instructions and cycle types.

7 **Timestamp.** Lists the timestamp values when a timestamp selection is made. Information on basic operations describes how you can select a timestamp.

Software Display Format

The Software display format shows only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Read extensions will be used to disassemble the instruction, but will not be displayed as a separate cycle in the Software display format. Data reads and writes are not displayed.

Out-of-order fetches are shown in the order the fetches are executed. An asterisk indicates an out-of-order fetch. The sample number of the out-of-order fetch will not be displayed if the previous executed instruction has a higher sample number. The sample number of the out-of-order fetch will be displayed if the previous executed instruction has a smaller sample number.

Since you cannot place the cursor on an instruction without a sample number, you will not be able to scroll to some out-of-order fetch instructions. To scroll to these instructions, you will have to switch to the Hardware display format.

Control Flow Display Format

The Control Flow display format shows only the first fetch of instructions that change the flow of control.

Instructions that generate a change in the flow of control in the P54/P55 microprocessor are as follows:

CALL	IRET	RET
INT	JMP	RSM

Instructions that might generate a change in the flow of control in the P54/P55 microprocessor are as follows:

BOUND	JL/JNGE	JNP/JPO
DIV	JLE/JNG	JNS
IDIV	JNB/JAE/JNC	JO
INTO	JNBE/JA	JP/JPE
JB/JNAE/JC	JNE/JNZ	JS
JBE/JNA	JNL/JGE	LOOP
JCXZ/JECXZ	JNLE/JG	LOOPNZ/LOOPNE
JE/JZ	JNO	LOOPZ/LOOPE

If a conditional jump branches to an address that is reached sequentially (no address break in the fetch sample), the disassembler cannot determine if the branch was taken. If there are two conditional jump instructions close together that branch to the same fetch line, then the disassembler may not be able to determine which conditional jump was actually taken. You can use the mark cycle function to correct the disassembly. Refer to *Marking Cycles* later in this section.

Subroutine Display Format

The Subroutine display format shows only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

Instructions that generate a subroutine call or a return in the P54/P55 microprocessor are as follows:

CALL	INT	IRET	RET	RSM

Instructions that might generate a subroutine call or a return in the P54/P55 microprocessor are as follows:

BOUND	DIV	IDIV	INTO

Changing How Data is Displayed

There are common fields and features that allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

You can make selections unique to the P54/P55 support to do the following tasks:

■ Change how data is displayed across all display formats

■ Change the interpretation of disassembled cycles

■ Display exception vectors

NOTE. All information defined in these fields pertain to the microprocessor that is being traced.

Optional Display Selections

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways:

- Specify the code segment size

- Choose an interrupt table

- Specify the starting address of the interrupt table

- Specify the size of the interrupt table

- Select to trace the Primary or Dual microprocessor

- Choose whether to display or suppress the hardware cycles from the microprocessor not being traced

The P54/P55 support has six additional fields: Code Segment Size, Interrupt Table, Interrupt Table Address, Interrupt Table Size, Trace Processor, and Other Processor. These fields appear in the area indicated in the information on basic operations.

Code Segment Size. You can select the default code size: 32-bit or 16-bit. The default code size is 16 bit.

Interrupt Table. You can specify if the interrupt table is Real, Virtual, or Protected. (Selecting Virtual is equivalent to selecting Protected.) The default is Real.

Interrupt Table Address. You can specify the starting address of the interrupt table in hexadecimal. The default starting address is 0x00000000.

Interrupt Table Size. You can specify the size of the interrupt table in hexadecimal. The default size is 0x400.

Trace Processor. You can select to disassemble data from the Primary or Dual microprocessor.

Other Processor. The "other" microprocessor is the one not being traced (not selected in the Trace Processor field). You can select to display or to suppress its bus cycles.

Dual Microprocessors Execution Tracing

When acquiring data from a SUT with two microprocessors, the disassembler can trace the execution flow of one microprocessor and display the hardware cycle types of the microprocessor not being traced. This means that the software disassembles only the instructions executed from the microprocessor being traced.

You can trace instructions from either the Primary microprocessor or the Dual microprocessor. You can also choose to display or not display (suppress) data from the microprocessor not selected in the Trace Processor field of the Disassembly property page (Disassembly Format Definition overlay).

To set up the mode of tracing, you need to set the Trace Processor and Other Processor fields in the Disassembly property page. Table 2–4 shows the combinations of Trace Processor and Other Processor field selections and their effects.

Table 2–4: Trace Processor and Other Processor field selections

Trace Processor	Other Processor	Effect
Primary	Suppress	Disassemble the Primary microprocessor only
Primary	Display Cycles	Disassemble the Primary microprocessor and display the hardware cycles of the Dual microprocessor
Dual	Suppress	Disassemble the Dual microprocessor only
Dual	Display Cycles	Disassemble the Dual microprocessor and display the hardware cycles of the Primary microprocessor

Figure 2–2 shows disassembled data from the Primary microprocessor and hardware cycles from the other microprocessor. A hyphen to the left of the mnemonic indicates data from the other microprocessor.

```
  Sample  Address   Data      Mnemonic                             Control
  -----------------------------------------------------------------------------
      16  000388B0  ABFFE1C3    RETS                           (32)  P_FETCH
          000388B4  B6EFFFEF  ( FLUSH )                              P_FETCH
      17  000408A8  ED33D233  – ( DUAL FETCH )                       D_FETCH
          000408AC  FF33F633  – ( DUAL FETCH )                       D_FETCH
      18  000388B8  FFB7D7FA  ( FLUSH )                              P_FETCH
          000388BC  FFFFFDFF  ( FLUSH )                              P_FETCH
      19  000408B0  BDDF26C3  – ( DUAL FETCH )                       D_FETCH
          000408B4  FF27FFBF  – ( DUAL FETCH )                       D_FETCH
      20  000207F4  00000005  ( MEM READ )                           P_MEM_RD
      21  000408B8  5DBE5FED  – ( DUAL FETCH )                       D_FETCH
          000408BC  7FFEFBFB  – ( DUAL FETCH )                       D_FETCH
      22  000388C0  44875050  ( FLUSH )                              P_FETCH
          000388C4  04870824  ( FLUSH )                              P_FETCH
      23  000307F4  00000005  – ( MEM READ )                         D_MEM_RD
      24  00038800  00009DE8  ( FLUSH )                              P_FETCH
          00038805  000EBE00    MOV ESI,#0000000E            (32)   P_FETCH
      25  000408C0  44875050  – ( DUAL FETCH )                       D_FETCH
          000408C4  04870824  – ( DUAL FETCH )                       D_FETCH
      26  0003880A  0AB90000    MOV ECX,#0000000A            (32)   P_FETCH
          0003880F  F3000000    REPZ                         (32)   P_FETCH
```

Figure 2–2: Data displayed from the Primary and Dual microprocessors

Figure 2–3 shows disassembled data from the Primary microprocessor only. Data from the Dual microprocessor is suppressed and not displayed.

```
  Sample  Address   Data      Mnemonic                             Control
  -----------------------------------------------------------------------------
      16  000388B0  ABFFE1C3    RETS                           (32)  P_FETCH
          000388B4  B6EFFFEF  ( FLUSH )                              P_FETCH
      18  000388B8  FFB7D7FA  ( FLUSH )                              P_FETCH
          000388BC  FFFFFDFF  ( FLUSH )                              P_FETCH
      20  000207F4  00000005  ( MEM READ )                           P_MEM_RD
      22  000388C0  44875050  ( FLUSH )                              P_FETCH
          000388C4  04870824  ( FLUSH )                              P_FETCH
      24  00038800  00009DE8  ( FLUSH )                              P_FETCH
          00038805  000EBE00    MOV ESI,#0000000E            (32)   P_FETCH
      26  0003880A  0AB90000    MOV ECX,#0000000A            (32)   P_FETCH
          0003880F  F3000000    REPZ                         (32)   P_FETCH
      28  00038810  003668AD    LODSD                        (32)   P_FETCH
          00038811  003668AD    PUSH #00000036               (32)   P_FETCH
          00038816  026A0000    PUSH #02                     (32)   P_FETCH
      30  00038818  4668026A    PUSH #02                     (32)   P_FETCH
          0003881A  4668026A    PUSH #00000046               (32)   P_FETCH
          0003881F  6A000000    PUSH #02                     (32)   P_FETCH
```

Figure 2–3: Disassembled data displayed from the Primary microprocessor only

Figure 2–4 shows disassembled data from the Dual microprocessor only. Data from the Primary microprocessor is suppressed and not displayed.

```
Sample  Address   Data       Mnemonic                          Control
---------------------------------------------------------------------------
    17  000408A8  ED33D233   XOR EDX,EDX                  (32)  D_FETCH
        000408AA  ED33D233   XOR EBP,EBP                  (32)  D_FETCH
        000408AC  FF33F633   XOR ESI,ESI                  (32)  D_FETCH
        000408AE  FF33F633   XOR EDI,EDI                  (32)  D_FETCH
    19  000408B0  BDDF26C3   RETS                         (32)  D_FETCH
        000408B4  FF27FFBF   ( FLUSH )                          D_FETCH
    21  000408B8  5DBE5FED   ( FLUSH )                          D_FETCH
        000408BC  7FFEFBFB   ( FLUSH )                          D_FETCH
    23  000307F4  00000005   ( MEM READ )                       D_MEM_RD
    25  000408C0  44875050   ( FLUSH )                          D_FETCH
        000408C4  04870824   ( FLUSH )                          D_FETCH
    27  00040800  00009DE8   ( FLUSH )                          D_FETCH
        00040805  000EBE00   MOV ESI,#0000000E            (32)  D_FETCH
    29  0004080A  0AB90000   MOV ECX,#0000000A            (32)  D_FETCH
        0004080F  F3000000   REPZ                         (32)  D_FETCH
```

Figure 2–4: Disassembled data displayed from the Dual microprocessor only

Branch Trace Messages

The disassembler interprets the information on the Address and Data Bus of Branch Trace Messages (BTMs) by reconstructing the address of the source or target of the branch instruction. Depending on which type of BTM is in use, either fast or normal, one or two BTMs will appear on the bus. The disassembler tracks BTMs as they appear on the bus. Figure 2–5 shows how the disassembler displays these cycles.

```
Sample  Address   Data       Mnemonic                          Control
---------------------------------------------------------------------------
     4  000207F4  00000005   ( MEM WRITE)                       P_MEM_WR
     6  00038810  003868AD   ( FLUSH )                          P_FETCH
        00038814  026A0000   ( FLUSH )                          P_FETCH
     8  000388A2  20------   ( BRANCH TRACE: TARGET )           P_SPECIAL
    10  00038800  08------   ( BRANCH TRACE: SOURCE )           P_SPECIAL
    14  00038818  33C03300   ( FLUSH )                          P_FETCH
        00038810  68C933DB   ( FLUSH )                          P_FETCH
```

Figure 2–5: Display of target and source Branch Trace Messages

Out-Of-Order Fetches

The P54/P55 microprocessor can prefetch cycles out of ascending order. For example, a branch to address 1008 could cause the following sample of addresses across the bus: 1008, 1000, 1018, and 1010. The data at address 1008 is executed, but the data at address 1000 is not. The data at addresses 1018 and 1010 are executed, but the data at address 1010 is executed before the data at 1018.

An example of the fetched order versus the executed order is shown below.

Fetched Order   Executed Order
1008   1008
1000   1010
1018   1018
1010

In the Hardware display format, the out-of-order fetches are displayed in the order they are fetched. They will be properly disassembled and identified by an asterisk (*) to the left of the instruction.

In the Hardware display format, you can determine the executed order of the out-of-order fetches by looking at the address of the out-of-order cycles and the subsequent cycles. Fetch cycles always have the sample numbers displayed.

In the Software display format, out-of-order fetches are displayed in the order they were executed. If the previously executed instruction had a larger sample number than the out-of-order fetch, the sample number will not be displayed. If the previous sample number is smaller than the out-of-order fetch, the sample number will be displayed. To mark an instruction without a sample number, you will have to switch to the Hardware display format.

In the Software display format, out-of-order fetches can cause up to sixteen lines of information to need to be displayed but only eight lines will actually be displayed. The disassembler displays <more> in the Mnemonic column to indicate that more than eight lines are available. To view more than eight lines of information, you must use the Hardware display format.

Speculative Prefetch Cycles

Speculative prefetch cycles can occur when the P54/P55 microprocessor fetches instructions that have been previously executed. To minimize prefetch delays, the P54/P55 microprocessor predicts the outcome of the branch instruction and starts prefetching at that address. When the branch instruction is executed, the target address is determined. If the P54/P55 microprocessor predicted the target address correctly, then the needed code has already been fetched. If it did not correctly predict the target address, then the speculative prefetch cycles that had been fetched will be flushed and fetching will begin at the target address.

Figure 2–6 shows an example of speculative prefetch cycles. The previous time (not shown) that the JNE instruction was executed, the branch was taken and the new target address was 0x3893D. The microprocessor assumed that the address would be 0x3893D and so started fetching at 0x38938 (which contains 0x3893D). Cycles at samples 746 and 748 are speculative prefetch cycles. When the instruction was executed, the microprocessor determined that the branch was not taken, flushed the speculative prefetch cycles, and started fetching at 0x38988 (sample 750), which contained the next instruction after the JNE.

```
  Sample  Address   Data      Mnemonic                                Control
--------------------------------------------------------------------------------
          00038986  B575C90F  JNE 0003893D                     (32)   P_FETCH
   734     000207D8  00000008  ( MEM READ )                            P_MEM_RD
   736     000207E8  00000046  ( MEM READ )                            P_MEM_RD
   738     00038988  000000BA  ( FLUSH )                               P_FETCH
          0003898C  24558900  ( FLUSH )                               P_FETCH
   740     00038990  20C2619D  ( FLUSH )                               P_FETCH
          00038994  6FBF6D00  ( FLUSH )                               P_FETCH
   742     00038998  CDBFDE6F  ( FLUSH )                               P_FETCH
          0003899C  FFEFFFF7  ( FLUSH )                               P_FETCH
   744     000389A0  FFFFEDAE  ( FLUSH )                               P_FETCH
          000389A4  F6FFF7EF  ( FLUSH )                               P_FETCH
   746     00038938  DB9BFF33  ( FLUSH )                               P_FETCH
          0003893C  0002A3E3  ( FLUSH )                               P_FETCH
   748     00038940  6D8A0000  ( FLUSH )                               P_FETCH
          00038944  204D8A10  ( FLUSH )                               P_FETCH
   750     00038988  000000BA  MOV EDX,#00000000                (32)   P_FETCH
          0003898D  24558900  MOV 24[EBP],EDX                  (32)   P_FETCH
```

Figure 2–6: Speculative Prefetch cycles

NOTE. The microprocessor also has a Branch Target Buffer and often performs speculative prefetching of branch target addresses (no matter if they are taken or are not taken). The disassembler usually interprets the correct flow of execution but cannot do so deterministically.

Cache Invalidation Cycles

Cache Invalidation cycles are needed to keep the microprocessor cache contents consistent with external memory. On a nonburst cycle that is also a Cache Invalidation cycle, the data and address will be valid as probed. On a burst cycle that is also a Cache Invalidation cycle, the data will be valid, but the addresses will not be valid as probed and the software will try to calculate the address from the surrounding cycles. Fetch cycles are disassembled. A letter c to the left of the mnemonic indicates a Cache Invalidation cycle, where the AHOLD signal was active.

Burst Cycles

On all burst cycles, only the first cycle contains a valid address. The P54/P55 microprocessor doesn't increment the address for a burst. The disassembler calculates the remaining burst cycle addresses for display.

System Management Mode (SMM)

The P54/P55 microprocessor provides a special mode called System Management Mode where the P54/P55 microprocessor CPU executes code from a separate, alternate memory space called SMRAM. The disassembler uses information from the SMIACT# signal to determine when the P54/P55 microprocessor is operating in this mode.

MMX Instruction Set   The P55 microprocessor includes the MMX instruction set. Since these instructions are potential subroutine instructions, the disassembler checks to see if an interrupt level 6 (illegal opcode) or 7 (device not available) occurred. If an interrupt 6 or 7 occurs, the interrupt will flush the bus.

When the disassembler detects that an instruction is from the MMX set, it displays an (MMX) to the right of the mnemonic.

MMX instructions are disassembled whether or not the microprocessor is set up to execute them.

Marking Cycles   The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it to one of the following cycle types:

- Opcode (the first word of an instruction)

- Extension (a subsequent word of an instruction)

- Flush (an opcode or extension that is fetched but not executed)

- Anything (any valid opcode, extension or flush)

- 16-bit or 32-bit default segment size

Mark selections are as follows:

```
Lo: Any          Any          Any          OPCODE
Lo: Any          Any          OPCODE       Any
Lo: Any          OPCODE       Any          Any
Lo: OPCODE       Any          Any          Any


Hi: Any          Any          Any          OPCODE
Hi: Any          Any          OPCODE       Any
Hi: Any          OPCODE       Any          Any
Hi: OPCODE       Any          Any          Any


EXTENSION CYCLE
FLUSH CYCLE

16-bit Default Segment Size
32-bit Default Segment Size

Undo marks on this cycle
```

For samples with two display lines, to change the cycle type to an Opcode or Anything, you must use the selections starting with Lo: for the first display line, and selections starting with Hi: for the second display line.

You can also use the Mark Opcode function to specify the default segment size mode (16-bit or 32-bit) for the cycle. The segment size selection changes the cycle the cursor is on and the remaining cycles to the end of memory or to the next mark.

The default segment size of the cycle is independent of any prefix override bytes in the particular fetch. For example, if you mark cycle 455 with a default size of 32 bits, but there are address/operand override prefixes in the instruction, the default size will be 32 bits but the size of the instruction will be 16 bits.

Information on basic operations contains more details on marking cycles.

Displaying Exception Vectors

The disassembler can display exception vectors. You can select to display the interrupt vectors for Real, Virtual, or Protected modes in the Interrupt Table field. (Selecting Virtual is equivalent to selecting Protected.)

You can relocate the table by entering the starting address in the Interrupt Table Address field. The Interrupt Table Address field provides the disassembler with the offset address; enter an eight-digit hexadecimal value corresponding to the offset of the base address of the exception table. The Interrupt Table Size field lets you specify a three-digit hexadecimal size for the table.

You can make these selections in the Disassembly property page (the Disassembly Format Definition overlay).

Table 2–5 lists the P54/P55 exception vectors for the Real Addressing mode.

Table 2–5: Exception vectors for Real Addressing mode

Exception number	Location in IV* table (in hexadecimal)	Displayed interrupt name
0	0000	DIVIDE ERROR
1	0004	DEBUG EXCEPTIONS
2	0008	NMI INTERRUPT
3	000C	BREAKPOINT INTERRUPT
4	0010	INTO DETECTED OVERFLOW
5	0014	BOUND RANGE EXCEEDED
6	0018	INVALID OPCODE
7	001C	DEVICE NOT AVAILABLE
8	0020	DOUBLE DEFAULT
9-11	0024-002C	RESERVED
12	0030	STACK EXCEPTION
13	0034	SEGMENT OVERRUN
14-15	0038-003C	RESERVED
16	0040	COPROCESSOR ERROR

Table 2–5: Exception vectors for Real Addressing mode (cont.)

Exception number	Location in IV* table (in hexadecimal)	Displayed interrupt name
17-31	0044-007C	RESERVED
32-255	0080-03FC	USER DEFINED

*   IV means interrupt vector.

Table 2–6 lists the P54/P55 exception vectors for the Protected Addressing mode.

Table 2–6: Exception vectors for Protected Addressing mode

Exception number	Location in IDT* (in hexadecimal)	Displayed exception name
0	0000	DIVIDE ERROR
1	0008	DEBUG EXCEPTIONS
2	0010	NMI INTERRUPT
3	0018	BREAKPOINT INTERRUPT
4	0020	INTO DETECTED OVERFLOW
5	0028	BOUND RANGE EXCEEDED
6	0030	INVALID OPCODE
7	0038	DEVICE NOT AVAILABLE
8	0040	DOUBLE FAULT
9	0048	RESERVED
10	0050	INVALID TSS
11	0058	SEGMENT NOT PRESENT
12	0060	STACK EXCEPTION
13	0068	SEGMENT OVERRUN
14	0070	PAGE FAULT
15	0078	RESERVED
16	0080	COPROCESSOR MODE
17	0088	ALIGNMENT CHECK
18	0090	MACHINE CHECK
19-31	0090-00F8	RESERVED
32-255	0100-07F8	USER DEFINED

*   IDT means interrupt descriptor table.

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your P54/P55 microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your SUT.

Information on basic operations describes how to view the file.

Specifications

Specifications

This chapter contains the following information:

- Probe adapter description

- Specification tables

- Dimensions of the probe adapter

- Channel assignment tables

- Description of how the module acquires P54/P55 signals

- List of other accessible microprocessor signals and extra probe channels

Probe Adapter Description

The probe adapter is nonintrusive hardware that allows the logic analyzer to acquire data from a microprocessor in its own operating environment with little effect, if any, on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and a socket for a P54/P55 microprocessor. The probe adapter connects to the microprocessor in the SUT. Signals from the microprocessor-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

All circuitry on the probe adapter is powered from the supplied power adapter.

The probe adapter accommodates the Intel P54C, P54CM, P55C, and P55CM microprocessors in a 273-pin PGA package.

Configuration   The probe adapter contains jumpers that need to be in certain positions for proper disassembly; Table 3–1 shows the jumper positions. For more information on these jumpers, refer to the descriptions on page 1–4.

Table 3–1: Jumper positions and function

Conventional probe adapter	Low-profile probe adapter	Position	Function
J1155	J1501	1–2	Match the P54/P55 microprocessor system speed at 40–80 MHz
		2–3	Match the P54/P55 microprocessor system speed at 25–50 MHz
J1160	J1500	1–2	Configure probe adapter for Custom clocking (disassembly)
		2–3	Configure probe adapter for timing analysis
J1165	J1401	1–2	Enable tracking of burst and pipelined cycles while BOFF# and HLDA are asserted
		2–3	Disable tracking of burst and pipelined cycles while BOFF# and HLDA are asserted. This setting can be used if an external master's signal timing is different from that of the P54C.
J1170	J1400	1–2	Enable Address Synthesis (A(2:0) are derived from BE(7:0)#)
		2–3	Disable Address Synthesis (A(2:0)=0)
J1340	J1404	1–2	Acquire the D/P# signal from pin AE35 of the socket being probed
		OPEN	Acquire the D/P# signal from an external source. If this jumper is left open, you will have to route the D/P# signal to pin 1 of this jumper from an external source. This allows you to probe your system from the Dual socket as long as the D/P# signal is accessible on the system board.

Specifications

These specifications are for a probe adapter connected between a compatible Tektronix logic analyzer and a SUT. Table 3–2 shows the electrical requirements the SUT must produce for the support to acquire correct data.

In Table 3–2, for the 136-channel module, one podlet load is 20 kΩ in parallel with 2 pF. For the 192-channel module, one podlet load is 100 kΩ in parallel with 10 pF.

Table 3–2: Electrical specifications

Characteristics	Requirements
SUT DC power requirements	
Voltage	4.75-5.25 VDC
Current	I max (calculated) 1.8 A I typ (measured) 1.2 A
Probe adapter power supply requirements	
Voltage	90-265 VAC
Current	1.1 A maximum at 100 VAC
Frequency	47-63 Hz
Power	25 W maximum

Table 3–2: Electrical specifications (cont.)

Characteristics	Requirements	
SUT clock		
Clock rate	Max. 66.66 MHz	
Minimum setup and hold time required		
BE7–0#, ADS#, W/R#, BRDY#, BRDYC#, HLDA, PM0/BP0, PM1/BP1, BP2, BP3	6 ns (Tsu min)	0.5 ns (Th min)
BOFF#, NA#, KEN#, AHOLD, PHIT#, INV, FERR#	2.5 ns (Tsu min)	2 ns (Th min)
All other signals	3.5 ns (Tsu min)	2 ns (Th min)

	Specification		
	AC load (by probe adapter)		DC load
Measured typical SUT signal loading	Conventional	Low-profile	
CLK	25 pF	26 pF	1 CY7B991 (standard)
			1 CY7B991 in parallel with 100 Ω + 15 pF (low-profile)
A31–A3	8–15 pF	8–15 pF	1 74FCT162501AT
D63–D0	8–15 pF	10–17 pF	1 74FCT162501AT
BE7#–BE0#	16–18 pF	18–19 pF	1 74FCT162501AT in parallel with 22V10
PM0/BP0, PM1/BP1#, BP2, BP3	9–10 pF	10–17 pF	1 16V8
CACHE#, SCYC, M/IO#, D/C#, RESET, D/P#, STPCLK#, EADS#, LOCK#, SMIACT#, BUSCHK#, TDO	8–13 pF	10–16 pF	1 74FCT162501AT
ADS#, W/R#, BRDY#, HLDA, ADSC#	8–12 pF	9–13 pF	1 22V10
BRDYC#	10 pF	10 pF	10K in parallel with 22V10
KEN#	15 pF	15 pF	10K in parallel with 74FCT646AT
PRDY, RESET, D/P#	16–19 pF	18–29 pF	1 74FCT162501AT
DP7-DP0	8–12 pF	13–15 pF	1 74FCT162501AT
BOFF#, NA#, AHOLD, PHIT#, INV, FERR#	11–13 pF	12–14 pF	1 74FCT646AT
All other signals	5–9 pF	5–9 pF	1 74FCT162501AT
Not connected signals	2 pF	2 pF	none

Table 3–3 shows the environmental specifications.

Table 3–3: Environmental specifications*

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F)†
Minimum operating	0° C (+32° F)
Non-operating	–55° C to +75° C (–67° to +167° F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

* **Designed to meet Tektronix standard 062-2847-00 class 5.**

† **Not to exceed P54/P55 microprocessor thermal considerations. Forced air cooling might be required across the CPU.**

Table 3–4 shows the certifications and compliances that apply to the probe adapter.

Table 3–4: Certifications and compliances

EC Compliance	There are no current European Directives that apply to this product.

Figure 3–2 shows the dimensions of the low-profile probe adapter. The figure also shows the minimum vertical clearance of the high-density probe cable.
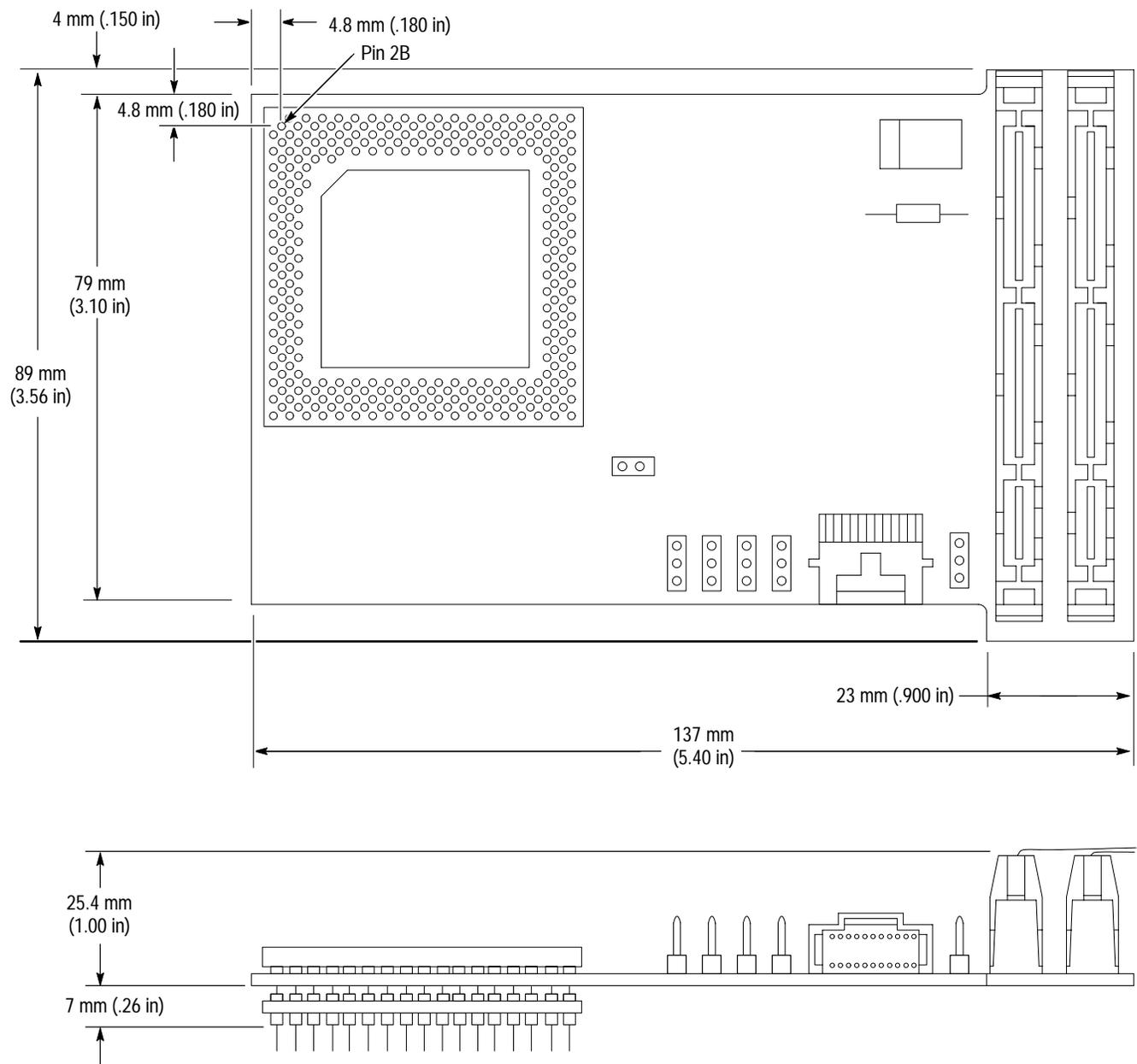
Figure 3–1: Dimensions of the low-profile probe adapter

Figure 3–2 shows the dimensions of the conventional probe adapter. Information on basic operations shows the vertical clearance of the channel and clock probes when connected to a probe adapter.
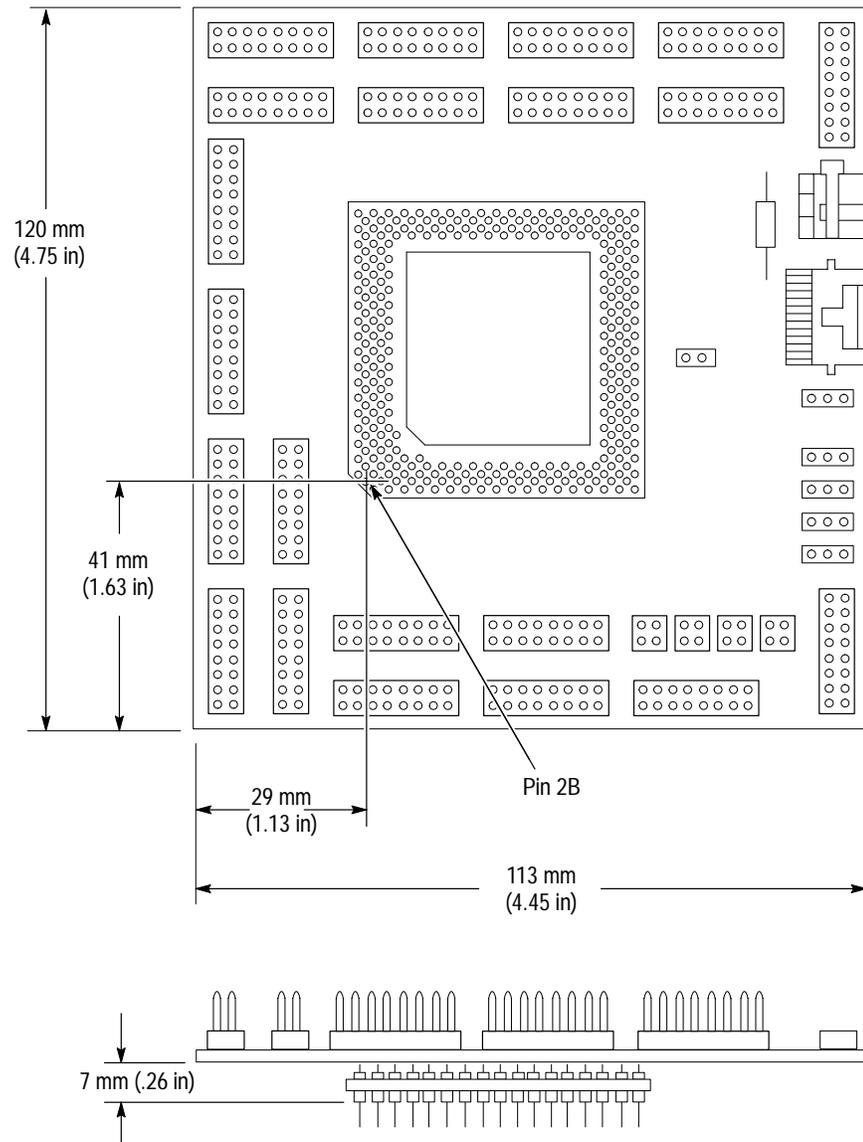
Figure 3–2: Dimensions of the conventional probe adapter

Channel Assignments   Channel assignments shown in Table 3–5 through Table 3–18 use the following conventions:

- All signals are required by the support unless indicated otherwise.

- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).

- Channel group assignments are for all modules unless otherwise noted.

- A pound sign (#) following a signal name indicates an active low signal.

- If there are two modules (such as used to form 192-channels), the module in the higher-numbered slot is referred to as the HI module and the module in the lower-numbered slot is referred to as the LO module.

Table 3–5 shows the probe section and channel assignments for the Address group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–5: Address group channel assignments

Bit order	136-channel section & probe	192-channel section & probe	P54/P55 signal name
31	A3:7	LO_A3:7	A31
30	A3:6	LO_A3:6	A30
29	A3:5	LO_A3:5	A29
28	A3:4	LO_A3:4	A28
27	A3:3	LO_A3:3	A27
26	A3:2	LO_A3:2	A26
25	A3:1	LO_A3:1	A25
24	A3:0	LO_A3:0	A24
23	A2:7	LO_A2:7	A23
22	A2:6	LO_A2:6	A22
21	A2:5	LO_A2:5	A21
20	A2:4	LO_A2:4	A20
19	A2:3	LO_A2:3	A19
18	A2:2	LO_A2:2	A18
17	A2:1	LO_A2:1	A17
16	A2:0	LO_A2:0	A16
15	A2:7	LO_A1:7	A15
14	A1:6	LO_A1:6	A14
13	A1:5	LO_A1:5	A13
12	A1:4	LO_A1:4	A12
11	A1:3	LO_A1:3	A11
10	A1:2	LO_A1:2	A10
9	A1:1	LO_A1:1	A9
8	A1:0	LO_A1:0	A8
7	A0:7	LO_A0:7	A7
6	A0:6	LO_A0:6	A6
5	A0:5	LO_A0:5	A5
4	A0:4	LO_A0:4	A4
3	A0:3	LO_A0:3	A3
2	A0:2	LO_A0:2	A2*
1	A0:1	LO_A0:1	A1*
0	A0:0	LO_A0:0	A0*

*　　Synthesized on the probe adapter from the BE7#-BE0# signals when the Address Synthesis jumper is positioned on pins1 and 2.

Table 3–6 shows the probe section and channel assignments for the Data group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–6: Data group channel assignments

Bit order	136-channel section & probe	192-channel section & probe	P54/P55 signal name
31	E3:7	HI_A3:7	D63
30	E3:6	HI_A3:6	D62
29	E3:5	HI_A3:5	D61
28	E3:4	HI_A3:4	D60
27	E3:3	HI_A3:3	D59
26	E3:2	HI_A3:2	D58
25	E3:1	HI_A3:1	D57
24	E3:0	HI_A3:0	D56
23	E2:7	HI_A2:7	D55
22	E2:6	HI_A2:6	D54
21	E2:5	HI_A2:5	D53
20	E2:4	HI_A2:4	D52
19	E2:3	HI_A2:3	D51
18	E2:2	HI_A2:2	D50
17	E2:1	HI_A2:1	D49
16	E2:0	HI_A2:0	D48
15	E1:7	HI_A1:7	D47
14	E1:6	HI_A1:6	D46
13	E1:5	HI_A1:5	D45
12	E1:4	HI_A1:4	D44
11	E1:3	HI_A1:3	D43
10	E1:2	HI_A1:2	D42
9	E1:1	HI_A1:1	D41
8	E1:0	HI_A1:0	D40
7	E0:7	HI_A0:7	D39
6	E0:6	HI_A0:6	D38
5	E0:5	HI_A0:5	D37
4	E0:4	HI_A0:4	D36
3	E0:3	HI_A0:3	D35
2	E0:2	HI_A0:2	D34
1	E0:1	HI_A0:1	D33
0	E0:0	HI_A0:0	D32

Table 3–7 shows the probe section and channel assignments for the Data_Lo group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–7: Data_Lo group channel assignments

Bit order	136-channel section & probe	192-channel section & probe	P54/P55 signal name
31	D3:7	LO D3:7	D31
30	D3:6	LO D3:6	D30
29	D3:5	LO D3:5	D29
28	D3:4	LO D3:4	D28
27	D3:3	LO D3:3	D27
26	D3:2	LO D3:2	D26
25	D3:1	LO D3:1	D25
24	D3:0	LO D3:0	D24
23	D2:7	LO D2:7	D23
22	D2:6	LO D2:6	D22
21	D2:5	LO D2:5	D21
20	D2:4	LO D2:4	D20
19	D2:3	LO D2:3	D19
18	D2:2	LO D2:2	D18
17	D2:1	LO D2:1	D17
16	D2:0	LO D2:0	D16
15	D1:7	LO D1:7	D15
14	D1:6	LO D1:6	D14
13	D1:5	LO D1:5	D13
12	D1:4	LO D1:4	D12
11	D1:3	LO D1:3	D11
10	D1:2	LO D1:2	D10
9	D1:1	LO D1:1	D9
8	D1:0	LO D1:0	D8
7	D0:7	LO D0:7	D7
6	D0:6	LO D0:6	D6
5	D0:5	LO D0:5	D5
4	D0:4	LO D0:4	D4
3	D0:3	LO D0:3	D3
2	D0:2	LO D0:2	D2
1	D0:1	LO D0:1	D1
0	D0:0	LO D0:0	D0

Table 3–8 shows the probe section and channel assignments for the Control group and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–8: Control group channel assignments

Bit order	136-channel section & probe	192-channel section & probe	P54/P55 signal name
14	C0:7	HI C2:7	D/P#
13	C3:0	LO C3:0	INIT
12	C2:0	LO C2:0*	RESET_L
11	C3:6	LO C3:6	PRDY†
10	C3:5	LO C3:5	BUSCHK#
9	C2:5	LO C2:5	SMIACT#
8	C2:6	LO C2:6	LOCK#
7	C0:6	HI C2:6	SCYC
6	C2:4	LO C2:4	LAST_D
5	C0:4	HI C2:4	AHOLD
4	C2:2	LO C2:2*	HLDA
3	C2:1	LO C2:1*	BOFF#
2	C2:7	LO C2:7*	M/IO#
1	C3:7	LO C3:7	D/C#
0	C3:3	LO C3:3	W/R#

*   **Both HI and LO are used for clocking, only the LO is displayed.**

†   **This signal is not required for disassembly.**

Table 3–9 shows the probe section and channel assignments for the DataSize group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in binary.

Table 3–9: DataSize group channel assignments

Bit order	136-channel section & probe	192-channel section & probe	P54/P55 signal name
7	C1:7	HI C3:7	BE7#
6	C1:6	HI C3:6	BE6#
5	C1:5	HI C3:5	BE5#
4	C1:4	HI C3:4	BE4#
3	C1:3	HI C3:3	BE3#
2	C1:2	HI C3:2	BE2#
1	C1:1	HI C3:1	BE1#
0	C1:0	HI C3:0	BE0#

Table 3–10 shows the 136-channel module probe section and channel assignment for the Cache group and the microprocessor signal to which the channel connects. By default, this channel group is not visible.

Table 3–10: 136-channel module: Cache group channel assignment

Bit order	Section: channel	P54/P55 signal name
0	C0:5	CACHE#*

*   **This signal is not required for disassembly.**

Table 3–11 shows the 136-channel module probe section and channel assignments for the Misc group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–11: 136-channel module: Misc group channel assignments

Bit Order	Section:channel	P54/P55 signal name
3	C3:1	CLK*
2	C2:3	ADS#*
1	C3:2	NA#*
0	C3:4	BRDY#*

*   **This signal is not required for disassembly.**

Table 3–12 shows the 192-channel module probe section and channel assignments for the Cache group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–12: 192-channel module: Cache group channel assignments

Bit order	Section: channel	P54/P55 signal name
9	HI C2:5	CACHE#*
8	HI D2:6	KEN#*
7	HI D3:0	EADS#*
6	HI D3:4	FLUSH#*
5	HI D3:7	PCD*
4	HI D3:3	PWT*
3	HI D1:4	HIT#*
2	HI D1:5	HITM#*
1	HI D2:7	INV*
0	HI D3:1	WB/WT#*

*   **This signal is not required for disassembly.**

Table 3–13 shows the 192-channel module probe section and channel assignments for the Debug group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–13: 192-channel module: Debug group channel assignments

Bit Order	Section:channel	P54/P55 signal name
4	HI D2:4	BP3*
3	HI D2:5	BP2*
2	HI D2:2	PM1/BP1*
1	HI D2:3	PM0/BP0*
0	HI D0:7	R/S#*

*   **This signal is not required for disassembly.**

Table 3–14 shows the 192-channel module probe section and channel assignments for the APIC group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–14: 192-channel module: APIC group channel assignments

Bit Order	Section:channel	P54/P55 signal name
2	HI D0:6	PICCLK*
1	HI D0:5	PICD0*
0	HI D0:4	PICD1*

* **This signal is not required for disassembly.**

Table 3–15 shows the 192-channel module probe section and channel assignments for the Priv_Bus group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–15: 192-channel module: Priv_Bus group channel assignments

Bit Order	Section:channel	P54/P55 signal name
3	HI D1:0	PBREQ#*
2	HI D1:1	PBGNT#*
1	HI D1:2	PHIT#*
0	HI D1:3	PHITM#*

* **This signal is not required for disassembly.**

Table 3–16 shows the 192-channel module probe section and channel assignments for the Parity group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–16: 192-channel module: Parity group channel assignments

Bit Order	Section: channel	P54/P55 Signal Name
7	HI C1:7	DP7*
6	HI C1:6	DP6*
5	HI C1:5	DP5*
4	HI C1:4	DP4*
3	HI C1:3	DP3*
2	HI C1:2	DP2*

Table 3–16: 192-channel module: Parity group channel assignments (cont.)

Bit Order	Section: channel	P54/P55 Signal Name
1	HI C1:1	DP1*
0	HI C1:0	DP0*

* **This signal is not required for disassembly.**

Table 3–17 shows the 192-channel module probe section and channel assignments for the Misc group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–17: 192-channel module: Misc group channel assignments

Bit Order	Section:channel	P54/P55 signal name
14	LO C3:1	CLK*
13	LO C2:3†	ADS#*
12	LO C3:2	NA#*
11	LO C3:4	BRDY#*
10	HI D2:0	BRDYC#*
9	HI D0:2	PEN#*
8	HI D3:6	APCHK#*
7	HI D3:2	PCHK#*
6	HI D0:0	STPCLK#*
5	HI D0:3	NMI*
4	HI D1:6	INTR*
3	HI D1:7	SMI#*
2	HI D0:1	IGNNE#*
1	HI D2:1	FERR#*
0	HI D3:5	HOLD*

* **This signal is not required for disassembly.**

† **Both HI and LO are used for clocking, but only the LO is displayed.**

Table 3–18 shows the probe section and channel assignments for the clock channels (not part of any group), and the signal to which each channel connects. For the 192-channel module, assignments are the same for HI and LO modules. An _D following a signal name indicates a signal derived on the probe adapter.

Table 3–18: Clock channel assignments

Clock channel	P54/P55 signal name	Clk or Qual
CLK3	CLK=*	CLK, rising
CLK2	LAST_D=*	QUAL
CLK1	PIPE_D=†	QUAL
CLK0	DVALID_D=†	QUAL

*   **Double probed when using a 136-channel module and triple probed when using a 192-channel module.**

†   **Single probed when using a 136-channel module and double probed when using a 192-channel module.**

These channels are used only to clock in data; they are not acquired or displayed. To acquire data from any of the signals shown in Table 3–18, you must connect another channel probe to the signal, a technique called double probing.

Mode Differences

The P54/P55 microprocessor can operate in either Component or Chip Set mode.

Component Mode

In Component mode (stand alone), the microprocessor interfaces directly to the system bus.

Chip Set Mode

The P54/P55 microprocessor, C5C cache controller, and the C8C cache memory (SRAM) can be combined to form a chip set or enhanced design. The two cache devices connect to the system bus and a memory bus controller interfaces to the microprocessor and cache devices.

The behavior of the P54/P55 microprocessor is affected when operating in Chip Set mode. The TMS 109 software and probe adapter still supports the P54/P55 microprocessor in this mode.

There are also two new signals: BRDYC# (pin L3) and ADSC# (pin N4).

In Component mode, the BRDYC# signal is seen as a "no connect" pin. The TMS 109 probe adapter uses the BRDYC# signal for clocking when it is active. The probe adapter has a pullup resistor on this line to hold it inactive when the P54/P55 is in Chip-Set mode. The BRDYC# signal can be probed on C1:0.

In Component mode, the ADSC# signal is seen as a "no connect" pin and is not used for clocking by the probe adapter.

How Data is Acquired

This part of this chapter explains how the module acquires P54/P55 signals using the TMS 109 software and probe adapter. This part also provides additional information on microprocessor signals accessible on or not accessible on the probe adapter, and on extra probe channels available for you to use for additional connections.

Custom Clocking

A special clocking program is loaded to the module every time you load the P54C support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple groups of channels at different times as they become valid on the P54/P55 bus. The module then sends all the logged-in signals to the trigger machine and to the memory of the module for storage.

In Custom clocking, the module clocking state machine (CSM) generates one master sample for each microprocessor bus cycle, no matter how many clock cycles are contained in the bus cycle.

Figure 3–3 shows two typical bus cycles: a single cycle transfer followed by a burst transfer. The ADS#, Address and Data signal forms are delayed by two CLK cycles. This diagram also shows the timing relationships of LAST_D and DVALID_D, the signals synthesized by sequential logic in the PALs.
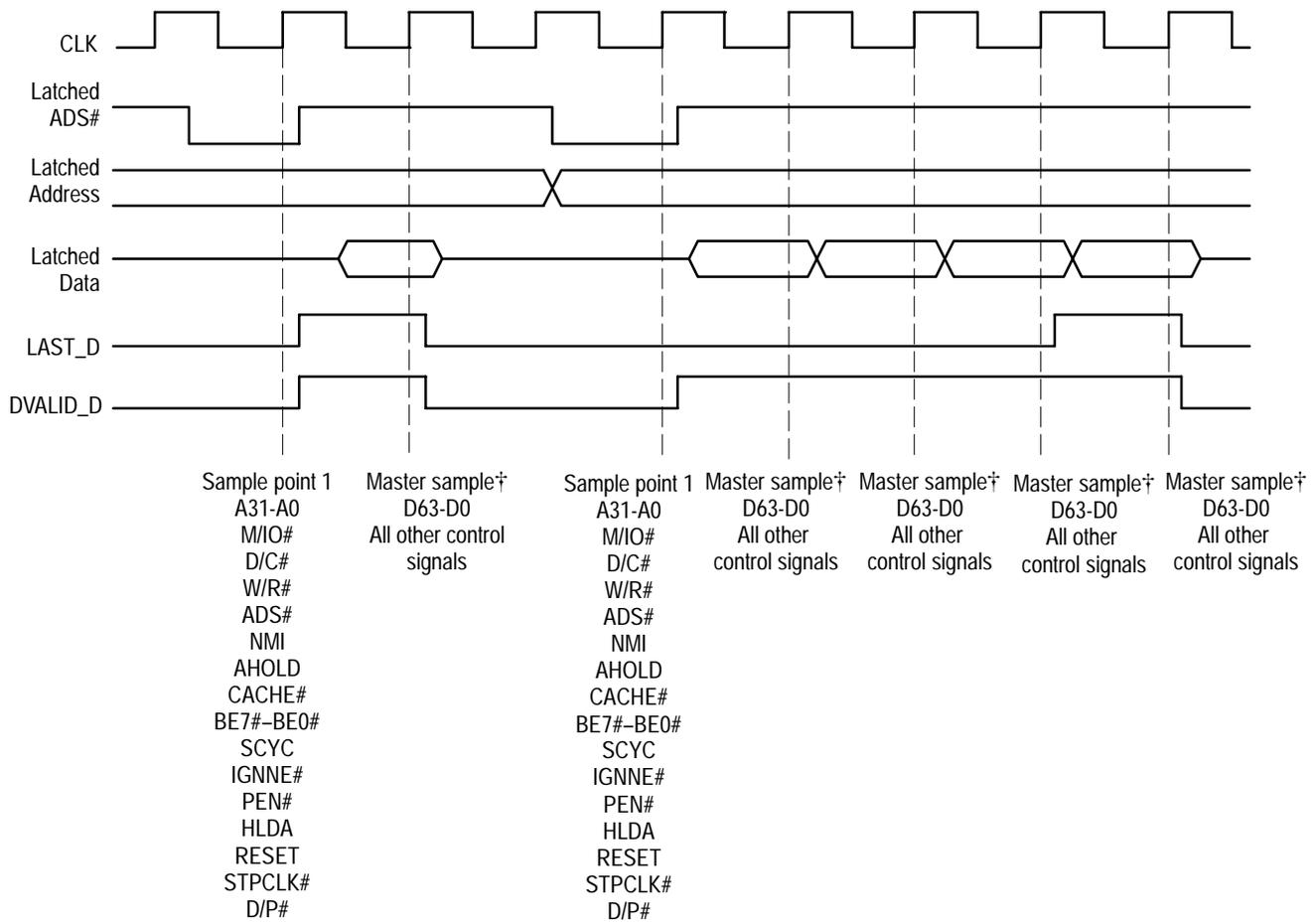
†Channels not set up in a channel group by the TMS 109 software are logged with the Master sample.

Figure 3–3: Nonpipelined single and Burst Transfer cycles

Relative to real time, nondelayed P54/P55 microprocessor signals, the first sample point in a cycle occurs two clocks after the ADS# signal is asserted. The second (and subsequent, if the cycle is a burst) sample point occurs two clocks after the BRDY# or BRDYC# signal.

Figure 3–4 shows a single cycle transfer pipelined into another single cycle transfer. The ADS#, Address and Data signal forms are delayed by two CLK cycles. This diagram also shows the timing relationships of LAST_D, DVALID_D, and PIPE_D, which are the signals synthesized by sequential logic in the PALs.

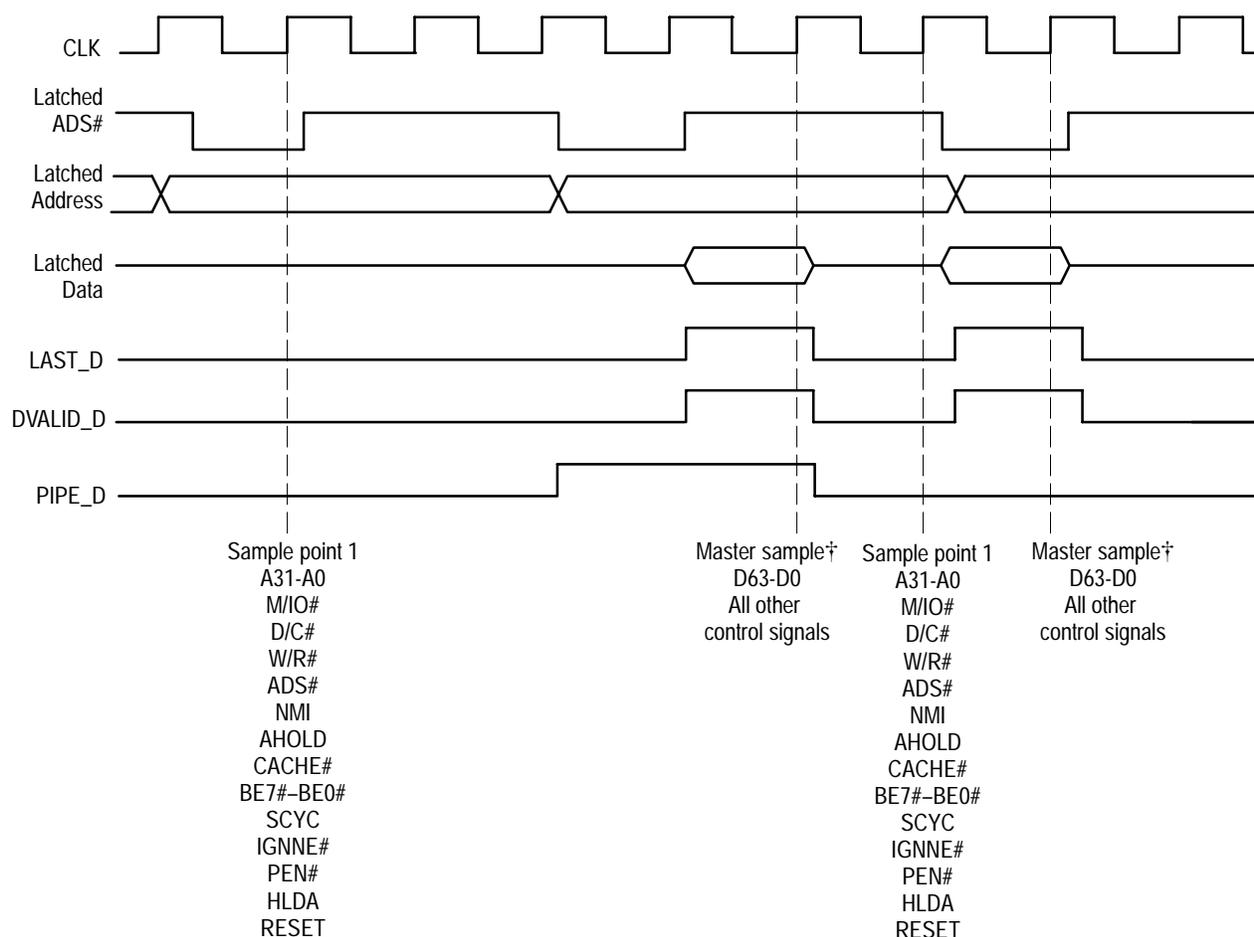|	Sample point 1	Master sample†	Sample point 1	Master sample†
	A31-A0	D63-D0	A31-A0	D63-D0
	M/IO#	All other	M/IO#	All other
	D/C#	control signals	D/C#	control signals
	W/R#		W/R#	
	ADS#		ADS#	
	NMI		NMI	
	AHOLD		AHOLD	
	CACHE#		CACHE#	
	BE7#–BE0#		BE7#–BE0#	
	SCYC		SCYC	
	IGNNE#		IGNNE#	
	PEN#		PEN#	
	HLDA		HLDA	
	RESET		RESET	

†Channels not set up in a channel group by the TMS 109 software are logged with the Master sample.

Figure 3–4: Pipelined cycles

With relationship to real time, nondelayed P54/P55 microprocessor signals, the first sample point in a cycle occurs two clocks after the ADS# signal is asserted. When the ADS# signal is asserted again to pipeline a second cycle into the first, the first sample point for that second cycle occurs three clocks after the last BRDY# or BRDYC# signal is returned from the first outstanding cycle.

ClockingOptions
The clocking algorithm for the P54/P55 microprocessor has two variations: Alternate Bus Master Cycles Excluded and Alternate Bus Master Cycles Included.

Alternate Bus Master Cycles Excluded. Whenever the HLDA signal is high, no bus cycles are logged in. Only bus cycles driven by the microprocessor (HLDA low) will be logged in. Backoff cycles (caused by the BOFF# signal) are stored.

Alternate Bus Master Cycles Included. All bus cycles, including alternate bus master cycles and backoff cycles, are logged in.

When the HLDA signal is high, the microprocessor has given up the bus to an alternate device. The design of the P54/P55 microprocessor system affects what data will be logged in. The module only samples the data at the pins of the microprocessor. To properly log in bus activity, any buffers between the microprocessor and the alternate bus master must be enabled and pointing at the P54/P55 microprocessor.

There are three possible P54/P55 microprocessor system designs and clocking interactions when an alternate bus master has control of the bus. The three different possibilities are listed below (in each case, the HLDA signal is logged in as a high level):

■ If the alternate bus master drives the same control lines as the P54/P55 microprocessor, and the P54/P55 microprocessor "sees" these signals, the bus activity is logged in like normal bus cycles except that the HLDA signal is high.

■ If none of the control lines are driven or if the P54/P55 microprocessor can not see them, the module will still clock in an alternate bus master cycle. The information on the bus, one clock prior to the HLDA signal going low, is logged in. If the ADS# signal goes low on the same clock when the HLDA signal goes low, the address that gets logged in will be the next address, not the address that occurred one clock before the HLDA signal went low.

■ If some of the P54/P55 microprocessor control lines are visible (but not all), the module logs in the signals it determines is valid from the control signals and logs in the remaining bus signals one clock cycle prior to the HLDA signal going low. If the ADS# signal goes low on the same clock that the HLDA signal goes low, the next address will be logged instead of the previously saved address.

When the BOFF# signal goes low (active), a backoff cycle has been requested, and the P54/P55 microprocessor gives up the bus on the next clock cycle. The module aborts the bus cycle that it is currently logging in (the P54/P55 microprocessor will restart this cycle once the BOFF# signal goes high). A backoff cycle will be logged in using one of the three interactions described for the HLDA signal (except that the BOFF# signal is stored as a low-level signal in each of the cases).

Alternate Microprocessor Connections

You can connect to microprocessor signals that are not required for disassembly so you can do more advanced timing analysis. These signals may or may not be accessible on the probe adapter board. The following paragraphs and tables list channels that are or are not accessible on the probe adapter board.

For a list of signals required or not required for disassembly, refer to the channel assignment tables starting on page 3–7.

Signals On the Probe Adapter

The probe adapter board contains pins for microprocessor signals that are not acquired by the support software.

Table 3–19 lists the pin-to-signal assignments of the In Target Probe (ITP) connector J1140 on the conventional probe adapter or J1700 on the low-profile probe adapter. The connector allows you to make connections from your ITP signals to the microprocessor on the probe adapter.

Table 3–19: P54/P55 signals on J1140/J1700

Jumper pin number	Signal name	Jumper pin number	Signal name
1	INIT_B*	11	PRDY*
2	DRESET	12	TDI†
3	RESET_B*	13	TDO*†
4	Ground	14	TMS†
5	Not connected	15	Ground
6	1 KΩ pullup to + 5V	16	TCK†
7	R/S#	17	Ground
8	Ground	18	TRST#†
9	Not connected	19	Not connected
10	Ground	20	Not connected

* Signal has a 27.4 Ω series resistor termination on the probe adapter.

† ITP signal.

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.

Figure 3–5 shows the location of the ITP connector, J1140, on the conventional probe adapter.

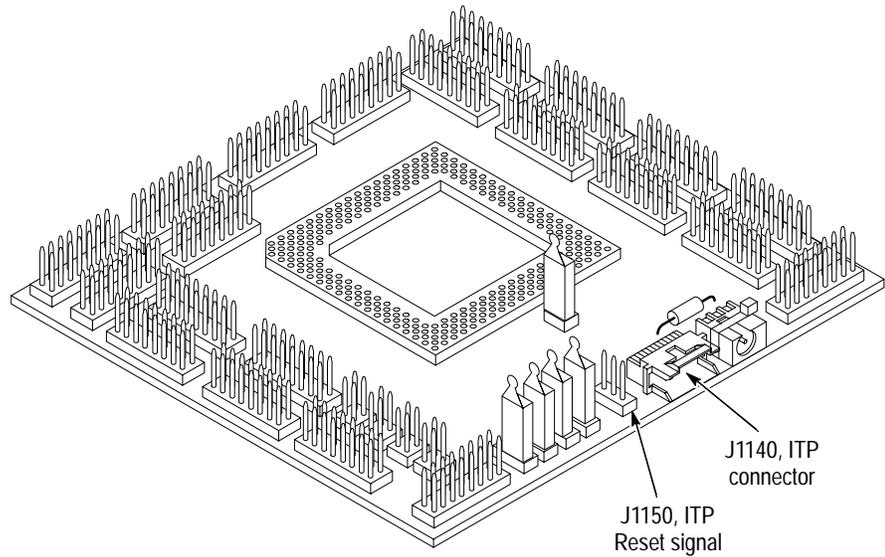**Figure 3–5: Location of J1140 and J1150 on the conventional probe adapter**

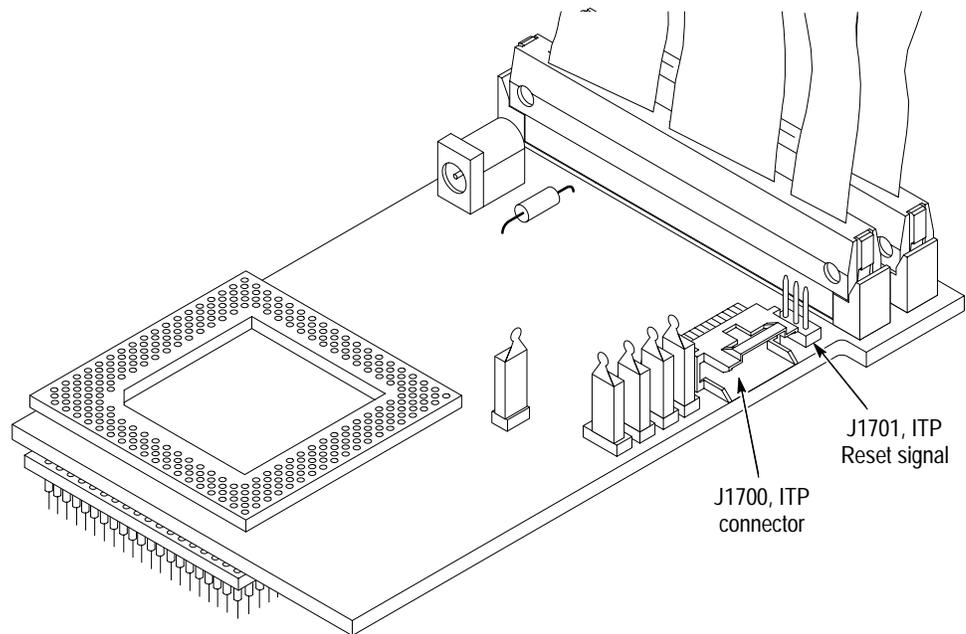Figure 3–6 shows the location of the ITP connector, J1700, on the low-profile probe adapter.

Figure 3–6: Location of J1700 and J1701 on the low-profile probe adapter

The probe adapter contains pins that allow you to connect the DBRESET (or the active low, open collector version OC_DBRESET#) signal to your SUT. Table 3–20 shows the pins and signals you can connect to on J1150 on the conventional probe adapter or J1701 on the low-profile probe adapter.

When using these signals, you need to make sure that the SUT is not driving the OC_DBRESET# or DBRESET signal.

You need to also make sure that the R/S#, TDI, TMS, TCLK, and TRST# signals are not driven. If this is not possible, you may clip these five pins on one of the sacrificial sockets provided with the probe adapter. Inserting this modified socket into your system socket will isolate these signals on the probe adapter for use by the ITP cable. For more information on the ITP, refer to the *ITP-502 In-target Probe Configuration Guide* by Intel Corporation.

Table 3–20: J1150/J1701 jumper pin assignments

Jumper pin number	P54/P55 signal name
1	OC_DBRESET# (Open Collector, active low version of DBRESET)
2	N/C
3	DBRESET

Figure 3–5 shows the location of jumper J1150 on the conventional probe adapter; Figure 3–6 shows the location of jumper J1701 on the low-profile probe adapter.

Signals Not On the Probe Adapter

P54/P55 microprocessor signals that are not accessible on the probe adapter are:

A20M#	BREQ	FRCMC#
ADSC#	EWBE#	IERR#
AP		

Extra Channels

Table 3–21 lists extra sections and channels that are left after you have connected all the probes used by the support. You can use these extra channels to make alternate SUT connections.

Table 3–21: Extra channels

Module	Channel	Description
192-channels	HI_C0:0–7	If you use these channels to connect to other signals in your SUT, they will be logged in one CPU clock after BRDY# (or BRDYC#) goes active for every transfer.
	LO_C0:0–7	If you use these channels to connect to other signals in your SUT, they will be logged in on the same CPU clock edge as D63-D0 for every transfer; that is, whenever BRDY# (or BRDYC#) is active.
	LO_C1:0–7	
136-channels	Qual:3-0	Extra channels

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.

Signals on the High-Density Probe

Table 3–22 lists P54/P55 signals that are not connected on the high-density probe for the 136-channel module. (The 192-channel module connects to these signals.) You can disconnect channel probes attached to microprocessor signals not required for disassembly to connect to these signals on the high-density probe.

For a list of signals required or not required for disassembly, refer to the channel assignment tables starting on page 3–7.

Table 3–22: 136-channel module: Signals on the high-density probe

Section: channel	P54/P55 signal	Section: channel	P54/P55 signal
HI_D3:7	PCD	HI_D1:7	SMI#
HI_D3:6	APCHK#	HI_D1:6	INTR
HI_D3:5	HOLD	HI_D1:5	HITM#
HI_D3:4	FLUSH#	HI_D1:4	HIT#
HI_D3:3	PWT	HI_D1:3	PHITM#
HI_D3:2	PCHK#	HI_D1:2	PHIT#
HI_D3:1	WB/WT#	HI_D1:1	PBGNT#
HI_D3:0	EADS#	HI_D1:0	PBREQ#
HI_D2:7	INV	HI_D0:7	R/S#
HI_D2:6	KEN#	HI_D0:6	PICCLK
HI_D2:5	BP2	HI_D0:5	PICD0
HI_D2:4	BP3	HI_D0:4	PICD1
HI_D2:3	PM0/BP0	HI_D0:3	NMI
HI_D2:2	PM1/BP1	HI_D0:2	PEN#

Table 3–22: 136-channel module: Signals on the high-density probe (Cont.)

Section: channel	P54/P55 signal	Section: channel	P54/P55 signal
HI_D2:1	FERR#	HI_D0:1	IGNNE#
HI_D2:0	BRDYC#	HI_D0:0	STPCLK#
HI_C1:7	DP7#	HI_C1:3	DP3#
HI_C1:6	DP6#	HI_C1:2	DP2#
HI_C1:5	DP5#	HI_C1:1	DP1#
HI_C1:4	DP4#	HI_C1:0	DP0#

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.

TMS 109 P54 & P55 Microprocessor Support Instruction Manual

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Maintenance

Maintenance

This chapter contains information on the following topics:

- Probe adapter circuit description

- How to replace a fuse

Probe Adapter Circuit Description

Both the conventional and low-profile probe adapters have the same circuit description. There are 21 active components on the probe adapter: three 22V10-7 PALs, seven 18-bit clocked latches, five 10-bit CMOS clocked latches, five 10-bit CMOS bus switch packages, and one PLL (phase locked loop) low-skew clock generator for clock distribution.

The PALs implement three sequential state machines that monitor the P54/P55 microprocessor bus and generate three important signals:

- PIPE_D indicates P54/P55 microprocessor bus pipelining is occurring

- LAST_D indicates the end of a P54/P55 microprocessor bus cycle

- DVALID_D indicates valid data is present on the P54/P55 microprocessor data bus

These signals are required for the Clocking State Machine (CSM) of the logic analyzer to accurately strobe addresses and data information from the P54/P55 microprocessor bus.

The P54/P55 microprocessor 32-bit address bus and those control signals valid with the address (for example W/R# and M/IO#) are latched with 74FCT162501 transceivers and held with ADS# in 74FCT2823 latches until the next ADS#. This makes the signals available for a longer time than the minimum time on the P54/P55 microprocessor. Latching also provides low loading and the shortest possible setup and hold time windows.

The P54/P55 microprocessor 64-bit data bus and some of the control signals are latched to realign the signals with the PIPE_D, LAST_D, and DVALID_D outputs from the PAL.

A PLL clock generator is used to provide eight, zero-delay copies of the P54/P55 microprocessor CLK input that are distributed to the latches and PALs.

The probe adapter uses up to two CLK periods of delay to realign signals for acquisition. Table 4–1 shows the relative signal delays when using the probe adapter. The Hardware CLK Delays column lists the number of clocks that signals are delayed on the probe adapter board when the Disassembly/timing jumper (J1160 on the conventional probe adapter or J1500 on the low-profile probe adapter) is in the D position. The Firmware CLK Delays column lists the number of clocks that signals are delayed by the CSM when P54C Custom clocking is selected. Hardware clock delays and firmware clock delays are additive.

Table 4–1: Microprocessor signal delays when using the probe adapter

Signal names	Hardware CLK delays	Firmware (CSM) CLK delays
A31–0, BE7–0#, ADS#, D/C#, W/R#, M/IO#, CACHE#, SCYC, AHOLD, D/P#	2	0
BOFF#	2	1
HLDA, D63–0, EADS#, LOCK#, SMIACT#, BUSCHK#, PRDY, DP(7:0), INIT, PCD, APCHK#, HOLD, FLUSH#, PWT, PCHK#, WB/WT#, INTR, HITM#, HIT#, SMI#, R/S#, CLK	1	1
RESET BRDY#, NA#, BRDYC#, KEN#, STPCLK#, INV, FERR#, NMI, PEN#, IGNNE#	1	0
BP2, BP3, PM0/BP0, PM1/BP1	*	1

* **These signals are latched after assertion and held until after the deassertion of BRDY# (or BRDYC#).**

When J1160/J1500 is in the T position, all hardware clock delays are zero, which makes the probe adapter transparent for timing measurements. All circuitry on the probe adapter is bypassed, changing all the latches to buffers and sending the P54/P55 microprocessor signals straight through to the podlets. Signal relationships are maintained with the addition of six ns maximum delay for those signals connected through buffers. Any signal that has a hardware clock delay identified in Table 4–1 will have a six ns maximum delay through the probe adapter.

There is one pullup resistor on the BRDYC# signal on the probe adapter. When the P54/P55 microprocessor is operating in normal (or component) mode, the pullup resistor pulls this signal high, which causes the acquisition module to see the BRDYC# signal as inactive. When the P54/P55 microprocessor is operating in Chip-Set mode, the pullup is overdriven.

Replacing Signal Leads

Information on basic operations describes how to replace signal leads (individual channel and clock probes).

Replacing Protective Sockets

Information on basic operations describes how to replace protective sockets.

Replacing the Fuse

If the fuse on the P54/P55 probe adapter opens (burns out), you can replace it with a 5 A, 125 V fuse. Figure 4–1 shows the location of the fuse on the conventional probe adapter board. Figure 4–2 shows the location of the fuse on the low-profile probe adapter board.
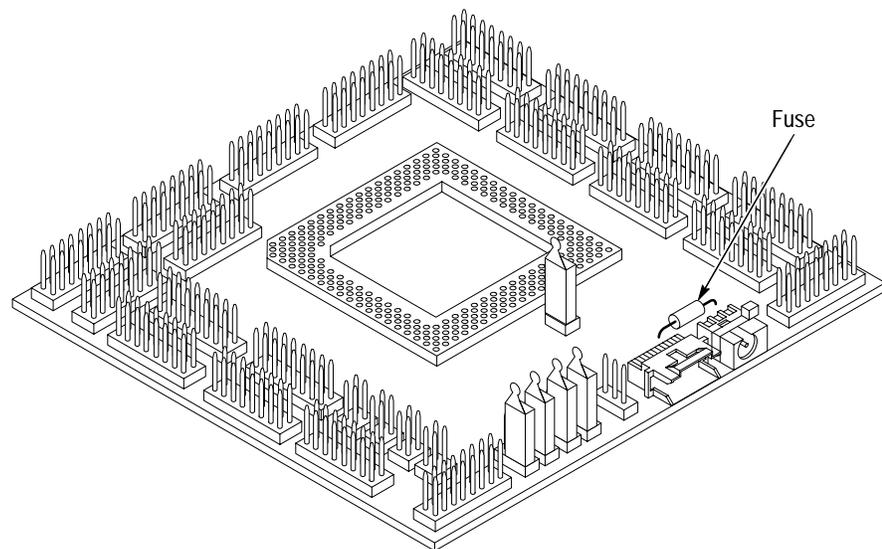

Fuse

Figure 4–1: Location of the fuse on the conventional probe adapter
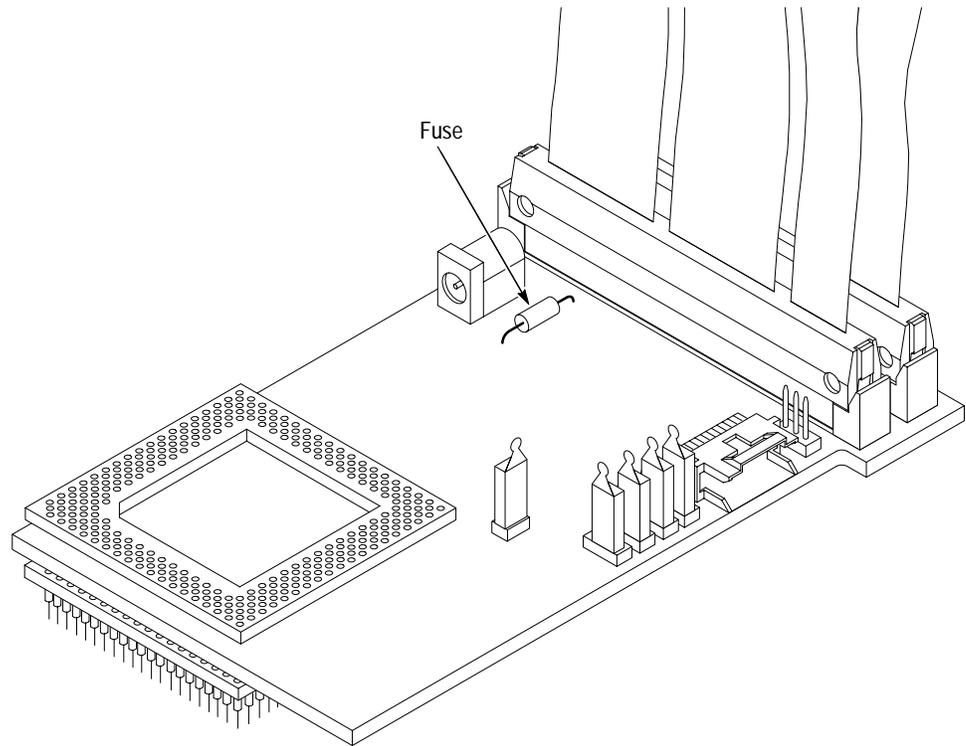
Fuse

Figure 4–2: Location of the fuse on the low-profile probe adapter

Replaceable Electrical Parts

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 109 P54/P55 microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

■ Part number

■ Instrument type or model number

■ Instrument serial number

■ Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

Parts list column descriptions

Column	Column name	Description
1	Component number	The component number appears on diagrams and circuit board illustrations, located in the diagrams section. Assembly numbers are clearly marked on each diagram and circuit board illustration in the *Diagrams* section, and on the mechanical exploded views in the *Replaceable Mechanical Parts* list section. The component number is obtained by adding the assembly number prefix to the circuit number (see Component Number illustration following this table). The electrical parts list is arranged by assemblies in numerical sequence (A1, with its subassemblies and parts, precedes A2, with its subassemblies and parts). Chassis-mounted parts have no assembly number prefix, and they are located at the end of the electrical parts list.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
6	Mfr. code	This indicates the code number of the actual manufacturer of the part.
7	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations   Abbreviations conform to American National Standard ANSI Y1.1–1972.

Component Number

Component number

A23A2R1234   **A23**   **A2**   **R1234**

Assembly number   Subassembly number   Circuit number
(optional)

Read: Resistor 1234 (of Subassembly 2) of Assembly 23

List of Assemblies   A list of assemblies is located at the beginning of the electrical parts list. The assemblies are listed in numerical order. When a part's complete component number is known, this list will identify the assembly in which the part is located.

Chassis Parts   Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index   The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
TK0875	MATSUO ELECTRONICS INC	831 S DOUBLAS ST	EL SEGUNDO CA 92641
TK2427	A/D ELECTRONIC	2121 17TH AVE SE	BOTHELL WA 97021
0LXM2	LZR ELECTRONICS INC	8051 CESSNA AVENUE	GAITHERSBURG MD 20879
0TJ19	QUALITY SEMICONDUCTOR INC	851 MARTIN AVENUE	SANTA CLARA CA 95050–2903
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
04222	AVX/KYOCERA DIV OF AVX CORP	19TH AVE SOUTH P O BOX 867	MYRTLE BEACH SC 29577
04713	MOTOROLA INC SEMICONDUCTOR PRODUCTS SECTOR	5005 E MCDOWELL RD	PHOENIX AZ 85008–4229
26742	METHODE ELECTRONICS INC	7447 W WILSON AVE	CHICAGO IL 60656–4548
50139	ALLEN–BRADLEY CO ELECTRONIC COMPONENTS	1414 ALLEN BRADLEY DR	EL PASO TX 79936
50434	HEWLETT–PACKARD CO OPTOELECTRONICS DIV	370 W TRIMBLE RD	SAN JOSE CA 95131–1008
53387	3M COMPANY ELECTRONIC PRODUCTS DIV	3M AUSTIN CENTER	AUSTIN TX 78769–2963
57668	ROHM CORPORATION	15375 BARRANCA PARKWAY SUITE B207	IRVINE CA 92718
58050	TEKA PRODUCTS INC	45 SALEM ST	PROVIDENCE RI 02907
61772	INTEGRATED DEVICE TECHNOLOGY	3236 SCOTT BLVD	SANTA CLARA CA 95051
61857	SAN–0 INDUSTRIAL CORP	91–3 COLIN DRIVE	HOLBROOK NY 11741
63058	MCKENZIE TECHNOLOGY	910 PAGE AVENUE	FREMONT CA 94538
65786	CYPRESS SEMICONDUCTOR CORP	3901 N 1ST ST	SAN JOSE CA 95134–1506
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A01	671–3253–00			CKT BD ASSY:P54C/CM PGA–296 SOCKETED	80009	671325300
A02	671–3453–00			CKT BD ASSY:P54C/CM,PGA–296 SOCKETED,LOW PROFILE	80009	671345300
A01	671–3253–00			CKT BD ASSY:P54C/CM PGA–296 SOCKETED	80009	671325300
A01C1190	283–5188–00			CAP,FXD,CERAMIC:MLC:100PF,5%,100V,NPO,1206	04222	12061A0101JAT1A
A01C1215	283–5188–00			CAP,FXD,CERAMIC:MLC;100PF,5%,100V,NPO,1206	04222	12061A0101JAT1A
A01C1215	290–5005–00			CAP,FXD,TANT:;47UF,10%,10V,5.8MM X 4.6MM	TK0875	267M–1002–476–K
A01C1230	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01C1240	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01C1241	283–5188–00			CAP,FXD,CERAMIC:MLC;100PF,5%,100V,NPO,1206	04222	12061A0101JAT1A
A01C1320	283–5188–00			CAP,FXD,CERAMIC:MLC;100PF,5%,100V,NPO,1206	04222	12061A0101JAT1A
A01C1350	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01C1351	283–5188–00			CAP,FXD,CERAMIC:MLC;100PF,5%,100V,NPO,1206	04222	12061A0101JAT1A
A01C1470	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01C1515	283–5188–00			CAP,FXD,CERAMIC:MLC;100PF,5%,100V,NPO,1206	04222	12061A0101JAT1A
A01C1550	290–5005–00			CAP,FXD,TANT:;47UF,10%,10V,5.8MM X 4.6MM	TK0875	267M–1002–476–K
A01C1570	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01C1615	283–5188–00			CAP,FXD,CERAMIC:MLC;100PF,5%,100V,NPO,1206	04222	12061A0101JAT1A
A01C1645	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01C1660	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01C2240	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01C2250	283–5187–00			CAP,FXD,CERAMIC:MLC;15PF,5%,100V,NPO,1206	04222	12061A0150JAT1A
A01C2311	283–5188–00			CAP,FXD,CERAMIC:MLC;100PF,5%,100V,NPO,1206	04222	12061A0101JAT1A
A01C2313	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01C2315	283–5188–00			CAP,FXD,CERAMIC:MLC;100PF,5%,100V,NPO,1206	04222	12061A0101JAT1A
A01C2340	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01C2365	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01C2371	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01C2420	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01C2450	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01C2470	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01C2475	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01C2510	283–5188–00			CAP,FXD,CERAMIC:MLC;100PF,5%,100V,NPO,1206	04222	12061A0101JAT1A
A01C2520	283–5188–00			CAP,FXD,CERAMIC:MLC;100PF,5%,100V,NPO,1206	04222	12061A0101JAT1A
A01C2527	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01C2550	283–5188–00			CAP,FXD,CERAMIC:MLC;100PF,5%,100V,NPO,1206	04222	12061A0101JAT1A
A01C2570	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01C2575	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01C2625	283–5188–00			CAP,FXD,CERAMIC:MLC;100PF,5%,100V,NPO,1206	04222	12061A0101JAT1A
A01C2670	283–5188–00			CAP,FXD,CERAMIC:MLC;100PF,5%,100V,NPO,1206	04222	12061A0101JAT1A
A01C2675	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A

Replaceable electrical parts list (cont.)

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A01C2677	283–5188–00			CAP,FXD,CERAMIC:MLC;100PF,5%,100V,NPO,1206	04222	12061A0101JAT1A
A01C2680	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A01F1220	159–0059–00			FUSE,WIRE LEAD:5A,125V,	61857	SPI–5A
A01J1100	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1140	131–4406–00			CONN,HDR:PCB,;MALE,RTANG,2 X 10,0.05 X 0.1CTR,0.350 H X 0.100TAIL,CTR PLZ,LATCHING,30	00779	104069–1
A01J1150	131–4530–00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230MLG X 0.120 TAIL,30GOLD,BD RETENTION	00779	104344–1
A01J1155	131–4530–00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230MLG X 0.120 TAIL,30GOLD,BD RETENTION	00779	104344–1
A01J1160	131–4530–00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230MLG X 0.120 TAIL,30GOLD,BD RETENTION	00779	104344–1
A01J1165	131–4530–00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230MLG X 0.120 TAIL,30GOLD,BD RETENTION	00779	104344–1
A01J1170	131–4530–00			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230MLG X 0.120 TAIL,30GOLD,BD RETENTION	00779	104344–1
A01J1190	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1200	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1210	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1290	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1295	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1340	131–1857–00			CONN,HDR:PCB,;MALE,STR,1 X 36,0.1 CTR,0.230	58050	082–3644–SS10
A01J1390	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1395	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1398	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1400	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1410	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1490	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1497	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1500	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1510	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1590	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1597	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1600	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1610	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1625	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1650	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1660	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1665	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1690	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A01J1695	131–5267–00			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB

Replaceable electrical parts list (cont.)

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A01JR1120	131–5148–00			JACK,POWER DC:PCB,;MALE,RTANG,2.0 MM DIAPIN,7 MM H X 3.3 MM TAIL,3COND,W/SWITCH,MTG POST,DC PWR JACK,1 AMP@12V	TK2427	ADC–016
A01P1155	–––––––––––			CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X2,0.1 CTR,0.630 H,BLK,W/HANDLE,JUMPER (SEE RMPL FIG.1)		
A01P1160	–––––––––––			CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X2,0.1 CTR,0.630 H,BLK,W/HANDLE,JUMPER (SEE RMPL FIG.1)		
A01P1165	–––––––––––			CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X2,0.1 CTR,0.630 H,BLK,W/HANDLE,JUMPER (SEE RMPL FIG.1)		
A01P1170	–––––––––––			CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X2,0.1 CTR,0.630 H,BLK,W/HANDLE,JUMPER (SEE RMPL FIG.1)		
A01P1340	–––––––––––			CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X2,0.1 CTR,0.630 H,BLK,W/HANDLE,JUMPER (SEE RMPL FIG.1)		
A01Q2250	151–5066–00			TRANSISTOR,SIG:MOS,N–CH;60V,0.115A,7.5 OHM	04713	2N7002LT1
A01R1150	321–5026–00			RES,FXD:THICK FILM;4.75K OHM,1%,0.125W,TC=100 PPM	50139	BCK4751FT
A01R1190	321–5006–00			RES,FXD:THICK FILM;100 OHM,1%,0.125W,TC=100	50139	BCK1000FT
A01R1235	321–5005–00			RES,FXD:THICK FILM;27.4 OHM,1%,0.125W,TC=100 PPM	57668	MCR18EZHFW 27E4
A01R1237	321–5018–00			RES,FXD:THICK FILM;1.0K OHM,1%,0.125W,TC=100 PPM	50139	BCK1001FT
A01R1315	321–5006–00			RES,FXD:THICK FILM;100 OHM,1%,0.125W,TC=100	50139	BCK1000FT
A01R1435	321–5005–00			RES,FXD:THICK FILM;27.4 OHM,1%,0.125W,TC=100 PPM	57668	MCR18EZHFW 27E4
A01R1515	321–5006–00			RES,FXD:THICK FILM;100 OHM,1%,0.125W,TC=100	50139	BCK1000FT
A01R1615	321–5006–00			RES,FXD:THICK FILM;100 OHM,1%,0.125W,TC=100	50139	BCK1000FT
A01R2245	321–5006–00			RES,FXD:THICK FILM;100 OHM,1%,0.125W,TC=100	50139	BCK1000FT
A01R2250	321–5030–00			RES,FXD:THICK FILM;10.0K OHM,1%,0.125W,TC=100 PPM	50139	BCK1002FT
A01R2270	321–5010–00			RES,FXD:THICK FILM;221 OHM,1%,0.125W,TC=100	50139	BCK221FT
A01R2271	321–5030–00			RES,FXD:THICK FILM;10.0K OHM,1%,0.125W,TC=100 PPM	50139	BCK1002FT
A01R2311	321–5006–00			RES,FXD:THICK FILM;100 OHM,1%,0.125W,TC=100	50139	BCK1000FT
A01R2313	321–5006–00			RES,FXD:THICK FILM;100 OHM,1%,0.125W,TC=100	50139	BCK1000FT
A01R2317	321–5005–00			RES,FXD:THICK FILM;27.4 OHM,1%,0.125W,TC=100 PPM	57668	MCR18EZHFW 27E4
A01R2370	321–5006–00			RES,FXD:THICK FILM;100 OHM,1%,0.125W,TC=100	50139	BCK1000FT
A01R2415	321–5006–00			RES,FXD:THICK FILM;100 OHM,1%,0.125W,TC=100	50139	BCK1000FT
A01R2417	321–5030–00			RES,FXD:THICK FILM;10.0K OHM,1%,0.125W,TC=100 PPM	50139	BCK1002FT
A01R2450	321–5005–00			RES,FXD:THICK FILM;27.4 OHM,1%,0.125W,TC=100 PPM	57668	MCR18EZHFW 27E4
A01R2500	321–5006–00			RES,FXD:THICK FILM;100 OHM,1%,0.125W,TC=100	50139	BCK1000FT
A01R2525	321–5006–00			RES,FXD:THICK FILM;100 OHM,1%,0.125W,TC=100	50139	BCK1000FT
A01R2550	321–5006–00			RES,FXD:THICK FILM;100 OHM,1%,0.125W,TC=100	50139	BCK1000FT
A01R2625	321–5006–00			RES,FXD:THICK FILM;100 OHM,1%,0.125W,TC=100	50139	BCK1000FT

Replaceable electrical parts list (cont.)

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A01R2627	321–5030–00			RES,FXD:THICK FILM;10.0K OHM,1%,0.125W,TC=100 PPM	50139	BCK1002FT
A01R2670	321–5006–00			RES,FXD:THICK FILM;100 OHM,1%,0.125W,TC=100	50139	BCK1000FT
A01R2675	321–5006–00			RES,FXD:THICK FILM;100 OHM,1%,0.125W,TC=100	50139	BCK1000FT
A01U1255	156–6879–00			IC,DIGITAL:CMOS,MISC;PROGRAMMABLE SKEW CLOCK BUFFER,TTL LEVEL	65786	CY7B991–5JC
A01U1270	163–0008–00			IC,DIGITAL:CMOS,PLD;OTP,22V10,7.5NS,190MA,PRGM 156–6516–00	80009	163–0008–00
A01U1315	156–6160–01			IC,DIGITAL:FCTCMOS,REGISTER;9–BIT,WITH RESISTOR TERMINATED OUTPUTS,3–STATE	0TJ19	QS74FCT2823BTQX
A01U1330	156–6514–01			IC,DIGITAL:FCTCMOS,TRANSCEIVER;18–BIT REGISTERED,RESISTOR TERMINATED OUTPUTS,3–STATE	61772	IDT74FCT162501A
A01U1370	160–9244–00			IC,DIGITAL:CMOS,PLD;OTP,22V10,7.5NS,111MHZ,190MA,PRGM 156–6516–00,RW–ADS	80009	160–9244–00
A01U1415	156–6160–01			IC,DIGITAL:FCTCMOS,REGISTER;9–BIT,WITH RESISTOR TERMINATED OUTPUTS,3–STATE	0TJ19	QS74FCT2823BTQX
A01U1417	156–6160–01			IC,DIGITAL:FCTCMOS,REGISTER;9–BIT,WITH RESISTOR TERMINATED OUTPUTS,3–STATE	0TJ19	QS74FCT2823BTQX
A01U1470	160–9169–01			IC,DIGITAL:CMOS,PLD,OTP 22V10,7.5NS,111MHZ,190MA,PRGM 156–6516–00,"BUS TRACKER,";22V10–7,PLCC28–1	80009	160–9169–01
A01U1515	156–6160–01			IC,DIGITAL:FCTCMOS,REGISTER;9–BIT,WITH RESISTOR TERMINATED OUTPUTS,3–STATE	0TJ19	QS74FCT2823BTQX
A01U1517	156–6160–01			IC,DIGITAL:FCTCMOS,REGISTER;9–BIT,WITH RESISTOR TERMINATED OUTPUTS,3–STATE	0TJ19	QS74FCT2823BTQX
A01U1570	160–9243–00			IC,DIGITAL:CMOS,PLD;OTP,22V10,7.5NS,111MHZ,190MA,PRGM 156–6516–00,RESET,22V10–7,PLCC28–1	80009	160–9243–00
A01U1575	136–1255–00			SOCKET,PGA:PCB,;296 POS,37 X 37,0.05 X 0.1CTR,0.165 H X 0.220 TAIL,GOLD/GOLD,INTERSTITIAL,PAT 37AH,LONG PINS	63058	PZA0296H118B5–37
A01U1625	156–6514–01			IC,DIGITAL:FCTCMOS,TRANSCEIVER;18–BIT REGISTERED,RESISTOR TERMINATED OUTPUTS,3–STATE	61772	IDT74FCT162501A
A01U1655	156–6514–01			IC,DIGITAL:FCTCMOS,TRANSCEIVER;18–BIT REGISTERED,RESISTOR TERMINATED OUTPUTS,3–STATE	61772	IDT74FCT162501A
A01U2340	156–6514–01			IC,DIGITAL:FCTCMOS,TRANSCEIVER;18–BIT REGISTERED,RESISTOR TERMINATED OUTPUTS,3–STATE	61772	IDT74FCT162501A
A01U2360	156–6514–01			IC,DIGITAL:FCTCMOS,TRANSCEIVER;18–BIT REGISTERED,RESISTOR TERMINATED OUTPUTS,3–STATE	61772	IDT74FCT162501A
A01U2370	156–6515–00			IC,DIGITAL:FCTCMOS,MISC;10–BIT BUS SWITCH	0TJ19	QS74QST3384Q
A01U2425	156–6465–00			IC,DIGITAL:FCTCMOS,TRANSCEIVER;OCTAL REGISTERED,3–STATE	61772	IDT74FCT646ATSO
A01U2470	156–6515–00			IC,DIGITAL:FCTCMOS,MISC;10–BIT BUS SWITCH	0TJ19	QS74QST3384Q
A01U2475	156–6515–00			IC,DIGITAL:FCTCMOS,MISC;10–BIT BUS SWITCH	0TJ19	QS74QST3384Q
A01U2525	163–0012–00			IC,DIGITAL:CMOS,PLD;EEPLD,16V8,7.5NS,130MA,PRGM 156–6548–00	80009	163–0012–00
A01U2550	156–6514–01			IC,DIGITAL:FCTCMOS,TRANSCEIVER;18–BIT REGISTERED,RESISTOR TERMINATED OUTPUTS,3–STATE	61772	IDT74FCT162501A
A01U2570	156–6515–00			IC,DIGITAL:FCTCMOS,MISC;10–BIT BUS SWITCH	0TJ19	QS74QST3384Q
A01U2575	156–6515–00			IC,DIGITAL:FCTCMOS,MISC;10–BIT BUS SWITCH	0TJ19	QS74QST3384Q

Replaceable electrical parts list (cont.)

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A01U2645	156–6514–01			IC,DIGITAL:FCTCMOS,TRANSCEIVER;18–BIT REGISTERED,RESISTOR TERMINATED OUTPUTS,3–STATE	61772	IDT74FCT162501A
A01U2665	156–6514–01			IC,DIGITAL:FCTCMOS,TRANSCEIVER;18–BIT REGISTERED,RESISTOR TERMINATED OUTPUTS,3–STATE	61772	IDT74FCT162501A

Replaceable Mechanical Parts

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 109 P54/P55 microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

■ Part number

■ Instrument type or model number

■ Instrument serial number

■ Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations   Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts   Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index   The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
80009	TEKTRONIX, INC.	P.O. BOX 500	BEAVERTON, OR, 97077-0001
TK1499	AMLAN INC	97 THORNWOOD RD	STAMFORD CT 06903–2617
TK2427	A/D ELECTRONIC	2121 17TH AVE SE	BOTHELL WA 97021
TK2548	XEROX BUSINESS SERVICES DIV OF XEROX CORPORATION	14181 SW MILLIKAN WAY	BEAVERTON OR 97077
0B445	ELECTRI–CORD MFG CO INC	312 EAST MAIN ST	WESTFIELD PA 16950
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
14310	AULT INC	7300 BOONE AVENUE NORTH	MINNEAPOLIS MN 55428
26742	METHODE ELECTRONICS INC	7447 W WILSON AVE	CHICAGO IL 60656–4548
53387	3M COMPANY ELECTRONIC PRODUCTS DIV	3M AUSTIN CENTER	AUSTIN TX 78769–2963
58050	TEKA PRODUCTS INC	45 SALEM ST	PROVIDENCE RI 02907
61857	SAN–0 INDUSTRIAL CORP	91–3 COLIN DRIVE	HOLBROOK NY 11741
63058	MCKENZIE TECHNOLOGY	910 PAGE AVENUE	FREMONT CA 94538
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
1–0	010–0578–00			1	PROBE ADAPTER:P54C/CM,PGA–296 SOCKETED;	80009	010057800
–1	671–3253–00			1	CKT BD ASSY:P54C/CM PGA–296 SOCKETED	80009	671325300
–2	131–5267–00			5	CONN,HDR PCB,;MALE,STR,2 X 40.O.1 CTR,0.234 MLG X 0.110 TAIL, 30 GOLD (J1150,J1155,J1161,J1165,J1170)	53387	131526700
–3	––– –––			1	CONN,HDR:PCB,;MALE,RTANG,2 X 10,0.05 X 0.1 CTR,0.350 H X 0.100TAIL,CTR PLZ,LATCHING,30 GOLD,W/HOLD DOWN (J1140 SEE REPL)		
–4	––– –––			1	FUSE,WIRE LEAD:5A,125V, (F1220 SEE REPL)		
–5	343–0549–00			1	STRAP,TIEDOWN,E:0.098 W X 4.0 L,ZYTEL	TK1499	HW–047
–6	131–5148–00			1	JACK,POWER DC:PCB,;MALE,RTANG,2.0 MM DIAPIN,7 MM H X 3.3 MM TAIL,3COND,W/SWITCH, MTG POST,DC PWR JACK,1 AMP@12V (JR1120)	TK2427	ADC–016
–7	131–4356–00			5	CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X2,0.1 CTR,0.630 H,BLK,W/HANDLE,JUMPER (P1155,P1160,P1165,P1170,1340)	26742	9618–302–50
–8	––– –––				CONN,HDR PCB';MALE,STR,1 X 3,0.1 CTR,0.0230 MLG X 0.120 TAIL, 30 GOLD,BD RETENTION (SEE REPL J1150,J1155,J1160,J1165,J1170)		
–9	––– –––			1	CONN,HDR:PCB,;MALE,STR,1 X 36,0.1 CTR,0.230 MLG X 0.100 TAIL,GOLD (J1340 SEE REPL)		
–10	136–1254–00			2	SOCKET,PGA:PCB,;296 POS,37 X 37,0.05 X 0.1 CTR,0.165 H X 0.180 TAIL,GOLD/GOLD,INTERSTITTAL,PAT 37AH (U1575)	63058	PZA296H–120B5–3
					STANDARD ACCESSORIES		
	070–9811–00			1	MANUAL,TECH:INSTRUCTION,P54 & P55,DISSASEMBLER, TMS 109	80009	070–9811–00
	070–9803–00			1	MANUAL, TECH:TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070–9803–00
	119–5061–01			1	POWER SUPPLY:25W,5V 5A,CONCENTRIC 2MM,90–265V,47–63HZ (NOT SHOWN)	14310	SW106KA002F01
	161–0104–00			1	CA ASSY,PWR:3,18 AWG,98 L,250V/10AMP,98 INCH, RTANG,IEC320,RCPT X STR,NEMA 15–5P,W/CORD GRIP	S3109	ORDER BY DE-SCRIPTION

Replaceable mechanical parts list (cont.)

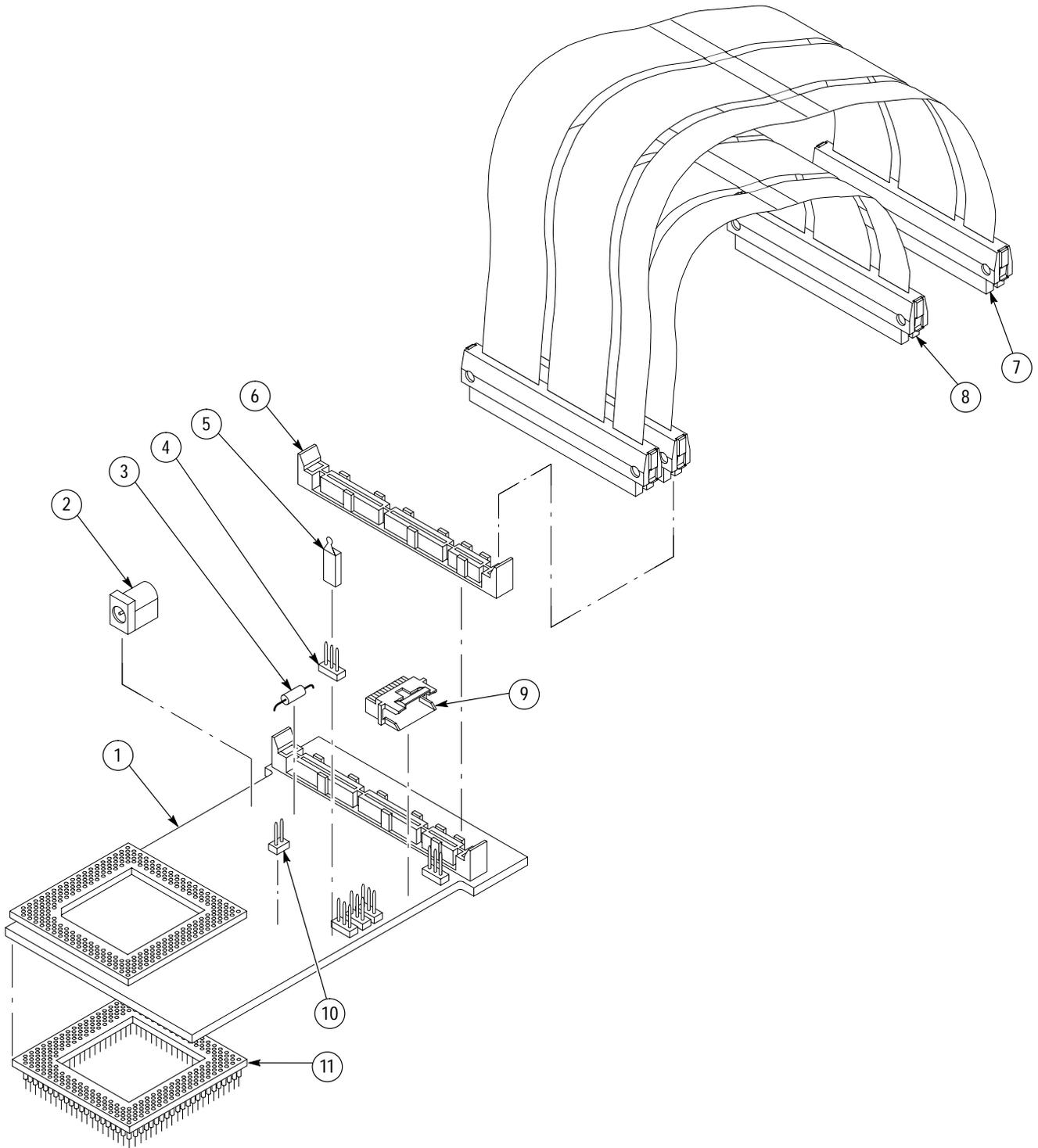| Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					OPTIONAL ACCESSORIES		
	070–9802–00			1	MANUAL, TECH:BASIC OPS MICRO SUP ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070–9802–00
	161–0104–06			1	CA ASSY,PWR:3,1.0MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, EUROPEAN,SAFETY CONTROLLED (OPT A1)	S3109	ORDER BY DE-SCRIPTION
	161–0104–07			1	CA ASSY,PWR:3,1.0MM SQ,240V/10AMP,2.5 METER, RTANG,IEC320,RCPT X 13A, FUSED, UK PLUG, (13A FUSE), UNITED KINGDOM,SAFETY CONTROL (OPT A2)	S3109	ORDER BY DE-SCRIPTION
	161–0104–05			1	CA ASSY,PWR:3,1.0MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, AUSTRALIA,SAFETY CONTROLLED (OPT A3)	S3109	ORDER BY DE-SCRIPTION
	161–0167–00			1	CA ASSY,PWR:3,0.75MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, SWISS,NO CORD GRIP, SAFETY CONTROLLED (OPT A5)	S3109	ORDER BY DE-SCRIPTION

Figure 1: P54/P55 conventional probe adapter exploded view

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
2–0	010–0583–00			1	PROBE ADAPTER:P54C/CM,PGA–296 SOCKETED,LOW PROFILE	80009	010058300
–1	671–3453–00			1	CKT BD ASSY:P54C/CM,PGA–296 SOCKETED,LOW PROFILE	80009	671345300
–2	–––––––––			1	JACK,POWER DC:PCB,;MALE,RTANG,2MM PIN,11MMH (0.433) X 3.5MM(0.137) TAIL,9MM(0.354) W,TIN,W/SWITCH, DC PWR JACK,2.0 MM (SEE REPL J1780)		
–3	–––––––––			1	FUSE,WIRE LEAD:5A,125V, (SEE REPL F1780)		
–4	–––––––––			5	CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30GOLD,BD RETENTION (SEE REPL J1400,J1401,J1500,J1501,1701)		
–5	131–4356–00			5	CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X2,0.1 CTR,0.630 H,BLK,W/HANDLE,JUMPER (P1400,P1401,P1404,P1500,01501)	80009	131435600
–6	–––––––––			2	CONN,BOX:PCB,MICRO–STRIP;FEMALE,STR,100 POS,0.05 CTR,W/GRD PLANE,0.320 H X 0.125 TAIL,LATCHING,4 ROW,0.05 PCB,STAGGER (SEE REPL J1800, J1900)		
–7	174–3419–00			1	CA ASSY,SP:TLC,MICRO–STRIP;TLC,50 OHM,FEP,1.4NS,13.0 L,100 POS,PLUG,LATCHING (W1800)	00779	2–340014–5
–8	174–3418–00			1	CA ASSY,RF:TLC,MICRO–STRIP;TLC,50 OHM,FEP,PROP DELAY 1.4NS,12.0 L,100 POS,PLUG,LATCHING BOTH ENDS (W1900)	00779	1–340014–0
–9	–––––––––			1	CONN,HDR:PCB,;MALE,RTANG,2 X 10,0.05 X 0.1 CTR,0.350 H X 0.100TAIL,CTR PLZ,LATCHING,30 GOLD,W/HOLD DOWN (SEE REPL J1700)		
–10	–––––––––			1	CONN,HDR:PCB,;MALE,STR,1 X 36,0.1 CTR,0.230 MLG X 0.100 TAIL,GOLD (SEE REPL J1404)		
–11	136–1254–00			2	SOCKET,PGA:PCB,;296 POS,37 X 37,0.05 X 0.1 CTR,0.165 H X 0.180 TAIL,GOLD/GOLD,INTERSTITTAL,PAT 37AH (U1180)	63058	PZA296H–120B5–3
					STANDARD ACCESSORIES		
	070–9811–00			1	MANUAL,TECH:INSTRUCTION,P54 & P55,DISSASEMBLER, TMS 109	80009	070–9811–00
	070–9803–00			1	MANUAL, TECH:TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070–9803–00
	119–5061–01			1	POWER SUPPLY:25W,5V 5A,CONCENTRIC 2MM,90–265V,47–63HZ (NOT SHOWN)	14310	SW106KA002F01
	161–0104–00			1	CA ASSY,PWR:3,18 AWG,98 L,250V/10AMP,98 INCH, RTANG,IEC320,RCPT X STR,NEMA 15–5P,W/CORD GRIP	S3109	ORDER BY DE-SCRIPTION

Replaceable mechanical parts list (cont.)

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					OPTIONAL ACCESSORIES		
	070–9802–00			1	MANUAL, TECH:BASIC OPS MICRO SUP ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070–9802–00
	161–0104–06			1	CA ASSY,PWR:3,1.0MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, EUROPEAN,SAFETY CONTROLLED (OPT A1)	S3109	ORDER BY DE-SCRIPTION
	161–0104–07			1	CA ASSY,PWR:3,1.0MM SQ,240V/10AMP,2.5 METER, RTANG,IEC320,RCPT X 13A, FUSED, UK PLUG, (13A FUSE), UNITED KINGDOM,SAFETY CONTROL (OPT A2)	S3109	ORDER BY DE-SCRIPTION
	161–0104–05			1	CA ASSY,PWR:3,1.0MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, AUSTRALIA,SAFETY CONTROLLED (OPT A3)	S3109	ORDER BY DE-SCRIPTION
	161–0167–00			1	CA ASSY,PWR:3,0.75MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, SWISS,NO CORD GRIP, SAFETY CONTROLLED (OPT A5)	S3109	ORDER BY DE-SCRIPTION

Figure 2: P54/P55 low-profile probe adapter exploded view

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
3–0	010– 0582–00			1	ADAPTER,PROBE:192–CHANNEL,HIGH DENSITY PROBE	80009	010058200
–1	380–1095–00			1	HOUSING,HALF:UPPER,192 CHANNEL HIGH DENSITY PROBE	80009	380109500
–2	211–0152–00			4	SCR,ASSEM WSHR:4–40 X 0.625,PNH,BRS,NP,POZ	TK0435	ORDER BY DESC
–3	131–5947–00			2	CONN BOX:CPCB, MICRO–STRIP;FEMALE,STR,100 POS,0.05 CTR,W/GRD PLANE,0.320 H X 0.124 TAIL, LATCHING, 4 ROW, 0.05 PCB, STAGGER (J150, J250)	80009	131594700
–4	671–3395–00			1	CKT BD ASSY:192–CHANNELS,HIGH DENSITY PROBE	80009	671339500
–5	380–1096–00			1	HOUSING,HALF:LOWER,192 CHANNEL HIGH DENSITY PROBE	80009	380109600
–6	348–0070–01			2	PAD,CUSHIONING:2.03 X 0.69 X 0.18 SI RBR	85471	ORDER BY DESC
–7	131–4917–00			8	CONN,HDR CPCB,;MALE,STR,1 X 2,0.1 CTR,0.235 MLF X 0.110 TAIL,20 BOLD, TUBE, HIGH TEMP (J300,J340J400,J440J500,J640,J600)	53387	131491700
–8	131–5267–00			5	CONN,HDR CPCB,;MALE,STR,2 X 40.O.1 CTR,0.234 MLG X 0.110 TAIL, 30 GOLD (J310,J320,J330,J340,J350,J360,J370,J410,J420,J430,J450,J460,J470,J510,J520,J530,J550,J560,J570,J610,J620,J630,J650,J660,J670)	53387	131526700
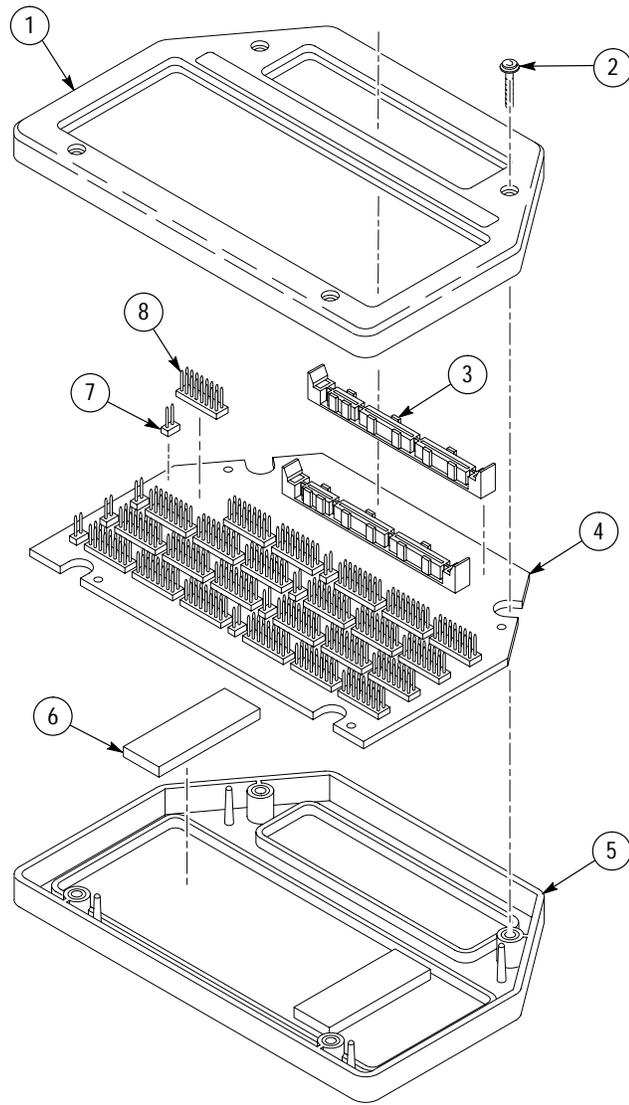
Figure 3: 192-Channel High-Density probe exploded view

Index

Index

A

about this manual set, xi
acquiring data, 2–5
Address group
    channel assignments, 3–7
    display column, 2–9
AHOLD signal, during Writeback cycle, 1–3
Alternate Bus Master Cycles, clocking option, 2–2
Alternate Bus Master cycles, 3–20
alternate signal connections, 3–21
APIC Group, channel assignments, 192-channel module, 3–14
asterisks, indicates out-of-order fetch, 2–15

B

basic operations, where to find information, xi
branch trace messages, 2–14
Burst cycles, addresses in state data, 1–3
burst cycles, 2–16
bus anomalies, 1–3
bus cycles, displayed cycle types, 2–7
Bus Hold cycles, 1–2

C

cache, instruction, 1–2
Cache group, channel assignments
    136-channel module, 3–12
    192-channel module, 3–13
Cache Invalidation cycles, 1–2, 2–16
certifications, 3–4
channel assignments
    Address group, 3–7
    APIC Group, 192-channel module, 3–14
    Cache group
        136-channel module, 3–12
        192-channel module, 3–13
    clocks, 3–15
    Control group, 3–11
    Data group, 3–9, 3–10
    DataSize group, 3–11
    Debug group, 192-channel module, 3–13
    Misc group
        136-channel module, 3–12
        192-channel module, 3–15
    Parity group, 192-channel module, 3–14
    Priv_Bus Group, 192-channel module, 3–14

channel groups, 2–1
channels, extra for alternate connections, 3–23
Chip Set mode, 3–16
clock channel assignments, 3–15
clock rate, 1–2
clocking, Custom, 2–1
    how data is acquired, 3–17
clocking options
    Alternate Bus Master Cycles, 2–2
    field names, 2–2
Code Segment Size field, 2–11
compliances, 3–4
connections
    other microprocessor signals, 3–21
    probe adapter to SUT, PGA, 1–7
        with a high-density probe, 1–10
Control Flow display format, 2–9
Control group
    channel assignments, 3–11
    symbol table, 2–2
Custom clocking, 2–1
    Alternate Bus Master Cycles, 2–2
    how data is acquired, 3–17
cycle types, 2–7

D

data
    acquiring, 2–5
    disassembly formats
        Control Flow, 2–9
        Hardware, 2–7
        Software, 2–9
        Subroutine, 2–10
    how it is acquired, 3–17
data bytes, invalid data group not displayed, 2–6
data display, changing, 2–10
Data group
    channel assignments, 3–9, 3–10
    display column, 2–9
Data_Lo group, display column, 2–9
DataSize group, channel assignments, 3–11
Debug group, channel assignments, 192-channel module, 3–13
demonstration file, 2–20
Descriptor Table reads and writes, 1–3
dimensions, probe adapter, 3–4, 3–5
Directory Table reads and writes, 1–3

        TMS 109 P54 & P55 Microprocessor Support Instruction Manual

TMS 109 P54 & P55 Microprocessor Support Instruction Manual