Instruction Manual

Tektronix

TMS 110
Pentium Pro Microprocessor Support

070-9812-00

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

Printed in the U.S.A.

Tektronix, Inc., P.O. Box 1000, Wilsonville, OR 97070–1000

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Use Proper AC Adapter. Use only the AC adapter specified for this product.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface: Microprocessor Support Documentation

This instruction manual contains specific information about the TMS 110 Pentium Pro microprocessor support and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor supports on the logic analyzer for which the TMS 110 Pentium Pro support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor supports, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor supports is included with each product. Each logic analyzer has basic information that describes how to perform tasks common to supports on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing disassembled data
- Using the probe adapter

Manual Conventions

This manual uses the following conventions:

- The term disassembler refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to online help, an installation manual, or a basic operations of microprocessor supports user manual.
- In the information on basic operations, the term XXX or P54C used in field selections and file names can be replaced with P6. This is the name of the microprocessor in field selections and file names you must use to operate the support.
- The term system under test (SUT) refers to the microprocessor-based system from which data will be acquired.

- The term logic analyzer refers to the Tektronix logic analyzer for which this product was purchased.
- The term module refers to a 204-channel or 192-channel module.
- A pound sign (#) following a signal name indicates an active low signal.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The manual set provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2440) 6:00 a.m. – 5:00 p.m. Pacific time Or, contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Contact your local Tektronix distributor or sales office. Or, visit our web site for a listing of worldwide service locations. http://www.tek.com
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000

Getting Started

Getting Started

This chapter provides information on the following topics:

- A description of the TMS 110 microprocessor support
- Logic analyzer software compatibility
- Your system under test requirements
- Support restrictions
- How to configure the probe adapter
- How to connect to the system under test (SUT)
- How to apply power to and remove power from the probe adapter

Support Description

The TMS 110 microprocessor support disassembles data from systems that are based on the Intel Pentium Pro microprocessor. The support runs on a compatible Tektronix logic analyzer equipped with at a 204-channel module or a 192-channel module.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 110 microprocessor support.

The TMS 110 supports the Pentium Pro microprocessor in a 387-pin PGA package.

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Mechanical Parts* chapter.

To use this support efficiently, you need to have the items listed in the information on basic operations as well as the *Pentium Pro Microprocessor User's Manual*, Intel, 1995.

Information on basic operations also contains a general description of supports.

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

To use the Pentium Pro support, the Tektronix logic analyzer must be equipped with two 102-channel modules, one 102-channel and one 136-channel module, or two 96-channel modules at a minimum. The module must be equipped with enough probes to acquire clock and channel data from signals in your Pentium Pro-based system.

In this manual, references to a 204-channel module includes the two 102-channel module or the one 102-channel and one 136-channel module combination. References to a 192-channel module is for the two 96-channel module combination.

Refer to information on basic operations to determine how many modules and probes the logic analyzer needs to meet the channel requirements.

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor supports in the information on basic operations as they pertain to your SUT.

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other Pentium Pro support requirements and restrictions.

System Clock Rate. The microprocessor support product supports the Pentium Pro microprocessor at speeds of up to 66 MHz[1].

SUT Power. Whenever the SUT is powered off, be sure to remove power from the probe adapter. Refer to *Applying and Removing Power* at the end of this chapter for information on how to remove power from the probe adapter.

92DM16 and TMS 110 Compatibility. The 92DM16 and TMS 110 support products are not compatible. You must use the 92DM16 software to acquire data with the 92DM16 probe adapter, and the TMS 110 software to acquire data with the TMS 110 probe adapter.

The power supply purchased from Intel for use with the 92DM16 and TMS 110 power supplies are not interchangeable.

1 **Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest devices supported.**

CAUTION. *Failure to use the TMS 110 power supply might permanently damage the probe adapter and Pentium Pro microprocessor. Do not use the 92DM16 power supply with the TMS 110 probe adapter.*

92DM16 Reference Memory Files. The TMS 110 application allows you to view reference memories acquired with the 92DM16 support product.

LA-OffLine 92DM16 Reference Memory Files. You can view LA-OffLine reference memories acquired with the 92DM16 probe adapter and software using the P6LAI support setup. However, you must retransfer the file from the DAS to your workstation to view it using the TMS 110 application.

Error Phase. The Error phase is not acquired unless an address parity error occurs.

Arbitration Phase. The Arbitration phase is not acquired .

Deferred Cycles. The Deferred cycles are acquired, but the disassembler might not link the deferred-reply to the deferred-request.

LINT1 and LINT0 Signals. The LINT1 and LINT0 signals are not acquired when the P6 support setup is used. However, the disassembler can still determine when an interrupt occurs. This includes Stop Clock cycles and Halt cycles.

Since the LINT1 and LINT0 signals are not acquired when the P6 support setup is used, interrupts, Stop Clock cycles, and Halt cycles are not shown in the Listing window.

Configuring the Probe Adapter

There are five jumpers on the probe adapter. One jumper is used to match the frequency of the SUT. Another jumper is used to synthesize A2-A0. The third is used to aquire data from asynchronous signals for disassembly or timing. The fourth is used to aquire data from synchronous signals for disassembly or timing. The fifth is used to clock in data for the P6 setup or for the P6_TMG setup.

System Frequency Jumper

The System Frequency jumper (J1200) must be positioned to match the frequency of the SUT. You should position the jumper on pins 1 and 2 if the frequency of the SUT is 45 MHz to 66 MHz. You should position the jumper on pins 2 and 3 if the frequency of the SUT is below 45 MHz.

Figure 1–1 shows the location of J1200 on the probe adapter.

A2-A0 Synthesis Jumper

The A2-A0 Synthesis jumper (J1201) should be positioned on pins 1 and 2 to synthesize address signals A2-A0 using the BE7#-BE0# signal bits in the Request phase. You can position the jumper on pins 2 and 3 to hold the A2-A0 signals high (false).

Figure 1–1 shows the location of J1201 on the probe adapter.

Asynchronous Signals Jumper

The Asynchronous Signals jumper (J1205) should be positioned on pins 1 and 2 to acquire asynchronous signals latched with the system clock, or on pins 2 and 3 to acquire these signals transparently buffered. Table 1–1 shows how to position this jumper depending on the selected support, the type of clocking you are using, and the type of display you want to view.

Table 1–1: Asynchronous Signals jumper information

J1205 Position*	Support Setup	Clocking	Data window
Pins 1 and 2	P6_TMG	Custom or External	Listing window, Disassembly, State, or Graph displays
Pins 2 and 3	P6_TMG	Internal	Waveform window, or Timing display

*** The position of J1205 does not matter when using the P6 support setup.**

Asynchronous signals do not transition based on the system clock; they have no defined timing relationship with the BCLK signal. Some of these signals transition relative to a clock other than BCLK, such as TCK and PICCK. Signals the TMS 110 product considers to be asynchronous are as follows:

INIT#	PREQ#	TDO
LINT0	PRDY#	THERMTRP#
LINT1	PWRTHTL#	TMS
PICCK	STPCLK#	TRST#
PICD0	TCK	TSENSE2#
PICD1	TDI	

You might want to acquire other system activity through the TMS 110 probe adapter such as APIC bus activity. To do this, you will need the TMS 801 APIC bus support probe adapter and a third module. To use the bus support product, this jumper must be positioned on pins 2 and 3.

Figure 1–1 shows the location of J1205 on the probe adapter.

Synchronous Signals Jumper

The Synchronous Signals jumper (J1206) should be positioned on pins 1 and 2 to acquire synchronous signals latched with the system clock, and on pins 2 and 3 to acquire these signals transparently buffered. Table 1–2 shows how to position this jumper depending on the selected support, the type of clocking you are using, and the type of display you want to view.

Table 1–2: Synchronous Signals jumper information

J1206 Position	Support Setup	Clocking	Data window
Pins 1 and 2	P6	Custom	Listing window, State, or Graph displays
	P6_TMG	Custom or External	Listing window, Disassembly, State, or Graph displays
Pins 2 and 3	P6_TMG	Internal	Waveform window, or Timing display

Synchronous signals have a timing relationship with the BCLK signal. The TMS 110 product considers signals not in the previous list to be synchronous.

You might want to acquire other system activity through the TMS 110 probe adapter such as APIC bus activity. To do this, you will need the TMS 801 APIC bus support probe adapter and a third module. To use the bus support product, this jumper must be positioned on pins 1 and 2.

Figure 1–1 shows the location of J1206 on the probe adapter.

Software Support Jumper

The Software Support jumper (J1207) must be set to match the software support setup you are using. Position the jumper on pins 1 and 2 when P6 Support is selected; the P6 setup is used to acquire and disassemble data. Position the jumper on pins 2 and 3 when P6_TMG Support is selected; the P6_TMG setup is used to acquire timing data.

Figure 1–1 shows the location of J1207 on the probe adapter.

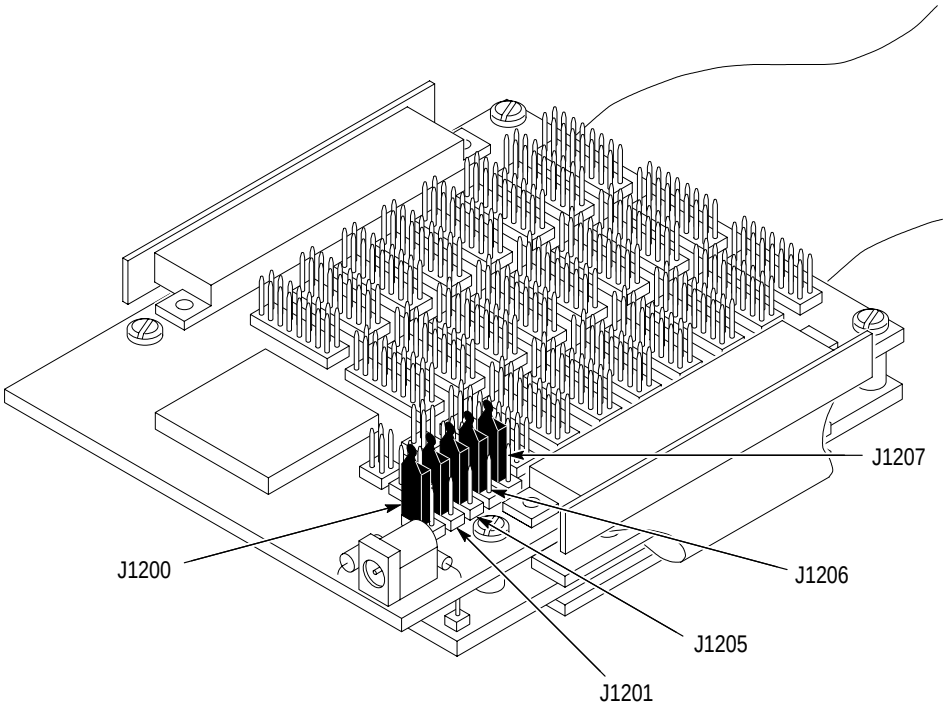


Figure 1–1: Jumper locations on the probe adapter

Connecting to a System Under Test

Before you connect to the SUT, you must connect the probes to the module. Your SUT must also have a minimum amount of clear space surrounding the microprocessor to accommodate the probe adapter. Refer to the *Specifications* chapter in this manual for the required clearances.

The channel and clock probes shown in this chapter are for a 204-channel module. The probes will look different if you are using a 192-channel module.

The general requirements and restrictions of microprocessor supports in the information on basic operations shows the vertical dimensions of a channel or clock probe connected to square pins on a circuit board.

CAUTION. *To avoid product damage, do not carry the probe adapter by only one end when moving it from one location to another. Whenever transporting the probe adapter, be sure to support both ends of the product and keep the flexible region flat. Figure 1–2 shows how to properly handle the probe adapter.*

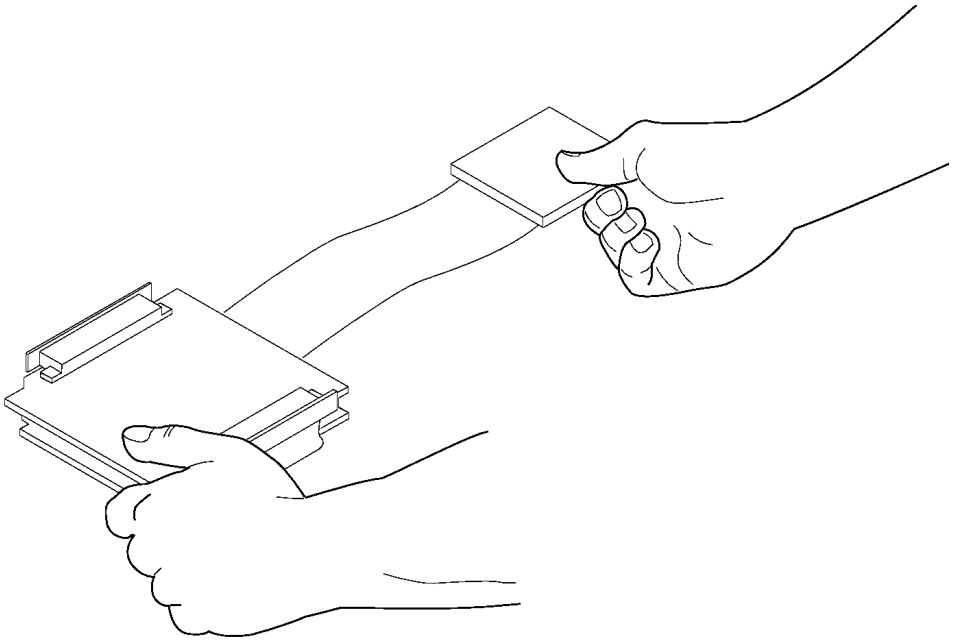


Figure 1–2: Proper handling of the probe adapter

NOTE. *The flexible region, lower board, and target board are fabricated as a single unit. If you damage the flexible region, the entire unit must be replaced.*

To connect the logic analyzer to a SUT using the probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probe adapter, the acquisition probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch the black foam on the underside of the probe adapter to discharge stored static electricity from the probe adapter.
3. Remove the microprocessor from your SUT.

CAUTION. *To avoid product damage, do not bend, crease, or stress the flexible region (cable) on the probe adapter. Handle the probe adapter carefully to avoid contact with sharp edges, such as on a circuit board or metal chassis.*

4. Line up the pin A1 indicator on the microprocessor with the pin A1 indicator on the probe adapter.

CAUTION. *Failure to correctly place the microprocessor into the probe adapter might permanently damage the microprocessor once power is applied.*

5. Place the microprocessor into the probe adapter as shown in Figure 1–3.

The heat sink for the Pentium Pro microprocessor in your SUT must be attached to the microprocessor, not to the microprocessor socket.

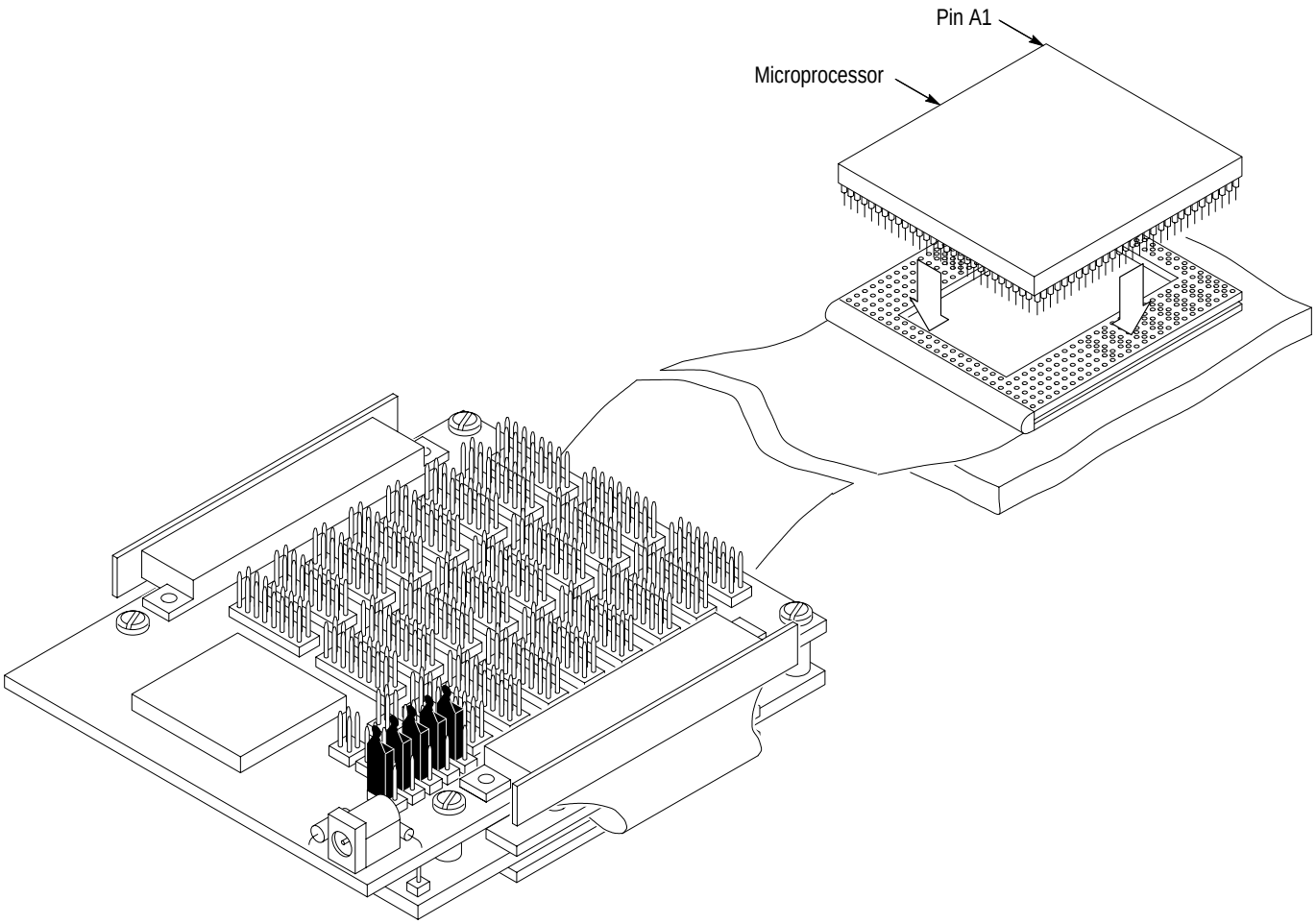


Figure 1–3: Placing the microprocessor into the probe adapter

6. Remove the black foam from the underside of the probe adapter.
7. Line up the pin A1 indicator on the probe adapter with the pin A1 indicator on your SUT. Do not bend, crease, or stress the flexible cable.
8. Place the probe adapter onto the SUT as shown in Figure 1–4.

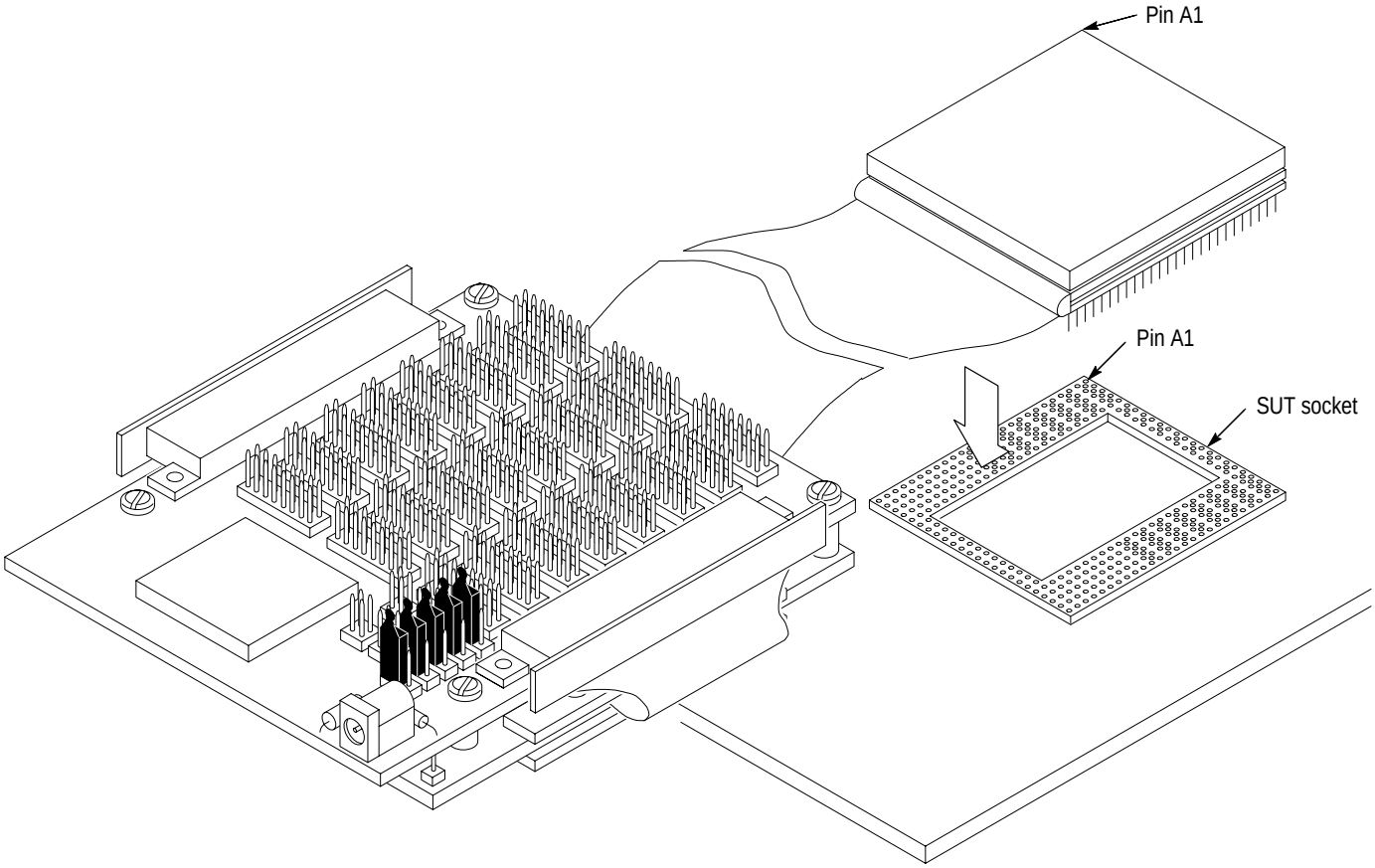


Figure 1–4: Placing the probe adapter onto the SUT

9. Connect the clock and 8-channel probes to the probe adapter as shown in Figure 1–5.

   Match the clock channel numbers on the probe labels from both the HI_ and LO_ modules to the corresponding pins on the probe adapter. Match the ground pins on the probes to the corresponding pins on the probe adapter.

Clock pins on the probe adapter do not have the HI_ or LO_ designators; they are labeled CK0, CK1, CK2, and CK3. Each pair of clock pins connects to the same signal on the probe adapter. The clock probes from both modules must connect to the appropriate clock pins for Custom or External clocking to function properly.

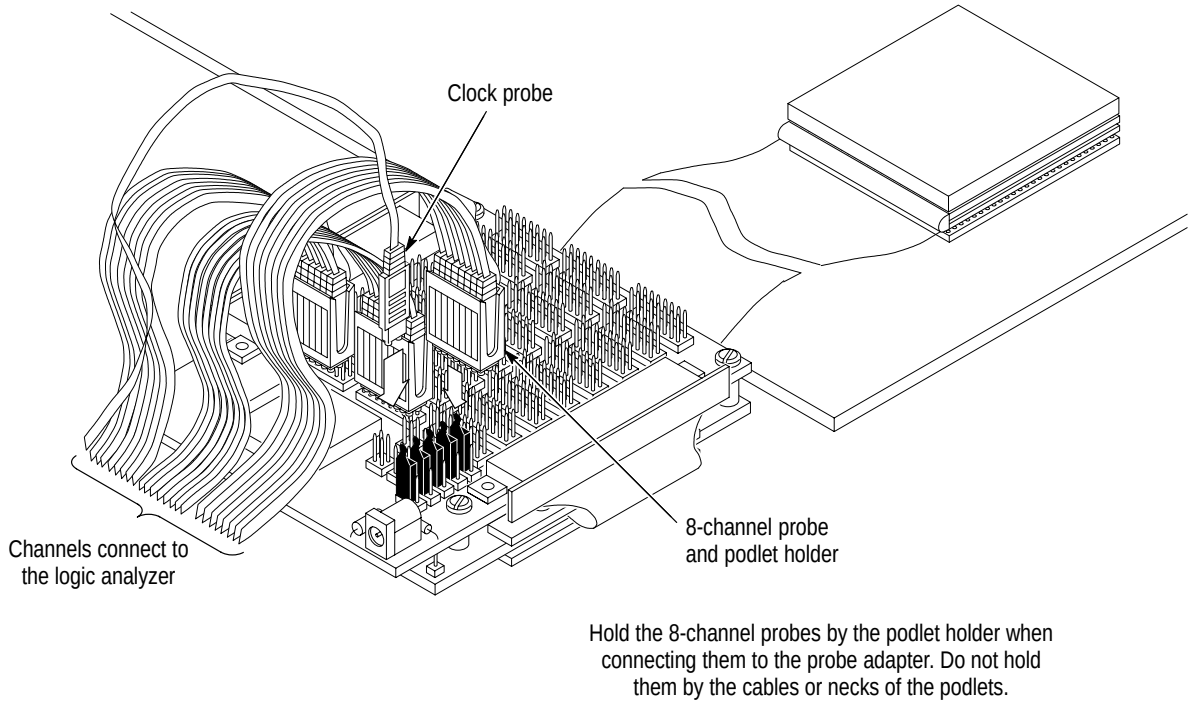


Figure 1–5: Connecting the probes to the probe adapter

Applying and Removing Power

A power supply for the TMS 110 Pentium Pro probe adapter is included with the product. The power supply provides +5 V power to the probe adapter. The center connector of the power jack connects to Vcc.

To apply power to the Pentium Pro probe adapter and SUT, follow these steps:

CAUTION. *Failure to use the +5 V power supply provided by Tektronix might permanently damage the probe adapter and Pentium Pro microprocessor. Do not mistake another power supply that looks similar to the +5 V power supply.*

1. Connect the +5 V power supply to the jack on the probe adapter. Figure 1–6 shows the location of the jack on the probe adapter.

CAUTION. *Failure to apply power to the probe adapter before applying power to your SUT might permanently damage the Pentium Pro microprocessor and SUT.*

2. Plug the power supply for the probe adapter into an electrical outlet.
3. Power on the SUT.

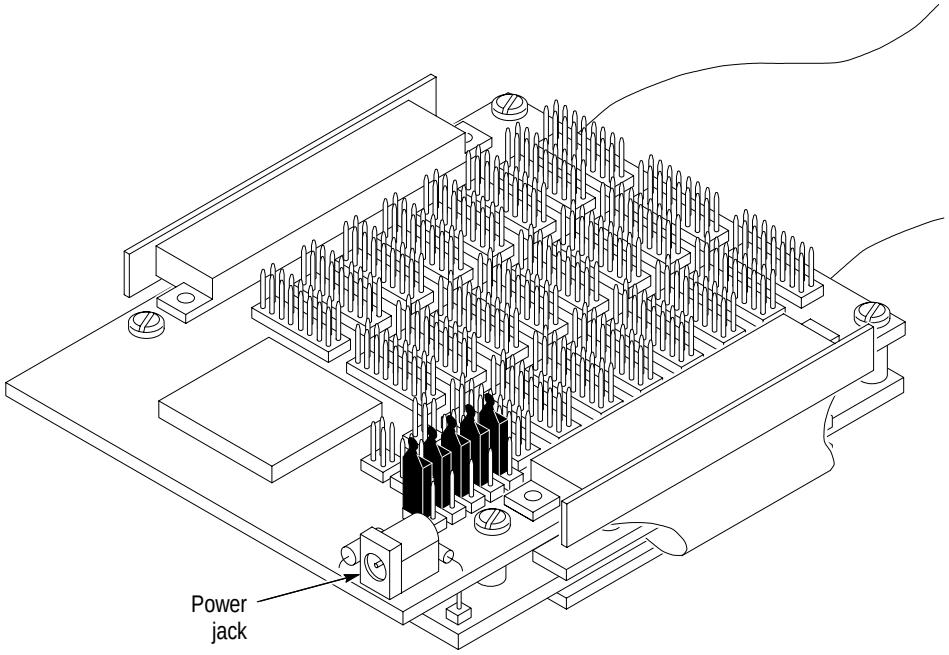


Figure 1–6: Location of the power jack

To remove power from the SUT and Pentium Pro probe adapter, follow these steps:

CAUTION. *Failure to power down your SUT before removing the power from the probe adapter might permanently damage the Pentium Pro microprocessor and SUT.*

1. Power off the SUT.
2. Unplug the power supply for the probe adapter from the electrical outlet.

Operating Basics

Setting Up the Support

This section provides information on how to set up the support. Information covers the following topics:

- Channel group definitions
- Clocking options
- Symbol table files
- Triggering

Remember that the information in this section is specific to the operations and functions of the TMS 110 Pentium Pro support on any Tektronix logic analyzer for which it can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and disassemble data, you need to load the support and specify setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The software automatically defines channel groups for the support. There are two setups available with the TMS 110 software: P6 and P6_TMG. You should use the P6 setup to acquire data for disassembly and the P6_TMG setup to acquire data for timing.

The channel groups defined for the P6 setup are A, Address, Attr, DeferID, DataSize, Extend, REQab, Err, Snoop, Response, Data, Data_Lo, DEP, Data_Ctl, Async, BR, PAL, and Misc.

The channel groups defined for the P6_TMG setup are A, Address, REQ, REQ_Ctl, Error, Snoop, Rsp, Data, Data_Lo, DEP, Data_Ctl, Async, Monitor, BR, REQ_SNP, AGNT_ID, APIC, and Misc.

To see which signal is in which channel group, refer to the channel group assignment tables beginning on page 3–6. Tables 3–5 through 3–23 show the channel assignments for the P6 setup. Tables 3–24 through 3–42 show the channel assignments for the P6_TMG setup.

Clocking Options

The TMS 110 support offers a microprocessor-specific clocking mode for the Pentium Pro microprocessor. This clocking mode is the default selection whenever you load the P6 support or P6_TMG Support.

A description of how cycles are sampled by the module using the TMS 110 support and probe adapter is found in the *Specifications* chapter.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

P6 Setup

The P6 setup includes three modes for acquiring data from a Pentium Pro microprocessor. The setup has a Custom Clocking field with the following modes:

Custom Clocking. The Active Phases Only option stores only cycles with active transaction phases. The Clock-by-Clock w/Demux option stores all cycles, but still demultiplexes the channels like the Active Phases Only option. The Branch Trace Data Only option stores only the Data phase and Agent ID of any Branch Trace Messages on the bus.

Tables 3–5 through 3–23 in the *Specifications* chapter show the channel group assignments for the P6 setup.

P6_TMG Setup

The P6_TMG setup has one Custom clocking option. This clocking option acquires all channels on every rising edge of the BCLK signal without demultiplexing the channels.

The P6_TMG setup is for general purpose analysis and can also be used with the External or Internal clocking modes. Descriptions of using these other clock modes with this microprocessor support package can be found in theinformation on basic operations under *General Purpose Analysis*.

Tables 3–24 through 3–42 in the *Specifications* chapter show the channel group assignments for the P6_TMG setup.

Symbols

The TMS 110 includes symbol table files for some of the channel groups defined by the P6 setup. No symbol table files are included for the channel groups defined by the P6_TMG setup. However, you can create a symbol table file for any channel group. Refer to your logic analyzer user manual for directions on how to create symbol tables.

Table 2–1 shows the name and bit pattern for the symbols in the P6_DID file, the DeferID group symbol table.

The first character in the symbol represents the Agent Type, determined from the DID7# signal. The P represents the Pentium Pro microprocessor agent that is the symmetric agent. The A represents the agent that is not a Pentium Pro microprocessor.

The second character represents the Agent ID, determined from the DID6#, DID5#, and DID4# signals. The last character represents the Transaction ID, determined from the DID3#, DID2#, DID1#, and DID0# signals.

Table 2–1: DeferID group symbol table definitions

Symbol	DeferID group value (DID7# DID6# DID5# DID4# DID3# DID2# DID1# DID0#)	Symbol	DeferID group value (DID7# DID6# DID5# DID4# DID3# DID2# DID1# DID0#)	Symbol	DeferID group value (DID7# DID6# DID5# DID4# DID3# DID2# DID1# DID0#)
P0_0	1 1 1 1 1 1 1 1	P2_0	1 1 0 1 1 1 1 1	P4_0	1 0 1 1 1 1 1 1
P0_1	1 1 1 1 1 1 1 0	P2_1	1 1 0 1 1 1 1 0	P4_1	1 0 1 1 1 1 1 0
P0_2	1 1 1 1 1 1 0 1	P2_2	1 1 0 1 1 1 0 1	P4_2	1 0 1 1 1 1 0 1
P0_3	1 1 1 1 1 1 0 0	P2_3	1 1 0 1 1 1 0 0	P4_3	1 0 1 1 1 1 0 0
P0_4	1 1 1 1 1 0 1 1	P2_4	1 1 0 1 1 0 1 1	P4_4	1 0 1 1 1 0 1 1
P0_5	1 1 1 1 1 0 1 0	P2_5	1 1 0 1 1 0 1 0	P4_5	1 0 1 1 1 0 1 0
P0_6	1 1 1 1 1 0 0 1	P2_6	1 1 0 1 1 0 0 1	P4_6	1 0 1 1 1 0 0 1
P0_7	1 1 1 1 1 0 0 0	P2_7	1 1 0 1 1 0 0 0	P4_7	1 0 1 1 1 0 0 0
P0_8	1 1 1 1 0 1 1 1	P2_8	1 1 0 1 0 1 1 1	P4_8	1 0 1 1 0 1 1 1
P0_9	1 1 1 1 0 1 1 0	P2_9	1 1 0 1 0 1 1 0	P4_9	1 0 1 1 0 1 1 0
P0_A	1 1 1 1 0 1 0 1	P2_A	1 1 0 1 0 1 0 1	P4_A	1 0 1 1 0 1 0 1
P0_B	1 1 1 1 0 1 0 0	P2_B	1 1 0 1 0 1 0 0	P4_B	1 0 1 1 0 1 0 0
P0_C	1 1 1 1 0 0 1 1	P2_C	1 1 0 1 0 0 1 1	P4_C	1 0 1 1 0 0 1 1
P0_D	1 1 1 1 0 0 1 0	P2_D	1 1 0 1 0 0 1 0	P4_D	1 0 1 1 0 0 1 0
P0_E	1 1 1 1 0 0 0 1	P2_E	1 1 0 1 0 0 0 1	P4_E	1 0 1 1 0 0 0 1
P0_F	1 1 1 1 0 0 0 0	P2_F	1 1 0 1 0 0 0 0	P4_F	1 0 1 1 0 0 0 0
P1_0	1 1 1 0 1 1 1 1	P3_0	1 1 0 0 1 1 1 1	P5_0	1 0 1 0 1 1 1 1
P1_1	1 1 1 0 1 1 1 0	P3_1	1 1 0 0 1 1 1 0	P5_1	1 0 1 0 1 1 1 0
P1_2	1 1 1 0 1 1 0 1	P3_2	1 1 0 0 1 1 0 1	P5_2	1 0 1 0 1 1 0 1
P1_3	1 1 1 0 1 1 0 0	P3_3	1 1 0 0 1 1 0 0	P5_3	1 0 1 0 1 1 0 0
P1_4	1 1 1 0 1 0 1 1	P3_4	1 1 0 0 1 0 1 1	P5_4	1 0 1 0 1 0 1 1
P1_5	1 1 1 0 1 0 1 0	P3_5	1 1 0 0 1 0 1 0	P5_5	1 0 1 0 1 0 1 0
P1_6	1 1 1 0 1 0 0 1	P3_6	1 1 0 0 1 0 0 1	P5_6	1 0 1 0 1 0 0 1
P1_7	1 1 1 0 1 0 0 0	P3_7	1 1 0 0 1 0 0 0	P5_7	1 0 1 0 1 0 0 0
P1_8	1 1 1 0 0 1 1 1	P3_8	1 1 0 0 0 1 1 1	P5_8	1 0 1 0 0 1 1 1
P1_9	1 1 1 0 0 1 1 0	P3_9	1 1 0 0 0 1 1 0	P5_9	1 0 1 0 0 1 1 0
P1_A	1 1 1 0 0 1 0 1	P3_A	1 1 0 0 0 1 0 1	P5_A	1 0 1 0 0 1 0 1
P1_B	1 1 1 0 0 1 0 0	P3_B	1 1 0 0 0 1 0 0	P5_B	1 0 1 0 0 1 0 0
P1_C	1 1 1 0 0 0 1 1	P3_C	1 1 0 0 0 0 1 1	P5_C	1 0 1 0 0 0 1 1
P1_D	1 1 1 0 0 0 1 0	P3_D	1 1 0 0 0 0 1 0	P5_D	1 0 1 0 0 0 1 0
P1_E	1 1 1 0 0 0 0 1	P3_E	1 1 0 0 0 0 0 1	P5_E	1 0 1 0 0 0 0 1
P1_F	1 1 1 0 0 0 0 0	P3_F	1 1 0 0 0 0 0 0	P5_F	1 0 1 0 0 0 0 0

Table 2–1: DeferID group symbol table definitions (cont.)

Symbol	DeferID group value (DID7# DID6# DID5# DID4# DID3# DID2# DID1# DID0#)	Symbol	DeferID group value (DID7# DID6# DID5# DID4# DID3# DID2# DID1# DID0#)	Symbol	DeferID group value (DID7# DID6# DID5# DID4# DID3# DID2# DID1# DID0#)
P6_0	1 0 0 1 1 1 1 1	A0_0	0 1 1 1 1 1 1 1	A2_0	0 1 0 1 1 1 1 1
P6_1	1 0 0 1 1 1 1 0	A0_1	0 1 1 1 1 1 1 0	A2_1	0 1 0 1 1 1 1 0
P6_2	1 0 0 1 1 1 0 1	A0_2	0 1 1 1 1 1 0 1	A2_2	0 1 0 1 1 1 0 1
P6_3	1 0 0 1 1 1 0 0	A0_3	0 1 1 1 1 1 0 0	A2_3	0 1 0 1 1 1 0 0
P6_4	1 0 0 1 1 1 1 1	A0_4	0 1 1 1 1 0 1 1	A2_4	0 1 0 1 1 0 1 1
P6_5	1 0 0 1 1 1 1 0	A0_5	0 1 1 1 1 0 1 0	A2_5	0 1 0 1 1 0 1 0
P6_6	1 0 0 1 1 1 0 1	A0_6	0 1 1 1 1 0 0 1	A2_6	0 1 0 1 1 0 0 1
P6_7	1 0 0 1 1 1 0 0	A0_7	0 1 1 1 1 0 0 0	A2_7	0 1 0 1 1 0 0 0
P6_8	1 0 0 1 1 1 1 1	A0_8	0 1 1 1 0 1 1 1	A2_8	0 1 0 1 0 1 1 1
P6_9	1 0 0 1 1 1 1 0	A0_9	0 1 1 1 0 1 1 0	A2_9	0 1 0 1 0 1 1 0
P6_A	1 0 0 1 1 1 0 1	A0_A	0 1 1 1 0 1 0 1	A2_A	0 1 0 1 0 1 0 1
P6_B	1 0 0 1 1 1 0 0	A0_B	0 1 1 1 0 1 0 0	A2_B	0 1 0 1 0 1 0 0
P6_C	1 0 0 1 1 1 1 1	A0_C	0 1 1 1 0 0 1 1	A2_C	0 1 0 1 0 0 1 1
P6_D	1 0 0 1 1 1 1 0	A0_D	0 1 1 1 0 0 1 0	A2_D	0 1 0 1 0 0 1 0
P6_E	1 0 0 1 1 1 0 1	A0_E	0 1 1 1 0 0 0 1	A2_E	0 1 0 1 0 0 0 1
P6_F	1 0 0 1 1 1 0 0	A0_F	0 1 1 1 0 0 0 0	A2_F	0 1 0 1 0 0 0 0
P7_0	1 0 0 0 1 1 1 1	A1_0	0 1 1 0 1 1 1 1	A3_0	0 1 0 0 1 1 1 1
P7_1	1 0 0 0 1 1 1 0	A1_1	0 1 1 0 1 1 1 0	A3_1	0 1 0 0 1 1 1 0
P7_2	1 0 0 0 1 1 0 1	A1_2	0 1 1 0 1 1 0 1	A3_2	0 1 0 0 1 1 0 1
P7_3	1 0 0 0 1 1 0 0	A1_3	0 1 1 0 1 1 0 0	A3_3	0 1 0 0 1 1 0 0
P7_4	1 0 0 0 1 1 1 1	A1_4	0 1 1 0 1 0 1 1	A3_4	0 1 0 0 1 0 1 1
P7_5	1 0 0 0 1 1 1 0	A1_5	0 1 1 0 1 0 1 0	A3_5	0 1 0 0 1 0 1 0
P7_6	1 0 0 0 1 1 0 1	A1_6	0 1 1 0 1 0 0 1	A3_6	0 1 0 0 1 0 0 1
P7_7	1 0 0 0 1 1 0 0	A1_7	0 1 1 0 1 0 0 0	A3_7	0 1 0 0 1 0 0 0
P7_8	1 0 0 0 1 1 1 1	A1_8	0 1 1 0 0 1 1 1	A3_8	0 1 0 0 0 1 1 1
P7_9	1 0 0 0 1 1 1 0	A1_9	0 1 1 0 0 1 1 0	A3_9	0 1 0 0 0 1 1 0
P7_A	1 0 0 0 1 1 0 1	A1_A	0 1 1 0 0 1 0 1	A3_A	0 1 0 0 0 1 0 1
P7_B	1 0 0 0 1 1 0 0	A1_B	0 1 1 0 0 1 0 0	A3_B	0 1 0 0 0 1 0 0
P7_C	1 0 0 0 1 1 1 1	A1_C	0 1 1 0 0 0 1 1	A3_C	0 1 0 0 0 0 1 1
P7_D	1 0 0 0 1 1 1 0	A1_D	0 1 1 0 0 0 1 0	A3_D	0 1 0 0 0 0 1 0
P7_E	1 0 0 0 1 1 0 1	A1_E	0 1 1 0 0 0 0 1	A3_E	0 1 0 0 0 0 0 1
P7_F	1 0 0 0 1 1 0 0	A1_F	0 1 1 0 0 0 0 0	A3_F	0 1 0 0 0 0 0 0

Table 2–1: DeferID group symbol table definitions (cont.)

Symbol	DeferID group value (DID7# DID6# DID5# DID4# DID3# DID2# DID1# DID0#)	Symbol	DeferID group value (DID7# DID6# DID5# DID4# DID3# DID2# DID1# DID0#)
A4_0	0 0 1 1 1 1 1 1	A6_0	0 0 0 1 1 1 1 1
A4_1	0 0 1 1 1 1 1 0	A6_1	0 0 0 1 1 1 1 0
A4_2	0 0 1 1 1 1 0 1	A6_2	0 0 0 1 1 1 0 1
A4_3	0 0 1 1 1 1 0 0	A6_3	0 0 0 1 1 1 0 0
A4_4	0 0 1 1 1 0 1 1	A6_4	0 0 0 1 1 0 1 1
A4_5	0 0 1 1 1 0 1 0	A6_5	0 0 0 1 1 0 1 0
A4_6	0 0 1 1 1 0 0 1	A6_6	0 0 0 1 1 0 0 1
A4_7	0 0 1 1 1 0 0 0	A6_7	0 0 0 1 1 0 0 0
A4_8	0 0 1 1 0 1 1 1	A6_8	0 0 0 1 0 1 1 1
A4_9	0 0 1 1 0 1 1 0	A6_9	0 0 0 1 0 1 1 0
A4_A	0 0 1 1 0 1 0 1	A6_A	0 0 0 1 0 1 0 1
A4_B	0 0 1 1 0 1 0 0	A6_B	0 0 0 1 0 1 0 0
A4_C	0 0 1 1 0 0 1 1	A6_C	0 0 0 1 0 0 1 1
A4_D	0 0 1 1 0 0 1 0	A6_D	0 0 0 1 0 0 1 0
A4_E	0 0 1 1 0 0 0 1	A6_E	0 0 0 1 0 0 0 1
A4_F	0 0 1 1 0 0 0 0	A6_F	0 0 0 1 0 0 0 0
A5_0	0 0 1 0 1 1 1 1	A7_0	0 0 0 0 1 1 1 1
A5_1	0 0 1 0 1 1 1 0	A7_1	0 0 0 0 1 1 1 0
A5_2	0 0 1 0 1 1 0 1	A7_2	0 0 0 0 1 1 0 1
A5_3	0 0 1 0 1 1 0 0	A7_3	0 0 0 0 1 1 0 0
A5_4	0 0 1 0 1 0 1 1	A7_4	0 0 0 0 1 0 1 1
A5_5	0 0 1 0 1 0 1 0	A7_5	0 0 0 0 1 0 1 0
A5_6	0 0 1 0 1 0 0 1	A7_6	0 0 0 0 1 0 0 1
A5_7	0 0 1 0 1 0 0 0	A7_7	0 0 0 0 1 0 0 0
A5_8	0 0 1 0 0 1 1 1	A7_8	0 0 0 0 0 1 1 1
A5_9	0 0 1 0 0 1 1 0	A7_9	0 0 0 0 0 1 1 0
A5_A	0 0 1 0 0 1 0 1	A7_A	0 0 0 0 0 1 0 1
A5_B	0 0 1 0 0 1 0 0	A7_B	0 0 0 0 0 1 0 0
A5_C	0 0 1 0 0 0 1 1	A7_C	0 0 0 0 0 0 1 1
A5_D	0 0 1 0 0 0 1 0	A7_D	0 0 0 0 0 0 1 0
A5_E	0 0 1 0 0 0 0 1	A7_E	0 0 0 0 0 0 0 1
A5_F	0 0 1 0 0 0 0 0	A7_F	0 0 0 0 0 0 0 0

Table 2–2 shows the name and bit pattern for the symbols in the P6_EXT file, the Extend group symbol table.

Table 2–2: Extend group symbol table definitions

Symbol	Extend group value ADS_L EXF4# EXF3# EXF2# EXF1# EXF0#	Meaning
SMM	1 0 1 X 1 X	Access from or to SMM space
SPLITCLK	1 1 0 X 1 X	Split clock cycle
DEFER_EN	1 1 1 X 0 X	Defer enabled
SMM_SPLIT	1 0 0 X 1 X	SMM access and split clock cycle
SMM_DEN	1 0 1 X 0 X	SMM access and Defer enabled
DEN_SPLIT	1 1 0 X 0 X	Defer enabled and split clock cycle
SMM_DE_SP	1 0 0 X 0 X	SMM access, Defer enabled, and split clock cycle
---	X X X X X X	No active Request phase

Table 2–3 shows the name and bit pattern for the symbols in the P6_REQ file, the REQab group symbol table.

Table 2–3: REQab group symbol table definitions

Symbol	REQab group value ADS# BNR# LOCK# REQa4 REQa3 REQa2 REQa1 REQa0 REQb4 REQb3 REQb2 REQb1 REQb0	Meaning
---	1 X X X X X X X X X X X X X	No active Request phase
DEFER_RPL	0 X X 0 0 0 0 0 X X X X X X	Defer reply
RESERVED0	0 X X 0 0 0 0 1 X X X X X X	Reserved request type
INT_ACK	0 X X 0 1 0 0 0 X X X 0 0	Interrupt acknowledge
SPECIAL	0 X X 0 1 0 0 0 X X X 0 1	Special request
RESERVED1	0 X X 0 1 0 0 0 X X X 1 X	Reserved request type
BRANCH_TR	0 X X 0 1 0 0 1 X X X 0 0	Branch trace message
RESERVED3	0 X X 0 1 0 0 1 X X X 0 1	Reserved request type
RESERVED4	0 X X 0 1 0 0 1 X X X 1 X	Reserved request type
I_O_RD_8	0 X X 1 0 0 0 0 X X X 0 0	I/O read, 8 bytes
I_O_RD_16	0 X X 1 0 0 0 0 X X X 0 1	I/O read, 16 bytes

Table 2–3: REQab group symbol table definitions (cont.)

Symbol	REQab group value ADS# BNR# LOCK# REQa4 REQa3 REQa2 REQa1 REQa0 REQb4 REQb3 REQb2 REQb1 REQb0	Meaning
I_O_RD_32	0 X X 1 0 0 0 0 X X X 1 0	I/O read, 32 bytes
I_O_READ*	0 X X 1 0 0 0 0 X X X X X	Any I/O read
I_O_WR_8	0 X X 1 0 0 0 1 X X X 0 0	I/O write, 8 bytes
I_O_WR_16	0 X X 1 0 0 0 1 X X X 0 1	I/O write, 16 bytes
I_O_WR_32	0 X X 1 0 0 0 1 X X X 1 0	I/O write, 32 bytes
I_O_WRITE*	0 X X 1 0 0 0 1 X X X X X	Any I/O write
RESERVED6	0 X X 1 1 0 0 X X X X X X	Reserved request type
FETCH	0 X X X X 1 0 0 X X X X X	Opcode fetch
MEM_RD_8	0 X X X X 1 1 0 X X X 0 0	Memory read, 8 bytes
MEM_RD_16	0 X X X X 1 1 0 X X X 0 1	Memory read, 16 bytes
MEM_RD_32	0 X X X X 1 1 0 X X X 1 0	Memory read, 32 bytes
MEM_READ*	0 X X X X 1 1 0 X X X X X	Any memory read
MEM_WR_8	0 X X X X 1 X 1 X X X 0 0	Memory write, 8 bytes
MEM_WR_16	0 X X X X 1 X 1 X X X 0 1	Memory write, 16 bytes
MEM_WR_32	0 X X X X 1 X 1 X X X 1 0	Memory write, 32 bytes
MEM_WRITE*	0 X X X X 1 X 1 X X X X X	Any memory write
INVALIDAT	0 X X X X 0 1 0 X X X 0 0	Invalidate
MEM_RD_IN	0 X X X X 0 1 0 X X X X X	Memory read and invalidate
RESERVED7	0 X X X X 0 1 1 X X X X X	Reserved request type

* **Symbols used only for triggering; they do not appear in the Disassembly or State displays.**

Table 2–4 shows the name and bit pattern for the symbols in the P6_SNP file, the Snoop group symbol table.

Table 2–4: Snoop group symbol table definitions

Symbol	Snoop group value SNOOP_D HIT# HITM# DEFER#	Meaning
Defer	1 X 1 0	DEFER# asserted
Shared	1 0 1 1	HIT# asserted
Dirty	1 1 0 X	HITM# asserted

Table 2–4: Snoop group symbol table definitions (cont.)

Symbol	Snoop group value SNOOP_D HIT# HITM# DEFER#	Meaning
Clean	1 1 1 X	No Snoop phase signals asserted
Stall	0 0 0 X	Snoop phase stall
---	0 X X X	No active Snoop phase

Table 2–5 shows the name and bit pattern for the symbols in the P6_RSP file, the Response group symbol table.

Table 2–5: Response group symbol table definitions

Symbol	Response group value RS2# RS1# RS0#	Meaning
---	1 1 1	No active Response phase
RETRY	1 1 0	Retry transaction
DEFERRED	1 0 1	Defered transaction
RESERVED	1 0 0	Reserved response type
HARD_FAIL	0 1 1	Hard failure
NO_DATA	0 1 0	No data from the response agent
IMP_WR_BK	0 0 1	Implicit write-back
NORM_DATA	0 0 0	Normal data response

Table 2–6 shows the name and bit pattern for the symbols in the P6_DC file, the Data_DC group symbol table.

Table 2–6: Data_DC group symbol table definitions

Symbol	Data_DC group value DRDY# DBSY# TRDY#	Meaning
Data	0 X X	Active Data phase
---	1 X X	No active Data phase

Table 2–7 shows the name and bit pattern for the symbols in the P6_ASY file, the Asynchronous group symbol table.

Table 2–7: Async group symbol table definitions

Symbol	Async group value RESET# FLUSH# BERR# TRCK_ER_D BINIT# INIT#	Meaning
Reset	X X 0 X X X	System Reset
Init	X 0 X X X X	System initialize
Binit	0 X X X X X	System Bus inititialize
Flush	1 1 1 0 X X	Cache flush
Bus Error	1 1 1 X 0 X	System bus error
Track Error	1 1 1 X X 1	PAL tracking error
---	X X X X X X	No active asynchronous signals

Table 2–8 shows the name and bit pattern for the symbols in the P6_PAL file, the PAL group symbol table.

The first character in the symbol represents the Processor ID, determined from the ID1_D and ID0_D signals. The second character represents the Request Count, determined from the RCNT2_D, RCNT1_D, and RCNT0_D signals. The third character represents the Snoop Count, determined from the SCNT2_D, SCNT1_D, and SCNT0_D signals.

When the value of the RCNT2_D-RCNT0_D or SCNT2_D-SCNT0_D signals is equal to 000, the count can be 0 or 8, and is displayed as 0/8.

Table 2–8: PAL group symbol table definitions

Symbol	PAL group value ID1_D ID0_D RCNT2_D RCNT1_D RCNT0_D SCNT2_D SCNT1_D SCNT0_D	Symbol	PAL group value ID1_D ID0_D RCNT2_D RCNT1_D RCNT0_D SCNT2_D SCNT1_D SCNT0_D
0 0/8 0/8	0 0 0 0 0 0 0 0	0 0/8 1	0 0 0 0 0 0 0 1
0 1 0/8	0 0 0 0 1 0 0 0	0 1 1	0 0 0 0 1 0 0 1
0 2 0/8	0 0 0 1 0 0 0 0	0 2 1	0 0 0 1 0 0 0 1
0 3 0/8	0 0 0 1 1 0 0 0	0 3 1	0 0 0 1 1 0 0 1
0 4 0/8	0 0 1 0 0 0 0 0	0 4 1	0 0 1 0 0 0 0 1
0 5 0/8	0 0 1 0 1 0 0 0	0 5 1	0 0 1 0 1 0 0 1
0 6 0/8	0 0 1 1 0 0 0 0	0 6 1	0 0 1 1 0 0 0 1
0 7 0/8	0 0 1 1 1 0 0 0	0 7 1	0 0 1 1 1 0 0 1
1 0/8 0/8	0 1 0 0 0 0 0 0	1 0/8 1	0 1 0 0 0 0 0 1
1 1 0/8	0 1 0 0 1 0 0 0	1 1 1	0 1 0 0 1 0 0 1
1 2 0/8	0 1 0 1 0 0 0 0	1 2 1	0 1 0 1 0 0 0 1
1 3 0/8	0 1 0 1 1 0 0 0	1 3 1	0 1 0 1 1 0 0 1
1 4 0/8	0 1 1 0 0 0 0 0	1 4 1	0 1 1 0 0 0 0 1
1 5 0/8	0 1 1 0 1 0 0 0	1 5 1	0 1 1 0 1 0 0 1
1 6 0/8	0 1 1 1 0 0 0 0	1 6 1	0 1 1 1 0 0 0 1
1 7 0/8	0 1 1 1 1 0 0 0	1 7 1	0 1 1 1 1 0 0 1
2 0/8 0/8	1 0 0 0 0 0 0 0	2 0/8 1	1 0 0 0 0 0 0 1
2 1 0/8	1 0 0 0 1 0 0 0	2 1 1	1 0 0 0 1 0 0 1
2 2 0/8	1 0 0 1 0 0 0 0	2 2 1	1 0 0 1 0 0 0 1
2 3 0/8	1 0 0 1 1 0 0 0	2 3 1	1 0 0 1 1 0 0 1
2 4 0/8	1 0 1 0 0 0 0 0	2 4 1	1 0 1 0 0 0 0 1
2 5 0/8	1 0 1 0 1 0 0 0	2 5 1	1 0 1 0 1 0 0 1
2 6 0/8	1 0 1 1 0 0 0 0	2 6 1	1 0 1 1 0 0 0 1
2 7 0/8	1 0 1 1 1 0 0 0	2 7 1	1 0 1 1 1 0 0 1
3 0/8 0/8	1 1 0 0 0 0 0 0	3 0/8 1	1 1 0 0 0 0 0 1
3 1 0/8	1 1 0 0 1 0 0 0	3 1 1	1 1 0 0 1 0 0 1
3 2 0/8	1 1 0 1 0 0 0 0	3 2 1	1 1 0 1 0 0 0 1
3 3 0/8	1 1 0 1 1 0 0 0	3 3 1	1 1 0 1 1 0 0 1
3 4 0/8	1 1 1 0 0 0 0 0	3 4 1	1 1 1 0 0 0 0 1
3 5 0/8	1 1 1 0 1 0 0 0	3 5 1	1 1 1 0 1 0 0 1
3 6 0/8	1 1 1 1 0 0 0 0	3 6 1	1 1 1 1 0 0 0 1
3 7 0/8	1 1 1 1 1 0 0 0	3 7 1	1 1 1 1 1 0 0 1

Table 2–8: PAL group symbol table definitions (cont.)

Symbol	PAL group value ID1_D ID0_D RCNT2_D RCNT1_D RCNT0_D SCNT2_D SCNT1_D SCNT0_D	Symbol	PAL group value ID1_D ID0_D RCNT2_D RCNT1_D RCNT0_D SCNT2_D SCNT1_D SCNT0_D
0 0/8 2	0 0 0 0 0 0 1 0	0 0/8 3	0 0 0 0 0 0 1 1
0 1 2	0 0 0 0 1 0 1 0	0 1 3	0 0 0 0 1 0 1 1
0 2 2	0 0 0 1 0 0 1 0	0 2 3	0 0 0 1 0 0 1 1
0 3 2	0 0 0 1 1 0 1 0	0 3 3	0 0 0 1 1 0 1 1
0 4 2	0 0 1 0 0 0 1 0	0 4 3	0 0 1 0 0 0 1 1
0 5 2	0 0 1 0 1 0 1 0	0 5 3	0 0 1 0 1 0 1 1
0 6 2	0 0 1 1 0 0 1 0	0 6 3	0 0 1 1 0 0 1 1
0 7 2	0 0 1 1 1 0 1 0	0 7 3	0 0 1 1 1 0 1 1
1 0/8 2	0 1 0 0 0 0 1 0	1 0/8 3	0 1 0 0 0 0 1 1
1 1 2	0 1 0 0 1 0 1 0	1 1 3	0 1 0 0 1 0 1 1
1 2 2	0 1 0 1 0 0 1 0	1 2 3	0 1 0 1 0 0 1 1
1 3 2	0 1 0 1 1 0 1 0	1 3 3	0 1 0 1 1 0 1 1
1 4 2	0 1 1 0 0 0 1 0	1 4 3	0 1 1 0 0 0 1 1
1 5 2	0 1 1 0 1 0 1 0	1 5 3	0 1 1 0 1 0 1 1
1 6 2	0 1 1 1 0 0 1 0	1 6 3	0 1 1 1 0 0 1 1
1 7 2	0 1 1 1 1 0 1 0	1 7 3	0 1 1 1 1 0 1 1
2 0/8 2	1 0 0 0 0 0 1 0	2 0/8 3	1 0 0 0 0 0 1 1
2 1 2	1 0 0 0 1 0 1 0	2 1 3	1 0 0 0 1 0 1 1
2 2 2	1 0 0 1 0 0 1 0	2 2 3	1 0 0 1 0 0 1 1
2 3 2	1 0 0 1 1 0 1 0	2 3 3	1 0 0 1 1 0 1 1
2 4 2	1 0 1 0 0 0 1 0	2 4 3	1 0 1 0 0 0 1 1
2 5 2	1 0 1 0 1 0 1 0	2 5 3	1 0 1 0 1 0 1 1
2 6 2	1 0 1 1 0 0 1 0	2 6 3	1 0 1 1 0 0 1 1
2 7 2	1 0 1 1 1 0 1 0	2 7 3	1 0 1 1 1 0 1 1
3 0/8 2	1 1 0 0 0 0 1 0	3 0/8 3	1 1 0 0 0 0 1 1
3 1 2	1 1 0 0 1 0 1 0	3 1 3	1 1 0 0 1 0 1 1
3 2 2	1 1 0 1 0 0 1 0	3 2 3	1 1 0 1 0 0 1 1
3 3 2	1 1 0 1 1 0 1 0	3 3 3	1 1 0 1 1 0 1 1
3 4 2	1 1 1 0 0 0 1 0	3 4 3	1 1 1 0 0 0 1 1
3 5 2	1 1 1 0 1 0 1 0	3 5 3	1 1 1 0 1 0 1 1
3 6 2	1 1 1 1 0 0 1 0	3 6 3	1 1 1 1 0 0 1 1
3 7 2	1 1 1 1 1 0 1 0	3 7 3	1 1 1 1 1 0 1 1

Table 2–8: PAL group symbol table definitions (cont.)

Symbol	PAL group value										Symbol	PAL group value									
	ID1_D	ID0_D	RCNT2_D	RCNT1_D	RCNT0_D	SCNT2_D	SCNT1_D	SCNT0_D				ID1_D	ID0_D	RCNT2_D	RCNT1_D	RCNT0_D	SCNT2_D	SCNT1_D	SCNT0_D		
0 0/8 4	0	0	0	0	0	1	0	0			0 0/8 5	0	0	0	0	0	1	0	1		
0 1 4	0	0	0	0	1	1	0	0			0 1 5	0	0	0	0	1	1	0	1		
0 2 4	0	0	0	1	0	1	0	0			0 2 5	0	0	0	1	0	1	0	1		
0 3 4	0	0	0	1	1	1	0	0			0 3 5	0	0	0	1	1	1	0	1		
0 4 4	0	0	1	0	0	1	0	0			0 4 5	0	0	1	0	0	1	0	1		
0 5 4	0	0	1	0	1	1	0	0			0 5 5	0	0	1	0	1	1	0	1		
0 6 4	0	0	1	1	0	1	0	0			0 6 5	0	0	1	1	0	1	0	1		
0 7 4	0	0	1	1	1	1	0	0			0 7 5	0	0	1	1	1	1	0	1		
1 0/8 4	0	1	0	0	0	1	0	0			1 0/8 5	0	1	0	0	0	1	0	1		
1 1 4	0	1	0	0	1	1	0	0			1 1 5	0	1	0	0	1	1	0	1		
1 2 4	0	1	0	1	0	1	0	0			1 2 5	0	1	0	1	0	1	0	1		
1 3 4	0	1	0	1	1	1	0	0			1 3 5	0	1	0	1	1	1	0	1		
1 4 4	0	1	1	0	0	1	0	0			1 4 5	0	1	1	0	0	1	0	1		
1 5 4	0	1	1	0	1	1	0	0			1 5 5	0	1	1	0	1	1	0	1		
1 6 4	0	1	1	1	0	1	0	0			1 6 5	0	1	1	1	0	1	0	1		
1 7 4	0	1	1	1	1	1	0	0			1 7 5	0	1	1	1	1	1	0	1		
2 0/8 4	1	0	0	0	0	1	0	0			2 0/8 5	1	0	0	0	0	1	0	1		
2 1 4	1	0	0	0	1	1	0	0			2 1 5	1	0	0	0	1	1	0	1		
2 2 4	1	0	0	1	0	1	0	0			2 2 5	1	0	0	1	0	1	0	1		
2 3 4	1	0	0	1	1	1	0	0			2 3 5	1	0	0	1	1	1	0	1		
2 4 4	1	0	1	0	0	1	0	0			2 4 5	1	0	1	0	0	1	0	1		
2 5 4	1	0	1	0	1	1	0	0			2 5 5	1	0	1	0	1	1	0	1		
2 6 4	1	0	1	1	0	1	0	0			2 6 5	1	0	1	1	0	1	0	1		
2 7 4	1	0	1	1	1	1	0	0			2 7 5	1	0	1	1	1	1	0	1		
3 0/8 4	1	1	0	0	0	1	0	0			3 0/8 5	1	1	0	0	0	1	0	1		
3 1 4	1	1	0	0	1	1	0	0			3 1 5	1	1	0	0	1	1	0	1		
3 2 4	1	1	0	1	0	1	0	0			3 2 5	1	1	0	1	0	1	0	1		
3 3 4	1	1	0	1	1	1	0	0			3 3 5	1	1	0	1	1	1	0	1		
3 4 4	1	1	1	0	0	1	0	0			3 4 5	1	1	1	0	0	1	0	1		
3 5 4	1	1	1	0	1	1	0	0			3 5 5	1	1	1	0	1	1	0	1		
3 6 4	1	1	1	1	0	1	0	0			3 6 5	1	1	1	1	0	1	0	1		
3 7 4	1	1	1	1	1	1	0	0			3 7 5	1	1	1	1	1	1	0	1		

Table 2–8: PAL group symbol table definitions (cont.)

Symbol	PAL group value ID1_D ID0_D RCNT2_D RCNT1_D RCNT0_D SCNT2_D SCNT1_D SCNT0_D	Symbol	PAL group value ID1_D ID0_D RCNT2_D RCNT1_D RCNT0_D SCNT2_D SCNT1_D SCNT0_D
0 0/8 6	0 0 0 0 0 1 1 0	0 0/8 7	0 0 0 0 0 1 1 1
0 1 6	0 0 0 0 1 1 1 0	0 1 7	0 0 0 0 1 1 1 1
0 2 6	0 0 0 1 0 1 1 0	0 2 7	0 0 0 1 0 1 1 1
0 3 6	0 0 0 1 1 1 1 0	0 3 7	0 0 0 1 1 1 1 1
0 4 6	0 0 1 0 0 1 1 0	0 4 7	0 0 1 0 0 1 1 1
0 5 6	0 0 1 0 1 1 1 0	0 5 7	0 0 1 0 1 1 1 1
0 6 6	0 0 1 1 0 1 1 0	0 6 7	0 0 1 1 0 1 1 1
0 7 6	0 0 1 1 1 1 1 0	0 7 7	0 0 1 1 1 1 1 1
1 0/8 6	0 1 0 0 0 1 1 0	1 0/8 7	0 1 0 0 0 1 1 1
1 1 6	0 1 0 0 1 1 1 0	1 1 7	0 1 0 0 1 1 1 1
1 2 6	0 1 0 1 0 1 1 0	1 2 7	0 1 0 1 0 1 1 1
1 3 6	0 1 0 1 1 1 1 0	1 3 7	0 1 0 1 1 1 1 1
1 4 6	0 1 1 0 0 1 1 0	1 4 7	0 1 1 0 0 1 1 1
1 5 6	0 1 1 0 1 1 1 0	1 5 7	0 1 1 0 1 1 1 1
1 6 6	0 1 1 1 0 1 1 0	1 6 7	0 1 1 1 0 1 1 1
1 7 6	0 1 1 1 1 1 1 0	1 7 7	0 1 1 1 1 1 1 1
2 0/8 6	1 0 0 0 0 1 1 0	2 0/8 7	1 0 0 0 0 1 1 1
2 1 6	1 0 0 0 1 1 1 0	2 1 7	1 0 0 0 1 1 1 1
2 2 6	1 0 0 1 0 1 1 0	2 2 7	1 0 0 1 0 1 1 1
2 3 6	1 0 0 1 1 1 1 0	2 3 7	1 0 0 1 1 1 1 1
2 4 6	1 0 1 0 0 1 1 0	2 4 7	1 0 1 0 0 1 1 1
2 5 6	1 0 1 0 1 1 1 0	2 5 7	1 0 1 0 1 1 1 1
2 6 6	1 0 1 1 0 1 1 0	2 6 7	1 0 1 1 0 1 1 1
2 7 6	1 0 1 1 1 1 1 0	2 7 7	1 0 1 1 1 1 1 1
3 0/8 6	1 1 0 0 0 1 1 0	3 0/8 7	1 1 0 0 0 1 1 1
3 1 6	1 1 0 0 1 1 1 0	3 1 7	1 1 0 0 1 1 1 1
3 2 6	1 1 0 1 0 1 1 0	3 2 7	1 1 0 1 0 1 1 1
3 3 6	1 1 0 1 1 1 1 0	3 3 7	1 1 0 1 1 1 1 1
3 4 6	1 1 1 0 0 1 1 0	3 4 7	1 1 1 0 0 1 1 1
3 5 6	1 1 1 0 1 1 1 0	3 5 7	1 1 1 0 1 1 1 1
3 6 6	1 1 1 1 0 1 1 0	3 6 7	1 1 1 1 0 1 1 1
3 7 6	1 1 1 1 1 1 1 0	3 7 7	1 1 1 1 1 1 1 1

Table 2–8: PAL group symbol table definitions (cont.)

Symbol	PAL group value ID1_D ID0_D RCNT2_D RCNT1_D RCNT0_D SCNT2_D SCNT1_D SCNT0_D	Symbol	PAL group value ID1_D ID0_D RCNT2_D RCNT1_D RCNT0_D SCNT2_D SCNT1_D SCNT0_D
X 0/8 0/8*	X X 0 0 0 0 0 0	X 4 0/8*	X X 1 0 0 0 0 0
X 0/8 1*	X X 0 0 0 0 0 1	X 4 1*	X X 1 0 0 0 0 1
X 0/8 2*	X X 0 0 0 0 1 0	X 4 2*	X X 1 0 0 0 1 0
X 0/8 3*	X X 0 0 0 0 1 1	X 4 3*	X X 1 0 0 0 1 1
X 0/8 4*	X X 0 0 0 1 0 0	X 4 4*	X X 1 0 0 1 0 0
X 0/8 5*	X X 0 0 0 1 0 1	X 4 5*	X X 1 0 0 1 0 1
X 0/8 6*	X X 0 0 0 1 1 0	X 4 6*	X X 1 0 0 1 1 0
X 0/8 7*	X X 0 0 0 1 1 1	X 4 7*	X X 1 0 0 1 1 1
X 1 0/8*	X X 0 0 1 0 0 0	X 5 0/8*	X X 1 0 1 0 0 0
X 1 1*	X X 0 0 1 0 0 1	X 5 1*	X X 1 0 1 0 0 1
X 1 2*	X X 0 0 1 0 1 0	X 5 2*	X X 1 0 1 0 1 0
X 1 3*	X X 0 0 1 0 1 1	X 5 3*	X X 1 0 1 0 1 1
X 1 4*	X X 0 0 1 1 0 0	X 5 4*	X X 1 0 1 1 0 0
X 1 5*	X X 0 0 1 1 0 1	X 5 5*	X X 1 0 1 1 0 1
X 1 6*	X X 0 0 1 1 1 0	X 5 6*	X X 1 0 1 1 1 0
X 1 7*	X X 0 0 1 1 1 1	X 5 7*	X X 1 0 1 1 1 1
X 2 0/8*	X X 0 1 0 0 0 0	X 6 0/8*	X X 1 1 0 0 0 0
X 2 1*	X X 0 1 0 0 0 1	X 6 1*	X X 1 1 0 0 0 1
X 2 2*	X X 0 1 0 0 1 0	X 6 2*	X X 1 1 0 0 1 0
X 2 3*	X X 0 1 0 0 1 1	X 6 3*	X X 1 1 0 0 1 1
X 2 4*	X X 0 1 0 1 0 0	X 6 4*	X X 1 1 0 1 0 0
X 2 5*	X X 0 1 0 1 0 1	X 6 5*	X X 1 1 0 1 0 1
X 2 6*	X X 0 1 0 1 1 0	X 6 6*	X X 1 1 0 1 1 0
X 2 7*	X X 0 1 0 1 1 1	X 6 7*	X X 1 1 0 1 1 1
X 3 0/8*	X X 0 1 1 0 0 0	X 7 0/8*	X X 1 1 1 0 0 0
X 3 1*	X X 0 1 1 0 0 1	X 7 1*	X X 1 1 1 0 0 1
X 3 2*	X X 0 1 1 0 1 0	X 7 2*	X X 1 1 1 0 1 0
X 3 3*	X X 0 1 1 0 1 1	X 7 3*	X X 1 1 1 0 1 1
X 3 4*	X X 0 1 1 1 0 0	X 7 4*	X X 1 1 1 1 0 0
X 3 5*	X X 0 1 1 1 0 1	X 7 5*	X X 1 1 1 1 0 1
X 3 6*	X X 0 1 1 1 1 0	X 7 6*	X X 1 1 1 1 1 0
X 3 7*	X X 0 1 1 1 1 1	X 7 7*	X X 1 1 1 1 1 1

Table 2–8: PAL group symbol table definitions (cont.)

Symbol	PAL group value ID1_D ID0_D RCNT2_D RCNT1_D RCNT0_D SCNT2_D SCNT1_D SCNT0_D	Symbol	PAL group value ID1_D ID0_D RCNT2_D RCNT1_D RCNT0_D SCNT2_D SCNT1_D SCNT0_D
0 X 0/8*	0 0 X X X 0 0 0	0 0/8 X*	0 0 0 0 0 X X X
0 X 1*	0 0 X X X 0 0 1	0 1 X*	0 0 0 0 1 X X X
0 X 2*	0 0 X X X 0 1 0	0 2 X*	0 0 0 1 0 X X X
0 X 3*	0 0 X X X 0 1 1	0 3 X*	0 0 0 1 1 X X X
0 X 4*	0 0 X X X 1 0 0	0 4 X*	0 0 1 0 0 X X X
0 X 5*	0 0 X X X 1 0 1	0 5 X*	0 0 1 0 1 X X X
0 X 6*	0 0 X X X 1 1 0	0 6 X*	0 0 1 1 0 X X X
0 X 7*	0 0 X X X 1 1 1	0 7 X*	0 0 1 1 1 X X X
1 X 0/8*	0 1 X X X 0 0 0	1 0/8 X*	0 1 0 0 0 X X X
1 X 1*	0 1 X X X 0 0 1	1 1 X*	0 1 0 0 1 X X X
1 X 2*	0 1 X X X 0 1 0	1 2 X*	0 1 0 1 0 X X X
1 X 3*	0 1 X X X 0 1 1	1 3 X*	0 1 0 1 1 X X X
1 X 4*	0 1 X X X 1 0 0	1 4 X*	0 1 1 0 0 X X X
1 X 5*	0 1 X X X 1 0 1	1 5 X*	0 1 1 0 1 X X X
1 X 6*	0 1 X X X 1 1 0	1 6 X*	0 1 1 1 0 X X X
1 X 7*	0 1 X X X 1 1 1	1 7 X*	0 1 1 1 1 X X X
2 X 0/8*	1 0 X X X 0 0 0	2 0/8 X*	1 0 0 0 0 X X X
2 X 1*	1 0 X X X 0 0 1	2 1 X*	1 0 0 0 1 X X X
2 X 2*	1 0 X X X 0 1 0	2 2 X*	1 0 0 1 0 X X X
2 X 3*	1 0 X X X 0 1 1	2 3 X*	1 0 0 1 1 X X X
2 X 4*	1 0 X X X 1 0 0	2 4 X*	1 0 1 0 0 X X X
2 X 5*	1 0 X X X 1 0 1	2 5 X*	1 0 1 0 1 X X X
2 X 6*	1 0 X X X 1 1 0	2 6 X*	1 0 1 1 0 X X X
2 X 7*	1 0 X X X 1 1 1	2 7 X*	1 0 1 1 1 X X X
3 X 0/8*	1 1 X X X 0 0 0	3 0/8 X*	1 1 0 0 0 X X X
3 X 1*	1 1 X X X 0 0 1	3 1 X*	1 1 0 0 1 X X X
3 X 2*	1 1 X X X 0 1 0	3 2 X*	1 1 0 1 0 X X X
3 X 3*	1 1 X X X 0 1 1	3 3 X*	1 1 0 1 1 X X X
3 X 4*	1 1 X X X 1 0 0	3 4 X*	1 1 1 0 0 X X X
3 X 5*	1 1 X X X 1 0 1	3 5 X*	1 1 1 0 1 X X X
3 X 6*	1 1 X X X 1 1 0	3 6 X*	1 1 1 1 0 X X X
3 X 7*	1 1 X X X 1 1 1	3 7 X*	1 1 1 1 1 X X X

Table 2–8: PAL group symbol table definitions (cont.)

Symbol	PAL group value (ID1_D ID0_D RCNT2_D RCNT1_D RCNT0_D SCNT2_D SCNT1_D SCNT0_D)	Symbol	PAL group value (ID1_D ID0_D RCNT2_D RCNT1_D RCNT0_D SCNT2_D SCNT1_D SCNT0_D)
X X 0/8*	X X X X X 0 0 0	X 2 X*	X X 0 1 0 X X X
X X 1*	X X X X X 0 0 1	X 3 X*	X X 0 1 1 X X X
X X 2*	X X X X X 0 1 0	X 4 X*	X X 1 0 0 X X X
X X 3*	X X X X X 0 1 1	X 5 X*	X X 1 0 1 X X X
X X 4*	X X X X X 1 0 0	X 6 X*	X X 1 1 0 X X X
X X 5*	X X X X X 1 0 1	X 7 X*	X X 1 1 1 X X X
X X 6*	X X X X X 1 1 0	0 X X*	0 0 X X X X X X
X X 7*	X X X X X 1 1 1	1 X X*	0 1 X X X X X X
X 0/8 X*	X X 0 0 0 X X X	2 X X*	1 0 X X X X X X
X 1 X*	X X 0 0 1 X X X	3 X X*	1 1 X X X X X X

* **Symbols used only for triggering; they are not displayed.**

Information on basic operations contains detals on how to use symbolic values for triggering, and displaying other channel groups symbolically, such as the Address channel group.

Triggering

The trigger description in the information on basic operations applies to the Pentium Pro disassembler. Because the disassembly is more complicated, some additional information is needed.

To trigger on a complete transaction from your Pentium Pro-based system, you will need to set up the module to trigger on more than one phase of a bus transaction. To set up a trigger specification, you need to know which transaction phases you are including in the trigger specification and which channel groups are valid during each phase. Table 2–13 on page 2–43 lists the channel groups that are valid during the various bus transaction phases.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. Information covers the following topics and tasks:

- Acquiring data
- Viewing instruction or transaction mnemonics
- Viewing disassembled data in various display formats
- Cycle type labels
- How to change the way data is displayed
- How to change disassembled cycles with the mark cycles function

Pentium Pro microprocessor-based systems operate with a transaction-style bus. The TMS 110 Pentium Pro software can acquire and disassembler data from multiple microprocessors in a system and link the five phases of each bus transaction together. The disassembler links all bus activity, but only disassembles instructions from one processor at a time. You can select which agent will be traced and how to display acquired data in the Disassembly property page (the Disassembly Format Definition overlay).

The disassembler can display bus cycles as instructions, as bus transactions, or as both instructions and transactions.

Instruction decoding is based on the type of memory the code is using. The default setup is to trace code operating within cacheable memory. You can change the setup to trace code operating within uncacheable memory. Refer to *Code Memory Type* in this section for information on the Code Memory Type field in the Disassembly property page (the Disassembly Format Definition overlay).

Acquiring Data

Once you load the P6 support, choose a clocking mode and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual.

Viewing Disassembled Data

The software disassembles bus transactions across all Pentium Pro microprocessors (and involving other devices) in the system. You can select the type of disassembly to display for the trace agent in the Mnemonic Shown field in the Disassembly property page (the Disassembly Format Definition overlay). With Instructions selected, the software disassembles opcode fetches into instructions from the trace agent.

You can view disassembled data in four different display formats: Hardware, Software, Control Flow, and Subroutine. Information on basic operations describes how to select the disassembly display formats.

The display formats show the A, Address, Data, Data_Lo, Mnemonic, and Async group values by default. Gaps in the acquired data, caused by data qualification specified in the Trigger menu, are indicated by a gray background behind any visible channel group.

NOTE. *Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–30.*

The disassembler displays special characters and strings in the Mnemonic column to indicate significant events.

Table 2–9 shows the special characters and strings unique to the Pentium Pro disassembler and gives a definition of what they represent.

Table 2–9: Special characters in the display and meaning

Character or string displayed	Meaning
m	The instruction was manually marked as a program fetch
****	Indicates there is insufficient data available for complete disassembly of the instruction; the number of asterisks will indicate the width of the data that is unavailable. Each two asterisks represent a byte.
#	Indicates an immediate value
(16) or (32)	Indicates the default segment size is 16 or 32 bits; only appears for fetch cycles
*	Indicates an out-of-order fetch; the single asterisk appears before the mnemonic string
–	Indicates an invalid phase or data
(??)	Indicates an invalid operand for the instruction

Table 2–9: Special characters in the display and meaning (cont.)

Character or string displayed	Meaning
'' ''	Indicates the transaction required multiple samples for the Data phase; the first sample shows all the information and subsequent samples show these ditto marks
<More>	Shown on the last line of a sample to indicate that there are more lines to display
INCOMPLETE TRANSACTION	Indicates that the sample had a Data phase, but was not linked with a Request phase
[blank space]	Nothing in the Mnemonic column indicates that the sample did not have a Data phase

The disassembler also displays cycle type labels. Table 2–10 shows these cycle type labels and gives a definition of the cycle they represent.

Table 2–10: Cycle type definitions

Cycle type	Definition
DEFER RPL	A Deferred Reply transaction
RESERVED 0	A Reserved 0 transaction
INT ACK	An Interrupt Acknowledge transaction
SPECIAL	A Special transaction
RESERVED 1	A Reserved 1 transaction
BRANCH TRACE	A Branch Trace transaction
BTM SOURCE	A Branch Trace transaction showing the source address (2 lines)
BTM TARGET	A Branch Trace transaction showing the target address (2 lines)
RESERVED 3	A Reserved 3 transaction
RESERVED 4	A Reserved 4 transaction
IO READ	An I/O Read transaction
IO WRITE	An I/O Write transaction
RESERVED 6	A Reserved 6 transaction
FETCH	A Fetch transaction
MEM READ	A Memory Read transaction
MEM WRITE	A Memory Write transaction
INVALIDATE	In Invalidate transaction
MEM RD IN	A Memory Read Invalidate transaction
RESERVED 7	A Reserved 7 transaction

Table 2–10: Cycle type definitions (cont.)

Cycle type	Definition
UNKNOWN	The combination of REQab bits is unexpected or unrecognized
SPEC: NOP	A Special transaction that is determined to be an NOP transaction
SPEC: SHUTDN	A Special transaction that is determined to be a Shutdown transaction
SPEC: FLUSH	A Special transaction that is determined to be a Flush transaction
SPEC: HALT	A Special transaction that is determined to be a Halt transaction
SPEC: SYNC	A Special transaction that is determined to be a Sync transaction
SPEC: FL ACK	A Special transaction that is determined to be a Flush Acknowledge transaction
SPEC: STP CLK	A Special transaction that is determined to be a Stop Clock Acknowledge transaction
SPEC: SMI ACK	A Special transaction that is determined to be an SMI Acknowledge transaction
RESET *	A special RESET cycle that is not a transaction
BUS INIT *	A special Bus Init cycle that is not a transaction
INIT *	Indicates that the INIT# signal was asserted for several samples, then deasserted and the Reset code is fetched at 0x0FFFFFFF0; this is not a transaction or cycle. The INIT# signal is from the ASYNC group.
(CACHE LINE FILL)†	A Fetch cycle computed by the disassembler to be a cache fill; data is fetched but not executed, is part of a 32 byte fetch, and might be stored in the cache.
(EXTENSION)†	A Fetch cycle computed by the disassembler to be an opcode extension
(FLUSH)†	A Fetch cycle computed by the disassembler to be flushed

* **Cycles not associated with an agent, that affect the entire system. RESET, BUS INIT, and INIT cycles are always displayed regardless of the selection in the Other Agent field in the Disassembly property page (Disassembly Format Definition overlay).**

† **Computed cycle type.**

Transaction mnemonics include various types of information as follows:

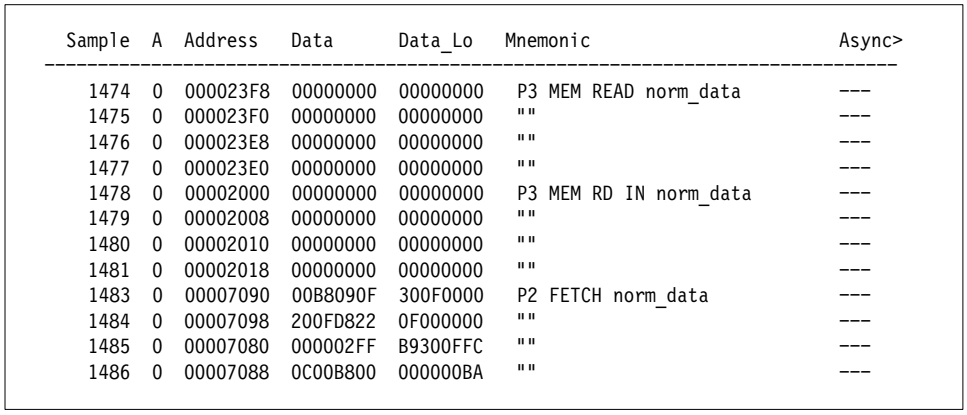
- Processor type and identification (ID)
- Request type
- Response type
- Errors, if any

A data sample can contain information for up to five phases of a bus transaction. Table 2–13, at the end of this chapter, shows the channel groups (defined by the P6 support setup) the disassembler considers valid for various phases of a transaction. For more information on how the disassembler handles bus transactions refer to *Basic Transaction Operations*.

Figure 2–1 shows an example of disassembled bus transactions in Hardware format. In this figure, By Transactions is selected in the Hardware Mode field and Transactions is selected in the Mnemonic Shown field of the Disassembly property page (the Disassembly Format Definition overlay).

***NOTE**. Be aware that the By Transaction selection in the Hardware Mode field is very different than the Transactions selection in the Mnemonic Shown field.*

This screen print shows three complete transactions; two are from the P3 agent, and one is from the P2 agent. All three transactions returned with normal data.



Sample	A	Address	Data	Data_Lo	Mnemonic	Async>
1474	0	000023F8	00000000	00000000	P3 MEM READ norm_data	---
1475	0	000023F0	00000000	00000000	""	---
1476	0	000023E8	00000000	00000000	""	---
1477	0	000023E0	00000000	00000000	""	---
1478	0	00002000	00000000	00000000	P3 MEM RD IN norm_data	---
1479	0	00002008	00000000	00000000	""	---
1480	0	00002010	00000000	00000000	""	---
1481	0	00002018	00000000	00000000	""	---
1483	0	00007090	00B8090F	300F0000	P2 FETCH norm_data	---
1484	0	00007098	200FD822	0F000000	""	---
1485	0	00007080	000002FF	B9300FFC	""	---
1486	0	00007088	0C00B800	000000BA	""	---

Figure 2–1: Transaction mnemonics in Hardware format

Hardware Display Format

In the Hardware display format, reads from interrupt and exception vectors are labeled with the vector name. For Fetch transactions issued by the trace agent, the disassembler displays instruction mnemonics if selected.

You can display disassembled data in the Hardware format in two modes: By phase or By transaction. The By Phase mode shows each sample of acquired data as they occurred. The By Transaction mode shows all phases as complete transactions and displays transaction information with the Data phase (group values are rearranged in the display).

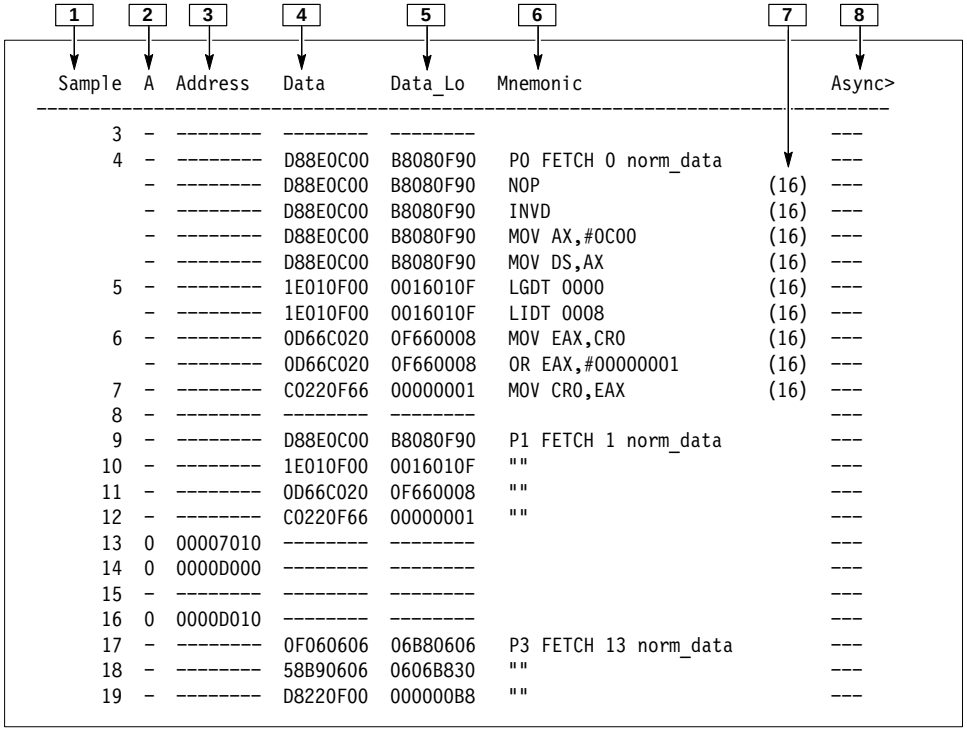
Hardware Mode By Phase. With By Phase selected in the Hardware Mode field of the Disassembly property page (the Disassembly Format Definition overlay), transactions from all agents are displayed regardless of the selection made in the Other Agents field.

For each sample, the data acquired is displayed with the sample. For invalid phases, associated channel groups have the values dashed out. If a Data phase is valid, a mnemonic is displayed. The sample number of the sample in which the request occurred also appears in the Mnemonic column.

Figure 2–2 shows an example of the By Phase mode of the Hardware display format. In this figure, Both is selected in the Mnemonics Shown field of the Disassembly property page (Disassembly Format Definition overlay).

If Instructions were selected in the Mnemonics Shown field, the transaction information on sample 4 would not be displayed.

Samples 4, 9, and 17 each show a different Pentium Pro microprocessor as the symmetric agent, the sample number from which the request came, the type of request (Fetches), and the type of response in the mnemonic. The mnemonic is shown with the Data phase.



Sample	A	Address	Data	Data_Lo	Mnemonic		Async>
3	–	--------	--------	--------			---
4	–	--------	D88E0C00	B8080F90	P0 FETCH 0 norm_data		---
	–	--------	D88E0C00	B8080F90	NOP	(16)	---
	–	--------	D88E0C00	B8080F90	INVD	(16)	---
	–	--------	D88E0C00	B8080F90	MOV AX,#0C00	(16)	---
	–	--------	D88E0C00	B8080F90	MOV DS,AX	(16)	---
5	–	--------	1E010F00	0016010F	LGDT 0000	(16)	---
	–	--------	1E010F00	0016010F	LIDT 0008	(16)	---
6	–	--------	0D66C020	0F660008	MOV EAX,CR0	(16)	---
	–	--------	0D66C020	0F660008	OR EAX,#00000001	(16)	---
7	–	--------	C0220F66	00000001	MOV CR0,EAX	(16)	---
8	–	--------	--------	--------			---
9	–	--------	D88E0C00	B8080F90	P1 FETCH 1 norm_data		---
10	–	--------	1E010F00	0016010F	""		---
11	–	--------	0D66C020	0F660008	""		---
12	–	--------	C0220F66	00000001	""		---
13	0	00007010	--------	--------			---
14	0	0000D000	--------	--------			---
15	–	--------	--------	--------			---
16	0	0000D010	--------	--------			---
17	–	--------	0F060606	06B80606	P3 FETCH 13 norm_data		---
18	–	--------	58B90606	0606B830	""		---
19	–	--------	D8220F00	000000B8	""		---

Figure 2–2: Hardware format in By Phase mode with instruction and transaction mnemonics

1 **Sample Column.** Lists the memory locations for the acquired data.

2 **A Group.** Lists data from channels connected to the A35-A32 part of the Pentium Pro Address bus.

3 **Address Group.** Lists data from channels connected to the A31-A0 part of the Pentium Pro Address bus.

4 **Data Group.** Lists data from channels connected to the D63-D32 part of the Pentium Pro Data bus.

5 **Data_Lo Group.** Lists data from channels connected to the D31-D0 part of the Pentium Pro Data bus.

6 **Mnemonic Column.** Lists the disassembled bus transactions.

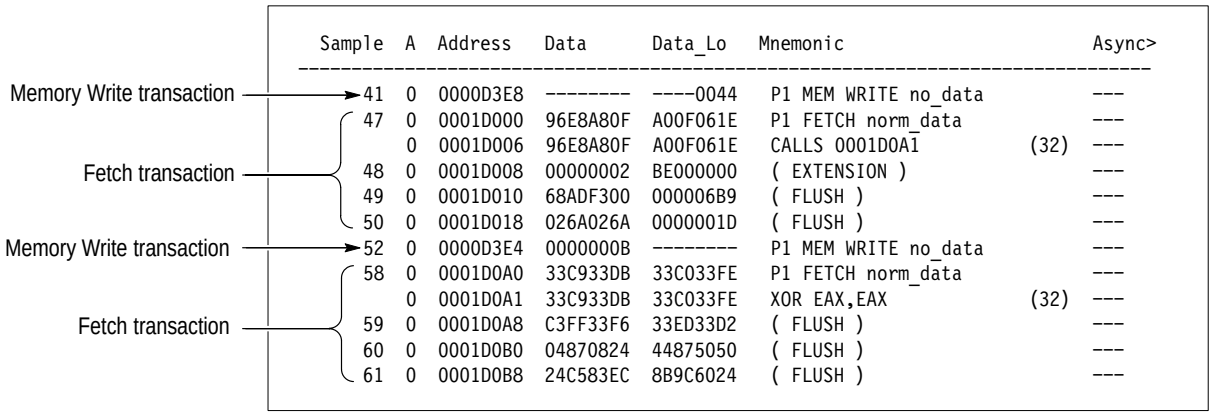
7 This part of the mnemonic, (16) or (32), indicates that the fetch is from a 16- or 32-bit code segment size and disassembled accordingly.

8 **Async Group.** Lists the data from the Async channel group.

Hardware Mode By Transaction. With `By Transaction` selected in the Hardware Mode field of the Disassembly property page (the Disassembly Format Definition overlay), all phases are shown as complete transactions and displayed with the Data phase.

The sample in which the Data phase occurs shows the information for complete transactions. The phases are rearranged so the channel group values associated with each transaction are displayed together. Phase information can be dashed in the display because it was not acquired or it was not required for that transaction.

Figure 2–3 shows an example of the By Transaction mode of the Hardware display format. In this figure, Both is selected in the Mnemonics Shown field of the Disassembly property page (the Disassembly Format Definition overlay).



Sample	A	Address	Data	Data_Lo	Mnemonic		Async>
41	0	0000D3E8	--------	----0044	P1 MEM WRITE no_data		---
47	0	0001D000	96E8A80F	A00F061E	P1 FETCH norm_data		---
	0	0001D006	96E8A80F	A00F061E	CALLS 0001D0A1	(32)	---
48	0	0001D008	00000002	BE000000	(EXTENSION)		---
49	0	0001D010	68ADF300	000006B9	(FLUSH)		---
50	0	0001D018	026A026A	0000001D	(FLUSH)		---
52	0	0000D3E4	0000000B	--------	P1 MEM WRITE no_data		---
58	0	0001D0A0	33C933DB	33C033FE	P1 FETCH norm_data		---
	0	0001D0A1	33C933DB	33C033FE	XOR EAX,EAX	(32)	---
59	0	0001D0A8	C3FF33F6	33ED33D2	(FLUSH)		---
60	0	0001D0B0	04870824	44875050	(FLUSH)		---
61	0	0001D0B8	24C583EC	8B9C6024	(FLUSH)		---

Figure 2–3: Hardware format in By Transaction mode with both instruction and transaction mnemonics

Figure 2–4 shows a more complex By Transaction mode display in Hardware format. In this figure, Both is selected in the Mnemonics Shown field of the Disassembly property page (the Disassembly Format Definition overlay). This screen print is from the P6 Demo system file which contains data from a SUT operating in cached memory.

In this figure, there are two Special transactions. Sample 1433 shows a Special Synchronous transaction that does not have a Data phase. When the transaction does not have a Data phase, the disassembler inserts an additional line without a sample number between complete lines to maintain a chronological order of bus transactions.

Sample	A	Address	Data	Data_Lo	Mnemonic	Async>
1430	0	00001020	00419301	00008002	P3 MEM READ norm_data	---
1431	0	00001028	00000000	00000000	""	---
1432	0	00001030	00000000	00000000	""	---
1433	0	00001038	00409B00	40001090	""	---
	0	C0000000	--------	--------	P2 SPEC: SYNC no_data	---
1441	0	00007100	00000000	BBEC8B00	P3 FETCH norm_data	---
1442	0	00007108	2AB95058	50038936	""	---
1443	0	00007110	00DE0D32	0F000000	""	---
1444	0	00007118	00003D58	300F0000	""	---
1446	0	00010080	00000000	00000000	P3 MEM RD IN norm_data	---
1447	0	00010088	00000000	00000000	""	---
1448	0	00010090	00000000	00000000	""	---
1449	0	00010098	00000000	00000000	""	---
1450	0	A0000000	--------	--------	P2 SPEC: FLUSH no_data	---
1455	0	00001060	00409300	20000402	P3 MEM READ norm_data	---

Figure 2–4: Complex data display in Hardware format in By Transaction mode

Transaction Without Data. Some transactions do not have data. Figure 2–5 shows a transaction without data in the Hardware display format. In this figure, samples 1567, 1568, 1569, and 1570 show data that is linked with the request on sample 1561 (a Fetch).

A request without data occurs in sample 1566, a Flush Special cycle. Since the transactions are shown in the order in which they occur, sample 1570 shows the request without data on the second line. Sample 1567 is an Invalidate cycle without data and is shown on the third line of sample 1570. There is no data to display in the Data and Data_Lo channel groups and the response `no_data` is also shown in the mnemonic. All group values are dashed out. You can see the group values associated with the transaction in the Software, Control Flow, or Subroutine display formats.

Sample	A	Address	Data	Data_Lo	Mnemonic	Async>
1560	0	00020060	--------	--------	P3 INVALIDATE 1560 no_data	---
1561	0	000070A0	--------	--------		---
1562	-	--------	--------	--------		---
1563	-	--------	--------	--------		---
1564	-	--------	--------	--------		---
1565	-	--------	--------	--------		---
1566	0	A0000000	--------	--------		---
1567	0	00020080	22OF9FFF	FFFF25C0	P2 FETCH 1561 norm_data	---
1568	-	--------	B8D98E00	20B966C0	""	---
1569	-	--------	05C10FF0	00000001	""	---
1570	-	--------	0000003D	00000080	""	---
	-	--------	--------	--------	P1 SPEC: FLUSH 1566 no_data	----->
	-	--------	--------	--------	P3 INVALIDATE 1567 no_data	----->
1571	-	--------	--------	--------		---
1572	-	--------	--------	--------		---
1573	-	--------	--------	--------		---
1574	-	--------	--------	--------		---

Figure 2–5: Transaction without data in the Hardware format

Software Display Format

For the trace agent, the Software display format shows only fetch transactions, Special cycles, and, occasionally, a transaction without a Data phase. Acquired data is always displayed By Transaction. Flush and Extension cycles are displayed, and Cache Line Fill cycles are not displayed.

This format is usually used with Instructions or Both selected in the Mnemonics Shown field of the Disassembly property page (the Disassembly Format Definition overlay).

The Special cycles displayed are as follows:

RESERVED 0	RESERVED 6	SPEC: FL ACK
INT ACK	RESERVED 7	SPEC: STP CK ACK
SPECIAL	SPEC: NOP	SPEC: SMI ACK
RESERVED 1	SPEC: SHUTDN	UNKNOWN
BRANCH TRACE	SPEC: FLUSH	RESET
RESERVED 3	SPEC: HALT	BUS INIT
RESERVED 4	SPEC: SYNC	INIT
RESERVED 5		

Some cycles not associated with an agent can affect the entire system. RESET, BUS INIT, and INIT cycles are always displayed regardless of the selection in the Other Agent field in the Disassembly property page (the Disassembly Format Definition overlay).

Control Flow Display Format

For the trace agent, the Control Flow display format shows only the first fetch of instructions which cause a branch in addressing, and Special cycles. Other transactions originated by the trace agent are not displayed.

This format is usually used with Instructions or Both selected in the Disassembly property page (the Disassembly Format Definition overlay).

Instructions that generate a change in the flow of control in the Pentium Pro microprocessor are as follows:

CALL	IRET	RET
INT	JMP	RSM

Instructions that might generate a change in the flow of control are as follows:

CMOV	JL/JNGE	JNS
FCMOV	JLE/JNG	JO
LOOP	JNB/JAE/JNC	JP/JPE
LOOPNZ/LOOPNE	JNBE/JA	JS
LOOPZ/LOOPE	JNE/JNZ	BOUND
JB/JNAE/JC	JNL/JGE	DIV
JBE/JNE	JNLE/JG	IDIV
JCXZ/JECXZ	JNO	INTO
JE/JZ	JNP/JPO	

The Special cycles displayed are as follows:

RESERVED 0	RESERVED 6	SPEC: FL ACK
INT ACK	RESERVED 7	SPEC: STP CK ACK
SPECIAL	SPEC: NOP	SPEC: SMI ACK
RESERVED 1	SPEC: SHUTDN	UNKNOWN
BRANCH TRACE	SPEC: FLUSH	RESET
RESERVED 3	SPEC: HALT	BUS INIT
RESERVED 4	SPEC: SYNC	INIT
RESERVED 5		

Some cycles not associated with an agent can affect the entire system. RESET, BUS INIT, and INIT cycles are always displayed regardless of the selection in the Other Agent field in the Disassembly property page (the Disassembly Format Definition overlay).

Subroutine Display Format

For the trace agent, the Subroutine display format shows only the first fetch of subroutine call and return instructions, and Special cycles. Other transactions originated by the trace agent are not displayed.

This format is usually used with Instructions or Both selected in the Mnemonics Shown field of the Disassembly property page (the Disassembly Format Definition overlay).

Instructions that generate a change in the flow of control in the Pentium Pro microprocessor are as follows:

CALL	IRET	RSM
INT	RET	

Instructions that might generate a change in the flow of control are as follows:

BOUND	IDIV
DIV	INTO

The Special cycles displayed are as follows:

RESERVED 0	RESERVED 6	SPEC: FL ACK
INT ACK	RESERVED 7	SPEC: STP CK ACK
SPECIAL	SPEC: NOP	SPEC: SMI ACK
RESERVED 1	SPEC: SHUTDN	UNKNOWN
BRANCH TRACE	SPEC: FLUSH	RESET
RESERVED 3	SPEC: HALT	BUS INIT
RESERVED 4	SPEC: SYNC	INIT
RESERVED 5		

Some cycles not associated with an agent can affect the entire system. RESET, BUS INIT, and INIT cycles are always displayed regardless of the selection in the Other Agent field in of the Disassembly property page (the Disassembly Format Definition overlay).

Changing How Data is Displayed

There are fields and features that allow you to further modify displayed data to suit your needs. You can make selections unique to this software to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception vectors

Optional Display Selections

You can make optional display selections for disassembled data to help you analyze the data. You can make these selections in the Disassembly property page (the Disassembly Format Definition overlay).

In addition to the common display options (described in the information on basic operations), you can change the displayed data in the following ways:

- Choose to display Branch Trace Messages on one or two lines
- Select which Pentium Pro microprocessor (agent) you want to trace
- Choose to display or suppress cycles from all nontrace Pentium Pro microprocessors or agents in the system
- Select the type of code memory
- Choose the type of disassembly to display
- Select a mode in which to display data in the Hardware format
- Select the code segment size
- Choose an interrupt table
- Specify the starting address of the interrupt table
- Specify the size of the interrupt table

The Pentium Pro microprocessor support product has eleven additional fields: BTM Display, Trace Agent, Other Agents, Code Memory Type, Mnemonics Shown, Hardware Mode, Code Segment Size, Interrupt Table, Interrupt Table Hi Address, Interrupt Table Lo Address, and Interrupt Table Size. These fields appear in the area indicated in the information on basic operations.

Figure 2–6 shows the setup of the Disassembly property page (the Disassembly Format Definition overlay) for the P6 Demo system file. The P6 Demo file contains data acquired from a SUT with cached memory.

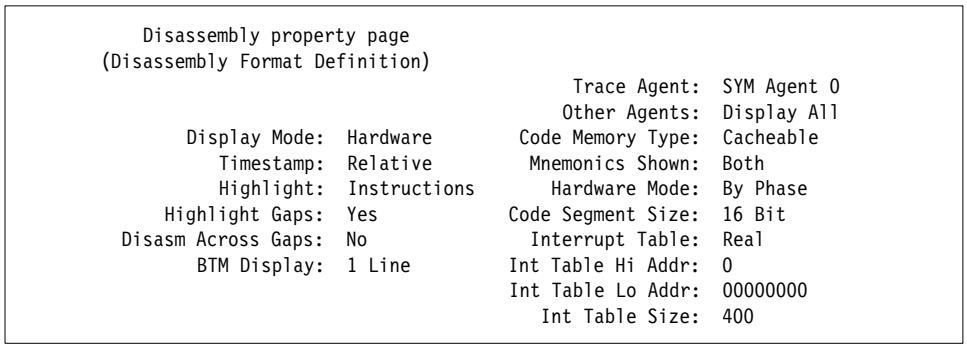


Figure 2–6: Disassembly property sheet (Disassembly Format Definition overlay) for the P6 Demo refmem file

Figure 2–7 shows the setup of the Disassembly property page (the Disassembly Format Definition overlay) for the P6 Demo2 system file. The P6 Demo2 file contains data from a SUT with uncached memory.

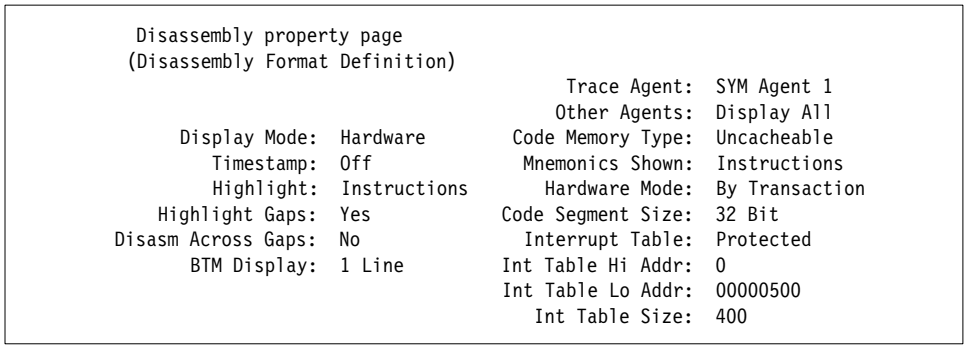


Figure 2–7: Disassembly property sheet (Disassembly Format Definition overlay) for the P6 Demo2 refmem file

BTM Display. You can display Branch Trace Messages on one or two lines. A single line display shows a Branch Trace Message as it occurred. A double line display shows the same address on the first line, and the destination address on the second line.

Trace Agent. You can select which Pentium Pro agent to trace. You can choose to trace one agent from the Symmetric Agents 0 through 7, or from the Priority Agents 0 through 7. Symmetric is abbreviated as SYM in the selection list, and priority is abbreviated as PRI. The default is SYM Agent 0.

Other Agents. You can choose to display or suppress bus cycles from agents other than the one selected in the Trace Agent field. You can choose to display the following types of cycles from other agents: all other cycles (Display All), only Fetch cycles, only Special cycles, or only Fetch and Special cycles. You can also choose to not display cycles from other agents (Suppress All). The default is Display All.

When viewing data in the Hardware display format and the selection in the Hardware Mode field is set to By Phase, all cycles from all agents are displayed. This combination effective sets the Other Agent field to Display All. Selections other than Display All are ignored.

Code Memory Type. You can choose the type of memory to disassemble as cacheable or unCacheable. If you select Cacheable, the disassembler will not attempt to determine which cycles are flushed. You will need to use the Mark Cycle function to change cycles to Flushed. If you select UnCacheable, the disassembler will attempt to flush unexecuted instruction fetch cycles. The default is Cacheable.

Mnemonic Shown. You can choose to display disassembled bus cycles as instruction mnemonics and cycle types (Instructions), as bus transactions (Transactions), or as both. The default is Both.

NOTE. *Be aware that the Transactions selection in the Mnemonic Shown field is very different than the By Transaction selection in the Hardware Mode field.*

Hardware Mode. When viewing data in the Hardware format, you can also choose to display the data by phase or by transaction. The By Phase selection shows all samples of acquired data in the order they occurred. The By Transaction selection rearranges the phases so the channel group values are displayed with the transaction. The sample containing the Data phase shows all the transaction information.

Selections in this field have no effect on the Software, Control Flow, or Subroutine display formats.

Code Segment Size. You can select the default code segment size to be 16 or 32 bit. The default is 16 bit.

Interrupt Table. You can specify if the interrupt table is Real or Protected. (Selecting Virtual is equivalent to selecting Protected.) The default is Real.

Int Table Hi Addr and Int Table Lo Addr. If your SUT has had its vector table relocated, you must use both Interrupt Table Address fields to inform the disassembler of the new base of the upper 4 address bits, A35-A32, as well as the new base of the lower 32 address bits, A31-A0. If the values in either the Int Table Hi Addr or Int Table Lo Addr fields are incorrect, the disassembler will not interpret interrupts or exceptions correctly.

You can use the Int Table Hi Addr field to inform the disassembler of the new base of the upper 4 address bits. You can specify the starting address in hexadecimal. The default starting address is 0.

You can use the Int Table Lo Addr field to inform the disassembler of the new base of the lower 32 address bits, A31-A0. You can specify the starting address of the interrupt table in hexadecimal. The maximum value is 0xFFFFFFFC and the minimum value is 0x00000000. The default starting address is 0x00000000. The starting address needs to begin on a long word boundary.

Interrupt Table Size. You can specify the size in bytes of the interrupt table. The maximum value is 0x800 and the minimum value is 0x000. The default size is 0x400.

Code Memory Type

Code can be executed from two types of memory regions: cacheable or uncacheable. The selection in the Code Memory Type field of the Disassembly property page (the Disassembly Format Definition overlay) must match the type of memory region accessed for code fetches by the agent selected in the Trace Agent field. If the selection in the Code Memory Type field does not match, disassembly will be incorrect.

The default setup is to trace code operating within cacheable memory. With cacheable memory, prefetched instructions are only visible on the system bus when cache lines are filled. The disassembler cannot determine instruction boundaries or which instructions are executed, so all prefetched instructions are assumed to be executed. No attempt is made to determine which instructions are flushed. You will need to use the Mark Cycle function to change cycles to Flushed.

You can execute code within uncacheable memory and change the disassembler setup to uncacheable memory to trace code execution. With uncacheable memory, every instruction is refetched. All instructions are visible on the system bus so they can be acquired and disassembled. The disassembler can determine unexecuted instructions, and displays them as (FLUSH).

Branch Trace Messages

You can display Branch Trace Messages (BTM) on one or two lines. You can select one line or two lines in the BTM Display field of the Disassembly property page (the Disassembly Format Definition overlay) to set up the way BTMs are displayed.

When two lines are selected, the first line shows the address of the instruction immediately following the instruction causing the branch and the second line shows shows the address of the instruction at the branch destination.

When one line is selected, a single line is displayed for each BTM. The Data and Data_Lo groups show the address of the instruction immediately following the instruction causing the branch and the address of the instruction at the branch destination, respectively.

Although BTMs are acquired with all the P6 support clocking options, you can use the Branch Trace Messages Only option to acquire only BTMs. No other cycles are acquired with this clocking option.

Figure 2–8 shows an example of BTMs displayed on one line.

```
  Sample  A  Address   Data      Data_Lo   Mnemonic                        Async>
-------------------------------------------------------------------------------
     258  0  00031030  8E002CB8  66C08ED8   ( FLUSH )                      ---
     265  0  00000000  0003102B  00031025   P0 BRANCH TRACE no_data         ---
     274  0  00031025  450A67C0  33660005   OR AL,01[DI]            (32)   ---
```

Figure 2–8: Branch Trace Messages display on one line

Figure 2–9 shows an example of BTMs displayed on two lines.

```
  Sample  A  Address   Data      Data_Lo   Mnemonic                        Async>
-------------------------------------------------------------------------------
     258  0  00031030  8E002CB8  66C08ED8   ( FLUSH )                      ---
     265  0  0003102B  --------  --------   P0 BTM SOURCE                  ---
          -  00031025  --------  --------      BTM TARGET                  ----->
     274  0  00031025  450A67C0  33660005   OR AL,01[DI]            (32)   ---
```

Figure 2–9: Branch Trace Messages display on two lines

Agent Tracing

When acquiring data from a SUT with multiple Pentium Pro microprocessors, the software disassembles only the instructions executed from the trace agent.

You can trace instructions and transactions from Symmetric Agents 0 through 7, or from Priority Agents 0 through 7, and also display or suppress data from the other agents not selected in the Trace Agent field. You can choose to display the following types of cycles for other agents: all other cycles (Display All), only Fetch cycles, only Special cycles, or only Fetch and Special cycles. You can also choose to not display cycles from other agents (Suppress All).

To set up the mode of tracing, you need to select an agent in the Trace Agent field, and to display or suppress bus cycles in the Other Agent field in the Disassembly property page (the Disassembly Format Definition overlay).

Deferred Transactions

The response to some bus transactions requests can be deferred. Transactions that have been deferred are shown in the mnemonic as `DID=##`, where ## is the identification number assigned when the request was deferred (DeferID number). The deferred reply shows the same DID=## as the original request. Each transaction is assigned a unique DID value that remains unique until the transaction is complete.

You can use the substring DID=##, where ## is the identification number, in the Search Definition dialog box (Disassembly Search Definition overlay) for finding transactions that go together.

Figure 2–10 shows an example of disassembled deferred transactions. A request that was deferred is on sample 83. The deferred reply transaction is on sample 105. The original request and deferred reply both show DID=00.

```
  Sample  A  Address   Data      Data_Lo   Mnemonic                          Async>
-------------------------------------------------------------------------------------
      81  0  012B2B90  --------  E1170CB4   P1 MEM READ norm_data             ---
          0  18000000  --------  --------   A1 DEFER RPL DID=00 no_data       ---
      83  0  00000020  --------  --------   P0 IO READ DID=00 deferred        ---
      89  0  001955F8  24748B56  1424448B   P1 FETCH norm_data                ---
      90  0  001955F0  53801AA4  940D89C9   ""                                ---
      91  0  001955E8  3308EC83  CC0008C2   ""                                ---
      92  0  001955E0  5DE58B5B  5E5FC033   ""                                ---
      94  0  012B2B78  --------  00051BB0   P1 MEM WRITE no_data              ---
     101  0  001955F8  24748B56  1424448B   P1 FETCH norm_data                ---
     102  0  001955F0  53801AA4  940D89C9   ""                                ---
     103  0  001955E8  3308EC83  CC0008C2   ""                                ---
     104  0  001955E0  5DE58B5B  5E5FC033   ""                                ---
     105  0  0C000000  --------  ------00   A1 DEFER RPL DID=00 norm_dat>     ---
     109  0  00195600  1AA49035  89555714   P1 FETCH norm_data                ---
```

Figure 2–10: Deferred transactions in Hardware format

Out-of-Order Fetches

The Pentium Pro microprocessor can prefetch cycles out of ascending order. For example, a branch to address 1008 will cause the following sample of addresses across the bus: 1008, 1000, 1018, and 1010. The data at address 1008 is executed, but the data at address 1000 is not; it just fills the cache. The data at addresses 1018 and 1010 are executed, but the data at 1010 is executed before the data at 1018. The fetched order versus the executed order in this example is as follows:

Fetched Order	Executed Order
1008	1008
1000	1010
1018	1018
1010	

In the Hardware display format, the out-of-order fetches are displayed in the order they are fetched. They will be properly disassembled and identified by an asterisk to the left of the instruction.

You can determine the executed order of the out-of-order fetches by looking at the address of the out-of-order cycles and subsequent cycles in the Hardware format. Fetch cycles always have the sample number displayed.

Figure 2–11 shows an example of an out-of-order fetch in the Hardware format.

```
  Sample  A  Address   Data      Data_Lo   Mnemonic
-------------------------------------------------------------------------------
     257  0  0001D028  7DE80000  004D6804   P1 FETCH norm_data
          0  0001D029  7DE80000  004D6804   PUSH #0000004D          (32)
     258  0  0001D020  6A026A00  00002D68   ( CACHE LINE FILL )
     259  0  0001D038  68000000  55850F00  *( FLUSH )
     260  0  0001D030  0000FF25  58000000   ( FLUSH )
     262  0  0000D3CC  0000004D  --------   P1 MEM WRITE no_data
     268  0  0001D028  7DE80000  004D6804   P1 FETCH norm_data
          0  0001D02E  7DE80000  004D6804   CALLS 0001D0B0          (32)
     269  0  0001D020  6A026A00  00002D68   ( CACHE LINE FILL )
     270  0  0001D038  68000000  55850F00  *( FLUSH )
     271  0  0001D030  0000FF25  58000000   ( EXTENSION )
     273  0  0000D3C8  --------  00000033   P1 MEM WRITE no_data
     279  0  0001D0B0  04870824  44875050   P1 FETCH norm_data
          0  0001D0B0  04870824  44875050   PUSH EAX                (32)
```

Figure 2–11: Out-of-Order fetches in Hardware format

In Software display, fetches are displayed in the order they were executed. If the previous executed instruction had a larger sample number than the fetch, the sample number is not displayed. If the previous sample had a smaller sample number than the fetch, the sample number is displayed. To mark an instruction without a sample number, you will have to change to the Hardware format.

Figure 2–12 shows an example of out-of-order fetches in the Software format.

Sample	A	Address	Data	Data_Lo	Mnemonic	
257	0	0001D028	7DE80000	004D6804	P1 FETCH norm_data	
	0	0001D029	7DE80000	004D6804	PUSH #0000004D	(32)
260	0	0001D030	0000FF25	58000000	(FLUSH)	
	0	0001D038	68000000	55850F00	*(FLUSH)	
268	0	0001D028	7DE80000	004D6804	P1 FETCH norm_data	
	0	0001D02E	7DE80000	004D6804	CALLS 0001D0B0	(32)
271	0	0001D030	0000FF25	58000000	(EXTENSION)	
	0	0001D038	68000000	55850F00	*(FLUSH)	
279	0	0001D0B0	04870824	44875050	P1 FETCH norm_data	
	0	0001D0B0	04870824	44875050	PUSH EAX	(32)

Figure 2–12: Out-of-Order fetches in Software format

System Management Mode

The Pentium Pro microprocessor can operate in System Management Mode. This is a special mode where the CPU executes code from a separate, alternate memory space called SMRAM. To view the signals associated with this mode, you need to change the radix of the Extend channel group to SYM and select the P6_EXT symbol table.

Marking Cycles

The disassembler has a Mark Cycle function that allows you to change the interpretation of a fetch cycle type. Using this function, you can select an opcode fetch cycle and change it to one of the following cycle types:

- Opcode (the first word of an instruction)
- Flush (an opcode or extension that is fetched but not executed)

You can only use the Mark Cycle function to change fetch cycles, except for Cache Line Fill cycles.

If the disassembler is set to trace code from cacheable memory, the disassembler assumes that any Cache Line Fill from a code segment that is not contiguous with the most recent code segment Cache Line Fill by that agent represents a program branch. For the same reason, the disassembler also assumes that the first byte of that prefetch is a valid opcode. If these assumptions are incorrect, you can use the Mark Cycles function to correct the disassembler's interpretation.

When viewing data in the Software format, and an out-of-order fetch does not have a sample number, you will have to change to Hardware format to mark the cycle.

There are two methods you can use to change the interpretation of a cycle. You can place marks on individual bytes of a sample or on the entire cycle.

Marking Individual Bytes. You can change the individual bytes of a sample to a Flush or Opcode cycle, as well as undo a mark placed on a byte. To do this, follow these steps:

1. Place the cursor on the cycle with the byte(s) to be marked.
2. Press **F4: MARK DATA**. A list of selections appear that allows you to select an individual byte to mark. For example, byte selections for sample 9 in the P6 Demo file are as follows:

```
-- -- -- --     -- -- -- 90          →
-- -- -- --     -- -- 0F --          →
-- -- -- --     -- 08 -- --          →
-- -- -- --     B8 -- -- --          →
-- -- -- 00     -- -- -- --          →
-- -- 0C --     -- -- -- --          →
-- 8E -- --     -- -- -- --          →
D8 -- -- --     -- -- -- --          →
```

3. Select the byte you want to mark and open the second list of marks.

```
Flush
Opcode
Undo
```

4. Select the cycle type you want associated with the byte and press **Return**.

Marking the Entire Cycle. You can change the entire cycle to a Flush cycle, change the default segment size, or undo all marks placed on a sample. To do this, follow these steps:

1. Place the cursor on the cycle to be marked.
2. Press **F4: MARK DATA**. A list of selections appear. Below the list of individual bytes are the mark selections for the entire cycle as follows:

```
FLUSH CYCLE
16-Bit Default Segment Size
32-Bit Default Segment Size
Undo marks on this cycle
```

3. Select the cycle type you want associated with the current cycle and press **Return**.

If you mark a cycle as a FLUSH CYCLE, and reopen the list of mark selections, all the individual bytes will appear as Flush in the selection list. An example is as follows:

```
--  --  --  --     --  --  --  90   (flush)  →
--  --  --  --     --  --  0F  --   (flush)  →
--  --  --  --     --  08  --  --   (flush)  →
--  --  --  --     B8  --  --  --   (flush)  →
--  --  --  00     --  --  --  --   (flush)  →
--  --  0C  --     --  --  --  --   (flush)  →
--  8E  --  --     --  --  --  --   (flush)  →
D8  --  --  --     --  --  --  --   (flush)  →
```

If you mark an individual byte as an Opcode, the flushed bytes before the byte marked Opcode remain flushed and the bytes that follow are undone as follows:

```
--  --  --  --     --  --  --  90   (flush)  →
--  --  --  --     --  --  0F  --   (flush)  →
--  --  --  --     --  08  --  --   (flush)  →
--  --  --  --     B8  --  --  --   (flush)  →
--  --  --  00     --  --  --  --   (opcode) →
--  --  0C  --     --  --  --  --            →
--  8E  --  --     --  --  --  --            →
D8  --  --  --     --  --  --  --            →
```

You can mark individual bytes and other marks will not be undone as follows:

```
--  --  --  --     --  --  --  90   (opcode) →
--  --  --  --     --  --  0F  --   (flush)  →
--  --  --  --     --  08  --  --   (flush)  →
--  --  --  --     B8  --  --  --   (flush)  →
--  --  --  00     --  --  --  --   (opcode) →
--  --  0C  --     --  --  --  --            →
--  8E  --  --     --  --  --  --            →
D8  --  --  --     --  --  --  --            →
```

In this situation, (FLUSH) will not be displayed in the Mnemonic column for the sample.

Information on basic operations contains more details on marking cycles.

Marking the Default Segment Size. You can use the Mark Cycle function to specify the default segment size mode (16-bit or 32-bit) for the cycle. The segment size selection changes the cycle the cursor is on and the remaining cycles to the end of memory or to the next mark.

The default segment size of the cycle is independent of any prefix override bytes in the particular fetch. For example, if you mark a cycle with a default segment size of 32 bits, but there are address/operand prefixes in the instruction, the default segment size will be 32 bits but the size of the instruction will be 16 bits.

Since you can only make one selection at a time, if you want to mark the opcode and the default segment size of a cycle, you must do them in separate steps.

Exception Vectors

For the trace agent, the disassembler also displays Pentium Pro exception vectors if the vector table resides in external memory. You can select to display the interrupt vectors for Real, Virtual, or Protected mode in the Interrupt Table field of the Disassembly property page (the Disassembly Format Definition overlay). (Selecting Virtual is equivalent to Protected.)

The disassembler initially assumes that the exception vector table is at address 00000000 (the default value). However, if the table is relocated, you can use the Int Table Hi Addr and Int Table Lo Addr fields in the Disassembly property page (the Disassembly Format Definition overlay) to match the new location.

The Int Table Hi Addr and Int Table Lo Addr fields provide the disassembler with the offset address; enter a one-digit hexadecimal value corresponding to the offset of the base of the upper 4 address bits, A35-A32, and an eight-digit hexadecimal value corresponding to the offset of the base of the lower 32 address bits, A31-A0, of the exception table.

When the Pentium Pro microprocessor processes an exception, the disassembler displays the type of exception, if known.

The exception names displayed cannot be used for triggering. You should use cycle types, such as MEM RDs, to set up the trigger specification.

Table 2–11 lists the Pentium Pro exception vectors for the Real Addressing mode.

Table 2–11: Exception vectors for Real Addressing mode

Exception number	Location in IV* table (in hexadecimal)	Displayed exception name
0	0000	DIVIDE ERROR
1	0004	DEBUG EXCEPTIONS
2	0008	NMI INTERRUPT
3	000C	BREAKPOINT INTERRUPT
4	0010	INTO DETECTED OVERFLOW
5	0014	BOUND RANGE EXCEEDED
6	0018	INVALID OPCODE
7	001C	DEVICE NOT AVAILABLE

Table 2–11: Exception vectors for Real Addressing mode

Exception number	Location in IV* table (in hexadecimal)	Displayed exception name
8	0020	DOUBLE FAULT
9-11	0024-002C	RESERVED
12	0030	STACK EXCEPTION
13	0034	SEGMENT OVERRUN
14-15	0038-003C	RESERVED
16	0040	COPROCESSOR ERROR
17-31	0044-007C	RESERVED
32-255	0080-03FC	USER DEFINED

*** IV means interrupt vector.**

Table 2–12 lists the Pentium Pro exception vectors for the Protected Addressing mode.

Table 2–12: Exception vectors for Protected Addressing mode

Exception number	Location in IDT* (in hexadecimal)	Displayed exception name
0	0000	DIVIDE ERROR
1	0008	DEBUG EXCEPTIONS
2	0010	NMI INTERRUPT
3	0018	BREAKPOINT INTERRUPT
4	0020	INTO DETECTED OVERFLOW
5	0028	BOUND RANGE EXCEEDED
6	0030	INVALID OPCODE
7	0038	DEVICE NOT AVAILABLE
8	0040	DOUBLE FAULT
9	0048	RESERVED
10	0050	INVALID TSS
11	0058	SEGMENT NOT PRESENT
12	0060	STACK EXCEPTION
13	0068	GENERAL PROTECTION
14	0070	PAGE FAULT
15	0078	RESERVED
16	0080	COPROCESSOR ERROR
17	0088	ALIGNMENT CHECK
18	0090	MACHINE CHECK

Table 2–12: Exception vectors for Protected Addressing mode (cont.)

Exception number	Location in IDT* (in hexadecimal)	Displayed exception name
19-31	0098-00F8	RESERVED
32-255	0100-07F8	USER DEFINED

*** IDT means interrupt descriptor table.**

Searching Through Data

You can use the Search Definition dialog box (Disassembly Search Definition overlay) to define specific data values to find in the disassembled data. Information on basic operations describes this dialog box.

You can search for types of mnemonics displayed by the disassembler.

***NOTE**. For the Pentium Pro support, you should only use the Hardware selection in the Mnemonic Type field. Any other selection will not be productive.*

To search for multiple phases of a single Pentium Pro transaction, the disassembled data should be displayed By Transaction. You can change the display to By Transaction in the Mnemonic Shown field of the Disassembly property page (Disassembly Format Definition overlay).

Figure 2–13 shows one method you can use to set up the Search Definition dialog box (Disassembly Search Definition overlay) for acquired Pentium Pro data.

```
Search Definition dialog box
(Disassembly Search Definition)

Mnemonic Type:  Hardware


                                  Search Criteria
92A96SD-1 ------------------------------------------------------------

    Group:  Data     Data _Lo   Mnemonic
     Mode:  Ignore   Equal      Text
    Radix:           Hex        Substring
  Sym Tbl:
                     =000007FF  = MEM READ
```

Figure 2–13: Search defined for Pentium Pro data

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your Pentium Pro microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your SUT.

Information on basic operations describes how to view the file.

Basic Transaction Operations

A data sample can contain information for up to five phases of a bus transaction. Table 2–13 shows the channel groups (defined by the P6 support setup) the disassembler considers valid for various phases of a transaction. The disassembler links the various phases of each transaction together.

Table 2–13: Valid groups for phases of a bus transaction

Request phase	Error phase	Snoop phase	Response phase	Data phase
A	Err	Snoop	Response	Data
Address				Data_Lo
Attr				Dep
DeferID				Data_Ctl
DataSize				Async
Extend				Mnemonic*
REQab				
PAL†				

***** **A group defined by the disassembler that is not a channel group.**

† **A group defined by the TMS 110 support that does not contain Pentium Pro signals; the group is valid for all phases, but only displays for Request phases.**

The Mnemonic column shows information about the bus transaction and is displayed with the Data phase. Figure 2–14 shows the order that this information is displayed in the Mnemonic column if it is acquired and disassembled.

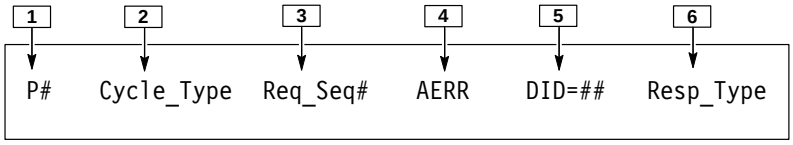


Figure 2–14: Types of information displayed in the Mnemonic column

1 **Agent Number.** The Pentium Pro microprocessor identification number as P# for the symmetric agent or A# for the nonmicroprocessor agent, where # is the AgentID number.

2 **Request Type.** The request type shown as cycle type labels; Table 2–10 lists the cycle type labels.

3 **Request Phase Sample Number.** The sample number of the Request phase (Hardware display format By Phase only)

4 **AERR# Signal Observed or Ignored.** The assertion of the AERR# signal; when AERR# is observed, the disassembler displays `AERR-OBSERVED`; when AERR# is ignored, the disassembler displays `(AERR).`

5 **Deferred Transactions.** Deferred response and deferred reply transactions shown as `DID=##`, where ## is the DeferID number of the original transaction.

6 **Response Type.** The type of response; the response matches the symbols in the Response group symbol table except in the mnemonic it is displayed as all lower case; Table 2–5 shows the Response group symbol table.

Some bus transactions will not have a Data phase. The absence of a Data phase can be caused by an error in the transaction before it has reached the Data phase, or when any one of the RESET#, INIT#, or BINIT# signals is asserted.

When the transaction does not have a Data phase, the disassembler inserts an additional line without a sample number between complete lines to maintain a chronological order of bus transactions.

Specifications

Specifications

This chapter contains the following information:

- Probe adapter description
- Specification tables
- Dimensions of the probe adapter
- Channel assignment tables
- Description of how the module acquires Pentium Pro signals
- List of other accessible microprocessor signals and extra acquisition channels

Probe Adapter Description

The probe adapter is nonintrusive hardware that allows the logic analyzer to acquire data from a microprocessor in its own operating environment with little effect, if any, on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of two circuit boards. The probe adapter connects to the SUT. Signals from the microprocessor-based system flow from the probe adapter to the podlet groups and through the probe signal leads to the module.

All circuitry on the probe adapter is powered from the power supply included with the product.

The probe adapter accommodates the Intel Pentium Pro microprocessor in a 387-pin PGA package.

Configuration

There are five jumpers on the probe adapter used to configure it for disassembler operation or to acquire timing data. Table 3–1 shows a summary of the jumpers, positions, and function. For more descriptive information, refer to *Configuring the Probe Adapter* on page 1–3.

Table 3–1: Jumper positions and function

Jumper	Position	Function
J1200	Pins 1, 2	Use when the frequency of the SUT is 45 to 66 MHz.
	Pins 2, 3	Use when the frequency of the SUT is below 45 MHz.

Table 3–1: Jumper positions and function (Cont.)

Jumper	Position	Function
J1201	Pins 1, 2	Use to synthesize A2-A0 using the BE7#-BE0# signal bits in the Request phase.
	Pins 2, 3	Use to hold A2-A0 high (false).
J1205*	Pins 1, 2	Use to acquire asynchronous signals using Custom or External clocking with the P6_TMG support setup.
	Pins 2, 3	Use to acquire asynchronous signals using Internal clocking with the P6_TMG support setup.
J1206	Pins 1, 2	Use to acquire synchronous signals using Custom clocking with the P6 support setup.
		Use to acquire synchronous signals for timing using Custom or External clocking with P6_TMG support setup.
	Pins 2, 3	Use to acquire synchronous signals using Internal clocking with the P6_TMG support setup.
J1207	Pins 1, 2	Use to acquire data with the P6 support setup; this setup must be used for disassembly (Custom clocking).
	Pins 2, 3	Use to acquire data with the P6_TMG support setup; this setup must be used for timing (Custom, External, or Internal clocking).

*** The position of J1205 does not matter when using the P6 support setup.**

Figure 3–1 shows the jumper locations on the probe adapter.

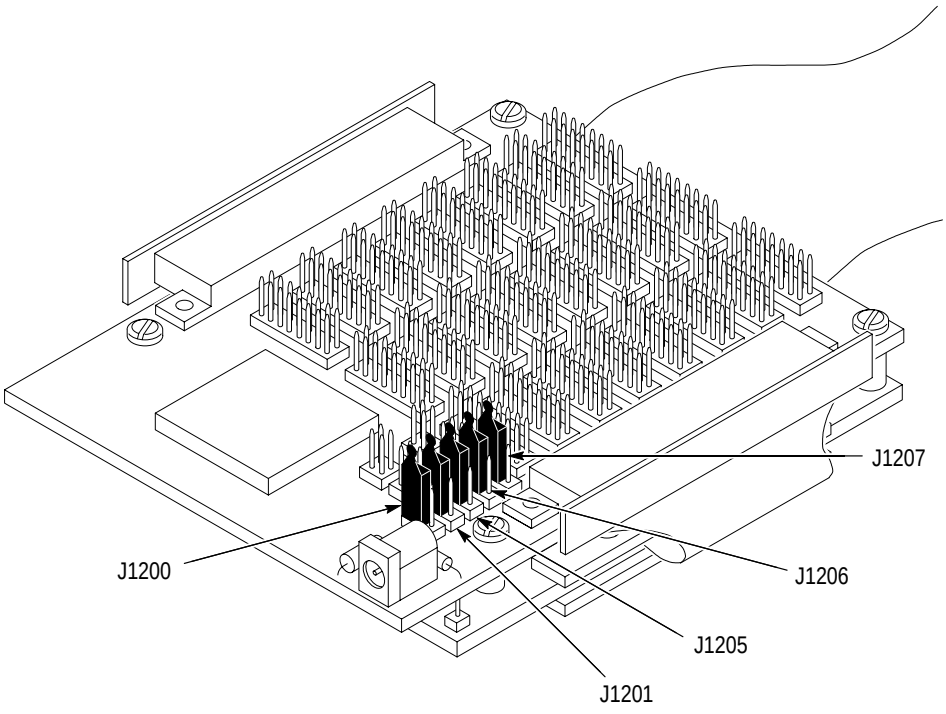


Figure 3–1: Jumper locations on the probe adapter

Specifications

These specifications are for a probe adapter connected between a compatible Tektronix logic analyzer and a SUT. The TMS 110 probe adapter meets the Pentium Pro GTL+ timing and loading requirements. Signal voltage swing in your SUT must be ± 400 mV around the GTL reference voltage.

Table 3–2 shows the electrical requirements the SUT must produce for the support to acquire correct data, and requirements for the power supply that provides power to the TMS 110 probe adapter.

In the table, for the 204-channel module, one podlet load is 20 kΩ in parallel with 2 pF. For the 192-channel module, one podlet load is 100 kΩ in parallel with 10 pF.

Table 3–2: Electrical specifications

Characteristics	Requirements	
Probe adapter power supply requirements		
Voltage	90-265 VAC	
Current	1.1 A maximum at 100 VAC	
Frequency	47-63 Hz	
Power	25 W maximum	
SUT clock		
Clock rate	Max. 66 MHz	
Minimum setup time required, all signals	4.5 ns	
Minimum hold time required, all signals	1.5 ns	
	Specification	
	AC load	**DC load**
Measured typical SUT signal loading, all signals	4 pF	75 kΩ

Figure 3–2 shows the input loading for GTL and 3.3 V tolerant signals on the TMS 110 probe adapter.

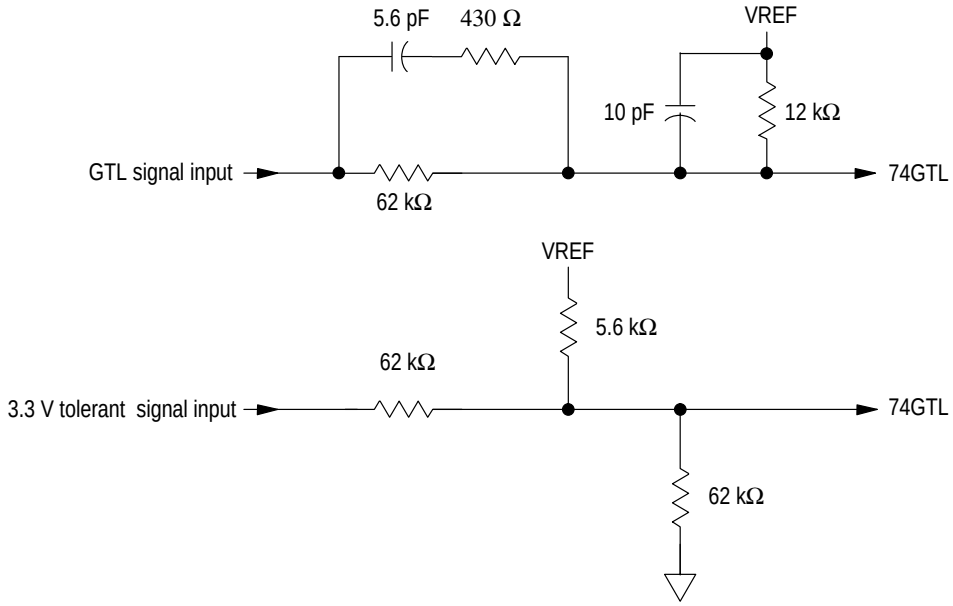


Figure 3–2: GTL signal and 3.3 V tolerant signal input loading

Table 3–3 shows the environmental specifications.

Table 3–3: Environmental specification*

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F)†
Minimum operating	0° C (+32° F)
Nonoperating	–55° C to +75° C (–67° to +167° F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Nonoperating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

*** Designed to meet Tektronix standard 062-2847-00 class 5.**

† **Not to exceed Pentium Pro microprocessor thermal considerations. Forced air cooling might be required across the CPU.**

Table 3–4 shows the certifications and compliances that apply to the probe adapter.

Table 3–4: Certifications and compliances

EC Compliance	There are no current European Directives that apply to this product.
Pollution Degree 2	Do not operate in environments where conductive pollutants may be present.

Figure 3–3 shows the dimensions of the probe adapter.

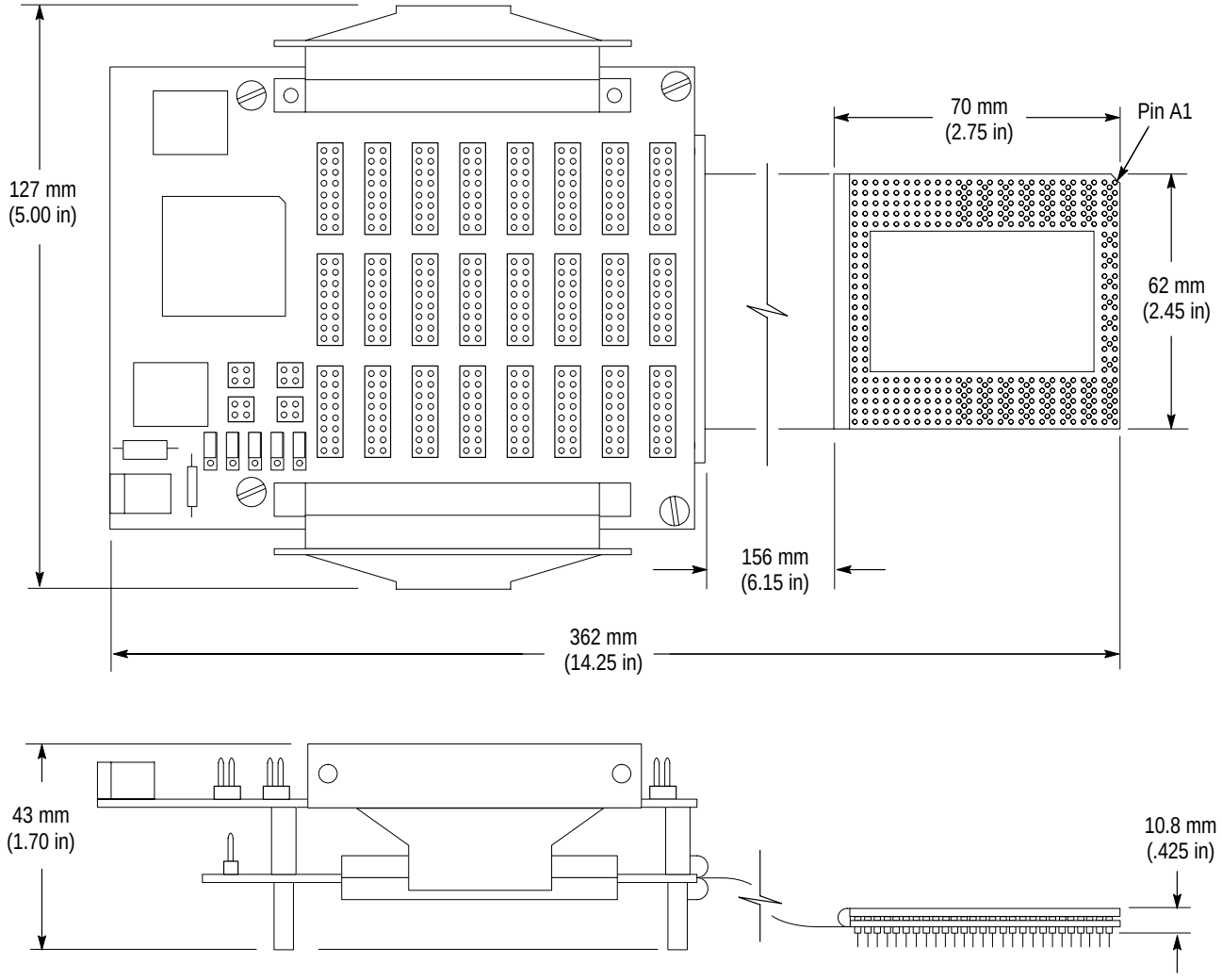


Figure 3–3: Dimensions of the probe adapter

Channel Assignments

Channel assignments shown in Table 3–5 through Table 3–42 use the following conventions:

- All signals are required for disassembly (P6 setup with Custom clocking) or general purpose analysis (P6_TMG setup with Custom, External, or Internal clocking) unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- A pound sign (#) following a signal name indicates an active low signal.
- An underscore D (_D) indicates a signal that is derived by the probe adapter.
- The module in the higher-numbered slot is referred to as the HI module and the module in the lower-numbered slot is referred to as the LO module.

P6 Setup

Tables 3–5 through 3–23 show the channel assignments for the P6 setup used to disassemble data with Custom clocking.

Table 3–5 shows the probe section and channel assignments for the A group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–5: P6: A group channel assignments

Bit order	Section: channel	Pentium Pro signal name
3	LO_C1:7	A35
2	LO_C1:3	A34
1	LO_C0:7	A33
0	LO_C0:3	A32

Table 3–6 shows the probe section and channel assignments for the Address group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–6: P6: Address group channel assignments

Bit order	Section: channel	Pentium Pro signal name
31	LO_A3:7	A31
30	LO_A3:6	A30
29	LO_A3:5	A29
28	LO_A3:4	A28
27	LO_A3:3	A27
26	LO_A3:2	A26
25	LO_A3:1	A25
24	LO_A3:0	A24
23	LO_A2:7	A23
22	LO_A2:6	A22
21	LO_A2:5	A21
20	LO_A2:4	A20
19	LO_A2:3	A19
18	LO_A2:2	A18
17	LO_A2:1	A17
16	LO_A2:0	A16
15	LO_A1:7	A15
14	LO_A1:6	A14
13	LO_A1:5	A13
12	LO_A1:4	A12
11	LO_A1:3	A11
10	LO_A1:2	A10
9	LO_A1:1	A9
8	LO_A1:0	A8
7	LO_A0:7	A7
6	LO_A0:6	A6
5	LO_A0:5	A5
4	LO_A0:4	A4
3	LO_A0:3	A3
2	LO_A0:2	A2
1	LO_A0:1	A1
0	LO_A0:0	A0

Table 3–7 shows the probe section and channel assignments for the Attr group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–7: P6: Attr group channel assignments

Bit order	Section: channel	Pentium Pro signal name
7	LO_D3:7	ATTR7#*
6	LO_D3:6	ATTR6#*
5	LO_D3:5	ATTR5#*
4	LO_D3:4	ATTR4#*
3	LO_D3:3	ATTR3#*
2	LO_D3:2	ATTR2#*
1	LO_D3:1	ATTR1#*
0	LO_D3:0	ATTR0#*

*** Signal not required for disassembly.**

Table 3–8 shows the probe section and channel assignments for the DeferID group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

There is a symbol table that you can use with this group. The name of the symbol table is P6_DID.

Table 3–8: P6: DeferID group channel assignments

Bit order	Section: channel	Pentium Pro signal name
7	LO_D2:7	DID7#
6	LO_D2:6	DID6#
5	LO_D2:5	DID5#
4	LO_D2:4	DID4#
3	LO_D2:3	DID3#
2	LO_D2:2	DID2#
1	LO_D2:1	DID1#
0	LO_D2:0	DID0#

Table 3–9 shows the probe section and channel assignments for the DataSize group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in binary.

Table 3–9: P6: DataSize group channel assignments

Bit order	Section: channel	Pentium Pro signal name
7	LO_D1:7	BE7#
6	LO_D1:6	BE6#
5	LO_D1:5	BE5#
4	LO_D1:4	BE4#
3	LO_D1:3	BE3#
2	LO_D1:2	BE2#
1	LO_D1:1	BE1#
0	LO_D1:0	BE0#

Table 3–10 shows the probe section and channel assignments for the Extend group and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically. The name of the symbol table is P6_EXT.

Table 3–10: P6: Extend group channel assignments

Bit order	Section: channel	Pentium Pro signal name
5	HI_C1:6	ADS_L
4	LO_D0:7	EXF4#
3	LO_D0:6	EXF3#
2	LO_D0:5	EXF2#
1	LO_D0:4	EXF1#
0	LO_D0:3	EXF0#

Table 3–11 shows the probe section and channel assignments for the REQab group and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically. The name of the symbol table is P6_REQ.

Table 3–11: P6: REQab group channel assignments

Bit order	Section: channel	Pentium Pro signal name
12	LO_C1:5	ADS#
11	LO_C3:2	BNR#
10	HI_C3:3	LOCK#
9	LO_C0:1	REQ4
8	LO_C1:4	REQ3
7	LO_C1:0	REQ2
6	LO_C0:4	REQ1
5	LO_C0:0	REQ0
4	LO_C2:1	REQb4
3	LO_C3:4	REQb3
2	LO_C3:0	REQb2
1	LO_C2:4	REQb1
0	LO_C2:0	REQb0

Table 3–12 shows the probe section and channel assignment for the Err group and the microprocessor signal to which the channel connects. By default, this channel group is not visible.

Table 3–12: P6: Err group channel assignment

Bit order	Section: channel	Pentium Pro signal name
0	HI_C2:1	AERR#

Table 3–13 shows the probe section and channel assignments for the Snoop group and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically. The name of the symbol table is P6_SNP.

Table 3–13: P6: Snoop group channel assignments

Bit order	Section: channel	Pentium Pro signal name
3	HI_C1:5	SNOOP_D
2	HI_C3:5	HIT#
1	HI_C3:1	HITM#
0	HI_C2:5	DEFER#

Table 3–14 shows the probe section and channel assignments for the Response group and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically. The name of the symbol table is P6_RSP.

Table 3–14: P6: Response group channel assignments

Bit order	Section: channel	Pentium Pro signal name
2	HI_C1:3	RS2#
1	HI_C0:7	RS1#
0	HI_C0:3	RS0#

Table 3–15 shows the probe section and channel assignments for the Data group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–15: P6: Data group channel assignments

Bit order	Section: channel	Pentium Pro signal name
31	HI_A3:7	D63
30	HI_A3:6	D62
29	HI_A3:5	D61
28	HI_A3:4	D60
27	HI_A3:3	D59
26	HI_A3:2	D58
25	HI_A3:1	D57
24	HI_A3:0	D56
23	HI_A2:7	D55
22	HI_A2:6	D54
21	HI_A2:5	D53
20	HI_A2:4	D52
19	HI_A2:3	D51
18	HI_A2:2	D50
17	HI_A2:1	D49
16	HI_A2:0	D48
15	HI_A1:7	D47
14	HI_A1:6	D46
13	HI_A1:5	D45
12	HI_A1:4	D44
11	HI_A1:3	D43
10	HI_A1:2	D42
9	HI_A1:1	D41
8	HI_A1:0	D40
7	HI_A0:7	D39
6	HI_A0:6	D38
5	HI_A0:5	D37
4	HI_A0:4	D36
3	HI_A0:3	D35
2	HI_A0:2	D34
1	HI_A0:1	D33
0	HI_A0:0	D32

Table 3–16 shows the probe section and channel assignments for the Data_Lo group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–16: P6: Data_Lo group channel assignments

Bit order	Section: channel	Pentium Pro signal name
31	HI_D3:7	D31
30	HI_D3:6	D30
29	HI_D3:5	D29
28	HI_D3:4	D28
27	HI_D3:3	D27
26	HI_D3:2	D26
25	HI_D3:1	D25
24	HI_D3:0	D24
23	HI_D2:7	D23
22	HI_D2:6	D22
21	HI_D2:5	D21
20	HI_D2:4	D20
19	HI_D2:3	D19
18	HI_D2:2	D18
17	HI_D2:1	D17
16	HI_D2:0	D16
15	HI_D1:7	D15
14	HI_D1:6	D14
13	HI_D1:5	D13
12	HI_D1:4	D12
11	HI_D1:3	D11
10	HI_D1:2	D10
9	HI_D1:1	D9
8	HI_D1:0	D8
7	HI_D0:7	D7
6	HI_D0:6	D6
5	HI_D0:5	D5
4	HI_D0:4	D4
3	HI_D0:3	D3
2	HI_D0:2	D2
1	HI_D0:1	D1
0	HI_D0:0	D0

Table 3–17 shows the probe section and channel assignments for the DEP group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–17: P6: DEP group channel assignments

Bit order	Section: channel	Pentium Pro signal name
7	HI_C1:4	DEP7#*
6	HI_C1:0	DEP6#*
5	HI_C0:4	DEP5#*
4	HI_C0:0	DEP4#*
3	LO_C1:6	DEP3#*
2	LO_C1:2	DEP2#*
1	LO_C0:6	DEP1#*
0	LO_C0:2	DEP0#*

*** Signal not required for disassembly.**

Table 3–18 shows the probe section and channel assignments for the Data_Ctl group and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically. The name of the symbol table is P6_DC.

Table 3–18: P6: Data_Ctl group channel assignments

Bit order	Section: channel	Pentium Pro signal name
2	LO_C0:5	DRDY#
1	HI_C3:6	DBSY#
0	LO_C2:6	TRDY#

Table 3–19 shows the probe section and channel assignments for the Async group and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically. The name of the symbol table is P6_ASY.

Table 3–19: P6: Async group channel assignments

Bit order	Section: channel	Pentium Pro signal name
5	HI_C3:2	BINIT#
4	HI_C2:6	INIT#
3	HI_C2:3	RESET#
2	HI_C3:7	FLUSH#
1	HI_C1:7	BERR#
0	HI_C0:2	TRCK_ER_D

Table 3–20 shows the probe section and channel assignments for the BR group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–20: P6: BR group channel assignments

Bit order	Section: channel	Pentium Pro signal name
4	HI_C2:7	BPRI#*
3	HI_C3:4	BR3#*
2	HI_C3:0	BR2#*
1	HI_C2:4	BR1#*
0	LO_C3:6	BR0#*

*** Signal not required for disassembly.**

Table 3–21 shows the probe section and channel assignments for the PAL group and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically. The name of the symbol table is P6_PAL.

Table 3–21: P6: PAL group channel assignments

Bit order	Section: channel	Pentium Pro signal name
7	LO_C2:5	ID1_D
6	LO_C3:1	ID0_D
5	HI_C0:1	RCNT2_D
4	HI_C0:6	RCNT1_D
3	HI_C1:1	RCNT0_D
2	LO_D0:2	SCNT2_D
1	LO_D0:1	SCNT1_D
0	LO_D0:0	SCNT0_D

Table 3–22 shows the probe section and channel assignments for the Misc group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–22: P6: Misc group channel assignments

Bit order	Section: channel	Pentium Pro signal name
7	HI_C1:2	ID1_LF
6	HI_C0:5	ID0_LF
5	LO_C3:7	Ab35*
4	LO_C3:3	Ab34*
3	LO_C2:7	Ab33*
2	LO_C2:3	Ab32*
1	LO_C1:1	PRDY#*
0	LO_C3:5	BTM_DF

*** Signal not required for disassembly.**

Table 3–23 shows the probe section and channel assignments for the clock channels (not part of any group) and the microprocessor signal to which each channel connects.

Table 3–23: P6: Clock channel assignments

Section: channel	Pentium Pro signal name
CK:3	BCLK=
CK:2	RS_DLL#
CK:1	DRDY_LLL#
CK:0	BTM_DF=

These channels are used only to clock in data; they are not acquired or displayed. To acquire data from any of the signals shown in Table 3–23, you must connect another channel probe to the signal, a technique called double probing. An equals sign (=) following a signal name indicates that it is already double probed.

P6_TMG Setup

Tables 3–24 through 3–42 show the channel assignments for the P6_TMG setup used for general purpose analysis with Custom, External, or Internal clocking.

Table 3–24 shows the probe section and channel assignments for the A group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–24: P6_TMG: A group channel assignments

Bit order	Section: channel	Pentium Pro signal name
3	LO_C1:7	A35
2	LO_C1:3	A34
1	LO_C0:7	A33
0	LO_C0:3	A32

Table 3–25 shows the probe section and channel assignments for the Address group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–25: P6_TMG: Address group channel assignments

Bit order	Section: channel	Pentium Pro signal name
31	LO_A3:7	A31
30	LO_A3:6	A30
29	LO_A3:5	A29
28	LO_A3:4	A28
27	LO_A3:3	A27
26	LO_A3:2	A26
25	LO_A3:1	A25
24	LO_A3:0	A24
23	LO_A2:7	A23
22	LO_A2:6	A22
21	LO_A2:5	A21
20	LO_A2:4	A20
19	LO_A2:3	A19
18	LO_A2:2	A18
17	LO_A2:1	A17
16	LO_A2:0	A16
15	LO_A1:7	A15
14	LO_A1:6	A14
13	LO_A1:5	A13
12	LO_A1:4	A12
11	LO_A1:3	A11
10	LO_A1:2	A10
9	LO_A1:1	A9
8	LO_A1:0	A8
7	LO_A0:7	A7
6	LO_A0:6	A6
5	LO_A0:5	A5
4	LO_A0:4	A4
3	LO_A0:3	A3
2	LO_A0:2	A2
1	LO_A0:1	A1
0	LO_A0:0	A0

Table 3–26 shows the probe section and channel assignments for the REQ group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in binary.

Table 3–26: P6_TMG: REQ group channel assignments

Bit order	Section: channel	Pentium Pro signal name
4	LO_C0:1	REQ4
3	LO_C1:4	REQ3
2	LO_C1:0	REQ2
1	LO_C0:4	REQ1
0	LO_C0:0	REQ0

Table 3–27 shows the probe section and channel assignments for the REQ_Ctl group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in binary.

Table 3–27: P6_TMG: REQ_Ctl group channel assignments

Bit order	Section: channel	Pentium Pro signal name
5	LO_C1:5	ADS#
4	LO_C3:2	BNR#
3	HI_C3:3	LOCK#
2	LO_C2:7	RP#
1	LO_C2:3	AP1#
0	LO_D0:4	AP0#

Table 3–28 shows the probe section and channel assignments for the Error group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in binary.

Table 3–28: P6_TMG: Error group channel assignments

Bit order	Section: channel	Pentium Pro signal name
6	HI_C2:1	AERR#
5	HI_C1:7	BERR#
4	HI_C3:2	BINIT#
3	LO_C3:3	FERR#
2	LO_C2:4	FRCERR
1	LO_C3:0	IERR#
0	LO_D2:7	IGNNE#

Table 3–29 shows the probe section and channel assignments for the Snoop group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–29: P6_TMG: Snoop group channel assignments

Bit order	Section: channel	Pentium Pro signal name
3	HI_C1:5	SNOOP_D
2	HI_C3:5	HIT#
1	HI_C3:1	HITM#
0	HI_C2:5	DEFER#

Table 3–30 shows the probe section and channel assignments for the Rsp group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in binary.

Table 3–30: P6_TMG: Rsp group channel assignments

Bit order	Section: channel	Pentium Pro signal name
3	LO_C3:4	RSP#
2	HI_C1:3	RS2#
1	HI_C0:7	RS1#
0	HI_C0:3	RS0#

Table 3–31 shows the probe section and channel assignments for the Data group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–31: P6_TMG: Data group channel assignments

Bit order	Section: channel	Pentium Pro signal name
31	HI_A3:7	D63
30	HI_A3:6	D62
29	HI_A3:5	D61
28	HI_A3:4	D60
27	HI_A3:3	D59
26	HI_A3:2	D58
25	HI_A3:1	D57
24	HI_A3:0	D56
23	HI_A2:7	D55
22	HI_A2:6	D54
21	HI_A2:5	D53
20	HI_A2:4	D52
19	HI_A2:3	D51
18	HI_A2:2	D50
17	HI_A2:1	D49
16	HI_A2:0	D48
15	HI_A1:7	D47
14	HI_A1:6	D46
13	HI_A1:5	D45
12	HI_A1:4	D44
11	HI_A1:3	D43
10	HI_A1:2	D42
9	HI_A1:1	D41
8	HI_A1:0	D40
7	HI_A0:7	D39
6	HI_A0:6	D38
5	HI_A0:5	D37
4	HI_A0:4	D36
3	HI_A0:3	D35
2	HI_A0:2	D34
1	HI_A0:1	D33
0	HI_A0:0	D32

Table 3–32 shows the probe section and channel assignments for the Data_Lo group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–32: P6_TMG: Data_Lo group channel assignments

Bit order	Section: channel	Pentium Pro signal name
31	HI_D3:7	D31
30	HI_D3:6	D30
29	HI_D3:5	D29
28	HI_D3:4	D28
27	HI_D3:3	D27
26	HI_D3:2	D26
25	HI_D3:1	D25
24	HI_D3:0	D24
23	HI_D2:7	D23
22	HI_D2:6	D22
21	HI_D2:5	D21
20	HI_D2:4	D20
19	HI_D2:3	D19
18	HI_D2:2	D18
17	HI_D2:1	D17
16	HI_D2:0	D16
15	HI_D1:7	D15
14	HI_D1:6	D14
13	HI_D1:5	D13
12	HI_D1:4	D12
11	HI_D1:3	D11
10	HI_D1:2	D10
9	HI_D1:1	D9
8	HI_D1:0	D8
7	HI_D0:7	D7
6	HI_D0:6	D6
5	HI_D0:5	D5
4	HI_D0:4	D4
3	HI_D0:3	D3
2	HI_D0:2	D2
1	HI_D0:1	D1
0	HI_D0:0	D0

Table 3–33 shows the probe section and channel assignments for the DEP group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–33: P6_TMG: DEP group channel assignments

Bit order	Section: channel	Pentium Pro signal name
7	HI_C1:4	DEP7#
6	HI_C1:0	DEP6#
5	HI_C0:4	DEP5#
4	HI_C0:0	DEP4#
3	LO_C1:6	DEP3#
2	LO_C1:2	DEP2#
1	LO_C0:6	DEP1#
0	LO_C0:2	DEP0#

Table 3–34 shows the probe section and channel assignments for the Data_Ctl group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in binary.

Table 3–34: P6_TMG: Data_Ctl group channel assignments

Bit order	Section: channel	Pentium Pro signal name
2	LO_C0:5	DRDY#
1	HI_C3:6	DBSY#
0	LO_C2:6	TRDY#

Table 3–35 shows the probe section and channel assignments for the Async group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–35: P6_TMG: Async group channel assignments

Bit order	Section: channel	Pentium Pro signal name
6	HI_C2:3	RESET#
5	HI_C2:6	INIT#
4	LO_C3:7	STPCLK#
3	HI_C3:7	FLUSH#

Table 3–35: P6_TMG: Async group channel assignments

Bit order	Section: channel	Pentium Pro signal name
2	HI_C0:2	TRCK_ER_D
1	LO_D1:4	RCNTE_D
0	LO_D2:0	SCNTE_D

Table 3–36 shows the probe section and channel assignments for the Monitor group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–36: P6_TMG: Monitor group channel assignments

Bit order	Section: channel	Pentium Pro signal name
10	LO_D1:3	BP3#
9	LO_D1:2	BP2#
8	LO_D1:1	BPM1#
7	LO_D1:0	BPM0#
6	LO_C1:1	PRDY#
5	LO_D3:4	PREQ#
4	LO_D2:4	TDI
3	LO_D2:3	TDO
2	LO_D2:2	TMS
1	LO_D2:5	TCK
0	LO_D2:1	TRST#

Table 3–37 shows the probe section and channel assignments for the BR group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–37: P6_TMG: BR group channel assignments

Bit order	Section: channel	Pentium Pro signal name
4	HI_C2:7	BPRI#
3	HI_C3:4	BR3#
2	HI_C3:0	BR2#
1	HI_C2:4	BR1#
0	LO_C3:6	BR0#

Table 3–38 shows the probe section and channel assignments for the REQ_SNP group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–38: P6_TMG: REQ_SNP group channel assignments

Bit order	Section: channel	Pentium Pro signal name
5	HI_C0:1	RCNT2_D
4	HI_C0:6	RCNT1_D
3	HI_C1:1	RCNT0_D
2	LO_D0:2	SCNT2_D
1	LO_D0:1	SCNT1_D
0	LO_D0:0	SCNT0_D

Table 3–39 shows the probe section and channel assignments for the AGNT_ID group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–39: P6_TMG: AGNT_ID group channel assignments

Bit order	Section: channel	Pentium Pro signal name
1	LO_C2:5	ID1_D
0	LO_C3:1	IDO_D

Table 3–40 shows the probe section and channel assignments for the APIC group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–40: P6_TMG: APIC group channel assignments

Bit order	Section: channel	Pentium Pro signal name
2	LO_D3:2	PICD1
1	LO_D3:1	PICD0
0	LO_D3:0	PICCLK

Table 3–41 shows the probe section and channel assignments for the Misc group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–41: P6_TMG: Misc group channel assignments

Bit order	Section: channel	Pentium Pro signal name
20	LO_D3:5	BCLK
19	HI_C2:2	WAIT_DLL
18	LO_C2:2	WAIT_DLL=
17	HI_C2:0	PHASE_D
16	LO_C2:0	PHASE_D=
15	HI_C1:2	ID1_LF
14	HI_C0:5	ID0_LF
13	LO_C2:1	REQb4#
12	LO_C3:5	BTM_DF
11	HI_C1:6	ADS_L
10	LO_D3:7	AER_OBS#
9	LO_D3:6	BNT_OBS#
8	LO_D0:7	LINT1
7	LO_D0:6	LINT0
6	LO_D1:7	TSENSE2#
5	LO_D1:6	THRMTRP#
4	LO_D3:3	SMI#
3	LO_D1:5	PWRTHTL#
2	LO_D2:6	A20M#
1	LO_D0:3	A3#=
0	LO_D0:5	LEBA

Table 3–42 shows the probe section and channel assignments for the clock channels (not part of any group), and the microprocessor signal to which each channel connects.

Table 3–42: P6_TMG: Clock channel assignments

Section: channel	Pentium Pro signal name
CK:3	BCLK=
CK:2	RS_DLL#

Table 3–42: P6_TMG: Clock channel assignments

Section: channel	Pentium Pro signal name
CK:1	DRDY_LLL#
CK:0	BTM_DF=

These channels are used only to clock in data; they are not acquired or displayed. To acquire data from any of the signals shown in Table 3–42, you must connect another channel probe to the signal, a technique called double probing. An equals sign (=) following a signal name indicates that it is already double probed.

How Data is Acquired

This part of this chapter explains how the module acquires Pentium Pro signals using the TMS 110 software and probe adapter. This part also provides additional information on microprocessor signals accessible on or not accessible on the probe adapter, and on extra acquisition channels available for you to use for additional connections.

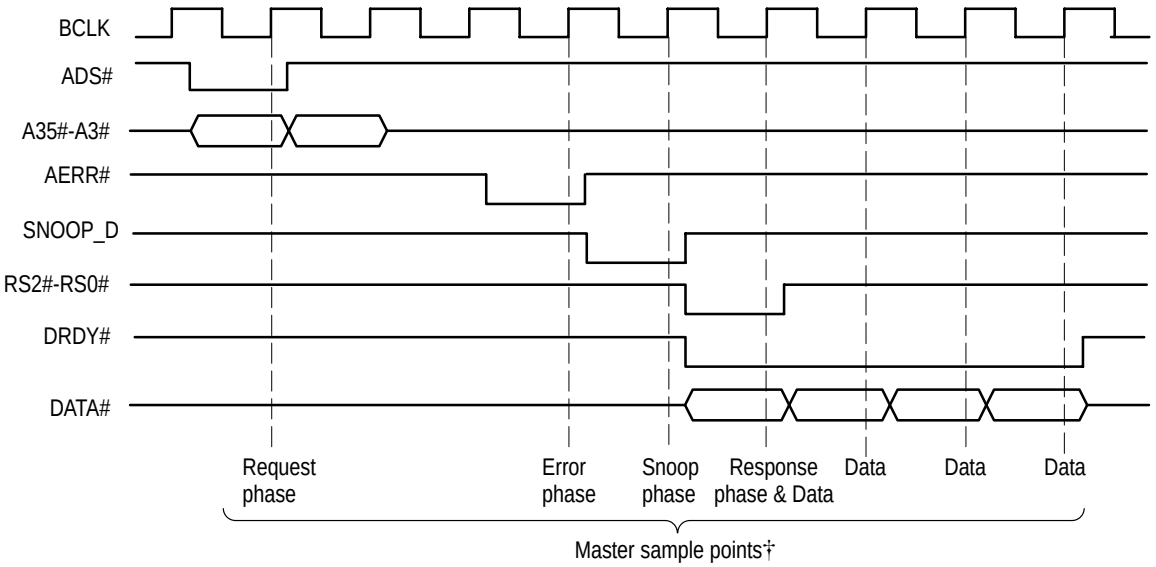
Custom Clocking

A special clocking program is loaded to the module every time you load the P6 support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple groups of channels at different times as they become valid on the Pentium Pro bus. The module then sends all the logged-in signals to the trigger machine and to the acquisition memory of the module for storage.

In Custom clocking, the module clocking state machine (CSM) generates one master sample for each Pentium Pro bus active phase.

Figure 3–4 shows the master sample points.



†Channels not set up in a channel group by the TMS 110 software are logged with the Master samples.

Figure 3–4: Pentium Pro bus timing for the P6 setup

Clocking Options

The clocking algorithm for the Pentium Pro microprocessor support has different variations for the P6 setup and the P6_TMG setup.

P6 Setup. The clocking algorithm has three variations: Active Phases Only, Clock-by-Clock w/ Demux, and Branch Trace Data Only.

Active Phases Only. Request, Snoop, Response, and Data phases are always logged. The clocking software logs a sample whenever the ADS#, AERR#, RS2#-RS0#, RESET#, BINIT#, INIT# or DRDY# signals are asserted, or when there is an active Snoop phase.

The clocking software stores a sample when it detects an active Request cycle. The sample contains request type, cycle type (read or write), and snoop count information, as well as an indication of how many Data cycles to expect during the transaction. The disassembly software calculates which response sample was associated with the Request cycle, and then determines which data samples to link to the Request, Response, and Snoop phase samples.

During the Request phase, the modules use demultiplexers to store REQa and REQb data in one sample. This means that although the A31-A24 and ATTR7-ATTR0 signals appear on the same Pentium Pro pins just one clock apart, the signals are actually acquired by different module sections and channels.

Clock-By-Clock w/Demux. The clocking software stores every cycle on every rising edge of the BCLK signal, but still demultiplexes the channels like the Active Phases Only.

Branch Trace Data Only. The clocking software logs the Data phase and Agent ID of the initiating microprocessor or device when a Branch Trace Message (BTM) is detected on the bus. Only BTMs are acquired.

P6_TMG Setup. The clocking software stores every cycle on every rising edge of the BCLK signal, but does not demultiplex them.

Alternate Microprocessor Connections

You can connect to microprocessor signals that are not required by the support so that you can do more advanced timing analysis. These signals might or might not be accessible on the probe adapter board.

For a list of signals required or not required for disassembly, refer to the channel assignment tables beginning on page 3–6. Remember that these channels are already included in a channel group. If you do connect these channels to other signals, you should set up another channel group for them.

Signals Not On the Probe Adapter

The CLKBYPASS#, GTLREFx, EMIx, and CUCTLPINx Pentium Pro signals are not accessible on the probe adapter.

Extra Channels

All probes are connected to the probe adapter. You can disconnect channel probes not required by the support to make alternate connections. The channel assignment tables in this chapter indicate channels not required for disassembly.

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Maintenance

Maintenance

This section contains information on the following topics:

- Probe adapter circuit description
- How to replace a fuse

Probe Adapter Circuit Description

An EPLD device on the probe adapter follows the bus activity from reset, and keeps track of the request count (RCNT2-RCNT0), the Agent ID (ID1, ID0), and the snoop count (SCNT2-SCNT0). The disassembler uses these counts, with the P6 support setup and Custom clocking, to disassemble data when there is an active Request phase on the sample.

The EPLD checks protocols on every rising edge of the BCLK signal for the ADS# signal to be asserted, the overflow or underflow of the request count, and the overflow or underflow of the snoop count. When a problem is detected, it is reported on the TRCK_ER_D, RCNTE_D, and SCNTE_D signals, respectively.

Snoop tracking logic in the EPLD asserts the SNOOP_D signal at the end of every Snoop phase. If the Snoop phase does not stall (extensions), SNOOP_D is asserted four clocks after the ADS# signal is asserted. If the Snoop phase does stall, SNOOP_D is asserted with the assertion of the HIT#, HITM#, and DEFER# signals for that transaction. In any case, SNOOP_D will only be asserted once each time ADS# is asserted regardless of the number of Snoop phase stalls.

The EPLD device stores Reset configuration information to determine if the AERR# and BINIT# signals are observed or ignored. The EPLD uses this information to keep correct request count and snoop count values. The AERR# and BINIT# signals are always acquired when they are asserted and the Active Phases Only clocking option is selected regardless of the Reset configuration and count values.

The EPLD device also combines the RS2#-RS0#, ADS#, SNOOP_D, DRDY#, RESET#, INIT#, BINIT# (when observed), and AERR# (when observed) into one derived signal for Custom clocking. The module samples all channels when PHASE_D is asserted and the Active Phases Only clocking option is selected.

When the Branch Trace Data Only clocking option is selected, the module only acquires the Data phase and Agent ID of the initiating microprocessor when a BTM (Branch Trace Message) is driven to the bus. The DRDY_LLL#, RS_DLL#, BTM_DF, and WAIT_DLL qualifiers for the clocking state machine (CSM) indicate when this occurs. These qualifiers are ignored for all other clocking options.

The DRDY_LLL# signal indicates when the D63-D0 bits are valid to latch which could occur before, during, or after the response to the BTM. The RS_DLL# signal indicates when a response has occurred on the Pentium Pro bus. The BTM_DF signal indicates if the response is associated with a BTM transaction; the CSM only checks this signal when RS_DLL# is asserted.

The WAIT_DLL signal indicates when the CSM can master strobe a sample of BTM data. This occurs when the CSM detects a response associated with the BTM transaction. The CSM also determines when to wait to acquire BTM data if it determines the response occurs after the data. The CSM only checks this signal when RS_DLL# and BTM_DF are asserted.

When the acquisition module acquires BTM data, the ID1_LF and ID0_LF bits indicate which Pentium Pro microprocessor drove the BTM on that sample. If the system has multiple Pentium Pro microprocessors, you can use these bits to qualify data out of the acquisition from other microprocessors.

An acquisition which uses the Branch Trace Data Only clocking option consists of one phase of one type of transaction, the Data phase of a BTM transaction. Since the Data and Data_Lo channel groups contain the source and destination addresses of the execution code in the order it occurred, you can scroll through the values displayed in those groups to follow the execution of the associated code.

Replacing Signal Leads

Information on basic operations describes how to replace signal leads (individual channel and clock probes).

Replacing the Fuse

If the fuse on the Pentium Pro probe adapter opens (burns out), you can replace it with a 3 A, 125 V fuse. Figure 4–1 shows the location of the fuse on the probe adapter.

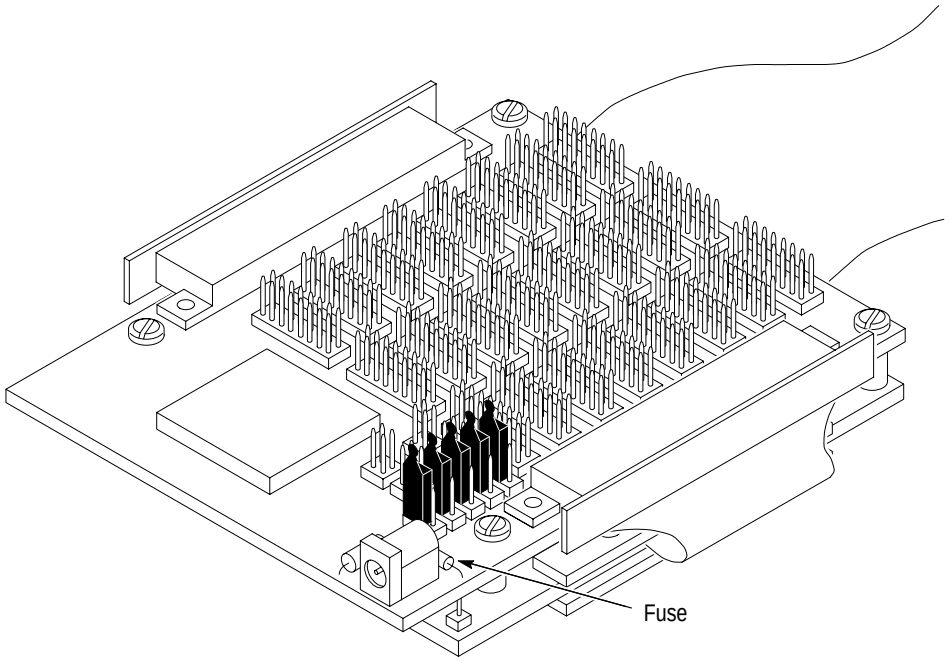


Figure 4–1: Location of the fuse

Replaceable Electrical Parts

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 110 Pentium Pro microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

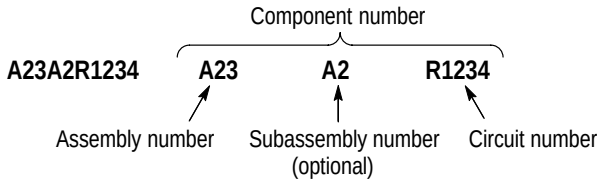
Parts list column descriptions

Column	Column name	Description
1	Component number	The component number appears on diagrams and circuit board illustrations, located in the diagrams section. Assembly numbers are clearly marked on each diagram and circuit board illustration in the *Diagrams* section, and on the mechanical exploded views in the *Replaceable Mechanical Parts* list section. The component number is obtained by adding the assembly number prefix to the circuit number (see Component Number illustration following this table). The electrical parts list is arranged by assemblies in numerical sequence (A1, with its subassemblies and parts, precedes A2, with its subassemblies and parts). Chassis-mounted parts have no assembly number prefix, and they are located at the end of the electrical parts list.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
6	Mfr. code	This indicates the code number of the actual manufacturer of the part.
7	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Component Number



Read: Resistor 1234 (of Subassembly 2) of Assembly 23

List of Assemblies

A list of assemblies is located at the beginning of the electrical parts list. The assemblies are listed in numerical order. When a part's complete component number is known, this list will identify the assembly in which the part is located.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
00779	AMP INC.	CUSTOMER SERVICE DEPT PO BOX 3608	HARRISBURG, PA 17105–3608
05791	LYN–TRON INC	SOUTH 6001 THOMAS MALLEN RD	SPOKANE, WA 99204
0LXM2	LZR ELECTRONICS INC	8051 CESSNA AVENUE	GAITHERSBURG, MD 20879
26742	METHODE ELECTRONICS INC	BACKPLAIN DIVISION 7444 WEST WILSON AVE	CHICAGO, IL 60656–4548
61857	SAN–O INDUSTRIAL CORP	91–3 COLIN DRIVE	HOLBROOK, NY 11741
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077–0001
TK0588	UNIVERSAL PRECISION PRODUCT	1775 NW CORNELIUS PASS RD	HILLSBORO, OR 97124
TK1158	POWEL & ASSOCIATES,INC	111 SOUTH FINDLAY STREET	SEATTLE, WA 98108

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A01	010–0596–00			PROBE ADAPTER:PENTIUMPRO,PGA–387 SOCKETED,PROBE ADAPTER,TMS 110	80009	010–0596–00
A01	129–1485–00			SPACER:SPACER MALE/FEMALE,0.500 LG X 0.250 DIA, NYLON	05791	NY 6881–6–3
A01	211–0558–00			SCREW,MACHINE:6–32 X 0.25,BDGH,NYL SLOT	TK1158	211–0558–00
A01	385–0013–00			SPACER,POST:0.75 L W/6–32 THD THRU,NYL 0.312 OD	TK0588	385–0013–00
A01	671–3789–00			CKT BD ASSY:"P6" PGA–387,SOCKETED, 389–2196–00 WIRED,TMS 110	80009	671–3789–00
A01F1000	159–0220–00			FUSE,WIRE LEAD:3A,125V,FAST	61857	SP5–3A
A01J1000	131–5527–00			JACK,POWER DC:PCB,MALE,RTANG,2MM PIN,11MM H(0.433) X 3.5MM(0.137) TAIL,9MM(0.354) W,TIN,W/SWI	0LXM2	DJ005A
A01J1200	131–4530–00			CONN,HDR:PCB,MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLDBD RETENTION	00779	104344–1
A01J1201	131–4530–00			CONN,HDR:PCB,MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLDBD RETENTION	00779	104344–1
A01J1205	131–4530–00			CONN,HDR:PCB,MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLDBD RETENTION	00779	104344–1
A01J1206	131–4530–00			CONN,HDR:PCB,MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLDBD RETENTION	00779	104344–1
A01J1207	131–4530–00			CONN,HDR:PCB,MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLDBD RETENTION	00779	104344–1
A01J1210	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1211	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1212	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1213	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1310	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1315	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1330	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1335	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1340	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1345	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1410	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1415	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4

Replaceable electrical parts list (cont.)

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A01J1430	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1435	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1440	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1445	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1510	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1515	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1530	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1535	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1540	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1545	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1610	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1615	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1630	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1635	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1640	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01J1645	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD	00779	104326–4
A01P1200	131–4356–00			CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER,	26742	9618–302–50
A01P1201	131–4356–00			CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER,	26742	9618–302–50
A01P1205	131–4356–00			CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER,	26742	9618–302–50
A01P1206	131–4356–00			CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER,	26742	9618–302–50
A01P1207	131–4356–00			CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER,	26742	9618–302–50

Replaceable Mechanical Parts

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 110 Pentium Pro microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
00779	AMP INC.	CUSTOMER SERVICE DEPT PO BOX 3608	HARRISBURG, PA 17105–3608
05791	LYN–TRON INC	SOUTH 6001 THOMAS MALLEN RD	SPOKANE, WA 99204
0LXM2	LZR ELECTRONICS INC	8051 CESSNA AVENUE	GAITHERSBURG, MD 20879
26742	METHODE ELECTRONICS INC	BACKPLAIN DIVISION 7444 WEST WILSON AVE	CHICAGO, IL 60656–4548
61857	SAN–O INDUSTRIAL CORP	91–3 COLIN DRIVE	HOLBROOK, NY 11741
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077–0001
TK0588	UNIVERSAL PRECISION PRODUCT	1775 NW CORNELIUS PASS RD	HILLSBORO, OR 97124
TK1158	POWEL & ASSOCIATES,INC	111 SOUTH FINDLAY STREET	SEATTLE, WA 98108

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
1–0	010–0596–00			1	PROBE ADAPTER:PENTIUMPRO,PGA–387 SOCKETED,PROBE ADAPTER,TMS 110	80009	010–0596–00
–1	671–3789–00			1	CIR BD ASSY:PENTIUMPRO PGA–387,SOCKETED, 389–2196–00 WIRED,TMS 110	80009	671–3789–00
–2	131–5527–00			1	JACK,POWER DC:PCB,MALE,RTANG,2MM PIN,11MM H(0.433) X 3.5MM(0.137) TAIL,9MM(0.354) W,TIN,W/SWI	0LXM2	DJ005A
–3	159–0220–00			1	FUSE,WIRE LEAD:3A,125V,FAST	61857	SP5–3A
–4	131–4530–00			5	CONN,HDR:PCB,MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION,	00779	104344–1
–5	131–4356–00			5	CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER,	26742	9618–302–50
–6	131–5267–00			5	CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD,	00779	104326–4
–7	211–0558–00			4	SCREW,MACHINE:6–32 X 0.25,BDGH,NYL SLOT	TK1158	211–0558–00
–8	385–0013–00			4	SPACER,POST:0.75 L W/6–32 THD THRU,NYL 0.312 OD	TK0588	385–0013–00
–9	361–1713–00			1	SPACER;PGA; BOTTOM TARGET END, PLASTIC	80009	361–1713–00
–10	136–1308–00			1	SOCKET;PGA; PCB; FEMALE, STR, 387 POS, GOLD/GOLD, LONG TAILS	80009	136–1308–00
–11	358–0814–00			1	STRAIN RELIEF; BOTTOM, TARGET END, PLASTIC	80009	358–0814–00
–12	129–1485–00			4	SPACER:SPACER MALE/FEMALE,0.500 LG X 0.250 DIA, NYLON	05791	NY 6881–6–3
–13				1	ORDER 010–0596–00	80009	010–0596–00
					STANDARD ACCESSORIES		
	070–9812–00			1	MANUAL,TECH:INSTRUCTION,PENTIUMPRO,DISSASEMBLER,TMS 110	80009	070–9812–00
	070–9803–00			1	MANUAL, TECH:TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070–9803–00
	061–4111–00			1	MANUAL, TECH:PROBE HANDLING; READ THIS FIRST	80009	061–4111–00
	061–4088–00			1	MANUAL,TECH:READ THIS FIRST; PENTIUMPRO PROBE HANDLING		061–4088–00
	119–5061–01			1	POWER SUPPLY:25W,5V 5A,CONCENTRIC 2MM,90–265V,47–63HZ (NOT SHOWN)	14310	SW106KA002F01
	161–0104–00			1	CA ASSY,PWR:3,18 AWG,98 L,250V/10AMP,98 INCH, RTANG,IEC320,RCPT X STR,NEMA 15–5P,W/CORD GRIP	S3109	ORDER BY DESCRIPTION

Replaceable mechanical parts list (cont.)

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					OPTIONAL ACCESSORIES		
	070–9802–00			1	MANUAL, TECH:BASIC OPS MICRO SUP ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070–9802–00
	161–0104–06			1	CA ASSY,PWR:3,1.0MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, EUROPEAN,SAFETY CONTROLLED (OPT A1)	S3109	ORDER BY DESCRIPTION
	161–0104–07			1	CA ASSY,PWR:3,1.0MM SQ,240V/10AMP,2.5 METER, RTANG,IEC320,RCPT X 13A, FUSED, UK PLUG, (13A FUSE), UNITED KINGDOM,SAFETY CONTROL (OPT A2)	S3109	ORDER BY DESCRIPTION
	161–0104–05			1	CA ASSY,PWR:3,1.0MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, AUSTRALIA,SAFETY CONTROLLED (OPT A3)	S3109	ORDER BY DESCRIPTION
	161–0167–00			1	CA ASSY,PWR:3,0.75MM SQ,250V/10AMP,2.5 METER, RTANG,IEC320,RCPT, SWISS,NO CORD GRIP, SAFETY CONTROLLED (OPT A5)	S3109	ORDER BY DESCRIPTION

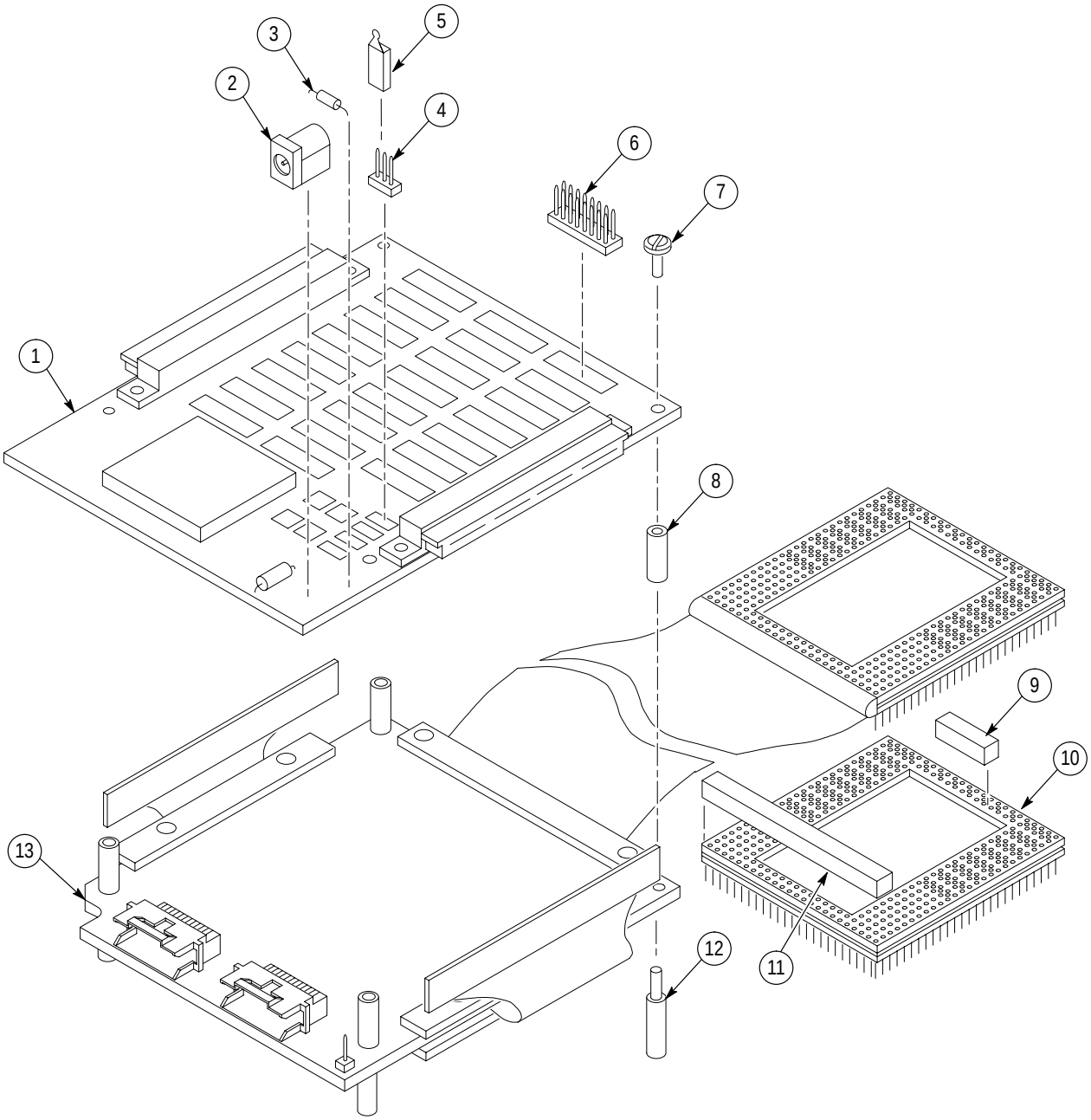


Figure 1: Pentium Pro probe adapter exploded view

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