Instruction Manual

Tektronix

TMS 204
68040, 68EC040 & 68LC040 Microprocessor Support

070-9822-00

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

Printed in the U.S.A.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface: Microprocessor Support Documentation

This instruction manual contains specific information about the TMS 204 68040 microprocessor support and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor supports on the logic analyzer for which the TMS 204 68040 support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor supports, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor supports is included with each product. Each logic analyzer has basic information that describes how to perform tasks common to supports on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing disassembled data
- The TMS 204 68040 probe adapter

Manual Conventions

This manual uses the following conventions:

- The phrase “information on basic operations” refers to online help, an installation manual, or a basic operations of microprocessor supports user manual.
- In the information on basic operations, the term XXX or P54C used in field selections and file names can be replaced with 68040A. This is the name of the microprocessor in field selections and file names you must use to operate the 68040 support.
- The term System Under Test (SUT) refers to the microprocessor-based system from which data will be acquired.
- The term logic analyzer refers to the Tektronix logic analyzer for which this product was purchased.

- The term module refers to a 102/136-channel or a 96-channel module.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The user manual provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or, contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Contact your local Tektronix distributor or sales office. Or, visit our web site for a listing of worldwide service locations. http://www.tek.com
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000

Getting Started

Getting Started

This chapter provides information on the following topics:

- The TMS 204 68040 microprocessor support
- Logic analyzer software compatibility
- Your 68040 system requirements
- 68040 support restrictions
- How to configure the probe adapter
- How to connect to the System Under Test (SUT)

Support Description

The TMS 204 microprocessor support disassembles data from systems that are based on the Motorola 68040 microprocessor. The support runs on a compatible Tektronix logic analyzer equipped with a 102/136-channel module, or a 96-channel module.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 204 microprocessor support.

Table 1–1 shows the microprocessors and packages from which the TMS 204 support can acquire and disassemble data.

Table 1–1: Supported microprocessors

Name	Package
68040	PGA
68EC040	PGA
68LC040	PGA

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Mechanical Parts* chapter.

To use this support efficiently, you need to have the items listed in the information on basic operations as well as the 68040 Microprocessor User's Manual, Motorola, 1989.

Information on basic operations also contains a general description of supports.

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

To use the 68040 support, the Tektronix logic analyzer must be equipped with at least a 102/136-channel module or a 96-channel module. The module must be equipped with enough probes to acquire channel and clock data from signals in your 68040-based system.

Refer to information on basic operations to determine how many modules and probes the logic analyzer needs to meet the channel requirements.

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor supports in the information on basic operations as they pertain to your SUT.

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other 68040 support requirements and restrictions.

System Clock Rate. The TMS 204 support product supports the 68040 microprocessor at speeds of up to 33 MHz[1].

Hardware Reset. If a hardware reset occurs in your 68040 system during an acquisition, the disassembler might acquire an invalid sample.

Cache Invalidation. Correct disassembly is not guaranteed for microprocessor systems that run cache invalidations concurrent with burst cycles.

Dynamic Bus Sizing. When the Bus Size Control signals (BS16# or BS8#) are asserted, the 68040 microprocessor allows the bus width to be changed for extra cycles (when more than one cycle is required for a transaction). The disassembler does not support changing the bus size for extra cycles. To keep the disassembler synchronized, Use Mark Opcode as described in the *Operating Basics* chapter.

1 **Specification at time of printing. Contact your logic analyzer sales representative for current information on the fastest devices supported.**

Data Reads and Writes. The dissassembler will not link data reads and writes with the instruction which causes them.

Locked Bus Cycles. The dissasembler will not identify locked bus cycles.

Configuring the Probe Adapter

Disabling the cache makes all instruction prefetches visible on the bus so they can be acquired and disassembled. The probe adapter contains a jumper you can use to disable the 68040 cache.

With the cache jumper in the NORM position, the SUT controls the cache and the CDIS~ signal is not affected.

With the cache jumper in the DIS position, the CDIS~ signal connects to a 332 Ω pull-down resistor on the probe adapter which disables the cache. You should also cut or remove pin T5 from the protective socket on the underside of the probe adapter to prevent contention with the driving signal.

Figure 1–1 shows the location of J990 on the probe adapter.

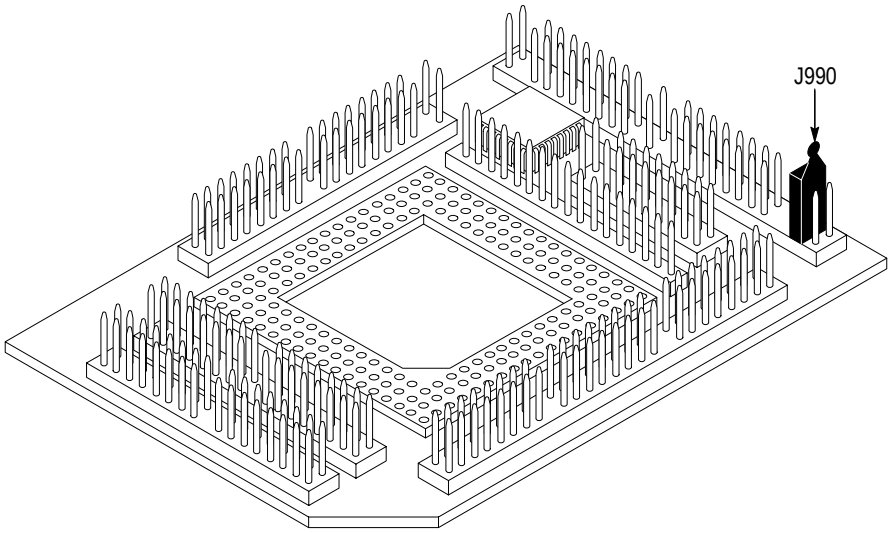


Figure 1–1: Jumper location on the probe adapter

Connecting to a System Under Test

Before you connect to the SUT, you must connect the probes to the module. Your SUT must also have a minimum amount of clear space surrounding the micro-

processor to accommodate the probe adapter. Refer to the *Specifications* chapter in this manual for the required clearances.

The channel and clock probes shown in this chapter are for a 102/136-channel module. Your probes will look different if you are using a 96-channel module.

The general requirements and restrictions of microprocessor supports in the information on basic operations shows the vertical dimensions of a channel or clock probe connected to square pins on a circuit board.

PGA Probe Adapter

To connect the logic analyzer to a SUT using a PGA probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probe adapter, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.
3. Place the probe adapter onto the antistatic shipping foam to support the probe as shown in Figure 1–2. This prevents the circuit board from flexing and the socket pins from bending.
4. Remove the microprocessor from your SUT.
5. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on the microprocessor.

CAUTION. *Failure to correctly place the microprocessor into the probe adapter might permanently damage the microprocessor once power is applied.*

6. Place the microprocessor into the probe adapter as shown in Figure 1–2.

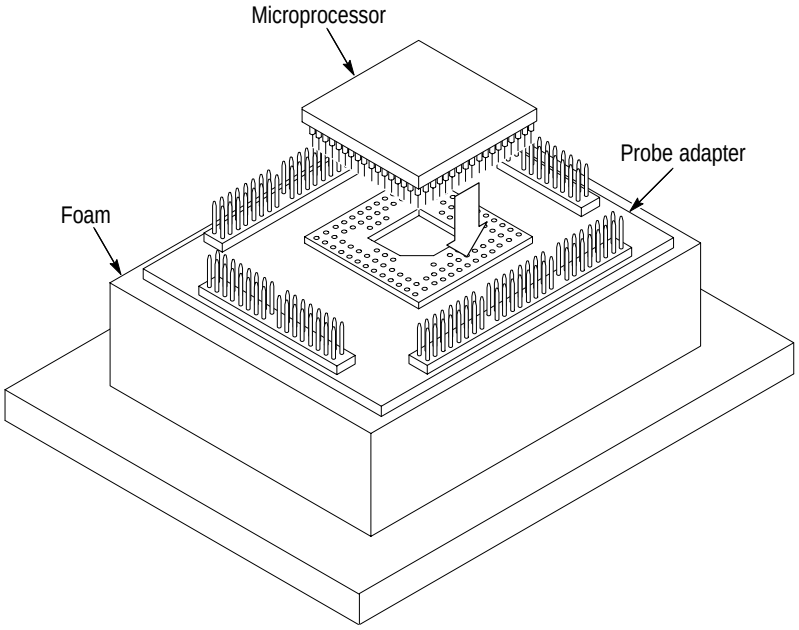


Figure 1–2: Placing a microprocessor into a PGA probe adapter

7. Connect the channel and clock probes to the probe adapter as shown in Figure 1–3. Match the channel groups and numbers on the probe labels to the corresponding pins on the probe adapter. Match the ground pins on the probes to the corresponding pins on the probe adapter.

8. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on your SUT.

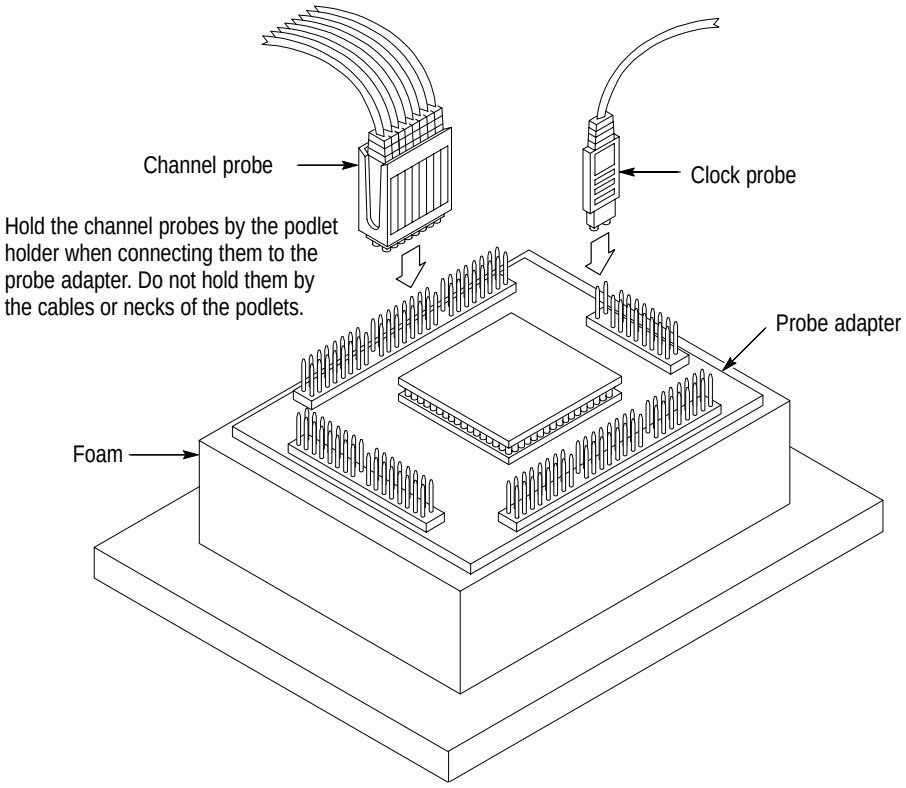


Figure 1–3: Connecting probes to a PGA probe adapter

9. Place the probe adapter onto the SUT as shown in Figure 1–4.

NOTE*. You might need to stack one or more replacement sockets between the SUT and the probe adapter to provide sufficient vertical clearance from adjacent components. However, keep in mind that this might increase loading, which can reduce the electrical performance of your probe adapter.*

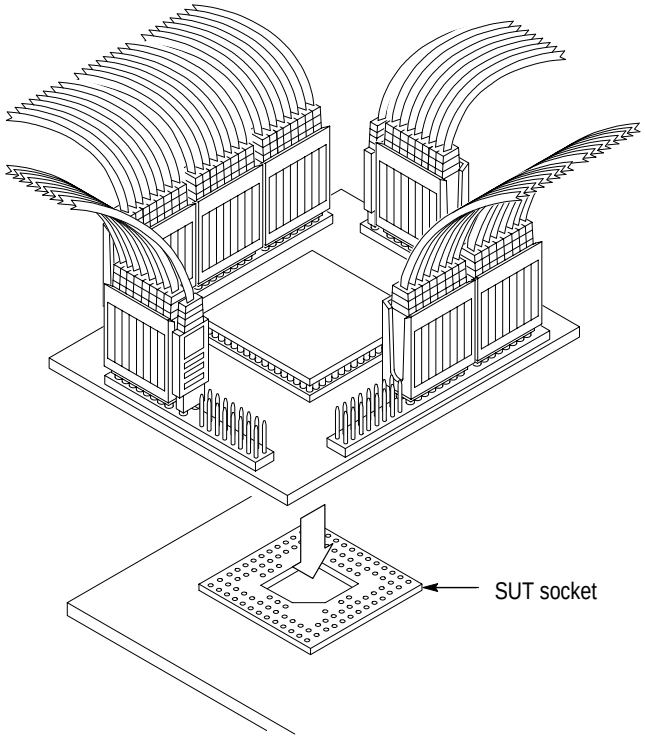


Figure 1–4: Placing a PGA probe adapter onto the SUT

Without a Probe Adapter

You can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your SUT.

To connect the probes to 68040 signals in the SUT using a test clip, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from it.

CAUTION. *Failure to place the SUT on a horizontal surface before connecting the test clip might permanently damage the pins on the microprocessor.*

3. Place the SUT on a horizontal static-free surface.
4. Use Table 1–2 to connect the channel probes to 68040 signal pins on the test clip or in the SUT.

   Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip.
5. Align pin 1 or A1 of your test clip with the corresponding pin 1 or A1 of the 68040 microprocessor in your SUT and attach the clip to the microprocessor.

Table 1–2: 68040 signal connections for channel probes

Section:channel	68040 signal	Section:channel	68040 signal
A3:7	A31	D3:7	D31
A3:6	A30	D3:6	D30
A3:5	A29	D3:5	D29
A3:4	A28	D3:4	D28
A3:3	A27	D3:3	D27
A3:2	A26	D3:2	D26
A3:1	A25	D3:1	D25
A3:0	A24	D3:0	D24
A2:7	A23	D2:7	D23
A2:6	A22	D2:6	D22
A2:5	A21	D2:5	D21
A2:4	A20	D2:4	D20
A2:3	A19	D2:3	D19
A2:2	A18	D2:2	D18
A2:1	A17	D2:1	D17
A2:0	A16	D2:0	D16
A1:7	A15	D1:7	D15
A1:6	A14	D1:6	D14
A1:5	A13	D1:5	D13
A1:4	A12	D1:4	D12
A1:3	A11	D1:3	D11
A1:2	A10	D1:2	D10

Table 1–2: 68040 signal connections for channel probes (cont.)

Section:channel	68040 signal	Section:channel	68040 signal
A1:1	A9	D1:1	D9
A1:0	A8	D1:0	D8
A0:7	A7	D0:7	D7
A0:6	A6	D0:6	D6
A0:5	A5	D0:5	D5
A0:4	A4	D0:4	D4
A0:3	A3	D0:3	D3
A0:2	A2	D0:2	D2
A0:1	A1	D0:1	D1
A0:0	A0	D0:0	D0
C3:7	BG_L~	C2:7	BCLK_B*
C3:6	TT1	C2:6	R/W~
C3:5	MI~	C2:5	LOCK~
C3:4	TM2	C2:4	TM0
C3:3	SIZ0	C2:3	TM1
C3:2	TT0	C2:2	TEA~
C3:1	TCI~	C2:1	TA~
C3:0	SIZ1	C2:0	TS~
C1:7	TLN1	C0:7	TIP~*
C1:6	IPL2~	C0:6	IPL0~
C1:5	AVEC~	C0:5	RSTI~*
C1:4	SC1	C0:4	UPA1*
C1:3	TLN0	C0:3	MDIS~*
C1:2	IPL1~	C0:2	IPEND~
C1:1	TB1~*	C0:1	CDIS~
C1:0	SC0	C0:0	UPA0*

*** Signal not required for disassembly.**

Table 1–3 shows the clock probes, and the 68040 signal to which they must connect for disassembly to be correct.

Table 1–3: 68040 signal connections for clock probes

Section:channel	68040 signal
CK:3	BCLK
CK:2	not connected
CK:1	BG~
CK:0	TIP~

Operating Basics

Setting Up the Support

This section provides information on how to set up the support. Information covers the following topics:

- Channel group definitions
- Clocking options
- Symbol table files

Remember that the information in this section is specific to the operations and functions of the TMS 204 68040 support on any Tektronix logic analyzer for which it can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and disassemble data, you need to load the support and specify setups for clocking, and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The disassembler automatically defines channel groups for the support product. The channel groups for the 68040 support are Address, Data, Control, Intr, Cache, and Misc.

Clocking Options

The TMS 204 support offers a microprocessor-specific clocking mode for the 68040 microprocessor. This clocking mode is the default selection whenever you load the 68040A support.

A description of how cycles are sampled by the module using the support and probe adapter is found in the *Specifications* chapter.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

The clocking options for the TMS 204 support are: 68040 Address / Data Bus Mode, and Alternate Bus Master Cycles.

68040 Address / Data Bus Mode

The 68040 has a multiplexed bus mode that supports the generation of a multiplexed address/data bus. When used in this mode, the address and data bus can be hard-wired together to form a single 32-bit address/data bus at the microprocessor (CPU) with address and data information time-multiplexed on the bus.

You select the 68040 address/data bus mode by selecting Multiplexed in the field. The default selection is Non-Multiplexed.

***NOTE**. If you select the Multiplexed mode, you should remove the channels connected to the data signals to reduce loading.*

Alternate Bus Master Cycles

An alternate bus master cycle is defined as the 68040 giving up the bus to an alternate device (a DMA device or another microprocessor). These types of cycles are acquired when you select Included.

Symbols

The TMS 204 support supplies one symbol table file. The 68040A_Ctrl file replaces specific Control channel group values with symbolic values when Symbolic is the radix for the channel group.

Table 2–1 shows the name, bit pattern, and meaning for the symbols in the file 68040A_Ctrl, the Control channel group symbol table.

Table 2–1: Control group symbol table definitions

	Control group value				
	BG~ TT1 TT0	TM2 TM1 TM0	LOCK~ TS~ TA~ R/W~	MI~ TEA~ SIZ1 SIZ0	
Symbol					Meaning
LPSTOP_ACK	0 1 1	0 0 0	1 X 0 0	1 1 1 0	LPSTOP Acknowledge cycle
LPSTOP_ERROR	0 1 1	0 0 0	1 X 1 0	1 0 1 0	LPSTOP Error – 68040 mode
BKPT_ACK	0 1 1	0 0 0	1 X 0 1	1 1 0 1	Breakpoint acknowledge cycle
BKPT_ERROR	0 1 1	0 0 0	1 X X 1	X 0 0 1	Breakpoint error
INT_ACK	0 1 1	X X X	1 X 0 1	1 1 0 1	Interrupt acknowledge cycle
SPUR_INTR	0 1 1	X X X	1 X 1 1	1 0 0 1	Spurious interrupt
BUS_ERROR	0 X X	X X X	X X 1 X	1 0 X X	Bus error
BUS_RETRY	0 X X	X X X	X X 0 X	1 0 X X	Bus error and retry
PREFETCH?	0 0 0	X 1 0	1 X X 1	X X X X	Probable instruction or extension

Table 2–1: Control group symbol table definitions (cont.)

Symbol	Control group value BG~ TT1 TT0	TM2 TM1 TM0	LOCK~ TS~ TA~ R/W~	MI~ TEA~ SIZ1 SIZ0	Meaning
MMU_DATA_RD	0 0 0	0 1 1	X X X 1	X X X X	MMU table search data read cycle
MMU_DATA_WR	0 0 0	0 1 1	X X X 0	X X X X	MMU table search data write cycle
MMU_DATA	0 0 0	0 1 1	X X X X	X X X X	Any MMU table search data access
MMU_PROG_RD	0 0 0	1 0 0	X X X 1	X X X X	MMU table search program read cycle
MMU_PROG_WR	0 0 0	1 0 0	X X X 0	X X X X	MMU table search program write cycle
MMU_PROG	0 0 0	1 0 0	X X X X	X X X X	Any MMU table search program access
RMW_READ	0 0 0	X X X	0 X X 1	X X X X	Read portion of locked RMW cycle
RMW_WRITE	0 0 0	X X X	0 X X 0	X X X X	Write portion of locked RMW cycle
RMW*	0 0 0	X X X	0 X X X	X X X X	Any portion of locked RMW cycle
DATA_SP_RD_16	0 0 1	X 0 1	X X X 1	X X 1 1	Data space read cycle – MOVE16
DATA_SP_READ	0 0 X	X 0 1	X X X 1	X X X X	Data space read cycle
DATA_SP_WR_16	0 0 1	X 0 1	X X X 0	X X 1 1	Data space write cycle – MOVE16
DATA_SP_WRITE	0 0 X	X 0 1	X X X 0	X X X X	Data space write cycle
PROG_SP_READ	0 0 0	X 1 0	X X X 1	X X X X	Program space read cycle
PROG_SP_WRITE	0 0 0	X 1 0	X X X 0	X X X X	Program space write cycle
CACHE_PUSH	0 0 0	0 0 0	X X X 0	X X X X	Data cache push access
ALT_ACC_READ	0 1 0	X X X	X X X 1	X X X X	Alternate access read cycle
ALT_ACC_WRITE	0 1 0	X X X	X X X 0	X X X X	Alternate access write cycle
ALT_ACC	0 1 0	X X X	X X X X	X X X X	Any alternate access cycle
ALT_BUS_READ	1 X X	X X X	X X X 1	X X X X	Alternate bus master read cycle
ALT_BUS_WRITE	1 X X	X X X	X X X 0	X X X X	Alternate bus master write cycle
ALT_BUS*	1 X X	X X X	X X X X	X X X X	Any alternate bus master cycle
READ	0 X X	X X X	X X X 1	X X X X	Any read cycle
WRITE	0 X X	X X X	X X X 0	X X X X	Any write cycle
SUPER_DATA–16*	0 0 1	1 0 1	X X X X	X X 1 1	Supervisor data space access – MOVE16
SUPR_DATA*	0 0 X	1 0 1	X X X X	X X X X	Supervisor data space access
SUPR_PROG*	0 0 0	1 1 0	X X X X	X X X X	Supervisor program space access
SUPERVISR*	0 0 X	1 X X	X X X X	X X X X	Any supervisor access
U_DATA_16*	0 0 1	0 0 1	X X X X	X X 1 1	User data space access – MOVE16
USER_DATA*	0 0 X	0 0 1	X X X X	X X X X	User data space access
USER_PROG*	0 0 0	0 1 0	X X X X	X X X X	User program space access
USER*	0 0 X	0 X X	X X X X	X X X X	Any user space access

Table 2–1: Control group symbol table definitions (cont.)

Symbol	Control group value BG~ TT1 TT0 / TM2 TM1 TM0 / LOCK~ TS~ TA~ R/W~ / MI~ TEA~ SIZ1 SIZ0	Meaning
DATA_SPACE_16*	0 0 1 / X 0 1 / X X X X / X X 1 1	Any data space access – MOVE16
DATA_SPAC*	0 0 X / X 0 1 / X X X X / X X X X	Any data space access
PROG_SPACE*	0 0 0 / X 0 1 / X X X X / X X X X	Any program space access

*** Symbols used only for triggering; they are not displayed.**

Information on basic operations describes how to use symbolic values for triggering, and displaying other channel groups symbolically, such as the Address channel group.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. Information covers the following topics:

- Acquiring data
- Viewing disassembled data in various display formats
- Cycle type labels
- How to change the way data is displayed
- How to change disassembled cycles with the mark cycles function

Acquiring Data

Once you load the 68040A support, choose a clocking mode and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual, whichever is available.

Viewing Disassembled Data

You can view disassembled data in four different display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE. *Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly.*

The default display format shows the Address, Data, and Control channel group values for each sample of acquired data.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–2 shows the special characters and strings displayed by the 68040 disassembler and gives a definition of what they represent.

Table 2–2: Special characters in the display and meaning

Character or string displayed	Meaning
m	The instruction was manually marked as a program fetch
**	Indicates there is insufficient data available for complete disassembly of the instruction; the number of asterisks will indicate the width of the data that is unavailable. Two asterisks represent a byte.
#	Indicates an immediate value
t	Indicates the number shown is in decimal, such as #12t
* ILLEGAL INSTRUCTION *	Decoded as an illegal instruction
A-LINE OPCODE	Displayed for an A-Line trap instruction
F-LINE OPCODE	Displayed for an F-Line trap instruction

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–3 shows these cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled with the vector name.

Table 2–3: Cycle type definitions

Cycle type	Definition
(LPSTOP BROADCAST)*	The 68040 enters an LPSTOP cycle
(BREAKPOINT ACK)*	A breakpoint acknowledge cycle
(INT ACK LEVEL: n)*	An interrupt acknowledge cycle
(SPURIOUS INTERRUPT)	The 68040 signals a spurious interrupt
(BUS ERROR)	A bus cycle error
(BUS ERROR RETRY)	A bus cycle error retry
(MMU TABLE READ)	A search and read cycle of the MMU table
(MMU TABLE WRITE)	A search and write cycle of the MMU table
(RMW READ)	The read portion of a read-modify-write cycle
(RMW WRITE)	The write portion of a read-modify-write cycle
(READ)	Any read cycle
(WRITE)	Any write cycle
(CACHE PUSH)	The 68040 writes cache to memory
(ALTERNATE ACCESS READ)	An alternate access read cycle
(ALTERNATE ACCESS WRITE)	An alternate access write cycle
(ALT BUS MASTER: READ)	An alternate bus master read cycle

Table 2–3: Cycle type definitions (cont.)

Cycle type	Definition
(ALT BUS MASTER: WRITE)	An alternate bus master write cycle
(UNKNOWN)	An unexpected or unrecognized combination of bits.
(PREFETCH IGNORED)*	A burst fill to the instruction cache that is not executed
(CACHE BURST FILL)*	A burst fill to the data cache
(EXTENSION)*	A fetch cycle computed to be an opcode extension
(FLUSH)*	A fetch cycle computed to be an opcode flush

* **Computed cycle types.**

Figure 2–1 shows an example of the Hardware display.

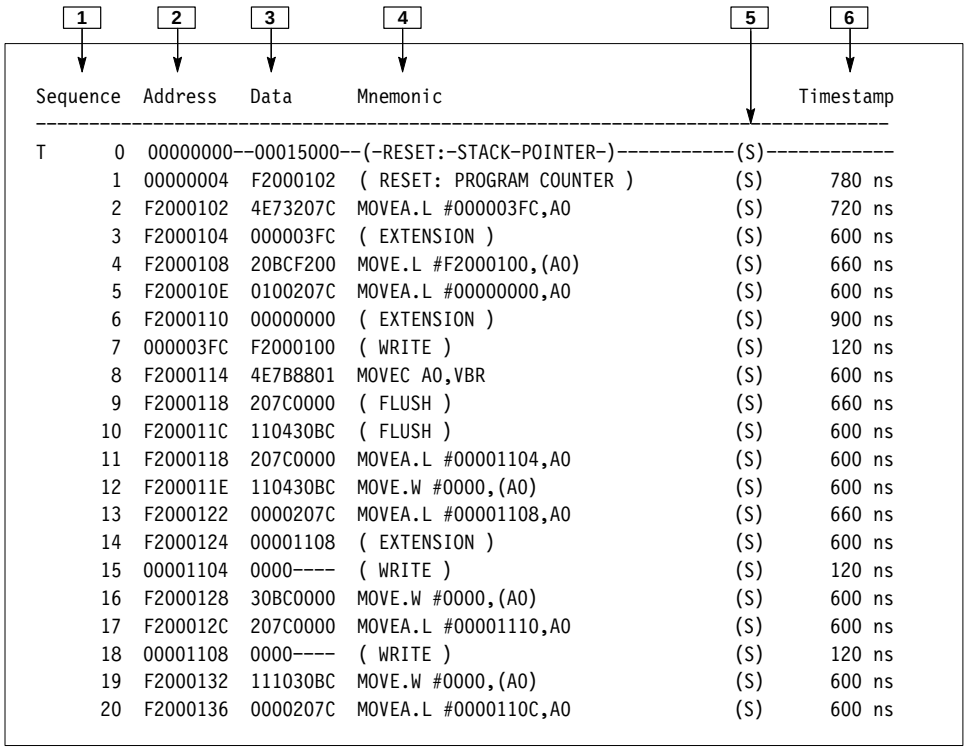


Figure 2–1: Hardware display format

1 **Sample Column.** Lists the memory locations for the acquired data.

2 **Address Group.** Lists data from channels connected to the 68040 Address bus.

3 **Data Group.** Lists data from channels connected to the 68040 Data bus.

4 **Mnemonic Column.** Lists the disassembled instructions and cycle types.

5 The disassembler displays an (S) or (U) in the mnemonic column to indicate the mode in which the microprocessor is operating, Supervisor or User.

6 **Timestamp.** Lists the timestamp values when a timestamp selection is made. Information on basic operations describes how you can select a timestamp.

Software Display Format

The Software display format shows only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Read extensions will be used to disassemble the instruction, but will not be displayed as a separate cycle in the Software display format. Data reads and writes are not displayed.

The Software display format also shows the following cycles:

- Reset cycle
- Halt cycle
- Bus Error cycle
- Special cycles: Breakpoint Ack, Int Ack, Internal Reg Access, Reset Vector
- Reads from the vector table that appear due to servicing interrupts or traps.
- Illegal instructions will be displayed
- Unknown cycle types; the disassembler does not recognize the Control group value

Control Flow Display Format

The Control Flow display format shows only the first fetch of instructions that change the flow of control.

The Control Flow display format also shows the following cycles:

- Bus error cycle
- Bus error retry cycle
- Spurious interrupts
- The special cycles: Breakpoint Ack, Int Ack, LPSTOP Broadcast, and Emulated instructions which cause exceptions.
- Reset vector
- Reads from the exception table that appear due to servicing exceptions
- Illegal instructions

- Unknown cycle types; the disassembler does not recognize the Control group value

Instructions that generate a subroutine call or a return in the 68040 microprocessor are as follows:

BRKPT	BSR	ILLEGAL
JSR	LPSTOP	RESET
RTD	RTE	RTR
RTS	STOP	TRAP

Instructions that might generate a subroutine call or a return in the 68040 microprocessor are as follows:

CHK	CHK2	DIVS
DIVSL	DIVU	DIVUL
TRAPcc	TRAPV	

Instructions that generate a change in the flow of control in the 68040 microprocessor are as follows:

Subroutine Display Format

The Subroutine display format shows only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

The Subroutine display format also shows the following cycles:

- Bus error cycle
- Bus error retry cycle
- Spurious interrupt
- The special cycles: Breakpoint Ack, Int Ack, LPSTOP Broadcast, and Emulated instructions which cause exceptions.
- Illegal instructions
- Unknown cycle types; the disassembler does not recognize the Control group value

Instructions that generate a subroutine call or a return in the 68040 microprocessor are as follows:

BRKPT	BSR	ILLEGAL
JSR	LPSTOP	RESET
RTD	RTE	RTR
RTS	STOP	TRAP

Instructions that might generate a subroutine call or a return in the 68040 microprocessor are as follows:

CHK	CHK2	DIVS
DIVSL	DIVU	DIVUL
TRAPcc	TRAPV	

Changing How Data is Displayed

There are fields and features that allow you to further modify displayed data to suit your needs. You can make selections unique to the 68040 support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception vectors

Optional Display Selections

You can make optional display selections for aquire disassembled data to help you analyze the data. You can make the selections in the Disassembly property page (the Disassembly Format Definition overlay).

In addition to the common display options (described in the information on basic operations), you can change the displayed data in the following ways:

- Specify the starting address of the vector base register
- Specify the size of the vector table

The 68040 support has two additional fields: Interrupt Table Address, and Interrupt Table Size. These fields appear in the area indicated in the information on basic operations.

Vector Base Register. You can specify the starting address of the vector base register in hexadecimal. The default starting address is 0x00000000.

Vector Table Size. You can specify the size of the vector table in hexadecimal. The default size is 0x400.

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it to one of the following cycle types:

- Opcode (the first byte of an instruction)

- Extension (a subsequent byte of an instruction)
- Flush (an opcode or extension that is fetched but not executed)
- Anything (any valid opcode, extension or flush)
- Read (marks a memory reference read as data)

Mark selections are as follows:

```
OPCODE       Any
OPCODE       Any
OPCODE       FLUSH
FLUSH        FLUSH
FLUSH        OPCODE
READ         READ
EXTENSION    EXTENSION
EXTENSION    OPCODE
EXTENSION    FLUSH


Undo Marks
```

Information on basic operations contains more details on marking cycles.

Displaying Exception Vectors

The disassembler can display exception vectors. You can select to display the interrupt vectors for Real, Virtual, or Protected modes in the Interrupt Table field. (Selecting Virtual is equivalent to selecting Protected.)

You can relocate the table by entering the starting address in the Interrupt Table Address field. The Interrupt Table Address field provides the disassembler with the offset address; enter an eight-digit hexadecimal value corresponding to the offset of the base address of the exception table. The Interrupt Table Size field lets you specify a three-digit hexadecimal size for the table.

You can make the selections in the Disassembly property page (the Disassembly Format Definition overlay).

Interrupt cycle types are computed and cannot be used to control triggering. When the 68040 microprocessor processes an interrupt, the disassembler displays the type of interrupt, if known.

Table NO TAG lists the 68040 exception vectors.

Table 2–4: Interrupt vectors

Exception number	Location in IV* table (in hexadecimal)	Displayed interrupt name
0	0000	RESET: INITIAL INTERRUPT STACK POINTER
1	0004	RESET: INITIAL PROGRAM COUNTER
2	0008	ACCESS FAULT
3	000C	ADDRESS ERROR
4	0010	ILLEGAL INSTRUCTION
5	0014	INTEGER DIVIDE BY ZERO
6	0018	CHK, CHK2 INSTRUCTION
7	001C	FTRAPcc, TRAPcc, TRAPV INSTRUCTIONS
8	0020	PRIVILEGE VIOLATION
9	0024	TRACE
10	0028	LINE 1010 EMULATOR
11	002C	LINE 1111 EMULATOR
12	0030	UNASSIGNED, RESERVED
13	0034	NOT USED BY MC68040
14	0038	FORMAT ERROR
15	003C	UNINITIALIZED INTERRUPT
16–23	0040–005C	UNASSIGNED, RESERVED
24	0060	SPURIOUS INTERRUPT
25	0064	LEVEL 1 INTERRUPT AUTO VECTOR
26	0068	LEVEL 2 INTERRUPT AUTO VECTOR
27	006C	LEVEL 3 INTERRUPT AUTO VECTOR
28	0070	LEVEL 4 INTERRUPT AUTO VECTOR
29	0074	LEVEL 5 INTERRUPT AUTO VECTOR
30	0078	LEVEL 6 INTERRUPT AUTO VECTOR
31	007C	LEVEL 7 INTERRUPT AUTO VECTOR
32–47	0080–00BC	TRAP #0–15 INSTRUCTION VECTORS
48	00CO	FP BRANCH OR SET ON UNORDERED CONDITION
49	00C4	FP INEXACT RESULT
50	00C8	FP DIVIDE BY ZERO
51	00CC	FP UNDERFLOW
52	00DO	FP OPERAND ERROR
53	00D4	FP OVERFLOW
54	00D8	FP SIGNALING NAN

Table 2–4: Interrupt vectors (cont.)

Exception number	Location in IV* table (in hexadecimal)	Displayed interrupt name
55	00DC	FP UNIMPLEMENTED DATA TYPE
56	00EO	NOT USED BY MC68040
57	00E4	NOT USED BY MC68040
58	00E8	NOT USED BY MC68040
59–63	00EC–00FC	UNASSIGNED, RESERVED
64–255	0100–03FC	USER DEFINED VECTORS (192)

*** IV means interrupt vector.**

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your 68040 microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use. You can view the system file without connecting the logic analyzer to your SUT.

Information on basic operations describes how to view the file.

Specifications

Specifications

This chapter contains the following information:

- Probe adapter description
- Specification tables
- Dimensions of the probe adapter
- Channel assignment tables
- Description of how the module acquires 68040 signals
- List of other accessible 68040 signals and extra acquisition channels

Probe Adapter Description

The probe adapter is a nonintrusive piece of hardware that allows the logic analyzer to acquire data from a 68040 microprocessor in its own operating environment with little effect, if any, on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and a socket for a 68040 microprocessor. The probe adapter connects to the microprocessor in the SUT. Signals from the microprocessor-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

All circuitry on the probe adapter is powered from the SUT.

The probe adapter accommodates the Motorola 68040, 68EC040, and 68LC040 microprocessors in a PGA package.

Configuration

Disabling the cache makes all instruction prefetches visible on the bus so they can be acquired and disassembled. The probe adapter contains a jumper you can use to disable the 68040 cache.

With the cache jumper in the NORM position, the SUT controls the cache and the CDIS~ signal is not affected.

With the cache jumper in the DIS position, the CDIS~ signal connects to a 332 Ω pull-down resistor on the probe adapter which disables the cache. To prevent contention with the driving signal, cut or remove pin T5 from the protective socket on the underside of the probe adapter.

Table 3–1 shows the jumper positions.

Table 3–1: Jumper positions

Jumper	Positions
J990 (PGA)	1–2 (NORM) 3–4 (DIS)

Specifications

These specifications are for a probe adapter connected to a compatible Tektronix logic analyzer, and the SUT. Table 3–2 shows the electrical requirements the SUT must produce for the support to acquire correct data

In Table 3–2, for the 102/136-channel module, one podlet load is 20 kΩ in parallel with 2 pF. For the 96-channel module, one podlet load is 100 kΩ in parallel with 10 pF.

Table 3–2: Electrical specification

Characteristics	Requirements	
SUT DC power requirements		
Voltage	4.75-5.25 VDC	
Current	I max (calculated) 210 mA I typ (measured) 146 mA	
SUT clock		
Clock rate	Min. 16.67 MHz Max. 33 MHz	
Minimum setup time required*		
All other signals	5 ns	
Minimum hold time required*		
BG~	5 ns	
All other signals	0 ns	
	Specification	
	AC load	**DC load**
Measured typical SUT signal loading		
Address	4 pF + podlet	(1) podlet
Data	6 pF + podlet	(1) podlet
TIP~	9 pF + (2) podlets	(2) podlets
CDIS~, TBI~, TM2, TLN0–1, AVEC	7 pF + podlet	(1) podlet

Table 3–2: Electrical specification (cont.)

Characteristics	Requirements	
BCLK, BG~	11 pF + podlet	20R6–5 + (1) podlet
RSTI~	11 pF + podlet	(1) podlet
Other signals	5 pF + podlet	(1) podlet

*** Signal setup and hold times are in relation to the rising edge of BCLK.**

Table 3–3 shows the environmental specifications.

Table 3–3: Environmental specification

Characteristic	Description
Temperature	
Maximum operating	+50°C (+122°F)*
Minimum operating	0°C (+32°F)
Non-operating	–55°C to + 75°C (–67°F to +167°F)
Humidity	10% to 95% relative humidity†
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

*** Not to exceed 68040 thermal considerations. Forced air cooling may be required across the CPU.**

† **Designed to meet Tektronix standard 062-2847-00 class 5.**

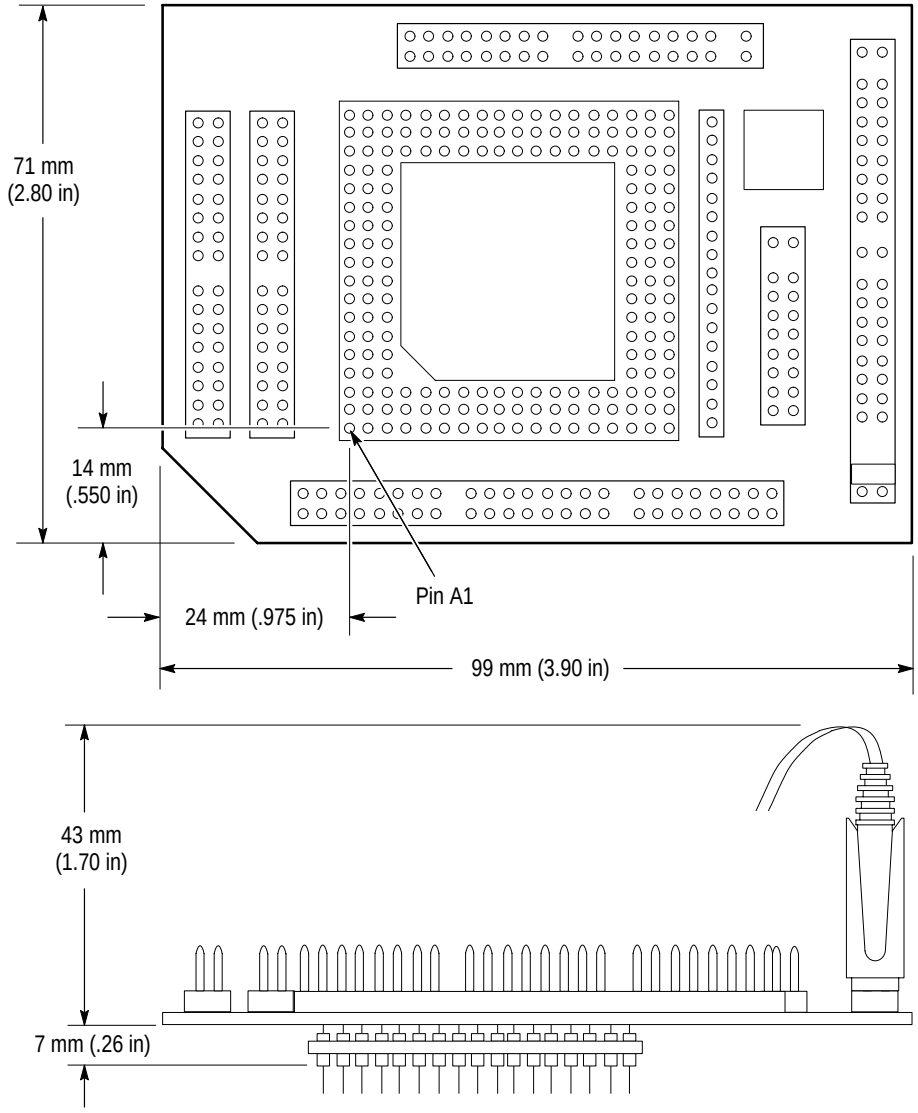


Figure 3–1: Minimum clearance of the PGA probe adapter

Table 3–4 shows the certifications and compliances that apply to the probe adapter.

Table 3–4: Certifications and compliances

EC Compliance	There are no current European Directives that apply to this product.
Pollution Degree 2	Do not operate in environments where conductive pollutants might be present.

Channel Assignments

Channel assignments shown in Table 3–5 through Table 3–11 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the Most Significant Bit (MSB) descending to the Least Significant Bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- A tilde (~) following a signal name indicates an active low signal
- An equals sign (=) following a signal name indicates that it is double probed.

Table 3–5 shows the probe section and channel assignments for the Address group, and the microprocessor signal to which each channel connects. By default this channel group is displayed in hexadecimal.

Table 3–5: Address group channel assignments

Bit order	Section:channel	68040 signal name
31	A3:7	A31
30	A3:6	A30
29	A3:5	A29
28	A3:4	A28
27	A3:3	A27
26	A3:2	A26
25	A3:1	A25
24	A3:0	A24
23	A2:7	A23
22	A2:6	A22
21	A2:5	A21
20	A2:4	A20
19	A2:3	A19
18	A2:2	A18
17	A2:1	A17
16	A2:0	A16
15	A1:7	A15
14	A1:6	A14
13	A1:5	A13
12	A1:4	A12
11	A1:3	A11
10	A1:2	A10
9	A1:1	A9
8	A1:0	A8
7	A0:7	A7
6	A0:6	A6
5	A0:5	A5
4	A0:4	A4
3	A0:3	A3
2	A0:2	A2
1	A0:1	A1
0	A0:0	A0

Table 3–6 shows the probe section and channel assignments for the Data group, and the microprocessor signal to which each channel connects. By default this channel group is displayed in hexadecimal.

Table 3–6: Data group channel assignments

Bit order	Section:channel	68040 signal name
31	D3:7	D31
30	D3:6	D30
29	D3:5	D29
28	D3:4	D28
27	D3:3	D27
26	D3:2	D26
25	D3:1	D25
24	D3:0	D24
23	D2:7	D23
22	D2:6	D22
21	D2:5	D21
20	D2:4	D20
19	D2:3	D19
18	D2:2	D18
17	D2:1	D17
16	D2:0	D16
15	D1:7	D15
14	D1:6	D14
13	D1:5	D13
12	D1:4	D12
11	D1:3	D11
10	D1:2	D10
9	D1:1	D9
8	D1:0	D8
7	D0:7	D7
6	D0:6	D6
5	D0:5	D5
4	D0:4	D4
3	D0:3	D3
2	D0:2	D2
1	D0:1	D1
0	D0:0	D0

Table 3–7 shows the probe section and channel assignments for the Control group, and the microprocessor signal to which each channel connects. By default this channel group is displayed symbolically.

Table 3–7: Control group channel assignments

Bit order	Section: channel	68040 signal name
13	C3:7	BG_L~
12	C3:6	TT1
11	C3:2	TT0
10	C3:4	TM2
9	C2:3*	TM1
8	C2:4	TM0
7	C2:5	LOCK~
6	C2:0*	TS~
5	C2:1*	TA~
4	C2:6	R/W~
3	C3:5	MI~
2	C2:2*	TEA~
1	C3:0	SIZ1
0	C3:3	SIZ0

* **Denotes a qualifier channel.**

Table 3–8 shows the section and channel assignments for the Interrupt group, and the microprocessor signal to which each channel connects for both the probe adapters. By default this channel group is displayed in binary.

Table 3–8: Interrupt group channel assignments

Bit Order	Section: channel	68040 signal name
4	C1:5	AVEC~
3	C0:2	IPEND~
2	C1:6	IPL2~
1	C1:2	IPL1~
0	C0:6	IPL0~

Table 3–9 shows the section and channel assignments for the Cache group, and the microprocessor signal to which each channel connects for the probe adapter. By default this channel group is displayed symbolically.

Table 3–9: Cache group channel assignments

Bit order	Section: Channel	68040 signal name
5	C1:7	TLN1
4	C1:3	TLN0
3	C1:4	SC1
2	C1:0	SC0
1	C3:1	TCI~
0	C0:1	CDIS~

Table 3–10 shows the section and channel assignments for the Misc group, and the microprocessor signal to which each channel connects for the probe adapter. By default this channel group is not visible

Table 3–10: Misc group channel assignments

Bit Order	Section: channel	68040 signal name
6	C2:7	BCLK_B
5	C0:5	RSTI~
4	C0:4	UPA1
3	C0:0	UPA0
2	C0:7	TIP~
1	C1:1	TBI~
0	C0:3	MDIS~

Table 3–11 shows the section and channel assignments for the clock probes (not part of any group) and the microprocessor signal to which each channel connects.

Table 3–11: Clock channel assignments

Section: channel	68040 Signal Name
CK:0	TIP~
CK:1	BG~
CK:2	not connected
CK:3	BCLK

The channels in Table 3–11 are used only to clock in data. These channels are not acquired or displayed. To acquire data from any of the signals shown in Table 3–11, you must connect another channel probe to the signal. This technique is called double probing. An equals sign (=) following a signal name indicates that it is already double probed.

How Data is Acquired

This part of this chapter explains how the module acquires 68040 signals using the TMS 204 software and probe adapter. This part also provides additional information on microprocessor signals accessible on or not accessible on the probe adapter, and on extra acquisition channels available for you to use for additional connections.

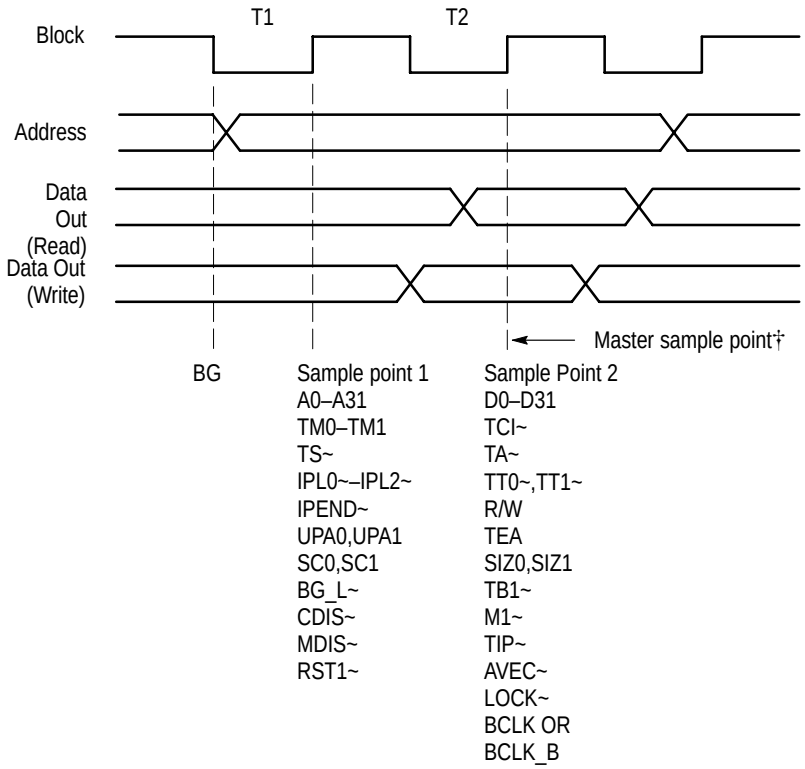
Custom Clocking

A special clocking program is loaded to the module every time you load the 68040 support. This special clocking is called Custom.

With custom clocking, the module logs in signals from multiple groups of channels at different times when they are valid on the 68040 bus. The module then sends all the logged-in signals to the trigger machine and to the acquisition memory of the module for storage.

In custom clocking, the module Clocking State Machine (CSM) generates one master sample for each 68040 bus cycle, no matter how many clock cycles are contained in the bus cycle.

Figure 3–2 shows the sample points and the master sample point for 68040 bus timing.



†Channels not set up in a channel group by the TMS 204 software are logged with the Master sample.

Figure 3–2: 68040 bus timing

Clocking Options

The clocking algorithm for the 68040 support has several variations: Alternate Bus Master Cycles Excluded, and Alternate Bus Master Cycles Included.

The 68040A software provides four modes for acquiring data. You can select the clocking modes by selecting the appropriate fields in the Clock menu.

68040 Address/Data Bus Mode. The 68040 has a multiplexed bus mode that supports the generation of a multiplexed address/data bus. When used in this mode, the address and data bus can be hard-wired together to form a single 32-bit address/data bus at the microprocessor (CPU) with address and data information time–multiplexed on the bus.

You select the 68040 address/data bus mode by selecting Multiplexed in the field. The default selection is Non-Multiplexed.

***NOTE**. If you select the Multiplexed mode, you should remove the channels connected to the data signals to reduce loading.*

Alternate Bus Master Cycles Included. An alternate Bus Master Cycle is defined as the 68040 giving up the bus to an alternate device (a DMA device or another microprocessor). These types of cycles are acquired when you select Included.

Alternate Bus Master Cycles Excluded. Alternate Bus Master Cycles are not acquired.

Alternate Microprocessor Connections

You can connect to microprocessor signals that are not required by the support so you can do more advanced timing analysis. These signals might or might not be accessible on the probe adapter board. The following paragraphs and tables list signals that are or are not accessible on the probe adapter board.

For a list of signals required or not required for disassembly, refer to the channel assignment tables beginning on page 3–5.

Signals On the Probe Adapter

The probe adapter board contains pins for microprocessor signals that are not acquired by the TMS 204 support. You can connect extra channels to these pins, because they can be useful for general purpose analysis.

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.

Table 3–12 shows the microprocessor signals available on J670 of the probe adapter.

Table 3–12: 68040 signals on J670

Pin number	Signal name	Pin number	Signal name
1	GND	10	DLE
2	CIOUT	11	BG~
3	TDO	12	PST1
4	TDI	13	PST2
5	TRST~	14	PST0
6	RSTO~	15	PST3
7	TCK	16	BB~

Table 3–12: 68040 signals on J670 (cont.)

Pin number	Signal name	Pin number	Signal name
8	TMS	17	BR~
9	PCLK	18	LOCKE~

Extra Channels

Table 3–13 lists extra sections and channels that are left after you have connected all the probes used by the support. You can use these extra channels to make alternate SUT connections.

Table 3–13: Extra module sections and channels

Module	Section: channels
102-channels	None
136-channels	E3:7-0, E2:7-0, E1:7-0, E0:7-0
96-channels	None

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Maintenance

Maintenance

This section contains information on the following topics:

- Probe adapter circuit description
- Replacing signal leads
- Replacing protective sockets

Probe Adapter Circuit Description

The TMS 204 probe adapter accommodates the Motorola 68040, 68EC040, or 68LC040 microprocessor in a 179-pin PGA package. The probe adapter contains one PAL that latches BG~ (a hardware pipeline) and reduces the load on the clock by buffering BCLK.

Replacing Signal Leads

Information on basic operations describes how to replace signal leads (individual channel and clock probes).

Replacing Protective Sockets

Information on basic operations describes how to replace protective sockets.

Replaceable Electrical Parts

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 204 68040 microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

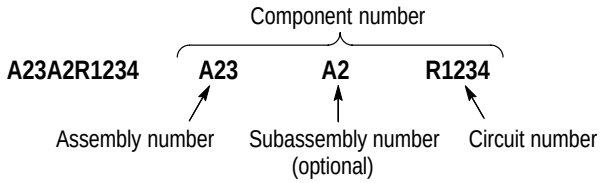
Parts list column descriptions

Column	Column name	Description
1	Component number	The component number appears on diagrams and circuit board illustrations, located in the diagrams section. Assembly numbers are clearly marked on each diagram and circuit board illustration in the *Diagrams* section, and on the mechanical exploded views in the *Replaceable Mechanical Parts* list section. The component number is obtained by adding the assembly number prefix to the circuit number (see Component Number illustration following this table). The electrical parts list is arranged by assemblies in numerical sequence (A1, with its subassemblies and parts, precedes A2, with its subassemblies and parts). Chassis-mounted parts have no assembly number prefix, and they are located at the end of the electrical parts list.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
6	Mfr. code	This indicates the code number of the actual manufacturer of the part.
7	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Component Number



Read: Resistor 1234 (of Subassembly 2) of Assembly 23

List of Assemblies

A list of assemblies is located at the beginning of the electrical parts list. The assemblies are listed in numerical order. When a part's complete component number is known, this list will identify the assembly in which the part is located.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
TK1462	YAMAICHI ELECTRONICS CO LTD 2ND FLOOR NEW KYOEI BLDG 17–11	3–CHROME SHIBAURA MINATO–KU	TOKYO JAPAN
TK2058	TDK CORPORATION OF AMERICA	1600 FEEHANVILLE DRIVE	MOUNT PROSPECT, IL 60056
09969	DALE ELECTRONICS INC	EAST HIGHWAY 50 P O BOX 180	YANKTON SD 57078
01295	TEXAS INSTRUMENTS INC SEMICONDUCTOR GROUP	13500 N CENTRAL EXPY PO BOX 655303	DALLAS TX 75262–5303
22526	BERG ELECTRONICS INC (DUPONT)	857 OLD TRAIL RD	ETTERS PA 17319
26742	METHODE ELECTRONICS INC	7447 W WILSON AVE	CHICAGO IL 60656–4548
50139	ALLEN–BRADLEY CO ELECTRONIC COMPONENTS	1414 ALLEN BRADLEY DR	EL PASO TX 79936
53387	3M COMPANY ELECTRONIC PRODUCTS DIV	3M AUSTIN CENTER	AUSTIN TX 78769–2963
58050	TEKA PRODUCTS INC	45 SALEM ST	PROVIDENCE RI 02907
63058	MCKENZIE TECHNOLOGY	910 PAGE AVENUE	FREMONT CA 94538
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A1	671–2551–00			CIRCUIT BD ASSY:68040/68EC040 PROBE ADAPTER, PGA179,SOCKETED;	80009	671255100
A1C280	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A1C340	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A1C480	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A1C530	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A1C550	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A1C740	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A1C810	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A1C880	283–5004–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,25V,X7R,1206	TK2058	C3216X7R1E104K–
A1J170	————————			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A1J200	————————			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A1J210	————————			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A1J670	————————			CONN,HDR:PCB,;MALE,STR,1 X 36,0.1 CTR,0.230		
A1J880	————————			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A1J910	————————			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A1J990	————————			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235	53387	2480–6122–TB
A1P990	————————			CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X 2,0.1		
A1R980	321–5012–00			RES,FXD:THICK FILM;332 OHM,1%,0.125W,TC=100	50139	BCK3320FT
A1U380	160–8830–00			IC,DIGITAL:STTL,PLD;PAL,20R6,125MHZ,210MA,P RGM 156–6381–00	80009	160–8830–00
A1U540	————————			SOCKET,PCB:PCB,;179 POS,18 X 18,0.1 CTR,0.173 H X 0.183 TAIL,GOLD/GOLD,PHOS BRZ,ACCOM0.015/0.026,PCB 0.024, PAT 1836	63058	PGA179H101B1–18

Replaceable Mechanical Parts

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 204 68040 microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
TK2548	XEROX BUSINESS SERVICES DIV OF XEROX CORPORATION	14181 SW MILLIKAN WAY	BEAVERTON OR 97077
26742	METHODE ELECTRONICS INC	7447 W WILSON AVE	CHICAGO IL 60656–4548
53387	3M COMPANY ELECTRONIC PRODUCTS DIV	3M AUSTIN CENTER	AUSTIN TX 78769–2963
58050	TEKA PRODUCTS INC	45 SALEM ST	PROVIDENCE RI 02907
63058	MCKENZIE TECHNOLOGY	910 PAGE AVENUE	FREMONT CA 94538
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
1–0	010–0551–00			1	PROBE,ADAPTER:68040 & 68EC040,PGA179,PROBE ADAPTER,LASI III;	80009	010055100
–1	671–2551–00			1	CIRCUIT BD ASSY:68040/68EC040 PROBE ADAPTER, PGA179,SOCKETED;	80009	671255100
–2	131–5267–00			2	CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD (J170,J200,J210,880,J910,J990)	53387	2480–6122–TB
–3	131–1857–00			1	CONN,HDR:PCB,;MALE,STR,1 X 36,0.1 CTR,0.230 MLG X 0.100 TAIL,GOLD (J670)	58050	082–3644–SS10
–4	136–1136–00			2	SOCKET,PCB:PCB,;179 POS,18 X 18,0.1 CTR,0.173 H X 0.183 TAIL,GOLD/GOLD,PHOS BRZ,ACCOM 0.015/0.026,PCB 0.024,PAT 1836 (U540)	63058	PGA179H101B1–18
–5	131–4356–00			1	CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X 2,0.1 CTR, 0.63 H,BLK,W/HANDLE,JUMPER (P990)	26742	9618–302–50
					STANDARD ACCESSSORIES		
	070–9822–00			1	MANUAL,TECH:INSTRUCTION,CHIP,DISSASEMBLER, TMS 204	80009	070–9822–00
	070–9803–00			1	MANUAL, TECH:TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070–9803–00
					OPTIONAL ACCESSORIES		
	070–9802–00			1	MANUAL, TECH:BASIC OPS MICRO SUP ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070–9802–00

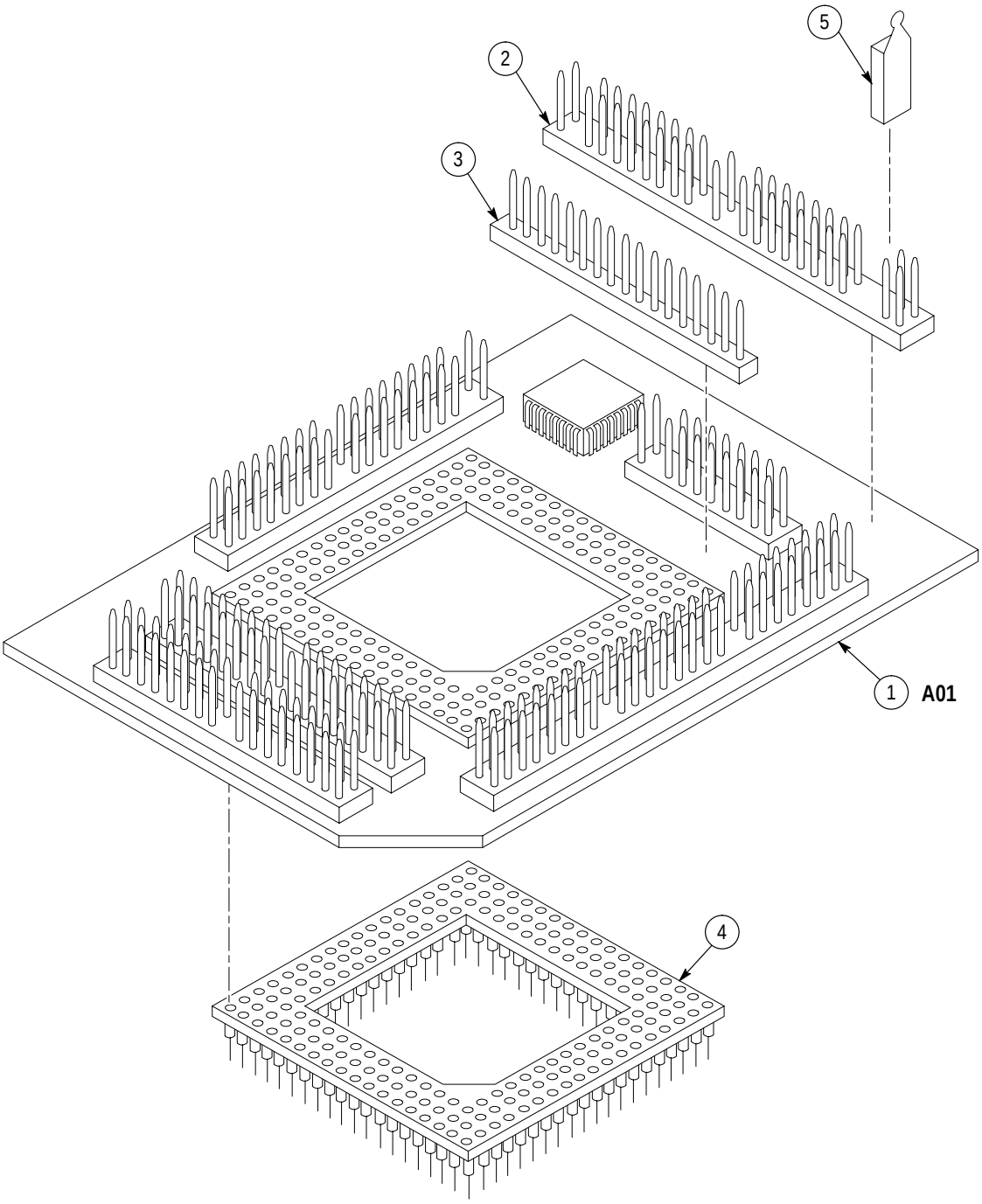


Figure 1: 68040 PGA probe adapter exploded view

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