Instruction Manual

Tektronix

TMS 205
68060 Microprocessor Support

070-9823-00

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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Printed in the U.S.A.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Use Proper Voltage Setting. Before applying power, ensure that the line selector is in the proper position for the power source being used.

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and markings on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface: Microprocessor Support Documentation

This instruction manual contains specific information about the TMS 205 68060 microprocessor support and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor supports on the logic analyzer for which the TMS 205 68060 support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor supports, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor supports is included with each product. Each logic analyzer has basic information that describes how to perform tasks common to supports on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing disassembled data
- The TMS 205 68060 probe adapter

Manual Conventions

This manual uses the following conventions:

- The term disassembler refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to online help, an installation manual, or a basic operations of microprocessor supports user manual.
- In the information on basic operations, the term XXX or P54C used in field selections and file names can be replaced with 68060. This is the name of the microprocessor in field selections and file names you must use to operate the 68060 support.
- The term system under test (SUT) refers to the microprocessor-based system from which data will be acquired.

- The term logic analyzer refers to the Tektronix logic analyzer for which this product was purchased.
- The term module refers to a 102/136-channel or a 96-channel module.
- 68060 refers to all supported variations of the 68060 microprocessor unless otherwise noted.
- An asterisk (*) following a signal name indicates an active low signal.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The user manual provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or, contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Contact your local Tektronix distributor or sales office. Or, visit our web site for a listing of worldwide service locations. http://www.tek.com
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000

Getting Started

Getting Started

This chapter provides information on the following topics:

- The TMS 205 68060 microprocessor support
- Logic analyzer software compatibility
- Your 68060 system requirements
- 68060 support restrictions
- How to configure the probe adapter
- How to connect to the system under test (SUT)

Support Description

The TMS 205 microprocessor support disassembles data from systems that are based on the Motorola 68060 microprocessor. The support runs on a compatible Tektronix logic analyzer equipped with a 102/136-channel module, or a 96-channel module.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 205 microprocessor support.

Table 1–1 shows the microprocessors and packages from which the TMS 205 support can acquire and disassemble data.

Table 1–1: Supported microprocessors

Name	Package
68060	PGA
68EC060	PGA
68LC060	PGA

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Mechanical Parts* chapter.

To use this support efficiently, you need to have the items listed in the information on basic operations as well as the *68060 Microprocessor User's Manual*, Motorola, 1994.

Information on basic operations also contains a general description of supports.

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

To use the 68060 support, the Tektronix logic analyzer must be equipped with at least a 102/136-channel module, or a 96-channel module. The module must be equipped with enough probes to acquire channel and clock data from signals in your 68060-based system.

Refer to information on basic operations to determine how many modules and probes the logic analyzer needs to meet the channel requirements.

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor supports in the information on basic operations as they pertain to your SUT.

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other 68060 support requirements and restrictions.

System Clock Rate. The TMS 205 support can acquire data from the 68060 microprocessor at speeds of up to 50 MHz[1].

68060 Operations or Functions Not Supported. The application does not support Cycle Longword Address, Processor Status lines, Debug Visibility mode, Emulator Debug mode, JTAG operation, or Bus Snooping.

68060 RESET and HALT Cycles. Reset and Halt cycles are not acquired.

Disabling the 68060 Cache. Disabling the cache makes all instruction prefetches visible on the bus so they can be acquired and disassembled.

1 **Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest devices supported.**

Configuring the Probe Adapter

Disabling the cache makes all instruction prefetches visible on the bus so they can be acquired and disassembled. The probe adapter contains a jumper you can use to disable the 68060 cache.

With the Cache jumper in the NORM position, the CDIS* signal connects to a 10 kΩ pull-up resistor on the probe adapter. The SUT controls the cache.

With the Cache jumper in the DIS position, the CDIS* signal connects to a 1 kΩ pull-down resistor on the probe adapter which disables the cache. You might also need to cut or remove pin T5 from the protective socket on the underside of the probe adapter to prevent contention with the driving signal.

Figure 1–1 shows the location of the Cache jumper, J680, on the probe adapter.

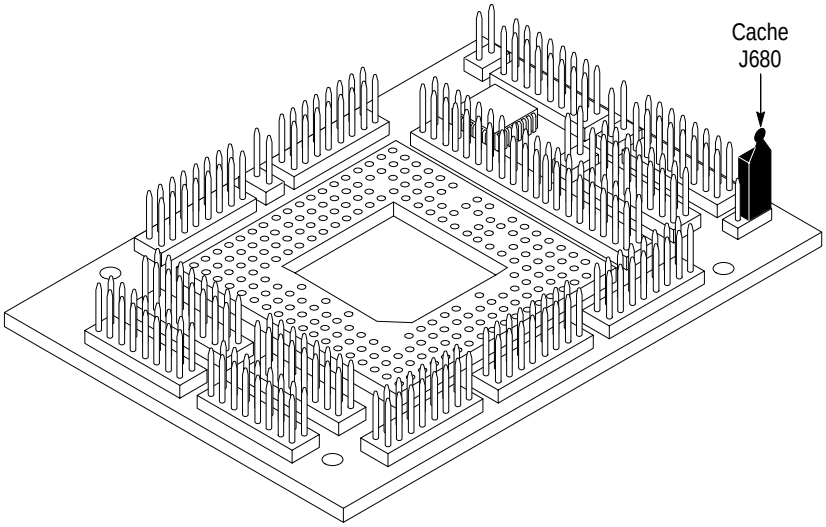


Figure 1–1: Jumper location on the probe adapter

Connecting to a System Under Test

Before you connect to the SUT, you must connect the probes to the module. Your SUT must also have a minimum amount of clear space surrounding the microprocessor to accommodate the probe adapter. Refer to the *Specifications* chapter in this manual for the required clearances.

The channel and clock probes shown in this chapter are for a 102/136-channel module. Your probes will look different if you are using a 96-channel module.

The general requirements and restrictions of microprocessor supports in the information on basic operations shows the vertical dimensions of a channel or clock probe connected to square pins on a circuit board.

PGA Probe Adapter

To connect the logic analyzer to a SUT using a PGA probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probe adapter, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.
3. Place the probe adapter onto the antistatic shipping foam to support the probe as shown in Figure 1–2. This prevents the circuit board from flexing and the socket pins from bending.
4. Remove the microprocessor from your SUT.
5. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on the microprocessor.

CAUTION. *Failure to correctly place the microprocessor into the probe adapter might permanently damage the microprocessor once power is applied.*

6. Place the microprocessor into the probe adapter as shown in Figure 1–2.

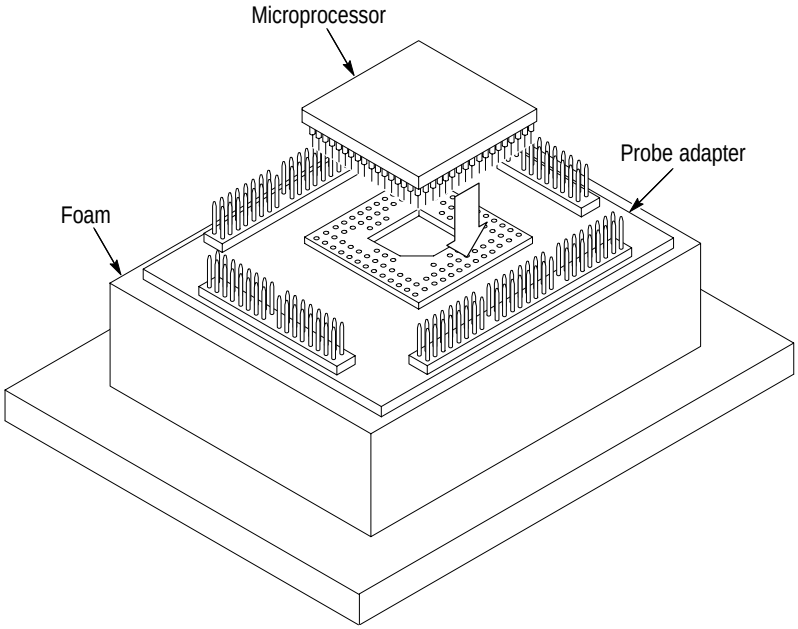


Figure 1–2: Placing a microprocessor into a PGA probe adapter

7. Connect the channel and clock probes to the probe adapter as shown in Figure 1–3. Match the channel groups and numbers on the probe labels to the corresponding pins on the probe adapter. Match the ground pins on the probes to the corresponding pins on the probe adapter.

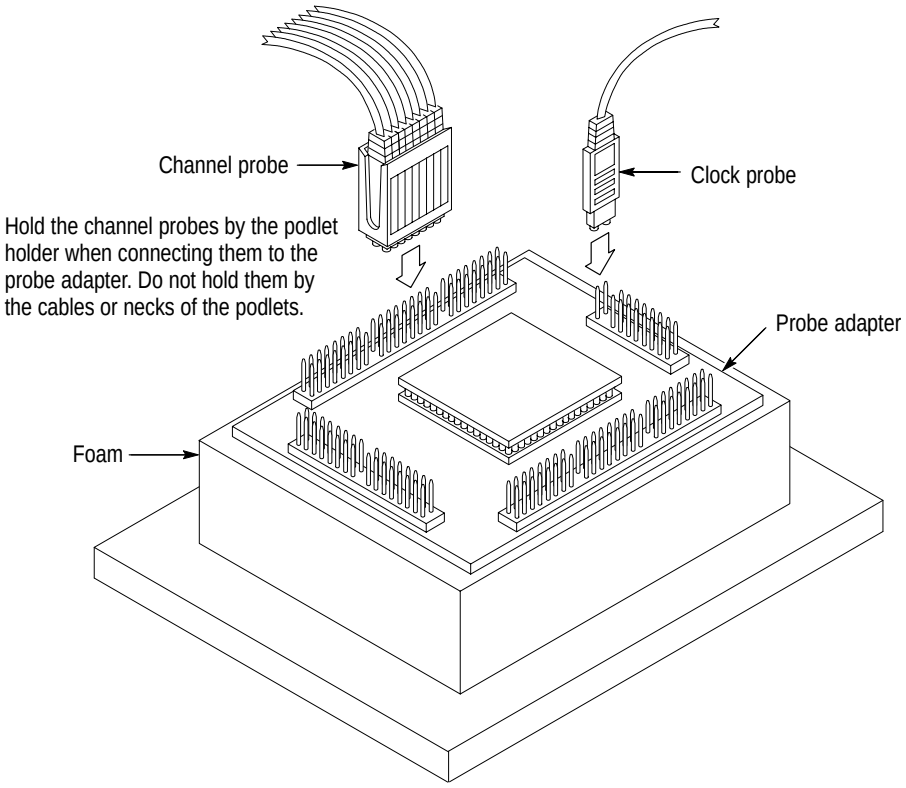


Figure 1–3: Connecting probes to a PGA probe adapter

8. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on your SUT.

9. Place the probe adapter onto the SUT as shown in Figure 1–4.

NOTE. *You might need to stack one or more replacement sockets between the SUT and the probe adapter to provide sufficient vertical clearance from adjacent components. However, keep in mind that this might increase loading, which can reduce the electrical performance of your probe adapter.*

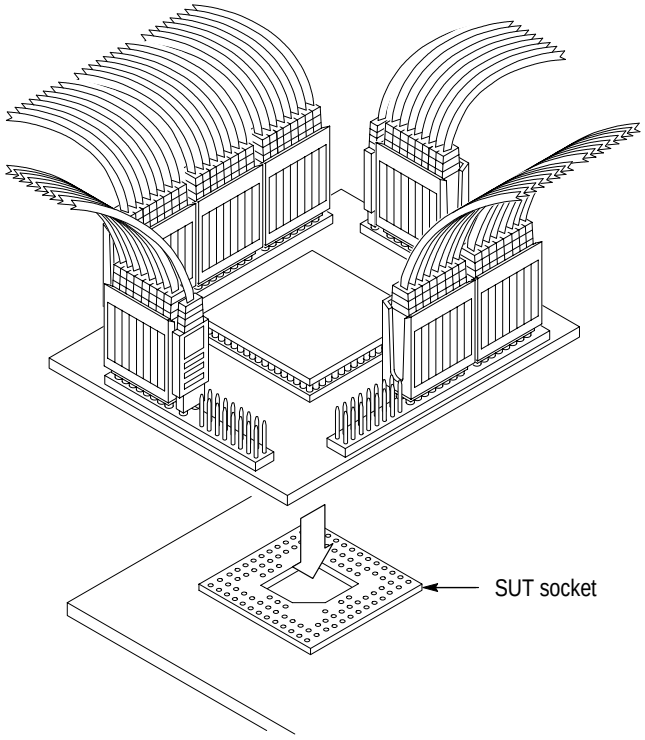


Figure 1–4: Placing a PGA probe adapter onto the SUT

Without a Probe Adapter

You can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your SUT.

To connect the probes to 68060 signals in the SUT using a test clip, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from it.

CAUTION. *Failure to place the SUT on a horizontal surface before connecting the test clip might permanently damage the pins on the microprocessor.*

3. Place the SUT on a horizontal static-free surface.

4. Use Table 1–2 to connect the channel probes to 68060 signal pins on the test clip or in the SUT.

Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip. The default display radix is OFF.

Table 1–2: 68060 signal connections for channel probes

Section:channel	68060 signal	Section:channel	68060 signal
A3:7	A31	D3:7	D31
A3:6	A30	D3:6	D30
A3:5	A29	D3:5	D29
A3:4	A28	D3:4	D28
A3:3	A27	D3:3	D27
A3:2	A26	D3:2	D26
A3:1	A25	D3:1	D25
A3:0	A24	D3:0	D24
A2:7	A23	D2:7	D23
A2:6	A22	D2:6	D22
A2:5	A21	D2:5	D21
A2:4	A20	D2:4	D20
A2:3	A19	D2:3	D19
A2:2	A18	D2:2	D18
A2:1	A17	D2:1	D17
A2:0	A16	D2:0	D16
A1:7	A15	D1:7	D15
A1:6	A14	D1:6	D14
A1:5	A13	D1:5	D13
A1:4	A12	D1:4	D12
A1:3	A11	D1:3	D11
A1:2	A10	D1:2	D10
A1:1	A9	D1:1	D9

Table 1–2: 68060 signal connections for channel probes (cont.)

Section:channel	68060 signal	Section:channel	68060 signal
A1:0	A8	D1:0	D8
A0:7	A7	D0:7	D7
A0:6	A6	D0:6	D6
A0:5	A5	D0:5	D5
A0:4	A4	D0:4	D4
A0:3	A3	D0:3	D3
A0:2	A2	D0:2	D2
A0:1	A1	D0:1	D1
A0:0	A0	D0:0	D0
C3:7	CLK‡	C2:7	CLKEN*‡
C3:6	LOCK*	C2:6	TM2
C3:5	SIZ0	C2:5	TM1
C3:4	SIZ1	C2:4	TM0
C3:3	MODE*†	C2:3	BG_D*†
C3:2	R/W*	C2:2	TRA*
C3:1	TT0	C2:1	TEA*
C3:0	TT1	C2:0	TA*
C1:7	TS*‡	C0:7	TLN0‡
C1:6	SAS*‡	C0:6	TLN1‡
C1:5	IPL0*‡	C0:5	MDIS*‡
C1:4	TBI*‡	C0:4	TCI*‡
C1:3	IPL1*‡	C0:3	CDIS*‡
C1:2	IPL2*‡	C0:2	UPA0‡
C1:1	IPEND*‡	C0:1	UPA1‡
C1:0	AVEC*‡	C0:0	CIOUT*‡

† **Signal logically derived.**

‡ **Signal not required for disassembly.**

Table 1–3 lists the clock probes and the 68060 signal to which they must connect for disassembly to be correct.

Table 1–3: 68060 signal connections for clock probes

Section:channel	68060 signal
CK:3	CLK=
CK:2	CLKEN*=
CK:1	TS*=
CK:0	SAS*=

5. Align pin 1 or A1 of your test clip with the corresponding pin 1 or A1 of the 68060 microprocessor in your SUT and attach the clip to the microprocessor.

Operating Basics

Setting Up the Support

This section provides information on how to set up the support. Information covers the following topics:

- Channel group definitions
- Clocking options
- Symbol table files

Remember that the information in this section is specific to the operations and functions of the TMS 205 68060 support on any Tektronix logic analyzer for which it can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and disassemble data, you need to load the support and specify setups for clocking, and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The software automatically defines the support channel groups. The channel groups for the 68060 support are Address, Data, Control, Interrupt, Cache, Misc, and Clock. If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 3–5.

Clocking Options

The TMS 205 support offers a microprocessor-specific clocking mode for the 68060 microprocessor. This clocking mode is the default selection whenever you load the 68060 support.

A description of how cycles are sampled by the module using the support and probe adapter is found in the *Specifications* chapter.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

The clocking option for the TMS 205 support is Alternate Bus Master Cycles.

Alternate Bus Master Cycles

An alternate bus master cycle is defined as the 68060 microprocessor giving up the bus to an alternate device (a DMA device or another microprocessor). These types of cycles are acquired when you select Included with SAS* (if the alternate bus master provides the Start Acknowledge Sampling signal), or Included, without SAS* (if the SAS* signal is not provided).

Symbols

The TMS 205 support supplies two symbol table files. The 68060_Ctrl file replaces specific Control channel group values with symbolic values when Symbolic is the radix for the channel group.

Information on basic operations describes how to use symbolic values for triggering and displaying other channel groups symbolically, such as the Address channel group.

Table 2–1 lists the name, bit pattern, and meaning for the symbols in the file 68060_Ctrl.

Table 2–1: Control group symbol table definitions

Symbol	Control group value BG* TT1 TT0 TM2 TM1 TM0 LOCK* MODE* TA* R/W* TRA* TEA* SIZ1 SIZ0	Meaning
LPSTOP_ACK	0 1 1 0 0 0 1 X 0 0 1 1 1 0	LPSTOP Acknowledge cycle
LPSTOP_ERR_40	0 1 1 0 0 0 1 0 1 0 1 0 1 0	LPSTOP Error, 68040 Mode*
LPSTOP_ERR_60	0 1 1 0 0 0 1 1 X 0 X 0 1 0	LPSTOP Error, 68060 Mode*
BKPT_ACK	0 1 1 0 0 0 1 X 0 1 1 1 0 1	Breakpoint Acknowledge cycle
BKPT_ERROR_40	0 1 1 0 0 0 1 0 1 1 1 0 0 1	Breakpoint Error, 68040 Mode*
BKPT_ERROR_60	0 1 1 0 0 0 1 1 X 1 X 0 0 1	Breakpoint Error, 68060 Mode*
INT_ACK	0 1 1 X X X 1 X 0 1 1 1 0 1	Interrupt Acknowledge cycle†
SPUR_INT_40	0 1 1 X X X 1 0 1 1 1 0 0 1	Spurious Interrupt, 68040 Mode*
SPUR_INT_60	0 1 1 X X X 1 1 X 1 X 0 0 1	Spurious Interrupt, 68060 Mode*
BUS_ERROR_40	0 X X X X X X 0 1 X 1 0 X X	Bus Error, 68040 Mode*
BUS_ERROR_60	0 X X X X X X 1 X X X 0 X X	Bus Error, 68060 Mode*
BUS_RETRY_40	0 X X X X X X 0 0 X 1 0 X X	Bus Retry, 68040 Mode*
BUS_RETRY_60	0 X X X X X X 1 X X 0 1 X X	Bus Retry, 68060 Mode*
PREFETCH?	0 0 0 X 1 0 1 X X 1 X X X X	Probable instruction or extension; includes PC-relative operands

Table 2–1: Control group symbol table definitions (cont.)

Symbol	Control group value BG* TT1 TT0 / TM2 TM1 TM0 / LOCK* MODE* TA* R/W* / TRA* TEA* SIZ1 SIZ0	Meaning
MMU_DATA_RD	0 0 0 / 0 1 1 / X X X 1 / X X X X	MMU Table Search Data Read cycle
MMU_DATA_WR	0 0 0 / 0 1 1 / X X X 0 / X X X X	MMU Table Search Data Write cycle
MMU_DATA	0 0 0 / 0 1 1 / X X X X / X X X X	Any MMU Table Search Data access
MMU_PROG_RD	0 0 0 / 1 0 0 / X X X 1 / X X X X	MMU Table Search Program Read cycle
MMU_PROG_WR	0 0 0 / 1 0 0 / X X X 0 / X X X X	MMU Table Search Program Write cycle
MMU_PROG	0 0 0 / 1 0 0 / X X X X / X X X X	Any MMU Table Search Program access
RMW_READ	0 0 0 / X X X / 0 X X 1 / X X X X	Read part of a Locked Read-Modify-Write cycle‡
RMW_WRITE	0 0 0 / X X X / 0 X X 0 / X X X X	Write part of a Locked Read-Modify-Write cycle§
RMW	0 0 0 / X X X / 0 X X X / X X X X	Any part of a Locked Read-Modify-Write cycle‡§
DATA_SP_RD_16	0 0 1 / X 0 1 / X X X 1 / X X 1 1	Data Space Read cycle; MOVE16
DATA_SP_READ	0 0 X / X 0 1 / X X X 1 / X X X X	Data Space Read cycle
DATA_SP_WR_16	0 0 1 / X 0 1 / X X X 0 / X X 1 1	Data Space Write cycle; MOVE16
DATA_SP_WRITE	0 0 X / X 0 1 / X X X 0 / X X X X	Data Space Write cycle
PROG_SP_READ	0 0 0 / X 1 0 / X X X 1 / X X X X	Program Space Read cycle
PROG_SP_WRITE	0 0 0 / X 1 0 / X X X 0 / X X X X	Program Space Write cycle
CACHE_PUSH	0 0 0 / 0 0 0 / X X X 0 / X X X X	Data Cache Push Write cycle
ALT_ACC_READ	0 1 0 / X X X / X X X 1 / X X X X	Alternate Access Read cycle
ALT_ACC_WRITE	0 1 0 / X X X / X X X 0 / X X X X	Alternate Access Write cycle
ALT_ACC	0 1 0 / X X X / X X X X / X X X X	Any Alternate Access cycle
ALT_BUS_READ	1 X X / X X X / X X X 1 / X X X X	Alternate Bus Master Read cycle
ALT_BUS_WRITE	1 X X / X X X / X X X 0 / X X X X	Alternate Bus Master Write cycle
ALT_BUS	1 X X / X X X / X X X X / X X X X	Any Alternate Bus Master cycle
READ	0 X X / X X X / X X X 1 / X X X X	Any Read cycle, known and unknown
WRITE	0 X X / X X X / X X X 0 / X X X X	Any Write cycle, known and unknown
SUPER_DATA_16	0 0 1 / 1 0 1 / X X X X / X X 1 1	Supervisor Data Space access; MOVE16
SUPER_DATA	0 0 X / 1 0 1 / X X X X / X X X X	Supervisor Data Space access
SUPER_PROG	0 0 0 / 1 1 0 / X X X X / X X X X	Supervisor Program Space access
SUPERVISOR	0 0 X / 1 X X / X X X X / X X X X	Any Supervisor Space access¶
USER_DATA_16	0 0 1 / 0 0 1 / X X X X / X X 1 1	User Data Space access; MOVE16
USER_DATA	0 0 X / 0 0 1 / X X X X / X X X X	User Data Space access

Table 2–1: Control group symbol table definitions (cont.)

Symbol	Control group value BG* TT1 TT0 TM2 TM1 TM0 LOCK* MODE* TA* R/W* TRA* TEA* SIZ1 SIZ0	Meaning
USER_PROG	0 0 0 0 1 0 X X X X X X X X	User Program Space access
USER	0 0 X 0 X X X X X X X X X X	Any User Space access**
DATA_SPACE_16	0 0 1 X 0 1 X X X X X X 1 1	Any Data Space access; MOVE16
DATA_SPACE	0 0 X X 0 1 X X X X X X X X	Any Data Space access
PROG_SPACE	0 0 0 X 1 0 X X X X X X X X	Any Program Space access

* When these Error or Retry symbols are used for triggering, you must select the appropriate one for the operating mode of the 68060 microprocessor. If the operating mode is not known, select a trigger program with an A or B event and use one of the symbols in event A and the other symbol in event B.

† When this symbol is used for triggering, the logic analyzer will also trigger on any Breakpoint Acknowledge cycle.

‡ When this symbol is used for triggering, the logic analyzer will also trigger on locked MMU Table Search Read cycles.

§ When this symbol is used for triggering, the logic analyzer will also trigger on locked MMU Table Search Write cycles.

¶ When this symbol is used for triggering, the logic analyzer will also trigger on any MMU Table Search Program access.

** When this symbol is used for triggering, the logic analyzer will also trigger on any MMU Table Search Data access, or on any Data Cache Push access.

Table 2–2 lists the name, bit pattern, and meaning for the symbols in the file 68060_Intr, the Interrupt group symbol table.

Table 2–2: Interrupt group symbol table definitions

Symbol	Interrupt group value AVEC* IPEND* IPL2* IPL1* IPL0*	Meaning
–	X X 1 1 1	No interrupt
IPL_1	X X 1 1 0	Level 1 interrupt request
IPL_2	X X 1 0 1	Level 2 interrupt request
IPL_3	X X 1 0 0	Level 3 interrupt request
IPL_4	X X 0 1 1	Level 4 interrupt request
IPL_5	X X 0 1 0	Level 5 interrupt request
IPL_6	X X 0 0 1	Level 6 interrupt request
IPL_7	X X 0 0 0	Level 7 interrupt request
IPEND	X 0 X X X	Interrupt pending

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. Information covers the following topics:

- Acquiring data
- Viewing disassembled data in various display formats
- Cycle type labels
- How to change the way data is displayed
- How to change disassembled cycles with the mark cycles function

Acquiring Data

Once you load the 68060 support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual, whichever is available.

Viewing Disassembled Data

You can view disassembled data in four display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE. *Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–11.*

The default display format shows the Address, Data, and Control channel group values for each sample of acquired data.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–3 lists the special characters and strings displayed by the 68060 disassembler and gives a definition of what they represent.

Table 2–3: Special characters in the display and meaning

Character or string displayed	Meaning
#	Indicates an immediate value
>>	The instruction was manually marked
t	Indicates the number shown is in decimal, such as #12t
****	Indicates there is insufficient data available for complete disassembly of the instruction; the number of asterisks will indicate the width of the data that is unavailable. Two asterisks represent one byte.
* ILLEGAL INSTRUCTION *	Decoded as an illegal instruction
A-LINE OPCODE	Displayed for an A-Line trap instruction
F-LINE OPCODE	Displayed for an F-Line trap instruction

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–4 lists these cycle type labels and gives a definition of the cycle they represent. Interrupt and exception vectors will be labeled with the vector name.

Table 2–4: Cycle type definitions

Cycle type	Definition
(LPSTOP BROADCAST)	68060 microprocessor is entering an LPSTOP cycle
(BREAKPOINT ACK)	Breakpoint Acknowledge cycle
(INTERRUPT ACK LEVEL: n)*	Interrupt Acknowledge cycle
(SPURIOUS INTERRUPT)	68060 microprocessor signals a spurious interrupt
(BUS ERROR)	Bus error cycle
(BUS ERROR RETRY)	Bus error retry cycle
(MMU TABLE READ)	Table search read cycle
(MMU TABLE WRITE)	Table search write cycle
(RMW READ)	Read part of a read-modify-write cycle
(RMW WRITE)	Write part of a read-modify-write cycle
(READ)	Read cycle
(WRITE)	Write cycle
(CACHE PUSH)	68060 microprocessor is writing cache to memory
(ALTERNATE ACCESS READ)	Alternate access read cycle
(ALTERNATE ACCESS WRITE)	Alternate access write cycle
(ALTERNATE BUS MASTER: READ)	Alternate bus master read cycle

Table 2–4: Cycle type definitions (cont.)

Cycle type	Definition
(ALTERNATE BUS MASTER: WRITE)	Alternate bus master write cycle
(UNKNOWN)	The combination of control bit values is unexpected and/or unrecognized
(PREFETCH IGNORED)*	Burst fill to the instruction cache that is not executed
(CACHE BURST FILL)*	Burst fill to the data cache
(EXTENSION)*	Instruction fetch spans additional cycle
(FLUSH)*	Instruction fetch not executed caused by a change in the control flow

* **Computed cycle types.**

Figure 2–1 shows an example of the Hardware display.

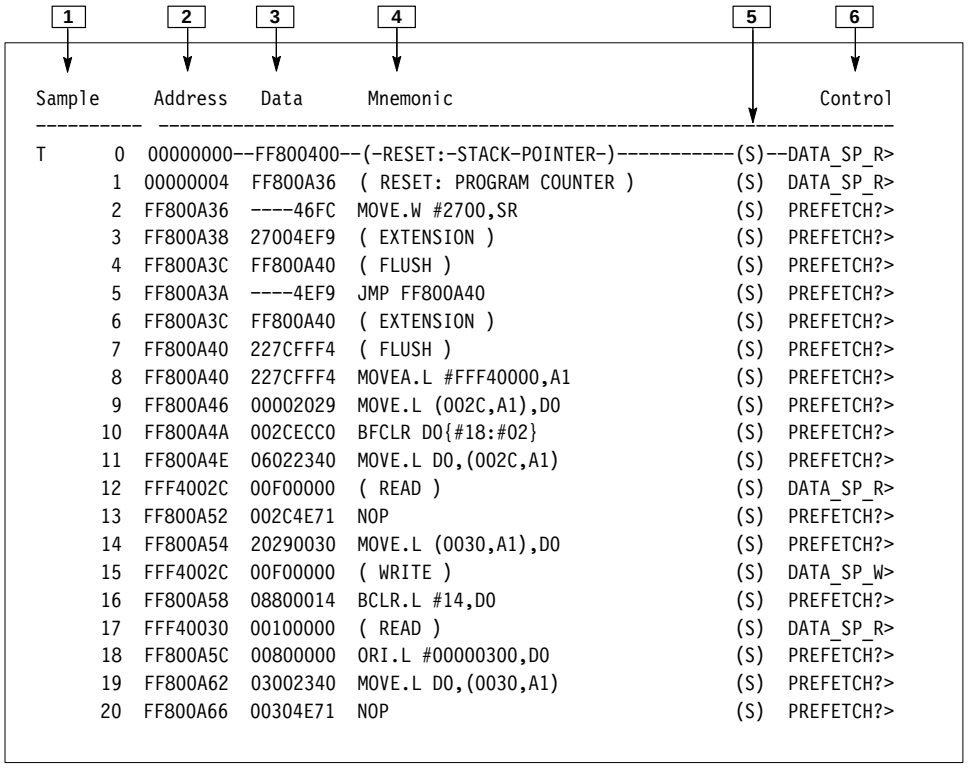


Figure 2–1: Hardware display format

1 **Sample Column.** Lists the memory locations for the acquired data.

2 **Address Group.** Lists data from channels connected to the 68060 Address bus.

3 **Data Group.** Lists data from channels connected to the 68060 Data bus.

4 **Mnemonic Column.** Lists the disassembled instructions and cycle types.

5 The disassembler displays an (S) or (U) in the mnemonic column to indicate the mode in which the microprocessor is operating (Supervisor or User).

6 **Control Group.** Lists data from channels connected to 68060 control signals.

Software Display Format

The Software display format shows the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Read extensions will be used to disassemble the instruction, but will not be displayed as a separate cycle in the Software display format. Data reads and writes are not displayed.

The Software display format also displays the following:

- Bus Error cycle
- Special cycles: Breakpoint Ack, Int Ack, LPSTOP Broadcast, and Emulated instructions which cause exceptions
- Reset Vector
- Reads from the exception vector table that appear due to servicing exceptions
- Illegal instructions
- (UNKNOWN) cycle types; the disassembler does not recognize the control group value

Control Flow Display Format

The Control Flow display format shows the first fetch of instructions that change the flow of control.

The Control Flow display format displays the following:

- Bus Error cycle
- Special cycles: Breakpoint Ack, Int Ack, LPSTOP Broadcast, and Emulated instructions which cause exceptions
- Reset Vector
- Reads from the exception vector table that appear due to servicing exceptions
- Illegal instructions
- (UNKNOWN) cycle types; the disassembler does not recognize the control group value

Instructions that always generate a change in the flow of control in the 68060 microprocessor are as follows:

BKPT	JSR	RTR
BRA	LPSTOP	RTS
BSR	RESET	STOP
ILLEGAL	RTD	TRAP
JMP	RTE	

Instructions that might generate a change in the flow of control in the 68060 microprocessor are as follows:

Bcc	FBcc	TRAPV
DBcc	TRAPcc	

Exceptions that might be interpreted by the disassembler as a change in the flow of control in the 68060 microprocessor are as follows:

CHK	DIVSL	DIVUL
DIVS	DIVU	

The Bcc instruction is a conditional branch. The DBcc instruction is a test condition (decrement, and branch).

Subroutine Display Format

The Subroutine display format shows the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

The Subroutine display format also displays the following:

- Bus Error cycle
- Special cycles: Breakpoint Ack, Int Ack, LPSTOP Broadcast, Emulated instructions which cause exceptions
- Reset Vector
- Reads from the exception vector table that appear due to servicing exceptions
- Illegal instructions
- (UNKNOWN) cycle types; the disassembler does not recognize the control group value

Instructions that always generate a subroutine call or a return in the 68060 microprocessor are as follows:

BKPT	JSR	RTD	RTS
BSR	LPSTOP	RTE	STOP
ILLEGAL	RESET	RTR	TRAP

Exceptions that might be interpreted by the disassembler as a subroutine call or a return in the 68060 microprocessor are as follows:

CHK	DIVSL	DIVUL	TRAPV
DIVS	DIVU	TRAPcc	

Changing How Data is Displayed

There are fields and features that allow you to modify displayed data to suit your needs. You can make selections unique to the 68060 support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception vectors

Optional Display Selections

You can make optional display selections for disassembled data to help you analyze the data. You can make optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

In addition to the common display options (described in the information on basic operations), you can change the displayed data in the following ways:

- Specify the starting address of the exception vector table
- Specify the size of the exception vector table

Vector Base Register. You can specify the starting address of the exception vector table in hexadecimal. The default starting address is 0x00000000.

Vector Table Size. You can specify the size of the exception vector table in hexadecimal. The default size is 0x400.

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it to one of the following cycle types:

- Opcode (the first word of an instruction)
- Extension (a subsequent word of an instruction)
- Flush (an opcode or extension that is fetched but not executed)
- Anything (any valid opcode, extension or flush)
- Read (marks a memory reference read as data)

Mark selections are as follows:

```
Opcode       Anything
Opcode       Opcode
Opcode       Flush
Flush        Flush
Flush        Opcode
Read         Read
Extension    Extension
Extension    Opcode
Extension    Flush

Undo Mark
```

Information on basic operations contains more details on marking cycles.

Displaying Exception Vectors

The disassembler can display 68060 exception vectors. You can select to display the interrupt vectors for Real, Virtual, or Protected modes in the Interrupt Table field. Selecting Virtual is equivalent to selecting Protected.

You can relocate the table by entering the starting address in the Vector Base Register field. The Vector Base Register field provides the disassembler with the offset address; enter an eight-digit hexadecimal value corresponding to the offset of the base address of the exception vector table. The Vector Table Size field lets you specify a three-digit hexadecimal size for the table.

You can make these selections in the Disassembly property page (the Disassembly Format Definition overlay).

Table 2–5 lists the 68060 exception vectors.

Table 2–5: Exception vectors

Exception number	Vector offset (in Hexadecimal)	Displayed exception name
0	000	RESET: STACK POINTER
1	004	RESET: PROGRAM POINTER
2	008	ACCESS FAULT VECTOR
3	00C	ADDRESS ERROR VECTOR
4	010	ILLEGAL INSTRUCTION VECTOR
5	014	ZERO DIVIDE VECTOR
6	018	CHK INSTR VECTOR
7	01C	TRAPcc, TRAPV VECTOR
8	020	PRIV VIOLATION VECTOR
9	024	TRACE VECTOR

Table 2–5: Exception vectors (cont.)

Exception number	Vector offset (in Hexadecimal)	Displayed exception name
10	028	LINE 1010 EMULATOR VECTOR
11	02C	LINE 1111 EMULATOR VECTOR
12	030	EMULATOR INTERRUPT VECTOR
13	034	RESERVED VECTOR #13t
14	038	FORMAT ERROR VECTOR
15	03C	UNINIT INTERRUPT VECTOR
16-23	040-05C	RESERVED VECTOR #16t through #23t
24	060	SPURIOUS INTERRUPT VECTOR
25	064	IPL 1 AUTOVECTOR
26	068	IPL 2 AUTOVECTOR
27	06C	IPL 3 AUTOVECTOR
28	070	IPL 4 AUTOVECTOR
29	074	IPL 5 AUTOVECTOR
30	078	IPL 6 AUTOVECTOR
31	07C	IPL 7 AUTOVECTOR
32-47	080-0BC	TRAP #0t through #15t VECTOR
48	0C0	FPU UNORDERED COND VECTOR
49	0C4	FPU INEXACT RESULT VECTOR
50	0C8	FPU ZERO DIVIDE VECTOR
51	0CC	FPU UNDERFLOW VECTOR
52	0D0	FPU OPERAND ERROR VECTOR
53	0D4	FPU OVERFLOW VECTOR
54	0D8	FPU SIGNALING NAN VECTOR
55	0DC	FPU UNIMP DATA TYPE VECTOR
56-59	0E0-0EC	RESERVED VECTOR #56t through #59t
60	0F0	UNIMP EFFECTIVE ADDR VECTOR
61	0F4	UNIMP INTEGER INSTR VECTOR
62	0F8	RESERVED VECTOR #62t
63	0FC	RESERVED VECTOR #63t
64-255	100-3FC	USER INT VECTOR #64t through #255t

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your 68060 microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your SUT.

Information on basic operations describes how to view the file.

Specifications

Specifications

This chapter contains the following information:

- Probe adapter description
- Specification tables
- Dimensions of the probe adapter
- Channel assignment tables
- Description of how the module acquires 68060 signals
- List of other accessible 68060 signals and extra acquisition channels

Probe Adapter Description

The probe adapter is a nonintrusive piece of hardware that allows the logic analyzer to acquire data from a 68060 microprocessor in its own operating environment with little effect, if any, on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and a socket for a 68060 microprocessor. The probe adapter connects to the microprocessor in the SUT. Signals from the microprocessor-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

All circuitry on the probe adapter is powered from the SUT.

The probe adapter accommodates the Motorola 68060, 68EC060 and 68LC060 microprocessors that use a 206-pin PGA package.

Configuring the Probe Adapter

There is one jumper on the probe adapter you can use to disable the 68060 cache. With the Cache jumper in the NORM position, the CDIS* signal connects to a 10 kΩ pull-up resistor on the probe adapter. The SUT controls the cache.

With the Cache jumper in the DIS position, the CDIS* signal connects to a 1 kΩ pull-down resistor on the probe adapter, which disables the cache. You might also need to cut or remove pin T5 from the protective socket on the underside of the probe adapter to prevent contention with the driving signal.

Figure 3–1 shows the location of the Cache jumper, J680, on the probe adapter.

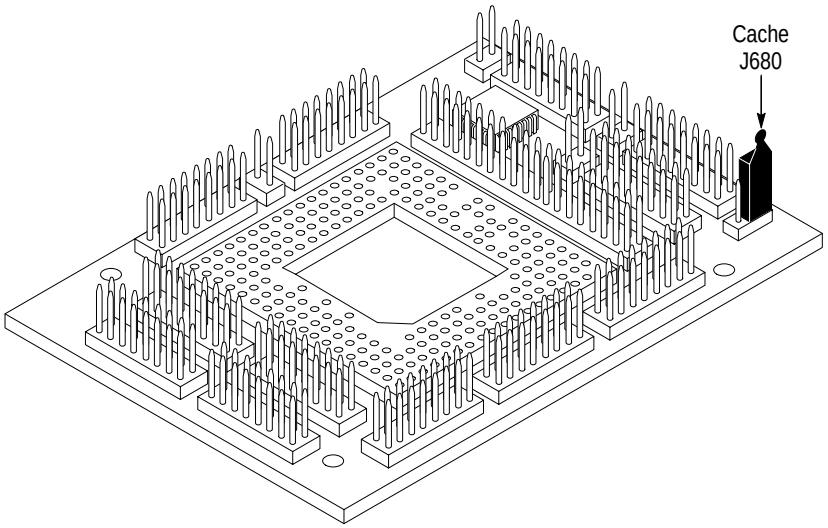


Figure 3–1: Jumper location on the probe adapter

Specifications

The following specifications are for a probe adapter connected to a compatible Tektronix logic analyzer and the SUT. Table 3–1 shows the electrical requirements the SUT must produce for the support to acquire correct data.

In Table 3–1, for the 102/136-channel module, one podlet load is 20 kΩ in parallel with 2 pF. For the 96-channel module, one podlet load is 100 kΩ in parallel with 10 pF.

Table 3–1: Electrical specifications

Characteristics	Requirements
SUT DC power requirements	
Voltage	3.13-3.47 VDC
Current	I max (calculated) 100 mA
SUT clock	
Clock rate	Max. 50 MHz
Minimum setup time required, all signals	5 ns
Minimum hold time required, all signals	0 ns

Table 3–1: Electrical specifications (Cont.)

Characteristics	Requirements	
	Specification	
Measured typical SUT signal loading	**AC load†**	**DC load**
CLK, CLKEN*‡	30 pF + 2 podlets	22V10 PAL in parallel with 2 podlets
TS*	12 pF + 2 podlets	22V10 PAL in parallel with 2 podlets
IPL1*	12 pF + 1 podlet	22V10 PAL in parallel with 1 podlet
RSTI*	12 pF	22V10 PAL
BG*, BB*, BTT*	10 pF	22V10 PAL
SAS*	10 pF + 2 podlets	2 podlets
R/W*, IPL2*, IPL0*, IPEND*	10 pF + 1 podlet	1 podlet
A31-A0, D31-D0, TT1, TT0, TM2-TM0, SIZ1, SIZ0, LOCK*, TA*, TRA*, TEA*, AVEC*, TLN1, TLN0, UPAI, UPA0, CIOUT*, TCI*, TBI*, MDIS*, CDIS*§	7 pF + 1 podlet	1 podlet
CLA*	7 pF	none
BR*, BGR*, TIP*, LOCKE*, BS3*-BS0*, SNOOP*, PST4-PST0, RSTO*, JTAG*, TRST*, TCK, TDI, TDO, TMS	5 pF	none

† **The AC loading value includes run capacitance and input capacitance of the PAL.**

‡ **The CLK and CLKEN* signals include 15 pF with a 100 Ω termination network.**

§ **The CDIS* signal includes a 10 kΩ pull-up resistor when the Cache jumper on the probe adapter is set to NORM or a 1 kΩ pull-down resistor when the Cache jumper is set to DIS.**

Table 3–2: Environmental specification†

Characteristic	Description
Temperature	
Maximum Operating	+50° C (+122° F)*
Minimum Operating	0° C (+32° F)
Non-Operating	–55° C to +75° C (–67° to +167° F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-Operating	15 km (50,000 ft) maximum
Electrostatic Immunity	The probe adapter is static sensitive

*** Not to exceed 68060 thermal considerations. Forced air cooling may be required across the CPU.**

† **Designed to meet Tektronix standard 062-2847-00 class 5.**

Table 3–3 shows the certifications and compliances that apply to the probe adapter.

Table 3–3: Certifications and compliances

EC Compliance	There are no current European Directives that apply to this product.
Pollution Degree 2	Do not operate in environments where conductive pollutants might be present.

Figure 3–2 lists the dimensions of the probe adapter. Information on basic operations lists the vertical clearance of the channel and clock probes when connected to a probe adapter in the description of general requirements and restrictions.

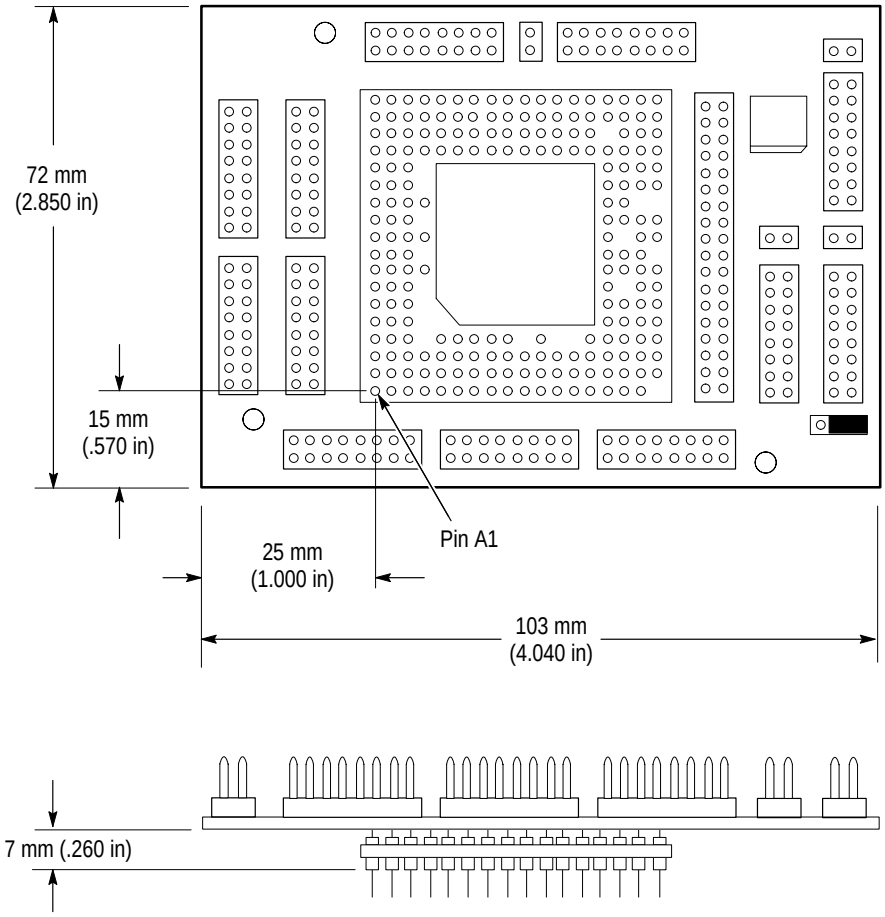


Figure 3–2: Minimum clearance of the probe adapter

Channel Assignments

Channel assignments listed in Table 3–4 through Table 3–11 use the following conventions:

- All signals are required by the support unless indicated otherwise
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB)
- Channel group assignments are for all modules unless otherwise noted
- An asterisk (*) following a signal name indicates an active low signal

- An equals sign (=) following a signal name indicates that it is double probed

Table 3–4 lists the probe section and channel assignments for the Address group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–4: Address group channel assignments

Bit order	Section: channel	68060 signal name
31	A3:7	A31
30	A3:6	A30
29	A3:5	A29
28	A3:4	A28
27	A3:3	A27
26	A3:2	A26
25	A3:1	A25
24	A3:0	A24
23	A2:7	A23
22	A2:6	A22
21	A2:5	A21
20	A2:4	A20
19	A2:3	A19
18	A2:2	A18
17	A2:1	A17
16	A2:0	A16
15	A1:7	A15
14	A1:6	A14
13	A1:5	A13
12	A1:4	A12
11	A1:3	A11
10	A1:2	A10
9	A1:1	A9
8	A1:0	A8
7	A0:7	A7
6	A0:6	A6
5	A0:5	A5
4	A0:4	A4
3	A0:3	A3
2	A0:2	A2

Table 3–4: Address group channel assignments (cont.)

Bit order	Section: channel	68060 signal name
1	A0:1	A1
0	A0:0	A0

Table 3–5 lists the section and channel assignments for the Data group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–5: Data group channel assignments

Bit order	Section: channel	68060 signal name
31	D3:7	D31
30	D3:6	D30
29	D3:5	D29
28	D3:4	D28
27	D3:3	D27
26	D3:2	D26
25	D3:1	D25
24	D3:0	D24
23	D2:7	D23
22	D2:6	D22
21	D2:5	D21
20	D2:4	D20
19	D2:3	D19
18	D2:2	D18
17	D2:1	D17
16	D2:0	D16
15	D1:7	D15
14	D1:6	D14
13	D1:5	D13
12	D1:4	D12
11	D1:3	D11
10	D1:2	D10
9	D1:1	D9
8	D1:0	D8
7	D0:7	D7

Table 3–5: Data group channel assignments (cont.)

Bit order	Section: channel	68060 signal name
6	D0:6	D6
5	D0:5	D5
4	D0:4	D4
3	D0:3	D3
2	D0:2	D2
1	D0:1	D1
0	D0:0	D0

Table 3–6 lists the section and channel assignments for the Control group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–6: Control group channel assignments

Bit order	Section: channel	68060 signal name
13	C2:3	BG_D*†
12	C3:0	TT1
11	C3:1	TT0
10	C2:6	TM2
9	C2:5	TM1
8	C2:4	TM0
7	C3:6	LOCK*
6	C3:3	MODE*†
5	C2:0	TA*
4	C3:2	R/W*
3	C2:2	TRA*
2	C2:1	TEA*
1	C3:4	SIZ1
0	C3:5	SIZ0

† **Signal logically derived.**

Table 3–7 lists the section and channel assignments for the Interrupt group, and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–7: Interrupt group channel assignments

Bit order	Section: channel	68060 signal name
4	C1:0	AVEC*†
3	C1:1	IPEND*†
2	C1:2	IPL2*†
1	C1:3	IPL1*†
0	C1:5	IPL0*†

† **Signal not required for disassembly.**

Table 3–8 lists the section and channel assignments for the Cache group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–8: Cache group channel assignments

Bit order	Section: channel	68060 signal name
7	C0:3	CDIS*†
6	C0:4	TCI*†
5	C0:6	TLN1†
4	C0:7	TLN0†
3	C0:5	MDIS*†
2	C0:0	CIOUT*†
1	C0:1	UPA1†
0	C0:2	UPA0†

† **Signal not required for disassembly.**

Table 3–9 lists the section and channel assignments for the Misc group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–9: Misc group channel assignments

Bit order	Section: channel	68060 signal name
2	C1:7	TS*†
1	C1:6	SAS*†
0	C1:4	TBI*†

† **Signal not required for disassembly.**

Table 3–10 lists the section and channel assignments for the Clock group, and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–10: Clock group channel assignments

Bit Order	Section: channel	68060 signal name
1	C3:7	CLK†
0	C2:7	CLKEN*†

† **Signal not required for disassembly.**

Table 3–11 lists the probe section and channel assignments for the clock probes (not part of any group) and the 68060 signal to which each channel connects.

Table 3–11: Clock channel assignments

Channel	68060 signal name
CK:0	SAS*=
CK:1	TS*=
CK:2	CLKEN*=
CK:3	CLK=

These channels are used only to clock in data; they are not acquired or displayed. To acquire data from any of the signals shown in Table 3–11, you must connect another channel probe to the signal, a technique called double probing. An equals sign (=) following a signal name indicates that it is already double probed.

How Data is Acquired

This section explains how the module acquires 68060 signals using the TMS 205 support and probe adapter. This section also provides additional information on microprocessor signals that are or are not accessible on the probe adapter, and on extra acquisition channels available for you to use for additional connections.

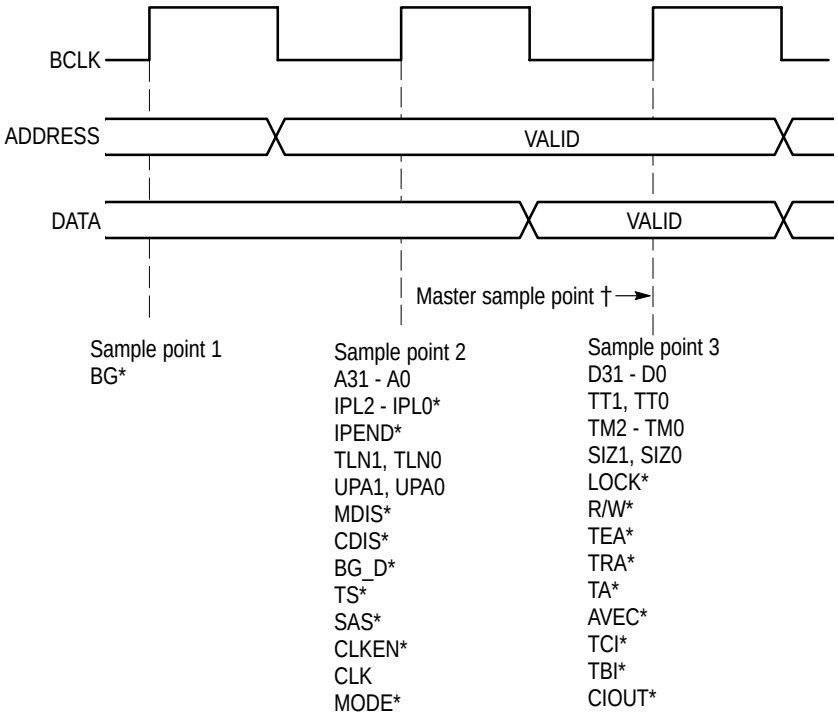
Custom Clocking

A special clocking program is loaded to the module every time you load the 68060 support. This special clocking is called Custom.

With Custom clocking, the module logs signals from multiple groups of channels at different times as they become valid on the 68060 bus. The module then sends all the logged-in signals to the trigger machine and to the acquisition memory of the module for storage.

In Custom clocking, the module clocking state machine (CSM) generates one master sample for each microprocessor bus cycle, no matter how many clock cycles are in the bus cycle.

Figure 3–3 shows the sample points and the master sample point.



†Channels not set up in a channel group by the TMS 205 software are logged with the Master sample.

Figure 3–3: 68060 bus timing

The BCLK signal is derived from the CLK and CLKEN* signals. A BCLK rising edge occurs when the CLK signal rises and the CLKEN* signal is asserted.

Sample point 1 immediately precedes Sample Point 2.

Sample point 2 is determined by the TS* signal.

Sample point 3 is determined by the SAS* and TA*, TRA*, or TEA* signals. This sample point can occur immediately following the second sample point or might not occur until several BCLKs later.

Clocking Options

The clocking algorithm for the 68060 microprocessor has three variations: Alternate Bus Master Cycles Excluded, Alternate Bus Master Cycles Included (without the SAS* signal), and Alternate Bus Master Cycles Included (with the SAS* signal).

Alternate Bus Master Cycles Excluded. Whenever the BG_D* signal is high, no bus cycles are logged. Only bus cycles initiated by the 68060 microprocessor (BG_D* low) will be logged.

Alternate Bus Master Cycles Included. All bus cycles, including alternate bus master cycles are logged in.

When the HLDA signal is high, the microprocessor has given up the bus to an alternate device. The design of the 68060 system affects what data will be logged in. The module only samples the data at the pins of the microprocessor. To properly log in bus activity, any buffers between the microprocessor and the alternate bus master must be enabled and pointing at the microprocessor.

There are two possible clocking interactions when an alternate bus master has control of the bus. The two different possibilities are listed below:

- If the alternate bus master drives the same control lines as the 68060 microprocessor, and the microprocessor “sees” these signals, the bus activity is logged in like normal bus cycles except that the BG_D* signal is high.
- If the control lines are not driven or if the 68060 microprocessor can not see them, the module will not clock in an Alternate Bus Master cycle. For example, if the 68060 microprocessor loses bus mastership, there is not any indication by the disassembler unless an Alternate Bus Master cycle occurs as seen at the 68060 microprocessor.

If the alternate bus master has an Acknowledge Termination Ignore State capability similar to that of the 68060 microprocessor, but does not provide the SAS* (Start Acknowledge Sampling) signal, then Alternate Bus Master cycles cannot be acquired.

Alternate Microprocessor Connections

You can connect to microprocessor signals that are not required by the support so you can do more advanced timing analysis. These signals might or might not be accessible on the probe adapter board. The following paragraphs and tables list signals that are or are not accessible on the probe adapter board.

For a list of signals required or not required for disassembly, refer to the channel assignment tables beginning on page 3–5. Remember that these channels are already included in a channel group. If you do connect these channels to other signals, you should set up another channel group for them.

Signals On the Probe Adapter

The probe adapter board contains pins for microprocessor signals that are not acquired by the TMS 205 software. You can connect extra podlets to these pins.

Table 3–12 lists the microprocessor signals available on J460, the AUX connector, of the probe adapter.

Table 3–12: 68060 signals on J460 (AUX)

Pin No.	Signal name	Pin No.	Signal name
1	GND	23	BGR*
2	RSTO*	24	CLA*
3	TDO	25	BG*
4	TDI	26	PST4
5	TRST*	27	PST1
6	TCK	28	PST2
7	JTAG*	29	PST0
8	TMS	30	TIP*
9	BS0*	31	PST3
10	BS1*	32	BTT*
11	BS2*	33	BB*
12	BS3*	34	SNOOP*
13	RSTI*	35	BR*
14-22	GND	36	LOCKE*

These channels are not defined in any channel group, and data acquired from them is not displayed. To display data, you will need to define a channel group.

Signals Not On the Probe Adapter

The THERM0 and THERM1 microprocessor signals are not accessible on the probe adapter.

Extra Channels

Table 3–13 lists extra sections and channels that are available after you have connected all the probes used by the support. You can use these extra channels to make alternate SUT connections.

Table 3–13: Extra module sections and channels

Module	Section: channels
102-channels	none
136-channels	E3:7-0, E2:7-0, E1:7-0, E0:7-0
96-channels	none

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Maintenance

Maintenance

This section contains a circuit description of the probe adapter.

Probe Adapter Circuit Description

The TMS 205 probe adapter contains a PAL that differentiates 68060 bus cycles from Alternate Bus Master cycles. The PAL is active and in operation at all times so it can send information to the Clocking State Machine (CSM) of the module. The CSM uses the information to determine whether or not to include Alternate Bus Master cycles based on the clocking option in the Clock menu (selection made in the Alternate Bus Master Cycles field).

When Alternate Bus Master cycles are included, an identifier is attached to each Alternate Bus Master cycle so they can be displayed correctly in the Disassembly and State menus. To be displayed in the State menu, you must be using the 68060_Ctrl symbol table for the Control group.

If the alternate bus master in your SUT provides the Start Acknowledge Sampling (SAS*) signal (which indicates when the alternate bus master will begin to sample the termination acknowledge signals TA*, TEA*, or TRA*), then you should use the clocking option that includes that signal. If the alternate bus master does not provide the SAS* signal, the CSM assumes the alternate bus master cycles are terminated whenever the TA*, TEA*, or TRA* signals are asserted.

The PAL equations have two state variables: BG_D* and BB_D*. When BB_D* is reset, BG_D* follows BG* one BCLK later. When BB_D* is set, BG_D* remains in its previous state. BB_D* is set the first time TS* is asserted; it is reset the first time BB* is deasserted, the first time BTT* is asserted, or anytime RSTI* is asserted.

BG_D* is allowed to change state (follow BG*) when BB_D* is being reset, but not when BB_D* is being set. BG_D* cannot be directly reset, but can follow BG* after BB_D* is reset.

The clock delay introduced by the PAL aligns the BG_D* signal with the TS* signal since the 68060 microprocessor is monitoring the BG* signal one BCLK prior to TS*. The CSM logs in the BG_D* and TS* signals when the signals are aligned by the PAL.

The PAL latches the state of the IPL1* signal while RSTI* is asserted. The inverted latched version of the IPL1* signal is called MODE*. The module uses the MODE* signal to determine whether the 68060 microprocessor is operating in the 68040 mode of Acknowledge Termination (encoded) or in the 68060 mode of Acknowledge Termination (unencoded).

Replacing Signal Leads

Information on basic operations describes how to replace signal leads (individual channel and clock probes).

Replacing Protective Sockets

Information on basic operations describes how to replace protective sockets.

Replaceable Electrical Parts

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 205 68060 microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

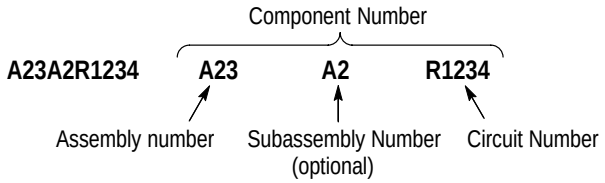
Parts list column descriptions

Column	Column name	Description
1	Component number	The component number appears on diagrams and circuit board illustrations, located in the diagrams section. Assembly numbers are clearly marked on each diagram and circuit board illustration in the *Diagrams* section, and on the mechanical exploded views in the *Replaceable Mechanical Parts* list section. The component number is obtained by adding the assembly number prefix to the circuit number (see Component Number illustration following this table). The electrical parts list is arranged by assemblies in numerical sequence (A1, with its subassemblies and parts, precedes A2, with its subassemblies and parts). Chassis-mounted parts have no assembly number prefix, and they are located at the end of the electrical parts list.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
6	Mfr. code	This indicates the code number of the actual manufacturer of the part.
7	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Component Number



Read: Resistor 1234 (of Subassembly 2) of Assembly 23

List of Assemblies

A list of assemblies is located at the beginning of the electrical parts list. The assemblies are listed in numerical order. When a part's complete component number is known, this list will identify the assembly in which the part is located.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
04222	AVX/KYOCERA DIV OF AVX CORP	19TH AVE SOUTH PO BOX 867	MYRTLE BEACH SC 29577
50139	ALLEN–BRADLEY CO ELECTRONIC COMPONENTS	1414 ALLEN BRADLEY DR	EL PASO TX 79936
53387	3M COMPANY ELECTRONIC PRODUCTS DIV	3M AUSTIN CENTER	AUSTIN TX 78769–2963
63058	MCKENZIE TECHNOLOGY	910 PAGE AVENUE	FREMONT CA 94538
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A1	671–3393–00			CKT BD ASSY:68060,PGA–206 SOCKETED	80009	671339300
A1C150	283–5187–00			CAP,FXD,CERAMIC:MLC;15PF,5%,100V,NPO,1206	04222	12061A150JAT1A
A1C270	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A1C340	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A1C370	283–5187–00			CAP,FXD,CERAMIC:MLC;15PF,5%,100V,NPO,1206	04222	12061A150JAT1A
A1C430	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A1C440	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A1C450	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A1C510	283–5114–00			CAP,FXD,CERAMIC:MLC;0.1UF,10%,50V,X7R,1206	04222	12065C104KAT(1A
A1J130	————————			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1J140	————————			CONN,HDR:PCB,;MALE,STR,1 X 2,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD,TUBE,HIGH TEMP (SEE RMPL FIG.1)		
A1J150	————————			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1J180	————————			CONN,HDR:PCB,;MALE,STR,1 X 2,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD,TUBE,HIGH TEMP (SEE RMPL FIG.1)		
A1J300	————————			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1J310	————————			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		

Replaceable electrical parts list (cont.)

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A1J370	————————			CONN,HDR:PCB,;MALE,STR,1 X 2,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD,TUBE,HIGH TEMP (SEE RMPL FIG.1)		
A1J379	————————			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1J380	————————			CONN,HDR:PCB,;MALE,STR,1 X 2,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD,TUBE,HIGH TEMP (SEE RMPL FIG.1)		
A1J400	————————			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1J410	————————			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1J460	————————			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1J470	————————			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1J480	————————			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1J620	————————			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1J640	————————			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1J650	————————			CONN,HDR:PCB,;MALE,STR,2 X 40,0.1 CTR,0.235 (SEE RMPL FIG.1)		
A1J680	————————			CONN,HDR:PCB,;MALE,STR,1 X 3,0.1 CTR,0.230MLG X 0.120 TAIL,30GOLD,BD RETENTION (SEE RMPL FIG.1)		
A1R150	321–5006–00			RES,FXD:THICK FILM;100 OHM,1%,0.125W,TC=100	50139	BCK1000FT
A1R370	321–5006–00			RES,FXD:THICK FILM;100 OHM,1%,0.125W,TC=100	50139	BCK1000FT
A1R570	321–5030–00			RES,FXD:THICK FILM;10.0K OHM,1%,0.125W,TC=100 PPM	50139	BCK1002FT
A1R670	321–5018–00			RES,FXD:THICK FILM;1.0K OHM,1%,0.125W,TC=100 PPM	50139	BCK1001FT
A1U370	163–0277–00			IC,DIGITAL:CMOS,PLD;EEPLD,22V10,LOW VOLTAGE,7.5NS, ICCQ=75MA,PRGM 156–6983–00	80009	163–0277–00
A1U440	————————			SOCKET,PGA:PCB;206 POS,18 X 18,0.1 CENTERS,0.165 H X 0.275 TAIL,GOLD/GOLD,LONG TAIL,PAT 1854,32DM36 (SEE RMPL FIG.1)		

Replaceable Mechanical Parts

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 205 68060 microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
TK2548	XEROX BUSINESS SERVICES DIV OF XEROX CORPORATION	14181 SW MILLIKAN WAY	BEAVERTON OR 97077
00779	AMP INC	2800 FULLING MILL PO BOX 3608	HARRISBURG PA 17105
26742	METHODE ELECTRONICS INC	7447 W WILSON AVE	CHICAGO IL 60656–4548
53387	3M COMPANY ELECTRONIC PRODUCTS DIV	3M AUSTIN CENTER	AUSTIN TX 78769–2963
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON OR 97077–0001

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
1–0	010–0581–00			1	ADAPTER,PROBE:68060,PGA–223 SOCKETED	80009	010058100
–1	131–4917–00			4	CONN,HDR:PCB,:MALE,STR,1 X 2,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD,TUBE,HIGH TEMP (J140,J180,J370,J380)	00779	104714–3
–2	131–5267–00			3	CONN,HDR:PCB,:MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD (J130,J150,J300,J310,J379,J400,J410,J460,J470,J480,J620, J640,J650)	53387	2480–6122–TB
–3	131–4356–00			1	CONN,SHUNT:SHUNT/SHORTING,;FEMALE,1 X 2,0.1 CTR, 0.63 H,BLK,W/HANDLE,JUMPER (P680)	26742	9618–302–50
–4	131–4530–00			1	CONN,HDR:PCB,:MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30GOLD,BD RETENTION (J680)	00779	104344–1
–5	671–3393–00			1	CKT BD ASSY:68060,PGA–223 SOCKETED	80009	671339300
–6	136–1279–00			2	SOCKET,PGA:PCB;206 POS,18 X 18,0.1 GENTERS,0.165 H X 0.275 TAIL GOLD/GOLD,LONG TAIL, PAT 1854	80009	136127900
					STANDARD ACCESSORIES		
	070–9823–00			1	MANUAL,TECH:INSTRUCTION,CHIP,DISSASEMBLER, TMS 205	80009	070–9823–00
	070–9803–00			1	MANUAL, TECH:TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070–9803–00
					OPTIONAL ACCESSORIES		
	070–9802–00			1	MANUAL, TECH:BASIC OPS MICRO SUP ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070–9802–00

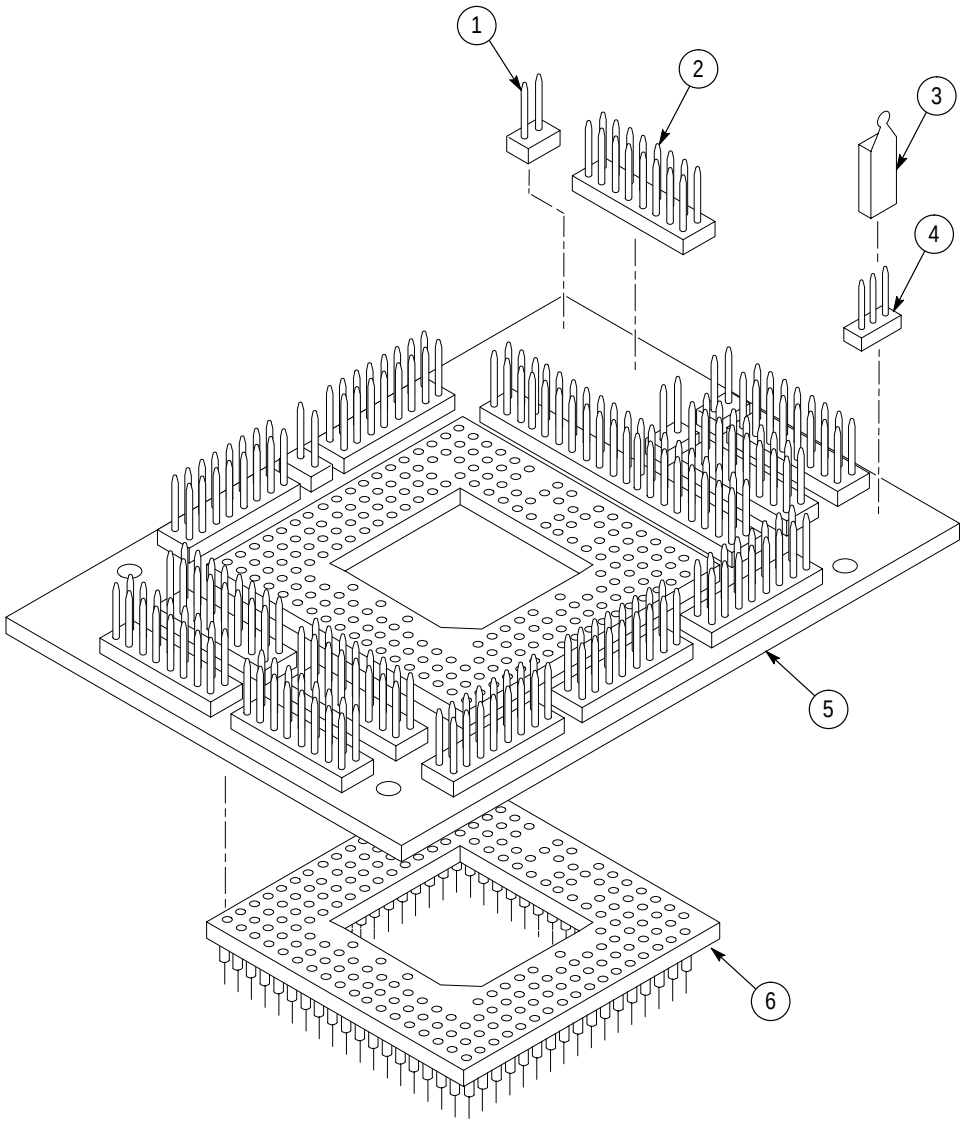


Figure 1: 68060 probe adapter exploded view

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