Instruction Manual

Tektronix

TMS 222
MCF5206/5206E Microprocessor Support

071-0149-01

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Ground the Product. This product is indirectly grounded through the grounding conductor of the mainframe power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface: Microprocessor Support Documentation

This instruction manual contains specific information about the TMS 222 MCF5206 microprocessor support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor support packages on the logic analyzer for which the TMS 222 MCF5206 support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor support packages is included with each product. Each logic analyzer has basic information describing how to perform tasks common to support packages on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to your system under test
- Setting up the logic analyzer to acquire data
- Acquiring and viewing disassembled data

Manual Conventions

This manual uses the following conventions:

The term “disassembler” refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.

The phrase “information on basic operations” refers to online help, an installation manual, or a basic operations of microprocessor supports user manual.

The term “5206” refers to all supported variations of the MCF5206 microprocessor unless otherwise noted.

In the information on basic operations, the term MCF5206 refers to both MCF5206 processor and MCF5206E processor unless stated otherwise.

The term “logic analyzer” refers to the Tektronix logic analyzer for which this product was purchased.

A tilde (~) following a signal name indicates an active low signal.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The manual set provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or, contact us by e-mail: tm_app_supp@tektronix.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Contact your local Tektronix distributor or sales office. Or, visit our web site for a listing of worldwide service locations. www.tektronix.com
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000

Getting Started

Getting Started

This chapter contains information on the TMS 222 microprocessor support, and information on connecting your logic analyzer to your system under test.

Support Description

The TMS 222 microprocessor support package disassembles data from systems that are based on the Motorola MCF5206 and MCF5206E microprocessors.

The TMS 222 supports the MCF5206 and MCF5206E microprocessors in a 160-pin QFP package.

To use this support efficiently, you need to have the items listed in the information on basic operations as well as the *MCF5206 User's Manual*, Motorola, 1995 and the *MCF5206E User's Manual*, Motorola, 1998.

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

For use with a Tektronix logic analyzer (TLA) the TMS 222 support requires a minimum of one 102-channel module.

Requirements And Restrictions

You should review the general requirements and restrictions of microprocessor supports in the information on basic operations as they pertain to your system under test.

You should review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other MCF5206 support requirements and restrictions.

System Clock Rate. The TMS 222 support can acquire data from the MCF5206 microprocessor at speeds of up to 33.33 MHz; it has been tested to 25 MHz and

the MCF5206E microprocessor at speeds of up to 54 MHz; it has been tested to 54 MHz.

This specification is valid at the time this manual was printed. Please contact your Tektronix sales representative for current information on the fastest devices supported.

Hardware Reset. If a hardware reset occurs in your MCF5206 system during an acquisition, the disassembler may acquire an invalid sample.

Disabling The Internal Cache. To disassemble acquired data, you must disable the internal cache. Disabling the cache makes all instruction prefetches visible on the bus so they can be acquired and disassembled.

Big-Endian Byte Ordering. The disassembler always uses Big-Endian byte ordering for instruction disassembly. Big-Endian byte ordering is when the most significant data byte is located at the highest address.

Data Reads And Writes. The disassembler will not link data reads and writes with the instructions which cause them.

Microprocessor Functionality Not Supported

Cache. Cache must be disabled (turned off) for correct disassembly.

Address Hold. Address Hold is not supported for the default memory region.

Alternate Bus Master Cycles. Alternate Bus Master Cycles are not supported.

Configuring The Probe Adapter

Configuring the Chip Select Module Switch. The probe adapter has a DIP switch that must be set according to the chip select module configuration of the MCF5206. Use Table 1–1 to configure the ChipSelect DIP switch. By default, all switches are off.

Table 1–1: DIP switch settings

Switch	Description
S0	CS0~
S1	CS1~
S2	CS2~
S3	CS3~
S4	CS4~
S5	CS5~
S6	CS6~
S7	CS7~

Examples of Switch Settings. The following example shows two possible settings:

- Example 1

  If CS0~, CS1~ and CS2~ are used as ChipSelects, the following configuration would be used:

  S0 – ON (CS0~)
  S1 – ON (CS1~)
  S2 – ON (CS2~)
  S3 – OFF (CS3~)
  S4 – OFF (CS4~)
  S5 – OFF (CS5~)
  S6 – OFF (CS6~)
  S7 – OFF (CS7~)

- Example 2

  If none of the ChipSelects are used, the following configuration would be used:

  S0 – OFF (CS0~)
  S1 – OFF (CS1~)
  S2 – OFF (CS2~)
  S3 – OFF (CS3~)
  S4 – OFF (CS4~)
  S5 – OFF (CS5~)
  S6 – OFF (CS6~)
  S7 – OFF (CS7~)

Connecting To A System Under Test With A Probe Adapter

To connect the logic analyzer to a system under test (SUT) using the probe adapter and test clip, follow these steps:

1. Turn off power to your SUT.

   It is not necessary to turn off the logic analyzer.

CAUTION. *To prevent static damage, handle all the above only in a static-free environment. Static discharge can damage the microprocessor, the probe adapter, the probes, or the module.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the logic analyzer.

Connect The Test Clip To The Probe Adapter

To connect the test clip to the probe adapter follow these steps:

3. Line up pin 1 on the test clip, to pin 1 on the connector located on the bottom of the probe adapter circuit board, as shown in Figure 1–1.

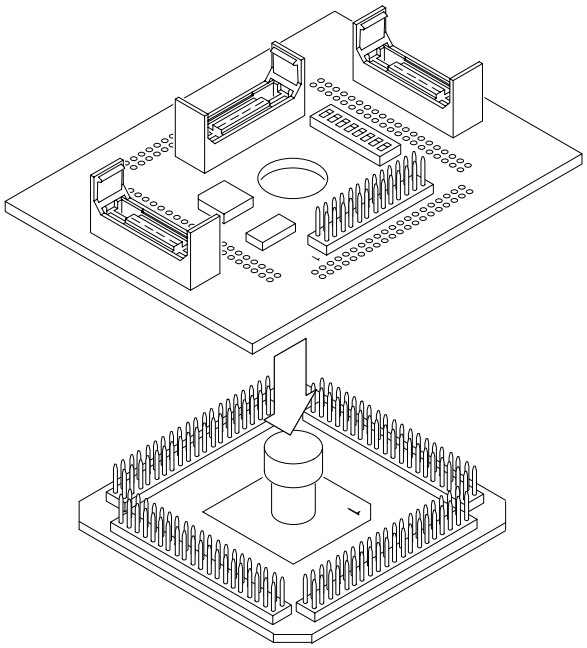


Figure 1–1: Connecting the test clip to the probe adapter

Connect The P6434 Probes To The Probe Adapter

To connect the P6434 probes to the probe adapter follow these steps:

CAUTION. *To prevent damage to the probe and probe adapter, always position the probe perpendicular to the mating connector and gently connect the probe. Incorrect handling of the P6434 probe while connecting it to the probe adapter can result in damage to the probe or to the mating connector on the probe adapter.*

4. Refer to Figure 1–2, and connect the P6434 probes to the probe adapter. Match the channel groups and numbers on the probe labels to the corresponding connectors on the probe adapter.
5. Position the probe tip perpendicular to the mating connector and gently connect the probe as shown in Figure 1–2.
6. When connected, push down the latch releases on the probe to set the latch.

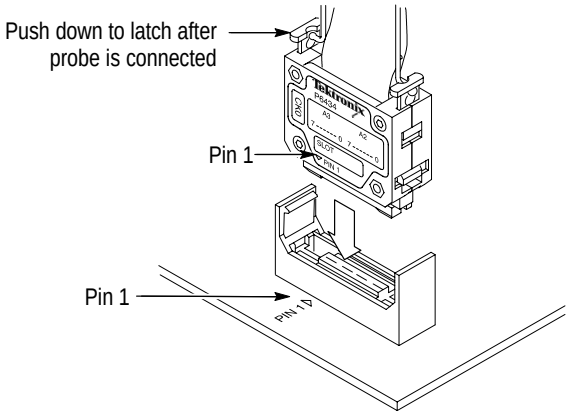


Figure 1–2: Connecting P6434 probes to the probe adapter

Connect The Probe Adapter Assembly To The System Under Test

To connect the probe adapter assembly (probe adapter and test clip) to your SUT follow these instructions:

7. Inspect the microprocessor on your SUT for bent or broken leads. Verify that the leads on the microprocessor are clean and free from dirt, dust, or any foreign material.
8. Inspect the pins of the test clip for bent or broken contacts. Verify that the leads on the test clip are clean and free from dirt, dust or any foreign material.
9. Verify that the locking devise on the test clip is not locked by turning the locking device counter-clockwise.
10. Place the probe adapter onto the SUT as shown in Figure 1–3.

CAUTION. *To prevent damage to electrical components when power is applied, correctly place the probe adapter onto the microprocessor..*

Center the clip on the microprocessor and apply an equal downward force on all four sides of the clip. It is important to keep the QFP test clip parallel to the microprocessor to avoid damage to the SUT or QFP test clip.

Do not apply leverage to the probe adapter when installing or removing it.

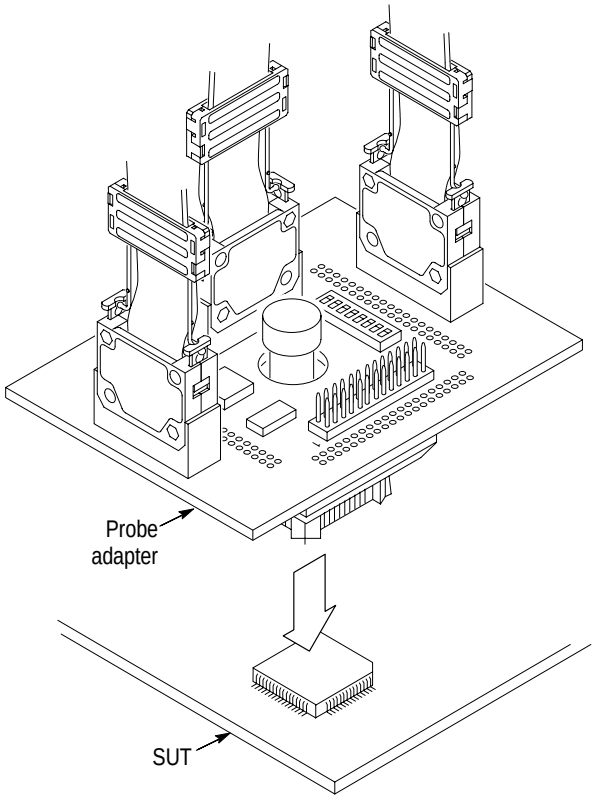


Figure 1–3: Placing the probe adapter onto the SUT

11. Lock the test clip to the microprocessor by turning the locking knob clockwise.

CAUTION. *To prevent faulty and unreliable connections, it is HIGHLY recommended that the test clip IS NOT used on any other microprocessor then the one it was originally connected to.*

The test clip was designed to be used on one and only one microprocessor. Because of the tight tolerances required for QFP test clip connectivity, the test clip that attaches to the microprocessor has a soft plastic collar that conforms to the unique shape of the target microprocessor.

The test clip has a manufacturers stated life expectancy of 8–10 connections.

CAUTION. *The probe adapter board might slip off or slip to one side of the microprocessor because of the extra weight of the probes. This can damage the microprocessor and the SUT.*

To prevent this from occurring, stabilize the probe adapter by placing a non-conductive object (such as non-conductive foam) between the probe adapter and the SUT.

Removing The Probe Adapter From The SUT

To remove the probe adapter from the SUT follow these steps:

1. Unlock the test clip from the microprocessor by turning the locking knob counter-clockwise.
2. Gently lift and pull the probe adapter off of the microprocessor.

Connecting To A System Under Test Without A Probe Adapter

You can use the channel and clock probes and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your SUT. To connect probes to MCF5206 signals in the SUT using a test clip, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from it.
3. Table 1–2 through Table 1–8 lists the channel probes the MCF5206 signal pins on the test clip or in the SUT to connect to.

   Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip.
4. Align pin 1 or A1 of your test clip with the corresponding pin 1 or A1 of the MCF5206 microprocessor in your SUT and attach the clip.

Channel Assignments

The following channel assignment tables show the probe section and channel assignments, and the signal to which each channel connects.

Channel assignments shown in Table 1–2 through Table 1–8 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- A tilde (~) following a signal name indicates an active low signal.

By default, the Address group is displayed in hexadecimal.

Table 1–2: Address group channel assignments

Bit order	Section:channel	MCF5206 signal name
31	A3:7	CS3~
30	A3:6	CS2~
29	A3:5	CS1~
28	A3:4	CS0~
27	A3:3	A27
26	A3:2	A26
25	A3:1	A25
24	A3:0	A24
23	A2:7	A23
22	A2:6	A22
21	A2:5	A21
20	A2:4	A20
19	A2:3	A19
18	A2:2	A18
17	A2:1	A17
16	A2:0	A16

Table 1–2: Address group channel assignments (cont.)

Bit order	Section:channel	MCF5206 signal name
15	A1:7	A15
14	A1:6	A14
13	A1:5	A13
12	A1:4	A12
11	A1:3	A11
10	A1:2	A10
9	A1:1	A9
8	A1:0	A8
7	A0:7	A7
6	A0:6	A6
5	A0:5	A5
4	A0:4	A4
3	A0:3	A3
2	A0:2	A2
1	A0:1	A1
0	A0:0	A0

By default, the Data group is displayed in hexadecimal.

Table 1–3: Data group channel assignments

Bit order	Section:channel	MCF5206 signal name
31	D3:7	D31
30	D3:6	D30
29	D3:5	D29
28	D3:4	D28
27	D3:3	D27
26	D3:2	D26
25	D3:1	D25
24	D3:0	D24
23	D2:7	D23
22	D2:6	D22
21	D2:5	D21
20	D2:4	D20
19	D2:3	D19
18	D2:2	D18

Table 1–3: Data group channel assignments (cont.)

Bit order	Section:channel	MCF5206 signal name
17	D2:1	D17
16	D2:0	D16
15	D1:7	D15
14	D1:6	D14
13	D1:5	D13
12	D1:4	D12
11	D1:3	D11
10	D1:2	D10
9	D1:1	D9
8	D1:0	D8
7	D0:7	D7
6	D0:6	D6
5	D0:5	D5
4	D0:4	D4
3	D0:3	D3
2	D0:2	D2
1	D0:1	D1
0	D0:0	D0

By default, the Control group is displayed symbolically. The symbol table file name is 5206_Ctrl.

Table 1–4: Control group channel assignments

Bit order	Section:channel	MCF5206 signal name
13	C2:3	TS~
12	C2:2	D_RAS~ †
11	C2:0	D_CAS~ †
10	C2:7	ATM
9	C1:6	ATM=
8	C1:3	R/W~
7	C1:7	DRAMW~
6	C1:5	TT1
5	C1:4	TT0
4	C1:2	BG~
3	C1:1	BD~

Table 1–4: Control group channel assignments (cont.)

Bit order	Section:channel	MCF5206 signal name
2	C3:1	TEA~
1	C0:6	RSTI~
0	C0:4	HIZ~

= **Double probe.**

† **Signal derived on the probe adapter.**

By default, the DataSize group is displayed symbolically. The symbol table file name is 5206_Dsiz.

Table 1–5: DataSize group channel assignments

Bit order	Section:channel	MCF5206 signal name
1	C3:7	SIZ1
0	C3:3	SIZ0

By default, the DramEnbl group is not visible.

Table 1–6: DramEnbl group channel assignments

Bit order	Section:channel	MCF5206 signal name
5	C3:6	RAS1~
4	C2:6	CAS3~
3	C3:4	CAS2~
2	C3:2	RAS0~
1	C3:0	CAS1~
0	C2:4	CAS0~

By default, the radix of the Misc group is OFF.

Table 1–7: Misc group channel assignments

Bit order	Section:channel	MCF5206 signal name
4	C3:5	TA~
3	C2:5	ATA~
2	C2:1	D_CS~ †
1	C1:0	BR~

Table 1–7: Misc group channel assignments (cont.)

Bit order	Section:channel	MCF5206 signal name
0	C0:7	CLK

† **Signal derived on the probe adapter.**

Table 1–8 lists the probe section and channel assignments for the clock probes. The clock probes are not part of any group.

Table 1–8: Clock channel assignments

Section:channel	MCF5206 signal name
CK:3	CLK=
CK:2	A2=
CK:1	A1=
CK:0	A0=
C2:3	TS~
C2:2	D_RAS~ †
C2:1	D_CS~ †
C2:0	D_CAS~ †
QUAL:1	NC
QUAL:0	NC

= **Doubled probe.**

† **Signal derived on the probe adapter.**

Table 1–9 lists the pinout of J136, the BDM (Background Debug Mode) connector.

Table 1–9: BDM connector pinout

MCF5206 signal name	J136 BDM connector pin number
NC (Developer Reserved)	1
TMS/BKPT~	2
GND	3
TRST~/DSCLK	4
GND	5
NC (Developer Reserved)	6

Table 1–9: BDM connector pinout (cont.)

MCF5206 signal name	J136 BDM connector pin number
RSTI~	7
TDI/DSI	8
+5V §	9
TDO/DSO	10
GND	11
PP7/PST3	12
PP6/PST2	13
PP5/PST1	14
PP4/PST0	15
PP3/DDATA3	16
PP2/DDATA2	17
PP1/DDATA1	18
PP0/DDATA0	19
GND	20
NC (Motorola Reserved)	21
NC (Motorola Reserved)	22
GND	23
CLK	24
VCC §	25
TEA~	26

§ **Supplied by the target. If the SUT can supply this voltage, then pin-9 on the BDM connector may be connected to pin-25 on the BDM connector. Otherwise an external +5V supply must be used to connect +5V to pin-9.**

CPU To Mictor Connections

To probe the microprocessor, you will need to make connections between the CPU and the Mictor pins of the P6434 Mass Termination Probe. Refer to the *P6434 Mass Termination Probe* manual, Tektronix part number 070-9793-XX, for more information on mechanical specifications. Tables 1–10 through 1–12 show the CPU pin to Mictor pin connections.

Tektronix uses a counterclockwise pin assignment. Pin 1 is located at the top left, and pin 2 is located directly below it. Pin 20 is located on the bottom right, and pin 21 is located directly above it (see Figure1–4).

AMP uses an odd side-even side pin assignment. Pin 1 is located at the top left, and pin 3 is located directly below it. Pin 2 is located on the top right, and pin 4 is located directly below it (see Figure1–4).

NOTE. *When designing Mictor connectors into your system under test, always follow the Tektronix pin assignment.*

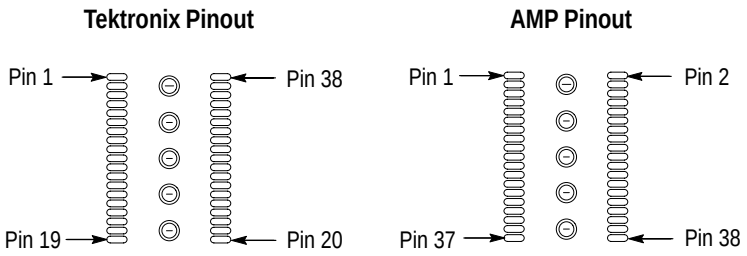


Figure 1–4: Pin assignments for a Mictor connector (component side)

Table 1–10: CPU to Mictor connections for Mictor A pins

Tektronix Mictor A pin number	AMP Mictor A pin number	LA channel	MCF5206 signal name	MCF5206 pin number
1	1	NC	NC	NC
2	3	NC	NC	NC
3	5	CLOCK:0	A0=	1
4	7	A3:7	CS3~	46
5	9	A3:6	CS2~	45
6	11	A3:5	CS1~	43
7	13	A3:4	CS0~	42
8	15	A3:3	A27	41
9	17	A3:2	A26	40
10	19	A3:1	A25	38
11	21	A3:0	A24	37
12	23	A2:7	A23	35
13	25	A2:6	A22	34
14	27	A2:5	A21	32
15	29	A2:4	A20	31
16	31	A2:3	A19	29
17	33	A2:2	A18	28

Table 1–10: CPU to Mictor connections for Mictor A pins (cont.)

Tektronix Mictor A pin number	AMP Mictor A pin number	LA channel	MCF5206 signal name	MCF5206 pin number
18	35	A2:1	A17	26
19	37	A2:0	A16	25
20	38	A0:0	A0	1
21	36	A0:1	A1	2
22	34	A0:2	A2	4
23	32	A0:3	A3	5
24	30	A0:4	A4	7
25	28	A0:5	A5	8
26	26	A0:6	A6	10
27	24	A0:7	A7	11
28	22	A1:0	A8	13
29	20	A1:1	A9	14
30	18	A1:2	A10	16
31	16	A1:3	A11	17
32	14	A1:4	A12	19
33	12	A1:5	A13	20
34	10	A1:6	A14	22
35	8	A1:7	A15	23
36	6	CLOCK:1	A1=	2
37	4	NC	NC	NC
38	2	NC	NC	NC
39	39	GND	GND	NC
40	40	GND	GND	NC
41	41	GND	GND	NC
42	42	GND	GND	NC
43	43	GND	GND	NC

= Double probe

Table 1–11: CPU to Mictor connections for Mictor C pins

Tektronix Mictor C pin number	AMP Mictor A pin number	LA channel	MCF5206 signal name	MCF5206 pin number
1	1	NC	NC	NC
2	3	NC	NC	NC
3	5	CLOCK:3	CLK=	135
4	7	C3:7	SIZ1	53
5	9	C3:6	RAS1~	71
6	11	C3:5	TA~	55
7	13	C3:4	CAS2~	75
8	15	C3:3	SIZ0	51
9	17	C3:2	RAS0~	70
10	19	C3:1	TEA~	57
11	21	C3:0	CAS1~	74
12	23	C2:7	ATM	50
13	25	C2:6	CAS3~	76
14	27	C2:5	ATA~	61
15	29	C2:4	CAS0~	72
16	31	C2:3	TS~	58
17	33	C2:2	D_RAS~	NC
18	35	C2:1	D_CS~	NC
19	37	C2:0	D_CAS~	NC
20	38	C0:0	NC	NC
21	36	C0:1	NC	NC
22	34	C0:2	NC	NC
23	32	C0:3	NC	NC
24	30	C0:4	HIZ~	125
25	28	C0:5	RTS2/RSTO~	133
26	26	C0:6	RSTI~	59
27	24	C0:7	CLK	135
28	22	C1:0	BR~	66
29	20	C1:1	BD~	67
30	18	C1:2	BG~	68
31	16	C1:3	R/W~	54
32	14	C1:4	TT0	47
33	12	C1:5	TT1	49
34	10	C1:6	ATM=	50
35	8	C1:7	DRAMW~	78

Table 1–11: CPU to Mictor connections for Mictor C pins (cont.)

Tektronix Mictor C pin number	AMP Mictor A pin number	LA channel	MCF5206 signal name	MCF5206 pin number
36	6	NC	NC	NC
37	4	NC	NC	NC
38	2	NC	NC	NC
39	39	GND	GND	NC
40	40	GND	GND	NC
41	41	GND	GND	NC
42	42	GND	GND	NC
43	43	GND	GND	NC

= Double probe

Table 1–12: CPU to Mictor connections for Mictor D pins

Tektronix Mictor D pin number	AMP Mictor A pin number	LA channel	MCF5206 signal name	MCF5206 pin number
1	1	NC	NC	NC
2	3	NC	NC	NC
3	5	NC	NC	NC
4	7	D3:7	D31	79
5	9	D3:6	D30	80
6	11	D3:5	D29	81
7	13	D3:4	D28	83
8	15	D3:3	D27	84
9	17	D3:2	D26	85
10	19	D3:1	D25	87
11	21	D3:0	D24	88
12	23	D2:7	D23	89
13	25	D2:6	D22	91
14	27	D2:5	D21	92
15	29	D2:4	D20	93
16	31	D2:3	D19	95
17	33	D2:2	D18	96
18	35	D2:1	D17	97
19	37	D2:0	D16	99

Table 1–12: CPU to Mictor connections for Mictor D pins (cont.)

Tektronix Mictor D pin number	AMP Mictor A pin number	LA channel	MCF5206 signal name	MCF5206 pin number
20	38	D0:0	D0	120
21	36	D0:1	D1	119
22	34	D0:2	D2	117
23	32	D0:3	D3	116
24	30	D0:4	D4	115
25	28	D0:5	D5	113
26	26	D0:6	D6	112
27	24	D0:7	D7	111
28	22	D1:0	D8	109
29	20	D1:1	D9	108
30	18	D1:2	D10	107
31	16	D1:3	D11	105
32	14	D1:4	D12	104
33	12	D1:5	D13	103
34	10	D1:6	D14	101
35	8	D1:7	D15	100
36	6	CLOCK:2	A2=	4
37	4	NC	NC	NC
38	2	NC	NC	NC
39	39	GND	GND	NC
40	40	GND	GND	NC
41	41	GND	GND	NC
42	42	GND	GND	NC
43	43	GND	GND	NC

= Double probe

Table 1–13 lists the MCF5206 signals that are not required by the Clocking State Machine (CSM) or the disassembler. The signals that are not required can be removed from their default connections and re-connected to other signals of interest. This is not possible with Mictor connectors on the probe adapter.

Table 1–13: Signals not required for clocking or disassembly

Section:channel	MCF5206 signal name
C3:5	TA~
C3:4	CAS2~
C3:0	CAS1~
C2:6	CAS3~
C2:5	ATA~
C2:4	CAS0~
C1:0	BR~
C0:7	CLK
C0:5	RTS2/RSTO~

Operating Basics

Setting Up the Support

The information in this section is specific to the operations and functions of the TMS 222 MCF5206 support on any Tektronix logic analyzer for which it can be purchased.

Before you acquire and disassemble data, you need to load the support and specify setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Groups

The software automatically defines channel groups for the support. The channel groups for the TMS 222 MCF5206 support are listed in the channel assignment tables beginning on page 1–9.

Custom Clocking

A special clocking program is loaded to the module every time the TMS 222 support is loaded. When “Custom” is selected, the sub-title “MCF5206 Microprocessor Clocking Support” will be added, and the clocking options will be displayed.

Clocking Options

The TMS 222 support has one mode of acquisition clocking called “DRAM TYPE”.

If the DRAM memory is Extended Data out (EDO) type the option “EDO DRAM” is selected.

If the DRAM memory is not Extend Data out (EDO) type the option “NON EDO DRAM” is selected as the default.

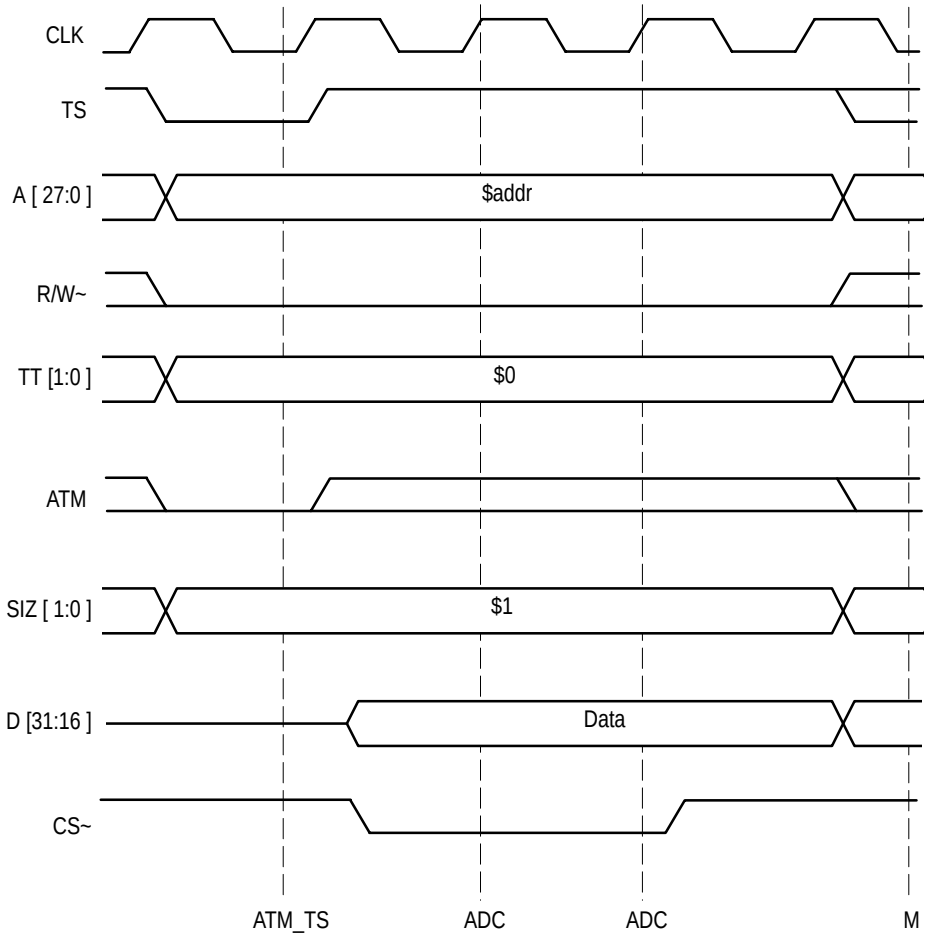


Figure 2–1: Byte Write Transfer from an 8-bit port.

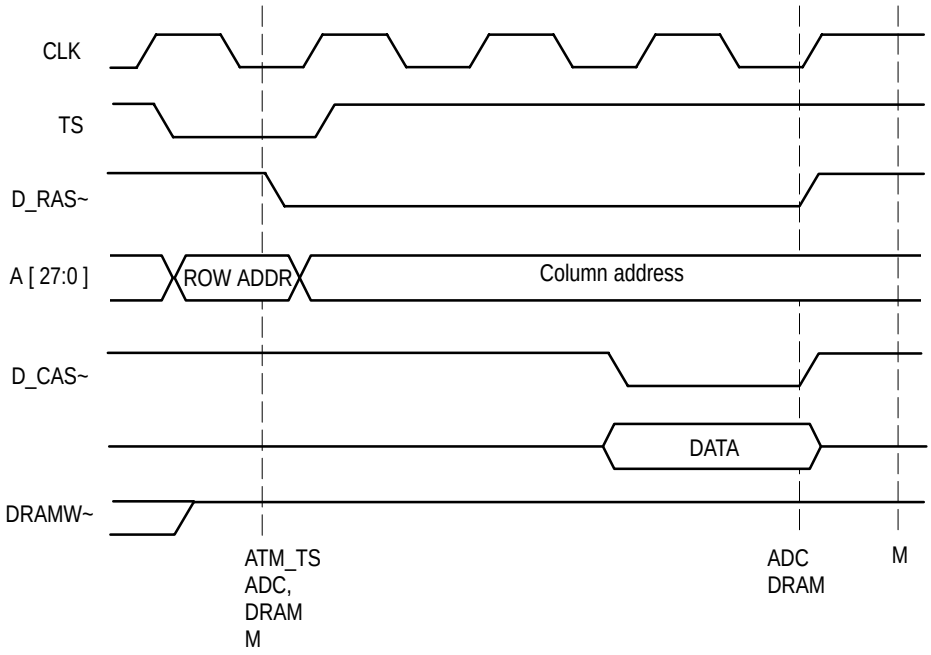


Figure 2–2: Byte Read transfer in normal mode with 8-bit NON EDO Dram

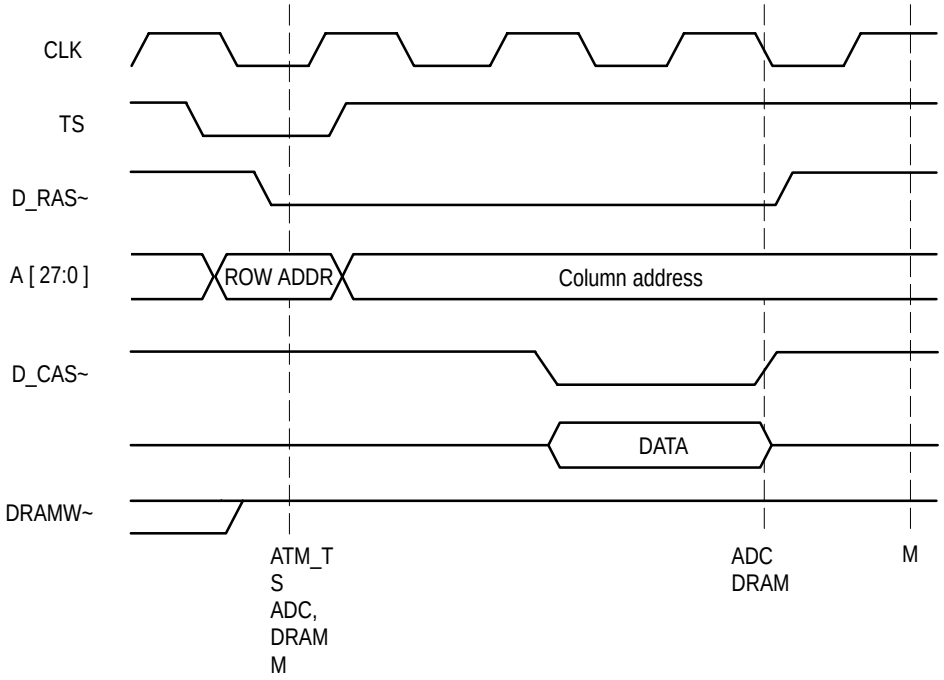


Figure 2–3: Byte Read transfer in normal mode with 8-bit EDO Dram

Symbols

The TMS 222 support supplies symbol table files. Each file replaces specific channel group values with symbolic values when Symbolic is the radix for the channel group.

Symbol tables are generally not for use in timing or 5206_T support disassembly.

Table 2–1 lists the name and bit pattern for the symbols in the file 5206_Ctrl, the Control channel group symbol table.

Table 2–1: Control group symbol table definitions

	Control group value			
	D_CAS~	DRAMW~	BD~	
	ATM	TT1	TEA~	
	TS~	ATM=	TT0	RSTI~
Symbol	D_RAS~	R/W~	BG~	HIZ~
MASTER RESET	X X	X X X X	X X X X	X X 0 0
NORMAL RESET	X X	X X X X	X X X X	X X 0 1
ALTERNATE BUS MASTER	X X	X X X X	X X X X	1 X 1 1
TRANSFER ERROR	X X	X X X X	X X X X	X 0 1 1
DRAM ROW ADDRESS	X 0	1 X X X	X X X X	0 1 1 1
SUP CODE	0 1	1 1 1 1	X 0 0 X	0 1 1 1
FETCH/READ	1 1	1 X X 1	X 0 0 X	0 1 1 1
DRAM SUP CODE	0 X	0 1 1 X	1 0 0 X	0 1 1 1
DRAM FETCH/READ	1 X	0 X X X	1 0 0 X	0 1 1 1
SUP CODE – DEBUG	0 1	1 1 1 1	X 1 0 X	0 1 1 1
FETCH/READ – DEBUG	1 1	1 X X 1	X 1 0 X	0 1 1 1
DRAM SUP CODE – DEBUG	0 X	0 1 1 X	1 1 0 X	0 1 1 1
DRAM FETCH/READ – DEBUG	1 X	0 X X X	1 1 0 X	0 1 1 1
SUP READ	0 1	1 0 1 1	X 0 0 X	0 1 1 1
DRAM SUP READ	0 X	0 0 1 X	1 0 0 X	0 1 1 1
SUP READ – DEBUG	0 1	1 0 1 1	X 1 0 X	0 1 1 1
DRAM SUP READ – DEBUG	0 X	0 0 1 X	1 1 0 X	0 1 1 1
SUP WRITE	0 1	1 0 1 0	X 0 0 X	0 1 1 1
WRITE	1 1	1 X X 0	X 0 0 X	0 1 1 1
DRAM SUP WRITE	0 X	0 0 1 X	0 0 0 X	0 1 1 1
DRAM WRITE	1 X	0 X X X	0 0 0 X	0 1 1 1
SUP WRITE – DEBUG	0 1	1 0 1 0	X 1 0 X	0 1 1 1
WRITE – DEBUG	1 1	1 X X 0	X 1 0 X	0 1 1 1
DRAM SUP WRITE – DEBUG	0 X	0 0 1 X	0 1 0 X	0 1 1 1

Table 2–1: Control group symbol table definitions (cont.)

Symbol	Control group value															
	TS~	D_RAS~	D_CAS~	ATM	ATM=	R/W~	DRAMW~	TT1	TT0	BG~	BD~	TEA~	RSTI~	HIZ~		
DRAM WRITE – DEBUG	1	X	0	X	X	X	0	1	0	X	0	1	1	1		
USER CODE	0	1	1	1	0	1	X	0	0	X	0	1	1	1		
DRAM USER CODE	0	X	0	1	0	X	1	0	0	X	0	1	1	1		
USER CODE – DEBUG	0	1	1	1	0	1	X	1	0	X	0	1	1	1		
DRAM USER CODE – DEBUG	0	X	0	1	0	X	1	1	0	X	0	1	1	1		
USER READ	0	1	1	0	0	1	X	0	0	X	0	1	1	1		
DRAM USER READ	0	X	0	0	0	X	1	0	0	X	0	1	1	1		
USER READ – DEBUG	0	1	1	0	0	1	X	1	0	X	0	1	1	1		
DRAM USER READ – DEBUG	0	X	0	0	0	X	1	1	0	X	0	1	1	1		
USER WRITE	0	1	1	0	0	0	X	0	0	X	0	1	1	1		
DRAM USER WRITE	0	X	0	0	0	X	0	0	0	X	0	1	1	1		
USER WRITE – DEBUG	0	1	1	0	0	0	X	1	0	X	0	1	1	1		
DRAM USER WRITE– DEBUG	0	X	0	0	0	X	0	1	0	X	0	1	1	1		
MOVEC INST READ	0	1	1	0	0	1	X	1	1	X	0	1	1	1		
DRAM MOVEC INST READ	0	X	0	0	0	X	1	1	1	X	0	1	1	1		
uP SPACE/ACK.	1	1	1	X	X	1	X	1	1	X	0	1	1	1		
DRAM uP SPACE/ACK.	1	X	0	X	X	X	1	1	1	X	0	1	1	1		
MOVEC INST WRITE	0	1	1	0	0	0	X	1	1	X	0	1	1	1		
DRAM MOVEC INST WRITE	0	X	0	0	0	X	0	1	1	X	0	1	1	1		
WRITE – uP SPACE/ACK.	1	1	1	X	X	0	X	1	1	X	0	1	1	1		
DRAM WRITE – uP SPACE/ACK.	1	X	0	X	X	X	0	1	1	X	0	1	1	1		
READ – ACK.	0	1	1	1	0	1	X	1	1	X	0	1	1	1		
DRAM READ – ACK.	0	X	0	1	0	X	0	1	1	X	0	1	1	1		
WRITE – ACK.	0	1	1	1	0	0	X	1	1	X	0	1	1	1		
DRAM WRITE – ACK.	0	X	0	1	0	X	0	1	1	X	0	1	1	1		
RESERVED ACCESS	X	X	X	X	X	X	X	0	1	X	0	1	1	1		

Table 2–2 lists the name and bit pattern for the file 5206_Dsiz, and the symbols in the DataSize group symbol table.

Table 2–2: DataSize group symbol table definitions

	DataSize group value
Symbol	**SIZ1 SIZ0**
LONG	0 0
BYTE	0 1
WORD	1 0
LINE	1 1

Acquiring And Viewing Disassembled Data

Acquiring Data

Once you load the MCF5206 support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual.

Viewing Disassembled Data

You can view disassembled data in six display formats: Timing, State, Hardware, Software, Control Flow, and Subroutine.

The information on basic operations describes how to select the disassembly display formats.

NOTE. *Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–12.*

The default display format shows the Address, Data, and Control channel group values for each sample of acquired data.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–3 shows these special characters and strings, and gives a description of what they represent.

Table 2–3: Description of special characters in the display

Character or string displayed	Description
>>	The instruction was manually marked as a program fetch
****	Indicates there is insufficient data available for complete disassembly of the instruction: the number of asterisks indicates the width of the data that is unavailable. Each two asterisks represent one byte.
#	Indicates an immediate value
t	Indicates the number shown is in decimal, such as #12t

Timing Display Format

A Timing-Waveform display file format is provided with this support. The Timing-Waveform display file format will set up the display and show the following waveforms:

CLK	TS~	Address (busform)
Data (busform)	D_RAS~	D_CAS~
D_CS~	DataSize (busform)	ATM
R/W~	DRAMW~	TT1
TT0	BR~	BG~
BD~	TEA~	RSTI~
HIZ~	TA~	ATA~

State Display Format

In State-Listing display, all bus cycles are displayed, but not disassembled.

Except for the group name, default group order, and default radix, the State-Listing display is unaffected by the support software.

Data searching (not microprocessor-specific instruction) is supported by the State-Listing display

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–4 shows these cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled with the vector name.

Table 2–4: Cycle type definitions

Cycle type label	Definition
(MASTER RESET)	Master Reset of the microprocessor
(NORMAL RESET)	Normal Reset of the microprocessor
(ALTERNATE BUS MASTER)	Alternate Bus Master cycle
(TRANSFER ERROR)	Transfer Error
(DRAM ROW ADDRESS)	DRAM Row Address
(SUP CODE)	Code
(FETCH/READ)	Code/Data
(DRAM SUP CODE)	DRAM Supervisor Code
(DRAM FETCH/READ)	DRAM Code/READ
(SUP CODE – DEBUG)	Supervisor Code in Debug Mode
(FETCH/READ – DEBUG)	Code/Data in Debug mode
(DRAM SUP CODE – DEBUG)	DRAM Supervisor code in Debug mode
(DRAM FETCH/READ – DEBUG)	DRAM Code/Data in Dbug mode

Table 2–4: Cycle type definitions (cont.)

Cycle type label	Definition
(SUP READ)	Supervisor Data DataRead
(DRAM SUP READ)	DRAM Supervisor Data Read
(SUP READ – DEBUG)	Supervisor Data Read in Debug mode
(DRAM SUP READ – DEBUG)	DRAM Supervisor Data Read in Debug mode
(SUP WRITE)	Supervisor Data Write
(WRITE)	Data Write
(DRAM SUP WRITE)	DRAM Supervisor Data Write
(DRAM WRITE)	DRAM Data Write
(SUP WRITE – DEBUG)	Supervisor Data Write in Debug mode
(WRITE – DEBUG)	Data Write in Debug mode
(DRAM SUP WRITE – DEBUG)	DRAM Supervisor Data Write in Debug mode
(DRAM WRITE – DEBUG)	DRAM Data Write in Debug mode
(USER CODE)	User Code
(DRAM USER CODE)	DRAM User Code
(USER CODE – DEBUG)	User Code in Debug mode
(DRAM USER CODE – DEBUG)	DRAM User Code in Debug mode
(USER READ)	User Data Read
(DRAM USER READ)	DRAM User Data Read
(USER READ – DEBUG)	User Data Read in Debug mode
(DRAM USER READ – DEBUG)	DRAM User Data Read in Debug mode
(USER WRITE)	User Data Write
(DRAM USER WRITE)	DRAM User Data Write
(USER WRITE – DEBUG)	User Data Write in Debug mode
(DRAM USER WRITE – DEBUG)	DRAM User Data Write in Debug mode
(MOVEC INST READ)	Movec Instruction Data Read
(DRAM MOVEC INST READ)	DRAM Movec Instruction Data Read
(uP SPACE/ACK)	CPU space/Intruupt Acknowledge
(DRAM uP SPACE/ACK)	CPU space/Interrupt Acknowledge
(MOVEC INST WRITE)	Movec Instruction Write
(DRAM MOVEC INST WRITE)	DRAM Movec Instruction Write
(WRITE – uP SPACE/ACK)	Write CPU space/Interrupt Acknowledge
(DRAM WRITE – uP SPACE/ACK)	DRAM Write CPU space/Interrupt Acknowledge
(READ – ACK)	Data Read / Interrupt Acknowledge

Table 2–4: Cycle type definitions (cont.)

Cycle type label	Definition
(DRAM READ – ACK)	DRAM Data Read / Interrupt Acknowledge
(WRITE – ACK)	Data Write / Interrupt Acknowledge
(DRAM WRITE – ACK)	DRAM Data Write / Interrupt Acknowledge
(RESERVED ACCESS)	Reserved access
(UNKNOWN)	The combination of control bits unrecognized
(EXTENSION) §	Extension part of the Instruction
(FLUSH) §	Instruction Fetch not executed
(READ) §	Data Read

§ **Computed cycle types.**

Figure 2–4 shows an example of the Hardware display.

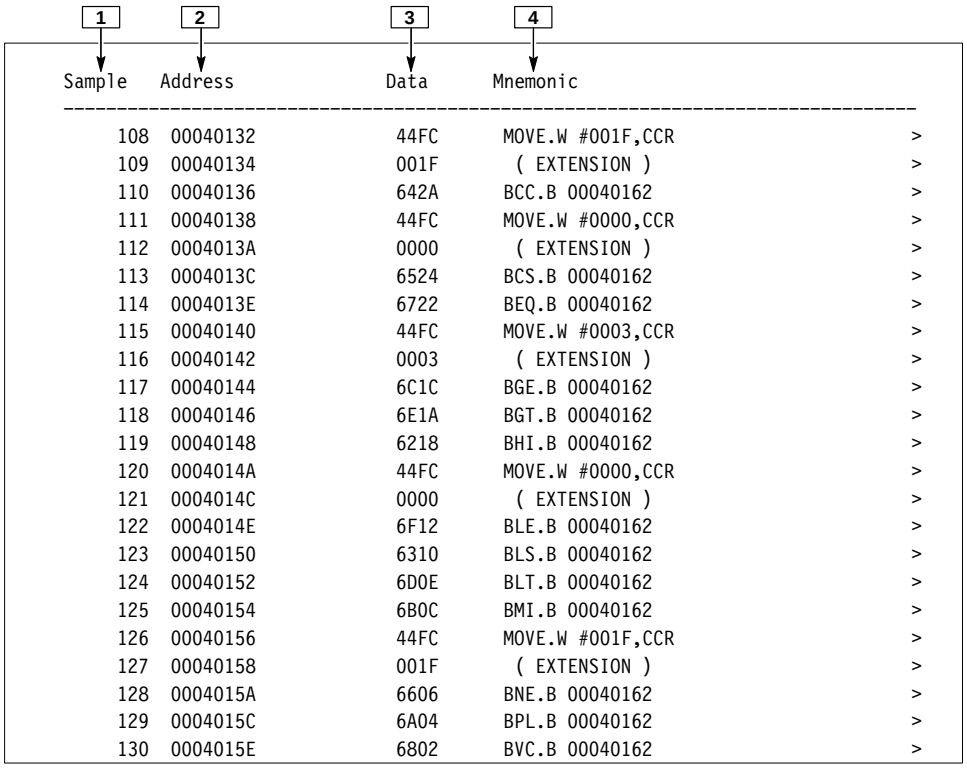


Figure 2–4: Hardware display format

1 **Sample Column.** Lists the memory locations for the acquired data.

2 **Address Group.** Lists data from channels connected to the MCF5206 address bus.

3 **Data Group.** Lists data from channels connected to the MCF5206 data bus.

4 **Mnemonics Column.** Lists the disassembled instructions and cycle types.

Software Display Format

The Software display format shows only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Read extensions will be used to disassemble the instruction, but will not be displayed as a separate cycle in the Software display format. Data reads and writes are not displayed.

Control Flow Display Format

The Control Flow display format shows only the first opcode fetch of instructions that cause a branch in the addressing will be displayed.

If a conditional branch branches to an address that is reaches sequentially, it might be impossible to determine if the branch was taken or not taken. In this instance the branch will not be displayed in the Control Flow display, and no flushing will be done.

Unconditional branches are always displayed whether or not the destination address is seen on the bus.

Instructions that unconditionally generate a change in the flow of control in the MCF5206 microprocessor are:

BRA	BSR	JMP	JSR
RTE	RTS	STOP	TRAP

Instructions that conditionally generate a change in the flow of control in the MCF5206 microprocessor are:

Bcc

Subroutine Display Format

The Subroutine display format shows only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

Instructions that unconditionally generate a subroutine call or a return in the MCF5206 microprocessor are:

BSR	JSR	RTE
RTS	STOP	TRAP

The following special cycles will also be displayed:

- Bus Error Cycles
- Reads from the interrupt table that appear due to servicing interrupts will be displayed (VBR must be set in the format overlay)
- Illegal instructions will be displayed
- (UNKNOWN) cycle types – the disassembler does not recognize the control group value

Signals On The Probe Adapter But Not Acquired

The following signals are present on the probe adapter, but not acquired by the disassembler software:

IRQ7~/IPL2~	IRQ4~/IPL1~	IRQ1~/IPLO~	TDI/DSI
TCK	TDO/DSO	SCL	TRST~/DSCLK
CTS2~	RXD2	TXD2	SDA
CTS1~	RXD1	TXD1	RTS1~
TIN0	TIN1	TOUT0	TOUT1
PP7/PST3	PP6/PST2	PP5/PST1	PP4/PST0
PP3/DDATA3	PP2/DDATA2	PP1/DDATA1	PP0/DDATA0
TMS/BKPT~	MTMOD		

To view these signals, an alternate probing method must be used.

Changing How Data is Displayed

There are common fields and features that allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

You can make selections unique to the MCF5206 support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception vectors

Disassembly Display Options

The TLA 700 Series supports the following disassembly display options:

- Show: Hardware (default), Software, Control Flow, Subroutine
- Highlight: Software (default), Control Flow, Subroutine, None

Optional Display Selections

The fields corresponding to the CS[0-7]~ Base Addresses and the DRAM Bank1 and Bank0 base addresses appear to be different on the TLA 700 Series then on the DAS 9200 Series because the TLA 700 Series has a user interface that can accommodate more than 13 fields.

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations), you can configure the data display for the following microprocessor specific fields:

Write Enable, Chip Select, or Address Line. Table 2–5 lists the configuration options for configuring the pins as address pins, chip select pins, or write enable pins.

The selections are:

W,W,W,W	W,W,C,C	W,W,C,A	W,W,A,A
W,C,C,C	W,C,C,A	W,C,A,A	W,A,A,A
C,C,C,C	C,C,A,A	C,A,A,A	A,A,A,A

Where:

W	the pin is used as a write enable
C	the pin is used as a chip select
A	the pin is used as an address line

Table 2–5: Address, Chip Select, or Write Enable Matrix

PAR[3-0]	A27/CS7/WE0	A26/CS6/WE1	A25/CS5/WE2	A24/CS4/WE3
0000	WE0	WE1	WE2	WE3
0001	WE0	WE1	CS5	CS4
0010	WE0	WE1	CS5	A24
0011	WE0	WE1	A25	A24
0100	WE0	CS6	CS5	CS4
0101	WE0	CS6	CS5	A24

Table 2–5: Address, Chip Select, or Write Enable Matrix (cont.)

PAR[3-0]	A27/CS7/WE0	A26/CS6/WE1	A25/CS5/WE2	A24/CS4/WE3
0110	WE0	CS6	A25	A24
0111	WE0	A26	A25	A24
1000	CS7	CS6	CS5	CS4
1001	CS7	CS6	CS5	A24
1010	CS7	CS6	A25	A24
1011	CS7	A26	A25	A24
1100	A27	A26	A25	A24
1101	Reserved			
1110	Reserved			
1111	Reserved			

DefaultMem Port Size. The DefaultMem Port Size selection indicates the port size of the default memory region. Select one of the following options:

32-bit
8-bit
16-bit

Bank0 Page, Port Size. There are nine different DRAM PortSize and PageSize combinations available. The combinations are listed for DRAM Bank0. Select one of the following selections:

512 Byte,32-bit
512 Byte,16-bit
512 Byte,8-bit
1 KB,32-bit
1 KB,16-bit
1 KB,8-bit
2 KB,32-bit
2 KB,16-bit
2 KB,8-bit

Bank1 Page, Port Size. There are nine different DRAM PortSize and PageSize combinations available. The combinations are listed for DRAM Bank1. Select one of the following selections:

512 Byte,32-bit
512 Byte,16-bit
512 Byte,8-bit
1 KB,32-bit
1 KB,16-bit
1 KB,8-bit
2 KB,32-bit
2 KB,16-bit
2 KB,8-bit

Bank[1-0] BaseAddr. This is a eight digit hexadecimal fill-in field. Enter the base address of the region controlled by RAS1~ and RAS0~ chip enables here.

The first four digits constitute the most significant 16-bits of the RAS1~ base address, and the next four digits constitute the most significant 16-bits of the RAS0~ base address.

NOTE. *For the BaseAddr fields only the most significant 16-bits matter. Bits 15-0 are taken to be zeroes.*

VBR. The TMS 222 will support interpretation of accesses to the vector table by labeling cycles according to the vector table accessed. If the vector table has been relocated, enter the new address of the vector table in this field.

Enter the hexadecimal base address of the vector table in this eight digit fill-in field to allow the TMS 222 software to locate the vector base register.

The default hexadecimal vector table base address is: 00000000

Vector Table Size. This is a 12-bit fill-in field that contains the value of the interrupt table. The value of the interrupt table will be used in computing the name of the interrupt whenever an exception occurs. The vector table size value must be divisible by four. The range of values are:

Maximum value:	400
Minimum value:	8
Default value:	400

CS[7-0]~ Port Size. The CS[7-0]~ port size is an eight digit hexadecimal fill-in field. The CS[7-0]~ port size field contains the port sizes of the regions con-

trolled by the chip selects 7-0. Enter the value for each digit with a value of 0, 1, or 2, where:

0	Long port (32-bit)
1	Byte port (8-bit)
2	Word port (16-bit)

Example: Entering a value of 00011122 would mean that CS7, CS6 and CS5 are 32-bit ports; CS4, CS3 and CS2 are 8-bit ports; and CS1 and CS0 are 16-bit ports.

CS[1-0]~ BaseAddr. The CS[1-0]~ BaseAddr is an eight digit hexadecimal fill-in field. The CS[1-0]~ BaseAddr field contains the BaseAddr of the regions controlled by CS1~ and CS0~. Enter the value for each digit where the first four digits constitute the most significant 16-bits of the CS1~ base address, and the next four digits constitute the most significant 16-bits of the CS0~ base address.

CS[3-2]~ BaseAddr. The CS[3-2]~ BaseAddr is an eight digit hexadecimal fill-in field. The CS[3-2]~ BaseAddr field contains the BaseAddr of the regions controlled by CS3~ and CS2~. Enter the value for each digit where the first four digits constitute the most significant 16-bits of the CS3~ base address, and the next four digits constitute the most significant 16-bits of the CS2~ base address.

CS[5-4]~ BaseAddr. The CS[5-4]~ BaseAddr is an eight digit hexadecimal fill-in field. The CS[5-4]~ BaseAddr field contains the BaseAddr of the regions controlled by CS5~ and CS4~. Enter the value for each digit where the first four digits constitute the most significant 16-bits of the CS5~ base address, and the next four digits constitute the most significant 16-bits of the CS4~ base address.

CS[7-6]~ BaseAddr. The CS[7-6]~ BaseAddr is an eight digit hexadecimal fill-in field. The CS[7-6]~ BaseAddr field contains the BaseAddr of the regions controlled by CS7~ and CS6~. Enter the value for each digit where the first four digits constitute the most significant 16-bits of the CS7~ base address, and the next four digits constitute the most significant 16-bits of the CS6~ base address.

Marking Cycles

The TMS 222 will only allow marking of instruction fetch cycles (which include read extensions and flush cycles). If the cursor is placed on any other cycle type, no cycle marks will be available.

TLA 700 Series. Marks are placed by using the Mark Opcode button. The Mark Opcode button is always be available. If the sample being marked is not an instruction fetch cycle, the Mark Opcode selections will be replaced by a note indicating that “An Opcode Mark cannot be placed at the selected data sample.”

When a cycle is marked, the character ">>" is displayed immediately to the left of the Mnemonics column. Cycles can be unmarked by using the "Undo Mark" selection, which will remove the character ">>".

DAS 9200 Series. Marks are placed by using the F4 key: Mark Data function key. The Mark Data function key is always be available. If the cursor is not on an instruction fetch cycle, then no microprocessor cycle marks will be available when the key is pressed.

When a cycle is marked, the letter "m" is displayed immediately to the left of the Sequence column. Cycles can be unmarked by using the "Undo Mark" selection, which will remove the letter "m".

Cycle Marking. The following marks will be available for instruction fetch cycles:

The selections for 32-bit transfer are:

Opcode	Anything
Opcode	Opcode
Opcode	Flush
Flush	Flush
Flush	Opcode
Extension	Extension
Extension	Opcode
Extension	Flush
Undo Mark	Remove all marks from the current sequence.

The selections for 8-bit and 16-bit transfers are:

Opcode	
Extension	
Flush	
Undo Mark	Remove all marks from the current sequence.

Displaying Exception Vectors

The disassembler can display exception vectors.

You can relocate the table by entering the starting address in the Vector Base Register field. The Vector Base Register field provides the disassembler with the offset address. Enter an eight-digit hexadecimal value corresponding to the offset of the base address of the exception table. The Vector Table Size field lets you specify a three-digit hexadecimal size for the table.

These fields are located in the Disassembly property page (Disassembly Format Definition overlay).

Table 2–6 lists the MCF5206 exception vectors.

Table 2–6: Exception vectors

Exception number	Location in table (in hexadecimal)	Displayed exception name
0	000	(INITIAL STACK POINTER)
1	004	(INITIAL PROGRAM COUNTER)
2	008	(ACCESS ERROR VECTOR)
3	00C	(ADDRESS ERROR VECTOR)
4	010	(ILLEGAL INSTRUCTION VECTOR)
5	014	(RESERVED VECTOR #14H)
6	018	(RESERVED VECTOR #18H)
7	01C	(RESERVED VECTOR #1CH)
8	020	(PRIV VIOLATION VECTOR)
9	024	(TRACE VECTOR)
10	028	(UNIMPLEMENTED LINE–A OPCODE)
11	02C	(UNIMPLEMENTED LINE–F OPCODE)
12	030	(DEBUG INTERRUPT VECTOR)
13	034	(RESERVED VECTOR #34H)
14	038	(FORMAT ERROR VECTOR)
15	03C	(UNINIT INTERRUPT VECTOR)
16-23	040-05C	(RESERVED VECTOR #40H #5CH)
24	060	(SPURIOUS INTERRUPT VECTOR)
25-31	064-07C	(ILP 1-7 AUTOVECTOR)
32-47	080-08C	(TRAP #0t-#15t VECTOR)
48-63	0C0-0FC	(RESERVED VECTOR #C0-#FC)
64-255	100-3FC	(USER INT VECTOR #64t-#255t)

Specifications

Specifications

Specification Tables

These specifications are for a probe adapter connected between a compatible Tektronix logic analyzer and a SUT. Table 3–1 shows the electrical requirements the SUT must produce for the support to acquire correct data. Table 3–2 shows the environmental specifications.

Figure 3–1 shows the dimensions of the probe adapter. Figure 3–1 shows the dimensions of the test clip.

Table 3–1: Electrical specifications

Characteristics	Requirements	
SUT DC power requirements		
Voltage MCF5206	4.75–5.25 V	
Current MCF5206	$I_{maximum}$ 150 mA $I_{typical}$ 150 mA	
Voltage MCF5206E	3.0–3.6 VDC	
Current MCF5206E	$I_{minimum}$ 1.5 mA	
SUT clock rate		
MCF5206 Maximum specified clock rate	33.33 MHz	
Tested clock rate	25 MHz	
MCF5206E Maximum specified clock rate	54 MHz	
Tested clock rate	54 MHz	
Minimum setup time required	2.5 ns	
Minimum hold time required	0 ns	
Typical signal loading		
MICTOR load (ML) §	20 KΩ in parallel with 2 pF	
Podlet load (CL) §	20 KΩ in parallel with 2 pF	
Characteristics	**Specification**	
Measured typical SUT signal loading	**AC load**	**DC load**
A18, A21, SIZ0, SIZ1, D28, D27, D25, D24, D15, D7, D6, D5, D4, D3, D1, D0	2 pF + 1 ML	1 ML

Table 3–1: Electrical specifications (cont.)

Characteristics	Requirements	
R/W~, TA~, TS~, BD~, BG~, D18, D14, D13, D12, D11, D10, D9, D8, D2	3 pF + 1 ML	1 ML
BR~, D22, D16	4 pF + 1 ML	1 ML
D23, D19, HIZ~	5 pF + 1 ML	1 ML
TT0, TT1, CAS2~, DRAMW~, D26, D20, RTS2~/RTS0~	6 pF + 1 ML	1 ML
A4, A10, A11, A20, A22, A23, D29, D21	7 pF + 1 ML	1 ML
A5, A6, A12, A13, A14, A15, A19, RSTI~	8 pF + 1 ML	1 ML
A3, A7, A8, A16, TEA~, D13	9 pF + 1 ML	1 ML
A9, A17	10 pF + 1 ML	1 ML
A24/CS4~/WE3~	12 pF + 1 ML	1 ML
CS0~	10 pF + 1 ML	1 IC*
CAS2~, TT0	6 pF + 1 ML	1 IC*
A26/CS6~/WE1~	8 pF + 1 ML	1 IC*
A27/CS7~/WE0~, CAS3~	9 pF + 1 ML	1 IC*
A25/CS5~/WE2~, RAS0~, CAS1~	10 pF + 1 ML	1 IC*
CAS0~	11 pF + 1 ML	1 IC*
A24/CS4~/WE3~, RAS1~	12 pF + 1 ML	1 IC*
CS2~, CS3~	14 pF + 1 ML	1 IC*
CS1~	16 pF + 1 ML	1 IC*
A0, A1, A2	19 pF + 1 ML + 1 CL	1 ML + 1 CL
CLK	17 pF + 1 ML + 1 CL	1 ML + 1 CL

ML is Mictor load, CL is clock load.

*** MCF5206 IC is PALCE22V10**
MCF5206E IC is GAL22LV10

Table 3–2: Environmental specifications*

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F)†
Minimum operating	0° C (+32° F)
Non-operating	–55° C to +75° C (–67° to +167° F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

*** Designed to meet Tektronix standard 062-2847-00 class 5.**

† **Not to exceed MCF5206 microprocessor thermal considerations. Forced air cooling might be required across the CPU.**

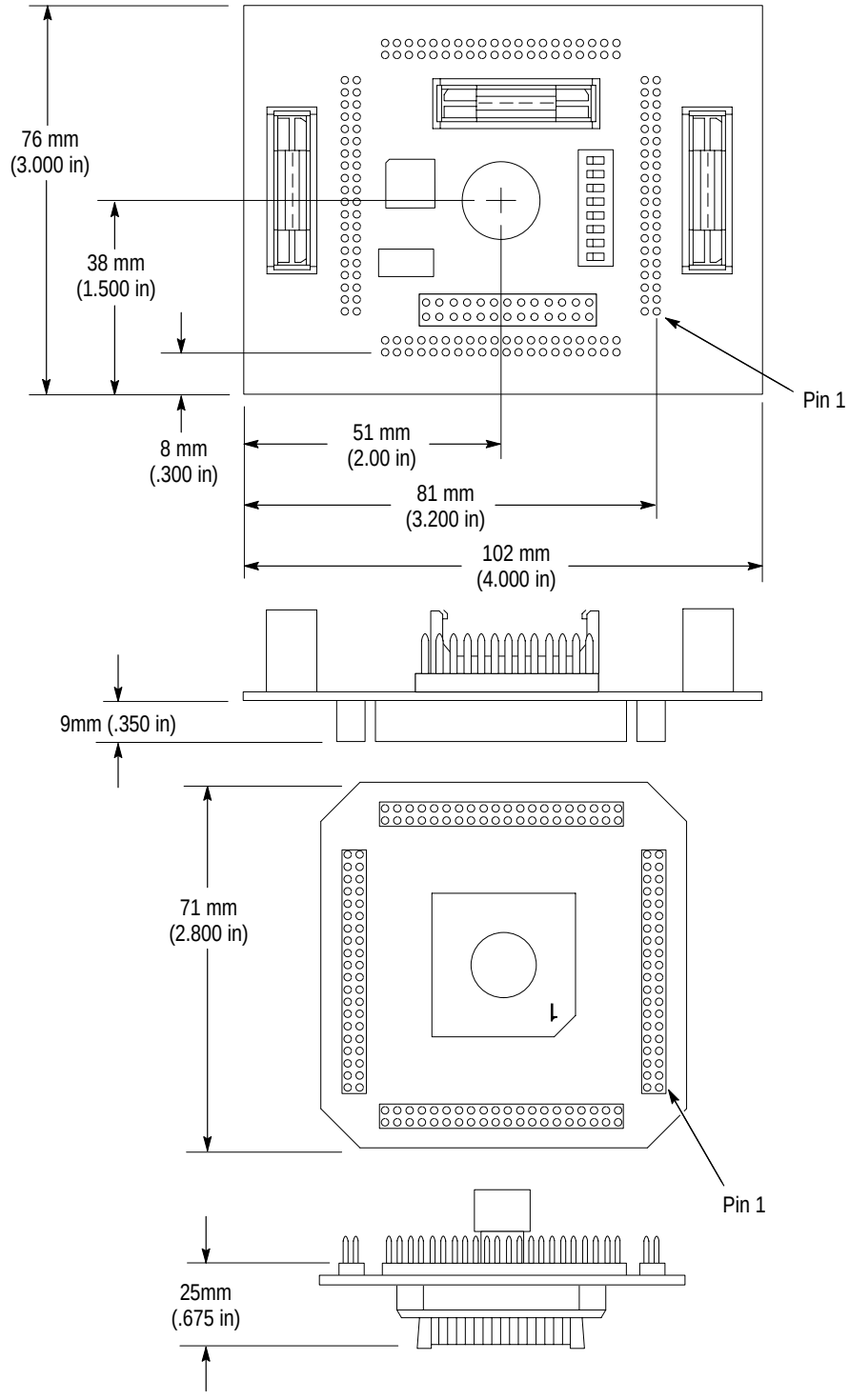


Figure 3–1: Dimensions of the probe adapter

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Maintenance

Maintenance

Probe Adapter Description

The probe adapter is nonintrusive hardware that allows the logic analyzer to acquire data from a microprocessor in its own operating environment with little or no effect on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and four connectors that interface with the supplied test clip. The test clip connects to the MCF5206 microprocessor located on your SUT. Signals from the microprocessor-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

The probe adapter accommodates the Motorola MCF5206 microprocessor in a 160-pin TQFP package.

At reset time, pins A[27-24]/CS[7-4]~/WE[3-0]~ can be configured as either Address pins, ChipSelect pins, or WriteEnable pins. To find out whether these pins are being used as ChipSelects, there is an eight position DIP switch S[7-0]. If any of the pins are being used as ChipSelects, the corresponding DIP switch is connected to the ON position. For example, if the A27/CS3~/WE3~ pin is configured as CS3~, switch S3 will be set to the ON position.

CS0~ is the chip enable for the boot region. There is a maximum of eight possible ChipSelects: CS[7-4]~, CS[3-0]~ A signal derived from the ChipSelects will be used as a qualifier. All the pins that are being used as ChipSelects are logically ANDed, and the output is used as the qual(D_CS~). If any of the pins are configured as CS it must be connected to the circuit by enabling the switch.

There are two RowAddressStrobe signals: RAS1~ and RAS0~. The derived common RowAddressStrobe signal is called D_RAS~ by logically ANDing the RAS1~ and RAS0~ signals.

There are four ColumnAddressStrobe signals: CAS[3-0]~. The derived common ColumnAddressStrobe signal is called D_CAS~ by logically ANDing the CAS[3-0]~ signals.

The probe adapter will meet LASI IV specifications.

Test Clip Inspection

Carefully inspect the test clip before each use. Inspect the contacts and verify that they are free of debris, and that none of the contacts are bent.

Replaceable Electrical Parts

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 222 MCF5206 and the MCF5206E microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

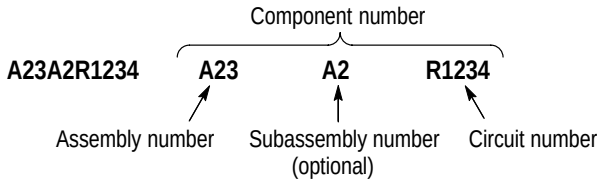
Parts list column descriptions

Column	Column name	Description
1	Component number	The component number appears on diagrams and circuit board illustrations, located in the diagrams section. Assembly numbers are clearly marked on each diagram and circuit board illustration in the *Diagrams* section, and on the mechanical exploded views in the *Replaceable Mechanical Parts* list section. The component number is obtained by adding the assembly number prefix to the circuit number (see Component Number illustration following this table). The electrical parts list is arranged by assemblies in numerical sequence (A1, with its subassemblies and parts, precedes A2, with its subassemblies and parts). Chassis-mounted parts have no assembly number prefix, and they are located at the end of the electrical parts list.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
6	Mfr. code	This indicates the code number of the actual manufacturer of the part.
7	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Component Number



Read: Resistor 1234 (of Subassembly 2) of Assembly 23

List of Assemblies

A list of assemblies is located at the beginning of the electrical parts list. The assemblies are listed in numerical order. When a part's complete component number is known, this list will identify the assembly in which the part is located.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
00779	AMP INC.	CUSTOMER SERVICE DEPT PO BOX 3608	HARRISBURG, PA 17105–3608
01KV9	MERIX CORP	1521 POPLAR LANE PO BOX 3000	FOREST GROVE, OR 97116
04222	AVX/KYOCERA	PO BOX 867	MYRTLE BEACH, SC 29577
09353	C & K COMPONENTS CORP	57 STANLEY AVE	WATERTOWN, MA 02172–4802
53387	3M COMPANY	ELECTRONICS PRODUCTS DIV 3M AUSTIN CENTER	AUSTIN, TX 78769–2963
57924	BOURNS INC	INTEGRATED TECHNOLOGY DIV. 1400 NORTH 1000 WEST	LOGAN, UT 84321
60381	PRECISION INTERCONNECT CORP.	16640 SW 72ND AVE	PORTLAND, OR 97224
85480	BRADY USA	NAMEPLATE DIVISION P O BOX 571 346 ELIZABETH BRADY RD	HILLSBOROUGH, NC 27278
TK0198	HAMILTON HALLMARK	9750 SW NIMBUS AVE	BEAVERTON, OR 97005
TK0198	AVNET INC	AVNET ELECTRONICS MKTG, AMERICA 15580 SW JAY STREET	BEAVERTON, OR 97006

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
–	006–2153–00			MARKER,IDENT:BRADY SPL B–969,FOR NO.00 0.093 X 0.125,96 PER CARD	85480	ORDER BY DESCRIPTION
–	105–1089–00			LATCH ASSY:LATCH HOUSING ASSY,VERTICAL MOUNT,0.48 H X 1.24 L,W/PCB SINGLE CLIP,P6434	60381	105–1089–00
–	131–5132–00			CONN,BOX:PCB,FEMALE,STR,2 X 20,0.1 CTR,0.325 H X 0.125 TAIL,10 GOLD,	53387	929852–01–20–10
–	131–5267–00			CONN,HDR:PCB,MALE,STR,2 X 40,0.1 CTR,0.235 MLG X 0.110 TAIL,30GOLD, HIGH TEMP,	00779	104326–4
–	131–6134–01			CONN,RCPT:SMD,MICTOR,FEMALE,STR,38 POS,0.025 CTR,0.240 H,W/0.108 PCB HOLD DOWNS.PALLADIUM	00779	767054–1
–	163–1109–00 *			IC,DIGITIAL:PRGM 156–7407–00:CMOS,PLD,EEPLD,22V10,140MA,5NS,5206,22V10–5,PLCC28–1,TUBE	TK0198	163–1109–00
–	163–1348–00 †			IC,DIGITIAL:PRGM 156–8320–00,CMOS,PLD:EEPLD,22LV10,130MA,4NS,3.3 VCC:22LV10–4,PLCC28,TUBE	TK0198	163–1348–00
–	260–5000–00			SWITCH,SLIDE:SPST,DIP8 POSITION,GOLD OVER NICKEL,3A,2PF,SEALED,90HBW08S,44MM T&R	09353	LD08HOSK1
–	283–5114–00			CAP,FXD,CERAMIC:MLC,0.1UF,10%,50V,X7R,1206,SMD, 8MM T&R	04222	12065C104KAT(1A OR 3A)
–	307–5041–01			RES,NTWK,FXD,FI:15,4.7K OHM,2%,PIN 16 COMMON,0.08W EA,1.2W PKG,50PPM,SMD,SO16.200,T&R	57924	4816P–002–472

***** *In the MCF5206 only*

† *In the MCF5206E only*

Diagrams and Circuit Board Illustrations

This section contains the troubleshooting procedures, block diagrams, circuit board illustrations, component locator tables, waveform illustrations, and schematic diagrams.

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975. Abbreviations are based on ANSI Y1.1-1972.

Logic symbology is based on ANSI/IEEE Standard 91-1984 in terms of positive logic. Logic symbols depict the logic function performed and can differ from the manufacturer's data.

The tilde (~) preceding a signal name indicates that the signal performs its intended function when in the low state.

Other standards used in the preparation of diagrams by Tektronix, Inc., include the following:

- Tektronix Standard 062-2476 Symbols and Practices for Schematic Drafting
- ANSI Y14.159-1971 Interconnection Diagrams
- ANSI Y32.16-1975 Reference Designations for Electronic Equipment
- MIL-HDBK-63038-1A Military Standard Technical Manual Writing Handbook

Component Values

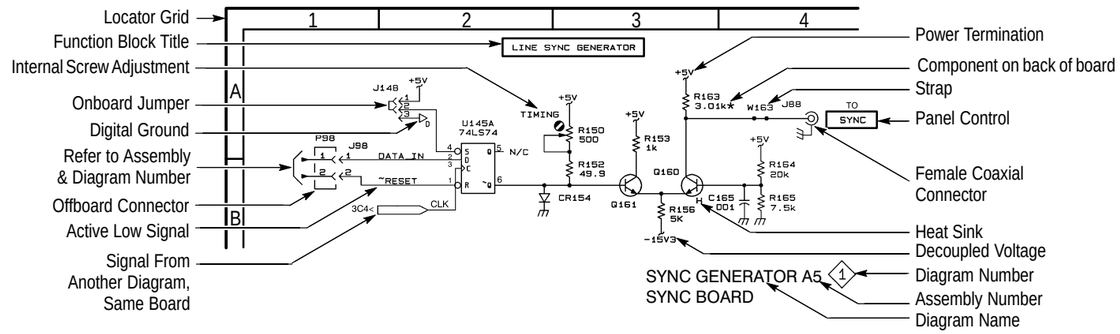
Electrical components shown on the diagrams are in the following units unless noted otherwise:

Capacitors: Values one or greater are in picofarads (pF).
Values less than one are in microfarads (µF).

Resistors: Values are in Ohms (Ω).

Graphic Items and Special Symbols Used in This Manual

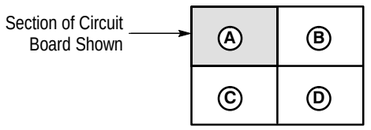
Each assembly in the instrument is assigned an assembly number (for example A5). The assembly number appears in the title on the diagram, in the lookup table for the schematic diagram, and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assembly in numerical sequence; the components are listed by component number.

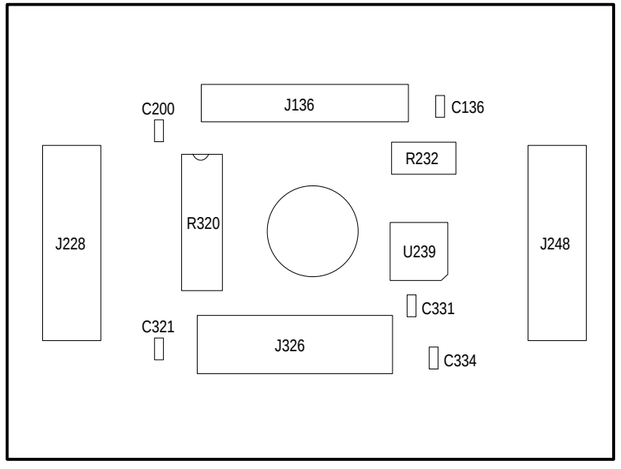


Component Locator Diagrams

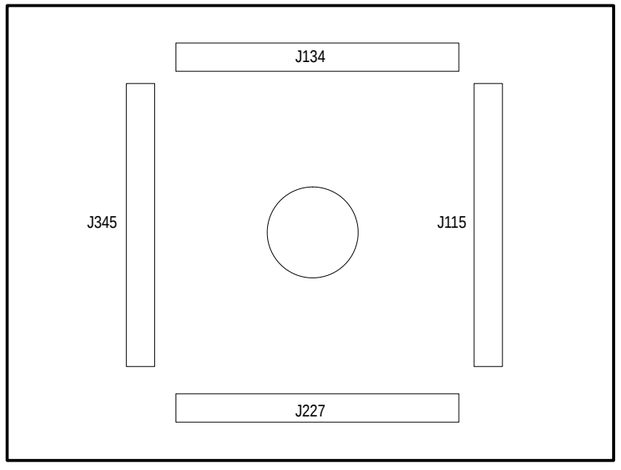
The schematic diagram and circuit board component location illustrations have grids marked on them. The component lookup tables refer to these grids to help you locate a component. The circuit board illustration appears only once; its lookup table lists the diagram number of all diagrams on which the circuitry appears.

Some of the circuit board component location illustrations are expanded and divided into several parts to make it easier for you to locate small components. To determine which part of the whole locator diagram you are looking at, refer to the small locator key shown below. The gray block, within the larger circuit board outline, shows where that part fits in the whole locator diagram. Each part in the key is labeled with an identifying letter that appears in the figure titles under component locator diagrams.

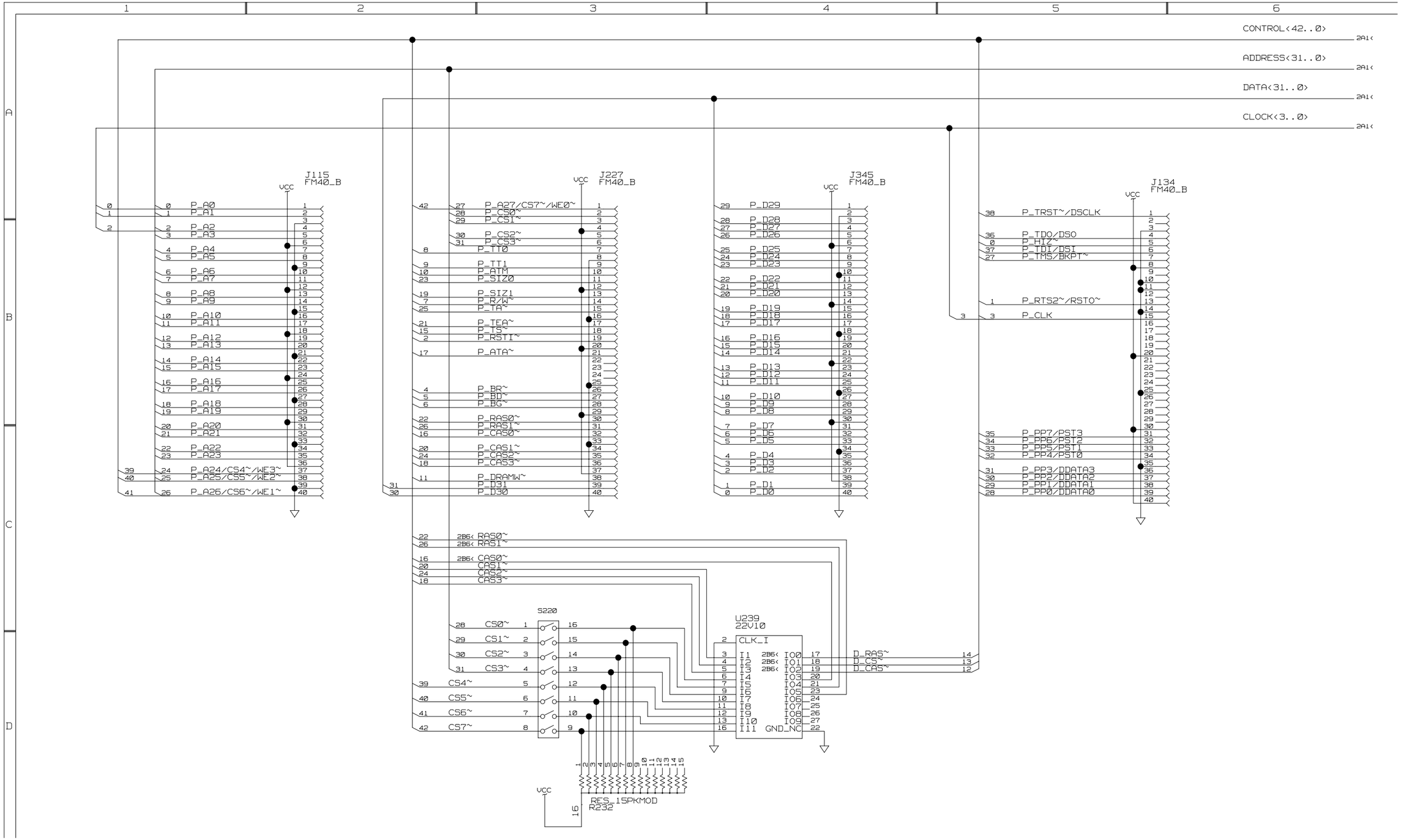



C200
J136
C136
R232
J228
R320
U239
J248
C331
C321
J326
C334

Front

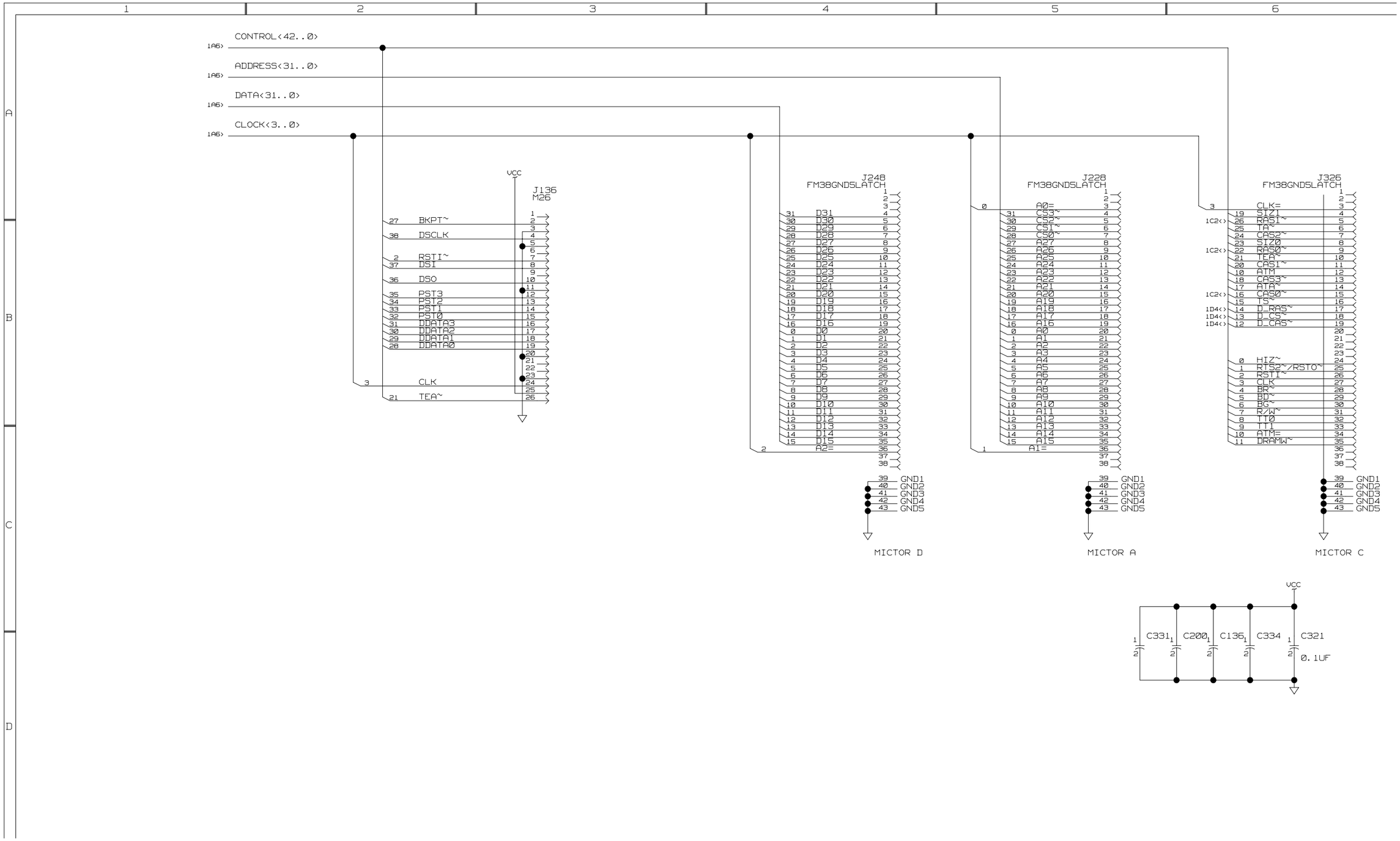

J134
J345
J115
J227

Back



UC, PAL LOGIC A01

1


CONTROL<42..0>
ADDRESS<31..0>
DATA<31..0>
CLOCK<3..0>
VCC
J136
M26
BKPT~
DSCLK
RSTI~
DSI
DSO
PST3
PST2
PST1
PST0
DDATA3
DDATA2
DDATA1
DDATA0
CLK
TEA~
J248
FM38GND5LATCH
D31
D30
D29
D28
D27
D26
D25
D24
D23
D22
D21
D20
D19
D18
D17
D16
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
A2=
GND1
GND2
GND3
GND4
GND5
MICTOR D
J228
FM38GND5LATCH
A0=
CS3~
CS2~
CS1~
CS0~
A27
A26
A25
A24
A23
A22
A21
A20
A19
A18
A17
A16
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
A1=
MICTOR A
J326
FM38GND5LATCH
CLK=
SIZ1
RAS1~
TA~
CAS2~
SIZ0
RAS0~
TEA~
CAS1~
ATM
CAS3~
ATA~
CAS0~
TS~
D_RAS~
D_CS~
D_CAS~
HIZ~
RTS2~/RSTO~
RSTI~
CLK
BR~
BD~
BG~
R/W~
TT0
TT1
ATM=
DRAMW~
MICTOR C
C331
C200
C136
C334
C321
0.1UF

Replaceable Mechanical Parts

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 222 MCF5206 and MCF5206E microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
00779	AMP INC.	CUSTOMER SERVICE DEPT PO BOX 3608	HARRISBURG, PA 17105–3608
53387	3M COMPANY	ELECTRONICS PRODUCTS DIV 3M AUSTIN CENTER	AUSTIN, TX 78769–2963
05276	ITT POMONA ELECTRONICS	1500 E NINTH ST	POMONA, CA 91766–3835
09353	C & K COMPONENTS CORP	15 RIVERDALE AVENUE	NEWTON, MA 02158
60381	PRECISION INTERCONNECT CORP.	16640 SW 72ND AVE	PORTLAND, OR 97224
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077–0001
04222	AVX/KYOCERA	PO BOX 867	MYRTLE BEACH, SC 29577
57924	BOURNS INC	INTEGRATED TECHNOLOGY DIV. 1400 NORTH 1000 WEST	LOGAN, UT 84321
TK0198	AVNET INC	AVNET ELECTRONICS MKTG, AMERICA 15580 SW JAY STREET	BEAVERTON, OR 97006

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
6–1–0	010–0620–00			1	ADAPTER, PROBE: 5206, QFP–160 PIN, TMS222 OPT 01	05276	010–0620–00
–1	671–4398–00			1	CIRCUIT BD ASSY: 5206, PQFP–160 SOLDERED, TMS222 01	80009	671–4398–00
–0	010–0634–00			1	ADAPTER, PROBE: 5206E, QFP–160 PIN, TMS222 OPT 02	80009	010–0634–00
–1	671–5012–00			1	CIRCUIT BD ASSY: 5206E, PQFP–160 SOLDERED, TMS222 OPT 02	80009	671–5012–00
–2	131–6134–01			3	CONN, RCPT: SMD, MICTOR, PCB, STR, 38 POS, FEMALE, 0.025 CTR, 0.240 H, W/0.108 PCB HOLD DOWNS. PALLAD	00779	767054–1
–3	105–1089–00			3	LATCH ASSY: LATCH HOUSING ASSY, VERTICAL MOUNT, 0.48 H X 1.24 L, W/PCB SINGLE CLIP, P6434	60381	105–1089–00
–4	260–5000–00			1	SWITCH, SLIDE: SPST, DIP8 POSITION, GOLD OVER NICKEL, 3A, 2PF, SEALED	09353	LD08HOSK1
–5	131–5267–00			1	CONN, HDR: PCB, MALE, STR, 2 X 40,0.1 CTR, 0.235 MLG X 0.110 TAIL, 30GOLD, HIGH TEMP	00779	104326–4
–6	131–5132–00			4	CONN, BOX:PCB, FEMALE, STR, 2 X 20, 0.1 CTR, 0.325 H X 0.125 TAIL, 10 GOLD	53387	929852–01–20–10
–7	103–0408–00			1	ADAPTER, QFP:ADAPTER, QFP, 160 POS, 0.65MM CTR, EIAJ QFP TO 0.25 SQ, 2X20 HDRS, TEST CLIP, 31.2MM L	05276	5645–2

Replaceable parts list (cont.)

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
	071–0149–01			1	MANUAL, TECH: INSTRUCTIONS, 5206/5602E, TMS 222	80009	071–0149–01
					OPTIONAL ACCESSORIES		
	P6434			3	P6434 MASS TERMINATION PROBE	80009	ORDER BY DESCRIPTION

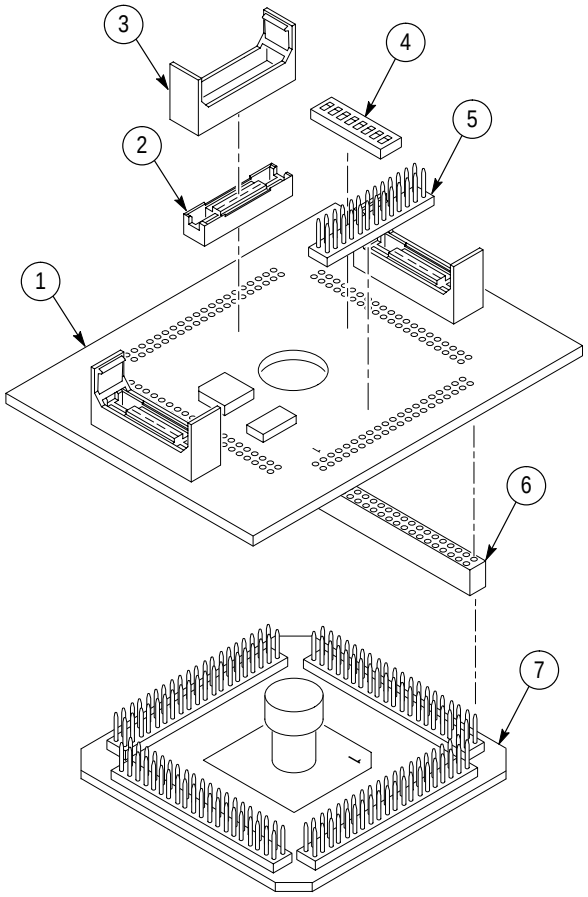


Figure 6–1: MCF5206 probe adapter exploded view

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