Instruction Manual

Tektronix

TMS 440
SH-3 7708 Microprocessor Support

071-0153-01

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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Tektronix, Inc., P.O. Box 1000, Wilsonville, OR 97070–1000

SOFTWARE WARRANTY

Tektronix warrants that the media on which this software product is furnished and the encoding of the programs on the media will be free from defects in materials and workmanship for a period of three (3) months from the date of shipment. If a medium or encoding proves defective during the warranty period, Tektronix will provide a replacement in exchange for the defective medium. Except as to the media on which this software product is furnished, this software product is provided “as is” without warranty of any kind, either express or implied. Tektronix does not warrant that the functions contained in this software product will meet Customer’s requirements or that the operation of the programs will be uninterrupted or error-free.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Use Proper Power Cord. Use only the power cord specified for this product and certified for the country of use.

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Ground the Product. This product is indirectly grounded through the grounding conductor of the mainframe power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

The common terminal is at ground potential. Do not connect the common terminal to elevated voltages.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Use Proper AC Adapter. Use only the AC adapter specified for this product.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Use Proper Fuse. Use only the fuse type and rating specified for this product.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, switch off the instrument power, then disconnect the power cord from the mains power.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface

This instruction manual contains specific information about the TMS 440 SH-3 7708 microprocessor support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor support packages on the logic analyzer for which the TMS 440 SH-3 7708 support was purchased, you will only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor support packages is included with each product. Each logic analyzer includes basic information that describes how to perform tasks common to support packages on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the support to acquire data from the system under test
- Acquiring and viewing disassembled data

Manual Conventions

This manual uses the following conventions:

- The term “disassembler” refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to online help, an installation manual, or a user manual covering the basic operations of microprocessor supports.
- In the information on basic operations, the term “XXX” or “P54C” appearing in field selections and file names must be replaced with SH-3. This term is the name of the microprocessor in field selections and file names you must use to operate the SH-3 7708 support.
- The term “SUT” (system under test) refers to the microprocessor-based system from which data will be acquired.

- The term “logic analyzer” refers to the Tektronix logic analyzer for which this product was purchased.
- The term “module” refers to an acquisition module.
- The term “HI module” refers to the module in the higher-numbered slot, and the term “LO module” refers to the module in the lower-numbered slot.
- SH-3 refers to all supported variations of the SH-3 7708 microprocessor unless otherwise noted.
- A tilde (~) following a signal name indicate an active low signal.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the user manual of the corresponding module. The manual set provides the information necessary to install, operate, maintain, and service the logic analyzer and its associated products.

Contacting Tektronix

Product Support	For questions about using Tektronix measurement products, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or contact us by e-mail: tm_app_supp@tektronix.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Tektronix offers extended warranty and calibration programs as options on many products. Contact your local Tektronix distributor or sales office. For a listing of worldwide service centers, visit our web site.
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000 USA
Website	Tektronix.com

Getting Started

Getting Started

This chapter contains information on the following topics and tasks:

- A description of the TMS 440 microprocessor support package
- Logic analyzer software compatibility
- Support restrictions
- How to connect to the system under test (SUT)
- Your system under test requirements
- How to apply power to and remove power from the probe adapter

Support Package Description

The TMS 440 microprocessor support package displays disassembled data from a system based on the Hitachi Micro Systems, Inc SH-3 7708 microprocessor.

The support runs on a TLA 700 Series logic analyzer equipped with a 102-channel module.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 440 microprocessor support.

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Parts* chapter.

To use this support efficiently, you need to have the items listed in the information on basic operations as well as the following documents:

- *SH7700 Series Programming Manual*, Hitachi Micro Systems, Inc 8/8/95 ADE–602–096
- *SH7708 Hardware User Manual*, Hitachi Micro Systems, Inc 9/10/96 ADE–602–105A
- *SH–3 Series Memory Interfacing*, Hitachi Micro Systems, Inc 11/22/96

Information on basic operations also contains a general description of support. Contact Tektronix for the availability of SH-3 7702 Support.

Logic Analyzer Software Compatibility

The floppy disk label on the microprocessor support states which version of logic analyzer software this support is compatible with.

Logic Analyzer Configuration

To use the SH-3 7708 support, the TLA 700 Series logic analyzer must be equipped with a 102-channel module at a minimum. The module must be equipped with enough probes to acquire channel and clock data from signals in your SH-3 7708-based system.

Refer to information on basic operations to determine how many modules and probes the logic analyzer needs to meet the channel requirements.

For the TLA 700 Series logic analyzer, the TMS 440 channel assignments follow the standard channel mapping and labeling scheme for P6434 probes. Follow the procedure to apply labels, using the standard method as described in the *P6434 Mass Termination Probe Instructions*.

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor support packages in the information on basic operations as they pertain to your SUT.

You should also review electrical, environmental, and mechanical specifications in *Specifications* in this manual as they pertain to your system under test, as well as the following descriptions of other SH-3 7708 support requirements and restrictions.

System Clock Rate. The SH-3 7708 microprocessor support can acquire data from the SH-3 7708 microprocessor operating at tested speeds of up to 60 MHz. This specification is valid at the time this manual was printed. Please contact your Tektronix Sales Representative for current information on the fastest devices supported.

Channel groups. The following table lists the SH-3 signals not required by the Clocking State Machine (CSM) or disassembler. SH-3 signals may be removed from their default connections and reattached to other signals of interest. Channel groups not required for clocking and disassembly are:

Signal name	Section:channel
CKE	C3–5
IOIS16~	C3–1
WAIT~	C0–2
IRQOUT~	C2–5
NMI~	C2–4
IRL0~	C0–3
IRL1~	C0–7
IRL2~	C3–0
IRL3~	C3–4

SUT Power. Whenever the SUT is powered off, remove power from the probe adapter. Refer to *Applying and Removing Power* on page 1–9 for information on how to remove power from the probe adapter.

Alternate Bus Master. Alternate bus master transactions are not processed in the disassembly.

Data Disassembly. For correct data display disassembly turn off (disable) the cache and the MMU address translation.

When the Address translation is enabled flushing could be incorrect (MMU page breaks interpreted as address breaks).

Byte Invalidation. Invalid bytes cannot be dashed out for reads from SRAM/ PSRAM/ROM/PCMCIA interfaces.

Opcode Fetch/Data Read. SH-3 7708 does not provide a signal to distinguish between “Data Read” and “Opcode Fetch”. The TMS 440 does make a reasonable estimate at looking a few sequences ahead at the address values yet in some instances you may need to use the “Mark Opcode” function.

Configuring the Probe Adapter

There are six jumpers on the probe adapter. The default position for all six jumpers is between pin 1 and pin 2 (See Figure 1–1). The custom clocking and acquisition software-setup choices function correctly when the jumpers are in the default position. Pin 2 of each jumper is connected to the logic analyzer through the Mictor connectors. These six jumpers are intended for future use.

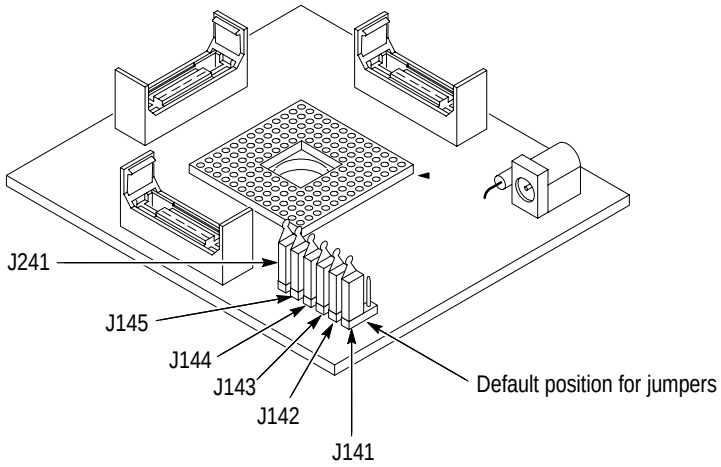


Figure 1–1: Jumper locations on the probe adapter

Connecting to a System Under Test With A Probe Adapter

Before you connect to the SUT (System Under Test), connect the probes to the module. Your SUT must also have a minimum amount of clear space surrounding the microprocessor to accommodate the probe adapter.

To connect the logic analyzer to a SUT using a probe adapter, follow these steps:

1. Turn off the power to your SUT. It is not necessary to turn off the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probe adapter, the probes, and the module. To prevent static damage, handle these components only in a static-free environment.*

Always wear a grounding wrist strap, heel strap, or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.

Connect the P6434 Probes to the Probe Adapter

3. Connect the P6434 probes to the probe adapter as shown in Figure 1–2. Match the channel groups and numbers on the probe labels to the corresponding pins on the probe adapter. Match the ground pins on the probes to the corresponding pins on the probe adapter.

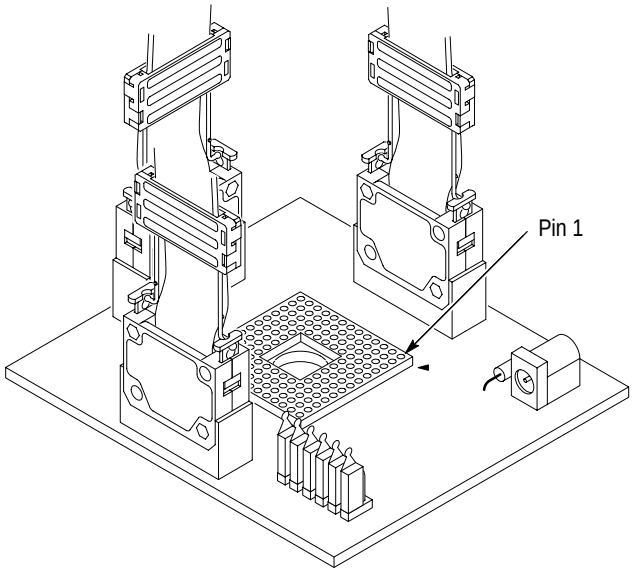


Figure 1–2: Connecting probes to a probe adapter

Connect the Test Clip to the Probe Adapter

4. Carefully seat the test clip on the PGA socket pins on the underside of the probe adapter as shown in Figure 1–3. Refer to the *Converter Clip Instructions* included with the probe adapter for more information about the test clip.

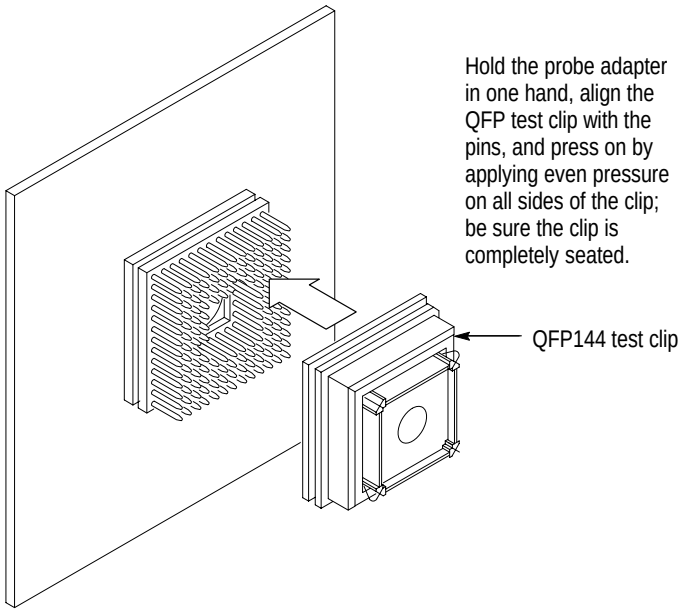


Figure 1–3: Seating the test clip on the probe adapter

Connect the Probe Adapter Assembly to the System Under Test

5. Inspect the microprocessor on your SUT for bent or broken leads. Verify that the leads on the microprocessor are clean and free from dirt, dust, or any foreign material.
6. Inspect the pins of the test clip for bent or broken contacts. Verify that the leads on the test clip are clean and free from dirt, dust or any foreign material.
7. Verify that the locking devise on the test clip is not locked by pushing and turning the locking device counterclockwise.

CAUTION. *Failure to correctly place the probe adapter assembly onto the microprocessor can permanently damage all electrical components when power is applied.*

Center the clip on the microprocessor and apply an equal downward force on all four sides of the clip, slightly rocking the probe adapter in a clockwise circle.

Do not apply leverage to the probe adapter when installing or removing it.

8. Place the probe adapter onto the SUT as shown in Figure 1–4.

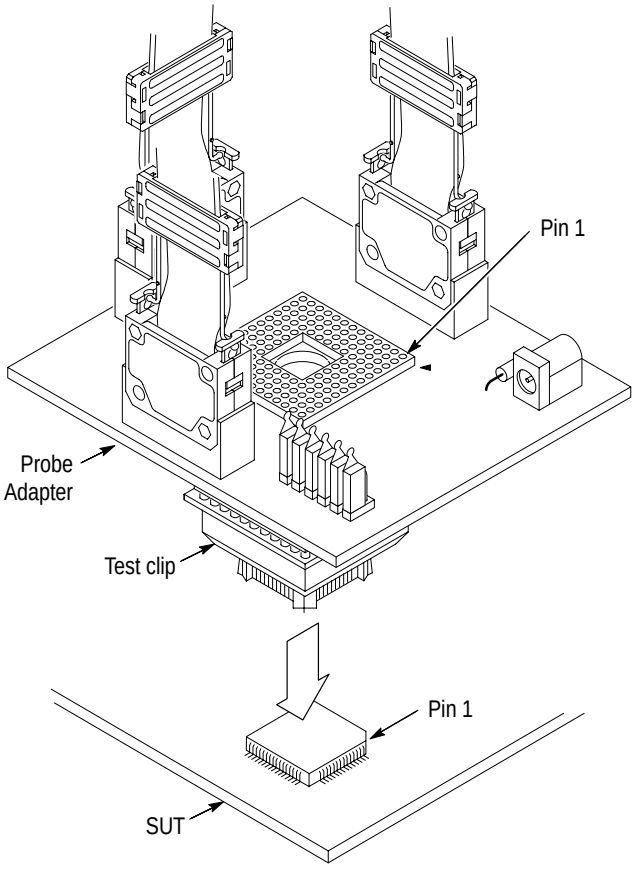


Figure 1–4: Placing the probe adapter assembly onto the SUT

9. Lock the test clip to the microprocessor by pushing and turning the locking device clockwise.

CAUTION. *The test clip was designed to be used on one and only one microprocessor. Because of the tight tolerances required for QFP test clip connectivity, the test clip that attaches to the microprocessor has a soft plastic collar that conforms to the unique shape of the target microprocessor.*

To avoid faulty and unreliable connections, it is highly recommended that the test clip is not used on any other microprocessor then the one it was originally connected to.

The test clip has a manufacturer's stated life expectancy of 8–10 connections.

CAUTION. *The probe adapter board might slip off or slip to one side of the microprocessor because of the extra weight of the probes. This can damage the microprocessor and the SUT. To prevent this from occurring, stabilize the probe adapter by placing a nonconductive object (such as foam) between the probe adapter and the SUT.*

Removing the Probe Adapter from the SUT

10. Unlock the test clip from the microprocessor by pushing and turning the locking device counterclockwise.

11. Gently lift and pull the probe adapter off of the microprocessor.

Connecting to a System Under Test Without A Probe Adapter

You can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your SUT.

To connect the probes to SH-3 7708 signals in the SUT using a test clip, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probes, and the logic analyzer module. To prevent static damage, handle these components only in a static-free environment.*

Always wear a grounding wrist strap, heel strap, or similar device while handling the microprocessor.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from it.

CAUTION. *Failure to place the SUT on a horizontal surface before connecting the test clip can permanently damage the pins on the microprocessor.*

3. Place the SUT on a horizontal static-free surface.

4. Use Table 1–1 through Table 1–8 to connect the channel probes to SH-3 7708 signal pins on the test clip or in the SUT.

Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip.

Applying and Removing Power

A power supply for the SH-3 7708 probe adapter is included with this microprocessor support. The power supply provides +5 volts power to the probe adapter.

To apply power to the SH-3 7708 probe adapter and SUT, follow these steps:

CAUTION. *Failure to use the +5 V power supply provided by Tektronix can permanently damage the probe adapter and SH-3 7708 microprocessor. Do not use any otherpower supply for the +5 V power supply.*

1. Connect the +5 V power supply to the jack on the probe adapter. Figure 1–5 shows the location of the jack on the adapter board.

CAUTION. *Failure to apply power to the probe adapter before applying power to your SUT can permanently damage the SH-3 7708 microprocessor and SUT.*

2. Plug the power supply for the probe adapter into an electrical outlet. When power is present on the probe adapter, an LED lights near the power jack.
3. Power on the SUT.

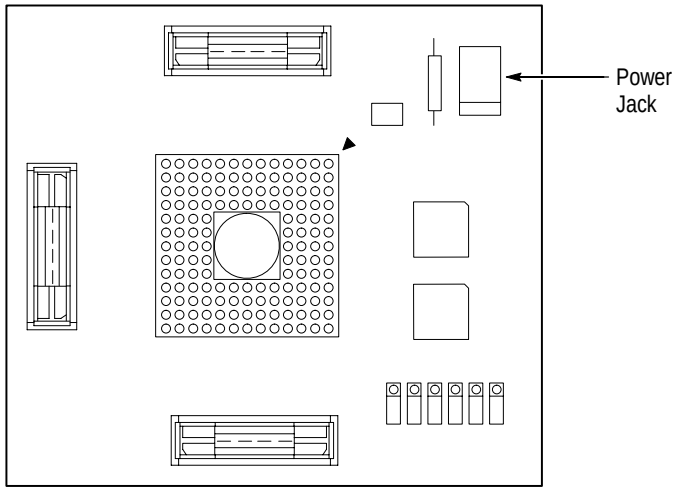


Figure 1–5: Location of the power jack

To remove power from the SUT and SH-3 7708 probe adapter, follow these steps:

CAUTION. *Failure to power down your SUT before removing the power from the probe adapter might permanently damage the SH-3 7708 microprocessor and SUT.*

1. Power off the SUT.
2. Unplug the power supply for the probe adapter from the electrical outlet.

Functionality Not Supported

Microprocessor. The cache must be turned off (disabled) for proper disassembly.

MMU address translation. The MMU address translation must be turned off for proper disassembly. When Address translation is enabled Flushing could be incorrect(MMU page breaks are interpreted as address breaks).

Channel Assignments

Channel assignments shown in Table 1–1 through Table 1–8 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB), descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- A tilde (~) following a signal name indicates an active low signal.
- An equals sign (=) following a signal name indicates that it is double probed.
- The module in the higher-numbered slot is referred to as the HI module and the module in the lower-numbered slot is referred to as the LO module.

Table 1–1 shows the probe section and channel assignments for the Address group and the microprocessor signal to which each channel connects. By default the Address channel group assignments are displayed in hexadecimal.

Table 1–1: Address channel group assignments

Bit order	Section:channel	SH-3 7708 signal name
31	A3:7	CS6~/CE1B~
30	A3:6	CS5~/CE1A~

Table 1–1: Address channel group assignments (cont.)

Bit order	Section:channel	SH-3 7708 signal name
29	A3:5	CS4~
28	A3:4	CS3~
27	A3:3	CS2~
26	A3:2	CS1~
25	A3:1	A25
24	A3:0	A24
23	A2:7	A23
22	A2:6	A22
21	A2:5	A21
20	A2:4	A20
19	A2:3	A19
18	A2:2	A18
17	A2:1	A17
16	A2:0	A16
15	A1:7	A15
14	A1:6	A14
13	A1:5	A13
12	A1:4	A12
11	A1:3	A11
10	A1:2	A10
9	A1:1	A9
8	A1:0	A8
7	A0:7	A7
6	A0:6	A6
5	A0:5	A5
4	A0:4	A4
3	A0:3	A3
2	A0:2	A2
1	A0:1	A1
0	A0:0	A0

Table 1–2 shows the probe section and channel assignments for the Data group and the microprocessor signal to which each channel connects. By default the Data channel group assignments are displayed in hexadecimal.

Table 1–2: Data channel group assignments

Bit order	Section:channel	SH-3 7708 signal name
31	D3:7	D31
30	D3:6	D30
29	D3:5	D29
28	D3:4	D28
27	D3:3	D27
26	D3:2	D26
25	D3:1	D25
24	D3:0	D24
23	D2:7	D23/Port7
22	D2:6	D22/Port6
21	D2:5	D21/Port5
20	D2:4	D20/Port4
19	D2:3	D19/Port3
18	D2:2	D18/Port2
17	D2:1	D17/Port1
16	D2:0	D16/Port0
15	D1:7	D15
14	D1:6	D14
13	D1:5	D13
12	D1:4	D12
11	D1:3	D11
10	D1:2	D10
9	D1:1	D9
8	D1:0	D8
7	D0:7	D7
6	D0:6	D6
5	D0:5	D5
4	D0:4	D4
3	D0:3	D3
2	D0:2	D2
1	D0:1	D1
0	D0:0	D0

Table 1–3 shows the probe section and channel assignments for the Control group and the microprocessor signal to which each channel connects. By default the Control channel group assignments are displayed as symbols. The symbol table file name is SH–3_Ctrl.

Table 1–3: Control channel group assignments

Bit order	Section:channel	SH-3 7708 signal name
10	Clk:3	L_BS~
9	Clk:1	L_RAS~
8	C2–3	DL_RASD~
7	Clk:2	L_CAS~
6	C2–0	DL_CASD~
5	C2–2	DL_WER~
4	C3–3	RD/WR~
3	C1–4	CASHH~/CAS2H~
2	C1–0	CASHL~/CAS2L~
1	C0–4	CASLH~
0	C0–0	CASLL~/CAS~/OE~

Table 1–4 shows the probe section and channel assignments for the CHip_Sel group and the microprocessor signal to which each channel connects. By default, this channel group is not displayed.

Table 1–4: Chip_Sel channel group assignments

Bit order	Section:channel	SH-3 7708 signal name
8	C3–6	MD4/CE2B~
7	C3–2	MD3/CE2A~
6	A3–7	CS6~/CE1B~
5	A3–6	CS5~/CE1A~
4	A3–5	CS4~
3	A3–4	CS3~
2	A3–3	CS2~
1	A3–2	CS1~
0	C2–6	CS0~

Table 1–5 shows the probe section and channel assignments for the Control2 group and the microprocessor signal to which each channel connects. By default, this channel group is not displayed.

Table 1–5: Control2 channel group assignments

Bit order	Section:channel	SH-3 7708 signal name
5	C1–3	RAS~/CE~
4	C1–7	MD5/RAS2~
3	C1–4	CASHH~/CAS2H~
2	C1–0	CASHL~/CAS2L~
1	C0–4	CASLH~
0	C0–0	CASLL~/CAS~/OE~

Table 1–6 shows the probe section and channel assignments for the WEN group and the microprocessor signal to which each channel connects. By default, this channel group is not displayed.

Table 1–6: WEN channel group assignments

Bit order	Section:channel	SH-3 7708 signal name
3	C1–5	WE3~/DQMUU~/ICIOWR~
2	C1–1	WE2~/DQMUL~/ICIORD~
1	C0–5	WE1~/DQMLU~
0	C0–1	WE0~/DQMLL~

Table 1–7 shows the probe section and channel assignments for the Misc group and the microprocessor signal to which each channel connects. By default, this channel group is not displayed.

Table 1–7: Misc channel group assignments

Bit order	Section:channel	SH-3 7708 signal name
15	C1–6	STATUS1
14	C1–2	STATUS0
13	C0–6	BACK~
12	C2–1	DL_STAT
11	C0–2	WAIT~
10	C3–1	IOIS16~
9	C3–5	CKE

Table 1–7: Misc channel group assignments (cont.)

Bit order	Section:channel	SH-3 7708 signal name
8	C2–5	IRQOUT~
7	Clk–0	CKIO
6	C2–7	BS~
5	C2–4	NMI
4	C0–3	IRL0~
3	C0–7	IRL1~
2	C3–0	IRL2~
1	C3–4	IRL3~
0	C3–7	RD~

Table 1–8 shows the signals on the probe adapter but not acquired.

Table 1–8: Signals that are on the probe adapter but not acquired

Signal Name	Pin Number
MD2/RXD	84
MD1/TXD	85
MD0/SCK	86
BREQ~	87
RESET~	88
TCLK	134
EXTAL	79
XTAL	80
CAP1	74
CAP2	77
XTAL2	136
EXTAL2	137

Nonintrusive Acquisition. The SH-3 7708 will not intercept, modify, or return signals to the system under test.

Acquisition Setup. The TMS 440 will affect the logic analyzer setup menus (and submenus) by modifying existing fields and adding micro-specific fields.

The TMS 440 will add the selection “SH-3” to the Load Support Package dialog box, located under the File pull-down menu. Once that “SH-3 support” has been loaded, the “Custom” clocking mode selection in the module Setup menu is also enabled.

CPU To Mictor Connections

To probe the microprocessor you will need to make connections between the CPU and the Mictor pins of the P6434 Mass Termination Probe. Refer to the P6434 Mass Termination Probe manual, Tektronix part number 070-9793-xx, for more information on mechanical specifications. Tables 1–9 through 1–11 show the CPU pin to Mictor pin connections.

Tektronix uses a counter-clockwise pin assignment. Pin-1 is located at the top left, and pin-2 is located directly below it. Pin-20 is located on the bottom right, and pin-21 is located directly above it.

AMP uses an odd side-even side pin assignment. Pin-1 is located at the top left, and pin-3 is located directly below it. Pin-2 is located on the top right, and pin-4 is located directly below it.

NOTE. *When designing Mictor connectors into your SUT, always follow the Tektronix pin assignment.*

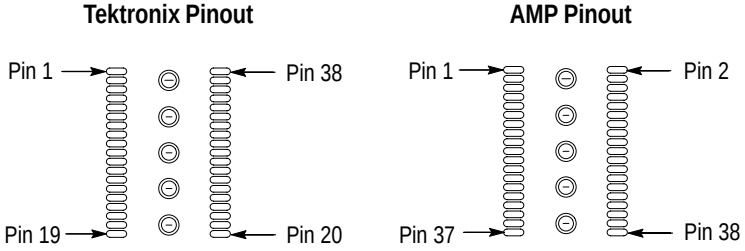


Figure 1–6: Pin assignments for a Mictor connector (component side)

Please pay close attention to the caution below.

CAUTION. *To protect the CPU and the inputs of the module, it is recommended that a 180Ω resistor is connected in series between each ball pad of the CPU and each pin of the Mictor connector. The resistor must be no farther away from the ball pad of the CPU than 1/2-inch.*

Table 1–9: CPU to Mictor connections for Mictor A pins

Tektronix Mictor A pin number	AMP Mictor A pin number	LA channel	SH-3 signal name	SH-3 7708 pin number
1	1	NC	NC	NC
2	3	NC	NC	NC
3	5	CLK:0	CKIO	101
4	7	A3:7	CS6~/CE1B~	108
5	9	A3:6	CS5~/CE1A~	109
6	11	A3:5	CS4~	110
7	13	A3:4	CS3~	111
8	15	A3:3	CS2~	112
9	17	A3:2	CS1~	113
10	19	A3:1	A25	72
11	21	A3:0	A24	71
12	23	A2:7	A23	70
13	25	A2:6	A22	67
14	27	A2:5	A21	66
15	29	A2:4	A20	65
16	31	A2:3	A19	64
17	33	A2:2	A18	63
18	35	A2:1	A17	62
19	37	A2:0	A16	61
20	38	A0:0	A0	37
21	36	A0:1	A1	38
22	34	A0:2	A2	39
23	32	A0:3	A3	40
24	30	A0:4	A4	43
25	28	A0:5	A5	44
26	26	A0:6	A6	45
27	24	A0:7	A7	46
28	22	A1:0	A8	47
29	20	A1:1	A9	48
30	18	A1:2	A10	51
31	16	A1:3	A11	52
32	14	A1:4	A12	53
33	12	A1:5	A13	56
34	10	A1:6	A14	57

Table 1–9: CPU to Mictor connections for Mictor A pins (cont.)

Tektronix Mictor A pin number	AMP Mictor A pin number	LA channel	SH-3 signal name	SH-3 7708 pin number
35	8	A1:7	A15	58
36	6	CLK:1	L_RAS~	–
37	4	NC	NC	NC
38	2	NC	NC	NC
39	39	GND	GND	GND
40	40	GND	GND	GND
41	41	GND	GND	GND
42	42	GND	GND	GND
43	43	GND	GND	GND

Table 1–10: CPU to Mictor connections for Mictor D pins

Tektronix Mictor D pin number	AMP Mictor D pin number	LA channel	SH-3 signal name	SH-3 7708 pin number
1	1	NC	NC	NC
2	3	NC	NC	NC
3	5	NC	NC	NC
4	7	D3:7	D31	140
5	9	D3:6	D30	141
6	11	D3:5	D29	142
7	13	D3:4	D28	143
8	15	D3:3	D27	1
9	17	D3:2	D26	2
10	19	D3:1	D25	3
11	21	D3:0	D24	4
12	23	D2:7	D23/Port7	5
13	25	D2:6	D22/Port6	8
14	27	D2:5	D21/Port5	9
15	29	D2:4	D20/Port4	10
16	31	D2:3	D19/Port3	11
17	33	D2:2	D18/Port2	12
18	35	D2:1	D17/Port1	13
19	37	D2:0	D16/Port0	14

Table 1–10: CPU to Mictor connections for Mictor D pins (cont.)

Tektronix Mictor D pin number	AMP Mictor D pin number	LA channel	SH-3 signal name	SH-3 7708 pin number
20	38	D0:0	D0	36
21	36	D0:1	D1	35
22	34	D0:2	D2	34
23	32	D0:3	D3	33
24	30	D0:4	D4	32
25	28	D0:5	D5	29
26	26	D0:6	D6	28
27	24	D0:7	D7	27
28	22	D1:0	D8	26
29	20	D1:1	D9	25
30	18	D1:2	D10	24
31	16	D1:3	D11	23
32	14	D1:4	D12	22
33	12	D1:5	D13	21
34	10	D1:6	D14	16
35	8	D1:7	D15	15
36	6	CLK:2	L_CAS~	–
37	4	NC	NC	NC
38	2	NC	NC	NC
39	39	GND	GND	GND
40	40	GND	GND	GND
41	41	GND	GND	GND
42	42	GND	GND	GND
43	43	GND	GND	GND

Table 1–11: CPU to Mictor connections for Mictor C pins

Tektronix Mictor C pin number	AMP Mictor C pin number	LA channel	SH-3 signal name	SH-3 7708 pin number
1	1	NC	NC	NC
2	3	NC	NC	NC
3	5	CLK–3	L_BS~	–

Table 1–11: CPU to Mictor connections for Mictor C pins (cont.)

Tektronix Mictor C pin number	AMP Mictor C pin number	LA channel	SH-3 signal name	SH-3 7708 pin number
4	7	C3:7	RD~	107
5	9	C3:6	MD4/CE2B~	103
6	11	C3:5	CKE	131
7	13	C3:4	IRL3~	90
8	15	C3:3	RD/WR~	106
9	17	C3:2	MD3/CE2A~	104
10	19	C3:1	IOIS16~	94
11	21	C3:0	IRL2~	91
12	23	C2:7	BS~	105
13	25	C2:6	CSO~	114
14	27	C2:5	IRQOUT~	95
15	29	C2:4	NMI	89
16	31	C2:3	DL_RASD~	–
17	33	C2:2	DL_WER~	–
18	35	C2:1	DL_STAT	–
19	37	C2:0	DL_CASD~	–
20	38	C0:0	CASLL~/CAS~/OE~	126
21	36	C0:1	WE0~/DQMLL~	124
22	34	C0:2	WAIT~	132
23	32	C0:3	IRL0~	93
24	30	C0:4	CASLH~	125
25	28	C0:5	WE1~/DQMLU~	123
26	26	C0:6	BACK~	96
27	24	C0:7	IRL1~	92
28	22	C1:0	CASHL~/CAS2L~	120
29	20	C1:1	WE2~/DQMUL~/ICIORD~	118
30	18	C1:2	STATUS0	98
31	16	C1:3	RAS~/CE~	129
32	14	C1:4	CASHH~/CAS2H~	119
33	12	C1:5	WE3~/DQMUU~/ICIOWR~	117
34	10	C1:6	STATUS1	97

Table 1–11: CPU to Mictor connections for Mictor C pins (cont.)

Tektronix Mictor C pin number	AMP Mictor C pin number	LA channel	SH-3 signal name	SH-3 7708 pin number
35	8	C1:7	MD5/RAS2~	130
36	6	NC	NC	NC
37	4	NC	NC	NC
38	2	NC	NC	NC
39	39	GND	GND	GND
40	40	GND	GND	GND
41	41	GND	GND	GND
42	42	GND	GND	GND
43	43	GND	GND	GND

Operating Basics

Setting Up the Support

The information in this section is specific to the operations and functions of the TMS 440 SH-3 7708 support on any Tektronix logic analyzer for which it can be purchased.

Before you acquire and display disassembled data, you need to load the support and specify the setups for clocking and triggering as described in the information on basic operations. The microprocessor support provides default values for each of these setups as well as user-definable settings.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the SH-3 7708 support are Address, Data, Control, Chip_Sel, Control2, WEN, and Misc. If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 1–10.

Clocking Options

The TMS 440 support offers a microprocessor-specific clocking mode for the SH-3 7708 microprocessor. This clocking mode is the default selection whenever you load the SH-3 support.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general-purpose analysis.

Custom Clocking

A special clocking program is loaded to the module every time you load the SH-3 support. This special clocking is called Custom.

In Custom clocking, the CSM (Clocking State Machine) generates one master sample for each microprocessor bus cycle, no matter how many clock cycles are contained in the bus cycle.

The Custom clocking for the SH-3 7708 processor has a Clock_option to take your input from the memory type connected to physical space areas 2 and 3.

The memory types for which the SH-3 7708 can provide Control signals are SRAM, Burst ROM, PCMCIA, DRAM, EDO DRAM, Puesdo-SRAM, and SDRAM.

The Control signals for these memories share pins. For example, WE3~/DQMUU/ICIOWR~ is used for SRAM, Puesdo-SRAM, and SDRAM and

is also used for the PCMCIA memories. Also, some qualifiers are latched on the rising edge of CKIO and some on the falling edge of CKIO. The qualifiers latched on the rising edge of CKIO are:

L_BS~, L_RAS~, L_CAS~ and DL_STAT

The qualifiers latched on the falling edge of CKIO are:

DL_RASD~, DL_CASD~ and DL_WER~

The TMS 440 has four modes of acquisition clocking. There is one select field with the following label:

Memory Type:

that will contain the following selections:

DRAM/PSRAM/NORMAL[1]	Cycles from those memories are acquired. (default)
SDRAM/NORMAL[1]	Cycles from those memories are acquired.
EDODRAM/NORMAL[1]	Cycles from those memories are acquired.
A2–DRAM/ A3–EDODRAM/NORMAL[1]	Cycles from Physical area2 – DRAM and area3 – EDODRAM are acquired.

[1] **NORMAL means SRAM/ROM/PCMCIA interfaces**

SRAM/ROM/PCMCIA Access. SRAM/ROM/PCMCIA accesses are handled by all four clocking options. The Address, Data, and Control signals are logged-in every trailing CKIO edge when the DL_WER~ qualifier is low, until the DL_WER~ goes high. When the DL_WER~ is high at the next rising CKIO edge it is mastered. The DL_WER~ for these cycles will go from low to high after a trailing edge of CKIO and before the rising edge of CKIO see figure 2–1.

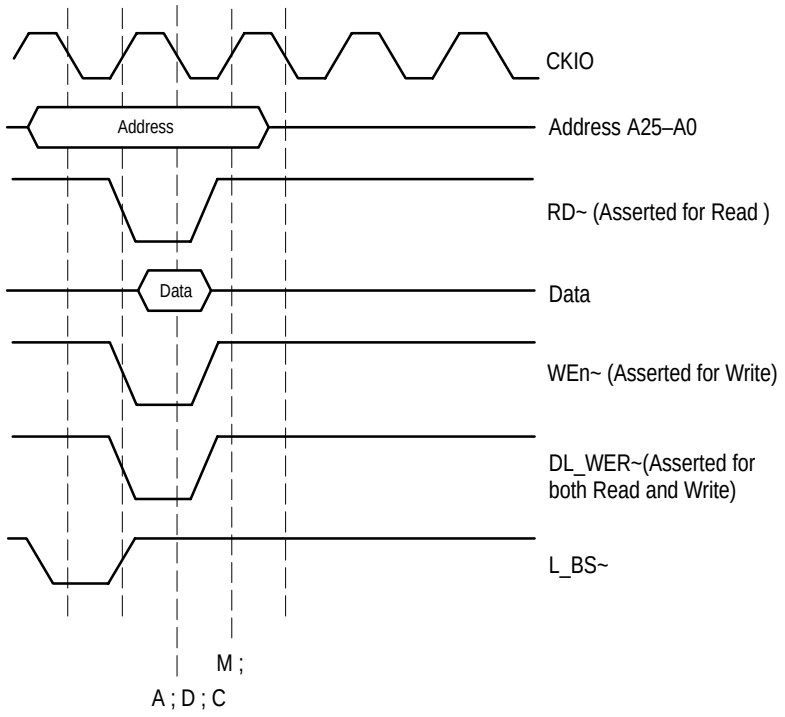


Figure 2–1: SRAM/ROM/PCMCIA Access bus timing

DRAM Access. DRAM accesses are handled by DRAM/PSRAM/NORMAL or A2–DRAM/A3–EDODRAM/NORMAL clocking options. The Address, Data, and Control signals are logged-in every trailing CKIO edge when the DL_CASD~ and DL_RASD~ qualifiers are low. When the DL_CASD~ is high at the next rising CKIO edge it is mastered. The DL_CASD~ for these cycles will go from low to high after a trailing edge of CKIO before the rising edge of CKIO see Figure 2–2.

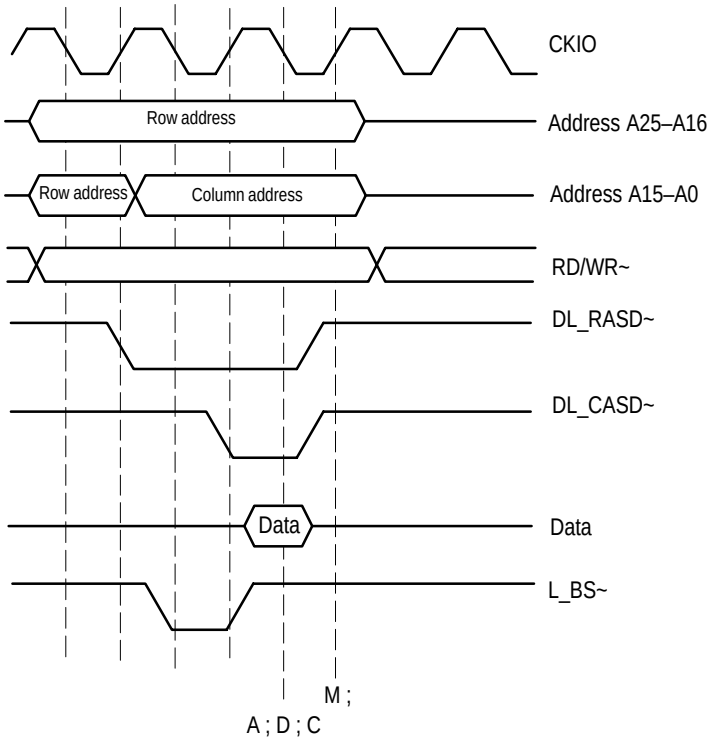


Figure 2–2: DRAM Access bus timing

EDO DRAM. EDO DRAM accesses are handled by EDODRAM/NORMAL or A2–DRAM/A3–EDODRAM/NORMAL clocking options. The Address, Data and Control signals are logged-in every rising CKIO edge after the DL_CASD~ qualifier is low. In the next trailing edge of CKIO, if DL_CASD~ is high, it is mastered, if DL_CASD~ is low Address, Data, and Control signals are logged-in the next rising edge of CKIO. The DL_CASD~ for these cycles will go from low to high after a trailing edge of CKIO before the rising edge of CKIO see Figure 2–3.

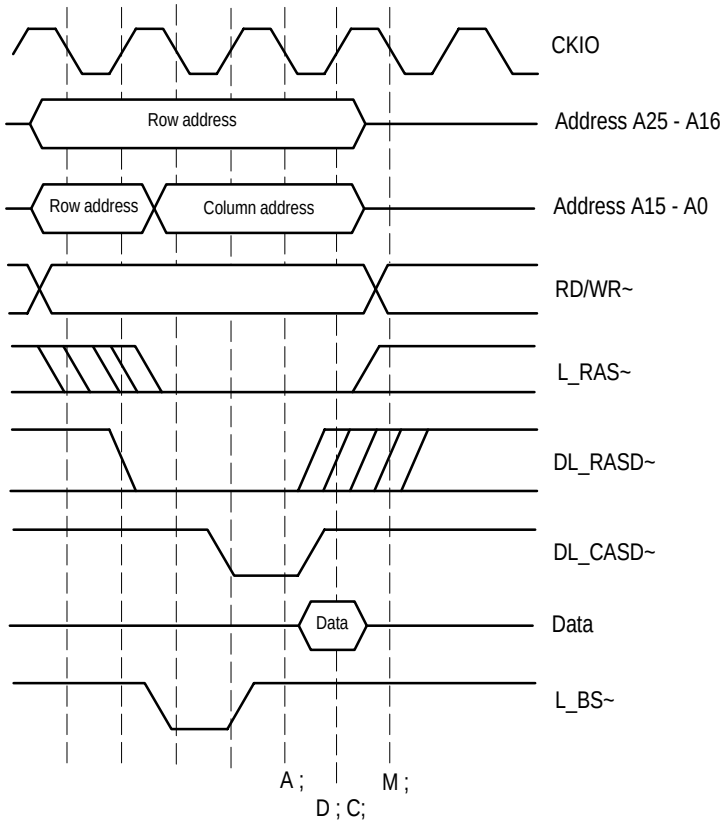


Figure 2–3: EDO DRAM Access bus timing

SDRAM Read. SDRAM accesses are handled by the SDRAM/NORMAL clocking options. The Row Address and Control signals are logged-in and mastered at the rising CKIO edge if the L_RAS~ is low and if DL_CASD~ and L_CAS~ is high see Figure 2–4.

In the coming rising edges of CKIO:

a. If the L_CAS~ is low, the Column Address and Control signals are logged-in and mastered.

b. If L_CAS~ and L_BS~ are low, the Column Address, Data and Control signals are logged-in and mastered.

If the Column address is mastered and data has not been acquired, as in the case of example b, then in the coming rising edges of CKIO if L_BS~ is low, the Data and Control signals are logged-in and mastered. It is possible to have L_RAS~, L_CAS~, and L_BS~ deasserted between Row Address and Column Address and between Column Address and Data. One of the main differences in the SDRAM Read cycles and SDRAM Write cycles shown below, is the RD/WR~ behavior.

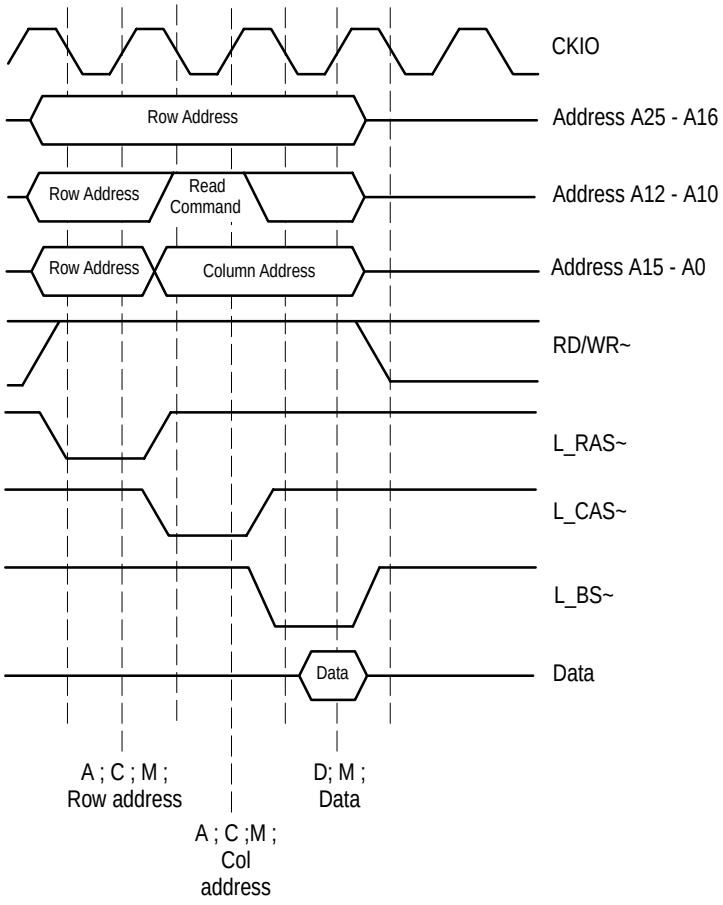


Figure 2–4: SDRAM Read bus timing

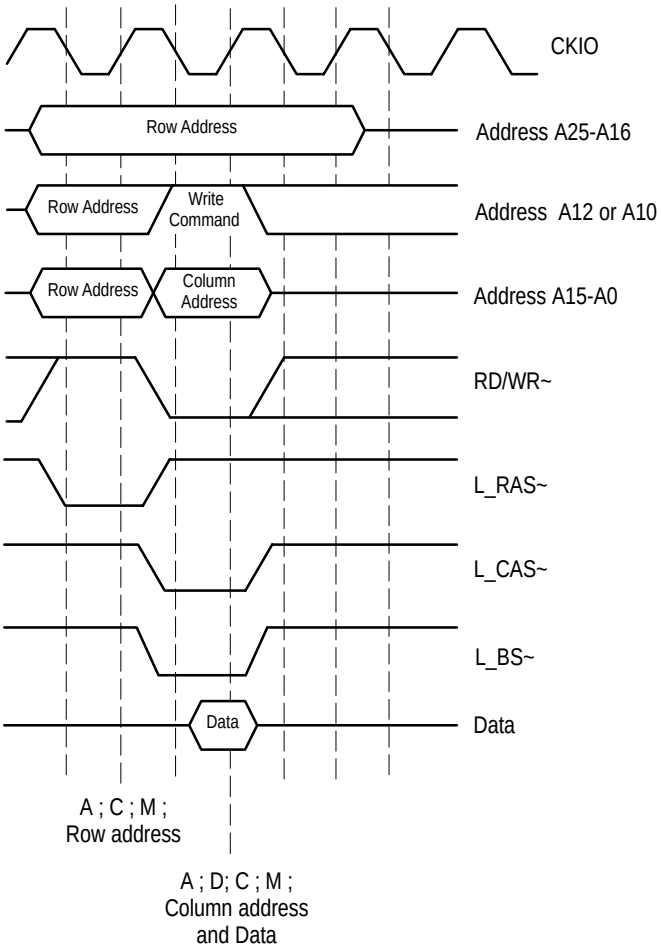


Figure 2–5: SDRAM Write bus timing

PSRAM Access. PSRAM accesses are handled by DRAM/PSRAM/NORMAL clocking option. In PSRAM Read, the Address, Data and Control signals are logged-in every trailing CKIO edge when the DL_CASD~ AND DL_RASD~ qualifiers are low. When the DL_CASD~ is high at the next rising CKIO edge, it is mastered. The DL_CASD~ for these cycles will go from low to high after a trailing edge of CKIO before the rising edge of CKIO.

In PSRAM Write, the Address, Data and Control signals are logged-in every trailing CKIO edge when the DL_WER~ AND DL_RASD~ qualifiers are low. When the DL_WER~ is high at the next rising CKIO edge, it is mastered. DL_WER~ for these cycles will go from low to high after a trailing edge of CKIO before the rising edge of CKIO see Figure 2–6.

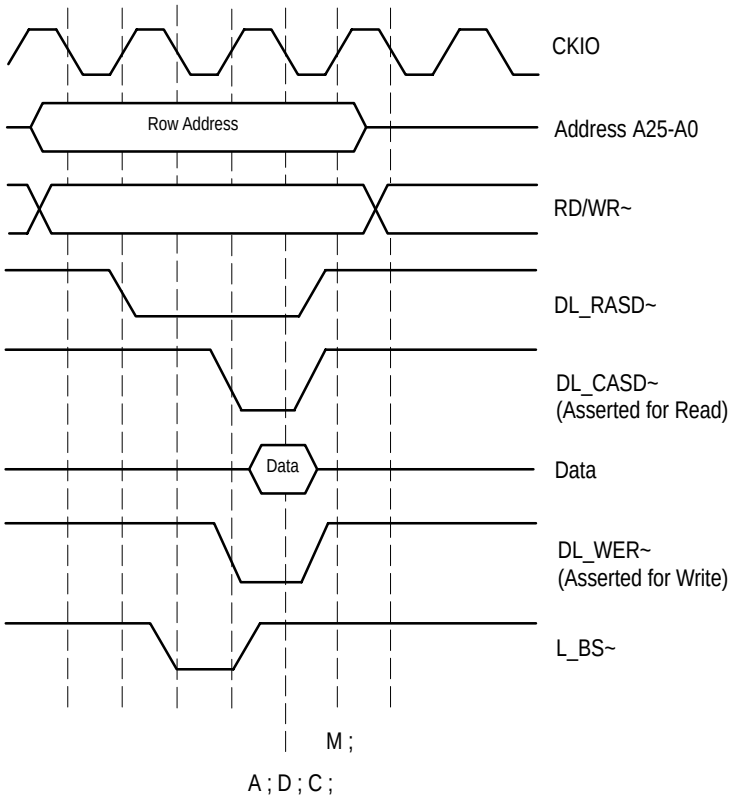


Figure 2–6: PSRAM Access bus timing

SDRAM Mode Register Accesses. SDRAM Mode Register Accesses are handled by the SDRAM/NORMAL clocking options. This access is marked mainly by L_RAS~ and L_CAS~ signals both going low together which does not happen for normal or burst in Read or Write Cycle types. When L_RAS~ AND L_CAS~ are both low at a rising CKIO edge, the Address, Data, and Control signals are logged-in and mastered see Figure 2–7.

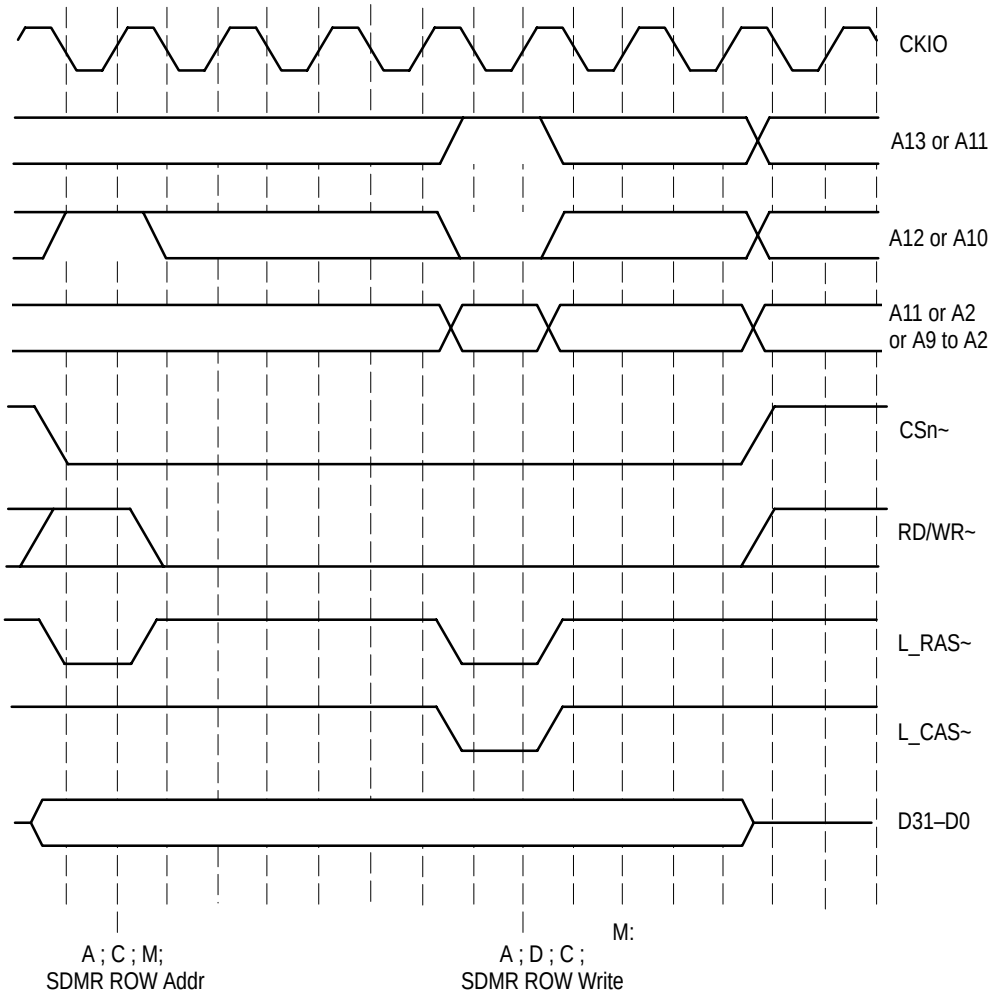


Figure 2–7: SDRAM Mode Register Write Cycles bus timing

Symbols

The TMS 440 support supplies one symbol table file. The SH-3_Ctrl file replaces specific Control channel group values with symbolic values when Symbolic is the radix for the channel group.

Symbol tables are generally not for use in timing or SH-3_T support disassembly.

Table 2–1 shows the name, bit pattern, and meaning for the symbols in the file SH-3_Ctrl, which contains the Control-channel group symbol table.

Table 2–1: Control group symbol table definitions

Symbol	Control group value L_BS~ L_RAS~ DL_RASD~ L_CAS~ DL_CASD~ DL_WER~ RD/WR~1 CASHH~ CASHL~ CASLH~ CASLL~	Meaning
"NORMAL READ"	1 1 1 1 1 0 1 X X X X	Memory read from SRAM/ROM/PCMCIA
"NORMAL WRITE"	1 1 1 1 1 0 0 X X X X	Memory write to SRAM/ROM/PCMCIA
"SDRAM COL ADDR"	1 1 1 0 X X X X X X X	SDRAM Column Address
"SDRAM DATA READ"	0 1 1 1 1 X 1 X X X X	SDRAM Data Read
"SDRAM COL ADDR & DATA READ"	0 1 1 0 X X 1 X X X X	SDRAM Column Address access and SDRAM Data Read done simultaneously
"SDRAM DATA WRITE"	0 1 1 1 1 X 0 X X X X	SDRAM Data Write
"SDRAM COL ADDR & DATA WRITE"	0 1 1 0 X X 0 X X X X	SDRAM Column Address access and SDRAM Data Write done simultaneously
"SDMR ROW ADDR"	1 0 X 1 1 1 0 1 1 1 1	SDRAM Mode Register Row Address
"SDRAM ROW ADDR"	1 0 X 1 X X 1 1 1 1 1	SDRAM Row Address
"PSRAM WRITE"	1 X 0 X 1 0 0 1 1 1 1	PSRAM Data Write
"EDO_DRAM / SDMR WRITE"	1 0 X X 1 1 0 1 1 1 0	EDO_DRAM Data Write or SDRAM Mode Register Write
"DRAM / SDMR WRITE"	1 X 0 X 0 1 0 1 1 1 0	DRAM Data Write or SDRAM Mode Register Write
"SDMR WRITE"	1 0 X 0 X 1 0 1 1 1 0	SDRAM Mode Register Write
"EDO_DRAM WRITE"	1 0 X X 1 1 0 X X X X	EDO_DRAM Data Write
"EDO_DRAM READ"	1 0 X X 1 1 1 X X X X	EDO_DRAM Data Read
"DRAM WRITE"	1 X 0 X 0 1 0 X X X X	DRAM Data Write
"PSRAM/DRAM READ"	1 X 0 X 0 1 1 X X X X	PSRAM Data Read or DRAM Data Read
"READ"	X X X X X X 1 X X X X	Read Cycle
"WRITE"	X X X X X X 0 X X X X	Write Cycle

NOTE*. NORMAL indicates SRAM/ROM/PCMCIA memory types; SDMR is SDRAM Mode Registe; SDRAM is Synchronous DRAM; PSRAM is Pseudo SRAM.*

Information on basic operations describes how to use symbolic values for triggering and for displaying other channel groups symbolically, such as for the Address channel group.

Acquiring and Viewing Disassembled Data

Acquiring Data

Once you load the SH-3 support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual.

Viewing Disassembled Data

You can view disassembled data in four display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

***NOTE**. Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–16.*

The default display format shows the Address, Data, and Control channel group values for each sample of acquired data.

If a channel group is not visible, you must use the Disassembly property page to make the group visible.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–2 lists these special characters and strings and gives a definition of what they represent.

Table 2–2: Meaning of special characters in the display

Character or string displayed	Definition
>>	Fetch cycle has been manually marked by you.
****	Indicates there is insufficient data available for complete disassembly of the instruction; the number of asterisks indicates the width of the data that is unavailable. Each two asterisks represent one byte.
#	Indicates an immediate value

Table 2–2: Meaning of special characters in the display (cont.)

Character or string displayed	Definition
t	Indicates the number shown is in decimal, such as #12t
>	There is insufficient room on the screen to show all available data.

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–3 lists these cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled with the vector name.

Table 2–3: Cycle type definitions

Cycle type	Definition
(ROW ADDR)	Row Address for an SDRAM access
(COL ADDR)	Column Address for an SDRAM access
(DATA READ)	Read Cycle
(DATA WRITE)	Write Cycle
(SDMR WRITE)	SDRAM Mode Register Write Cycle
(UNKNOWN)	Unexpected and/or unrecognized.
(EXTENSION)[1]	A fetch cycle computed to be an opcode extension
(FLUSH)[1]	A fetch cycle computed to be an opcode flush

[1] **Computed cycle types.**

Sample	SH-3 Address	SH-3 Data	SH-3 Mnemonic	Timestamp
990	TEST6	6106C709	(FLUSH)	37.801,500 us
991	F400003O	--------	(ROW ADDR)	37.868,500 us
992	F40036B4	--------	(COL ADDR)	37.902,000 us
993	080032B4	----0009	NOP	37.935,500 us
	080032B6	0009----	NOP	
994	F400003O	--------	(ROW ADDR)	38.019,000 us
995	F40036B8	--------	(COL ADDR)	38.052,000 us
996	080032B8	----C32O	TRAPA #20	38.085,000 us
	080032BA	002B----	(FLUSH)	
997	GEN_EXC>	----D003	MOV.L @(GEN_EXCEP_SVC+1O),RO	38.418,500 us
	GEN_EXC>	----D003	(GENERAL EXCEPTION)	
998	GEN_E>+2	----1OFF	MOV.L R15,@(START+F,RO)	38.618,000 us
999	GEN_E>+4	----DF03	MOV.L @(GEN_EXCEP_SVC+14),R15	38.868,500 us
1000	GEN_E>+6	----D104	MOV.L @(GEN_EXCEP_SVC+18),R1	39.068,000 us
1001	GEN_>+1O	----0600	(DATA READ)	39.301,500 us
1002	GEN_>+12	----0800	(DATA READ)	39.501,000 us
1003	F4000004	--------	(ROW ADDR)	39.668,000 us
1004	0800063C	0800503C	(DATA WRITE)	39.701,000 us
1005	GEN_>+14	----2DDO	(DATA READ)	39.951,000 us
1006	GEN_>+16	----0800	(DATA READ)	40.151,000 us
1007	GEN_E>+8	----D404	MOV.L @(GEN_EXCEP_SVC+1C),R4	40.384,500 us
1008	GEN_E>+A	----412B	JMP @R1	40.584,000 us
1009	GEN_>+18	----1OE4	(DATA READ)	40.817,500 us
1010	GEN_>+1A	----A000	(DATA READ)	41.017,000 us
1011	GEN_E>+C	----0009	NOP	41.250,500 us
1012	GEN_E>+E	----0000	(FLUSH)	41.450,000 us
1013	GEN_>+1C	----0100	(DATA READ)	41.683,500 us
1014	GEN_>+1E	----0000	(DATA READ)	41.883,500 us
1015	00001OE4	----1088	MOV.L R8,@(START+8,RO)	42.117,000 us
1016	00001OE6	----1099	MOV.L R9,@(START+9,RO)	42.316,500 us
1017	00001OE8	----1OAA	MOV.L R10,@(START+A,RO)	42.566,500 us
1018	00001OEA	----1OBB	MOV.L R11,@(START+B,RO)	42.766,500 us

Figure 2–8: Hardware display format

Software Display Format

The Software display format shows only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Read extensions will be used to disassemble the instruction, but will not be displayed as a separate cycle in the Software display format. Data reads and writes are not displayed.

Control Flow Display Format

The Control Flow display format shows only the first fetch of instructions that change the flow of control. Branches not taken will not be displayed.

Instructions that generate a change in the flow of control in the SH-3 7708 microprocessor are as follows:

BRA	BRAF	JMP	BSR	BSRF
JSR	RTS	RTE	TRAPA	

Instructions that may generate a change in the flow of control in the SH-3 7708 microprocessor are as follows:

BF	BF/S	BT	BT/S

Subroutine Display Format

The Subroutine display format shows only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

Instructions that generate a subroutine call or a return in the SH-3 7708 microprocessor are as follows:

BSR	BSRF	JSR	RTS
RTE	TRAPA		

Changing How Data is Displayed

There are common fields and features that allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

You can make selections unique to the SH-3 7708 support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception vectors

Optional Display Selections

You can make optional selections for acquired disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways:

Show:	Hardware (Default) Software Control Flow Subroutine
Highlight:	Software (Default) Control Flow Subroutine None
Disassemble Across Gaps:	Yes (Default) No

VBR. If you relocate the vector table, the disassembler can be informed of the new location by entering a Hex base address of eight digits in the fill in field. The default value for VBR (Vector Based Register) is 00000000.

NOTE. *The reset exception vector addresses can not be relocated, only the general and interrupt exception vectors can be relocated.*

Byte Order. You can select the byte ordering for the predominant instruction fetches as Little-Endian (default) or Big-Endian.

MMU Address Translation. Specify if the MMU (Memory Management Unit) address translation is disabled (default) or enabled on your system.

Bus Widths (CS0 – CS6). Select the Bus Width (Memory Size) of the memory areas CS0 to CS6 using the following notation:

B	BYTE (8-bit bus)
W	WORD (16-bit bus)
L	LONG (32-bit bus)

The left most character corresponds to CS0 area and the right most one corresponds to CS6. The character corresponding to an unused area can have any value B, W or L. The available selections are:

BBBBBBB All areas of CS0 to CS6 are a BYTE wide
BBBBBBL CS0 to CS5 have an 8-bit bus width. A bus width of CS7 is 16 bits.
BBBBBBW CS0 to CS5 have an 8-bit bus width. Bus width of CS7 is 32 bits.

.
.
.

WLLLLLL CS0:16-bit, CS1 to CS6:32-bit

.
.
.

LLLLLLL All areas are 32-bit width

Below is an example of the CS0 area having a 16-bit bus width and CS1 and CS2 control areas with a 32-bit bus width. Areas CS3 to CS6 are not used.

The first character is a W, since area CS0 is 16 bit, the second and third character is an L. since they are 32 bit. The rest of the characters are not used and can have any value. So the selection should be:

WLLBBBB

and the default selection is:

LLLLLLL

Memory Type in Area 3. Select the type of memory in Area 3 on your SUT:

Normal (default)
DRAM
SDRAM
PSRAM

Memory Type in Area 2. Select here the type of memory in Area 2 on your SUT:

Normal (default)
DRAM
SDRAM

AMX Bits in MCR. Select from the following possible combinations according to your MCR register setting for the SUT:

00
01
10
11

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it to one of the following cycle types:

- Extension – an extension to an instruction opcode
- Flush – a flushed cycle
- Opcode – an instruction opcode
- Undo Mark – removes all marks from the current sequence
- Data Read – mark cycle as data read

Mark selections for a 32-bit bus are as follows:

```
Data Read
Opcode       Opcode
Opcode       Flush
Flush        Opcode
Flush        Flush
Undo Mark
```

Mark selections for a 16-bit bus are as follows:

```
Data Read
Opcode
Flush
Undo Mark
```

Mark selections for an 8-bit bus are as follows:

```
Data Read
Opcode
Extension
Flush
Undo Mark
```

Displaying Exception Vectors

The disassembler can display exception vectors.

You can relocate the table by entering the starting address in the VBR field. The VBR field provides the disassembler with the base address; enter an eight-digit hexadecimal value corresponding to the base address of the exception table.

You can make these selections in the Disassembly property page (the Disassembly Format Definition overlay).

Table 2–4: Exception vectors for Addressing mode

Exception number	Location in interrupt vector table (in hexadecimal)	Displayed exception name
0	0000	(RESET EXCEPTION)
1	0100	(GENERAL EXCEPTION)
2	0400	(TLB MISS EXCEPTION)
3	0600	(INTERRUPT)

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your SH-3 7708 microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use, and you can view it without connecting the TLA 700 Series logic analyzer to your SUT.

Specifications

Specifications

These specifications are for a probe adapter connected between a compatible Tektronix logic analyzer and a SUT.

Table 3–1 lists the electrical requirements the SUT must produce for the SH-3 probe adapter to acquire correct data. Table 3–2 lists the environmental specifications.

Table 3–1: Electrical specifications

Characteristics	Requirements	
Probe adapter DC power requirements		
Voltage	4.75 – 5.25 VDC	
Current	I_{max} 400 mA I_{typ} 210 mA	
AC adapter		
Input Voltage rating	90 – 265 V	
Input Frequency Rating	47 – 63 Hz	
Output Voltage Rating	5 V	
Output Current Rating	5 V	
Output Power Rating	25 W	
SUT clock rate		
Maximum specified clock rate	60 MHz	
Tested clock rate	60 MHz	
Minimum setup time required		
TLA 700 logic analyzer	2.5 ns	
Minimum hold time required		
TLA 700 logic analyzer	0 ns	
Typical signal loading		
TLA 700 MICTOR load (ML) §	20 kΩ in parallel with 2 pF	
TLA 700 podlet load (CL) §	20 kΩ in parallel with 2 pF	
Measured typical SUT signal loading	**AC load**	**DC load**
CKIO	35 pF + ML[1]	2 PALCE22V10 + 1 CL[1]
RAS~/CE~	25 pF + ML	2 PALCE22V10 + 1 ML
CASLL~/CAS~/OE~	30 pF + ML	2 PALCE22V10 + 1 ML
BS~	24 pF + ML	1 PALCE22V10 + 1 ML

Table 3–1: (Cont.) Electrical specifications

Characteristics	Requirements	
Measured typical SUT signal loading	**AC load**	**DC load**
STATUS0	22 pF + ML	1 PALCE22V10 + 1 ML
BACK~	20 pF + ML	1 PALCE22V10 + 1 ML
WE3~/DQMUU~/ICIOWR~	17 pF + ML	1 PALCE22V10 + 1 ML
CASHH~/CAS2H~, CASHL~/CAS2L~	16 pF + ML	1 PALCE22V10 + 1 ML
WE1~/DQMLU~, RD~, STATUS1	15 pF + ML	1 PALCE22V10 + 1 ML
MD5/RAS2~	14 pF + ML	1 PALCE22V10 + 1 ML
CASLH~, WE2~/DQMUL~/ICIORD~	10 pF + ML	1 PALCE22V10 + 1 ML
WE0~/DQMLL~, MD4/CE2B~	9 pF + ML	1 PALCE22V10 + 1 ML
IRL1~	6 pF + ML	1 PALCE22V10 + 1 ML
CKE	14 pF + ML	1 ML
D31, D4	11 pF + 1 ML	1 ML
RD/WR~	6pF + 1 ML	1 ML
CS6~/CE1B~, CS4~, CS3~, CS2~, CS1~, WAIT~, CS0~, D30, D29, D8, D7, D3, D1,	10 pF + 1 ML	1 ML
MD4/CE2B~, NMI, D28, D15, D0, A8, A9	9 pF + 1 ML	1 ML
IRQOUT~, IOIS16~, IRL0~, IRL2~, IRL3~, MD3/CE2A~, D27, D26, D20/Port4, D12, D9, D2, A0, A3, A4, A1, A25	8 pF + 1 ML	1 ML
D18/Port2, D14, D13, D12, D6, D5, A7, A10, A11, A13, A15, A19, A21	7 pF + 1 ML	1 ML
D25, D24, D23/Port7, D19/Port3, D11, D10, A12, A14, A18, A20, A23, IT~	6 pF + 1 ML	1 ML
A2, A5, A6, A16, A17 A22, A24, D17/port1, D16/Port0	5 pF + 1 ML	1 ML
D22/Port6	4 pF + 1 ML	1 ML
D21/Port5	3 pF + 1 ML	1 ML

1 **ML is Mictor load, CL is clock load.**

Table 3–2 lists the environmental specifications.

Table 3–2: Environmental specifications[1]

Characteristic	Description
Temperature	
Maximum operating	+50 °C (+122 °F)[2]
Minimum operating	0 °C (+32° F)
Non-operating	–55 °C to +75 °C (–67 to +167 °F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

1 Designed to meet Tektronix standard 062-2847-00, class 5.

2 Not to exceed SH-3 7708 microprocessor thermal considerations. Forced air cooling might be required across the CPU.

Figure 3–1 shows the dimensions of the probe adapter and test clip.

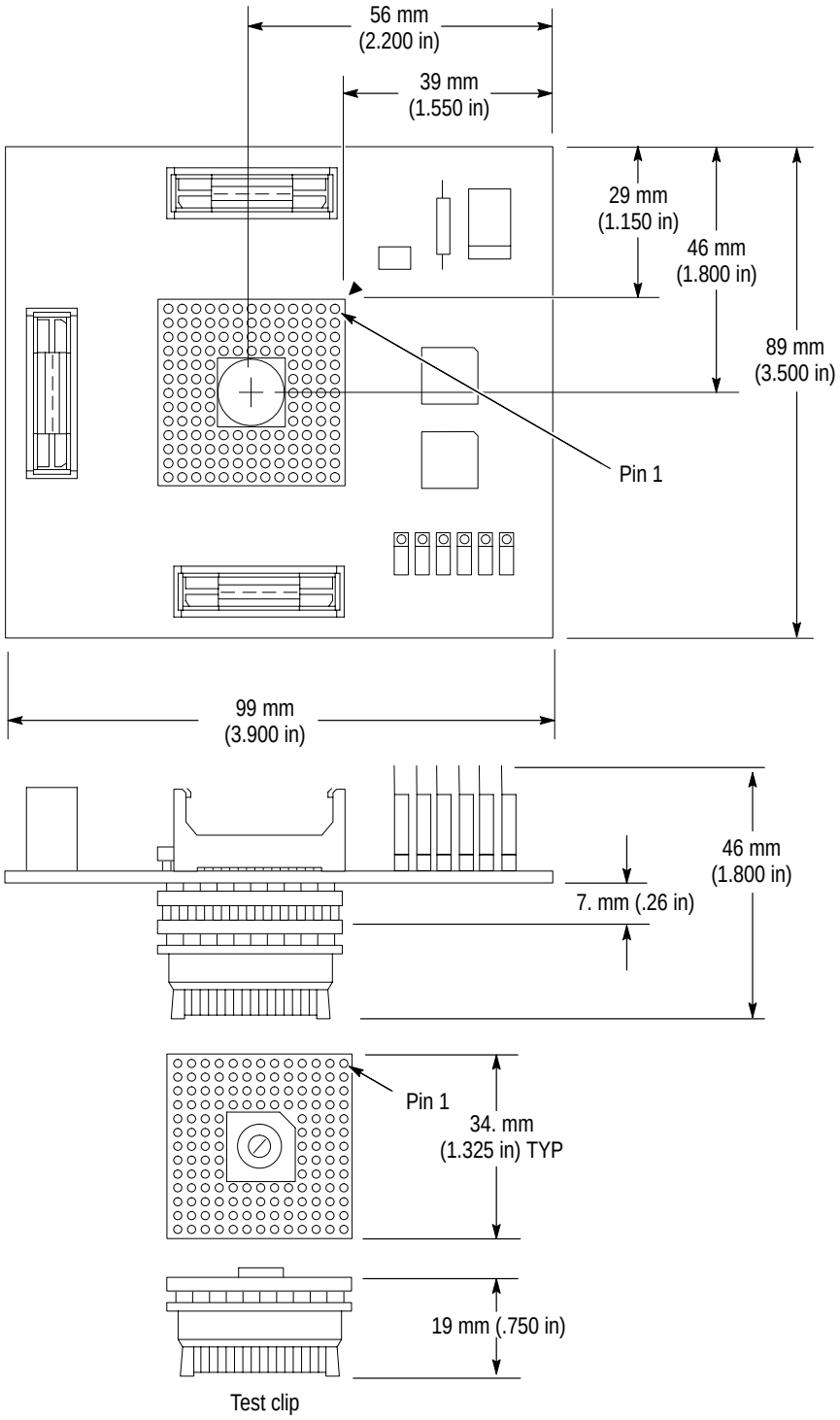


Figure 3–1: Dimensions of the probe adapter assembly and test clip

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Maintenance

Maintenance

This chapter contains information on the following topics:

- Probe adapter circuit description
- How to replace a fuse

Probe Adapter Circuit Description

The probe adapter is nonintrusive hardware that allows the logic analyzer to acquire data from a microprocessor in its own operating environment with little or no effect on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter assembly consists of a circuit board, a sacrificial socket, and a test clip for the SH-3 7708 microprocessor. The probe adapter connects to the microprocessor on the SUT. Signals from the microprocessor-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

The probe adapter accommodates the Hitachi Micro Systems, Inc SH-3 7708 microprocessor in a 144-pin QFP package.

A number of the SH-3 7708 signals are used to generate qualifiers by using the hardware on the probe adapter. These signals along with other SH-3 7708 signals go to the module through the Mictor connectors.

The SH-3 7708 support acquires all bus activity, as long as the SH-3 7708 is in normal operation. It does not acquire when the SH-3 7708 is in Reset, Sleep, and Standby Modes, or under Bus arbitration. Use the Status1, Status0, and Back~ signals in the Misc group for SH-3 7708 troubleshooting. To know the processor activity that puts the SH-3 7708 out of normal operation, you could trigger on the Status1 goes high or Status0 goes high or Back~ goes low and acquire in Internal Mode.

Replacing Signal Leads

Information on basic operations describes how to replace signal leads (individual channel and clock probes).

Replacing Protective Sockets

Information on basic operations describes how to replace protective sockets.

Replacing the Fuse

If the fuse on the SH-3 7708 probe adapter opens (burns out), you can replace it with a 5 A, 125 V fuse. Figure 4–1 shows the location of the fuse on the probe adapter.

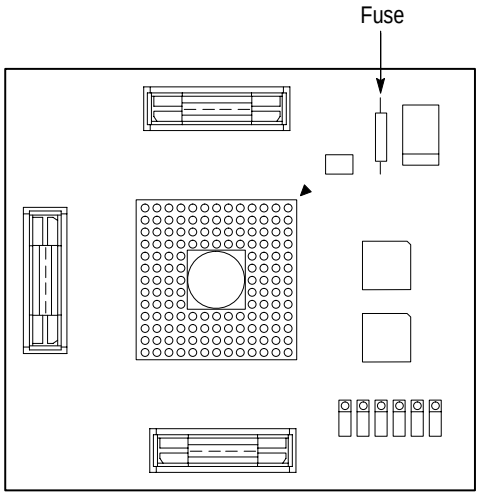


Figure 4–1: Location of the fuse

Replaceable Electrical Parts

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 440 SH-3 7708 microprocessor support.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

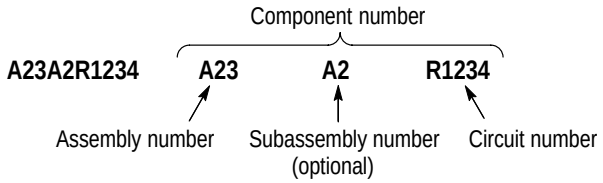
Parts list column descriptions

Column	Column name	Description
1	Component number	The component number appears on diagrams and circuit board illustrations, located in the diagrams section. Assembly numbers are clearly marked on each diagram and circuit board illustration in the *Diagrams* section, and on the mechanical exploded views in the *Replaceable Mechanical Parts* list section. The component number is obtained by adding the assembly number prefix to the circuit number (see Component Number illustration following this table). The electrical parts list is arranged by assemblies in numerical sequence (A1, with its subassemblies and parts, precedes A2, with its subassemblies and parts). Chassis-mounted parts have no assembly number prefix, and they are located at the end of the electrical parts list.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
6	Mfr. code	This indicates the code number of the actual manufacturer of the part.
7	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Component Number



Read: Resistor 1234 (of Subassembly 2) of Assembly 23

List of Assemblies

A list of assemblies is located at the beginning of the electrical parts list. The assemblies are listed in numerical order. When a part's complete component number is known, this list will identify the assembly in which the part is located.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
04222	AVX/KYOCERA	PO BOX 867	MYRTLE BEACH, SC 29577
00779	AMP INC.	CUSTOMER SERVICE DEPT PO BOX 3608	HARRISBURG, PA 17105–3608
01KV9	MERIX CORP	1521 POPLAR LANE PO BOX 3000	FOREST GROVE, OR 97116
26742	METHODE ELECTRONICS INC	BACKPLAIN DIVISION 7444 WEST WILSON AVE	CHICAGO, IL 60656–4548
50434	HEWLETT PACKARD	370 W TRIMBLE ROAD	SAN JOSE, CA 95131–1008
50579	SIEMENS COMPONENTS INC	OPTOELECTRONICS DIVISION 1900 HOMESTEAD RD	CUPERTINO, CA 95014
56845	DALE ELECTRONIC COMPONENTS	2300 RIVERSIDE BLVD PO BOX 74	NORFOLK, NE 68701
59124	KOA SPEER ELECTRONICS INC	BOLIVAR DRIVE PO BOX 547	BRADFORD, PA 16701
60381	PRECISION INTERCONNECT CORP.	16640 SW 72ND AVE	PORTLAND, OR 97224
61857	SAN–O INDUSTRIAL CORP	91–3 COLIN DRIVE	HOLBROOK, NY 11741
63058	BERG ELECTRONICS INC.	MCKENZIE SOCKET DIV 910 PAGE AVE	FREMONT, CA 94538–7340
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077–0001
85480	BRADY USA	NAMEPLATE DIVISION P O BOX 571 346 ELIZABETH BRADY RD	HILLSBOROUGH, NC 27278
TK0198	HAMILTON HALLMARK	9750 SW NIMBUS AVE	BEAVERTON, OR 97005
TK0875	MATSUO ELECTRONICS	2134 MAIN STREET SUITE 200	HUNTINGTON BEACH, CA 92648
TK2449	SINGATRON ENTERPRISE CO LTD	13925 MAGNOLIA AVE	CHINO, CA 91710

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
	671–4406–00			CIRCUIT BD ASSY:PQFP–144 PINS,SOLDERED,679–4406–00 TESTED,389–2579–00 WIRED,TMS440 OPT 02	80009	671–4406–00
	105–1089–00			LATCH ASSY:LATCH HOUSING ASSY,VERTICAL MOUNT,0.48 H X 1.24 L,W/PCB SINGLE CLIP,P6434	60381	105–1089–00
	131–4356–00			CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER,	26742	9618–302–50
	131–4530–00			CONN,HDR:PCB,MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION,	00779	104344–1
	131–5527–00			JACK,POWER DC:PCB,MALE,RTANG,2MM PIN,11MM H(0.433) X 3.5MM(0.137) TAIL,9MM(0.354) W,TIN,W/SWI	TK2449	DJ–005–A
	131–6134–01			CONN,PLUG:SMD,MICTOR,PCB,FEMALE,STR,38 POS,0.025 CTR,0.245 H,GOLD,TLA7QS	00779	767004–1
	136–1324–00			SOCKET,PGA:PCB,FEMALE,144 POS,12 X 12,OPEN CENTER,SHORT PINS,PGA–144H101B1–1302–R	63058	PGA–144H101B1–1 302–R
	136–1325–00			SOCKET,PGA:PCB,FEMALE,STR,144 POS,12 X 12,LONG PINS,VENDOR NUMBER,PGA–144H115B1–1302–R	63058	PGA–144H115B1–1 302–R
	150–5001–00			DIODE,OPTO:LED,GRN,565NM,2.0VF AT 10MA IF,12.5VF MAX,0.4MCD MIN AT 10MA,LG S260–DO,SOT–23,	50579	LG S260–DOGEGURT
	152–5045–00			DIODE,SIG:SCHOTTKY,20V,1.2PF,24 OHM,HSMS–2810,TO–236/SOT–23,8MM T&R	50434	HSMS–2810–T31
	159–0059–00			FUSE,WIRE LEAD:5A,125V	61857	SPI–5A
	163–1106–00			IC,DIGITAL:PRGM 156–7407–00,CMOS,PLD,EEPLD,22V10,140MA,5NS,PAL1,22V10–5,PLCC28–1,TUBE	TK0198	163–1106–00
	163–1107–00			IC,DIGITAL:PRGM 156–7407–00,CMOS,PLD,EEPLD,22V10,140MA,5NS,PAL2,22V10, PLCC28–1,TUBE	TK0198	163–1107–00
	283–5114–00			CAP,FXD,CERAMIC;MLC;0.1UF,10%,50V,X7R,1206;SMD,8MM T&R	04222	12065C104KAT(1A OR 3A)
	290–5005–00			CAP,FXD,TANT:47UF,10%,10V,5.8MM X 4.6MM,5846,SMD,T&R	TK0875	267M–1002–476–K R–533
	307–5131–00			RES,NTWK,FXD,FI:(4) 180 OHM,5%,63MW EACH,50V,200PPM,ISOLATED,ARRAY,SMD,T&R	56845	CRA06S0803–181J–RT1
	321–5454–00			RES,FXD,FILM:332 OHM,1%,50V,62.5MW,0603,SMD,T&R	59124	RK73H1J3320FT

Diagrams

Diagrams and Circuit Board Illustrations

This section contains the troubleshooting procedures, block diagrams, circuit board illustrations, component locator tables, waveform illustrations, and schematic diagrams.

Symbols

Graphic symbols and class designation letters are based on ANSI Standard Y32.2-1975. Abbreviations are based on ANSI Y1.1-1972.

Logic symbology is based on ANSI/IEEE Standard 91-1984 in terms of positive logic. Logic symbols depict the logic function performed and can differ from the manufacturer's data.

The tilde (~) preceding a signal name indicates that the signal performs its intended function when in the low state.

Other standards used in the preparation of diagrams by Tektronix, Inc., include the following:

- Tektronix Standard 062-2476 Symbols and Practices for Schematic Drafting
- ANSI Y14.159-1971 Interconnection Diagrams
- ANSI Y32.16-1975 Reference Designations for Electronic Equipment
- MIL-HDBK-63038-1A Military Standard Technical Manual Writing Handbook

Component Values

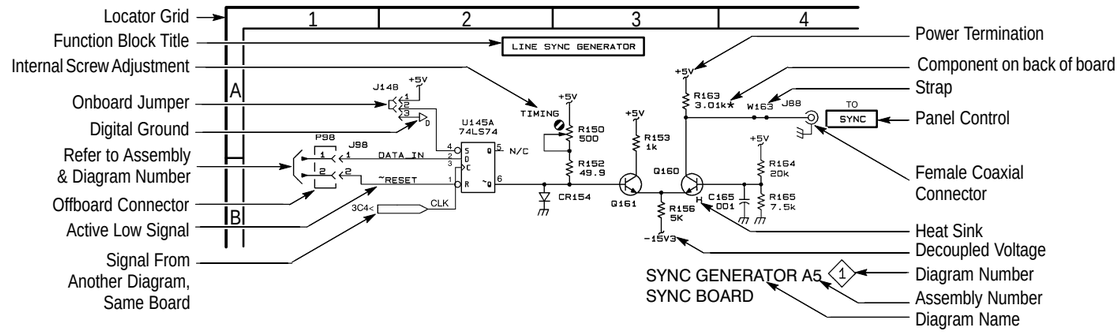
Electrical components shown on the diagrams are in the following units unless noted otherwise:

Capacitors: Values one or greater are in picofarads (pF).
Values less than one are in microfarads (μF).

Resistors: Values are in Ohms (Ω).

Graphic Items and Special Symbols Used in This Manual

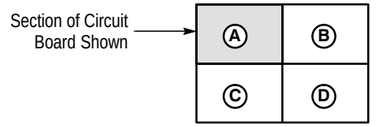
Each assembly in the instrument is assigned an assembly number (for example A5). The assembly number appears in the title on the diagram, in the lookup table for the schematic diagram, and corresponding component locator illustration. The Replaceable Electrical Parts list is arranged by assembly in numerical sequence; the components are listed by component number.

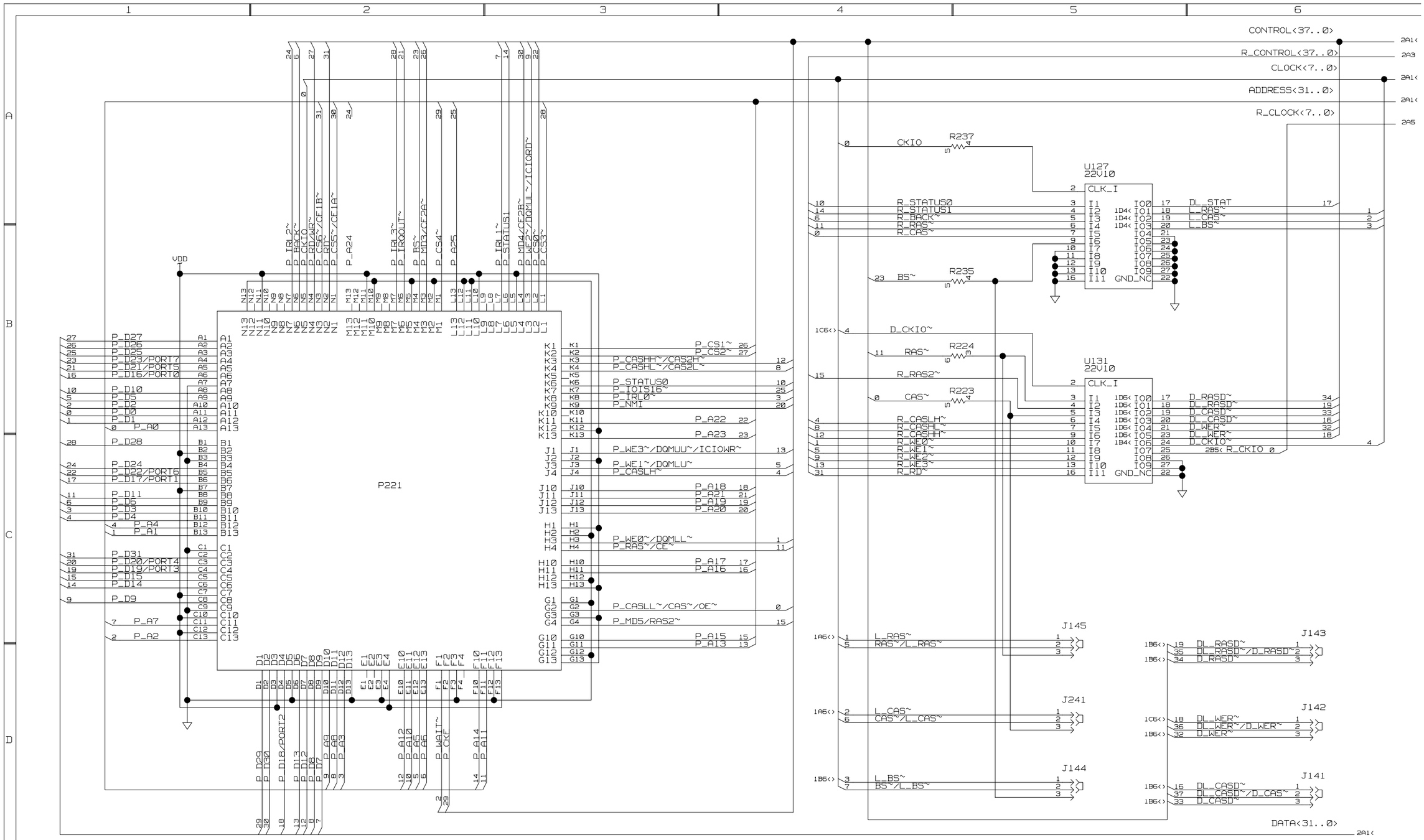


Component Locator Diagrams

The schematic diagram and circuit board component location illustrations have grids marked on them. The component lookup tables refer to these grids to help you locate a component. The circuit board illustration appears only once; its lookup table lists the diagram number of all diagrams on which the circuitry appears.

Some of the circuit board component location illustrations are expanded and divided into several parts to make it easier for you to locate small components. To determine which part of the whole locator diagram you are looking at, refer to the small locator key shown below. The gray block, within the larger circuit board outline, shows where that part fits in the whole locator diagram. Each part in the key is labeled with an identifying letter that appears in the figure titles under component locator diagrams.

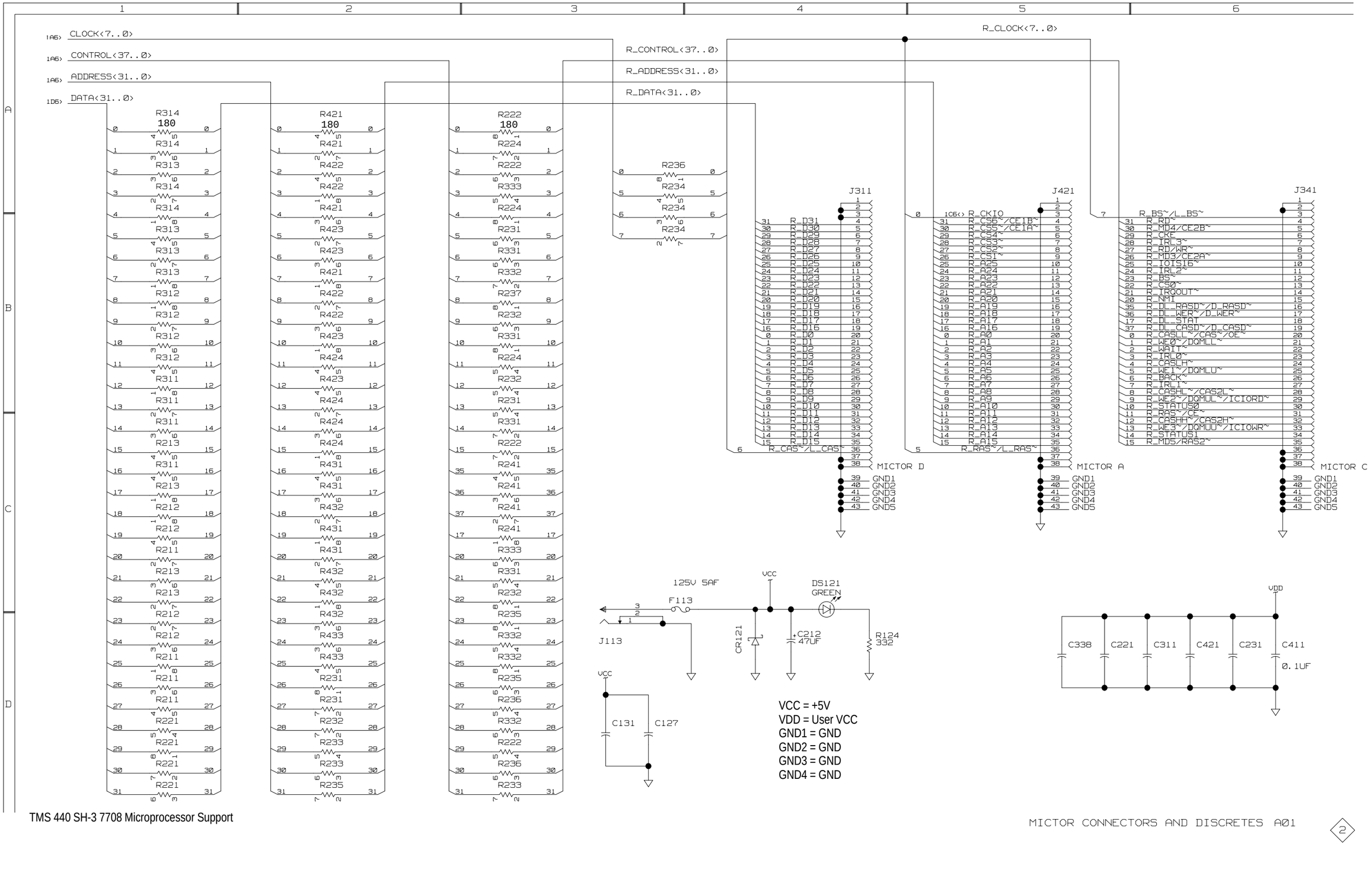




TMS 440 SH-3 7708 Microprocessor Support

UC, PAL LOGIC A01

1



TMS 440 SH-3 7708 Microprocessor Support

MICTOR CONNECTORS AND DISCRETES A01

Replaceable Mechanical Parts

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 440 SH-3 7708 microprocessor support.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
00779	AMP INC.	CUSTOMER SERVICE DEPT PO BOX 3608	HARRISBURG, PA 17105–3608
05276	ITT POMONA ELECTRONICS	1500 E NINTH ST	POMONA, CA 91766–3835
0KB05	NORTH STAR NAMEPLATE INC	5750 NE MOORE COURT	HILLSBORO, OR 97124–6474
14310	AULT INC	7300 BOONE AVE NORTH BROOKLINE PARK	MINNEAPOLIS, MN 55428
26742	METHODE ELECTRONICS INC	BACKPLAIN DIVISION 7444 WEST WILSON AVE	CHICAGO, IL 60656–4548
60381	PRECISION INTERCONNECT CORP.	16640 SW 72ND AVE	PORTLAND, OR 97224
61857	SAN–O INDUSTRIAL CORP	91–3 COLIN DRIVE	HOLBROOK, NY 11741
63058	BERG ELECTRONICS INC.	MCKENZIE SOCKET DIV 910 PAGE AVE	FREMONT, CA 94538–7340
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077–0001
S3109	FELLER U.S. CORPORATION	72 VERONICA AVE UNIT #4	SOMERSET, NJ 08873
TK1943	NEILSEN MANUFACTURING INC	3501 PORTLAND RD NE	SALEM, OR 97303
TK2449	SINGATRON ENTERPRISE CO LTD	13925 MAGNOLIA AVE	CHINO, CA 91710
TK2548	XEROX CORPORATION	14181 SW MILLIKAN WAY	BEAVERTON, OR 97005

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
5–1–0	010–0621–00			1	ADAPTER,PROBE:SH7708,PQFP–144 PINS, PROBE ADAPTER,TMS440 OPT 02	80009	010–0621–00
–1	671–4406–00			1	CIRCUIT BD ASSY:PQFP–144 PINS,SOLDERED,679–4406–00 TESTED,389–2579–00 WIRED,TMS440 OPT 02	80009	671–4406–00
–2	131–6134–01			3	CONN,RCPT:SMD,MICTOR,FEMALE,STR,38 POS,0.025 CTR,0.240 H,W/0.108 PCB HOLD DOWNS.PALLADIUM	00779	767054–1
–3	105–1089–00			3	LATCH ASSY:LATCH HOUSING ASSY,VERTICAL MOUNT,0.48 H X 1.24 L,W/PCB SINGLE CLIP,P6434	60381	105–1089–00
–4	131–4356–00			6	CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER,	26742	9618–302–50
–5	131–4530–00			6	CONN,HDR:PCB,MALE,STR,1X3,0.1 CTR,0.230 MLG X 0.120 TAIL, 30 GOLD, BD RETENTION	00779	104344–1
–6	131–5527–00			1	JACK,POWER DC:PCB,MALE,RTANG,2MM PIN,11MM H(0.433) X 3.5MM(0.137) TAIL,9MM(0.354) W,TIN,W/SWI	TK2449	DJ–005–A
–7	159–0059–00			1	FUSE,WIRE LEAD:5A,125V	61857	SPI–5A
–8	136–1324–00			2	SOCKET,PGA:PCB,FEMALE,144 POS,12 X 12,OPEN CENTER,SHORT PINS,PGA–144H101B1–1302–R	63058	PGA–144H101B1–1 302–R
–9	103–0415–00			1	ADAPTER,PQFP:TEST CLIP,144,PQFP–144(6151),TMS440 02	05276	6151
					STANDARD ACCESSORIES		
	071–0153–00			1	MANUAL,TECH INSTRUCTIONS,SH 7708;TMS440	80009	071–0153–00
	070–9803–00			1	MANUAL,TECH;TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070–9803–00
	161–0104–00			1	CA ASSY,PWR:3,18 AWG,98 L,250V/10AMP,98 INCH,RTANG,IEC320,RCPT X STR,NEMA 15–5P,W/CORD GRIP,	S3109	ORDER BY DESCRIPTION
	119–5061–01			1	POWER SUPPLY:25W,5V 5A,CONCENTRIC 2MM,90–265V,47–63 HZ IEC,15X8.6X5 CM, UL,CSA, TUV,IEC,SELF	14310	SW108KA0002F01
					OPTIONAL ACCESSORIES		
	P6434 *			3	P6434 MASS TERMINATION PROBE	80009	ORDER BY DESCRIPTION
	161–0104–05			1	CA ASSY,PWR:3,1.0MM SQ,250V/10A,2.5 METER,RTANG,IEC320,RCPT,AUSTRALIA,SAFTEY CONTROLLED (OPT A3)	S3109	ORDER BY DESCRIPTION
	161–0104–06			1	CA ASSY,PWR:3,1.0MM SQ 250V/10A,2.5 METER,RTANG,IEC320,RCPT, EUROPEAN,SAFTEY CONTROLLED(OPT A1)	S3109	ORDER BY DESCRIPTION
	161–0104–07			1	CA ASSY,PWR:1.0MM SQ 250V/10A,2.5 METER,RTANG,IEC320,RCPT X 13A,FUSED,UK PLUG,(13A FUSE),UNITED KINGDOM,SAFTEY CONTROL(OPT A2)	S3109	ORDER BY DESCRIPTION
	161–0167–00			1	CA ASSY,PWR:3,0.75MM SQ 250V/10A,2.5 METER,RTANG,IEC320,RCPT,SWISS,SAFTEY CONTROLLED(OPT A5)	S3109	ORDER BY DESCRIPTION

*** Check the P6434 manual for detailed replaceable part number information.**

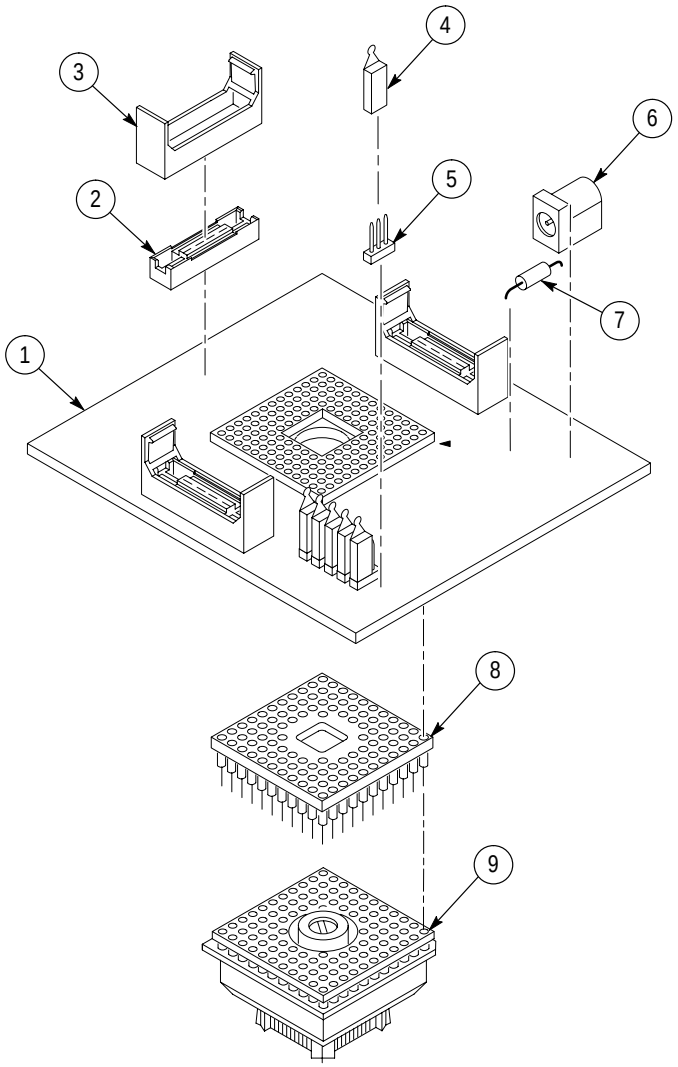


Figure 7–1: SH-3 7708 probe adapter exploded view

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