Instruction Manual

Tektronix

TMS 480
Am29030, Am29035 & Am29040
Microprocessor Support

070-9827-00

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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SOFTWARE WARRANTY

Tektronix warrants that the media on which this software product is furnished and the encoding of the programs on the media will be free from defects in materials and workmanship for a period of three (3) months from the date of shipment. If a medium or encoding proves defective during the warranty period, Tektronix will provide a replacement in exchange for the defective medium. Except as to the media on which this software product is furnished, this software product is provided “as is” without warranty of any kind, either express or implied. Tektronix does not warrant that the functions contained in this software product will meet Customer’s requirements or that the operation of the programs will be uninterrupted or error-free.

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In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period and make suitable arrangements for the performance of service. Customer shall be responsible for packaging and shipping the defective product to the service center designated by Tektronix, with shipping charges prepaid. Tektronix shall pay for the return of the product to Customer if the shipment is to a location within the country in which the Tektronix service center is located. Customer shall be responsible for paying all shipping charges, duties, taxes, and any other charges for products returned to any other locations.

This warranty shall not apply to any defect, failure or damage caused by improper use or improper or inadequate maintenance and care. Tektronix shall not be obligated to furnish service under this warranty a) to repair damage resulting from attempts by personnel other than Tektronix representatives to install, repair or service the product; b) to repair damage resulting from improper use or connection to incompatible equipment; c) to repair any damage or malfunction caused by the use of non-Tektronix supplies; or d) to service a product that has been modified or integrated with other products when the effect of such modification or integration increases the time or difficulty of servicing the product.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

Do not apply a potential to any terminal, including the common terminal, that exceeds the maximum rating of that terminal.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING High Voltage

Protective Ground (Earth) Terminal

CAUTION Refer to Manual

Double Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface: Microprocessor Support Documentation

This instruction manual contains specific information about the TMS 480 29030/35/40 microprocessor support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor support packages on the logic analyzer for which the TMS 480 29030/35/40 support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor support packages is included with each product. Each logic analyzer has basic information that describes how to perform tasks common to support packages on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing disassembled data
- Using the probe adapter

Manual Conventions

This manual uses the following conventions:

- The term disassembler refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase "information on basic operations" refers to online help, an installation manual, or a basic operations of microprocessor supports user manual.
- In the information on basic operations, the term XXX or P54C used in field selections and file names must be replaced with 2903X. This is the name of the microprocessor in field selections and file names you must use to operate the 29030/35/40 support.
- The term system under test (SUT) refers to the microprocessor-based system from which data will be acquired.

- The term logic analyzer refers to the Tektronix logic analyzer for which this product was purchased.
- The term module refers to a 102/136-channel or a 96-channel module.
- 2903X refers to all supported variations of the Am29030, Am29035 and Am29040 microprocessors unless otherwise noted.
- An asterisk (*) following a signal name indicates an active low signal.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The manual set provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or, contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Contact your local Tektronix distributor or sales office. Or, visit our web site for a listing of worldwide service locations. http://www.tek.com
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000

Getting Started

This chapter provides information on the following topics and tasks:

- A description of the TMS 480 microprocessor support package
- Logic analyzer software compatibility
- Logic analyzer routing
- Support restrictions
- How to configure the probe adapter
- How to connect to the system under test (SUT)
- How to apply power to and remove power from the probe adapter

Support Description

The TMS 480 microprocessor support package disassembles data from systems that are based on the Advanced Micro Devices 29030/35/40 microprocessor. The support runs on a compatible Tektronix logic analyzer equipped with a 102/136-channel module or a 96-channel module.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 480 microprocessor support.

Table 1–1 shows the microprocessors and packages from which the TMS 480 support can acquire and disassemble data.

Table 1–1: Supported microprocessors

Name	Package	Clock speed
Am29030	PGA	33 MHz
Am29035	PQFP*	16 MHz
Am29040	PGA and CQFP*	50 MHz

* **A PGA-to-QFP converter clip is not available for the TMS 480 product. However, you can connect directly to the microprocessor signals and still use the disassembler.**

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Mechanical Parts* chapter.

To use this support efficiently, you need to have the items listed in the information on basic operations as well as the following manuals;

- The *Am29030/35 User's Manual*, Advanced Micro Devices, 1991.
- The *Am29040 User's Manual*, Advanced Micro Devices, 1994.

Information on basic operations also contains a general description of supports.

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

To use the TMS 480 support, the Tektronix logic analyzer must be equipped with either a 102/136-channel module or a 96-channel module at a minimum. The module must be equipped with enough probes to acquire channel and clock data from signals in your 29030/35/40-based system.

Refer to information on basic operations to determine how many modules and probes the logic analyzer needs to meet the channel requirements.

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor supports in the information on basic operations as they pertain to your SUT.

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other 29030/35/40 support requirements and restrictions.

System Clock Rate. The support product supports the Am29030 microprocessor at speeds of up to 33 MHz[1], the Am29035 microprocessor at speeds of up to 16 MHz[1], and the Am29040 microprocessor at speeds of up to 50 MHz[1].

Am29035 Microprocessor Support. A PGA-to-PQFP converter clip is not available with the TMS 480 product. However, you can connect directly to the 29035 signals in your SUT, and still use the 2903X support setup and disassembler.

[1] **Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest devices supported.**

Am29040 Microprocessor Support. A PGA-to-CQFP converter clip is not available with the TMS 480 product for the 29040 microprocessor in a CQFP package. However, you can connect directly to the 29040 signals in your SUT, and still use the 2903X support setup and disassembler.

Disabling the Instruction Cache. To disassemble acquired data, you must disable the internal instruction cache. Disabling the cache makes all instruction prefetches visible on the bus so they can be acquired and disassembled.

Little-Endian Byte Ordering. The TMS 480 does not support Little-Endian byte ordering.

Burst Access Mode. The TMS 480 does not support the Burst Access mode for interleaved memories.

Slave Cancellation of Burst Access Mode. The TMS 480 does not support slave cancellation of the Burst Access mode.

Configuring the Probe Adapter

The probe adapter does not require any configuration.

Connecting to a System Under Test

Before you connect to the SUT, you must connect the probes to the module. Your SUT must also have a minimum amount of clear space surrounding the microprocessor to accommodate the probe adapter. Refer to the *Specifications* chapter in this manual for the required clearances.

The channel and clock probes shown in this chapter are for a 102/136-channel module. The probes will look different if you are using a 96-channel module.

The general requirements and restrictions of microprocessor supports in the information on basic operations shows the vertical dimensions of a channel or clock probe connected to square pins on a circuit board.

PGA Probe Adapter

To connect the logic analyzer to a SUT using a PGA probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probe adapter, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor and probe adapter.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. Then, touch any of the ground pins of the probe adapter to discharge stored static electricity from the probe adapter.
3. Place the probe adapter onto the antistatic shipping foam to support the probe as shown in Figure 1–1. This prevents the circuit board from flexing and the socket pins from bending.
4. Remove the microprocessor from your SUT.
5. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on the microprocessor.

CAUTION. *Failure to correctly place the microprocessor into the probe adapter might permanently damage the microprocessor once power is applied.*

6. Place the microprocessor into the probe adapter as shown in Figure 1–1.

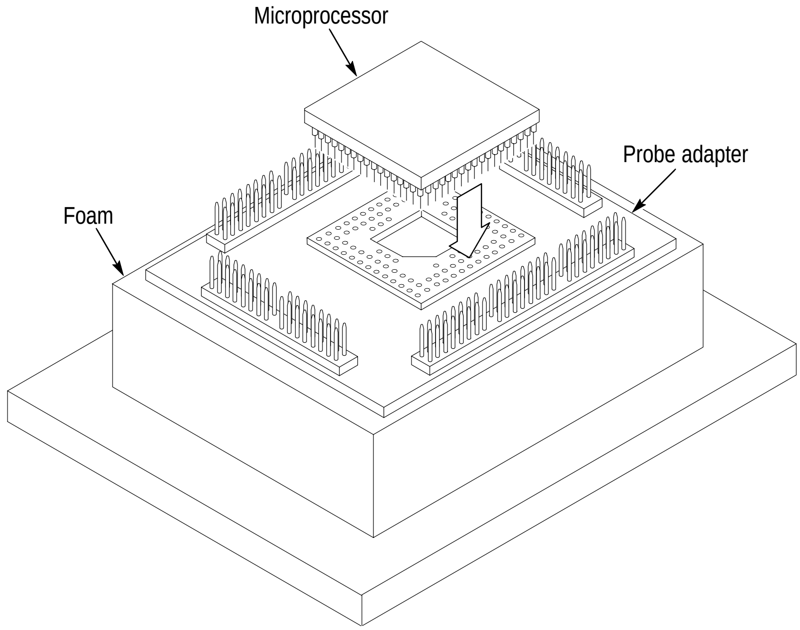

Figure 1–1: Placing a microprocessor into a PGA probe adapter

7. Connect the channel and clock probes to the probe adapter as shown in Figure 1–2. Match the channel groups and numbers on the probe labels to the corresponding pins on the probe adapter. Match the ground pins on the probes to the corresponding pins on the probe adapter.

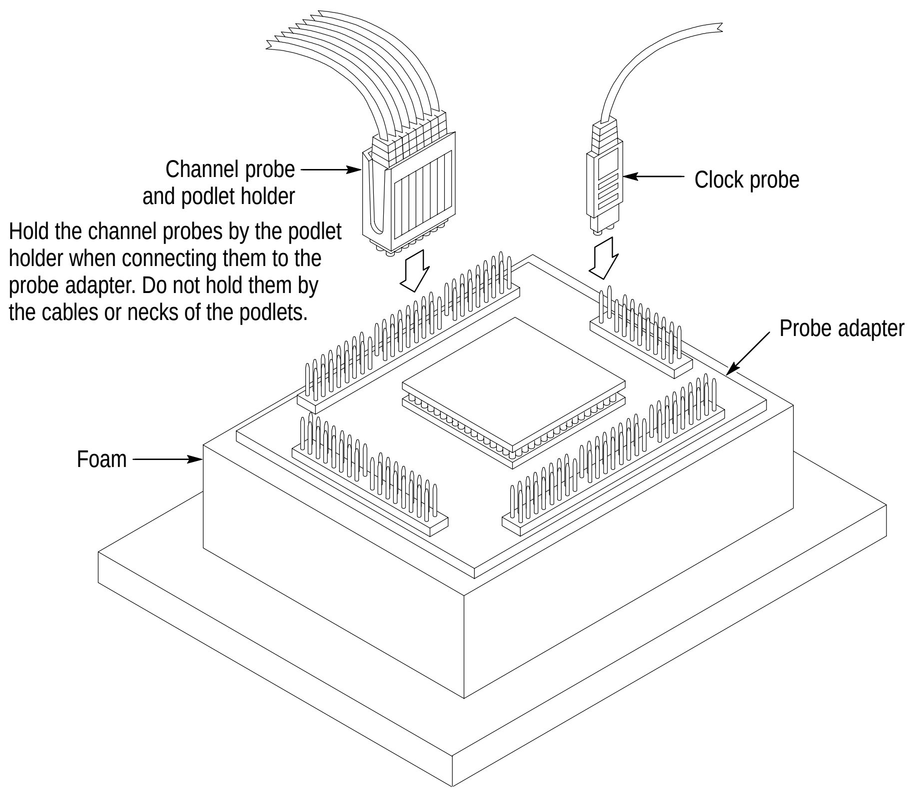

Figure 1–2: Connecting probes to a PGA probe adapter

8. Line up the pin A1 indicator on the probe adapter board with the pin A1 indicator on your SUT.

9. Place the probe adapter onto the SUT as shown in Figure 1–3.

NOTE. *You might need to stack one or more replacement sockets between the SUT and the probe adapter to provide sufficient vertical clearance from adjacent components. However, keep in mind that this might increase loading, which can reduce the electrical performance of your probe adapter.*

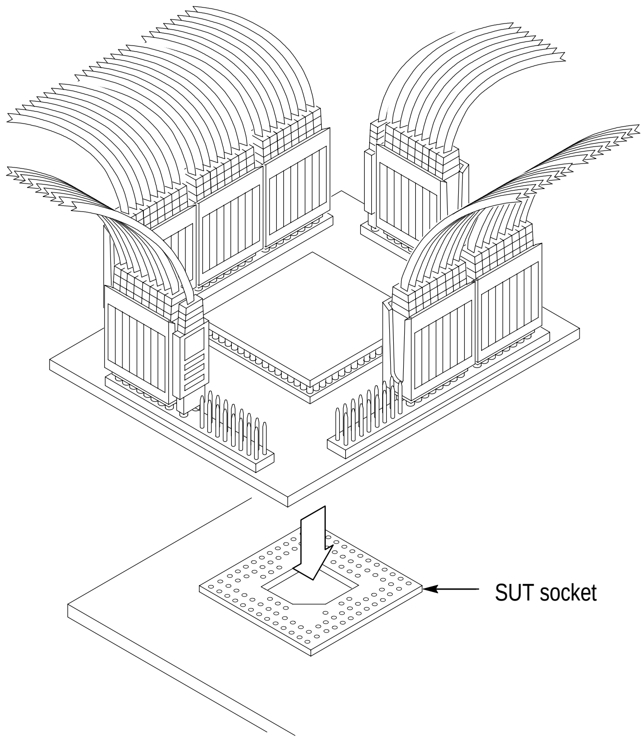

Figure 1–3: Placing a PGA probe adapter onto the SUT

Without a Probe Adapter

You can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your SUT.

To connect the probes to 29030/35/40 signals in the SUT using a test clip, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the microprocessor.

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2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from it.

3. Use Table 1–2 to connect the channel probes to 29030/35/40 signal pins on the test clip or in the SUT.

   Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip.

Table 1–2: 29030/35/40 signal connections for channel probes

Section:channel	29030/35/40 signal	Section:channel	29030/35/40 signal
A3:7	A31	D3:7	D31
A3:6	A30	D3:6	D30
A3:5	A29	D3:5	D29
A3:4	A28	D3:4	D28
A3:3	A27	D3:3	D27
A3:2	A26	D3:2	D26
A3:1	A25	D3:1	D25
A3:0	A24	D3:0	D24
A2:7	A23	D2:7	D23
A2:6	A22	D2:6	D22
A2:5	A21	D2:5	D21
A2:4	A20	D2:4	D20
A2:3	A19	D2:3	D19
A2:2	A18	D2:2	D18
A2:1	A17	D2:1	D17
A2:0	A16	D2:0	D16
A1:7	A15	D1:7	D15
A1:6	A14	D1:6	D14
A1:5	A13	D1:5	D13
A1:4	A12	D1:4	D12
A1:3	A11	D1:3	D11
A1:2	A10	D1:2	D10
A1:1	A9	D1:1	D9
A1:0	A8	D1:0	D8
A0:7	A7	D0:7	D7
A0:6	A6	D0:6	D6
A0:5	A5	D0:5	D5
A0:4	A4	D0:4	D4
A0:3	A3	D0:3	D3
A0:2	A2	D0:2	D2

Table 1–2: 29030/35/40 signal connections for channel probes (cont.)

Section:channel	29030/35/40 signal	Section:channel	29030/35/40 signal
A0:1	A1	D0:1	D1
A0:0	A0	D0:0	D0
C3:7	STAT0	C1:7	RESET*
C3:6	OPT2	C1:6	TRAP1*
C3:5	OPT1	C1:5	TRAP0*
C3:4	OPT0	C1:4	INTR3*
C3:3	IO/M*	C1:3	INTR2*
C3:2	R/W*	C1:2	INTR1*
C3:1	RDN*	C1:1	INTR0*
C3:0	I/D*	C1:0	WARN*
C2:7	LOCK*	C0:7	IDP3
C2:6	ERR*	C0:6	IDP2
C2:5	STAT2	C0:5	BWE3*
C2:4	STAT1	C0:4	BWE2*
C2:3	REQ*	C0:3	BWE1*
C2:2	RDY*	C0:2	BWE0*
C2:1	BURST*	C0:1	IDP1
C2:0	BGRT*	C0:0	IDP0

Table 1–3 shows the clock probes and the 29030/35/40 signal to which they must connect for disassembly to be correct.

Table 1–3: 29030/35/40 signal connections for clock probes

Section:channel	29030/35/40 signal
CK:1	RDN*=
CK:0	MEMCLK

4. Align pin 1 or A1 of your test clip with the corresponding pin 1 or A1 of the 29030/35/40 microprocessor in your SUT and attach the clip.

Setting Up the Support

This section provides information on how to set up the support. Information covers the following topics:

- Channel group definitions
- Clocking options
- Symbol table files

Remember that the information in this section is specific to the operations and functions of the TMS 480 29030/35/40 support on any Tektronix logic analyzer for which it can be purchased. Information on basic operations describes general tasks and functions.

Before you acquire and disassemble data, you need to load the support and specify setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the 29030/35/40 support are Address, Data, Control, Intr, Bwrtenbl, and Misc. If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 3–4.

Clocking Options

The TMS 480 support offers a microprocessor-specific clocking mode for the 29030/35/40 microprocessor. This clocking mode is the default selection whenever you load the 2903X support.

A description of how cycles are sampled by the module using the support and probe adapter is found in the *Specifications* chapter.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general purpose analysis.

The clocking options for the TMS 480 support are: Alternate Bus Master Cycles and Narrow Access Width.

Alternate Bus Master Cycles

An Alternate Bus Master cycle is defined as the 29030/35/40 microprocessor giving up the bus to an alternate device (a DMA device or another microprocessor). These types of cycles are acquired when you select Included.

Narrow Access Width

A narrow access read can be 8- or 16-bits wide. You can select an 8-Bit Narrow Read interface or a 16-Bit Narrow Read interface.

Symbols

The TMS 480 support supplies three symbol table files. The 2903X_Ctrl file replaces specific Control channel group values with symbolic values when Symbolic is the radix for the channel group.

Table 2–1 shows the name, bit pattern, and meaning for the symbols in the file 2903X_Ctrl, the Control channel group symbol table.

Table 2–1: Control group symbol table definitions

Symbol	Control group value																Meaning
	R/W#	IO/MEM#	I/D#	BURST#	REQ#	RDY#	ERR#	OPT2	OPT1	OPT0	STAT2	STAT1	STAT0	LOCK#	RDN#	BGRT#	
FETCH_WD	1	0	1	X	0	0	1	X	X	X	X	X	X	X	1	0	Opcode read from a 32 bit memory area
FETCH_NR	1	0	1	X	0	0	1	X	X	X	X	X	X	X	0	0	Opcode read from a 8/16 bit memory area
READ	1	0	0	1	0	0	1	0	0	0	X	X	X	1	X	X	A word–length read from a 32 bit memory area
WRITE	0	0	0	1	0	0	1	0	0	0	X	X	X	1	X	X	A word–length write to a 32 bit memory area
IO_READ	1	1	0	1	0	0	1	X	X	X	X	X	X	1	X	X	A read from an I/O port
IO_WRITE	0	1	0	1	0	0	1	X	X	X	X	X	X	1	X	X	A write to an I/O port
BURST_RD	1	X	0	0	0	0	1	X	X	X	X	X	X	X	X	X	A Burst read from an I/O or Memory
BURST_WR	0	X	0	0	0	0	1	X	X	X	X	X	X	X	X	X	A Burst write to an I/O or Memory
NAR_RD	1	0	0	1	0	0	1	0	X	X	X	X	X	1	0	X	A 32 bit or 16 bit or 8 bit read from a narrow memory area i.e 8/16 bit Memory
HW_WR	0	0	0	1	0	0	1	0	1	0	X	X	X	1	X	X	A 16 bit write to a 32 bit or 16 bit memory region
BYTE_WR	0	0	0	1	0	0	1	0	0	1	X	X	X	1	X	X	A 8 bit write to a 32 bit or 16 bit or 8 bit memory region
LKD_IO_RD	1	1	0	1	0	0	1	X	X	X	X	X	X	0	X	X	A locked data read from an I/O port
LKD_IO_WR	0	1	0	1	0	0	1	X	X	X	X	X	X	0	X	X	A locked data write to an I/O port
LKD_M_RD	1	0	0	1	0	0	1	X	X	X	X	X	X	0	X	X	A locked data read from an Memory region
LKD_M_WR	0	0	0	1	0	0	1	X	X	X	X	X	X	0	X	X	A locked data write to a Memory region
ABM_RD	1	X	0	X	1	0	1	X	X	X	X	X	X	X	X	1	An Alternate Bus Master read from memory or I/O
ABM_WR	0	X	0	X	1	0	1	X	X	X	X	X	X	X	X	1	An Alternate Bus Master write to memory or I/O
HALT/STEP	X	X	X	X	X	X	X	X	X	X	0	0	0	X	X	0	Microprocessor is in Halted/Single Step mode
WAIT	X	X	X	X	X	X	X	X	X	X	0	1	1	X	X	0	Microprocessor is in Wait mode

Table 2–2 shows the name, bit pattern, and meaning for symbols in the file 2903X_Bwrtenbl, the Bwrtenbl (byte write enable) group symbol table.

Table 2–2: Bwrtenbl group symbol table definitions

Symbol	Bwrtenbl group value BWE3# IBWE2# BWE1# BWE0#	Meaning (Big-Endian access)
LSB_WR	0 1 1 1	A least significant byte write (such as a byte 0 write)
LSB1_WR	1 0 1 1	A byte 1 write
LSB2_WR	1 1 0 1	A byte 2 write
MSB_WR	1 1 1 0	A most significant byte write (such as a byte 3 write)
LSHW_WR	0 0 1 1	A least significant half-word write (such as a byte 0 and byte 1 write)
MSHW_WR	1 1 0 0	A most significant half-word write (such as a byte 2 and byte 3 write)
WRD_WR	0 0 0 0	A word-length write

Table 2–3 shows the name, bit pattern, and meaning for symbols in the file 2903X_Intr, the Intr (Interrupt) group symbol table.

Table 2–3: Intr group symbol table definitions

Symbol	Intr group value TRAP1# TRAP0# INTR3# INTR2# INTR1# INTR0# WARN#	Meaning
TRAP1	0 X X X X X X	A TRAP1 vector has occured
TRAP0	X 0 X X X X X	A TRAP0 vector has occured
INTR3	X X 0 X X X X	A INTR3 vector has occured
INTR2	X X X 0 X X X	A INTR2 vector has occured
INTR1	X X X X 0 X X	A INTR1 vector has occured
INTR0	X X X X X 0 X	A INTR0 vector has occured
WARN	X X X X X X 0	A WARN vector has occured

Information on basic operations describes how to use symbolic values for triggering and for displaying other channel groups symbolically, such as the Address channel group.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. Information covers the following topics and tasks:

- Acquiring data
- Viewing disassembled data in various display formats
- Cycle type labels
- Changing how data is displayed
- Changing disassembled cycles with the mark cycles function

Acquiring Data

Once you load the 2903X support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the basic operations user manual.

Viewing Disassembled Data

You can view disassembled data in four display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

***NOTE**. Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–9.*

The default display format shows the Address, Data, and Control channel group values for each sample of acquired data.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–4 shows these special characters and strings, and gives a definition of what they represent.

Table 2–4: Meaning of special characters in the display

Character or string displayed	Meaning
≫ or m	The instruction was manually marked as a program fetch
#	Indicates an immediate value
t	Indicates the number shown is in decimal, such as #12t
??	Indicates one register number that is not available
?????	Indicates insufficient data; the instruction cannot be disassembled

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–5 shows these cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors will be labeled with the vector name.

Table 2–5: Cycle type definitions

Cycle type	Definition
(WD_RD, PGMD_WD)	OPT programmed to read 32-bit from 32-bit memory
(HW_RD, PGMD_WD)	OPT programmed to read 32-bit from 16-bit memory
(BYTE_RD, PGMD_WD)	OPT programmed to read 32-bit from 8-bit memory
(WD_RD, PGMD_HW)	OPT programmed to read 16-bit from 32-bit memory
(HW_RD, PGMD_HW)	OPT programmed to read 16-bit from 16-bit memory
(BYTE_RD, PGMD_HW)	OPT programmed to read 16-bit from 8-bit memory
(WD_RD, PGMD_BYTE)	OPT programmed to read; 8-bit from 32-bit memory
(HW_RD, PGMD_BYTE)	OPT programmed to read; 8-bit from 16-bit memory
(BYTE_RD, PGMD_BYTE)	OPT programmed to read 8-bit from 8-bit memory
(WD_WR, PGMD_WD)	OPT programmed to write 32-bit
(HW_WR, PGMD_HW)	OPT programmed to write 16-bit
(BYTE_WR, PGMD_BYTE)	OPT programmed to write 8-bit
(I/O_READ)	Data Read from I/O port
(I/O_WRITE)	Data write to I/O port
(LKD_I/O_RD)	Locked data read from I/O port
(LKD_I/O_WR)	Locked data write to I/O port
(LKD_M_RD)	Locked data read from memory
(LKD_M_WR)	Locked data write to memory
(BURST_RD)	Data read from memory in burst

Table 2–5: Cycle type definitions (cont.)

Cycle type	Definition
(BURST_WR)	Data write to memory in burst
(ALT_BM_RD)	Data read by another processor
(ALT_BM_WR)	Data write by another processor
(HALT/STEP)	Processor is halted/single step mode
(WAIT)	Processor is in wait mode
(FLUSH)†	Fetch cycle not executed
(EXTENSION)†	Data read from program space to complete opcode fetch sequence
(UNKNOWN)	The combinations of control bits is unexpected and/or unrecognized

† **Computed cycle types.**

Figure 2–1 shows an example of the Hardware display.

```
  1          2        3          4                                                   5
  Sample  Address   Data      Mnemonic                                               Timestamp
--------------------------------------------------------------------------------------------
     180  0000002C  03------  ( BURST_RD )                                         250 ns
     181  0000002D  FF------  ( BURST_RD )                                         250 ns
     182  00000030  02------  ( BYTE_RD PGMD_HW )                                  250 ns
     183  00000031  01------  ( BYTE_RD PGMD_HW )                                  250 ns
     184  8000002F  80000B00  ( LKD_M_RD )                                         500 ns
     185  8000002F  FFFFFFFF  ( LKD_M_WR )                                         380 ns
     186  800001C0  03FF640A  CONST    GR100,0000FF0A                              370 ns
     187  800001C4  02806400  CONSTH   GR100,80000000                              120 ns
     188  800001C8  1E2A6964  STORE    0,2A,GR105,GR100                            130 ns
     189  800001CC  70400101  NOP                                                  130 ns
     190  8000FF0A  800A800A  ( HW_WR PGMD_HW )                                    490 ns
     191  800001D0  1E296964  STORE    0,29,GR105,GR100                            380 ns
     192  800001D4  86FE80C1  SRA      LR126,LR0,LR65                              130 ns
     193  800001D8  1E286964  STORE    0,28,GR105,GR100                            120 ns
     194  800001DC  A000000A  JMP      80000204                                    120 ns
     195  8000FF0A  0A0A0A0A  ( BYTE_WR PGMD_BYTE )                                380 ns
     196  800001E0  70400101  NOP                                                  380 ns
     197  800001E4  69610000  ( FLUSH )                                            120 ns
     198  800001E8  6A616184  ( FLUSH )                                            130 ns
     199  800001EC  6C616184  ( FLUSH )                                            120 ns
     200  8000FF0A  800A800A  ( WD_WR PGMD_WD )                                    370 ns
     201  80000200  70400101  ( FLUSH )                                            380 ns
     202  80000204  030F40AA  CONST    GR64,00000FAA                               130 ns
```

Figure 2–1: Hardware display format

1 **Sample Column.** Lists the memory locations for the acquired data.

2 **Address Group.** Lists data from channels connected to the 29030/35/40 address bus.

3 **Data Group.** Lists data from channels connected to the 29030/35/40 data bus.

4 **Mnemonics Column.** Lists the disassembled instructions and cycle types.

5 **Timestamp.** Lists the timestamp values when a timestamp selection is made. Information on basic operations describes how you can select a timestamp.

Software Display Format

The Software display format shows only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Read extensions will be used to disassemble the instruction, but will not be displayed as a separate cycle in the Software display format. Data reads and writes are not displayed.

Control Flow Display Format

The Control Flow display format shows only the first fetch of instructions that change the flow of control.

Instructions that generate a change in the flow of control in the 29030/35/40 microprocessor are as follows:

CALL	IRET	JMP
CALLI	IRETINV	JMPI

Instructions that might generate a change in the flow of control in the 29030/35/40 microprocessor are as follows:

JMPF	JMPFI	JMPTI
JMPFDEC	JMPT	

Subroutine Display Format

The Subroutine display format shows only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

Instructions that generate a subroutine call or a return in the 29030/35/40 microprocessor are as follows:

CALL	IRET
CALLI	IRETINV

Changing How Data is Displayed

There are common fields and features that allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

You can make selections unique to the 29030/35/40 support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception vectors

There are no optional fields for this support package. Refer to the information on basic operations for descriptions of common fields.

Optional Display Selections

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways:

- Select the type of microprocessor to disassemble data from
- Select the width of narrow access reads
- Specify the starting address of the exception vector table

The 29030/35/40 microprocessor support product has three additional fields: Processor Select, Select Narrow Access Width, and Vector Area Base. These fields appear in the area indicated in the basic operations user manual.

Processor Select. You can set up the application to disassemble data from one of the following microprocessor: 29030, 29035, or 29040.

Select Narrow Access Width. You can define the width of narrow access reads as 8 bits or 16 bits.

Vector Area Base. You can specify the starting address of the vector table in hexadecimal. The default starting address is 0x00000000.

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it to one of the following cycle types:

- Opcode (the first word of an instruction)
- Flush (an opcode or extension that is fetched but not executed)

```
Opcode
Flush
```

```
Undo Mark
```

Information on basic operations contains more details on marking cycles.

Displaying Exception Vectors

The disassembler can display exception vectors.

You can relocate the vector table by entering the starting address in the Vector Area Base field. The Vector Area Base field provides the disassembler with the offset address; enter an eight-digit hexadecimal value corresponding to the offset of the base address of the vector table.

You can make these selections in the Disassembly property page (the Disassembly Format Definition overlay).

Table 2–6 lists the 29030/35/40 exception vectors for the Real Addressing mode.

Table 2–6: Exception vectors

Vector number	Displayed exception name
0	(Illegal Opcode)
1	(Unaligned Access)
2	(Out of Range)
3	(Reserved)
4	(Reserved/Parity Error)†
5	(Protection Violation)
6	(Instruction Access Exception)
7	(Data Access Exception)
8	(User – Mode Instruction TLB Miss)
9	(User – Mode Data TLB miss)
10	(Supervisor – Mode Instruction TLB Miss)
11	(Supervisor – Mode Data TLB Miss)
12	(Instruction MMU Protection Violation)
13	(Data MMU Protection Violation)
14	(Timer)

Table 2–6: Exception vectors (cont.)

Vector number	Displayed exception name
15	(Trace)
16	(INTR0*)
17	(INTR1*)
18	(INTR2*)
19	(INTR3*)
20	(TRAP0*)
21	(TRAP1*)
22	(Floating Point Exception)
23	(Reserved)
24–29	(Reserved for Instruction Emulation, opcodes D8 to DD)
30	(MULTM/Reserved)†
31	(MULTMU/Reserved)†
32	(MULTIPLY/Reserved)†
33	(DIVIDE)
34	(MULTIPLU)
35	(DIVIDU)
36	(CONVERT)
37	(SQRT)
38	(CLASS)
39-41	(Reserved for Instruction Emulation, opcodes E7 to E9)
42	(FEQ)
43	(DEQ)
44	(FGT)
45	(DGT)
46	(FGE)
47	(DGE)
48	(FADD)
49	(DADD)
50	(FSUB)
51	(DSUB)
52	(FMUL)
53	(DMUL)

Table 2–6: Exception vectors (cont.)

Vector number	Displayed exception name
54	(FDIV)
55	(DDIV)
56	(Reserved for Instruction Emulation, opcode F8)
57	(FDMUL)
58-63	(Reserved for Instruction Emulation, opcodes FA to FF)
64-255	(ASSERT and EMULATE Instruction Traps, vector number specified by instruction)

† **Vector name displayed based on the selection in the Processor field of the Disassembly Format Definition overlay or the Processor Support submenu.**

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided so you can see an example of how your 29030/35/40 microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your SUT.

Information on basic operations describes how to view the file.

Specifications

This chapter contains the following information:

- Probe adapter description
- Specification tables
- Dimensions of the probe adapter
- Channel assignment tables
- Description of how the module acquires 29030/35/40 signals
- List of other accessible microprocessor signals and extra probe channels

Probe Adapter Description

The probe adapter is nonintrusive hardware that allows the logic analyzer to acquire data from a microprocessor in its own operating environment with little effect, if any, on that system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and a socket for a 29030/35/40 microprocessor. The probe adapter connects to the microprocessor in the SUT. Signals from the microprocessor-based system flow from the probe adapter to the channel groups and through the probe signal leads to the module.

The probe adapter accommodates the Advanced Micro Devices 29030 or 29040 microprocessor in a 145-pin PGA package. You will need to devise a way to connect directly to the signals for the 29035 microprocessor in a PQFP package and the 29040 microprocessor in a CQFP package.

Configuration

The probe adapter does not require any configuration.

Specifications

These specifications are for a probe adapter connected between a compatible Tektronix logic analyzer and a SUT. Table 3–1 shows the electrical requirements the SUT must produce for the support to acquire correct data.

In Table 3–1, for the 102/136-channel module, one podlet load is 20 kΩ in parallel with 2 pF. For the 96-channel module, one podlet load is 100 kΩ in parallel with 10 pF.

Table 3–1: Electrical specifications

Characteristics	Requirements	
SUT DC power requirements		
Voltage & current	Probe adapter does not require power	
SUT clock rate		
29030	Max. 33 MHz	
29035	Max. 16 MHz	
29040	Max. 50 MHz	
Minimum setup time required, all signals	5 ns	
Minimum hold time required, all signals	0 ns	
	Specification	
Measured typical SUT signal loading	**AC load**	**DC load**
A31-A0, ID31-ID0, R/W*, IO/M*, I/D*, BURST*, REQ*, RDY*, ERR*, OPT2-OPT0, STAT2-STAT0, LOCK*, BGRT*, TRAP1*, TRAP0*, INTR3*-INTR0*, WARN*, IDP3-IDP0, MEMCLK BWE3*-BWE0*	1 podlet	1 podlet
RDN*	2 podlets	2 podlets

Table 3–2 shows the environmental specifications.

Table 3–2: Environmental specifications*

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F)†
Minimum operating	0° C (+32° F)
Non-operating	–55° C to +75° C (–67° to +167° F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum
Electrostatic immunity	The probe adapter is static sensitive

* **Designed to meet Tektronix standard 062-2847-00 class 5.**

† **Not to exceed 29030/35/40 microprocessor thermal considerations. Forced air cooling might be required across the CPU.**

Table 3–3 shows the certifications and compliances that apply to the probe adapter.

Table 3–3: Certifications and compliances

EC Compliance	There are no current European Directives that apply to this product.

Figure 3–1 shows the dimensions of the probe adapter. Information on basic operations shows the vertical clearance of the channel and clock probes when connected to a probe adapter.

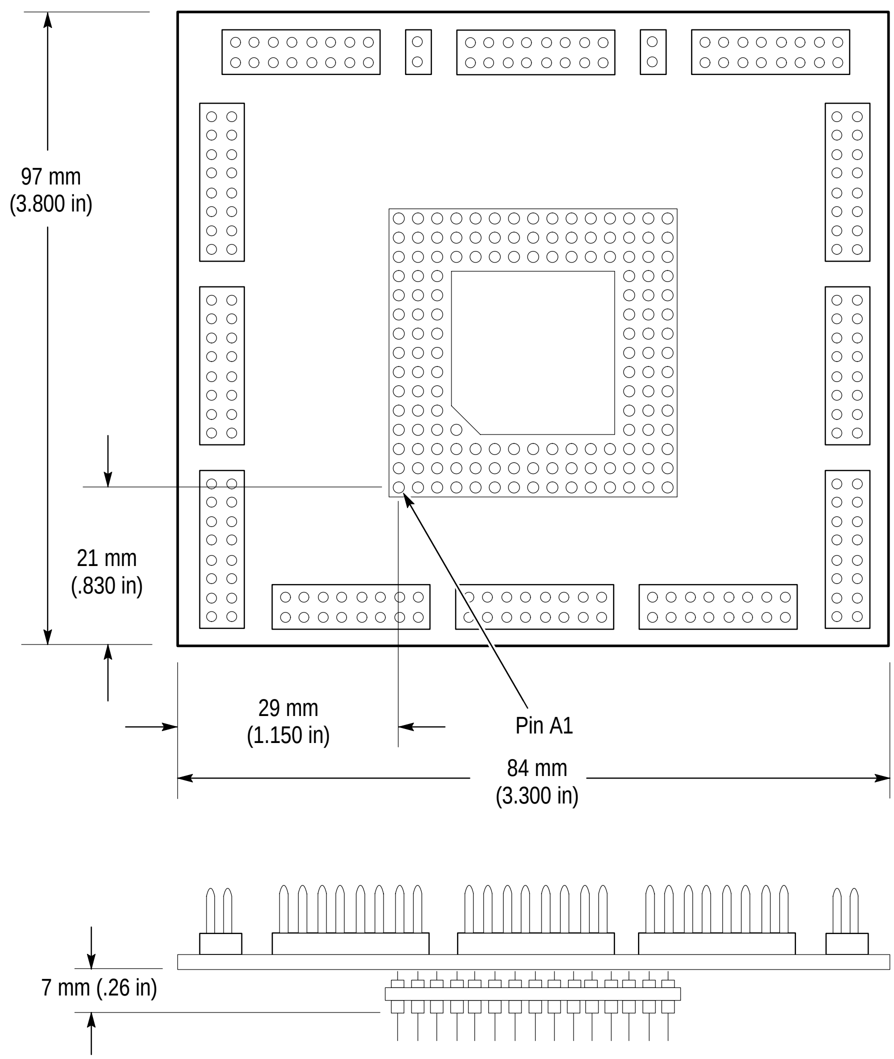


Figure 3–1: Dimensions of the probe adapter

Channel Assignments

Channel assignments shown in Table 3–4 through Table 3–10 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- An asterisk (*) following a signal name indicates an active low signal.

Table 3–4 shows the probe section and channel assignments for the Address group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–4: Address group channel assignments

Bit order	Section:channel	29030/35/40 signal name
31	A3:7	A31
30	A3:6	A30
29	A3:5	A29
28	A3:4	A28
27	A3:3	A27
26	A3:2	A26
25	A3:1	A25
24	A3:0	A24
23	A2:7	A23
22	A2:6	A22
21	A2:5	A21
20	A2:4	A20
19	A2:3	A19
18	A2:2	A18
17	A2:1	A17
16	A2:0	A16
15	A1:7	A15
14	A1:6	A14
13	A1:5	A13
12	A1:4	A12
11	A1:3	A11
10	A1:2	A10
9	A1:1	A9

Table 3–4: Address group channel assignments (cont.)

Bit order	Section:channel	29030/35/40 signal name
8	A1:0	A8
7	A0:7	A7
6	A0:6	A6
5	A0:5	A5
4	A0:4	A4
3	A0:3	A3
2	A0:2	A2
1	A0:1	A1
0	A0:0	A0

Table 3–5 shows the probe section and channel assignments for the Data group and the microprocessor signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–5: Data group channel assignments

Bit order	Section:channel	29030/35/40 signal name
31	D3:7	ID31
30	D3:6	ID30
29	D3:5	ID29
28	D3:4	ID28
27	D3:3	ID27
26	D3:2	ID26
25	D3:1	ID25
24	D3:0	ID24
23	D2:7	ID23
22	D2:6	ID22
21	D2:5	ID21
20	D2:4	ID20
19	D2:3	ID19
18	D2:2	ID18
17	D2:1	ID17
16	D2:0	ID16
15	D1:7	ID15
14	D1:6	ID14

Table 3–5: Data group channel assignments (cont.)

Bit order	Section:channel	29030/35/40 signal name
13	D1:5	ID13
12	D1:4	ID12
11	D1:3	ID11
10	D1:2	ID10
9	D1:1	ID9
8	D1:0	ID8
7	D0:7	ID7
6	D0:6	ID6
5	D0:5	ID5
4	D0:4	ID4
3	D0:3	ID3
2	D0:2	ID2
1	D0:1	ID1
0	D0:0	ID0

Table 3–6 shows the probe section and channel assignments for the Control group and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–6: Control group channel assignments

Bit order	Section:channel	29030/35/40 signal name
15	C3:2	R/W*
14	C3:3	IO/M*
13	C3:0	I/D*
12	C2:1	BURST*
11	C2:3	REQ*
10	C2:2	RDY*
9	C2:6	ERR*
8	C3:6	OPT2
7	C3:5	OPT1
6	C3:4	OPT0
5	C2:5	STAT2
4	C2:4	STAT1

Table 3–6: Control group channel assignments (cont.)

Bit order	Section:channel	29030/35/40 signal name
3	C3:7	STAT0
2	C2:7	LOCK*
1	C3:1	RDN*
0	C2:0	BGRT*

Table 3–7 shows the probe section and channel assignments for the Intr group and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–7: Intr group channel assignments

Bit order	Section:channel	29030/35/40 signal name
6	C1:6	TRAP1*†
5	C1:5	TRAP0*†
4	C1:4	INTR3*†
3	C1:3	INTR2*†
2	C1:2	INTR1*†
1	C1:1	INTR0*†
0	C1:0	WARN*†

† **Signal not required for disassembly.**

Table 3–8 shows the probe section and channel assignments for the Bwrtenbl group and the microprocessor signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–8: Bwrtenbl group channel assignments

Bit order	Section:channel	29030/35/40 signal name
3	C0:5	BWE3*†
2	C0:4	BWE2*†
1	C0:3	BWE1*†
0	C0:2	BWE0*†

† **Signal not required for disassembly.**

Table 3–9 shows the probe section and channel assignments for the Misc group and the microprocessor signal to which each channel connects. By default, this channel group is not visible.

Table 3–9: Misc group channel assignments

Bit order	Section:channel	29030/35/40 signal name
4	C1:7	RESET*†
3	C0:7	IDP3†
2	C0:6	IDP2†
1	C0:1	IDP1†
0	C0:0	IDP0†

† **Signal not required for disassembly.**

Table 3–10 shows the probe section and channel assignments for the clock probes (not part of any group) and the 29030/35/40 signal to which each channel connects.

Table 3–10: Clock channel assignments

Section:channel	29030/35/40 signal name
CK:1	RDN*=
CK:0	MEMCLK

How Data is Acquired

This part of this chapter explains how the module acquires 29030/35/40 signals using the TMS 480 software and probe adapter. This part also provides additional information on microprocessor signals accessible on or not accessible on the probe adapter, and on extra probe channels available for you to use for additional connections.

Custom Clocking

A special clocking program is loaded to the module every time you load the 2903X support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple groups of channels at different times as they become valid on the 29030/35/40 bus. The module then sends all the logged-in signals to the trigger machine and to the memory of the module for storage.

In Custom clocking, the module clocking state machine (CSM) generates one master sample for each microprocessor bus cycle, no matter how many clock cycles are contained in the bus cycle.

The MEMCLK signal is used to clock in address, data, and control signals (shown as ADC in the figures). The RDN*, BURST*, RDY*, REQ*, and BGRT* signals are used as qualifiers for sampling valid data on the rising edge of MEMCLK.

Data is valid when the RDY* signal is asserted. The RDY* signal is ignored by the microprocessor in the first cycle of Simple Accesses and the first cycle of initial Burst Accesses.

Simple Access. A Simple Access occurs when the REQ* and BGRT* signals are low on the rising edge of the MEMCLK signal and the BURST* signal is high. A sample is taken and a master sample is logged. On the next rising edge of MEMCLK, if REQ* and BGRT* are low and BURST* is high, another sample is taken and a master sample is logged.

Figure 3–2 shows the master sample points for a Simple Access.

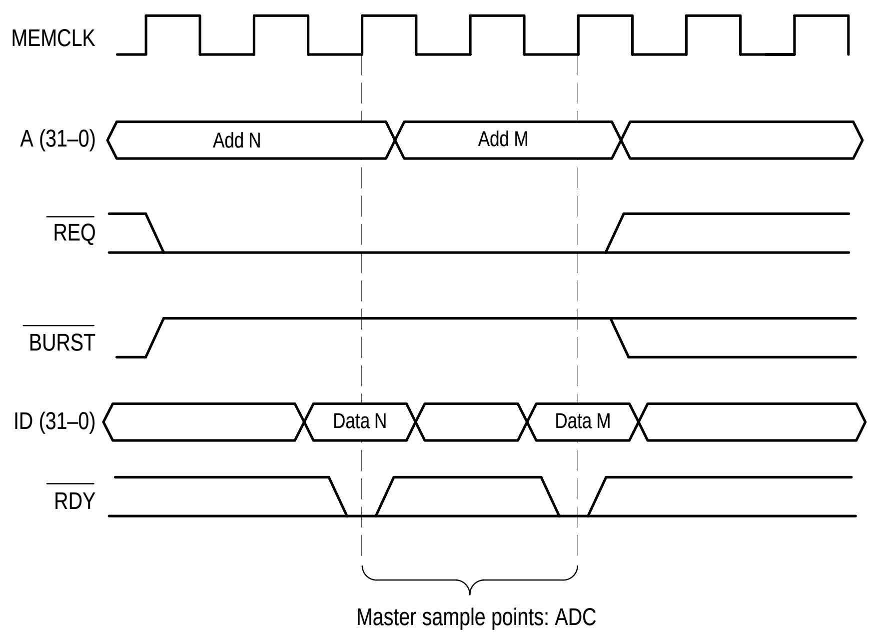


Figure 3–2: 29030/35/40 bus timing: Simple Access

Burst Access. A Burst Access occurs when the REQ* and BGRT* signals are low on the rising edge of the MEMCLK signal and the BURST* signal is low. A sample is taken and a master sample is logged. On every subsequent rising edge of MEMCLK, as long as the REQ*, BGRT*, and BURST* signals remain low, another sample is taken and a master sample is logged.

When the BURST signal goes high, it indicates that the access is the last of that group of Burst Accesses. On the rising edge of MEMCLK when the BURST* signal is high, and REQ* and BGRT* are low, the last sample is taken and a master sample is logged.

Figure 3–3 shows the master sample points for a Burst Access.

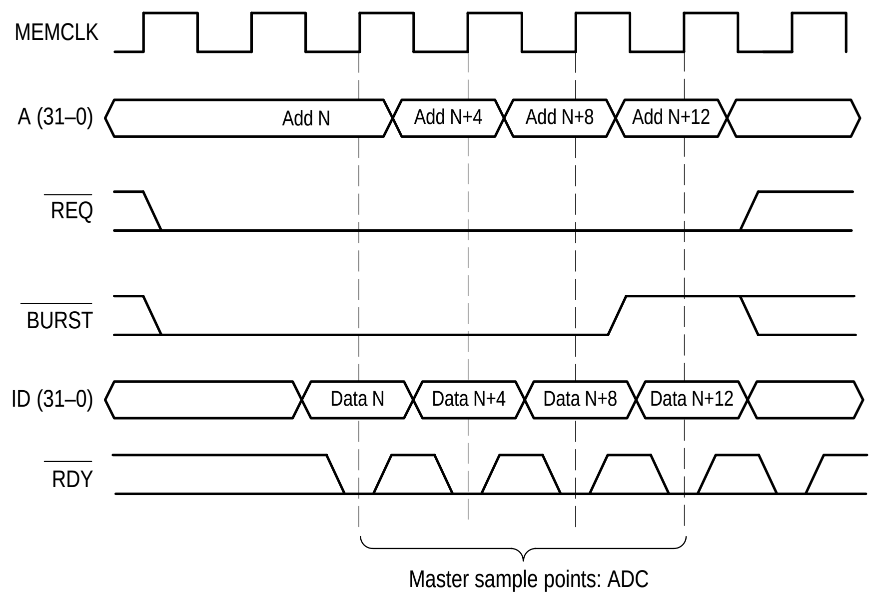


Figure 3–3: 29030/35/40 bus timing: Burst Access

Clocking Options

The clocking algorithm for the 29030/35/40 microprocessor support has four variations: Alternate Bus Master Cycles Excluded, Alternate Bus Master Cycles Included, Narrow Access Width 8 Bit, and Narrow Access Width 16 Bit.

Alternate Bus Master Cycles Excluded. Alternate Bus Master cycles are not acquired or displayed.

Alternate Bus Master Cycles Included. All bus cycles, including Alternate Bus Master cycles, are logged.

Narrow Access Width: 8 Bit. When the read/write access is narrow, the access width is 8 bits.

Narrow Access Width: 16 Bit. When the read/write access is narrow, the access width is 16 bits.

Alternate Microprocessor Connections

You can connect to other signals that are not required by the support so that you can analyze other signal activity in your system. These signals might or might not be accessible on the probe adapter board. The following paragraphs and tables list signals that are or are not accessible on the probe adapter board.

For a list of signals required or not required for disassembly, refer to the channel assignment tables beginning on page 3–4. Remember that these channels are already included in a channel group. If you do connect these channels to other signals, you should set up another channel group for them.

Signals Not On the Probe Adapter

The probe adapter does not provide access for the following microprocessor signals:

- DI*
- DIV2*
- HIT*
- MSERR
- PGMODE*
- PWRCLK
- SUP/US*
- TCK
- TDI
- TDO
- TEST*
- TMS
- TRST*
- WBC*
- MSERR
- MPGM1
- MPGM0

- LOCK*
- CNTL1
- CNTL0
- BREQ*
- ERYLA*
- INCLK

Extra Channels

Table 3–11 lists extra sections and channels that are left after you have connected all the probes used by the support. You can use these extra channels to make alternate SUT connections.

Channels not defined in a channel group by the TMS 480 software are logged in with the Master sample point.

Table 3–11: Extra module sections and channels

Module	Section: channels
102-channels	Qual:1, Qual:0
136-channels	E3:7-0, E2:7-0, E1:7-0, E0:7-0, Qual:3-0
96-channels	None

These channels are not defined in any channel group and data acquired from them is not displayed. To display data, you will need to define a channel group.

Maintenance

This chapter contains a circuit description for the probe adapter.

Probe Adapter Circuit Description

The probe adapter does not contain any active circuitry.

Replacing Signal Leads

Information on basic operations describes how to replace signal leads (individual channel and clock probes).

Replacing Protective Sockets

Information on basic operations describes how to replace protective sockets.

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 480 29030/35/40 microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

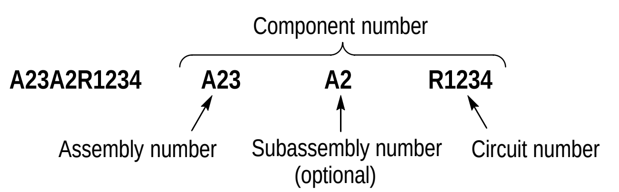
Parts list column descriptions

Column	Column name	Description
1	Component number	The component number appears on diagrams and circuit board illustrations, located in the diagrams section. Assembly numbers are clearly marked on each diagram and circuit board illustration in the *Diagrams* section, and on the mechanical exploded views in the *Replaceable Mechanical Parts* list section. The component number is obtained by adding the assembly number prefix to the circuit number (see Component Number illustration following this table). The electrical parts list is arranged by assemblies in numerical sequence (A1, with its subassemblies and parts, precedes A2, with its subassemblies and parts). Chassis-mounted parts have no assembly number prefix, and they are located at the end of the electrical parts list.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
6	Mfr. code	This indicates the code number of the actual manufacturer of the part.
7	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Component Number



Read: Resistor 1234 (of Subassembly 2) of Assembly 23

List of Assemblies

A list of assemblies is located at the beginning of the electrical parts list. The assemblies are listed in numerical order. When a part's complete component number is known, this list will identify the assembly in which the part is located.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
63058	MCKENZIE TECHNOLOGY	910 PAGE AVE	FREMONT, CA 945387340
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077–0001
TK0860	LABEL GRAPHICS INC	ATTN: DALE GREMAUX 6700 SW BRADBURY CT	PORTLAND, OR 97224

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A01	010–0595–00			PROBE ADAPTER:29030/35/40,PGA–145,PROBE ADAPTER	80009	010–0595–00
A01	119–4889–00			PROBE ADAPTER:29030/40,PGA–145, OEM	80009	119–4889–00
A01	136–0952–00			SOCKET,PGA:PCB,145 POS,15 X 15,0.1 CTR,0.173 H X 0.183 TAIL,GOLD/GOLD,OPEN CTR,PATTERN 152	63058	PGA145H101B1152 1F

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 480 29030/35/40 microprocessor support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
63058	MCKENZIE TECHNOLOGY	910 PAGE AVE	FREMONT, CA 945387340
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077–0001
TK0860	LABEL GRAPHICS INC	ATTN: DALE GREMAUX 6700 SW BRADBURY CT	PORTLAND, OR 97224

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
1–0	010–0595–00			1	PROBE ADAPTER:29030/35/40,PGA–145	80009	010–0595–00
–1	119–4889–00			1	PROBE ADAPTER:29030/40,PGA–145, OEM	80009	119–4889–00
–2	136–0952–00			1	SOCKET,PGA:PCB,145 POS,15 X 15,0.1 CTR,0.173 H X 0.183 TAIL,GOLD/GOLD,OPEN CTR,PATTERN 152	63058	PGA145H101B1152 1F
					STANDARD ACCESSORIES		
	070–9827–00			1	MANUAL,TECH:INSTRUCTION,29030/35/40,DISSASEMBLER, TMS 480	80009	070–9827–00
	070–9803–00			1	MANUAL, TECH:TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070–9803–00
					OPTIONAL ACCESSORIES		
	070–9802–00			1	MANUAL, TECH:BASIC OPS MICRO SUP ON DAS/TLA 500 SERIES LOGIC ANALYZERS	80009	070–9802–00

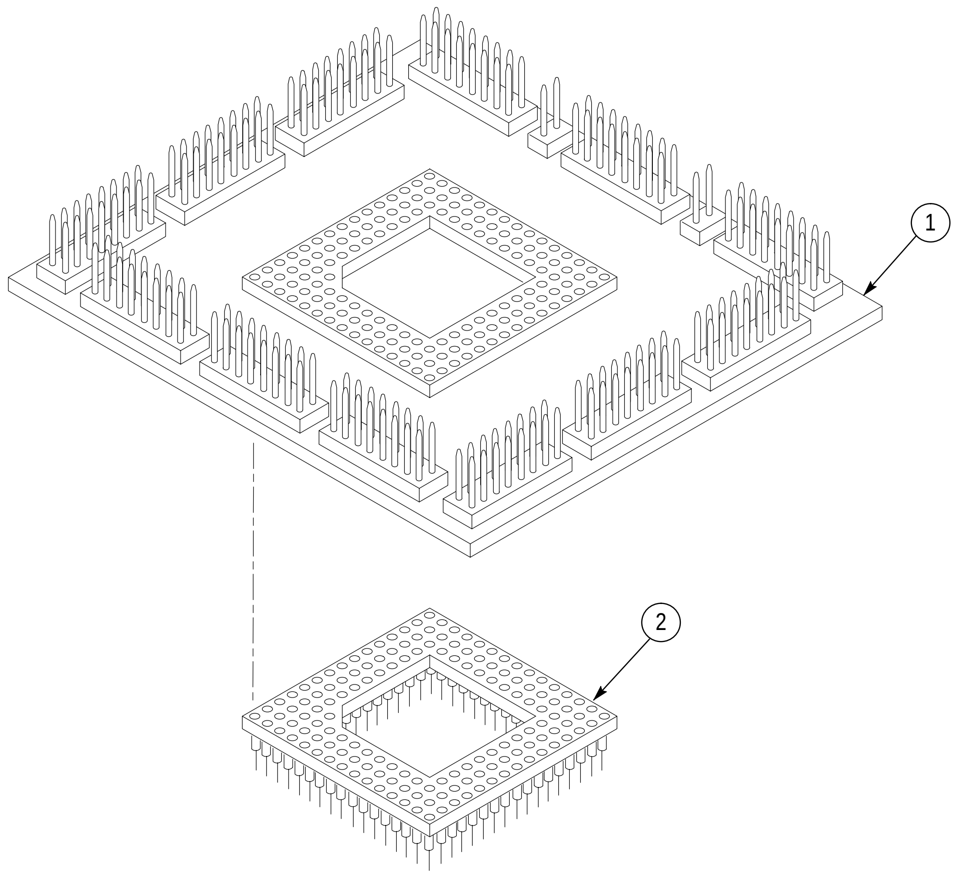


Figure 1: 29030/35/40 probe adapter exploded view

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