Instruction Manual

Tektronix

TMS 561
MPC850/823/801 Microprocessor Support

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Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Ground the Product. This product is indirectly grounded through the grounding conductor of the mainframe power cord. To avoid electric shock, the grounding conductor must be connected to earth ground. Before making connections to the input or output terminals of the product, ensure that the product is properly grounded.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

The common terminal is at ground potential. Do not connect the common terminal to elevated voltages.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Preface

This instruction manual contains specific information about the TMS 561 MPC850 microprocessor support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor support packages on the logic analyzer for which the TMS 561 MPC850 support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of microprocessor support packages is included with each product. Each logic analyzer includes basic information that describes how to perform tasks common to support packages on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing disassembled data

Manual Conventions

This manual uses the following conventions:

- The term “disassembler” refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to online help, an installation manual, or a user manual covering the basic operations of microprocessor support..
- In the information on basic operations, the term “XXX” or “P54C” appearing in field selections and file names must be replaced with MPC8XX. This term is the name of the microprocessor in field selections and file names you must use to operate the MPC850 support.
- The term “logic analyzer” refers to the Tektronix logic analyzer for which this product was purchased.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the user manual of the corresponding module. The manual set provides the information necessary to install, operate, maintain, and service the logic analyzer and its associated products.

Contacting Tektronix

Product Support	For questions about using Tektronix measurement products, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Tektronix offers extended warranty and calibration programs as options on many products. Contact your local Tektronix distributor or sales office. For a listing of worldwide service centers, visit our web site.
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000 USA
Website	Tektronix.com

Getting Started

Getting Started

This chapter contains information on the TMS 561 MPC850 microprocessor support and information on connecting your logic analyzer to your system under test.

Support Package Description

The TMS 561 microprocessor support package displays disassembled data from systems based on the Motorola MPC8XX microprocessor.

To use this support efficiently, refer to information on basic operations and the following documents:

- *MPC850 User's Manual, Motorola, 1997*
- *MPC823 User's Manual, Motorola, 1997*
- *MPC801 User's Manual, Motorola, 1997*

The microprocessors the TMS 561 support can acquire and display as disassembled data are:

MPC801
MPC823
MPC850

Logic Analyzer Software Compatibility

The label on the microprocessor support floppy disk states which version of logic analyzer software the support is compatible with.

Logic Analyzer Configuration

For use with a TLA 700 Series, the TMS 561 support requires a minimum of one 102-channel module.

Requirements and Restrictions

Review the electrical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other MPC850 support requirements and restrictions.

Hardware Reset. If a hardware reset occurs in your MPC850 system during an acquisition, the application disassembler might acquire an invalid sample.

System Clock Rate. The MPC850 microprocessor support can acquire data from the MPC850/823 microprocessor operating at speeds of up to 50 MHz and the MPC801 microprocessor at 40 MHz. The tested clock rate for the MPC850/823 microprocessor is 33 MHz and for the MPC801 microprocessor is 40 MHz. The operating clock rate specifications were measured at the time of printing. Contact your Tektronix sales representative for current information on the fastest devices supported.

CPM Related Information. The CPM related information protocols that appear on the serial bus are not acquired by the TMS 561 support software.

Disabling the Instruction Cache. To display disassembled acquired data, you must disable the internal instruction cache. Disabling the cache makes all instruction prefetches visible on the bus so that they can be acquired and displayed disassembled.

Disabling the Data Cache. To display acquired data, you must disable the data cache. Disabling the data cache makes visible all loads and stores to memory on the bus, including data reads and writes, so the software can acquire and display them.

Nonintrusive Acquisition. The MPC850 microprocessor support will not intercept, modify, or present signals back to the system under test.

Programming the UPMs. The MPC8XX microprocessor has an on-chip memory controller that supports the DRAM interface. The on-chip memory controller has three machines:

General Purpose Chip Select Machine (GPCM)

Two User Programmable Machines (UPMs), UPMA and UPMB

To acquire correct column addresses when the DRAM is used for burst access, program the UPM to acquire waveforms on assertion of TA* at the rising clock edge; the corresponding column address appears on the bus.

The programming in the UPM is flexible. The following programmed UPM words for the UPM controlled burst accesses to 32-bit DRAM with a speed of 60 ns. The words must be placed at the UPM start address 0x08 for burst read and at the UPM start address 0x20 for burst write. There are many examples of different patterns of words that will achieve the same result.

8fffec24
0fffec04
08ffec00
00ffec0c
03ffec04
00ffec40
00ffcc0c
0cffcc44
00ffec00
03ffec0c
00ffec44
00ffcc00
3fffc847

DRAM and Non-DRAM. When the acquisition has both DRAM and non-DRAM accesses, the clocking option Memory Device selected is DRAM. In this case, the non-DRAM transactions repeat the same address since there is an acquisition of the same address at TS* assertion at the rising edge of the clock.

If the acquisition has both DRAM and non-DRAM transactions and if the clocking option selected for the Memory Device is non-DRAM, then the row address will not be acquired for the DRAMs and the address is displayed incorrectly.

Support Software. The MPC850 Support Software is not tested for SDRAM and EDO memory types.

Tsiz0 and AT2 Pins. Pins Tsiz0 and AT2 must be programmed for the same functionality to correctly disassemble data.

Address Translation. The address translation must be turned off for proper disassembly.

Functionality Not Supported

Interrupt Signals. The interrupt signals are not acquired by the TMS 561 support software; however, the interrupts are identified when looking at the address displayed for the interrupt service.

Extra Acquisition Channels. Extra Acquisition Channels are not available.

Alternate Bus Master. Alternate bus master transactions are not processed in the disassembly.

CPM Cycles. The TMS 561 support software cannot distinguish between the Core or CPM cycles.

Show Cycle The show cycle signals are not acquired by the TMS 561 support software.

External Master Cycles. Asynchronous External Master cycles are not acquired.

Connecting the Logic Analyzer to a System Under Test

You can use either channel probes, clock probes, leadsets or a commercial adapter to make connections between the logic analyzer and your system under test.

NOTE*. Contact your Tektronix sales representative for information on the availability of a commercial probe adapter.*

To connect the probes to MPC8XX signals in the system under test follow these steps:

1. Turn off power to your system under test. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the microprocessor, the probes, and the logic analyzer module. To prevent static damage, handle these components only in a static-free environment.*

Always wear a grounding wrist strap, heel strap, or similar device while handling the microprocessor.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer.
3. Place the system under test on a horizontal static-free surface.
4. Use Table 1–1 through Table 1–6 to connect the channel probes to MPC8XX signal pins in the system under test.

   Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your system under test.

Channel Assignments

Channel assignments listed in Table 1–1 through Table 1–6 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are listed starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- An asterisk symbol (*) following the signal name indicates an active low signal.
- An equals symbol (=) following a signal name indicates that it is double probed.
- The module in the higher-numbered slot is referred to as the HI module and the module in the lower-numbered slot is referred to as the LO module.

  The TLA 704 logic analyzer has the lower-numbered slots on the top and the TLA 711 logic analyzer has the lower-numbered slots on the left.

Table 1–1 lists the probe section and channel assignments for the Address group and the microprocessor signal for each channel connect. By default, this channel group is displayed in hexadecimal.

Table 1–1: Address channel group assignments

Bit order	Section:channel	MPC8XX signal name
31	A3:7	BS_AB0*[1]
30	A3:6	BS_AB1*[1]
29	A3:5	BS_AB2*[1]
28	A3:4	BS_AB3*[1]
27	A3:3	OE*[1]

Table 1–1: Address channel group assignments (Cont.)

Bit order	Section:channel	MPC8XX signal name
26	A3:2	AS*[1]
25	A3:1	A6
24	A3:0	A7
23	A2:7	A8
22	A2:6	A9
21	A2:5	A10
20	A2:4	A11
19	A2:3	A12
18	A2:2	A13
17	A2:1	A14
16	A2:0	A15
15	A1:7	A16
14	A1:6	A17
13	A1:5	A18
12	A1:4	A19
11	A1:3	A20
10	A1:2	A21
9	A1:1	A22
8	A1:0	A23
7	A0:7	A24
6	A0:6	A25
5	A0:5	A26
4	A0:4	A27
3	A0:3	A28
2	A0:2	A29
1	A0:1	A30
0	A0:0	A31

1 **The MPC8XX microprocessor has a 32-bit Address bus internally, only 26-bits of the Address Signals are visible outside the MPC8XX microprocessor. The 32-bits of Address are displayed in the disassembly by taking the Base Address as your input for each bank. Channels A3:7 – A3:2 are included in the Address group although other signals of interest could be assigned to these channels.**

Table 1–2 lists the probe section and channel assignments for the Data group and the microprocessor signal for each channel connect. By default, this channel group is displayed in hexadecimal.

Table 1–2: Data channel group assignments

Bit order	Section:channel	MPC8XX signal name
31	D3:7	D0
30	D3:6	D1
29	D3:5	D2
28	D3:4	D3
27	D3:3	D4
26	D3:2	D5
25	D3:1	D6
24	D3:0	D7
23	D2:7	D8
22	D2:6	D9
21	D2:5	D10
20	D2:4	D11
19	D2:3	D12
18	D2:2	D13
17	D2:1	D14
16	D2:0	D15
15	D1:7	D16
14	D1:6	D17
13	D1:5	D18
12	D1:4	D19
11	D1:3	D20
10	D1:2	D21
9	D1:1	D22
8	D1:0	D23
7	D0:7	D24
6	D0:6	D25
5	D0:5	D26
4	D0:4	D27
3	D0:3	D28
2	D0:2	D29
1	D0:1	D30
0	D0:0	D31

Table 1–3 lists the probe section and channel assignments of the Control group and the microprocessor signal for each channel connect. The default radix of the Control group is SYMBOLIC. The symbol table file name is MPC850_Ctrl. By default, this channel group is displayed as symbols.

Table 1–3: Control channel group assignments

Bit order	Section:channel	MPC8XX signal name
11	C2:0	TS*
10	C0:1	AT1
9	C0:5	AT2
8	C1:1	AT3
7	C3:4	RD/WR*
6	C3:5	BDIP*
5	C2:1	TA*
4	C2:2	TEA*
3	C2:3	RETRY*
2	C2:5	BI*
1	C0:4	BR*
0	C1:0	BG*

Table 1–4 lists the probe section and channel assignments for the Tsize group and the microprocessor signal for each channel connect. The symbol table file name is MPC850_Tsiz. By default, this channel group is displayed as symbols.

Table 1–4: Tsize channel group assignments

Bit order	Section:channel	MPC8XX signal name
2	C2:4	TSIZ0
1	C3:0	TSIZ1
0	C3:1	BURST*

Table 1–5 lists the probe section and channel assignments for the Chipsel group and the microprocessor signal for each channel connect. The symbol table file name is MPC850_Csel. By default, this channel group is displayed as symbols.

Table 1–5: Chipsel channel group assignments

Bit order	Section:channel	MPC8XX signal name
7	C0:2	CS0*
6	C0:6	CS1*
5	C1:2	CS2*
4	C1:6	CS3*
3	C0:3	CS4*
2	C0:7	CS5*
1	C1:3	CS6*
0	C1:7	CS7*

Table 1–6 lists the probe section and channel assignments for the Misc group and the microprocessor signal for each channel connect. By default, this channel group is not visible.

Table 1–6: Misc channel group assignments

Bit order	Section:channel	MPC8XX signal name
8	C2:7	CLKOUT
7	C0:0	STS*
6	C1:4	BB*
5	C1:5	RSV*
4	C2:6	VF0
3	C3:2	VF1
2	C3:6	VF2
1	C3:3	VFLS0
0	C3:7	VFLS1

Table 1–7 lists the probe section and channel assignments for the clock probes (not part of any group), and the MPC8XX signal to which each channel connects.

Table 1–7: Clock and qualifier channel assignments

LA section and probe	MPC8XX signal name	Description
CLK:0	BR*=	Clock used as qualifier
CLK:1	BB*=	Clock used as qualifier
CLK:2	CLKOUT=	Clock used as clock
CLK:3	BG*=	Clock used as qualifier
C2:0	TS*	Used as qualifier
C2:1	TA*	Used as qualifier
C2:2	TEA*	Used as qualifier
C2:3	RETRY*	Used as qualifier

Table 1–8 lists channel groups not required for clocking and disassembly by the MPC850 microprocessor support.

Table 1–8: Channel groups not required for clocking and disassembly

MPC8XX Signal Name	TLA 700 Channel
CLKOUT[1]	C2:7
STS*[1]	C0:0
BB*[1]	C1:4
RSV*[1]	C1:5
VF0[1]	C2:6
VF1[1]	C3:2
VF2[1]	C3:6
VFLS0[1]	C3:3
VFLS1[1]	C3:7

1 **Misc Group**

Acquisition Setup. The MPC850 support will affect the logic analyzer setup menus and submenus by modifying existing fields and adding micro-specific fields.

The MPC850 support will add the selection MPC850 to the Load Support Package dialog box, located under the File pulldown menu. Once that MPC850

support has been loaded, the Custom clocking mode selection in the module Setup menu is also enabled.

CPU To Mictor Connections

To probe the microprocessor, you will need to make connections between the CPU and the Mictor pins of the P6434 Mass Termination Probe. Refer to the P6434 Mass Termination Probe manual, Tektronix part number 070-9793-xx, for more information on mechanical specifications. Table 1–9 through Table 1–11 lists the CPU pin to Mictor pin connections.

CAUTION. *To protect the CPU and the inputs of the module, it is recommended that a 180 Ω resistor be connected in series between each ball pad of the CPU and each pin of the Mictor connector. The resistor must be within 1/2-inch of the ball pad of the CPU.*

Table 1–9: CPU to Mictor connections for Mictor A pins

Tektronix Mictor A pin number	AMP Mictor A pin number	LA Channel	MPC8XX signal name	BGA Ball MPC850/823	BGA Ball MPC801
1	1	NC	NC	NC	NC
2	3	NC	NC	NC	NC
3	5	Clock:0	BR*=	B11	E3
4	7	A3:7	NC	NC	NC
5	9	A3:6	NC	NC	NC
6	11	A3:5	NC	NC	NC
7	13	A3:4	NC	NC	NC
8	15	A3:3	NC	NC	NC
9	17	A3:2	NC	NC	NC
10	19	A3:1	A6	M13	G14
11	21	A3:0	A7	N15	E16
12	23	A2:7	A8	N16	F15
13	25	A2:6	A9	M15	D16
14	27	A2:5	A10	L13	E15
15	29	A2:4	A11	M16	F14
16	31	A2:3	A12	M14	C16
17	33	A2:2	A13	L14	D15
18	35	A2:1	A14	L15	E14
19	37	A2:0	A15	L16	B15
20	38	A0:0	A31	F16	A11

Table 1–9: CPU to Mictor connections for Mictor A pins (Cont.)

Tektronix Mictor A pin number	AMP Mictor A pin number	LA Channel	MPC8XX signal name	BGA Ball MPC850/823	BGA Ball MPC801
21	36	A0:1	A30	G15	A13
22	34	A0:2	A29	H16	B16
23	32	A0:3	A28	G16	A12
24	30	A0:4	A27	K16	A16
25	28	A0:5	A26	F14	B11
26	26	A0:6	A25	H14	C12
27	24	A0:7	A24	H13	A14
28	22	A1:0	A23	H15	B13
29	20	A1:1	A22	G14	C11
30	18	A1:2	A21	J14	C13
31	16	A1:3	A20	J15	B14
32	14	A1:4	A19	K15	A15
33	12	A1:5	A18	G13	B12
34	10	A1:6	A17	K13	C14
35	8	A1:7	A16	K14	C15
36	6	Clock:1	BB*=	A11	C2
37	4	NC	NC	NC	NC
38	2	NC	NC	NC	NC
39	39	GND	GND	GND	GND
40	40	GND	GND	GND	GND
41	41	GND	GND	GND	GND
42	42	GND	GND	GND	GND
43	43	GND	GND	GND	GND

Table 1–10: CPU to Mictor connections for Mictor D pins

Tektronix Mictor D pin number	AMP Mictor D pin number	LA Channel	MPC8XX signal name	BGA Ball MPC850/823	BGA Ball MPC801
1	1	NC	NC	NC	NC
2	3	NC	NC	NC	NC
3	5	NC	NC	NC	NC
4	7	D3:7	D0	M1	R16
5	9	D3:6	D1	L1	T14

Table 1–10: CPU to Mictor connections for Mictor D pins (Cont.)

Tektronix Mictor D pin number	AMP Mictor D pin number	LA Channel	MPC8XX signal name	BGA Ball MPC850/823	BGA Ball MPC801
6	11	D3:5	D2	J2	T12
7	13	D3:4	D3	J1	T11
8	15	D3:3	D4	L2	T16
9	17	D3:2	D5	H1	T10
10	19	D3:1	D6	F1	T8
11	21	D3:0	D7	E1	T6
12	23	D2:7	D8	M2	P14
13	25	D2:6	D9	K2	R13
14	27	D2:5	D10	K3	P11
15	29	D2:4	D11	K1	T13
16	31	D2:3	D12	M4	P13
17	33	D2:2	D13	M3	R15
18	35	D2:1	D14	J3	N10
19	37	D2:0	D15	J4	P10
20	38	D0:0	D31	E3	N6
21	36	D0:1	D30	D2	P5
22	34	D0:2	D29	E2	R6
23	32	D0:3	D28	F4	P6
24	30	D0:4	D27	L3	T15
25	28	D0:5	D26	E4	N7
26	26	D0:6	D25	G4	P7
27	24	D0:7	D24	F3	R7
28	22	D1:0	D23	L4	P12
29	20	D1:1	D22	H4	R8
30	18	D1:2	D21	F2	P8
31	16	D1:3	D20	G3	R9
32	14	D1:4	D19	G2	P9
33	12	D1:5	D18	H3	R10
34	10	D1:6	D17	K4	R14
35	8	D1:7	D16	H2	N9
36	6	Clock:2	CLKOUT=	D1	T5

Table 1–10: CPU to Mictor connections for Mictor D pins (Cont.)

Tektronix Mictor D pin number	AMP Mictor D pin number	LA Channel	MPC8XX signal name	BGA Ball MPC850/823	BGA Ball MPC801
37	4	NC	NC	NC	NC
38	2	NC	NC	NC	NC
39	39	GND	GND	GND	GND
40	40	GND	GND	GND	GND
41	41	GND	GND	GND	GND
42	42	GND	GND	GND	GND
43	43	GND	GND	GND	GND

Table 1–11: CPU to Mictor connections for Mictor C pins

Tektronix Mictor C pin number	AMP Mictor C pin number	LA Channel	MPC8XX signal name	BGA Ball MPC850/823	BGA Ball MPC801
1	1	NC	NC	NC	NC
2	3	NC	NC	NC	NC
3	5	Clock:3	BG*=	C10	D2
4	7	C3:7	VLFS1	C8	G2
5	9	C3:6	VF2	A9	F1
6	11	C3:5	BDIP*	A13	C3
7	13	C3:4	RD/WR*	C13	C4
8	15	C3:3	VFLS0	A8	G1
9	17	C3:2	VF1	C9	G3
10	19	C3:1	BURST*	B10	E1
11	21	C3:0	TSIZ1	E15	B10
12	23	C2:7	CLKOUT	D1	T5
13	25	C2:6	VF0	B9	F2
14	27	C2:5	BI*	B12	D3
15	29	C2:4	TSIZ0	F15	C10
16	31	C2:3	RETRY*	B7	J2
17	33	C2:2	TEA*	C11	A1
18	35	C2:1	TA*	A12	B2
19	37	C2:0	TS*	D10	B1
20	38	C0:0	STS*	D6	K3
21	36	C0:1	AT1	B8	H4

Table 1–11: CPU to Mictor connections for Mictor C pins (Cont.)

Tektronix Mictor C pin number	AMP Mictor C pin number	LA Channel	MPC8XX signal name	BGA Ball MPC850/823	BGA Ball MPC801
22	34	C0:2	CS0*	D12	B4
23	32	C0:3	CS4*	B16	A6
24	30	C0:4	BR*	B11	E3
25	28	C0:5	AT2	D7	H2
26	26	C0:6	CS1*	A14	A4
27	24	C0:7	CS5*	D13	B6
28	22	C1:0	BG*	C10	D2
29	20	C1:1	AT3	D8	H3
30	18	C1:2	CS2*	B14	C5
31	16	C1:3	CS6*	C14	C6
32	14	C1:4	BB*	A11	C2
33	12	C1:5	RSV*	D9	G4
34	10	C1:6	CS3*	A15	B5
35	8	C1:7	CS7*	B15	A5
36	6	NC	NC	NC	NC
37	4	NC	NC	NC	NC
38	2	NC	NC	NC	NC
39	39	GND	GND	GND	GND
40	40	GND	GND	GND	GND
41	41	GND	GND	GND	GND
42	42	GND	GND	GND	GND
43	43	GND	GND	GND	GND

Operating Basics

Setting Up the Support

This section provides information on how to set up the support. The information covers the following topics:

- Clocking options
- Symbol table files

The information in this section is specific to the operations and functions of the TMS 561 MPC850 support on any Tektronix logic analyzer for which it can be purchased.

Before you acquire and display disassemble data, you need to load the support and specify the setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the MPC850 support are Address, Data, Control, Tsize, Chipsel and Misc. If you want to know which signal is in which group, refer to the channel assignment tables beginning on page 1–5.

Clocking

Custom Clocking

A special clocking program is loaded to the module every time you load the MPC850 support. This special clocking is called Custom.

When Custom is selected, the Custom Clocking Options menu has the subtitle MPC850 Microprocessor Clocking Support added, and clocking options are displayed.

When using Custom clocking, the module logs signals from mutiple channels groups at different times as they become valid on the MPC8XX bus. The module then sends all the logged-in signals to the trigger machine and memory for storage.

For DRAM accesses, the row address is captured on the assertion of TS* at the rising edge of the clock. The column address, data and other signals are captured on the assertion of TA* at the rising edge of the clock.

For the non-DRAM accesses, the address, data and other signals are captured on the assertion of TA* at the rising edge of the clock.

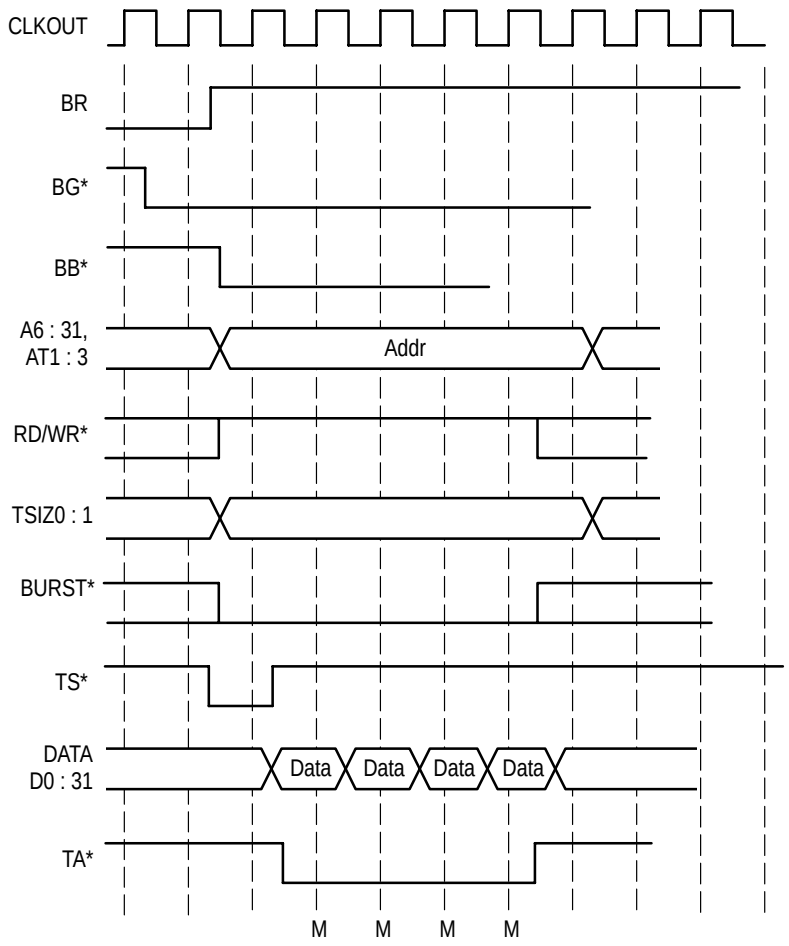

Figure 2–1: MPC8XX Bus Timing Diagram

Clocking Options

The TMS 561 support offers a microprocessor-specific clocking mode for the MPC8XX microprocessor. This clocking mode is the default selection whenever you load the MPC850 support.

Disassembly will not be correct with the Internal or External clocking modes. Information on basic operations describes how to use these clock selections for general-purpose analysis.

Bus Arbitration. Select Internal for the internal on-chip arbiter and the External for external, central-bus arbiter.

Internal (default)
External

Memory Device. Select DRAM for DRAM memories to acquire both row and column addresses appearing on the bus. Select non-DRAM for devices like SRAM, Flash ROM, and others where the absolute address appears on the bus.

DRAM (default)
Non-DRAM

RETRY. Select Retry Activated if the pin is programmed for the functionality of RETRY*.

Activated (default)
Inactivated

Alternate Master Cycles. Select Excluded where the alternate master cycles are not acquired. Select Included where the alternate master cycles are acquired and not disassembled.

Excluded (default)
Included

Symbols

The TMS 561 support provides three symbol-table files. The MPC850_Ctrl file replaces specific Control-channel group values with symbolic values when Symbolic is the radix for the channel group.

Table 2–1 lists the name, bit pattern, and description for the symbols in the file MPC850_Ctrl in the Control channel group symbol table.

Table 2–1: Control group symbol table definitions

Symbol	Control group value TS* AT1 AT2 AT3	RD/WR* BDIP* TA* TEA*	RETRY* BI* BR* BG*	Description
SUP PTR INST FETCH	X 0 0 0	1 X 0 1	X X X X	Normal Instruction, Program Trace,Privilege State
SUP INST FETCH	X 0 0 1	1 X 0 1	X X X X	Normal Instruction, Privilege State
SUP RSV DATA READ	X 0 1 0	1 X 0 1	X X X X	Reservation Data Read, Privilege State

Table 2–1: Control group symbol table definitions (Cont.)

Symbol	Control group value TS* AT1 AT2 AT3	RD/WR* BDIP* TA* TEA*	RETRY* BI* BR* BG*	Description
SUP RSV DATA WRITE	X 0 1 0	0 X 0 1	X X X X	Reservation Data Write, Privilege State
SUP DATA READ	X 0 1 1	1 X 0 1	X X X X	Normal Data Read, Privilege State
SUP DATA WRITE	X 0 1 1	0 X 0 1	X X X X	Normal Data Write, Privilege State
USR PTR INST FETCH	X 1 0 0	1 X 0 1	X X X X	Normal Instruction, Program Trace, Problem State
USR INST FETCH	X 1 0 1	1 X 0 1	X X X X	Normal Instruction, Problem State
USR RSV DATA READ	X 1 1 0	1 X 0 1	X X X X	Reservation Data Read, Problem State
USR RSV DATA WRITE	X 1 1 0	0 X 0 1	X X X X	Reservation Data write, Problem State
USR DATA READ	X 1 1 1	1 X 0 1	X X X X	Normal Data Read, Problem State
USR DATA WRITE	X 1 1 1	0 X 0 1	X X X X	Normal Data Write, Problem State
TRANSFER ERROR	X X X X	X X X 0	X X X X	Transfer Error Cycle
RETRY	X X X X	X X 1 1	0 X X X	Retry Cycle
ROW ADDRESS	0 X X X	X X 1 X	X X X X	Row Address Information for DRAM memory devices

Table 2–2 lists the name, bit pattern, and description for the symbols in the file MPC850_Tsiz in the Tsize channel group symbol table.

Table 2–2: Tsize group symbol table definitions

Symbol	Tsize group value TSIZ0 TSIZ1 BURST*	Description
BYTE	0 1 1	Single beat one-byte transaction
HALF WORD	1 0 1	Single beat half-word (two-byte) transaction
WORD	0 0 1	Single beat word (four-byte) transaction
BURST	0 0 0	Burst (four beats – sixteen bytes) transaction

Table 2–3 lists the name, bit pattern, and description for the symbols in the file MPC850_Csel in the Chipsel channel group symbol table.

Table 2–3: Chipsel Control group symbol table definitions

Symbol	Chipsel group value CS0* CS1* CS2* CS3* CS4* CS5* CS6* CS7*	Description
CHIP SELECT 0	0 1 1 1 1 1 X X	Enables memory at a programmed Addr as defined in BR0 and OR0 registers
CHIP SELECT 1	1 0 1 1 1 1 X X	Enables memory at a programmed Addr as defined in BR1 and OR1 registers
CHIP SELECT 2	1 1 0 1 1 1 X X	Enables memory at a programmed Addr as defined in BR2 and OR2 registers
CHIP SELECT 3	1 1 1 0 1 1 X X	Enables memory at a programmed Addr as defined in BR3 and OR3 registers
CHIP SELECT 4	1 1 1 1 0 1 X X	Enables memory at a programmed Addr as defined in BR4 and OR4 registers
CHIP SELECT 5	1 1 1 1 1 0 X X	Enables memory at a programmed Addr as defined in BR5 and OR5 registers
CHIP SELECT 6	1 1 1 1 1 1 0 1	Enables memory at a programmed Addr as defined in BR6 and OR6 registers
CHIP SELECT 7	1 1 1 1 1 1 1 0	Enables Memory at a Programmed Addr as defined in BR7 and OR7 registers
CHIP SELECT 6/7	1 1 1 1 1 1 0 0	Enables Memory at a Programmed Addr as defined in BR6/7 and OR6/7 registers
NO CHIP SELECT	1 1 1 1 1 1 1 1	None of the Chip Selects are asserted

Information on basic operations describes how to use symbolic values for triggering and for displaying other channel groups symbolically, such as for the Address channel group.

Acquiring and Viewing Disassembled Data

This section describes how to acquire data and view it disassembled. The information covers the following topics and tasks:

- Acquiring data
- Viewing disassembled data in various display formats
- Labeling Cycle type
- Changing the way data is displayed
- Changing disassembled cycles with the mark cycles function

Acquiring Data

Once you load the MPC850 support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your online help or *Appendix A: Error Messages and Disassembly Problems* in the Basic Operations User manual.

Viewing Disassembled Data

You can view disassembled data in four display formats: Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE*. Selections in the Disassembly property page must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–11*.

The default display format displays the Address, Data, Control, Tsize, Chipsel and Misc, channel group values for each sample of acquired data.

If a channel group is not visible, you must use the Disassembly property page to make the group visible.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–4 lists these special characters and strings, and gives a definition of what they represent.

Table 2–4: Description of special characters in the display

Character or string displayed	Definition
>> On the TLA 700	The instruction was manually marked using the Mark Cycle function.
0x	This indicates the given number is in Hexadecimal. Example: 0xEFFE
****	Indicates there is insufficient data available for complete disassembly of the instruction; the number of asterisks indicates the width of the data that is unavailable. Each two asterisks represent one byte.

Hardware Display Format

In the hardware display format, the disassembler displays certain cycle-type labels in parentheses, see Table 2–5.

Table 2–5: Cycle-type labels for sequences and definitions

Cycle type	Definition
(SUP RSV DATA : READ)	Reservation data, read, privilege state
(SUP RSV DATA : WRITE)	Reservation data, write, privilege state
(SUP DATA : READ)	Normal data, read, privilege state
(SUP DATA : WRITE)	Normal data, write, privilege state
(USR RSV DATA : READ)	Reservation data, read, user state
(USR RSV DATA : WRITE)	Reservation data, write, user state
(USR DATA : READ)	Normal data, read, user state
(USR DATA : WRITE)	Normal data, write, user state
(TRANSFER ERROR)	Transfer error cycle
(RETRY)	Retry cycle
(ROW ADDRESS)	Row Address Information in case of DRAM memories
(ADDRESS)	Address information for SRAM memories. This situation is possible with DRAM as a clocking option and the memory access is also done for SRAM memories. Then the same address will be acquired twice for SRAM.
(ROW_ADDR / ADDRESS)	Information entered in the user interface for the BRx register is invalid for the machine selected for memories.

Table 2–5: Cycle-type labels for sequences and definitions (Cont.)

Cycle type	Definition
(ALT MASTER)	Alternate Master Cycles
(UNKNOWN)	Unknown Cycle type. This combination of control bits is unexpected and/or unrecognized

Table 2–6 lists the following cycle types that are computed cycle types and not identifiable from their control signals.

Table 2–6: Cycle-type labels

Cycle type label	Definition
(CACHE FILL)	The processor will fetch only for filling the cache line but is not executed
(FLUSH)	The instruction is fetched but not executed
(EXTENSION)	This cycle is an extension to a preceding instruction opcode
* ILLEGAL INSTRUCTION *	Not a valid instruction

Figure 2–2 illustrates an example of the Hardware display.

Sample	MPC850 Address	MPC850 Data	MPC850 Mnemonics	MPC850 Control	MPC850 Tsize	MPC850 Chipsel	Timestamp
714	LOOP+6	06B4----	(EXTENSION)	SUP INST FETCH	HALF WORD	CHIP SELECT 0	77.462,000 us
716	LOOP+8	2C0C----	cmpi crf0,0,r12,0x0	SUP INST FETCH	WORD	CHIP SELECT 0	77.762,000 us
718	LOOP+A	0000----	(EXTENSION)	SUP INST FETCH	HALF WORD	CHIP SELECT 0	77.942,000 us
720	LOOP+C	4182----	bc 0xC,2,LOOP	SUP INST FETCH	WORD	CHIP SELECT 0	78.242,000 us
722	FFF05D42	FFF4----	(EXTENSION)	SUP INST FETCH	HALF WORD	CHIP SELECT 0	78.422,000 us
724	LOOP	8987----	lbz r12,0x0(r7)	SUP INST FETCH	WORD	CHIP SELECT 0	78.662,000 us
726	LOOP+2	0000----	(EXTENSION)	SUP INST FETCH	HALF WORD	CHIP SELECT 0	78.842,500 us
728	0E90002F	------00	(SUP DATA : READ)	SUP DATA READ	BYTE	CHIP SELECT 3	79.232,500 us
730	LOOP+4	558C----	rlwinm r12,r12,0,26,26	SUP INST FETCH	WORD	CHIP SELECT 0	79.532,500 us
732	LOOP+6	06B4----	(EXTENSION)	SUP INST FETCH	HALF WORD	CHIP SELECT 0	79.712,500 us
734	LOOP+8	2C0C----	cmpi crf0,0,r12,0x0	SUP INST FETCH	WORD	CHIP SELECT 0	80.012,500 us
736	LOOP+A	0000----	(EXTENSION)	SUP INST FETCH	HALF WORD	CHIP SELECT 0	80.192,000 us
738	LOOP+C	4182----	bc 0xC,2,LOOP	SUP INST FETCH	WORD	CHIP SELECT 0	80.492,500 us
740	FFF05D42	FFF4----	(EXTENSION)	SUP INST FETCH	HALF WORD	CHIP SELECT 0	80.672,500 us
742	LOOP	8987----	lbz r12,0x0(r7)	SUP INST FETCH	WORD	CHIP SELECT 0	80.912,000 us
744	LOOP+2	0000----	(EXTENSION)	SUP INST FETCH	HALF WORD	CHIP SELECT 0	81.092,500 us
746	0E90002F	------00	(SUP DATA : READ)	SUP DATA READ	BYTE	CHIP SELECT 3	81.482,500 us
748	LOOP+4	558C----	rlwinm r12,r12,0,26,26	SUP INST FETCH	WORD	CHIP SELECT 0	81.782,500 us
750	LOOP+6	06B4----	(EXTENSION)	SUP INST FETCH	HALF WORD	CHIP SELECT 0	81.962,500 us
752	LOOP+8	2C0C----	cmpi crf0,0,r12,0x0	SUP INST FETCH	WORD	CHIP SELECT 0	82.262,500 us
754	LOOP+A	0000----	(EXTENSION)	SUP INST FETCH	HALF WORD	CHIP SELECT 0	82.442,500 us
756	LOOP+C	4182----	bc 0xC,2,LOOP	SUP INST FETCH	WORD	CHIP SELECT 0	82.742,500 us
758	FFF05D42	FFF4----	(EXTENSION)	SUP INST FETCH	HALF WORD	CHIP SELECT 0	82.922,500 us
760	LOOP	8987----	lbz r12,0x0(r7)	SUP INST FETCH	WORD	CHIP SELECT 0	83.162,500 us
762	LOOP+2	0000----	(EXTENSION)	SUP INST FETCH	HALF WORD	CHIP SELECT 0	83.342,500 us
764	0E90002F	------00	(SUP DATA : READ)	SUP DATA READ	BYTE	CHIP SELECT 3	83.732,500 us
766	LOOP+4	558C----	rlwinm r12,r12,0,26,26	SUP INST FETCH	WORD	CHIP SELECT 0	84.032,500 us
768	LOOP+6	06B4----	(EXTENSION)	SUP INST FETCH	HALF WORD	CHIP SELECT 0	84.212,500 us
770	LOOP+8	2C0C----	cmpi crf0,0,r12,0x0	SUP INST FETCH	WORD	CHIP SELECT 0	84.512,500 us
772	LOOP+A	0000----	(EXTENSION)	SUP INST FETCH	HALF WORD	CHIP SELECT 0	84.692,500 us
774	LOOP+C	4182----	bc 0xC,2,LOOP	SUP INST FETCH	WORD	CHIP SELECT 0	84.992,500 us
776	FFF05D42	FFF4----	(EXTENSION)	SUP INST FETCH	HALF WORD	CHIP SELECT 0	85.172,500 us
778	LOOP	8987----	lbz r12,0x0(r7)	SUP INST FETCH	WORD	CHIP SELECT 0	85.412,500 us
780	LOOP+2	0000----	(EXTENSION)	SUP INST FETCH	HALF WORD	CHIP SELECT 0	85.592,500 us
782	0E90002F	------00	(SUP DATA : READ)	SUP DATA READ	BYTE	CHIP SELECT 3	85.982,500 us
784	LOOP+4	558C----	rlwinm r12,r12,0,26,26	SUP INST FETCH	WORD	CHIP SELECT 0	86.282,500 us
786	LOOP+6	06B4----	(EXTENSION)	SUP INST FETCH	HALF WORD	CHIP SELECT 0	86.462,500 us
788	LOOP+8	2C0C----	cmpi crf0,0,r12,0x0	SUP INST FETCH	WORD	CHIP SELECT 0	86.762,000 us
790	LOOP+A	0000----	(EXTENSION)	SUP INST FETCH	HALF WORD	CHIP SELECT 0	86.942,500 us
792	LOOP+C	4182----	bc 0xC,2,LOOP	SUP INST FETCH	WORD	CHIP SELECT 0	87.242,500 us
794	FFF05D42	FFF4----	(EXTENSION)	SUP INST FETCH	HALF WORD	CHIP SELECT 0	87.422,500 us
796	LOOP	8987----	lbz r12,0x0(r7)	SUP INST FETCH	WORD	CHIP SELECT 0	87.662,000 us
798	LOOP+2	0000----	(EXTENSION)	SUP INST FETCH	HALF WORD	CHIP SELECT 0	87.842,000 us
800	0E90002F	------00	(SUP DATA : READ)	SUP DATA READ	BYTE	CHIP SELECT 3	88.232,500 us
802	LOOP+4	558C----	rlwinm r12,r12,0,26,26	SUP INST FETCH	WORD	CHIP SELECT 0	88.532,500 us

Figure 2–2: Example of the hardware display format

Software Display Format

The Software display format displays only the first fetch of executed instructions. Flushed cycles and extensions are not displayed, even though they are part of the executed instruction. Data reads and writes are not displayed.

Control Flow Display Format

The Control Flow display format displays only the first fetch of instructions that change the flow of control.

Instructions that generate a change in the flow of control in the MPC8XX microprocessor are as follows:

bl	bla	sc	rfi

Instructions that might generate a change in the flow of control in the MPC8XX microprocessor are as follows:

bc	bca	bcl	bcla
bclr	bclrl	bcctr	bcctrl
tw	twi		

***NOTE**. Special cycles displayed in Subroutine display format are also displayed in the Control Flow Display Format.*

Subroutine Display Format

The Subroutine display format displays only the first fetch of subroutine call and return instructions. It will display conditional subroutine calls if they are considered to be taken.

Instructions that generate a subroutine call or a return in the MPC8XX microprocessor are as follows:

sc rfi

Instructions that might generate a subroutine call or a return in the MPC8XX microprocessor are as follows:

tw twi

Changing How Data is Displayed

There are common fields and features that allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page.

You can make selections unique to the MPC850 support to do the following tasks:

- Change how data is displayed across all display formats
- Change the interpretation of disassembled cycles
- Display exception cycles

Optional Display Selections

You can make optional selections for disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways:

For the TLA 700 Series:

Show: Hardware (default)
Software
Control Flow
Subroutine

Highlight: Software (default)
Control Flow
Subroutine
None

Disasm Across Gaps:
Yes
No (default)

Micro Specific Fields

Base Register 0. The Base Register 0 contains the Base Address and Address types for Chip Select 0.

The Default value of BR0: 00000000

Base Register 1. The Base Register 1 contains the Base Address and Address types for Chip Select 1.

The Default value of BR1: 00000000

Base Register 2. The Base Register 2 contains the Base Address and Address types for Chip Select 2.

The Default value of BR2: 00000000

Base Register 3. The Base Register 3 contains the Base Address and Address types for Chip Select 3.

The Default value of BR3: 00000000

Base Register 4. The Base Register 4 contains the Base Address and Address types for Chip Select 4.

The Default value of BR4: 00000000

Base Register 5. The Base Register 5 contains the Base Address and Address types for Chip Select 5.

The Default value of BR5: 00000000

Base Register 6. The Base Register 6 contains the Base Address and Address types for Chip Select 6.

The Default value of BR6: 00000000

Base Register 7 . The Base Register 7 contains the Base Address and Address types for Chip Select 7.

The Default value of BR7: 00000000

NOTE*. The Base Register provides the information for base address, port size and the machine selected. If the information is not correct, the disassembled data may be corrupted.*

Byte Ordering. Byte ordering is selected from one of the following options.

Byte Order:	Big Endian (default) Lit Endian PPC Little

Exception Prefix. Valid Exception Prefix is selected from one of the following two options, depending on the system configuration.

Exception Prefix :	000 (default) FFF

AMA bits. The memory controller is programmed for DRAM interface. The programming is based on the DRAM configuration used for the interface using the AMA bits in the machine mode register A, respectively. To access DRAM the machine UPMA is used. The AMA bits are set as programmed in machine mode register A.

Refer to Table 15–8 in the *MPC850 User's manual* or *MPC823 User's manual* or Table 15–6 in the *MPC801 User's Manual* for details on programming the AMX bits.

The options are:

AMA:
000 (default)
001
010
011
100
101

AMB bits. The memory controller is programmed for DRAM interface. The programing is based on the DRAM configuration used for the interface using the AMB bits in machine mode register B, respectively. To access the DRAM, the machine UPMB is used. The AMB bits are set when programmed in the machine mode register B.

Refer to Table 15–8 in *MPC850 User's manual* or *MPC823 User's manual* or Table 15–6 in the *MPC801 User's Manual* for details on programming the AMX bits.

The options are:

AMB:
000 (default)
001
010
011
100
101

Other Options for Chip Selects, Arbitration and Row Suppression. The following information is entered to determine if Chip Selects pins 6 and 7 are enabled, internal arbitration is enabled, and if you want to suppress row cycles for DRAM memories.

Value[1]	Definition
1 bit for CS(6:7)	Inactive
1 bit for Int_Arb	Internal on-chip arbiter is enabled
0 bit for Row_Sup	Do not suppress row cycles

[1] Default for CS(6:7), Int_Arb, and Row_Sup = 0xE

Marking Cycles

The disassembler has a Mark Opcode function that allows you to change the interpretation of a cycle type. Using this function, you can select a cycle and change it.

NOTE. *The* TMS 561 *support will only allow marking of instruction fetch cycles that also includes read extensions and flush cycles.*

Marks are placed by using the Mark Opcode button. The Mark Opcode button will always be available. If the sample being marked is not an address cycle or data cycle of the potential bus master, the Mark Opcode selections will be replaced by a note indicating that an Opcode Mark cannot be placed at the selected data sample.

When a cycle is marked, the character >> is displayed immediately to the left of the Mnemonics column. Cycles can be unmarked by using the Undo Mark selection, which will remove the character >>.

Table 2–7 describes the mark selections.

Table 2–7: Mark selections and definitions

Mark selection or combination†	Definition
`Opcode`	Marks cycle as an instruction opcode
`Extension`	Marks cycle as an extension to an instruction opcode
`Flush`	Marks cycle as a flushed cycle
`Undo Mark`	Removes all marks

Displaying Exception Labels

The disassembler can display MPC8XX exception labels. The exception table must reside in external memory for interrupt and exception cycles to be visible to the disassembler.

Select the table prefix in the Exception Prefix field. The Exception Prefix field provides the disassembler with the prefix value. Select a three-digit hexadecimal value from the two values provided, corresponding to the prefix of the exception table.

These fields are located in the Disassembly property page.

Table 2–8 lists the MPC8XX interrupt and exception labels.

Table 2–8: Interrupt and exception labels

Offset	Displayed interrupt or exception name
0x00000	(RESERVED)
0x00100	(SYSTEM RESET)
0x00200	(MACHINE CHECK)
0x00300	(DATA STORAGE)
0x00400	(INSTRUCTION STORAGE)
0x00500	(EXTERNAL)
0x00600	(ALIGNMENT)
0x00700	(PROGRAM)
0x00900	(DECREMENTER)
0x00A00	(RESERVED)
0x00B00	(RESERVED)
0x00C00	(SYSTEM CALL)
0x00D00	(TRACE)
0x01000	(SOFTWARE EMULATION)
0x01100	(INSTRUCTION TLB MISS)
0x01200	(DATA TLB MISS)
0x01300	(INSTRUCTION TLB ERROR)
0x01400	(DATA TLB ERROR)
0x01500 to 0x01BFF	(RESERVED)
0x01C00	(DATA BREAKPOINT)
0x01D00	(INSTRUCTION BREAKPOINT)
0x01E00	(PERIPHERAL BREAKPOINT)
0x01F00	(NON MASKABLE DEVELOPMENT PORT)

Viewing an Example of Disassembled Data

A demonstration system file is provided so you can see an example of how your MPC8XX microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use and you can view it without connecting the logic analyzer to your system under test.

Information on basic operations describes how to view the file.

Specifications

Specifications

This chapter contains information regarding the specifications of the support.

Specification Tables

Table 3–1 lists the electrical requirements the system under test must produce for the support to acquire correct data.

Table 3–1: Electrical specifications

Characteristics	Requirements
System under test clock rate	
Specified clock rate	
MPC850/823	50 MHz Maximum
MPC801	40 MHz Maximum
Tested clock rate	
MPC850/823	33 MHz Maximum
MPC801	40 MHz Maximum
Minimum setup time required	2.5 ns
Minimum hold time required	0 ns

Replaceable Parts List

Replaceable Parts

This section contains a list of the replaceable parts for the TMS 561 MPC850 microprocessor support product.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order.

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077–0001

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					STANDARD ACCESSORIES		
	071–0374–00			1	MANUAL, TECH: INSTRUCTIONS, MPC850, TMS561	80009	071–0374–00
	070–9803–00			1	MANUAL,TECH:INSTRUCTION,MICROPROCESSOR SUPPORT,PKG INSTALLATION,TLA700 SERIES,LOGIC ANALYZER	TK2548	070–9803–00

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