Instruction Manual

Tektronix

TMS 806
Accelerated Graphics Port Bus Support

070-9906-00

There are no current European directives that apply to this product. This product provides cable and test lead connections to a test object of electronic measuring and test equipment.

Warning
The servicing instructions are for use by qualified personnel only. To avoid personal injury, do not perform any servicing unless you are qualified to do so. Refer to all safety summaries prior to performing service.

Printed in the U.S.A.

Tektronix, Inc., P.O. Box 1000, Wilsonville, OR 97070–1000

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General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

Only qualified personnel should perform service procedures.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

To Avoid Fire or Personal Injury

Connect and Disconnect Properly. Do not connect or disconnect probes or test leads while they are connected to a voltage source.

Observe All Terminal Ratings. To avoid fire or shock hazard, observe all ratings and marking on the product. Consult the product manual for further ratings information before making connections to the product.

Do Not Operate Without Covers. Do not operate this product with covers or panels removed.

Avoid Exposed Circuitry. Do not touch exposed connections and components when power is present.

Do Not Operate With Suspected Failures. If you suspect there is damage to this product, have it inspected by qualified service personnel.

Do Not Operate in Wet/Damp Conditions.

Do Not Operate in an Explosive Atmosphere.

Keep Product Surfaces Clean and Dry.

Provide Proper Ventilation. Refer to the manual's installation instructions for details on installing the product so it has proper ventilation.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

WARNING
High Voltage

Protective Ground
(Earth) Terminal

CAUTION
Refer to Manual

Double
Insulated

Service Safety Summary

Only qualified personnel should perform service procedures. Read this *Service Safety Summary* and the *General Safety Summary* before performing any service procedures.

Do Not Service Alone. Do not perform internal service or adjustments of this product unless another person capable of rendering first aid and resuscitation is present.

Disconnect Power. To avoid electric shock, disconnect the main power by means of the power cord or, if provided, the power switch.

Use Care When Servicing With Power On. Dangerous voltages or currents may exist in this product. Disconnect power, remove battery (if applicable), and disconnect test leads before removing protective panels, soldering, or replacing components.

To avoid electric shock, do not touch exposed connections.

Preface

This instruction manual contains specific information about the TMS 806 Accelerated Graphics Port bus support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating bus support packages on the logic analyzer for which the TMS 806 Accelerated Graphics Port support was purchased, you will probably only need this instruction manual to set up and run the support.

If you are not familiar with operating bus support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support.

Information on basic operations of bus support packages is included with each product. Each logic analyzer has basic information that describes how to perform tasks common to support packages on that platform. This information can be in the form of online help, an installation manual, or a user manual.

This manual provides detailed information on the following topics:

- Connecting the logic analyzer to the system under test
- Setting up the logic analyzer to acquire data from the system under test
- Acquiring and viewing data
- Using the probe adapter

Manual Conventions

This manual uses the following conventions:

- In the information on basic operations, the term XXX or P54C used in field selections and file names must be replaced with AGP. This is the name of the bus in field selections and file names you must use to operate the Accelerated Graphics Port support.
- The term system under test (SUT) refers to the bus-based system from which data will be acquired.
- The term logic analyzer refers to the Tektronix logic analyzer for which this product was purchased.
- The term module refers to a 136-channel module.
- A pound sign (#) following a signal name indicates an active low signal.

Logic Analyzer Documentation

A description of other documentation available for each type of Tektronix logic analyzer is located in the corresponding module user manual. The manual set provides the information necessary to install, operate, maintain, and service the logic analyzer and associated products.

Contacting Tektronix

Product Support	For application-oriented questions about a Tektronix measurement product, call toll free in North America: 1-800-TEK-WIDE (1-800-835-9433 ext. 2400) 6:00 a.m. – 5:00 p.m. Pacific time Or, contact us by e-mail: tm_app_supp@tek.com For product support outside of North America, contact your local Tektronix distributor or sales office.
Service Support	Contact your local Tektronix distributor or sales office. Or, visit our web site for a listing of worldwide service locations. http://www.tek.com
For other information	In North America: 1-800-TEK-WIDE (1-800-835-9433) An operator will direct your call.
To write us	Tektronix, Inc. P.O. Box 1000 Wilsonville, OR 97070-1000

Getting Started

Getting Started

This chapter provides information on the following topics and tasks:

- A description of the TMS 806 bus support package
- Logic analyzer software compatibility
- Your system-under-test (SUT) requirements
- Support restrictions
- How to configure the probe adapter
- How to connect to the system under test

Support Description

The TMS 806 bus support package displays data from systems that are based on the Accelerated Graphics Port bus (AGP bus). The support runs on a compatible Tektronix logic analyzer equipped with a 136-channel module.

Refer to information on basic operations to determine how many modules and probes your logic analyzer needs to meet the minimum channel requirements for the TMS 806 bus support. Information on basic operations also contains a general description of the supports.

A complete list of standard and optional accessories is provided at the end of the parts list in the *Replaceable Mechanical Parts* chapter.

To use this support efficiently, you need to have the items listed in the information on basic operations as well as the *Accelerated Graphics Port Interface Specification*, Intel, 1996.

Logic Analyzer Software Compatibility

The label on the bus-support floppy disk states which version of logic analyzer software is compatible with the support.

Logic Analyzer Configuration

To use the TMS 806 support, the Tektronix logic analyzer must be equipped with a 136-channel module at a minimum. The module must be equipped with enough probes to acquire channel and clock data from signals in your AGP bus-based system.

Refer to information on basic operations to determine how many modules and probes the logic analyzer needs to meet the channel requirements.

Requirements and Restrictions

You should review the general requirements and restrictions of bus supports in the information on basic operations as they pertain to your SUT.

You should also review electrical, environmental, and mechanical specifications in the *Specifications* chapter in this manual as they pertain to your system under test, as well as the following descriptions of other AGP support requirements and restrictions.

System Clock Rate

The TMS 806 support package can acquire data from the AGP bus operating at speeds of up to 66 MHz[1].

2X Mode Time Alignment

When your SUT runs in 2X or 2X_SBA mode, you must align the setup time of the logic analyzer with the source synchronous bus before you acquire data. This procedure starts on page 2–6.

NOTE. *If your system meets the timing requirements specified in the* Accelerated Graphics Port Interface Specification, *Intel, 1996, this support will correctly acquire data. If your system runs in 2X or 2X_SBA mode, you must first align the setup time of the logic analyzer with the source synchronous bus as described on page 2–6.*

Fast Write PCI Cycles

The TMS 806 support package does not acquire Fast Write PCI cycles.

AGP 4X Bus Support

The TMS 806 support package does not acquire data from systems based on the AGP-4X bus.

Merged Module Pair

If you have a pair of modules that are merged in the logic analyzer, you can demerge them (and use either one). If you want the modules to remain merged, then the probe adapter must connect to the module in the lower numbered slot.

1 **Specification at time of printing. Contact your Tektronix sales representative for current information on the fastest buses supported.**

Configuring the Probe Adapter

The probe adapter contains two jumpers: J100 must be positioned to match the operating mode of your SUT (PIPE or SBA) and J200 must be positioned to match the data transfer rate of your SUT (1X or 2X).

Table 1–1 shows the possible jumper positions. For more information on when to use each combination, refer to Table 2–6 on page 2–6. Figure 1–1 shows the jumper locations on the AGP probe adapter.

Table 1–1: Jumper positions

Support setup	Jumper setting	J100 position	J200 position
AGP_1X	PIPE	Pins 1 and 2	Pins 1 and 2
	SBA	Pins 2 and 3	Pins 1 and 2
AGP_2X*	PIPE	Pins 1 and 2	Pins 2 and 3
	SBA	Pins 2 and 3	Pins 2 and 3

*** You must follow the procedure to align the setup time of the logic analyzer with the source synchronous bus before you acquire data.**

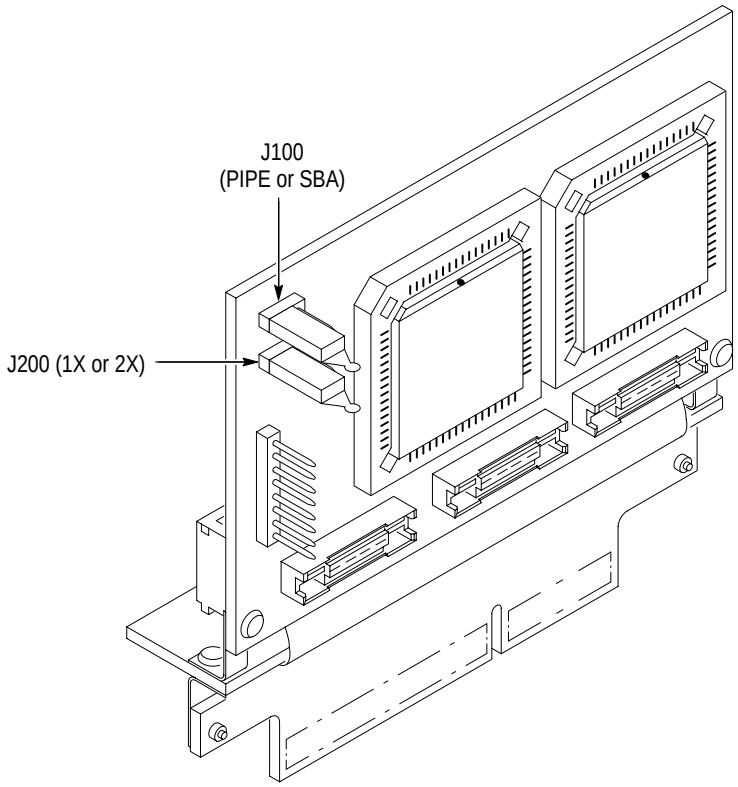


Figure 1–1: Jumper locations on the AGP probe adapter

Connecting to a System Under Test

Your SUT must have a minimum amount of clear space surrounding the AGP Graphics Card connector to accommodate the probe adapter. Refer to Figure 3–1 on page 3–3 for the required clearances.

NOTE. *Do not allow the probe adapter to interfere with any adjacent PCI slot, slot 1 or slot 0 microprocessors. If necessary, you can use the P6434 Low-Profile Extenders to avoid mechanical interference with other circuit boards in your SUT.*

To connect the logic analyzer to a SUT using the probe adapter, follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the graphics card, the probe adapter, the probes, or the module. To prevent static damage, handle all of these products only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the graphics card and probe adapter.

2. Before you remove the probe adapter from the bag it is shipped in, touch the bag to the ground connector located on the back of the logic analyzer to discharge stored static electricity from the probe adapter. To discharge your stored static electricity, touch the ground connector.
3. Follow the procedure from the AGP Graphics Card vendor to remove the AGP Graphics card from your SUT.
4. Line up the pin A1 indicator on the AGP Graphics card with the pin A1 indicator on the probe adapter.

CAUTION. *Failure to correctly place the AGP Graphics card into the probe adapter might permanently damage the graphics card, probe adapter, or SUT once power is applied.*

5. Insert the AGP Graphics card into the probe adapter as shown in Figure 1–2.

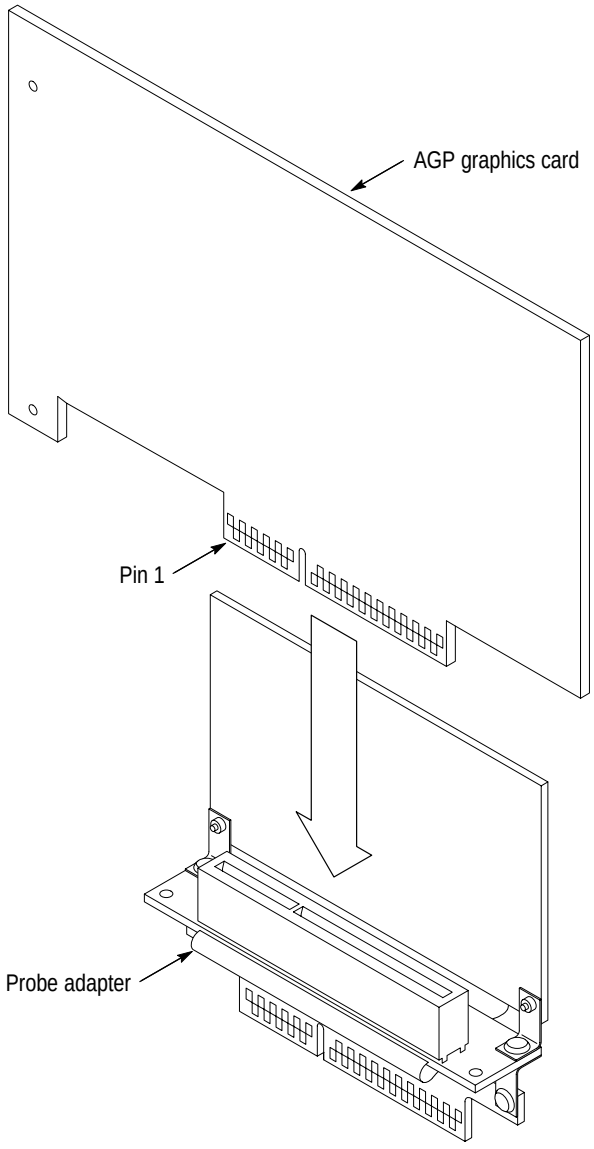


Figure 1–2: Placing the AGP Graphics card into the probe adapter

6. Line up the pin A1 indicator on the AGP probe adapter with the pin A1 indicator for the AGP Graphics card connector in the SUT.

CAUTION. *Failure to correctly place the probe adapter into the SUT can permanently damage the graphics card, probe adapter, or SUT once power is applied.*

7. Insert the probe adapter into the AGP graphics card connector as shown in Figure 1–3.

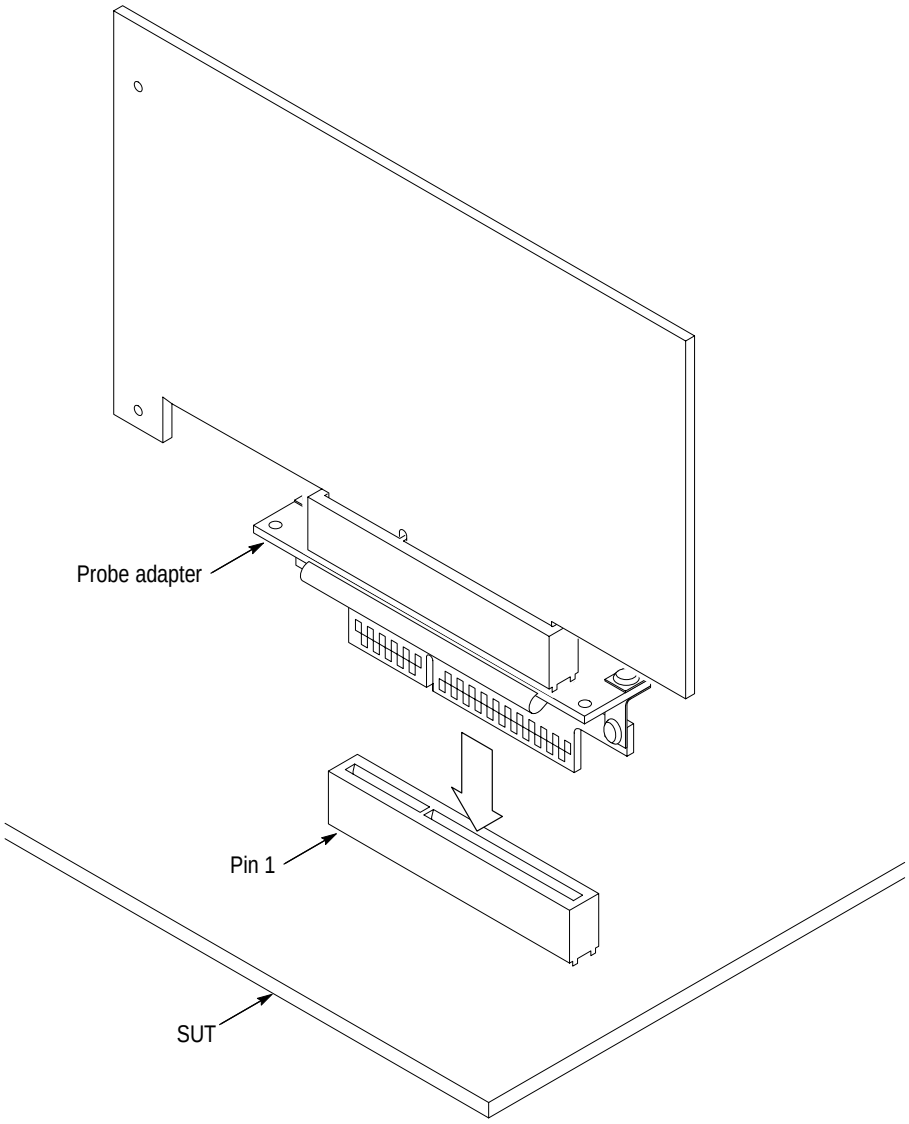


Figure 1–3: Placing the probe adapter into the SUT bus connector

8. Line up the pin 1 indicator on the probe label with pin 1 of the connector on the probe adapter. Match the A, C, and E probes with the corresponding A, C, and E probe connectors.

NOTE*. The D probe is not needed and is not connected for this support.*

CAUTION. *Incorrect handling of the P6434 probe while connecting it to the probe adapter can result in damage to the probe or to the mating connector on the probe adapter. To avoid damaging the probe and probe adapter, always position the probe perpendicular to the mating connector and gently connect the probe.*

9. Position the probe tip perpendicular to the mating connector and gently connect the probe as shown in Figure 1–4.

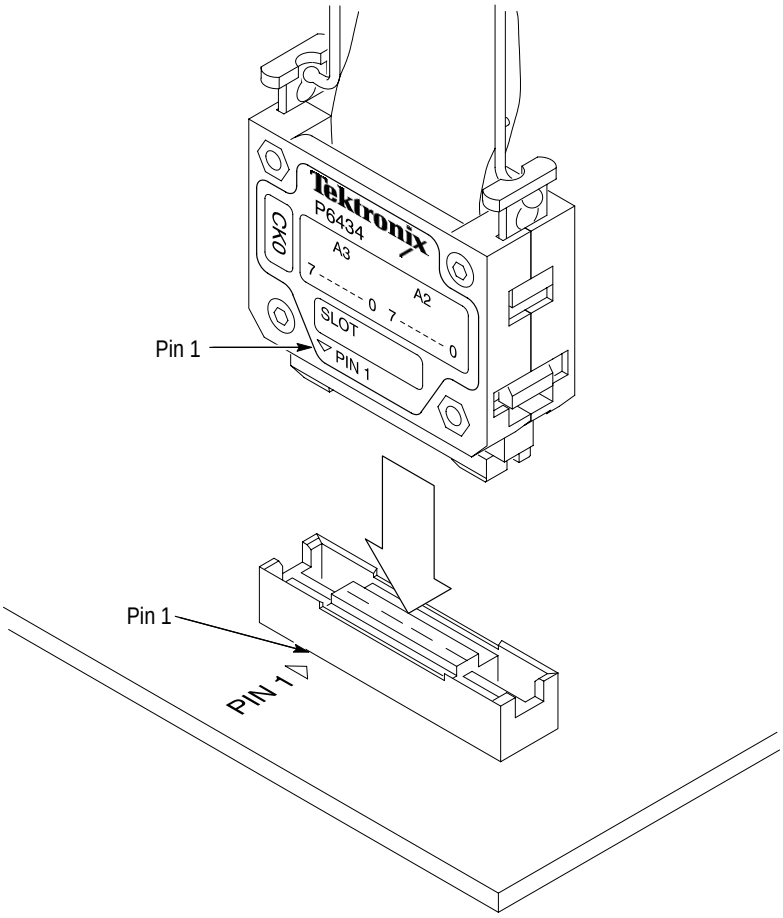


Figure 1–4: Connecting a probe to the probe adapter

10. Connect the module ends of the P6434 probes to the corresponding connectors (match label colors) on the logic analyzer. The probe module ends are keyed.

11. Apply forced air cooling across the AGP graphics card consistent with the recommendations of the manufacturer.

Operating Basics

Setting Up the Support

This section describes how to set up the support and includes the following topics:

- Channel group definitions
- Clocking options
- Symbol table files
- Software and probe adapter configurations
- Logic analyzer setup time alignment procedure for the AGP_2X setup

Remember that the information in this section is specific to the operations and functions of the TMS 806 AGP support package. Information on basic operations describes general tasks and functions.

Before you acquire and display data, you need to load the support and specify setups for clocking and triggering as described in the information on basic operations. The support provides default values for each of these setups, but you can change them as needed.

Channel Group Definitions

The software automatically defines channel groups for the support. There are two setups available with the TMS 806 software: AGP_1X and AGP_2X.

AGP_1X Setup

The channel groups defined for the AGP_1X setup are AD, BE, Command, Status, SBE, SBA, QI_Ctrl, Inc_QCnt, Dec_QCnt, Control and Misc.

To see which signal is in which channel group, refer to the channel group assignment tables beginning on page 3–7. Tables 3–5 through 3–15 show the channel assignments for the AGP_1X setup.

AGP_2X Setup

The channel groups defined for the AGP_2X setup are AD_Hi, AD_Lo, BE_Hi, BE_Lo, Command, Status, SBE, SBA_Hi, SBA_Lo, QI_Ctrl, Inc_QCnt, Dec_QCnt, Control, Misc, AD_STB1, AD_STB0 and SB_STB.

To see which signal is in which channel group, refer to the channel group assignment tables beginning on page 3–12. Tables 3–16 through 3–32 show the channel assignments for the AGP_2X setup.

Before you acquire data from a SUT with a source-synchronous bus, you must align the setup time on the logic analyzer. This procedure starts on page 2–6.

Clocking Options

The TMS 806 support offers a bus-specific clocking mode for the AGP bus. Custom clocking is the default selection whenever you load the AGP_1X or AGP_2X support. The clocking algorithm for both setups has two variations: Active Cycles Only or Clock-by-Clock.

Active Cycles Only. Address, Data and Status signals are always logged. The clocking software stores a sample whenever there is an active cycle.

Clock-By-Clock. The clocking software stores every cycle on every rising edge of the CLK signal.

A description of how cycles are sampled by the module using the support and probe adapter is found in the *Specifications* chapter beginning on page 3–20.

Symbols

The TMS 806 support supplies five symbol table files. Each file replaces specific channel group values with symbolic values when Symbolic is the radix for the channel group. Table 2–1 shows the name, bit pattern, and meaning for the symbols in the file AGP_Command, the Command channel group symbol table.

Table 2–1: Command group symbol table definitions

Symbol	Command group value		Meaning
	IRDY# FRAME# PIPE#	C/BE3# C/BE2# C/BE1# C/BE0#	
–	X 1 1	X X X X	Not an AGP or PCI command
Bus Fault	X 0 0	X X X X	Bus Fault
AGP_Rd_LP	X 1 0	0 0 0 0	AGP Low Priority Read
AGP_Rd_HP	X 1 0	0 0 0 1	AGP High Priority Read
AGP_Wr_LP	X 1 0	0 1 0 0	AGP Low Priority Write
AGP_Wr_HP	X 1 0	0 1 0 1	AGP High Priority Write
AGP_Lg_Rd_LP	X 1 0	1 0 0 0	AGP Low Priority Long Read
AGP_Lg_Rd_HP	X 1 0	1 0 0 1	AGP High Priority Long Read
AGP_Flush	X 1 0	1 0 1 0	AGP Flush command
AGP_Fence	X 1 0	1 1 0 0	AGP Fence command
AGP_Ext_Addr	X 1 0	1 1 0 1	AGP Extended Address command
AGP_Lg_Rd	X 1 0	1 0 0 X	AGP Long Read
AGP_Rd	X 1 0	0 0 0 X	AGP Read

Table 2–1: Command group symbol table definitions (cont.)

Symbol	Command group value IRDY# FRAME# PIPE# C/BE3# C/BE2# C/BE1# C/BE0#	Meaning
AGP_Wr	X 1 0 0 1 0 X	AGP Write
AGP_Cmd	X 1 0 X X X X	Any AGP command
PCI_Int_Ack	1 0 1 0 0 0 0	PCI Interrupt Acknowledge
PCI_Special	1 0 1 0 0 0 1	PCI Special command
PCI_I/O_Rd	1 0 1 0 0 1 0	PCI Input/Output Read
PCI_I/O_Wr	1 0 1 0 0 1 1	PCI Input/Output Write
PCI_Mem_Rd	1 0 1 0 1 1 0	PCI Memory Read
PCI_Mem_Wr	1 0 1 0 1 1 1	PCI Memory Write
PCI_Config_Rd	1 0 1 1 0 1 0	PCI Configuration Read
PCI_Config_Wr	1 0 1 1 0 1 1	PCI Configuration Write
PCI_Mem_Rd_Mul	1 0 1 1 1 0 0	PCI Memory Read Multiple
PCI_Ext_Addr	1 0 1 1 1 0 1	PCI Extended Address
PCI_Mem_Rd_Line	1 0 1 1 1 1 0	PCI Memory Read Line
PCI_Mem_Rd_Inv	1 0 1 1 1 1 1	PCI Memory Write and Invalidate
PCI_I/O_R/W	1 0 1 0 0 1 X	PCI Input/Output Read/Write
PCI_Mem_R/W	1 0 1 0 1 1 X	PCI Memory Read/Write
PCI_Config_R/W	1 0 1 1 0 1 X	PCI Configuration Read/Write
PCI_Cmd	1 0 1 X X X X	Any PCI command
~	0 0 1 X X X X	PCI data (not the last data)

Table 2–2 shows the name, bit pattern, and meaning for the symbols in the file AGP_Status, the Status channel group symbol table.

Table 2–2: Status group symbol table definitions

Symbol	Status group value GNT# ST2 ST1 ST0	Meaning
–	1 X X X	Grant not asserted
~	0 1 1 1	Transaction Request
Rd_LP	0 0 0 0	Low Priority Read
Rd_HP	0 0 0 1	High Priority Read
Wr_LP	0 0 1 0	Low Priority Write

Table 2–2: Status group symbol table definitions (cont.)

Symbol	Status group value				Meaning
	GNT#	ST2	ST1	ST0	
Wr_HP	0	0	1	1	High Priority Write
Rd	0	0	0	X	Any Read
Wr	0	0	1	X	Any Write
Rd/Wr	0	0	X	X	Any Read or Write
LP	0	0	X	0	Any Low Priority
HP	0	0	X	1	Any High Priority

Table 2–3 shows the name, bit pattern, and meaning for the symbols in the file AGP_SBE, the Side Band Enable channel group symbol table.

Table 2–3: SBE group symbol table definitions

Symbol	SBE group value					Meaning
	SBE_D#	SBA7	SBA6	SBA5	SBA4	
–	1	X	X	X	X	Not a Sideband command
T-1	0	0	X	X	X	Type 1 Sideband command
T-2	0	1	0	X	X	Type 2 Sideband command
T-3	0	1	1	0	X	Type 3 Sideband command
T-4	0	1	1	1	0	Type 4 Sideband command
SBE	0	X	X	X	X	Any Sideband command

Table 2–4 shows the name, bit pattern, and meaning for the symbols in the file AGP_QI_Ctrl, the QI Control channel group symbol table.

Table 2–4: QI group symbol table definitions

Symbol	QI Control group value			Meaning
	VAL_ID#	QICNT_ID1	QICNT_ID0	
–	1	X	X	Valid ID not asserted
Rd_LP	0	0	0	Low Priority Read
Rd_HP	0	0	1	High Priority Read
Wr_LP	0	1	0	Low Priority Write
Wr_HP	0	1	1	High Priority Write

Table 2–5 shows the name, bit pattern, and meaning for the symbols in the file AGP_Control, the Control channel group symbol table.

Table 2–5: Control group symbol table definitions

Symbol	Control group value RST# RBF# REQ# IRDY# PME# SERR# GNT# TRDY# PERR# PIPE# DEVSEL# PAR FRAME# STOP#	Meaning
Reset	0 X X X X X X X X X X X X	Reset
Sys_Err	1 X X 0 X X X X X X X X X	System Error
Par_Err	1 X X X 0 X X X X X X X X	Parity Error
AGP_Addr	1 X X X X X X 0 1 1 1 1 X	AGP Address
PCI_Addr	1 X X X X X X 1 0 1 1 1 X	PCI Address
PCI_Data	1 X X X X X X 1 X 0 0 0 1	PCI Data
PCI_Abort	1 X X X X X X 1 X 0 X 1 0	PCI Target Abort
PCI_Discon	1 X X X X X X 1 X 0 X 0 0	PCI Target Disconnect
IRDY TRDY	1 X X X X X X X X 0 0 X X	IRDY/TRDY asserted
IRDY	1 X X X X X X X X 0 X X X	IRDY asserted
TRDY	1 X X X X X X X X X 0 X X	TRDY asserted
Rd_Buf_Fl	1 X 0 X X X X X X X X X X	Read Buffer Full
Grant	1 X X X X X X 0 X X X X X	Grant asserted
Request	1 X X X X X 0 X X X X X X	Request asserted
Stop	1 X X X X X X X X X X X 0	Stop asserted
Dev_Sel	1 X X X X X X X X X X 0 X	Device Select asserted
Pwr_Mgmt_En	1 0 X X X X X X X X X X X	Power Management Enable
Pipe	1 X X X X X X 0 1 X X X X	PIPE asserted
Frame	1 X X X X X X 1 0 X X X X	Frame asserted
–	1 1 1 1 1 X 1 1 1 1 1 1 1	Bus inactive
AGP_Cycle	X X X X X X X X 1 X X 1 1	AGP cycle*

* **For more information, refer to the *Acquiring Only AGP or PCI Cycles* on page 2–21.**

Information on basic operations describes how to modify an existing symbol table, create new symbol tables, and use symbolic values for triggering and displaying other channel groups symbolically, such as the Address channel group.

Support Setup and Probe Adapter Configurations

The AGP support package includes two setups, and two jumpers (on the probe adapter). Table 2–6 shows combinations you can use based on the operating mode of the AGP bus and the type of data you want to acquire.

Table 2–6: Support and probe adapter setup combinations

Bus operating mode	Support set-up*	J100 position	J200 position	Data acquired
1X PIPE	AGP_1X	PIPE	1X	1X PIPE and PCI
1X SBA		SBA	1X	1X SBA and PCI
2X PIPE	AGP_2X†	PIPE	2X	2X PIPE and PCI
2X SBA		SBA	2X	2X SBA and PCI

***** **The AGP_2X setup demultiplexes data; the AGP_1X setup does not.**

† **Before you acquire data from a SUT with a source-synchronous bus, you must align the setup time on the logic analyzer as described next.**

Logic Analyzer Time Alignment for the AGP_2X Setup

The setup time alignment of the logic analyzer to a SUT with a source-synchronous bus is crucial. To ensure that the logic analyzer acquires correct data, you must follow these procedures and make setup timing adjustments.

Some figures only show the relevant parts of setup windows and dialog boxes.

NOTE. *If you do not align the setup time for the logic analyzer when using the AGP_2X setup, acquired data will be incorrect.*

Figure 2–1 shows the function of the setup time alignment procedures.

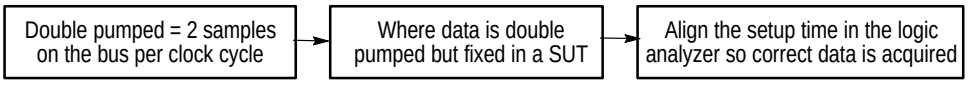


Figure 2–1: Function of the setup time alignment procedures

Figure 2–2 shows a block diagram of the setup time alignment procedure.

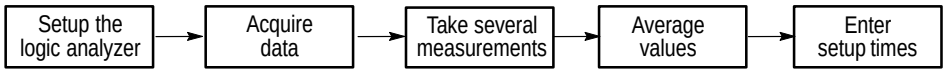


Figure 2–2: Block diagram of the setup time alignment procedure

There are two procedures to align the setup time. Each procedure is based on the operating mode of the AGP bus in your SUT: 2X or 2X_SBA.

NOTE. *You must follow these procedures each time you move the probe adapter to another AGP system operating in 2X or 2X_SBA mode.*

Aligning for 2X Mode

To determine the proper time to sample 2X data, you need to check the timing relationship between the rising edge of the CLK signal and the AD_Hi, BE_Hi, AD_STB1 and AD_STB0 channel groups.

In the MagniVu display, the AD_Hi and BE_Hi channel groups contain double-pumped data. (Double-pumped data is when there are two samples on the bus per clock cycle.)

In this procedure, you will take measurements to align the demultiplexed timing for the AD_Hi, AD_Lo, BE_Hi, BE_Lo, AD_STB1 and AD_STB0 groups.

You will use the cursors to take eight sets of measurements, which should take about 15 minutes. Before you start, photocopy Table 2–7 and fill it in as you go.

Table 2–7: Calculating the setup time offset of the logic analyzer for 2X mode

Value number	AD_Hi, BE_Hi	AD_Hi, BE_Hi		AD_Hi, BE_Hi	AD_STB1 or AD_STB0	AD_STB1 or AD_STB0
1						
2						
3						
4						
5						
6						
7						
8						
Smallest		Not used		Not used		Not used
Largest	Not used		Not used		Not used	
Averages	1.		2.		3.	

To align the setup time of the logic analyzer with a source-synchronous bus operating in 2X mode, refer to Figure 2–3 through Figure 2–13 and follow these steps:

1. From the System window, in the File menu, select Load System.
2. From the Load System dialog box, select Program Files, then TLA700, then Supports, and AGP_2X. Figure 2–3 shows the Load System window with the 2X Cal Setup.tla and AGP_2X.tla system setups.

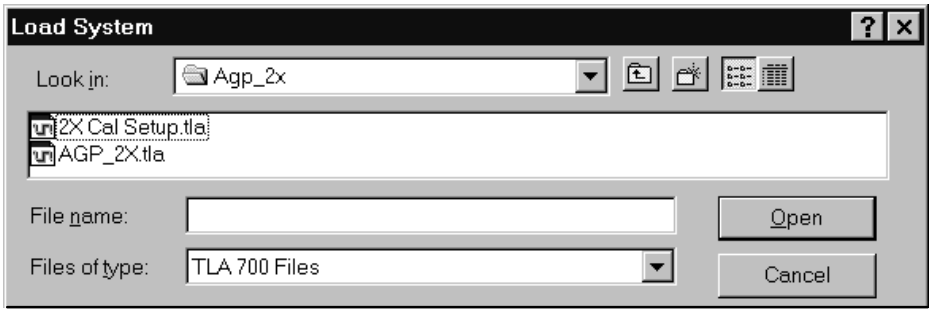


Figure 2–3: Setup: Load System menu

3. Select the 2X Cal Setup.tla file. Click No in the caution dialog box. If an Information dialog box appears, click OK.

   The Load System Options dialog box may or may not appear.

4. If the Load System Options dialog box appears and the AGP_2X setup is not loaded to the Current System, then drag the AGP_2X icon to the desired module and click OK.

   Figure 2–4 shows the Load System Options dialog box before dragging the AGP_2X icon to the module in the Current System.

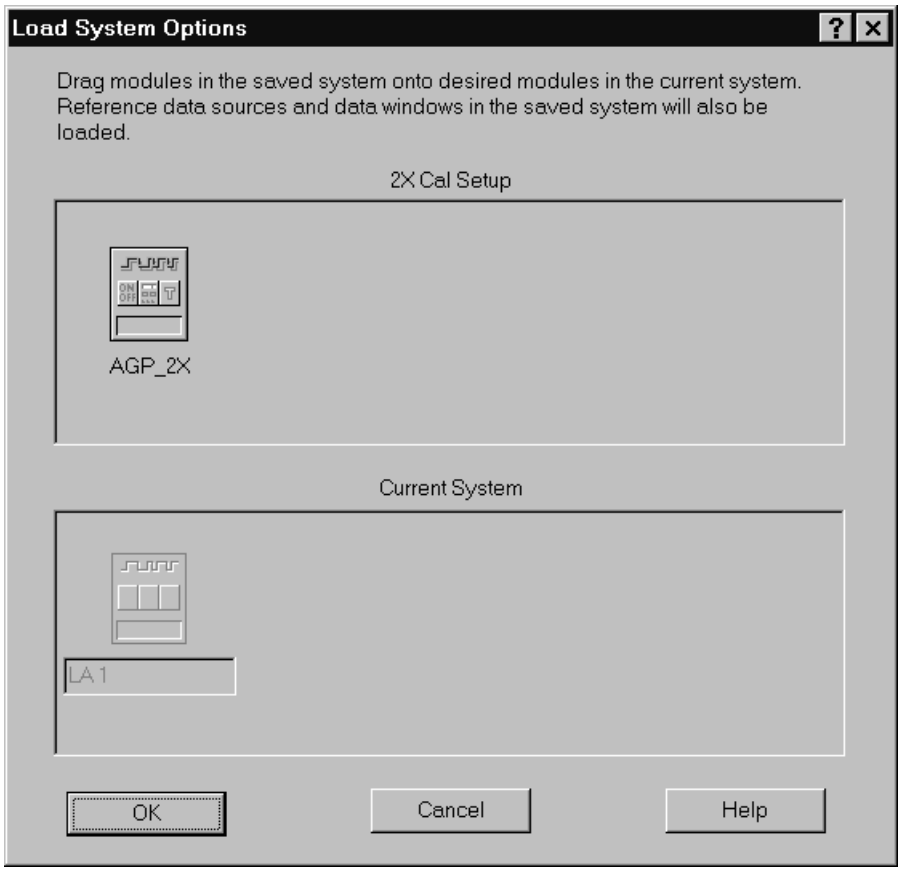


Figure 2–4: Load System Options dialog box

Figure 2–5 shows the 2X Cal Setup file loaded in the System window.

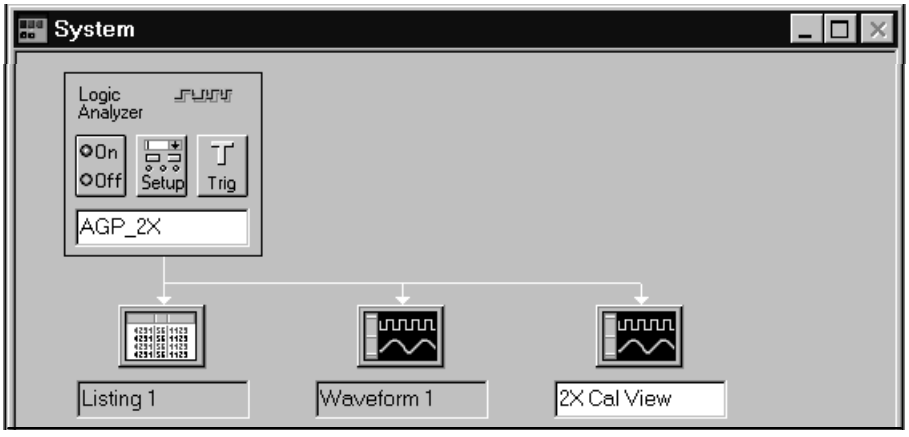


Figure 2–5: System window with the 2X Cal Setup file

5. The logic analyzer must trigger on the Status channel group. Click the Trigger icon. The Trigger: AGP_2X dialog box appears with a predefined trigger. Figure 2–6 shows the setup to trigger on any Read cycle.

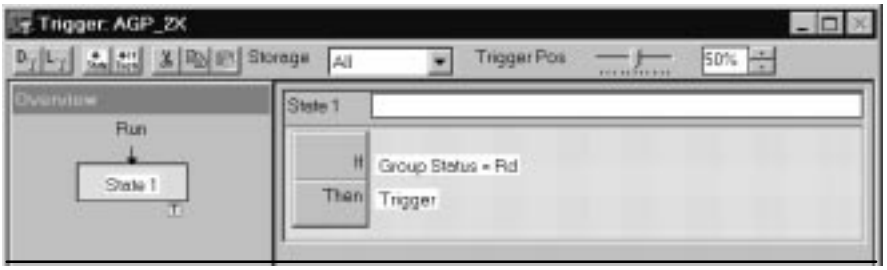


Figure 2–6: Trigger setup for any Read cycle in the Status channel group

6. With the SUT running, click the RUN button to acquire data. After triggering, select the 2X Cal View Waveform window.

   Figure 2–7 shows acquired data in a MagniVu display. The first display line is called Mag_Sample and contains small marks; each mark represents 500 picoseconds. The Time/Div in the display is set to 2 nanoseconds.

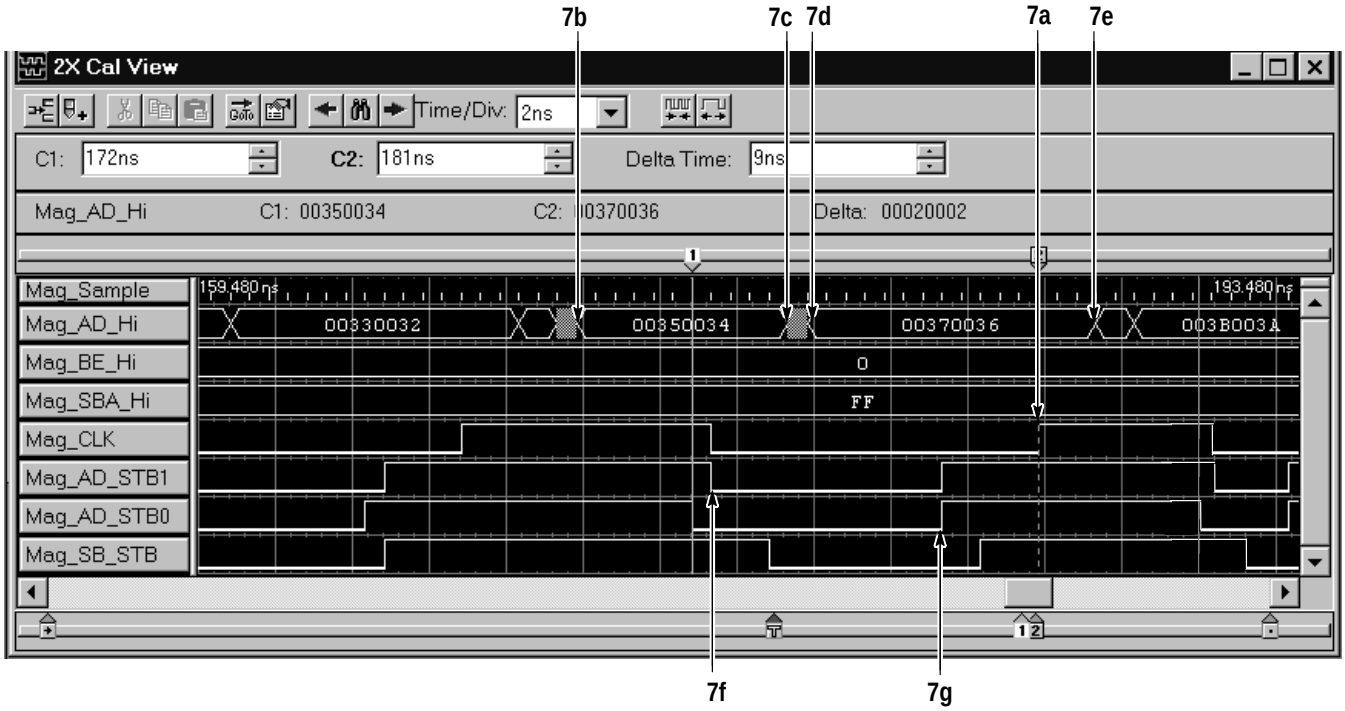


Figure 2–7: 2X Cal View Waveform window, MagniVu on

7. To calculate the setup time, refer to Figure 2–7 and follow these steps:

a. Position Cursor 2 on the rising edge of the CLK signal after both the AD_STB1 and AD_STB0 signals have been active and are asserted.

b. Move Cursor 1 to the previous change in the latest value of either the AD_Hi or the BE_Hi channel group before the falling edge of either AD_STB1 or AD_STB0. Figure 2–7 shows that the first measurement is taken from the AD_Hi channel group in this example.

Enter the Delta Time value in the second column of Table 2–7.

NOTE. *If there are no data transitions on the BE_Hi channel group, you can set the timing for the BE_Hi and BE_Lo channel groups to the same values as for the AD_Hi and AD_Lo channel groups.*

c. Move Cursor 1 to the next change in value of the AD_Hi channel group.

Enter the Delta Time value in the third column of the table.

NOTE. *If there is only one transition, also enter this value in the fourth column of the table.*

d. Move Cursor 1 to the next change in value of the AD_Hi channel group.

Enter the Delta Time value in the fourth column of the table.

e. If there are several transitions, as shown in Figure 2–7, move Cursor 1 to the next change in value of the AD_Hi channel group after the rising edge of either AD_STB1 or AD_STB0.

Enter the Delta Time value in the fifth column of the table.

f. Move Cursor 1 to the latest falling edge of either the AD_STB1 or AD_STB0 channel groups.

Enter the Delta Time value in the sixth column of the table.

g. Move Cursor 1 to the earliest rising edge of either the AD_STB1 or AD_STB0 channel groups.

Enter the Delta Time value in the seventh column of the table.

8. Position Cursor 2 on the next rising edge of the CLK signal after both the AD_STB1 and AD_STB0 signals have toggled.

Repeat steps 7b through 7g and enter the values in the second row.

9. Repeat step 8 twice and enter the values in the third and fourth rows.

10. You also need to take measurements with the logic analyzer triggered on any Write cycle in the Status channel group. Click the Trigger icon. The Trigger: AGP_2X dialog box appears. Change the RD to WR. Figure 2–8 shows the setup to trigger on any Write cycle.

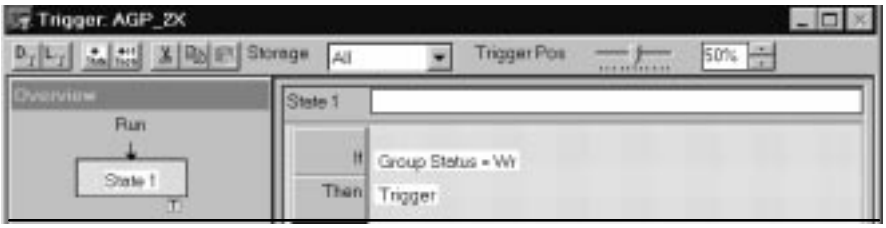


Figure 2–8: Trigger setup for any Write cycle in the Status channel group

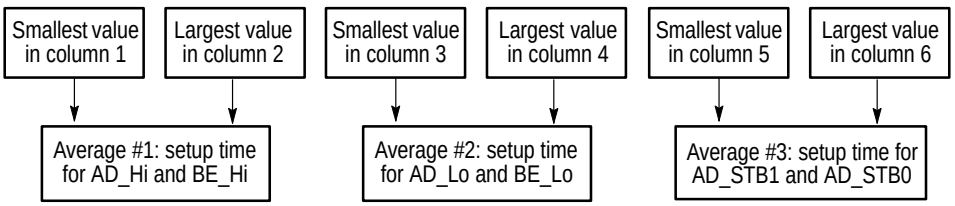
11. With the SUT running, click the RUN button to acquire data. After triggering, select the 2X Cal View Waveform window. Figure 2–7 shows acquired data.

12. Repeat steps 7 through 9 and enter the values in the fifth, sixth, seventh, and eight rows of Table 2–7.

13. Enter either the smallest or largest value of the measurements taken in each column as indicated in the two rows toward the end of the table.

14. Calculate the average value between each pair as shown in Figure 2–9.

Enter the averages in the last two rows of Table 2–7.



Note: Round each average down to the closest half nanosecond and add one nanosecond to that number. The results are the setup time values.

Figure 2–9: Averaging pairs of values for the 2X mode setup times

15. Round each average down to the closest half nanosecond and add one to that value.

16. To enter the setup time values from the Setup: AGP_2X dialog box, click the More button to the right of the Custom Clocking field. A Custom Options AGP_2X dialog box appears.

17. Enter the values that you calculated in the Setup Time column to the right of the AD_Hi, AD_Lo, BE_Hi, BE_Lo, AD_STB1, and AD_STB0 channel groups and click OK.

    Figure 2–10 shows the Custom Options AGP_2X dialog box and the Setup Time column. The values that you enter in this column will be different.

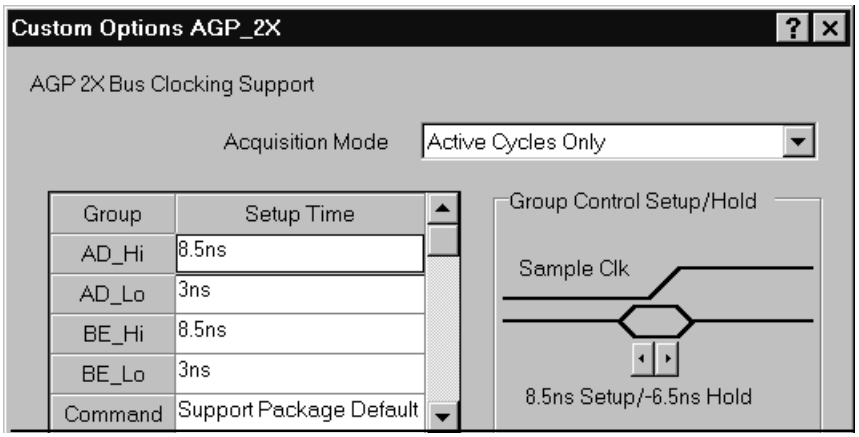


Figure 2–10: Custom Options AGP_2X dialog box

18. With the SUT running, click the RUN button to acquire data. After triggering, select the Listing window.

    Figure 2–18 on page 2–23 shows valid state data after aligning the edges.

19. To save the setup time values to restore at a later time, select Save System As ... from the File menu. As long as you do not change the SUT, you do not need to recalculate these values.

    If you want to save the setup only, make sure that the Save Acquired Data box is clear (no check).

Aligning for 2X_SBA Mode

To determine the proper time to sample AGP_2X SBA data, you need to check the timing relationship between the rising edge of the CLK signal and the SBA_Hi, SBA_Lo, and SB_STB channel groups.

In the MagniVu display, the SBA_Hi channel group contains double pumped data. You will take the following measurements to align the demultiplexed timing for the SBA_Hi, SBA_Lo and SB_STB groups.

You will use the cursors to take four sets of measurements. Before you start, photocopy Table 2–8 and fill it in as you take the measurements.

Table 2–8: Calculating the setup time offset of the logic analyzer for 2X_SBA mode

Value number	SBA_Hi	SBA_Hi		SBA_Hi	SB_STB	SB_STB
1						
2						
3						
4						
Smallest		Not used		Not used		Not used
Largest	Not used		Not used		Not used	
Averages	1.		2.		3.	

To align the setup time of the logic analyzer with the source-synchronous bus operating in 2X_SBA mode, refer to Figure 2–11 through Figure 2–13 and follow these steps:.

1. Perform the 2X Mode procedure. This takes about 15 minutes.
2. The logic analyzer must trigger on the SBE channel group. Click the Trigger icon. The Trigger: AGP_2X dialog box appears. Change the group from Status to SBE and the WR to SBE. Figure 2–11 shows the setup to trigger on any SBE cycle.

Figure 2–11: Trigger setup for any SBE cycle in the Status channel group

3. With the SUT running, click the RUN button to acquire data. After triggering, select the 2X Cal View Waveform window. Figure 2–12 shows the acquired data.

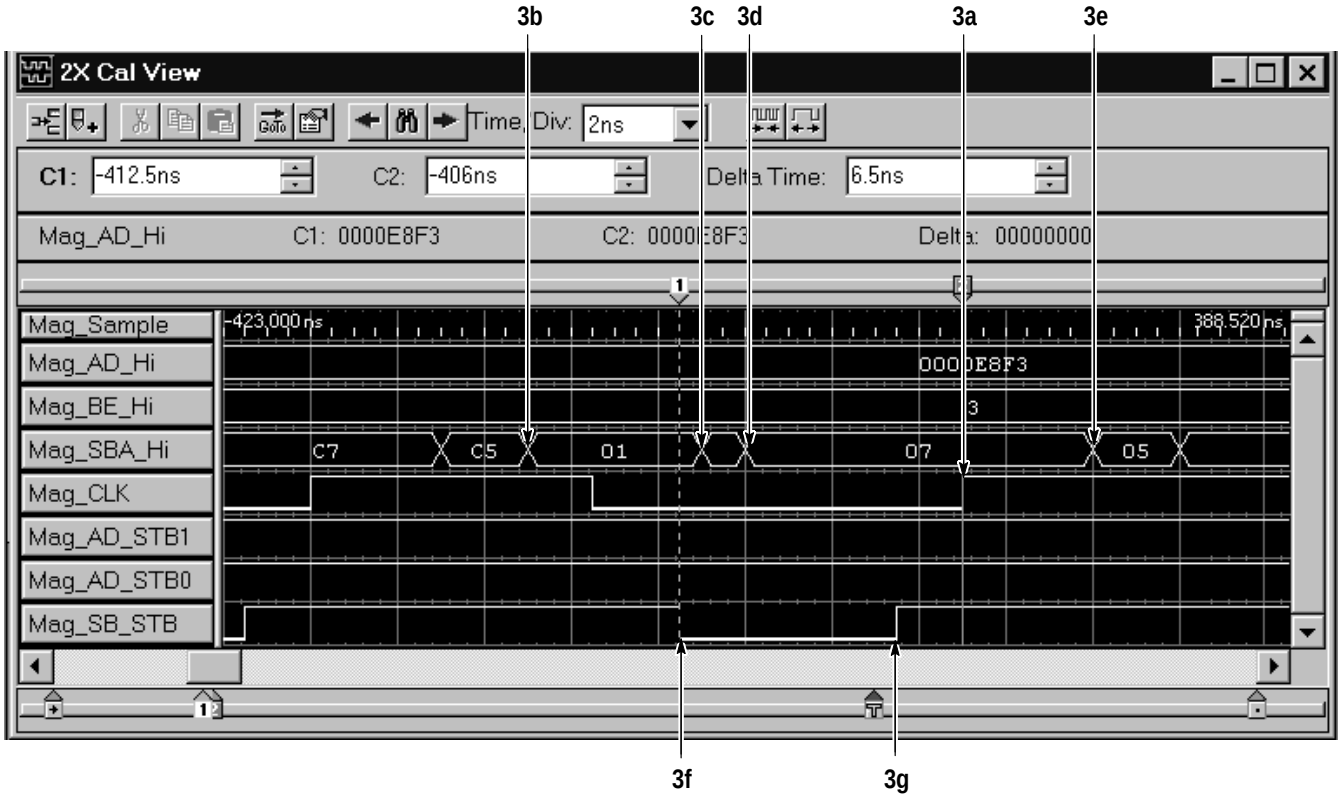


Figure 2–12: 2X Cal View display triggered on any SBE cycle, MagniVu on

To calculate the setup time, refer to Figure 2–12 and follow these steps:

a. Position Cursor 2 on the rising edge of the CLK signal after the SB_STB signal has been active.

b. Move Cursor 1 to the previous change in the latest value of the SBA_Hi channel group before the falling edge of SB_STB.

Enter the Delta Time value in the second column of Table 2–8.

c. Move Cursor 1 to the next change in value of the SBA_Hi group.

Enter the Delta Time value in the third column of the table.

NOTE. *If there is only one transition, also enter this value in the fourth column of the table.*

d. If there are multiple transitions, like in Figure 2–12, move Cursor 1 to the next change in value of the SBA_Hi channel group.

Enter the Delta Time value in the fourth column of the table.

e. Move Cursor 1 to the next change in value of the SBA_Hi channel group after the rising edge of SB_STB.

Enter the Delta Time value in the fourth column of the table.

f. Move Cursor 1 to the falling edge of the SB_STB channel group.

Enter the Delta Time value in the sixth column of the table.

g. Move Cursor 1 to the rising edge of the SB_STB channel group.

Enter the Delta Time value in the seventh column of the table.

4. Position Cursor 2 on the next rising edge of the CLK signal after the SB_STB signal has toggled.

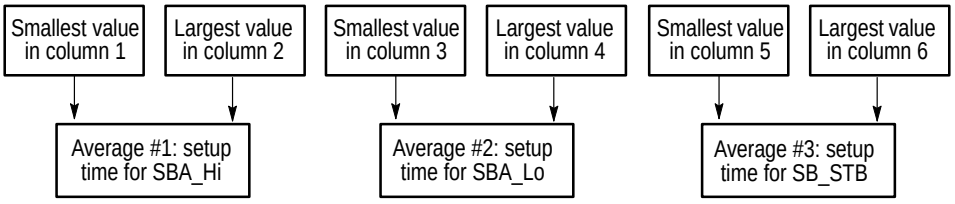
Repeat steps 3b through 3g and enter the values in the second row.

5. Repeat step 4 two more times and enter the values in the third and fourth rows of Table 2–8.

6. Enter either the smallest or largest value of the measurements taken in each column as indicated in the two rows toward the end of the table.

7. Calculate the average value between each pair as shown in Figure 2–13.

Enter the averages in the last row of Table 2–8.



Note: Round each average down to the closest half nanosecond and add one nanosecond to that number. The results are the setup time values.

Figure 2–13: Averaging pairs of values for the 2X_SBA mode setup times

8. Round each average down to the closest half nanosecond and add one to that value.

9. To enter the setup time values from the Setup: AGP_2X dialog box, click the More button to the right of the Custom Clocking field. A Custom Options AGP_2X dialog box appears.

10. Enter the values you calculated in the Setup Time column to the right of the SBA_Hi, SBA_Lo and SB_STB channel groups and click OK.

Figure 2–10 shows an example of the Custom Options AGP_2X dialog box and the Setup Time column. The selected signal names and values you enter in this column will be different.

11. With the SUT running, click the RUN button to acquire data. After triggering, select the Listing window.

Figure 2–20 on page 2–24 shows valid state data after aligning the edges.

12. To save the setup time values to restore at a later time, select Save System As ... from the File menu. As long as you do not change the SUT, you do not need to recalculate these values.

If you want to save the setup only, make sure that the Save Acquired Data box is clear (no check).

Acquiring and Viewing Data

This section describes how to acquire data and view it in a listing window with the following topics and tasks:

- Acquiring data
- Changing the way data is displayed
- AGP bus commands

Acquiring Data

Once you load the AGP setup, you can choose a clocking mode, specify the trigger, and acquire data. If the SUT is operating in 2X or 2X_SBA mode, you must first align the setup time of the logic analyzer with the source synchronous bus as described on page 2–6.

***NOTE**. If you do not align the setup time for the logic analyzer when using the AGP_2X setup, acquired data will be incorrect.*

If you have any problems acquiring data, refer to information on basic operations in your online help. If the solutions do not remedy the problem, then you might have a marginal Clock signal.

Compensating for a Marginal CLK Signal

If the SUT has a marginal CLK signal, you might not acquire correct data. To adjust the logic analyzer to compensate for a marginal CLK signal, refer to Figure 2–14 and follow these steps:

1. With MagniVu, acquire data and view the duty cycle of the CLK signal.
2. If the clock has a duty cycle well above 50%, try increasing the CLK signal threshold.

   If the clock has a duty cycle well below 50%, try decreasing the CLK signal threshold.

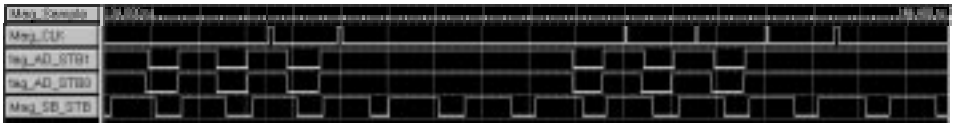


Figure 2–14: Marginal CLK signal, MagniVu on

3. To adjust the threshold, follow these steps:

   a. Go to the Setup window and click Set Thresholds to open the Probe Threshold dialog box.

   b. Select the CLK:3 signal and adjust as necessary. Click Close.

   Figure 2–15 shows the CLK signal after the threshold was increased to catch the clean rising edge of the signal above the plateau.

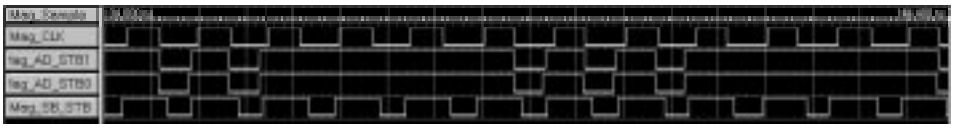


Figure 2–15: Adjusted threshold CLK signal, MagniVu on

4. If the CLK signal does not improve, use an oscilloscope to determine an optimal threshold. Look for a threshold level that has a good rising edge, not a plateau or wavy edge. Figure 2–16 shows a marginal CLK signal.

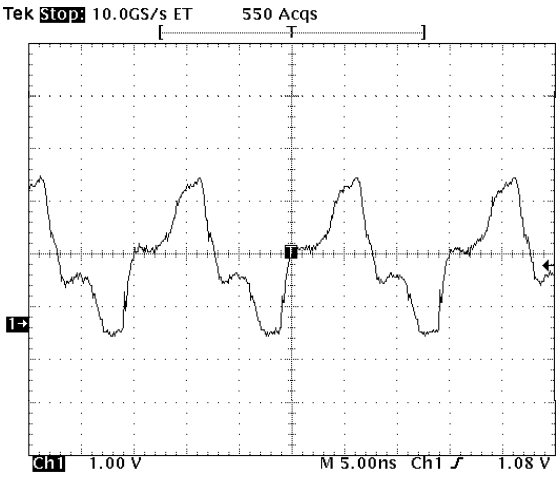


Figure 2–16: Marginal CLK signal on an oscilloscope

Using Low-Profile Extenders

When acquiring data using Low-Profile Extenders, you might need to adjust the threshold voltage for the increased capacitance loading of the probes.

If the SUT is operating in 2X_SBA mode, the data valid time for the SBA7 – SBA0 signals during the falling edge of the SB_STB signal is critical. The data valid time for SBA7 – SBA0 must be no less than 2.5 ns.

To compensate for the increased capacitive loading, you can increase the voltage thresholds for the E3:7-0 and E2:7-0 probe sections to 1.45 V. To do this, go to the Setup menu, access the Probe Threshold dialog box, and change the voltage threshold for the two probe sections.

After changing the probe voltage thresholds, you must align the setup time of the logic analyzer to the source synchronous bus. You need to perform both the 2X and 2X_SBA procedures, as described on page 2–6.

***NOTE**. If you do not align the setup time for the logic analyzer when using the AGP_2X setup, acquired data will be incorrect.*

Acquiring Only AGP or PCI Cycles

In some cases, you might need to acquire only AGP cycles or only PCI cycles. This can be done with storage qualification. You can use storage qualification to acquire data from your SUT operating in any mode (1X, 2X, PIPE, or SBA).

When you use storage qualification to ignore AGP or PCI cycles, you can still setup the logic analyzer to trigger on either cycle type. All trigger events are stored regardless of their cycle type.

AGP Cycles. To acquire only AGP cycles, follow these steps:

1. In the Trigger Setup window, select Conditional storage instead of All.
2. Change the Storage clause to the following settings:

```
If:   Group Control = AGP_Cycle
Or    Channel LOGIT_D# = Low
Then: Store Sample
```

PCI Cycles. To acquire only PCI cycles, follow these steps:

1. In the Trigger Setup window, select Conditional storage instead of All.

2. Change the Storage clause to the following settings:

```
If:   Group Control = PCI_Addr
Or    Group Control = PCI_Data
Or    Group Control = PCI_Abort
Or    Group Control = PCI_Discon
Then: Store Sample
```

Because storage qualification shares event recognizer resources with the rest of the trigger setup, you might not need to include the last one or two events in the Storage clause shown above.

After you acquire data, the Listing window will indicate a qualification gap with a grey line between samples. To make the gaps invisible, select the Listing Window tab in the Properties menu, clear the Show Qualifications Gaps (no check mark), and click OK.

NOTE. *In PCI Master Abort cycles, the data portion is acquired as an AGP cycle instead of as a PCI cycle. This occurs because the DEVSEL# or STOP# signal is not asserted during a PCI Master Abort cycle.*

Changing How Data is Displayed

There are common fields and features that allow you to further modify displayed data to suit your needs. There are no optional fields for this support package. Refer to the information on basic operations for descriptions of common fields.

Displaying Data

Data in the Listing window displays cycles based on each clocking option. This manual does not contain any examples of the Clock-By-Clock clocking option.

Figure 2–17 shows an example of displayed data using the AGP_1X setup with Active Cycles Only clocking when J100 is in the PIPE position and J200 is in the 1X position.

Sample	AD	BE	Command	Status	QI_Ctrl	Inc_QCnt	Dec_QCnt	Control	Timestamp
61200	0000E8FF	0011	PCI_I/O_Wr	-	Rd_LP	00	00	PCI_Addr	1.594,500 us
61201	00B20000	0111	-	-	Rd_LP	00	00	PCI_Data	30.000 ns
61202	E0100007	0000	AGP_Rd_LP	-	Rd_LP	01	01	AGP_Addr	481.000 ns
61203	E0140007	0100	AGP_Wr_LP	-	Wr_LP	01	01	AGP_Addr	105.500 ns
61204	E0180007	1000	AGP_Lg_Rd_LP	-	Rd_LP	02	02	AGP_Addr	105.000 ns
61205	E0180007	1000	-	Wr_LP	Rd_LP	02	00	Grant	30.500 ns
61206	00010000	0000	-	-	Rd_LP	02	02	IRDY	30.000 ns
61207	00030002	0000	-	-	Rd_LP	02	02	Request	15.000 ns
61208	00050004	0000	-	-	Rd_LP	02	02	TRDY	15.000 ns
61209	00070006	0000	-	-	Rd_LP	02	02	Request	15.000 ns
61210	00090008	0000	-	-	Rd_LP	02	02	Request	15.000 ns
61211	000B000A	0000	-	-	Rd_LP	02	02	Request	15.000 ns
61212	000D000C	0000	-	-	Rd_LP	02	02	TRDY	15.000 ns
61213	000F000E	0000	-	-	Rd_LP	02	02	Request	15.000 ns
61214	00110010	0000	-	-	Rd_LP	02	02	Request	15.000 ns
61215	00130012	0000	-	-	Rd_LP	02	02	Request	15.000 ns
61216	00150014	0000	-	-	Rd_LP	02	02	TRDY	15.500 ns
61217	00170016	0000	-	-	Rd_LP	02	02	Request	14.500 ns
61218	00190018	0000	-	-	Rd_LP	02	02	Request	15.500 ns
61219	001B001A	0000	-	-	Rd_LP	02	02	Request	15.000 ns
61220	001D001C	0000	-	-	Rd_LP	02	02	Request	15.000 ns
61221	001F001E	0000	-	~	Rd_LP	02	00	Grant	15.000 ns
61222	E01C0007	0001	AGP_Rd_HP	-	Rd_HP	01	02	AGP_Addr	30.000 ns
61223	E01C0007	0001	-	Rd_LP	Rd_LP	01	01	Grant	30.000 ns
61224	00010000	0000	-	-	Rd_LP	01	01	TRDY	15.500 ns
61225	00030002	0000	-	-	Rd_LP	01	01	Request	15.000 ns
61226	00050004	0000	-	-	Rd_LP	01	01	IRDY-TRDY	15.000 ns
61227	00070006	0000	-	-	Rd_LP	01	01	IRDY	15.000 ns
61228	00090008	0000	-	-	Rd_LP	01	01	Request	14.500 ns

Figure 2–17: AGP_1X PIPE mode

Figure 2–18 shows an example of displayed data using the AGP_2X setup with Active Cycles Only clocking when J100 is in the PIPE position and J200 is in the 2X position.

Sample	AD_Hi	AD_Lo	BE_Hi	BE_Lo	Command	Status	QI_Ctrl	Inc_QC	Dec_QC	Control	Timestamp
262131	00010058	00010058	1010	1010	PCI_Config_Rd	-	Rd_LP	00	00	PCI_Addr	2.737,500 us
262132	01800180	01800180	1100	1100	-	-	Rd_LP	00	00	PCI_Data	90.000 ns
262133	00010018	00010018	1010	1010	PCI_Config_Rd	-	Rd_LP	00	00	PCI_Addr	3.429,000 us
262134	0000E801	0000E801	0000	0000	-	-	Rd_LP	00	00	PCI_Data	90.500 ns
262135	0000E8FF	0000E8FF	0011	0011	PCI_I/O_Wr	-	Rd_LP	00	00	PCI_Addr	1.594,000 us
262136	00B20000	00B20000	0111	0111	-	-	Rd_LP	00	00	PCI_Data	30.000 ns
262137	E0100000	E0100000	0000	0000	AGP_Rd_LP	-	Rd_LP	01	01	AGP_Addr	481.500 ns
262138	E0100008	E0100008	0000	0000	AGP_Rd_LP	-	Rd_LP	02	02	AGP_Addr	105.500 ns
262139	E0100010	E0100010	0000	0000	AGP_Rd_LP	-	Rd_LP	03	03	AGP_Addr	105.000 ns
262140	E0100018	E0100018	0000	0000	AGP_Rd_LP	-	Rd_LP	04	04	AGP_Addr	105.500 ns
262141	E0100020	E0100020	0000	0000	AGP_Rd_LP	-	Rd_LP	05	05	AGP_Addr	105.500 ns
262142	E0100028	E0100028	0000	0000	AGP_Rd_LP	-	Rd_LP	06	06	AGP_Addr	105.000 ns
262143	E0100028	E0100028	0000	0000	-	Rd_LP	Rd_LP	05	05	Grant	30.000 ns
262144	00010000	00030002	0000	0000	-	Rd_LP	Rd_LP	04	04	TRDY	15.000 ns
262145	00050004	00070006	0000	0000	-	Rd_LP	Rd_LP	03	03	TRDY	15.000 ns
262146	00090008	000B000A	0000	0000	-	Rd_LP	Rd_LP	02	02	TRDY	15.000 ns
262147	000D000C	000F000E	0000	0000	-	~	Rd_LP	02	00	TRDY	15.000 ns
262148	E0100030	E0100030	0000	0000	AGP_Rd_LP	-	Rd_LP	03	03	AGP_Addr	30.500 ns
262149	E0100030	E0100030	0000	0000	-	Rd_LP	Rd_LP	02	02	Grant	30.000 ns
262150	00110010	00130012	0000	0000	-	~	Rd_LP	02	00	TRDY	15.000 ns
262151	E0100038	E0100038	0000	0000	AGP_Rd_LP	-	Rd_LP	03	03	AGP_Addr	30.000 ns

Figure 2–18: AGP_2X PIPE mode

Figure 2–19 shows an example of displayed data using the AGP_1X setup with Active Cycles Only clocking when J100 is in the SBA position and J200 is in the 1X position.

Sample	AD	BE	Command	Status	SBA	SBE	QI_Ctrl	Inc_QCnt	Dec_QCnt	Control	Timestamp
262122	01800180	1100	-	-	FF	-	Rd_LP	00	00	PCI_Data	90.000 ns
262123	00010018	1010	PCI_Config_Rd	-	FF	-	Rd_LP	00	00	PCI_Addr	3.339,500 us
262124	0000E801	0000	-	-	FF	-	Rd_LP	00	00	PCI_Data	90.000 ns
262125	0000E8FF	0011	PCI_I/O_Wr	-	FF	-	Rd_LP	00	00	PCI_Addr	1.759,500 us
262126	00B20000	0111	-	-	FF	-	Rd_LP	00	00	PCI_Data	30.000 ns
262127	0000E8F3	0011	-	-	C0	T-3	Rd_LP	00	00	-	436.500 ns
262128	0000E8F3	0011	-	-	E0	-	Rd_LP	00	00	-	15.000 ns
262129	0000E8F3	0011	-	-	84	T-2	Rd_HP	00	00	-	15.000 ns
262130	0000E8F3	0011	-	-	10	-	Rd_HP	00	00	-	15.000 ns
262131	0000E8F3	0011	-	-	00	T-1	Rd_HP	01	00	-	15.000 ns
262132	0000E8F3	0011	-	-	00	-	Rd_HP	01	00	-	15.000 ns
262133	0000E8F3	0011	-	-	94	T-2	Wr_HP	00	00	-	15.000 ns
262134	0000E8F3	0011	-	-	20	-	Wr_HP	00	00	-	15.000 ns
262135	0000E8F3	0011	-	-	00	T-1	Wr_HP	01	00	-	15.500 ns
262136	0000E8F3	0011	-	-	00	-	Wr_HP	01	00	-	15.000 ns
262137	0000E8F3	0011	-	-	84	T-2	Rd_HP	01	00	-	15.000 ns
262138	0000E8F3	0011	-	-	10	-	Rd_HP	01	00	-	15.000 ns
262139	0000E8F3	0011	-	-	00	T-1	Rd_HP	02	00	-	15.000 ns
262140	0000E8F3	0011	-	-	08	-	Rd_HP	02	00	-	15.000 ns
262141	0000E8F3	0011	-	-	94	T-2	Wr_HP	01	00	-	15.000 ns
262142	0000E8F3	0011	-	-	20	-	Wr_HP	01	00	-	15.000 ns
262143	0000E8F3	0011	-	Wr_HP	00	T-1	Wr_HP	01	01	Grant	15.500 ns
262144	0000E8F3	0011	-	-	08	-	Wr_HP	01	00	-	14.500 ns
262145	00010000	0000	-	-	84	T-2	Rd_HP	02	00	IRDY	15.000 ns
262146	00030002	0001	-	-	10	-	Rd_HP	02	00	-	15.000 ns
262147	00030002	0001	-	-	00	T-1	Rd_HP	03	00	-	15.500 ns
262148	00030002	0001	-	-	10	-	Rd_HP	03	00	-	15.000 ns

Figure 2–19: AGP_1X SBA mode

Figure 2–20 shows an example of displayed data using the AGP_2X setup with Active Cycles Only clocking when J100 is in the SBA position and J200 is in the 2X position.

Sample	AD_Hi	AD_Lo	BE_Hi	BE_Lo	Status	SBA_Hi	SBA_Lo	SBE	QI_Ctrl	Inc	Dec	Control	Timestamp
262140	0000E8F3	0000E8F3	0011	0011	-	00	E8	T-1	Rd_LP	DB	DB	-	15.000 ns
262141	0000E8F3	0000E8F3	0011	0011	-	00	F0	T-1	Rd_LP	DC	DC	-	15.500 ns
262142	0000E8F3	0000E8F3	0011	0011	-	00	F8	T-1	Rd_LP	DD	DD	-	15.000 ns
262143	0000E8F3	0000E8F3	0011	0011	Rd_LP	FF	FF	-	Rd_LP	DC	DC	Grant	30.000 ns
262144	00010000	00030002	0000	0000	Rd_LP	FF	FF	-	Rd_LP	DB	DB	TRDY	15.000 ns
262145	00050004	00070006	0000	0000	-	FF	FF	-	Rd_LP	DB	DB	TRDY	15.000 ns
262146	0000E8F3	0000E8F3	0011	0011	Rd_LP	FF	FF	-	Rd_LP	DA	DA	Grant	45.000 ns
262147	00090008	000B000A	0000	0000	Rd_LP	FF	FF	-	Rd_LP	D9	D9	TRDY	15.000 ns
262148	000D000C	000F000E	0000	0000	Rd_LP	FF	FF	-	Rd_LP	D8	D8	TRDY	15.000 ns
262149	00110010	00130012	0000	0000	-	FF	FF	-	Rd_LP	D8	D8	TRDY	15.500 ns
262150	00130016	00130016	0000	0000	-	01	00	T-1	Rd_LP	D9	D9	-	15.000 ns

Figure 2–20: AGP_2X SBA mode

AGP Bus Commands

Complete AGP bus requests follow a specific format.

PIPE Mode

Figure 2–21 shows the format of complete bus requests in PIPE mode.

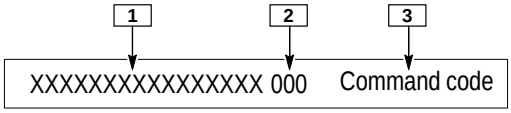


Figure 2–21: Format of a complete AGP bus request in PIPE mode

1 **AGP Bus Address Field.** The 29-bit Address field.

2 **AGP Bus Length Field.** Contains the access length in units of Q-words (8 bytes) and displaces the lower order 3 bits of address. A value of 000 means that a single Q-word (8 bytes) of data is requested. A value of 111 means that 8 Q-words are requested.

For a Long Read cycle, a value of 000 means that four Q-words are requested. A value of 111 means that 32 Q-words are requested.

3 **AGP Command Code Field.** The 4-bit bus used to identify the bus operation or command.

Refer to the *Accelerated Graphics Port Interface Specifications* for complete information on access ordering, Read and Write flow control, and bus transactions. The descriptions are too extensive to list in this manual.

SBA Mode

Table 2–9 shows the format of complete bus requests in SBA mode.

Table 2–9: Format of a complete AGP bus request in SBA mode

Encoding	Description
S7 S6 S5 S4 S3 S2 S1 S0	Shows the alignment of messages on the physical sideband wires.
1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	The Bus Idle encoding indicates that the bus is idle and is also referred to as No OPeration (NOP). When the SUT is running the 1X transfer mode, this command is limited to a single clock tick of eight bits (all ones) while the 2X transfer mode requires the full sixteen bits, as shown.
0 A A A A A A A 14 08 A A A A A L L L 07 03	The Length and Lower Address Bits encoding transfers the AGP access length field (LLL) and lower 12 address bits (A14 – A3) across the sideband address port, and a memory access is initiated. This is a Type 1 sideband command. The remainder of the AGP access request (A31 – A15) and bus command is defined by what was last transmitted using the other two sideband address port commands (Type 2 and Type 3). Note that A2 – A0 are assumed to be zero when using this encoding and these bits are not transferred.

Table 2–9: Format of a complete AGP bus request in SBA mode (cont.)

Encoding	Description
1 0 C C C C – A 15 A A A A A A A A 23 16	The Command and Mid Address Bits encoding transfers the AGP bus command (CCCC) and mid-order 9 address bits (A23 – A15) across the sideband address port; no memory access is initiated. This is a Type 2 sideband command. When followed by the previous command (Type 1), this command provides for memory access anywhere within a naturally aligned 16 MB "page."
1 1 0 – A A A A 35 32 A A A A A A A A 31 24	The Upper Address Bits encoding transfers the upper 12 address bits (A35 – A24) across the sideband address port; no memory access is initiated. This is a Type 3 sideband command. When followed by the two previous commands (Type 2 and Type 1), this command provides access anywhere within a 32-bit physical address space. The extra four bits (A35 – A32) are place holders to avoid aliasing problems in the face of possible address expansion.
1 1 1 0 A A A A 39 36 A A A A A A A A 47 40	The Extended Address Bits encoding transfers the extended 12 address bits (A47 – A36) across the sideband address port; no memory access is initiated. This is a Type 4 sideband command. When followed by the three previous commands (Type 3, Type 2 and Type 1), this command provides for memory access anywhere within a 48–bit physical address space.
1 1 1 1 0 * * * * * * * * * * *	This is Reserved encoding and must not be issued by an AGP compliant master. Intel might define this in the future.

AGP Bus Transactions

Figure 2–22 shows the basic state diagram for an AGP bus transaction.

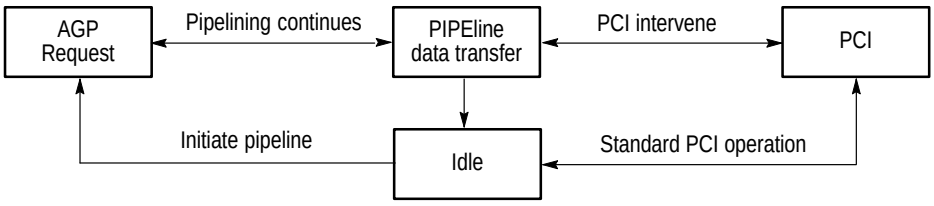


Figure 2–22: Basic state diagram for an AGP bus transaction

Specifications

Specifications

This chapter contains the following information:

- Probe adapter description
- Specification tables
- Loading and equivalent circuits
- Channel assignment tables
- Description of how the module acquires AGP bus signals

Probe Adapter Description

The probe adapter is nonintrusive hardware that allows the logic analyzer to acquire data from a bus in its own operating environment with little effect, if any, on the target system. Information on basic operations contains a figure showing the logic analyzer connected to a typical probe adapter. Refer to that figure while reading the following description.

The probe adapter consists of a circuit board and a socket for an Accelerated Graphics Port bus module. The probe adapter plugs into the bus at the AGP connector. Signals from the bus flow from the probe adapter to the P6434 probes and through the probe cables to the logic analyzer.

The probe adapter accommodates the Accelerated Graphics Port bus. All circuitry on the probe adapter is powered from the SUT.

Specifications

These specifications are for a probe adapter connected between a compatible Tektronix logic analyzer and a SUT. Table 3–1 shows the electrical requirements the SUT must produce for the support to acquire correct data.

In Table 3–1, one podlet load is 20 kΩ in parallel with 2 pF.

Table 3–1: Electrical specifications

Characteristics	Requirements
SUT DC power requirements	
5 V Vcc Voltage	4.75–5.25 VDC
5 V Vcc Current	I max (calculated) 300 mA

Table 3–1: Electrical specifications (cont.)

Characteristics	Requirements	
3.3 V Vcc Voltage	3.20–3.40 VDC	
3.3 V Vcc Current	I max (calculated) 100 mA	
SUT clock rate	Max. 66 MHz	
Minimum setup time required 2X mode only, SBA7 – SBA0 signals relative to the falling edge of SB_STB	1 ns	
Minimum hold time required 2X mode only, SBA7 – SBA0 signals relative to the falling edge of SB_STB	1.3 ns	
All 1X mode and remaining 2X mode signals	Must meet timing requirements as shown in the *Accelerated Graphics Port Interface Specification*, section 4	
	Specification	
Measured typical SUT signal loading	**AC load**	**DC load**
FRAME#, PIPE#, ST2-ST0, GNT#, IRDY#, TRDY#, C/B3#-C/B0#	4 pF + 1 podlet	74LVT + 1 podlet
SBA7-SBA4, SBA2	8 pF + 1 podlet	74LVT + 1 podlet
CLK	12 pF + 1 podlet	74LVT + 1 podlet
Remaining signals	1 podlet	1 podlet

Note; *All Reserved pins are connected through the probe adapter. All VCC3.3 pins are shorted together on the probe adapter. All Vddq3.3 pins are shorted together on the probe adapter. All 5.0 V pins are shorted together on the probe adapter.*

Table 3–2 shows the environmental specifications.

Table 3–2: Environmental specifications*

Characteristic	Description
Temperature	
Maximum operating	+50° C (+122° F)†
Minimum operating	0° C (+32° F)
Non-operating	–55° C to +75° C (–67° to +167° F)
Humidity	10 to 95% relative humidity
Altitude	
Operating	4.5 km (15,000 ft) maximum
Non-operating	15 km (50,000 ft) maximum

Table 3–2: Environmental specifications* (cont.)

Characteristic	Description
Electrostatic immunity	The probe adapter is static sensitive

***** **Designed to meet Tektronix standard 062-2847-00 class 5.**

† **Not to exceed Accelerated Graphics Port bus thermal considerations. Forced air cooling might be required.**

Table 3–3 shows the compliances that apply to the probe adapter.

Table 3–3: Certifications and compliances

EC Compliance	There are no current European Directives that apply to this product.

Figure 3–1 shows the dimensions of the probe adapter.

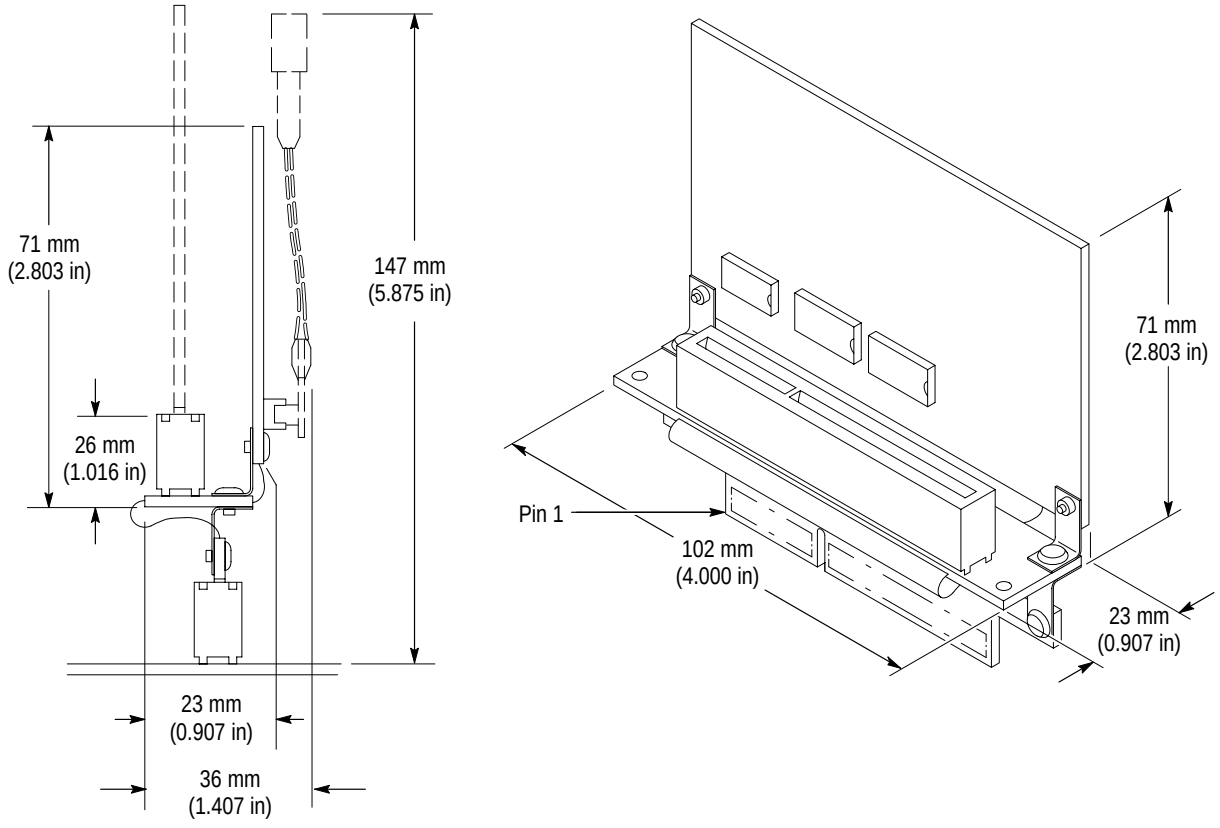


Figure 3–1: Dimensions of the probe adapter

Loading and Equivalent Circuits

The load presented to the SUT by the AGP probe adapter is low. The load is equivalent to a 2 pF capacitance with 20 kΩ resistance returned to a 2.2 V supply. The following approximation of the probe adapter loading is sufficient for most circuit-simulation calculations.

Figure 3–2 shows the load on buffered signals with three 74LVT integrated circuits.

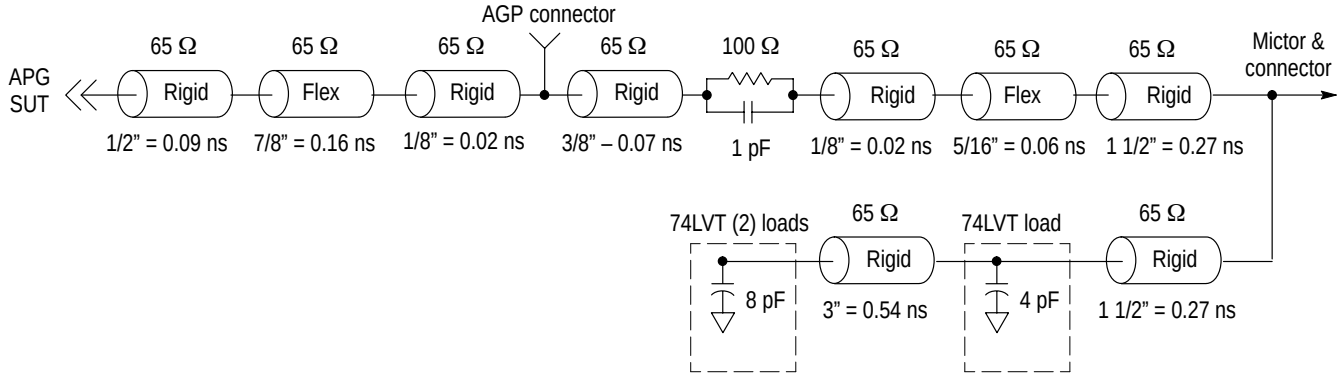


Figure 3–2: Clocking and buffered signals with three 74LVT loads

Figure 3–3 shows the load on buffered signals with two 74LVT integrated circuits.

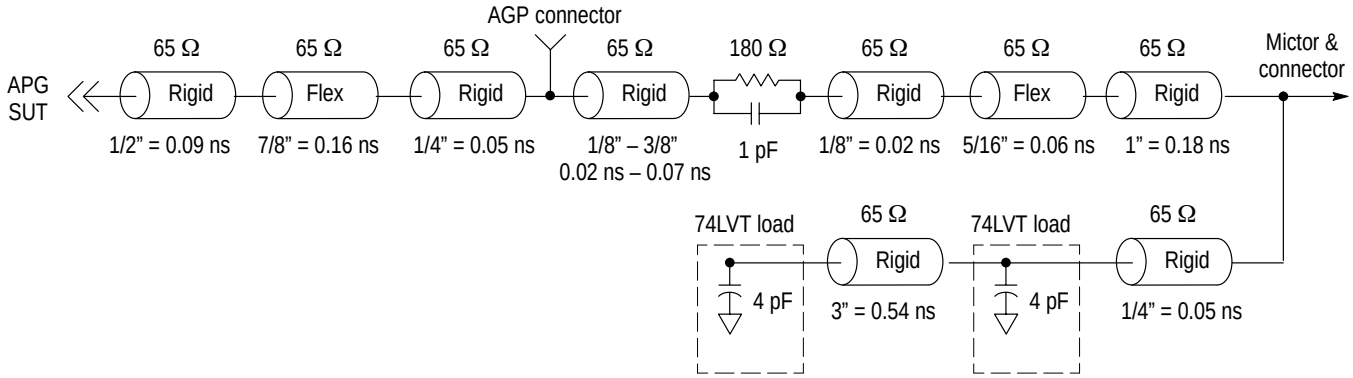


Figure 3–3: Buffered signals with two 74LVT loads

Figure 3–4 shows the load on buffered signals with one 74LVT integrated circuit.

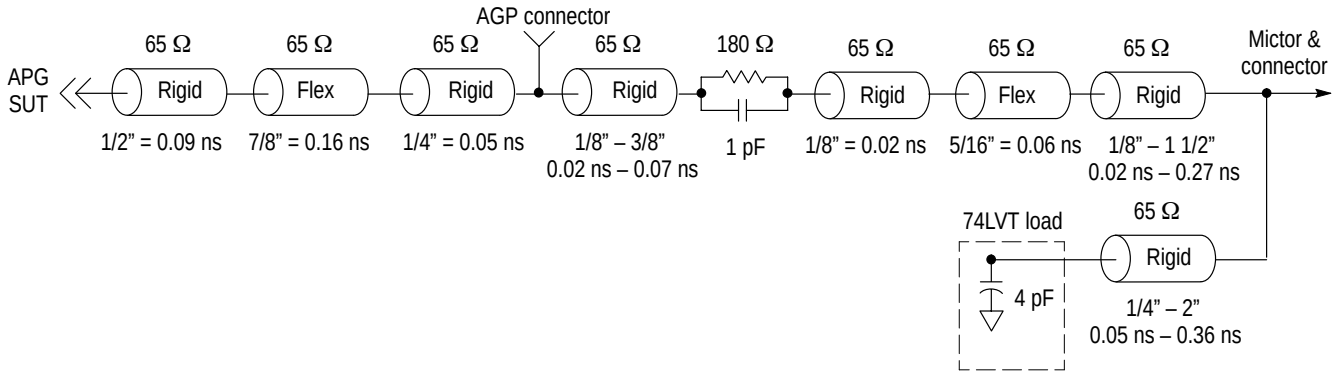


Figure 3–4: Buffered signals with one 74LVT load

Figure 3–5 shows the load on all signals that are not buffered or latched.

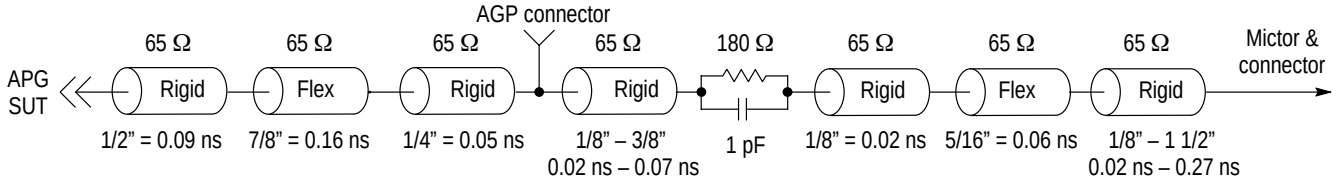


Figure 3–5: Nonlatched signals (all other signals)

The load presented to the Mictor connector by the P6434 probe is low. The load is equivalent to a 2 pF capacitance with 20 kΩ resistance returned to a 2.2 V supply. The following approximation of the probe loading is sufficient for most circuit-simulation calculations.

Figure 3–6 shows the equivalent circuit of the P6434 probe. Table 3–4 shows the values you can use to calculate characteristics of the Lossy delay lines shown in the next two figures.

Table 3–4: Lossy delay line values

Characteristic	Value
C (capacitance)	1.58 pF per inch
L (inductance)	8.9 nH per inch
R (resistance)	.067 Ω per inch
Z_0 (impedance)	75 Ω

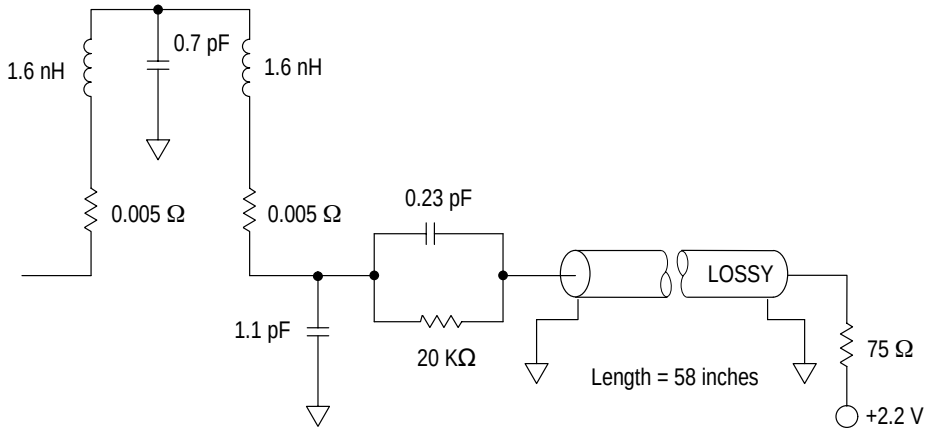


Figure 3–6: Equivalent circuit for the P6434 probe

The Low-Profile Extender used with the P6434 probe increases the load. The additional load is equivalent to a 100 Ω resistor connected in series with approximately three inches of 75 Ω coaxial cable to the probe tip.

Although the extender can increase the loading, using the extender might be necessary in situations where there is as little as half an inch of clearance.

The extender is useful in a SUT where signal risetimes are greater than one or two nanoseconds. Faster risetimes cause transmission line reflections on signals.

Figure 3–7 shows the equivalent circuit for the P6434 probe with a Low-Profile Extender.

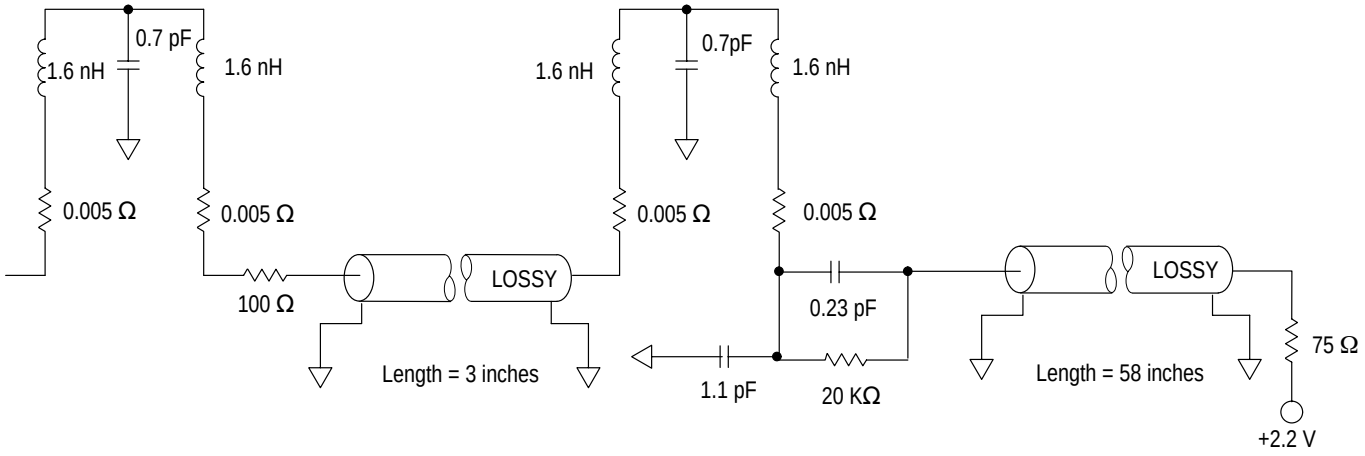


Figure 3–7: Equivalent circuit for the P6434 probe with a Low-Profile Extender

Channel Assignments

Channel assignments shown in Table 3–5 through Table 3–32 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are shown starting with the most significant bit (MSB) descending to the least significant bit (LSB).
- An _D following a signal name indicates that the signal is derived.
- A pound sign (#) following a signal name indicates an active low signal.
- For the AGP_2X setup, an _M following a signal name indicates that the signal is demultiplexed.

AGP_1X Setup. Tables 3–5 through 3–15 show the channel assignments for the AGP_1X setup used to acquire data for general purpose analysis with Custom, External, or Internal clocking.

Table 3–5 shows the probe section and channel assignments for the AD group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–5: AGP_1X: AD group channel assignments

Bit order	Section:channel	Accelerated Graphics Port signal name
31	A3:7	AD31
30	A3:6	AD30
29	A3:5	AD29
28	A3:4	AD28
27	A3:3	AD27
26	A3:2	AD26
25	A3:1	AD25
24	A3:0	AD24
23	A2:7	AD23
22	A2:6	AD22
21	A2:5	AD21
20	A2:4	AD20
19	A2:3	AD19
18	A2:2	AD18
17	A2:1	AD17
16	A2:0	AD16

Table 3–5: AGP_1X: AD group channel assignments (cont.)

Bit order	Section:channel	Accelerated Graphics Port signal name
15	A1:7	AD15
14	A1:6	AD14
13	A1:5	AD13
12	A1:4	AD12
11	A1:3	AD11
10	A1:2	AD10
9	A1:1	AD9
8	A1:0	AD8
7	A0:7	AD7
6	A0:6	AD6
5	A0:5	AD5
4	A0:4	AD4
3	A0:3	AD3
2	A0:2	AD2
1	A0:1	AD1
0	A0:0	AD0

***NOTE**. The AGP_1X setup does not require a P6434 probe for the D3:7 – 0, D2:7 – 0, D1:7 – 0, D0:7 – 0, CK:2 or QUAL:0 channels.*

Table 3–6 shows the probe section and channel assignments for the BE group and the bus signal to which each channel connects. By default, this channel group is displayed in binary.

Table 3–6: AGP_1X: BE group channel assignments

Bit order	Section:channel	Accelerated Graphics Port signal name
3	C3:5	C/BE3#
2	C3:1	C/BE2#
1	C3:0	C/BE1#
0	C3:4	C/BE0#

Table 3–7 shows the probe section and channel assignments for the Command group and the bus signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–7: AGP_1X: Command group channel assignments

Bit order	Section:channel	Accelerated Graphics Port signal name
6	C2:6	IRDY#
5	E3:1	FRAME#
4	C3:2	PIPE#
3	C3:5	C/BE3#
2	C3:1	C/BE2#
1	C3:0	C/BE1#
0	C3:4	C/BE0#

Table 3–8 shows the probe section and channel assignments for the Status group and the bus signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–8: AGP_1X: Status group channel assignments

Bit order	Section:channel	Accelerated Graphics Port signal name
3	C2:4	GNT#
2	C3:7	ST2
1	C3:3	ST1
0	C2:7	ST0

Table 3–9 shows the probe section and channel assignments for the SBE (Side Band Enable) group and the bus signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–9: AGP_1X: SBE group channel assignments

Bit order	Section:channel	Accelerated Graphics Port signal name
4	C1:7	SBE_D#
3	E2:7	SBA7
2	E2:6	SBA6
1	E2:5	SBA5
0	E2:4	SBA4

Table 3–10 shows the probe section and channel assignments for the SBA (Side Band Address) group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–10: AGP_1X: SBA group channel assignments

Bit order	Section:channel	Accelerated Graphics Port signal name
7	E2:7	SBA7
6	E2:6	SBA6
5	E2:5	SBA5
4	E2:4	SBA4
3	E2:3	SBA3
2	E2:2	SBA2
1	E2:1	SBA1
0	E2:0	SBA0

Table 3–11 shows the probe section and channel assignments for the QI_Ctrl group and the bus signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–11: AGP_1X: QI_Ctrl group channel assignments

Bit order	Section:channel	Accelerated Graphics Port signal name
2	C1:6	VAL_ID#*
1	C1:3	QICNT_ID1*
0	C1:2	QICNT_ID0*

*** Signal not required by the Clocking State Machine.**

Table 3–12 shows the probe section and channel assignments for the Inc_QCnt group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–12: AGP_1X: Inc_QCnt group channels

Bit order	Section:channel	Accelerated Graphics Port signal name
7	C0:7	QICNT7*
6	C0:6	QICNT6*
5	C0:5	QICNT5*
4	C0:4	QICNT4*
3	C0:3	QICNT3*
2	C0:2	QICNT2*
1	C0:1	QICNT1*
0	C0:0	QICNT0*

*** Signal not required by the Clocking State Machine.**

Table 3–13 shows the probe section and channel assignments for the Dec_QCnt group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–13: AGP_1X: Dec_QCnt group channels

Bit order	Section:channel	Accelerated Graphics Port signal name
7	E1:7	QDCNT7*
6	E1:6	QDCNT6*
5	E1:5	QDCNT5*
4	E1:4	QDCNT4*
3	E1:3	QDCNT3*
2	E1:2	QDCNT2*
1	E1:1	QDCNT1*
0	E1:0	QDCNT0*

*** Signal not required by the Clocking State Machine.**

Table 3–14 shows the probe section and channel assignment for the Control group and the bus signal to which the channel connects. By default, this channel group is displayed symbolically.

Table 3–14: AGP_1X: Control group channel assignments

Bit order	Section:channel	Accelerated Graphics Port signal name
13	QUAL:1	RST#
12	E3:7	PME#*
11	E3:0	RBF#*
10	E3:2	SERR#*
9	E3:6	PERR#*
8	E3:3	PAR*
7	C3:6	REQ#*
6	C2:4	GNT#
5	C3:2	PIPE#
4	E3:1	FRAME#
3	C2:6	IRDY#
2	C2:5	TRDY#
1	E3:4	DEVSEL#*
0	QUAL:3	STOP#

*** Signal not required by the Clocking State Machine.**

Table 3–15 shows the probe section and channel assignments for the Misc group and the bus signal to which each channel connects. By default, this channel group is not visible.

Table 3–15: AGP_1X: Misc group channel assignments

Bit order	Section:channel	Accelerated Graphics Port signal name
5	CLK:3	CLK
4	C2:0	LOGIT_D#
3	C2:3	FRAME_D#
2	QUAL:2	PIPE_D#
1	C2:2	IRDY_D#
0	C2:1	TRDY_D#

AGP_2X Setup. Tables 3–16 through 3–32 show the channel assignments for the AGP_2X setup used for general purpose analysis with Custom, External, or Internal clocking.

Table 3–16 shows the probe section and channel assignments for the AD_Hi group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

NOTE*. The AD31 – AD0 signals are demultiplexed from the A group to the D group. The AD_Hi channel group contains the first 32 bits of data and the AD_Lo channel group contains the second 32 bits of data (from AD31 – AD0). Because the AD31 – AD0 signals are double pumped, the AD_Hi group contains the AD31 – AD0 signals.*

Table 3–16: AGP_2X: AD_Hi group channel assignments

Bit order	Section:channel	Accelerated Graphics Port signal name
31	A3:7	AD31
30	A3:6	AD30
29	A3:5	AD29
28	A3:4	AD28
27	A3:3	AD27
26	A3:2	AD26
25	A3:1	AD25
24	A3:0	AD24

Table 3–16: AGP_2X: AD_Hi group channel assignments (cont.)

Bit order	Section:channel	Accelerated Graphics Port signal name
23	A2:7	AD23
22	A2:6	AD22
21	A2:5	AD21
20	A2:4	AD20
19	A2:3	AD19
18	A2:2	AD18
17	A2:1	AD17
16	A2:0	AD16
15	A1:7	AD15
14	A1:6	AD14
13	A1:5	AD13
12	A1:4	AD12
11	A1:3	AD11
10	A1:2	AD10
9	A1:1	AD9
8	A1:0	AD8
7	A0:7	AD7
6	A0:6	AD6
5	A0:5	AD5
4	A0:4	AD4
3	A0:3	AD3
2	A0:2	AD2
1	A0:1	AD1
0	A0:0	AD0

Table 3–17 shows the probe section and channel assignments for the AD_Lo group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

NOTE. *The AD_Lo channel group is the demultiplex target for the second group of 32 bits of data on the AD31 – AD0 signals and contains the AD31_M – AD0_M signals.*

Because the D3:7 – 0, D2:7 – 0, D1:7 – 0 and D0:7 – 0 probe sections are in use, they are NOT extra channels, even though probes are not connected to them.

Table 3–17: AGP_2X: AD_Lo group channel assignments

Bit order	Section:channel	Accelerated Graphics Port signal name
31	D3:7	AD31_M
30	D3:6	AD30_M
29	D3:5	AD29_M
28	D3:4	AD28_M
27	D3:3	AD27_M
26	D3:2	AD26_M
25	D3:1	AD25_M
24	D3:0	AD24_M
23	D2:7	AD23_M
22	D2:6	AD22_M
21	D2:5	AD21_M
20	D2:4	AD20_M
19	D2:3	AD19_M
18	D2:2	AD18_M
17	D2:1	AD17_M
16	D2:0	AD16_M
15	D1:7	AD15_M
14	D1:6	AD14_M
13	D1:5	AD13_M
12	D1:4	AD12_M
11	D1:3	AD11_M
10	D1:2	AD10_M
9	D1:1	AD9_M
8	D1:0	AD8_M
7	D0:7	AD7_M
6	D0:6	AD6_M
5	D0:5	AD5_M
4	D0:4	AD4_M
3	D0:3	AD3_M
2	D0:2	AD2_M
1	D0:1	AD1_M
0	D0:0	AD0_M

Table 3–18 shows the probe section and channel assignments for the BE_Hi group and the bus signal to which each channel connects. By default, this channel group is displayed in binary.

NOTE. *Since data is double-pumped, the support samples the AD31 – AD0 signals twice in one clock cycle, as well as the C/BE3# – C/BE0# signals. The acquired C/BE# data is demultiplexed as if it had been acquired on the 5, 4, 1, and 0 channels of both the C3 and C1 probe sections.*

Table 3–18: AGP_2X: BE_Hi group channel assignments

Bit order	Section:channel	Accelerated Graphics Port signal name
3	C3:5	C/BE3#
2	C3:1	C/BE2#
1	C3:0	C/BE1#
0	C3:4	C/BE0#

Table 3–19 shows the probe section and channel assignments for the BE_Lo group and the bus signal to which each channel connects. By default, this channel group is displayed in binary.

NOTE. *The BE_Lo channel group is the demultiplex target for the second group of four bits of the C/BE3# – BE0# and contains the C/BE3_M# – C/BE0_M# signals.*

Table 3–19: AGP_2X: BE_Lo group channel assignments

Bit order	Section:channel	Accelerated Graphics Port signal name
3	C1:5	C/BE3_M#
2	C1:1	C/BE2_M#
1	C1:0	C/BE1_M#
0	C1:4	C/BE0_M#

Table 3–20 shows the probe section and channel assignments for the Command group and the bus signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–20: AGP_2X: Command group channel assignments

Bit order	Section:channel	Accelerated Graphics Port signal name
6	C2:6	IRDY#
5	E3:1	FRAME#
4	C3:2	PIPE#
3	C3:5	C/BE3#
2	C3:1	C/BE2#
1	C3:0	C/BE1#
0	C3:4	C/BE0#

Table 3–21 shows the probe section and channel assignments for the Status group and the bus signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–21: AGP_2X: Status group channel assignments

Bit order	Section:channel	Accelerated Graphics Port signal name
3	C2:4	GNT#
2	C3:7	ST2
1	C3:3	ST1
0	C2:7	ST0

Table 3–22 shows the probe section and channel assignments for the SBE (Side Band Enable) group and the bus signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–22: AGP_2X: SBE group channel assignments

Bit order	Section:channel	Accelerated Graphics Port signal name
4	C1:7	SBE_D#
3	E2:7	SBA7
2	E2:6	SBA6
1	E2:5	SBA5
0	E2:4	SBA4

Table 3–23 shows the probe section and channel assignments for the SBA_Hi (Side Band Address) group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

NOTE. *Since data is double-pumped, the support samples the AD31 – AD0 signals twice in one clock cycle, as well as the SBA7 – SB0 signals. The acquired SBA data is demultiplexed as if it had been acquired on both the E2:7 – 0 and the E0:7 – 0 channels.*

Table 3–23: AGP_2X: SBA_Hi group channel assignments

Bit order	Section:channel	Accelerated Graphics Port signal name
7	E2:7	SBA7
6	E2:6	SBA6
5	E2:5	SBA5
4	E2:4	SBA4
3	E2:3	SBA3
2	E2:2	SBA2
1	E2:1	SBA1
0	E2:0	SBA0

Table 3–24 shows the probe section and channel assignments for the SBA_Lo (Side Band Address) group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

NOTE. *The SBA_Lo channel group is the demultiplex target for the second group of eight bits of the SBA bus and contains the SBA7_M – SBA0_M signals.*

Table 3–24: AGP_2X: SBA_Lo group channel assignments

Bit order	Section:channel	Accelerated Graphics Port signal name
7	E0:7	SBA7_M
6	E0:6	SBA6_M
5	E0:5	SBA5_M
4	E0:4	SBA4_M
3	E0:3	SBA3_M
2	E0:2	SBA2_M
1	E0:1	SBA1_M
0	E0:0	SBA0_M

Table 3–25 shows the probe section and channel assignments for the QI_Ctrl group and the bus signal to which each channel connects. By default, this channel group is displayed symbolically.

Table 3–25: AGP_2X: QI_Ctrl group channel assignments

Bit order	Section:channel	Accelerated Graphics Port signal name
2	C1:6	VAL_ID#*
1	C1:3	QICNT_ID1*
0	C1:2	QICNT_ID0*

*** Signal not required by the Clocking State Machine.**

Table 3–26 shows the probe section and channel assignments for the Inc_QCnt group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–26: AGP_2X: Inc_QCnt group channel assignments

Bit order	Section:channel	Accelerated Graphics Port signal name
7	C0:7	QICNT7*
6	C0:6	QICNT6*
5	C0:5	QICNT5*
4	C0:4	QICNT4*
3	C0:3	QICNT3*
2	C0:2	QICNT2*
1	C0:1	QICNT1*
0	C0:0	QICNT0*

*** Signal not required by the Clocking State Machine.**

Table 3–27 shows the probe section and channel assignments for the Dec_QCnt group and the bus signal to which each channel connects. By default, this channel group is displayed in hexadecimal.

Table 3–27: AGP_2X: Dec_QCnt group channel assignments

Bit order	Section:channel	Accelerated Graphics Port signal name
7	E1:7	QDCNT7*
6	E1:6	QDCNT6*
5	E1:5	QDCNT5*
4	E1:4	QDCNT4*
3	E1:3	QDCNT3*
2	E1:2	QDCNT2*
1	E1:1	QDCNT1*
0	E1:0	QDCNT0*

*** Signal not required by the Clocking State Machine.**

Table 3–28 shows the probe section and channel assignments for the Control group and the bus signal to which the channel connects. By default, this channel group is displayed symbolically.

Table 3–28: AGP_2X: Control group channel assignments

Bit order	Section:channel	Accelerated Graphics Port signal name
13	QUAL:1	RST#
12	E3:7	PME#*
11	E3:0	RBF#*
10	E3:2	SERR#*
9	E3:6	PERR#*
8	E3:3	PAR*
7	C3:6	REQ#*
6	C2:4	GNT#
5	C3:2	PIPE#
4	E3:1	FRAME#
3	C2:6	IRDY#
2	C2:5	TRDY#
1	E3:4	DEVSEL#*
0	QUAL:3	STOP#

*** Signal not required by the Clocking State Machine.**

Table 3–29 shows the probe section and channel assignment for the Misc channel group and the bus signal to which the channel connects. By default, this channel group is not visible.

Table 3–29: AGP_2X: Misc group channel assignments

Bit order	Section:channel	Accelerated Graphics Port signal name
5	CLK:3	CLK
4	C2:0	LOGIT_D#
3	C2:3	FRAME_D#
2	QUAL:2	PIPE_D#
1	C2:2	IRDY_D#
0	C2:1	TRDY_D#

Table 3–30 shows the probe section and channel assignment for the AD_STB1 group and the bus signal to which the channel connects. By default, this channel group is not visible.

Table 3–30: AGP_2X: AD_STB1 channel assignment

Section:channel	Accelerated Graphics Port signal name
CLK:0	AD_STB1

Table 3–31 shows the probe section and channel assignment for the AD_STB0 group and the bus signal to which the channel connects. By default, this channel group is not visible.

Table 3–31: AGP_2X: AD_STB0 channel assignment

Section:channel	Accelerated Graphics Port signal name
CLK:1	AD_STB0

Table 3–32 shows the probe section and channel assignment for the SB_STB group and the bus signal to which the channel connects. By default, this channel group is not visible.

Table 3–32: AGP_2X: SB_STB channel assignment

Section:channel	Accelerated Graphics Port signal name
E3:5	SB_STB

How Data is Acquired

This part of the chapter explains how the module acquires Accelerated Graphics Port signals using the TMS 806 software and probe adapter. This part also provides additional information on bus signals accessible on or not accessible on the probe adapter, and on extra probe channels available for you to use for additional connections, if any.

Custom Clocking

A special clocking program is loaded to the module every time you load the AGP support. This special clocking is called Custom.

With Custom clocking, the module logs in signals from multiple groups of channels at different times as they become valid on the Accelerated Graphics Port bus. The module then sends all the logged-in signals to the trigger machine and to the memory of the module for storage.

In Custom clocking, the module clocking state machine (CSM) generates one master sample for each bus cycle, no matter how many clock cycles occur in the bus cycle.

Although all cycle types are acquired, there are too many to illustrate in this manual. Refer to the *Accelerated Graphics Port Interface Specifications* for descriptions of the other cycle types. The next six figures show examples of some common AGP cycles.

Figure 3–9 shows the Master Sample (MS) points for a PCI Read Transaction cycle.

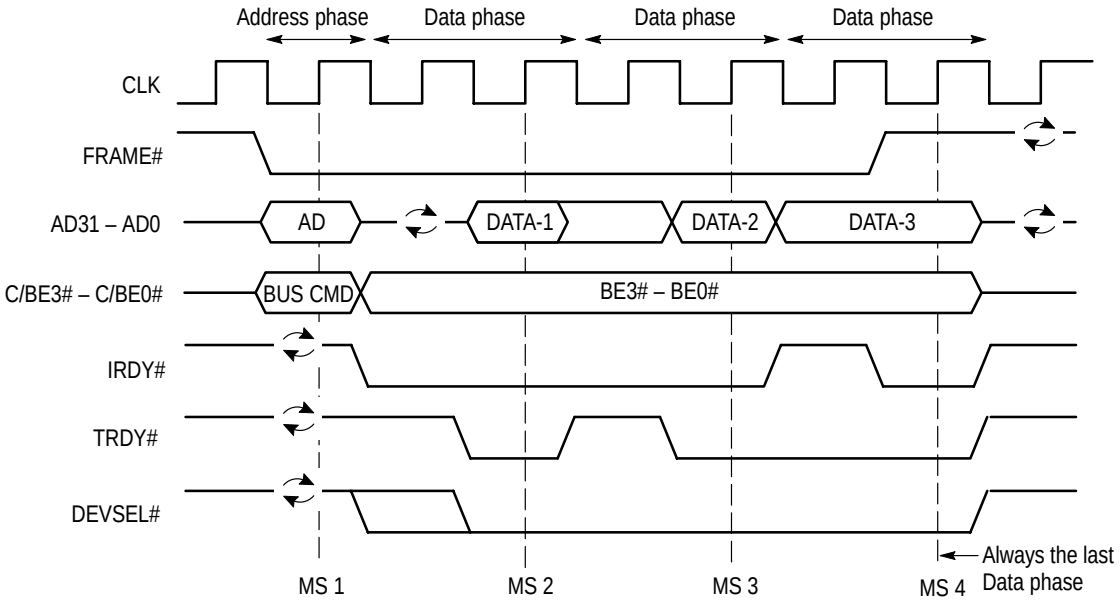


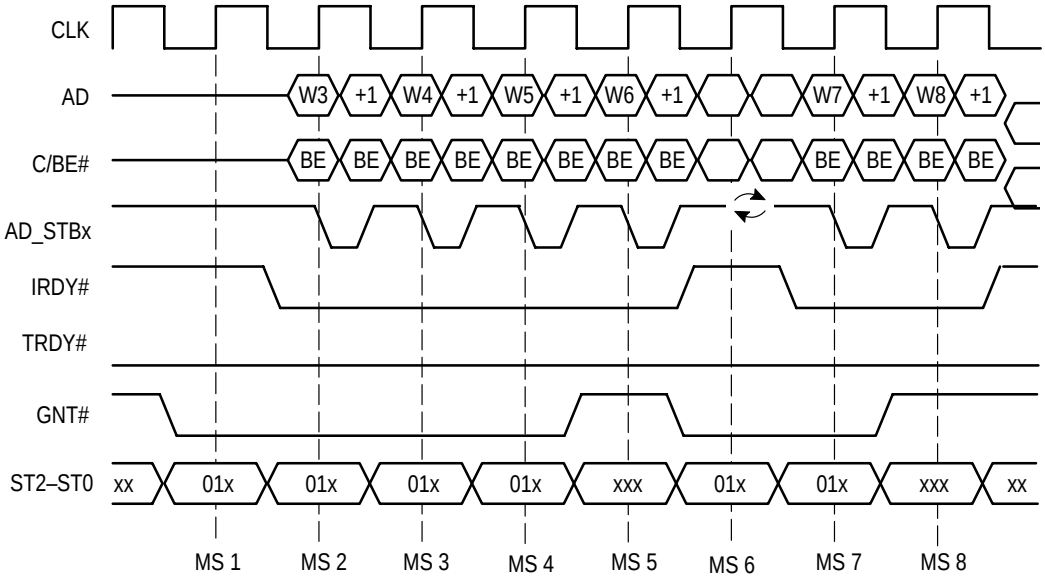
Figure 3–8: PCI Read Transaction cycle

Table 3–33 lists the qualifying signals for each Master Sample point (MS) as shown in Figure 3–8.

Table 3–33: Qualifying signals for PCI Read Transaction cycle samples

MS number	Active qualifier signals	Signals acquired
MS 1	FRAME#	AD31 – AD0, C3 – C0
MS 2	FRAME#, IRDY#, TRDY#	AD31 – AD0, BE3# – BE0#
MS 3	Same as MS2	Same as MS2
MS 4	IRDY#, TRDY#	Same as MS2

Figure 3–9 shows the Master Sample (MS) points for a Write Data Transfer cycle with the AGP_2X setup.



*Note: The AGP_2X setup demultiplexes the AD31 – AD0 and C/BE3# – C/BE0# signals.

Figure 3–9: Write Data Transfer cycle using the AGP_2X setup

Table 3–34 lists the qualifying signals for each Master Sample point (MS) shown in Figure 3–9.

Table 3–34: Qualifying signals for Write Data Transfer cycle samples, 2X mode

MS number	Active qualifier signals	Signals acquired
MS 1	GNT#	ST2 – ST0, GNT#
MS 2	GNT#, AD_STB1, AD_STB0	AD_STB1, AD_STB0, BE3# – BE0#, AD31 – AD0, ST2 – ST0, GNT#
MS 3	Same as MS2	Same as MS2
MS 4	Same as MS2	Same as MS2
MS 5	AD_STB1, AD_STB0	AD_STB1, AD_STB0, BE3# – BE0#, AD31 – AD0
MS 6	GNT#	ST2 – ST0, GNT#
MS 7	GNT#, AD_STB1, AD_STB0	AD_STB1, AD_STB0, BE3# – BE0#, AD31 – AD0, ST2 – ST0, GNT#
MS 8	AD_STB1, AD_STB0	AD_STB1, AD_STB0, BE3# – BE0#, AD31 – AD0

Figure 3–10 shows the Master Sample (MS) points for a Read Data Transfer cycle with the AGP_1X setup.

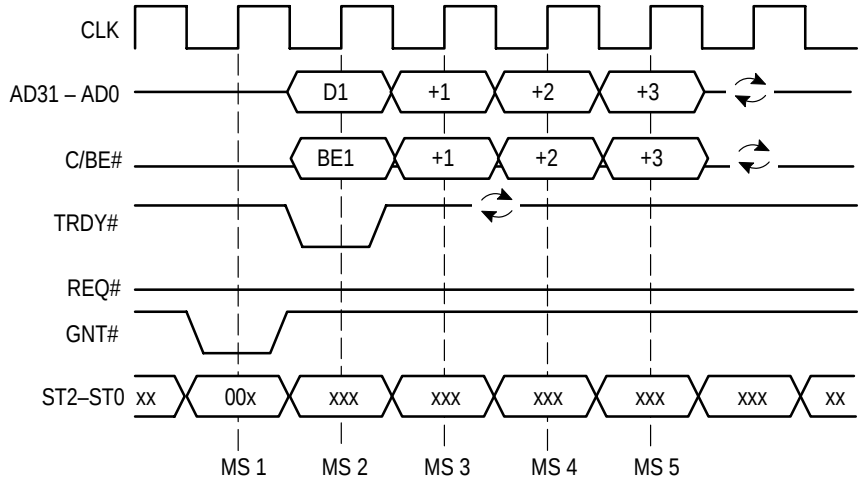


Figure 3–10: Read Data Transfer cycle using the AGP_1X setup

Table 3–35 lists the qualifying signals for each Master Sample point (MS) shown in Figure 3–10.

Table 3–35: Qualifying signals for Read Data Transaction cycle samples, 1X mode

MS number	Active qualifier signals	Signals acquired
MS 1	GNT#	ST2 – ST0, GNT#
MS 2	TRDY# or IRDY#	AD31 – AD0, BE3# – BE0#
MS 3	None*	Same as MS2
MS 4	Same as MS3*	Same as MS2
MS 5	Same as MS3*	Same as MS2

*** The CSM tracking request length is based on the activity of TRDY# and IRDY#.**

Figure 3–11 shows the Master Sample points for a Data Transaction Request cycle in PIPE mode.

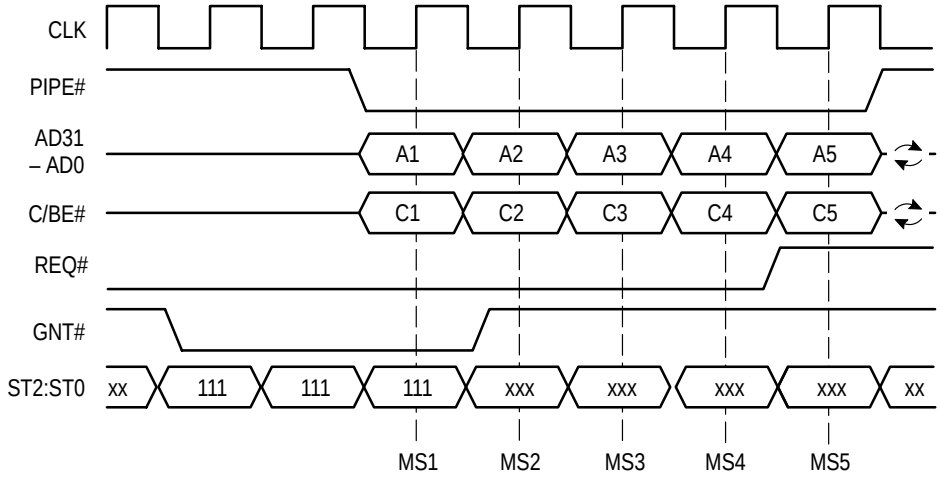


Figure 3–11: Data Transaction Request cycles in PIPE mode

Table 3–36 lists the qualifying signals for each Master Sample point (MS) shown in Figure 3–11.

Table 3–36: Qualifying signals for Data Transaction Request cycle samples, PIPE

MS number	Active qualifier signals	Signals acquired
MS 1	PIPE#	AD31 – AD0, C3 – C0, PIPE#
MS 2	Same as previous Master Sample	Same signals acquired
MS 3	Same as previous Master Sample	Same signals acquired
MS 4	Same as previous Master Sample	Same signals acquired
MS 5	Same as previous Master Sample	Same signals acquired

Figure 3–12 shows the Master Sample points for the Side Band Address mode using the AGP_1X setup.

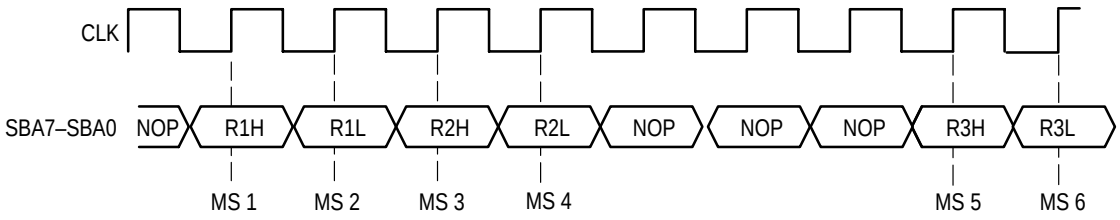


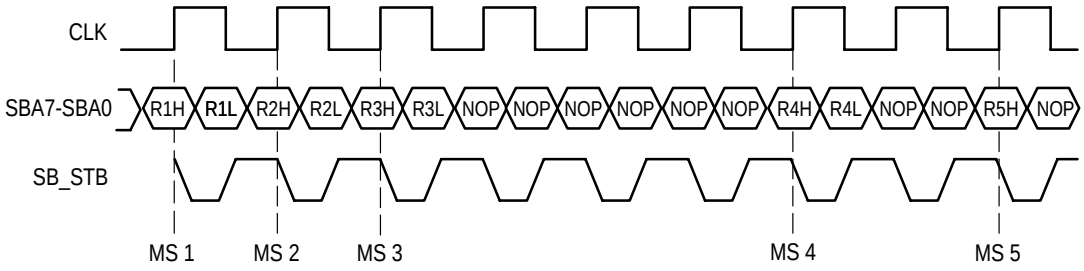
Figure 3–12: Side Band Address mode using the AGP_1X setup

Table 3–36 lists the qualifying signals for each Master Sample point (MS) shown in Figure 3–12.

Table 3–37: Qualifying signals for SBA mode samples, AGP_1X setup

MS number	Active qualifier signals	Signals acquired
MS 1	LOGIT_D#	SBA7 – SBA0, SBE_D#
MS 2	Same as MS1	Same as MS1
MS 3	Same as MS1	Same as MS1
MS 4	Same as MS1	Same as MS1
MS 5	Same as MS1	Same as MS1
MS 6	Same as MS1	Same as MS1

Figure 3–13 shows the Master Sample points for the Side Band Address mode using the AGP_2X setup.



*Note: The AGP_2X setup demultiplexes the SBA bus.

Figure 3–13: Side Band Address mode using the AGP_2X setup

Table 3–36 lists the qualifying signals for each Master Sample point (MS) shown in Figure 3–13.

Table 3–38: Qualifying signals for SBA mode samples, AGP_2X setup

MS number	Active qualifier signals	Signals acquired
MS 1	LOGIT_D#	SBA7 – SBA0, SBE_D#, SB_STB
MS 2	Same as MS1	Same as MS1
MS 3	Same as MS1	Same as MS1
MS 4	Same as MS1	Same as MS1
MS 5	Same as MS1	Same as MS1

Clocking Options

The clocking algorithm for the Accelerated Graphics Port support has two variations: Active Cycles Only and Clock-by-Clock.

Since the data bus is double pumped in 2X mode, the probe adapter and logic analyzer acquire two samples of some signals on every rising edge of the CLK signal. The signals that are sampled twice are AD31 – AD0, SBA7 – SBA0, and C/BE3# – CBE0#.

Active Cycles Only. This clocking option only clocks in cycles with valid data on the AD, SBA, C/BE#, and ST buses.

Clock-By-Clock. This clocking option stores every cycle on every rising edge of the CLK signal.

Alternate Bus Connections

You can connect to other signals that are not required by the support so that you can analyze other signal activity in your system. These signals might or might not be accessible on the probe adapter board. The following paragraphs and tables list signals that are or are not accessible on the probe adapter board.

Signals On the Probe Adapter

The probe adapter board contains pins for bus signals that are not acquired by the TMS 806 support. You can connect other probes to these pins, because the signals and voltages can be useful for general purpose analysis.

If you acquire data from these signals, they are not defined in any channel group, and data acquired from them is not displayed. To display data, you will need to define a channel group.

Table 3–39 shows the bus signals and voltages available on J201 of the probe adapter.

Table 3–39: Accelerated Graphics Port signals on J201

Pin number	Signal name
1	GND
2	OVRCNT#
3	VDDQ +3.3
4	VCC +3.3
5	USB–
6	USB+
7	+5 V
8	+12 V

The Universal Serial Bus (USB+ and USB–) signals are not terminated. The characteristic impedance of the probe circuit board is 65 ohms. You need to take this into account when terminating the USB signals.

Signals Not On the Probe Adapter

The probe adapter does not provide access for the INTA# or INTB# signals.

Extra Channels

Three P6434 probes are connected to the probe adapter for both the AGP_1X and AGP_2X setups.

If you are using the AGP_1X setup, you can use the 34 channels available with two P6417 probe to connect to other signals in your SUT for general purpose analysis. The available channels are: D3:7-0, D2:7-0, D1:7-0, D0:7-0, CLK:2 and QUAL:0.

If you are using the AGP_2X setup, there are only two extra channels, CLK:2 and QUAL:0. Since the AGP_2X setup demultiplexes the AD31-AD0 signals, data is acquired on the D3:7-0, D2:7-0, D1:7-0, and D0:7-0 channels even though these probe sections are not physically connected.

WARNING

The following servicing instructions are for use only by qualified personnel. To avoid injury, do not perform any servicing other than that stated in the operating instructions unless you are qualified to do so. Refer to all Safety Summaries before performing any service.

Maintenance

Maintenance

This chapter contains the following topics:

- *Probe Adapter Circuit Description*
- *Replacing a Complex Programmable Logic Device*
- *Replacing a Rivet*

Probe Adapter Circuit Description

The probe adapter contains two CPLD integrated circuits. Each CPLD follows AGP bus activity from Reset and keeps track of the depth of four counters: Read Low Priority, Read High Priority, Write Low Priority, and Write High Priority.

The PIPE CPLD tracks AGP bus activity when the SUT is operating in 1X or 2X PIPE mode. The SBA CPLD tracks AGP bus activity when operating in 1X or 2X SBA mode. Two jumpers allow you to choose which CPLD is operating (PIPE CPLD or SBA CPLD) and the mode in which your SUT is operating (1X or 2X).

Both CPLDs track the bus by sampling eighteen signals on each rising edge of the CLK signal. The signals are as follows:

C/BE3#	PIPE#	SBA4
C/BE2#	RST#	SBA2
C/BE0#	SB_STB	ST2
FRAME#	SBA7	ST1
GNT#	SBA6	ST0
IRDY#	SBA5	TRDY#

The CPLDs use these signals to track the AGP bus activity and provide control and queue count information along with other qualification information from the bus to the logic analyzer when there are active cycles on the bus.

Queue Counters

The support acquires post-increment and post-decrement counter values as data. All four counter values start when the Reset signal is deasserted. The maximum count value is 255 for each counter.

The GNT# Signal. When the GNT# signal is not asserted, the QDCNT7 – QDCNT0 signals correspond to the Read_Lo counter.

When the GNT# signal is asserted, and the value of the ST2 – ST0 signals is 111, the QDCNT7 – QDCNT0 signals correspond to the Write_Hi counter.

In all other cases, the QDCNT7 – QDCNT0 signals correspond to the appropriate queue counter as indicated by the ST2 – ST0 signals.

The SBA Signal. When the SBA mode is enabled, the QICNT7 – QICNT0 signals correspond to the last counter selected by an SBA Type-2 command. This is the result of the VAL_ID#, QICNT_ID1, and QICNT_ID0 signals being static selections after the SBA Type-2 command.

For an SBA Type-2 FENCE command, the QICNT7 – QICNT0 signals correspond to the Write_Lo counter and the VAL_ID# signal is not asserted (high).

After a Reset and prior to the first SBA Type-2 command, the QICNT7 – QICNT0 signals correspond to the Write_Hi counter and VAL_ID# is not asserted (high).

For all other SBA Type-2 commands, the QICNT7 – QICNT0 signals correspond to the last counter selected by the SBA Type-2 command and VAL_ID# is asserted (low).

For an SBA Type-1 command, the counter that increments is the last one selected by an SBA Type-2 command. For an SBA Type-2 Fence command, none of the counters increment.

The PIPE# Signal. When the PIPE# mode is enabled, but the PIPE# signal is not asserted, the QICNT7 – QICNT0 signals correspond to the Read_Lo counter and VAL_ID# is asserted (low).

When PIPE# is asserted for a FENCE command, the QICNT7 – QICNT0 signals correspond to the Write_Lo counter and VAL_ID# is not asserted (high).

When PIPE# is asserted for an EXTENDED ADDRESS command, the QICNT7 – QICNT0 signals correspond to the Write_Hi counter and VAL_ID# is not asserted (high).

When PIPE# is asserted for any other command, the QICNT_ID1, QICNT_ID0, and QICNT7 – QICNT0 signals correspond to the counter defined by the C/BE3# – C/BE0# signals and VAL_ID# is asserted (low). If a FENCE or an EXTENDED ADDRESS command occurs, the counter does not increment. For all other commands, the counter does increment.

The VAL_ID# Signal. When the VAL_ID# signal is asserted (low), any counter can correspond to the QICNT7 – QICNT0 signals.

When the VAL_ID# signal is not asserted (high), the QICNT7 – QICNT0 signals correspond to the Write_Lo or Write_Hi counter. The counter values can be valid when VAL_ID# is not asserted. This state can occur when the current PIPE cycle is a FENCE or an EXTENDED ADDRESS command or in the current SBA cycle where the previous SBA Type-2 command was a FENCE command.

Derived Signals

The derived signals are the PIPE_D#, FRAME_D#, IRDY_D#, TRDY_D#, SBE_D# and LOGIT_D# signals. The clocking state machine uses these signals to determine when to log data from the AGP bus.

The PIPE_D#, FRAME_D#, IRDY_D# and TRDY_D# signals are delayed by two clocks from the corresponding signals on the AGP bus.

The SBE_D# signal identifies when a Side Band Address command is present on the SBA7 – SBA0 signals.

The LOGIT_D# signal identifies when to log in data to the logic analyzer. This signal is derived by combining several signals in the CPLD relative to the GNT# and SBA signals.

Replacing a Complex Programmable Logic Device

You can replace either Complex Programmable Logic Device (CPLD). To do so, refer to Figure 4–1 and follow these steps:

1. Turn off power to your SUT. It is not necessary to turn off power to the logic analyzer.

CAUTION. *Static discharge can damage the graphics card, the probe adapter, the probes, or the module. To prevent static damage, handle all of the above only in a static-free environment.*

Always wear a grounding wrist strap or similar device while handling the graphics card and probe adapter.

2. Before you remove the probe adapter from the SUT, touch the ground connector located on the back of the logic analyzer to discharge your stored static electricity.
3. Remove the probe adapter and AGP Graphics Card from your SUT.

4. Place the probe adapter with the AGP Graphics Card on a flat anti-static surface. Remove the graphics card from the probe adapter.

5. Remove the PIPE CPLD (U270) or the SBA CPLD (U230), using a CPLD extraction tool.

6. Line up the pin A1 indicator on the CPLD with the pin A1 indicator on the socket on the probe adapter.

CAUTION. *Failure to correctly place the CPLD into the socket on the probe adapter might permanently damage the probe adapter, or SUT once power is applied.*

7. Insert the CPLD into the socket as shown in Figure 4–1.

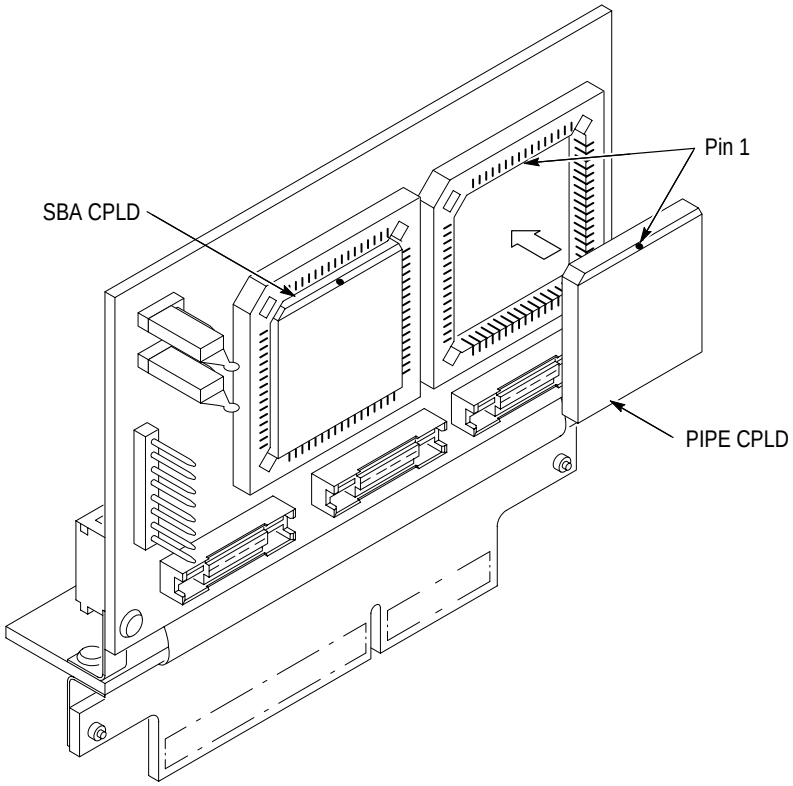


Figure 4–1: Replacing a CPLD

Replacing a Rivet

If you need to replace a rivet, you must orient it correctly. Figure 4–2 shows the correct orientation.

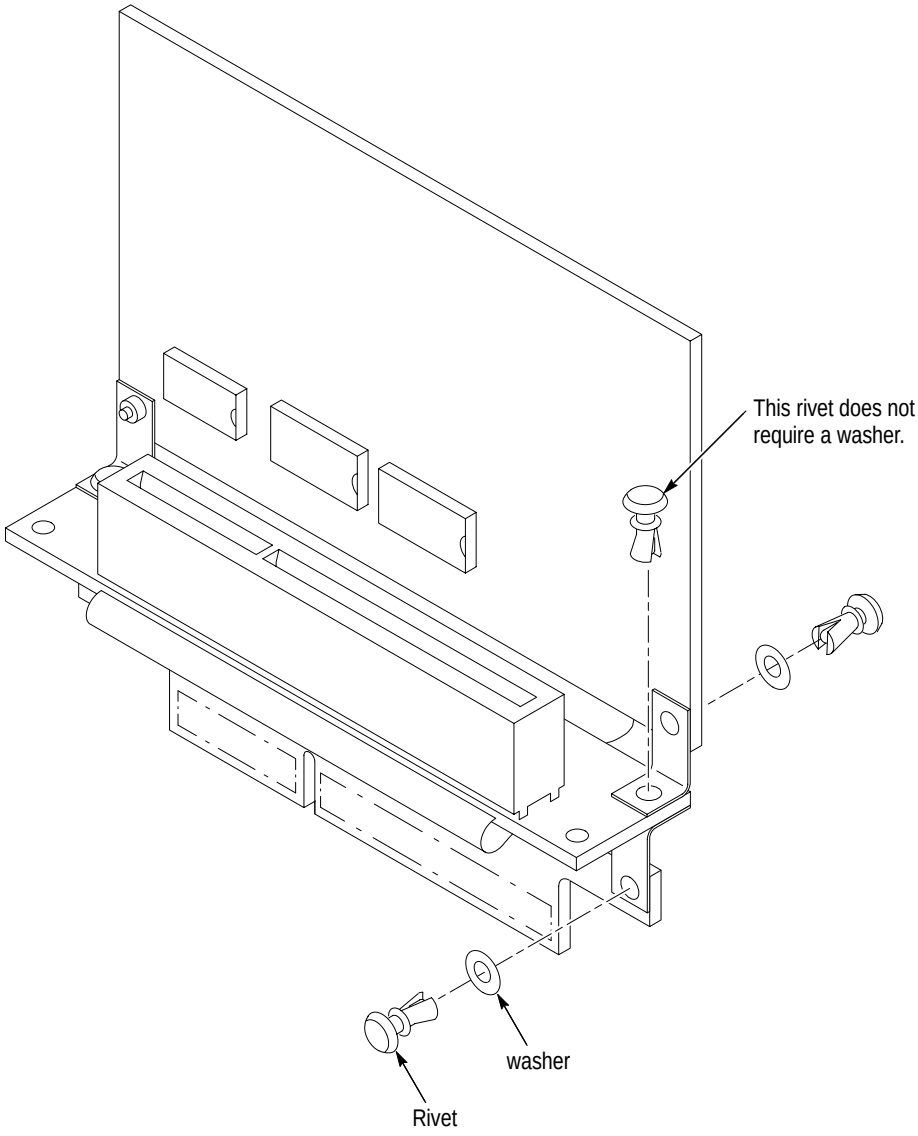


Figure 4–2: Rivet orientation

Replaceable Electrical Parts

Replaceable Electrical Parts

This chapter contains a list of the replaceable electrical components for the TMS 806 Accelerated Graphics Port bus support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Using the Replaceable Electrical Parts List

The tabular information in the Replaceable Electrical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes each column of the electrical parts list.

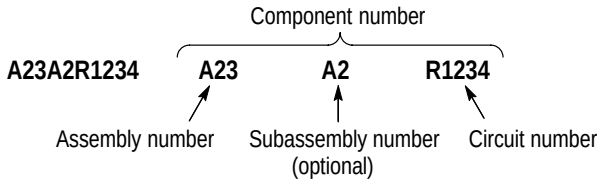
Parts list column descriptions

Column	Column name	Description
1	Component number	The component number appears on diagrams and circuit board illustrations, located in the diagrams section. Assembly numbers are clearly marked on each diagram and circuit board illustration in the *Diagrams* section, and on the mechanical exploded views in the *Replaceable Mechanical Parts* list section. The component number is obtained by adding the assembly number prefix to the circuit number (see Component Number illustration following this table). The electrical parts list is arranged by assemblies in numerical sequence (A1, with its subassemblies and parts, precedes A2, with its subassemblies and parts). Chassis-mounted parts have no assembly number prefix, and they are located at the end of the electrical parts list.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entry indicates the part is good for all serial numbers.
5	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
6	Mfr. code	This indicates the code number of the actual manufacturer of the part.
7	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Component Number



Read: Resistor 1234 (of Subassembly 2) of Assembly 23

List of Assemblies

A list of assemblies is located at the beginning of the electrical parts list. The assemblies are listed in numerical order. When a part's complete component number is known, this list will identify the assembly in which the part is located.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
00779	AMP INC.	CUSTOMER SERVICE DEPT PO BOX 3608	HARRISBURG, PA 17105–3608
06915	RICHCO	5825 N TRIPP AVE P.O. BOX 804238	CHICAGO, IL 60646
26742	METHODE ELECTRONICS INC	BACKPLANE DIVISION 7444 WEST WILSON AVE	CHICAGO, IL 60656–4548
53387	3M COMPANY	ELECTRONICS PRODUCTS DIV 3M AUSTIN CENTER	AUSTIN, TX 78769–2963
5Y400	TRIAX METAL PRODUCTS INC	1880 SW MERLO DRIVE	BEAVERTON, OR 97006
22526	BERG ELECTRONICS INC	825 OLD TRAIL ROAD	ETTERS, PA 17319
TK0198	HAMILTON HALLMARK	9750 SW NIMBUS AVE	BEAVERTON, OR 97005
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077–0001

Replaceable electrical parts list

Component number	Tektronix part number	Serial no. effective	Serial no. discont'd	Name & description	Mfr. code	Mfr. part number
A01	671–4129–00			CIRCUIT BD ASSY:AGP,BUS SUPPORT BD,389–2403–00 WIRED,TMS806 OPT 01	80009	671–4129–00
A01J100	131–4356–00			CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER,	26742	9618–302–50
A01J200	131–4356–00			CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER,	26742	9618–302–50
A01J201	131–6003–00			CONN,HDR:PCB,MALE,STR,1 X 8, 0.1 CTR,0.235 MLG X 0.112 TAIL,30 GOLD,0.035 DIA PCB	53387	2408–6112TB
A01J420	131–6134–01			CONN,RCPT:SMD,MICTOR,PCB,STR,38 POS,FEMALE,0.025 CTR,0.240 H,W/0.108 PCB HOLD DOWNS.PALLAD	00779	767054–1
A01J450	131–6134–01			CONN,RCPT:SMD,MICTOR,PCB,STR,38 POS,FEMALE,0.025 CTR,0.240 H,W/0.108 PCB HOLD DOWNS.PALLAD	00779	767054–1
A01J480	131–6134–01			CONN,RCPT:SMD,MICTOR,PCB,STR,38 POS,FEMALE,0.025 CTR,0.240 H,W/0.108 PCB HOLD DOWNS.PALLAD	00779	767054–1
A01P100	131–4530–00			CONN,HDR:PCB,MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION,	00779	104344–1
A01P200	131–4530–00			CONN,HDR:PCB,MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION,	00779	104344–1
A01U230	163–0984–00			IC,DIGITAL:PRGM 156–7667–00:CMOS,CPLD,EEPLD,MAX 7000E FAMILY,7128E,128 M/C,64 I/O,4 IN,7.5NS	TK0198	163–0984–00
A01U270	163–0998–00			IC,DIGITAL:PRGM 156–7667–00:CMOS,CPLD,EEPLD,MAX7000E FAMILY,7128E,128 M/C,64 I/O,4 IN,7.5NS,	TK0198	163–0998–00

DIAGRAMS AND CIRCUIT BOARD ILLUSTRATION

SYMBOLS

Graphic symbol and class designation letters are based on ANSI Y32.14, 1973 in terms of positive logic. logic symbols are depicted according to the manufacturer's data book information (not according to function).

Letter symbols for quantities used in electrical science and electrical engineering are based on ANSI Y10.5, 1968.

Drafting practices, line conventions, and lettering conform to ANSI Y14.12, 1966 and ANSI Y14.2, 1973.

Abbreviations are based on ANSI Y1.1, 1972.

You can inquire about these ANSI standards by contacting:

American National Standard Institute
1430 Broadway
New York, New York 10018

COMPONENT VALUES

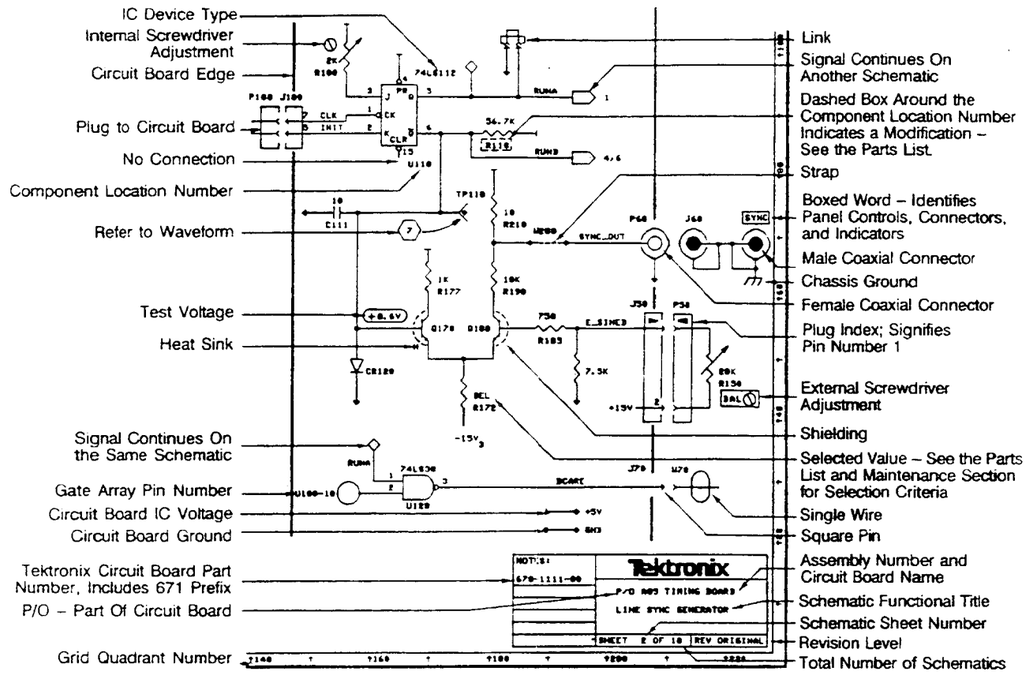
Electrical components shown on the diagram are in the following units unless noted otherwise:

Capacitors = Values one or greater are in picofarads (pF)
Values less than one are in microfarads (μF)

Resistors = Ohms (Ω)

ACTIVE-LOW SIGNAL INDICTORS

A common convention used for indicating an active-low signal (a signal performing its intended function when it is in a low state) is an overbar, as shown in the signal name $\overline{\text{RESET}}$. The overbar may be used in this manual whenever a reference is given to an active-low signal. However, the same active-low signal. However, the same active-low signal is indicated on the schematic with a tilde (~), or a slash (/) following the signal name (e.g., RESET ~ or RESET/).



The information and special symbols below may appear in this manual.

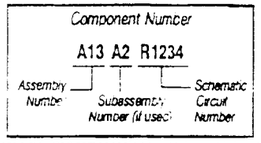
ASSEMBLY NUMBERS

Each assembly in the instrument is assigned as assembly number e.g., A5). The assembly number appears in the title of each:

- schematic diagram (lower right corner)
- circuit board component location look up table (when shown).
- schematic or circuit board component location look up table (when shown).

The Replaceable Electrical Parts list is arranged by assemblies in numerical order. The components are listed alphabetically by component location numbers. Look at the following example to see how to construct a component number.

COMPONENT NUMBER EXAMPLE

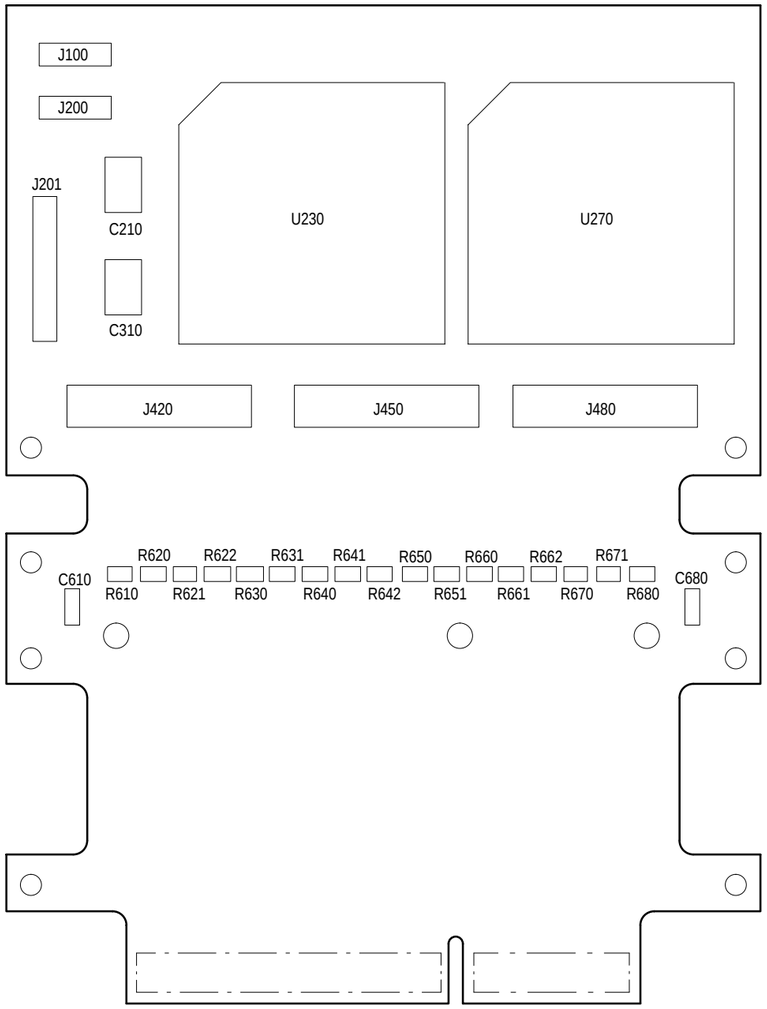


Chassis mounted components have no Assembly Number prefix – see end of Replaceable Parts List.

GRID COORDINATES

The schematic diagram(s) and circuit board component location illustration both have grids. A look up table (when shown) provides grid coordinates for ease of locating components. There may be two tables for each assembly: one for the circuit board component location illustration and one for the schematic diagram(s).

Frontside



Backside

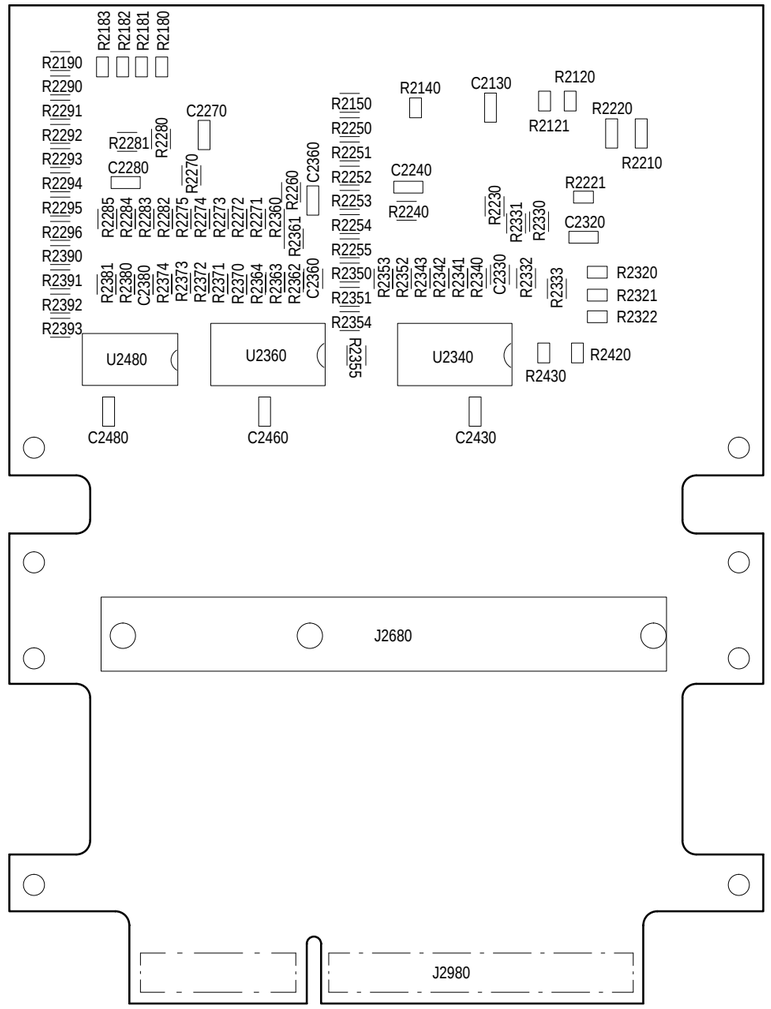
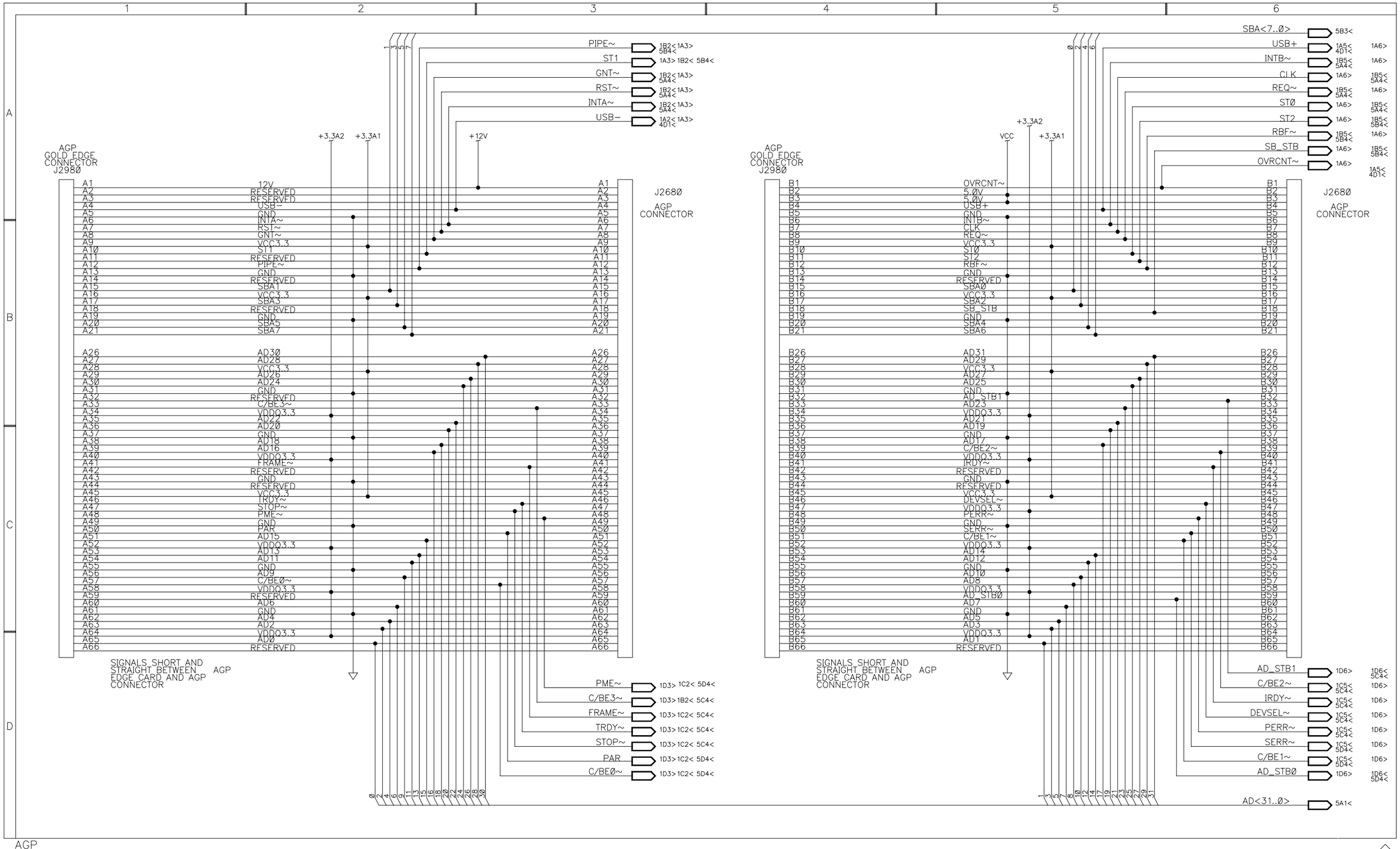
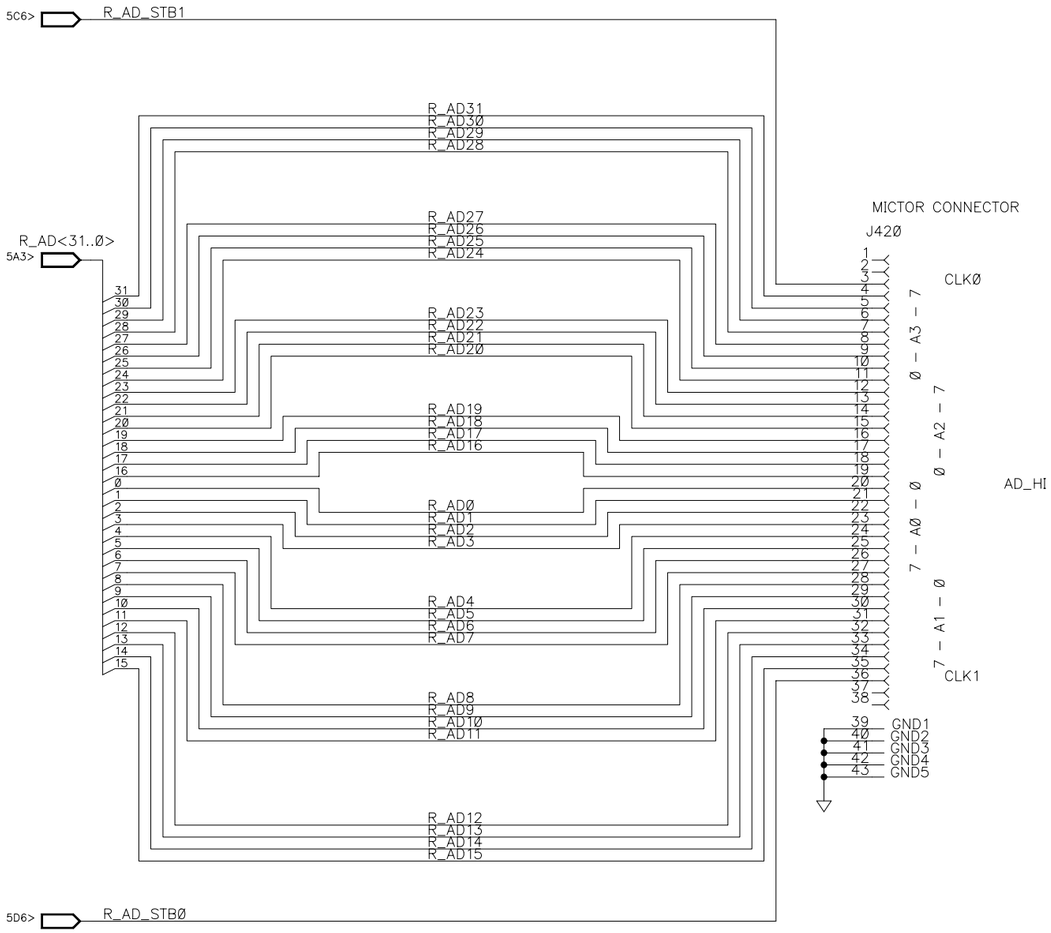


Figure 1: AGP probe adapter exploded mechanical view



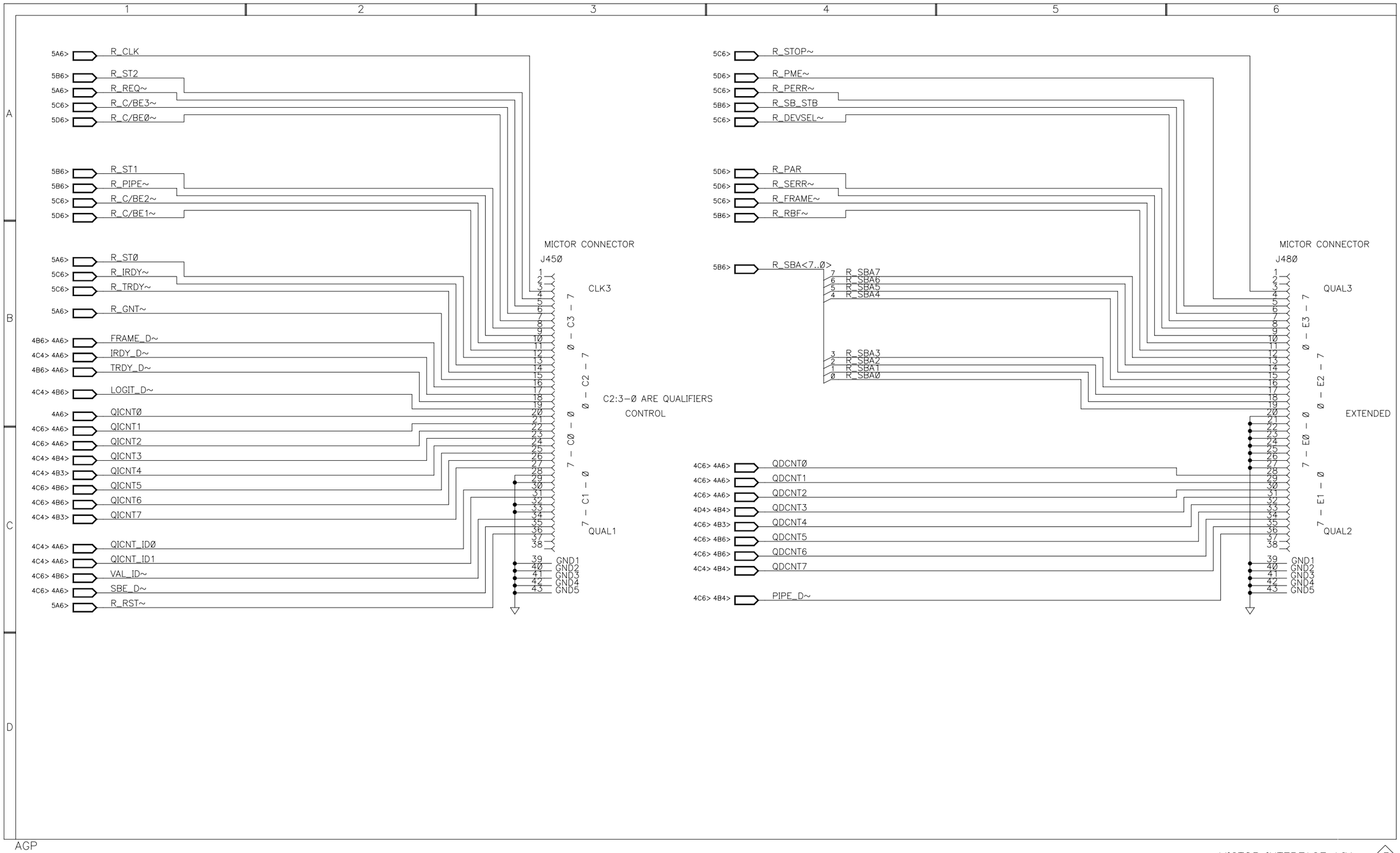
AGP

AGP INTERFACE A01 1



AGP

MICTOR INTERFACE AØ1 2



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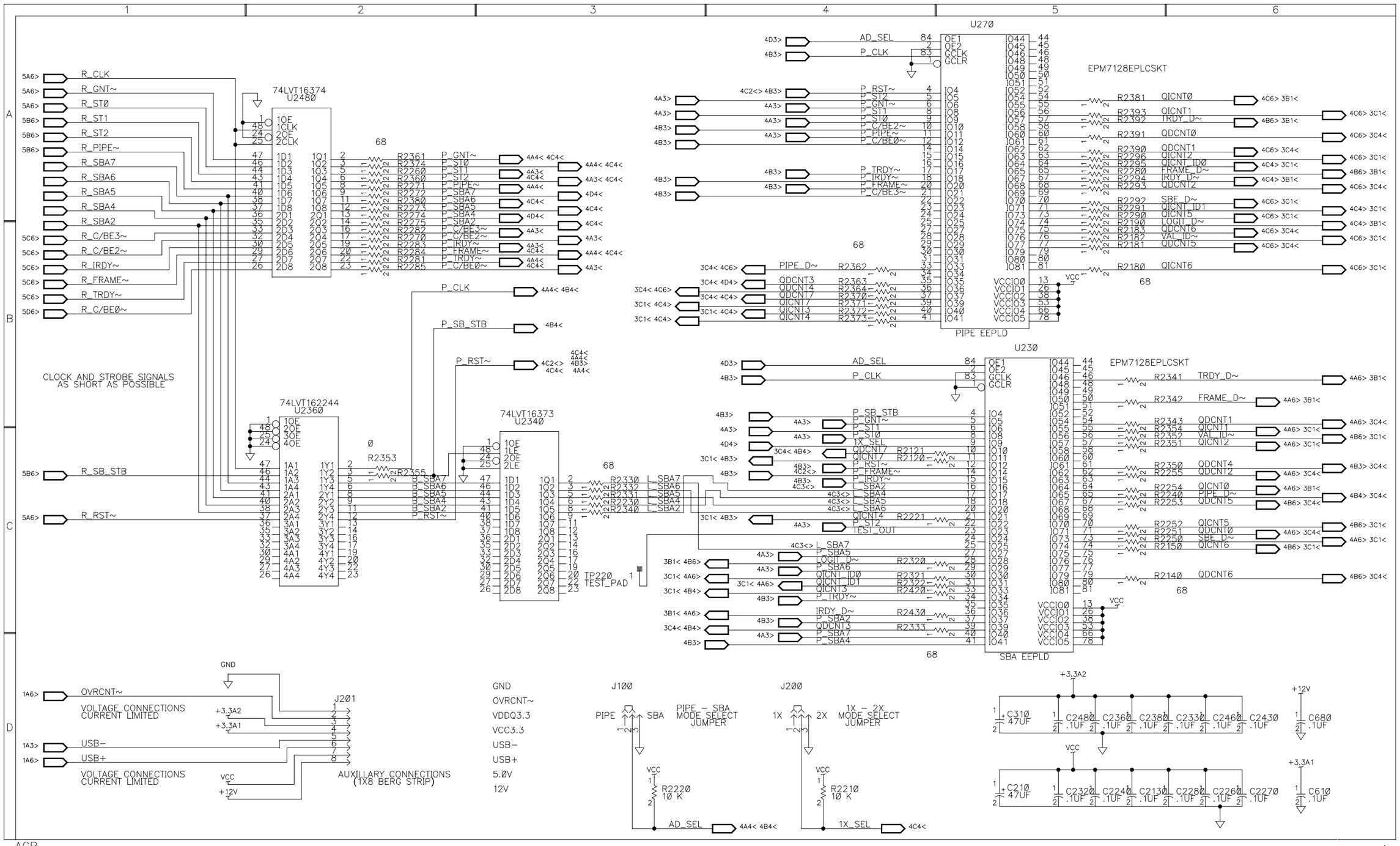
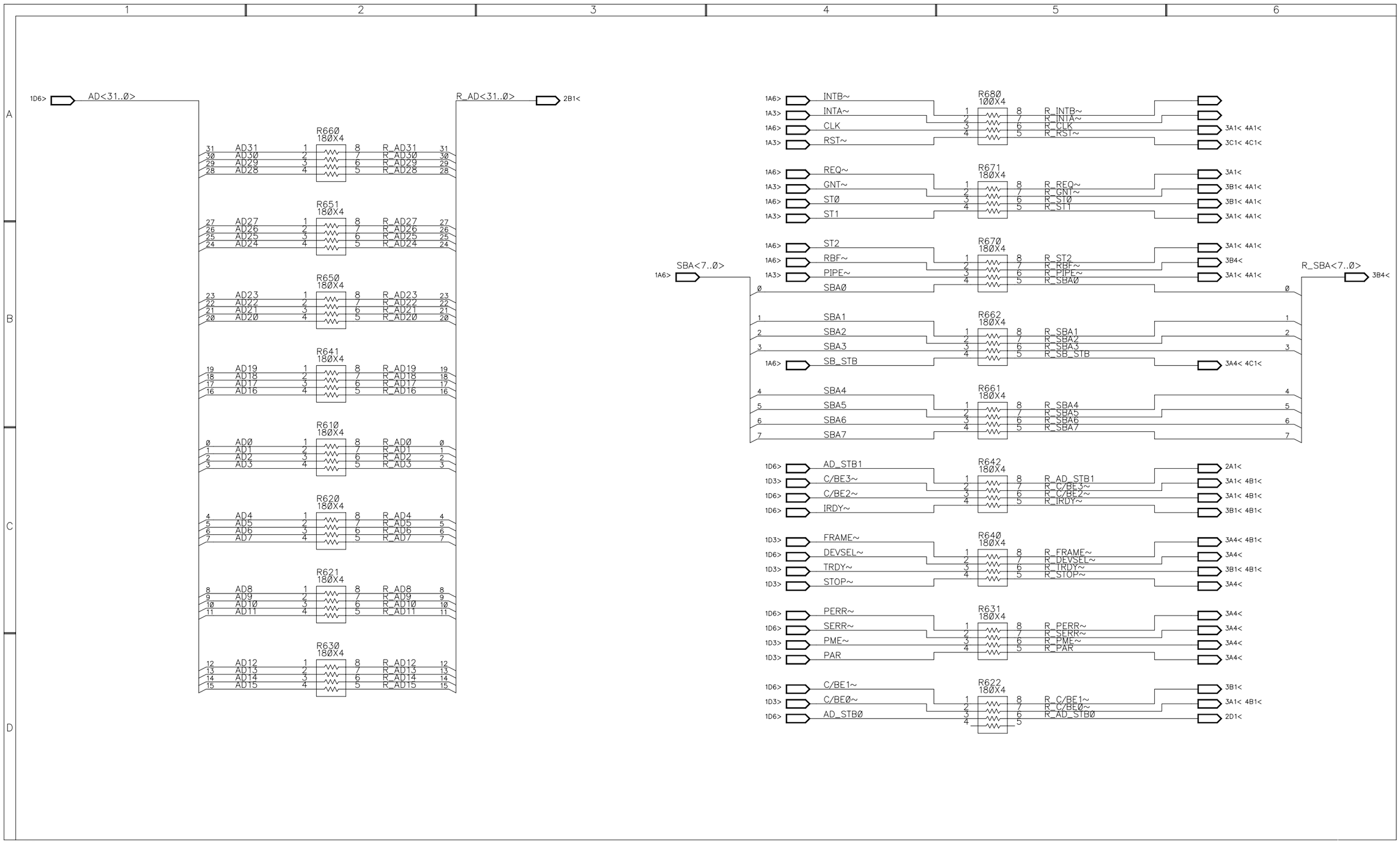
MICTOR INTERFACE AØ1 3


74LVT16374
U2480
74LVT162244
U2360
74LVT16373
U2340
U270
U230
EPM7128EPLCSKT
PIPE EEPLD
SBA EEPLD
CLOCK AND STROBE SIGNALS
AS SHORT AS POSSIBLE
VOLTAGE CONNECTIONS
CURRENT LIMITED
AUXILLARY CONNECTIONS
(1X8 BERG STRIP)
PIPE — SBA
MODE SELECT
JUMPER
1X — 2X
MODE SELECT
JUMPER
R_CLK
R_GNT~
R_ST0
R_ST1
R_ST2
R_PIPE~
R_SBA7
R_SBA6
R_SBA5
R_SBA4
R_SBA2
R_C/BE3~
R_C/BE2~
R_IRDY~
R_FRAME~
R_TRDY~
R_C/BE0~
R_SB_STB
R_RST~
P_CLK
P_SB_STB
P_RST~
PIPE_D~
QDCNT3
QDCNT4
QDCNT7
QICNT7
QICNT3
QICNT4
AD_SEL
P_GNT~
P_ST1
P_ST0
P_C/BE2~
P_PIPE~
P_C/BE0~
P_TRDY~
P_IRDY~
P_FRAME~
P_C/BE3~
IRDY_D~
P_SBA2
QDCNT3
P_SBA7
P_SBA4
1X_SEL
QDCNT7
QICNT7
P_ST2
TEST_OUT
LOGIT_D~
P_SBA6
QICNT_ID0
QICNT_ID1
QICNT3
P_IRDY~
TP220
TEST_PAD
QICNT0
QICNT1
TRDY_D~
QDCNT0
QDCNT1
QICNT2
QICNT_ID0
FRAME_D~
IRDY_D~
QDCNT2
SBE_D~
QICNT_ID1
QICNT5
LOGIT_D~
QDCNT6
VAL_ID~
QDCNT5
QICNT6
TRDY_D~
FRAME_D~
QDCNT1
QICNT1
VAL_ID~
QICNT2
QDCNT4
QDCNT2
QICNT0
QDCNT5
SBE_D~
QICNT6
QDCNT6
OVRCNT~
USB–
USB+
GND
VDDQ3.3
VCC3.3
5.0V
12V
AGP
LOGIC & MISC CONNECTIONS A01
4



AGP

ISOLATION RESISTOR CONNECTIONS A01

Replaceable Mechanical Parts

Replaceable Mechanical Parts

This chapter contains a list of the replaceable mechanical components for the TMS 806 Accelerated Graphics Port bus support. Use this list to identify and order replacement parts.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Using the Replaceable Mechanical Parts List

The tabular information in the Replaceable Mechanical Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
00779	AMP INC.	CUSTOMER SERVICE DEPT PO BOX 3608	HARRISBURG, PA 17105–3608
06915	RICHCO	5825 N TRIPP AVE P.O. BOX 804238	CHICAGO, IL 60646
26742	METHODE ELECTRONICS INC	BACKPLAIN DIVISION 7444 WEST WILSON AVE	CHICAGO, IL 60656–4548
53387	3M COMPANY	ELECTRONICS PRODUCTS DIV 3M AUSTIN CENTER	AUSTIN, TX 78769–2963
5Y400	TRIAX METAL PRODUCTS INC	1880 SW MERLO DRIVE	BEAVERTON, OR 97006
22526	BERG ELECTRONICS INC	825 OLD TRAIL ROAD	ETTERS, PA 17319
TK0198	HAMILTON HALLMARK	9750 SW NIMBUS AVE	BEAVERTON, OR 97005
0KB01	STAUFFER SUPPLY CO	810 SE SHERMAN	PORTLAND, OR 97214–4657
80009	TEKTRONIX INC	14150 SW KARL BRAUN DR PO BOX 500	BEAVERTON, OR 97077–0001

Replaceable mechanical parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
1–1	671–4129–00			1	CIRCUIT BD ASSY:AGP,BUS SUPPORT BD,389–2403–00 WIRED,TMS806 OPT 01	80009	671–4129–00
–2	136–5010–00			2	SOCKET,PLCC:SMD,84 POS,0.05 CTR,0.186 H,TIN,W/PLZ POST,TUBE PACK	22526	69802–084
–3	163–0998–00			1	IC,DIGITAL:PRGM 156–7667–00:CMOS,PLD,EEPLD,MAX 7000E FAMILY,7128E,128 M/C,64 I/O,4 IN,7.5NS; PIPE	TK0198	163–0998–00
–4	163–0984–00			1	IC,DIGITAL:PRGM 156–7667–00:CMOS,PLD,EEPLD,MAX 7000E FAMILY,7128E,128 M/C,64 I/O,4 IN,7.5NS; SBA	TK0198	163–0984–00
–5	131–6134–01			3	CONN,RCPT:SMD,MICTOR,PCB,STR,38 POS,FEMALE,0.025 CTR,0.240 H,W/0.108 PCB HOLD DOWNS.PALLAD	00779	767054–1
–6	131–4530–00			2	CONN,HDR:PCB,MALE,STR,1 X 3,0.1 CTR,0.230 MLG X 0.120 TAIL,30 GOLD,BD RETENTION,	00779	104344–1
–7	131–4356–00			2	CONN,SHUNT:SHUNT/SHORTING,FEMALE,1 X 2,0.1 CTR,0.63 H,BLK,W/HANDLE,JUMPER,	26742	9618–302–50
–8	131–6003–00			1	CONN,HDR:PCB,MALE,STR,1 X 8, 0.1 CTR,0.235 MLG X 0.112 TAIL,30 GOLD,0.035 DIA PCB	53387	2408–6112TB
–9	407–4519–00			4	BRACKET:PROBE ADAPTER BRACE,SST,TMS806	5Y400	407–4519–00
–10	210–1307–00			4	WASHER,LOCK:0.115 ID,SPLIT,0.025 THK,SI BRZ NP	0KB01	ORDER BY DESCRIPTION
–11	210–0127–00			6	RIVET,SNAP:0.118 TO 0.157 THICK,NYLON,BLACK,TMS806	06915	SR–3055B
					STANDARD ACCESSORIES		
	070–9906–00			1	MANUAL,TECH:INSTRUCTION,AGP BUS,TMS 806	80009	070–9906–00
	070–9803–00			1	MANUAL, TECH:TLA 700 SERIES MICRO SUPPORT INSTALLATION	80009	070–9803–00
	010–0612–00			3	LOW-PROFILE EXTENDER FOR P6434 PROBE	80009	010–0612–00

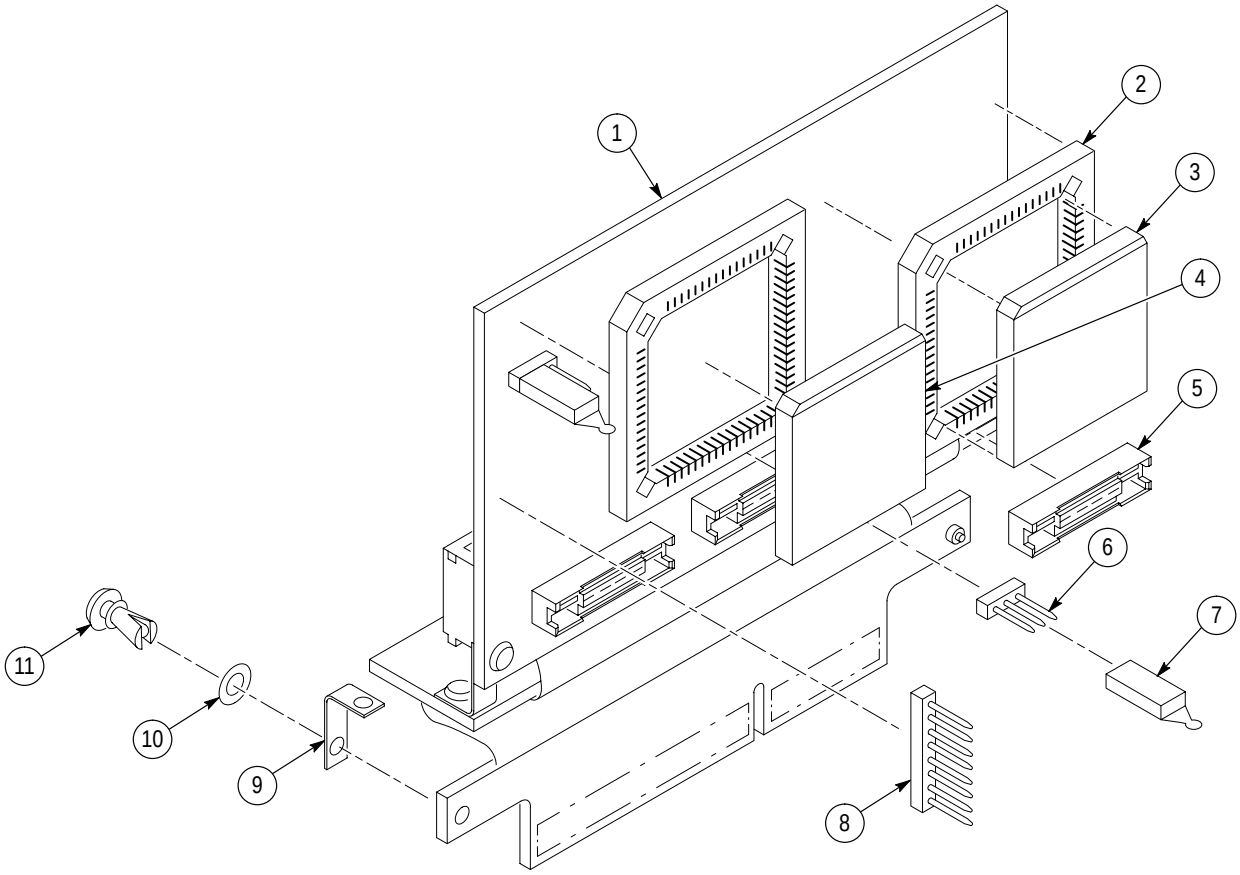


Figure 6–1: Accelerated Graphics Port probe adapter exploded view

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