TYPE 556 LECTURE NOTES

CONFIDENTIAL

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1. General Description
2. Vertical Amplifiers - some new ideas have DC regulators, cross switching.
3. Sweep Triggers - some part value changes, but otherwise very similar to 547.
4. Sweep Generators - very similar to 547 except for sweep unblanking section.
5. Delay Pick-Off - a low pass filter in the comparator circuit, but otherwise almost exactly 547 circuit.
6. Logic, Blanking, and Sync Amplifiers - logic circuit is new.
7. Horizontal Amplifier - exactly 547 except only 10X mag.
8. CRT Circuit - new; 555 HV regulation problems have been cured.
9. Power Supply - new all transistors.
10. Calibrator - multi different, but uses 547 dividers.

TYPE 556 INTRODUCTION

I. GENERAL DESCRIPTION

A. General Purpose Laboratory Scope

1. Basically a Type 555 with 547 type circuitry.

2. Vertical is compatible with letter series plug-ins.

3. Rackmount available.

4. Shielded to reduce radiation interference.

B. Vertical

1. Designed for "1" series plug-ins, but will accept letter series.

2. Passband of 50 Mc with Type 1A1.

a. Risetime with 1A1 is 7.00 ns.

3. Mostly transistorized to reduce thermal drift.

4. Fixed - tuned delay line.

5. No vertical signal out.

C. Horizontal

1. Identical A and B sweeps.

a. Sweep rates 5 sec to .1 μs unmagnified.

b. X1 and X10 mag.

c. No stability control.

d. Sweep will free-run in absence of triggers when TRIGGERING control is switched to AUTO (Bright Line automatic).

2. Horizontal Display Switch
    a. Ext (A, B, left plug-in) (A, B, right plug-in).
    b. B Dely'd by A.
    c. External Horizontal.
3. Alternate
    a. A sweep and B sweep displayed alternately.
    b. Trace separation shifts A vertical so both traces can be observed - separation controlled by front panel control.
    c. Sweeps may be set at different sweep rates.
    d. When used with 1A1 or CA, both sweeps appear on both channels.
    e. Two traces are displayed simultaneously with a single trace plug-in, and may be horizontally positioned independently.
    f. Contrast control reduces trace intensity in the A Intens by B except for the B portion of the trace which is normal intensity.
4. Single Sweep
    a. Ready lights indicate when sweep is armed and ready to accept a trigger.
    b. Reset controlled by RESET push-buttons.
5. Sweep Delay
    a. B Dely'd by A.
    b. Jitter less than 1 part in 20,000.
    c. Delay time multiplier is a 10 turn HELIPOT.

6. EXTERNAL Horizontal Amplifiers
    a. 1-10 variable control.
    b. X10 compensated attenuator.
    c. 1 meg at about 65 pF input Z.
    d. 450 kHz passband with variable at max gain.
    e. Sensitivity is about 80 mV/cm uncalibrated.
7. Triggering A and B identical.
    a. Triggering over entire vertical range.
    b. Trigger selectable from:
        (1) Int normal - right or left vertical.
        (2) Int plug-in - right or left plug-in.
        (3) Ext.
        (4) Line.
    c. Coupling:
        (1) AC.
        (2) AC LF reject.
        (3) AC HF reject.
        (4) DC.
    d. ± Slope.
    e. Automatic or triggered.

D. CRT
1. 5" round glass CRT, T5560.
2. Characteristics nearly identical to T5470.

3. 6 x 10 cm display area for each beam less 1 cm in each corner.
4. 4 cm of overlap between beams.
5. 10 kV accelerating potential.
6. Front panel electrical TRACE ROTATION.
7. Front panel ASTIGMATISM, INTENSITY, FOCUS, and SCALE illumination controls with graduated scales.
8. Z axis modulation (AC coupled) to each cathode.
9. DC unblanking.

E. Calibrator

1. 1 kHz square wave.
2. 0.2 mV to 100V in 18 steps.
3. 50Ω output Z at all millivolt steps.
4. 100V DC available.
5. 5 mA, 1 kHz square wave through a front panel current loop for calibrating current probes.

F. Power Supply

1. Regulates from 100V to 130V.
2. -150, +100, +225, +350V regulated supplies.
3. All transistorized.
4. 1 zener regulated 10V supply.
5. 1 unregulated 6V - 8.5V supply.
6. Supplies regulate with plug-ins removed.
7. No time delay relay.
8. Fan cooling, thermal cut-out.

II. VERTICAL AMPLIFIERS

A. The Vertical Amplifiers provide the driving voltages for the CRT vertical deflection plates.

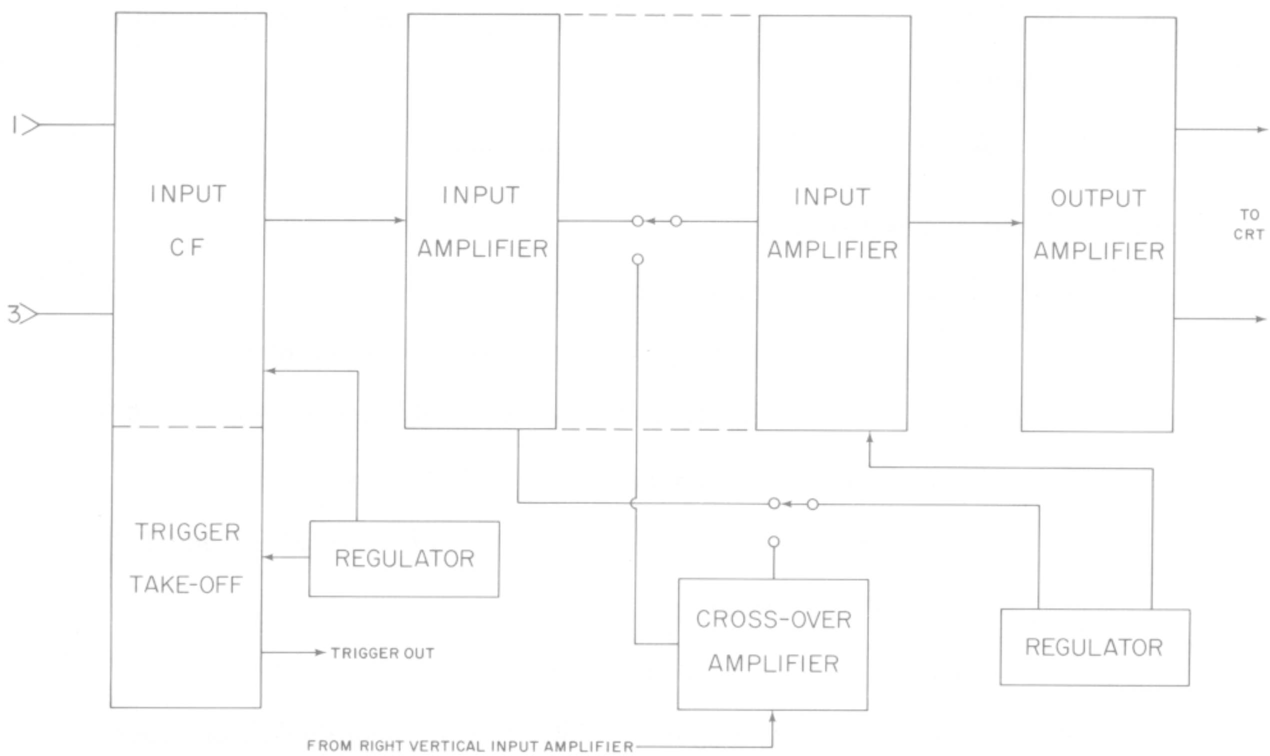
1. A push-pull trigger take-off is provided.

B. Circuit Requirements

1. Output is a push-pull voltage of 7.2 V/cm*.
   a. For 6 cm display, each plate must swing 21.6V*.
   b. Deflection plate voltage at beam electrical center is 172V.
2. Input sensitivity is standardized at 0.1 V/cm push-pull.
   a. Plug-In output is elevated to 67.5V DC at pins 1 and 3 of blue ribbon connector.
3. Nominal vertical amplifier gain is 72.
4. Maximum plate swing at the CRT is approximately 65V or about three 6 cm screen diameters.
   a. Each plate will go from about 140V to 205V.
5. No vertical signal out.
6. Trigger signal to A and B trigger generators.
   a. Push-pull 0.7 V/cm.
   b. Output impedance is 93Ω.

*Nominal CRT deflection factor.

C. Block Diagram



TYPE 556 LEFT VERTICAL AMPLIFIER
BLOCK DIAGRAM

B-556-0200
5-2-'66 mw

D. Left Input CF, Trigger Take-Off and Regulator

1. The circuit is made up of a pair of cathode followers driving a pair of emitter follower/amplifiers, a voltage regulator and a pair of emitter followers.

   a. V3A and V3B are halves of a 12AT7.

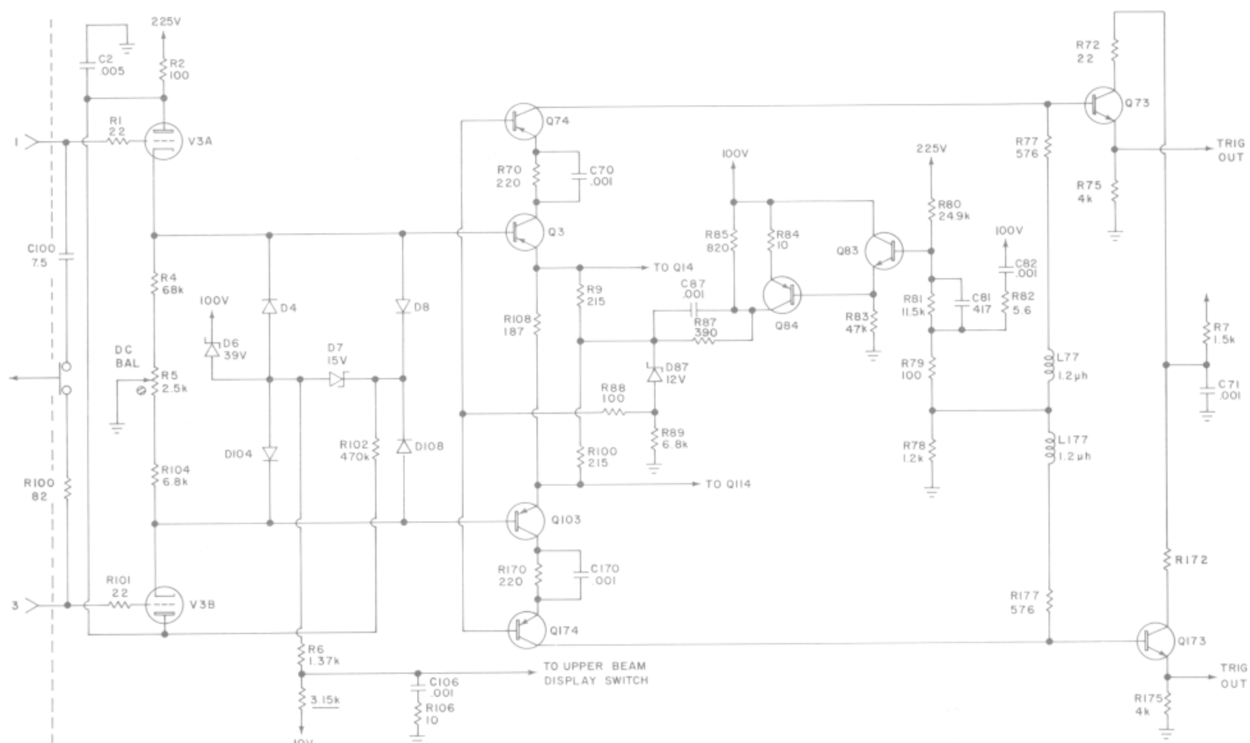
   b. Q3 and Q103 are 2N2929 germanium PNP transistors.

c. D4, D104, D8, D108 are 6185 silicon diodes.

d. Q74, Q174 are PNP germanium transistors.

e. Q83, Q73, Q173 are NPN silicon transistors.

f. Q84 is a 151-087, J3138 silicon transistor.



TYPE 556 LEFT VERTICAL AMPLIFIER
INPUT C.F., TRIGGER TAKE-OFF AND REGULATOR

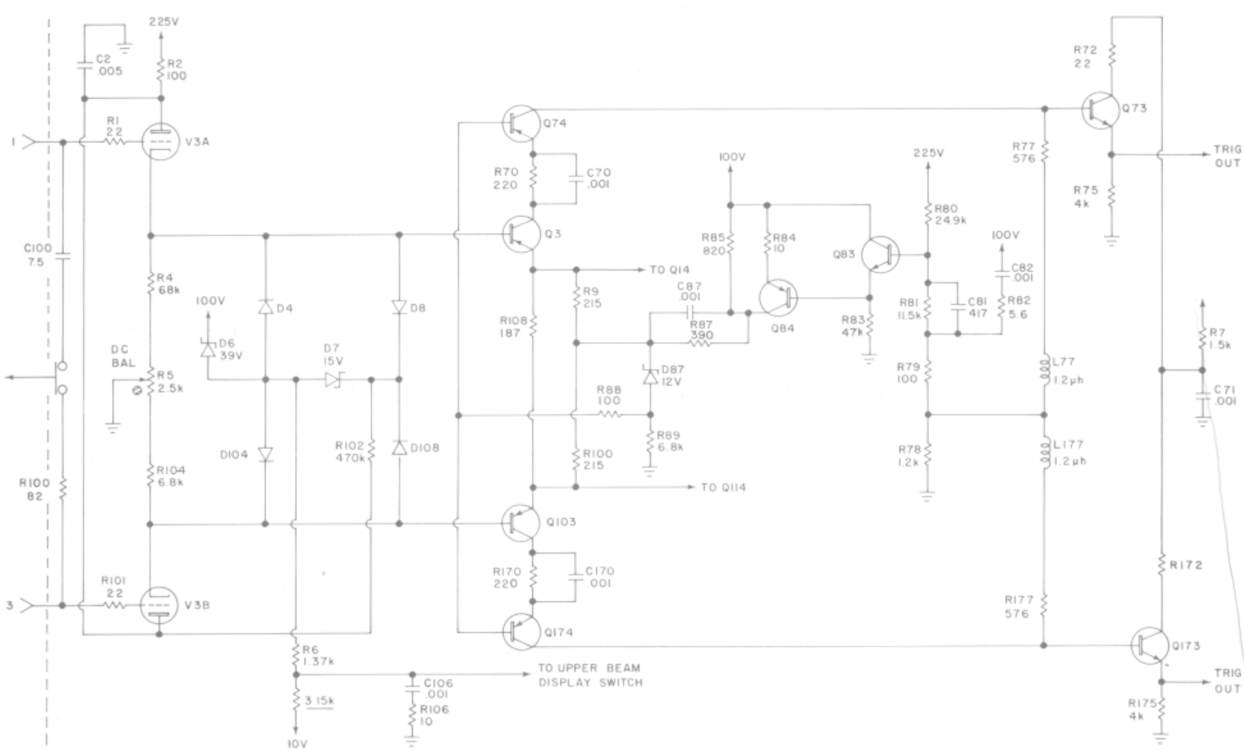
B-556-0201
4-11-'66jg A

2. The input is compatible with existing letter series plug-ins and does not restrict the bandpass of the 1 series plug-ins.
   a. 0.1 V/cm input sensitivity and 67.5V DC levels are compatibility requirements of all letter plug-ins.
   b. Plug-ins like the Type N with high output impedance require a high input impedance.
      (1) The cathode followers provide the high input Z.
   c. The letter series plug-in characteristics were not controlled above 30 Mc.
      (1) Used with a wide bandpass vertical like the Type 556 would result in waveform distortion -- overshoot, ringing, etc.
      (2) A 7.5 pF capacitor and a 82Ω resistor are connected between pins 1 and 3 whenever a letter series plug-in is used.
      (3) A switch actuated by letter series plug-ins connects the RC to the circuit.
      (4) Plug-ins like the 1A1 have a hole in the rear panel so the switch will not be pressed.
3. The cathode followers are not cathode coupled.
4. A VERT DC BAL control corrects for unbalance in the amplifier.
   a. If the VERT POSITION control in the plug-in sets the level on pins 1 and 3 the same, the trace should be centered.

b. The VERT DC BAL control has a swing of about 8 cm to assure this DC balance without selecting tubes and transistors.

5. The CF is directly coupled to the push-pull amplifier/emitter follower.

a. Q3 and Q103 are emitter followers for the vertical signal path and are the lower half of push-pull cascode amplifiers for the trigger take-off path.



TYPE 556 LEFT VERTICAL AMPLIFIER
INPUT C.F., TRIGGER TAKE-OFF AND REGULATOR

B-556-0201
4-11-66jg

6. D4 and D104 are catching diodes that prevent Q3 and Q103 bases from dropping below 61V.

   a. The 61V level is set by D6 from the 100V bus.

   b. If the plug-in is removed when the scope is on (or V1003 is removed from its socket), the diodes catch the bases at 60V, preventing transistor damage.

   c. D8 and D108 are catching diodes that limit the positive rise at the CF cathodes to +76V.

      (1) This positive limit is set by D7, a 15V zener.

      (2) R102 provides "keep alive" current through D7 when D8 and D108 are not conducting.

   d. R6, R7, and R8 furnish current through D6 to maintain the 39V drop.

      (1) Voltage at junction of R6, 7, 8 is used for vertical diode gate switching for cross-over amplifier.

      (2) C106 and R106 dissipate transients on the switching bus.

7. Q3 and Q103 act as emitter followers for the signal path.

   a. The output is taken from the emitters and goes to the bases of Q14 and Q114.

   b. Q3 and Q103 also form the lower half of push-pull cascode amplifiers for the trigger pick-off circuit.

   c. R70 and R170 are thermal compensating resistors compensated for high frequencies by C70 and C170.

8. Q74 and Q174 are the upper halves of a push-pull cascode amplifier which drives Q73 and Q173, trigger output emitter followers.

   a. R77 and R177 are the collector loads for the cascode amplifier.

   b. L77 and L177 provide high frequency peaking.

   c. There is no DC output level adjustment.

9. Q83 and Q84 form a regulator which keeps the DC output level of the trigger pick-off circuit constant.

   a. If a plug-in with an output level less than 67.5V is plugged in.

      (1) The level at the CF (V3) cathodes will become more negative.

      (2) The output of Q3, Q103 emitters will become more negative and this level change will appear at Q14, Q114 bases.

      (3) The negative level change will also tend to cause the current through the cascode amplifiers to increase.

      (4) A more positive voltage across R78 causes Q83 to conduct more -- its emitter will go in a positive direction reducing current through Q84.

      (5) Less voltage drop will appear across R89. (The voltage will be equal to the plug-in output level change.)

(6) D87 keeps the voltage drop from Q74, Q174 bases to Q103, Q3 emitters constant.

(7) The change in input voltage now appears as a change in voltage across Q74, Q174 and the output voltage at R78 returns to its original value. The output DC level of the trigger take-off returns to its former value.

10. The current regulator Q83, Q84 can respond to rapid changes of current through R78.

    a. C81, C87 provide high frequency compensation.

    b. Common mode signal cancellation improves the common mode rejection of the amplifier.

11. Q73, Q173 furnish a push-pull low impedance signal to the trigger circuits.

12. C2, R2, R7, C71, R82, C82 provide decoupling.

E. Left Vertical Input Amplifier and Regulator

1. Q14 and Q114 are the input stage for a push-pull cascode amplifier.

    a. In normal (left plug-in) operation, Q44 and Q144 are the output stage.

    b. In right plug-in operation, the crossover amplifier becomes the input stage.

    c. A diode gate switches between the two input circuits.

2. A 170 ns delay line delays the signal between the two sections of the cascode amplifier.

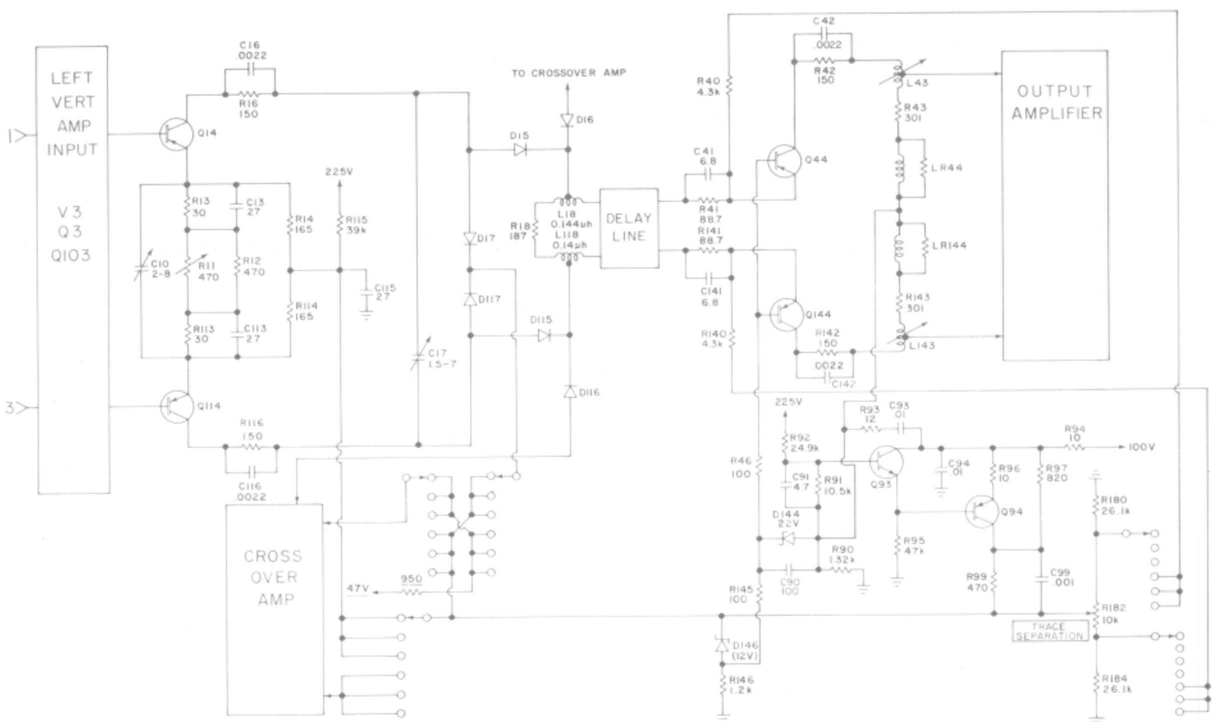
   a. The delay follows the diode gate.

   b. A Tek made counter spiral wound shielded delay line is used.

   c. No delay line adjustments are needed.

   d. The line has a characteristic impedance of 186Ω (93Ω each side).

   e. .01 inch wire is used with a DC resistance of about 8Ω.



TYPE 556 LEFT VERTICAL AMPLIFIER
INPUT AMPLIFIER AND REGULATOR

B-556-0202
4-11-'66 jg

3. The delay line must be terminated at both ends in 93Ω on each side.

   a. The output impedance is 88.7Ω, R41, R14, and the 5Ω emitter impedance of Q44 and Q144.

   b. The reverse termination is R18, 187Ω.

4. Q14, Q114, Q44, Q144 are all germanium PNP transistors.

   a. D17, D117, D16, D116, D15, D115 are all silicon diodes.

5. R13 and R113 set the minimum resistance between Q114 and Q14 emitters.

   a. R11 sets the maximum range of R12.

   b. R12 sets the normal amplifier gain.

   c. R14 and R114 are emitter resistors.

   d. C13 and C113 are high frequency peaking compensations.

   e. C10 is a variable HF compensation to compensate for circuit variations (settings of R11, etc.).

   f. C115 is an oscillation suppressor for high frequencies.

   g. R115 provides partial current to the stage during normal operation and full current (2.5 mA) when operated in right plug-in mode.

   h. R15 and R116 are thermal compensations; C16 and C116 compensate them for high frequencies.

   i. C17 is a high frequency compensation which helps to reverse terminate the line to 186Ω.

j. Tee coils L18 and L118 appear as a section of transmission line.

6. R41 and R141 with the 5Ω emitter impedance of Q44 and Q144 are the termination for the delay line in 186Ω.

   a. C41 and C141 compensate for rising emitter impedance with increasing frequency.

   b. Trace separation current is coupled to the emitters of Q44 and Q144 through R40 and R140 in the RIGHT PLUG-IN positions of the UPPER BEAM DISPLAY switch.

   c. R42 and R142 are temperature compensations compensated for high frequencies by C42 and C142.

   d. L43 and L143 are high frequency peaking coils.

   e. R43 and R143 are the collector loads.

   e. LR44 and LR144 are high frequency compensations.

7. In normal operation +72V is connected to the junction of D17 and D117.

   a. D17 and D117 are back biased, D15 and D115 are forward biased, D16 and D116 are backward biased.

   b. The regulator (Q93, Q94) is connected to R14, R114.

   c. In crossover operation (right plug-in input), D17, D117 have 47V applied to their junction; the voltage at the delay line is 62V.

      (1) D17 and D117 conduct; D15 and D115 are back biased; D16 and D116 are forward biased.

(2) The crossover amplifier, a replica of Q14, Q114 stage is then connected into the circuit.

8. The vertical regulator corrects for variations in common mode levels from plug-ins.

   a. The operation is the same as the trigger pick-off regulator.

   b. The regulator will keep the voltage drop across R90 constant.

   c. Any common mode voltage change at the bases of Q14 and Q114 will cause the regulator to feed back an equal change to the bases of Q44, Qp44, and to the junction of R14 and R114.

   d. Feedback keeps the emitter/collector voltage and current through Q14 and Q114 constant.

   e. The input voltage change will appear across Q44 and Q144 resulting in constant voltage levels being sent to the output amplifier.

9. D144 protects the base/collector junctions of Q44 and Q144.

   a. C91 and C99 are high frequency compensations.

   b. C94 and R94 are a decoupling network.

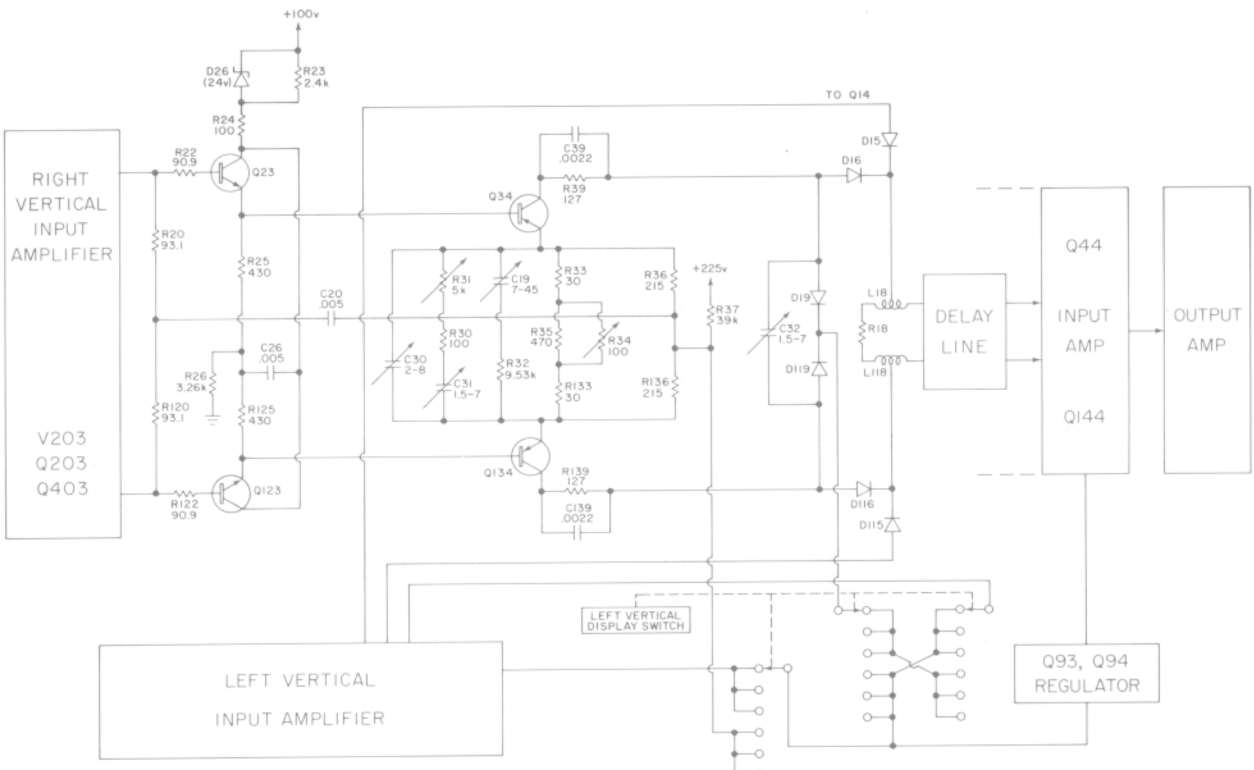
   c. R97 bypasses current around Q94 lowering transistor dissipation.

   d. C90 prevents oscillations.

   e. R93 and C93 limit the high frequency response of the regulator.

   f. R180, R182, R184 are the TRACE SEPARATION divider used in "right plug-in" operation.

F. Cross-Over Amplifier



TYPE 556 LEFT VERTICAL AMPLIFIER
VERTICAL CROSS-OVER AMPLIFIER

B-556-0203
5-19-'66 mw

1. The cross-over amplifier makes it possible to drive both vertical amplifiers from the right plug-in.

   a. The cross-over amplifier is switched in and out of the circuit by a diode gate.

   b. Q23 and Q123 are push-pull emitter followers to reduce loading of the right vertical amplifier.

c. Q34 and Q134 are the lower halves of a push-pull cascode amplifier when switched into operation.

d. Q34 and Q134 replace Q14 and Q114 used in normal operation.

e. The regulator is switched to the appropriate amplifier.

f. In cross-over operation D19 and D119 are backward biased, D16 and D116 are forward biased, and D15, D115 are backward biased cutting off the normal amplifier.

g. R20, R120 terminate the cross-over coax cables.

h. R22 and R122 are oscillation suppressors.

i. D26 provides a solid 24V offset from 100V for the collectors of Q23 and Q123 -- R23 bypasses part of the current.

j. R25, R125 are emitter load resistors; C26 and R26 provide common mode rejection; R24 is an emitter decoupling resistor.

k. C20 provides common mode feedback.

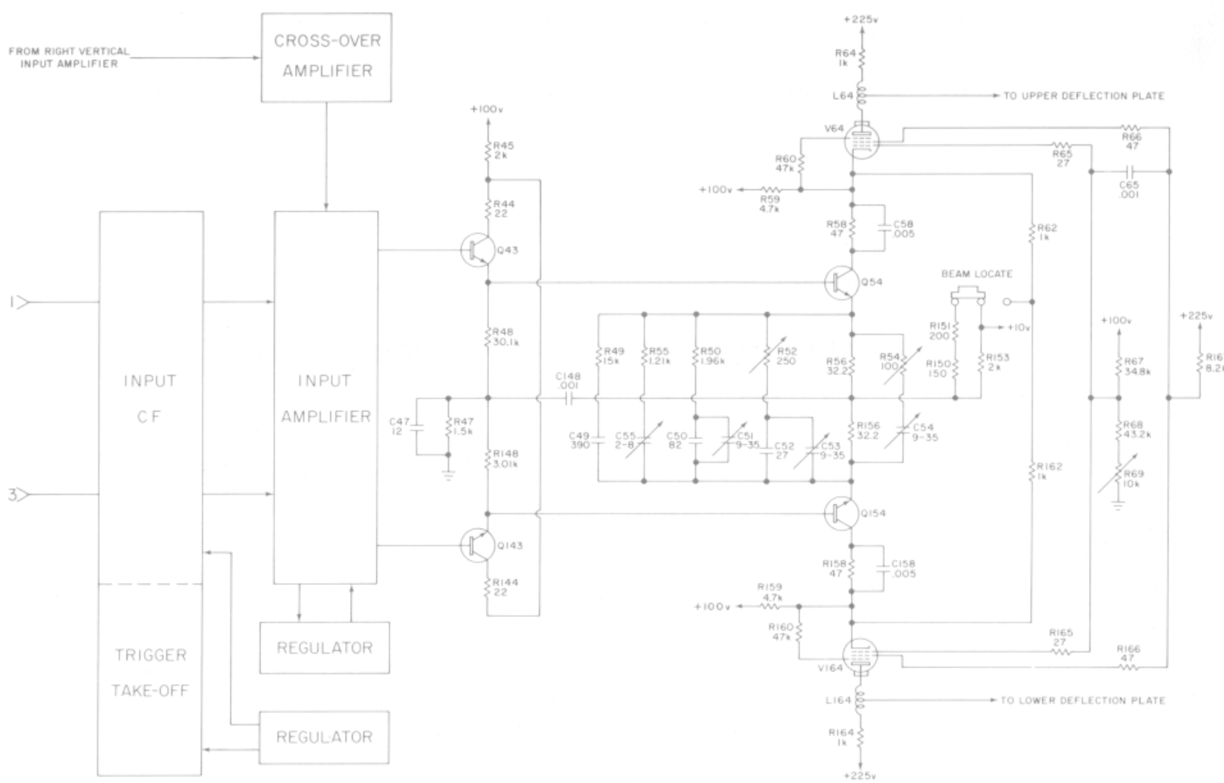
l. C30, R31, R31, C31, C19, R32, and C32, are all high frequency adjustments to compensate various time constants.

m. R33 and R133 set the minimum coupling between emitters of Q34 and Q134 while R35 sets the maximum range of R34.

n. R39 and R139 are temperature compensations bypassed for high frequencies by C39 and C139.

o. R37 supplies current to emitters of Q34 and Q134 when the amplifiers are not in operation and partial current in cross-over operation (2.5 mA).

G. Output Amplifier



TYPE 556 LEFT VERTICAL AMPLIFIER
OUTPUT AMPLIFIER

B-556-0204
5-23-'66 mw

1. The output amplifier is composed of Q43, Q143 emitter followers; Q54, Q154 silicon amplifiers -- the lower halves of push-pull cascode amplifiers; and V64, V164, the upper halves of the hybrid output amplifier.

2. Q43 and Q143 provide high impedance inputs to follow the high impedance output of the previous grounded base stage, Q44 and Q144, and provide low impedance drive for Q54 and Q154.
3. Use of cascode amplifiers reduces the effect of Miller capacitance in the output amplifiers.
   a. Q43 and Q143 are 151-109 silicon NPN transistors.
   b. Q54 and Q154 are 2N3137 NPN silicon transistors.
   c. V64 and V164 are 8608 pentodes with a GM of about 50,000 -- they are 8233 tubes with a plate cap for lower capacity.
   d. The output amplifier has a gain of about 25, giving an overall vertical gain of about 75 (depending on CRT sensitivity).
4. A beam locate switch is connected in the emitters of Q54 and Q154.
   a. Pushing the beam locate switch removes R151 and R150 from the circuit, limiting the current through Q54 and Q154. This limits their amplification and brings a presentation back on the screen.
   b. R62 and R162 are added from the output tube cathodes to +10V keeping output tube current constant.
   c. Power supply voltages must be accurate to keep output characteristics of the amplifier constant. R69 adjusts the grid voltage of the output stage to provide optimum thermal compensation for Q54 and Q154.

5. C148 and C65 are added to increase common mode rejection.

6. R49, C49, R55, C55, R50, C50, C51, R52, C52, C53, R54, and C54 are high frequency compensations with different time constants for adjusting high frequency coupling between the emitters of Q54 and Q154.

7. R56 and R156 set the DC coupling between emitters and the gain of the stage.

8. R65, R66, R165, R166, R44, R144 are oscillation suppressors.

9. R167 is a screen dropping resistor.

10. R58 and R158 are temperature compensations bypassed at high frequencies by C58 and C158.

11. R59 and R159 shunt current around the output tubes.

    a. More current was needed for Q54 and Q154 than the output tube ratings.

12. L64 and L164 provide high frequency peaking.

    a. R64 and R164 are plate loads.

    b. R60 and R160 are suppressor decoupling resistors.

12. R47, R48, R148 provide long tailing for Q43 and Q143.

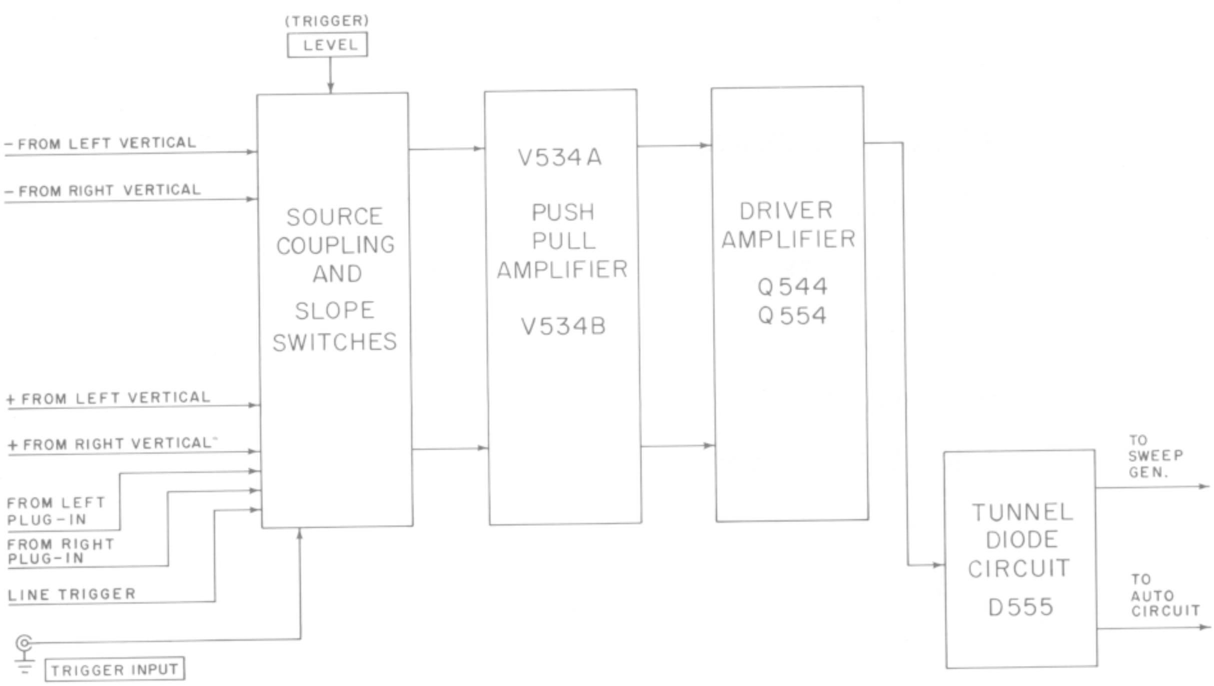
    a. R47 is a common non-precision resistor with high wattage rating.

    b. Common mode signal is developed across R47, but is bypassed for very high frequencies by C47.

III. SWEEP TRIGGERS

A. Two nearly identical trigger circuits provide triggers to the A Sweep and B Sweep Generators.

1. This discussion will refer to the A trigger circuit.



TYPE 556 A SWEEP TRIGGER
BLOCK DIAGRAM

B. The circuit consists of a cathode coupled push-pull amplifier, a push-pull-to-single ended amplifier and a bistable tunnel diode.

C. The output is a 500 mV positive going pulse with a risetime of about 1/2 ns.

D. Operating modes (selected from front panel lever wafer switches).

1. TRIGGERING SOURCE
   a. INT NORMAL - right or left plug-in.
   b. INT PLUG-IN - right or left plug-in.
   c. LINE.
   d. EXT.
2. TRIGGER COUPLING
   a. AC.
   b. AC LF REJ.
   c. DC.
   d. AC HF REJ.
3. TRIGGERING SLOPE
   a. + or -
4. MODE
   a. Triggered,
   b. Automatic.

E. INPUTS (selected by the SOURCE switch)

1. EXTERNAL (front panel jack).
   a. 1M at about 30 pF.
2. LINE
   a. About 1V RMS.
   b. The sine wave is attenuated so the triggering level control will allow triggering at any point on the waveform.

3. PLUG-IN

   a. From pin 5 of the blue ribbon connector.

4. INTERNAL

   a. A push-pull signal from the Vertical Amplifier Trigger Pick-Off.

   b. About 800 mV/cm push-pull.

F. Control

1. TRIGGERING LEVEL

   a. Selects the level on the input waveform at which triggering will occur.

   b. An X10 range increase switch is actuated when the TRIGGERING LEVEL knob is pulled.

   c. Two ranges allow a wide dynamic range for big signals and a sensitive adjustment for smaller signals.

G. Input Circuits

1. NORM INT Mode

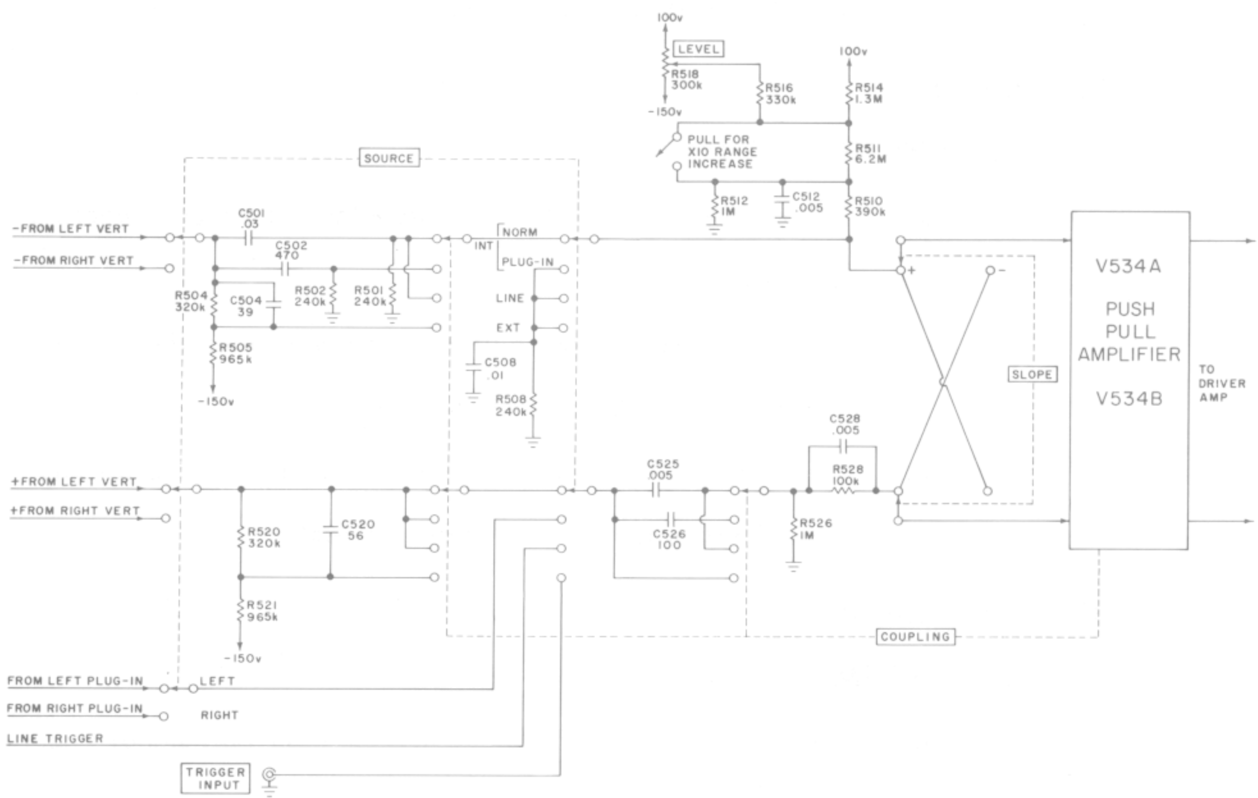
   a. The input is a 700 mV to 800 mV/cm push-pull signal from the Vertical Trigger Pick-Off circuit.

   b. Source impedance is 186Ω (93Ω each side).

   c. In AC, AC LF REJ, AC HF REJ, and DC the input is push-pull.

      (1) The push-pull input tends to reject common mode noise.

d. In the DC position of the COUPLING switch, the plus side of the input from the Vertical Amplifier is attenuated about 25% by the INT TRIG DC LEVEL divider.



TYPE 556 A SWEEP TRIGGER
INPUT CIRCUITS

B-556-0206
1-12-'66dl

e. There is no internal trigger DC level adjustment.

2. PLUG-IN INT Mode

a. A single ended signal from the plug-in via pin 5 of the blue ribbon connector.

b. Signal amplitude is a minimum 500 mV/cm (typically about 900 mV/cm).

   (1) Directly in parallel with CH 1 TRIGGER out jack on a 1A1.

c. Makes it possible to trigger internally from one channel of a multi channel plug-in.

3. LINE Mode

   a. 6.3V AC is attenuated to about 1V RMS.

   b. The AC sine wave is applied to V534B grid.

   c. DC coupling is available as well as AC, AC LF REJ, and HF REJ.

4. EXT Mode

   a. Tied to the front panel TRIGGER INPUT jacks (BNC).

   b. A 100k protective resistor is provided, bypassed by a .005 μF capacitor.

   c. Input impedance is 1M at about 30 pF.

   d. Will trigger on 200 mV.

5. Coupling Switch

   a. The AC position places a capacitor in both sides of the feed from the Vertical Amplifier in the NORM INT mode.

      (1) Trigger input is 3 dB down at about 30 Hz.

   b. The AC LF REJ position places a 100 pF capacitor in one side of the NORM INT input and a 470 pF capacitor in the other.

      (1) 3 dB down at about 2.5 kHz.

c. The DC position of the switch connects both inputs to a divider.

d. Regulators in the vertical amplifier make a DC trigger level adjustment unnecessary.

e. The HF REJ position places a .0022 μF cap between the trigger amplifier plates.

(1) 3 dB down at 60 Hz and 60 kHz.

6. TRIGGERING LEVEL Control

a. Has a normal range (knob pushed in) of about ±2.5V at V534 grid.

(1) Meter loading may give erroneous reading.

b. X10 range increase (knob pulled out) increases the range to ±25V.

c. Sets the DC level on V534A grid (or V534B grid when in -SLOPE).

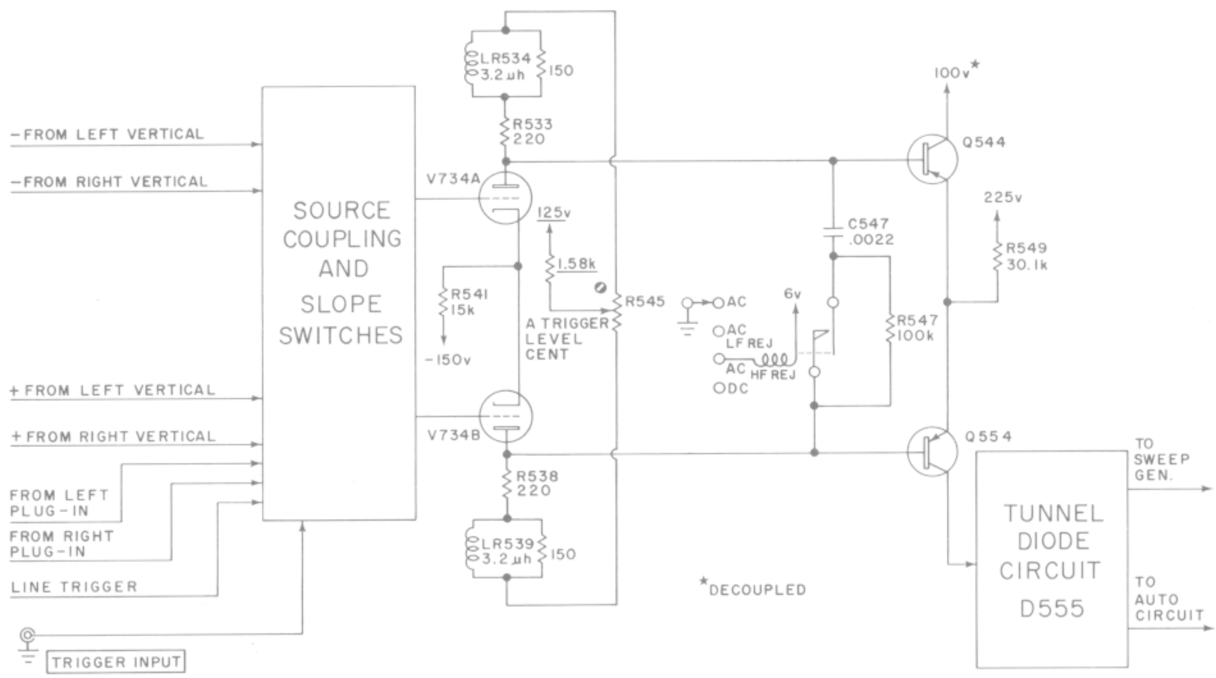
7. SLOPE Switch

a. Reverses the polarity of the input signal.

b. Connection to V534A and V534B grids is reversed.

c. In DC position in INT NORM mode and in PLUG-IN, LINE and EXT, the signal can be switched to V534A grid instead of V534B grid.

H. Push-Pull Amplifier



TYPE 556 A SWEEP TRIGGER
PUSH PULL & DRIVER AMPLIFIER

B-556-0207
1-13-'66dl

1. The amplifier uses two halves of a 6DJ8 dual triode.

   a. Vacuum tubes make high input Z (EXT mode) practical.

2. When a push-pull signal is received (NORM INT mode with AC or AC LF REJ coupling), the circuit is a cathode coupled push-pull amplifier.

3. When a single ended signal is used, the circuit becomes a paraphase inverter.

4. The circuit can be considered a differential amplifier. The circuit measures the difference voltage between the grids.

    a. The TRIGGERING LEVEL control can swing the grids as much as ±25V (X10 RANGE INCREASE).

    b. The long-tail cathodes allow the grids to work at these levels with little change in plate current.

5. The amplifier has a voltage gain of about 2.

    a. The output has a swing of about 1.4 V/cm push-pull.

6. Low value plate load resistors assure fast response to a fast trigger.

7. Plate current is supplied through the TRIGGER LEVEL CENTERING control and an equivalent 1760Ω to 126V.

8. The TRIGGER LEVEL CENTERING control sets the current through V534 in the middle of the tunnel diode hysteresis range for either + or - slope.

    a. A screwdriver calibration adjustment.

    b. Normally, the adjustment will set equal currents through Q544 and Q554.

I. Driver Amplifier

1. The Driver Amplifier is an emitter coupled push-pull to single ended amplifier.

    a. Q544 and Q554 are Motorola 2N3906 silicon PNP transistors (151-0188).

2. The triggering waveform switches current from one transistor to the other.

3. The emitters are long-tailed to 225V.

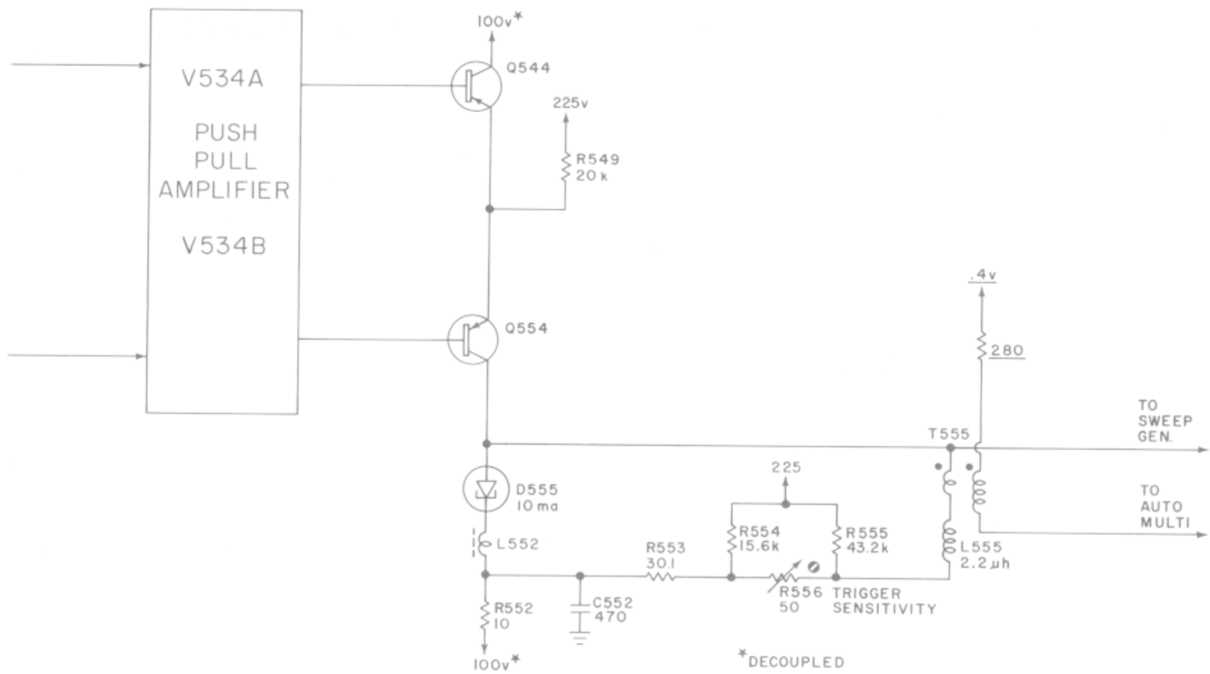
    a. Emitter voltage is 103V.

    b. Quiescently, about 3 mA flows through each transistor.

4. As current in Q554 increases, the TD flips to its high state starting sweep.

J. Tunnel Diode Circuit

1. The Tunnel Diode circuit provides a triggering pulse of uniform amplitude and shape regardless of the shape of the input trigger.



TYPE 556 A SWEEP TRIGGER
TUNNEL DIODE CIRCUIT

2. The circuit uses a 10 mA tunnel diode.

3. Choice of tunnel diode load resistance places the TD in a bistable configuration.

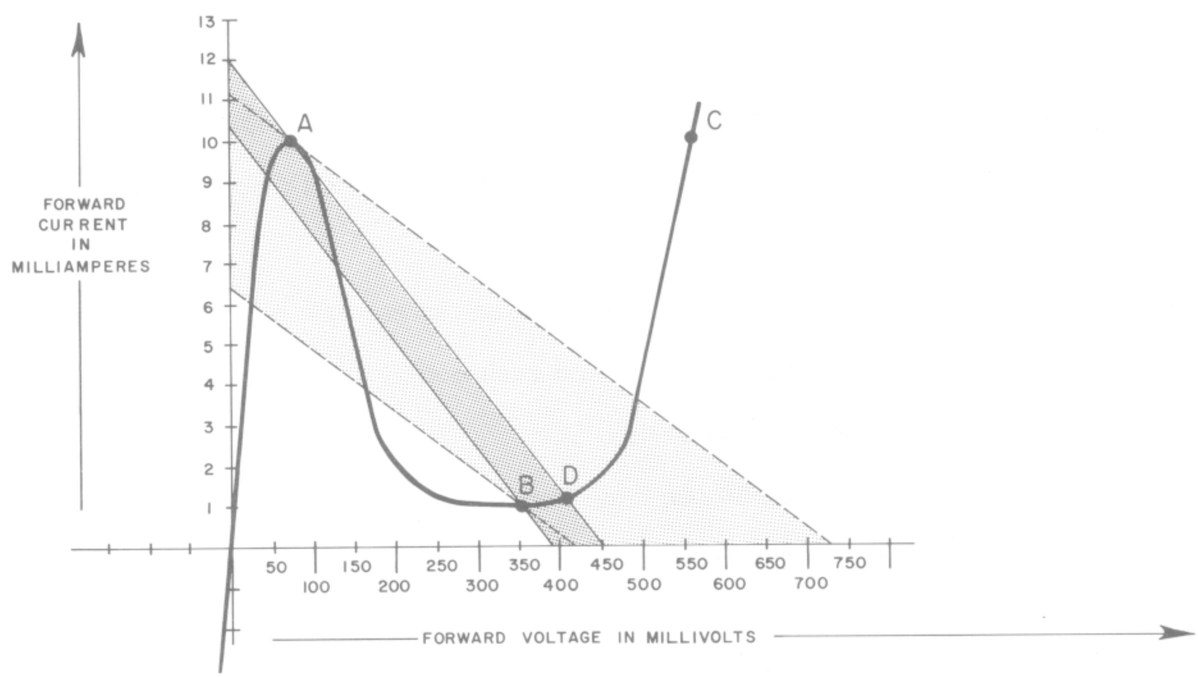
   a. R553 and R556 are the TD load.

4. A bistable tunnel diode has <u>current</u> hysteresis.

   a. The width of the hysteresis gap is determined by the TD load.

   b. The load resistance and, therefore, the width of the hysteresis gap can be controlled by the TRIGGER SENSITIVITY control.

5. Tunnel diode curve.



TD253 TUNNEL DIODE CURVE

D-12a-0003
3-18-'64 jg

a. The limits of the hysteresis gap can be represented by the load lines.

(1) The top of the hysteresis gap (point A) appears in the TD low voltage state.

(2) The bottom of the gap (point B) appears in the high state.

b. The slope of the load lines determines the width of the hysteresis gap.

(1) The setting of the TRIGGER SENSITIVITY control sets the slope of the load lines.

(2) The less the resistance, the steeper the slope.

c. The darker shaded area represents a relatively sensitive setting of the TRIGGER SENSITIVITY control (narrow hysteresis gap).

d. The lighter shaded area represents a relatively insensitive setting (wide hysteresis gap).

6. Current Distribution

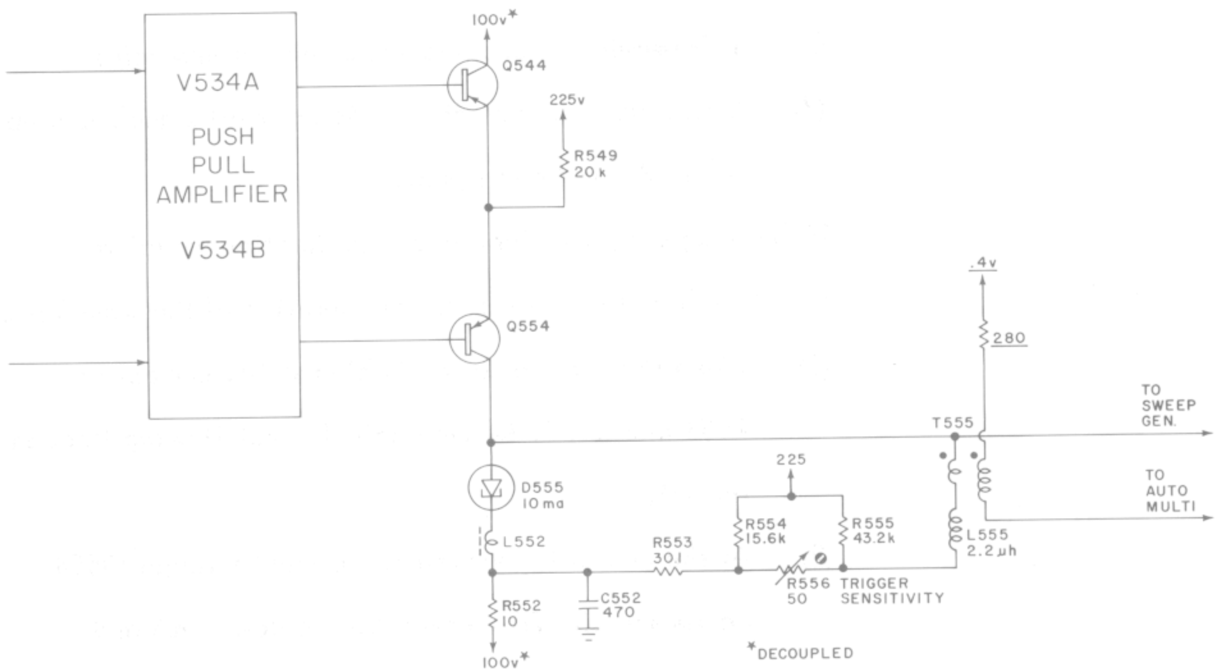
a. Q554 can draw from 0 to 6 mA from the TD circuit.

b. The current through R553 depends on whether the TD is in its low or high state.

c. About 5.5 mA flows through R553 when the TD is in its low state and about 15 mA in its high state.

d. The TD must draw a least 10 mA to flip it to its high state and less than 1 mA to flip it to its low state.

7. Assume the TD is in its low state awaiting a trigger.



TYPE 556 A SWEEP TRIGGER
TUNNEL DIODE CIRCUIT

B-556-0208
1-17-'66dl

a. The triggering waveform biases Q554 to greater conduction.

b. Increased current through the TD flips it to its high state.

(1) L555 presents a high impedance load momentarily and the TD flips to point C.

(2) The load line, as the TD switches, is essentially flat.

c. If the triggering waveform is a fast pulse, the TD flips back to its low state.

(1) The change from point C to point B on the TD curve is slowed by L555.

(2) This provides a count-down at high frequencies.

(3) Count-down begins at 1-5 Mc on small signals and up to 10 Mc on large signals.

d. If the triggering waveform is a long duration waveform, the TD will rest at point D for the duration of the waveform.

(1) When the TD flipped to its high state, current in R553 increased, leaving only 1.5 mA flowing through the TD.

(2) At the end of the waveform, current through Q554 decreases; the TD current drops below 1 mA and flips to its low state.

e. The circuit has returned to its quiescent state.

8. The output waveform is taken across the TD.

a. As the TD flips to its high state, the voltage appears across T555 primary as a step about 500 mV in amplitude.

b. The voltage drop across the TD raises to 560 mV (from 75 mV), then as L555 allows current to flow in the load resistance, the TD drops to point D.

(1) The result is a 100 mV overshoot.

c. The step (and overshoot) is differentiated in the Sweep Generator circuit.

(1) The result is a 2 ns pulse with a risetime of a 1/2 ns.

9. T555 secondary feeds the AUTO multi.

a. The waveform at T555 secondary is a negative going .8V pulse of about 700 ns duration with about 40 ns risetime.

10. L552 is a ferrite bead that keeps fast transients from flipping the TD.

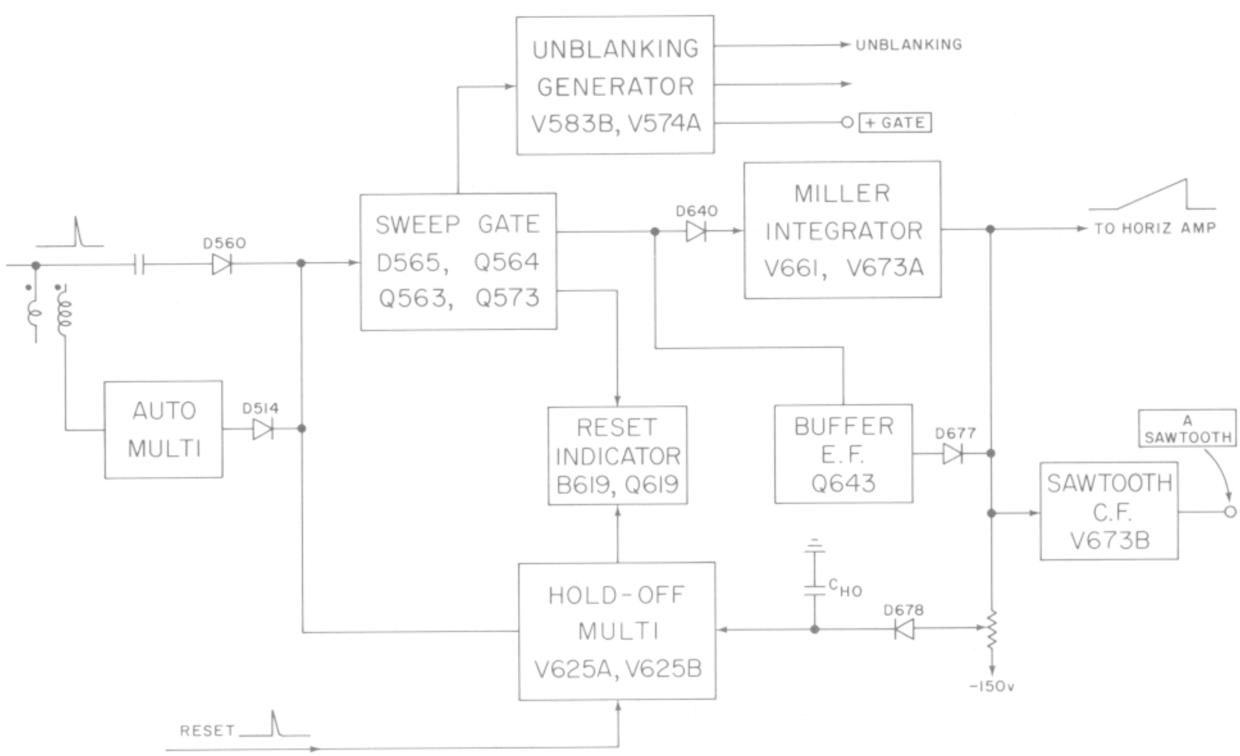
11. R552 and C552 provide decoupling.

IV. SWEEP GENERATORS

A. The A and B Sweep Generators are almost exactly alike.

1. The A sweep is the delaying sweep.
2. Identical sweep speeds.
3. Both generate 105V linear sweep ramps.
4. Both produce 10V gate waveforms at front panel jacks.
5. Both generate unblanking waveforms.
6. Both have sawtooth out waveforms at front panel jacks.
7. The A Sweep Generator will be described here.

B. Block Diagram



TYPE 556 A SWEEP GENERATOR
BLOCK DIAGRAM

B-556-0209
1-11-'66 mw

C. Basic Circuits

1. Sweep Gate
2. Miller Integrator
3. Hold-Off Multi
4. Unblanking Generator
5. Auto Multi
6. Reset Indicator
7. Buffer E.F.
8. Sawtooth C.F.

D. Improvements Over 555

1. Simpler controls.
2. Faster time from trigger to start of sweep.
3. Smaller physical size circuit layout - solid state circuitry where practical.
4. Lower power requirements - transistors.
5. Better reliability - transistors - precision resistors.
6. Better stability than older versions.

E. Block Logic

1. A positive going trigger flips the sweep gating TD to its high state.
2. The positive step generated by the TD is amplified and inverted in the Sweep Gating circuit and applied to the disconnect diode, D640.
3. D640 cuts off, allowing the Miller tube to begin its sweep ramp.
4. The positive going ramp is fed to the Horizontal Amplifier.
5. A portion of the ramp is picked off by the sweep length control and fed to the Hold-Off Multi.

6. When the sweep has reached sufficient length, the Hold-Off Multi flips.

7. As the Hold-Off Multi flips, it switches the sweep gating TD to a low state that cannot be influenced by a trigger.

8. The Disconnect Diode conducts and retrace starts.

9. At the start of retrace, the Hold-Off Diode opens.

10. The Hold-Off circuit (capacitor) delays the fall of the waveform, allowing retrace to finish and the sweep circuits to reach their stable state.

11. At the end of hold-off, the Hold-Off Multi flips and switches the sweep gating TD to its triggerable condition.

F. Sweep Timing Switches

1. The A and B timing circuits are the same in most respects.
    a. The B switch has a B Sawtooth Slope calibration control.

2. A VARIABLE control is provided for both A sweep and B sweep (variable time/cm).
    a. The controls provide a variable time increase of at least 2.5:1 (typically 3:1) over the calibrated sweep ranges.
    b. An UNCAL lamp lights when the VARIABLE know is turned away from its calibrated position.
        (1) The calibrated position is also indicated by a detent on the control.

3. Sweep timing components:
    a. Timing caps.
        (1) Timing positions from 1 sec to 5 sec use 10 µF Tek made dry polycarbonate caps.

(2) Positions .1 sec to .5 sec use 1 μF Tek made dry polycarbonate caps.

(3) Positions 10 ms to 50 ms use .1 μF Tek dry polycarbonate caps.

(4) Positions 1 ms to 5 ms use .01 μF Tek polycarbonate caps.

(5) Positions .1 ms to .5 ms use .001 μF Tek polycarbonate caps.

(6) Positions from 0.1 μS to 50 μS use variable caps.

b. Timing resistors.

(1) The timing resistors used in the 5 sec, .5 sec, etc., positions are 1% pyro film 7M resistors.

(2) All other resistors are 1% metal film resistors.

(3) R660A, B C, are matched for less than a 0.25% spread in tolerance.

(4) R660 D, E, F are matched for less than a 0.25% spread in tolerance.

(5) Grounding the top of the resistors not in use helps maintain a constant current through the VARIABLE control in all switch positions and ages all resistors equally.

c. Hold-off capacitors are 10% tubular caps.

G. A Sweep Generator

1. Sweep Gate

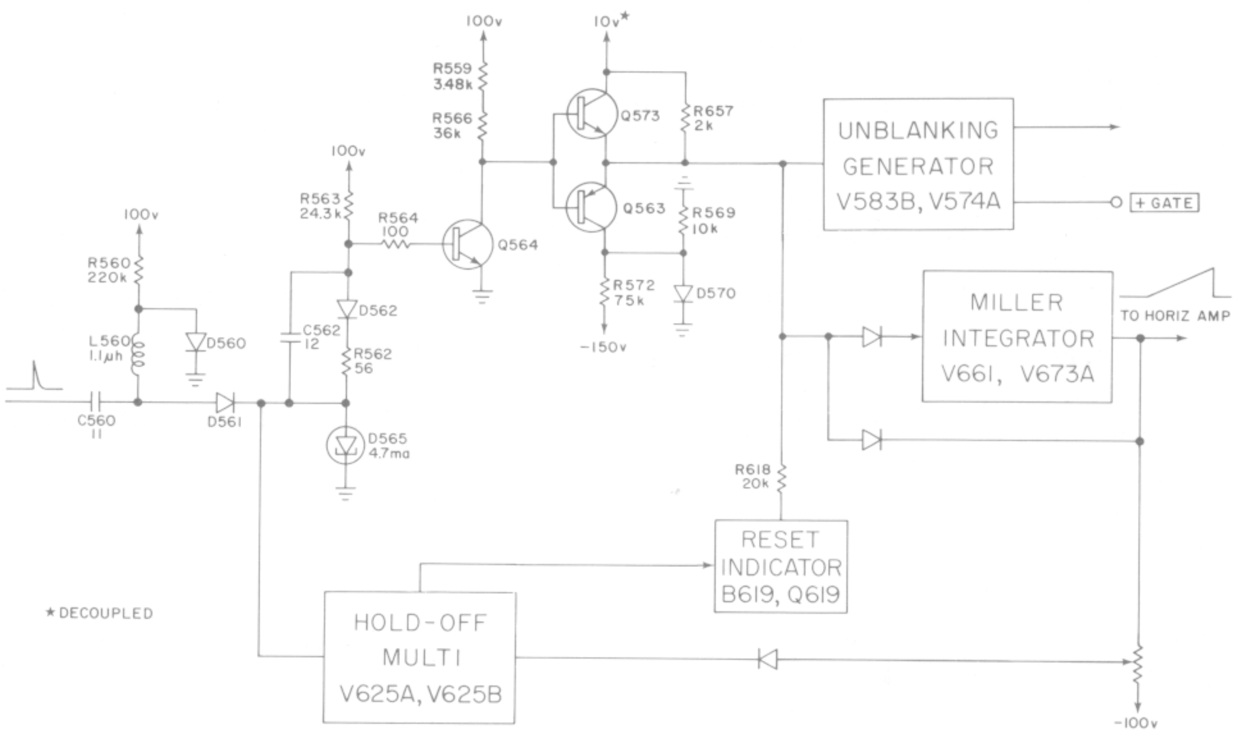
a. The sweep gate provides a negative going step to initiate sweep and a positive going step to stop it.

2. The circuit includes a tunnel diode and three transistors.

a. D565 is a 4.7 mA 152-0125 tunnel diode.

b. Q564 and Q573 are NPN silicon 2N3904 transistors.

c. Q563 is a PNP silicon 2N3906 transistor.



TYPE 556 A SWEEP GENERATOR
SWEEP GATE CIRCUIT

B-556-0210
1-14-'66 mw

3. The TD has three operating conditions controlled by the Hold-Off Multi and incoming triggers.

a. Triggerable state - the TD is in its low state with 3.6 mA forward current.

b. High state - a trigger will raise forward current to 4.7 mA and flip it to its high state with about 500 mV drop across the diode.

c. Locked out (low state) with a 3.2 mA reverse current.

4. Stable (triggerable) condition:

a. 3.6 mA forward current set by R559 and R563 flows through the TD.

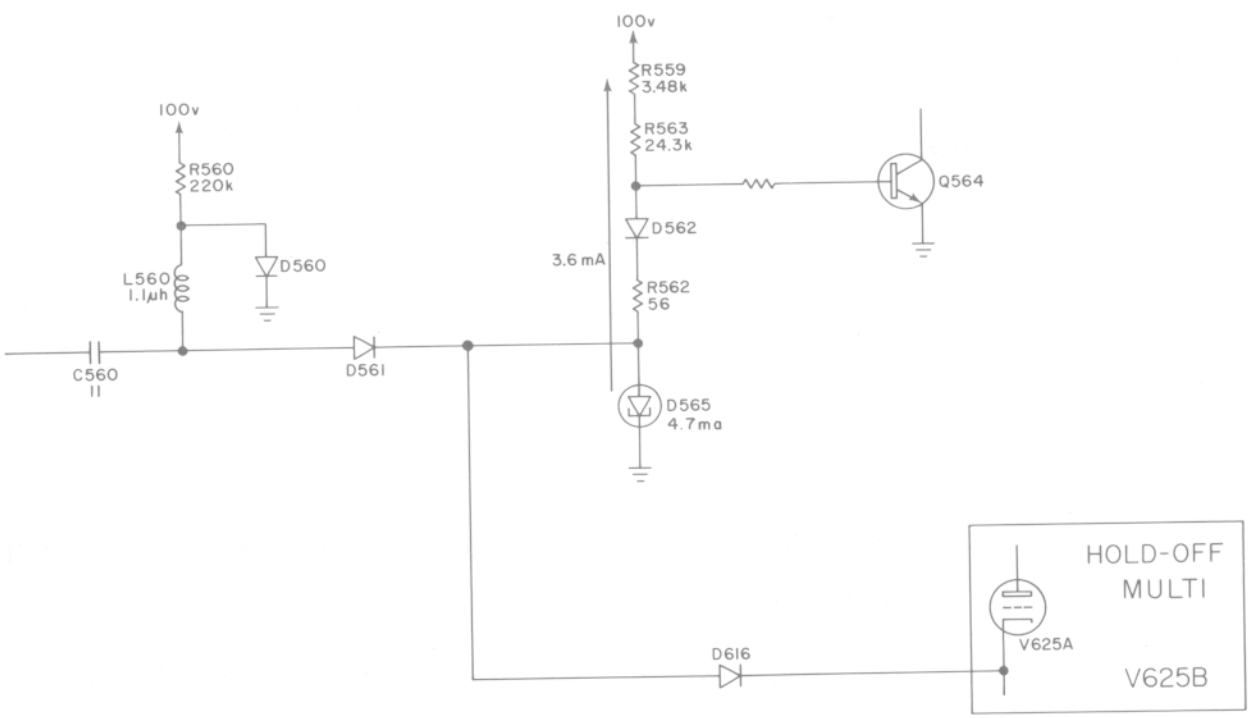
b. Q284 collector rests at 10.5 volts.

c. D561 is held near the edge of conduction by the voltage drop across D560.

5. A positive trigger will cause D561 to conduct.

a. The diode current added to the 3.6 mA already flowing through the TD will flip it to its high state.

b. Only 1.1 mA is required to bring the TD to its rated 4.7 mA.



TYPE 556 A SWEEP GENERATOR
SWEEP GATE CURRENT DISTRIBUTION NO. 1

B-556-0211.1
1-14-'66 mw

6. As the TD flips to its high state, Q564 saturates.

   a. Q564 is a silicon transistor which needs about 0.7V to turn it on.

      (1) D562 acts as a 0.3V zener combined with the voltage drop across R561 to achieve the required turn voltage for Q564.

      (2) C561 bypasses high frequency changes around D562 and R561.

TYPE 556 A SWEEP GENERATOR
WAVEFORMS

B- 556-0212
8-15-'66 df

b. The collector of Q564 drops to 0V from +10.5V.

c. The negative step is applied to the bases of Q573 and Q563.

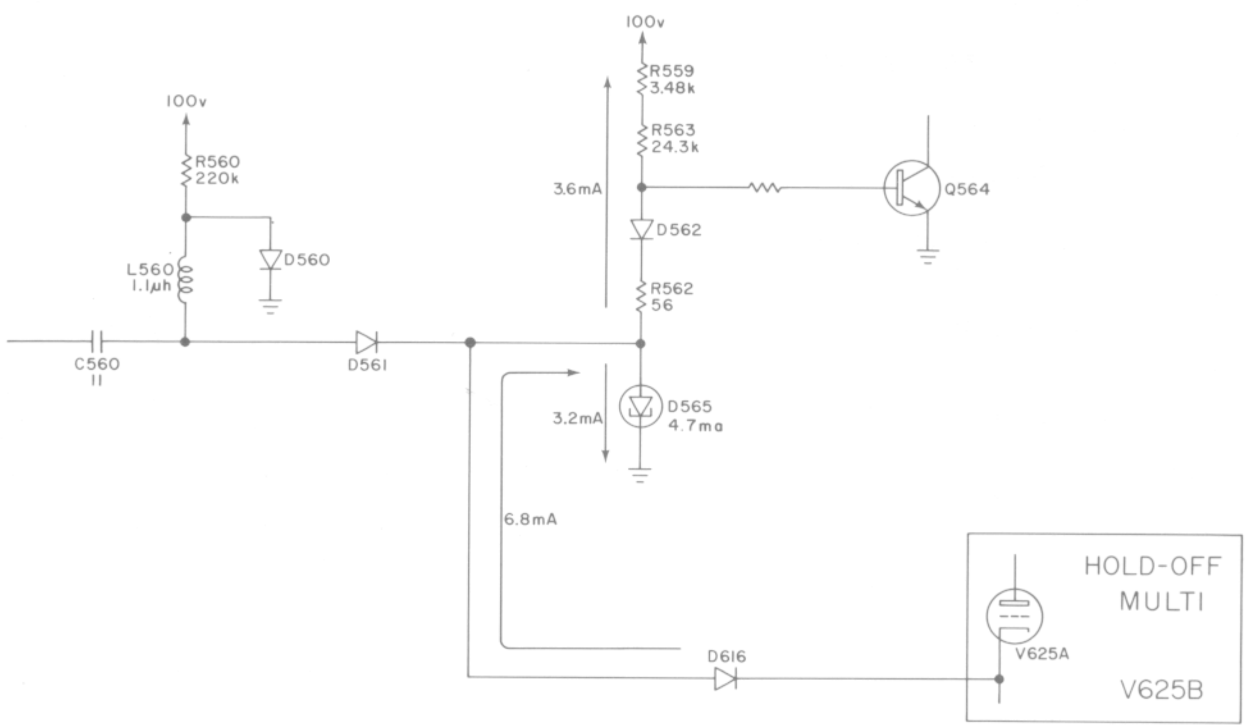
d. The negative step from the emitters of Q563, Q573 cuts off D640 starting the sweep.

7. At the end of trace, the Hold-Off Multi turns V625A off.

a. 6.8 mA now flows through R627 from the -150V supply through D616.

b. 3.2 mA of reverse current through D285 flips it to its low, locked out state.

c. A trigger cannot flip the TD to its high state.



TYPE 556 A SWEEP GENERATOR
SWEEP GATE CURRENT DISTRIBUTION NO. 2

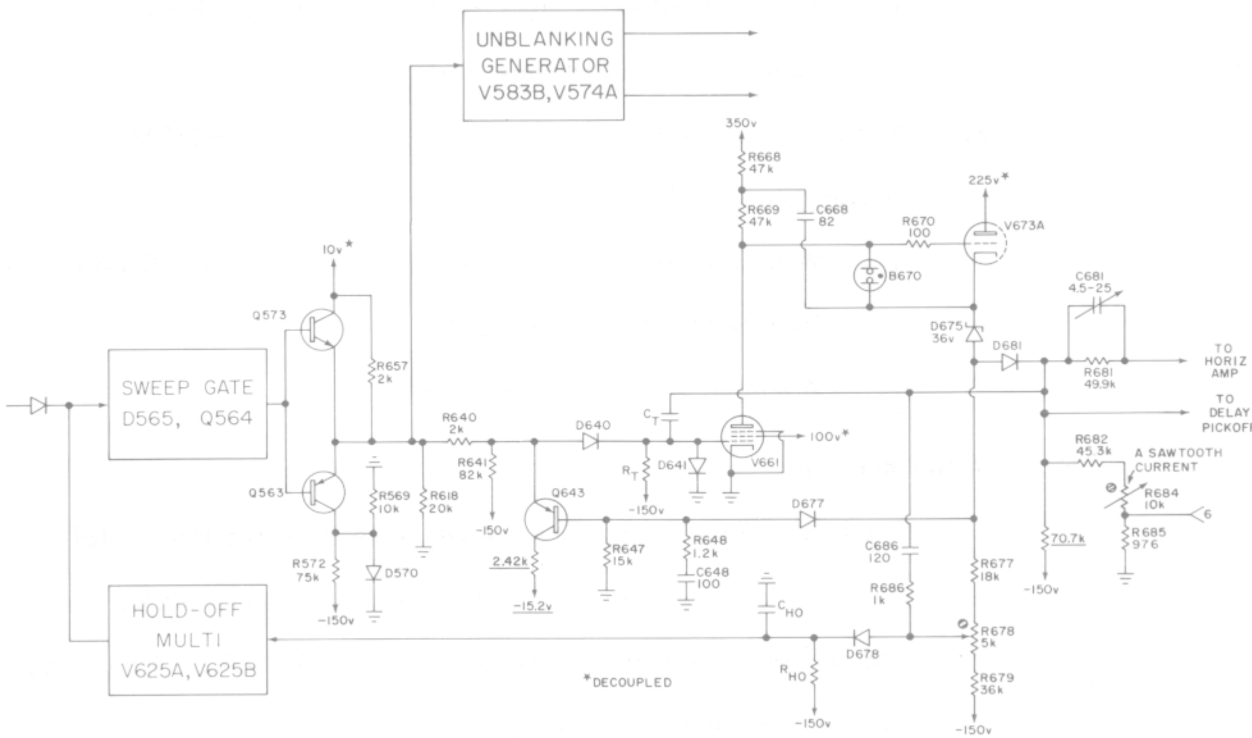
B-556-0211.2
1-14-'66 mw

8. As the TD flips to its low state, Q564 returns to its stable, unsaturated, condition.
    a. As Q564 collector rises to 10.5V, D640 conducts.
    b. Sweep stops and retrace starts.
9. At the end of hold-off, the current from the Hold-Off Multi ceases (blocked by D616).
    a. With 3.6 mA flowing from R559 and R563, the TD returns to its forward biased low state.
    b. A trigger will start a new cycle.

H. Miller Run-Up

1. The Miller Run-Up supplies the sweep ramp to the Horizontal Amplifier and the Sweep A voltage to a front panel jack.
2. The Miller circuit uses a 12AU6 tube, a half 6DJ8, a transistor, four diodes and a zener diode.
    a. The Miller tube (V661) is a 12AU6 pentode.
    b. The run-up cathode follower is 1/2 6DJ8.
    c. Q643 is a 2N3251 silicon 151-0188 PNP transistor.
    d. D640 is a GaAs Tek made diode.
    e. D641 is a selected 1N3579 silicon diode.
    f. D677 and D681 are Tek spec 152-0061 silicon diodes.
    g. D675 is a Motorola 1N3033 20% 36V zener.

3. In the stable state, the tubes, diodes, and transistor are conducting.



TYPE 556 A SWEEP GENERATOR
MILLER INTEGRATOR

B-556-0213
1-17-'66 mw

a. V661 grid rests at -1.7V.

b. V661 plate rests at about 26V.

c. The output at D681 is about -3V.

4. A DC feedback loop composed of D640, V661, V673A, D677, and Q643 assure a consistent, stable starting potential for the sweep.

a. By using Q643 as a current amplifier, only the base current needs to be switched by D677.

b. Actual clamping current flows through Q643 collector.

c. A step at the beginning of fast sweeps is minimized.

5. The 10V negative step from the Sweep Gate cuts off the disconnect diode, D640 and Q643.

a. D641 protects D640 from excessive reverse voltage.

6. Sequence of operation at start of sweep.

a. With D640 open, the Miller tube grid starts toward -150V, charging the timing cap (C_T) through the timing resistor (R_T).

(1) Different values of precision timing resistors and precision Tek made timing capacitors are switched with each time/cm range.

b. The Miller tube plate begins to run up.

c. The ramp waveform is fed back to the top of the timing capacitor.

d. The positive going change at the top of the capacitor opposes the change at the bottom (grid end) of the capacitor.

e. As a result of the feedback action, the Miller tube grid runs down less than 500 mV.

f. Since the voltage drop across the timing resistor remains virtually the same, the charging current into C_T remains constant.

g. Because a constant charging current into a capacitor results in a linear ramp of voltage across the capacitor, the output ramp is linear.

7. V673A provides a low impedance to charge C_T and drive the sweep out CF.

   a. B670 protects V673A during turn-on and if V661 is removed from its socket or fails.

   b. D675 allows normal operating plate voltage for the Miller tube (V661) when the DC output level is 0V.

8. Bootstrap capacitor C668 improves gain at high sweep speeds and assures sweep linearity.

9. Sequence of operation at the end of sweep.

   a. The positive step from the Sweep Gate turns on D640 and Q643 after a brief delay.

   b. When D640 conducts, the Miller tube grid rises to its stable, no sweep condition.

   c. The Miller tube plate pulls down and retrace starts.

   d. C_T discharges through D640, R640.

   e. D681 disconnects, allowing retrace to continue while the loop composed of D677, Q643, D640, V661, and V293A becomes connected.

      (1) The Miller circuit and the clamping loop reach their quiescent condition before retrace is finished.

10. The positive going output sweep ramp rises from near 0V to about 150V to drive the Horizontal Amplifier.

    a. The Horizontal Amplifier input is an operational amplifier.

b. R681 is R_{in} for the Operational Amplifier.

c. The output, as it feeds through the 50Ω coax, is a current waveform.

11. The Sweep Length Control picks off a portion of the sweep ramp to feed the Hold-Off circuit.

    a. The ramp at the Sweep Length arm runs from about -55V to +15V.

    b. R676, C676 compensate the Sweep Length divider.

I. Hold-Off Circuit

1. The Hold-Off Multi provides a change of current that flips the Sweep Gating TD to its low state, stopping sweep. It also delays arming the Sweep Gating TD until retrace is finished and the Miller circuit has become stabilized.

2. The Hold-Off circuit consists of the Hold-Off diode, the Hold-Off resistors and capacitors, and the Hold-Off multi.

3. A dual triode and three diodes are used in the circuit.

    a. V625A and V625B are two halves of a 6DJ8.

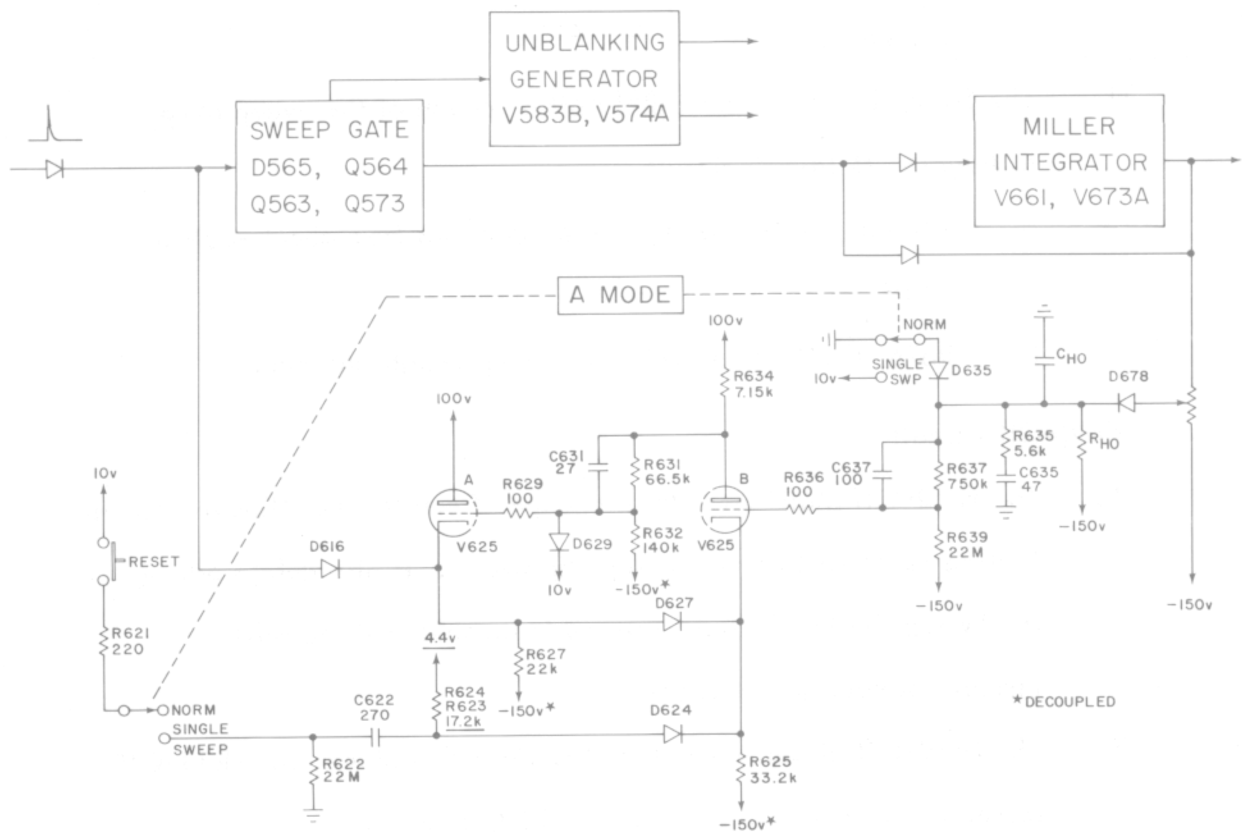
    b. D627 and D635 are GE 1N3605 silicon 152-0185 diodes.

    c. D678 is a 152-0061 silicon diode.

4. V625A and V625B form a bistable Schmitt multi.

5. In the steady state (the Sweep Gating TD armed waiting for a trigger), V625A is conducting and V625B is cut-off.

6. Steady state DC levels - V625A and V625B:



TYPE 556 A SWEEP GENERATOR
HOLD-OFF MULTI

B-556-0214
1-17-'66jg

a. V625A grid - pin No. 2, +10V.

b. V625A cathode - pin No. 3, +12V.

c. V625A plate - pin No. 1, +100V.

d. V625B grid - pin No. 7, -5V.

e. V625B cathode - pin No. 8, +11V.

f. V625B plate - pin No. 6, +90V.

7. With V625A cathode at 12V, D616 is back biased allowing no current to flow to the TD, D565.

8. The Hold-Off Multi remains in its stable state until the sweep ramp has reached its required amplitude.

9. The portion of the sweep ramp picked off the Sweep Length control has a range of -55 to about +15V.

10. The Hold-Off bus is clamped to ground by D635.

    a. The Hold-Off bus cannot go negative.

    b. D678, therefore, is cut off until the sweep waveform on its anode reaches 0V.

    c. D635 cuts off and the voltage on the bus rises to 15V charging the Hold-Off capacitor, C678, to this potential.

11. A voltage divider composed of R637 and R639 drops the DC level of the ramp until it has a range of from +8V to -5V.

12. V625B cathode is held at 11V by current through D627.

    a. Cut off bias is about 4V.

    b. When the grid reaches 3V the tube begins conduction.

13. The multi flips as V625B turns on and V625A turns off.

14. With V624A off, its cathode drops to about -1V.

    a. D627 cuts off, leaving R627 to supply reverse current through D565 via D616.

    b. 6.8 mA flows through D616 to the TD circuit.

c. This current forces 3.2 mA of reverse current through the TD, flipping it to its low state stopping the sweep.

d. The TD is in its locked out condition.

TYPE 556 A SWEEP GENERATOR WAVEFORMS

B-556-0212
8-15-'66 df

15. V625B plate pulls down to 60V.

a. V625A grid drops to -8V as D629 cuts off.

16. As retrace starts and the voltage at the sweep length control starts down, D678, the Hold-Off diode, cuts off.

a. The Hold-Off capacitor C678 holds D678 cathode to a slower voltage change, allowing the diode to disconnect.

b. The charge on C678 leaks off slowly through R675, the Hold-Off resistor, providing Hold-Off delay.

(1) Hold-Off capacitors and Hold-Off resistors are switched with settings of the TIME/CM control.

(2) On sweep ranges of 5 μs or faster, C635 becomes the Hold-Off capacitor.

(3) During fast sweeps, R635 keeps C635 from delaying the sweep range.

17. As the Hold-Off waveform drops V625B grid in a negative direction, its plate rises and its cathode runs down.

18. When V625A cathode reaches 4.4V, D624 conducts.

19. As V625B cathode reaches -1V, D627 conducts.

a. V625A grid has risen to -3V.

b. Conducting D627 pulls V625A cathode into conduction.

20. The Hold-Off Multi flips.

a. V625A turns on and V625B cuts off.

b. The circuit has returned to its steady triggerable state.

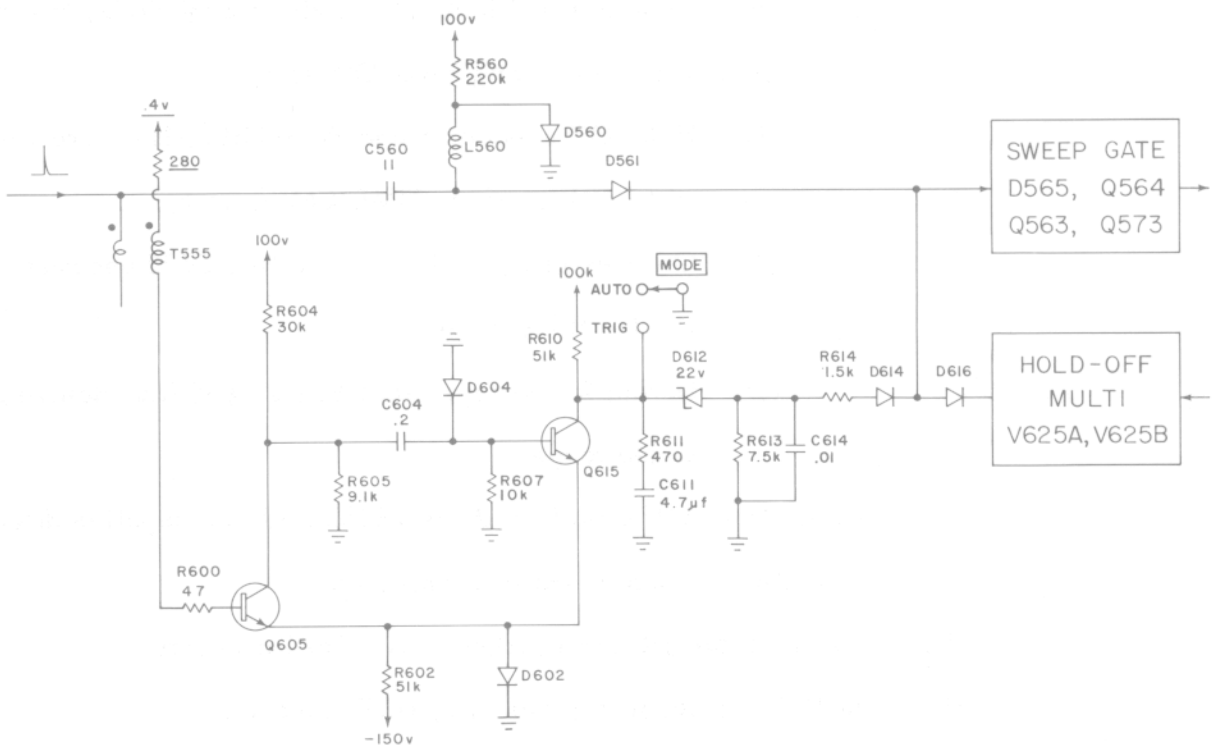
J. Auto Circuit

1. In the absence of triggers, the Auto circuit allows the Sweep circuit to free-run at a rate set by the TIME/CM switch.

a. The feature is called the "Bright Line Automatic".

2. When triggers arrive at a rate of 30 Hz or more, the sweep circuit is automatically switched to the triggered mode.

3. The condition when no triggers are present and the AUTO-TRIG switch is in the TRIG mode.



TYPE 556 A SWEEP GENERATOR
AUTO MULTI

B-556-0215
1-17-'66jg

a. The Sweep Gate TD is armed with a 3.6 mA forward current through the diode.

b. The Hold-Off Multi is in the armed condition, V625B cut off, V625A conducting.

c. There is no sweep.

4. The condition when the AUTO-TRIG switch is in the Auto mode and no triggers are present.

a. D614 is conducting.

b. About 1.2 mA flows through the diode.

c. The 1.2 mA comes from the TD.

d. Added to the quiescent TD current of 3.6 mA, this current will flip the TD to its high state and start the sweep.

e. After hold-off, when the Hold-Off Multi returns to its stable state, the TD will flip to its high state and begin a new sweep.

g. The circuit will continue to free run.

5. The Auto Multi is a transistorized monostable multi.

   a. Q265 and Q375 are silicon, 2N3904 NPN transistors.

   b. D602, 604, 614 are 1N3605 silicon diodes.

   c. D612 is a 1N969A, 10% 22V zener diode.

6. In the stable state (no triggers arriving), Q605 is conducting and Q615 is cut off.

   a. Q605 is tied through an equivalent 279Ω to an equivalent 0.4V.

   b. Q615 base is returned to ground through R607.

7. When the AUTO-TRIG switch is in the AUTO position, a divider is formed of R610, D612, and R613.

   a. 1.2 mA flows through R614 and D614 to keep the sweep free running.

8. When a negative going trigger arrives, Q605 cuts off.

   a. The multi flips to its unstable state.

   b. Q605 is cut off and Q615 conducts.

   c. Q615 collector pulls down to 1V.

   d. The collector level is transmitted through the 20V zener to cut off D614.

   e. The Auto circuit is disconnected from the Sweep Gate.

   f. The Sweep Circuit functions in the normal triggered mode.

9. The Multi remains in its unstable condition for about 6 ms.

   a. The time constant is determined by C604 and R607.

   b. While the multi is in the unstable state, C611 discharges from 23 volts to about 5 volts.

      (1) Faster trigger rates will discharge C611 to voltages less than 5 volts.

10. When the multi returns to its stable state, C611 begins to charge toward 100V.

    a. If no trigger has arrived by the Time C611 has charged to 23 volts, D614 will conduct.

    b. The sweep system will free run.

    c. If a trigger arrives within 55 ms, the Auto Multi will recycle.

    d. C611 will not charge high enough to allow D614 to conduct.

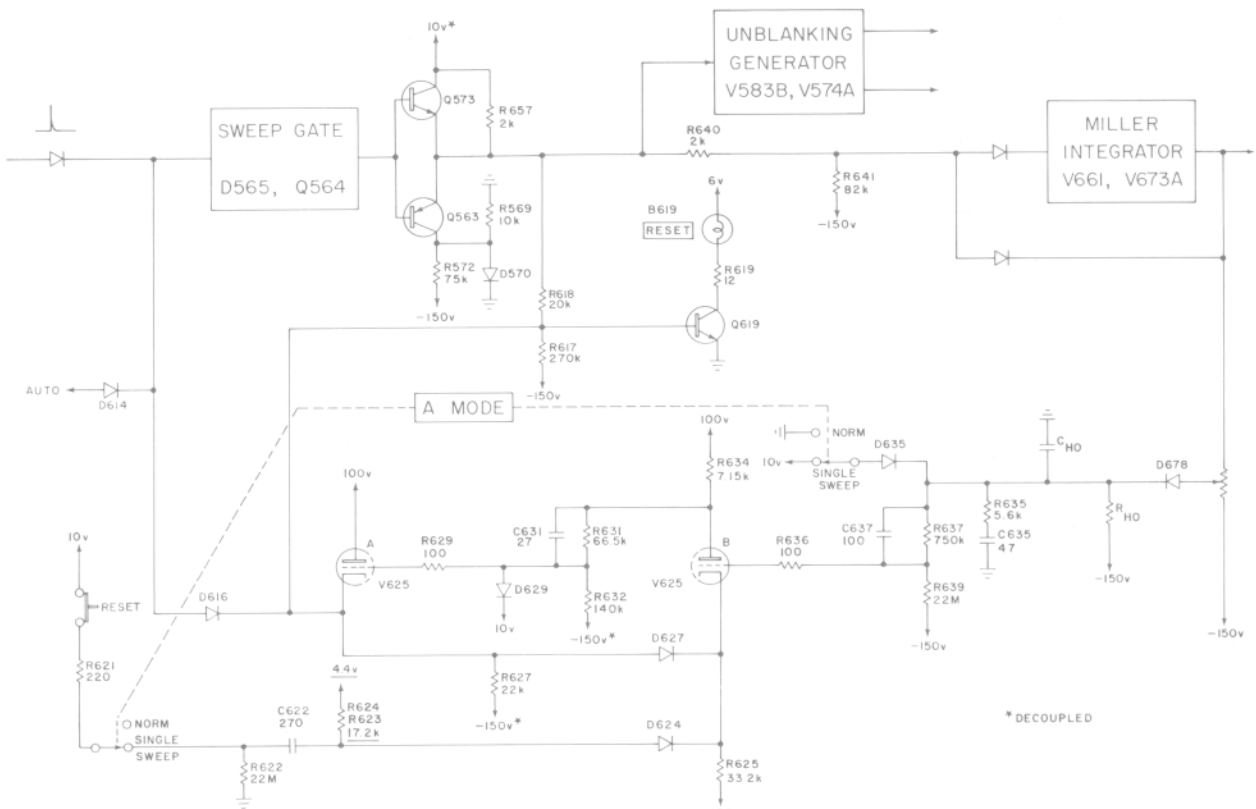
    e. As long as D614 remains cut off, the sweep will not free run.

K. Ready Light Circuit

1. The Ready Light indicates that the sweep circuit is ready to accept a trigger.

   a. The Ready Light, B619, lights when the sweep gating TD is in its low state and the Hold-Off Multi is in its quiescent state (625B cut off).

   b. It extinguishes as soon as the sweep starts.



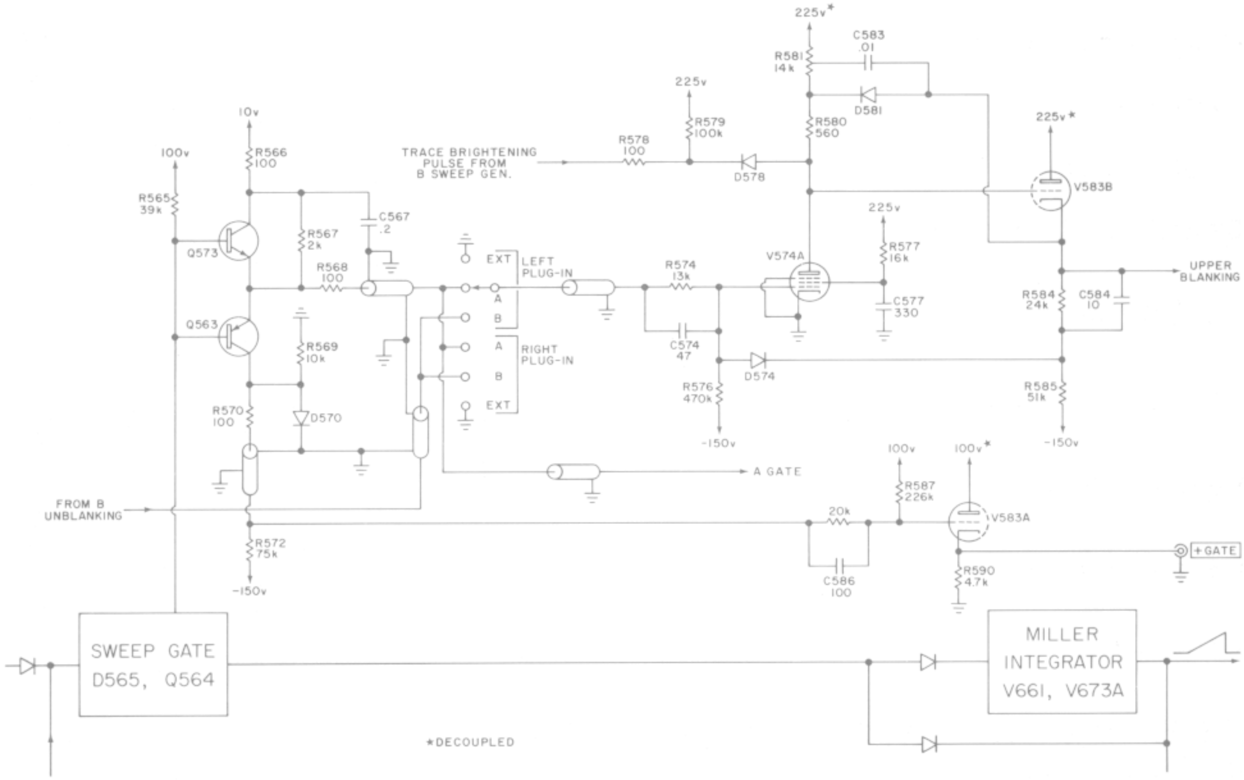
TYPE 556 A SWEEP GENERATOR
SINGLE SWEEP

B-556-0216
1-19-'66jg

2. The circuit is a transistor and a light.
   a. Q619 is a 2N2924 silicon NPN transistor.
   b. B619 is a No. 683 5V, 50 mA incandescent bulb.
3. The Ready Light driver transistor (Q619) will conduct only when V625B is cut off and Q573 emitter is at +10V.
   a. The circuit can be considered an AND gate.
4. When a trigger arrives, the TD flips into its high state, biasing Q619 into saturation.
   a. Sweep starts.
   b. Q573 emitter goes negative.
   c. Q619 base goes negative.
   d. Q619 collector rises.
   e. The ready light goes out.
5. At the end of sweep, the Hold-Off Multi flips, bringing V625B into conduction.
   a. Q619 base is pulled down to cut-off as V625A cathode goes to -1V.
   b. The TD goes into its reverse bias condition.
   c. Q573 emitter goes positive.
   d. Q619 base is pulled positive but not far enough for conduction.
6. At the end of hold-off, the Hold-Off Multi flips back, turning on V625A.
   a. V625A cathode rises to +12V bringing Q619 into conduction.

b. The TD goes into its stable state awaiting a trigger.

c. The Ready Light lights.



TYPE 556 A SWEEP GENERATOR
UNBLANKING GENERATOR

B-556-0217
2-8-'66 mw

L. Unblanking and Gate Amplifier

1. The circuit provides a positive going unblanking waveform and a +Gate A waveform with the same duration as the sweep.

a. The unblanking waveform is about 60V peak-to-peak.

b. The Gate A waveform has an amplitude of more than 10V peak-to-peak.

2. V583A and V583B are each one-half 6DJ8.

TYPE 556 A SWEEP GENERATOR WAVEFORMS

B-556-0212
8-15-'66 df

3. V574A is one section of a 6M11.

4. D578, D581, and D574 are 152-0061 silicon diodes.

5. The condition prior to sweep:

   a. Q564 collector, 10.5V.

b. Q573 emitter, 9.5V.

c. Q563 collector, -15V.

d. V583A grid pin No. 2, -5V.

e. V574A pin No. 2, -0.8V.

f. V583B cathode pin No. 8, 60V.

6. Condition during sweep:

a. Q564 collector, 0V.

b. Q573 emitter, +0.5V.

c. Q563 collector, +0.5V.

d. V583A grid pin No. 2, +8.5V.

e. V574A grid pin No. 2, -3.2V.

f. V583B cathode pin No. 8, +135V.

7. Prior to sweep, Q564 and Q563 are cut off, Q573 is conducting.

a. Q573 provides a low impedance drive to V574A which is located in the HV oscillator compartment.

8. V583A is cut off with its grid at -5V and the cathode at ground.

9. V574A is conducting.

a. The grid is at -0.8V set by current through D574.

(1) D574 conduction sets the lower unblanking waveform level.

b. V574A plate voltage rests at about 49V with no sweep.

10. Sequence of operation as sweep begins.

    a. D565 goes to its high state.

    b. Q564 saturates.

    c. Q563 turns on, its collector rising until D570 conducts.

    d. Q573 emitter drops to 0.5V cutting V574A off.

    e. As V574A grid goes negative, D574 disconnects.

    f. V574A plate rises quickly aided by bootstrap capacitor C581.

    g. V574A plate rises until D578 conducts from low impedance source, Q793 emitter.

        (1) D578 sets positive unblanking waveform level.

        (2) D581 allows V574A to pull V583B cathode negative quickly as unblanking waveform ends.

11. When sweep ends V574A plate runs down until D574 again conducts.

    a. C584 compensates R584, R585 divider for correct unblanking waveform termination.

12. When Q563 conducts as sweep begins:

    a. Q563 collector goes positive to 0.5V from -15V.

    b. V583A conducts and its cathode runs up to about +10V forming the +A Gate.

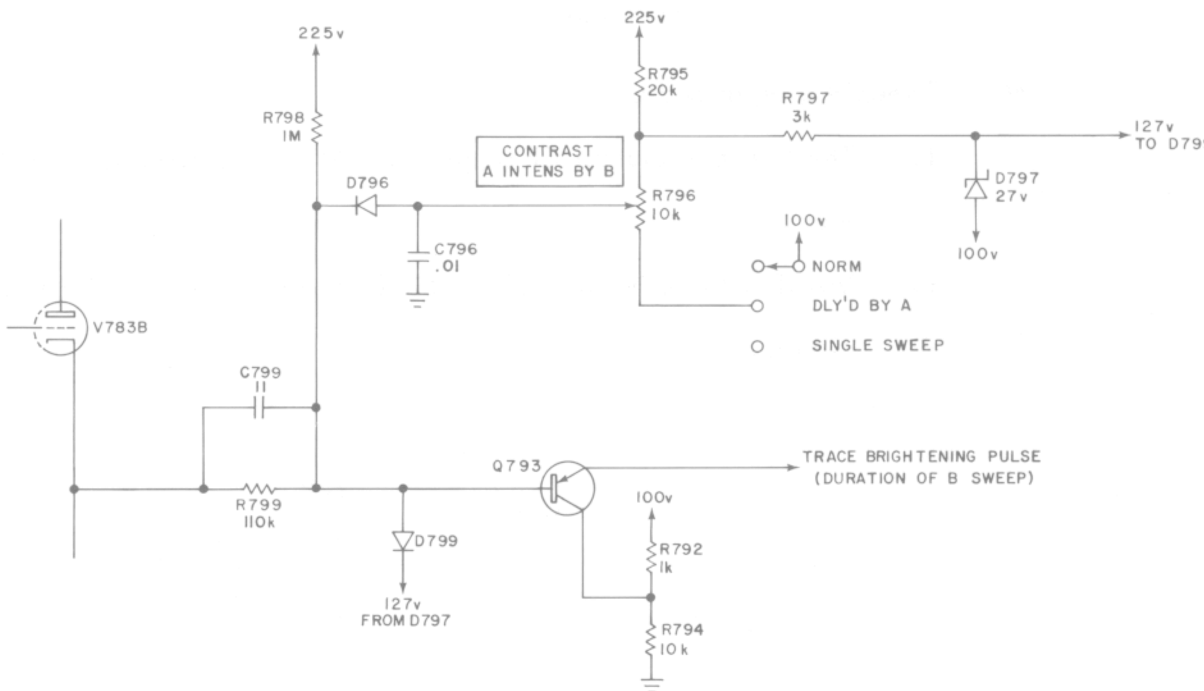
        (1) Output impedance is about 200Ω.

        (2) Plate current ratings will be exceeded at low sweep speeds if the output is shorted.

13. Delayed sweep unblanking:

a. Delayed sweep unblanking has a contrast control.

b. CONTRAST A INTENS BY B allows A sweep to be set at a level less than normal brightness.



TYPE 556
DELAYED SWEEP TRACE INTENSITY

B-556-0218
7-26-'66df

c. B intensification will appear at normal brightness.

d. Current through D796 sets EF Q793 output from +100 to +127V as R796 is varied.

(1) Output level from Q793 sets D578 plate catching diode level which limits A sweep unblanking waveform level.

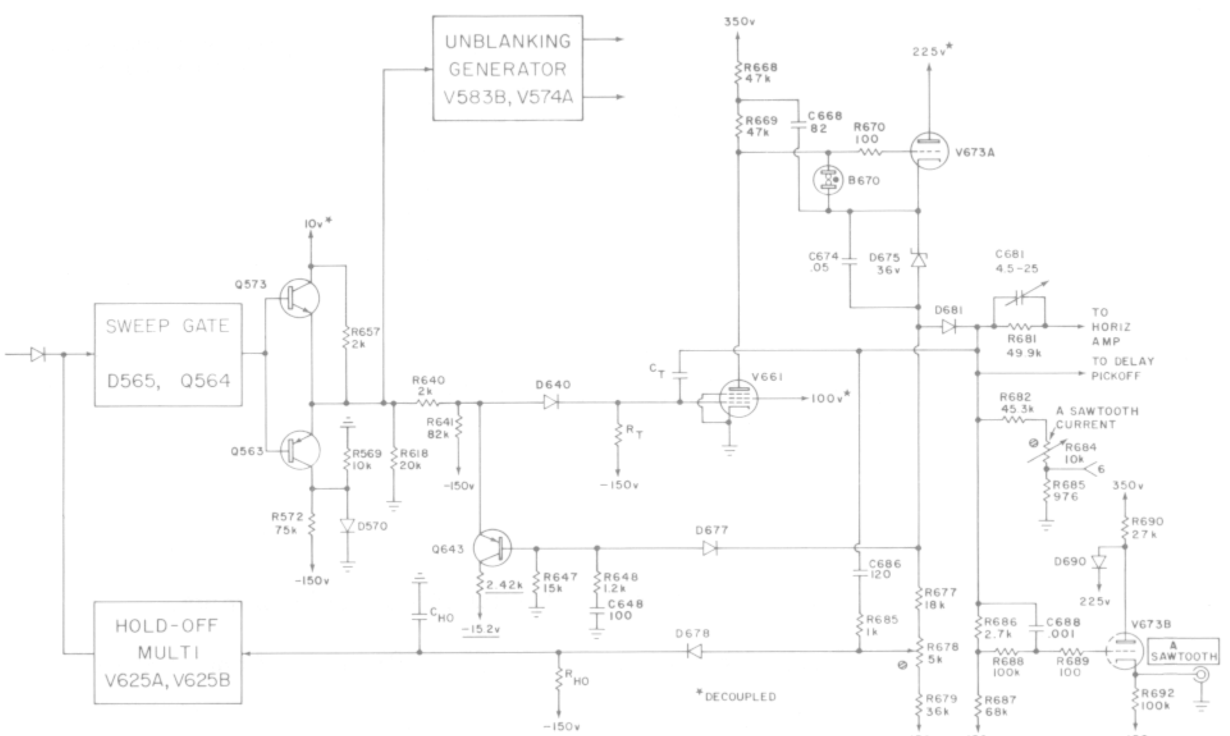
c. Positive B unblanking waveform causes D796 to disconnect allowing Q793 base voltage to follow B waveform positive until D799 limits swing.

(1) Duration of B waveform appears as a brightened portion of sweep.

M. Sweep A Output and CF

1. The Sweep A Output CF supplies a 100V sweep ramp to a front panel jack.

2. V673B is the other half of the 6DJ8 used in the run-up CF in the sweep circuit.



TYPE 556 A SWEEP GENERATOR
A SAWTOOTH OUT

B-556-0219
1-20-'66jg

3. Output impedance is about 100Ω.

4. The divider composed of R686 and R687 places the start of the ramp at 0V.

5. R688 limits grid current if the output is shorted to ground.

   a. D690 sets plate voltage at +225V.

   b. In case of an output short, D690 will decouple and limit plate current to a safe amount.

6. R682, R684, and R685 set sawtooth input to spectrum analyzer plug-ins.

N. Single Sweep

1. Single Sweep mode is selected by a front panel level wafer switch.

   a. Two positions: normal, single sweep (B has 3 positions).

   b. A push button is used for RESET.

2. Two modes of SINGLE SWEEP are available.

   a. Manual RESET in the Auto mode.

   b. Manual RESET in the Triggered mode.

3. The Single Sweep function of the sweep circuit utilizes the operation of the Hold-Off Multi.

4. Switching the SINGLE SWEEP mode switch to SINGLE SWEEP places the Hold-Off Multi in its "locked out" condition.

   a. D635 ties to +10V.

   b. V625B grid is lifted by D635 to 4V.

   c. V625B conducts, V625A is cut off.

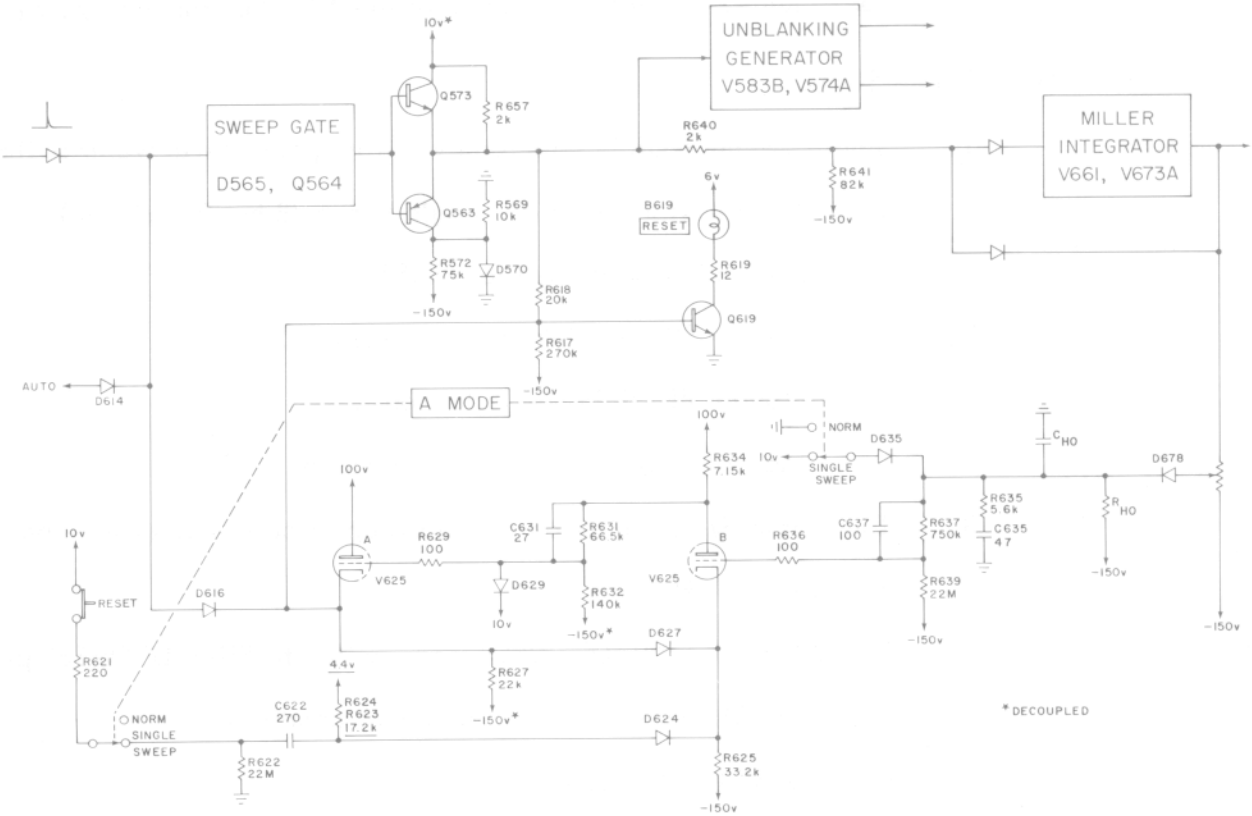
d. V345B cathode is at 5V.

e. D362 and D363 are cut off.

5. SINGLE SWEEP condition in the AUTO mode.

a. D614 is conducting.

b. When the Hold-Off Multi flips, sweep will start without waiting for a trigger.



TYPE 556 A SWEEP GENERATOR
SINGLE SWEEP

B-556-0216
1-19-'66jg

6. When the RESET button is pressed, a positive going pulse is generated.
   a. The pulse turns on D624.
   b. V625B cathode is lifted out of conduction.
   c. The Multi flips (V625A conducting, V625B cut off).
   d. The Sweep Gating TD flips to its high state and sweep starts.
7. At the end of sweep, the Hold-Off Multi will flip as in normal operation.
8. As the Hold-Off waveform drops, V625B, D635 conducts.
   a. Hold-Off cannot be completed.
   b. V625B stays in conduction.
   c. The circuit remains locked out.
   d. The circuit has delivered one single sweep.
9. SINGLE SWEEP condition in the TRIG mode.
   a. D614 is cut off.
   b. When the Hold-Off Multi flips, the Sweep Gating TD is armed and will flip to its high state with the arrival of the first trigger.
10. As in Auto mode operation, the RESET pulse lifts V625B cathode to cut-off and flips the Hold-Off Multi.
   a. The Sweep Gating TD has 3.6 mA forward current flowing.
   b. The TD is in its armed state.
   c. The READY LIGHT lights.
   d. Arrival of the first Trigger will flip the multi and start sweep.

11. At the end of sweep, the Hold-Off Multi will flip, stopping sweep as in normal operation.

    a. The READY LIGHT goes out.

12. The circuit is locked out at the end of a single sweep and will not respond to a trigger.

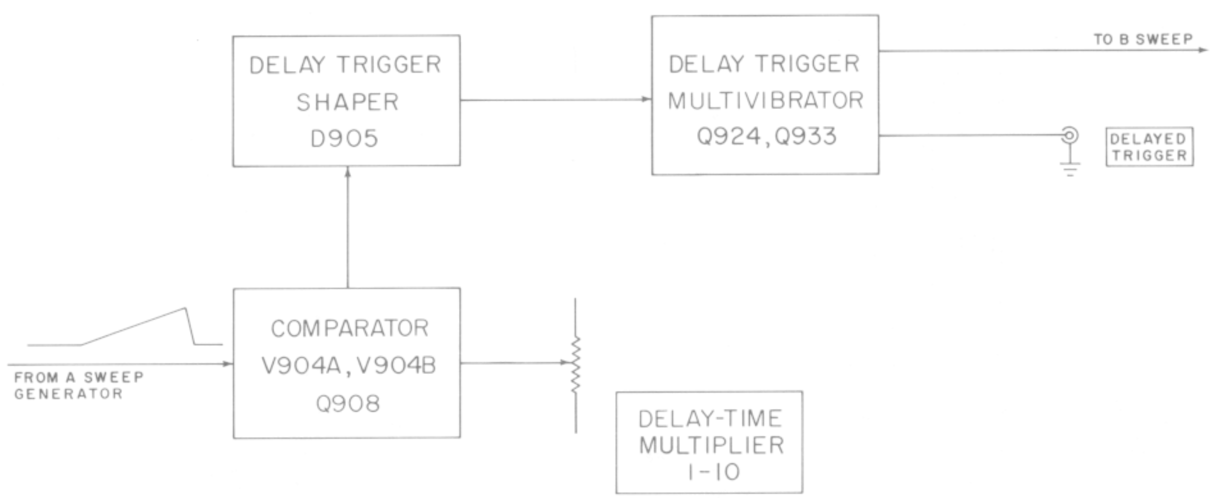
13. Another reset pulse will arm the circuit.

V. DELAY PICK-OFF

A. The Delay Pickoff provides a delayed trigger pulse to the B Sweep Generator.

1. The delay time is calibrated.
2. A DLY'D TRIG is available at a front panel jack whenever A sweep is running.
3. The delayed trigger pulse is fed to the B Sweep Generator only in the B DLY'D BY A mode.

B. Block Diagram



TYPE 556 DELAY PICKOFF
BLOCK DIAGRAM

B-556-0220
1-18-'66dl

C. Block Logic

1. The 100V sawtooth from the A Sweep Generator is fed to the comparator circuit.

2. After a delay controlled by the DELAY TIME MULTIPLIER, a step appears at the comparator output.

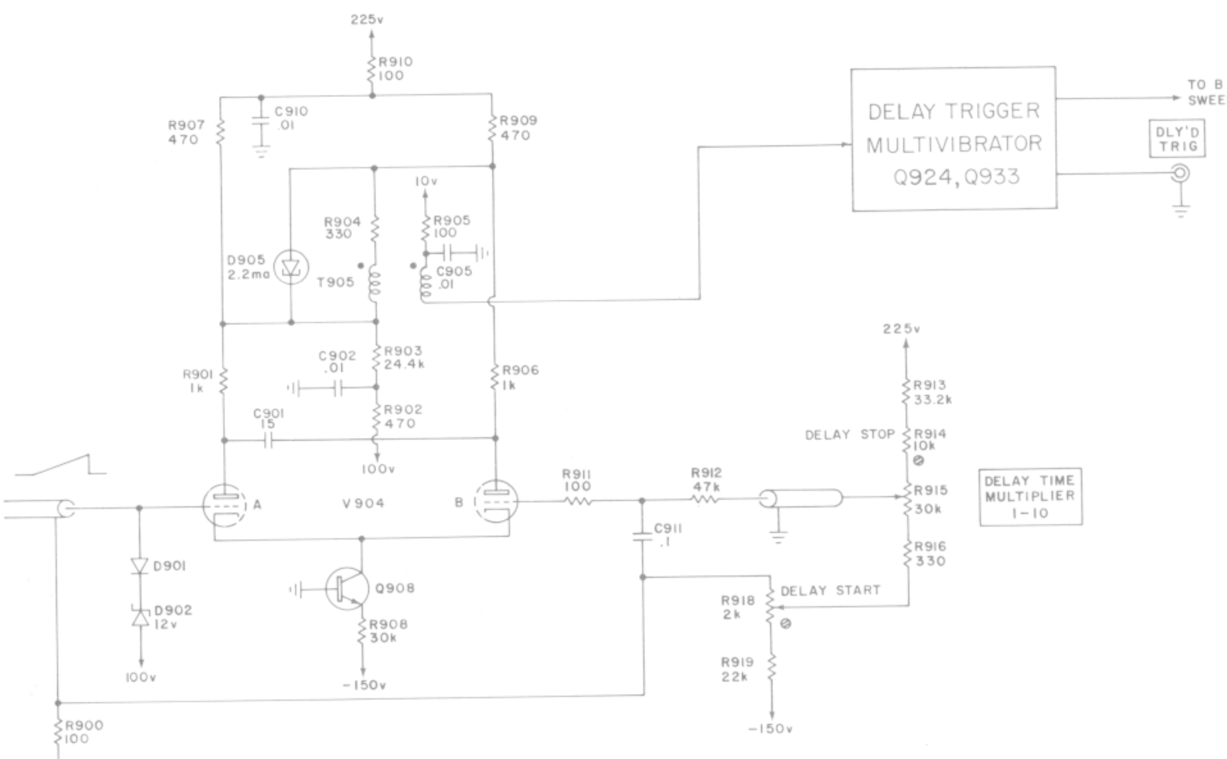
3. The step is regenerated in the Delayed Trigger Multi.

4. The positive going delayed pulse trigger is about 10V peak-to-peak.

5. The positive going pulse goes to the A Sweep Generator.

D. Comparator

1. The comparator provides a negative going step delayed a calibrated time after the start of B Sweep.



TYPE 556 DELAY PICKOFF
COMPARATOR & DELAY TRIGGER SHAPER

B-556-0221
1-21-66jg

2. The circuit uses two triodes, a transistor, and a tunnel diode.
   a. V904A and V904B are two halves of a 6DJ8.
   b. Q908 is a constant current regulator.
   c. D905 is a 2.2 mA tunnel diode.
3. The positive going 100V A sweep is applied to V904A grid.
   a. The A sweep ramp starts at about -2V.
   b. Depending on sweep length and sweep speed, the ramp amplitude will vary from 110V (10.5 cm) to 135V at fast sweep speeds.
4. The DELAY TIME MULTIPLIER sets the level on V404B grid.
   a. The DELAY TIME MULTIPLIER is a 10 turn Helipot with a resistance of 30k.
      (1) Resistance tolerance is ±3%.
      (2) Linearity is ±.1%.
   b. Properly calibrated, the control has a range of from -2V to 100V.
      (1) DELAY START adjust can vary the start from -5V to +1V.
      (2) DELAY STOP can vary the stop from 93V to 107V.
      (3) There is interaction between DELAY START and DELAY STOP adjust.
5. The constant current transistor, Q908, limits the change of current through V904 as the ramp runs up.
   a. Current variations are small from start to finish of the sawtooth ramp.

(1) With a 30k resistor in place of V93B, current would vary from 5 mA to 8.3 mA.

b. The constant current improves Delay Time timing.

6. Prior to sweep, V904A is cut off.

7. 5 mA passes through R908, V904B, R906, and R909. 5 mA flows through R903 and R907.

a. The TD is not conducting.

8. With the DELAY TIME MULTIPLIER set at midrange (50V, for example), the input ramp must reach 49V bevore V904A begins to conduct.

a. As the ramp runs up, 5 mA transfers from V904B to V904A.

b. As the current through D905 reaches 2.2 mA, the TD flips to its high state.

c. R904 and the primary of T905 form the TD load.

9. When the TD flips, a negative going pulse is coupled by T905 to the base of Q924.

10. During retrace, current switches back to V904B.

a. The TD switches back to its low state.

11. R900 isolates the A Sawtooth coax from ground at the delay pick-off end.

a. Noise on the coax is fed differentially into the comparator by C911 and coax capacity-reducing trigger pick-off jitter.

12. R901, C901, R906 form a low pass filter to reduce noise to the TD circuit which reduces trigger jitter.

13. R910, C910, R902, C902, R905, and C905 decouple the regulated supplies.

E. Delayed Trigger Multi

1. The Delayed Trigger Multi is a monostable multi. It produces one output pulse for each Delayed Trigger from T905.

2. Q924 is a 2N3906 silicon PNP transistor.

3. Q933 is a 2N3904 silicon NPN transistor.

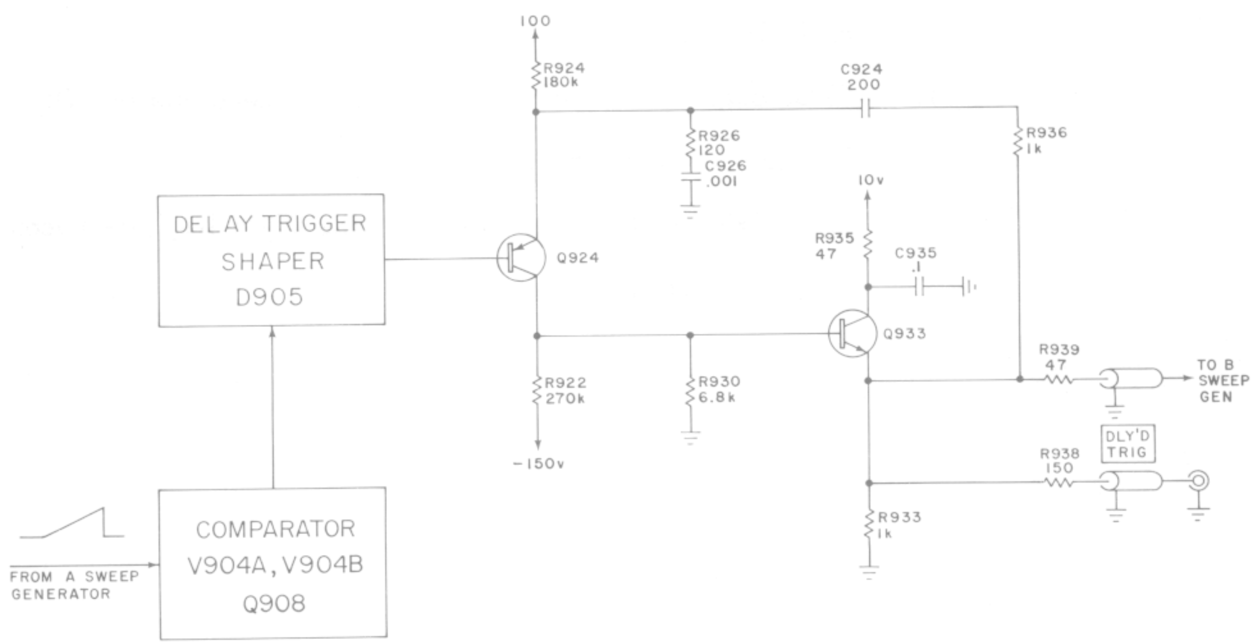
4. Quiescently, Q924 is conducting about 0.5 mA.

   a. Base returns to +10V.

   b. Collector voltage is -0.5V.

      (1) Collector load equivalent is 6.5k to -4.4V.

5. Q933 is turned off.



TYPE 556 DELAY PICKOFF
DELAY TRIGGER MULTIVIBRATOR

B-556-0222
1-21-'66jg

4. The negative going step from T905 drives the base of Q924 negative turning it on harder.

   a. A +12V step drives the base of Q933 positive turning it on.

   b. A +10V pulse appears at Q933 emitter.

   c. Part of the pulse is returned through R936, C924 to Q924 emitter saturating Q924.

   d. RC time of R936, C924, R926, C926 keep Q924 saturated for nearly 1 µs.

   e. At the end of the cycle, the multi reverts to its original state -- Q924 conducting 0.5 mA and Q933 turned off (-.5V on its base).

   f. Q933 output pulses are sent to "B" sweep generator and Dly'd Trig jack on front panel.

      (1) R938 limits emitter current if the Dly'd Trig jack becomes grounded.

VI. LOGIC, BLANKING, AND SYNC AMPLIFIERS

A. The Alternate Trace Logic circuit only operates when the UPPER BEAM DISPLAY switch is in the "Right plug-in A" position and the LOWER BEAM DISPLAY switch is in the "B" position.

1. The Logic circuit enables a multi-channel plug-in to switch channels properly when the Left Mode switch is turned to "Right plug-in A".
2. The Logic circuit operates in the NORMAL, DELY'D BY A, and SINGLE SWEEP positions of the B Mode switch.
3. In the NORMAL position, the Logic circuit keeps the A sweep from restarting until the B sweep has finished running.
   a. If the "B" sweep doesn't run, the "A" sweep will remain locked out.
4. The Logic circuit provides a channel switching pulse to alternate trace plug-ins.

B. Two inputs drive the Logic circuit.

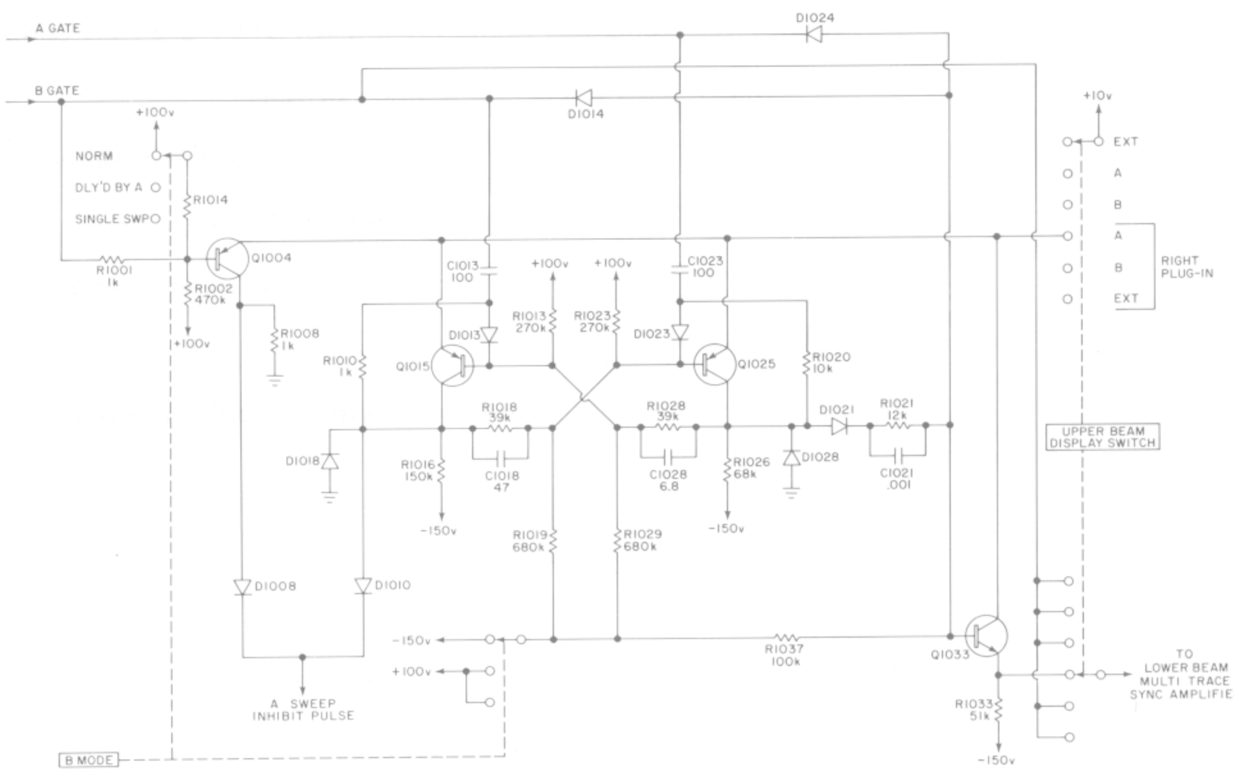
1. A negative 10V "A" gate.
2. A negative 10V "B" gate.
3. The gate goes from +10V to 0V in each case.
   a. +10V = no gate out.

C. Alternate Trace Logic (upper beam display switch in <u>A-Right plug-in</u>):

1. With the B MODE switch in normal, the Logic circuit holds "A" sweep locked out until "B" sweep finishes running.
   a. "A" sweep runs once but cannot re-run until "B" finishes.
   b. When "B" finishes running, the plug-in channels are switched by the Logic circuit.

2. With the "B" MODE switch in the DELY'D BY "A" or SINGLE SWEEP position, A sweep cannot re-run while "B" sweep is running.

   a. Alternate switching pulses come from the gate waveform of the sweep that finishes last.



TYPE 556 ALTERNATE TRACE LOGIC

B-556-0223
5-25-'66 mw

D. Logic Circuitry

1. In NORMAL operation Q1004 (PNP silicon) is cut off by current through R1014.
2. Q1033 is an emitter follower (NPN silicon)
3. Q1015 and Q1025 (PNP silicon) form a bistable multivibrator.
   a. The two transistors are turned off by their respective gates (Q1025, "A" gate) (Q1015, "B" gate) when the gates turn off.
   b. If either transistor is off, it can only be turned on by turning the other transistor off.
   c. The transistors switch from cut-off to saturation.
   d. Collector voltages switch from +10V at saturation to -0.5V at cut off.
   e. D1028 and D1018 clamp the collector voltages near ground when the respective transistors are cut off.
4. A positive pulse is applied to the base of Q1025 through D1023 and C1023 when the "A" gate stops (goes from 0V to +10V).
   a. The positive pulse turns Q1025 off.
   b. Q1025 collector goes negative and this change is coupled through C1028 to the base of Q1015 and turns Q1015 on.
   c. A positive inhibit pulse is applied to the "A" sweep hold-off circuit from the collector of Q1015 through D1010, locking the A sweep out.

d. When the "B" sweep gate turns off (goes positive), it will apply a positive pulse through C1013 and D1013 turning Q1015 off.

e. Negative Q1015 collector waveform coupled through C1018 turns Q1025 on.

f. When Q1025 turns on its collector waveform will rise from -0.5V to +10V, causing Q1033, an emitter follower, to have a +10V waveform on its emitter.

g. A positive going waveform at the emitter of Q1033 will be differentiated by C1061, R1060, and be applied to the channel switching circuit for alternate trace switching.

E. Delayed By A and Single Sweep Operation

1. Q1015 and Q1025 are turned off by +100V applied to R1019 and R1029.

2. Q1004 is turned on by disconnecting R1014 from +100V.

   a. Q1004 operates as an amplifier.

3. "B" gate applied to the base of Q1004 results in a +10V sweep inhibit pulse being applied to "A" sweep hold-off through D1008.

   a. "A" sweep cannot run again until "B" finishes.

4. Q1033 has a positive current source applied to its base through R1037.

   a. D1021 disconnects the multi from the circuit.

   b. The diode gate, D1024 and D1014, selects whichever sweep gate is on to hold Q1033 base at ground level.

c. The last gate to finish (go positive to +10V) will cause Q1033 Emitter to go positive and generate a channel switching pulse for the plug-in.

F. Sync Amplifier

1. The Sync Amplifier uses a 6DJ8 dual triode.

   a. There are two nearly identical Sync Amplifiers in the 556; the lower beam amplifier will be described here.

2. When a multi-trace plug-in is not in use or is used in a mode other than ALT, the cathode of the A section is tied through 1M to +100V and the plate to -150V through 1.8M.

3. When a multi-trace plug-in is in its ALT mode:

   a. The plate is connected to 225V through 10k in a 1A1.

   b. The cathode is tied to the base of a transistor (and DC ground through a blocking oscillator transformer primary) in a 1A1 and to ground in a CA.

4. The output waveform for a 1A1 is a positive going current pulse at pin 8 of the blue ribbon connector.

   a. A CA uses a negative going pulse at pin 16 of the blue ribbon connector.

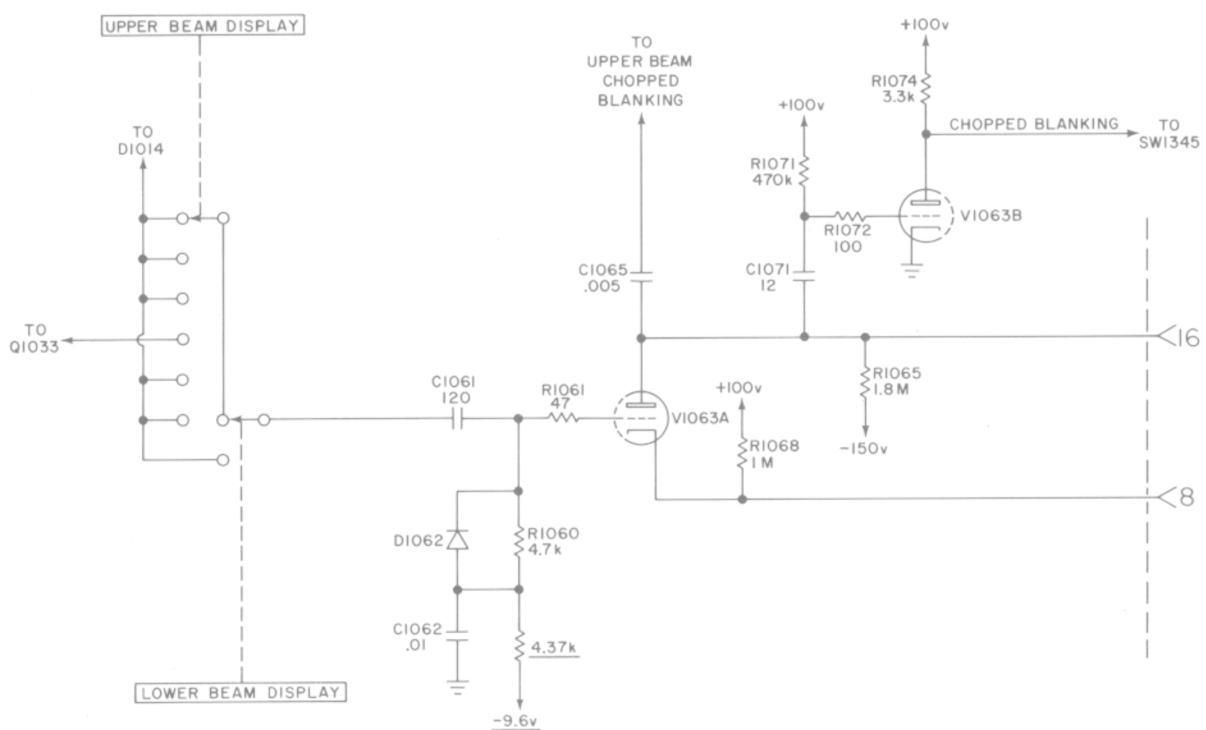
5. V1063A is cut off with about 10V fixed bias from R1063, R1062 divider.

6. The 10V step from the sweep gates or logic circuits is differentiated by C1061 and R1060.

a. D1062 removes any negative spikes.

b. Positive feedback from C1074 boosts the positive pulse.

c. The left plug-in doesn't alternate when the UPPER BEAM DISPLAY is set to RIGHT PLUG-IN.



B-556-0224
5-26-'66 mw

TYPE 556 MULTI-TRACE SYNC AMPLIFIER

7. The positive pulses from the gates or Q1033 drives V1063A into conduction.
   a. The pulse of cathode current switches the 1A1.
   b. With a CA in ALT mode, the plate pulls down about 60V (from 180V) to switch the plug-in,
8. The negative pulse on V1063A plate turns V1063B off.
9. The waveform at V1063B plate is positive going 45V pulse.
   a. The pulse is fed back through C1074 to V1063A grid as positive feedback.

G. Chopped Blanking Amplifier

1. V1063B, half of the 6DJ8 used as a Sync Amp, serves as the Chopped Blanking Amplifier.
   a. There are two nearly identical Chopped Blanking Amplifiers in the Type 556.
   b. When the UPPER BEAM DISPLAY switch is set to Right plug-in, the right plug-in chopped waveform is applied to both amplifiers.
2. Quiescently the tube is conducting heavily -- 17 mA.
   a. The plate voltage is 100V.
3. When a multi-trace plug-in is switched to CHOPPED mode, plate and cathode returns are removed from V1063A.
   a. The tube offers no load to the Chopped Blanking circuit.

4. The negative going chopped waveform pulse from pin No. 16 through C1071 reduces the grid voltage on V1063B.

   a. The plate of V1063B goes positive about 15 volts with a CA.

   b. This 12V pulse is the CHOPPED blanking waveform.

   c. The pulse is AC coupled through .01 µF to the CRT cathode.

   d. The 1A1 and M blanking pulses are broad compared to their frequency so as much as 50% of the trace is lost in the CHOPPED mode.

      (1) Chopped blanking waveform with an M runs about twice that of the CA.

5. A CHOPPED BLANKING switch (CRT circuit diagram) selects either CHOPPED BLANKING or Z AXIS modulation.

   a. There are two switches, one for each beam, located on the rear of the instrument.

VII. HORIZONTAL AMPLIFIER

A. The Horizontal Amplifiers provide push-pull sweep voltages for the horizontal CRT deflection plates.

B. The Horizontal Amplifiers are identical except for the inputs (only A will be described).

C. Output is a push-pull voltage ramp 200V peak-to-peak for 10 cm.

1. Nominal CRT deflection sensitivity is 20 V/cm (spec 18V to 22 V/cm).
2. 80-210V was the variation in horizontal plate voltage on one instrument (X1).
3. X10 mag variation was from ground to +340V.
4. Maximum sweep rate displayed is 10 ns/cm.

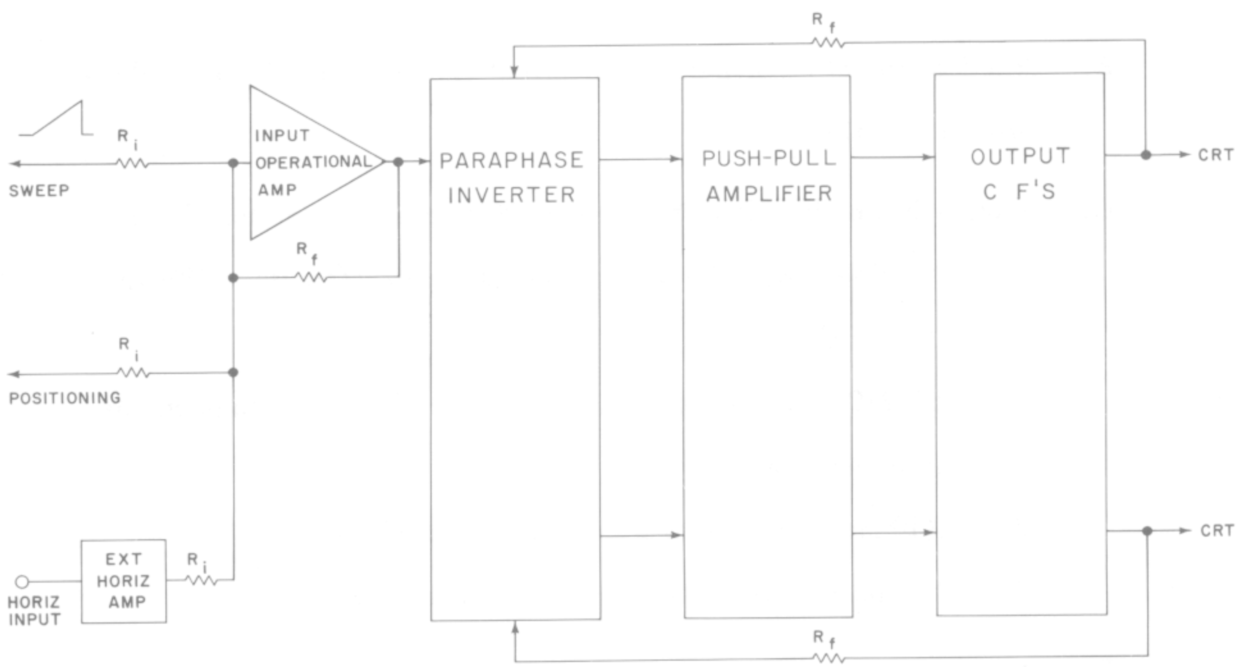
D. Inputs to:

1. A sweep sawtooth.
2. B sweep sawtooth.
3. Ext horizontal amplifier.
4. Positioning information.
5. (B Amplifier cannot be switched to A sweep sawtooth).

E. Magnifier Ranges

1. X1, X10.

F. Block Diagram



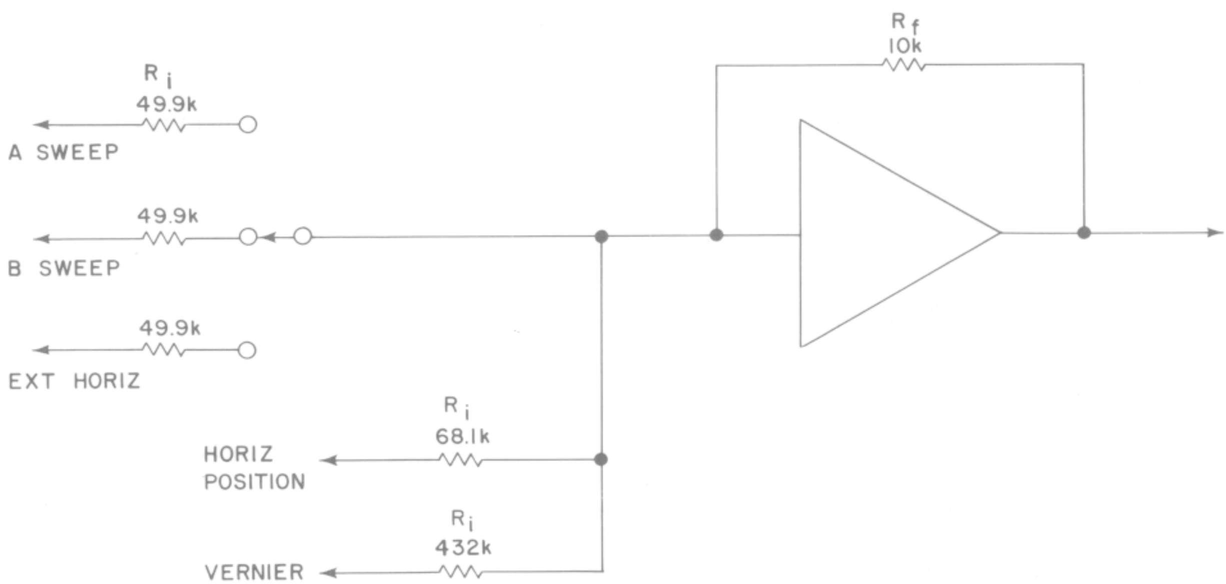
TYPE 556 HORIZONTAL AMPLIFIER
BLOCK DIAGRAM

B-556-0225
3-28-66jg

G. Basic Circuits

1. Operational Amplifier.
2. Paraphase Inverter.
3. Push-Pull Amplifier.
4. CF Output Stage.
5. HF Current Booster
6. Horizontal External Amplifier

H. Basic Operational Amplifier



TYPE 556 HORIZONTAL AMPLIFIER
BASIC OPERATIONAL AMPLIFIER

B-556-0226
3-29-66jg

1. The Basic Operational Amplifier is a transistor High Gain Amplifier.

   a. The Operational Amplifier provides a low impedance for transmission of the sweep ramp through shielded cables.

2. R_f is composed of the 10X Cal. R1146 and R1147.

3. There are five adder inputs (R_i):

   a. 49.9k (from the B Sweep Generator (R881).

   b. 49.9k from the A Sweep Generator (R681).

   c. 49.9k from the External Horizontal Amplifier (R1116).

   d. 68.1k from the Horizontal Positioning Control (R1137).

   e. 432k from the Vernier Control (R1139).

4. Operational Amplifier gain = $\frac{R_f}{R_i}$ for $k = \infty$.

   a. For Sweep A = $\frac{10k}{50k} = 0.2$.

   b. 100V input x .2 = 20V. Sawtooth signal at Q554 base is 20V.

   c. Gain is a function of resistor ratios, not transistor beta.

5. The signal voltage develops across R_f.

   a. The resultant signal current balances out the input current at the base of the input transistor.

   b. The feedback current at this point is diminished by 1/gain of the stage without feedback.

   c. The result is a very low impedance (virtual ground) at the input transistor base.

6. The input signal current is 200 μA/cm from both sweeps with X1 Mag and 20 _A/cm with 10X Mag or in the Ext. Horiz. input.

I. Input Operational Amplifier

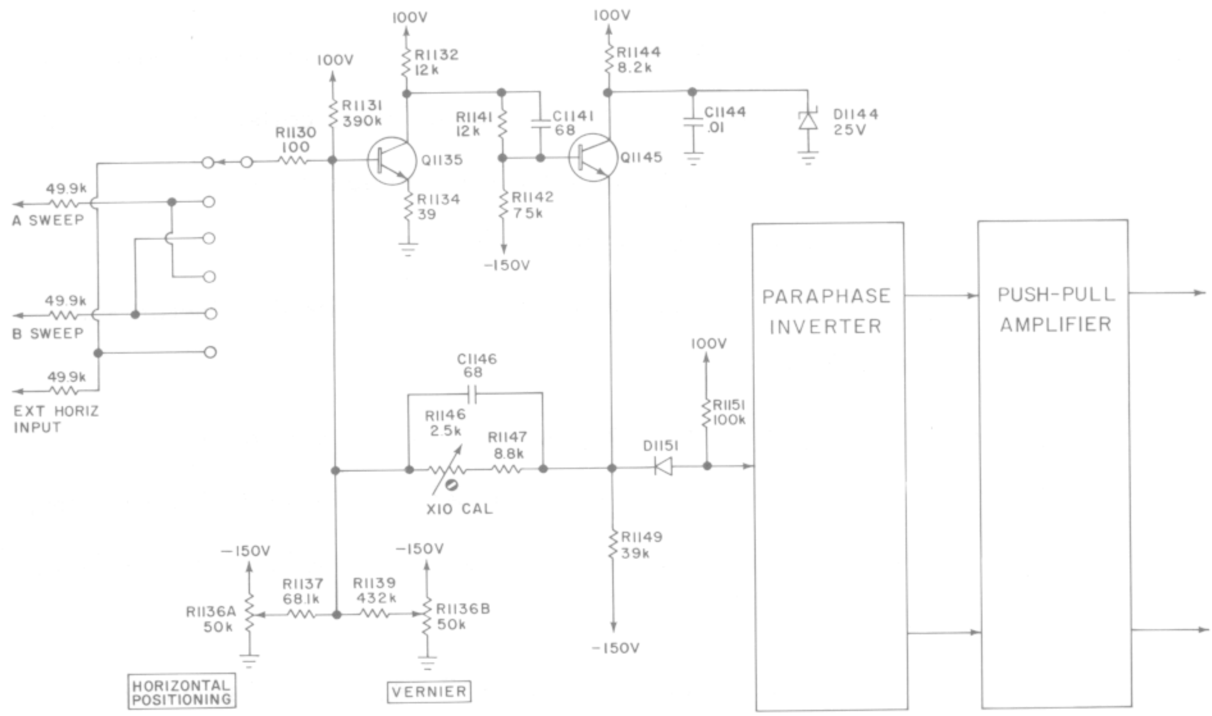
1. Two transistors, a zener, and a small signal diode are used in the amplifier.

   a. Q1135 is a silicon RCA NPN 2N3118 (151-121).

   b. Q1145 is a silicon Fairchild NPN 2N1893 (151-066).

c. D1144 is a Motorola 1M25Z10 10% 25V zener.

d. D1151 is a 1N3605 silicon diode.



TYPE 556 HORIZONTAL AMPLIFIER
UPPER INPUT OPERATIONAL AMPLIFIER

B-556-0227
3-29-66jg

2. The sweep inputs to the Horizontal Amplifiers are selected by the front panel Display switches.

3. The Position and Vernier controls are single front panel controls - a backlash potentiometer is used for vernier control.

   a. The position controls have a range of about 11 cm in X1 position.

      (1) Increases to 110 cm with mag.

b. The vernier control has about 0.5 cm control with 1X mag.

4. Input from the Ext. Horiz. Amplifiers is selected by the Display switches.

5. Q1135 base has less than a volt of signal and is near zero volts.

6. The amplifier signal is taken across Q1135 collector load R1132.

   a. A divider drops the DC level to near ground.

   b. C1141 compensates the divider.

7. R1147 and the X10 cal adjust form the R_f for the Operational Amplifier.

   a. R_f has a value of 10k with R1146 at design center.

   b. C1146 prevents feedback delay at the start of fast sweeps.

8. Q1145, an emitter follower, has a low impedance 25V collector supply.

   a. If Q1145 current exceeds 9 mA, D1144 disconnects.

   b. R1144 limits Q1145 collector supply at 25V.

   c. Normally D1144 clamps the collector supply at 25V.

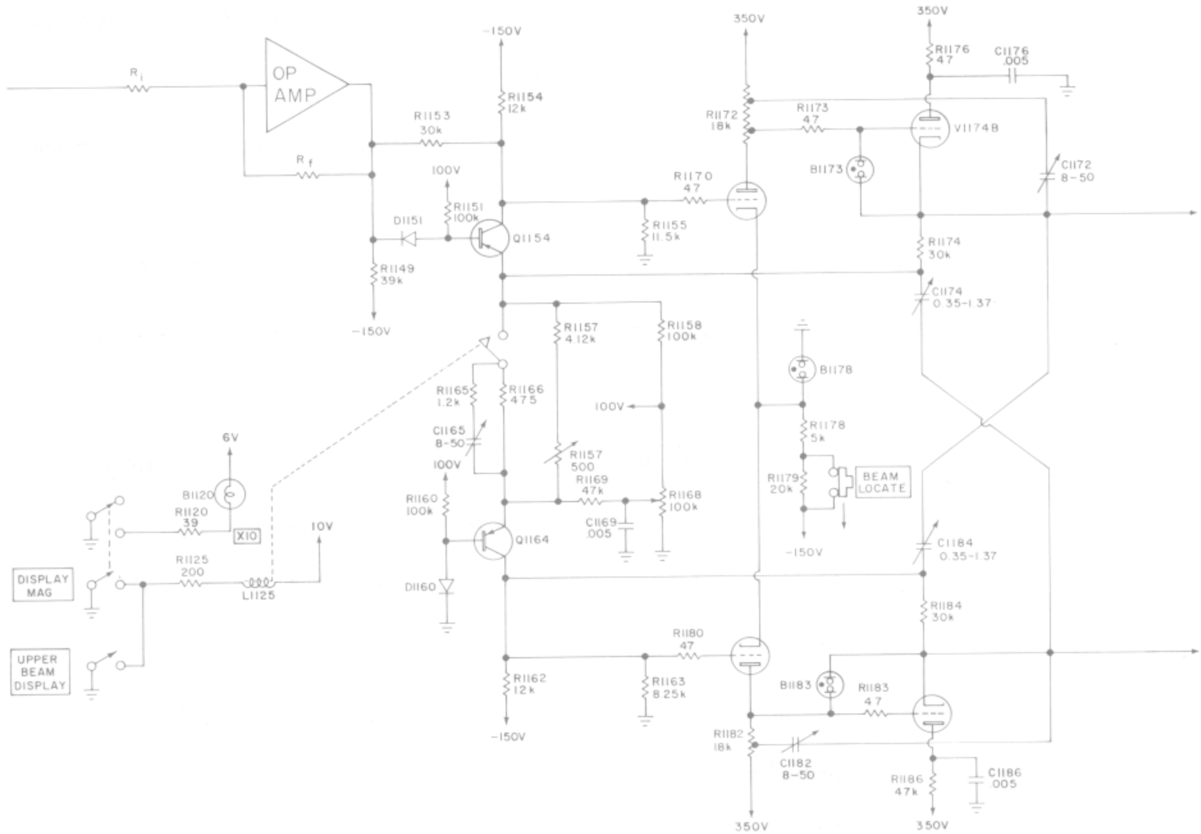
   d. C1144 provides decoupling for zener noise.

9. Q1145 is long-tailed to -150V.

10. The Operational Amplifier output (Q1145 emitter) is a negative going sawtooth about 20V peak-to-peak.

    a. Center screen voltage is zero.

J. Paraphase Inverter



TYPE 556 HORIZONTAL AMPLIFIER
PARAPHASE INVERTER

B-556-0228
4-5-'66jg

1. The paraphase inverter converts the 20V sawtooth single ended input waveform to push-pull.
    a. Gain is about 0.5.
2. The signal from the operational amplifier is a negative going 20V peak-to-peak ramp (2 V/cm in X1 mag position).
    a. Center screen level on Q1154 base is about 0V.
    b. The signal is coupled through D115 to the base of Q1154.

c. D1151 decouples if positioning and sweep raises Q1154 reverse base current higher than 1 mA.

(1) BV_{EBO} for a 2N2207 is 2V.

(2) When D1151 disconnects, base breakdown current is limited by R1151.

(3) This occurs with Mag on and the trace positioned far to the left.

d. D1160 provides temperature compensation for D1151.

3. Q1154 can saturate at the end of sweep if the trace is positioned far to the right.

4. Q1154, Q1164 collector resistors are selected to allow negative feedback from Q1154 collector to Q1145 emitter.

a. Collector load resistors are equivalent 4.88k to -61V including R1153.

b. Feedback resistor R1153 compensates for characteristic unbalance of a paraphase inverter.

c. The collectors set at about -33V center screen.

d. The collectors have about a 7V peak-to-peak swing.

(1) With X10 MAG on, the collector can swing from about -58V to +7V.

(2) Because the feedback loop is broken when the transistors cut off, the collector waveform at the limits of MAG excursion is very ragged.

(3) The displayed portion of the magnified sweep, however, is linear to within 3% for the center 8 cm.

5. At center screen, about 5.7 mA flows through each transistor.
    a. 1 mA flows through R1158 (and R1169).
    b. 4.7 mA supplies cathode current through the feedback resistors for the output CF's.
6. Gain of the amplifier is controlled (in the MAG position) by changing emitter resistance.
    a. The tying resistors limit negative feedback (like in the 533/543 Horizontal Amplifier) and limit gain.
        (1) The smaller the resistor, the less negative feedback and the greater the gain.
        (2) 475Ω is used in the X10 MAG position.
        (3) The X1 position uses only R1157 and the X1 CAL resistor that ties the emitters together.
        (4) In this position, the X1 CAL controls feedback to adjust gain.
    b. An out of phase current from V1174B cathode is fed back through R1174 to reinforce the signal on Q1154 emitter.
    c. An out-of-phase signal from V1184B cathode is fed back through R1184 to Q1164 emitter.
        (1) The driving signal on the emitter is decreased.
        (2) The signal on the collector is decreased.

7. The SWEEP/MAG REG adjust balances emitter current in Q1154, Q1164.

   a. The control is most effective when minimum feedback is imposed.

   b. It sets the center trace DC level on the CRT plates as MAG is switched on and off.

      (1) The center of the trace will not move as MAG is switched off or on.

8. High frequency compensation.

   a. Variable high frequency peaking capacitors are provided across the switched-in emitter tying resistors in the MAG positions.

   b. Positive feedback couples through cross coupled capacitors, C1174 and C1184, at fast sweep speeds.

      (1) The feedback reduces the negative feedback to Q1154, Q1164 emitters increasing gain.

      (2) Since the capacitors are variable, they provide an adjustment for high frequency peaking.

9. SWEEP MAGNIFIER switch.

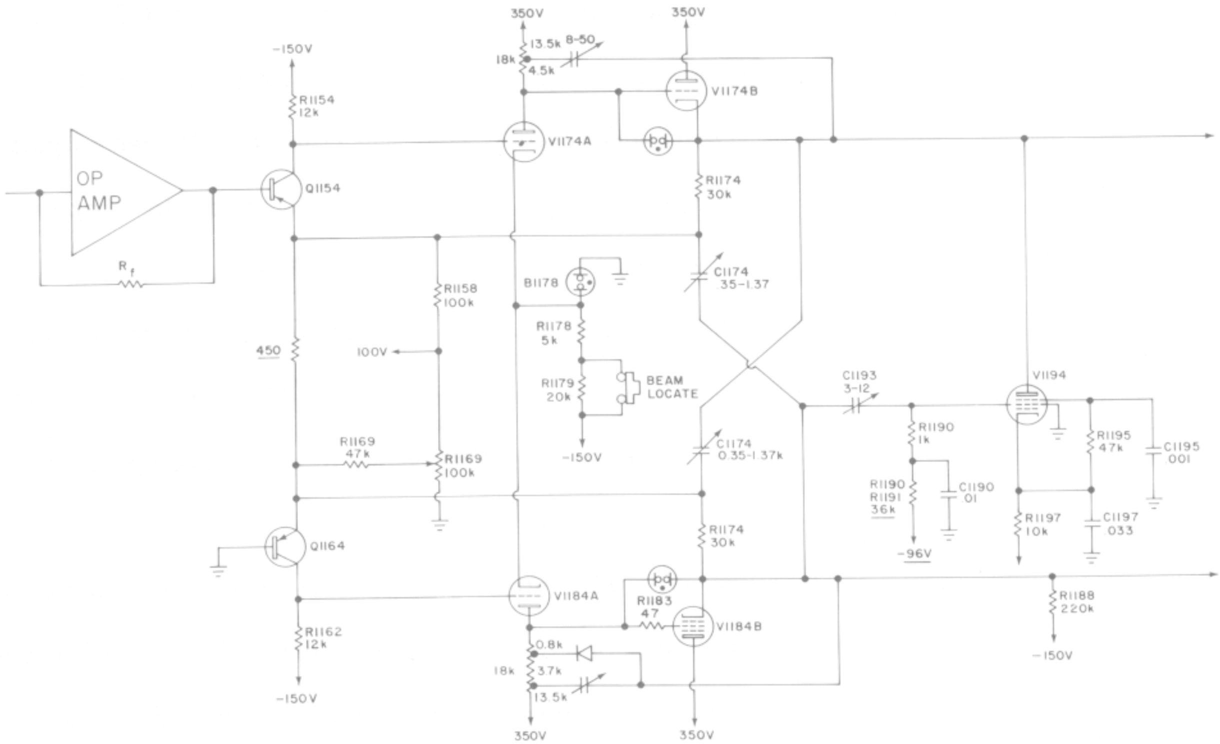
   a. The switch is below the HORIZONTAL DISPLAY switch.

   b. A MAG ON light lights when in the MAG position.

J. Push-Pull Amplifier and Output CF's

   1. The push-pull stage contributes most of the Horizontal Amplifier Gain.

a. It is a cathode coupled push-pull amplifier with a gain of about 20.



TYPE 556 HORIZONTAL AMPLIFIER
PUSH PULL AMPLIFIER AND OUTPUT CF'S

B-556-0229
3-30-'66 jg

b. Common mode signal is balanced out by the unity coupling.

c. One amplifier triode V1174A and its cathode follower V1174B are halves of a 6DJ8.

d. V1184A and V1184B are halves of another 6DJ8.

2. At trace center, V1174A and V1184A grids set at about -33V.

3. With 4V bias, the cathodes are at -29V.

   a. About 12 mA flows through each tube.

4. The plates have about a 110 volt swing from 80V to 190V.

5. Bootstrapping is provided by variable capacitors C572 and C582 to provide high frequency peaking at fast sweep speeds.

   a. Positive feedback, from the cathode follower outputs, couples through the bootstrap capacitors to a tap on the plate load resistors, R1172 and R1182.

   b. This signal voltage is in phase and about 95% of the amplitude of the signal on V1174A (and V1184A) plate.

      (1) The figure 95% comes from the average gain of a long-tail CF.

   c. As V1174A plate swings positive with large, fast sweeps and the tube approaches cut off, current is supplied through C1172.

   d. Bootstrap capacitors are variable to provide HF peaking.

6. The Output CF's provide a low impedance drive to the Horizontal deflection plates.

   a. Deflection plate capacitance is about 2.4 pF per plate.

7. V1194 is a high frequency capacitance driver.

   a. V1194 is an RCA 6197 pentode.

   b. At fast sweep speeds, the fast negative going sawtooth cuts off V1174B.

      (1) The time constant composed of R1174 and CRT deflection plate capacitance is not fast enough to follow the fastest sweeps.

      (2) An unexceptably non-linear trace results.

c. V1194 provides the current required to charge the deflection plate capacitance.

(1) At the faster sweep speeds, where V1174B begins to cut off, a positive going sweep ramp is coupled through C1193 to drive V1184.

(2) The positive going sweep ramp drives V1194 to greater current conduction. The current is provided to charge the deflection plate capacitance.

d. At fast sweep speeds, the left hand deflection plate is driven through V1194.

e. Since C1193 is variable, it can be used to adjust high speed timing.

f. Linear sweeps of up to 10 ns/cm can be displayed.

8. D1182 and R1188 speed up retrace time at fast sweep speeds.

a. While V1174B cuts off during trace time at high sweep speeds, V1184B cuts off during retrace.

b. This does not alter sweep linearity, but at the fastest sweep rates, retrace would exceed hold-off time.

(1) Hold-off time would have to be extended with a resultant loss of duty cycle.

c. During retrace, V1184B grid drops rapidly and V1184B cuts off.

d. As V1184A plate pulls down below V1184B cathode, D1182 conducts.

(1) D1182 is normally cut off.

e. Current to charge deflection plate capacitance is supplied by the r_p of V1184 and R1188.

f. Linearity is not a factor during retrace - just speed.

9. B1183 (a NE-23 neon) protects D1182 from reverse breakdown when V1184A cuts off.

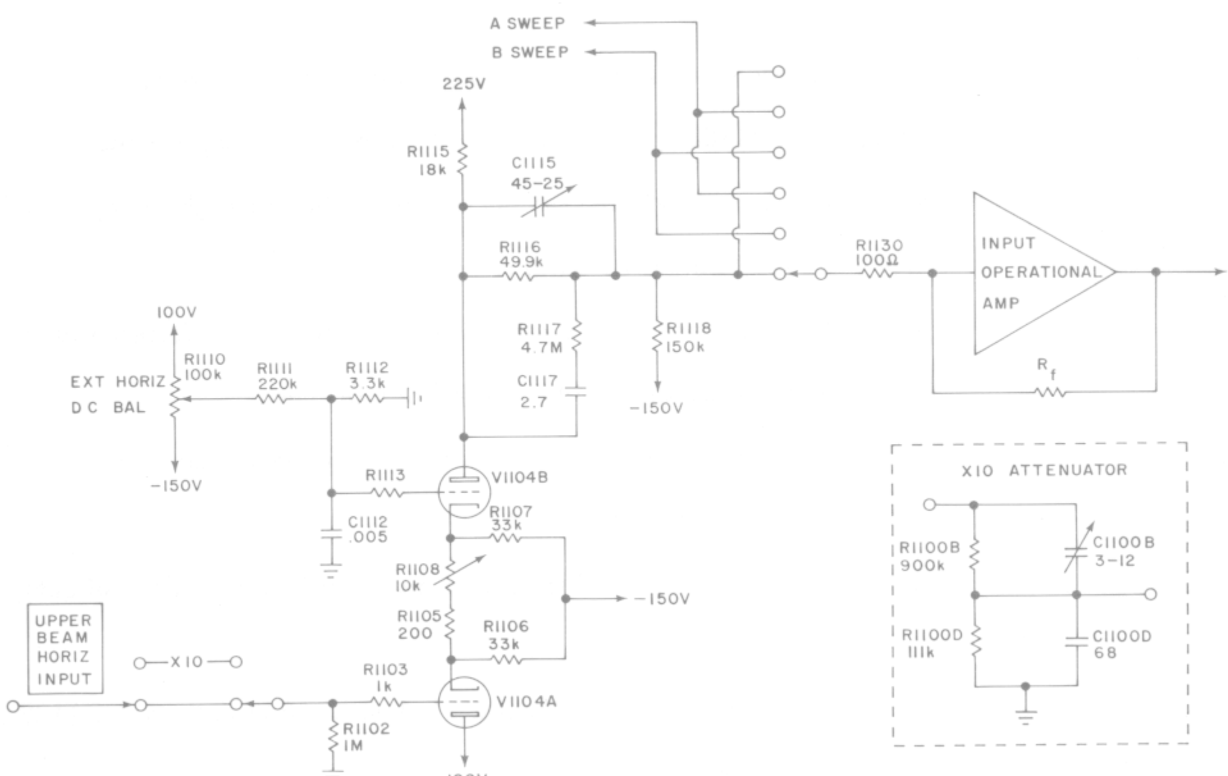
a. D1182 is a Raytheon 6061 diode with a PIV rating of 200V.

10. In the MAG positions, the output swings from 0V to 330V, limited by the power supply.

11. An off screen trace may be found by pushing the BEAM LOCATE switch.

a. The BEAM LOCATE switch reduces horizontal amplifier gain by lowering current through V1274A and V1284A.

K. EXT HORIZONTAL Amplifier



TYPE 556 HORIZONTAL AMPLIFIER
EXTERNAL HORIZONTAL AMPLIFIER

B-556-0230
3-30-66 jg

2. The External Horizontal Amplifier is a long-tailed cathode coupled amplifier using 6DJ8's.

   a. Sensitivity is about 80 mV/cm uncalibrated.

      (1) The MAG is on continuously in EXT HORIZ mode.

3. X1 and X10 (attenuator) inputs are available.

   a. Input impedance is 1 meg at about 50 pF.

      (1) Input Z is not standardized.

   b. The X10 input uses a conventional X10 compensated attenuator.

4. The VARIABLE control has a range of at least 10:1.

   a. Gain is controlled by varying the coupling to the grounded grid stage.

5. The EXT HORIZ DC BAL adjust prevents shift of the CRT beam as the VARIABLE control is rotated.

   a. When properly adjusted, V1104A and V1104B cathodes are at the same potential.

   b. No static current flows through the VARIABLE control.

   c. With no current through the VARIABLE control, its adjustment cannot effect DC current in V1104A or move the beam.

6. The output signal, taken across R1115, has a swing of 1 V/cm.

   a. The equivalent R_L is 13.2k to 165V.

   b. The voltage drive is converted to a current drive in R1116.

   c. The signal current through R1130 is 20 µA/cm.

   d. C1115 helps standardize input capacitance to the operational amplifier to match that of the sweep inputs.

7. Bandpass limitations.

   a. The bandpass of the external horizontal amplifier is at least 450 kHz.

   b. The limitation is imposed by unbypassed cathodes in the cathode coupled amplifier.

      (1) Cathodes cannot be bypassed as VARIABLE control would change the time constant with control settings.

VIII. CRT CIRCUIT

A. The CRT and High Voltage Supply consists of the CRT, its regulated high voltage supplies, and the controls necessary to focus and orient the displays.

B. Outputs from the regulated supplies:

1. 8.15 kV for the CRT post accelerator anode.
2. -1.85 kV for each CRT cathode.
3. -1.95kV (variable, floating supply) for each CRT grid.

C. Z Axis Modulation

1. AC coupled to the cathode.

D. Blanking and Unblanking

1. DC unblanking from A and B Sweep Generators.
2. Multi trace chopped blanking from plug-in to the CRT cathode - AC coupled.

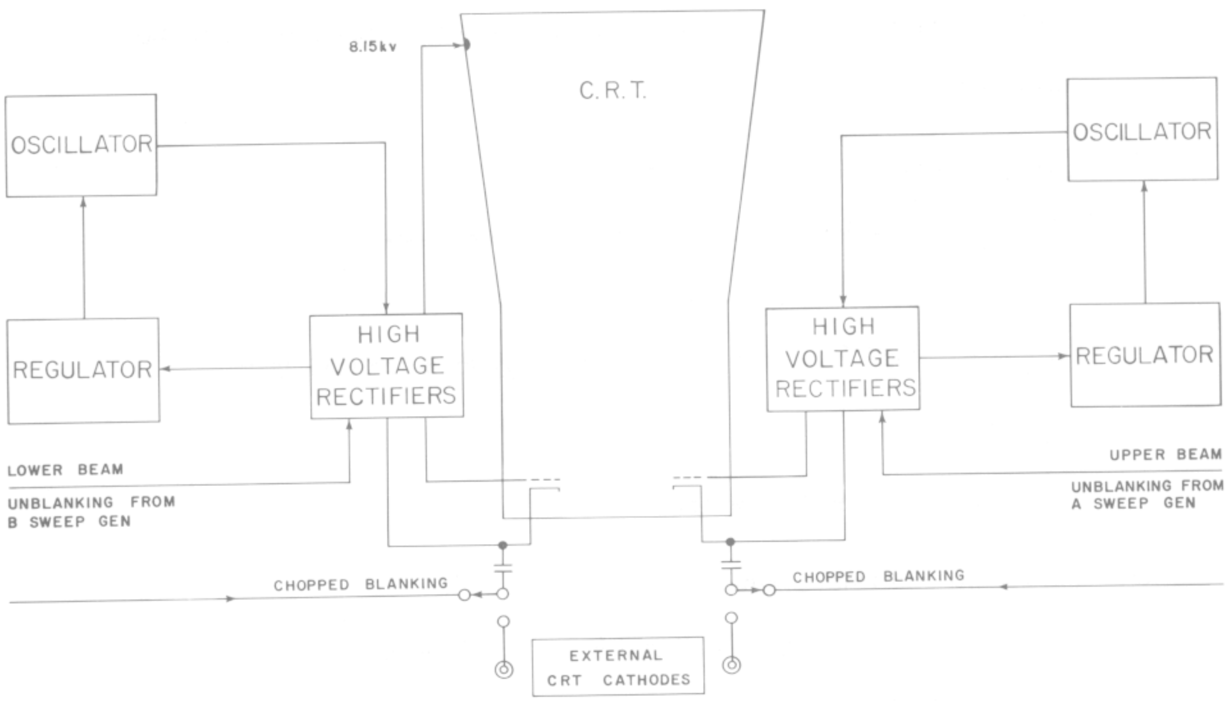
E. Front Panel Controls

1. Focus controls (2).
2. Intensity controls (2).
3. Astigmatism controls (2).
4. Trace rotation.

F. Internal Adjustments

1. Center geometry.
2. Edge geometry.
3. High voltage (2).

G. Block Diagram



TYPE 556 CRT AND HIGH VOLTAGE SUPPLY
BLOCK DIAGRAM

B-556-0231
2-11-66jg

H. Basic Circuits

1. Oscillator (2).
2. HV regulator (2).
3. High voltage rectifiers.
4. CRT.
5. 40 second delay circuit.

I. Block Logic

1. The free running oscillators develop 35 kHz sine waves.

2. The sine wave is stepped up in the high voltage transformers and rectified in five supplies.

3. The 8.15 kV supplies the CRT post-accelerator anode, -1.85 kV supplies the cathodes, and -1.95 kV supplies the grids.

   a. There are two -1.85 kV supplies and two -1.95 kV supplies.

4. A sample from each cathode supply is fed back to its regulator.

5. The regulator controls the oscillator output.

6. A feedback loop is formed consisting of the oscillator, the cathode rectified supply, and the regulator.

7. The feedback loop keeps the HV supplies constant.

8. Unblanking information is superimposed on the CRT grid voltage to provide DC coupled unblanking during trace.

J. Oscillator (the lower beam oscillator is described here):

1. The oscillator is a modified Armstrong oscillator which uses a 6GF5 pentode (a GE compactron).

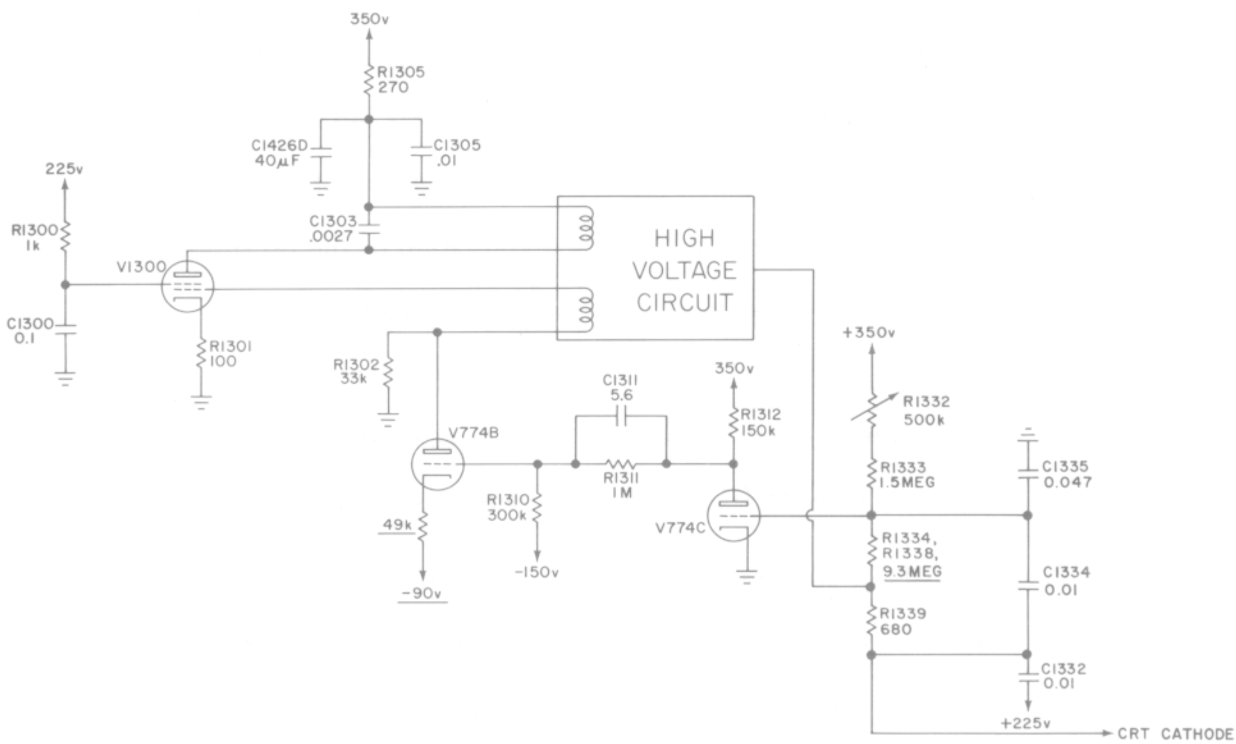
2. C1303 (and stray transformer capacitance) with the HV transformer plate winding primary form the oscillator tank circuit.

   a. The oscillator is tuned to approximately 35 kHz.

3. High voltage supply must have good regulation in a dual beam scope to avoid blooming and shrinking of traces.

   a. Only negative half cycle of oscillator sine wave rectified by D1332 supplies information to regulator.

b. R and C values of feedback circuit turn V1300 on hard at beginning of negative cycle and turn it off before D1332 quits conducting.



TYPE 556 CRT AND HIGH VOLTAGE SUPPLY
OSCILLATOR AND REGULATOR CIRCUIT

B-556-0232
2-14-'66 jg

c. No energy is put into the circuit by V1300 after D1332 quits conducting so the positive half of the oscillator waveform does not increase drastically as it does in most scopes when the intensity is increased.

d. A single beam scope compensates for positive half cycle variations by making R1327 about 1 meg and adding about 27k in series with the cathode.

(1) When the intensity is increased the positive half cycle increases, the voltage tripler puts out higher voltage, but increased tube current through the 1 meg anode resistor and the 27k cathode resistors offset the increase.

e. A sample of each negative oscillator cycle is fed back through divider C1333 and C1334 to control the grid of V1300 and consequently its plate output.

(1) V1300 draws current peaks of 150 mA at high intensity.

(2) V1300 does not draw grid current.

(a) Grid waveform varies from -150V to -20V.

(3) The screen of V1300 returns to +225 through low resistance to make high current peaks possible.

(4) R1301 provides protection if V774B fails.

(5) Plate current is supplied by the regulated +350V.

(6) Grid bias for V1300 is furnished by V774B plate current through R1302.

(7) Separate plate and grid windings for the oscillator are used to prevent "squeeging" or blocking oscillations.

K. Regulator Amplifier

1. V774B and V774C are two-thirds of a GE compactron.

   a. R1307 keeps cathode to filament voltage difference below 100V rating of the tube.

2. The regulator amplifier, V774B and V774C, amplifies both the DC and AC signal from the CRT cathode supply divider.

3. High voltage adjustment:

   a. As resistance is decreased at R1332, V774C bias is reduced - grid goes more positive.

   b. The positive DC change is inverted and amplified in both V774B and V774C.

   c. The oscillator will be biased to greater output.

   d. All high voltage supplies in lower beam increase.

   e. As the CRT cathode supply increases toward 1900V, V774C grid will return to near its original voltage.

      (1) AC variations are fed back by the same system.

      (2) As the system is an operational amplifier, the net result is increasing the output with virtually no change at the input grid, V774C.

      (3) C1311 compensates V774B grid network.

4. The same feedback system operates to hold the CRT cathode voltage constant as beam current, component change, and line voltage changes attempt to change it.

L. High Voltage Rectifier

1. The lower beam circuit consists of the high voltage transformer, three vacuum tube diodes, two solid state diodes, and the filter circuits.

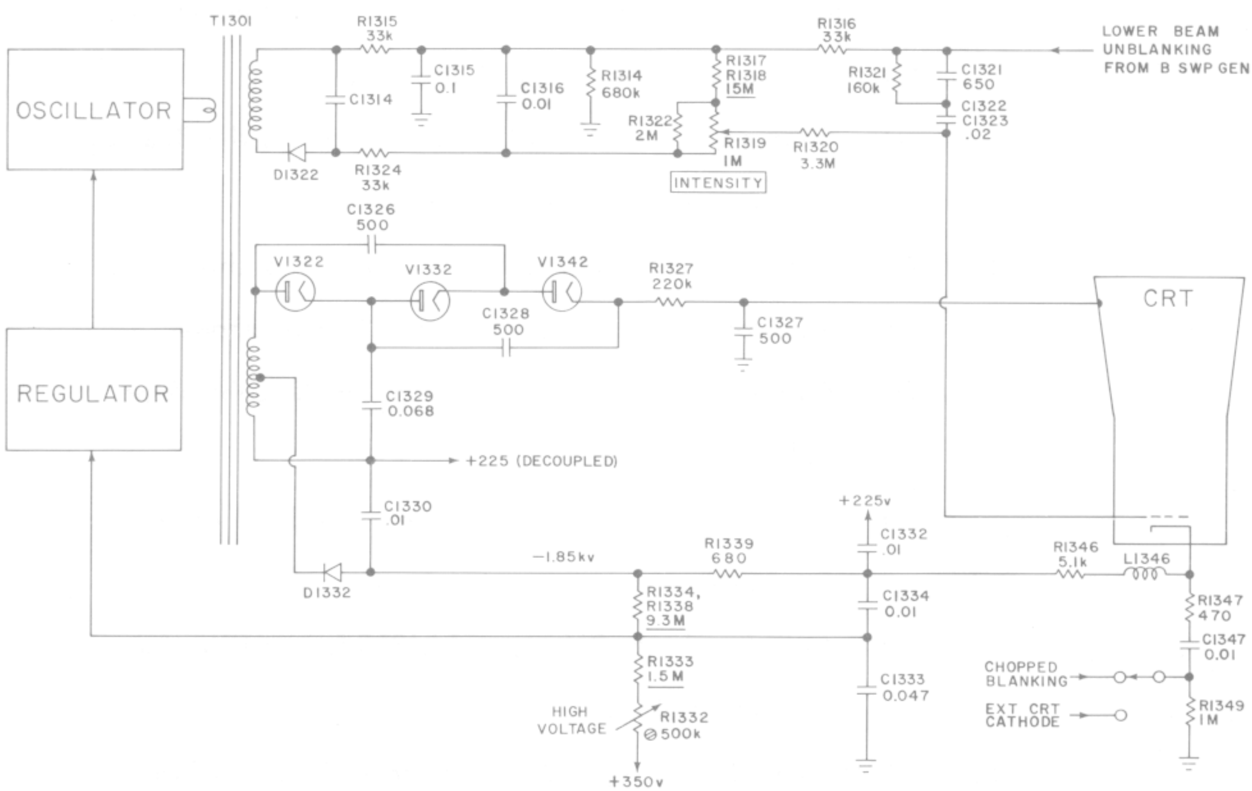
2. The upper beam circuit does not have any vacuum tube diodes.

3. There are five high voltage supplies:

   a. 8.15 kV for the CRT post-accelerator.

   b. -1.85 kV for the CRT cathodes (2).

   c. -1.9 kV for the CRT grids (2).



TYPE 556 CRT AND HIGH VOLTAGE SUPPLY
HIGH VOLTAGE CIRCUIT

B-556-0233
2-14-66jg

4. The high voltage transformer is Tek made.

    a. The two high voltage secondaries are bifilar wound.

5. The grid supplies use solid state rectifiers to reduce aging problems.

    a. The entire grid supplies are floating on the unblanking waveform to provide DC coupled unblanking to the CRT grid.

    b. The positive side of the supply receives the unblanking waveform.

    c. The fast (high frequency) portions of the waveform bypass the supply to drive the CRT grid directly.

        (1) Stray capacitance, wiring, etc., prevent the floating supply from following fast unblanking.

    d. A network of RC circuits couple the unblanking information across the floating supply and preserve the waveshape.

        (1) C1322, C1323 are coupling caps for the unblanking voltage.

        (2) R1321 and C1321 prevent a slight overshoot on the front of the unblanking waveform.

        (3) C1314, C1316, R1324, and R1315 form a filter for the output of D1322.

    e. R1315, C1315, R1314, R1316 help shape the unblanking waveshape.

f. The Intensity control forms part of a 16M divider across the supply.

(1) The control picks off some of the -1950V for grid bias.

(2) Range is from -1950 to -1860 approximately.

(3) CRT cut-off bias is approximately 90V.

(4) The control gives a bias range (grid to cathode voltage) of -100V to -10V.

(5) Grid current is limited by R1318.

(6) The wide bias range allows for variations in supply voltages, CRT's, and component aging.

(7) R1320 also isolates the floating supply from the AC coupled fast portions of the unblanking waveform.

5. The CRT post-accelerator anode supply uses three 5642's as a half-wave voltage tripler*.

a. +8150V is supplied at about 350 μA.

b. R1327, C1327 filters the 35 kHz ripple.

(1) This also reduces 35 kHz radiation from the faceplate.

6. The CRT cathode supply uses a single sold state diode (7701-5X) as a half-wave rectifier to deliver -1850V at about 2.5 mA maximum.

a. A tap off the anode winding of the HV transformer is used.

* Typical Oscilloscope Circuitry, page 12-8.

b. C1330, C1332, C1334, and R1339 provide filtering.

c. A series of resistors R1332-R1339 provide a cathode supply bleeder and divider to ground.

d. The DC level is divided down to about -4V for V774C's grid.

e. C1333 and C1334 form an AC divider for V774C grid.

(1) About 0.1V of 50 kc signal appears between this point and ground.

f. The cathode supply (and all HV supplies) is adjusted by the high voltage adjustment for each beam.

g. A solid state semiconductor is used to reduce change in +8150 with change in cathode current.

M. CRT Circuit

1. The CRT is a T5560 aluminized five inch flat-faced dual gun CRT with electrostatic focus and deflection. It has a 200 megohm helix that provides post-deflection acceleration with an internal lighted graticule.

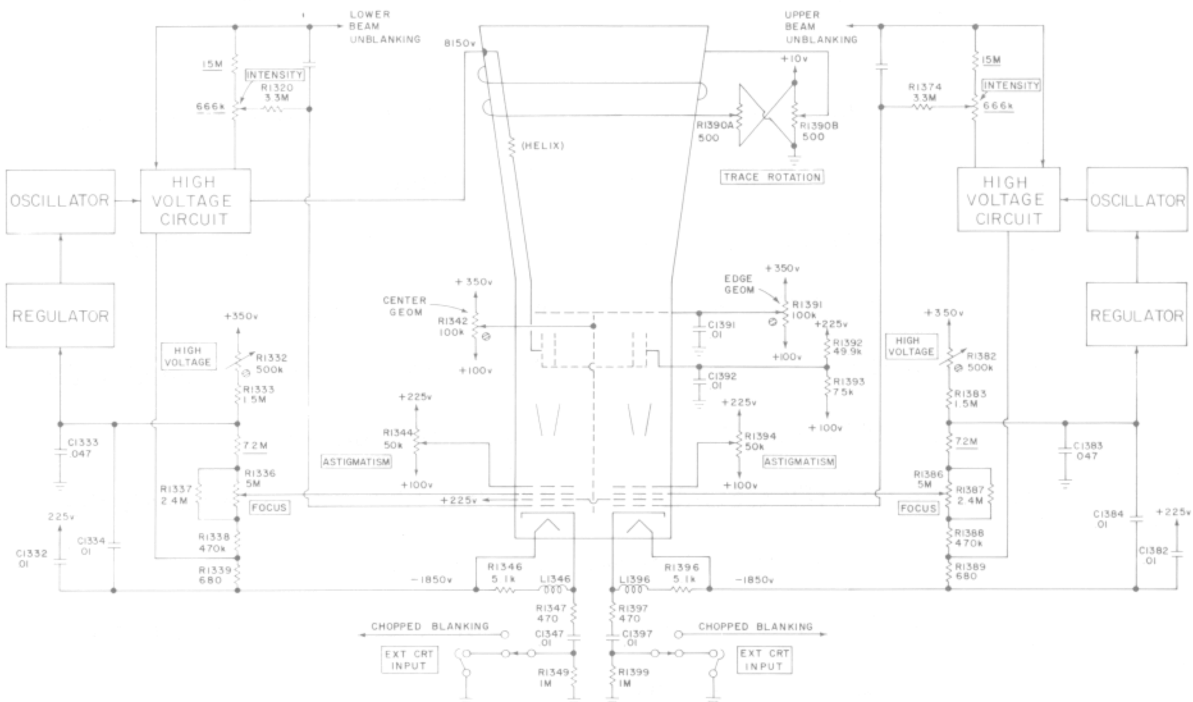
a. Normal phosphor is P31.

b. Display area is 6 x 10 cm for each beam with at least 4 cm of vertical overlap (four 1 cm^2 corners are missing).

2. Total accelerating potential is 10 kV.

3. The 60V unblanking waveform biases the tube on during trace.

4. The FOCUS control is part of the CRT cathode supply bleeder (there are 2 focus controls).



TYPE 556 CRT AND HIGH VOLTAGE SUPPLY
CRT CIRCUIT

B-556-0234
2-18-66jg

a. The control is a 5M pot shunted by a 3.3M resistor.

(1) Without the FOCUS pot, the bleeder has a 5% tolerance.

(2) A dependable, better than 20% tolerance, 1.66 meg pot is not readily available.

(3) A closer than 20% tolerance bleeder string is desirable as it provides a more certain useful range of the FOCUS control.

(4) R1337, a 5% component, provides an 8% tolerance bleeder string.

(5) Range is approximately -1700V to -1400V (150V to 450V relative to the cathode).

5. The ASTIGMATISM control is a 50k pot with a range of 100V to 225V (1950V to 2075V relative to the cathode).

6. The EDGE GEOMETRY control is a 100k pot with a range of 100V to 350V (1950V to 2300V relative to the cathode).

7. The CENTER GEOMETRY control is a 100k pot which adjusts the gun shield voltage between +100V to +350V.

8. TRACE ROTATION control is a dual 500Ω pot connected to the +10V supply in the vertical.

   a. The coil is connected around the CRT under the shield.

   b. Coil resistance is 100Ω.

9. A helix winding with a minimum resistance of 200M is connected between the post accelerator and pin No. 9 of the CRT.

   a. Pin No. 9 goes to about +175V at a divider and the vertical plate deflection shields.

10. The CRT heater is elevated to -1850 to eliminate heater cathode breakdown.

11. Z axis modulation is possible through rear panel CRT cathode connectors.

   a. The input is designed for use with marker pulses and will differentiate a square wave.

   b. 5V will usually be adequate to modulate the display at normal intensity.

      (1) A 50V square wave (from a calibrator, for example) will pull the HV supply out of regulation.

   c. A BNC cap covers and grounds the input when not in use.

      (1) With the cap removed, the beginning of the trace will be dimmed at fast sweep speeds.

      (2) Capacitive coupling from grid to cathode will lift the cathode at the beginning of unblanking if the cap is removed and the C must discharge through R1346 and L1346 to return to normal intensity.

   d. A CRT Cathode Selector switch on the rear panel selects either DUAL TRACE CHOP BLANKING or EXT CRT CATHODE jack.

   e. R1346 and L1346 isolate the Z axis drive and chopped blanking from the high voltage supply.

   f. Impedance looking into the EXT CRT CATHODE jack is about 5.5k minimum and varies with frequency due to the inductor and the AC coupling.

g. Z axis input is AC coupled -.01 μF.

h. R1397 damps ringing at the start of the trace.

(1) The grid-to-cathode capacitance together with lead inductance would ring as the unblanking pulse tried to pull on the CRT cathode.

15. Dual trace chop blanking pulse is about 17V peak-to-peak.

16. The upper beam circuitry and oscillator are almost identical except for the HV Tripler.

17. A 40 sec delay circuit allows the high voltage to increase gradually while the CRT circuits are stabilizing.

a. Q1334 is a transistor clamp which turns off slowly after power supply voltages come on.

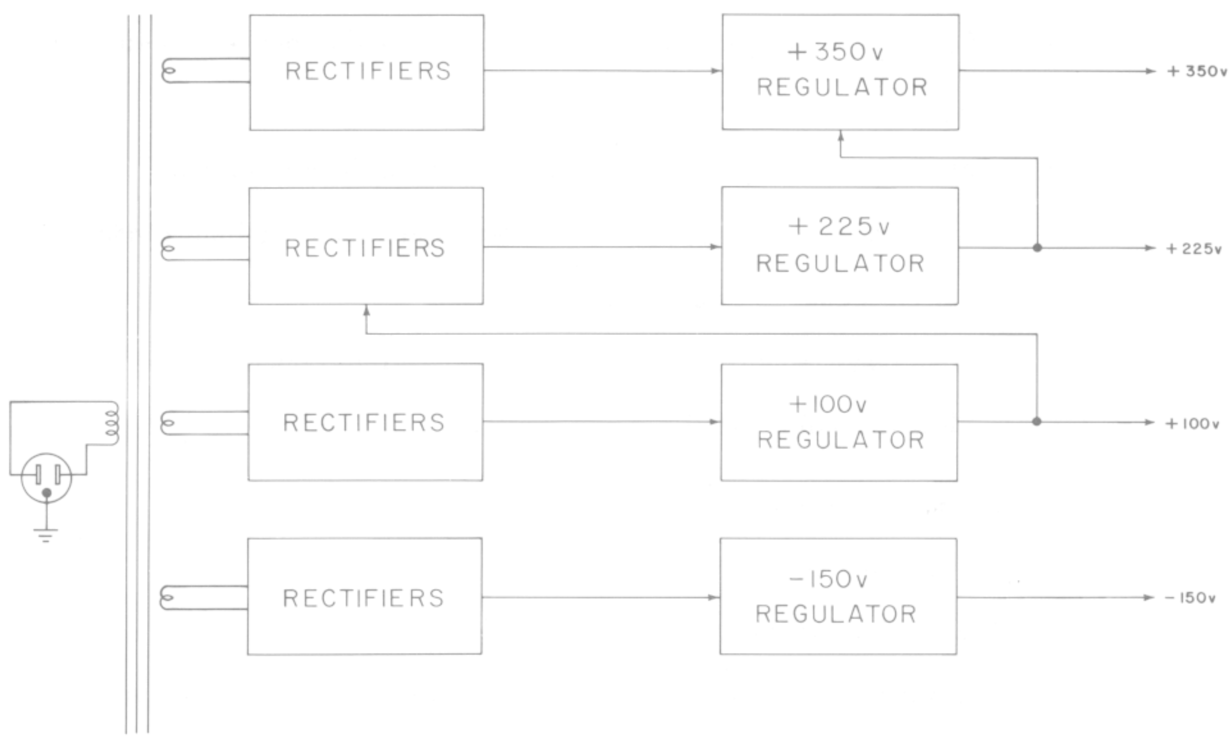
IX. POWER SUPPLY

A. The low voltage power supply provides four regulated voltage sources for use in scope main frame and plug-ins.

1. Supplies will regulate at low line voltages with the plug-ins removed.

2. The supplies will regulate with primary voltages from 100V to 130V (115V connection).

B. Block Diagram



TYPE 556 POWER SUPPLY
BLOCK DIAGRAM

B-556-0235
2-3-'66jg

C. Block Logic

1. A common power transformer supplies all regulated supplies and heater needs in the scope main frame and its plug-in.

2. Regulated supplies:

   a. -150V, ±1%, 5 mV ripple (adjustable).

   b. +100V, ±1%, 5 mV ripple (adjustable).

   c. +225V, 125V ±.5% from +100V, 10 mV ripple (adjustable).

   d. +350V, ±2%, 15 mV ripple.

3. The -150V supply uses ZZ1000 glow tube as reference.

4. The 100V, 225V and 350V supplies use the regulated -150V as reference.

5. Four sets of bridge rectifiers provide DC for the four regulated supplies.

6. No peak limiting resistors are used because the wiring and transformer secondary resistances are high enough to limit diode current peaks to safe values.

7. Each power supply winding has enough current capability to blow the main fuse if a diode shorts.

D. Transformer Circuit

1. The power transformer is Tek made.

   a. The primary is insulated to 600V.

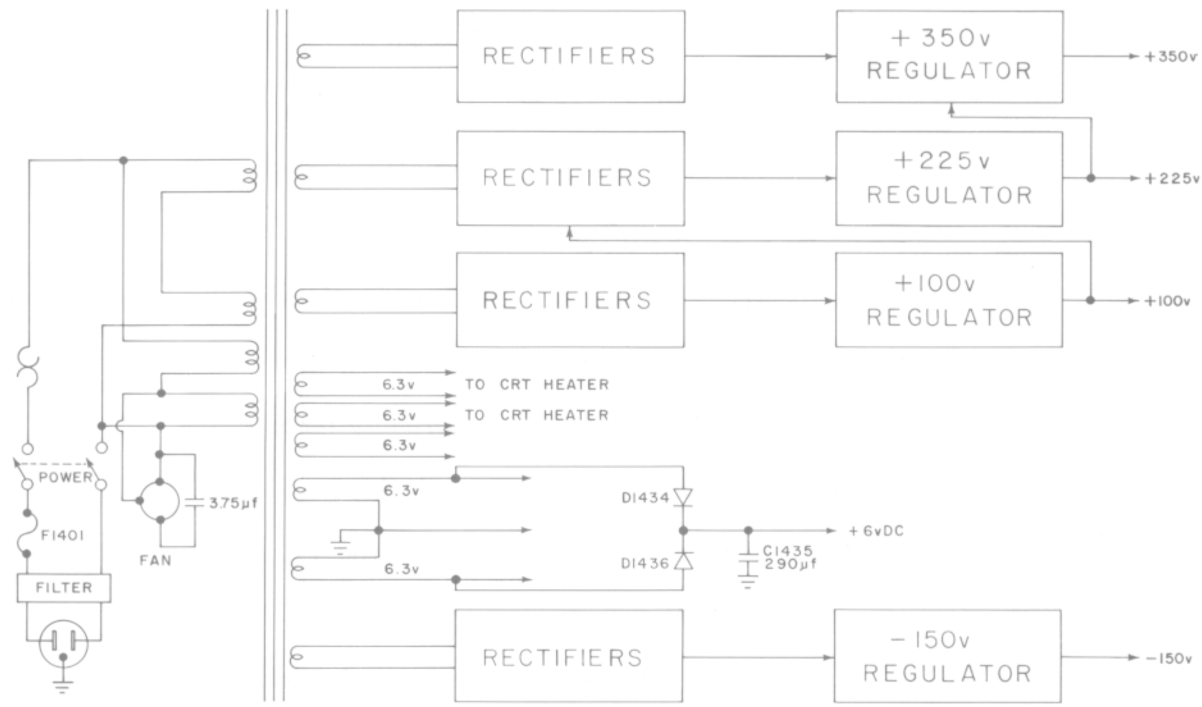
2. Besides the four windings for the bridge rectifiers, five heater windings are provided.

   a. Two 6.3V, .6a for CRT heaters.

      (1) Elevated to -1850V.

b. 6.3V, 1.6A for Horizontal Amplifier output tubes.

(1) Elevated to 100V through 100k.



TYPE 556 POWER SUPPLY
TRANSFORMER CIRCUIT

B-556-0236
2-4-66jg

c. 6.3V, 7.5A for the Vertical Amp output tubes and plug-ins.

d. 6.3V, 10.5A for the remainder of the tube heaters and the Power On light and graticule lights.

(1) The LINE TRIGGER voltage is fed from this winding.

3. A detachable 3 wire power cord is suppled.

4. Both sides of the power line are interrupted by the Power On switch. One side has a fuse and the thermal cutout.

   a. The fuse is a 10.0A, 3AG "Slo-Blo".

   b. The termal cutout will open at 140°F ±5°.

      (1) When the transformer primary is connected for 115V, or 230V, the fan will not continue to run after the cutoff opens.

      (2) The cutout resets automatically when temperatures return to normal.

   c. RF filter is used in the primary leads.

5. A fan provides forced air ventilation.

   a. The fan is connected across the 115V line after the thermal cutout.

   b. When the transformer primary is connected for 230V, the fan is connected to a 115V tap on the primary winding.

   c. The fan operates from 50 to 60 cps.

6. The transformer has two main primary windings.

   a. When connected in parallel, the scope will operate on 100V to 130V.

   b. When connected in series, the scope will operate on 200V to 260V.

   c. Two extra windings allow additional voltages of 90V to 117V and 180V to 234V.

7. Line frequency is 50 to 60 cps.

   a. Line frequency can be increased to 400 cps with a mod to drive the fan (50-60 or 400 cps).

8. Regulation specs are optimized at $\leq$2% sine wave distortion.

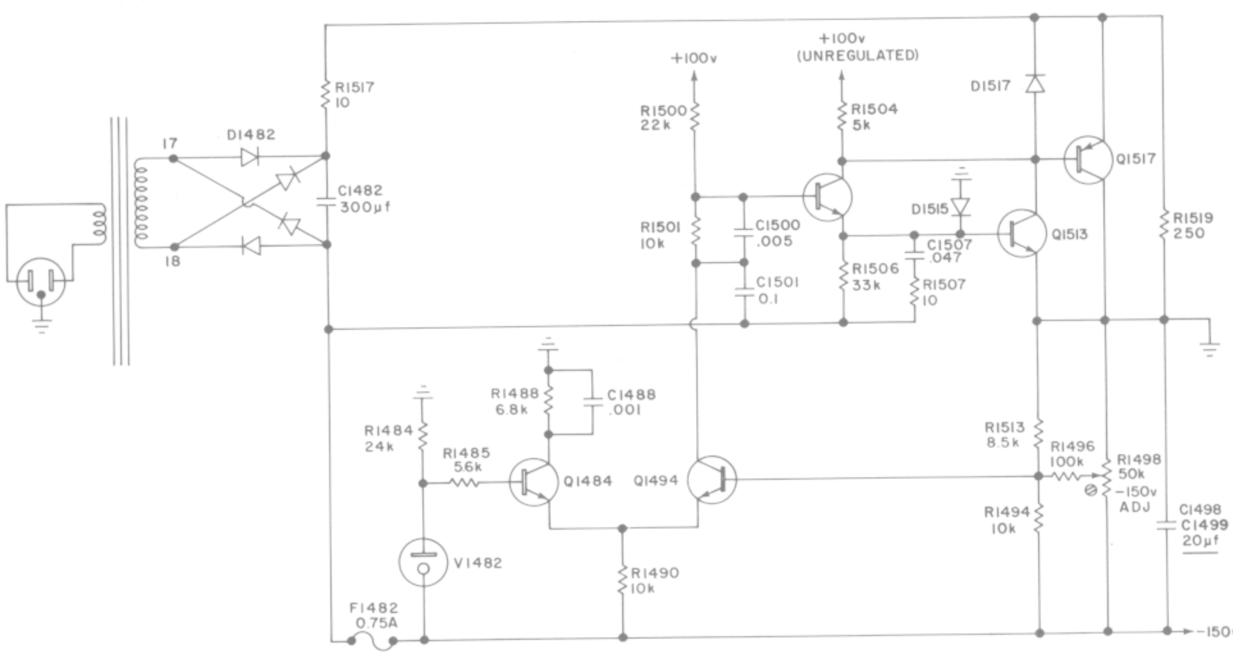
   a. Typical acceptable distortion is <2%.

   b. Increased distortion will change the range of line voltages over which the scope will regulate.

   c. Saturable reactor regulators (for example) may distort the sine wave sufficiently to prevent the Low Voltage Power Supply from meeting regulation specs.

E. -150V Supply

1. The -150V supply is a series regulated supply fed by a full wave silicon bridge.



TYPE 556 POWER SUPPLY
-150v SUPPLY

B-556-0237
2-10-'66jg

2. The supply delivers an average of 480 mA.

a. Connections to pin number 9 in each plug-in compartment supply the plug-ins through 100Ω decoupling resistors.

3. The supply uses a 145V transformer winding rated at 0.50A.
4. A full wave silicon bridge supplies 200V DC to the regulator.
    a. The bottom of the supply is set to -150V.
    b. The top of the supply ranges from 13 to 62 volts as the line voltage is varied from 100 to 130 volts.
    c. The rectifiers are RCA 1N3194, 750 mA silicon diodes with a 400V PIV (152-066).
    d. C1482 filters the rectifier output.
5. A ZZ1000 voltage regulator tube is used as a reference for the supply.
    a. 3 mA flows through the tube.
    b. It operates nominally at 81V.
    c. Voltage tolerance at 3.2 mA is 80.1V to 82.5V.
    d. The tube is designed for 30,000 hours of life.
6. The -150V supply has a 5 mV ripple spec (test spec).
7. The -150V adj sets the -150V supply accurately.
    a. The -150V supply has a ±1% test spec.
    b. The -150 volt control connects to the error sensing divider.
8. Q1484 and Q1494 are connected as an emitter coupled comparator or amplifier.
    a. The comparator compares the voltage from the sensing resistors on Q1494 base with the error voltage from the ZZ1000 on the base of Q1484.
    b. Since this is a negative supply, error voltages appear with opposite polarity from the positive supplies.

(1) An increased load requirement makes the -150V output less negative.

(2) Increased line voltage causes the -150V to go more negative.

c. Error signals applied to the base of Q1484.

d. Differential operation of the comparator increases the temperature stability of the power supply. V1482 also has very good temperature characteristics.

9. Amplified error signal is fed to the base of Q1504 through an RC network of R1500, C1500, R1501, and C1501.

a. This network allows the regulator to respond at a relatively slow rate which reduces the possibility of oscillation (less than 50 kHz).

(1) The regulator will not cancel high frequency variations on the power supply.

(2) C1500 feeds back ripple to the base of Q1504 while C1501 limits the frequencies fed back.

b. Q1504 and Q1513 are Darlington connected for increased beta gain to drive Q1517.

c. C1507 and R1507 are frequency compensations to prevent oscillations and limit regulator frequency response.

10. Q1517 is the series regulating transistor.

a. R1517 limits the maximum current through Q1517 in case of short on the -150V supply.

(1) If the supply is shorted, Q1517 saturates with about 10 amps of current through it until F1482 opens.

11. D1515 and D1517 protect against reverse emitter base breakdown.

12. There is no 10Ω protective resistor in the bridge.

a. There is enough current capability in the winding to blow the primary fuse if a diode shorts.

b. Transformer secondary resistance limits peak diode currents within diode ratings.

13. All other power supplies use the -150V supply as a reference for their voltage output.

F. +100V Supply

1. The +100V supply is a series regulated supply fed by a full wave silicon bridge rectifier.

2. The supply delivers an average of about 1800 mA depending on the plug-in used.

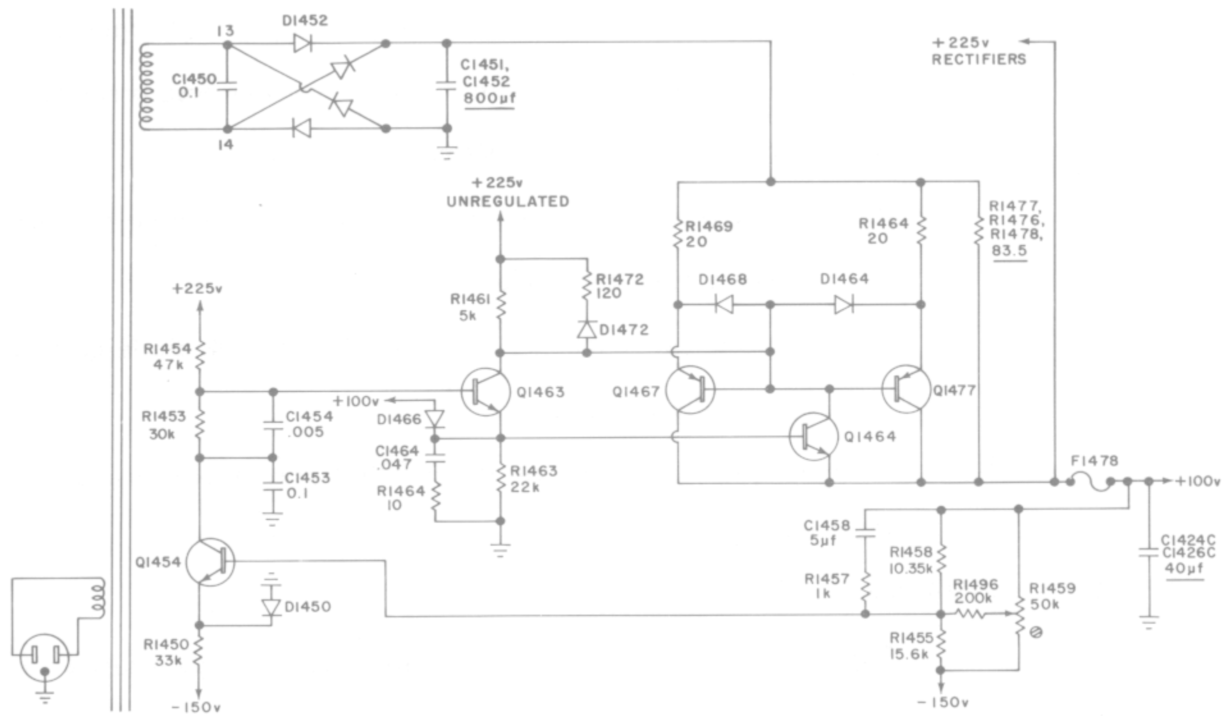
a. The current for the +225V and +350V supplies also passes through the regulator but not through the output fuse.

b. A connection to pin 10 of the blue ribbon connectors (through 100Ω decoupling) supplies the plug-in; for example 55mA for a type 1A1.

c. About 300mA is provided for the DC heater strings.

(1) The string includes the vertical input C.F. and the Miller tube in each sweep.

(2) The series filaments in the main frame drop the +100V to 75V for the plug-in heaters.



TYPE 556 POWER SUPPLY
+100v SUPPLY

B-556-0238
2-7-'66jg

3. The supply uses a 116V RMS transformer secondary rated at 1.8A.

4. A full wave silicon bridge supplies 146V DC at 115V line.

   a. The rectifier diodes are MR1032A Motorola 3.0 Amp 200P.I.V. silicon diodes, 152-0198.

   b. C1450 reduces silicon switching transients.

   c. C1451 and C1452 filter the rectifier output.

5. The wiring and transformer secondary resistance limit the peak diode current.

   a. A shorted diode will blow the primary fuse.

6. Q1454 is the error amplifier.

   a. R1456 and R1459 set the +100V.

   b. R1458 and R1455 are the error sampling resistors.

   c. C1458 and R1457 improve regulator transient response.

   d. D1450 provides temperature compensation for the emitter base junction of Q1454.

7. Q1463 and Q1464 are Darlington connected, provide the needed gain to control the series regulator transistors.

   a. C1462, C1454, and C1453 limit the response of the regulator to low frequencies and reduce possibility of oscillations. High frequency variations above 50 kHz are not cancelled by the regulator.

      (1) C1454 feeds ripple back to the base of Q1463.

   b. D1466 protects the emitter base junction of Q1464.

8. Q1467 and Q1477 are the series regulators.

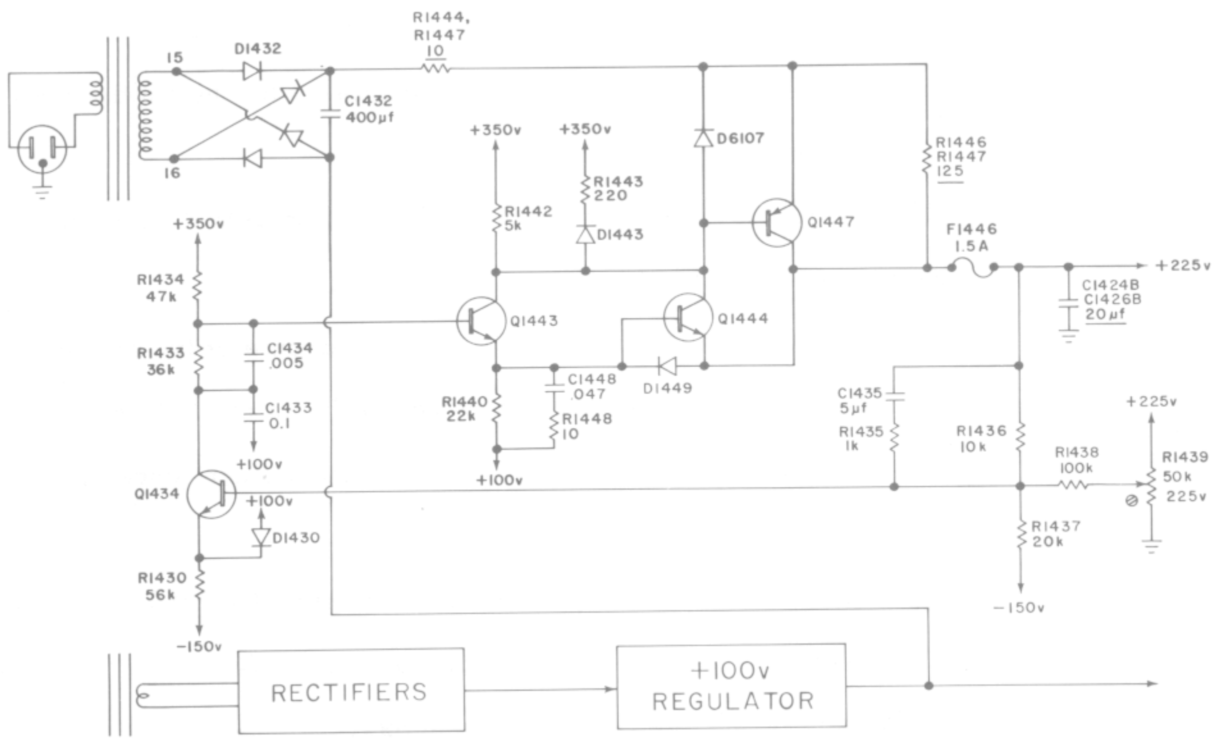
   a. D1469 and D1464 provide emitter-base protection for Q1467 and Q1477.

   b. R1469 and R1464 limit current through saturated Q1467 and A1477 when power supply output is shorted until F1478 blows.

   c. R1476, R1477 and R1478 bypass part of the supply output current around the regulator transistors.

   d. Current through Q1467 and Q1477 and the shunt resistors total about 1.8 Amps with about 800 mA through F1478.

G. +225V Supply



TYPE 556 POWER SUPPLY
+225v SUPPLY

B-556-0239
2-9-66jg

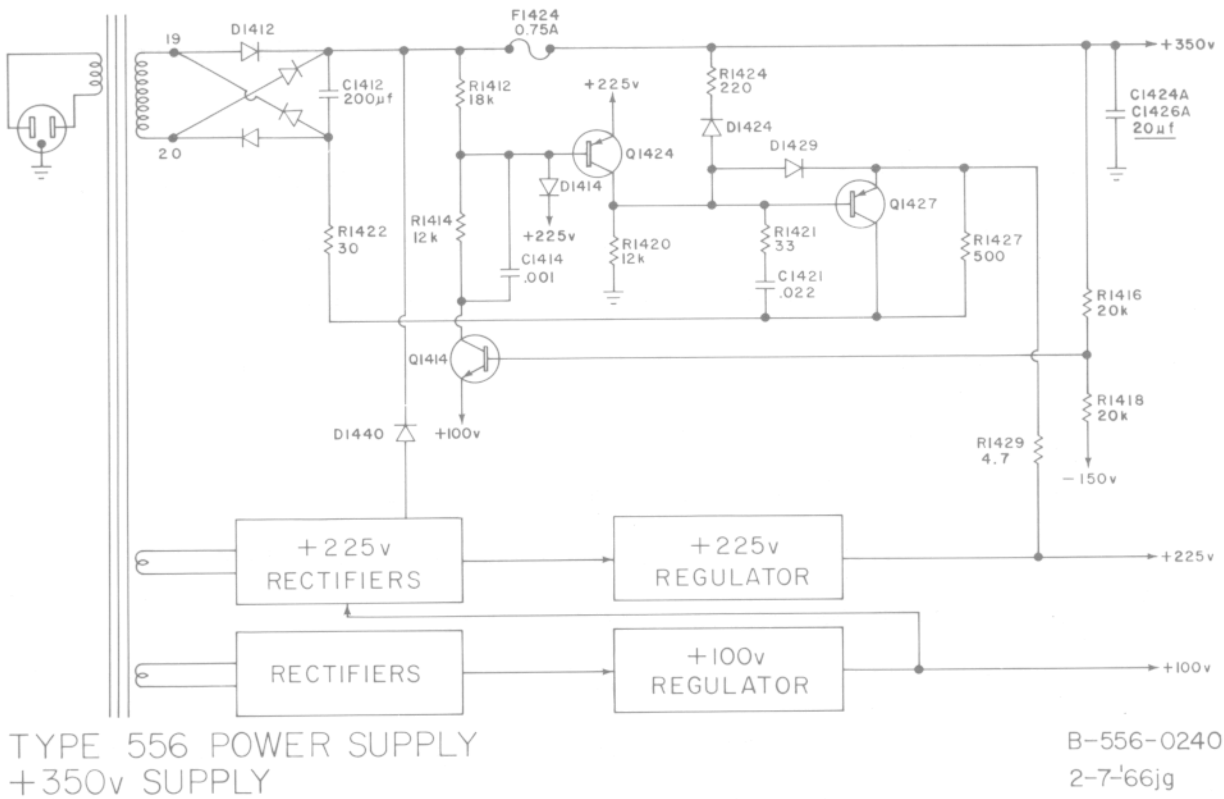
1. The +225V supply is stacked on the +100V regulated supply before the fuse.

   a. The +225V supply is stacked on the regulated supply to keep variations across Q1447 below 80V with high line voltage.

   b. Stacking on the unregulated supply would exceed this limit.

2. R1436 and R1437 are the voltage error sensing dividers for error amplifier Q1434.
   a. C1435 and R1435 improve regulator transient response.
   b. C1424B and C1426B shunt high frequency variations from the load to the ground.
3. Q1434 is the error amplifier. D1430 provides temperature compensation.
4. C1448, C1433 and C1434 reduce the frequency response of the regulator circuit to low frequencies only (below 50 kHz).
5. Q1443 and Q1444 are Darlington connected amplifiers which control series transistor Q1447.
   a. C1435 compensates the sensing divider.
   b. D1449 provides emitter-base protection for Q1444.
6. Q1447 is the series regulator transistor.
   a. D1444 provides emitter-base protection.
   b. R1444 and R1447 provide saturation current limiting for Q1447 until F1446 blows when the supply output is shorted.
   c. R1445 and R1446 shunt part of the supply current around Q1447.
7. The +225V winding is rated 130V at 1 Amp.
   a. A bridge rectifier provides 168 volts across filter capacitor C1432 at 115 line volts.
   b. The bridge rectifiers are 1N3194's rated at 0.75A, 400 P.I.V. (152-066).

H. +350V Supply



1. A 126V, 350 mA winding supplies 155V at 115 line volts.

   a. C1412 filters the output voltage.

   b. The bridge rectifiers are 152-066 in 13194's rated at 400 P.I.V., 0.75A.

   c. The supply is stacked on the regulated +225V supply to reduce variations across Q1427 with line voltage changes.

2. R1416 and R1418 are the error sampling resistors.
   a. Q1414 is the error amplifier.
   b. C1414 limits regulator frequency response.
3. Q1424 is an amplifier which drives the series regulator Q1427.
   a. D1414 protects the emitter-base junction of Q1424.
   b. R1429 provides a voltage drop which gives Q1424 an operating voltage.
4. Q1427 is the series regulator.
   a. D1429 protects the base-emitter junction of Q1427.
   b. R1421 and C1421 provide compensation to prevent oscillation of the regulator by limiting high frequency response.
   c. R1427 is a current shunt.
   d. R1422 limits saturation current through Q1427 until F1424 blows when the output of the 350V supply is shorted.
   e. D1440 keeps the +350V supply from going below the +225 unregulated voltage in case the supply blows a fuse. Otherwise the transistors in the +350V supply could be damaged.

I. Other Supplies

1. The +10V is obtained from a +10V zener in the long tail circuit of the vertical output stages. The +10V supply drives light bulbs and reed switches.

2. +6V supply which comes from the rectified output of terminals 9, 10, 11 and 12 of the power transformer.
   a. D1434 and D1436 rectify the output.
   b. C1435 filters the output.
   c. There is no tolerance on this supply.
   d. This supply is used for driving reeds and lamps.

J. Short Protection

1. If the +350V supply is shorted, R1424 and D1424 will cause Q1427 to saturate and thereby protect it.
   a. R1443 and D1443 will also cause Q1447 to saturate.
   b. R1472 and D1472 will also cause Q1467 and Q1477 to saturate.
2. Shorting of any stacked supply will also cause the supplies it is stacked on to protect themselves.
3. R1435 and R1457 protect Q1434 and Q1454 from excessive reverse current through the electrolytics if the respective supplies are shorted and the fuse blows.
4. Each supply is fused in addition to a primary fuse.

X. CALIBRATOR

A. The calibrator supplies 1 kHz square wave to the front panel jack (BNC).

1. 18 steps from .2 mV to 100V.
2. 100V DC.
3. 5 mA square wave through a current loop.
4. 5 mA DC through a current loop.

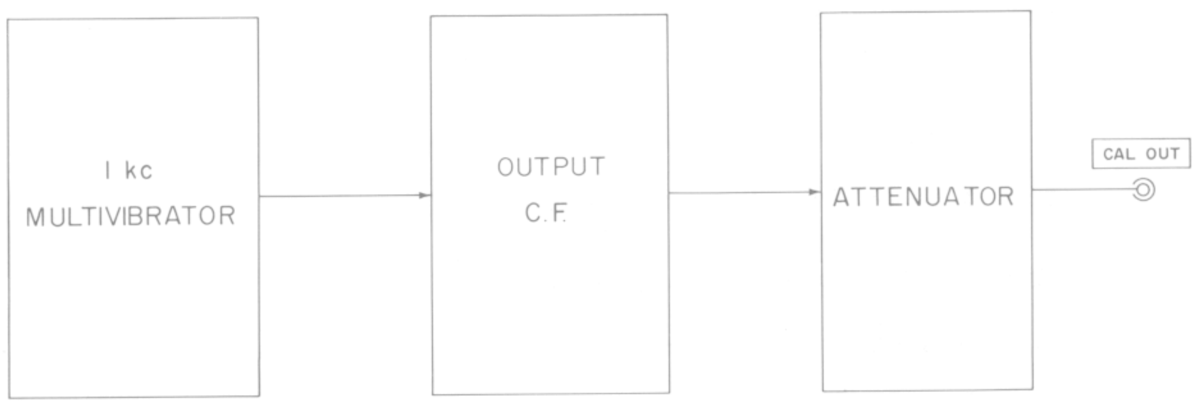
B. Operating Characteristics (Factory Spec)

1. Frequency approximately 1 kHz (±25%).
2. Duty factor 45% to 55%.
3. Output voltage:
   a. 0.2 mV to 50V ±2%.
   b. 100V DC and 100V square wave ±1%.
4. Risetime ≤1.5 μs.

C. Output Impedance

1. 50Ω in 0.2 mV to 200 mV positions.
   a. A 50Ω load will reduce the amplitude by one-half.
2. Impedance increasing to 4k at 50V.
3. 150Ω in 100V (AC and DC positions).
4. Accuracy of 50Ω impedance ±2%.

D. Block Diagram



TYPE 556 CALIBRATOR
BLOCK DIAGRAM

B-556-0241
2-1-'66jg

E. Block Logic

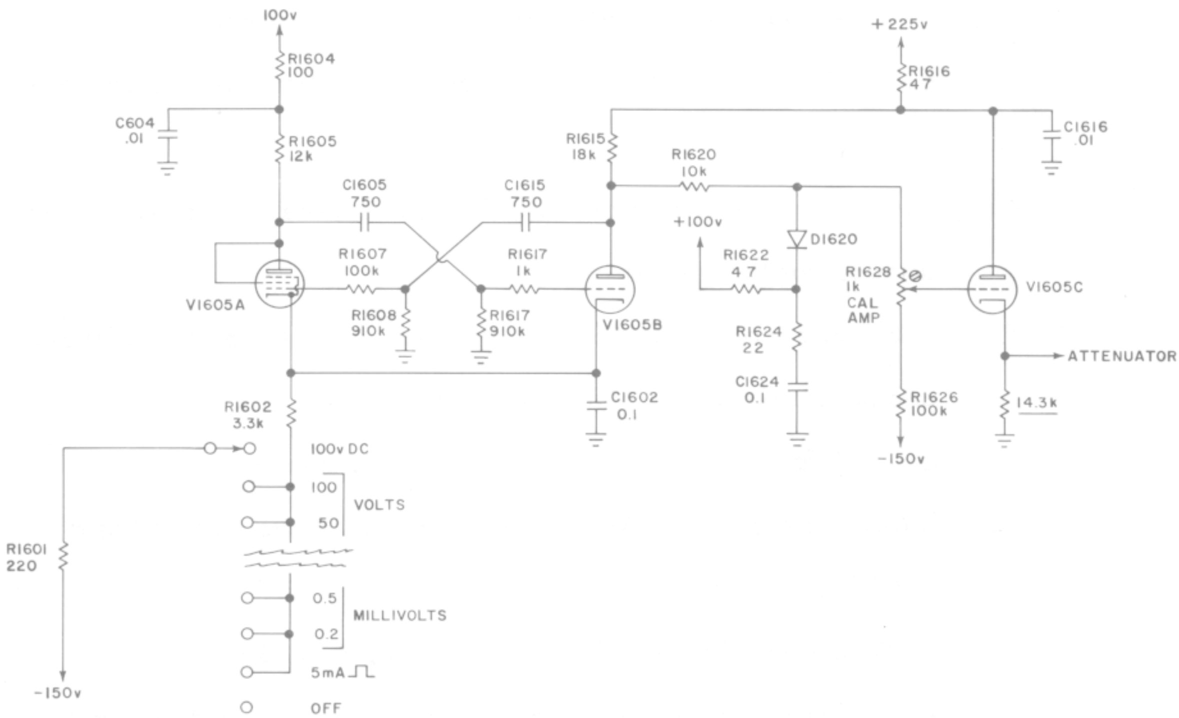
1. The calibrator circuit consists of a 1 kHz astable multivibrator driving an output CF.

2. The output is clamped at ground and 100V to provide a precise 100V peak-to-peak square wave.

3. A precision attenuator using 1% and 1/4% resistors attenuates the calibrator voltage for use at the Cal Out jack.

F. Multivibrator

1. The multivibrator is a symmetrical 1 kHz plate coupled astable multi using a three section 6M11 compactron.



TYPE 556 CALIBRATOR
MULTIVIBRATOR

B-556-0242
2-3-'66jg

2. The multi circuit follows basic design in that a triode and a triode connected pentode are used to get a symmetrical output.

3. The grids are returned to ground making the multi switching less susceptible to noise.

4. The compactron has a maximum 100V cathode to filament rating so the full -150V supply couldn't be used. R1602 is used to reduce the cathode voltage.

5. The pentode section, V1605A is triode connected. It has a low plate resistor, R1605, so it draws the same current as V1605B.

   a. Constant current is drawn through R1602 from the -150V supply so there is very little signal developed across it.

   b. The cathode is bypassed to ground to eliminate any possible signal.

6. R1601 is in the circuit because the 556 uses the 547 cal switch which already has the resistor on it.

7. R1607 is a large value to allow the plate of V1605B to rise quickly and not be limited by V1605A grid current.

   a. A fast rising calibrator waveshape is assured.

8. V1605A plate has a +100V to -60V swing. V1605B plate has a +145V to -70V swing.

9. V1605C is a cathode follower with a very high Gm.

   a. The actual voltage from grid to cathode is about one volt.

   b. Small bias keeps the calibrator output constant with age.

10. R1628 (cal amp) provides a variable 2V offset adjustment for the grid of V1605C making it possible to set the cathode to exactly 100V.

    a. The 100V supply is well stabilized and adjustable so it helps the calibrator give an accurage output voltage.

    b. Any change in the 100V supply will also change the calibrator output voltage.

11. The output waveform is shaped when the grid of V1605C is caught at 100V by D1620 as the plate of V1605B rises, and when the cathode of V1605C reaches ground as its grid is driven negative.

12. V1605C cathode returns to ground through an equivalent 14.3k in the hundred volt positions of the calibrator switch.

    a. A total of 7 mA flows through the cathode follower.

13. Decoupling keeps switching transients out of the power supply.

    a. R1601, R1602, and C1602 decouple from the -150V supply.

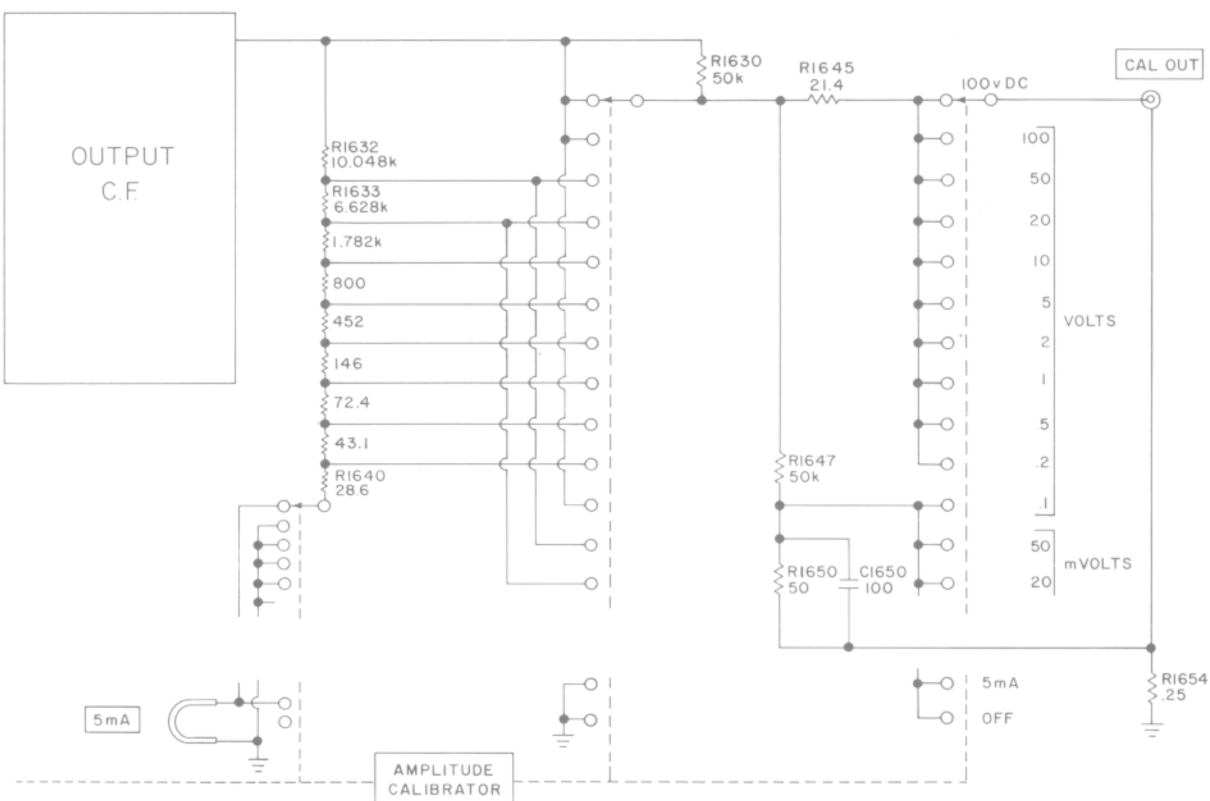
    b. R1604, C1604 decouple the +100V supply.

    c. R1616, C1616 decouple from the +225V supply.

    d. R1622, R1624, C1624 prevent a ringing and add decoupling from the +100V supply.

G. Attenuator

1. The attenuator divides the 100V square wave to the one current and 18 voltage positions.



TYPE 556 CALIBRATOR
ATTENUATOR

B-556-0243
2-1-'66jg

2. 100V DC position.

   a. The cathode supply to the multivibrator is opened.

   b. The output is clamped at 100V by D1620.

   c. The 20k divider composed of R1632 through R1640 supplies 5 mA cathode current to V1605C.

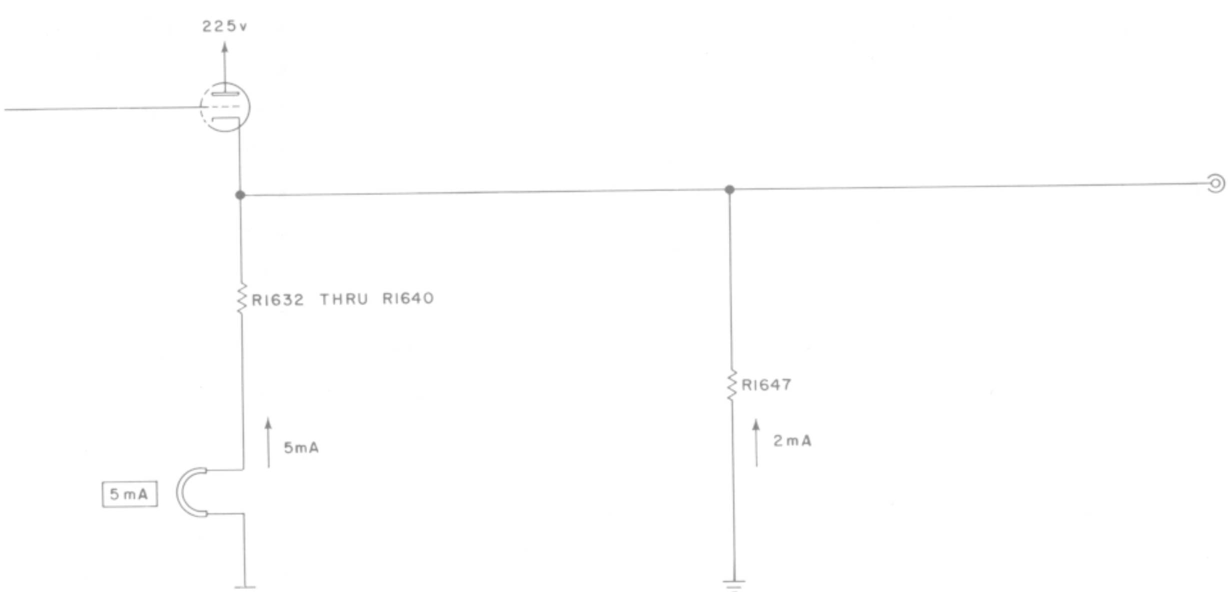
      (1) The divider returns to ground through a front panel current loop to provide 5 mA DC.

3. 100V square wave position.

   a. The 100V peak-to-peak square wave is connected directly to the CAL OUT jack.

   b. R1630 is shorted out.

4. In both 100V positions of the CAL switch, 5 mA flows through the divider and 2 mA flows through R1647.



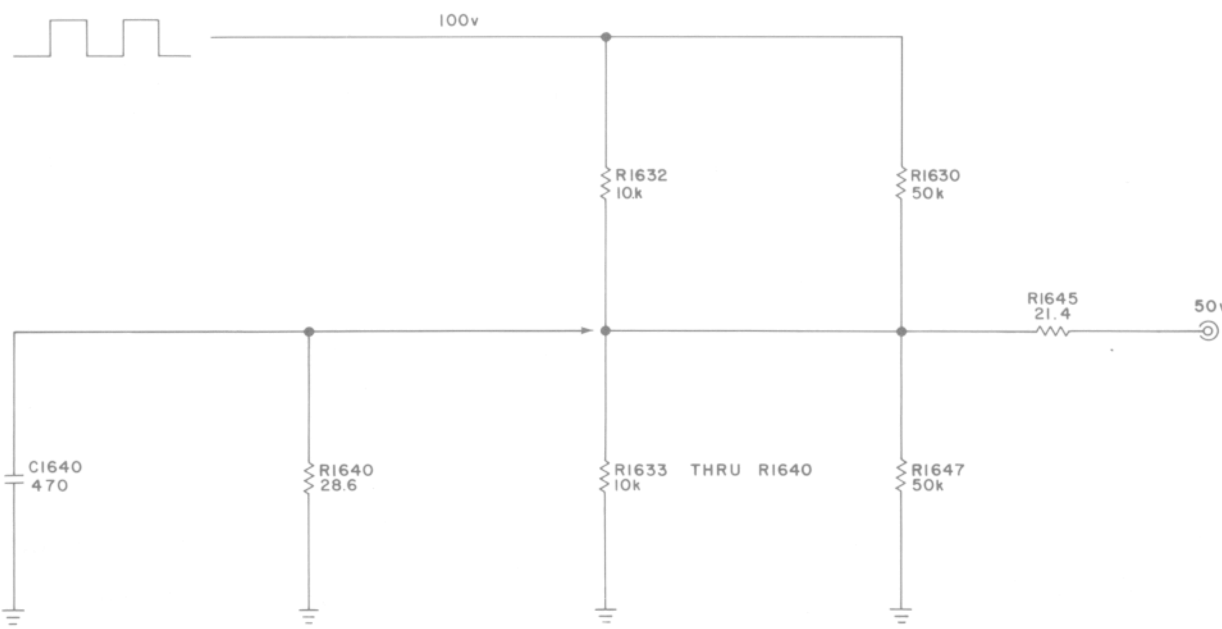
TYPE 556 CALIBRATOR
100v POSITIONS

B-556-0244
2-2-66jg

a. Output impedance is about 150Ω.

(1) Cathode transimpedance shunted by 14k.

5. .2V to 50V positions.



TYPE 556 CALIBRATOR
50v POSITION

B-556-0245
2-1-66jg

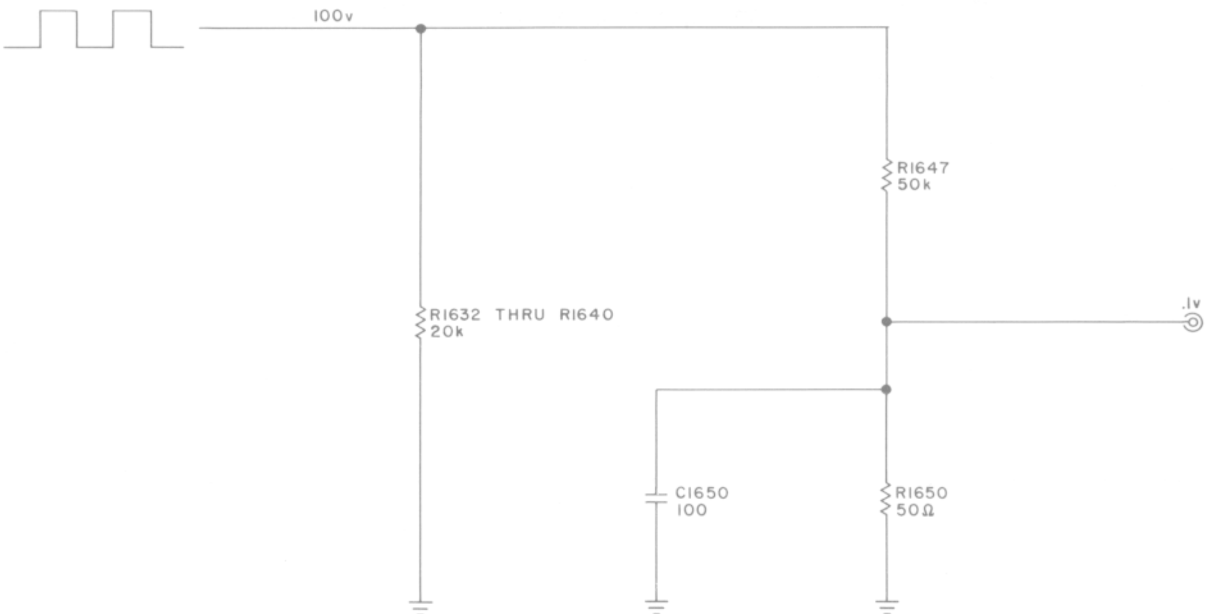
a. Taps on the divider R1632 through R1640 provide the voltage divisions.

b. In the .2V position, R1645 adds to R1640 to provide 50Ω output impedance.

c. C1640 (from R1640 to ground) compensates the low impedance tap to prevent overshoot in the .2V position.

d. Impedance at switch positions .5V through 50V increase in impedance to about 4k at the 50V positions.

6. .1V position.



TYPE 556 CALIBRATOR
.1v POSITION

B-556-0246
2-1-66jg

a. R1630 is shorted out.

b. R1647 and R1650 form a 1000:1 divider.

c. R1650 provides 50Ω output impedance.

d. C1650 compensates the low impedance portion of the divider to prevent overshoot.

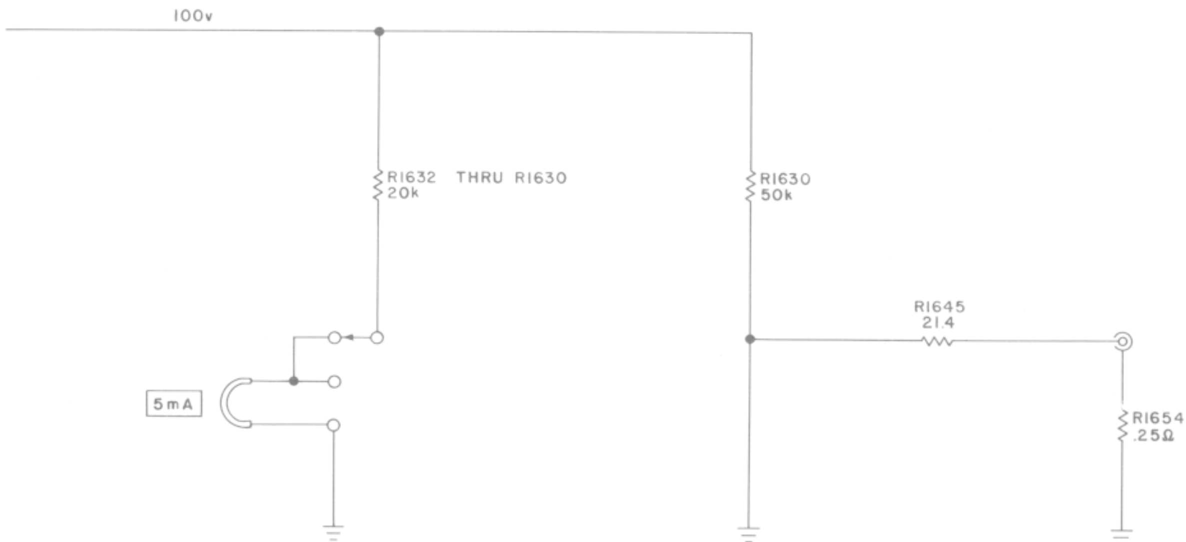
7. .2 mV to 50 mV positions.

a. These millivolt positions use the same taps on R1633 through R1640 as the corresponding voltage positions.

b. The square wave at volts amplitude is then divided to millivolts by R1647 and R1650.

c. Output impedance is 50Ω.

d. C1650 compensates the low end of the divider.



TYPE 556 CALIBRATOR
5mA POSITION

B-556-0247
2-1-66jg

8. 5 mA position.

   a. Current through the divider 20k string provides a 5 mA square wave through the current loop.

   b. The current loop is provided primarily to calibrate a current probe.

   c. The CAL OUT is disconnected in this position preventing accidental loading of the current square wave.

9. R1654 placed between the CAL OUT jack ground return and ground breaks up ground loops in the system when a coax is used at the CAL OUT jack.

SLIDE LIST

Vertical Amplifier

B-556- 0200
0201
0202
0203
0204

Sweep Triggers

B-556- 0205
0206
0207
0208
0209

Sweep Generators

B-556- 0210
0211.1
0212
0211.2
0213
0214
0215
0216
0217
0218
0219

Delay Pick-Off

B-556- 0220
0221
0222

Alternate Trace Logic

B-556- 0223

Multi Trace Sync Amplifier

B-556- 0224

Horizontal Amplifier

B-556- 0225
0226
0227
0228
0229
0230

CRT Circuit

B-556- 0231
0232
0233
0234

Power Supply

B-556- 0235
0236
0237
0238
0239
0240

Calibrator

B-556- 0241
0242
0243
0244
0245
0246
0247

SCHEMATIC SLIDES

556	A Sweep Generator (M)	C-556-0005
556	A Sweep Timing Switch (M)	C-556-0010
556	A Sweep Trigger (M)	C-556-0015
556	Alternate Trace Logic and Blanking (M)	C-556-0020
556	B Sweep Generator (M)	C-556-0025
556	B Sweep Timing Switch (M)	C-556-0030
556	B Sweep Trigger (M)	C-556-0035
556	Calibrator (M)	C-556-0040
556	CRT Circuit (M)	C-556-0045
556	Delay Pickoff (M)	C-556-0050
556	Heater Wiring (M)	C-556-0055
556	Left Vertical Amplifier (M)	C-556-0060
556	Lower Beam Horizontal Amplifier (M)	C-556-0065
556	Plug-In Jack Details (M)	C-556-0070
556	Power Supply (M)	C-556-0075
556	Right Vertical Amplifier (M)	C-556-0080
556	Upper Beam Horizontal Amplifier (M)	C-556-0085

IMPORTANT

VOLTAGE AND WAVEFORM CONDITIONS

Circuit voltages were measured with a 20,000 Ω/V DC VOM. All readings are in volts. Voltages were measured with respect to ground unless otherwise indicated.

Waveforms shown are actual waveform photographs taken with a Tektronix Oscilloscope Camera equipped with a projected graticule.

Voltages and waveforms on the schematics (shown in blue) are not absolute and may vary between instruments. Any apparent differences between the voltage levels measured with the voltmeter and those shown on the waveforms are due to such causes as circuit loading of the voltmeter, different conditions and measurement resolution.

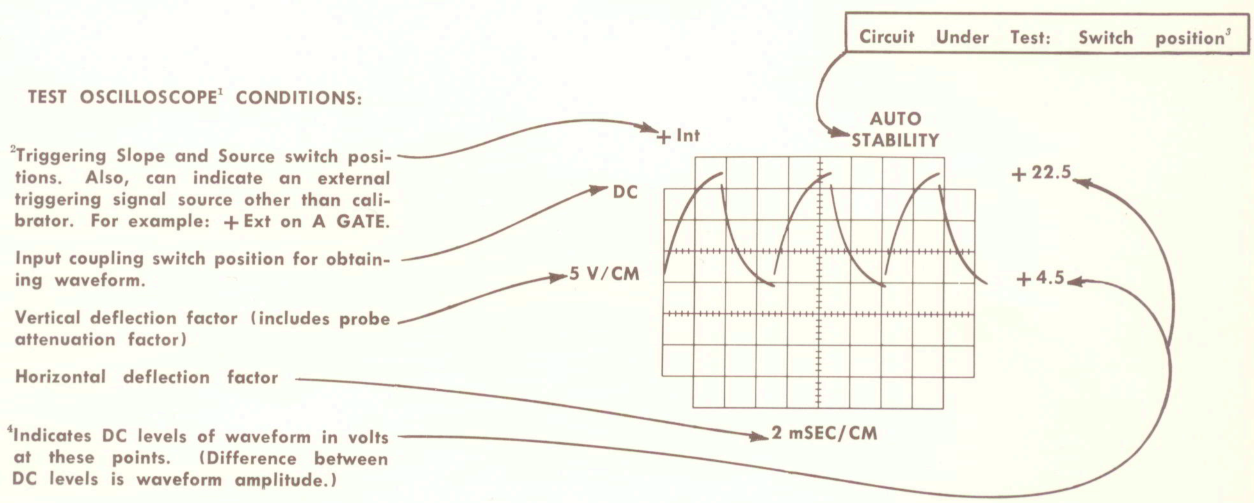
Note that two types of graticules appear on the schematic diagram (also, see Fig. 4-10 in the Maintenance section). The 6 × 10 cm graticule identifies the separate test oscilloscope used for signal tracing and the 8 × 10 cm graticule identifies the Type 556. The Type 556 was used to signal trace its own circuits except for the Alternate Trace Logic and Lower Beam CRT circuits. A separate test oscilloscope was needed to signal trace these circuits.

The waveforms were obtained using a plug-in and 10× probe that gave the test oscilloscope/plug-in/probe system the following characteristics: Minimum deflection factor of 0.05 V/cm using a 10× probe; frequency response of DC to 10 MHz or higher. For most waveforms, +Ext triggering (on the Type 556 Amplitude Calibrator 2-V peak-to-peak signal, A GATE, or B GATE) and AC vertical-input coupling was used to show waveform amplitudes, time relationship and polarity; DC coupling was used to obtain the instantaneous DC levels when practical. The following illustration shows how to interpret the information given around the waveform.

CAUTION

When troubleshooting the circuits, be sure the probe tip or test prods can be used in tight places without causing an accidental short circuit. If care is not used, a short circuit can cause damage to several semiconductors, particularly in the vertical amplifiers.

Any letter-series or 1-series type of vertical preamplifier plug-in unit can be used in the Type 556 Oscilloscope section under test when troubleshooting that section. Voltages and waveforms were obtained under the following general conditions. Use these conditions in addition to those found on the individual diagram.



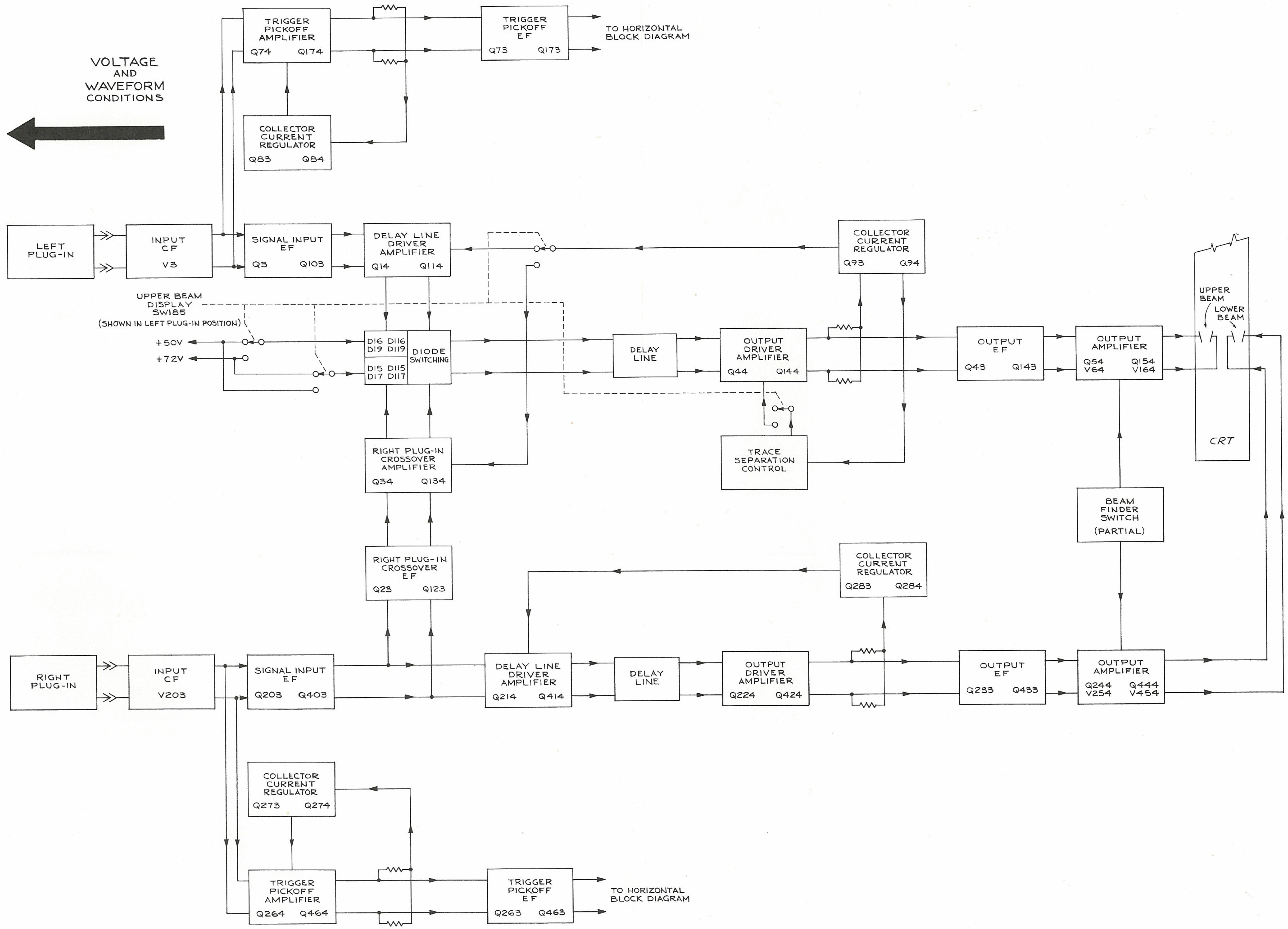
[1]The term "test oscilloscope" is the oscilloscope used for signal tracing. It can be either the separate oscilloscope or the one section of the Type 556 used to signal trace the other section as previously explained.

[2]Triggering conditions that differ from +Ext triggering on 2-V calibrator signal.

[3]Switch position that differs from established conditions for whole diagram.

[4]Omitted if DC levels are high and waveform is too low in amplitude to determine actual levels. For approximate DC level use the voltmeter reading given at the same circuit test point.

(Cont'd on Horizontal Block Diagram)


VOLTAGE AND WAVEFORM CONDITIONS
TRIGGER PICKOFF AMPLIFIER Q74 Q174
TRIGGER PICKOFF EF Q73 Q173
TO HORIZONTAL BLOCK DIAGRAM
COLLECTOR CURRENT REGULATOR Q83 Q84
LEFT PLUG-IN
INPUT CF V3
SIGNAL INPUT EF Q3 Q103
DELAY LINE DRIVER AMPLIFIER Q14 Q114
COLLECTOR CURRENT REGULATOR Q93 Q94
UPPER BEAM DISPLAY SW185
(SHOWN IN LEFT PLUG-IN POSITION)
+50V
+72V
D16 D116 D19 D119
D15 D115 D17 D117
DIODE SWITCHING
DELAY LINE
OUTPUT DRIVER AMPLIFIER Q44 Q144
OUTPUT EF Q43 Q143
OUTPUT AMPLIFIER Q54 Q154 V64 V164
UPPER BEAM
LOWER BEAM
CRT
TRACE SEPARATION CONTROL
RIGHT PLUG-IN CROSSOVER AMPLIFIER Q34 Q134
BEAM FINDER SWITCH (PARTIAL)
RIGHT PLUG-IN CROSSOVER EF Q23 Q123
COLLECTOR CURRENT REGULATOR Q283 Q284
RIGHT PLUG-IN
INPUT CF V203
SIGNAL INPUT EF Q203 Q403
DELAY LINE DRIVER AMPLIFIER Q214 Q414
DELAY LINE
OUTPUT DRIVER AMPLIFIER Q224 Q424
OUTPUT EF Q233 Q433
OUTPUT AMPLIFIER Q244 Q444 V254 V454
COLLECTOR CURRENT REGULATOR Q273 Q274
TRIGGER PICKOFF AMPLIFIER Q264 Q464
TRIGGER PICKOFF EF Q263 Q463
TO HORIZONTAL BLOCK DIAGRAM

MRH
666

Conditions for section of Type 556 under test[1]; i.e., Upper Beam or Lower Beam, whichever applies:

Plug-In Unit

Input signal for obtaining:	
Voltage readings[2]	See individual diagram
Waveforms	2-V peak to peak from Type 556 Amplitude Calibrator
Input coupling for calibrator signal	AC
Deflection Factor	1 V/cm
Vertical Position	Centered[3]

Triggering Controls

SOURCE	See individual diagram where applicable
COUPLING	AC
SLOPE	+
MODE	TRIG[4]
LEVEL	≈20° cw from 0[5] (knob pushed in)

Upper or Lower Beam Controls

DISPLAY	See individual diagram where applicable
POSITION	As is except for diagrams ⟨11⟩ and ⟨12⟩
DISPLAY MAG	×1

A or B TIME/CM Controls

VARIABLE	CALIBRATED
A TIME/CM	.1 mSEC
B TIME/CM	.1 mSEC[6]
A or B MODE switches	See individual diagram where applicable

CRT Controls

INTENSITY	ccw[7]
FOCUS	As is except centered for diagram ⟨13⟩
ASTIGMATISM	As is except centered for diagram ⟨13⟩

Lower Center-Panel Controls

UPPER BEAM EXT HORIZ	cw
LOWER BEAM EXT HORIZ	cw
TRACE ROTATION	As is
TRACE SEPARATION	Centered
SCALE ILLUM	As desired
DELAY-TIME MULTIPLIER	3.00
BEAM LOCATE	As is
AMPLITUDE CALIBRATOR	2 VOLTS
POWER	ON

Upper or Lower Beam Rear-Panel Conditions

CRT Cathode Selector	EXT CRT CATHODE
EXT CRT CATHODE connector	Shorting cover connected
Line Voltage	115 V

[1]Exception: Conditions apply to both sides for diagram ⟨10⟩.

[2]No signal is applied to some circuits under test to establish quiescent conditions for obtaining voltage readings.

[3]Set for 0 V between vertical deflection plate pins for diagrams ⟨1⟩ and ⟨2⟩.

[4]B Triggering MODE set to AUTO STABILITY for diagram ⟨10⟩ voltages.

[5]For exceptions see individual diagrams where applicable.

[6]Set to 50 µSEC for diagram ⟨10⟩.

[7]For section under test beam; so the display obtained by the other beam (used for signal tracing) can be photographed. If desired, the section under test beam can be set for normal brightness so a dual-beam display can be obtained for all diagrams except diagram ⟨13⟩.

Schematic Symbols

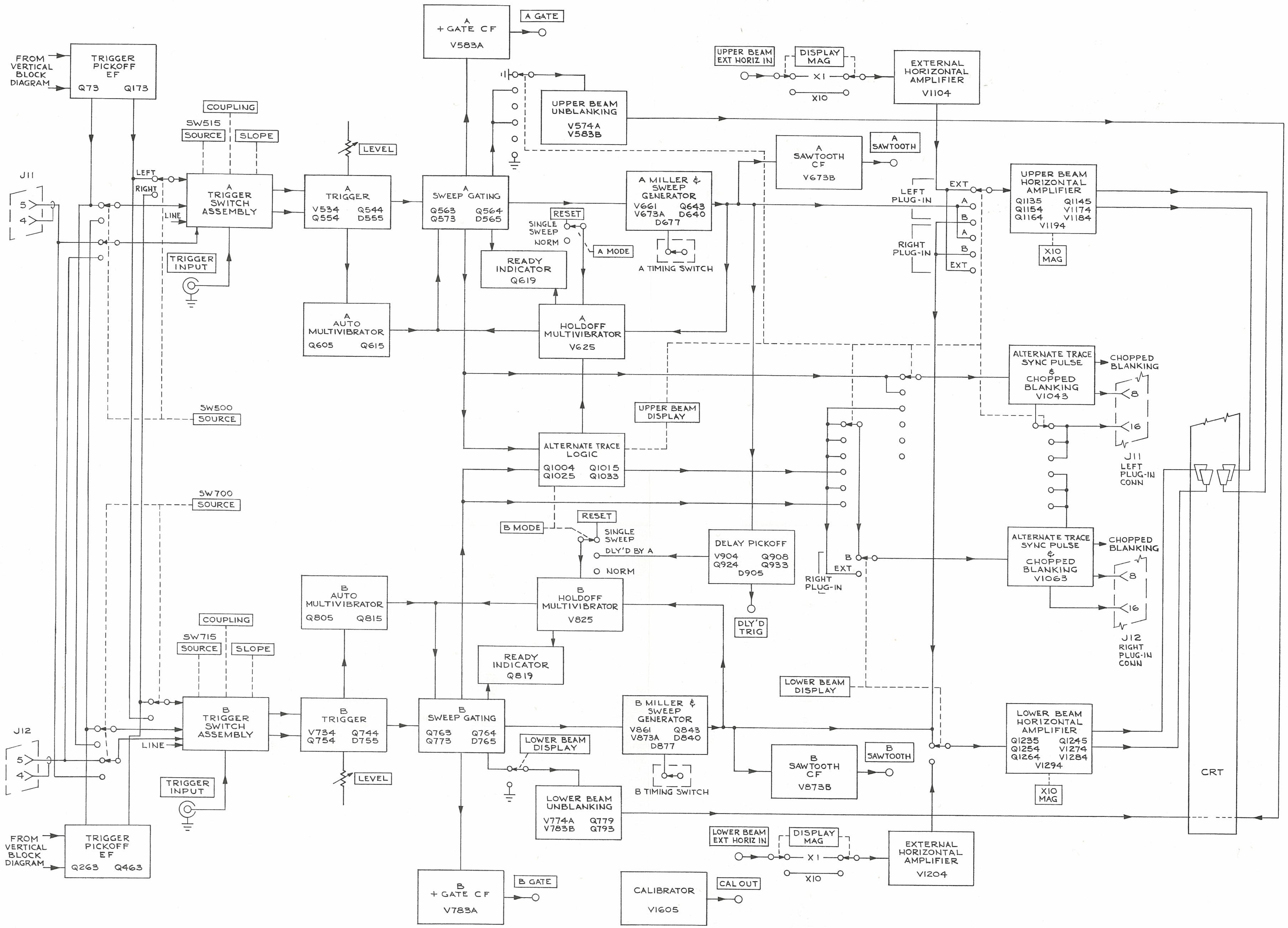
The following symbols are used on the schematics:

Screwdriver adjustment

Front-panel control or connector.

Connection made at indicated pin on circuit board.

Blue line encloses components located on circuit board.



TYPE 556 OSCILLOSCOPE

A1

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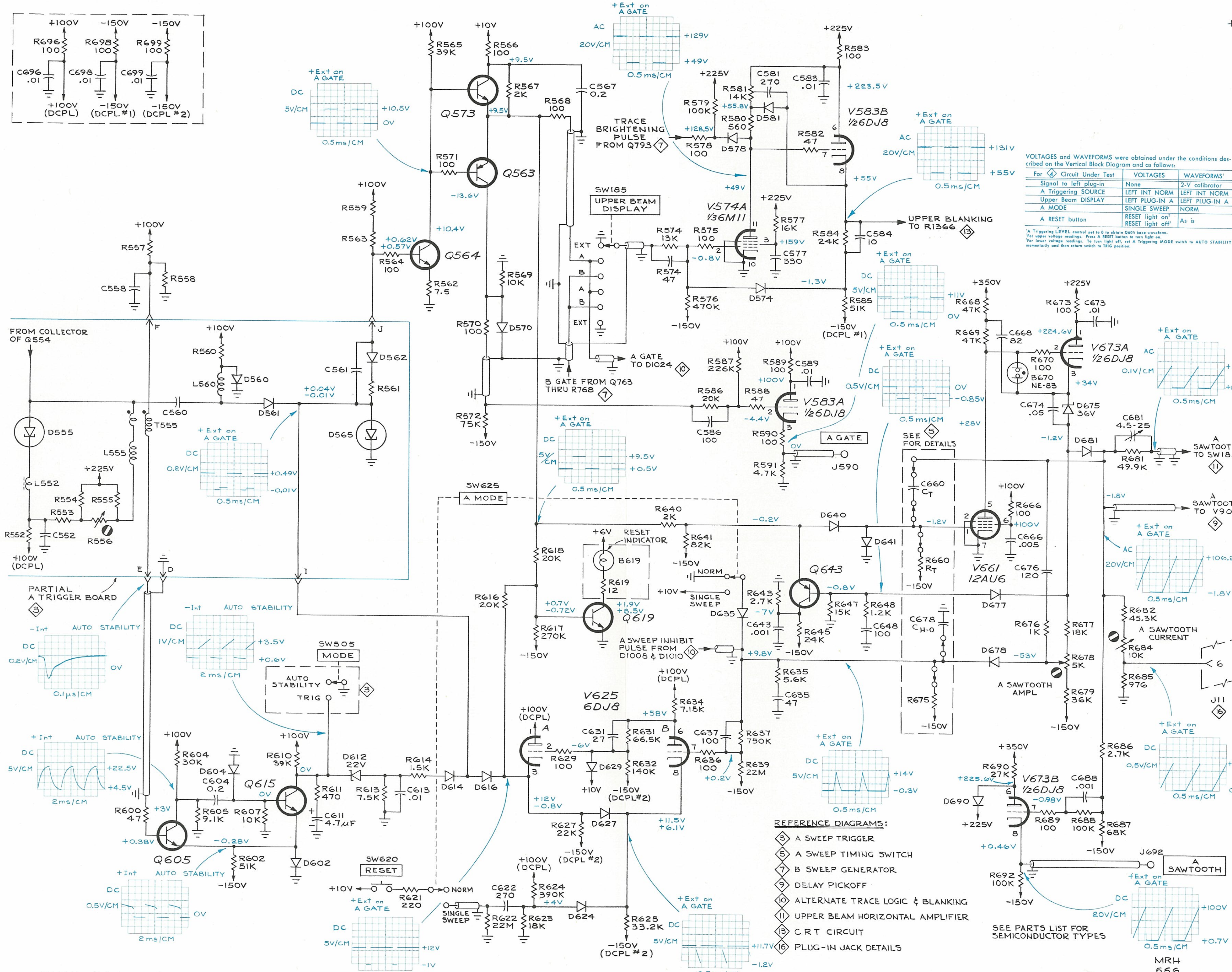
HORIZONTAL BLOCK DIAGRAM



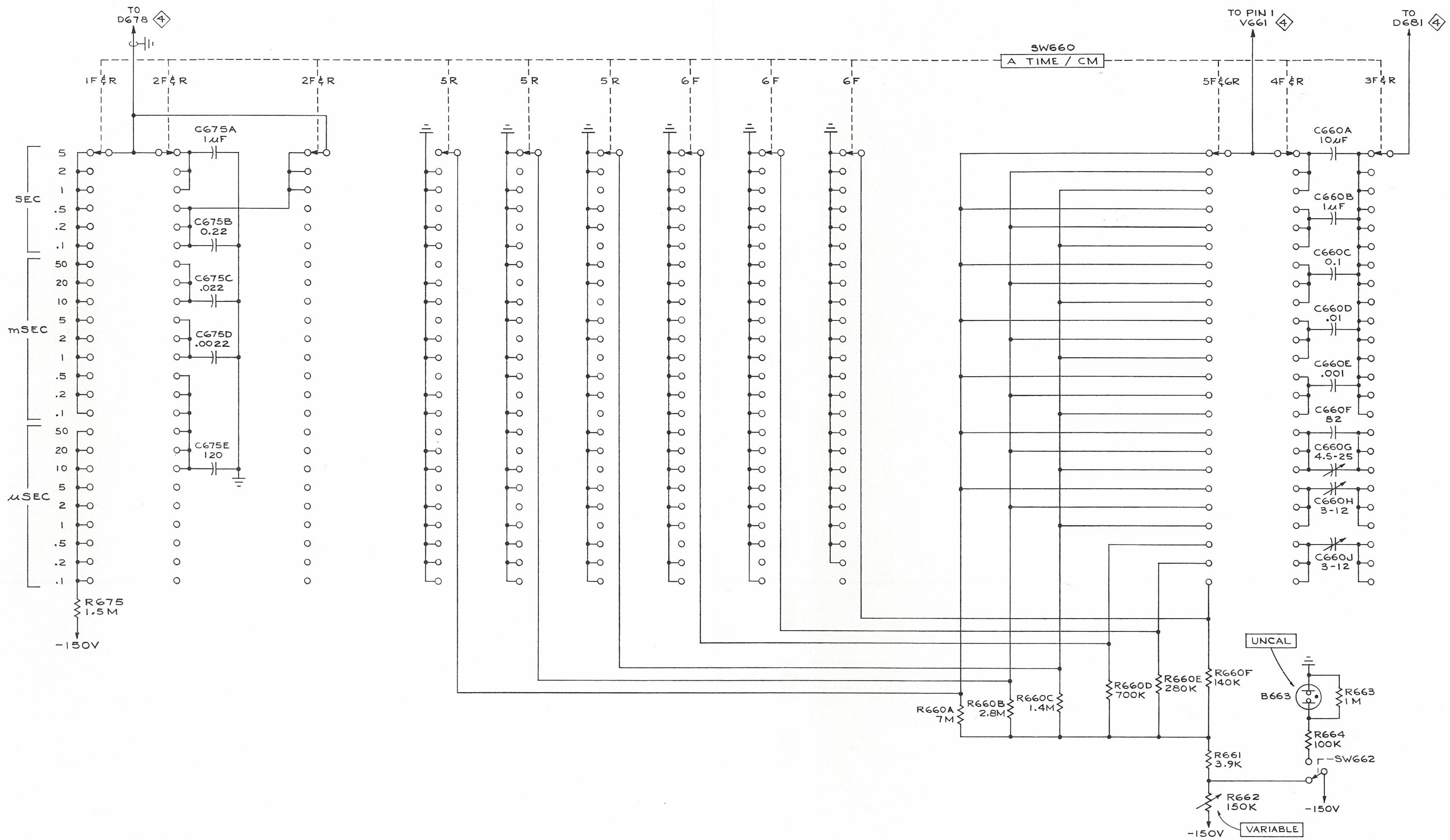
VOLTAGES and WAVEFORMS were obtained under the conditions described on the Vertical Block Diagram and as follows:

For ④ Circuit Under Test	VOLTAGES	WAVEFORMS[1]
Signal to left plug-in	None	2-V calibrator
A Triggering SOURCE	LEFT INT NORM	LEFT INT NORM
Upper Beam DISPLAY	LEFT PLUG-IN A	LEFT PLUG-IN A
A MODE	SINGLE SWEEP	NORM
A RESET button	RESET light on[2] RESET light off[3]	As is

[1] A Triggering LEVEL control set to 0 to obtain Q605 base waveform.
[2] For upper voltage readings. Press A RESET button to turn light on.
[3] For lower voltage readings. To turn light off, set A Triggering MODE switch to AUTO STABILITY momentarily and then return switch to TRIG position.

REFERENCE DIAGRAMS:

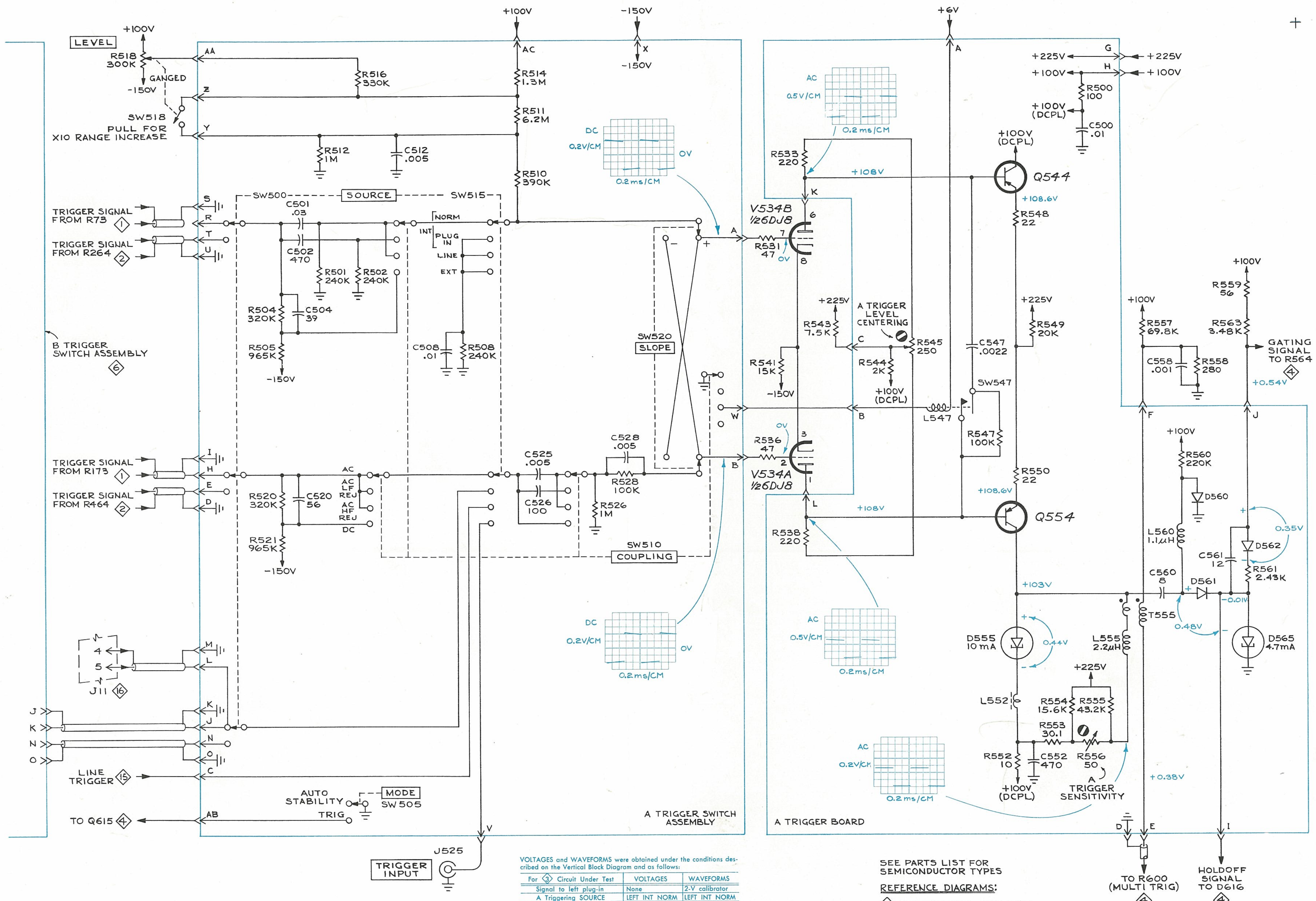
- ③ A SWEEP TRIGGER
- ⑤ A SWEEP TIMING SWITCH
- ⑦ B SWEEP GENERATOR
- ⑨ DELAY PICKOFF
- ⑩ ALTERNATE TRACE LOGIC & BLANKING
- ⑪ UPPER BEAM HORIZONTAL AMPLIFIER
- ⑬ CRT CIRCUIT
- ⑯ PLUG-IN JACK DETAILS



REFERENCE DIAGRAM:

4 A SWEEP GENERATOR

MRH
666



VOLTAGES and WAVEFORMS were obtained under the conditions described on the Vertical Block Diagram and as follows:

For ⟨3⟩ Circuit Under Test	VOLTAGES	WAVEFORMS
Signal to left plug-in	None	2-V calibrator
A Triggering SOURCE	LEFT INT NORM	LEFT INT NORM
A Triggering LEVEL	0[1]	≈20° cw from 0
A MODE	SINGLE SWEEP[2]	SINGLE SWEEP

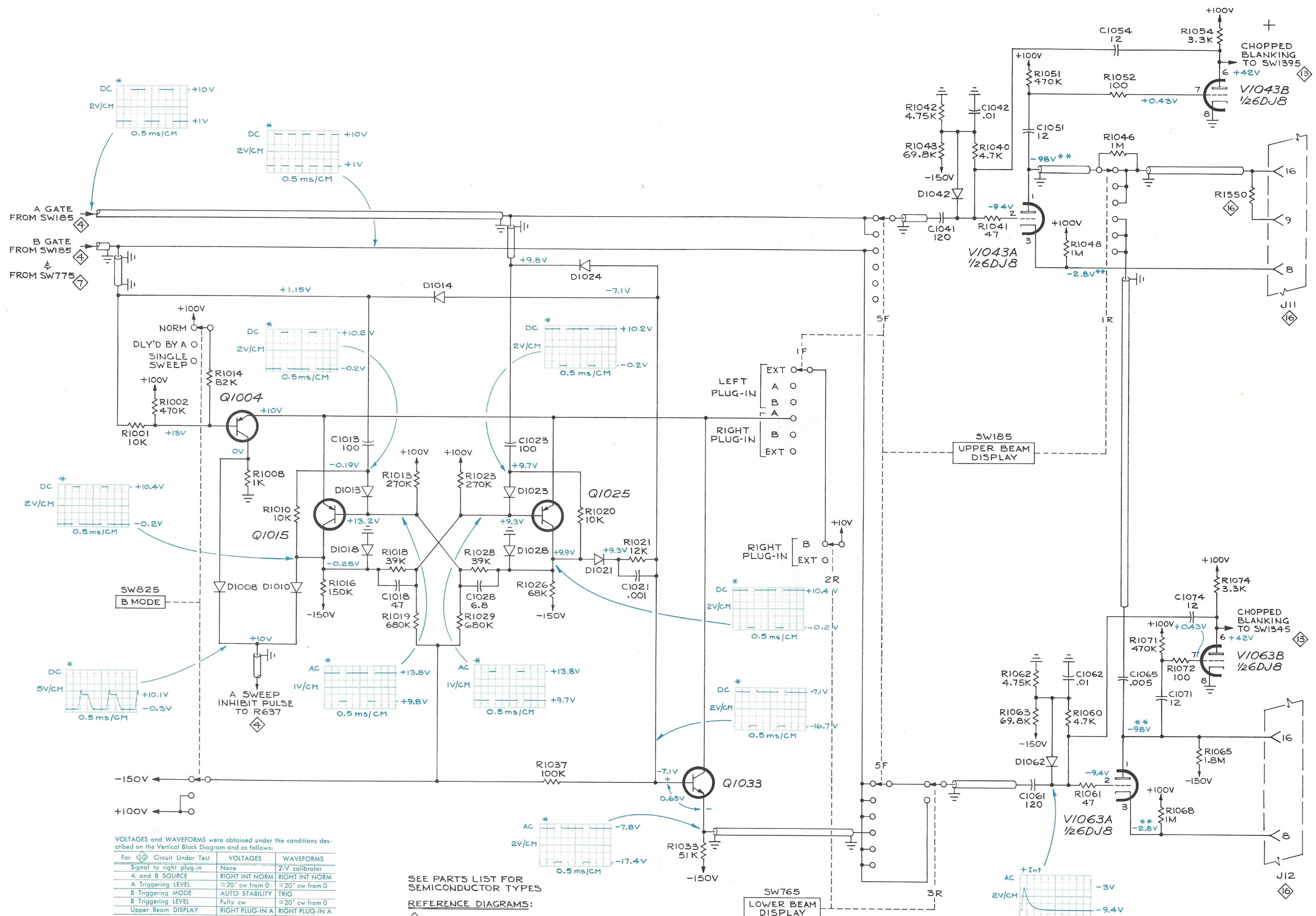
[1] Set for 0 V at pin 7 of V534B.
[2] A RESET light is off.

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

REFERENCE DIAGRAMS:

- ⟨1⟩ LEFT VERTICAL AMPLIFIER
- ⟨2⟩ RIGHT VERTICAL AMPLIFIER
- ⟨4⟩ A SWEEP GENERATOR
- ⟨6⟩ B SWEEP TRIGGER
- ⟨15⟩ HEATER WIRING
- ⟨16⟩ PLUG-IN JACK DETAILS

MRH 666



VOLTAGES and WAVEFORMS were obtained under the conditions described on the Vertical Block Diagram and as follows:

For ⟨10⟩ Circuit Under Test	VOLTAGES	WAVEFORMS
Signal to right plug-in	None	2-V calibrator
A and B SOURCE	RIGHT INT NORM	RIGHT INT NORM
A Triggering LEVEL	≈20° cw from 0	≈20° cw from 0
B Triggering MODE	AUTO STABILITY	TRIG
B Triggering LEVEL	Fully cw	≈20° cw from 0
Upper Beam DISPLAY	RIGHT PLUG-IN A	RIGHT PLUG-IN A
A TIME/CM	.1 mSEC	.1 mSEC
Lower Beam DISPLAY	RIGHT PLUG-IN B	RIGHT PLUG-IN B
B TIME/CM	50 μSEC	50 μSEC
A MODE	SINGLE SWEEP	NORM
B MODE	NORM	NORM
A and B RESET buttons	As is	As is

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

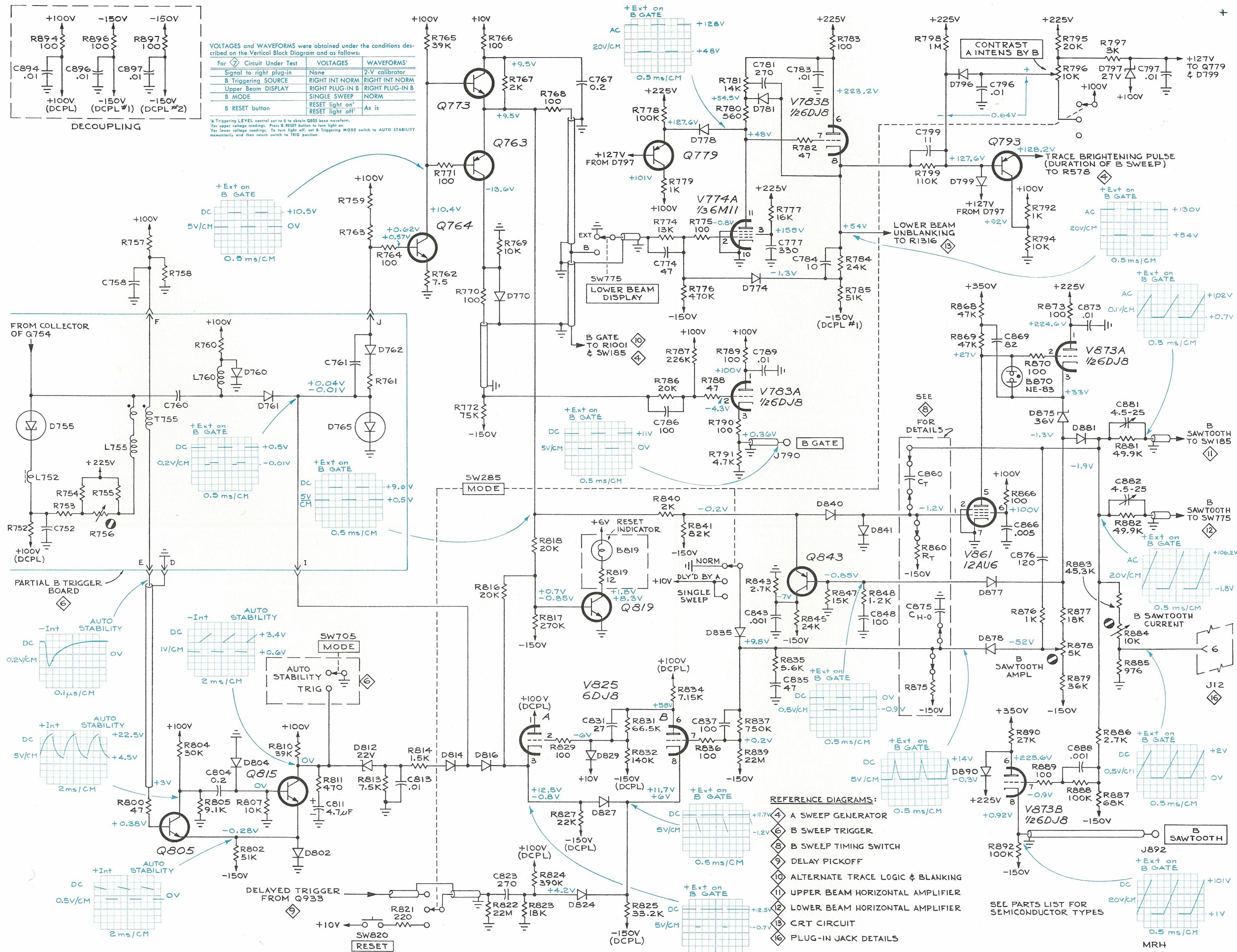
REFERENCE DIAGRAMS:

- ⟨4⟩ A SWEEP GENERATOR
- ⟨7⟩ B SWEEP GENERATOR
- ⟨13⟩ CRT CIRCUIT
- ⟨16⟩ PLUG-IN JACK DETAILS

* DENOTES +Ext on A GATE

** VOLTAGES DEPEND ON PLUG-IN USED

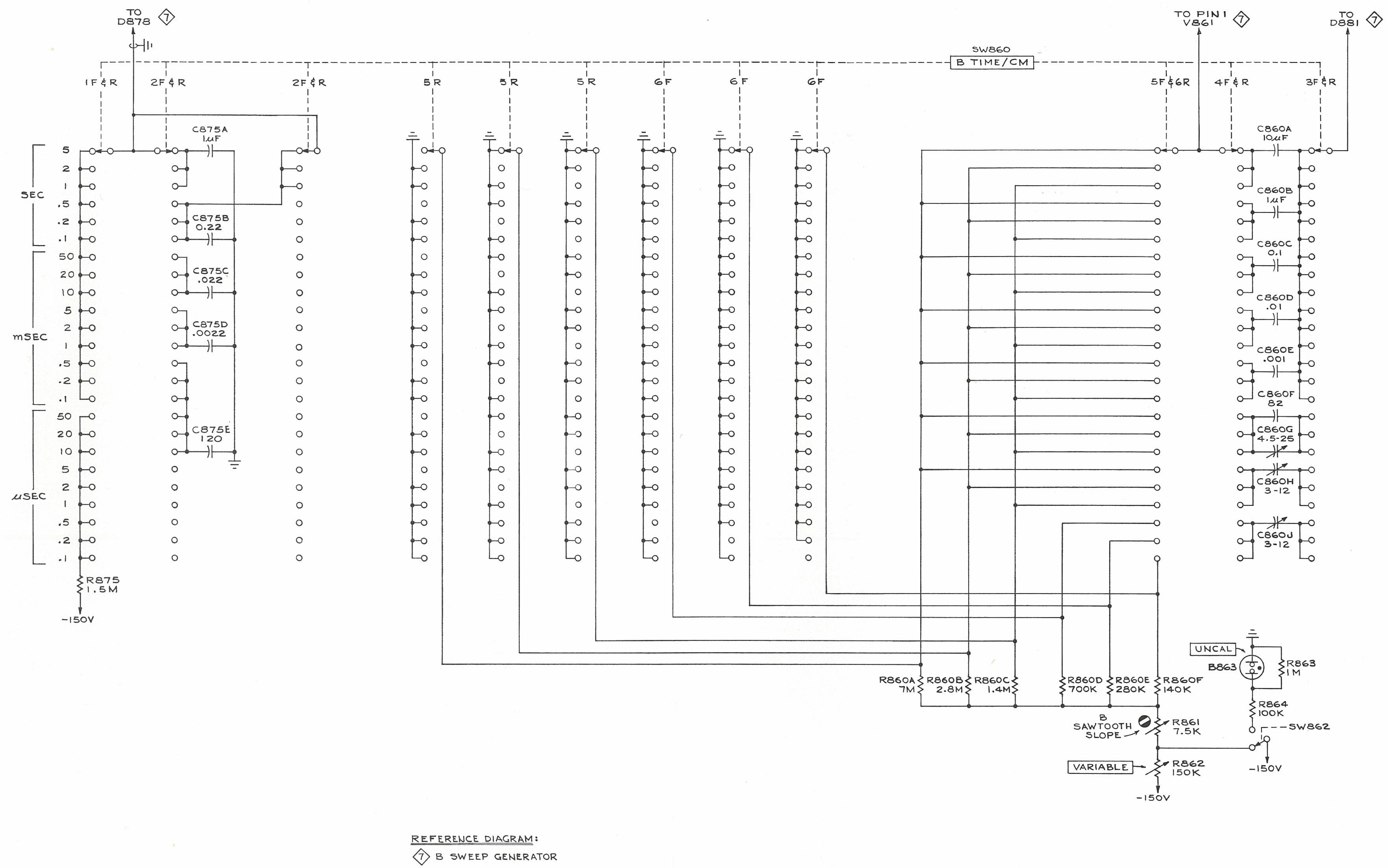
MRH 666

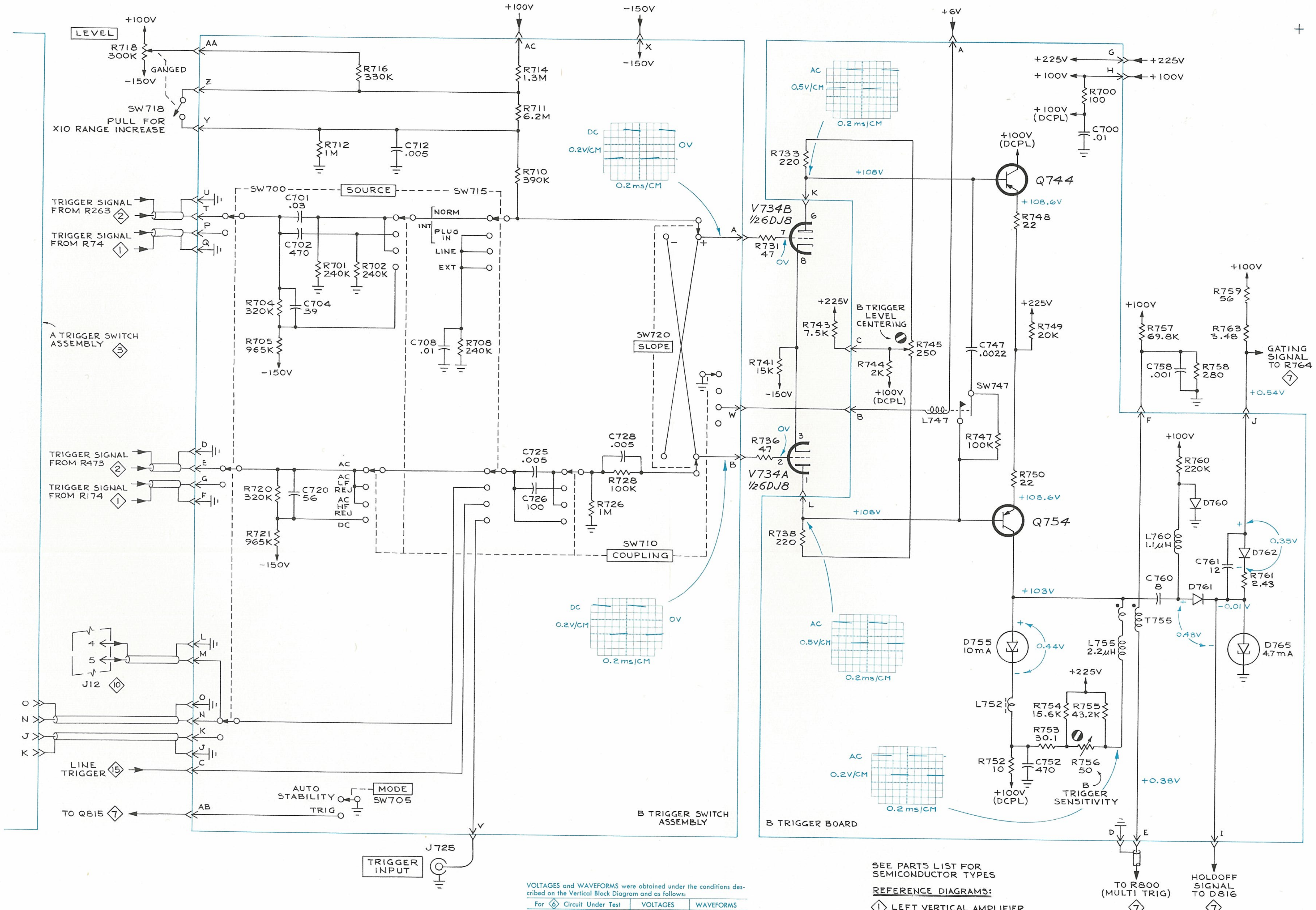


VOLTAGES and WAVEFORMS were obtained under the conditions described on the Vertical Block Diagram and as follows:

For 7 Circuit Under Test	VOLTAGES	WAVEFORMS[1]
Signal to right plug-in	None	2-V calibrator
B Triggering SOURCE	RIGHT INT NORM	RIGHT INT NORM
Upper Beam DISPLAY	RIGHT PLUG-IN B	RIGHT PLUG-IN B
B MODE	SINGLE SWEEP	NORM
B RESET button	RESET light on[2] / RESET light off[3]	As is

[1] B Triggering LEVEL control set to 0 to obtain Q805 base waveform.
[2] For upper voltage readings. Press B RESET button to turn light on.
[3] For lower voltage readings. To turn light off, set B Triggering MODE switch to AUTO STABILITY momentarily and then return switch to TRIG position.


TO D878
TO PIN 1 V861
TO D881
SW860
B TIME/CM
1F & R
2F & R
2F & R
5R
5R
5R
6F
6F
6F
5F & 6R
4F & R
3F & R
SEC
mSEC
μSEC
C875A 1μF
C875B 0.22
C875C .022
C875D .0022
C875E 120
C860A 10μF
C860B 1μF
C860C 0.1
C860D .01
C860E .001
C860F 82
C860G 4.5-25
C860H 3-12
C860J 3-12
R875 1.5M
-150V
R860A 7M
R860B 2.8M
R860C 1.4M
R860D 700K
R860E 280K
R860F 140K
B SAWTOOTH SLOPE
R861 7.5K
VARIABLE
R862 150K
UNCAL
B863
R863 1M
R864 100K
SW862
REFERENCE DIAGRAM:
7 B SWEEP GENERATOR
MRH 666



VOLTAGES and WAVEFORMS were obtained under the conditions described on the Vertical Block Diagram and as follows:

For ⑥ Circuit Under Test	VOLTAGES	WAVEFORMS
Signal to right plug-in	None	2-V calibrator
B Triggering SOURCE	RIGHT INT NORM	RIGHT INT NORM
B Triggering LEVEL	0[1]	≈20° cw from 0
B MODE	SINGLE SWEEP[2]	SINGLE SWEEP

[1] Set for 0 V at pin 7 of V734B.
[2] B RESET light is off.

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

REFERENCE DIAGRAMS:

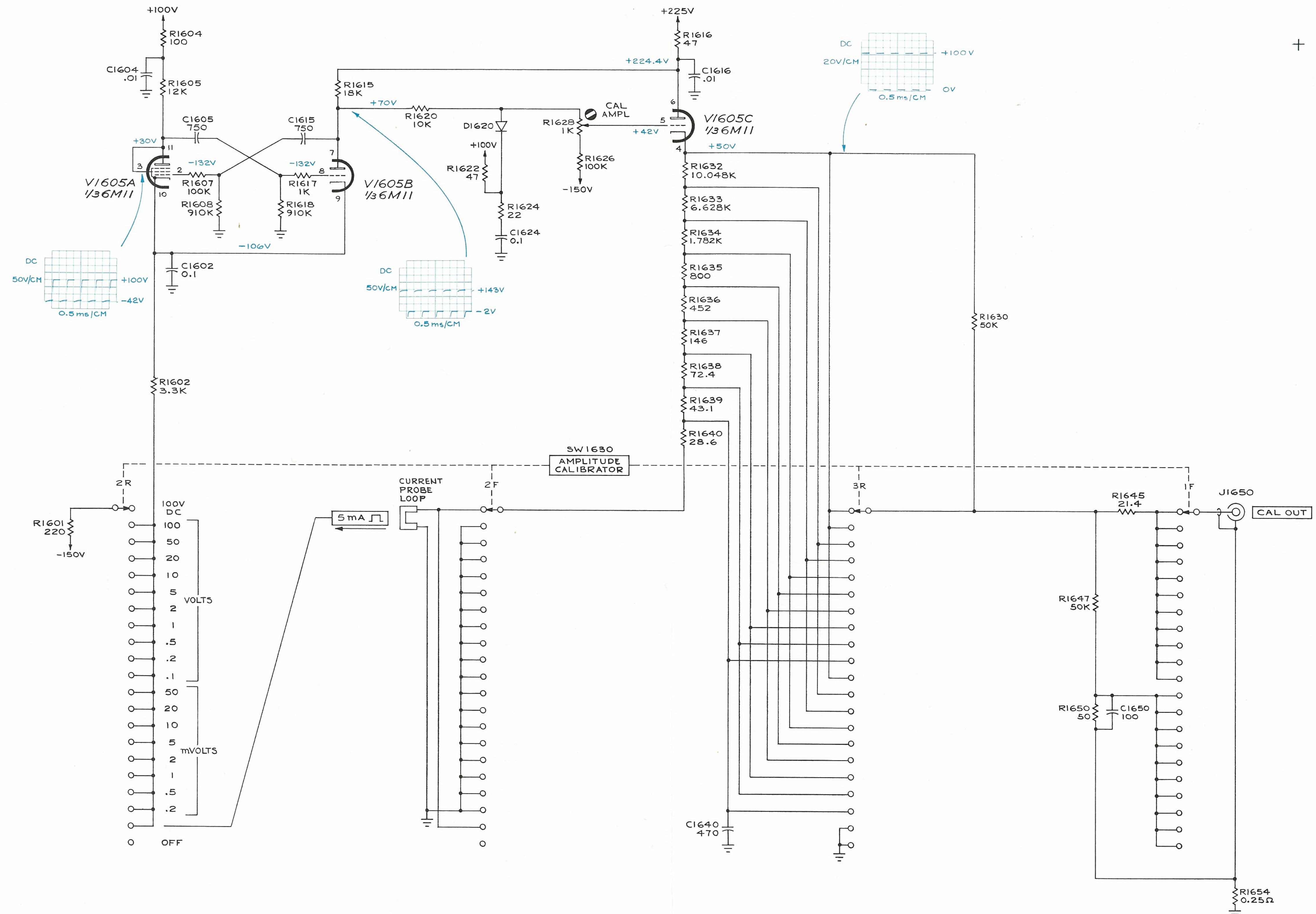
- ① LEFT VERTICAL AMPLIFIER
- ② RIGHT VERTICAL AMPLIFIER
- ③ A SWEEP TRIGGER
- ⑦ B SWEEP GENERATOR
- ⑮ HEATER WIRING
- ⑯ PLUG-IN JACK DETAILS

MRH
666

TYPE 556 OSCILLOSCOPE

A2

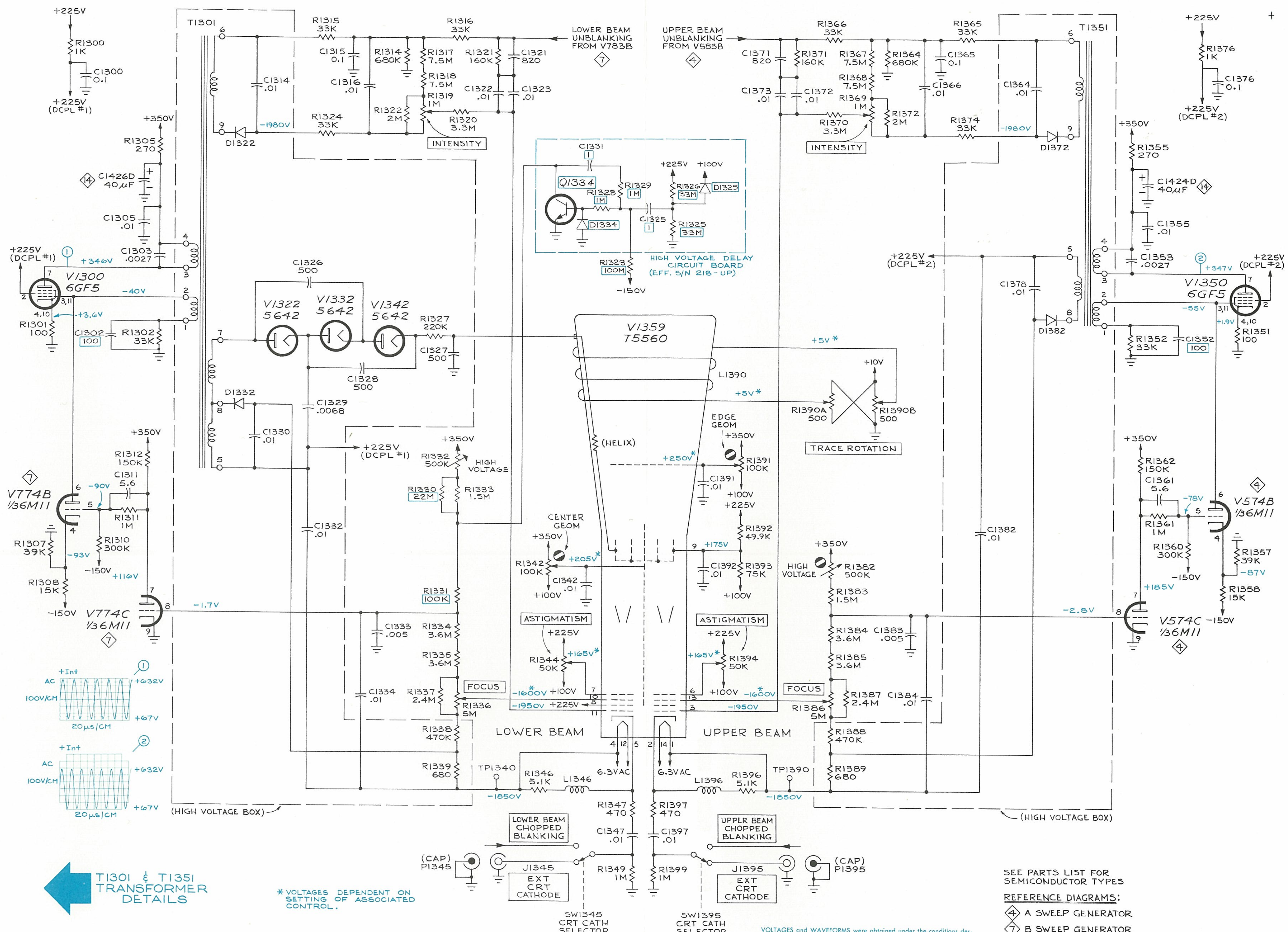
B SWEEP TRIGGER ⑥



VOLTAGES and WAVEFORMS were obtained under the conditions described on the Vertical Block Diagram. Applicable control settings are:

AMPLITUDE CALIBRATOR............2 VOLTS
POWER..............................ON

MRH
666



T1301 & T1351 TRANSFORMER DETAILS

* VOLTAGES DEPENDENT ON SETTING OF ASSOCIATED CONTROL.

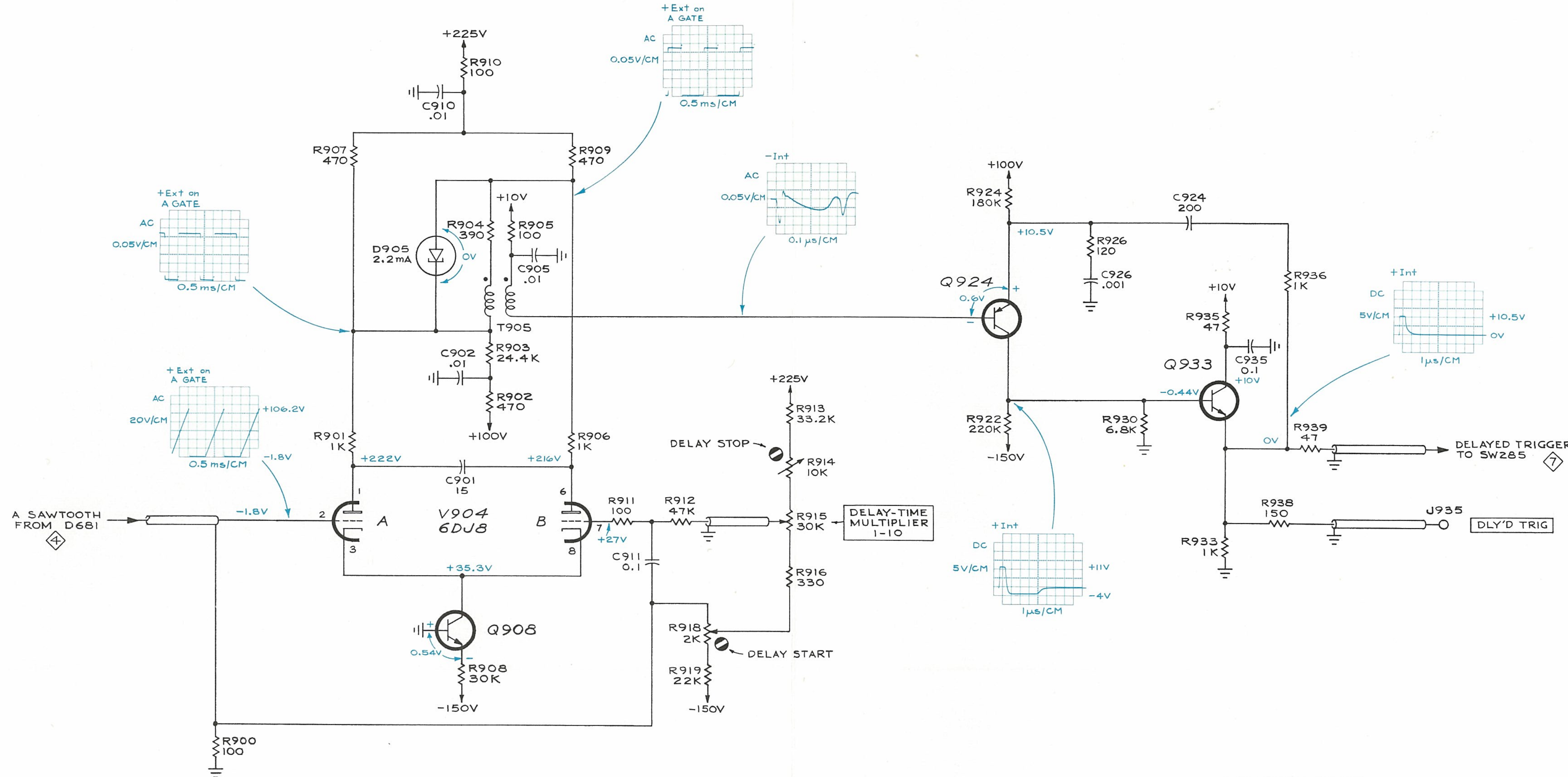
VOLTAGES and WAVEFORMS were obtained under the conditions described on the Vertical Block Diagram. Only the CRT control settings apply for this diagram (13).
Set INTENSITY control fully ccw: meter loading increases beam intensity.

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

REFERENCE DIAGRAMS:
- (4) A SWEEP GENERATOR
- (7) B SWEEP GENERATOR
- (14) POWER SUPPLY

MRH
966

CRT CIRCUIT (13)



SEE PARTS LIST FOR SEMICONDUCTOR TYPES

REFERENCE DIAGRAMS:

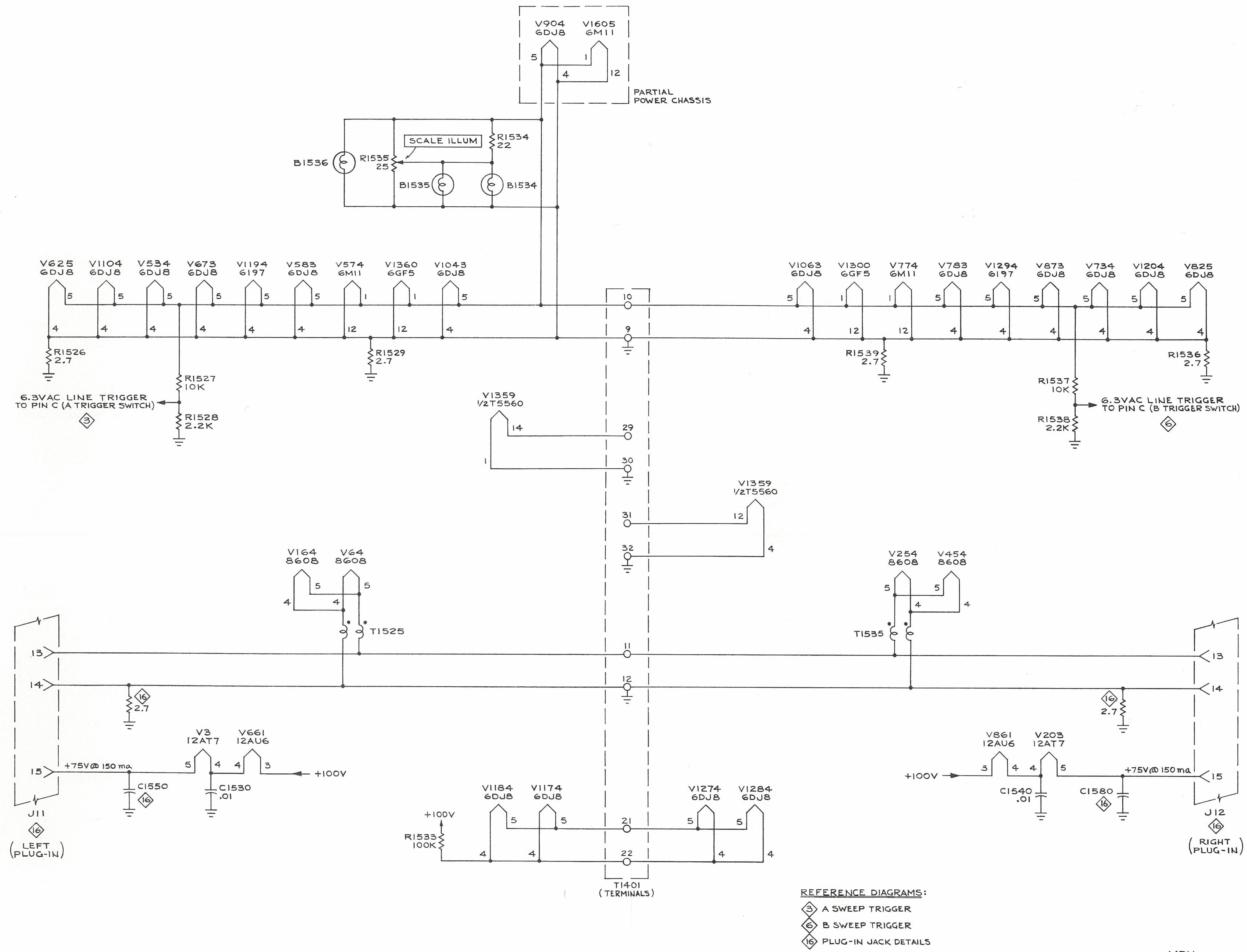
4 A SWEEP GENERATOR

7 B SWEEP GENERATOR

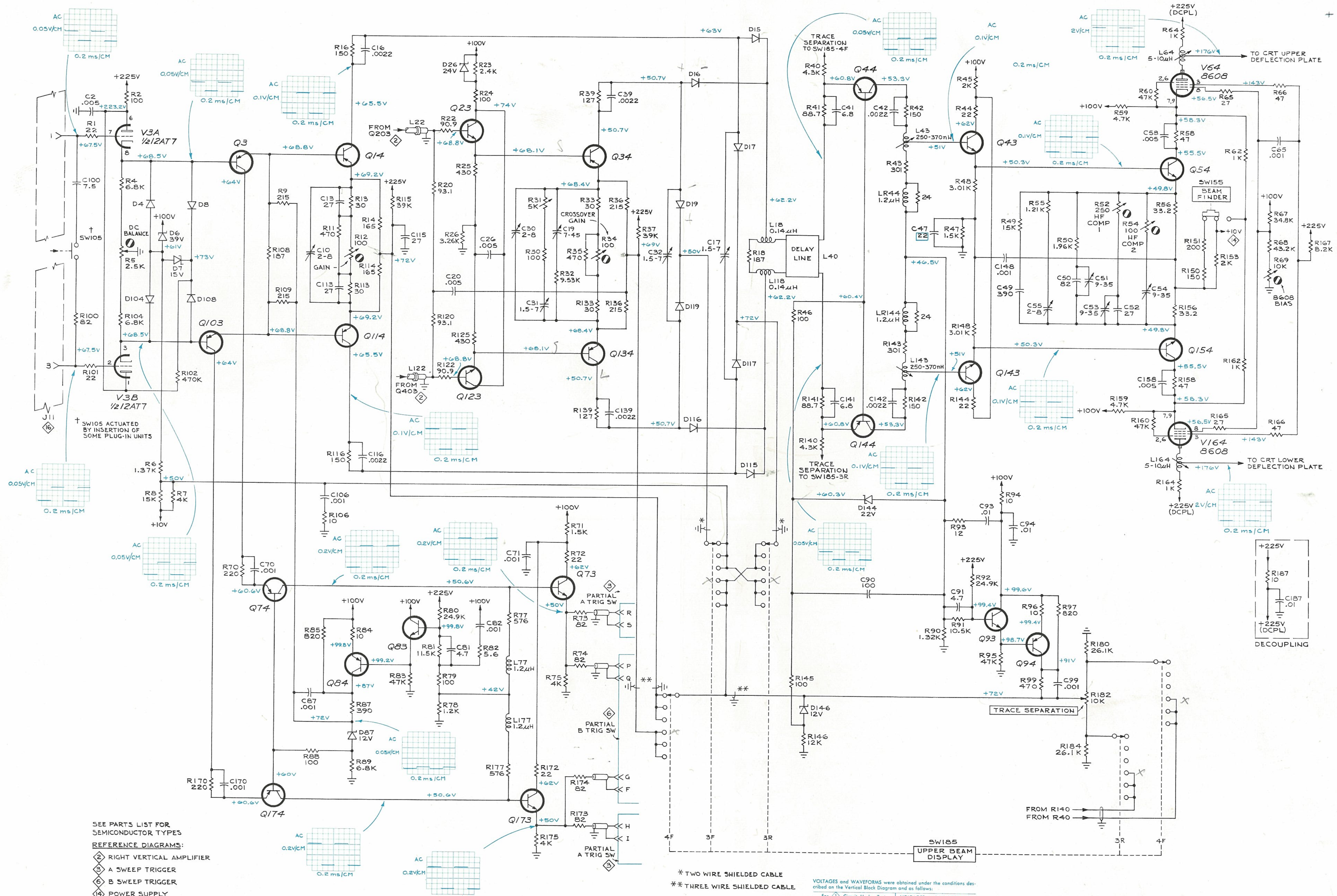
VOLTAGES and WAVEFORMS were obtained under the conditions described on the Vertical Block Diagram and as follows:

For 9 Circuit Under Test	VOLTAGES	WAVEFORMS
Signal to left plug-in	None	2-V calibrator
A Triggering SOURCE	LEFT INT NORM	LEFT INT NORM
Upper Beam DISPLAY	LEFT PLUG-IN A	LEFT PLUG-IN A
A MODE	SINGLE SWEEP	NORM
A RESET button	As is	As is

MRH
666



V904 6DJ8
V1605 6M11
PARTIAL POWER CHASSIS
SCALE ILLUM
B1536
R1535 25
B1535
B1534
R1534 22
V625 6DJ8
V1104 6DJ8
V534 6DJ8
V673 6DJ8
V1194 6197
V585 6DJ8
V574 6M11
V1360 6GF5
V1043 6DJ8
V1063 6DJ8
V1300 6GF5
V774 6M11
V783 6DJ8
V1294 6197
V873 6DJ8
V734 6DJ8
V1204 6DJ8
V825 6DJ8
R1526 2.7
R1527 10K
R1528 2.2K
R1529 2.7
6.3VAC LINE TRIGGER TO PIN C (A TRIGGER SWITCH)
R1539 2.7
R1536 2.7
R1537 10K
R1538 2.2K
6.3VAC LINE TRIGGER TO PIN C (B TRIGGER SWITCH)
V1359 1/2T5560
V164 8608
V64 8608
T1525
V254 8608
V454 8608
T1535
V3 12AT7
V661 12AU6
+75V@ 150 ma
C1550
C1530 .01
+100V
V861 12AU6
V203 12AT7
C1540 .01
C1580
J11
(LEFT PLUG-IN)
J12
(RIGHT PLUG-IN)
V1184 6DJ8
V1174 6DJ8
V1274 6DJ8
V1284 6DJ8
R1533 100K
T1401 (TERMINALS)
REFERENCE DIAGRAMS:
3 A SWEEP TRIGGER
6 B SWEEP TRIGGER
16 PLUG-IN JACK DETAILS
MRH 666



SEE PARTS LIST FOR SEMICONDUCTOR TYPES

REFERENCE DIAGRAMS:

- ⟨2⟩ RIGHT VERTICAL AMPLIFIER
- ⟨3⟩ A SWEEP TRIGGER
- ⟨6⟩ B SWEEP TRIGGER
- ⟨14⟩ POWER SUPPLY
- ⟨16⟩ PLUG-IN JACK DETAILS

* TWO WIRE SHIELDED CABLE

** THREE WIRE SHIELDED CABLE

VOLTAGES and WAVEFORMS were obtained under the conditions described on the Vertical Block Diagram and as follows:

For ⟨1⟩ Circuit Under Test	VOLTAGES and WAVEFORMS
Signal to left plug-in	2-V calibrator
Upper Beam DISPLAY	LEFT PLUG-IN A

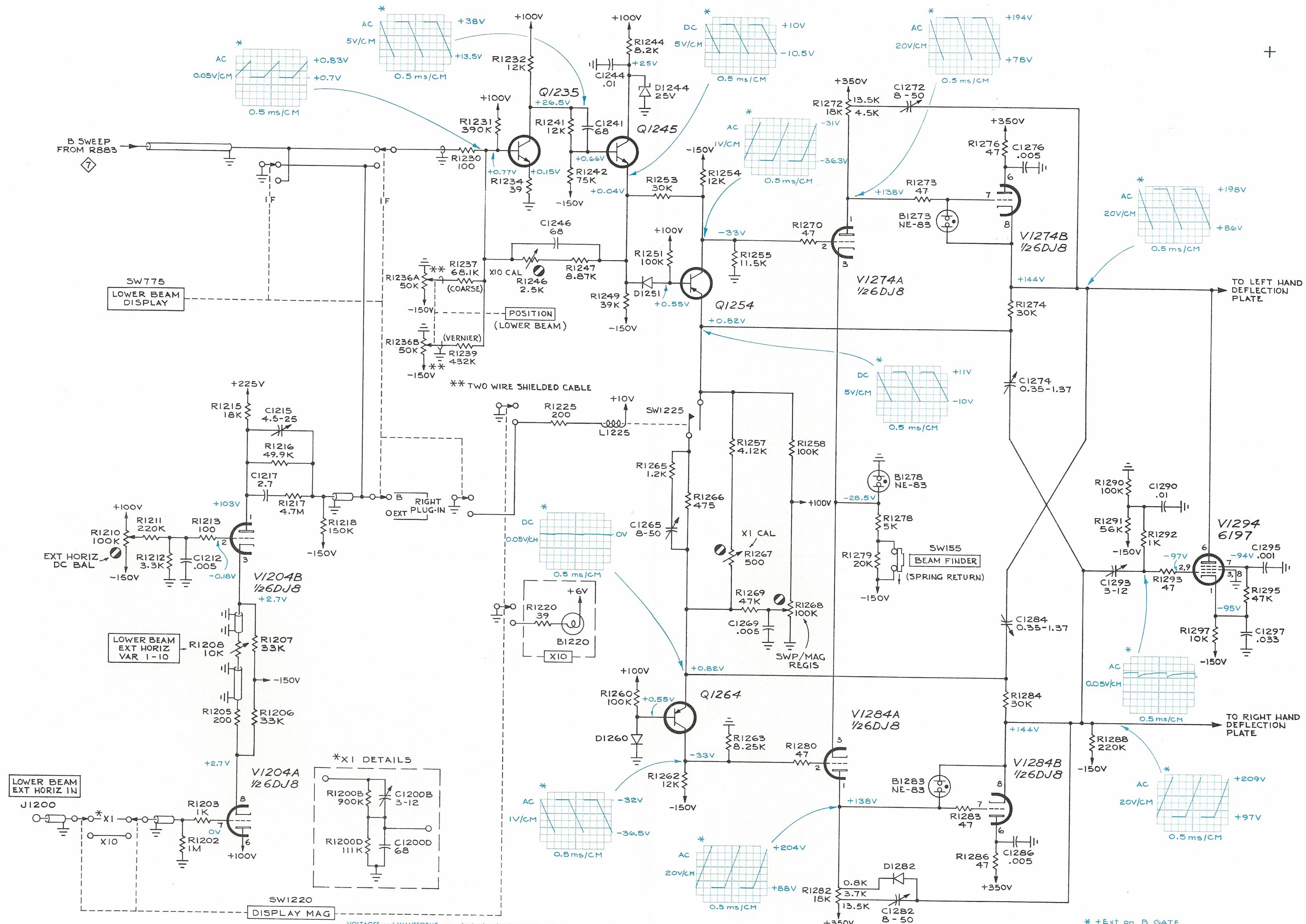
NOTE: Using some plug-ins, there may be a difference in waveform amplitudes at pins 1 and 3 of J11 as shown here. (Also, a difference signal appears at R87-D87 junction.) This is normal and amplitude differences may also exist in the succeeding amplifier stages.

TYPE 556 OSCILLOSCOPE

B

MRH
966

LEFT VERTICAL AMPLIFIER ⟨1⟩



VOLTAGES and WAVEFORMS were obtained under the conditions described on the Vertical Block Diagram and as follows:

For ⟨12⟩ Circuit Under Test	VOLTAGES	WAVEFORMS
Signal to right plug-in	None	2-V calibrator
B Triggering SOURCE	RIGHT INT NORM	RIGHT INT NORM
Lower Beam DISPLAY	RIGHT PLUG-IN EXT	RIGHT PLUG-IN B
POSITION	Set for 0 V between horizontal deflection plate pins	Set for lower beam to start at left side of graticule
B MODE	NORM	NORM
B RESET button	As is	As is

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

REFERENCE DIAGRAM:

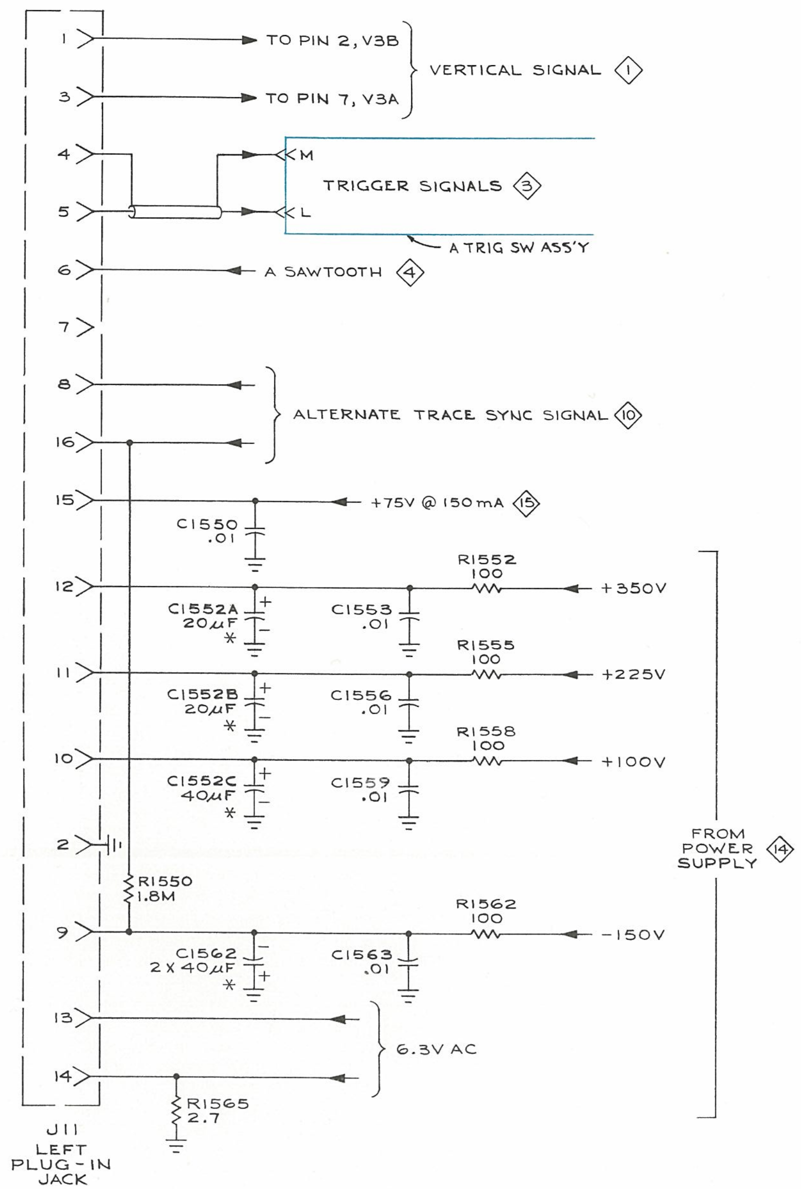
⟨7⟩ B SWEEP GENERATOR

TYPE 556 OSCILLOSCOPE

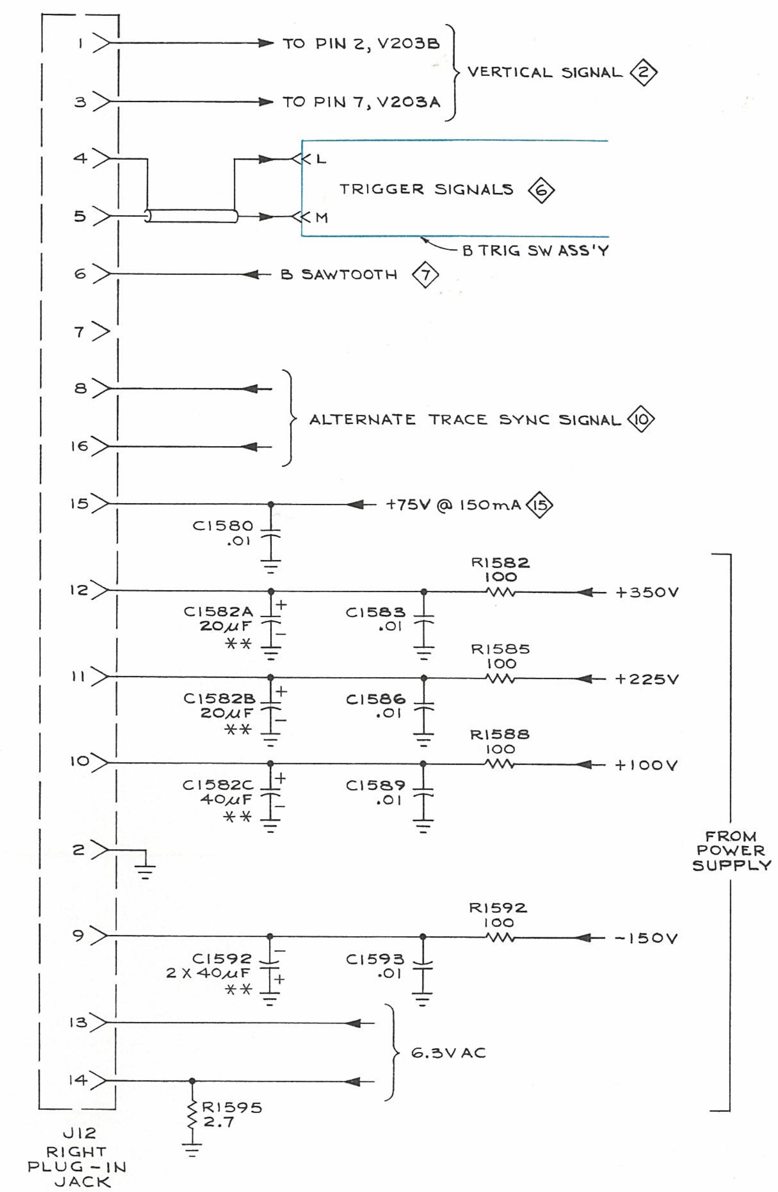
A1

MRH 666

LOWER BEAM HORIZONTAL AMPLIFIER ⟨12⟩



*LOCATED ON LEFT VERTICAL CHASSIS

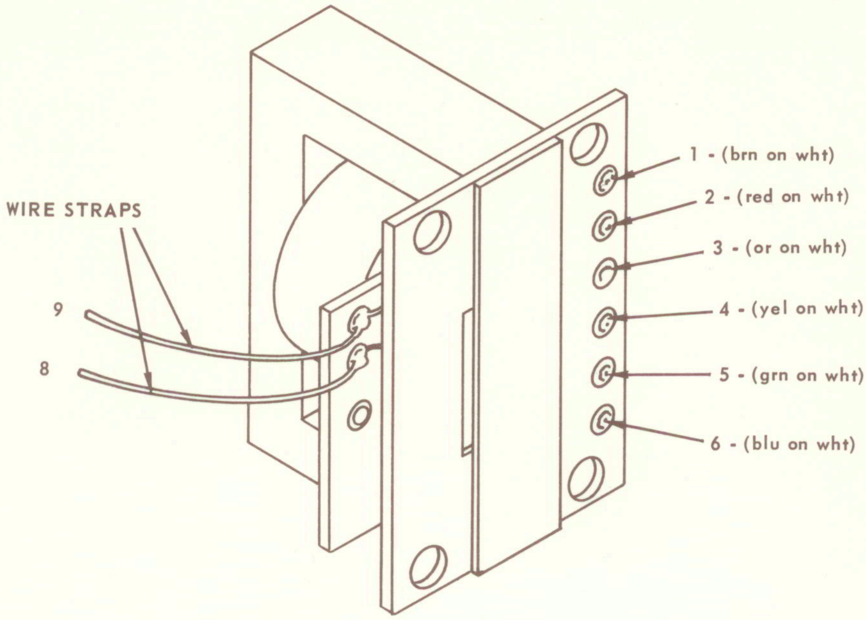


**LOCATED ON RIGHT VERTICAL CHASSIS

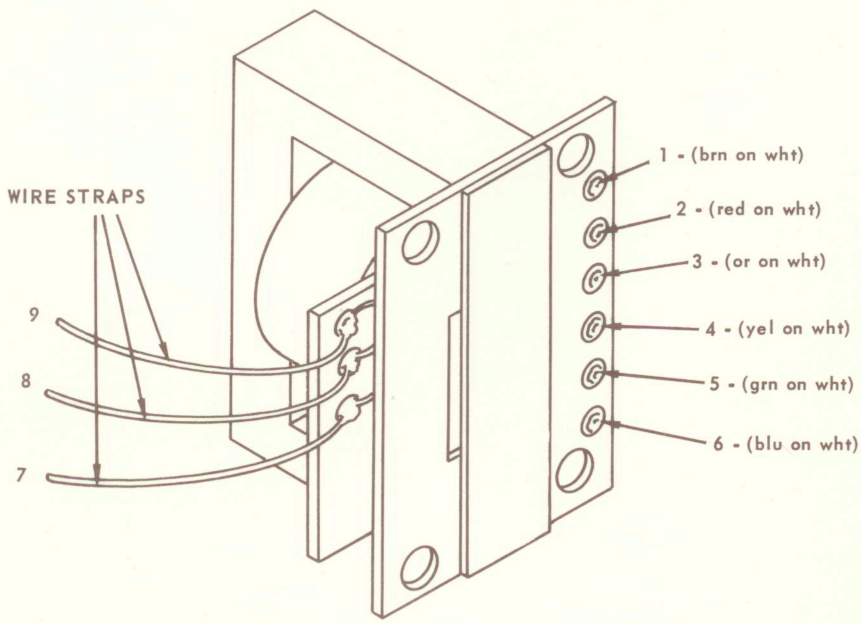
REFERENCE DIAGRAMS:

- 1 LEFT VERTICAL AMPLIFIER
- 2 RIGHT VERTICAL AMPLIFIER
- 3 A SWEEP TRIGGER
- 4 A SWEEP GENERATOR
- 6 B SWEEP TRIGGER
- 7 B SWEEP GENERATOR
- 10 ALTERNATE TRACE LOGIC & BLANKING
- 14 POWER SUPPLY
- 15 HEATER WIRING

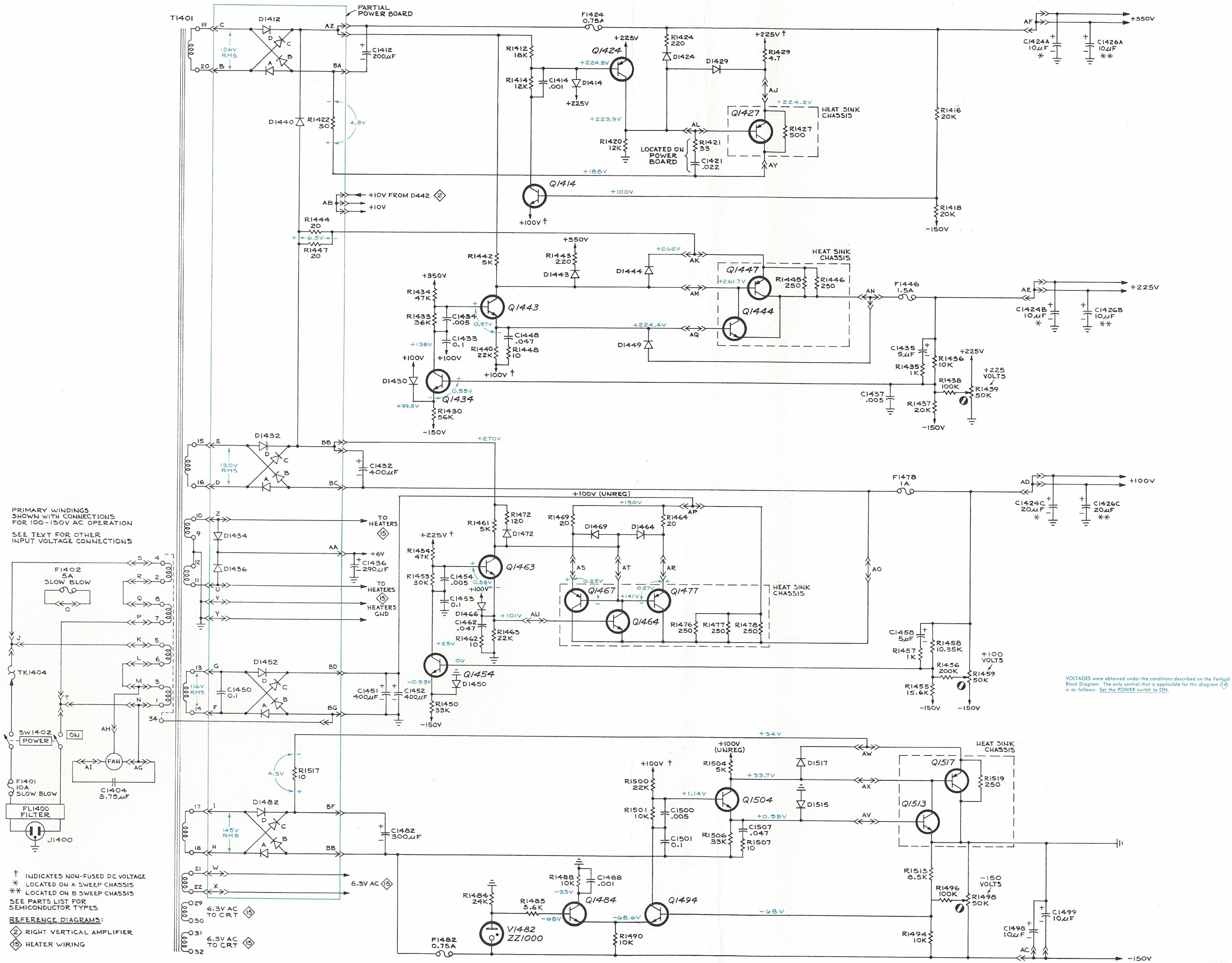
MRH
666

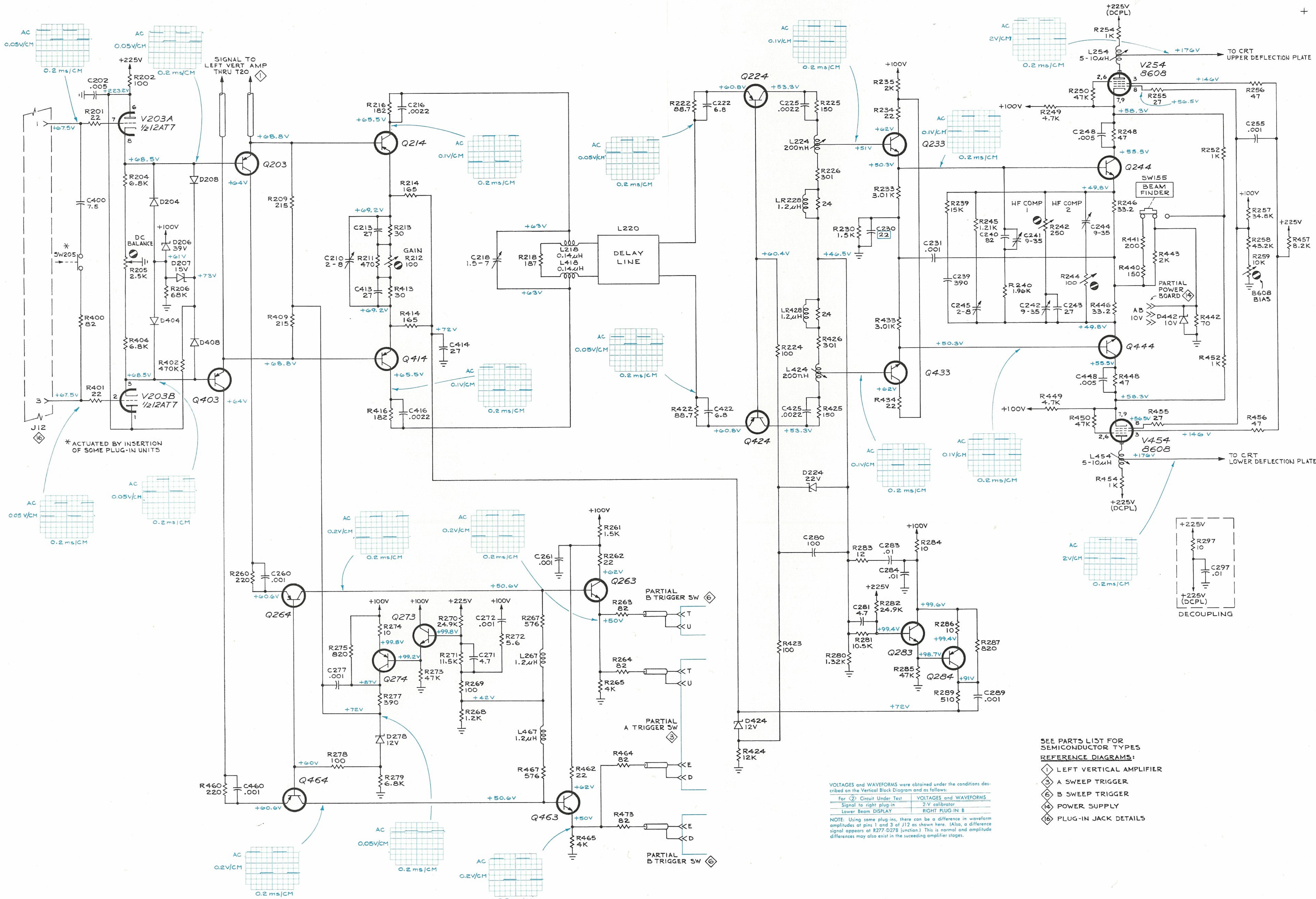


T1351
(Upper Beam)
TRANSFORMER DETAILS



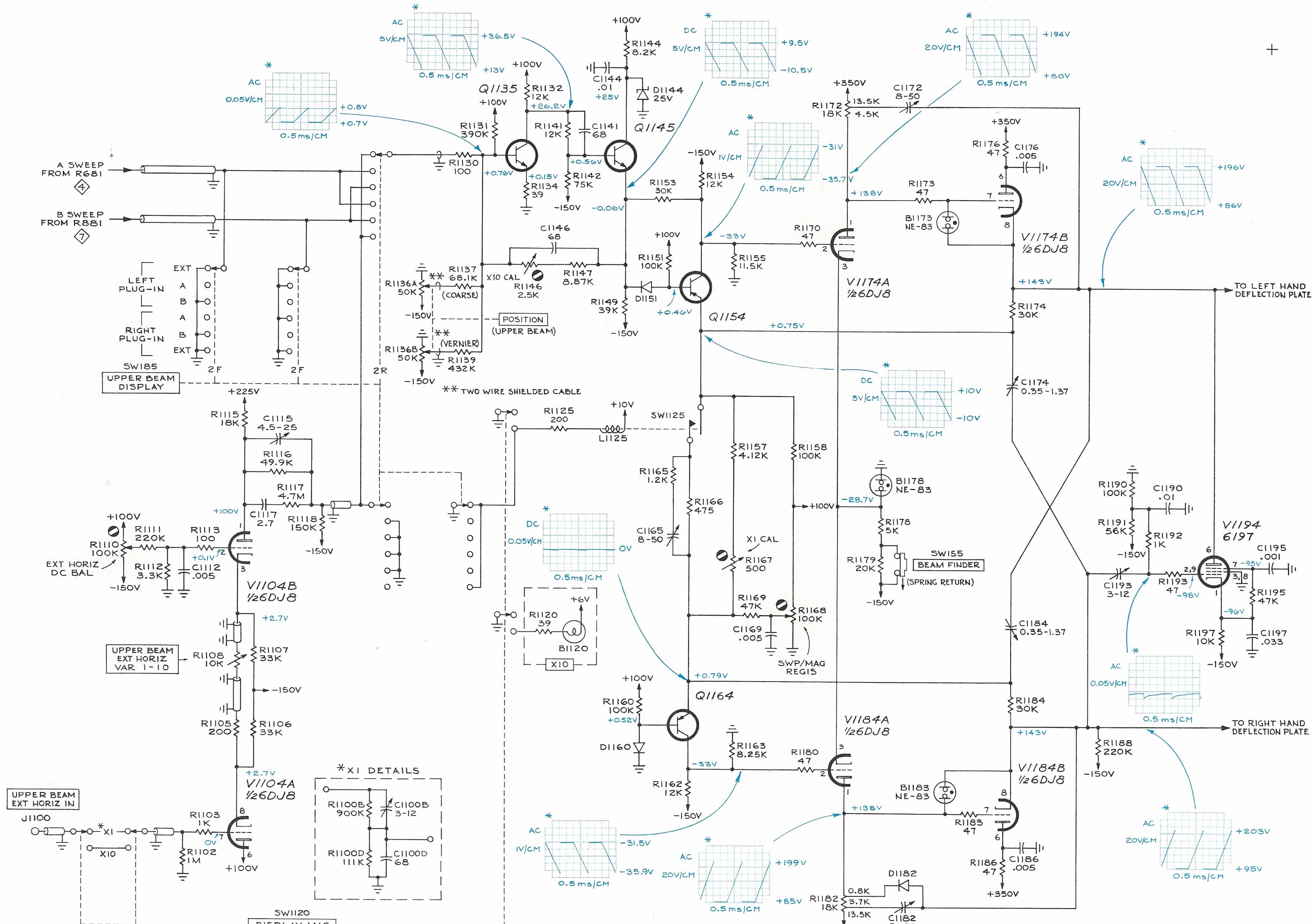
T1301
(Lower Beam)
TRANSFORMER DETAILS


T1401
PARTIAL POWER BOARD
+350V
+225V
+100V
-150V
+10V FROM D442
HEAT SINK CHASSIS
LOCATED ON POWER BOARD
+100V (UNREG)
TO HEATERS
HEATERS GND
6.3V AC
6.3V AC TO CRT
PRIMARY WINDINGS SHOWN WITH CONNECTIONS FOR 100-150V AC OPERATION
SEE TEXT FOR OTHER INPUT VOLTAGE CONNECTIONS
F1402 5A SLOW BLOW
TK1404
SW1402 POWER
ON
FAN
F1401 10A SLOW BLOW
FL1400 FILTER
J1400
† INDICATES NON-FUSED DC VOLTAGE
* LOCATED ON A SWEEP CHASSIS
** LOCATED ON B SWEEP CHASSIS
SEE PARTS LIST FOR SEMICONDUCTOR TYPES
REFERENCE DIAGRAMS:
2 RIGHT VERTICAL AMPLIFIER
15 HEATER WIRING
VOLTAGES were obtained under the conditions described on the Vertical Block Diagram. The only control that is applicable for this diagram 14 is as follows: Set the POWER switch to ON.



MRH
966

RIGHT VERTICAL AMPLIFIER ②



VOLTAGES and WAVEFORMS were obtained under the conditions described on the Vertical Block Diagram and as follows:

For (11) Circuit Under Test	VOLTAGES	WAVEFORMS
Signal to left plug-in	None	2-V calibrator
A Triggering SOURCE	LEFT INT NORM	LEFT INT NORM
Upper Beam DISPLAY	LEFT PLUG-IN EXT	LEFT PLUG-IN A
POSITION	Set for 0 V between horizontal deflection plate pins	Set for upper beam to start at left side of graticule
A MODE	NORM	NORM
A RESET button	As is	As is

SEE PARTS LIST FOR SEMICONDUCTOR TYPES

REFERENCE DIAGRAMS:

(4) A SWEEP GENERATOR

(7) B SWEEP GENERATOR

* + Ext on A GATE

MRH
666

TYPE 556 OSCILLOSCOPE

A1

UPPER BEAM HORIZONTAL AMPLIFIER (11)