Micro Power Systems

MP7623

CMOS
Multiplying 12-Bit
Digital-to-Analog Converter

FEATURES

- **Pin Compatible with MP7541**
- **12-Bit Linearity**
- **Four Quadrant Multiplication**
- **Low Feedthrough Error**
- **Low Power Consumption**
- **Latch-Up Resistant**
- **Stable, More Accurate Segmented DAC Approach**
- **Ultra Stable**
  - **0.2 ppm/°C Max Linearity Tempco**
  - **2 ppm/°C Max Gain Error Tempco**
- **Guaranteed Monotonic Over Temperature**
- **Low Output Capacitance**
  - **C_{OUT1} = 52 pF at full scale, Gives Fastest Settling Times, and Larger Stable Bandwidth Capability**
- **Low (330 µV/mV) Sensitivity to Amplifier Offset**
- **Low Glitch Energy**
- **TTL/CMOS Compatible**
- **CDIP, PDIP, SOIC & PLCC Packages Available**

BENEFITS

- **Better Performance over Temperature**
- **Increased Accuracy**
- **Lower System Cost for Given Accuracy**
- **Faster Operation**

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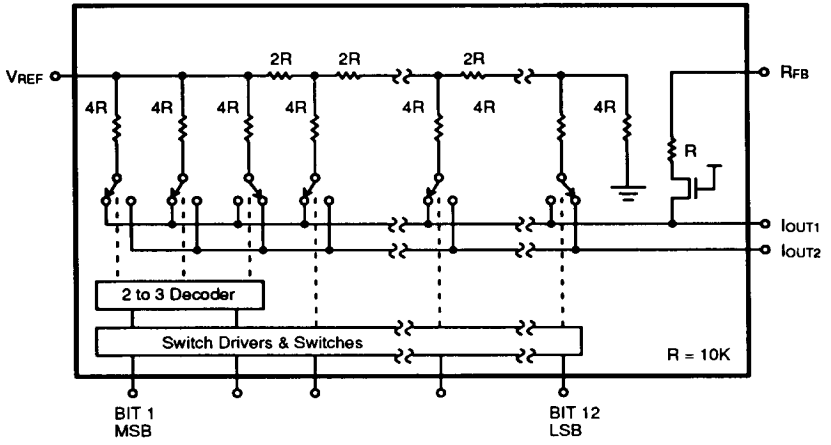
GENERAL DESCRIPTION

The MP7623 is a 12-bit DAC with a substantial increase in speed and analog performance over the industry standard 7541. The MP7623 incorporates a unique decoding technique yielding lower glitch, higher speed and excellent accuracy over temperature and time. 12-bit linearity is achieved with minimal or no trimming. The MP7623 is manufactured using MPS's advanced thin film resistors and double metal CMOS process. Outstanding features include:

- Stability: Both integral and differential linearity tempco are rated at 0.2 ppm/°C maximum, and monotonicity is guaranteed over the entire temperature range including the industrial and military ranges. Scale factor tempco is a low 2 ppm/°C maximum.
- Low Output Capacitance: Due to smaller MOSFET switch geometries allowed by decoding, the output capacitance at Iout1 is a low 52 pF/26 pF and 13pF / 45 pF at I_{OUT2} for the conditions full-scale/zero. This is four times less than the 7541. Lower capacitance allows the MP7623 to achieve faster CMOS DAC settling times; less than 1 µsec for a 10 V step to 0.01% when utilizing a high speed output amplifier. Larger output amplifier bandwidths are available (for a given amplifier loop gain) because a smaller feedback "zero" compensating capacitor is required to offset the smaller I_{OUT} capacitance.
- Low Sensitivity to Output Amplifier Offset: 4 quadrant multiplying CMOS DACs provide an output current into the virtual ground of an op amp. The additional linearity error incurred by amplifier offset is reduced by a factor of 2 in the MP7623 over conventional R-2R DACs, to 330µV per millivolt of offset.

Specified for operation over the commercial / industrial (–40 to +85°C) and military (–55 to +125°C) temperature ranges, the MP7623 is available in Plastic and Ceramic dual-in-line, Surface Mount (SOIC), and Plastic Leaded Chip Carrier (PLCC) packages.

SIMPLIFIED BLOCK DIAGRAM

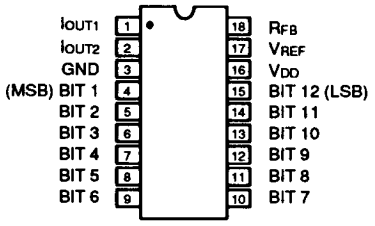


3 Segment D/A Converter with Termination to DGND
Logical "1" at Digital Input Steers Current to I_{OUT1}

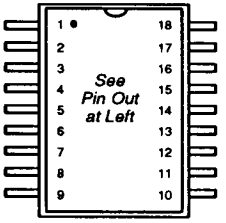
ORDERING INFORMATION

Package Type	Temperature Range	Part No.	Relative Accuracy	Differential Non-Linearity	Gain Error
Plastic Dip	–40 to +85°C	MP7623JN	±1 LSB	±1 LSB	±0.4% FSR
Plastic Dip	–40 to +85°C	MP7623KN	±1/2 LSB	±1/2 LSB	±0.4% FSR
SOIC	–40 to +85°C	MP7623JS	±1 LSB	±1 LSB	±0.4% FSR
SOIC	–40 to +85°C	MP7623KS	±1/2 LSB	±1/2 LSB	±0.4% FSR
PLCC	–40 to +85°C	MP7623JP	±1 LSB	±1 LSB	±0.4% FSR
PLCC	–40 to +85°C	MP7623KP	±1/2 LSB	±1/2 LSB	±0.4% FSR
Ceramic Dip	–40 to +85°C	MP7623AD	±1 LSB	±1 LSB	±0.4% FSR
Ceramic Dip	–40 to +85°C	MP7623BD	±1/2 LSB	±1/2 LSB	±0.4% FSR
Ceramic Dip	–55 to +125°C	MP7623SD	±1 LSB	±1 LSB	±0.4% FSR
Ceramic Dip	–55 to +125°C	MP7623SD/883	±1 LSB	±1 LSB	±0.4% FSR
Ceramic Dip	–55 to +125°C	MP7623TD	±1/2 LSB	±1/2 LSB	±0.4% FSR
Ceramic Dip	–55 to +125°C	MP7623TD/883	±1/2 LSB	±1/2 LSB	±0.4% FSR

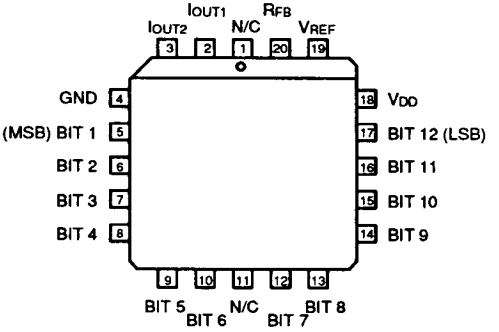
PIN CONFIGURATIONS



18 Pin CDIP, PDIP (0.300")



18 Pin SOIC (Jedec, 0.300")



20 Pin PLCC (0.350")

PIN OUT DEFINITIONS

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CDIP, PDIP, SOIC

PIN NO.	NAME	DESCRIPTION
1	I_{OUT1}	Current Output 1
2	I_{OUT2}	Current Output 2
3	GND	Ground
4	BIT 1	Data Input Bit 1 (MSB)
5	BIT 2	Data Input Bit 2
6	BIT 3	Data Input Bit 3
7	BIT 4	Data Input Bit 4
8	BIT 5	Data Input Bit 5
9	BIT 6	Data Input Bit 6

PIN NO.	NAME	DESCRIPTION
10	BIT 7	Data Input Bit 7
11	BIT 8	Data Input Bit 8
12	BIT 9	Data Input Bit 9
13	BIT 10	Data Input Bit 10
14	BIT 11	Data Input Bit 11
15	BIT 12	Data Input Bit 12 (LSB)
16	V_{DD}	Positive Power Supply
17	V_{REF}	Reference Input Voltage
18	R_{FB}	Internal Feedback Resistor

PLCC

PIN NO.	NAME	DESCRIPTION
1	N/C	No Connection
2	I_{OUT1}	Current Output 1
3	I_{OUT2}	Current Output 2
4	GND	Ground
5	BIT 1	Data Input Bit 1 (MSB)
6	BIT 2	Data Input Bit 2
7	BIT 3	Data Input Bit 3
8	BIT 4	Data Input Bit 4
9	BIT 5	Data Input Bit 5
10	BIT 6	Data Input Bit 6

PIN NO.	NAME	DESCRIPTION
11	N/C	No Connection
12	BIT 7	Data Input Bit 7
13	BIT 8	Data Input Bit 8
14	BIT 9	Data Input Bit 9
15	BIT 10	Data Input Bit 10
16	BIT 11	Data Input Bit 11
17	BIT 12	Data Input Bit 12 (LSB)
18	V_{DD}	Positive Power Supply
19	V_{REF}	Reference Input Voltage
20	R_{FB}	Internal Feedback Resistor

ELECTRICAL CHARACTERISTICS

(V_{DD} = + 15 V, V_{REF} = +10 V unless otherwise noted)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
STATIC PERFORMANCE (1)								FSR = Full Scale Range
Resolution (All Grades)	N	12			12		Bits	
Integral Non-Linearity (Relative Accuracy)	INL						LSB	Best Fit Straight Line Spec. (Max INL – Min INL) / 2
J, A, S				±1		±1		
K, B, T				±1/2		±1/2		
Differential Non-Linearity	DNL						LSB	All grades monotonic over full temperature range.
J, A, S			±1/2	±1		±1		
K, B, T			±1/4	±1/2		±1/2		
Gain Error	GE		±0.3	±0.4		±0.4	% FSR	Using Internal R_{FB}
Gain Temperature Coefficient (2)	TC_{GE}					2	ppm/°C	ΔGain/ΔTemperature
Non-Linearity Tempco (2)			0.1	0.2			ppm/°C	of FSR
Power Supply Rejection Ratio	PSRR		5	50		100	ppm/%	$\lvert\Delta Gain/\Delta V_{DD}\rvert$ ΔV_{DD} = ± 5%
DYNAMIC PERFORMANCE (2)								
Current Settling Time	ts		0.5	1			µs	Full Scale Change to 1/2 LSB
AC Feedthrough at I_{OUT1}	FT			1			mV p-p	V_{REF} = 10KHz, 20 Vp-p, sinewave
REFERENCE INPUT								
Voltage Input Range (2)				±25			V	
Input Resistance	R_{IN}	5	10	20	5	20	KΩ	
DIGITAL INPUTS (3)								
Logical "1" Voltage	V_{IH}	+2.4			+2.4		V	
Logical "0" Voltage	V_{IL}			+0.8		+0.8	V	
Input Leakage Current	I_{LKG}			±1.0		±1.0	µA	
Input Capacitance (2)								
Data	C_{IN}			8			pF	
ANALOG OUTPUTS								
Output Capacitance (2)								
	C_{OUT1}			52			pF	DAC Inputs all 1's
	C_{OUT1}			26			pF	DAC Inputs all 0's
	C_{OUT2}			13			pF	DAC Inputs all 1's
	C_{OUT2}			45			pF	DAC Inputs all 0's
Scale Factor (2)			100	200			µA/V_{REF}	
Output Leakage	I_{OUT}		<1	10		200	nA	

ELECTRICAL CHARACTERISTICS (CONT'D)

Parameter	Symbol	25°C Min	25°C Typ	25°C Max	Tmin to Tmax Min	Tmin to Tmax Max	Units	Test Conditions/Comments
POWER SUPPLY (4)								
Functional Voltage Range (2)	V_{DD}	4.5	15	16	4.5	16	V	
Supply Current	I_{DD}			2		2	mA	All digital inputs = 0 V or all = 5 V

NOTES:

(1) Full Scale Range (FSR) is 10V for unipolar mode and ±10V for bipolar.
(2) Guaranteed but not production tested.
(3) Digital input levels should not go below ground or exceed the positive supply voltage, otherwise damage may occur.
(4) Specified values guarantee functionality. Refer to other parameters for accuracy.

Specifications are subject to change without notice

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ABSOLUTE MAXIMUM RATINGS (1) (T_A = +25°C unless otherwise noted)

V_{DD} to GND ..... +17 V
Digital Input Voltage to GND (2) .. GND –0.5 to V_{DD} +0.5 V
I_{OUT1}, I_{OUT2} to GND ..... GND –0.5 to V_{DD} +0.5 V
V_{REF} to GND (2) ..... ±25 V
V_{RFB} to GND (2) ..... ±25 V

Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C
Package Power Dissipation Rating to 75°C
CDIP, PDIP, SOIC, PLCC 450mW
Derates above 75°C ..... 6mW/°C

NOTES:

(1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.
(2) Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. *All inputs have protection diodes* which will protect the device from short transients outside the supplies of less than 20mA for less than 100µs.

APPLICATION NOTES

Refer to Applications Section for Additional Information