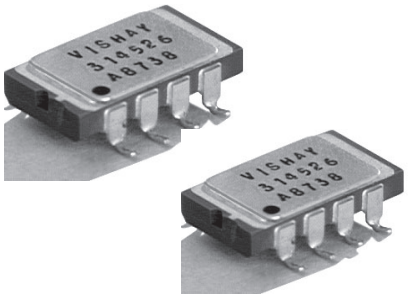
Bulk Metal® Foil Technology
Surface Mount Hermetic Resistor Networks in Gull Wing Configuration



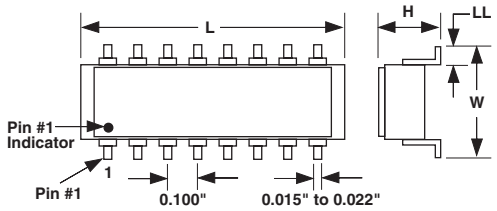
Product may not be to scale

Vishay Model VSM networks incorporate all the performance features of Vishay Bulk Metal® Foil technology in a product ready for surface mounting. The 8, 14 and 16 pin side brazed DIPs are a ceramic package. Ceramic has the advantage of electrical isolation on the underside, and, in DIP form, a favorable pin arrangement when two networks are to be placed side by side and connected together.
Review data sheet "7 technical reasons to specify Bulk Metal Foil resistor networks".

ORDERING INFORMATION - VSM40, VSM42, VSM45 OR VSM46 NETWORKS

Networks are built to your requirements. Send your schematic and electrical requirements to the Applications Engineering Department. (See data sheet "Network Worksheet".) A unique part number will be assigned which defines all aspects of your network.

FIGURE 1 - PACKAGE SIZES AND CHARACTERISTICS



NOTE:

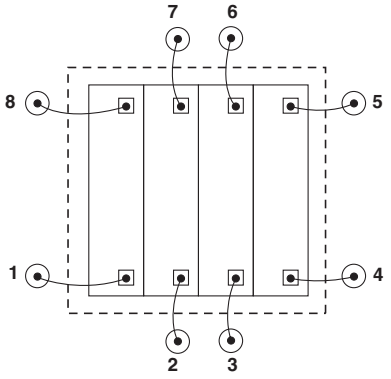
1. These networks utilize Vishay Bulk Metal® Foil resistor chips V5X5 and V15X5 or VTF15X5 Thin Film chips.
2. The V5X5 and V15X5 chips have maximum resistance values of 10K and 33K respectively in Bulk Metal® Foil and 500K in VTF15X5 Thin Film chips.
3. The V5X5 and V15X5 chip(s) can be intermixed in a package.

VISHAY MODEL	NO. OF PINS	MAXIMUM DIMENSIONS IN INCHES (MM)				CHIP CAPACITY		MAXIMUM POWER RATING (WATTS) AT + 70 °C
		L	W	H	LL	V5X5	V15X5	
VSM40	8	0.405 (10.29)	0.470 (11.938)	0.180 (4.572)	0.090 (2.286)	12	4	0.4
VSM42	8	0.540 (13.716)	0.470 (11.938)	0.180 (4.572)	0.090 (2.286)	12	4	0.4
VSM45	14	0.785 (19.914)	0.470 (11.938)	0.180 (4.572)	0.090 (2.286)	30	10	1.2
VSM46	16	0.810 (20.574)	0.470 (11.938)	0.180 (4.572)	0.090 (2.286)	36	12	1.4

FIGURE 2 - SAMPLE CIRCUIT DESIGN AND CHIP LAYOUT

NOTE:

Usable area is represented by the dotted lines - a rectangle 0.150 Inches x 0.200 Inches. Illustrations not to scale. Chips shown undersize for clarity. Drawing view is from the top looking down into the package.



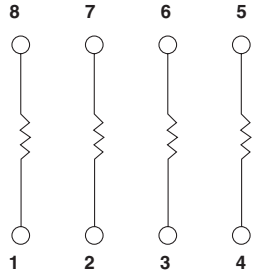
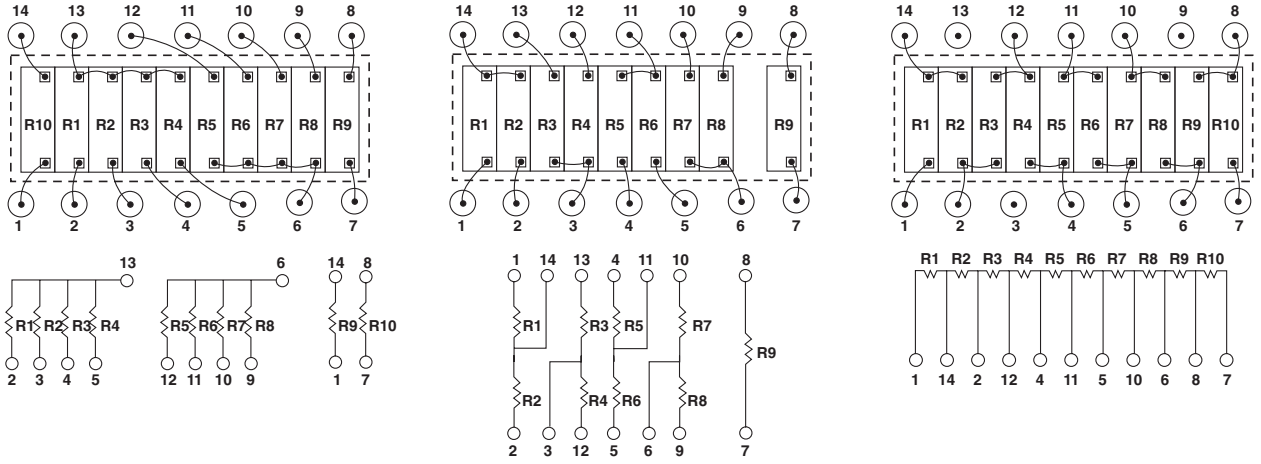


FIGURE 3 - SAMPLE CIRCUIT DESIGNS AND CHIP LAYOUTS

NOTE:

Usable area is represented by the dotted lines - a rectangle 0.150" x 0.500". Illustrations not to scale. Chips shown undersize for clarity. Drawing view is from the top looking down into the package.



TWO DECADES OF BCD LADDER PLUS TWO SCALING RESISTORS

FOUR DIVIDERS PLUS APPLICATION RESISTOR

TEN RESISTOR DIVIDER

FIGURE 4 - SAMPLE CIRCUIT DESIGNS AND CHIP LAYOUTS

NOTE:

Usable area is represented by the dotted lines - a rectangle 0.150" x 0.600". Illustrations not to scale. Chips shown undersize for clarity. Drawing view is from the top looking down into the package.

ELEVEN RESISTOR DIVIDER

EIGHT RESISTOR PACKAGE

FIVE RESISTOR CURRENT SUMMING NETWORK