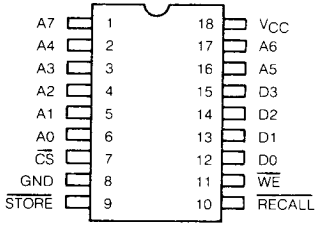
52212
1K BIT (256 x 4) NVRAM

- **1K Bit Static RAM backed by 1K Bit Electrically Erasable PROM**
- **Fully 5V Only Operation**
- **Directly TTL Compatible**
- **In Circuit E^2PROM Changes**
- **SRAM Cycle Time less than 300 ns**
- **Power-Failure Protection**
- **Unlimited Recall Cycles**
- **Memory Margining Capability**
- **Operating Ranges**

52212	0°C to +70°C
52212 I	−40°C to +85°C
52212 HR	−55°C to +125°C

The NCR 52212 non-volatile RAM combines 1K(256x4) bits of conventional static RAM (SRAM) with an identical size array of Electrically Erasable PROM (E^2PROM). Non-volatile data can be stored in the E^2 PROM while independent data is accessed simultaneously in the SRAM. Data can be transferred back and forth between the SRAM and E^2PROM by simple Store and Recall operations. A Store signal transfers data from the SRAM to the non-volatile E^2PROM where it is safely stored even when power is removed. The data stored in the non-volatile E^2PROM can be recalled an unlimited number of times. The 52212 requires only a single 5 volt power supply for all modes of operation. The device is completely TTL compatible with fully static timing and three-state outputs. The NCR 52212 is available in an 18 pin package in commercial, industrial, and high reliability versions.

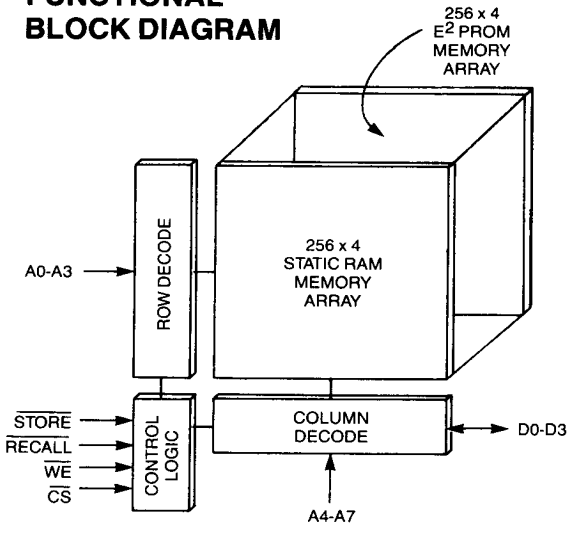
PIN CONFIGURATION



PIN NAMES

A0-A7	Address Inputs
D0-D3	Data I/O
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{STORE}$	Store Operation
$\overline{RECALL}$	Array Recall Operation
V_{CC}	5V ± 10% Supply Voltage

FUNCTIONAL BLOCK DIAGRAM



DEVICE OPERATION

SRAM READ/WRITE

The NCR 52212 can be read like a conventional static RAM. With $\overline{CS}$ low and $\overline{WE}$ high, valid data will be presented to the output pins. With $\overline{CS}$ low and $\overline{WE}$ low, the SRAM can be written to like a conventional static RAM.

STORE*

Transferring data from the SRAM to the non-volatile E^2PROM is controlled by the Store operation. When $\overline{STORE}$ is brought low, the entire contents of the SRAM array are copied into the non-volatile E^2PROM array. The data in the SRAM array is unaffected by a Store operation. The $\overline{RECALL}$ line is inhibited by a Store operation, and $\overline{CS}$ can either be high or low.

The I/O terminals are in the high impedance state during a Store operation. The contents of the E^2PROM remain valid with or without power being supplied. The data retention time of the E^2PROM can be measured by memory margining.

During power up or power down, precaution must be taken to prevent an unintentional Store cycle. Holding $\overline{STORE}$ high or $\overline{RECALL}$ low will inhibit the initiation of a Store cycle.

RECALL*

The data stored in the non-volatile E^2PROM array is transferred back into SRAM by the Recall operation. When $\overline{RECALL}$ is brought low, the entire contents of the E^2PROM are copied back into the SRAM array (overwriting any data already existing in the SRAM). The data in the E^2PROM is unaffected by a Recall operation. The I/O terminals are in a high impedance state during a Recall operation. The $\overline{STORE}$ line is inhibited by a Recall operation and $\overline{CS}$ can either be high or low. To ensure a Recall cycle is initiated on power up, a $\overline{RECALL}$ signal should be applied until VCC reaches specification limits.

MEMORY MARGINING

The NCR 52212 supports margining of the memory transistors. Memory margining allows device retention time to be projected for the purpose of device evaluation. An application note describing the memory margining algorithm is available.

MODE SELECTION

MODE	INPUTS			
	$\overline{CS}$	$\overline{WE}$	$\overline{STORE}$	$\overline{RECALL}$
READ	L	H	H	H
WRITE	L	L	H	H
STORE	X	X	L	H
RECALL	X	X	H	L

* To ensure a valid Store or Recall cycle, do not apply $\overline{STORE}$ and $\overline{RECALL}$ at the same time.

ABSOLUTE MAXIMUM RATINGS

All inputs or outputs relative to ground . . . . . – 0.5 to + 7V

Storage temperature without data retention . . . . . – 65°C to + 150°C

Stresses above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operational limits stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	52212			52212I			52212HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
V_{CC}	Supply voltage	4.5		5.5	4.5		5.5	4.5		5.5	V
V_{IH}	Input high level voltage	2.0		V_{CC}	2.0		V_{CC}	2.0		V_{CC}	V
V_{IL}	Input low level voltage	– 0.3		0.8	– 0.3		0.8	– 0.3		0.8	V
T_A	Ambient Temperature	0		70	– 40		85	– 55		125	°C

All voltages are with respect to ground

STATIC ELECTRICAL CHARACTERISTICS, OVER RECOMMENDED OPERATION CONDITIONS (UNLESS OTHERWISE NOTED)

Symbol	Parameter	Condition	52212			52212I			52212HR**			Unit
			Min	Typ*	Max	Min	Typ*	Max	Min	Typ*	Max	
I_{IN}	Input leakage current	V_{IN} = 0V to + 5.5V		0.1	10		0.1	10		0.1	10	μA
I_O	I/O leakage current	V_O = 0.4V to 5.5V Chip Deselected		0.1	10		0.1	10		0.1	10	μA
I_{CC}	Supply Current	Outputs Open		30	50		30	50		30	60	mA
V_{OH}	Output high voltage	I_{OH} = – 400μA	2.4			2.4			2.4			V
V_{OL}	Output low voltage	I_{OL} = 2.1 mA			0.4			0.4			0.4	V
T_S	Non-Volatile storage time		1.0									yr

* Typical values are at 25°C and nominal supply voltages.

CAPACITANCE T_A = 25°C, f = 1.0MHz, V_{CC} = 5V

Symbol	Parameter	Condition	52212			52212I			52212HR**			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
C	Capacitance of Input & Data I/O pins	All pins at VSS (ground)			10			10			10	pF

** The 52212 HR data is preliminary and is subject to change.

NCR

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS (UNLESS OTHERWISE NOTED)

READ CYCLE

Symbol	Parameter	52212			52212I			52212HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{RC}	Read Cycle Time	300			300			450			ns
t_{ACC}	Address Access Time			300			300			450	ns
t_{A}	Chip Select To Data Active	0			0			0			ns
t_{CS}	Chip Select Access Time			100			120			120	ns
t_{OH}	Output Hold Time	10			10			10			ns
t_{OZ}	Chip Select Output High Impedance Time			90			90			90	ns

WRITE CYCLE

Symbol	Parameter	52212			52212I			52212HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{WC}	Write Cycle Time	300			300			450			ns
t_{CW}	Chip Select to End of Write	150			150			300			ns
t_{WP}	Write Pulse Width	150			150			300			ns
t_{WR}	Write Release Time	25			25			25			ns
t_{DTW}	Output High Impedence From Write Enable			100			100			100	ns
t_{DW}	Data to Write Time Overlap	150			150			200			ns
t_{OW}	Output Active from End of Write	10			10			10			ns
t_{DH}	Data Hold From Write Time	20			20			20			ns
t_{AS}	Address Setup	50			50			50			ns

STORE CYCLE

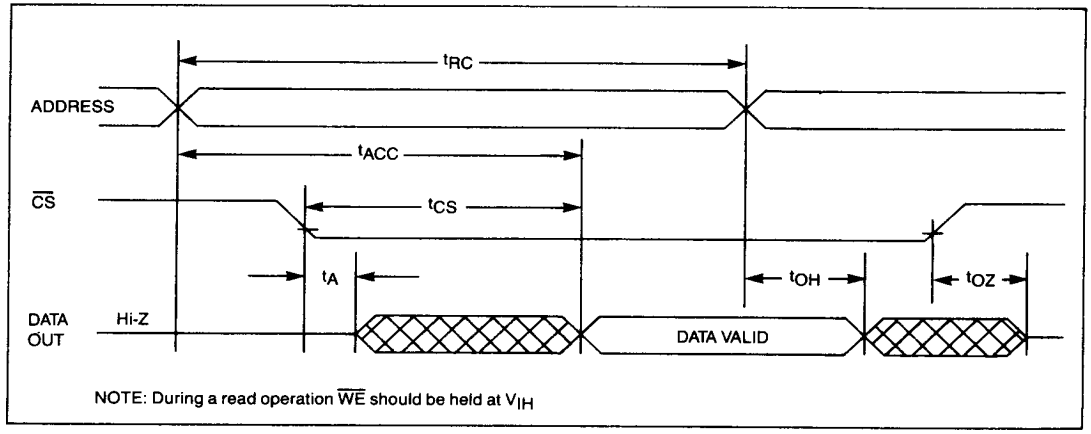
Symbol	Parameter	52212			52212I			52212HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{STC}	Store Cycle Time			10			10			10	ms
t_{STP}	Store Pulse Width	100			100			100			ns
t_{STZ}	Store to Output Hi-Z			100			100			100	ns
N_{SC}	Number of Store Cycles	10^4			10^4			10^4			

RECALL CYCLE

Symbol	Parameter	52212			52212I			52212HR**			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
t_{RCC}	Array Recall Cycle Time		30	70			260			360	μs
t_{RCP}	Recall Pulse Width	200			200			450			ns
t_{RCZ}	Recall to Output Hi-Z			100			100			100	ns

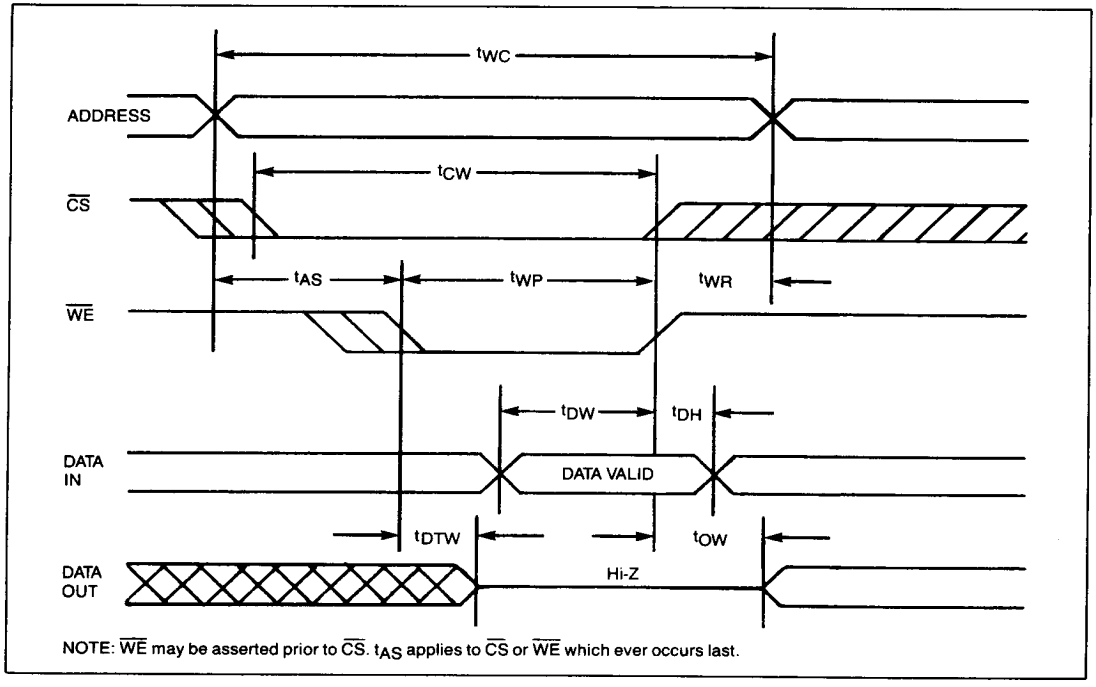
**The 52212 HR data is preliminary and is subject to change.

READ CYCLE



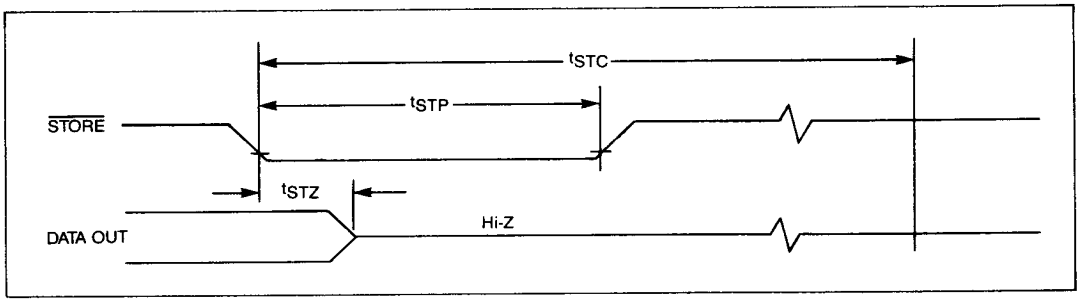
NOTE: During a read operation $\overline{WE}$ should be held at V_{IH}

WRITE CYCLE

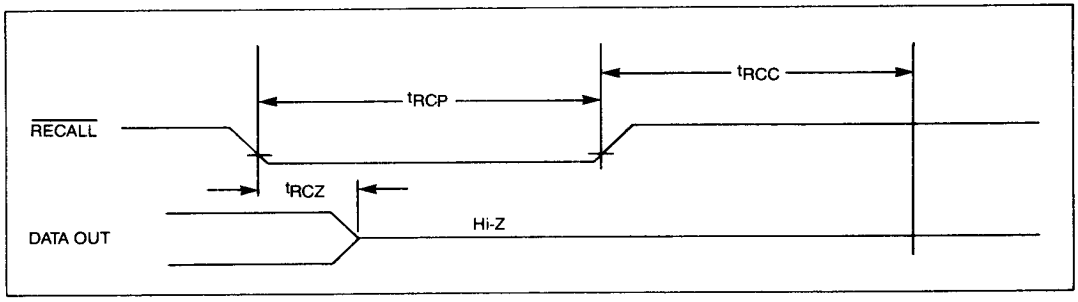


NOTE: $\overline{WE}$ may be asserted prior to $\overline{CS}$. t_{AS} applies to $\overline{CS}$ or $\overline{WE}$ which ever occurs last.

STORE CYCLE



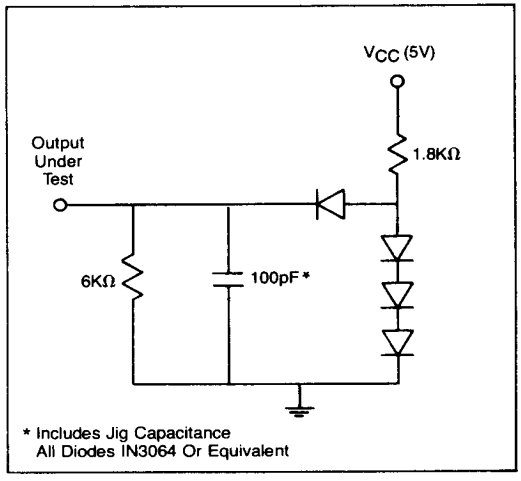
RECALL CYCLE



A. C. CONDITION OF TESTS

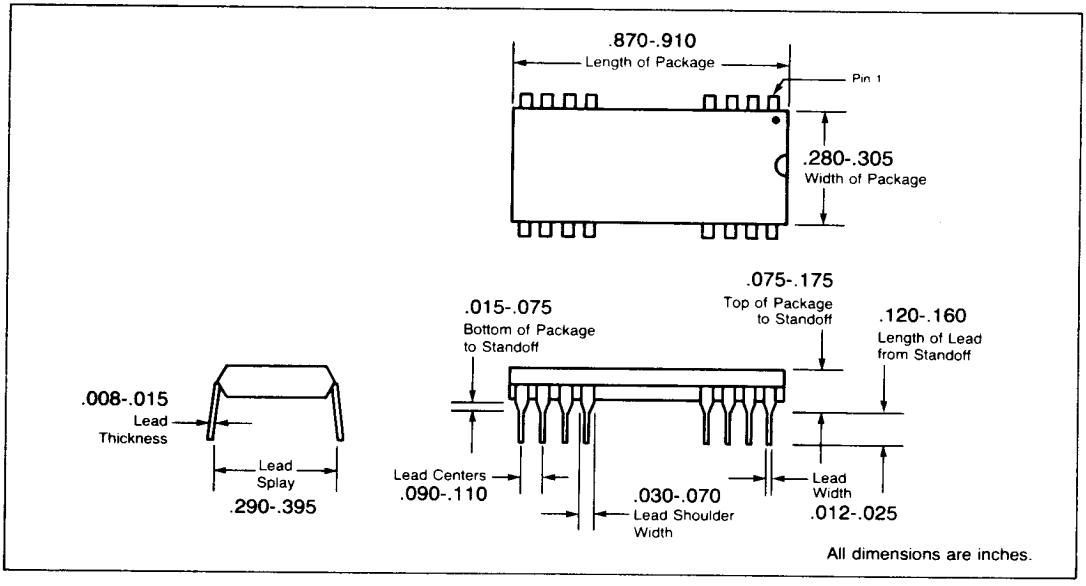
Input Pulse Levels . . . . . 0.8 Volts to 2.0 Volts
Inputs Rise & Fall Times. . . . . 10 ns
Output Timing Levels . . . . . 0.8 Volts to 2.0 Volts

TEST LOAD CIRCUIT



MECHANICAL DATA 18 PIN

CERAMIC DEVICES



PLASTIC DEVICES