



# CAT22C12

## 1K-Bit Nonvolatile CMOS Static RAM

### FEATURES

- Low Power CMOS Technology
- Single 5V Supply
- Fast RAM Access Times:
  - 200ns
  - 300ns
- Infinite E<sup>2</sup>PROM to RAM Recall
- CMOS and TTL Compatible I/O
- Power Up/Down Protection
- Low CMOS Power Consumption:
  - Active: 50mA Max.
  - Standby: 30μA Max.
- JEDEC Standard Pinouts:
  - 18 pin DIP
- 100,000 Program/Erase Cycles (E<sup>2</sup>PROM)
- 10 Year Data Retention
- Commercial, Industrial and Automotive Temperature Ranges

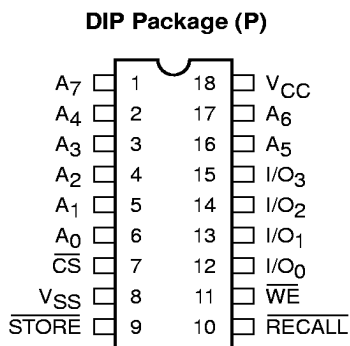
### DESCRIPTION

The CAT22C12 NVRAM is a 1K bit nonvolatile memory organized as 256 words x 4 bits. The high speed static RAM array is bit for bit backed up by a nonvolatile E<sup>2</sup>PROM array which allows for easy transfer of data from RAM array to E<sup>2</sup>PROM (STORE) and from E<sup>2</sup>PROM to RAM (RECALL). STORE operations are completed in 10ms max. and RECALL operations typically within 1.5μs. The CAT22C12 features unlimited RAM write operations either through external RAM writes or inter-

nal recalls from E<sup>2</sup>PROM. Internal false store protection circuitry prohibits STORE operations when V<sub>CC</sub> is less than 3.5V typ.

The CAT22C12 is manufactured using Catalyst's advanced CMOS floating gate technology. It is designed to endure 100,000 program/erase cycles (E<sup>2</sup>PROM) and has a data retention of 10 years. The device is available in a JEDEC approved 18 pin plastic DIP package.

### PIN CONFIGURATION

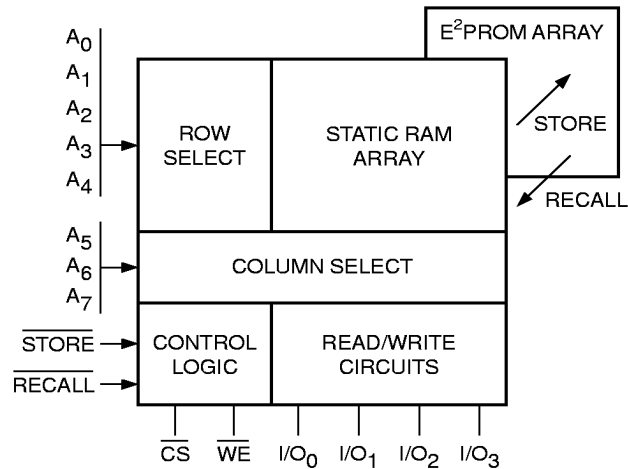


### PIN FUNCTIONS

Pin Name	Function
A <sub>0</sub> -A <sub>7</sub>	Address
I/O <sub>0</sub> -I/O <sub>3</sub>	Data In/Out
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
RECALL	Recall
STORE	Store
V <sub>CC</sub>	+5V
V <sub>SS</sub>	Ground

5155 FHD F01

**BLOCK DIAGRAM**



5155 FHD F02

**MODE SELECTION<sup>(1)(2)(3)</sup>**

Mode	Input				I/O
	$\overline{CS}$	$\overline{WE}$	RECALL	STORE	
Standby	H	X	H	H	Output High-Z
RAM Read	L	H	H	H	Output Data
RAM Write	L	L	H	H	Input Data
(E <sup>2</sup> PROM→RAM)	X	H	L	H	Output High-Z RECALL
(E <sup>2</sup> PROM→RAM)	H	X	L	H	Output High-Z RECALL
(RAM→E <sup>2</sup> PROM)	X	H	H	L	Output High-Z STORE
(RAM→E <sup>2</sup> PROM)	H	X	H	L	Output High-Z STORE

**POWER-UP TIMING<sup>(4)</sup>**

Symbol	Parameter	Min.	Max.	Units
VCCSR	V <sub>CC</sub> Slew Rate	.5	.005	V/ms

Note:

- (1)  $\overline{RECALL}$  signal has priority over  $\overline{STORE}$  signal when both are applied at the same time.
- (2)  $\overline{STORE}$  is inhibited when  $\overline{RECALL}$  is active.
- (3) The store operation is inhibited when V<sub>CC</sub> is below ≈ 3.5V.
- (4) This parameter is tested initially and after a design or process change that affects the parameter.

**ABSOLUTE MAXIMUM RATINGS\***

Temperature Under Bias .....	-55°C to +125°C
Storage Temperature .....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground <sup>(2)</sup> .....	-2.0 to +V <sub>CC</sub> +2.0V
V <sub>CC</sub> with Respect to Ground .....	-2.0V to +7.0V
Package Power Dissipation Capability (T <sub>a</sub> = 25°C) .....	1.0W
Lead Soldering Temperature (10 secs) .....	300°C
Output Short Circuit Current <sup>(3)</sup> .....	100 mA

**\*COMMENT**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside of those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

**RELIABILITY CHARACTERISTICS**

Symbol	Parameter	Min.	Max.	Units	Reference Test Method
N <sub>END</sub> <sup>(1)</sup>	Endurance	10,000		Cycles/Byte	MIL-STD-883, Test Method 1033
T <sub>DR</sub> <sup>(1)</sup>	Data Retention	10		Years	MIL-STD-883, Test Method 1008
V <sub>ZAP</sub> <sup>(1)</sup>	ESD Susceptibility	2000		Volts	MIL-STD-883, Test Method 3015
I <sub>LTH</sub> <sup>(1)(4)</sup>	Latch-Up	100		mA	JEDEC Standard 17

**D.C. OPERATING CHARACTERISTICS**

V<sub>CC</sub> = +5V ±10%, unless otherwise specified.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.	Max.		
I <sub>CC</sub>	Current Consumption (Operating)			50	mA	All Inputs = 5.5V T <sub>A</sub> = 0°C All I/O's Open
I <sub>SB</sub>	Current Consumption (Standby)			30	μA	$\overline{CS} = V_{CC}$ All I/O's Open
I <sub>LI</sub>	Input Current			2	μA	0 ≤ V <sub>IN</sub> ≤ 5.5V
I <sub>LO</sub>	Output Leakage Current			10	μA	0 ≤ V <sub>OUT</sub> ≤ 5.5V
V <sub>IH</sub>	High Level Input Voltage	2.0		V <sub>CC</sub>	V	
V <sub>IL</sub>	Low Level Input Voltage	0.0		0.8	V	
V <sub>OH</sub>	High Level Output Voltage	2.4			V	I <sub>OH</sub> = -2mA
V <sub>OL</sub>	Low Level Output Voltage			0.4	V	I <sub>OL</sub> = 4.2mA
V <sub>DH</sub>	RAM Data Holding Voltage	1.5		5.5	V	V <sub>CC</sub>

**CAPACITANCE** T<sub>A</sub> = 25°C, f = 1.0 MHz, V<sub>CC</sub> = 5V

Symbol	Parameter	Max.	Unit	Conditions
C <sub>I/O</sub> <sup>(1)</sup>	Input/Output Capacitance	10	pF	V <sub>I/O</sub> = 0V
C <sub>IN</sub> <sup>(1)</sup>	Input Capacitance	6	pF	V <sub>IN</sub> = 0V

Note:

- (1) This parameter is tested initially and after a design or process change that affects the parameter.
- (2) The minimum DC input voltage is -0.5V. During transitions, inputs may undershoot to -2.0V for periods of less than 20 ns. Maximum DC voltage on output pins is V<sub>CC</sub> +0.5V, which may overshoot to V<sub>CC</sub> +2.0V for periods of less than 20 ns.
- (3) Output shorted for no more than one second. No more than one output shorted at a time.
- (4) Latch-up protection is provided for stresses up to 100 mA on address and data pins from -1V to V<sub>CC</sub> +1V.

**A.C. CHARACTERISTICS, Write Cycle**

V<sub>CC</sub> = +5V ±10%, unless otherwise specified.

Symbol	Parameter	22C12-20		22C12-30		Unit	Conditions
		Min.	Max.	Min.	Max.		
t <sub>WC</sub>	Write Cycle Time	200		300		ns	C <sub>L</sub> = 100pF +1TTL gate V <sub>OH</sub> = 2.2V V <sub>OL</sub> = 0.65V V <sub>IH</sub> = 2.2V V <sub>IL</sub> = 0.65V
t <sub>CW</sub>	$\overline{CS}$ Write Pulse Width	150		150		ns	
t <sub>AS</sub>	Address Setup Time	50		50		ns	
t <sub>WP</sub>	Write Pulse Width	150		150		ns	
t <sub>WR</sub>	Write Recovery Time	25		25		ns	
t <sub>DW</sub>	Data Valid Time	100		100		ns	
t <sub>DH</sub>	Data Hold Time	0		0		ns	
t <sub>WZ</sub> <sup>(1)</sup>	Output Disable Time		100		100	ns	
t <sub>OW</sub>	Output Enable Time	0		0		ns	

**A.C. CHARACTERISTICS, Read Cycle**

V<sub>CC</sub> = +5V ±10%, unless otherwise specified.

Symbol	Parameter	22C12-20		22C12-30		Unit	Conditions
		Min.	Max.	Min.	Max.		
t <sub>RC</sub>	Read Cycle Time	200		300		ns	C <sub>L</sub> = 100pF +1TTL gate V <sub>OH</sub> = 2.2V V <sub>OL</sub> = 0.65V V <sub>IH</sub> = 2.2V V <sub>IL</sub> = 0.65V
t <sub>AA</sub>	Address Access Time		200		300	ns	
t <sub>CO</sub>	$\overline{CS}$ Access Time		200		300	ns	
t <sub>OH</sub>	Output Data Hold Time	0		0		ns	
t <sub>LZ</sub> <sup>(1)</sup>	$\overline{CS}$ Enable Time	0		0		ns	
t <sub>HZ</sub> <sup>(1)</sup>	$\overline{CS}$ Disable Time		100		100	ns	

Note:

(1) This parameter is tested initially and after a design or process change that affects the parameter.

**A.C. CHARACTERISTICS, Store Cycle**

$V_{CC} = +5V \pm 10\%$ , unless otherwise specified.

Symbol	Parameter	Limits		Units	Conditions
		Min.	Max.		
t <sub>STC</sub>	Store Time		10	ms	C <sub>L</sub> = 100pF + 1TTL gate V <sub>OH</sub> = 2.2V, V <sub>OL</sub> = 0.65V V <sub>IH</sub> = 2.2V, V <sub>IL</sub> = 0.65V
t <sub>STP</sub>	Store Pulse Width	200		ns	
t <sub>STZ</sub> <sup>(1)</sup>	Store Disable Time		100	ns	
t <sub>OST</sub> <sup>(1)</sup>	Store Enable Time	0		ns	

**A.C. CHARACTERISTICS, Recall Cycle**

$V_{CC} = +5V \pm 10\%$ , unless otherwise specified.

Symbol	Parameter	Limits		Units	Conditions
		Min.	Max.		
t <sub>RCC</sub>	Recall Cycle Time	1.4		μs	C <sub>L</sub> = 100pF + 1TTL gate V <sub>OH</sub> = 2.2V, V <sub>OL</sub> = 0.65V V <sub>IH</sub> = 2.2V, V <sub>IL</sub> = 0.65V
t <sub>RCP</sub>	Recall Pulse Width	300		ns	
t <sub>RCZ</sub>	Recall Disable Time		100	ns	
t <sub>ORC</sub>	Recall Enable Time	0		ns	
t <sub>ARC</sub>	Recall Data Access Time		1.1	μs	

Note:

(1) This parameter is tested initially and after a design or process change that affects the parameter.

**DEVICE OPERATION**

The configuration of the CAT22C12 allows a common address bus to be directly connected to the address inputs. Additionally, the Input/Output (I/O) pins can be directly connected to a common I/O bus if the bus has less than 1 TTL load and 100pF capacitance. If not, the I/O path should be buffered.

When the chip select ( $\overline{CS}$ ) pin goes low, the device is activated. When  $\overline{CS}$  is forced high, the device goes into the standby mode and consumes very little current. With the nonvolatile functions inhibited, the device operates like a Static RAM. The Write Enable ( $\overline{WE}$ ) pin selects a write operation when  $\overline{WE}$  is low and a read operation when  $\overline{WE}$  is high. In either of these modes, an array byte (4 bits) can be addressed uniquely by using the address lines ( $A_0$ – $A_7$ ), and that byte will be read or written to through the Input/Output pins ( $I/O_0$ – $I/O_3$ ).

The nonvolatile functions are inhibited by holding the  $\overline{STORE}$  input and the  $\overline{RECALL}$  input high. When the  $\overline{RECALL}$  input is taken low, it initiates a recall operation which transfers the contents of the entire E<sup>2</sup>PROM array into the Static RAM. When the  $\overline{STORE}$  input is taken low,

it initiates a store operation which transfers the entire Static RAM array contents into the E<sup>2</sup>PROM array.

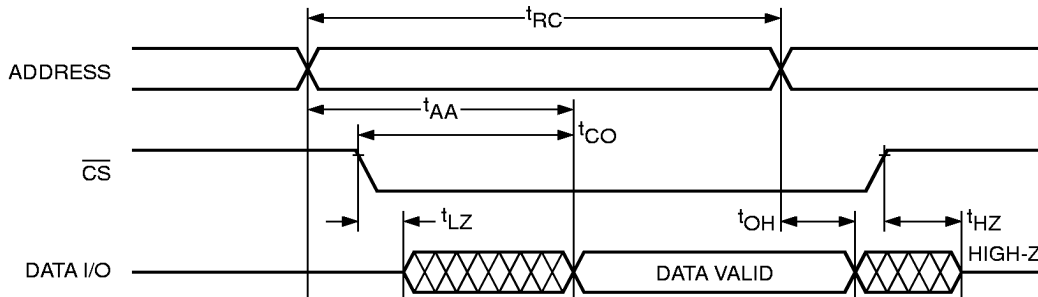
**Standby Mode**

The chip select ( $\overline{CS}$ ) input controls all of the functions of the CAT22C12. When a high level is supplied to the  $\overline{CS}$  pin, the device goes into the standby mode where the outputs are put into a high impedance state and the power consumption is drastically reduced. With  $I_{SB}$  less than 100 $\mu$ A in standby mode, the designer has the flexibility to use this part in battery operated systems.

**Read**

When the chip is enabled ( $\overline{CS} = \text{low}$ ), the nonvolatile functions are inhibited ( $\overline{STORE} = \text{high}$  and  $\overline{RECALL} = \text{high}$ ). With the Write Enable ( $\overline{WE}$ ) pin held high, the data in the Static RAM array may be accessed by selecting an address with input pins  $A_0$ – $A_7$ . This will occur when the outputs are connected to a bus which is loaded by no more than 100pF and 1 TTL gate. If the loading is greater than this, some additional buffering circuitry is recommended.

**Figure 1. Read Cycle Timing**



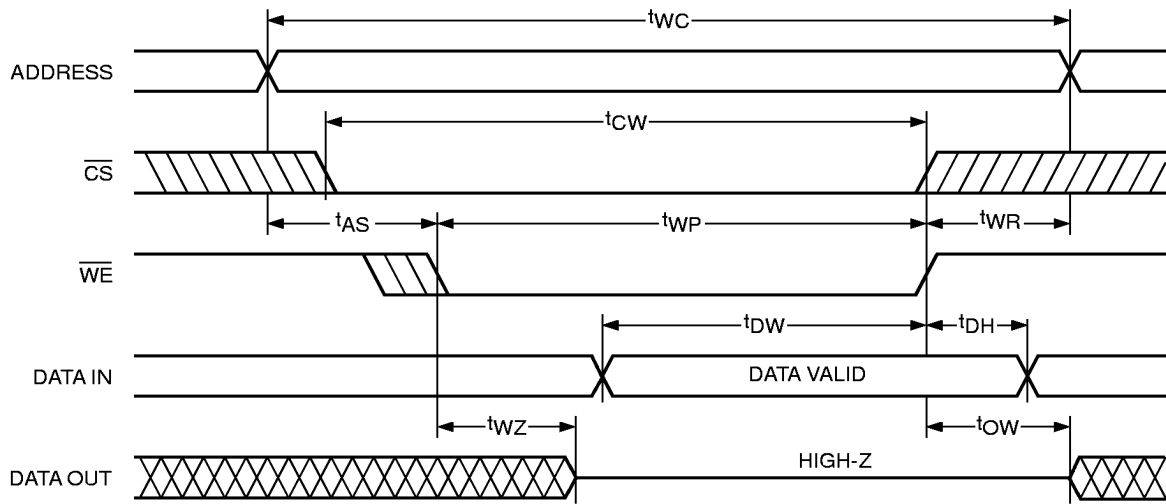
5153 FHD F06

**Write**

With the chip enabled and the nonvolatile functions inhibited, the Write Enable ( $\overline{WE}$ ) pin will select the write mode when driven to a low level. In this mode, the address must be supplied for the byte being written. After the set-up time ( $t_{AS}$ ), the input data must be supplied to pins I/O<sub>0</sub>–I/O<sub>3</sub>. When these conditions, in-

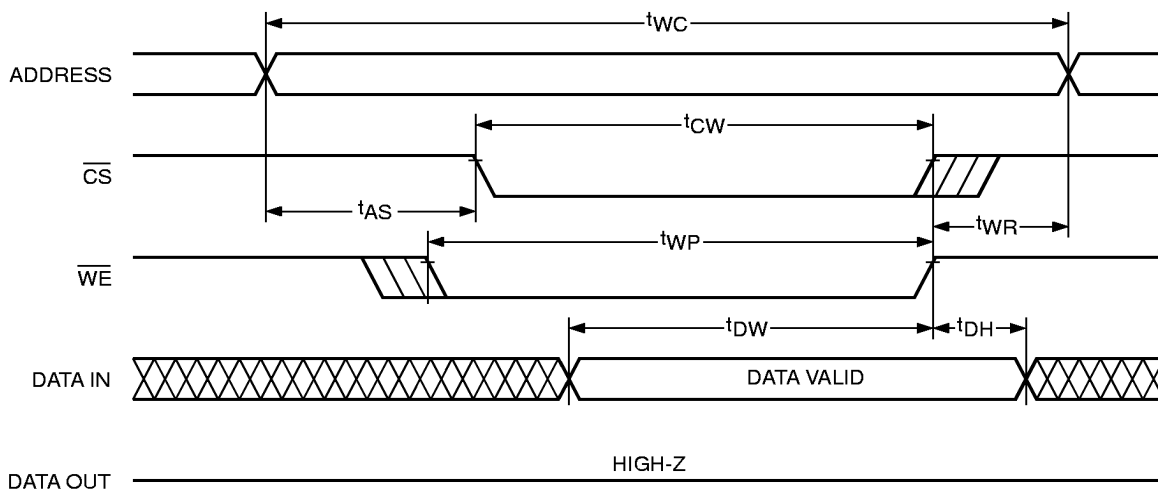
cluding the write pulse width time ( $t_{WP}$ ) are met, the data will be written to the specified location in the static RAM. A write function may also be initiated from the standby mode by driving  $\overline{WE}$  low, inhibiting the nonvolatile functions, supplying valid addresses, and then taking  $\overline{CS}$  low and supplying input data.

**Figure 2. Write Cycle Timing**



5155 FHD F04

**Figure 3. Early Write Cycle Timing**



5153 FHD F05

**Recall**

At any time, except during a store operation, taking the RECALL pin low will initiate a recall operation. This is independent of the state of  $\overline{CS}$ ,  $\overline{WE}$ , or  $A_0-A_7$ . After the RECALL pin has been held low for the duration of the Recall Pulse Width ( $t_{RCP}$ ), the recall will continue independent of any other inputs. During the recall, the entire contents of the E<sup>2</sup>PROM array is transferred to the Static RAM array. The first byte of data may be externally accessed after the recalled data access time from end of recall ( $t_{ARC}$ ) is met. After this, any other byte may be accessed by using the normal read mode.

If the RECALL pin is held low for the entire Recall Cycle time ( $t_{RCC}$ ), the contents of the Static RAM may be immediately accessed by using the normal read mode. A recall operation can be performed an unlimited number of times without affecting the integrity of the data.

The outputs I/O<sub>0</sub>–I/O<sub>3</sub> will go into the high impedance state as long as the RECALL signal is held low.

**Store**

At any time, except during a recall operation, taking the STORE pin low will initiate a store operation. This takes

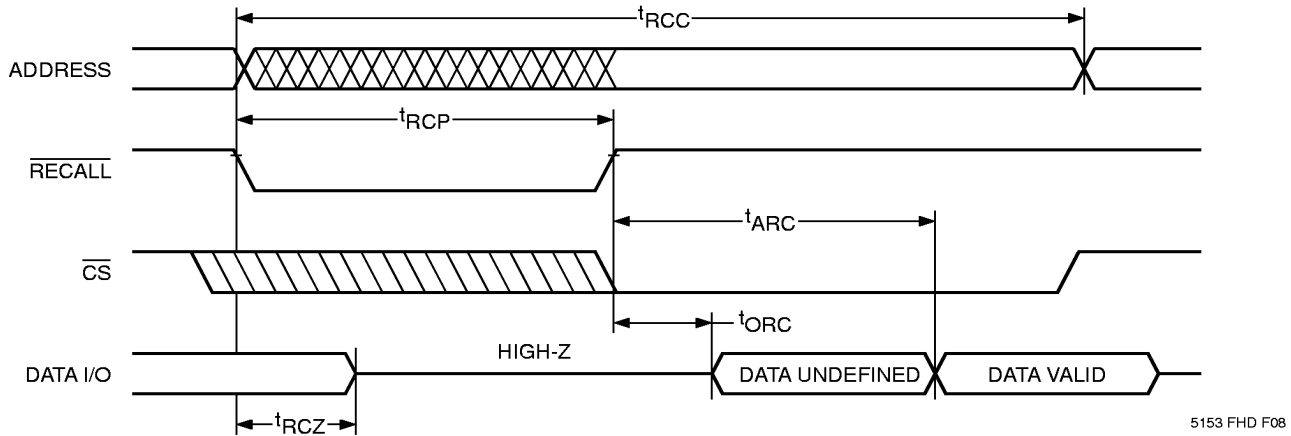
place independent of the state of  $\overline{CS}$ ,  $\overline{WE}$  or  $A_0-A_7$ . The STORE pin must be held low for the duration of the Store Pulse Width ( $t_{STP}$ ) to ensure that a store operation is initiated. Once initiated, the STORE pin becomes a “Don’t Care”, and the store operation will complete its transfer of the entire contents of the Static RAM array into the E<sup>2</sup>PROM array within the Store Cycle time ( $t_{STC}$ ). If a store operation is initiated during a write cycle, the contents of the addressed Static RAM byte and its corresponding byte in the E<sup>2</sup>PROM array will be unknown.

During the store operation, the outputs are in a high impedance state. A minimum of 100,000 store operations can be performed reliably and the data written into the E<sup>2</sup>PROM array has a minimum data retention time of 10 years.

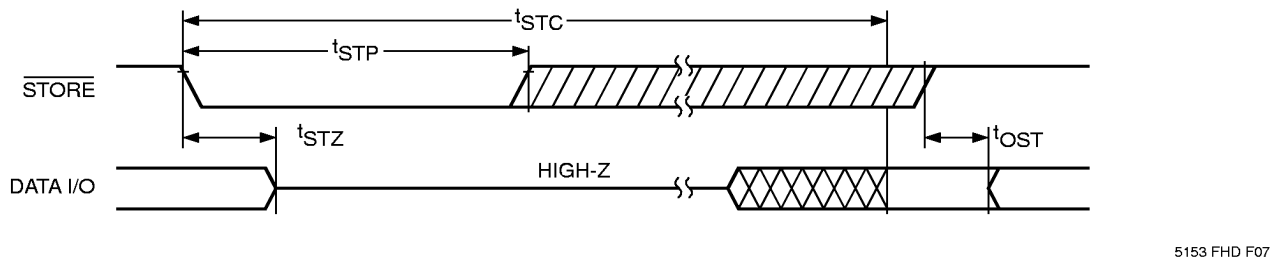
**DATA PROTECTION DURING POWER-UP AND POWER-DOWN**

The CAT22C12 has on-chip circuitry which will prevent a store operation from occurring when  $V_{CC}$  falls below 3.5V typ. This function eliminates the potential hazard of spurious signals initiating a store operation when the system power is below 3.5V typ.

**Figure 4. Recall Cycle Timing**

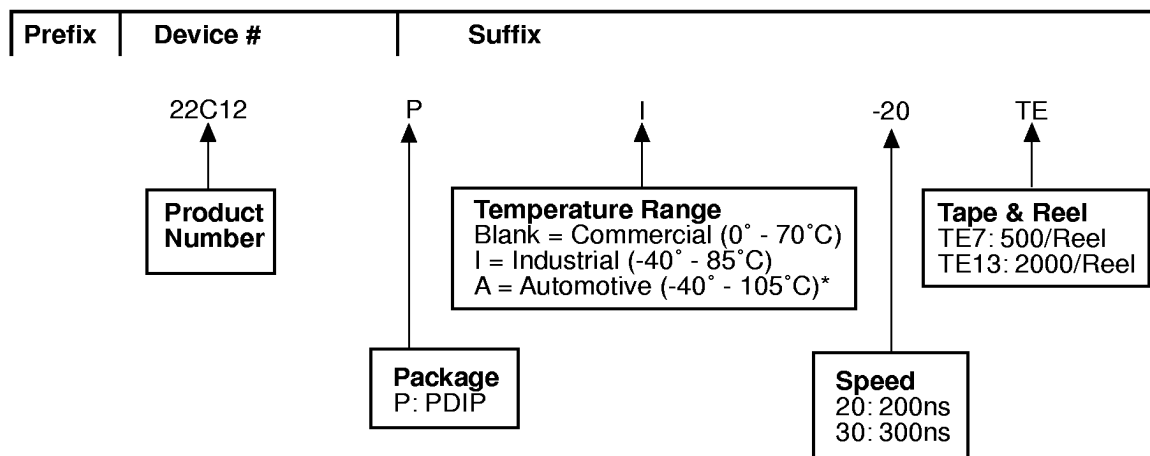


**Figure 5. Store Cycle Timing**





**ORDERING INFORMATION**



22C12 F08

\* -40° to +125°C is available upon request