Service Manual

Selective Level Meter SLM-12

SELECTIVE LEVEL METER SPM-12

Frequency range 200 Hz to 4.5 MHz (4.8 MHz)

Service Manual 608 C ...

1.1.78 GD
0.3.1.78 2444

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Wandel & Goltermann

PRECISION ELECTRONIC
MEASURING INSTRUMENTS

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CONTENTS

6. PRELIMINARY REMARKS TO SERVICE MANUAL

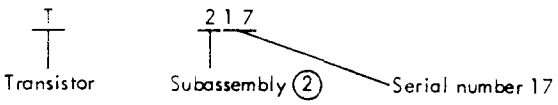
6. PRELIMINARY REMARKS TO SERVICE MANUAL

The following sections 6.1. to 6.5. explain the applied abbreviations, symbols and schematics as used in the "Service Handbook" (Service Manual and Appendix including circuit diagram, layout drawings and component lists).

The tabulated list of applied measurement items in section 6.6. presents the minimum complement of measurement equipment needed for all the measurements suggested in the Service Manual.

6.1. COMPONENT DESIGNATION

The various subassemblies are annotated with an individual number, for instance (2) Input amplifier. Each component located in this subassembly has the number 2 as its first digit. The two subsequent digits define the serial number of the component; for instance, resistor 96 would be R 296, or diode 22 is GI 222 and so on. The prefix letter characterises the type of component.

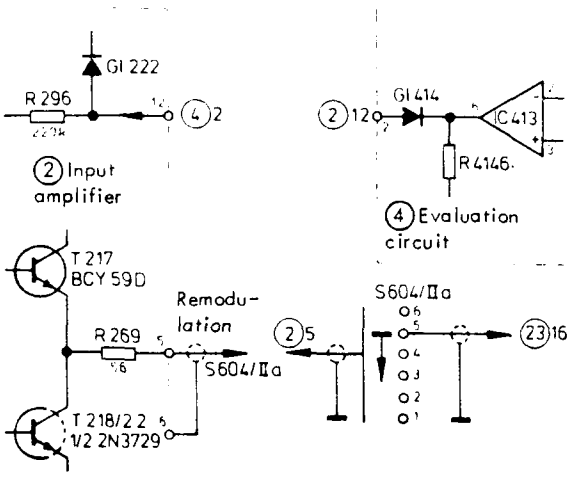


The abbreviations used to designate the components are given in section 6.3.

6.2. INTERCONNECTION BETWEEN SUBASSEMBLIES

Since the circuit diagrams are given separately for each subassembly, it is important that all interconnections are shown clearly. The following drawing explains the method used in this manual.

In the sketch below, point 12 of module (2) is connected to point 2 of module (4), and there is a shielded connection from point 5 of module (2) to switch S 604/IIa of subassembly (6).



6.3. ABBREVIATIONS AND SYMBOLS

In order to achieve greater simplicity, the following abbreviations and symbols have been used in the text and on the circuit diagrams:

6.3.1. Discrete components

Battery	B	
Socket	Bu	
Diode, rectifier	GI	
Zener diode	G	
LED	GI	
Thyristor	GI	
Varactor diode	GI	
Inductance	L	
Meter	J	
Capacitor	C	
Potentiometer	P	
Quartz crystal	Q	
Relay	Rel	
Relay contact	rel	
Resistor	R	
Thermistor PTC resistor	R	
Switch	S	
Fuse	Si	
Control lamp	SL	
Transistor	T	
Transistor (FET)	T	
Transformer	Ü	

Other important abbreviations:

(2) = subassembly (2) = circuit diagram (2)

607-L = Printed circuit board "L"

point 6 = Circuit reference/connection No. 6

TP 302 = Test point 302 (in subassembly (3))

6. PRELIMINARY REMARKS TO SERVICE MANUAL

6.3.2. Digital symbols

In the following, some of the most important digital logic-switching symbols are given, although the list is not presented as complete.

The two possible states of binary logic are designated "L" (low) and "H" (high). The voltages corresponding to each state are defined as being closer to- ∞ for the "L" range and closer to + ∞ for the "H" range.

6.3.2.1. General symbols

Symbol for negation

of an input

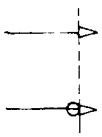
or output:

The dashed line represents the boundary line of the circuit.

Symbol for dynamic input

a) The operation is such that a transition of the input signal from L to H produces an effect similar to a "H" pulse

b) As in a) except operation effective on a H to L transition



Trigger inputs (G inputs)

Static control

operates with a "H" signal — G

operates with a "L" signal — G

one transition control

operates with a L - H transition — G

operates with a H - L transition — G

two transition controls

operates with a L-H-L pulse

operates with a H-L-H pulse

Preparatory inputs

E_X — E_X = preparing input

X — X = triggering input

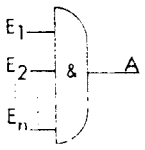
The circuit delivers a "H" pulse when the signal at X transits from L to H, providing a "H" signal is already present at input E_X.

Same as above. However, operative when signal at X input transits from H to L.

Note: Any storage time is to be noted (E_X) !

6.3.2.2. Digital signal gates

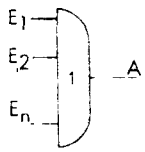
The AND gate



An "H" signal appears at output A only when an "H" signal is applied to all the inputs simultaneously. (Conjunction AND gate)

E_1	E_2	A
L	L	L
L	H	L
H	L	L
H	H	H

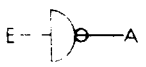
The OR gate



An "H" signal appears at the output when at least one input has an "H" applied to it. (Disjunction)

E_1	E_2	A
L	L	L
L	H	H
H	L	H
H	H	H

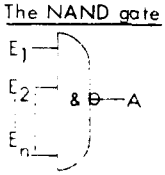
The NOT gate



The input signal always appears inverted at the output (Inverter)

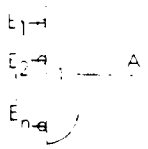
E	A
H	L
L	H

The NAND gate



An L signal appears at the output when an "H" signal is fed in at all inputs

E_1	E_2	A
L	L	H
L	H	H
H	L	H
H	H	L

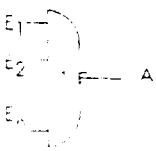


Alternative symbol
De Morgan's rule states the alternative symbol is true whereby:

$$A = \overline{E_1 \wedge E_2 \wedge \ldots E_n}$$

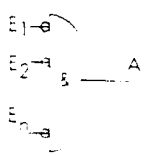
$$A = \bar{E}_1 \vee \bar{E}_2 \vee \ldots \bar{E}_n$$

The NOR gate



An L signal appears at the output, when at least one input has an "H" applied

E_1	E_2	A
L	L	H
L	H	L
H	L	L
H	H	L



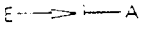
Alternative form
According to De Morgan's rule:

$$A = \overline{E_1 \vee E_2 \vee \ldots E_n}$$

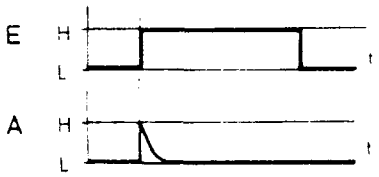
$$A = \bar{E}_1 \wedge \bar{E}_2 \wedge \ldots \bar{E}_n$$

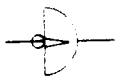
6. PRELIMINARY REMARKS TO SERVICE MANUAL

Differentiators



Symbol for circuits which convert a L-H transition into a L-H-L needle pulse





Symbol for circuits which convert a H-L transition into a H-L-H needle pulse

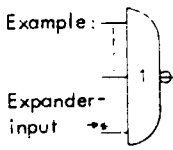
Wired AND

The symbol "wired AND" signifies that two or more circuits are wired in such a way that it simulates an AND logic without actually using an AND logic element

NOR Gate with power fan out

Where the logic element is capable of being loaded, the boundary line at the output side is drawn thick. This signifies that the output from this module is capable of driving several other modules simultaneously. In IC technology this is described as "fan out" capability.

Extending the input circuit by means of an "Expander" input



NOR circuit with four inputs. A further special input permits extending the logic circuit through external circuitry.

6.3.2.3. Bistable circuits with memory behavior

Two different basic types are discussed here: the Flip-Flop (FF) and the monostable (MF)

Flip-Flops

These toggle circuits have two stable states: Depending on the input signal, the flip-flop assumes one of the two states.

If one of the two states is defined as the normal position, then that output which assumes the H status is identified by a block bar.

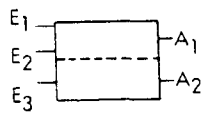
Static input signals (explanation and example)

If the signal at input E1 changes from L to H, then the FF toggles, independently of the slope of the L-H transition, to the status which is identified by an H status at output A_1. Thus, output A_2 is forced to be in the L status.

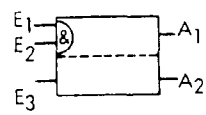
If the signal at input E_1 changes from H to L, then the FF remains in the previously assumed state. Only after the signal changes from L to H at input E_2, does the FF toggle to the second stable status identified by an H status at output A_2, (here taken as the normal position). Output A_1 is then forced to assume L status. This state is maintained by the FF even though the signal at input E_2 may change from H to L. Generally it is impermissible, to apply L-H transition signals simultaneously to inputs E_1 and E_2.

E_1	E_2	A_1	A_2	
H	L	H	L	
L	L	H	L	
L	H	L	H	
L	L	L	H	
H	L	H	L	
H	H			no FF action

If a flip-flop has several inputs without special identifications, then these inputs are disjunctive-coupled (OR gate).
That means:
The flip-flop toggles with a transition from L to H at inputs E_1 or E_2, or at both; the state becomes that identified by an H status at output A_1.

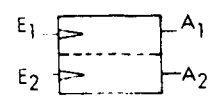


In the following symbol, the inputs E_1 and E_2 are conjunctive-coupled (AND gate).
That means:
The flip-flop first toggles when the two inputs E_1 and E_2 simultaneously assume the H status



Examples with dynamic signals at the inputs

The symbol represents a FF with two dynamic inputs E_1 and E_2. A L-H transition at input E_1 toggles the Flip-Flop to the state identified by an H appearing at A_1. Similarly a L-H transition at E_2 toggles the Flip-Flop to the state identified by an H appearing at A_2.



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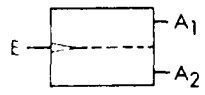
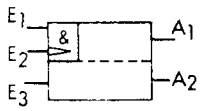
A symbol ⊳ (or ⊲) shown against the dashed line signifies that the Flip-Flop toggles from one stable state to the other alternately at each L-H (orH-L) transition. Thus an H (or L) appears alternately at A_1 and A_2.

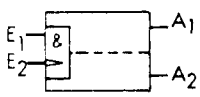


Flip-Flops with preparatory inputs

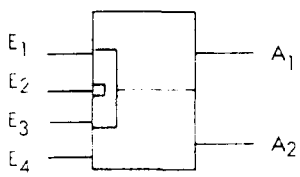
This Flip-Flop reacts to a L-H transition at the dynamic input E_2 only if simultaneously an H signal is present at input E_1. In this case the Flip-Flop toggles to the state in which an H appears at output A_1. E_3 is a static input.



In the following switching symbol, the dynamic input reacts when the two other inputs have been prepared, i.e. every L-H transition at input E_2 toggles the flip-flop when at the same time an H status exists at input E_1.



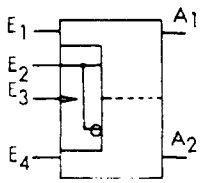
J-K Master Slave Flip-Flop (e.g. SN 7473 from Texas Instruments)



t_n		$t_n + 1$	
E_1	E_3	A_1	A_2
L	L	A_{1n}	A_{1n}
L	H	L	H
H	L	H	L
H	H	$\bar{A}_{1n}$	A_{1n}

t_n : point of time prior to clock pulse
$t_n + 1$: point of time after clock pulse
E_2 : clock input
E_4 : non-synchronuous reset input (independent from E_2)
"L" at E_4 forces A_1 to "L"

D Type Flip-Flop (edge-triggered) (also as on example of the SN 7474 from Texas Instruments)



Flip-Flop with preparing input E_2 and a higher ordered triggering input E_3

E_1 and E_4 are directly effective at the outputs.

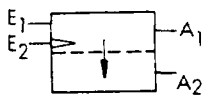
t_n	$t_n + 1$	
E_2	A_1	A_2
L	L	H
H	H	L

Monostable circuits

These also known as one-shot multivibrators. They have only one stable state (normally open) and a quasi-stable state (closed); whereby the arrow is drawn to show which output is in the normally closed state.

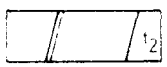
Example :
In the following monostable, an L status applied to the static input E_1, or a L-H transition at the dynamic input E_2, toggles the circuit from the normally open status to become the quasi-stable closed status (H state at output A_1)

After the retoggle time t_R, whose period is determined by an internal RC network, the monostable toggles back to the normally open status.

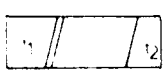


6.3.2.4. Delay networks

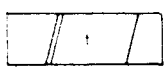
Delays the transition from L to H



Delays the transition from H to L



The transition from L to H as well as the transition from H to L are delayed, but the delay times are different



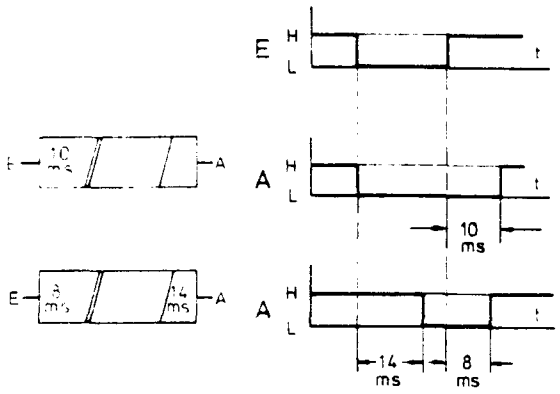
The transition L to H and from H to L are delayed by the same amount

The double slant stroke identifies the input side.

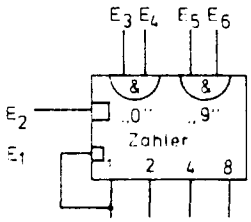
The delay time can be noted on the symbol in units of time, e.g. ms or µs.

6. PRELIMINARY REMARKS TO SERVICE MANUAL

Application examples:



6.3.2.5. BCD decade counter as integrated circuit



Condition for setting to figure 0:
E_3 and E_4 at H status
E_5 or E_6, or both, in L status

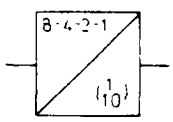
Conditions for setting to figure 9:
E_5 and E_6 at H status
E_3 or E_4, or both, in L status

During counting (pulse input E_2), there must be at least one input in the "L" status at each of the two AND networks.

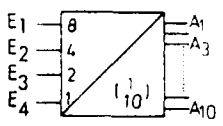
Figure	Outputs			
	1	2	4	8
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

6.3.2.6. Code converter as integrated circuit (IC)

Conversion of the 8-4-2-1 BCD code into the 1 out of 10 code



Simplified (example)



with individual inputs and outputs

6.4. COLOUR CODE

Abbreviations of connection lead colours

bl	blue
bk	barewire
br	brown
fl	transparent
ge	yellow
gn	green
gr	grey
rs	pink
rt	red
Schirm	screened
sw	black
vio	violet
ws	white
wsbl	white/blue
wsbr	white/brown

6.5. ORDERING SPARE PARTS

The most important locations for information pertaining to needed spare parts are the spare parts lists. Circuit component numbers prefixed with Bv. or WN are to be requested from the manufacturer.

Spare part orders must quote the serial number of the parent equipment and the circuit position of the required spare part, e.g.

BN 608 Nr. 524098 G/T 711

The type(BN) and serial number is located on a white tag located in the lower part of the left hand handle of the set. The letter suffix of the serial number is part of important information.

The designation of spare printed circuit boards can be seen on the circuit diagrams in the appendix. The P.C. board number consists of a boxed figure-letter combination, e.g.

608-A 3

The complete order designation is shown in the following example:

BN 608 Nr. 524098 G/608-A 3

6.6. TEST EQUIPMENT

The following equipment is recommended to measure voltages, signals, pulses etc. Similar equipment from other manufacturers may also be used.

6. PRELIMINARY REMARKS TO SERVICE MANUAL

DEVICE	Recommended type	Manufacturer
Level Measuring Setup	PSM-5	W&G
Level Generator 200 Hz...4.5 Hz	PS-12	W&G
Multiwatt Test Set with probe	EPM-1	W&G
Attenuator 75 Ω, 0 - 60 dB	3 D 120	Siemens
Universal Filter	UF-1	W&G
Return loss bridge	RFZ-5	W&G
Multimeter 100 kΩ/V	UM	AEG

Table 6-1 Test equipment

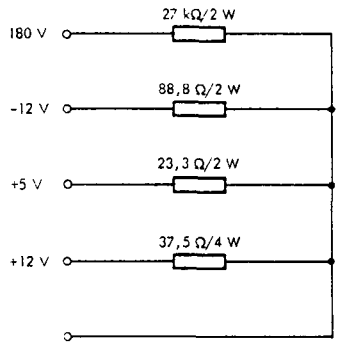
7. FAULT LOCALIZATION AND REPAIR INSTRUCTIONS

7. FAULT TRACING AND REPAIR

Caution : The mains power supply of the SPM-12 is a voltage converter. It is not protected against damage from short circuits or no-load operation.

After removal of the cover plates, the instrument must only be operated from a.d.c. power supply with current limiting (15 V, 5 A).

If the converter on its own is to be tested, a substitute load as per the following circuit must be connected :



7.1. Dismantling the instrument

7.1.1. Removal of instrument from case

Caution : Disconnect mains lead prior to opening the instrument case

7.1.1.1. Instruments from series C and D

The instrument chassis can be pulled out of the case after removal of four large screws located in the four corners of the front panel.

The chassis construction facilitates easy access to all subassemblies. Designations are printed on all modules, whose locations are shown in figs. 7-3 to 7-5.

7.1.1.2. Instruments from series E :

Remove diecast coverplate after unscrewing 6 Allan-head screws. (Key is on the rear panel). Then pull out complete chassis including front and rear panels.
If chassis is difficult to move, slacken Allan-head screws in bottom cover. See Fig. 7-1, white arrows.

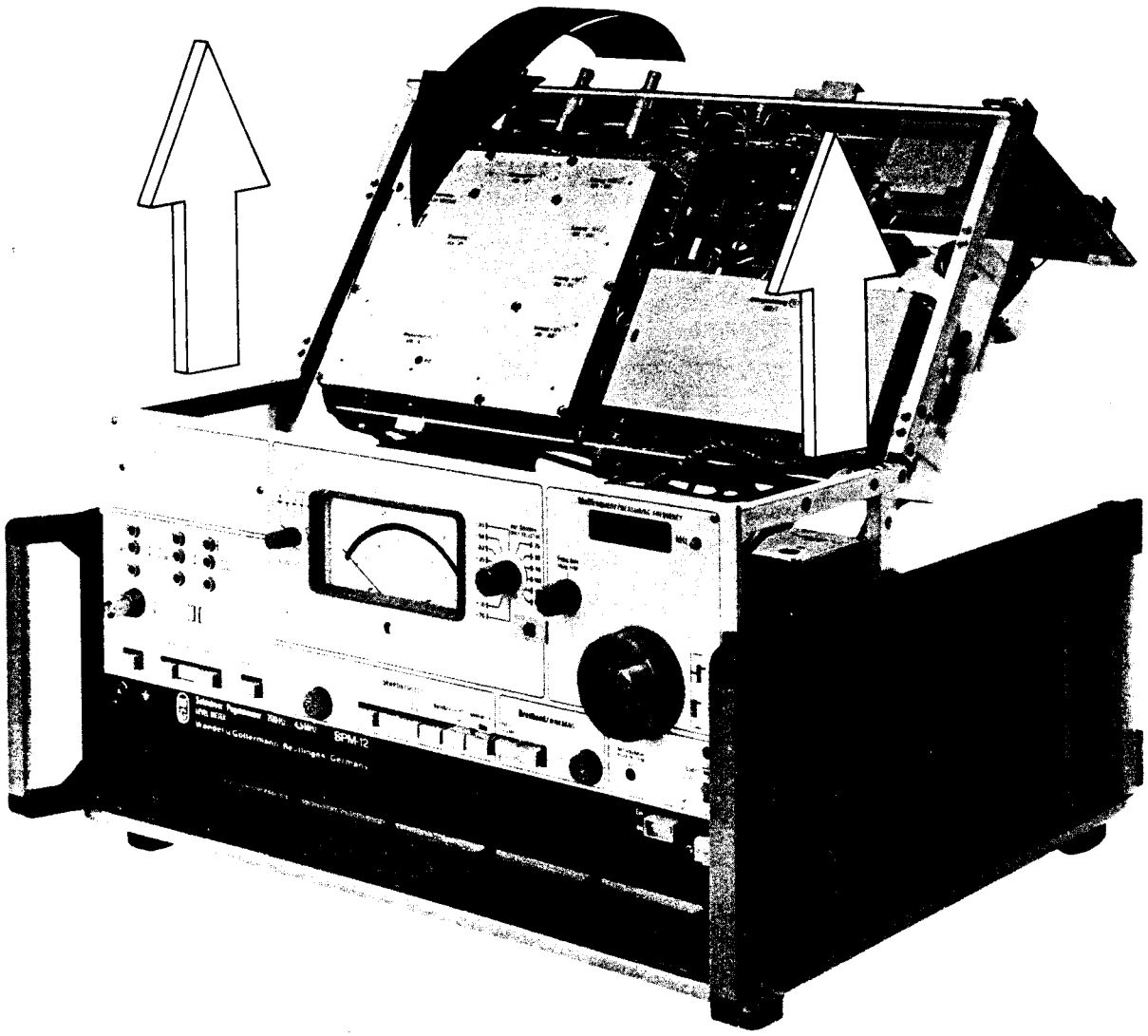


Fig. 7-1 Removal from case (white arrows) of E-series instrument, tilting of chassis (after removal from case, black arrow)

7.1.2. Opening of upper position of the chassis

The rear upper position of the chassis is tilted upwards to allow access to subassemblies located in the instrument centre. First remove instrument from case (see 7.1.1.). Then remove two screws from the the lower corners of the rear panel and two screws from the hinges at the upper side members of chassis frame (see Fig.7-2a). The rear chassis position can now be tilted upwards and secured in this position (see Fig.7-2b).

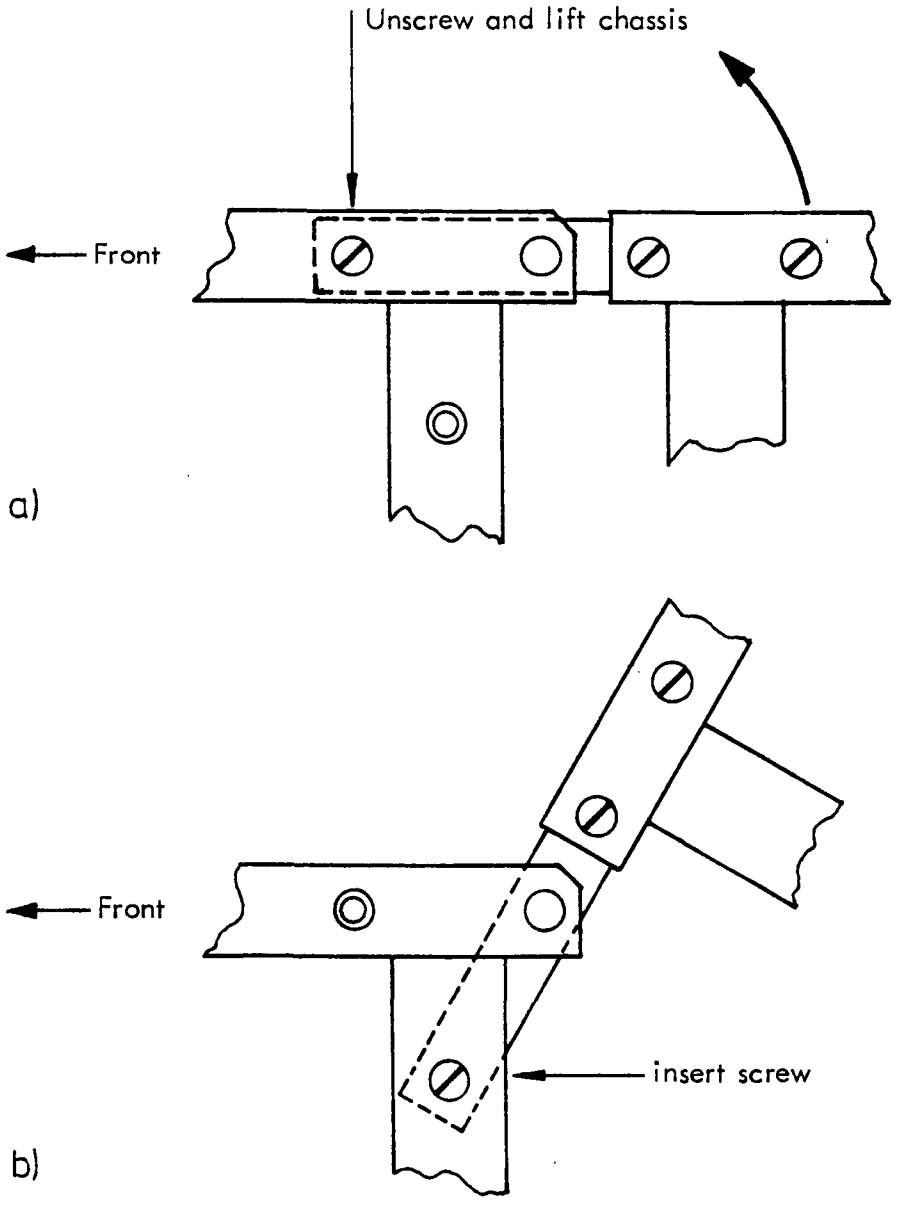


Fig. 7-2 Tilting of chassis (View of upper righthand side-member of chassis

7.1.3. Removal of screw box covers

The metal covers are secured by 4 screws (mains converter by 13 screws). The covers can be removed after unscrewing.
The covers of the metallized plastic boxes can be lifted by insertion of a small hook into the slot in the cover.

7.1.4. Removal of p.c. boards

P.C. boards can be lifted after removing the appropriate screws. If boards are to be removed, all electrical connections must be opened first (wires, edge connectors, coax. connectors).

Some connections are made via pins and sockets. It is important to remove and replace the p.c. board evenly to avoid bending the pins. The miniature coax.connectors are also sensitive. Make sure to align the plug pins with the socket centre. Most of the p.c. boards are earthed through printed circuit sections. Proper earth connection must be ensured when refitting p.c. boards.

7.1.5. Removal of knobs

To remove a knob, slacken the screw in the centre of the clamping device. (A special tool is available, type W-9, W-20 or W-21). Then pull knob off shaft. If the knob sticks, slightly tap the slackened centre screw.

7.2. Location of subassemblies

Fig. 7-3 to 7-5 show a chassis view with screen covers removed. Subassemblies, test points for the level diagram (◇) and most alignment elements are marked.

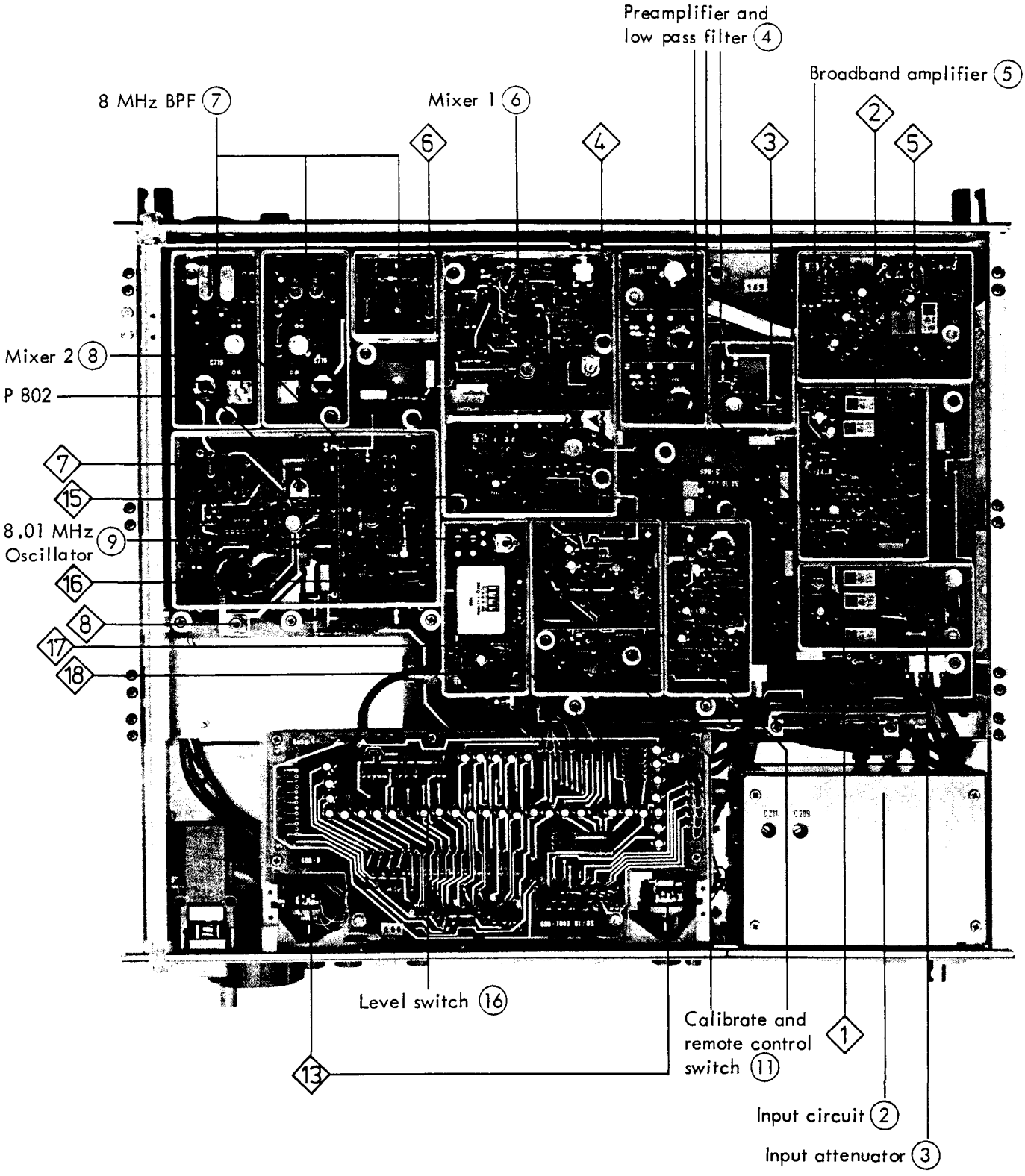


Fig. 7-3 Bottom view of SPM-12

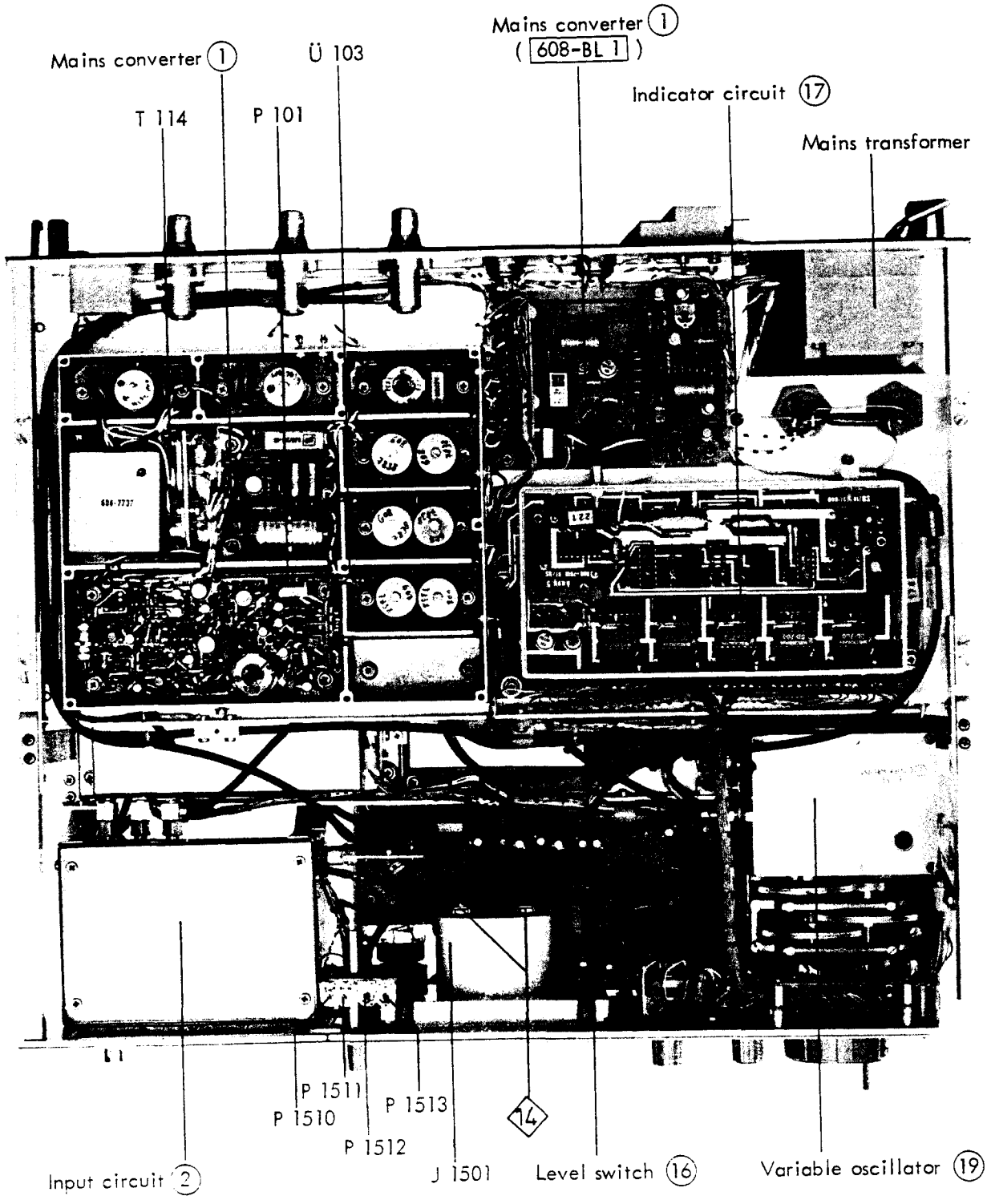


Fig. 7-4 Top view of SPM-12

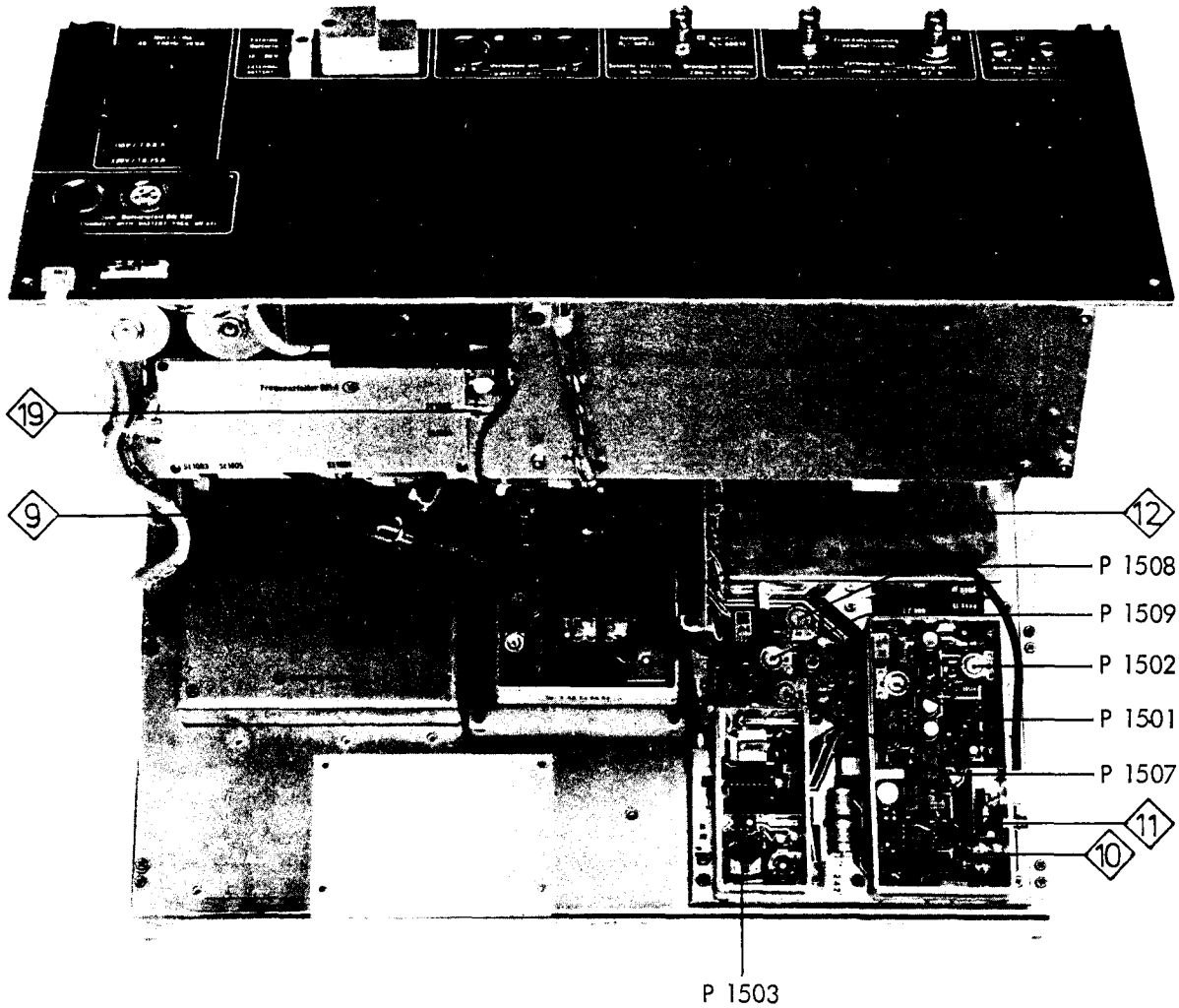


Fig. 7-5 Top view of SPM-12 chassis tilted up

7.3. Fault tracing

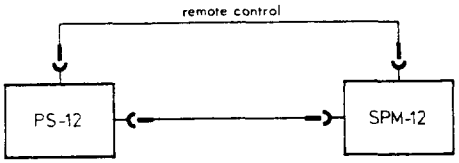
We recommend the following preliminaries to fault tracing :

- check that no operational error has been made
- consult the description of special cases (section 7.3.1.)
- proceed as per fault tracing diagram. The fault tracing diagram is designed to cover instrument faults, but not operational errors.
  Fault tracing within a subassembly requires knowledge of the circuit description (Chapter 10)

7.3.1. Special cases

- "Selective measurements"

Frequency indicator permanently at 2000



a) No level indication, but calibrator works : variable oscillator faulty

b) Correct level indication, but calibration does not function : Frequency divider defective

No frequency indication : check indicator circuit, + 5 V switching, and 180 V supply

- "Calibrate": No function in "Measurement" nor "Calibrate"

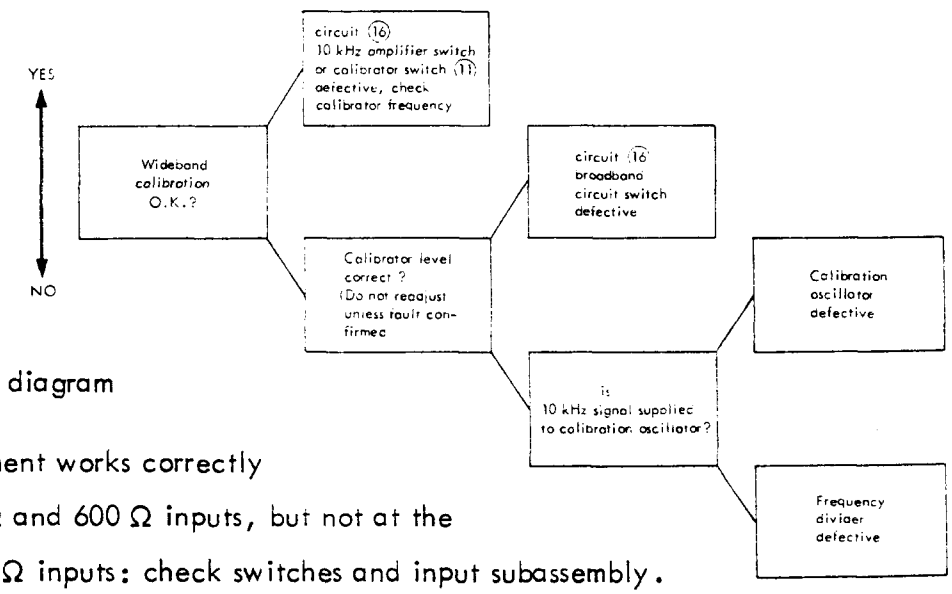
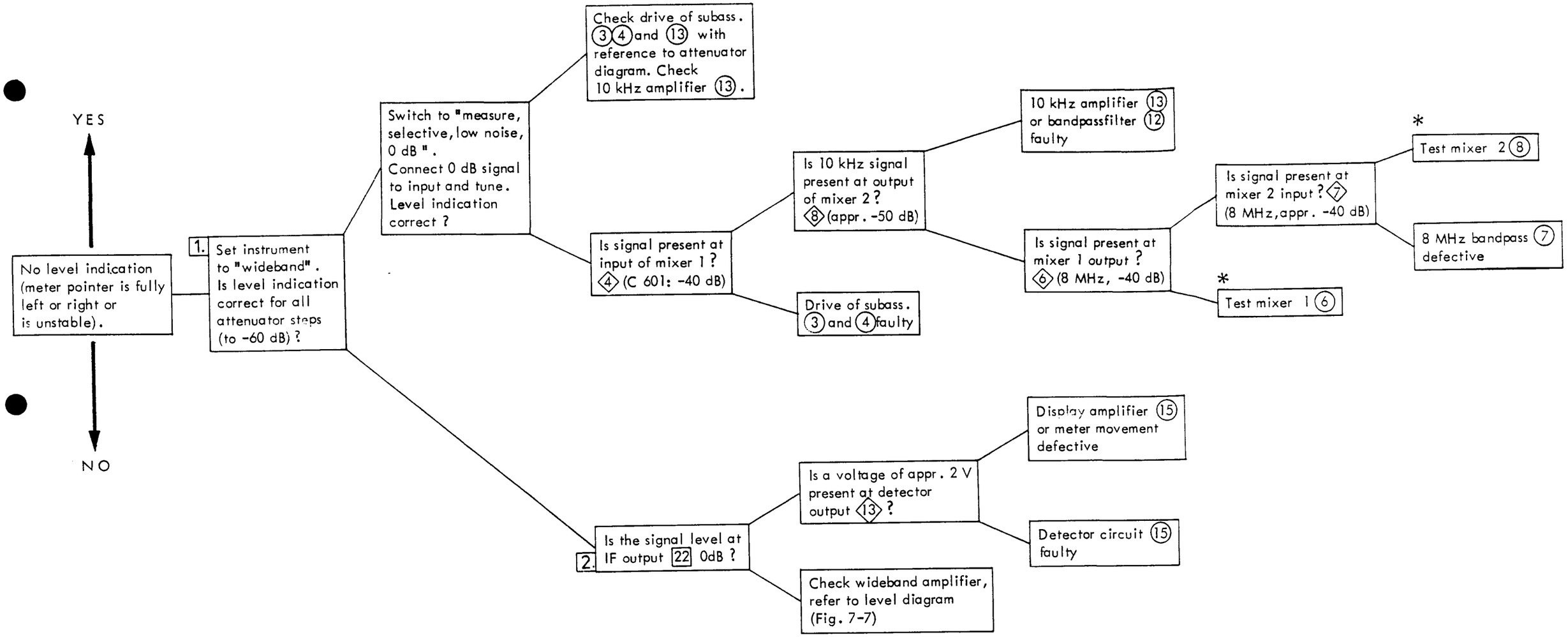
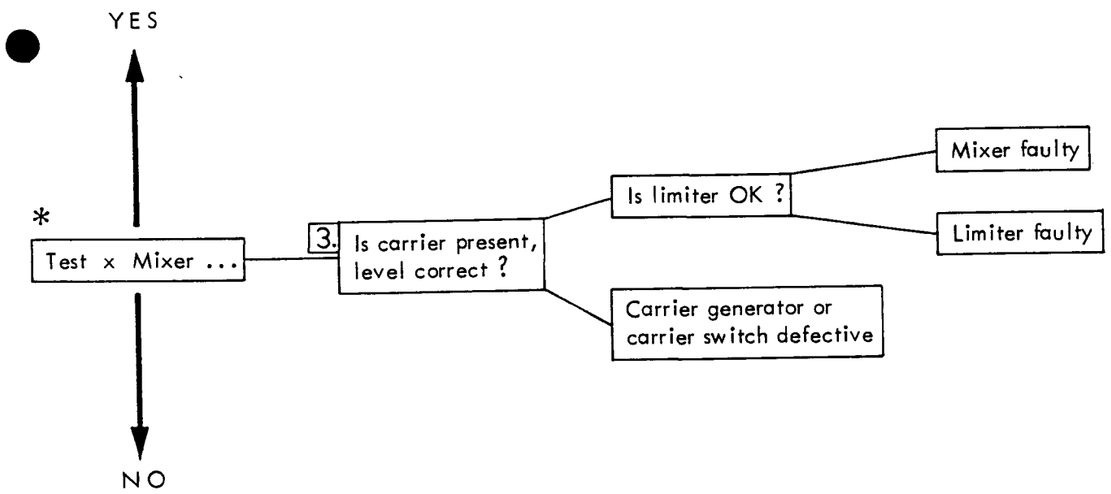


Fig. 7-6 a
Fault tracing diagram

- The instrument works correctly at the 75 Ω and 600 Ω inputs, but not at the 124 Ω-150 Ω inputs: check switches and input subassembly.





Notes:

1. Change input level and SPM-12 sensitivity accordingly from -60 to +20 dB.
2. If the level indication is wrong only at certain switch positions, the fault is located in subass. (3), (4), (5) or (16) and can be quickly located by means of the attenuator diagram. Otherwise set SPM-12 and generator level to 0 dB.
3. Damage of cables or the miniature connector Bu 1109 - St 3 (19) or Bu 1102 - Bu 1101 may lead to interruption or high attenuation in the carrier path of mixer 1.

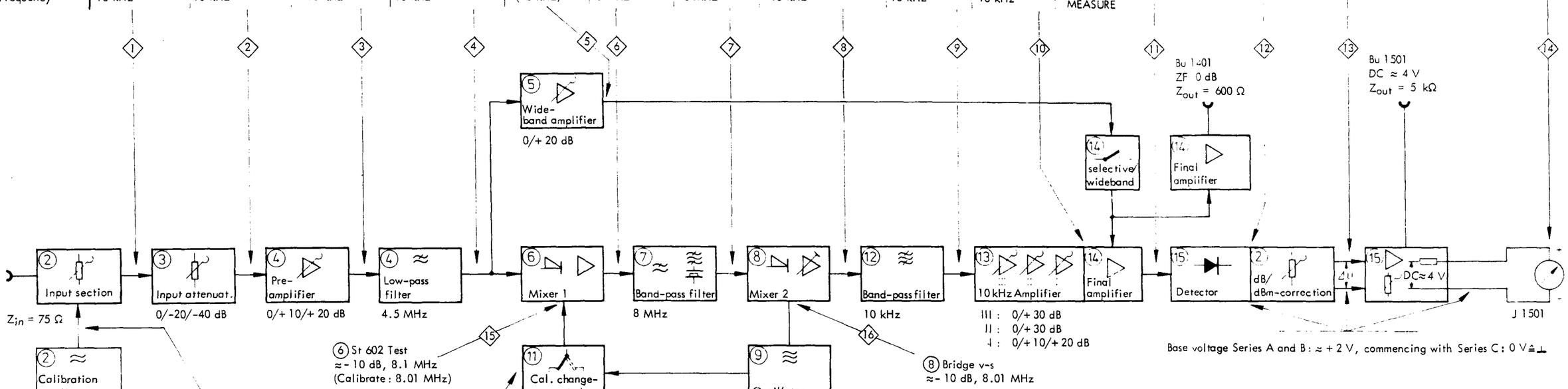
Fig. 7-6 Fault Finding Plan SPM-12

Measure

Test point	③ R 304	④ TP 401	④ Bridge f-e	⑥ C 601	⑤ Point 12	⑦ Bridge d-c	⑧ Bridge z-y	⑧ St 802 Test	⑫ St 1201	⑬ R 1334	⑮ Bridge a-b	⑮ between point D and b×	⑯ calibr. point (slider)	⑮ J 1501
Level	0 dB (0 dB)	- 40 dB (- 20 dB)	- 40 dB (- 20 dB)	- 40 dB (- 20 dB)	(- 20 dB)	- 38 dB	≈ -44 dB	- 51 dB, Align. P 802	≈ -41 dB	≈ -21 dB	≈ -10 dB	⊿U = 5.3 V	⊿U = 1.87 V	477 µA
Frequency	100 kHz	100 kHz	100 kHz	100 kHz	(100 kHz)	8 MHz	8 MHz	10 kHz	10 kHz	10 kHz	(10 kHz (100 kHz)	DC voltage	DC voltage	Direct current
Notes :				at St 601 Test : - 55.6 dB (-35.6 dB)				both poles + 12 V DC				× Series A and B: ...D and 4		for 0 dB reading

Calibrate

Level	- 40 dB (- 40 dB)	- 80 dB (- 40 dB)	-80 dB (- 20 dB)	- 80 dB (- 20 dB)	(- 20 dB)	- 78 dB	≈ -84 dB	- 91 dB	≈ -81 dB	≈ -21 dB	other values as with MEASURE
Frequency	10 kHz	10 kHz	10 kHz	10 kHz	(10 kHz)	8 MHz	8 MHz	10 kHz	10 kHz	10 kHz	



Calibrate

Test point	⑩ St 901	⑩ Bu 1002	② St 207	⑪ C 1125
Level	≈ -3 dB	Pulse	- 40 dB	≈ -3 dB
Frequency	8.01 MHz	10 kHz	10 kHz	8.01 MHz

Measurement condition :

Measure : SPM-12 in mode "low noise selective" or "wideband" respectively. Input level 0 dB, input frequency 100 kHz, level switch to 0 dB.

Calibrate : SPM-12 in mode "low noise selective" or "calibrate wideband" respectivly. Values in brackets for "wideband".

Levels are measured with a selective level meter and probe ≧ 10 kΩ II ≧ 7 pF, e.g. PM-5 with probe head TK-8 (Wandel & Goltermann).
It should be considered that the load by the probe head may result in a level variation of points of high impedance.

D.C. voltages measured with meter of 100 kΩ/V to ground

Fig. 7-7 Level diagram

	S 1601	Sensitivity dB	Pre-attenuator	Pre-amplifier	Wideband-amplifier	Σ
Measure	1	+20	-40	0	0	-40
	2	+10	-40	+10	0	-30
	3	0	-20	0	0	-20
	4	-10	-20	+10	0	-10
	5	-20	0	0	0	0
	6	-30	0	+10	0	+10
	7	-40	0	+20	0	+20
	8	-50	0	+10	+20	+30
	9	-60	0	+20	+20	+40
Calibrate			0	+20	0	+20

Fig. 7-8 Attenuator-amplifier combination in mode "wideband" (attenuation in dB)

S 1601		Wideband part			10-kHz-Amplifier							
					Measure				Calibrate			
	Sensitivity dB	pre-attenuator	Pre-amplifier	Σ	3	2	1	Σ	3	2	1	Σ
1	+20	-40	0	-40	0	0	0	0	+30	+30	0	+60
2	+10	-40	0	-40	0	0	+10	+10	+30	+30	0	+60
3	0	-40	0	-40	0	0	+20	+20	+30	+30	0	+60
4	-10	-40	0	-40	+30	0	0	+30	+30	+30	0	+60
5	-20	-40	0	-40	+30	0	+10	+40	+30	+30	0	+60
6	-30	-40	0	-40	+30	0	+20	+50	+30	+30	0	+60
7	-40	-40	0	-40	+30	+30	0	+60	+30	+30	0	+60
8	-50	-40	0	-40	+30	+30	+10	+70	+30	+30	0	+60
9	-60	-40	+10	-30	+30	+30	+10	+70	+30	0	+20	+50
10	-70	-20	0	-20	+30	+30	+10	+70	+30	0	+10	+40
11	-80	-20	+10	-10	+30	+30	+10	+70	+30	0	0	+30
12	-90	0	0	0	+30	+30	+10	+70	0	0	+20	+20
13	-100	0	+10	+10	+30	+30	+10	+70	0	0	+10	+10
14	-110	0	+20	+20	+30	+30	+10	+70	0	0	0	0
15	-120	0	+20	+20	+30	+30	+20	+80	0	0	0	0

Fig. 7-9 Attenuator/amplifier combination in mode selective, low noise, dB (attenuation in dB)

S 1601	Sensitivity (dBm)	Wideband part			10-kHz-Amplifier							
		pre-attenuator	pre-amplifier	Σ	Measure 3	2	1	Σ	Calibrate 3	2	1	Σ
1	+20	-40	0	-40	0	0	0	0	+30	+30	0	+60
2	+10	-40	0	-40	0	0	+10	+10	+30	+30	0	+60
3	0	-40	0	-40	0	0	+20	+20	+30	+30	0	+60
4	-10	-40	0	-40	+30	0	0	+30	+30	+30	0	+60
5	-20	-40	0	-40	+30	0	+10	+40	+30	+30	0	+60
6	-30	-40	0	-40	+30	0	+20	+50	+30	+30	0	+60
7	-40	-40	0	-40	+30	+30	0	+60	+30	+30	0	+60
8	-50	-40	+10	-30	+30	+30	0	+60	+30	0	+20	+50
9	-60	-20	0	-20	+30	+30	0	+60	+30	0	+10	+40
10	-70	-20	+10	-10	+30	+30	0	+60	+30	0	0	+30
11	-80	0	0	0	+30	+30	0	+60	0	0	+20	+20
12	-90	0	+10	+10	+30	+30	0	+60	0	0	+10	+10
13	-100	0	+20	+20	+30	+30	0	+60	0	0	0	0
14	-110	0	+20	+20	+30	+30	+10	+70	0	0	0	0
15	-120	0	+20	+20	+30	+30	+20	+80	0	0	0	0

Fig. 7-10 Attenuator-amplifier combination in mode selective-low distortion dBm (attenuation in dB)

S 1601	Sensitivity dB	Wideband part			10-kHz-Amplifier							
		pre-attenuator	pre-amplifier	Σ	Measure 3	2	1	Σ	Calibrate 3	2	1	Σ
1	+20	-40	0	-40	0	0	0	0	+30	+30	0	+60
2	+10	-40	0	-40	0	0	+10	+10	+30	+30	0	+60
3	0	-40	0	-40	0	0	+20	+20	+30	+30	0	+60
4	-10	-40	0	-40	+30	0	0	+30	+30	+30	0	+60
5	-20	-40	0	-40	+30	0	+10	+40	+30	+30	0	+60
6	-30	-40	+10	-30	+30	0	+10	+40	+30	0	+20	+50
7	-40	-20	0	-20	+30	0	+10	+40	+30	0	+10	+40
8	-50	-20	+10	-10	+30	0	+10	+40	+30	0	0	+30
9	-60	0	0	0	+30	0	+10	+40	0	0	+20	+20
10	-70	0	+10	+10	+30	0	+10	+40	0	0	+10	+10
11	-80	0	+20	+20	+30	0	+10	+40	0	0	0	0
12	-90	0	+20	+20	+30	0	+20	+50	0	0	0	0
13	-100	0	+20	+20	+30	+30	0	+60	0	0	0	0
14	-110	0	+20	+20	+30	+30	+10	+70	0	0	0	0
15	-120	0	+20	+20	+30	+30	+20	+80	0	0	0	0

Fig. 7-11 Attenuator-Amplifier combination in mode "selective-low noise" (attenuation in dB)

8. CHECKING OF IMPORTANT TECHNICAL SPECIFICATIONS

8. CHECKING OF IMPORTANT TECHNICAL SPECIFICATIONS

This section describes methods to test the most important performance parameters of the equipment. Where possible, commercially available test equipment has been suggested.

If not specifically stated otherwise, the tests should be performed at mains voltages and temperatures within the rated operating conditions. A warm-up time of 30 minutes as stated in the specifications has to be allowed for.

Aim of the specification test is to confirm that the indication of a measured value is within the guaranteed limits of error. The specification test is only applicable without reservations if the intrinsic error of the test equipment that is used is negligible. Otherwise, the following rule applies. If the intrinsic error of the utilized test equipment is $\pm m$, and if the guaranteed error limit for the equipment under test is $\pm e$, then :

- a result exceeding $\pm (e + m)$ proves that the equipment under test definitely exceeds the guaranteed error limits.
- a result better than $\pm (e - m)$ proves that the equipment under test is definitely within the guaranteed error limits.

The criterion e is quoted in the description of each measurement. The criterion m depends upon the utilized test equipment and has to be determined in each individual case.

The measuring method itself excerts influence upon m only if the prescribed test equipment is said to be mandatory, or if special conditions need to be observed.

The suggested order should be observed when the equipment specifications are to be tested systematically. A re-alignment of the equipment should be attempted only if it is found to exceed the limit $\pm (e + m)$.

8.1. Frequency Indication

Required test equipment :

1 Level Generator PS-12 W&G

1 Frequency counter FZ-4 W&G

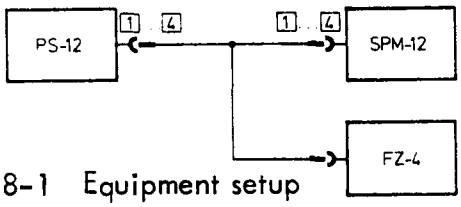


Fig.8-1 Equipment setup

Equipment setting :

PS-12 any frequency (e.g. 1000.00 kHz)
any level (e.g. 0 dB)

SPM-12 selective, smallest bandwidth [19] expanded meter scale [13]

Tune level meter for maximum meter indication. Permissible error (e) of frequency indication : $\pm 5 \times 10^{-6} \pm 10$ Hz

The frequency calibration of the SPM-12 may also be checked by means of a standard frequency signal.

8.2. Level indication 0 dB/dBm, f = 10 kHz

Required test equipment :

Level Generator 10 kHz, e.g. PS-12 W&G

Milliwatt Test Set with accessories : EPM-1 W&G

Probe Head TK-10, 75 Ω W&G

Attenuator 9.03 dB, 75 Ω W&G

T-piece and connector adapters according to connector system. (Spinner, W&G)

The SPM-12 may be converted from voltage, level calibration (dB) to power level calibration (dBm), see section 5.2.5. of the instruction manual. Therefore, either the test setup 8.2.1. (dB voltage level) or 8.2.2. (dBm, power level) may be used.

8.2.1. Level check 0 dB, f = 10 kHz

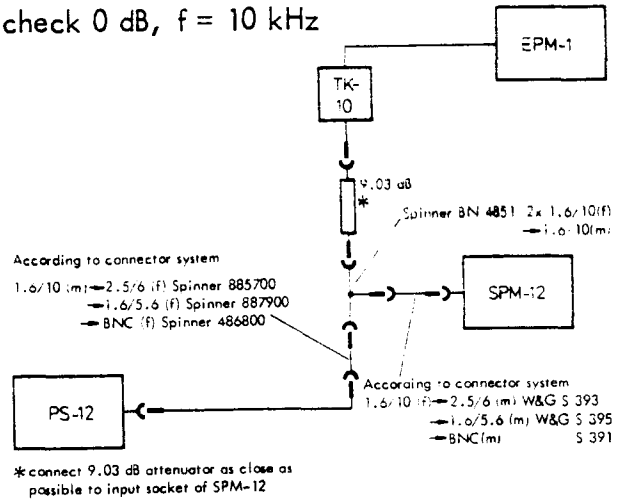


Fig.8-2 Measuring setup

Instrument setting :

SPM-12 : Measuring range 0 dB, expanded scale ([13] and [14] to "0")
Wideband or selective (bandwidth 500 Hz) [19]
f = 10 kHz ([15] , [17])
R_e = 100 kΩ ([7])

PS-12 : Z = 75 Ω ([11])
Level : 0 dB [5] [6] [7])
f = 10 kHz ([14] , [16])

Switch off SPM-12 and check that the mechanical meter zero is accurate, the equipment being in horizontal position. Correct zero setting if necessary with adjustment screw underneath meter face.

Calibration of Milliwatt Test Set EPM-1 :

Connect 9.03 dB attenuator and probehead TK-10. Set EPM-1 to calibrator level 0 dB, R_i = 0 (S 303). Connect attenuator and probehead to calibrator output Bu 303 and zero under indication with pot. P 202.

Test :

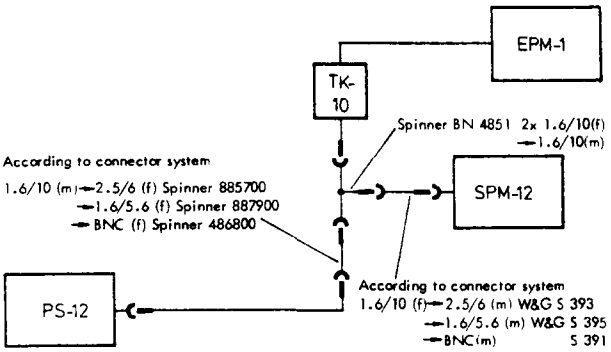
Connect probehead TK-10 via attenuator to the input of SPM-12, see Fig. 8-2. Set generator level until EPM-1 reads zero (dB). Calibrate SPM-12 in the mode used (wideband or selective), change over to "measurement" and note the deviation of the SPM-12 indication.

Permissible error limit in mode "wideband", "selective/low noise" or "low distortion"

± 0.1 dB

Tune the SPM-12 carefully to maximum signal when using the selective measurement mode.

8.2.2. Level check 0 dBm, f = 10 kHz



Connect probe head TK-10 as close as possible to input of SPM-12

Fig. 8-3 Test setup

Instrument setting :

SPM-12 : Measuring range 0 dBm, expanded scale (13 and 14 to 0)
Measurement mode "wideband" or "selective" (bandwidth 500 Hz) 19
f = 10 kHz (15 , 17) Impedance 100 kΩ (7)
Impedance 75 Ω (11), Level: 0 dBm (5 , 6 , 7)
f = 10 kHz (14 , 16)

Check mechanical zero of SPM-12 meter scale prior to measurement (switch power off)

Calibration of EPM-1: Set calibrator to 0 dBm, R_i = 0

Connect TK-10 to calibrator output Bu 303 and set meter to 0 dBm with P 202.

Measurement :

Connect probehead TK-10 to input of SPM-12. Set generator level of PS-12 for zero indication of EPM-1. Calibrate SPM-12 in the measurement mode being used (selective or wideband). After calibration read deviation of SPM-12 indication permissible error in "wideband", "selective/low noise" or "selective/low distortion" mode :

± 0.1 dBm

Tune SPM-12 carefully to signal maximum if using selective mode.

8.3. Frequency response (200 Hz) 2 kHz - 4.5 MHz (4.8 MHz, 6 MHz)

Required test equipment

1 Generator, e.g. PS-12		W&G
1 Milliwatt Test Set EPM-1 with accessories :		W&G
1 Probe head TK-10, 75 Ω		W&G
1 T-pad	75 Ω BN 595/1	W&G

1 Connector adapters as per connector system

8.3.1. Measuring range 0 dBm

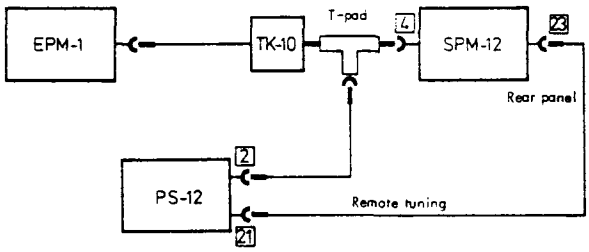


Fig. 8-4 Test setup

Connect T-pad directly without cable, to the input socket Bu 202 of SPM-12.

Equipment setting :

SPM-12 : - Switch equipment to power level calibration. Measuring range 0 dBm, expanded scale (13, 14 to 0),. Measuring mode "wide-band" or "selective" (bandwidth 500 Hz 19)
f = 10 kHz (15, 17)
Impedance = 75 Ω (5)

PS-12 : - Set equipment to voltage level calibration (dB), output level aprrox. - 3 dB (5, 6, 7)
f = 10 kHz (14, 16)
Impedance = 75 Ω (11)

EPM-1: - Measuring range 0 dBm ± 0.2 dB

Measurement :

Set send level for 0 dBm indication on EPM-1. Set SPM-12 indication to 0 dBm by adjusting the calibration pot. 18 (selective) or 20 (wideband).

Tune SPM-12 over the range (200 Hz[1]) 2 kHz...4.5 MHz (4.8 MHz, 6 MHz). Keep SPM-12 input level constant. Note maximum of positive or negative deviation of SPM-12 level indication.

Permissible frequency response (e) of level indication, relative to f = 10 kHz is given in table 8-1.

Series	Freq. range	Selective	Wideband
C...F	200 Hz to 300 Hz	± 0.07 dB	± 0.15 dB
	300 Hz to 4.5 MHz	± 0.07 dB	± 0.1 dB
	4.5 MHz to 4.8 MHz	± 0.4 dB	± 0.45 dB
G...	200 Hz to 300 Hz	± 0.07 dB	± 0.15 dB
	300 Hz to 5 MHz	± 0.07 dB	± 0.1 dB
	5 MHz to 6 MHz	± 0.15 dB	± 0.25 dB

Table 8-1 Frequency response of level indication

1) Valid for equipment fitted with 25 Hz filter. Perform measurement in 25 Hz-bandwidth.

Note : In mode "selective", the PS-12 is remotely controlled from SPM-12. To achieve synchronization, a frequency calibration of the PS-12 is necessary (see section 2.6. of the PS-12 instruction manual).

8.3.2. Frequency response of level indication in ranges other than 0 dB/dBm.
Required test equipment as per 8.3.1., and additionally
1 adjustable attenuator, e.g. RT-1 W&G

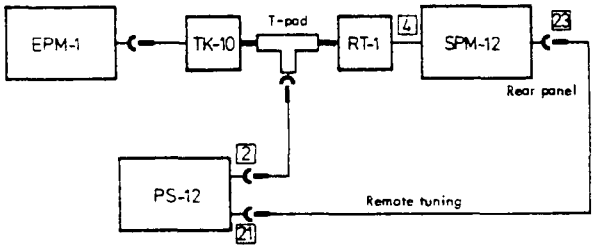


Fig. 8-5 Test setup

Connect RT-1 and SPM-12, T-pad and RT-1 as close together as possible i.e. without use of interconnecting cables.

Equipment setting :

The RT-1 is used to reduce the SPM-12 input level. If an RT-1 is not available other attenuator pads may be used. It is necessary to know the frequency response of the pads if it is not so small that the error may be neglected.

Measurement : as per 8.3.1.

The error limit (e) of the frequency response may be seen from table 8-2

	Selective	Wideband
(200 Hz) 2 kHz... 4.5 MHz	± 0.1 dB	
300 Hz... 4.5 MHz		± 0.10 dB
200 Hz... 4.5 MHz		± 0.15 dB

Table 8-2 Error limits of level indication

8.4. Level indication 0 dBm, balanced inputs

(only for option BN 608/1)

Required test equipment :

1 Milliwatt Test Set with accessories :	EPM-1	W&G
1 Balanced Probe Head	TKS-10	W&G
1 Probe head Adaptor	TKSA-150	W&G
1 do.	TKSA-600	W&G
1 Calibration Adaptor	TKSE-150	W&G
1 do.	TKSE-600	W&G
1 Level Generator, e.g.	PS-12	W&G

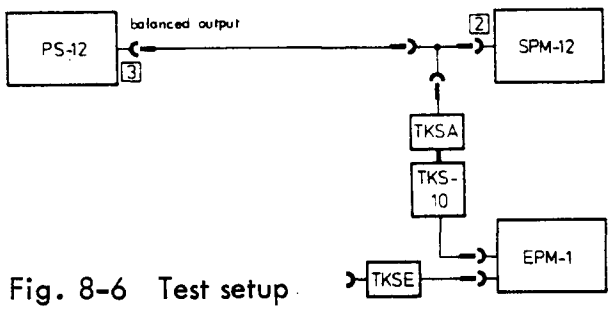


Fig. 8-6 Test setup

Equipment setting :

SPM-12 : Switch to power level calibration (dBm) . Measuring range 0 dBm, expanded scale ([13] , [14] to 0)
Wideband measuring mode [19]
Select high impedance [17]
Press button "150 Ω" input [6]

PS-12 : Switch to voltage level calibration (dB)
Impedance 150 Ω [11]
F = 10 kΩ ([14] , [16])

EPM-1 : Measuring range 0 dBm ± 0.2 dBm

8.4.1. Balanced inputs 150 Ω, 124 Ω

Calibration of EPM-1 :

Connect TKSE-150 to EPM-1 calibrator output Bu 303.

Connect probe head TKS-10 via Adaptor TKSA-150

Connect TKSA to TKSE. Set S 303 to 0 dB/R_i = 0 Ω.

Adjust meter to 0 dBm using pot P 202.

Measurement : (150 Ω input)

Connect probehead TKS-10 via adaptor TKSA-150 directly (without interconnection cable) in parallel with the balanced input (150 Ω) of the SPM-12 [2] . Adjust generator level to read 0 dBm on EPM-1. Calibrate SPM-12, switch to "measure" and read SPM-12.

Repeat measurement at 6kHz, 2 MHz, and 4.5 MHz (5 MHz).

Permissible error limits (e)

Series	Freq. range	Error limit
C...F	6 kHz...2 MHz	± 0.3 dB
	2 MHz...4.5 MHz	-0.3 dB/+0.4 dB
G...	6 kHz...2 MHz	± 0.3 dB
	2 MHz...5 MHz	± 0.4 dB

Table 8-3 Error limits of level indication

Measurement of 124 Ω input:

Tune SPM-12 to f = 10 kHz, press "124 Ω" key. Set send level to read - 0.826 dBm on EPM-1 (set EPM-1 to range - 0.8 dBm ± 0.2 dBm). Calibrate SPM-12, switch to "measure" and read indicator.

Repeat measurement at 6 kHz, 2 MHz and 4.5 MHz (5 MHz).

Limits of error (e) are as per the following table

Series	Freq. range	Error limit
C...F	6 kHz...4.5 MHz	± 0.3 dB
G	6 kHz...5 MHz	± 0.3 dB

Table 8-4 Error limits of level indication

8.4.2. Balanced input 600 Ω

Calibration of EPM-1

Connect TKSE-600 to the calibrator output (Bu 303) of EPM-1. Connect probe head TKS-10 via TKSA-600 to the calibration adaptor TKSE-600. Set calibrator level to 0 dB/75 Ω and adjust meter to 0 dB using calibration pot P 202.

Equipment setting :

PS-12 Impedance 150 Ω (11)
f = 10 kHz (14 , 16)
Use 150 Ω output (13)

SPM-12 Use 600 Ω input 3 key 7 depressed

Measurement :

Connect TKS-10 via adapter TKSA-600 directly, i.e. without interconnection cables, parallel to the balanced 600 Ω input 3 of the SPM-12. Adjust send level to read 0 dBm on EPM-1 meter.

Calibrate SPM-12, switch to "measure" and read indicator.

Repeat measurement at f = 200 Hz and f = 20 kHz.

Error limit (e) of level indication in the frequency range 200 Hz...20 kHz : ± 0.3 dB

8.5. Attenuator errors

The error limits of the attenuator are measured at the factory using dedicated test equipment. A check using normal commercial equipment is possible though only with limitations due to the required high accuracy. However, actual faults in the attenuator circuit will result in greater errors which may then be discovered by less accurate means.

Required equipment :

1 Level Generator 10 kHz, e.g. PS-12	W&G
1 Calibrated attenuator, 75 Ω, e.g. 3 D 120	Siemens

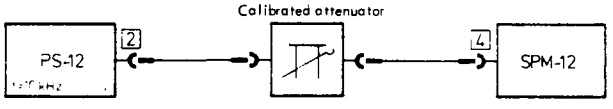


Fig.8-7 Test setup

Equipment setting :

PS-12	Impedance : 75 Ω (11)
	Level : 0 dB (5, 6, 7)
	Frequency : 10 kHz (14, 16)
Attenuator	Set to 0 dB attenuation
SPM-12	Level range 0 dB, expanded scale 13, 14 to 0
	Measuring mode wideband or selective (bandwidth 500 Hz, 19)

Measurement :

Set send level to read 0 dB on SPM-12. Increase both the attenuation of the attenuator and the sensitivity of the SPM-12 in steps of 10 dB and note the deviation of the SPM-12 indicating meter.

The permissible error is calculated from the inaccuracy of the attenuator plus the error limits of the test object.

Error limit (e) of the SPM-12 attenuator is ± 0, 1 dB

In "low noise" mode of measurement, the stray coupling between generator and receiver may impair the measurement in the more sensitive ranges. When measuring these, reduce both the generator level and the attenuator setting by a similar amount, e.g. 40 dB.

8.6. Inaccuracies of the meter scales

Required test equipment and test setup as per section 8.5.

Equipment setting :

PS-12	frequency : 10 kHz ([14], [16])
	level : - 8 dB/dBm ([5], [6], [7])
	impedance : 75 Ω ([11])
Attenuator	- 2 dB attenuation
SPM-12	wideband mode ([19])
	range : - 10 dB/dBm ([14])
	impedance : 75 Ω ([5])

8.6.1. Inaccuracy of the non-expanded meter scale measurement

Set SPM-12 to unexpanded scale, [13] -20...+ 2 dB.

Adjust generator level until SPM-12 meter is at "0" mark. Set attenuator to 0 dB, 1 dB, 3 dB, 5 dB etc. to 20 dB and read meter.

Error limit (e) of the scale division

1.5% of f.s.d. $\hat{=}$ 0.9 mm length of scale arc

8.6.2. Inaccuracy of the expanded meter scale

Switch SPM-12 to "expanded scale", scale expander [13] to "0". Attenuator to 0 dB. Adjust send level to achieve SPM-12 0 dB(dBm) indication. Switch attenuator to 0.1 dB, 0.2 dB etc. to 2.0 dB. Observe meter indication and note maximum positive and negative deviation (A).

Set send level to - 8 dB(dBm), attenuator to 2 dB, scale expander [13] of SPM-12 to "0". Set send level until SPM-12 meter reads "0". Now increase attenuation of the attenuator in 2 dB steps and read meter, switching the scale expander in 2 dB steps. This measures the error of the scale expander (B).

Calculate the maximum positive and negative deviation from the values (A) and (B).

Limit of the scale division error inclusive error of the scale expander, at ambient temperature of 23°C : ± 0.07 dB

8.7. Selectivity

A generator signal of high spectral purity is required to test the selectivity. Non-harmonic spurious signals must be more than 70 dB below fundamental.

Required test equipment :

1 Generator, e.g. PS-12 W&G

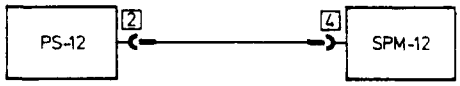


Fig. 8-8 Test setup

Equipment setting :

PS-12	arbitrary frequency
	Level : 0 dB(dBm) (5, 6, 7)
	Impedance : 75 Ω (11)
SPM-12	Measuring mode : selective, low noise (19)
	Range : 0 dB, non-expanded (13, 14)
	Impedance : 75 Ω (5)

Measurement :

Select bandwidth according to table 8-5. Tune receiver carefully to signal maximum and adjust send level until level meter reads 0 dB(dBm).

Detune PS-12 or SPM-12 by Δf. Increase receiver sensitivity by no more than 50 dB. Indicated attenuation should be as per table 8-5.

Bandwidth	Frequency change Δf	Attenuation
1.74 kHz	± 2 kHz	≧ 60 dB
500 Hz	± 2 kHz	≧ 60 dB
25 Hz	± 250 Hz ± 70 Hz	≧ 60 dB ≧ 25 dB

Table 8-5

8.8. Intrinsic distortion

Required test equipment:

1 Level Generator, with 2nd and 3rd harmonic distortion better than 50 dB

e.g. PS-12 W&G

1 Low pass filter, Attenuation of 2 f_c and 3 $f_c \geqq 40$ dB

e.g. UF-1 W&G

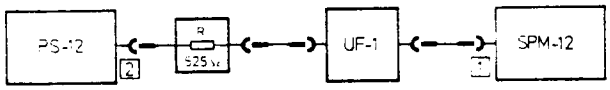


Fig.8-9 Test Setup

Equipment setting :

PS-12 frequency 16 kHz ([14], [16])
level appr. : - 7 dB ([5], [6], [7])
Impedance : 75 Ω ([11])

UF-1 Low pass
Basic attenuation 10 dB
cutoff frequency 16 kHz
source impedance : 600 Ω
output impedance 60 kΩ

SPM-12 Selective measurement 500 Hz bandwidth, low distortion [19]
Measuring range - 20 dB, non expanded ([13], [14])
Output impedance : 100 kΩ ([7])

Tune SPM-12 to 16 kHz fundamental frequency and adjust send level until SPM-12 reads - 20 dB.

Now tune SPM-12 to 32 kHz (k_2) and increase sensitivity by 50 dB (70 dB range).

Meter indication should be < - 90 dB.

Increase sensitivity by a further 10 dB (range - 80 dB). Meter should read < - 90 dB ($a_{k2} > 70$ dB).

Proceed similarly at f = 48 kHz (k_3).

Meter should read :

Sensitivity increase 50 dB level < -90 dB

- " - 60 dB level < -90 dB

This test demonstrates that the instrument is within the guaranteed intrinsic distortion specifications of a_{k2}, $a_{k3} \geqq 80$ dB after 50 dB sensitivity increase [1]. The SPM-12 may be switched temporarily to "low noise" to be able to tune to the harmonics (k_2 and k_3).

1) 10 dB overload (i.e. sensitivity increase of 60 dB in lieu of 50 dB) results in 2 x 10 dB increase of k_2 and k_3. If a 60 dB increase results in $a_k > 70$ dB, then $a_k > 80$ dB will correspond to a 50 dB sensitivity increase.

8.9. Reflection factor

Required Test equipment:

1 Return-loss Bridge, e.g. RFZ-5 W&G

1 Level Measuring Setup, e.g. PSM-5 W&G

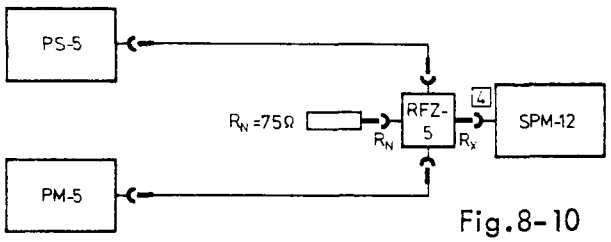


Fig.8-10 Test Setup

* Connect R_x-outlet of the RFZ-5 directly, i.e. without interconnecting cables, to Bu 202 (4 in BN 608/1) of SPM-12.

Instrument setting:

PS-5 : frequency 10 kHz
level 0 dB
impedance 75 Ω

PM-5 : frequency 10 kHz
impedance 75 Ω
low noise mode
bandwidth 3.5 kHz

RFZ-5 : Adjust bridge balance at 10 kHz and 4.5 MHz and calibrate in conjunction with PSM-5

SPM-12 : Measuring range 0 dB, Impedance 75 Ω
Instrument switched on

Measure return loss (a_r) at 10 kHz, 2 MHz and 4.5 MHz. Permissible return loss $a_r \geqq 40$ dB, corresponding to $r \leqq 0.01$

9. ALIGNMENT INSTRUCTIONS

9. Alignment Instructions

Re-alignment of the equipment should be attempted only if it is confirmed by measurement (chapter 8) that the instrument is not within the guaranteed specifications, i.e. that the limits ± (e + m) are being exceeded.

As mentioned in chapter 7, the equipment should be powered by an external source with current limiting (≦ 15 V, ≦ 5 A). Only if there is no other alternative, the instrument may be operated from the mains supply.

9.1. Alignment of frequency response

9.1.1. Impedance 75 Ω, selective

Required test equipment :

1 Level Generator, 200 Hz - 4.5 MHz, 0 dB, 75 Ω,

e.g. PS-12 W&G

1 attenuator or attenuator pads to obtain attenuation of 10, 20, 30, 40, 50 and 60 dB (75 Ω), whose frequency response must either be known or be much better than that of the permissible response of the SPM-12.

The attenuator is not required if the Level Generator is capable of supplying levels of 0, - 10, - 20...- 60 dB with known frequency response.

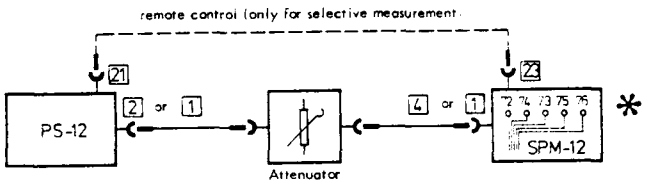


Fig.9-1 Test setup

*) Desolder cable loom (colors wt/gn, wt/bl, wt, wt/rd or gr) from points 72, 74, 73, 75, 76 of p.c. board 608-D . The wideband circuit may now be switched as required by grounding the free ends of the cable loom.

Equipment setting:

PS-12 Output 75 Ω coaxial, level 0 dB, frequency 10 kHz or remote control by SPM-12

SPM-12 Input 75 Ω coaxial, frequency 10 kHz (reference frequency), low noise selective mode, 0 dB/expanded scale.

Alignment

The alignment sequence is shown in table 9-1. Prior to alignment, adjust SPM-12 for 0-dB indication at reference frequency using calibration pot. [18] . Then tune across the frequency band and measure the frequency response at 200 Hz, 2 kHz, 200 kHz, 2 MHz and 4.5 MHz.

Switch [14] of SPM-12	Attenuation between Generator and SPM-12	Level at SPM-12 input	Wire to be grounded	Align with
+20 dB	20 dB	-20 dB	white	L 402
+20 dB	30 dB	-30 dB	white&white/blue	L 403
+20 dB	40 dB	-40 dB	white&white/red	L 404
0 dB	20 dB	-20 dB	-	C 305 (100 kHz) R 303 (4,5 MHz)
-20 dB	20 dB	-20 dB	white/grey	C 312 (100 kHz) P 301 (4,5 MHz)

Table 9-1 Frequency response alignment 75 Ω Input impedance, selective

Permissible frequency response after elimination of the test setup frequency response : ± 0.09 dB

Permissible frequency response after elimination of that of the test setup ± 0.065 dB

9.1.2. Impedance 75 Ω, wideband

Required test equipment and test setup as per 9.1.1. but without remote control of generator.

Equipment setting as per 9.1.1. but switch SPM-12 to "wideband".

Alignment : Proceed as per 9.1.1. but use table 9-2 and calibration pot [20] to set reference indication.

Switch [14] of SPM-12	Attenuation between Generator and SPM-12	Level at SPM-12 Input	Wire to be grounded	Align with
+20 dB	40 dB	-40 dB	white&white/red	L 502
+20 dB	50 dB	-50 dB	white&white/blue&grey	L 503 ↑ Repeat
+20 dB	60 dB	-60 dB	white&white/red&grey	L 503 ↓ alignment

Table 9-2 Frequency response alignment. Input impedance 75 Ω, wideband

9.1.3. Input impedance 124 Ω

Required test equipment

1 Level Generator, frequency range 200 Hz - 4.5 MHz,
0 dB, 124 Ω e.g. PS-12 W&G

1 calibrated interconnection cable, 124 Ω

Test setup

Connect 124 Ω output of generator with 124 Ω input [2] of SPM-12 by means of calibrated cable.

Equipment setting:

PS-12 : 0 dB, 124 Ω, frequency 10 kHz

SPM-12 : 0 dB expanded ([13] and [14] to 0)
124 Ω, wideband
Set meter indication to "0" mark using calibration pot [20] .

Alignment

Set generator to 4.5 MHz and align with C 218 SPM-12 for 0 dB indication. Then, check frequency response at 4 MHz, 3 MHz, 2 MHz, 1 MHz, 500 kHz, 100 kHz and 6 kHz.

Permissible frequency response after elimination of test equipment frequency response : ± 0.09 dB

9.1.4. Alignment of input low pass filter

Re-align input low pass filter if insufficient attenuation in the stopband range (above 8 MHz), or ripple above tolerance in the passband have become apparent.

Required test equipment

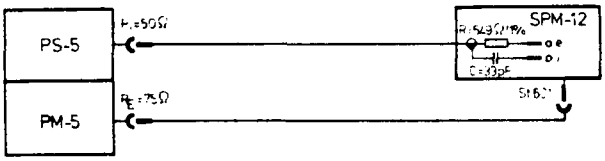
1 Level measuring setup 10 kHz to ≧ 20 MHz, generator output impedance 50 Ω, meter input impedance 75 Ω, e.g. PSM-5 W&G

1 Connection cable PS-5, other end open, length 75 cms

1 Connection cable PM-5, other end Subminax (length 75 cm)

1 Resistor 549 Ω 1%

1 Capacitor 33 pF



Remove jumper wire f-e from input lowpass (4)

Fig.9-2 Test setup

Equipment setting :

PS-5 : output impedance 50 Ω, level 0 dB
frequency 100 kHz

PM-5 : input impedance 75 Ω, level range - 20 dB bandwidth 500 Hz, low noise, calibrated.

PM-5 reading should be - 24 dB ± 1 dB

Pole alignment

Adjust for attenuation maximum at the following frequencies :

Frequency f (kHz)	Alignment element	PM-5 Indication	Pole attenuation
8000 ± 2	L 407	≦ -104 dB	a ≧ 80 dB
8500 ± 100	L 406	≦ -100 dB	a ≧ 76 dB
16500 ± 100	C 436	≦ -103 dB	a ≧ 79 dB
19500 ± 100	C 425	≦ -103 dB	a ≧ 79 dB

Repeat alignment. Then check attenuation at the following frequencies :

Frequency range (kHz)	PM-5 indication	Attenuation
8000 ± 10	≦ -100 dB	a ≧ 76 dB
Attenuation maximum at appr. 11 MHz	≦ - 79 dB	a ≧ 55 dB
Attenuation maximum at appr. 18 MHz	≦ -103 dB	a ≧ 79 dB

Alignment of passband range

PS-5 : Output impedance 50 Ω, approx. - 5 dB. Adjust level to read -30 dB on PM-5 at 100 kHz

PM-5 : Input impedance 75 Ω, - 30 dB lin, using scale expander

Check first that the attenuation at 4.5 kHz is 0.3 ± 0.1 dB relative to 100 kHz. Then adjust passband ripple to be 0.3 ± 0.1 dB, (after deduction of frequency response of test setup).

See also the frequency response in Fig. 9-3

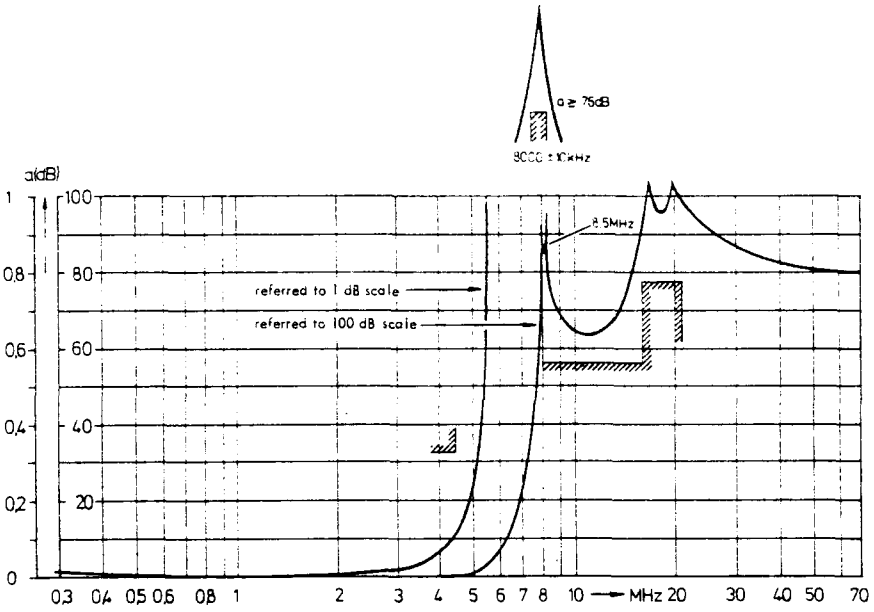


Fig. 9-3 Typical attenuation curve of the input low-pass filter

9.2. Adjustment of the SPM-12 indicator circuit

Adjust mechanical zero of the indicating meter after power was switched off.

9.2.1. Pre-alignment of rectifier

(necessary only after component replacement).

- Offset adjustment of IC 1504

Switch SPM-12 to "measure, wideband, 0 dB, non-expanded scale".

Connect circuit points x and y with resistor 39 Ω and ground y. Set meter pointer to -∞ using P 1509.

Remove 30 Ω resistor and the ground connection.

- Adjustment of diode bias and offset of IC 1501. Switch SPM-12 to "measure, wideband, 0 dB, non-expanded scale". Short b - c, d - w and z - aa. Open connection a - b. Rotate P 1502 (25 kΩ) from stop to stop and check that f.s.d. can be achieved. Then adjust P 1502 until meter pointer just moves a minute fraction off -∞ .

Remove short z - aa and adjust P 1501 (100 Ω) until meter pointer again just moves away from -∞.

Remove shorts b - c and d- w, reconnect a - b.

Alignment of L 1504

Switch SPM-12 to "Calibrate, selective, 0 dB, non-expanded scale". Rotate calibration potentiometer until meter reads approx.0 dB. Tune to maximum with L 1504.

9.2.2. Alignment of the indicator circuit

Required test equipment :

1 Level Generator, 75 Ω, 0 dB e.g. PS-12 W&G

1 Attenuator having 2, 4, 6, 8 dB attenuation, e.g. 3 D 120 Siemens

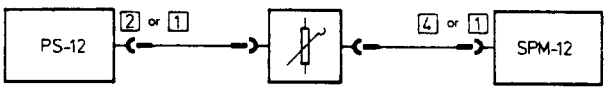


Fig.9-4 Test setup

Equipment setting :

Attenuator	0 dB
PS-12	Impedance 75 Ω, frequency 20 kHz,
	Level : 0 dB at SPM-12 input
SPM-12	Switch [14] to dB, impedance 75 Ω

Alignment:

- P 1503

Switch SPM-12 to "measure wideband" ([19]), switch [13] to "- 20...+ 2", calibration pot [20] approx. to centre.

Adjust approx. 0 dB indication using P 1503, tune to minimum with L 1504, then re-align P 1503 until meter reads precisely 0 dB.

- P 802

Switch SPM-12 to "measure selective, low noise, bandwidth 1.74 kHz" and tune to indicator maximum (20 kHz). Set calibration pot [18] to approximately centre and re-adjust for 0 dB indication using P 802.

- Rectifier linearity

Switch SPM-12 to "wideband" mode. Open a - b. Shut b - c, d - w and aa - z.

Adjust P 1502 until meter pointer is located between the - 10 and - 20 dB mark (i.e. not at the lower limit). Remove short aa - z and proceed similarly with P 1501 (take care of slow reaction). Remove short d - w and close a - b.

Using the calibrated attenuator, check that scale divisions correspond to 2-dB-increments.

Permissible deviation : 1% of f.s.d.

● 0 dB point when switching from normal to expanded scale.

Set 0 dB indication as a reference, using calibration potentiometer [20] . Then set attenuator to 2 dB and switch [13] to "0" (expanded). Correct deviation from - 2 dB mark using P 1507.

Set attenuator to 0 dB and align P 1508 to 0 dB meter indication. Repeat adjustment alternatingly until 0 dB and - 2 dB are indicated precisely.

● Divider for scale expander (15)

Decrease level through attenuator in 2-dB-increments, switch [13] correspondingly and adjust the relevant potentiometer (P 1510 to P 1513) until meter reads "0".

9.3. Alignment of 10 kHz calibration signal

The indicator circuit must be aligned prior to proceeding with this step.

Since the accuracy of the SPM-12 depends upon the accuracy of the calibration signal, sufficiently accurate measuring equipment is required to readjust the calibrator output.

Required test equipment and accessories:

1 Milliwatt Test Set EPM-1 W&G

1 Probehead TK-10 75 Ω W&G

T-junctions and connector adaptors as per connector system used

1 Level Generator, 10 kHz, 0 Ω output impedance e.g. PS-12 W&G

1 Differential Voltmeter to further expand the SPM-12 meter indication.

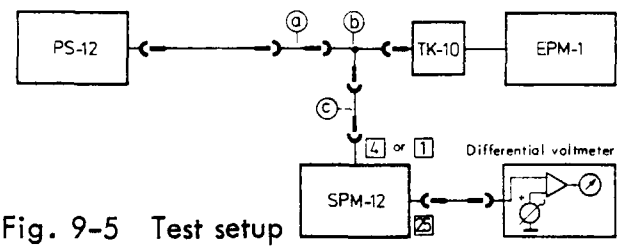


Fig. 9-5 Test setup

Connect b and c directly, i.e. without cable, to SPM-12.

Adaptors in fig.9-5 according to connector system:

(a) 1.6/10 (m) → 2.5/6 (f) Spinner 885700
→ 1.6/5.6 (f) Spinner 887900
→ BNC (f) Spinner

(b) Spinner BN 4851 2x1.6/10 (f)) 1.6/10 (m)

(c) 1.6/10 (f) → 2.5/6 (m) W & G S 393
→ 1.6/5.6 (m) W & G S 395
→ BNC (m) W & G S 391

Equipment setting :

EPM-1	Calibrate from 0 dB, R_i = 0 output
	Measuring range 0 dB ± 0.2 dB
PS-12	Voltage level calibration (dB)
	frequency : 10 kHz. Key [10] (R_i = 0) depressed.
	Adjust output level for 0 dB indication on EPM-1
SPM-12	Measure, selective, smallest bandwidth
	low noise, voltage level calibration (dB).
	Expanded scale, switch [13] to 0
	Measuring range [14] to 0 dB,
	Key [7] (high impedance) depressed.
	Tune to PS-12 signal

Differential voltmeter

0 dB indication of SPM-12 results in 4.000 V at output [26].
A level difference of 0.01 dB causes a voltage difference of 23 mV.

Adjustment P 201, V 201:

Set accurate 0 dB reference indication using potentiometer [18]. Use differential voltmeter to further expand scale. Then press "Cal" button and adjust level of calibration oscillator to also indicate precisely 0 dB. Check that Ü 201 (cal.osc. frequency) is accurately tuned to the centre of the passband range.

9.4. Adjustment of mixer I balance

Switch SPM-12 to "measure, selective/low noise bandwidth 1.74 kHz" Tune to 0.00 kHz. Set switches [14] to "- 10 dB" and [13] to "- 20 ...+ 2". SPM-12 meter should indicate ≦ - 30 dB. This corresponds to a residual carrier attenuation of ≧ 50 dB. If this is not achievable, the mixer balance must be readjusted using P 601 (5 kΩ) and C 632 (3...10 pF).

9.5. Return loss and input balance ratio

A re-alignment is normally not necessary unless input circuit components have been replaced.

For realignment, a Return loss or Signal Balance Ratio Measuring Setup (e.g. PS-12 + SPM-12 + RFZ-12 or SDZ-12) is required. The relevant alignment is carried out in such a way that best performance across the whole frequency range is achieved. It is adviseable to use sweep measuring methods.

Parameter	75 Ω reflexion	124 Ω Reflexion	124, 150 Ω balance
Component	C 202	C 209	C 211

See Instruction Manual of measuring equipment used, for information concerning equipment setup and measuring procedure.

9.6. Alignment of mains power supply/converter

Prior to alignment, terminate the converter circuit with a load substitute. (see section 7.)

9.6.1. Alignment of instruments of series C to E

- Remove short ag - ak.
- apply 11 V d.c. to "external battery" connector and check that appr. 13.5 V appear across points 72-81 and that switching pulses are present at point ak.
- Re-connect ag - ak and adjust 12 V at converter output using P 101.
- Increase 11 V supply to approx 70 V and measure base voltage of T 114 at pt. 96. Eliminate negative voltages by increasing R 118.

Caution : The supply voltage must not be increased further if the 12 V Converter output voltage begins to rise.

9.6.2. Alignment of instruments of series F

- Remove short a - b
- Apply 11 V d.c. to "external battery" connector.
  Set P 103 to maximum resistance.
- Set output voltage to 14 V doing P 101. If not achievable, readjust P 103
- Reconnect a - b and adjust for 12 V at output using P 104.
- Monitor both voltage at pt. 59 608 - AR1 via oscilloscope and input current via ammeter.

Increase input voltage from 11 V to 70 V. Input voltage must not be increased further if output voltage exceeds 12.5 V, or input current rises. Increase P 103. Repeat measurement. Adjust P 103 until voltage is in accordance with CRO-trace Fig.9-6 (pt.59 608-AR1 at input voltage 70 V)

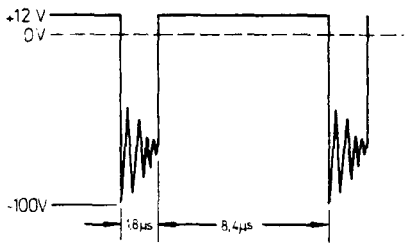


Fig.9-6 CRO-trace at point 59 608-AR1

Align for negative spikes of 100 V. Repeat alignment of P 101 and P 104.
Temporarily open short a - b and check that multivibrator IC 103/2.2 still oscillates.

10. DESCRIPTION OF FUNCTION

10. Description of functions

10.1. Description of block diagram SPM-12 BN 608

The input signal passes via the input circuit (2) to the input attenuator (3) and the pre-amplifier (4). The standard unit is fitted with coaxial 75 Ω input only, but options are available with additional balanced inputs (124 Ω, 150 Ω, 600 Ω). All inputs may be switched to "high impedance".

Input attenuator (3) and preamplifier (4) together produce between 20 dB gain and 40 dB attenuation switchable in increments of 10 dB, depending upon the setting of measuring range and mode of operation keys. The subsequent low pass filter (4) determines the upper measuring frequency limit (4.5 MHz) and provides sufficient I.F. and image frequency attenuation.

10.1.1. Mode : "measure, selective"

In selective mode, the input signal is applied to mixer 1 (6), where it is converted to the I.F. of 8 MHz. The carrier is supplied by tuning oscillator (19) (or by a signal at the remote tuning input (24)) via the calibrate/remote control switch (11) and the carrier limiter (6). 8 MHz I.F. selectivity is achieved with a crystal filter (7), whose out-of-band attenuation is improved by the preceeding low pass filter. The crystal band pass allows the lower sideband of the mixer product to pass, but supresses the 8.02 MHz image frequency of mixer 2.

The 8 MHz signal is then converted to 10 kHz by mixer 2 (8). The 8.01 MHz carrier is supplied by the temperature compensated crystal oscillator (9).

The bandwidth of the meter is determined by the 10 kHz B.P.F. in the 2nd I.F. stage, which has a resultant effective noise bandwidth of 1.74 kHz in conjunction with the 8 MHz crystal filter. The bandwidth of 500 Hz is achieved by switching an additional tuned circuit into operation. A 25 Hz bandwidth 10 kHz B.P.F. (18) is available as an option.

The following 10 kHz amplifier (13) may be switched in 10 dB increments from 0 to 80 dB gain. The necessary setting is determined by the subassembly "level switch" (16) depending upon the measuring range and the mode of operation.

The following 10 kHz amplifier (13) may be switched in 10 dB increments from 0 to 80 dB gain. The necessary setting is determined by the subassembly "level switch" (16) depending upon the measuring range and the mode of operation.

A level of - 20 dB at the output of the 10 kHz-amplifier (13) leads to a 0 dB indication at the meter. The final amplifier (14) is used to match the output of the 10 kHz amplifier to the signal selector (15). This is followed by a scale expander giving 2 dB f.s.d. when in use.
As an option, the demodulator (20) is available for SSB-detection.

10.1.2. "Measure, wideband" mode of operation

In this mode, the wideband amplifier (5) is used in lieu of the I.F. strip ((6) to (13)) The gain of the wideband amplifier may be switched between 0 dB and 20 dB to obtain a level of - 20 dB at the input of the final amplifier (14). Further signal amplification and detection is as per section 10.1.1.
The coded level switch (16) ensures correct distribution of gain or attenuation over the subassemblies (3), (4) and (5)

10.1.3. "Calibrate, selective" mode of operation

The calibration oscillator is located in the input circuit subass. (2). It is synchronized by the 8.01 MHz oscillator (9) via a frequency divider (10). The calibrator supplies a stable - 40 dB signal at a fixed frequency of 10 kHz.

When the calibration button is depressed, the input attenuator is disconnected from the signal input and switched to the calibrator output. Since a higher precision of the attenuation circuit can be realized more easily in the I.F. section than in the broadband input circuit, the setting of the input circuit is not altered during calibration and the necessary correction to obtain f.s.d. of the indicating meter is made in the I.F. circuit. The encoding circuit for this process is located in subassembly Level Switch (16). This way, the less precise attenuator setting of the broadband circuit is calibrated using the high precision I.F. circuit.

The instrument is tuned automatically to the calibrator frequency of 10 kHz by disconnecting Mixer I from the tuning oscillator and driving it with the same carrier frequency as mixer 2.

Meter calibration is obtained by a potentiometer at the detector output.

10.1.4. "Calibrate, wideband" mode of operation

It is not possible to interchange attenuators when calibrating in "wideband" mode as is the case in "selective" mode. Therefore, the sensitivity of the input attenuator pre-amplifier - wideband amplifier combination ③, ④, ⑤ is fixed to - 40 dB during calibration, resulting in 0 dB indication at - 40 dB input level. Accordingly, the attenuator error in "wideband" mode is larger than in "relative" mode.

10.2. Circuit description

10.2.1. Power supply/Converter ①

The level meter SPM-12 may be operated from mains power or else from an external d.c. source. The power supply circuit ① then generates the rail voltages of + 180 V, + 5 V, + 12 V and - 12 V.

The basic diagram is shown in Fig. 10-1

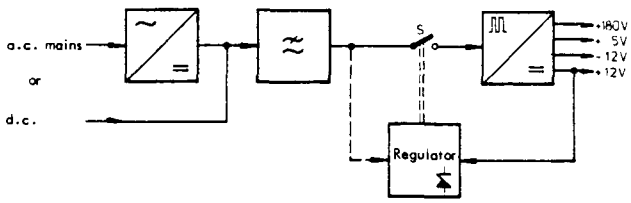


Fig. 10-1 Principle of power supply/converter

The d.c. voltage, or the rectified a.c. voltage is chopped by S. The resulting pulses are transformed into the required voltages and rectified. The regulator circuit monitors the rectified positive 12 V output voltage and influences the duty cycle of S in order to keep the output voltage constant.

The mains power supply consists of the mains filter 608-L, the voltage selector S 102, the transformer Ü 101 and the rectifier Gl 103-Gl 106.

The d.c. voltage across pt. 55 and pt 52 is in the order of 30 V at mains operation and between + 10.8 V and + 68 V at battery operation. The filters 608-AP and 608-AQ prevent the chopper frequency from entering the supply line (s).
The regulator circuit 608-AS drives transistor T 114 : During the switching cycle, energy from the supply source is stored in the primary inductance of the converter transformer Ü 102. During closure of T 114, the stored energy is transferred from

the transformer secondary into the load. The secondary winding ⑧ - ⑬ (180 V) is divided into three sections in order to maintain a low internal capacitance of the coil. The secondary voltage is rectified by Gl 122, Gl 123, Gl 128 to Gl 130 and filtered. The Zener diodes Gl 141 to 144 are limiting the output voltages.

During wideband operation or calibration points 2 and 18 are connected to ground. Rel 101 disconnects the 5 V supply of the counter circuit which is not in use in these modes. T 121 is then cutoff and T 122 energizes the decimal point of the read-out to obtain a visual indication of the instrument "on" state.

The regulator circuit (Series C...F). Upon switching on, the Darlington amplifier T 105, T 108 supplies a current into capacitor C 120 of the regulator. As soon as the Zener voltage of Gl 112 has been reached, the multivibrator 1 (T 101, T 102) commences oscillation. The square wave switches transistors T 103, T 104 (via Gl 113, Gl 114, R 109 or Gl 113, Gl 116 and R 110 respectively) and transistors T 106 and T 107. The power transistor T 114 is switched via T 106, R 118 and R 124. Transistor T 107 ensures precise cutoff of T 114. R 103 and R 104 of multivibrator I are chosen to obtain an "on" cycle of T 114 of as short a duration as practicable. In order to transfer the same amount of energy the "on" cycle of T 114 must be shorter the higher the input voltage is. Thus, R 103 is connected to the supply voltage, causing the duty cycle to vary with supply voltage variations.

The operational amplifier IC 101 toggles if the voltage at pt. 81 (608-AW) exceeds 13.5 V, connecting the supply voltage via Gl 138 and Gl 138 to multivibrator 2 (T 119, T 120), which then commences oscillation. Now, the actual regulator circuit takes over control of T 114. The regulator consists of T 117, T 118 and C 129. The diodes Gl 148 and Gl 134 keep the base voltage of T 117 at a constant 8.4 V. The 12 V d.c. being divided by R 161, P 101 and R 162 is connected to base of T 118. Upon reading 8.4 V, T 117 begins to draw current which is independent of the positive 12 V - d.c. The current flows into capacitor C 129. Then the base-emitter junction of T 116 is limiting the voltage across C 129-T 117. Table 10-1 shows how the switching pulses for T 114 are formed depending upon the voltage at pt.81. These pulses go alternatively to T 103 to switch T 114 and to T 109 and T 112, which turn off multivibrator I via T 102. Simultaneously with T 112, the

current source T 105, T 108 is switched off. Winding ②③ of transformer Ü 102 supplies now power to the regulator circuit 608 AS.

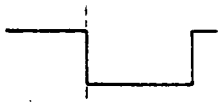
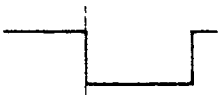
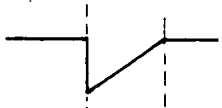
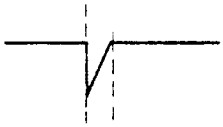
Voltage at pt.81 current through T 117	U_1 I_1	$U_2 > U_1$ $I_2 > I_1$
Multivibrator 2 (Collector T 119)		
Base of T 116		
Voltage across R 143 Switching pulses for T 114		

Table 10-1 Voltage regulation

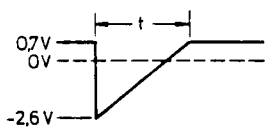
The pulse transformer Ü 103 provides isolation between the primary of the power supply (Battery) and the secondary (⊥). The transformer is driven via the AND circuit T 115, T 116 : only if the supply of multivibrator 2 is on, pulses are passed to Ü 103. To compensate for the pulse deformation caused by removal of the d.c. component, the differential amplifier T 111, T 113 with diode limiter Gl 126, Gl 127 is used. C 112 is a filter capacitor and C 113 is a bypass to R 140 to increase the amplitude. The C-R combination R 157, C 142 in the base circuit of the control amplifier T 118 compensates the phase shift caused by the input filter thus ensuring stability of the regulator circuit.

To start the regulating process as fast as possible, the capacitor C 142 is charged via Gl 136 from a low impedance source. The stabilized output voltages are available at pts. 76, 83, 82, 86, 79. The total load, distributed over 4 outputs,may amount to 7.5 W.

Regulator circuit (Series F)

Upon switching on, the Darlington amplifier T 105, T 108 drives a current into capacitor C 103, generating the supply voltage for the regulator primary. The relaxation oscillator T 102, IC 101/4.2 commences oscillation.

C 112 is charged via R 111 and P 101 and is discharged when IC 101/4.2 switches on, resulting in the following pulse shape:



The charge current, and thus the width "t" of the triangle, can be changed by P 101. The frequency is determined by R 106 and C 108 . IC 101/4.3 is switched on and T 103 is switched by triangular pulses. Thus, square pulses are generated at Collector T 103. IC 101/4.4 is driven by these via Gl 122, R 117, R 119 (R 118, R 120 respectively).

The square pulses being generated at the respective collectors switch the transistors T 104, and T 106. The power transistor T 114 is switched via T 104, P 103 and R 127, T 106 ensures precise cutoff of T 114.
The duty cycle of the oscillator (T 102, IC 101/4.2) is adjusted by P 101 for an "on" state of the power transistor T 114 of shortest possible duration, resulting in appr. 14.0 V at pt. 72 and 81.

Two measures avoid linear increase of the output voltage following an input voltage rise :

- The pulsewidth decreases since R 111 is connected to the input voltage (C 112 becomes charged faster)
- R 107 by passing Gl 112 result in variation of oscillator frequency with input voltage changes.

A voltage of 13.0 V at pt. 72, 81 switches
operating amplifier toggles and connects supply to oscillator 2 (Multivibrator IC 103/2.2) via Gl 169, Gl 167, Gl 168 and Gl 150.
The multivibrator commences oscillations. The circuit of the actual regulator consists of T 109, T 110, C 126.

The base of T 109 is permanently connected to a constant 8.4 V. As soon as the base of T 110 exceeds this value, T 110 allows current proportional to the input voltage to pass (pt.72-81), charging C 126 via T 111. At C 126/T 111, triangular pulses are generated, the width of which vary depending upon the output voltage. These cause a varying duty cycle of IC 103/2.1, and, via IC 102, IC 101/4.4, T 104 and T 106, of the power transistor T 114. Thus, the output voltage is regulated by variation of the duty cycle.

Footnote : The control loop may be opened for fault tracing purposes. (Connection ag - ak to series E or a - b from series F). To check the regulator, open ag - ak and separate pt. 97 from 72-81. Check pulse width variation at ak as a function of voltage changes at pt. 97.

As soon as the multivibrator IC 103/2.2 oscillates, the oscillator 1 (T 102, IC 101/4.2) is switched off via IC 103/2.1, IC 102, Gl 114, T 101, IC 101/4.1, Gl 170, IC 101/4.3 by connecting the base of IC 101/4.2 to ground and blocking IC 101/4.3. Simultaneously, the current source T 105, T 108 is turned off by IC 101/4.1.
The current for the regulator is now supplied by Ü 102 winding ① - ⑧ and Gl 110, Gl 111.

The optical isolator IC 102 is used to achieve isolation between the "primary" (-Battery) of the converter and the "secondary" (ground). IC 102 is driven by IC 103/2.1 (ANDcircuit): A signal is passed onto IC 102 only if the supply for multivibrator IC 103/2.2 is switched on.
To compensate the phase shift caused by the output filter and to ensure stability of the control loop, the C-R combination C 131, R 160 is fitted. T 111 and T 112 provide additional gain to give pt. 72 (sensor) lower impedance.

The regulated supply voltages are available at the points 76, 82, 83, 86, 79.
The maximum load, distributed of the four outputs, may amount to 7.5 W.

Converter starting circuit
The circuit on p.c. board 608-BL consists mainly of two Schmitt-trigger circuits (ST-1 and ST 2). ST-1 (T 123, T 124) is actuated when anode of Gl 108 is more positive than its cathode. This is the case when the unit is supplied from the mains:
$V_{mains} > {}^{B}Batt$
T 125 is cut off if $V_{Batt} > V_{mains}$ causing T 124 to conduct, and T 123 to be cut off.

When the mains is switched on, T 123 becomes conductive and feeds current into the "Converter off" line, until the base voltage has become more positive than the base of T 124, being permanently connected to + 10 V. The treshold of ST-1 is set by P 102 for a no-load potential of ≅30 V at electrolytic C 102.

The purpose of ST 2 (T 126, T 127) is to hold the converter off for 0.2 s after every supply connection (mains or battery). The 0.2 s delay are also present with any brief supply interruption, with the limitation that ST 2 is activated only if the supply exceeds 25 V and the interruption is of a certain minimum duration, i.e. T 126 is conducting for 200 ms feeding current into the "converter off" line.

Note : St-2 (T 126, T 127) has been deleted from series C incl. The starting circuit consists of only ST 1 (T 123, T 124) 608-BL

10.2.2. Input circuit (2)

The standard version (BN 608) has only one coaxial input, which can either be terminated in 75 Ω or switched to high impedance with S 201. The termination consists of R 201 ‖ R 203. L 201, C 201 and C 204 pre-limit the frequency range. Additionally, C 204 is used to adjust the return loss of the input.

The calibration signal generator is also located in the input subassembly. The circuit around T 201 generates a 10 kHz sinusoidal calibration signal from the 10 kHz pulse signal derived from frequency divider (10). During calibration, pulses are present at St 105 which drive T 201 periodically into saturation thus exciting the tuned circuit formed by C 206, C 207 and Ü 201. Once the resonant frequency of the tuned circuit corresponds to the pulse frequency, Collector T 201 carries a sine wave with 2nd- and 3rd order harmonic distortion of app. 30 dB. (Fig. 10-2)

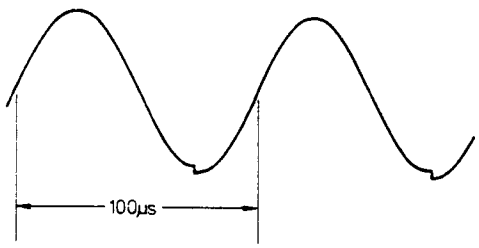


Fig. 10-2 Calibration signal at Collector T 201

The tuned circuit coil is tapped to generate signals for either voltage or power level calibration. Either signal is available as calibration level at St 207 after attenuation R 206, P 201, R 210.

The calibration levels are - 40 dB for voltage calibration (dB) and - 49.03 dB for power load calibration (dBm), at 75 Ω input impedance.

The signal detector supplies a voltage proportional to the magnitude of the signal. Since these are different in voltage (dB) or power level measurement (dBm) if $Z \neq 600\ \Omega$, a correction is made prior to the meter indication. (R 208, R 209).

The conversion from dB to dBm is carried out by short circuit plugs "a" to "i". The plugs are located at the edge connector in the input circuit.

The special version BN 608/1 is fitted with 4 inputs, which may be switched from terminated to high impedance.

The 75 Ω inputs (coax. and CF connectors) are connected in parallel. The input circuit is identical to that of the standard version. The 600 Ω - input circuit contains only the balancing transformer Ü 202, termination resistor R 204 and coupling capacitor C 207.

The 124/150 Ω input circuit contains additional compensating elements further to the switchable termination to level the return loss (Lowpass complement L 202, C 208, C 209), and to adjust the balance (C 206, C 210, C 211). To load the transformer secondary with as low a capacitance as possible, a high impedance, low distortion buffer amplifier having unity gain follows. At the output, correction of the frequency response is provided by C 208. Rel 202 is fitted to prevent signal distortion by the input diodes if the amplifier is inoperable but the signal source is still connected.

The input is selected with switch S 201. The calibration signal is generated identically to the method used in the coaxial input circuit. On account of the additional input resistances, the tuned circuit transformer Ü 201 is fitted with additional taps for dBm-correction; for the same reason, the dBm d.c. divider is extended.

10.2.3. Input attenuator (3)

The input circuit (2) is followed by the input attenuator (3). This is a capacitor-compensated resistive divider. The relay Rel 301 in front of the attenuator serves as a calibration/measurement changeover switch. The measuring signal is applied to Bu 302 and the calibration signal is applied to Bu 301 correspondingly.

The attenuation is switched with the relay Rel 302 and Rel 303 between 0,20 and 40 dB. The capacitive component of the attenuation may be adjusted for 20 dB with C 305 and for 40 dB with C 312. P 301 and R 315 are used to adjust the frequency response at the critical value of 40 dB. The attenuator load may be adjusted by P 302, which permits correction of any attenuation tolerance.

10.2.4. Pre-amplifier (4)

The pre-amplifier is an amplifier circuit with negative feedback. Thus T 401, T 403, T 405 and T 406 appear as if they were one single transistor having nearly ideal characteristics.

The input impedance is governed by the properties of the input transistor T 401 and attains values of 250 kΩ ‖ 10 pF. The diodes GI 401 and GI 402 protect the amplifier input from voltage transients. The gain within the feedback loop is reduced by R-C networks at the amplifier transistors, prior to the point where cut-off frequencies of the transistors and stray capacitances become influential.

Amplifier instability is thus safely avoided.

The gain of the preamplifier is approximately determined by the ratio of collector resistor to emitter resistor of T 406. Since the collector resistor of T 406, R 426 + R 427 is also the termination for the lowpass filter, the amplifier gain is switched in the T 406 emitter circuit. The gain can be switched in 3 steps : 0 dB, 10 dB or 20 dB. The maximum output level is - 20 dB. Inductances to compensate the amplifier frequency response at high frequencies are connected in series with the gain determining resistors. The R-C networks in parallel further compensate the frequency response.

A passive L-C lowpass filter follows which limits the receiver frequency range. It suppresses frequencies above 4.5 MHz and particularly at 8 MHz (1st I.F.) and the image frequency range from 16 to 20.5 MHz. The filter is formed by a 9th order CAUER lowpass whose attenuation pole location has been adapted to meet above requirement. L 406 and L 407 determine the location of the attenuation poles near 8 MHz, L 405 and L 408 the attenuation poles in the vicinity of the image frequency band.

10.2.5. Wideband amplifier (5)

The wideband amplifier is similar to the preamplifier except that the gain can be switched from unity to 20 dB.

10.2.6. Mixer 1 (6)

The mixer is a differential amplifier having a non-inverting and an inverting output, which are connected alternately by carrier cycle to the load resistance.

The carrier processing is done in limiter IC 603. The preceeding carrier lowpass filter suppresses all carrier harmonics, thus supplying a nearly pure sine wave, which is converted by clipping to a square wave having an on/off ratio of precise-

ly 1 : 1. The limiter consists mainly of the array IC 603, i.e. two r.f. cascaded differential amplifiers. For low d.c. power consumption the amplifiers are series connected.
In "wideband" mode, the supply voltage of the limiter is switched off to avoid coupling of the carrier upon the wideband signal path.
The voltage sources with T 602/4.3 and T 602/4.4 determine the bias.

Two push-pull square signals are available at the limiter output (IC 603 pt.11 and 12) which are supplied to the mixer.

The signal is connected to the differential amplifier input consisting of the two transistors of IC 601 (connections 2,3 and 8,9). The collectors of these transistors are in carrier rhythm connected via the transistor at pts. 10, 11 (and 4, 5 respectively) to the load resistor R 612 thus generating the mixer product.

The idle current in either half of the differential amplifiers is determined by either current source T 602/4.1. or T 602/4.2. This balance makes the gain independent from temperature variations and dependent only upon the value of R 615. The arrangement enforces additionally a balanced current flow, resulting in a small residual carrier.

To approximate the characteristics of an ideal mixer as far as possible, the balance of the d.c. currents can be adjusted with P 601 and the balance of the rise and fall time of the carrier square wave can be adjusted with C 632.

10.2.7. 8 MHz Bandpass filter (7)

This bandpass filter consists of an L-C L.P.F and two similar, cascaded lattice filters. The L.P.F improves the stopband attenuation of the filter combination.

At resonance, the bridge arms with the crystals have equal impedance, the bridge is balanced and there is no signal at the output.
The resonant frequency of the crystals differs from one another. Hence, the bridge is not in balance when the frequency approaches these points, thus forming the passband range.

10.2.8. Mixer 2 (8)

Mixer 1 and mixer 2 differ only in the matching to the surrounding circuit. The circuit description of mixer 1 (10.2.6.) is also valid for mixer 2.

10.2.9. 8.01 MHz Oscillator (9)

This oscillator generates a frequency of 8.01 MHz ± 10 Hz which is used as master frequency in the SPM-12. It is utilized directly or after frequency division.

The oscillator circuit is temperature compensated and voltage controlled to vary the oscillator frequency, followed by a gain - regulated R.F. amplifier, and a network to generate the temperature control voltage for the varactor diode. The p.c. board is prepared to take a module manufactured by either Valvo, Philips or ITT.

The output voltage of the oscillator is amplified by T 901 and goes via buffer T 902 to mixer 2 (8), to the cal/remote switch (11) and via pt.28 to the frequency divider (10).

10.2.10. Frequency divider 801 : 1 (10)

Frequency divider (10) derives a 10 kHz signal from the crystal-controlled 8.01 MHz signal, which is required for the calibrator (2) and for the frequency display (17). The divider group is made up of three stages dividing by 3 : 1 and 89 : 1. After the second divider, the 890 kHz for detector (15) is branched off. The first divider is assembled from individual components. The actual divider is a monostable with T 1004 and T 1007. The time constant of the divider is determined, in general terms, by R 1013, C 1010 and C 1009. T 1005 facilitates low impedance charge inversion of C 1010. The output of the 1st divider supplies a nearly symmetrical signal of 10 V p/p.

The second divider consists of two intergrated D-flip-flops and a NAND-gate. The circuit configuration forms a divider with timing as per fig. 10-3.

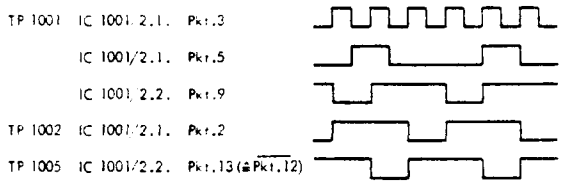


Fig. 10-3
Pulse diagram of 2nd divider 3: 1

The 3rd divider is a seven-stage binary counter IC 1003. The NAND-gate IC 1004/3.1 recognizes the state "HLHHLLL" (≙ 88) and permits the 89th pulse to reset the counter to zero. Thus, one pulse every 100 µs is produced at the output. T 1008 supplies H-level during the calibration cycle, only then permitting the 10 kHz pulse train to pass to the calibrator.

10.2.11. Calibration/remote change over switch (11)

The purpose of the switch is to supply the corresponding carrier to mixer 1 in either mode. During measurement, mixer 1 receives the carrier from the tuning oscillator (19) (Bu 1103). The signal of an external oscillator, however, must be used as a carrier if such a device is connected to Bu 1101. The internal oscillator and the frequency display are then switched off. During calibration, the 8.01 MHz signal is supplied to mixer 1.

Calibration change-over switch

During calibration, pt.5 is set to 0 V. This cuts off T 1109, T 1110, T 1108 and turns on T 1111, T 1112 and T 1113. In this state, the 8.01 MHz Oscillator is connected to mixer 1 via T 1113 and T 1112. T 1108 and T 1110 are cut off and attenuate the carrier at TP 1101 by approx.90 dB. In this mode, C 1109 and C 1110 with Gl 1101 and Gl 1102 are acting as filter elements. A similar situation occurs in the opposite mode "measurement," T 1111, T 1112 and T 1113 being cutoff and T 1108, T 1109 and T 1110 switched on.

The transistors T 1112 or T 1110 resp. amplify, resulting in approx. -10 dB carrier level at the output.

The remote control change-over switch circuit is somewhat simpler. Normally, T 1105 and T 1106 are switched on and the internal carrier is supplied via Bu 1103 to the calibration switch. If, however, an external oscillator is connected to Bu 1101 creating a d.c. path from the base of T 1101 to ground via R 1103, Bu 1101, R 1102, T 1101 will conduct and T 1104 and T 1103 switch on. T 1106 and T 1105 are thus cutoff and the carrier is supplied to the calibration switch from Bu 1101 via Ü 1101 and T 1103. Simultaneously T 1102 switches the 5 V supply off and T 1107 disables the internal tuning oscillator which is now not required.

10.2.12. 10kHz Bandpass filter (12)

1.74 kHz section

The bandpass filter with the inductances L 1201 to L 1208 (except L 1206) has an impedance of 1 kΩ. L 1201 is a transformer to match the 300 Ω input impedance to the 1 kΩ-impedance of the filter. L 1208 is tapped to match the termination of 3 kΩ to the filter output impedance.

500 Hz section

An additional tuned circuit L 1206/C 1207 narrows the passband range of the filter from the 1.8 kHz/3 dB points to approx. 500 Hz. The increased insertion loss thus caused is substituted by R 1204 and P 1201 in position "1.74 kHz". Relais 1201 is used to switch the bandwidths.

25 Hz section

25 Hz/3 dB bandwidth is achieved by a additional crystal filter (18). Pins 7, 8, 9 and 10 or p.c. board 608-2 are prepared for the additional filter. If this is not fitted, pins7 and 10 are shorted.

10.2.13. 10-kHz-amplifier (13)

The 10-kHz-amplifier increases the signal coming from the bandpass filters to a level of - 20 dB. For this purpose, the amplifier gain can be switched in 10 dB steps from unity to 80 dB. The setting depends upon the position of the level switch and the selected mode of operation.

The amplifier consists of three gain stages and an active bandpass filter, all connected in series. To keep the power consumption of the subassembly low, every two stages are connected in series to the 12 V-supply. Each amplifier stage has thus a supply voltage of 6 V. The bias for the amplifiers is then at + 3 V and +9V.

T 1301 ensures low impedance drive of the divider transformer Ü 1301. The transformer has a tap each at 15 dB gain and 15 dB attenuation, either one of which is connected via the MOSFET switch IC 1301 to the amplifier IC 1303.
Since the amplifier itself has a gain of 15 dB, the resulting gain will be either unity or 30 dB. The second amplifier stage is identical to the first one. The third

stage can be switched to unity, 10 dB or 20 dB gain. Two taps supply levels which are 10 dB higher or lower than the input level; the opamp is set to a gain of 12 dB. The total gain of the third stage is 20 dB, 10 dB or 0 dB and additionally 2 dB to compensate for the insertion loss of the I.F. noise filters. IC 1305 and IC 1307 form a 3rd order lowpass and highpass resembling jointly a bandpass filter which limits the effective noise bandwidth of the subassembly from over 100 kHz to approximately 15 kHz. The Zener diodes GI 1301 to 1303 protect the MOSFET switch, since 100 kΩ resistors cannot be used in this application.

10.2.14. Power Amplifier (14)

The power amplifier is a broadband amplifier connected to the 10 kHz amplifier (13) in "selective" mode or to the wideband amplifier (5) in "wideband" mode. In either case, the gain is 10 dB. The change-over wide/selective is achieved through two collector stages IC 1401/5.1 and IC 1401/5.2 which work with a common emitter resistor R 1404. The change-over is initiated by transistor IC 1401/5.3. If in conductive state, IC 1401/5.2 is cutoff and IC 1401/5.1 becomes a normal emitter follower for the 10 kHz signal. In cutoff state, the base of IC 1401/5.2 assumes a higher potential than the base of IC 1401/5.1 which is then blocked. In this case IC 1401/5.2 acts as emitter follower for the wideband signal. The state of IC 1401/5.3 determines the mode of operation.

The 10 dB poweramplifier consists of the two transistor stages IC 1401/5.4 and IC 1401/5.5. The first one is an emitter stage, whose gain is determined by the ratio of R 1415 to R 1416. The frequency response is straightened by C 1409 and adjusted by C 1408 together with the frequency response of the detector circuit. The signal is connected to the detector (15) via the emitter follower IC 1401/5.5. This output simultaneously drives the grounded-base stage T 1402 having a gain of 10 dB. The output, at the collector, has an impedance of 600 Ω (R 1423) and serves as a 10 kHz I.F. output.

10.2.15. Signal detector (15)

10.2.15.1 Detector circuit

The basic circuit of the signal detector is shown in Fig. 10-4. The best approxi-

mation to an r.m.s. detector for sinusoidal and noise signals is obtained with a resistance ratio of R_1/R_2 of 15.2.

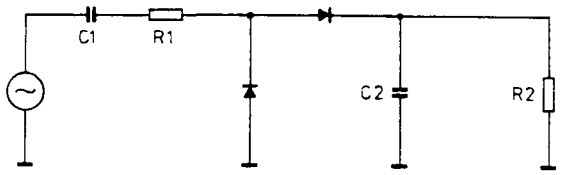


Fig. 10-4 Rectifier circuit

Error caused by departure from ideal diode characteristics is compensated with a control loop (Fig. 10-5). Thus the output

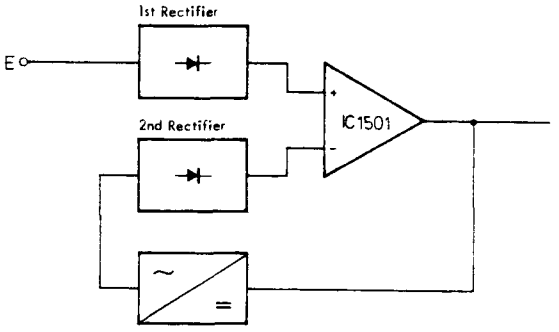


Fig. 10-5 Principle of rectifier control loop

voltage of IC 1501 is converted into an a.c. signal and then connected to a detector that is identical to the one used for the input signal. The operational amplifier aims at keeping both input voltages equal; hence, both a.c. and the output d.c. assume a quasi-r.m.s. value.

Both detectors are, in principle, connected as per Fig. 10-4. The diodes, all fitted in the same case, are assumed to be equal. Both diode pairs are biased with a current of 6 µA. The bias can be balanced by P 1501.

A further linearity improvement of the detector is achieved by adjustment of the offset by P 1502. The a.c. conversion is obtained through two CMOS-switches IC 1502, which alternately connect opamp-output IC 1501 and ground to the tuned circuit L 1504/C 1523. The switches are driven with 222.5 kHz which is derived from the 890 kHz signal from frequency divider (10) by division through IC 1503.

The detector circuit is designed for a lower cutoff frequency of 200 Hz; this however makes the time constant too long for sweep operation. A transistor switch (T 1504, T 1505) disconnects the capacitors C 1509, C 1513 in sweep mode, re-

sulting in a cutoff frequency of 10 kHz.

L 1501 to 1503, C 1520 to C 1522 form a low pass filter which prevents interference of the chopper with the indicator circuit.

The d.c. is first connected to the divider in input circuit subass. (2) for dB/dBm conversion, and then to the indicator circuit via the calibration potentiometers P 1602 and P 1603 and the changeover switch "selective/wideband".

10.2.15.2. Indicator circuit

The display amplifier drives both the indicating meter and the d.c. output. The gain depends upon the position of switch S 1501. In setting "non-expanded" the gain is approx. 2.3 times. In the remaining positions of switch S 1501, the 2 dB increments from 0 to - 2 dB...-8 to - 10 dB of the total range may be expanded to full scale. Thus, the amplifier gain is increased from 11.1 to 27.8 times depending upon the switch position whilst, at the same time, the current source T 1509 produces zero-offset. In position "0 dB expanded", the gain is adjusted by P 1508 and the zero-offset by P 1507. In the positions (- 2 to - 8 dB) expanded, the gain is adjusted by P 1510 to P 1513. The d.c. output is connected to the amplifier via R 1561 and the meter via R 1567 and R 1633.

During calibration, the display amplifier is switched by Rel 1501 to "0 dB expanded" independent from the setting of S 1501 and a capacitor C 1602 or C 1603 is brought into circuit in order to suppress the calibrator noise.

10.2.16. Level switch (16)

The level switch subassembly (16) consists of the level switch S 1601, the mode of operation keys S 1602 and the two p.c. boards [608-D] and [608-E].

10.2.16.1. P.C. board [608-D]

This circuit contains the encoding for the control of the broadband circuit portions (Input divider (3): pt. 72, 74, Preamplifier (4): pt.73, 75, wideband amplifier (5): pt.76) and the encoding to control the I.F. amplifier (pt.77 to 89). The mode of operation is selected by an H-level at the points 52,55 or 56. The code is as per

tables 10-2 to 10-5. In the mode "cal/wideband", a fixed setting is selected by connecting pt. (16) 51 to H-level and pt. (16) 52 to L-level.

10.2.16.2. P.C. board 608-E

This circuit contains the encoding to control the I.F. amplifier, and the key assembly for selection off operational mode and bandwidth.

The I.F. attenuator is changed during calibration in order to obtain 0 dB meter reading at - 40 dB calibrator level for every wideband setting.

The change-over "measure/calibrate-selective" is accomplished via the control leads coming from push button array S 1602 I c, interchanging transistor group T 1646, T 1648, T 1650, T 1652 with T 1647, T 1649, T 1651, T 1653.

The outputs (16) 9, 10, 11, 13, 14, 16 and 18 control the CMOS switches in the 10 kHz amplifier. The operational modes of the instrument are selected with the pushbutton bank. Electrical interlocks prevent operator error. The meter current for instance, is looped through the keys v/vi or vii (bandwidth) in conjunction with the calibrator buttons i or ix producing a meter deflection only if the selected calibrator button corresponds to the selected mode of operation.

10.2.17. Indicator circuit (17)

The circuit consists of the p.c. boards 608-U with gate and 4 : 1 counter to compensate the last-digit error, 608-T as control circuit and counter, and 608-Q and 608-S as display.

- PC board 608-U

H-level at pt. 41 permits the carrier from Bu 1701 via C 1701 and IC 1725/4.4 to pass onto 4 : 1 divider IC 1729.

The last digit error is caused by the fact that the number of pulses actually going through a gate depend upon the point in time in which the gate is opened. (see Fig. 10-6).

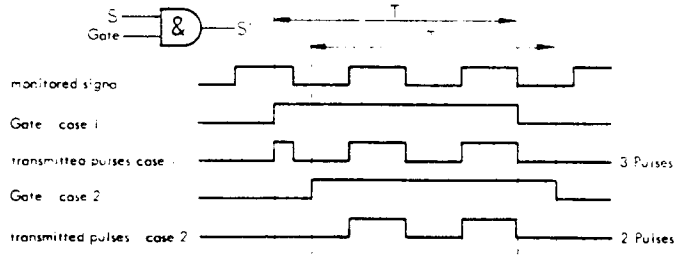


Fig. 10-6
Occurance of last digit error

S 1601 / Pt. (16)...	1	2	3	4	5	6	7	8	9	10 → 15	1→15 calibrate
72	L	L								L	L
74					L	L	L	L	L		L
73		L		L		L		L			
75							L		L		L
76								L	L		
77-44						L					
78-43					L						
81-40				L							
82-39			L								
83-38		L									
84-37	L									L	L
79-42											
80-41											
86-35											
85-36											
87-34											
90-31											
88-33											
89-32											
13	H	H	H	H	H	H	H	H	H	H	H	H
14											
16	H	H	H	H	H	H	H	H	H	H	H	H
18											
10	H	H	H	H	H	H	H	H	H	H	H	H
11											
9											

	Measure	Calibrate
(16) 51	L	H
(16) 52	H	L
(16) 53	L	L
(16) 55	L	L
(16) 56	L	L

T 1601 to T 1609 conduct in position "measure"

Table 10-2 Encoding for "wideband"

S 1601 / Pt. (16)...	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
72	L	L	L	L	L	L	L	L	L						
74												L	L	L	L
73									L		L		L		
75														L	L
76															
77-44													L		
78-43												L			
81-40											L				
82-39										L					
83-38									L						
84-37	L	L	L	L	L	L	L	L							
79-42															L
80-41								L	L	L	L	L	L	L	
86-35							L								
85-36						L									
87-34					L										
90-31				L											
88-33			L												
89-32		L													
measure 13	H	H	H												
measure 14				H	H	H	H	H	H	H	H	H	H	H	H
measure 16	H	H	H	H	H	H									
measure 18							H	H	H	H	H	H	H	H	H
measure 10	H			H			H								
measure 11			H			H									H
measure 9		H			H			H	H	H	H	H	H	H	
calibrate 13												H	H	H	H
calibrate 14	H	H	H	H	H	H	H	H	H	H	H				
calibrate 16									H	H	H	H	H	H	H
calibrate 18	H	H	H	H	H	H	H	H							
calibrate 10	H	H	H	H	H	H	H	H			H			H	H
calibrate 11									H			H			
calibrate 9										H			H		

(16)	52	L	T 1610 to T 1618, T 1620 conduct
(16)	53	H	T 1627 to T 1631 conduct
(16)	55	L	
(16)	56	L	

Table 10-3 Encoding for "selective, low distortion, dB"

S 1601 / Pt. (16)...	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
72	L	L	L	L	L	L	L	L							
74											L	L	L	L	L
73								L		L		L			
75													L	L	L
76															
77-44												L			
78-43											L				
81-40										L					
82-39									L						
83-38								L							
84-37	L	L	L	L	L	L	L								
79-42															L
80-41														L	
86-35							L	L	L	L	L	L	L		
85-36						L									
87-34					L										
90-31				L											
88-33			L												
89-32		L													
measure 13	H	H	H												
measure 14				H	H	H	H	H	H	H	H	H	H	H	H
measure 16	H	H	H	H	H	H									
measure 18							H	H	H	H	H	H	H	H	H
measure 10	H			H			H	H	H	H	H	H	H		
measure 11			H			H									H
measure 9		H			H									H	
calibrate 13											H	H	H	H	H
calibrate 14	H	H	H	H	H	H	H	H	H	H					
calibrate 16								H	H	H	H	H	H	H	H
calibrate 18	H	H	H	H	H	H	H								
calibrate 10	H	H	H	H	H	H	H			H			H	H	H
calibrate 11								H			H				
calibrate 9									H			H			

(16) 52 L T 1610 to 1615, T 1617 to T 1620,

(16) 53 L T 1632 to 1636 conduct

(16) 55 H

(16) 56 L

Table 10-4 Encoding for "selective, low distortion, dBm"

Pt. (16)... \ S 1601	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
72	L	L	L	L	L	L									
74									L	L	L	L	L	L	L
73								L		L		L			
75													L	L	L
76															
77-44										L					
78-43									L						
81-40								L							
82-39							L								
83-38						L									
84-37	L	L	L	L	L										
79-42															L
80-41														L	
86-35													L		
85-36												L			
87-34					L	L	L	L	L	L	L				
90-31				L											
88-33			L												
89-32		L													
measure 13	H	H	H												
measure 14				H	H	H	H	H	H	H	H	H	H	H	H
measure 16	H	H	H	H	H	H	H	H	H	H	H	H			
measure 18													H	H	H
measure 10	H			H									H		
measure 11			H									H			H
measure 9		H			H	H	H	H	H	H	H			H	
calibrate 13									H	H	H	H	H	H	H
calibrate 14	H	H	H	H	H	H	H	H							
calibrate 16						H	H	H	H	H	H	H	H	H	H
calibrate 18	H	H	H	H	H										
calibrate 10	H	H	H	H	H			H			H	H	H	H	H
calibrate 11						H			H						
calibrate 9							H			H					

(16) 52 L T 1610 to 1615, T 1619, T 1620

(16) 53 L T 1637 to 1643 conduct

(16) 55 L

(16) 56 H

Table 10-5 Encoding for "selective, low noise"

The purpose of the presettable 4 : 1 counter is to generate persistently a certain number of pulses for a certain frequency. The counter generates an output pulse upon transition from 3 (HH) to 0 (LL). A last-digit error is generated should the counter alternatively have assumed position 3 or 0 at the end of the gate time. IC 1728/2.1 and IC 1728/2.2 recognize, and the flip-flops 1727/4.1 and 1727/4.2 memorize this case. When one flip-flop is set, the other one is reset with delay (R 1727 + C 1703 or R 1728 + C 1704 respectively) causing IC 1726/4.2 to produce a pulse if 0 succeeded 3, similarly, IC 1726/4.4 produces a pulse if 3 succeeded 0. These pulses set flip-flop IC 1726/4.1 and IC 1726/4.3 which presets the counter to 3 for the next cycle in the first case (3→0) and to 1 in the second case (0→3). Fig. 10-7 shows an example.

Number of pulses at counter input	Succeeding states of the counter	number of pulses at the counter output
16	3 0 1 2 3 0 1 2 3 0 1 2 3 0 1 2 3	4
7	1 2 3 0 1 2 3 0	2 ↓ reducing frequency
8	3 0 1 2 3 0 1 2 3	2
8	1 2 3 0 1 2 3 0 1	2
7	1 2 3 0 1 2 3 0	2
7	3 0 1 2 3 0 1 2	2
	...	

Fig. 10-7 Example of presettable 4 : 1 counter operation

● P.C. Board 608-T

Two circuit groups are located on this board : control circuit and counterchain. The control circuit supplies the control signals "Gate" (pt.41) "store" (pt.46) and "set" (pt.45). The circuit consists of a number of cascaded 10 : 1 frequency dividers which are clocked by the 10 kHz signal.

Fig. 10-8 shows a measurement cycle with a gate time of 40 ms (100 Hz resolution). To obtain a gate time of 400 ms (10 Hz resolution), IC 1719/4.1 is cutoff and the gate-flip-flop IC 1724/2.1 is only reset (via IC 1719/4.2) if IC 1709/4.3 reads state "40" (IC 1715, IC 1711). The remaining process is identical to that of the 40 ms cycle.

S 1701 determines the gate time via IC 1724/2.2 by the signal "set". The correlation to the "set" pulse ensures the circuit is not switched during actual measurement.

The counter chain consists of five cascaded BCD counters, each one being connected to a latch and a decoder/driver. The state of the counter at the time the gate is closed is transferred into the latch upon command "store", which comes from the control circuit. Thereafter the counters are reset to zero. The counter representing the highest decimal (IC 1703) is a presettable circuit. If 40 ms gate time is selected, the counter is preset to 2 ≙ LLHL by the reset pulse (via the set impulse), for 400 ms gate time, the counter is preset to 0 ≙ LLLL.

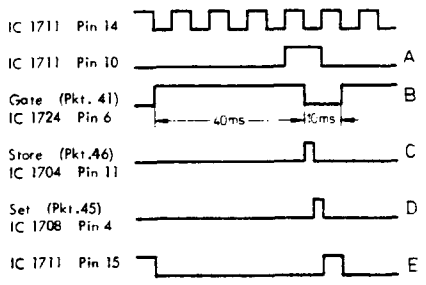


Fig. 10-8
Measuring cycle at gate time of 10 ms

A	precondition for gate FF to toggle
B	pulses are counted during gate time
C	counter state is latched, state of 4 : 1 counter is decoded
D	setting of both counters
E	reset of counter IC 1711 and IC 1715

10.2.18. 10 kHz/25 Hz Bandpass filters (18) (Option BN 608/50)

The filter is a crystal lattice circuit with a 3-dB-bandwidth of 25 Hz. The principle of such a filter is described under 10.2.

This filter requires 320 kΩ termination at either end. The amplifier impedance R 1805 is transformed to the required value with Ü 1801. Ü 1802 transforms the high filter impedance into the 3 kΩ required by the subsequent circuit. Adjustment of the attenuation poles around the centre frequency may be done by addition of a capacitor C 1811 to either one of the crystals (pins o-p or m-n). This way the lower inductance of one of the crystals is matched to that of the other one. The transformers Ü 1801 and Ü 1802 are tuned to 10 kHz. The tuning capacitors are

split to achieve temperature compensation. The amplifier T 1801 and T 1802 compensates the insertion loss of the filter and the loss resulting from feedback. The amplifier T 1803 and T 1804 is added to linearize the passive portion of the filter by feedback.

Rel 1801 connects input and output of the filter when the supply voltage is switched off, bypassing the filter circuit.

10.2.19. Tuning oscillator (19)

This is a L-C oscillator whose frequency can be tuned from 8 to 14.2 MHz.

The tuned circuit L 1 and C 1 is fed from T 1 with very high impedance via the grounded base stage T 8. Positive feed back is applied via T 2 to the emitter of T 1, resulting in very small loading of the tank circuit. The circuit is tuned by variation of C 1. The oscillator frequency passes from T 2 to T 5 which drives the buffer stages T 6 and T 7. The impedance of both outputs is 75 Ω, supplying a level of ≧ - 10 dB when terminated. Via the transistors T 3 and T 4, a pulse signal to drive the frequency display is generated at output St. 1. Fine tuning is done with a d.c. voltage at Gl 5.

The oscillator is disabled for remote control by cutting off T 1 via socket Bu 2.

10.2.20. Demodulator accessory (20)

The purpose of the demodulator is to make SSB modulation audible. Voice modulation can be demodulated with reasonable intelligibility. The upper or lower sideband and either 1 kHz or 2 kHz output frequency can be selected with switches S 2001 and S 2002. The PLL circuit IC 2002 contains a VCO and phase detector, governing a range from ≦ 8 to 12 kHz. The phase detector is supplied with two 1 kHz signals, one is derived via a 10 : 1 frequency divider (IC 2001) from the 10 kHz frequency already used in the SPM-12. The other one is derived by division (IC 2003) from the VCO output. The phase detector supplies a control voltage causing the oscillator frequency to assume a value which will result in a 1 kHz signal at the record input of the phase detector. The second frequency divider is switchable to divide by 8, 9, 11 or 12 in order to obtain 8, 9, 11 or 12 kHz at the output of the PLL circuit (TP 2002).

The carrier square wave at TP 2002 is processed in transistors T 2002 to T 2005 and

then supplied to current-fed differential amplifier/mixer. The signal voltage (10 kHz I.F.) is supplied from Bu 2002 via the buffer stage T 2004/4.4.

An ideally balanced mixer suppresses the carrier and the signal at the output allowing only the mixer products to occur.

The signal at TP 2003 is passed via an amplifier to a lowpass/highpass combination (IC 2005 and IC 2006). The lowpass suprresses all unwanted mixer products, and the high pass suppresses low-frequency signals at phase jitter measurement.

The resulting gain of the circuit is unity. Input and output impedance is 600 Ω.