October 1988

Z7220A
High-Performance Graphics Display Controller

Description

The Z7220A High-performance Graphics Display Controller (HGDC) is an intelligent microprocessor peripheral designed to be the heart of a high-performance raster-scan computer graphics and character display system. Positioned between the video display memory and the microprocessor bus, the HGDC performs the tasks needed to generate the raster display and manage the display memory. Processor software overhead is minimized by the HGDC's sophisticated instruction set, graphics figure drawing, and DMA transfer capabilities. The display memory supported by the HGDC can be configured in any number of formats and sizes up to 256K 16-bit words. The display can be zoomed and panned, while partitioned screen areas can be independently scrolled. With its light pen input and multiple controller capability, the HGDC is ideal for advanced computer graphics applications.

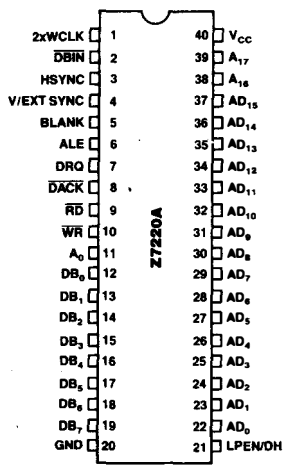
System Considerations

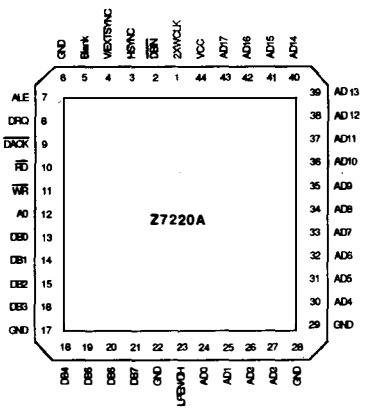
The HGDC is designed to work with a general purpose microprocessor to implement a high-performance computer graphics system. Through the division of labor established by the HGDC's design, each of the system components is used to the maximum extent through a six-level hierarchy of simultaneous tasks. At the lowest level, the HGDC generates the basic video raster timing, including sync and blanking signals. Partitioned areas on the screen and zooming are also accomplished at this level. At the next level, video display memory is modified during the figure drawing operations and data moves. Third, display memory addresses are calculated pixel by pixel as drawing progresses. Outside the HGDC at the next level, preliminary calculations are done to prepare drawing parameters. At the fifth level, the picture must be represented as a list of graphics figures drawable by the HGDC. Finally, this representation must be manipulated, stored, and communicated. By handling the first three levels, the HGDC takes care of the high-speed and repetitive tasks required to implement a graphics system.

Features

- ☐ Microprocessor Interface
  - DMA transfers
  - FIFO Command Buffering
- ☐ Display Memory Interface
  - Up to 256K words of 16 bits
  - Read-Modify-Write (RMW) Display Memory cycles as fast as 500ns
  - Dynamic RAM refresh cycles for nonaccessed memory
- ☐ Light Pen Input
- ☐ Drawing Hold Input
- ☐ External video synchronization mode
- ☐ Graphics Mode
  - Four megabit, bit-mapped display memory
- ☐ Character Mode
  - 8K character code and attributes display memory
- ☐ Mixed Graphics and Character Mode
  - 64K if all characters
  - 1 megapixel if all graphics
- ☐ Graphics Capabilities
  - Figure drawing of lines, arc/circles, rectangles, and graphics characters in 500ns per pixel
  - Display 1024-by-1024 pixels with 4 planes of color or grayscale
  - Two independently scrollable areas
- ☐ Character Capabilities
  - Auto cursor advance
  - Four independently scrollable areas
  - Programmable cursor height
  - Characters per row: up to 256
  - Character rows per screen: up to 100
- ☐ Video Display Format
  - Zoom magnification factors of 1 to 16
  - Panning
  - Command-settable video raster parameters
- ☐ Technology
  - Single +5V, NMOS, 40-pin DIP
- ☐ DMA Capability
  - Byte or word transfers
  - 4 clock periods per byte transferred
- ☐ On-chip pull-up resistor for VSYNC/EXT, HSYNC and $\overline{\text{DACK}}$, and a pull-down resistor for LPEN/DH

Pin Configuration





44-Pin Plastic Chip Carrier (PCC)
Pin Assignments

Pin Identification

Pin No.	Symbol	Direction	Function
1	2xWCLK	In	Clock Input
2	$\overline{DBIN}$	Out	Display Memory Read Input Flag
3	HSYNC	Out	Horizontal Video Sync Output
4	V/EXT SYNC	In/Out	Vertical Video Sync Output or External VSYNC Input
5	BLANK	Out	CRT Blanking Output
6	ALE ($\overline{RAS}$)	Out	Address Latch Enable Output
7	DRQ	Out	DMA Request Output
8	$\overline{DACK}$	In	DMA Acknowledge Input
9	$\overline{RD}$	In	Read Strobe Input for Microprocessor Interface
10	$\overline{WR}$	In	Write Strobe Input for Microprocessor Interface
11	A_0	In	Address Select Input for Microprocessor Interface
12–19	DB_0–DB_7	In/Out	Bidirectional Data Bus to Host Microprocessor
20	GND	—	Ground
21	LPEN/DH	In	Light Pen Detect Input/Drawing Hold Input
22–34	AD_0–AD_{12}	In/Out	Address and Data Lines to Display Memory
35–37	AD_{13}–AD_{15}	In/Out	Utilization Varies with Mode of Operation
38	A_{16}	Out	Utilization Varies with Mode of Operation
39	A_{17}	Out	Utilization Varies with Mode of Operation
40	V_{CC}	—	+5V ± 10% Power Supply

Character Mode Pin Utilization

Pin No.	Symbol	Direction	Function
35–37	AD_{13}–AD_{15}	Out	Line Counter Bits 0 to 2 Outputs
38	A_{16}	Out	Line Counter Bit 3 Output
39	A_{17}	Out	Cursor Output and Line Counter Bit 4

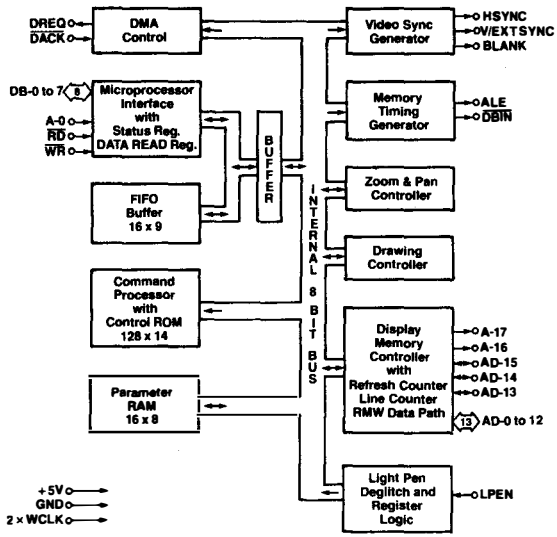
Mixed Mode Pin Utilization

Pin No.	Symbol	Direction	Function
35–37	AD_{13}–AD_{15}	In/Out	Address and Data Bits 13 to 15
38	A_{16}	Out	Attribute Blink and Clear Line Counter Output
39	A_{17}	Out	Cursor and Bit-map Area Flag Output

Graphics Mode Pin Utilization

Pin No.	Symbol	Direction	Function
35–37	AD_{13}–AD_{15}	In/Out	Address and Data Bits 13 to 15
38	A_{16}	Out	Address Bit 16 Output
39	A_{17}	Out	Address Bit 17 Output

Block Diagram



HGDC Components

Microprocessor Bus Interface

Control of the HGDC by the system microprocessor is achieved through an 8-bit bidirectional interface. The status register is readable at any time. Access to the FIFO buffer is coordinated through flags in the status register and operates independently of the various internal HGDC operations, due to the separate data bus connecting the interface and the FIFO buffer.

Command Processor

The contents of the FIFO are interpreted by the command processor. The command bytes are decoded, and the succeeding parameters are distributed to their proper destinations within the HGDC. The command processor yields to the bus interface when both access the FIFO simultaneously.

DMA Control

The DMA control circuitry in the HGDC coordinates transfers over the microprocessor interface when using an external DMA controller. The DMA Request and Acknowledge handshake lines directly interface with a DMA controller, so that display data can be moved between the microprocessor memory and the display memory.

Parameter RAM

The 16-byte RAM stores parameters that are used repetitively during the display and drawing processes. In character mode, this RAM holds four sets of partitioned display area parameters; in graphics mode, the drawing pattern and graphics character take the place of two of the sets of parameters.

Video Sync Generator

Based on the clock input, the sync logic generates the raster timing signals for almost any interlaced, non-interlaced, or "repeat field" interlaced video format. The generator is programmed during the idle period following a reset. In video sync slave mode, it coordinates timing between multiple HGDCs.

Memory Timing Generator

The memory timing circuitry provides two memory cycle types: a two-clock period refresh cycle and the read-modify-write (RMW) cycle which takes four clock periods. The memory control signals needed to drive the display memory devices are easily generated from the HGDC's ALE and DBIN outputs.

Zoom and Pan Controller

Based on the programmable zoom display factor and the display area entries in the parameter RAM, the zoom and pan controller determines when to advance to the next memory address for display refresh and when to go on to the next display area. A horizontal zoom is produced by slowing down the display refresh rate while maintaining the video sync rates. Vertical zoom is accomplished by repeatedly accessing each line a number of times equal to the horizontal repeat. Once the line count for a display area is exhausted, the controller accesses the starting address and line count of the next display area from the parameter RAM. The system microprocessor, by modifying a display area starting address, can pan in any direction, independently of the other display areas.

Drawing Controller

The drawing processor contains the logic necessary to calculate the addresses and positions of the pixels of the various graphics figures. Given a starting point and the appropriate drawing parameters, the drawing controller needs no further assistance to complete the figure drawing.

Display Memory Controller

The display memory controller's tasks are numerous. Its primary purpose is to multiplex the address and data information in and out of the display memory. It also contains the 16-bit logic unit used to modify the display memory contents during RMW cycles, the character mode line counter, and the refresh counter for dynamic RAMS. The memory controller apportions the video field time between the various types of cycles.

Light Pen Deglitcher/Drawing Hold

Only if two rising edges on the light pen input occur at the same point during successive video fields are the pulses accepted as a valid light pen detection. A status bit indicates to the system microprocessor that the light pen register contains a valid address. If this input is held high for a period greater than four 2xWCLK cycles, drawing execution is halted.

Programmer's View of HGDC

The HGDC occupies two addresses on the system microprocessor bus through which the HGDC's status register and FIFO are accessed. Commands and parameters are written into the HGDC's FIFO and are differentiated based on address bit A_0. The status register or the FIFO can be read as selected by the address line.

A0	READ	WRITE
0	Status Register	Parameter Into FIFO
1	FIFO Read	Command Into FIFO

HGDC Microprocessor Bus Interface Registers

Commands to the HGDC take the form of a command byte followed by a series of parameter bytes as needed for specifying the details of the command. The command processor decodes the commands, unpacks the parameters, loads them into the appropriate registers within the HGDC, and initiates the required operations.

The commands available in the HGDC can be organized into five categories as described in the following section.

HGDC Commands Summary

Video Control Commands

1. RESET1 — Resets the HGDC to its idle state. Resynchronizes video timing. Blanks the display.
2. RESET2 — Resets the HGDC to its idle state. Does not resynchronize video timing. Blanks the display.
3. RESET3 — Resets the HGDC to its idle state. Does not resynchronize video timing. Does not blank the display.
4. SYNC — Specifies the video display format.
5. VSYNC — Selects master or slave video synchronization mode.
6. CCHAR — Specifies the cursor and character row heights.

Display Control Commands

1. START — Ends Idle mode and unblanks the display.
2. BLANK1 — Controls the blanking and unblanking of the display, along with video resynchronization.
3. BLANK2 — Controls the blanking and unblanking of the display. Does not blank the display.
4. ZOOM — Specifies zoom factors for the display and graphics characters writing.
5. CURS — Sets the position of the cursor in display memory.
6. PRAM — Defines starting addresses and lengths of the display areas and specifies the eight bytes for the graphics character.
7. PITCH — Specifies the width of the X dimension of display memory.

Drawing Control Commands

1. WDAT — Writes data words or bytes into display memory.
2. MASK — Sets the mask register contents.
3. FIGS — Specifies the parameters for the drawing controller.
4. FIGD — Draws the figure as specified above.
5. GCHRD — Draws the graphics character into display memory.

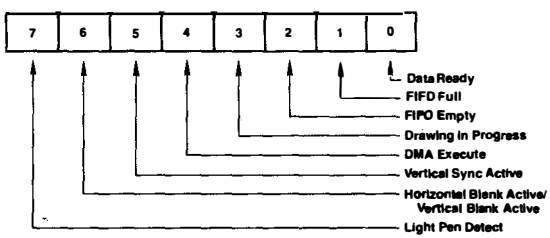
Data Read Commands

1. RDAT — Reads data words or bytes from display memory.
2. CURD — Reads the cursor position.
3. LPRD — Reads the light pen address.

DMA Control Commands

1. DMAR — Requests a DMA read transfer.
2. DMAW — Requests a DMA write transfer.

Status Register Flags



Status Register (SR)

SR-7: Light Pen Detect

When this bit is set to 1, the light pen address (LAD) register contains a deglitched value that the system microprocessor may read. This flag is reset after the 3-byte LAD is moved into the FIFO in response to the light pen read command.

SR-6: Horizontal Blank Active/Vertical Blank Active

A 1 value for this flag signifies that horizontal retrace blanking or vertical retrace blanking is currently underway dependent on the status of the VH bit in SYNC or the RESETx parameter 6.

SR-5: Vertical Sync

Vertical retrace sync occurs while this flag is a 1. The vertical sync flag coordinates display format modifying commands to the blanked interval surrounding vertical sync. This eliminates display disturbances.

SR-4: DMA Execute

This bit is a 1 during DMA data transfers.

SR-3: Drawing in Progress

While the HGDC is drawing a graphics figure, this status bit is a 1.

SR-2: FIFO Empty

This bit and the FIFO-full flag coordinate system microprocessor accesses with the HGDC FIFO. When it is 1, the Empty flag ensures that all the commands and parameters previously sent to the HGDC have been interpreted.

SR-1: FIFO Full

A 1 at this flag indicates a full FIFO in the HGDC. A 0 ensures that there is room for at least one byte. This flag needs to be checked before each write into the HGDC.

SR-0: Data Ready

When this flag is a 1, it indicates that a byte is available to be read by the system microprocessor. This bit must be tested before each read operation. It drops to a 0 while the data is transferred from the FIFO into the microprocessor interface data register.

FIFO Operation and Command Protocol

The first-in, first-out buffer (FIFO) in the HGDC handles the command dialogue with the system microprocessor. This flow of information uses a half-duplex technique, in which the single 16-location FIFO is used for both directions of data movement, one direction at a time. The FIFO's direction is controlled by the system microprocessor through the HGDC's command set. The host microprocessor coordinates these transfers by checking the appropriate status register bits.

The command protocol used by the HGDC requires differentiation of the first byte of a command sequence from the succeeding bytes. The first byte contains the operation code and the remaining bytes carry parameters. Writing into the HGDC causes the FIFO to store a flag value alongside the data byte to signify whether the byte was written into the command or the parameter address. The command processor in the HGDC tests this bit as it interprets the entries in the FIFO.

The receipt of a command byte by the command processor marks the end of any previous operation. The number of parameter bytes supplied with a command is cut short by the receipt of the next command byte. A read operation from the HGDC to the microprocessor can be terminated at any time by the next command.

The FIFO changes direction under the control of the system microprocessor. Commands written into the HGDC always put the FIFO into write mode if it was not in it already. If it was in read mode, any read data in the FIFO at the time of the turnaround is lost. Commands which require an HGDC response, such as RDAT, CURD and LPRD, put the FIFO into read mode after the command is interpreted by the HGDC's command processor. Any commands and parameters behind the read-evoking command are discarded when the FIFO direction is reversed.

Read-Modify-Write Cycle

Data transfers between the HGDC and the display memory are accomplished using a read-modify-write (RMW) memory cycle. The four-clock period timing of the RMW cycle is used to: 1) output the address, 2) read data from the memory, 3) modify the data, and 4) write the modified data back into the initially selected memory address. This type of memory cycle is used for all interactions with display memory including DMA transfers, except for the two-clock period display and RAM refresh cycles.

The operations performed during the modify portion of the RMW cycle merit additional explanation. The circuitry in the HGDC uses three main elements: the Pattern register, the Mask register, and the 16-bit Logic unit. The Pattern register holds the data pattern to be moved into memory. It is loaded by the WDAT parameters or, during drawing, from the parameter RAM. The Mask register contents determine which bits of the read data will be modified. Based on the contents of these registers, the Logic unit performs the selected operations of REPLACE, COMPLEMENT, SET, or CLEAR on the data read from display memory.

The Pattern register contents are ANDed with the Mask register contents to enable the actual modification of the memory read data, on a bit-by-bit basis. For graphics drawing, one bit at a time from the Pattern register is combined with the Mask. When ANDed with the bit set to a 1 in the Mask register, the proper single pixel is modified by the Logic unit. For the next pixel in the figure, the next bit in the Pattern register is selected and the Mask register bit is moved to identify the pixel's location within the word. The Execution word address pointer register, EAD, is also adjusted as required to address the word containing the next pixel.

In character mode, all of the bits in the Pattern register are used in parallel to form the respective bits of the modify data word. Since the bits of the character code word are used in parallel, unlike the one-bit-at-a-time graphics drawing process, this facility allows any or all of the bits in a memory word to be modified in one RMW memory cycle. The Mask register must be loaded with ones in the positions where modification is to be permitted.

The Mask register can be loaded in either of two ways. In graphics mode, the CURS command contains a 4-bit dAD field to specify the dot address. The command processor converts this parameter into the 1-of-16 format used in the Mask register for figure drawing. A full 16 bits can be loaded into the Mask register using the MASK command. In addition to the character mode use mentioned above, the 16-bit MASK load is convenient in graphics mode when all of the pixels of a word are to be set to the same value.

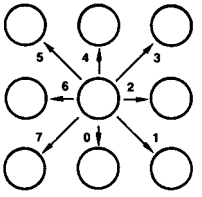
The Logic unit combines the data read from display memory, the Pattern register, and the Mask register to generate the data to be written back into display memory. Any one of four operations can be selected: REPLACE, COMPLEMENT, CLEAR or SET. In each case, if the respective Mask bit is 0, that particular bit of the read data is returned to memory unmodified. If the Mask bit is 1, the modification is enabled. With the REPLACE operation, the Pattern register data simply takes the place of the read data for modification enabled bits. For the other three operations, a 0 in the modify data allows the read data bit to be returned to memory. A 1 value causes the specified operation to be performed in the bit positions with set Mask bits.

Figure Drawing

The HGDC draws graphics figures at the rate of one pixel per read-modify-write (RMW) display memory cycle. These cycles take four clock periods to complete. At a clock frequency of 8MHz, this is equal to 500ns. During the RMW cycle the HGDC simultaneously calculates the address and position of the next pixel to be drawn.

The graphics figure drawing process depends on the display memory addressing structure. Groups of 16 horizontally adjacent pixels form the 16-bit words which are handled by the HGDC. Display memory is organized as a linearly addressed space of these words. Addressing of individual pixels is handled by the HGDC's internal RMW logic.

During the drawing process, the HGDC finds the next pixel of the figure which is one of the eight nearest neighbors of the last pixel drawn. The HGDC assigns each of these eight directions a number from 0 to 7, starting with straight down and proceeding counterclockwise.



Drawing Directions

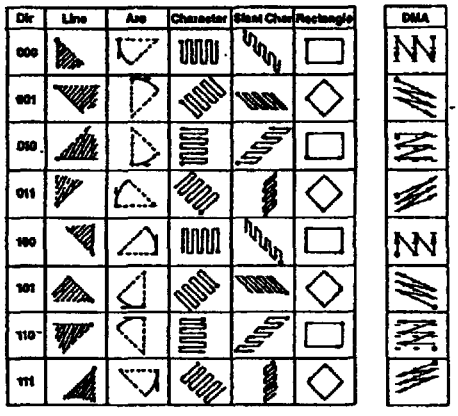
Figure drawing requires the proper manipulation of the address and the pixel bit position according to the drawing direction to determine the next pixel of the figure. To move to the word above or below the current one, it is necessary to subtract or add the number of words per line in display memory. This parameter is called the pitch. To move to the word to either side, the Execute word address cursor, EAD, must be incremented or decremented as the dot address pointer bit reaches the LSB or the MSB of the Mask register. To move to a pixel within the same word, it is necessary to rotate the dot address pointer register to the right or left. The table below summarizes these operations for each direction.

Dir	Operations to Address the Next Pixel
000	EAD – P→EAD
001	EAD – P→EAD dAD (MSB) = 1:EAD – 1→EAD dAD→LR
010	dAD (MSB) = 1:EAD – 1→EAD dAD→LR
011	EAD – P→EAD dAD (MSB) = 1:EAD – 1→EAD dAD→LR
100	EAD – P→EAD
101	EAD – P→EAD dAD (LSB) = 1:EAD – 1→EAD dAD→RR
110	dAD (LSB) = 1:EAD – 1→EAD dAD→RR
111	EAD – P→EAD dAD (LSB) = 1:EAD – 1→EAD dAD→RR

Note: P = Pitch, LR = Left Rotate, RR = Right Rotate, EAD = Execute Word Address, and dAD = Dot Address stored in the Mask register.

Whole word drawing is useful for filling areas in memory with a single value. By setting the Mask register to all 1s with the MASK command, both the LSB and MSB of the dAD will always be 1, so that the EAD value will be incremented or decremented for each cycle regardless of direction. One RMW cycle will be able to affect all 16 bits of the word for any drawing type. One bit in the Pattern register is used per RMW cycle to write all the bits of the word to the same value. The next Pattern bit is used for the word, etc.

For the various figures, the effect of the initial direction upon the resulting drawing is shown below:



Note that during line drawing, the angle of the line may be anywhere within the shaded octant defined by the DIR value. Arc drawing starts in the direction initially specified by the DIR value and veers into an arc as drawing proceeds. An arc may be up to 45° in length. DMA transfers are done on word boundaries only, and follow the arrows indicated in the table to find successive word addresses. The slanted paths for DMA transfers indicate the HGDC changing both the X and Y components of the word address when moving to the next word. It does not follow a 45° diagonal path by pixels.

Drawing Parameters

In preparation for graphics figure drawing, the HGDC's Drawing processor needs the figure type, direction and drawing parameters, the starting pixel address, and the pattern from the microprocessor. Once these are in place within the HGDC, the Figure Draw command, FIGD, initiates the drawing operation. From that point on, the system microprocessor is not involved in the drawing process. The HGDC Drawing controller coordinates the RMW circuitry and address registers to draw the specified figure pixel by pixel.

The algorithms used by the processor for figure drawing are designed to optimize its drawing speed. To this end, the specific details about the figure to be drawn are reduced by the microprocessor to a form conducive to high-speed address calculations within the HGDC. In this way the repetitive, pixel-by-pixel calculations can be done quickly, thereby minimizing the overall figure drawing time. The table below summarizes the parameters.

Drawing Type	D2	D	D2	D1	DM
Initial Value①	0	0	0	−1	−1
Line	|Δ|	2(|ΔC| − |Δ|)	2(|ΔC| − |Δ|)	2|ΔC|	–
Arc②	ratio ϕ	r−1	2(r−1)	−1	ratio θ ↓
Rectangle	B	A−1	B−1	−1	A−1
Area Fill	B−1	A	A	–	–
Graphic Character③	B−1	A	A	–	–
Read & Write Data	W−1	–	–	–	–
DMAW	D−1	C−1	–	–	–
DMAR	D−1	C−1	(C−1)/2†	–	–

Notes: All numbers are shown in base 10 for convenience. The HGDC accepts base 2 numbers (2s complement notation) where appropriate.

① Initial values for the various parameters needed at each drawing process cycle.

② Circles are drawn with 8 arcs, each of which span 45°, so that sin ϕ = 1/√2 and sin θ = 0.

③ Graphic characters are a special case of bit-map area filling in which B and A < 8. If A = 8 there is no need to load D and D2.

Symbol Definitions

−1 = All ONES value.

– = No parameter bytes sent to HGDC for this parameter.

Δl = The larger of Δx or Δy.

ΔD = The smaller of Δx or Δy.

r = Radius of curvature, in pixels.

ϕ = Angle from major axis to end of the arc, ϕ < 45°.

θ = Angle from major axis to start of the arc, θ < 45°.

↑ = Round up to the next higher integer.

↓ = Round down to the next lower integer.

A = Number of pixels in the initially specified direction.

B = Number of pixels in the direction at right angles to the initially specified direction.

W = Number of words to be accessed.

C = Number of bytes to be transferred in the initially specified direction. (Two bytes per word if word transfer mode is selected.)

D = Number of words to be accessed in the direction at right angles to the initially specified direction.

D0 = Drawing count parameter which is one less than the number of RMW cycles to be executed.

DM = Data masked from drawing during arc drawing.

† = Needed only for word mode.

Graphics Character Drawing

Graphics characters can be drawn into display memory pixel by pixel. The up to 8-by-8 character display is loaded into the HGDC's parameter RAM by the system microprocessor. Consequently, there are no limitations on the character set used. By varying the drawing parameters and drawing direction, numerous drawing options are available. In area fill applications, a character can be written into display memory as many times as desired without reloading the parameter RAM.

Once the parameter RAM has been loaded with up to eight graphics character bytes by the appropriate PRAM command, the GCHRD command can be used to draw the bytes into display memory starting at the cursor. The zoom magnification factor for writing, set by the ZOOM command, controls the size of the character written into the display memory in integer multiples of 1 through 16. The bit values in the PRAM are repeated horizontally and vertically the number of times specified by the zoom factor.

The movement of these PRAM bytes to the display memory is controlled by the parameters of the FIGS command.

Based on the specified height and width of the area to be drawn, the parameter RAM is scanned to fill the required area.

For an 8-by-8 graphics character, the first pixel drawn uses the LSB of RA-15, the second pixel uses bit 1 of RA-15, and so on, until the MSB of RA-15 is reached.

The HGDC jumps to the corresponding bit in RA-14 to continue the drawing. The progression then advances toward the LSB of RA-14. This snaking sequence is continued for the other 6 PRAM bytes. This progression matches the sequence of display memory addresses calculated by the drawing processor as shown above. If the area is narrower than 8 pixels wide, the snaking will advance to the next PRAM byte before the MSB is reached. If the area is less than 8 lines high, fewer bytes in the parameter RAM will be scanned. If the area is larger than 8 by 8, the HGDC will repeat the contents of the parameter RAM in two dimensions, as required to fill the area with the 8-by-8 mosaic. (Fractions of the 8-by-8 pattern will be used to fill areas which are not multiples of 8 by 8.)

Parameter RAM Contents: RAM Address RA-0 to RA-15

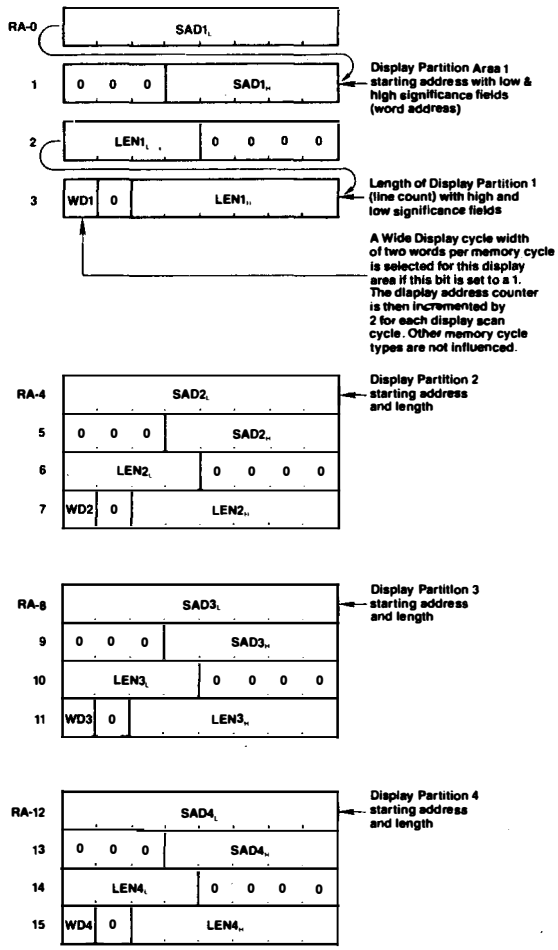
The parameters stored in the parameter RAM, PRAM, are available for the HGDC to refer to repeatedly during figure drawing and raster-scanning. In each mode of operation the values in the PRAM are interpreted by the HGDC in a predetermined fashion. The host microprocessor must load the appropriate parameters into the proper PRAM locations. PRAM loading command allows the host to write into any location of the PRAM and transfer as many bytes as desired. In this way any stored parameter byte or bytes may be changed without influencing the other bytes.

The PRAM stores two types of information. For specifying the details of the display area partitions, blocks of four bytes are used. The four parameters stored in each block include the starting address in display memory of each display area, and its length. In addition, there are two mode bits for each area which specify whether the area is a bit-mapped graphics area or a coded-character area, and whether a 16-bit or a 32-bit wide display cycle is to be used for that area.

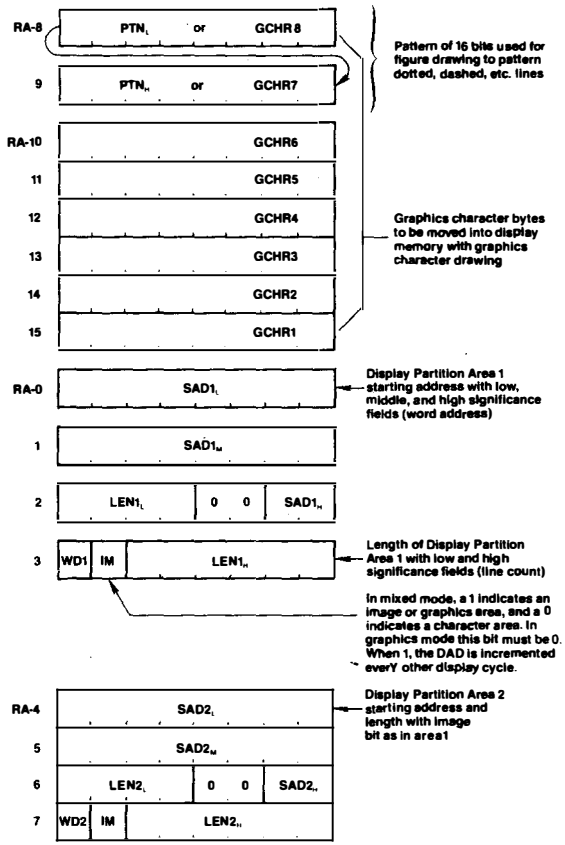
The other use for the PRAM contents is to supply the pattern for figure drawing when in a bit-mapped graphics area or mode. In these situations, PRAM bytes 8 through 16 are reserved for this patterning information. For line, arc, and rectangle drawing (linear figures) locations 8 and 9 are loaded into the Pattern register to allow the HGDC to draw dotted, dashed, etc. lines. For area filling and graphics bit-mapped character drawing locations 8 through 15 are referenced for the pattern or character to be drawn.

Details of the bit assignments are shown for the various modes of operation.

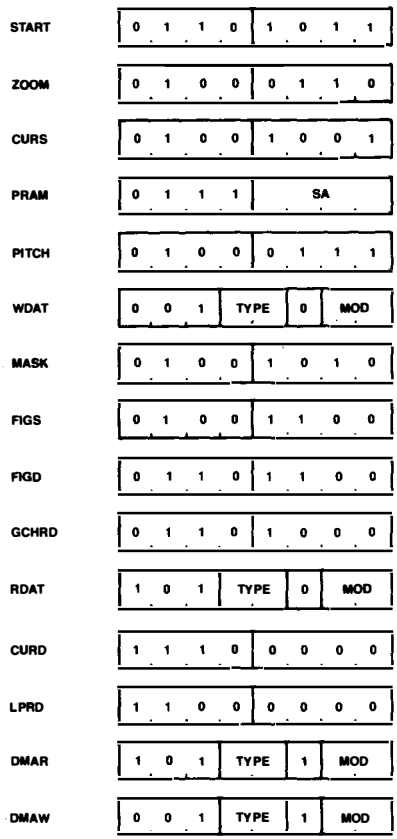
Character Mode



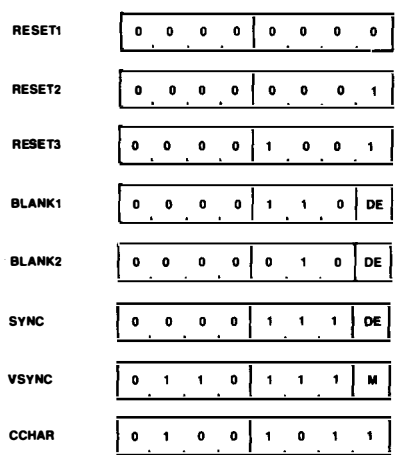
Graphics and Mixed Graphics and Character Modes



Command Bytes Summary

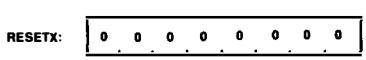


Command Bytes Summary



Video Control Commands

Reset

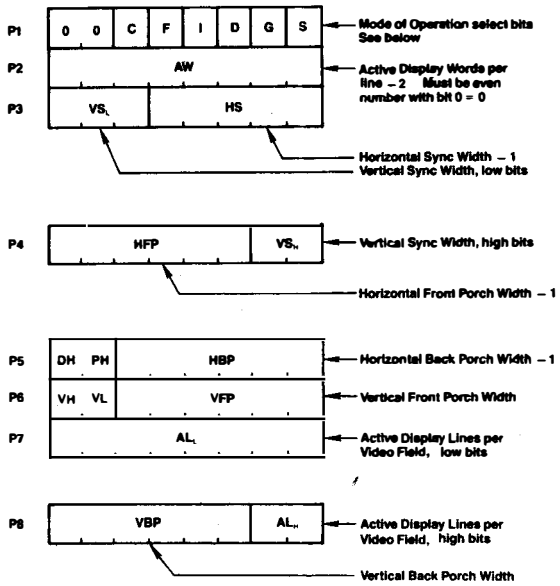


Blank the display, enter idle mode, and initialize within the HGDC:
- FIFO
- Command Processor
- Internal Counters

This command can be executed at any time and does not modify any of the parameters already loaded into the HGDC.

If followed by parameter bytes, this command also sets the sync generator parameters as described below. Idle mode is exited with the START command.

RESET1: Resync video timing in slave mode.
RESET2: Blank the display and do not resync.
RESET3: Unblank the display and do not resync.



In graphics mode, a word is a group of 16 pixels. In character mode, a word is one character code and its attributes, if any. The number of active words per line must be an even number from 2 to 256. An all-zero parameter value selects a count equal to 2^n where n = number of bits in the parameter field for vertical parameters. All horizontal widths are counted in display words. All vertical intervals are counted in lines.

If the Drawing Hold (DH) is set to one, pin 21 (LPEN/DH) is used as the drawing hold control pin. When the input to LPEN/DH is held high for over four 2 x WCLK clocks, the drawing address output is temporarily held and the display address is output.

The HGDC allows an even or odd number of lines per frame. Selection is via the VL flag, the seventh bit of the sixth parameter byte following a RESET or SYNC command. When VL is 0, an odd number of display lines is generated.

VL	Number of lines in interlaced mode
0	Odd, as in 7220
1	Even

When VH = 0, status operation is as in the 7220.

VH	Blank Status Bit Definition
0	Status register bit 6 indicates Horizontal Blank
1	Status register bit 6 indicates Vertical Blank

PH is the most significant bit (9) of the display pitch parameter. Use the PITCH command to set the lower eight bits.

SYNC Generator Period Constraints

Horizontal Back Porch Constraints

1. In general:
   HBP ≥ 3 Display Word Cycles (6 clock cycles).
2. If the Image bit or WD mode changes within one video field:
   HBP ≥ 5 Display Word Cycles (10 clock cycles).
3. If interlaced, mixed mode, or split screen is used:
   HBP ≥ 5 Display Word Cycles (10 clock cycles).

Horizontal Front Porch Constraints

1. In general:
   HFP ≥ 2 Display Word Cycles (4 clock cycles).
2. If the HGDC is used in the video sync Slave mode:
   HFP ≥ 4 Display Word Cycles (8 clock cycles).
3. If the Light Pen is used:
   HFP ≥ 6 Display Word Cycles (12 clock cycles).
4. If interlaced mode, DMA, or ZOOM is used:
   HFP ≥ 3 Display Word Cycles (6 clock cycles).

Horizontal SYNC Constraints

1. If Interlaced display mode is used:
   HS ≥ 5 Display Word Cycles (6 clock cycles).
2. If DRAM Refresh is enabled:
   HS ≥ 2 Display Word Cycles (4 clock cycles).

Modes of Operation Bits

C	G	Display Mode
0	0	Mixed Graphics & Character
0	1	Graphics Mode
1	0	Character Mode
1	1	Invalid

I	S	Video Framing
0	0	Non-interlaced
0	1	Invalid
1	0	Interlaced Repeat Field for Character Displays
1	1	Interlaced

Repeat Field Framing: 2 field sequence with 1/2 line offset between otherwise identical fields.

Interlaced Framing: 2 field sequence with 1/2 line offset. Each field displays alternate lines.

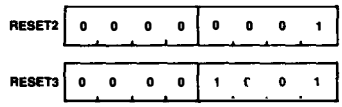
Non-interlaced Framing: 1 field brings all the information to the screen.

D	Dynamic RAM Refresh Cycles Enable
0	No Refresh — Static RAM
1	Refresh — Dynamic RAM

Dynamic RAM refresh is important when high display zoom factors or DMA are used in such a way that not all of the rows in the RAMs are regularly accessed during display raster generation and for otherwise inactive display memory.

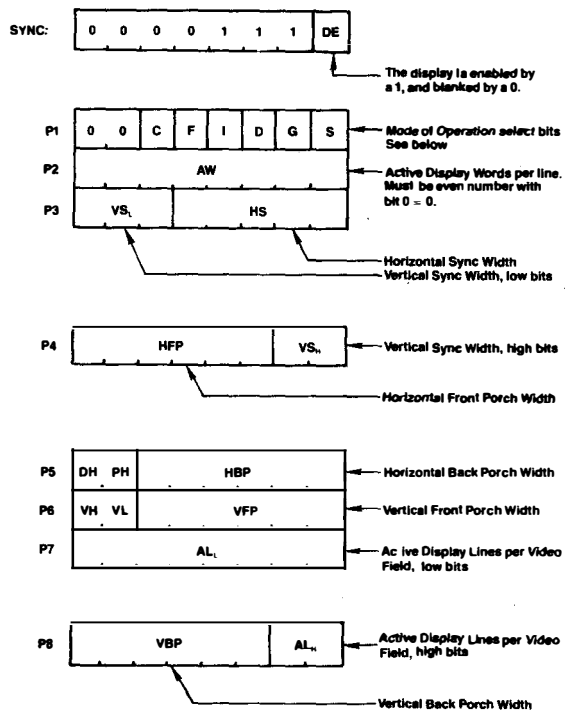
F	Drawing Time Window
0	Drawing during active display time and retrace blanking
1	Drawing only during retrace blanking

Access to display memory can be limited to retrace blanking intervals only, so that no disruptions of the image are seen on the screen.



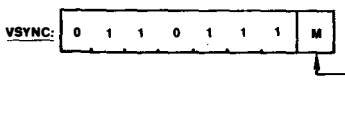
Both commands allow a reset while preventing reinitialization of the internal sync generator by an external sync source (slave mode).

SYNC Format Specify



This command also loads parameters into the sync generator. The various parameter fields and bits are identical to those at the RESET command. The HGDC is not reset nor does it enter idle mode.

Vertical Sync Mode



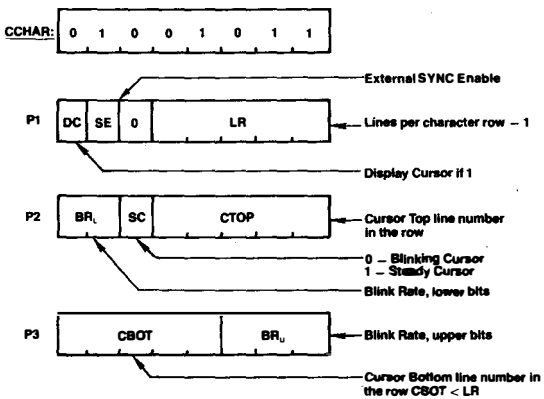
When using two or more HGDCs to contribute to one image, one HGDC is defined as the master sync generator, and the others operate as its slaves. The VSYNC pins of all HGDCs are connected together.

Slave Mode Operation

A few considerations should be observed when synchronizing two or more HGDCs to generate overlayed video via the V/EXT SYNC pin. As mentioned above, the Horizontal Front Porch (HFP) must be four or more display cycles wide. This is equivalent to eight or more clock cycles. This gives the slave HGDCs time to initialize their internal video sync generators to the proper point in the video field to match the incoming vertical sync pulse (VSYNC). This resetting of the generator occurs just after the end of the incoming VSYNC pulse, during the HFP interval. Enough time during HFP is required to allow the slave HGDC to complete the operation before the start of the HSYNC interval.

Once the HGDCs are initialized and set up as master and slaves, they must be given time to synchronize. It is a good idea to watch the VSYNC status bit of the master HGDC and wait until after one or more VSYNC pulses have been generated before the display process is started. The START command will begin the active display of data and will end the video synchronization process, so be sure there has been at least one VSYNC pulse generated to which the slaves can synchronize.

Cursor and Character Characteristics

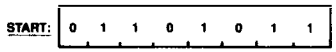


In graphics mode, LR should be set to 0. The blink rate parameter controls both the cursor and attribute blink rates. The cursor blink-on time = blink-off time = 2 x BR (video frames). The attribute blink rate is always one-half the cursor rate but with a 3/4-on-1/4-off duty cycle. **All three parameter bytes must be output for interlaced displays, regardless of mode.** For interlaced displays in graphics mode, the parameter BR_L = 3.

When SE = 0, the HGDC, in slave mode, detects the falling edge of EX. SYNC on the first frame. When SE = 1, the HGDC, in slave mode, detects the falling edge of EX. SYNC on every frame.

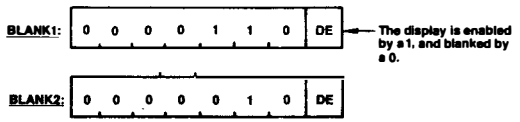
Display Control Commands

Start Display and End Idle Mode



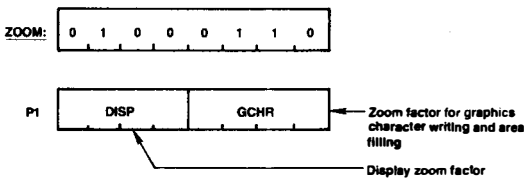
The START command generates the video signals as specified by the RESETX or SYNC command.

Display Blanking Control



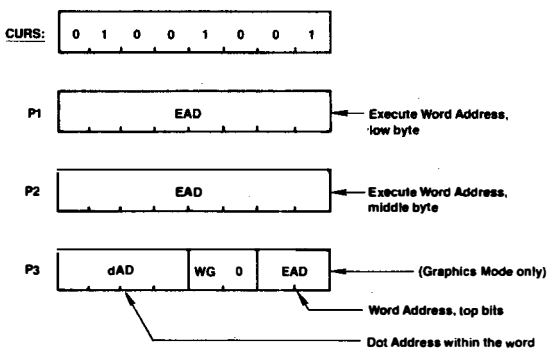
BLANK 2 does not cause the resyncing of an HGDC in slave mode. BLANK 1 does cause the resyncing of an HGDC in slave mode.

Zoom Factors Specify



Zoom magnification factors of 1 through 16 are available using codes 0 through 15, respectively.

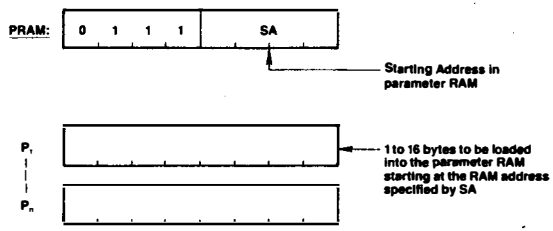
Cursor Position Specify



In character mode, the third parameter byte is not needed. The cursor is displayed for the word time in which the display scan address (DAD) equals the cursor address. In graphics mode, the cursor word address specifies the word containing the starting pixel of the drawing; the dot address value specifies the pixel within that word.

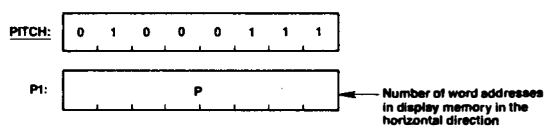
When the WG bit is set to one, any data following the WDAT command is written as is. When the WG bit is set to zero, the pattern written is determined by the least significant bit of each parameter byte following the WDAT command. This bit is expanded into 16 identical bits which form the pattern.

Parameter RAM Load



From the starting address SA, any number of bytes may be loaded into the parameter RAM at incrementing addresses, up to location 15. The sequence of parameter bytes is determined by the next command byte entered into the FIFO. The parameter RAM stores 16 bytes of information in predefined locations which differ for graphics and character modes. See the parameter RAM discussion for bit assignments.

Pitch Specification

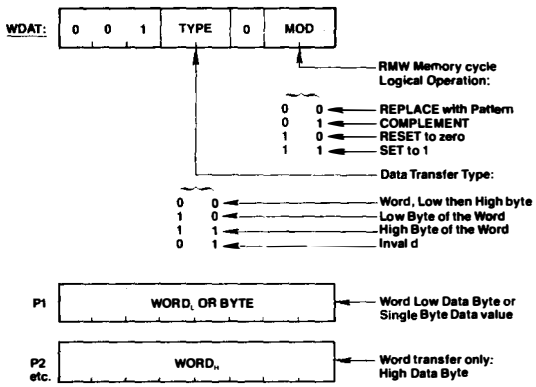


This value is used during drawing by the drawing processor to find the word directly above or below the current word, and during display to find the start of the next line.

The Pitch parameter (width of display memory) is set by two different commands. In addition to the PITCH command, the RESET (or SYNC) command also sets the pitch value. The "active-words-per-line" parameter, which specifies the width of the raster-scan display, also sets the pitch of the display memory. Note that the AW value is two less than the display window width. The PITCH command must be used to set the proper memory width larger than the window width.

Drawing Control Commands

Write Data into Display Memory



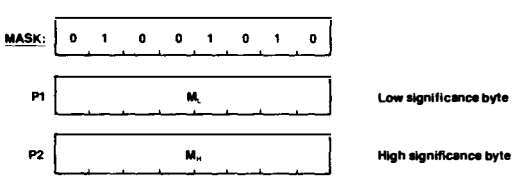
Upon receiving a set of parameters (two bytes for a word transfer, one for a byte transfer), one RMW cycle into video memory is done at the address pointed to by the cursor EAD. The EAD pointer is advanced to the next word, according to the previously specified direction. More parameters can then be accepted.

For byte writes, the unspecified byte is treated as all zeros during the RMW memory cycle.

In graphics bit-map situations, only the LSB of the WDAT parameter bytes is used as the pattern in the RMW operations. Therefore it is possible to have only an all ones or all zeros pattern. If the WG bit of the third parameter of the CURS command is set to one, any byte following the WDAT command is written as is. In coded character applications all the bits of the WDAT parameters are used to establish the drawing pattern.

The WDAT command operates differently from the other commands which initiate RMW cycle activity. It requires parameters to set up the Pattern register while the other commands use the stored values in the parameter RAM. Like all of these commands, the WDAT command must be preceded by a FIGS command and its parameters. Only the first three parameters need be given following the FIGS opcode to set up the type of drawing, the DIR direction, and the DC value. The DC parameter + 1 will be the number of RMW cycles done by the HGDC with the first set of WDAT parameters. Additional sets of WDAT parameters will see a DC value of 0 which will cause only one RMW cycle to be executed per set of parameters.

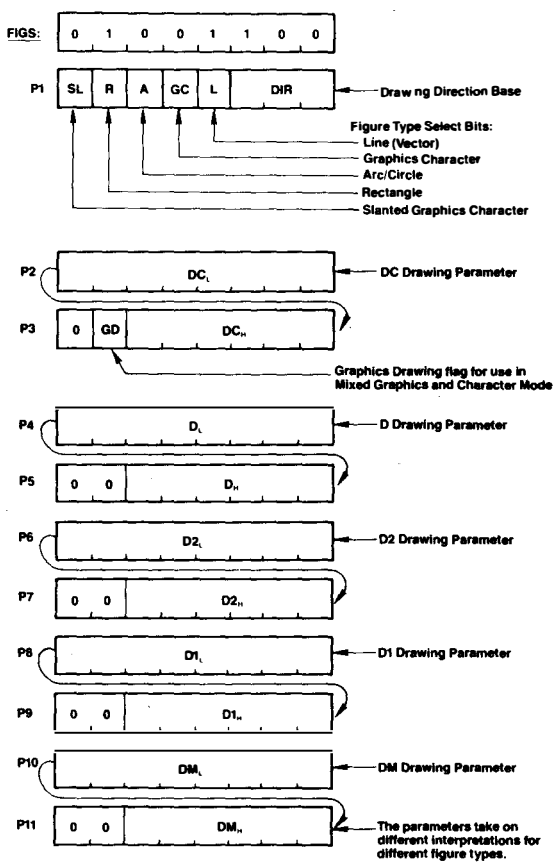
Mask Register Load



This command sets the value of the 16-bit Mask register of the figure drawing processor. The Mask register controls which bits can be modified in the display memory during a read-modify-write cycle.

The Mask register is loaded both by the MASK command and the third parameter byte of the CURS command. The MASK command accepts two parameter bytes to load a 16-bit value into the Mask register. All 16 bits can be individually one or zero, under program control. The CURS command, on the other hand, puts a 1-of-16 pattern into the Mask register based on the value of the Dot Address value, dAD. If normal single-pixel-at-a-time graphics figure drawing is desired, there is no need to do a MASK command at all since the CURS command will set up the proper pattern to address the proper pixels as drawing progresses. For coded character DMA, and screen setting and clearing operations using the WDAT command, the MASK command should be used after the CURS command if its third parameter byte has been output. The Mask register should be set to all ones for any "word-at-a-time" operation.

Figure Drawing Parameters Specify

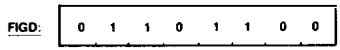


Valid Figure Type Select Combinations

SL	R	A	GC	L	Operation
0	0	0	0	0	Character Display Mode Drawing, Individual Dot Drawing, DMA, WDAT, and RDAT
0	0	0	0	1	Straight Line Drawing
0	0	0	1	0	Graphics Character Drawing and Area Filling with Graphics Character Pattern
0	0	1	0	0	Arc and Circle Drawing
0	1	0	0	0	Rectangle Drawing
1	0	0	1	0	Slanted Graphics Character Drawing and Slanted Area Filling

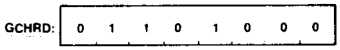
Only these bit combinations assure correct drawing operation.

Figure Draw Start



On execution of this instruction, the HGDC loads the parameters from the parameter RAM into the drawing processor and starts the drawing process at the pixel pointed to by the cursor, EAD, and the dot address, dAD.

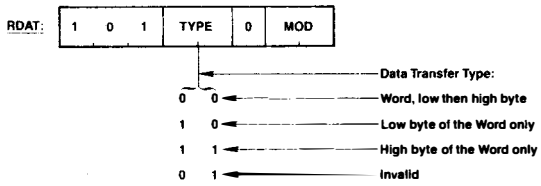
Graphics Character Draw and Area Filling Start



Based on parameters loaded with the FIGS command, this command initiates the drawing of the graphics character or area filling pattern stored in parameter RAM. Drawing begins at the address in display memory pointed to by the EAD and dAD values.

Data Read Commands

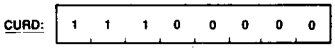
Read Data from Display Memory



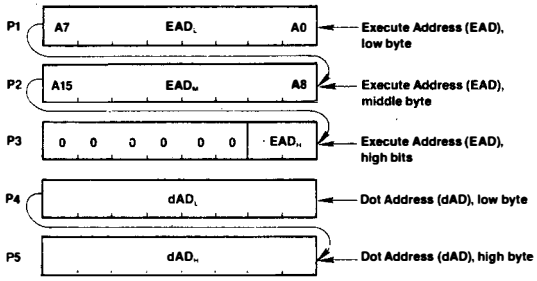
Using the DIR and DC parameters of the FIGS command to establish direction and transfer count, multiple RMW cycles can be executed without specification of the cursor address after the initial load (DC = number of words or bytes).

As this instruction begins to execute, the FIFO buffer direction is reversed so that the data read from display memory can pass to the microprocessor. Any commands or parameters in the FIFO at this time will be lost. A command byte sent to the HGDC will immediately reverse the buffer direction back to write mode, and all RDAT information not yet read from the FIFO will be lost. MOD should be set to 00 if no modification to video buffer is desired.

Cursor Address Read



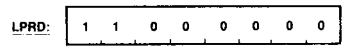
The following bytes are returned by the HGDC through the FIFO:



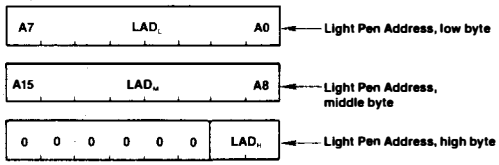
The execute address, EAD, points to the display memory word containing the pixel to be addressed.

The dot address, dAD, within the word is represented as a 1-of-16 code for graphics drawing operations.

Light Pen Address Read



The following bytes are returned by the HGDC through the FIFO:

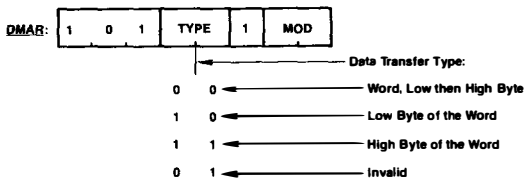


The light pen address, LAD, corresponds to the display word address, DAD, at which the light pen input signal is detected and deglitched.

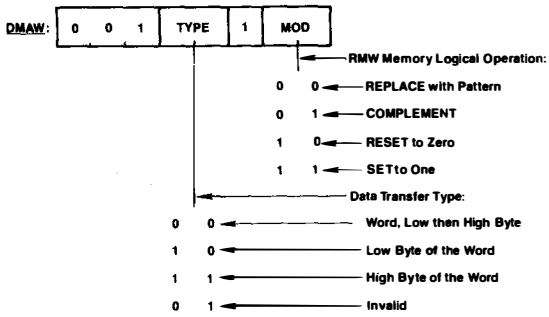
The light pen may be used in graphics, character, or mixed modes but only indicates the word address of light pen position.

DMA Control Commands

DMA Read Request



DMA Write Request



AC Characteristics

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%; GND = 0 V

		6 MHz Limits		8 MHz Limits			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
Read Cycle (GDC ⟷ CPU)							
Address setup to $\overline{RD}\downarrow$	t_{AR}	0		0		ns	
Address hold from $\overline{RD}\uparrow$	t_{RA}	0		0		ns	
$\overline{RD}$ pulse width	t_{RH1}	t_{RD1} + 20	t_{RCY} − 1/2 t_{CLK}	t_{RD1} + 20	t_{RCY} − 1/2 t_{CLK}	ns	
Data delay from $\overline{RD}\downarrow$	t_{RD1}		75		55	ns	C_L = 50 pF
Data floating from $\overline{RD}\uparrow$	t_{DF}	0	75	0	55	ns	
$\overline{RD}$ pulse cycle	t_{RCY}	4 t_{CLK}		4 t_{CLK}		ns	
Write Cycle (GDC ⟷ CPU)							
Address setup to $\overline{WR}\downarrow$	t_{AW}	0		0		ns	
Address hold from $\overline{WR}\uparrow$	t_{WA}	10		10		ns	
$\overline{WR}$ pulse width	t_{WW}	80	t_{WCY} − t_{CLK}	60	t_{WCY} − t_{CLK}	ns	
Data setup to $\overline{WR}\uparrow$	t_{DW}	65		45		ns	
Data hold from $\overline{WR}\uparrow$	t_{WD}	0		10		ns	
$\overline{WR}$ pulse cycle	t_{WCY}	4 t_{CLK}		4 t_{CLK}		ns	
DMA Read Cycle (GDC ⟷ CPU)							
$\overline{DACK}$ setup to $\overline{RD}\downarrow$	t_{KR}	0		0		ns	
$\overline{DACK}$ hold from $\overline{RD}\uparrow$	t_{RK}	0		0		ns	
$\overline{RD}$ pulse width	t_{RR2}	t_{RD2} + 20		t_{RD2} + 20		ns	
Data delay from $\overline{RD}\downarrow$	t_{RD2}		1.5 t_{CLK} + 80		1.5 t_{CLK} + 60	ns	C_L = 50 pF
DREQ delay from 2xWCLK↑	t_{REQ}		100		75	ns	C_L = 50 pF
DREQ setup to $\overline{DACK}\downarrow$	t_{QK}	0		0		ns	
$\overline{DACK}$ high-level width	t_{DK}	t_{CLK}		t_{CLK}		ns	
$\overline{DACK}$ pulse cycle	t_E	4 t_{CLK} (1)		4 t_{CLK} (1)		ns	
DREQ↓ delay from $\overline{DACK}\downarrow$	$t_{KQ(R)}$		t_{CLK} + 100		t_{CLK} + 80	ns	C_L = 50 pF
$\overline{DACK}$ low-level width	t_{LK}	2 t_{CLK}		2 t_{CLK}			

AC Characteristics (cont)

T_A = 0 to +70°C; V_{CC} = 5.0 V ±10%; GND = 0 V

		6 MHz Limits		8MHz Limits			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Test Conditions**
DMA Write Cycle (GDC ⟷ CPU)							
$\overline{DACK}$ setup to $\overline{WR}$↓	t_{KW}	0		0		ns	
$\overline{DACK}$ hold from $\overline{WR}$↑	t_{WK}	0		0		ns	
RMW Cycle (GDC ⟷ Display Memory)							
Address/data display from 2xWCLK↑	t_{AD}	20	105	15	80	ns	C_L = 50 pF
Address/data floating from 2xWCLK↑	t_{DFF}	20	105	15	80	ns	C_L = 50 pF
Input data setup to 2xWCLK↓	t_{DIS}	0		0		ns	
Input data hold from 2xWCLK↓	t_{DIH}	t_{DE}		t_{DE}		ns	
$\overline{DBIN}$ delay from 2xWCLK↓	t_{DE}	20	80	15	60	ns	C_L = 50 pF
ALE↑ delay from 2xWCLK↑	t_{RR}	20	80	15	60	ns	C_L = 50 pF
ALE↓ delay from 2xWCLK↓	t_{RF}	20	65	15	50	ns	C_L = 50 pF
ALE high width	t_{RW}	1/3 t_{CLK}		1/3 t_{CLK}		ns	C_L = 50 pF
ALE low width	t_{RL}	1.5 t_{CLK} − 30		1.5 t_{CLK} − 30		ns	
Address setup to ALE↓	t_{AA}	30		30			
Display Cycle (GDC ⟷ Display Memory)							
Video signal display from 2xWCLK↑	t_{VD}		90		70	ns	C_L = 50 pF
Input Cycle (GDC ⟷ Display Memory)							
Input signal setup to 2xWCLK↑	t_{PS}	10		10		ns	
Input signal width	t_{PW}	t_{CLK}		t_{CLK}		ns	
Clock (2xWCLK)							
Clock rise time	t_{CR}		15		15	ns	
Clock fall time	t_{CF}		15		15	ns	
Clock high pulse width	t_{CH}	70		52		ns	
Clock low pulse width	t_{CL}	70		52		ns	
Clock cycle	t_{CLK}	165	10000	125	10000	ns	

Note:

(1) For high-byte and low-byte transfers: $t_E = 5\ t_{CLK}$.

Capacitance

T_A = 25°C; V_{CC} = GND = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Capacitance	C_{IN}			10	pF	fc = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	
Output Capacitance	C_{OUT}			20	pF	V_I (unmeasured)
Clock Input Capacitance	Cϕ			20	pF	= 0V

DC Characteristics

T_A = 0°C to +70°C; V_{CC} = 5V ± 10%; GND = 0V

Parameter	Symbol	Limits Min	Typ	Max	Unit	Test Conditions
Input Low Voltage	V_{IL}	−0.5		0.8	V	①
Input High Voltage	V_{IH}	2.2		V_{CC} + 0.5	V	② ③
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 µA
Input Low Leak Current (except VSYNC, DACK)	I_{IL}			−10	µA	V_I = 0V
Input Low Leak Current (VSYNC, DACK)	I_{IL}			−500	µA	
Input High Leak Current (except LPEN/DH)	I_{IH}			+10	µA	V_I = V_{CC}
Input High Leak Current (LPEN/DH)	I_{IH}			+500	µA	
Output Low Leak Current	I_{OL}			−10	µA	V_O = 0V
Output High Leak Current	I_{OH}			+10	µA	V_O = V_{CC}
Clock Input Low Voltage	V_{CL}	−0.5		0.8	V	
Clock Input High Voltage	V_{CH}	3.5		V_{CC} + 1.0	V	
V_{CC} Supply Current	I_{CC}			270	mA	

Notes: ① For 2xWCLK, V_{IL} = −0.5V to +0.6V.
② For 2xWCLK, V_{IH} = +3.9V to V_{CC} +1.0V.
③ For $\overline{WR}$, V_{IH} = 2.5V to V_{CC} +0.5V.

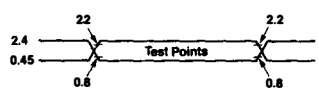
Absolute Maximum Ratings* (Tentative)

Ambient Temperature under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
Voltage on Any Pin with Respect to Ground	−0.5V to +7V
Power Dissipation	1.5 w

* Comment: Exposing the device to stresses above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

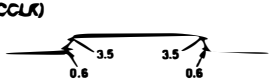
AC Testing Conditions

Input Waveform for AC Test (Except 2xCCLK)



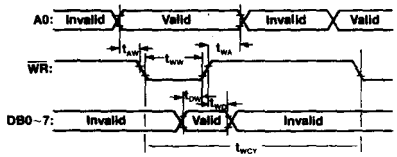
Output Waveform for AC Test

Clock Timing (2xCCLK)

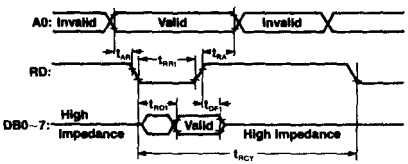


Timing Waveforms

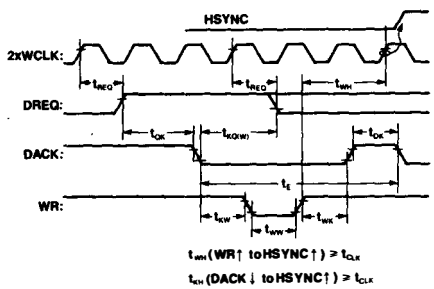
Microprocessor Interface Write Timing



Microprocessor Interface Read Timing

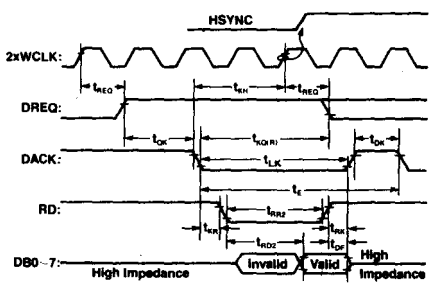


Microprocessor Interface DMA Write Timing



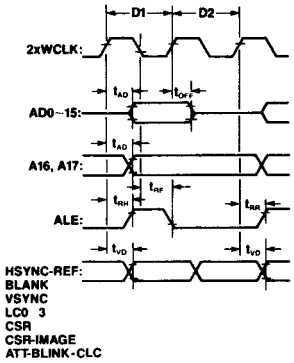
t_{WH} (WR↑ to HSYNC↑) ≥ t_{CLK}
t_{KH} (DACK↓ to HSYNC↑) ≥ t_{CLK}

Microprocessor Interface DMA Read Timing

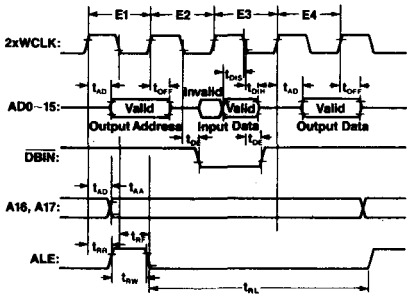


Timing Waveforms (Cont.)

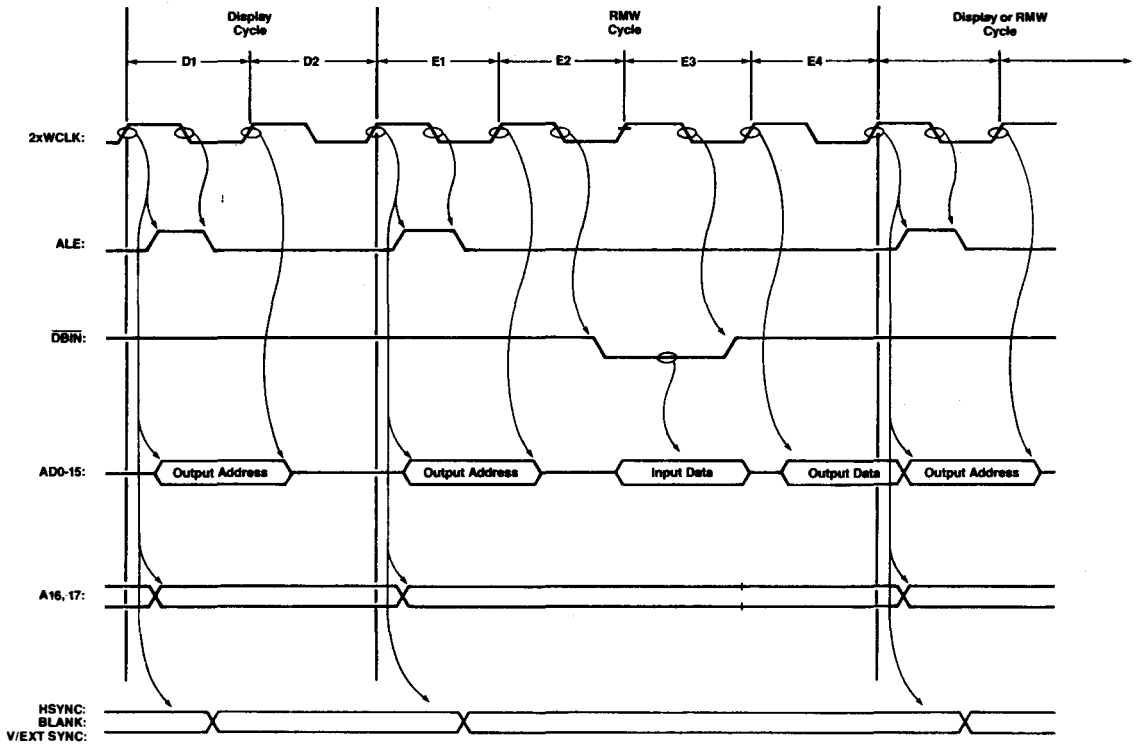
Display Memory Display Cycle Timing



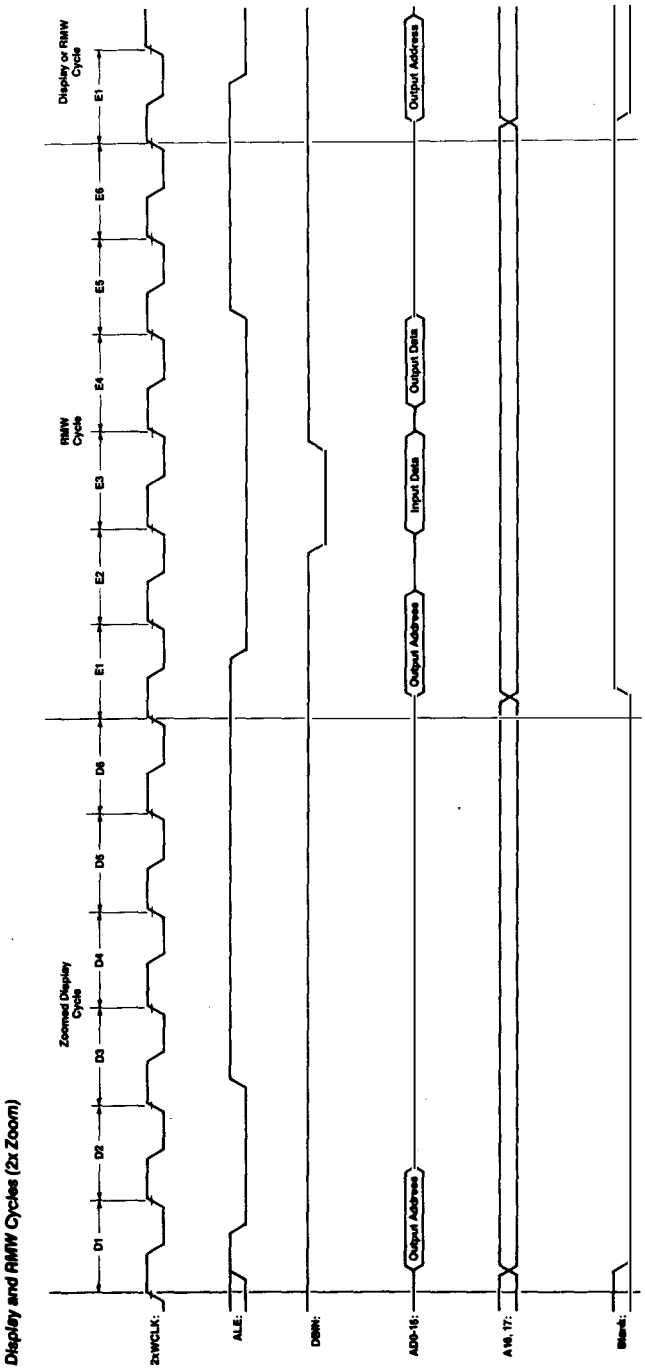
Display Memory RMW Timing



Display and RMW Cycles (1x Zoom)

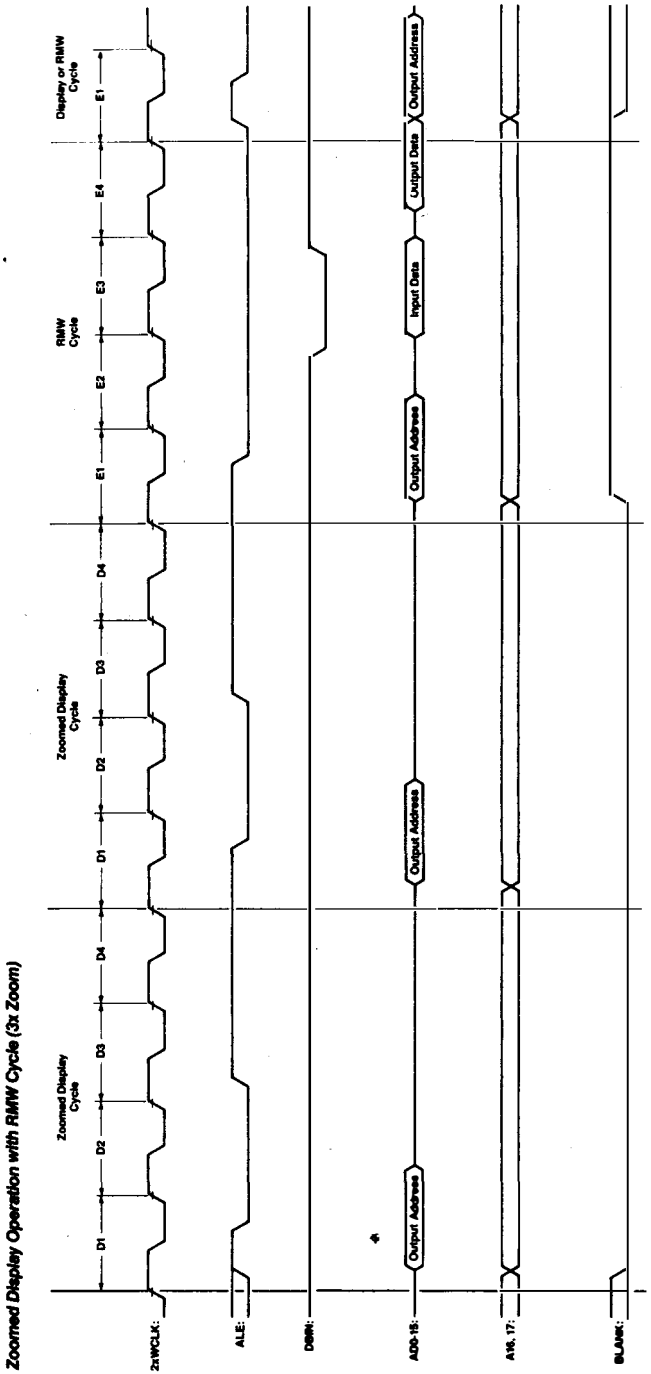


Timing Waveforms (Cont.)



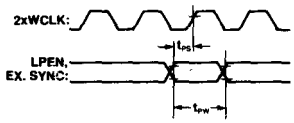
Display and RMW Cycles (2x Zoom)

Timing Waveforms (Cont.)

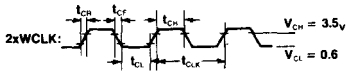


Timing Waveforms (Cont.)

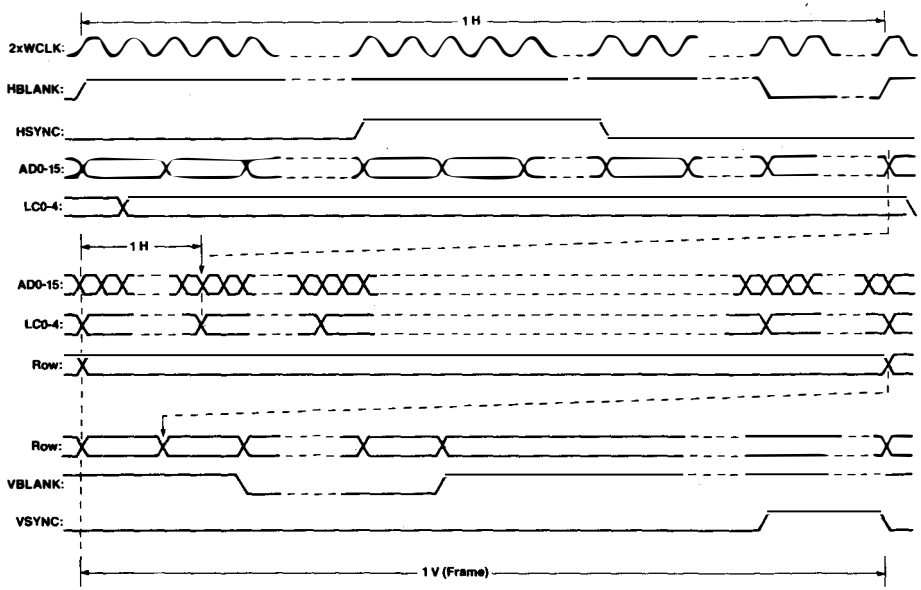
Light Pen and External Sync Input Timing



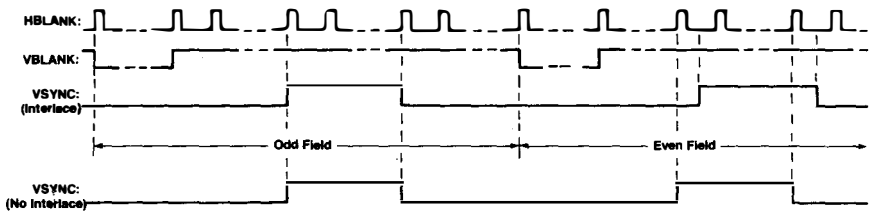
Clock Timing (2xWCLK)



Video Sync Signals Timing

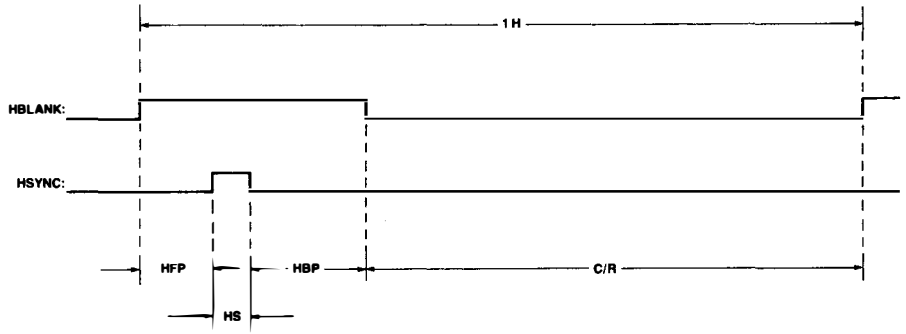


Interlaced Video Timing

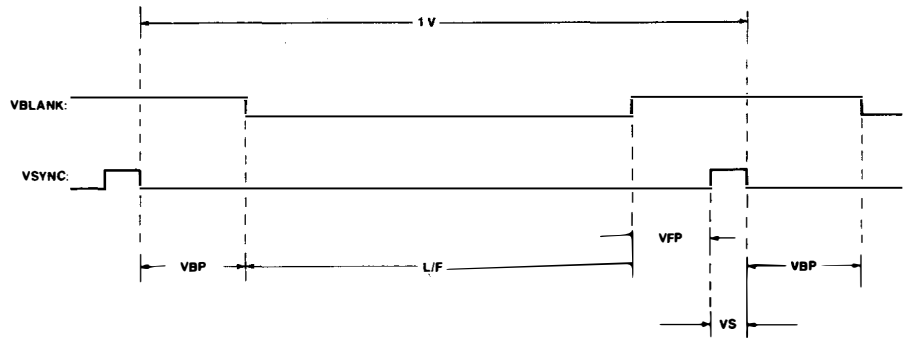


Timing Waveforms (Cont.)

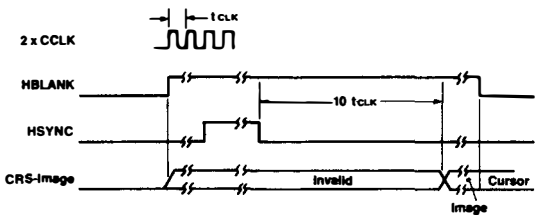
Video Horizontal Sync Generator Parameters



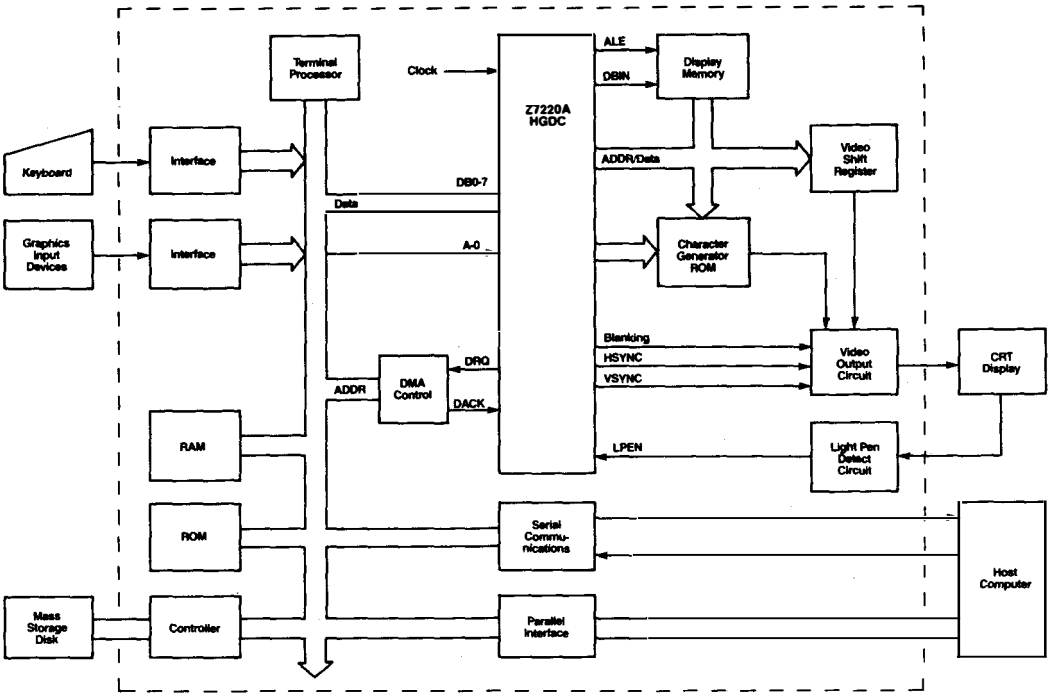
Video Vertical Sync Generator Parameters



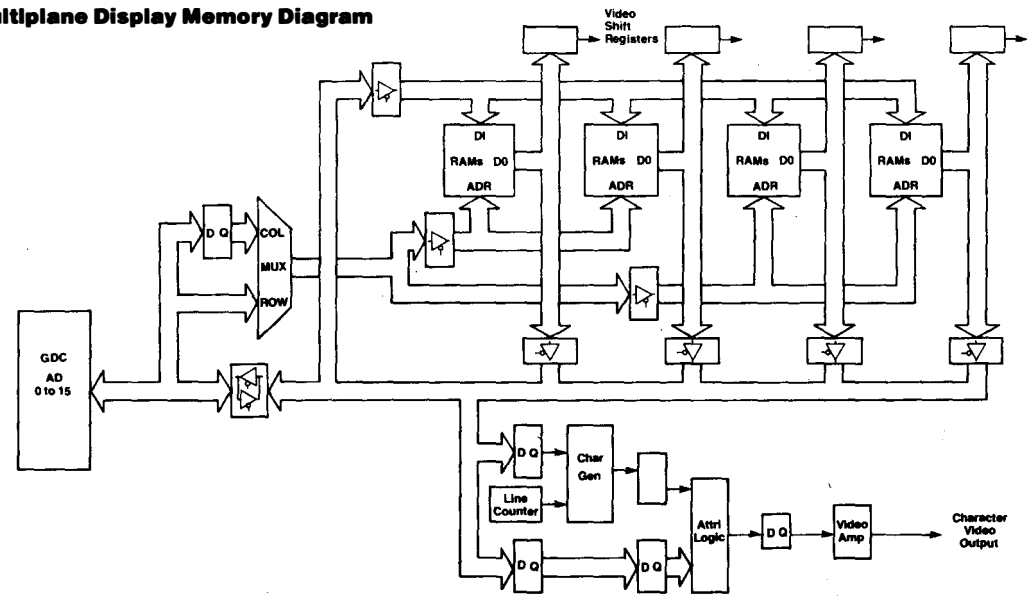
Cursor — Image Bit Flag



Block Diagram of a Graphics Terminal



Multiplane Display Memory Diagram



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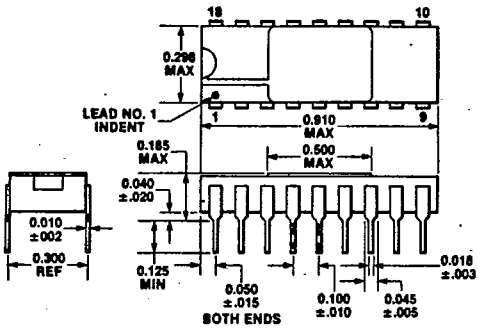
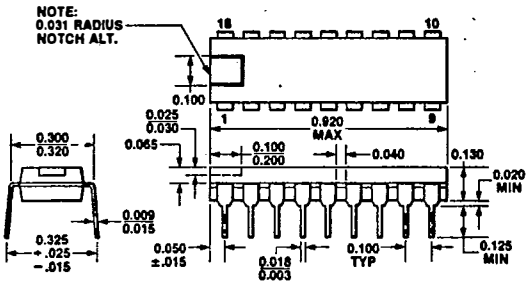
PACKAGE INFORMATION

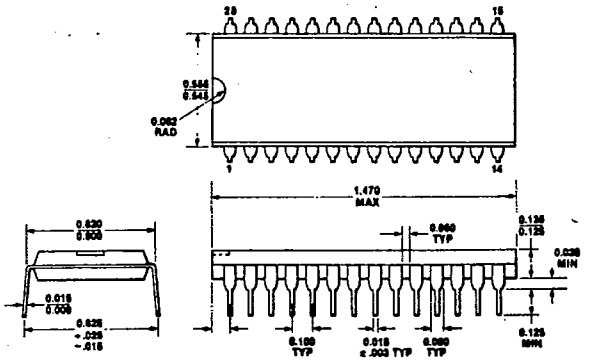


18-Pin Ceramic Package



18-Pin Plastic Package

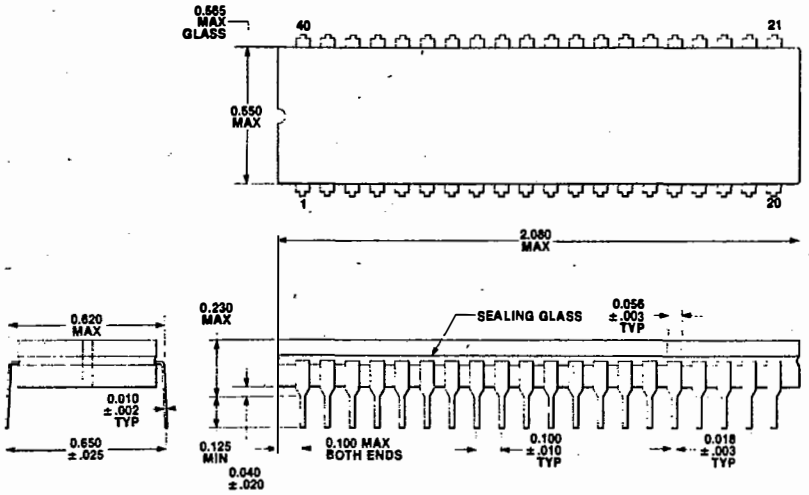
NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4



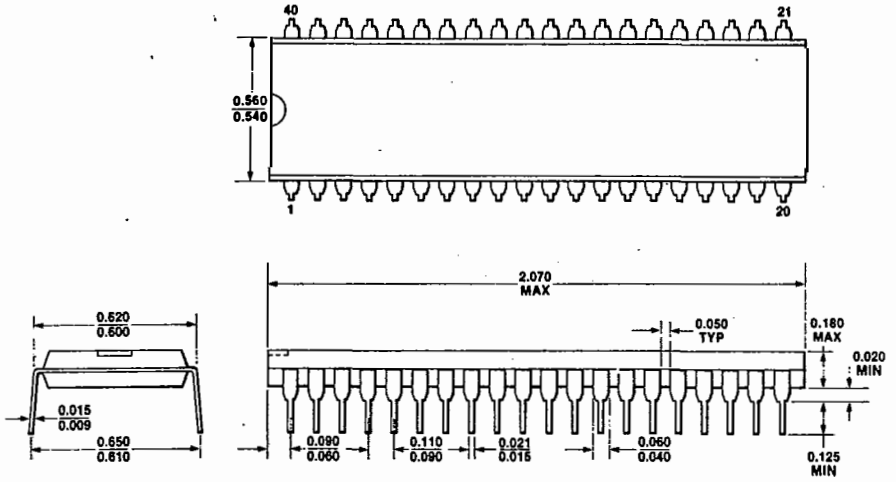
28-Pin Plastic Package

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

PACKAGE INFORMATION (Continued)



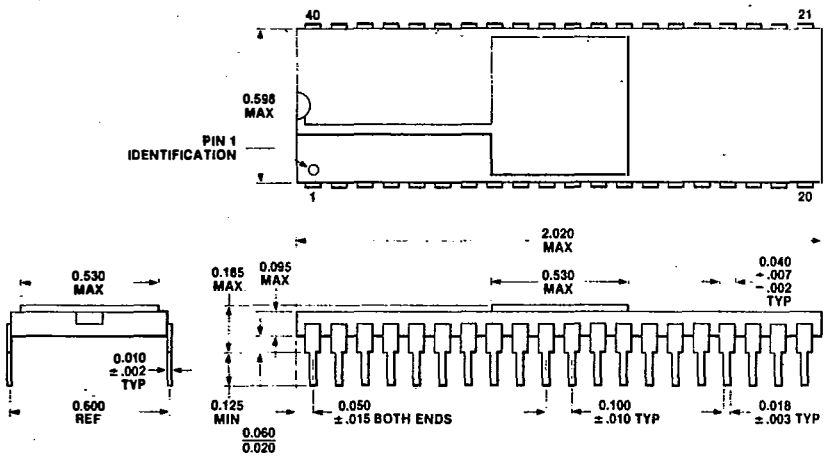
40-Pin Dual-In-Line Package (DIP), Cerdip



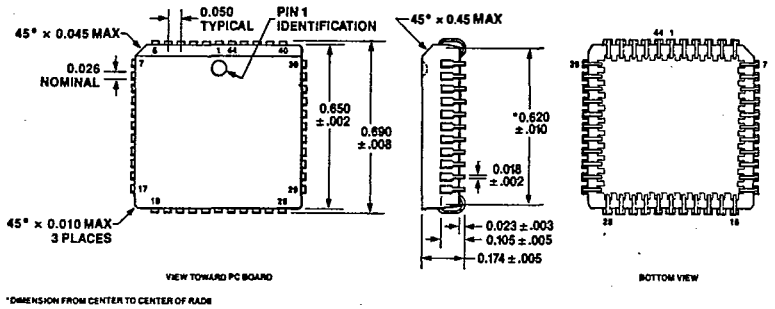
40-Pin Dual-In-Line Package (DIP), Plastic

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.

PACKAGE INFORMATION (Continued)

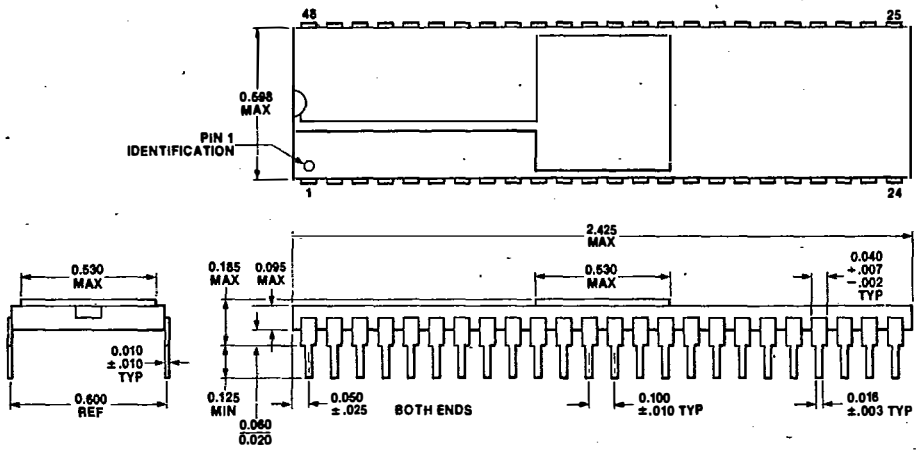


40-Pin Dual-In-Line Package (DIP), Ceramic

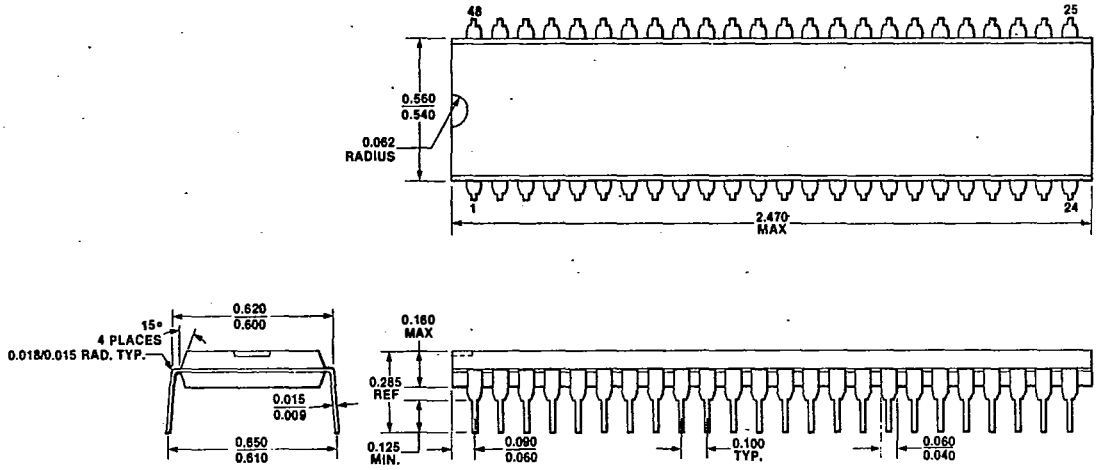


44-Pin Plastic Chip Carrier (PCC)

PACKAGE INFORMATION (Continued)



48-Pin Dual-in-Line Package (DIP), Ceramic



48-Pin Dual-in-Line Package (DIP), Plastic

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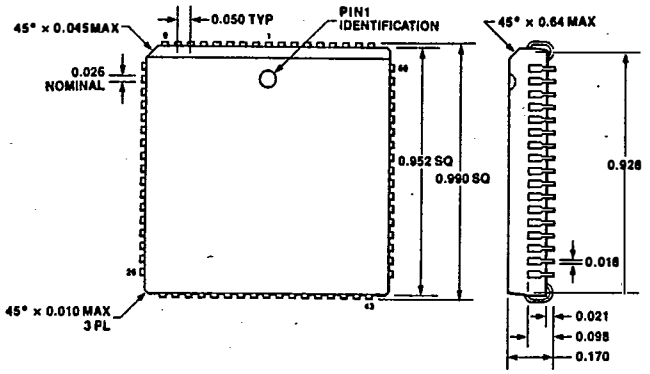
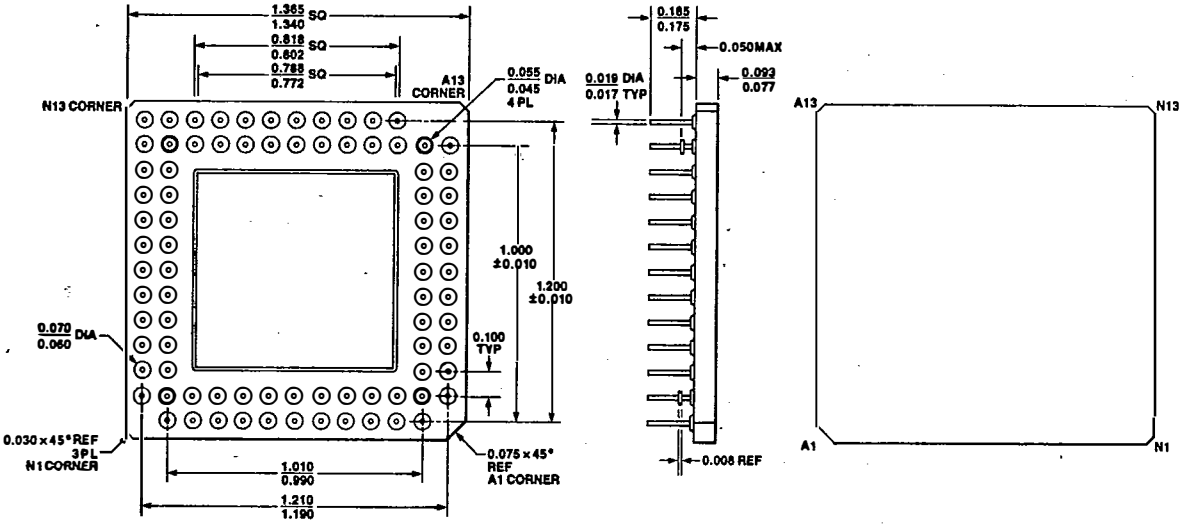
PACKAGE INFORMATION (Continued)



68-Pin Plastic Chip Carrier (PCC)



84-Pin Grid Array (PGA), Bottom View

View toward PC Board

NOTE: Package dimensions are given in inches. To convert to millimeters, multiply by 25.4.