MAINTENANCE HANDBOOK

4808

Multifunction Calibrator

MAINTENANCE HANDBOOK

for

THE DATRON 4808

MULTIFUNCTION CALIBRATOR

Part 1 - Calibration and Servicing Information

and

Part 2 - Technical Descriptions

For any assistance contact your nearest Datron Sales and Service center.
Addresses can be found at the back of this handbook.

850277 Issue 1 (MAR 1992)

Due to our policy of continuously updating our products, this handbook may contain minor differences in specification, components and circuit design to the instrument actually supplied. Amendment sheets precisely matched to your serial number are available on request.

CE

This product complies with the requirements of the following European Community Directives:
89/336/EEC (Electromagnetic Compatibility) and 73/23/EEC (Low Voltage)
as amended by 93/68/EEC (CE Marking).

However, noisy or intense electromagnetic fields in the vicinity of the equipment can disturb the measurement circuit. Users should exercise caution and use appropriate connection and cabling configurations to avoid misleading results when making precision measurements in the presence of electromagnetic interference.

DANGER
HIGH VOLTAGE

THIS INSTRUMENT IS CAPABLE OF DELIVERING A LETHAL ELECTRIC SHOCK !

I+, I- Hi and Lo terminals
Carry the Full Output Voltage
THIS CAN KILL !

Guard terminal is sensitive to over-voltage
It can damage your instrument !

Unless **you** are **sure** that it is **safe** to do so,
DO NOT TOUCH
the **I+ I- Hi** or **Lo leads** and **terminals**

DANGER

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PART 1

CALIBRATION AND SERVICING INFORMATION

SECTION 1 CALIBRATION

1. Routine Calibration procedures are given in the *User's Handbook, Section 8.*
2. Users are recommended to have first completed the Verification Procedures in *Section 7* of the *User's Handbook.*

1.1 GUIDE TO CALIBRATION

Circumstances Calling For Subsequent Recalibration

SCHEDULED RECALIBRATION

Routine calibration is carried out from the front panel, avoiding thermal disturbance and allowing immediate return to use. The 4808 is fully calibrated before leaving the factory. The specifications for the 4808 are based on standard intervals of up to 24 hours, 90 days or 1 year from calibration. Some users will wish to maintain the highest accuracy by recalibrating at short intervals (e.g. every 24 hours). In these cases, recalibration becomes a routine task. For this reason, Routine Autocalibration procedures are given in *Section 8* of the *User's Handbook.*

Users may wish to choose alternative schemes, accounting for:

- The accuracy required when in use,
- The instrument specifications *(User's Handbook Section 6)*
- The scheduled calibration intervals normally adopted by the user's organization

The Routine Calibration procedures are sufficient for all normal recalibration purposes, except when Pre-cal is called for *(Refer to Table 1.1).*

RESTANDARDIZATION

Occasions may arise when it is necessary to trim the instrument's internal Master Reference. For example, when the 4808 is to be made traceable to a different National Standard, after transportation from one country to another *(Refer to AUTOCAL FACILITIES page 1-5).*

CALIBRATION MEMORY CORRUPTION

Battery Change

Calibration constants are stored in an internal memory which remains energized by a battery. The Lithium battery which powers the non-volatile calibration memory should be replaced after 5 years *(Refer to Section 4.3).* After replacement, a full Pre-calibration is required followed by a complete Routine Autocalibration.

Memory Check failure

Whenever the **CAL** key is pressed, new calibration constants are checked to be within prescribed limits before being stored. Values outside prescribed limits flag a *Fail 6.* The same check is also performed:

- When the instrument is powered-up
- Each time the output is switched ON
- During each self-test routine

CRITICAL PART CHANGES

Recalibration (or Verification) is necessary after replacement of a critical PCB assembly or a critical component. These are listed in Table 1.1 *(see page 1-2),* indicating the extent of the recalibration necessary.

Ohms Internal Adjustments

- If the Power Supply/Current Heatsink has been changed it may be necessary to adjust the quiescent bias current (IQ) by internal adjustment. Refer to *Section 4.7* for further information.
- If a standard resistor value has been changed by subjecting it to undue stress, it may be possible to recalibrate by internal adjustment. Refer to *Section 4.4* for further information.

Recalibration Procedures in Section 1

REMOTE CALIBRATION VIA THE IEEE 488 BUS

The device-dependent commands necessary for routine calibration of the instrument over the IEEE 488 bus are described in *Section 5 of the User's Handbook.* A guide-line example is given in *Section 1.2 of this manual,* but this needs to be adapted for the bus controller in use.

PRE-CALIBRATION PROCEDURES *(Section 1.3)*

In an initial internal calibration process at manufacture, certain 'Pre-cal' parameters are established in a special calibration memory.

Under certain conditions (detailed in *Table 1.1*) these parameters need to be re-established by completing the 'Pre-Cal' procedure before a Full Routine Autocalibration.

REMOTE PRE-CALIBRATION

A guide line example is given in *Section 1.5,* but this needs to be adapted for the bus controller in use.

Assembly	Components Replaced	Calibration Required
Digital *(11.2)*	Complete Assembly Lithium Battery *(Sect. 4.3)* Non-volatile RAM (M10/M23) Non-volatile RAM Supply commutation components	Pre- & Routine Calibration Pre- & Routine Calibration Pre- & Routine Calibration Pre- & Routine Calibration
Reference Divider *(11.4)*	Complete Assembly Reference Assembly *(11.4-1)* Any set of main, guard or LSD switch FET's Reference Buffer Switch Driver Flip Flops or their preselected resistors R79	Pre- & Routine Calibration Pre- & Routine Calibration Pre- & Routine Calibration Pre- & Routine Calibration Pre- & Routine Calibration Pre- & Routine Calibration
DC Assembly *(11.5)*	Complete Assembly 1V attenuator R73/R74 100mV attenuator R69/70/71/72/75/7672/75/76 100V/1000V attenuator R8/9/25/26/46/47/64/65/88/95/98	DC (All Ranges) only. DC (1V, 100mV, 10mV, 1mV, 100µV Ranges) only. DC (100µV - 100mV Ranges) only. DC (100V, 1000V Ranges) only.
Sine Source *(11.6)*	Complete Assembly	Specification Verification at User's Discretion
AC Assembly *(11.7)*	Complete Assembly Sense Amplifier Reference Inverter AC/DC Transfer & Integrators	Routine Calibration Routine Calibration Routine Calibration Routine Calibration
Current/Ohms Current Assembly *(11.8)*	Complete Assembly (N.B. Internal Adjustment required, refer to *Section 4.4*) ÷10 attenuator (R43/44) (DCI function) Current shunts R8/9/10/79/80 (DCI function) M8 and associated components Current shunts Feedback resistor R45	DC/AC Current and Ohms DC/AC Current DC Current DC Current AC Current AC Current AC Current
Current/Ohms Ohms Assembly *(11.8)*	Standard Resistors, associated pre-selected/variable trimmer resistors (Ohms function)	Internal adjustment *(Section 1.4)* Ohms calibration (replaced values only)
All Other Assemblies Not Listed Above		Specification Verification at User's Discretion

Table 1.1

PREPARING THE 4808

Before any calibration is carried out, prepare the 4808 as follows:

1. Turn on and allow a minimum of 2 hours to warm up in the specified environment.

2. Cancel any MODE selection keys, ensure OUTPUT set to OFF.

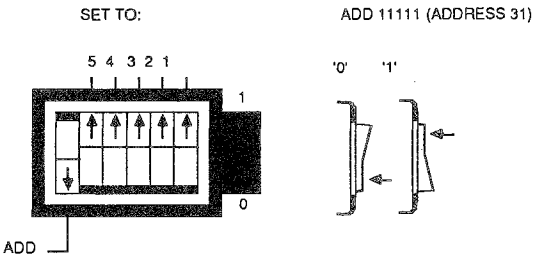
3. IEEE 488 Address switch:
   Set to ADD 11111 (Address 31) unless the 4808 is to be calibrated via the IEEE 488 interface.

4. CALIBRATION ENABLE key switch:
   Insert Calibration Key and turn to ENABLE.

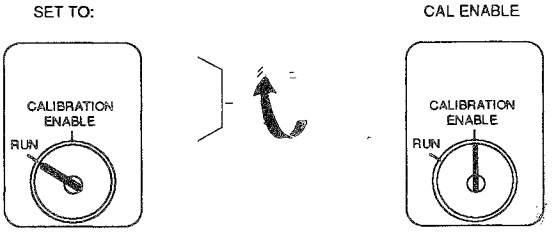
These actions activate the four calibration modes (labelled in red on the front panel), and present the cal legend on the MODE display.

Caution
Inadvertent use of the cal key can overwrite the calibration memory!

IEEE 488 ADDRESS
(LOCATED ON THE REAR PANEL)



SECURITY KEYSWITCH
(LOCATED ON THE REAR PANEL)



CAUTION:
Re-configuration of measurement circuitry should only be attempted when all voltage sources are OUTPUT OFF.

Before setting OUTPUT ON ensure the correct polarities have been selected and that any measurement device has been set to low sensitivity.

NOTE
The message *Error 3* appears on the left-hand MODE display for any attempt to select an inappropriate mode.

WARNING:

Terminals marked with the ⚠ symbol carry the output of the 4808. These terminals and any other connections to the load under test could carry lethal voltages. Under no circumstances should users touch any of the front (or rear) panel terminals unless they are first satisfied that no dangerous voltage is present.

RETURNING THE 4808 TO USE

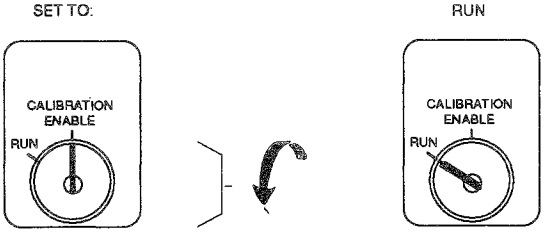
When any calibration is completed, return the 4808 to use as follows:

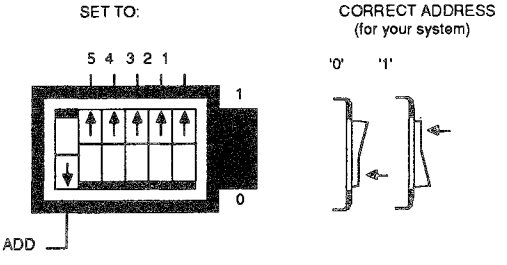
1. Ensure that **Output off** LED is lit.

2. CALIBRATION ENABLE key switch:
   Turn to **RUN** and withdraw calibration key.

3. IEEE 488 Address switch:
   Restore to **correct address** if the 4808 is to be used in an IEEE 488 system.

The cal legend and calibration modes are deactivated.





EQUIPMENT REQUIREMENTS

Before removing the 4808 from service check that the necessary calibration equipment is available. The equipment summary, listed by function, relates to the procedures recommended in this handbook:

Caution
When choosing a set of current shunts ensure that their power dissipation ratings are sufficient to avoid permanent degradation from the self-heating effects of the current being checked. This applies particularly to the 1Amp shunt.

DC FUNCTION

Low Voltage (100mV to 10V)
An adjustable DC Voltage source of suitable accuracy
Example: Datron 4000A Autocal Standard

A battery-operated null detector with variable sensitivity, able to withstand 1200V across its input terminals:
Example: Keithley Instruments Model 155

High voltage (100V and 1000V)
A Precision Divider
Example: Datron 4902/S High Voltage Divider.

A battery-operated null detector with variable sensitivity, able to withstand 1200V across its input terminals:
Example: Keithley Instruments Model 155

Current (100µA to 1A)
A DC Voltmeter, of suitable accuracy standardized at 1V and 100mV.
Example: Datron 1281.

A set of calibrated current shunts of suitable accuracy.
Example: Tinsley 5685 "Wilkins" Standard Resistors.

AC FUNCTION

Voltage (1V to 1000V)
An Adjustable DC Voltage Source of suitable accuracy.
Example: Datron 4000 or 4000A Autocal Standard.

An AC/DC Thermal Transfer Standard capable of operating over the range 1V to 1100V RMS.
Example: Characterized Holt 6B

2-wire HF compensation (1V to 10V)
An AC DVM of suitable accuracy
Example: Datron 1281

Millivolts at LF(1mV to 100mV)
A commercially-available Inductive Voltage Divider of suitable accuracy and frequency response; with ratios of 10:1, 100:1 and 1000:1.
Example: Tinsley 5560J

An AC DVM of suitable accuracy and frequency response.
Example: Datron 1281 or similar.

Millivolts at HF (1mV to 100mV)
An AC DVM of suitable accuracy and frequency response.
Example: Datron 1281 or similar.

Current (1mA to 1A)
A DC Current Source of suitable accuracy.
Example: Datron 4000 or 4000A Autocal Standard

AC/DC Thermal Transfer and a set of Calibrated Thermal-Transfer Current Shunts of suitable accuracy.
Example: Holt 6B and HCS-1 AC/DC Shunts.

An AC/DC transfer switching unit
Example: Holt HCS-1

Current (Alternate) (1µA to 1A)
A set of calibrated AC Shunts of suitable value and accuracy.
Example: Tinsley 5685 AC/DC Standard resistors.

An AC DVM of suitable accuracy and frequency response.
Example: Datron 1281 or similar.

A Buffer capable of operating with negligible errors from DC to 5kHz at a 1Volt level

RESISTANCE

2-Wire & 4-Wire (10Ω to 100MΩ)
A set of standard resistors covering 10Ω to 100MΩ. The 10Ω to 10kΩ should be 4-wire type.

Example:	For 10Ω - 10kΩ	Tinsley 5685
	For 100kΩ - 10MΩ	Guildline 9330

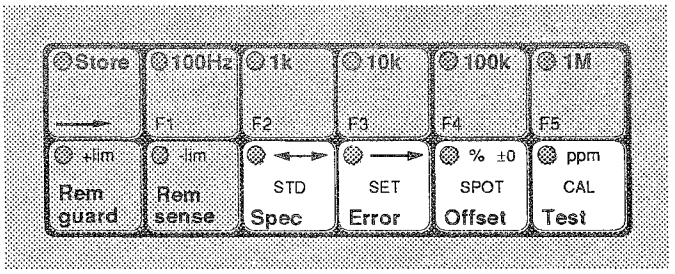
An accurate resistance bridge, or other ratiometric device for measuring resistance to the required accuracy.

A Datron 1281 used as a transfer-measurement device.

AUTOCAL FACILITIES

These keys are activated by two rear panel switches *(refer to page 1-3 'Preparing the 4808')*. When these modes are active, the legend 'cal' is presented on the left-hand MODE display.

The following is a general description of the facilities available. For specific information see the introduction proceeding each of the function's calibration routines.



CAL

The 4808 assumes that the selected range is to be calibrated at the exact Full Range value or at Zero. The instrument decides on 'Zero Offset' or 'Full Range Gain' from the right-hand OUTPUT display value (defined by the same limits as for 'SET'), and executes the calibration. If the value initially set on the OUTPUT display is below 2% of Full Range value, the instrument assumes that an offset calibration is requested, and if at 2% or above, a gain calibation is assumed.

CAL (with pre-selection)

If the CAL key is pressed after first pressing STD, SET or ±0, the CAL key executes, then cancels, the preselected AUTOCAL mode.

Caution
The following keys preselect an AUTOCAL mode, modifying the action of the CAL key.

SET

The SET key allows gain or offset calibration to a Calibration Standard value which cannot be adjusted to a nominal Full Range value or to absolute zero.

Before selecting SET, the ◇ keys are operated to place the Calibration Standard value on the OUTPUT display and set the 4808 output level.

Pressing SET then informs the 4808 that calibration is to be carried out at this value. The instrument acknowledges by duplicating the value on the MODE display.

Next, the ◇ keys are manipulated to null the 4808 output against the Calibration Standard (the OUTPUT display changes during this adjustment).

Pressing the CAL key executes the calibration. The 4808 memorizes the difference between the two display values, and exits from SET mode. This is shown by transfer of the Standard value from the left-hand MODE display to the right-hand OUTPUT display. The instrument uses the difference to modify stored constants, which in 'RUN' mode correct both positive and negative outputs on the calibrated range only.

±0 / SPOT

On the DCV function, the ±0 key is used to align the ON+ and ON- zeros of all DC voltage and current ranges, by a two part calibration on the 10V range. It is only necessary when the ON+ and ON- zeros of the 10V range do not coincide at the same null.

On the ACV and ACI function, the function of the key changes to SPOT Frequency calibration. When SPOT is pressed, the 4808 assumes that the spot frequency is to be changed, and so defaults the frequency to 1kHz. When used with SET, SPOT calibration can be carried out within 10% of the full range value, but when SPOT is used without SET, the 4808 assumes that the calibration is to be at Full Range. After SPOT calibration, selecting Spot Frequency at the calibrated value achieves the highest possible accuracy (*see User's Manual, Section 4*). It is only necessary to perform Spot Frequency calibration if the accuracy achievable is required in use. For recall procedures see the User's Manual page 4-10.

STD

Caution
Using the STD key changes the gain of all voltage and current ranges.

The STD key allows a user to re-standardize by trimming the value of the internal Master Reference voltage effectively changing the gain of all DC voltage and current ranges in the same ratio. The facility can be used to avoid a full recalibration of the 4808 when Laboratory References have been re-standardized (for instance when the instrument has been moved from one country to another).

First check ±0 Alignment. The STD calibration is carried out on either the 1V or 10V range, using the DC Low Voltage procedure. Select STD after placing the Calibration standard value on the OUTPUT display. Continue the routine from step (1). Procedurally STD differs from SET only in the use of the STD key instead of the SET key.

GENERAL NOTES

INTERCONNECTIONS

It is recognised that interconnection instructions may need to be adapted to meet an individual user's requirements. It is assumed that users will possess some knowledge of the operation and use of standards equipment.

SENSE AVAILABILITY AS FOLLOWS

1V 10V 100V 1000V - Local/Remote Sense
1mV 10mV 100mV - Local Sense only
All current ranges - not applicable
(Local: 2-wire sense, Remote: 4-wire sense)

Output must be OFF to change sense connection (except that Remote changes automatically to Local when switching to Millivolt Ranges).

OUTPUT OFF DEFAULT WHEN UPRANGING

The 4808 cannot enter High-Voltage state with OUTPUT ON. Consequently, when ranging-up, the operating system allows the upranging to occur, but defaults to OUTPUT OFF for two specific cases:

1. When upranging to the 1000V Range.
2. When upranging to the 100V Range:
   To a voltage of 90V or more on DC
   To a voltage of 75V or more on AC

Otherwise, OUTPUT remains ON when changing OUTPUT RANGE.
Refer to User's Handbook, Section 4.

GENERAL PROCEDURE

Prepare the instrument for calibration *(refer to 'Preparing the 4808' procedure on page 1-3)*. Note that your instrument will not necessarily have all options fitted

The available options for the 4808 are as follows:

Option 10: DC Voltage function to ±200V.

Option 20: AC Voltage function to 200V.

Option 30: Integral 1000V amplifier for AC Voltage and/or DC Voltage functions. (Requires either Option 10, Option 20 or both.)

Option 40: Current converter to provide DC Current and AC Current functions. (DC Current capability requires Option 10, AC Current capability requires Option 20.)

Option 50: Resistance function. (Requires Option 10 or Option 20.)

Option 60: DC Current and/or AC Current range extension to 11A. This option includes the Datron 4600 Transconductance Amplifier and all necessary cabling. (Requires Option 40.)

The message *'Error 3'* appears on the left-hand MODE display for any attempt to select an inappropriate mode. Select the equipment and procedures to be used. Set all sources to zero and all measurment devices to low sensitivity and configure using the interconnection diagram provided. If calibrating DC function, start with ±0 Alignment check routine. When all calibration has been completed use the 'Return to Use' routine on page 1-3.

Calibration Routine

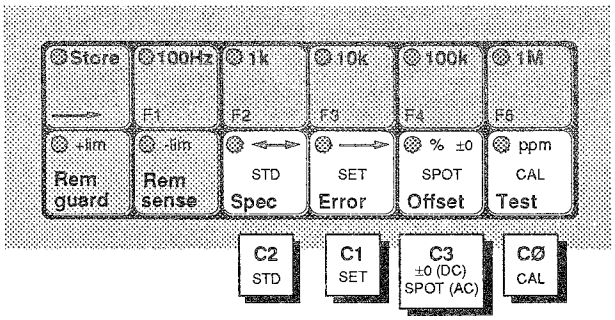
Set the 4808 to OUTPUT ON and Full Range value. Adjust the 4808 output to equal the calibration standard and press CAL. The right-hand OUTPUT display changes to nominal.

Calibration Routine (with preselection)

The OUTPUT display is set to the Calibration Standard value, the 4808 output is switched ON, and one of the calibration mode preselector keys (STD, SET or ±0) is pressed. The 4808 output is adjusted to equal the Calibration Standard value, and the CAL key is pressed to execute the calibration.

1.2 REMOTE CALIBRATION GUIDELINES

The operation of the instrument in systems applications via the IEEE 488 interface, is described in Section 5 of the User's Handbook. In addition to its capability as a programmable calibrator, the 4808 can itself be calibrated under remote control. Full autocalibration of the instrument over the bus implies availability of a suitably programmed controller, programmable standards, programmable Null Detector, and a programmable Thermal Transfer.



Transfer of Calibration Facilities

Calibration Commands

The table below lists the device-dependant commands used for Routine Calibration. The relevant calibration codes are also listed.

These commands can only be activated when two conditions have been fulfilled:

1. the CALIBRATION ENABLE keyswitch on the instrument Rear Panel must be set to ENABLE, and
2. the IEEE Interface command-code W1 must have been received and activated.

Additional commands can be activated when 'PRE-CAL ENABLE' switch is enabled. *Refer to 1.5 Remote Pre-Calibration Guidlines.*

When the 4808 is under remote control over the bus, the command-code WØ overrides the settings of the CALIBRATION ENABLE and internal PRE-CALIBRATION ENABLE switches, disabling the 'C' codes.

General Procedure

The Main Register is set to the Calibration Standard value (M***...), the 4808 Output is switched ON (01), and one or a specified sequence of the calibration mode command codes (C1, C2, C3, I) may be transmitted.

The 'M' Code is adjusted to obtain a null at the Calibration Standard value, and CØ is transmitted to execute the calibration.

Availability of Command Codes

Command Codes (Key caps)	Description	Functions and Facilities					
		DC Voltage	DC Current	AC Voltage	AC Current	2-Wire Ω	4-Wire Ω
CØ (CAL)	Range Zero	100mV-1000V Ranges	All Ranges			10Ω-1MΩ Ranges	
	Gain calibration to Nominal Full Range	100mV-1000V Ranges	All Ranges	All Ranges	All Ranges	10Ω-1MΩ Ranges	All Ranges
*C1 (SET)	Zero offset for range at User's selected value	All Ranges	All Ranges				
	Gain for range at User's selected value	All Ranges	All Ranges	All Ranges	All Ranges		
*C2 (STD)	Internal Reference gain at user's Standard value	1V &10V Ranges		1V &10V Ranges			
*C3 (±0)	Alignment of internal ON+ and ON- zeros	10V Range					
I	User's Message	Refer to User's Handbook Section 5 'Programming of Bus Transmissions'					

*Preselector - must be activated later by command code CØ (CAL)

COMMAND CODE FACILITIES (Routine Calibration)

For a General description see 'Autocal Facilities' *page 1-5.*

Calibration Codes

C1 (SET)

C1 gives calibration at any point in the selected range by allowing the user to input the value of the calibration standard used (initial M code used). Before executing the calibration CØ uses the final 'M' Code value to distinguish between Zero (offset calibration) and Full Range (gain calibration). The limits of Offset or Full Range depend on function selected *(Refer to User's Handbook, Section 8).*

C2 (STD)

C2 allows a user to compensate for changes of the internal Master Reference voltage. For best accuracy it is recommended this procedure is carried out in DC function. Note that the gains of all voltage and current ranges change in the same ratio. Execute with CØ.

CØ (execute pre-selection)

CØ executes one of the above preselected AUTO-CAL modes.

CØ (CAL only)

If Command CØ is sent without pre-selection code C1/C2 the instrument assumes that the selected range is to be calibrated at either Zero or Full Range. It uses the value input by the 'M' Code to distinguish between Zero (offset calibration) and Full Range (gain calibration) according to the function selected *(Refer to User's Handbook, Section 8).*

Guidelines - An Example

The following sequence suggests a method of calibrating the instrument 1V Range Gain against a buffered standard cell value of +1.018057V. It is assumed that the instrument is correctly addressed with its Calibration Keyswitch set to ENABLE and the instrument Output is OFF. Connect the Null Detector, set to low sensitivity, between the Standard Cell buffer and the 4808. The nulling operation is seperated into its own string, as it is likely to be iterative.

SET Calibration of 1V DC Gain
FØR5GØSØW1M+1.018057C101=M(for null)CØ

The example suggests only the broad outline of one of many sequences which could be used to perform instrument calibrations.

Calibration Command Strings

The following AC command strings are given for the sole purpose of illustrating the methodology designed into the 4808 for remote calibration modes. Some reference to external operations is inferred. The nulling operation is seperated into its own string, as it is likely to be iterative.

It is assumed that the 4808 has previously been programmed in function and range (not autorange RØ) and that the external circuit is set up correctly. The 4808 is already programmed into its calibration mode by W1, with the calibration keyswitch set to ENABLE, and output OFF.

a. Nominal Full Range LF Gain Calibration:
H(LF)A1O1=M (for null)=CØ=OØ=

b. Nominal Full Range HF Gain Calibration:
H(HF)A1O1=M(for null)=CØ=OØ=

c. Combined Nominal LF and HF Gain Cal:
H(LF)A1O1=M(for null)=CO=
H(HF)=M(for null)=CO=O0=

d. Non-nominal LF Gain Calibration:
H(LF) M(20%-200%FR)C1=
O1=M(for null)=CØ=OØ=

e. Non-nominal HF Gain Calibration:
H(HF) M(20%-200%FR)C1=
O1=M(for null)=CO=O0=

f. Combined Non-nominal LF and HF Gain Cal:
H(LF)M(20%-200%FR)C1=
O1=M(for null)=CØ=
H(HF)M(20%-200%FR)C1=
M(for null)=CØ=OØ=

g. Standardization at Nominal Full Range
1V or 10V Range only):
H(LF)A1C2O1=M(for null)=CØ=OØ=

h. Standardization at a Non-nominal value
(1V or 10V range only):
H(LF)M(20%-200%FR)C2=
O1=M(for null)=CØ=OØ=

1.3 PRE-CALIBRATION

1.3.1 Introduction

GENERAL

In an initial calibration process at manufacture, certain 'PRE-CAL' parameters are established in a special calibration memory to define the overall linearity of the instrument, and to allow maximum routine calibration memory span for adjustments. For normal purposes, these factory defined pre-calibration parameters are valid for the life of the instrument, and subsequent Routine Calibration procedures are sufficient to maintain calibration.

Preparation for the pre-calibration operation includes removal of the Top Cover, to facilitate selection of pre-calibration mode and operation of the calibration memory clear push-button. DC and AC pre-calibration must then be completed followed by a Full Routine Recalibration. Thereafter, all routine calibrations may be performed from the front panel or over the IEEE Interface without removing the covers.

Circumstances Calling for Pre-Calibration

The stored parameters are invalidated by replacement of certain critical parts of the instrument.

- The Lithium battery which powers the whole calibration memory when the instrument supply is switched off. This should be replaced at five-year intervals *(Refer to Section 4.3)*.
- The Digital Assembly
- The Reference Divider Assembly
- Critical components in the Digital or Reference Divider, AC and Sine Source assemblies

A full list appears on flap of page 1-2. After replacement of any of these parts, new parameters must be stored in the pre-calibration memory, by procedures (in manual or remote control) detailed in this section.

EQUIPMENT REQUIREMENTS

DC

- A precision divider capable of dividing 20.000,000V to 10.000,000V to a ratio error of better than 0.1ppm between tappings. For example a Datron 4902/S precision divider or alternatively a Datron 4903 DC Calibration Unit.
- A DC 10V reference with an accuracy of better than 2ppm. Example: Datron Instruments 4000A or a bank of standard cells.

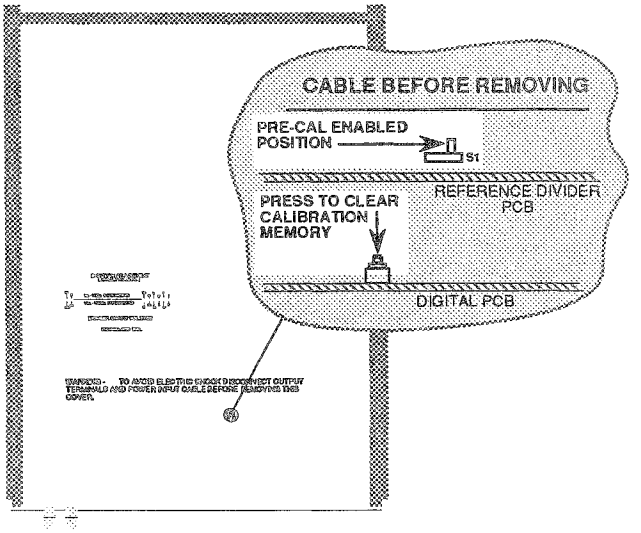
AC

- A precision voltmeter capable of 1V AC measurement with a stability between readings of better than ±5ppm. Example: Datron Instruments 1281
- An inductive voltage divider with ratios of x1.0 and x0.1 capable of dividing 10.000,00V to 1.000,000V to an accuracy better than 2ppm.
- An AC/DC Thermal Transfer Standard. Example: Holt Model 6B

PREPARING THE 4808

Before clearing the pre-calibration store, prepare the 4808 as described on *page 1-3*. The adjustments detailed in the following sequences include intentionally clearing the instrument's pre-calibration memory, which loses ALL previous calibration information. Therefore before proceeding make certain that the reasons for carrying out a complete recalibration are valid. (If in any doubt, consult your Datron Service Centre)

Identification of Access Holes



These holes provide access to the 'PRE-CAL ENABLE' switch and the 'CLEAR CALIBRATION MEMORY' switch.

a. Release 6 screws retaining the top cover.

b. Lift the top cover at the front of the instrument and locate the two holes which give access to the two-position 'PRE-CAL ENABLE' switch and the press-button 'CLEAR CALIBRATION MEMORY' switch.

c. Locate the hole which gives access to the PRE-CAL ENABLE switch. Insert an insulated tool in the hole and move the pre-cal switch to the right (Enable). The legend 'cal', as presented on the left-hand MODE display, also appears on the right-hand OUTPUT display.

Caution
The following operation (d.) clears all the calibration memory stores as part of pre-calibration. Proceed only if this is required.

d. Locate the hole which gives access to the Calibration Memory CLEAR push-button. Insert an insulated tool in the hole and press the button to clear the calibration memory.

e. Refit the top cover but do not secure.

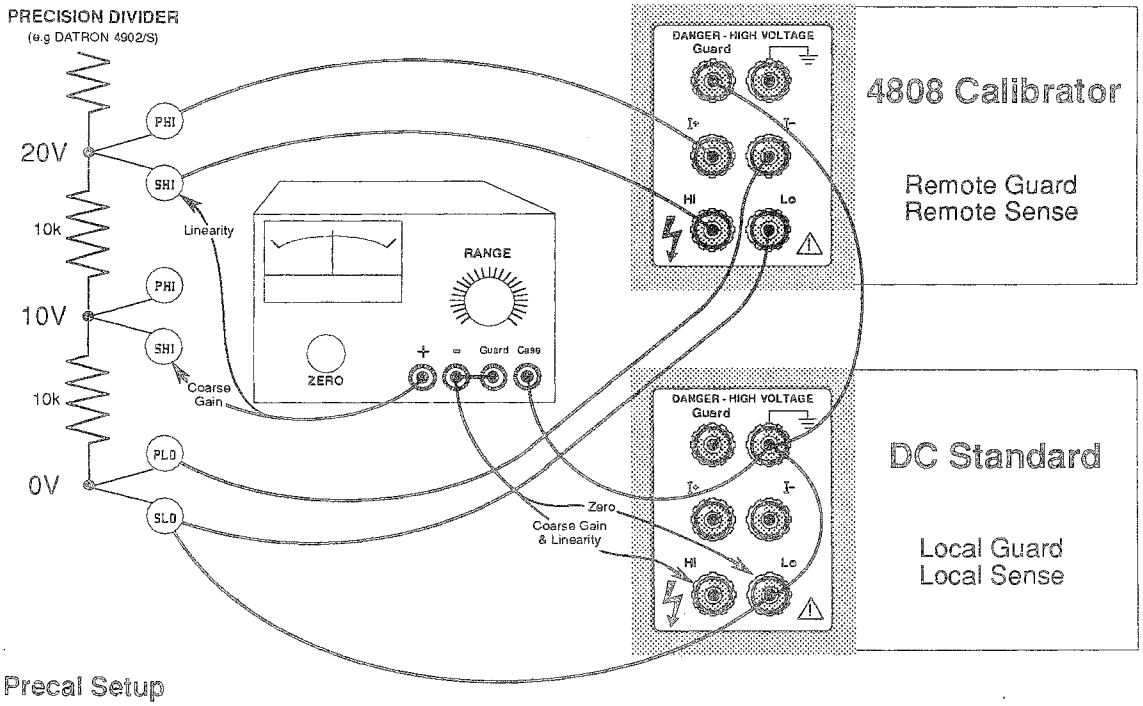
Complete the following pre-calibration procedure *(Paras 1.3.2 overleaf)*.

1.3.2 Procedure

DCV Precal

± Zero Calibration

First complete the ±0 Alignment Calibration Procedure in *Section 8 of the User's Handbook*, but with pre-calibration mode selected.



DCV Precal Setup

Ensure the 4808 Output off LED is lit, cancel any MODE keys, select Remote Sense and deselect Remote Guard. Select DCV FUNCTION and 10V RANGE. Connect the Precision Divider to the instrument terminals as shown. Use short leads.

Coarse Gain

a. 4808
Ensure OUTPUT OFF and select the 10V RANGE.

b. Precision Divider/Null Detector
Set the Null Dectector to Low sensitivity and connect to the Precision Divider at 10V tapping.

c. 4808
Connect to the precision divider as shown. Select ON+ with zero OUTPUT.

d. DC Standard/Null Detector
If the DC Standard is a buffered bank of standard cells, switch the Buffer output to zero. However if an electronic reference is used connect Null Detector -ve lead to Reference Low.

Set Null Detector to high sensitivity. Zero Null Detector. Reduce Null Detector sensitivity.

Switch on or reconnect the 10V DC Standard Hi to Null detector.

e. 4808
Select SET, its LED lights. Adjust the OUTPUT keys for Full Scale OUTPUT (+19.999999V).

Use instrument OUTPUT ◇ keys to adjust the Null Detector reading to zero.

Press CAL: the SET LED goes out.

Linearity

f. Precision Divider/Null Detector
Reduce Null Detector sensitivity. Reconfigure Null Detector Hi to divider 20V tapping.

g. DC Standard/Null Detector
If the DC Standard is a buffered bank of standard cells, switch the Buffer output to zero. However if an electronic reference is used, connect the Null Detector -ve lead to the DC Standard's Low terminal.

Set Null Detector to high sensitivity. Zero Null Detector. Increase Null Detector sensitivity.

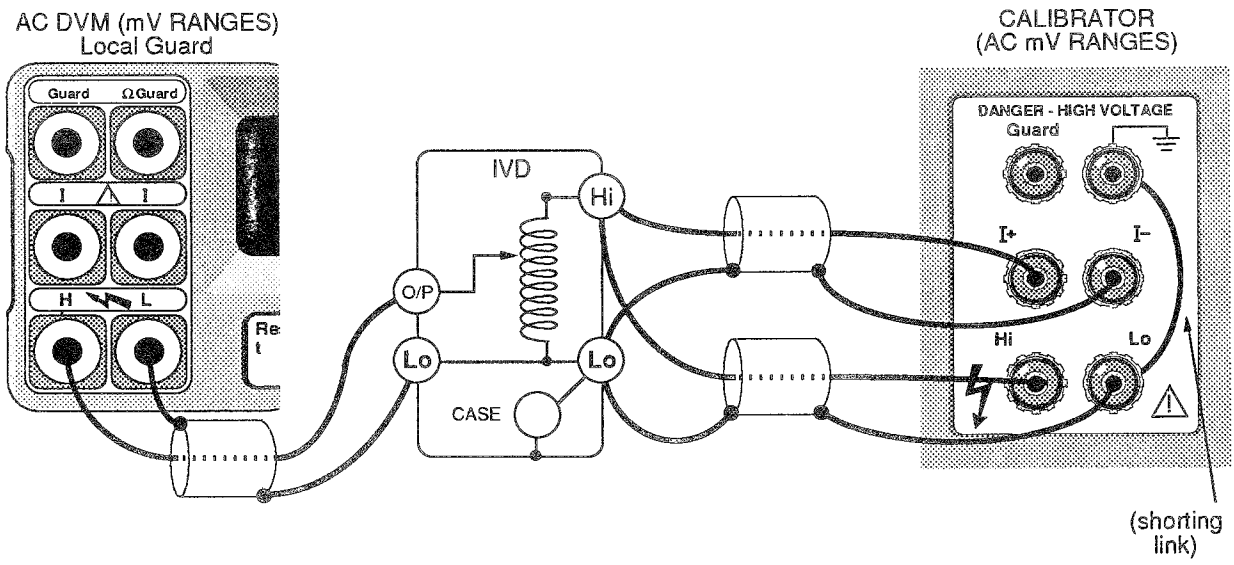
Switch on or reconnect the 10V reference Hi to Null detector.

h. 4808
Select STD, its LED lights. Press ON+ and Full Range OUTPUT (10.000000V).

j. Null Detector
Increase Null Detector sensitivity and use 4808 OUTPUT ◇ keys to adjust the reading to zero.

k. 4808
Press the CAL key: the STD LED goes OFF. Pre-cal is now completed. Select OUTPUT OFF and disconnect.

ACV LF Precal



ACV LF Precal Linearity Setup

Ensure the 4808 Output off LED is lit, cancel any MODE keys, select Remote Sense and deselect Remote Guard. Select ACV FUNCTION and connect the IVD to the instrument terminals as shown. Use short leads. Select the 1kHz Frequency Range.

10% Range

a. IVD
Select x1.0 ratio.

b. 4808
Select 10V range, at 1kHz on the 1kHz Frequency range. Select 1.000,00V. Press the ±0 key, its LED lights. Use instrument OUTPUT ◇ keys to adjust the DVM reading to 1V. Press CAL: the ±0 LED remains lit and 1.000,00V (nominal 10% Full Range) appears on the right-hand OUTPUT display.

Full Range

c. IVD
Select the x0.1 ratio to divide the 4808 output by 10.

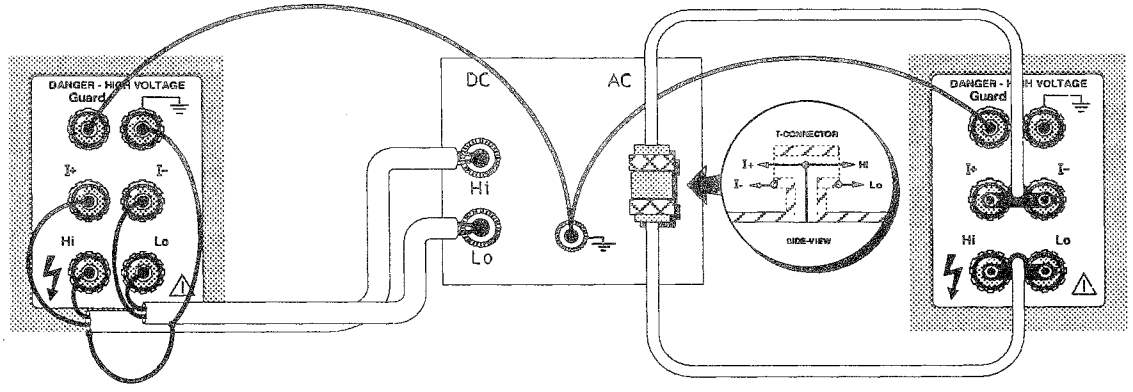
d. 4808
Select Full Range. Use instrument OUTPUT ◇ keys to adjust the DVM reading to 1V. Press the CAL key: the ±0 LED goes OFF. Recheck, without pre-selection, at 1V and 10V. If required repeat the procedure. Select OUTPUT OFF and disconnect. Pre-cal is now completed. Disable pre-cal and complete a Full Routine Calibration.

ACV HF Precal

DC Standard
Remote Sense and Remote Guard

Thermal Transfer

4808
Remote Sense and Remote Guard



ACV HF Precal Linearity Setup

With OUTPUT OFF, connect the 4808 and DC Voltage Standard to the Thermal Transfer AC and DC inputs, respectively.

10% Range

a. 4808
On AC function, select the 10V range, select the 1MHz frequency range and use the FREQUENCY ◇ keys to display 1MHz. Use the OUTPUT ◇ keys to output 1V and set OUTPUT ON. Press the SPOT key.

b. DC Voltage Standard
Set to 1V output and set OUTPUT ON.

c. Thermal Transfer Standard
Configure for DCV measurement at the 1V level and adjust for Null. Configure for ACV measurement at the 1V level.

d. 4808
Use the OUTPUT ◇ keys to adjust the OUTPUT display reading to obtain a null on the Thermal Transfer Standard. Press the CAL key.

Full Range

e. DC Voltage Standard
Set to 10V Output, select OUTPUT ON.

f. Thermal Transfer Standard
Configure for DCV measurement at the 10V level and adjust for Null. Configure for ACV measurement at the 10V level.

g. 4808
Press Full range key to display 10V and use the OUTPUT ◇ keys to obtain a null on the Thermal Transfer. Press the CAL key.

PRE-CAL DISABLE

When pre-calibration is complete the pre-cal enable switch must be set to RUN.

CAUTION: DO NOT press the internal push-button which clears the calibration memory. If this is done, any parameters stored in the calibration memory are cleared; so pre-calibration is cancelled, and must be repeated.

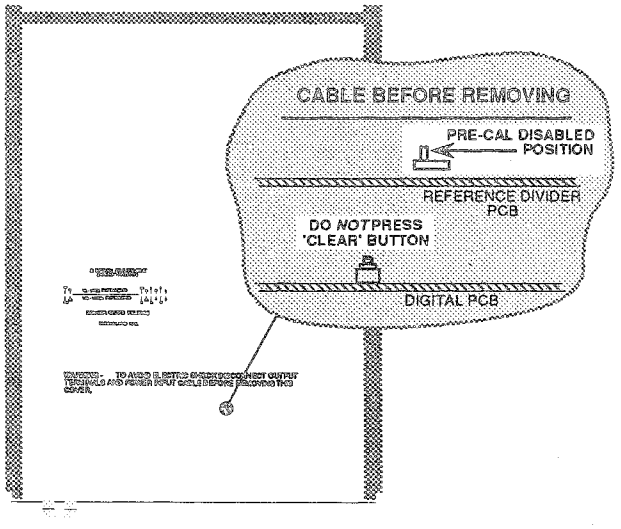
a. Lift the top cover at the front.

b. Locate the hole which gives access to the PRE-CAL ENABLE switch.

c. Insert an insulated tool in the hole Pre-cal and move the switch to the left (RUN). The legend 'cal' remains on the MODE display, but disappears from the OUTPUT display.

d. Refit and secure the top cover.

A Full Routine Calibration is necessary before completion of the Return to Use procedure on *page 1-3*.



1.4 INTERNAL OHMS ADJUSTMENT

Introduction

The Autocal procedure for routine calibration of the 4808's Resistance function is described in *Section 8 of the User's Handbook.*

The method of calibration is to measure the value of each standard resistor, and store the measured value in non-volatile calibration memory. Subsequently, each time a resistance RANGE is selected, the previously calibrated value is displayed.

If a standard resistor has been subjected to undue stress, its value may have moved outside its tolerance (signalled by an *Error 6* message during Routine Autocalibration). If the value is less than approx. 50ppm outside tolerance, it can be adjusted internally using a variable trimmer. For values out of tolerance in excess of 50ppm it is likely that the resistor has been over-stressed, in which case consult your Datron Service Centre.

Manual Trimming Procedure

The following procedure is a supplement to Routine Autocalibration. It is necessary only when the 4-wire calibration detailed in *Section 8 of the User's Handbook* has resulted in an *'Error 6'* message.

It can also be used when, for operational reasons, it is necessary to adjust a resistor to its nominal value. For this purpose a continuously-reading method of measurement is convenient.

a. Release eight screws retaining the top cover.

b. Lift the top cover at the front of the instrument and locate the 8 holes giving access for 'Ω OPTION ADJUSTMENT'.

c. Insert an insulated screw driver tool in the hole for the range selected, and adjust the preset resistor (rotating clockwise increases the resistance value).

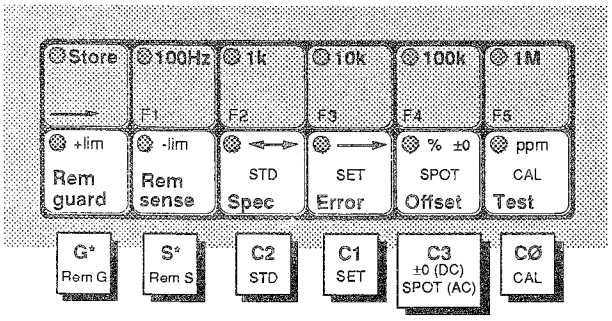
d. Re-measure the 4-wire value and repeat operation (c) until the desired value is obtained.

e. Re-calibrate the range for 4-wire and 2-wire connections as detailed in *Section 8 of the User's Handbook.*

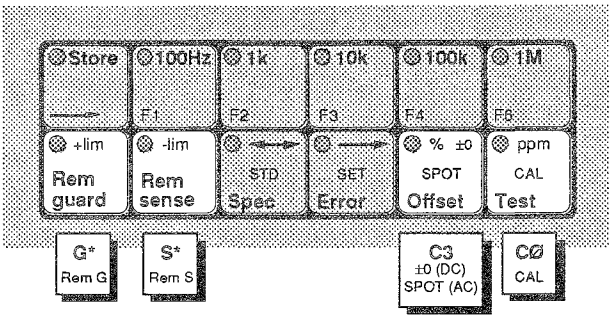
f. Repeat the manual trimming procedure above for all ranges as required.

g. Finally refit and secure the top cover using the eight screws removed in (a), above.

1.5 REMOTE PRE-CALIBRATION GUIDELINES



Transfer of DC pre-calibration facilities



Transfer of AC pre-calibration facilities

General Procedure

The transfer of Pre-calibration facilities to remote control is illustrated above. The general procedure follows that for remote Routine Calibration; the external circuit is connected as for manual pre-calibration.

These commands can only be activated when the following conditions have been fulfilled:

- The CALIBRATION ENABLE keyswitch on the instrument. Rear Panel must be set to ENABLE.
- Ensure that the IEEE address switch is set correctly.
- The IEEE Interface command-code W1 must have been received and activated.
- The internal PRE-CAL ENABLE switch is set to ENABLE.

When the 4808 is under remote control over the bus, the command code WØ overrides the setting of the CALIBRATION ENABLE and internal PRE-CAL ENABLE switches, disabling the 'C' codes.

Pre-Calibration Command Strings

The following command strings are given for the sole purpose of illustrating the methodology for the remote pre-calibration mode. Some reference to external operations is inferred. The nulling operation is separated into its own string, as it is likely to be iterative.

It is assumed that the external circuit is set up correctly.

The 4808 has already been programmed into its calibration mode by W1, with the CALIBRATION ENABLE keyswitch and the internal PRE-CAL ENABLE switch set to ENABLE.

The calibration memory stores have been cleared, and the 4808 Output is OFF.

The string sequence for DC pre-calibration is as follows:

1. ±Zero

FØR6M+ØO1C3=	(Set-up and ±0 preselection)
M***=	(Iterative nulling operation)
CØ=M-Ø=	('CAL' and -ON)
M***=	(Iterative nulling operation)
CØ=OØ=	('CAL' then OUTPUT OFF)

2. Coarse Gain and Linearity

FØR6C4M+19.999999O1=	(Set-up and linearity preselection)
M***=	(Iterative nulling operation)
CØ=OØ=	('CAL' then OUTPUT OFF)
C5=M+10.000000O1=	(Set-up and linearity preselection)
M***=	(Iterative nulling operation)
CØ=OØ=	('CAL' then OUTPUT OFF)

The string sequence for AC pre-calibration is as follows:

Full Range and 1/10th Range Linearity;
first for LF, and then for HF

F1R6H***C3O1=M***=	(Program to frequency and voltage)
M***=	(Iterative nulling operation)
CØ=M***=	(First 'CAL' of two-part process)
M***=	(Iterative nulling operation)
CØ=OØ	(Second 'CAL' cancels preselected mode)

Notes on the Use of the Null Detector

The Null Detector is normally connected in series with the 4808 Hi lead. A high-impedance-input device should be chosen to reduce off-null currents due to differences in the outputs of the DC voltage source and the 4808. A battery-operated instrument is preferred to ensure adequate isolation.

Some Null Detectors possess high input impedance only when their readings are on-scale, so care should be taken to ensure that drain currents from the DC Voltage source do not become excessive. This applies particularly if the DC source is a standard cell or a bank of cells.

Six points are important:

1. The null detector should be connected to the 4808 (or 4808 load resistor) only when the 4808 **Output off** LED is lit. (with output OFF, the I+, I-, Hi and Lo terminals are at high impedance).

2. Always set the null detector to its lowest sensitivity before connecting up, and increase sensitivity only when the voltages output by the DC Voltage source and the 4808 are close in value.

3. Do not change polarity of the 4808 or DC Voltage source without first switching the 4808 OUTPUT OFF. Care must be taken to ensure that the correct polarity on key is pressed, to avoid excessive voltages being connected across the null detector, particularly when checking the 4808 directly against a standard cell.

4. Most Null Detectors are equipped with a 'Self-zero' or 'Zero-check' facility. For maximum accuracy, the Null Detector range zero should be checked before each calibration nulling operation is performed. However, when gain-calibrating the 4808 Voltage and Current Ranges, the zero offset of the calibration voltage source is nullified by adjustment of the Null Detector zero control. This setting should not be altered until the corresponding Range gain has been calibrated.

5. **WARNING**
   During performance checks and calibration a common mode voltage equal to the full range voltage is present at the Null Detector input terminals. On 1000V checks this voltage is potentially lethal, so EXTREME CAUTION must be observed when making adjustments to the null detector sensitivity.

6. CAUTION
   The Null Detector used must be able to withstand voltages up to 1200V between its input terminals. Such voltages will be present during the time that the 4808 is ramping from zero to 1000V Full range after setting OUTPUT ON. Inadvertent disconnection of the Precision Divider terminals can transfer full output across the Null detector.

Calibration Source Zero Offsets

It is common practice to accept a small offset in the output of a voltage calibration standard, providing that the same offset is present at all output values, including zero.

A more difficult situation arises if there is a 'DC turnover offset' between the source's positive and negative output values. In this case, a difference in DC value will be observed when switching the source between its positive and negative outputs with zero volts selected. This type of error is normally adjusted out on the 4808 by a preliminary '±0' calibration on the 10V Range, to a null detected across its output terminals. This sets both ON+ and ON- zeros to the same DC level; and as the same linear analog circuitry is used to generate both output polarities, range calibration of zero and gain in positive polarity is then all that is required.

The 4808 analog circuitry is fully floating, so its output may be referred to any common mode voltage within the range specified in *Section 6.3 of the User's Handbook.* In particular, each Range zero may be aligned to absolute zero in Local Sense by calibration to a null across its Hi and Lo (Sense) terminals. But if it is then gain-calibrated against an offset source without re-zeroing to that source's offset zero, normal mode gain errors will result. It is therefore essential that any offset in the source's output be nullified before gain calibration is carried out. This can be done at Range zero, simply by trimming the Null Detector null.

The notional sequence of calibration for the 4808 should be as follows:

a. ±0
   Check that the 10V Range 'ON+' and 'ON-' zeros coincide at absolute zero (Adjust if necessary).

b. Range Zeros
   Carry out 'ON+' zero calibration on all Ranges against the same absolute zero.

c. Range Gain
   Each Range Gain in turn, (Null Detector connections as shown for Voltage or Current)
   i. At 'ON+' zero output from both source and 4808, trim the Null Detector for null.
   ii. At the required positive DC level, calibrate the 4808 Range gain.

This sequence ensures that the 4808 'ON+' and 'ON-' zeros are both set to absolute zero, and that both positive and negative polarities are accurately gain-calibrated to a unipolar source.

If it is required to check the 4808 'ON-' gain calibrations against a bipolar source, the source's 'ON-' zero offset must first be nullified, as described in (c. i.) opposite.

SECTION 2 FAULT DIAGNOSIS

WARNING
HAZARDOUS ELECTRICAL POTENTIALS ARE EXPOSED WHEN THE INSTRUMENT COVERS ARE REMOVED.
ELECTRIC SHOCK CAN KILL

CAUTION
The instrument warranty can be invalidated if damage is caused by unauthorised repairs or modifications. Check the warranty detailed in the "Terms and Conditions of Sale". It appears on the invoice for your instrument.

2.1 INTRODUCTION

2.1.1 Use of Diagnostic Guides

The diagnostic guides given in Section 2.2 are intended to aid the user in locating a failed printed circuit board or other assembly. The self-diagnostic capabilities of the instrument provide the first step in fault analysis by displaying a FAIL message on the left-hand MODE display. Initial actions to be taken after the occurence of a FAIL message are given, where applicable, in the diagnostic guides of Section 2.2. The FAIL message localizes the failure into a distinct functional area and the "Fault Condition" summary in each guide relates the function failure to a probable hardware boundary.

The identities of the assemblies involved in the failure are given beneath the fault condition summary, but it is unlikley that all assemblies listed will prove to be faulty. For successful failure analysis, it is advisable to be familiar with the electronic functioning of the instrument and with the physical location of the assemblies. To assist in these aspects, the diagnostic guides include references to relevant parts of this publication.

2.1.2 Effects of Protective Measures on Diagnosis

2.1.2.1 Protective Suppression of Fault Conditions

The 4808 incorporates built-in protection in hardware and software. To minimize damage, protective circuitry acts immediately, backed up by a pre-programed CPU response to detected failure symptoms. If possible the CPU informs the user by presenting a failure message on the MODE display.

When investigating a failure, it should therefore be anticipated that protective measures will have suppressed the original fault conditions. A useful starting-point is to identify the origin of the failure message to localize the area of search.

2.1.2.2 FAIL 5 as Default State

Faults which result in display messages FAIL 2, 3 or 4 can pose a safety hazard to the operator, and apply excessive voltage to external circuitry. To protect against this, the instrument is programmed to default to FAIL 5 state as rapidly as possible after its initial response to the failure symptoms. The CPU switches Output OFF and trips the safety monitor (Watchdog). If the conditions of the original failure message have been removed the display changes to FAIL 5.

In normal use, an operator will probably notice only FAIL 5, and miss the original failure message. In FAIL 5 state, front panel control is inhibited until **Reset** is pressed. This returns the instrument to the state for which the original fault conditions and failure message were produced, but with Output OFF.

2.1.2.3 To Observe the Original Failure Message

Two procedures can be used:

a. Carry out the self-test routine of Section 2.3.
The failure message may recur during this test.

b. Reset the instrument to reproduce the fault, carefully watching the MODE display.
The original failure message could reappear momentarily, prior to defaulting into FAIL 5.

Then select the appropriate diagnostic guide in Section 2.2.

2.1.3 FAIL 6

FAIL 6 reports two types of NV RAM failure.

a. Overall sumcheck failure.
Sumcheck values are calculated at Power on, Self-Test and recovery from FAIL. If the instruments stored calibration constants are outside maximum or minimum permissible values a Fail 6 message is displayed.

b. Limits check of the calibration constants.
Values are checked when read from the NV RAM at every OUTPUT change. When a Fail 6 occurs the output remains on and the stored gain or zero correction value is defaulted to x1 or x0 respectively.

2.2 DIAGNOSTIC GUIDES

2.2.1 *FAIL 1* (Excessive Internal Temperature)

INITIAL ACTION

1. Wait approximately 1 minute until the CPU has defaulted the instrument to OUTPUT OFF. The CPU clears the FAIL 1 message and enables the keyboard.
2. Switch OUTPUT ON.
3. No failure display - no further action. FAIL 1 recurs - fault persists.

FAULT CONDITION

High temperature sensed in:

- Positive Heatsink Assembly, or
- Negative Heatsink Assembly.

Fault indication signal OVERTEMP active.

POSSIBLE FAULT LOCATIONS

- Positive Heatsink Assembly *(page 11.13-1)*.
- Negative Heatsink Assembly *(page 11.13-2)*.
- Power Amplifier Assembly *(page 11.9-1)*.

FURTHER INFORMATION IN THIS HANDBOOK

Technical Descriptions: *Section 7.12.9*.

2.2.2 *FAIL 2* (Over-Voltage)

INITIAL ACTION

1. Ensure that OUTPUT is OFF
   (4808 should have tripped to FAIL 5).
2. Power OFF any external voltage source.

N.B. This failure can be caused by injection of an *external* voltage across the terminals OR the output of high voltage when not requested by the user.

DC - voltages in excess of 130V.

AC - voltages between the limits of 75V to 110V RMS.

2. Disconnect external leads from the terminals.
3. Press Reset.
4. Carry out self-test sequence.
5. FAIL 2 recurs - fault persists.
6. No failure display - Reproduce original conditions in Local Sense with no external connections.
7. No failure display - check external circuit and proceed with careful use.
8. FAIL 2 recurs - fault persists.

FAULT CONDITION

1. Over voltage circuit on the DC Assembly has detected the excess voltage between PHi and PLo lines and has activated HV ST signal to the CPU, and
2. The CPU has recognized that the instrument is not in High Voltage State, so has generated FAIL 2 display, then
3. The CPU has switched Output OFF, tripped the watchdog and generated FAIL 5 display.

POSSIBLE FAULT LOCATIONS

- Injection of external voltage.
- D.C Assembly *(page 11.5-1)*.
- Power Amplifier Assembly *(page 11.9-1)*.

FURTHER INFORMATION IN THIS HANDBOOK

Self-test procedure: *Section 2.3*.

Technical descriptions: *Section 7.3.7*.

2.2.3 *FAIL 3* (Control Data Corrupted)

INITIAL ACTION

No immediate action required.

FAULT CONDITION

1. Control data corrupted.
2. CPU has detected errors in serial transfer of data between out-guard and in-guard circuits, and generated FAIL 3 display, then
3. The CPU has switched Output OFF, tripped the watchdog and generated FAIL 5 display.

POSSIBLE FAULT LOCATIONS

- Reference Divider Assembly *(page 11.4-1)*.
- Analog Interface Assembly *(page 11.3-1)*.

FURTHER INFORMATION IN THIS HANDBOOK

Technical descriptions: *Section 6.4*.

2.2.4 *FAIL 4* (Precision Divider Fault)

INITIAL ACTION

No immediate action required.

FAULT CONDITION

1. Precision divider fault.
2. CPU has detected errors in the most-significant data bits set in the precision divider input data latches, and generated FAIL 4 display, then
3. The CPU has switched Output OFF, tripped the watchdog and generated FAIL 5 display.

POSSIBLE FAULT LOCATION

- Analog Interface Assembly *(page 11.3-1)*.

FURTHER INFORMATION IN THIS HANDBOOK

Technical description: *Section 6.5.2.3*.

2.2.5 *FAIL 5* (Safety Circuits 'Watchdog' Tripped)

INITIAL ACTION

Use the checking sequence below, watching the MODE display carefully at each stage to detect any FAIL number appearing immediately before FAIL 5. If no failure message occurs, carry on to the next stage.

Stage 1: Press Reset.

Stage 2: Carry out self-test sequence (Section 2.3).

Stage 3: Set Output ON.

Stage 4: Proceed with careful use.

If FAIL 2 occurs at stage 3, ensure that it is not due to injection of an exessive external voltage by disconnecting the instrument terminals and repeating the checks. If FAIL 5 alone occurs, proceed to "Fault Condition" below. For any FAIL other than FAIL 5, transfer to the diagnostic guide for that message.

FAULT CONDITION

18mS monostable (M10 in reference divider) has been deprived of at least two trigger pulses and has timed out, activating "BARK" and "BARK DELAYED" (BARK +47mS) signals from M13 in the reference divider assembly.

Summary of "BARK" effects:

1. Removes the drive from the High Voltage (1kV) transformer.
2. Disables the 400V Power Supply.
3. BARK status message sent to CPU signalling a failure.
4. CPU starts controlled shut-down.

Summary of "BARK DELAYED" effects:

1. Disconnects the voltage Power and Sense circuits from the instrument output terminals.
2. BARK DELAYED disables the registers of the serial/parallel data converters.
3. Outputs from control latches in the reference divider pcb are disabled by setting into "Tristate". Each output line has a pull-up or pull-down resistor which sets the analog circuitry into a safe condition.

POSSIBLE FAULT LOCATIONS

- Digital Assembly (No gated WRT STRB pulses at J2/J3-29) *(page 11.2-2)*.
- Analog Interface Assembly (No SSDA strobe pulses; or Watchdog disabled) *(page 11.3-3)*.
- Reference Divider Assembly (Incorrect functioning of Watchdog setup circuitry) *(page 11.4-5)*.

N.B. The Watchdog is designed primarily to ensure that CPU malfunctions do not set up dangerous conditions in the analog circuitry.

FURTHER INFORMATION IN THIS HANDBOOK

Technical description: *Section 6.4*.

2.2.6 *FAIL 6* (Calibration Memory Fault)

INITIAL ACTION

1. Select Output OFF, Spec OFF, Error OFF.
2. Perform self-test sequence (Section 2.3) or select Output ON at the requested value.
3. No failure display - no further action.
4. FAIL 6 recurs - recalibration required.
5. Select Cal *(refer to Section 1)*.
6. Recalibrate *(refer to Section 1)*.
7. Calibration failure - fault persists.

FAULT CONDITION

Calibration memory fault on Digital pcb assembly.

POSSIBLE FAULT LOCATION

- Digital Assembly *(page 11.2-3)*

FURTHER INFORMATION IN THIS HANDBOOK

Self-test procedures: *Section 2.3*.

Calibration procedures: *Section 1*.

Technical descriptions: *Section 6.1*.

2.2.7 *FAIL 7* (P.A. 400V Power Failure)

INITIAL ACTION

1. Switch power OFF.
2. Check line supply is correct for input voltage setting.
3. Switch power ON - no failure display - no further action.
4. FAIL 7 recurs - fault persists.

FAULT CONDITION

- Positive or Negative 400V power supply failure
- Fault indication signal 400V(2) FAIL active
- Check line input voltage

POSSIBLE FAULT LOCATIONS

- Power Amplifier Assembly *(page 11.9-1)*.
- Reference Divider Assembly *(page 11.4-1)*.
- Positive Heatsink Assembly *(page 11.13-1)*.
- Negative Heatsink Assembly *(page 11.13-2)*.
- Power Supply/Current Heatsink Assembly *(page 11.13-3)*.
- Mother Board *(page 11.16-1)*.

FURTHER INFORMATION IN THIS HANDBOOK

Technical descriptions: *Sections 6.7*.

2.2.8 *FAIL 8* (P.A. 38V Power Failure)

INITIAL ACTION

1. Switch power OFF.
2. Check line supply is correct for input voltage setting.
3. Switch power on - no failure display - no further action.
4. FAIL 8 recurs - fault persists.

FAULT CONDITION

- Positive or Negative 38V power supply failure.
- Fault indication signal 38V(2) FAIL active.
- Check line input voltage.
- It is possible for a misleading FAIL 8 message to occur, caused by a logic supply failure, in particular -15 Volts. The FAIL 9 message will have been displayed momentarily. Refer for fault location and further information to FAIL 9.

POSSIBLE FAULT LOCATIONS

- Power Amplifier Assembly *(page 11.9-1)*.
- Reference Divider Assembly *(page 11.4-1)*.
- Power Supplies *(page 11.12-1)*.
- Mother Board *(page 11.16-1)*.

FURTHER INFORMATION IN THIS HANDBOOK

Technical descriptions: *Section 6.7*.

2.2.9 *FAIL 9* (P.A. 15V Power Failure)

INITIAL ACTION

1. Switch power OFF.
2. Check line supply is correct for input voltage setting.
3. Switch power on - no failure display - no further action.
4. FAIL 9 recurs - fault persists.

FAULT CONDITION

- Positive or Negative 15V power supply failure. This is indicated by a transitory Fail 9 followed by Fail 8.
- Fault indication signal 15V(2) FAIL active.
- Also 400V power supply is disabled.
- Check line input voltage.

POSSIBLE FAULT LOCATIONS

- Power Amplifier Assembly *(page 11.9-1)*.
- Reference Divider Assembly *(page 11.4-1)*.
- Power Supplies *(page 11.11-1)*.

FURTHER INFORMATION IN THIS HANDBOOK

Technical descriptions: *Section 6.7*.

2.2.10 *Error EF* (External Frequency selected but not detected)

INITIAL ACTION

- If External Frequency Lock is not required:

  Ensure external frequency selection switch (S53) is set to OFF.

- If External Frequency Lock reference is required:

  1. Ensure reference frequency is available at Rear Panel connector J53.
  2. Ensure Rear Panel switch S53 is set to ON.

FAULT CONDITION

- The external reference signal detector has set 'EXT REF ST' to Logic Ø.

POSSIBLE FAULT LOCATIONS

- External circuit.
- Interconnection Assembly *(page 11.17-2)*.
- Mother Assembly *(page 11.16-4)*.
- Analog Interface Assembly *(page 11.3-4)*.

FURTHER INFORMATION IN THIS HANDBOOK

Technical descriptions:

External Frequency Lock: Section 8.3.

2.3.3 Stage 2 *(Fig. 2.2)*

Stage 2 of the self-test sequence is entered when the Test key is pressed AFTER the completion of Stage 1 and BEFORE any other key.

The keyboard LED indicators are lit in a sequence which proceeds from left to right along the rows of keys, while the Test LED remains lit.

The next tests in the sequence require operator participation in order to check key functioning. Operation of the ◇, Full Range and Zero keys is shown by a symbol on the display immediately above or close to the appropriate key. Operation of FREQUENCY RANGE, MODE, RANGE, FUNCTION and OUTPUT control keys is shown by the appropriate key's LED. In these tests the display or LED remains lit until another key is pressed.

At any part of Stage 2, pressing the Test key will end the test and cancel the Test LED.

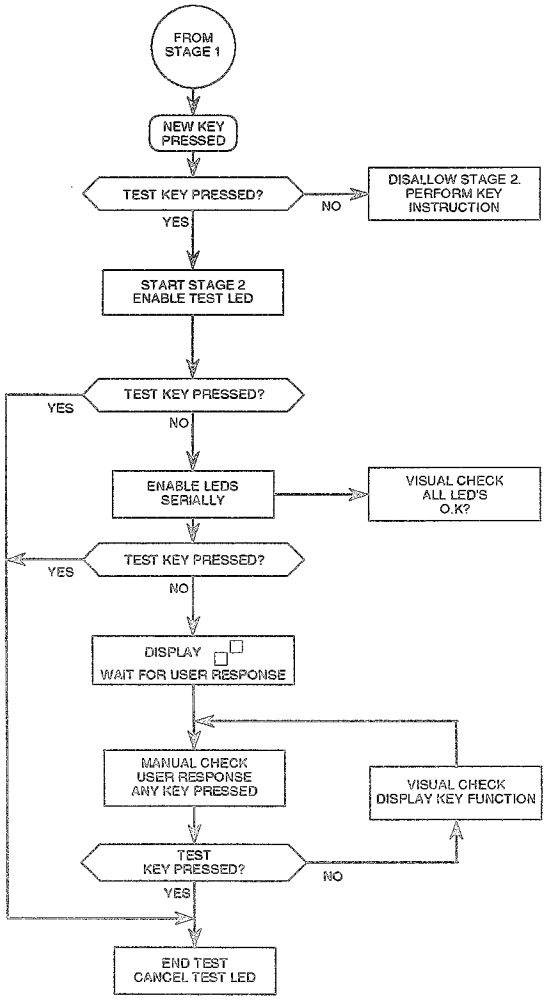


FIG. 2.2 SELF TEST SEQUENCE STAGE 2

2.4 FUSE PROTECTION

In addition to the electronic protection devices used in the instrument, fuses protect against catastrophic component failure.

2.4.1 Fuse Replacement

A blown fuse is merely a symptom of failure, in the large majority of cases the cause lies elsewhere.

CAUTION

Every occurrence of a blown fuse should be investigated to find the cause. Only when satisfied that the cause is known, and has been removed, should a user replace a fused link by a serviceable item.

2.4.2 Reasons For Fusing

The fuses in the calibrator fall into two groups:

a. Clip-in anti-surge fuses in the Power Supplies and Mother Board protect the power source from damage.

b. Soldered-in fuses are used in some locations to ensure that the printed circuit tracks are protected in the unlikely event of extreme failure conditions.

2.4.3 Locating a Blown Fuse

The ultimate causes of blown fuses are so extensive that it is impractical to list them. In many cases the underlying cause, or the blown fuse itself, will activate an electronic protective process which can conceal some of the symptoms.

Fault location in the Calibrator should proceed from the primary indications of fault condition (e.g. failure messages described in *Section 2.2*). These will lead to particular areas of investigation, and at this point the relevant circuit fuses should be checked first. Whether fuses are blown or not, the checks will add to the information available for further diagnosis.

Table 2.1 (overleaf) lists fuse locations. The table is indexed in Circuit Diagram page order, giving fuse values. The types of fuses to be used can be found in the component lists of *Section 12*.

LOCATION AND DESIGNATOR	VALUE/FITTING	PROTECTED CIRCUITS	*Page*
DC Assembly			
F1	1A/Solder-in	DC 10V, 100V & 1kV Error	*11.5-1*
F2	250mA/Solder-in	SHI(DCV)	*11.5-2*
F3	1A/Solder-in	Power Lo/Guard	*11.5-2*
F4	1A/Solder-in	Power Lo	*11.5-2*
F5	1A/Solder-in	DC 1kv	*11.5-1*
F6	1A/Solder-in	PHI(V)	*11.5-2*
AC Assembly			
F1	1A/Solder-in	1V range only & Current ranges up to 10mA	*11.7-1*
F2	1A/Solder-in	All AC Voltage ranges (PHI(ACV))	*11.7-1*
I/Ω Assembly			
F1 Not used	- - -	- - -	- - -
F2	375mA/Solder-in	PLO(Ohms)	*11.8-3*
F3	1A/Solder-in	SLO(Ohms)	*11.8-3*
F4	375mA/Solder-in	PHI(Ohms)	*11.8-3*
F5	2.5A/Solder-in	All Current/Ohms Outputs	*11.8-1*
Power Supply (OG)			
F101	4A/Clip-in	Digital and Display supplies	*11.10-1*
Power Supply (IG)			
F1	4A/Clip-in	Supplies -22V(2)	*11.11-1*
F2	4A/Clip-in	Supplies +22V(2)	*11.11-1*
F3	3.15A/Clip-in	Supplies +15V(2)	*11.11-1*
F4	3.15A/Clip-in	Supplies -10V(2), -15V(2)	*11.11-1*
F5	1A/Clip-in	Supplies -8V(2)	*11.11-2*
F6	1A/Clip-in	Supplies +8V(2)	*11.11-2*
Power Supply (38V)			
F1	1A/Solder-in	-38V Supply Line	*11.12-1*
F2	1A/Solder-in	+38V Supply Line	*11.12-1*
Mother Board			
F1	1A/Clip-in	Transformer secondary to 400V PSU	*11.16-5*
F2	1A/Clip-in	Transformer secondary to 400V PSU	*11.16-5*
F3	2.5A/Solder-in	Transformer secondary to 38V PSU	*11.16-5*
F4	2.5A/Solder-in	Transformer secondary to 38V PSU	*11.16-5*
Power Input Module			
220/240V	3A/Clip-in	All circuits	*11.17-2*
100/120V	6.25A/Clip-in	All circuits	*11.17-2*

TABLE 2.1 FUSE LOCATION AND PURPOSE

SECTION 3 DISMANTLING AND REASSEMBLY

3.1. GENERAL PRECAUTIONS

3.1.1 WARNINGS

1. ISOLATE THE INSTRUMENT FROM POWER SUPPLIES BEFORE DISMANTLING OR REASSEMBLING.
2. THE COMBINED REMOVAL OF TOP AND BOTTOM COVERS, GROUND/GUARD ASSEMBLIES AND REAR PANEL ASSEMBLY; LEAVES THE MOULDED INTERNAL CHASSIS UNSUPPORTED. THIS CAN CONSTITUTE A SAFETY HAZARD TO BOTH PERSONNEL AND EQUIPMENT.

3.1.2 CAUTIONS

1. Removal of the Top Ground/Guard Assembly invalidates the manufacturers calibration certification.
2. Handle the instrument carefully, especially when inverted, to avoid shaking printed circuit boards loose.
3. Do not touch the pcb edge connectors.
4. Ensure that no wires are trapped when fitting ground/guard assemblies.
5. Ensure that washers, nuts etc. do not fall into the instrument, and are correctly refitted at subsequent reassembly.

3.2 General Mechanical Layout *(page 11.0-1 and 11.18-1 to 11.18-7)*

All circuits are housed within a single unit on printed circuit board assemblies, the eight major PCBs being plugged into a "Mother" PCB assembly.

The 4808 AUTOCAL STANDARD can be used as a bench-top instrument, or it may be rack mounted in a standard 19" rack.

3.2.1 Front Panel

Six output terminals with captive, insulated caps are provided on the front panel. The front panel also retains polarizing filters for the displays.

3.2.2 Rear Panel

The recessed Power Input plug, Power Fuses and Line Voltage Selector are contained in an integral filter module at the centre of the rear panel.

The Calibration Enable switch (with removable key), and the External Frequency Input BNC socket (J53) are mounted directly on the panel between the Power Input module and the cooling-air intake filter.

The intake filter is retained by a grille but is removable for cleaning. At the extreme left of the panel, an extractor fan draws cooling air through the filter and internal heat exchangers, discharging to atmosphere.

The IEEE 488 standard connector socket (J27) with instrument address switch, the Calibration Interval Switch and the external frequency switch (S53) are all mounted on the Interconnection PCB assembly. This is fitted on spacers to the inside face of the panel with external components protruding to the rear. Socket J54 is provided to facilitate future expansion.

3.3 LOCATION AND ACCESS

3.3.1 External Construction

Rigid side extrusions, together with the front and rear panel assemblies, form the basic chassis of the instrument. The side extrusions have handles and rear spacers fitted for bench-top use, or are fitted with 'ears' and slides for rack mounting (*see User's Handbook, Section 2*).

The top cover locates into the side extrusions and is secured by screws. The bottom cover is attached in the same way, and includes six domed feet. An operator's instruction card pulls forward from below.

3.3.2 Internal Construction

The chassis is enclosed top and bottom by ground and guard screens. The upper ground and guard screens allow most internal adjustments to be performed without removal. Locations of adjustable components, instructions and warnings are printed on its upper surface.

The interior of the chassis is divided into two compartments. A thermally-enclosed compartment occupies the forward half of the chassis, and is used to house the low power, precision printed circuit board assemblies.

The rear compartment contains high power components, is air-cooled and further subdivided. One section is positioned across the intake airflow, housing the In-guard and Out-guard Power Supply assemblies and providing anchorage for the Mains (Line) Transformer assembly. The other section houses three Heatsink assemblies, provides anchorage for the LF Transformer assembly, High Voltage assembly and 38V Power Supply assembly.

Filtered air passes over the power supplies, mixes with air in the rear compartment, is drawn through the heatsink assemblies, and is finally expelled from the instrument by the extractor fan.

Guard screens are provided against the outer walls of the power supply sub-compartment and the heatsink compartment.

Interconnections between the Power Amplifier assembly, all forward-compartment assemblies, and the Front assembly are made via a Mother PCB. The latter fits across the bottom of the forward compartment, extending at the front to the Front assembly and at the rear to the 38V Power Supply. Four moulded stiffeners keep the mother pcb rigid, also providing lateral locating slots for printed circuit boards and guard screens.

The main printed circuit boards in the forward compartment fit across the full width of the instrument chassis. They slide into vertical slots cut into the moulded chassis, their PCB edge-connection fingers making electrical contacts with sockets mounted on the Mother Assembly. Interleaved between the assemblies are screening shields. These are also guided by slots, and make similar electrical contact.

The Power Amplifier assembly PCB slots in behind the forward compartment across the full width. It connects to the Mother PCB in the same way, but has additional discrete electrical connections for the high power lines.

Each PCB is identified by the color of its ejector lever. The color name is coded at its correct location on the top of the internal moulded chassis (refer to *Table 3.1*). Also, each assembly's edge connector is uniquely configured to prevent incorrect fitting.

The Front PCB assembly, carrying the display components, connects into the front end of the mother PCB outside the thermally-insulated compartment.

3.4 GENERAL ACCESS

- ENSURE THAT POWER IS OFF.
- Heed the General Precautions 3.1.1 & 3.1.2.

If, during a procedure, sufficient access has been obtained then no further dismantling is required.

3.4.1 TOP COVER
(page 11.18-1)

- Removal

a. Remove the eight M4 x 12mm socket head countersunk screws from cover.

b. Remove cover by lifting at the front.

- Fitting

Locate cover at rear first, then reverse the removal procedure.

3.4.2 BOTTOM COVER
(page 11.18-1)

- Removal

a. Invert the instrument.

b. Remove the eight M4 x 12mm socket head countersunk screws from cover.

c. Remove cover by lifting at the front.

- Fitting

Locate cover at rear first, then reverse the removal procedure.

3.4.3 FRONT PANEL
(page 11.18-6)

Remove covers *(paras 3.4.1 and 3.4.2)*.

- Removal

a. Remove the four M4 x 6mm screws from the side-walls of the front panel.

b. Ease the front panel forwards and disconnect the ribbon cable which connectsto the switch pc board and power switch.

c. Remove the Front Panel.

- Fitting

Reverse the removal procedure, referring to *page 11.18-4*.

3.4.4 TOP GROUND/GUARD SHEET
(page 11.18-3)

- Removal of the Top ground/guard shield involves breaking Datron's calibration seal and renders manufacturer's calibration invalid.
- Instrument cooling air-flow adversly affected. Internal temperature rise triggers Fail 1. Power OFF and allow to cool as required.
- Remove the top cover *(para. 3.4.1)*.

- **Removal**

a. Refer to *page 11.18-3* and remove:

1. ten M4 x 8mm pozi-countersunk screws;
2. six M3 x 6mm pozi-pan screws and M3 shakeproof washers;
3. one M3 x 12mm pozi-pan screw and M3 shakeproof washer.

b. Remove the top ground/guard assembly.

- **Fitting**

Reverse the removal procedure.

3.4.5 BOTTOM GROUND SHEET
(page 11.18-2 detail 8)

Invert the instrument
Remove the bottom cover *(para. 3.4.2)*.

- **Removal**

a. Refer to *page 11.18-2 detail 8* and remove:

1. ten M4 x 8mm pozi-countersunk screws;
2. six M3 x 6mm pozi-pan screws and M3 shakeproof washers;

b. Remove the bottom ground sheet assembly.

- **Fitting**

Reverse the removal procedure.

3.4.6 BOTTOM GUARD PLATE
(page 11.18-2 detail 7)

- Invert the instrument. Remove the bottom cover *(para. 3.4.2)*. Remove the bottom ground sheet assembly *(para. 3.4.5)*.

- **Removal**

a. Refer to *page 11.18-2 detail 7* and remove ten M3 x 6mm pozi-countersunk screws.

b. Remove the bottom guard plate.

- **Fitting**

Reverse the removal procedure ensuring that no wiring is strained or trapped.

3.5. REMOVAL AND FITTING

Note:
Do not remove the Top Ground/Guard sheet if only selecting pre-cal, erasing cal memory, or removing Instruction Card or Rear Panel.

In addition to the following location instructions, refer to the Reference Handbook *page 11.0-1*.

Assembly	Access Required (Heed Caution 3.1)	Location (Page Detail in bracket)	Ejector Color	Section
Instruction Card	-	11.18-1	-	3.5.1
Front Bezel and Switch Assembly	3.4.5	11.18-6	-	3.5.2
Display Assembly	3.4.5	11.18-4	-	3.5.3
Digital Analog Interface Reference Divider Output Control Sine Source AC Current (OR Current Link pcb)	3.4.4	Chassis Identifier Code: BLK BRN RED ORG YEL GRN BLU BLU	BLACK BROWN RED ORANGE YELLOW GREEN BLUE BLUE	3.5.4
Common Guard and Ground Screens	3.4.4	11.18-2 and 11.18-3	-	3.5.5
Power Amplifier	3.4.4	11.18-2 (4) VLT	VIOLET	3.5.6
Power Supplies Out-Guard In-Guard ±38V	3.4.4	11.18-2 (1) 11.18-2 (2) 11.18-2 (5)	- - -	3.5.7 3.5.8 3.5.9
Heatsinks	3.4.4	11.18-2 (4)	-	3.5.10
High Voltage	3.4.4	11.18-2 (5)	-	3.5.11
Transformers Mains (Line) HF LF	3.4.4	11.18-5 (9) 11.18-4 (6) 11.18-5 (10)	- - -	3.5.12 3.5.13 3.5.14
Mother Board	-	11.18-4 (3)	-	-
Interconnections	3.5.28	11.18-7 (15)	-	-
Terminal Board	3.4.3	11.18-5 (8)	-	3.5.15
Rear Panel	-	11.18-4 (6)	-	3.5.16
Instrument Assembly	-	-	-	-

TABLE 3.1 INTERNAL LOCATION AND ACCESS

3.5.1 INSTRUCTION CARD

(page 11.18-3)

- **Removal**

a. Pull the instruction card forward to its fullest extent.

b. Bow the card and release the rear lugs from the slots.

- **Fitting**

c. Reverse the removal procedure.

3.5.2 SWITCH PCB ASSEMBLY

(page 11.18-6 detail 12)

Remove Front Panel *(para. 3.4.5)*

- **Removal**

a. Remove the eighteen M3 x 6mm pozi-pan screws and wavy washers which secure the switch pcb assembly to the front bezel.

- **Fitting**

Reverse the removal procedure.

3.5.3 DISPLAY ASSEMBLY

(page 11.18-4 detail 6)

Remove Front Panel *(para. 3.4.5)*

- **Removal**

a. Remove the five M3 x 6mm pozi-pan screws and wavy washers and the two M3 x 12mm pozi-pan scews and wavy washers which secure the display assembly to the chassis assembly.

b. Ease the lower edge of the display assembly PCB away from the Mother PCB, to disengage the mating connectors.

c. Remove the assembly.

- **Fitting**

Reverse the removal procedure. Ensure all mating connectors are full engaged and that the surfaces of displays are clean.

3.5.4 MAJOR PCB ASSEMBLIES

- ENSURE THAT THE INSTRUMENT POWER IS OFF.

- **Removal**

a. Identify the PCB assembly to be removed (see *Table 3.1*)

Note (operations b to d):
The I/Ω's Link PCB has only one ejector. To remove, grip the top edge and pull gently while levering the ejector upwards and outwards.

b. Place the thumb of each hand under the lip of the two ejectors on the PCB assembly to be removed.

c. Gently lever the ejectors upwards and outwards to release the edge connectors.

d. Remove the assembly.

- **Fitting**

a. Identify the chassis location of the PCB assembly to be fitted (See *Table 3.1 and page 11.0-1*).

Note:
The single ejector of the I/Ω's Link PCB locates to the 'BLU' identifier of the chassis.

b. Ensure the ejectors are in the 'down' position.

c. Insert the PCB edges into the identified slots in the side walls of the chassis.

d. Allow the PCB to slide down to the Mother PCB, then press home by gently pushing down on the ejectors.

3.5.5 COMMON, GUARD AND GROUND SCREENS

(page 11.18-2 and 11.18-3)

- The first screen (counting from front to back) is the Ground Screen and has two securing screws. Of the six remaining screens the first five are aluminium, single screw and interchangable. The rearmost screen is steel and not interchangable. Each plate mates with a miniature connector on the Mother PCB adjacent to the side wall of the chassis.

- Removal

a. Remove any adjacent assemblies to obtain access.

b. Undo securing screw(s).

c. Grip the plate and lift out from the chassis.

- Fitting

a. Insert the plate into the correct slots in the side walls of the chassis (ensure correct orientation).

b. Allow the plate to slide down to the Mother PCB, then gently press home.

c. Secure with a 3 x 6mm Pozi-screw and shakeproof washer (two for the ground screen).

d. Replace assemblies removed for access.

3.5.6 POWER AMPLIFIER ASSEMBLY

(page 11.18-2 detail 4)

- Do not pull on the connector wires. Some resistance to movement will be felt from the locking clips of the connector bases.

- Removal

a. Disconnect the five connectors from the assembly as shown on *page 11.18-1 detail 4*.

b. Fold back the connectors and wires clear of the assembly.

c. Place the thumb of each hand under the lip of the two ejectors.

d. Gently lever the ejectors upwards and outwards to release the edge connectors.

e. Remove the assembly.

- Fitting

a. Ensure that all wires and connectors are clear of the PCB area.

b. Insert the PCB edges into their respective slots in the side walls of the chassis; component side facing the rear of the instrument.

c. Allow the assembly to slide down to the Mother PCB taking care not to trap any wires.

d. Ensure the ejectors are in the 'down' position then press the assembly home by gently pushing down on the ejectors.

e. Identify and fit the five connectors J1 to J5, as shown on *page 11.18-1 detail 4*.

3.5.7 OUT-GUARD POWER SUPPLY
(page 11.18-2 detail 1)

- Do not pull on the connector wires. Some resistance to movement will be felt from the locking clips of the connector bases.

- **Removal**

a. Disconnect J1, J2 and J3 from the In-Guard Power Supply Assembly *(page 11.18-2 detail 2)*.

b. Disconnect the connectors J5 and J31/32 from the PCB.

c. Fold back the connectors and wires clear of the assembly.

d. Grip the top edge of the PCB and lift gently from the chassis.

e. Remove the assembly.

- **Fitting**

a. Ensure that all wires and connectors are clear of the PCB area.

b. Insert the PCB edges into their respective slots in the chassis sub-compartment.

c. Allow the assembly to slide down to the miniature connectors on the chassis, taking care not to trap any wires.

d. Fit the J3 connector to the assembly.

e. Press the assembly home by gently pushing down on the top edge of the PCB.

f. Fit J1, J2 and J3 to the In-Guard Power Supply Assembly.

3.5.8 IN-GUARD POWER SUPPLY ASSEMBLY
(page 11.18-2 detail 2)

- Do not pull on the connector wires. Some resistance to movement will be felt from the locking clips of the connector bases.
- The Out-Guard Power Supplies components can obstruct the removal of the In-Guard Power Supply. Remove Out-Guard Power Supply Assembly *(para 3.5.7)*

- **Removal**

a. Disconnect the three connectors J1, J2 and J3 from the PCB.

b. Fold back the connectors and wires clear of the assembly.

c. Grip the top edge of the PCB and lift gently from the chassis.

d. Remove the assembly.

- **Fitting**

a. Ensure all wires and connectors are clear of the PCB area.

b. Insert the PCB edges into the respective slots in the chassis sub-compartment.

c. Allow the assembly to slide down to the miniature connectors on the chassis, taking care not to trap any wires.

d. Press the assembly home by gently pushing the top edge of the PCB.

e. Fit the Out-Guard Power Supply *(para. 3.5.7)*

f. Identify and fit the three connectors J1, J2 and J3 as shown on *page 11.18-2 detail 2*.

3.5.9 38V POWER SUPPLY
(page 11.18-2 detail 5)

Heed the General Precautions 3.1.

- **Removal**

a. Grip the edges of the pcb and pull the assembly vertically upwards. Some resistance will be felt from the edge connector.

- **Fitting**

a. Locate the assembly into the guides

b. Apply downward pressure until the connector is felt to have engaged.

3.5.10 HEATSINK ASSEMBLIES
(page 11.18-2 detail 4)

- Heed the Warnings and Cautions *3.1.1 & 3.1.2*. Allow heatsinks to cool before handling. Do not pull on the connector wires. When disconnecting connectors, some resistance to movement will be felt from the locking clips of the connector bases.
- Although the heatsink assemblies are discrete items, removal is simplified when performed in the following order:
  1. Negative Heatsink assembly. 2. Positive Heatsink assembly. 3. Power Supply / Current Heatsink assembly.

- Removal

a. Remove the six M3 x 12mm pozi-countersunk screws from the heatsink retaining plate.

b. Remove the heatsink retaining plate.

c. Disconnect connectors:

J1 at the NEGATIVE HEATSINK ASSEMBLY
J2 at the POWER AMPLIFIER ASSEMBLY

d. Remove Negative Heatsink assembly.

e. Disconnect J3 at the Power Amplifier assembly

f. Remove the Positive Heatsink assembly

g. Disconnect at the following points:

J1	Power Amplifier Assembly
J31, J19	Mother Assembly
J1	In-Guard PSU Assembly

h. Remove the Power Supply / Current Heatsink assembly.

- Fitting

Reverse the removal procedure. To ensure correct location, turn the PCB side of each heatsink to face inwards

3.5.11 HIGH VOLTAGE ASSEMBLY
(page 11.18-2 detail 5)

- Removal

a. Refer to *page 11.18-2 detail 5*.
Lift the assembly upwards as shown in the diagram.

b. Remove the connections J2 and J3.

c. Lift the assembly clear of the instrument.

- Fitting

Reverse the removal procedure. Refer to *page 11.18-2 detail 5*.

3.5.12 MAINS (LINE) TRANSFORMER ASSEMBLY
(page 11.18-5 detail 9)

- Removal

a. Disconnect the connectors from the transformer at the following assemblies:

J2	-	In-guard Power Supply PCB Assembly *(facing page 11.18-2 detail 2.)*
J3	-	In-guard Power Supply PCB Assembly *(facing page 11.18-2 detail 2.)*
J5	-	Out-guard Power Supply PCB Assembly *(facing page 11.18-2 detail 1.)*
J6	-	Interconnection Assembly *(facing page 11.18-5 detail 8.)*
J31/32	-	Out-guard Power Supply PCB Assembly *(facing page 11.18-2 detail 1.)*
J32	-	Mother PCB Assembly *(facing page 11.18-2 detail 3.)*
J33	-	Mother PCB Assembly *(facing page 11.18-2 detail 3.)*

b. Turn the instrument to stand on its left side (on Left Hand extrusion)

c. Release the four M8 x 110mm bolts, washers and nylock nuts.

d. Remove the M3 x 8mm pozi-countersunk screw, M3 steel nut and shakeproof washer which secures the solder tag terminals of four ground wires. Fold back the wire which is fitted to the rear panel assembly.

e. Remove the Mains (Line) Transformer assembly.

- Fitting

Refer to *page 11.18-5 detail 9*; reverse the removal procedure.

3.5.13 HF TRANSFORMER ASSEMBLY

(page 11.18-4 detail 6)

- **Removal**

a. Remove four M3 x 8mm pozi-pan screws *(see Fig. 3.1).*

b. Disconnect connectors at the following points:

J2 - High Voltage Assembly;
J5 - Power Amplifier Assembly.

c. Remove the HF transformer assembly.

- **Fitting**

Reverse the removal procedure referring to *Fig. 3.1.*

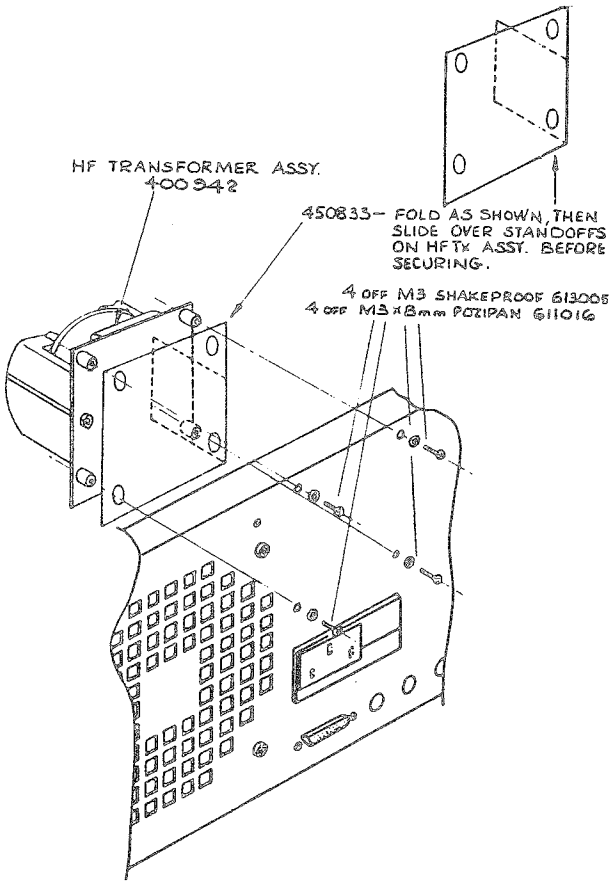


FIG 3.1 HF TRANSFORMER

3.5.14 LF TRANSFORMER ASSEMBLY

(page 11.18-5 detail 10)

- Remove High Voltage Assembly *(3.5.10)* and the Heatsinks *(3.5.9.)*

- Removal

a. Disconnect connector J4 from the Power Amplifier and J3 from the High Voltage Assembly *(see Fig. 3.2).*

b. Turn the instrument to stand on its right hand side (on R.H. extrusion).

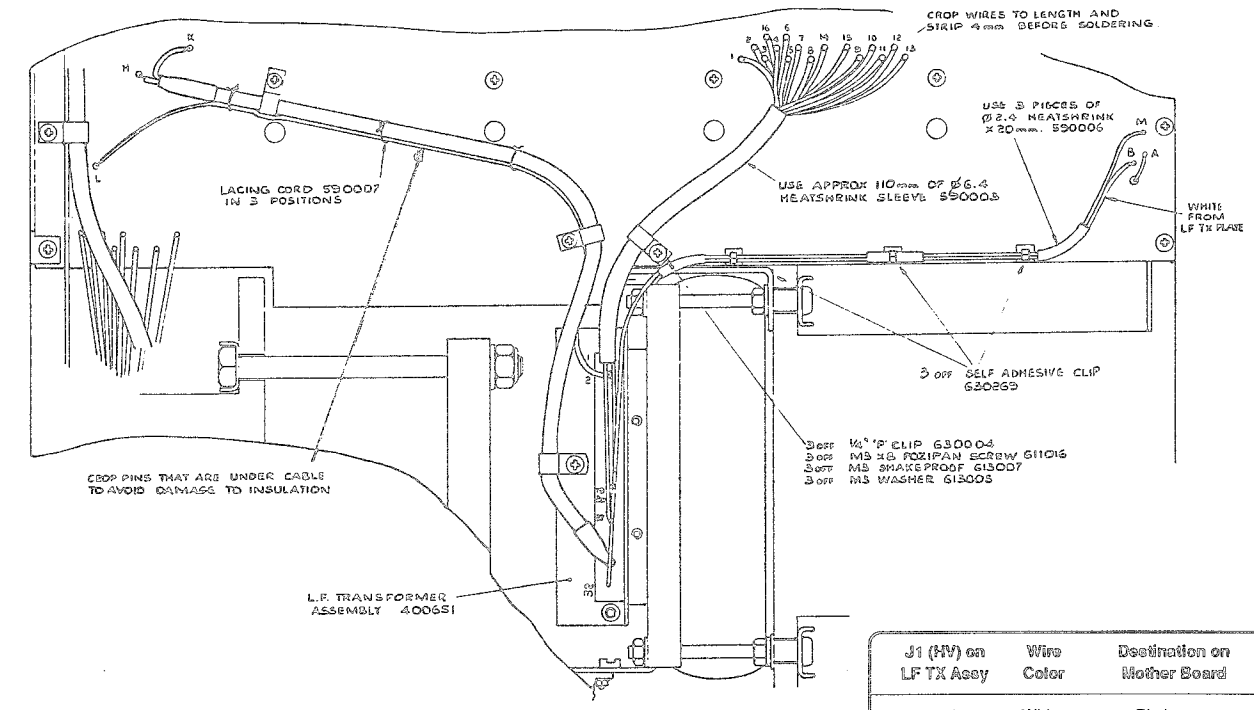
c. Desolder J34 from the mother board and connections A, B, M, H, K, & L. Remove associated supporting clips.

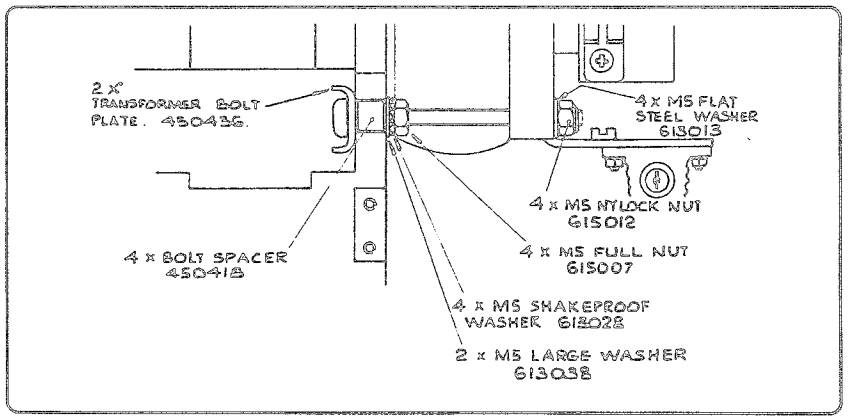
d. From the LF Transformer; remove the four M5 nylock nuts and flat steel washers, Remove a pair of the transformer assembly M5 x 65mm screws closest to the rear panel and the transformer bolt plate.

e Slide out the LF Transformer.

- Fitting

Reverse the removal procedure. Refer to *Fig. 3.2* and *page 11.18-2 detail 10.*





J1 (HV) on LF TX Assy	Wire Color	Destination on Mother Board
2, 3	White	Pin L
6	Black	J34-8
7	Brown	J34-5
8	Red	J34-6
9	Orange	J34-4
10	Yellow	J34-9
12	Blue	J34-12
13	Violet	J34-13
14	Red/Grn	J34-3
15	White	J34-10
16	Green	J34-14
17	Red/Blk	J34-7
18	Grey	J34-15
19	Red/White	J34-2
20	Pink	J34-1
21	Red/Blue	J34-16
22	Orng/Blk	J34-11
28	Coax	Center - Pin H Screen - Pin K
31	White	Pin M

J1-6 to J1-22 are inside Heatshrink Sleeve

FIG 3.2 LF TRANSFORMER

3.5.15 TERMINAL PCB ASSEMBLY

(page 11.18-5 detail 8)

- Remove Front panel *(para 3.4.3)*.

- Removal

a. Remove the four M3 x 6mm pozi-pan screws *(page 11.18-4 detail 8)*

b. The terminal board can be tipped down to facilitate component access.

- Fitting

Reverse the removal procedure.

3.5.16 REAR PANEL ASSEMBLY

(page 11.18-4 detail 6)

- Do not remove the rear panel assembly when Top and Bottom covers and Ground/Guard assemblies are removed. Perform the following operations with Top and Bottom covers and Ground/Guard assemblies fitted, or with AT LEAST the Top OR Bottom Ground Sheet assembly fitted.
- This procedure provides access to rear panel-mounted components by releasing the Rear Panel assembly and moving it away from the chassis to the extent allowed by internal wiring connections.

- Removal

a. Remove the six screws of the two rear spacers *page 11.18-4 detail 7*.

b. Remove the two rear spacers.

c. Remove the four screws of the filter grill.

d. Remove the filter grille and filter.

e. Remove the Pozi-pan screw revealed by the removal of the filter and grill.

f. Remove the four rear panel screws *(page 11.18-4 detail 6)*

g. Looking at the rear, locate the upper right hand screw securing the extractor fan. Above this screw, locate an M3 x 6mm Pozi-pan screw (screw fixing hole only shown on diagram). Removal of the screw allows the rear panel to be detached (see cut-away sketch above Rear Panel in *detail 6* of *page 11.18-4*).

h. Gently pull the Rear Panel assembly away from the chassis to the extent allowed by the wiring. Do not stress the wires.

- Fitting

a. Press the Rear Panel assembly to the chassis while ensuring that:

   i. The wires lay in the cut-out in the moulded internal chassis;

   ii. The ribbon cables fit in the recess in the moulded internal chassis;

   iii. All other wires are free and not trapped by the rear panel assembly.

b. Fit screws, filter, filter grille and rear spacers, reversing the procedure.

SECTION 4 SERVICING & INTERNAL ADJUSTMENTS

4.1 INTRODUCTION

This section provides procedures for any maintenance or calibration operations which require removal of covers or partial dismantling. The operations fall into three Categories:

A: Routine Servicing (*TABLE 4.1a*);
B: Internal Calibration Adjustments (*TABLE 4.1b*);
C: Adjustment Following Replacement of PCBs (*TABLE 4.1c* - overleaf).

Category A	Routine Servicing			
Servicing Required	Time Interval	Procedure *(Section 4)*	Calibration Required	Calibration Procedure
Clean the Air Intake Filter	1 year (or less in adverse conditions)	*4.2*	-	-
Change Lithium Battery (non-volatile calibration memory)	5 years	*4.3*	(a) Full pre-cal then (b) Full routine recalibration	*Sect. 1.3* *User's Handbook, Sect. 8*

TABLE 4.1a.

Category B	Internal Calibration Adjustments			
Indication	Adjustment Required	Procedure *(Section 4)*	Calibration Required	Calibration Procedure
"ERROR 6" (during Routine Recalibration)	Re-set internal trimmers	*4.4*	Routine 4-wire & 2-wire Ω	*Sect.1.4 and User's Handbook, Sect. 8*

TABLE 4.1b.

Category C	Adjustments Following Replacement of PCBs			
PCB Assembly	**Adjustments**	**Procedure** *(Section 4)*	**Pre-cal** *(Sect. 1.3)*	**Routine cal** *(Sect. 1.1)*
Terminal	Capacitive Load Test	*4.6*	-	Full
Digital	-	-	Full	Full
Reference Divider	-	-	Full	Full
DC	Capacitive Load Test	*4.6*	-	Full
Sine Source	-	-	-	Full
AC	Capacitive Load Test Sense Amp zeros	*4.6* *4.10*	-	Full
Current/Ohms Assembly	Quiescent Current Compliance Resistance	*4.7* *4.8* *4.4*	-	All I ranges All I ranges Ohms
Power Amp	100V PA bias	*4.5*	-	-
Mother	Common-mode null	*4.9*	Full	Full
Out-guard PSU	Common-mode null	*4.9*	-	Full
Heatsinks +ve & -ve	100V PA bias	*4.5*	-	-
Power supply Current Heatsinks	Quiescent Current	*4.7*	-	All I ranges
HF or LF Transformer	-	-	-	1kV Range
Mains (line) Transformer	Common-mode null	*4.9*	-	-

TABLE 4.1C.

4.1.1 General Procedure Notes

a. Disconnect the instrument from any power source before attempting to dismantle it (for dismantling and reassembly instructions consult *Section 3*).

b. If the top ground/guard assembly is removed, subsequent testing with Power On should be completed in less than 5 minutes to avoid overheating.

c. After servicing ensure that all connections have been made correctly and that thetop and bottom shields and covers have been replaced. Leave assembled instrument powered-up for at least 1 hour before carrying out any adjustment.

d. Although replacement assemblies are set up by the manufacturer, the internal adjustments recommended in *Table 4.1* must be carried out to ensure correct operation. These adjustments need to be carried out once the assembly is installed in the user's instrument, in order to account for interaction between assemblies.

WARNING

HAZARDOUS ELECTRICAL POTENTIALS ARE EXPOSED WHEN THE INSTRUMENT COVERS ARE REMOVED.

ELECTRIC SHOCK CAN KILL!

CAUTIONS

AFTER ANY MAINTENANCE OPERATIONS WHICH INCLUDE REMOVAL OF TOP OR BOTTOM GROUND ASSEMBLY, CARRY OUT THE FULL SELF-TEST SEQUENCE (*Section 2.3*) BEFORE RETURNING TO NORMAL USE.

DAMAGE CAUSED BY UNAUTHORISED REPAIRS OR MODIFICATIONS CAN INVALIDATE INSTRUMENT WARRANTY. CHECK THE WARRANTY DETAILED IN THE "TERMS AND CONDITIONS OF SALE". IT APPEARS ON THE INVOICE FOR YOUR INSTRUMENT.

4.2 CLEANING THE AIR INTAKE FILTER

(Datron Part No. 450277-1)

4.2.1 Servicing Frequency

The filter should be cleaned at intervals no greater than one year. In dusty conditions the frequency should be increased.

4.2.2 Removal

a. Remove the four M3 x 10mm pozi-countersunk screws which retain the filter grille.

b. Remove the filter grille and reticulated foam filter.

4.2.3 Cleaning

a. Wash the foam filter in a dilute solution of household detergent (hand hot).
Rinse thoroughly in clean hand-hot water and dry completely, without using excessive heat.

b. Clean the grille, and the grille holes in the rear panel (use a vacuum cleaner and soft brush on the rear panel).

4.2.4 Inspection

Examine the foam filter for wear, replacing if links are broken.

4.2.5 Reassembly

Place the filter in the grille housing and secure the grille to the rear panel using the four M3 x 10mm pozi-countersunk screws.

4.3 LITHIUM BATTERY - REPLACEMENT

(Datron Part No. 920101)

FIRST READ THESE NOTES!

- This procedure is to be performed at intervals of 5 years from new.
- Procedure 4.3.1 allows calibration memory to be retained during battery replacement. This requires the use of an Extender Card *(Datron Part No. 400625)* to give access to the battery, and during its removal provide a supply to the non-volatile RAMs. To ensure memory integrity the soldering iron used must be isolated from Mains (Line) ground by at least 50kΩ.
- Procedure **4.3.3** resets the calibration memory to its nominal state (but does not require the use of an extender card) during replacement of the battery. If this method is used a Precalibration and **full** Routine Recalibration *(Section 1.3 and 1.1)* **must** follow before the instrument specification can be realized, as calibration data will have been corrupted. In this case it is therefore recommended that the battery be replaced immediately prior to a scheduled full recalibration.

4.3.1 Procedure (Calibration Maintained)

a. Ensure that power OFF is selected.

b. Remove the top cover and top ground/guard assembly *(Section 3.4.1 and 3.4.4)*.

c. Remove the Digital Assembly from the chassis (*Section 3.5.4*).
Do not place the assembly on any conducting surface or touch the gold edge connector.

d. Place extender card in digital assembly slot.
Push Digital Assembly onto extender card.

Caution

- If the calibrator has been in use; allow to cool for 2 hours. From power ON (step f.) the internal temperature of the instrument will begin to rise. Ensure the procedure is completed within approximately 15 minutes; any Fail 1 message which occurs during this time period can be safely ignored.
- Precautions must be taken to prevent solder or other material falling into the calibrator.
- Ensure continuity of Mains (Line) supply while battery is disconnected.

e. Select power ON. To reduce power dissipation ensure output remains OFF.

f. Remove battery *(refer to Fig. 4.1)*.

g. Fit and solder in a new battery. Select power OFF (calibration maintained).

h. Refit the Digital Assembly into the chassis *(Section 3.5.4)*.

4.3.2 Procedure (Calibration lost)

Follow the procedure 4.3.1 ignoring steps (d.) and (e.)

4.3.3 Return to Use

Refit the top ground/guard assembly into the chassis (*Section 3.4.4*).
Refit the top cover (*Section 3.4.1*).

NOTE: Users who have followed procedure 4.3.2 must now carry out Pre-calibration and full Routine Calibration in accordance with *Section 1.3* and *1.1* respectively.

i. Push sleeve back along the red wire to expose the solder joint.

ii. Unsolder the red wire from the positive terminal of the battery.

iii. Unsolder the negative terminal of the battery from resistor R60 at the wrap-joint.

iv. Remove battery from battery clip

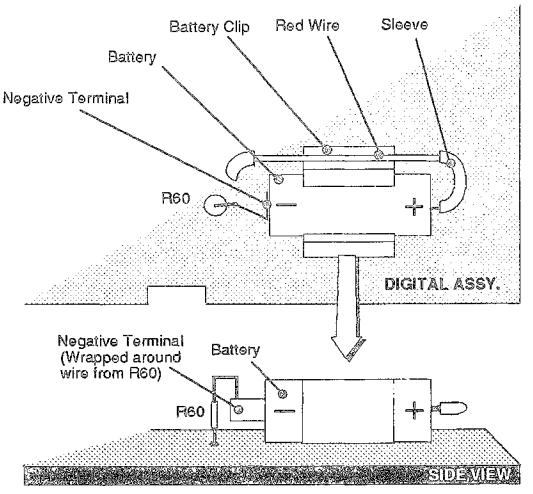


FIG. 4.1 BATTERY REPLACEMENT

4.4 OHMS FUNCTION — STANDARD RESISTOR ADJUSTMENT

4.4.1 Introduction

Routine adjustment of the standard resistors used in Ω function is not required. A resistor is calibrated by the user entering its measured value into a non-volatile calibration memory. This value is subsequently recalled and displayed to the user each time the resistor is selected.

4.4.2 *'Error 6'* Message

'Error 6' is displayed if the value entered by the user during calibration is outside the resistor's tolerance — i.e outside the calibration memory span. Under normal use the resistor drift will be well within the tolerance, so ***'Error 6'*** should only appear if the user enters an erroneous value.

4.4.3 Undue Resistor Stress

If the resistor has been subjected to undue stress, it is possible that its value may have changed slightly, and be outside its tolerance. If it is less than approximately 50ppm outside tolerance an internal trimmer can be adjusted, and the value can be calibrated.

4.4.4 Possible Damage

A stressed resistor may have been damaged if its value is greater than 50ppm outside its tolerance. It is advisable to have such a resistor tested or replaced by Datron Service Center.

4.4.5 To Reset Internal Trimmers

Follow the procedure detailed in *Section 1.4* to adjust the resistor value. If this is unsuccessful contact your Datron Service Center.

4.5 BIAS CURRENT ADJUSTMENT — 100V PA

(Refer to Layout Drawing 480618 Page 11.9-1 and 480637 Page 11.13-1)

Adjustment of the 100V/1kV amplifier bias voltages must be carried out after fitting a replacement Power amplifier assembly or Heatsink assembly. The following procedure ensures the drain voltages of Q4 and Q2 are +120V and -120V respectivly.

USE EXTREME CARE THROUGHOUT THE FOLLOWING PROCEDURES.

4.5.1 Test Equipment Required

Digital voltmeter (any Datron Autocal voltmeter)

4.5.2 Initial Conditions

Remove top cover.
Remove top ground/Guard assembly.
Ensure 38V/400V selector is set to 400V.

4.5.3 Procedure

a. Set 4808 Power OFF to connect DVM as follows;

b. Power Amplifier Assembly
Connect DVM in DC function, Lo to ⏚ 2C (near Q20) and Hi to Tab of Q4.

WARNING

At Power ON (even with Output OFF) the heatsinks are maintained at LETHAL VOLTAGES!
Use insulated adjustment tool.

c. Select Power ON .

d. Positive Heatsink Assembly — adjust R10 for a reading of +120V (5V).

e. Power OFF, disconnect DVM.

4.5.4 Return to Use

Refit top ground/guard shield and top cover.

4.6 CAPACITIVE LOAD TEST

(Refer to Layout Drawing 480536 Page 11.5-1)

The AC 1kV current overload detector on the DC Assembly monitors output current. ERROR OL is displayed when output current limit is exceeded.

After replacing the DC Assembly, Terminal assembly, AC assembly, PA assembly, Positive or Negative Heatsinks, or the HF transformers it is necessary to ensure the limit level is re-set to account for any capacitance changes. The value of R84 will lie between 2k43Ω and 3k65Ω. R84 will be selected from the E96 (1%) series.

4.6.1 Test Equipment Required

a. Test Load (1kΩ non-inductive resistor, capable of dissipating 20 Watts).

b. Digital Voltmeter fitted with AC Volts Ranges (any Datron Autocal multimeter)

4.6.2 Initial Conditions

Top cover removed.
Remove top ground/guard assembly.
Ensure 38V/400V power supply selector set to 400V.

4.6.3 Procedure

WARNING

THE PROCEDURES INVOLVE THE MEASUREMENT OF LETHAL VOLTAGES. USE EXTREME CARE TO AVOID ELECTRIC SHOCK.

a. Ensure 4808 Power OFF.

b. On DC board remove Link J, and make Link L. DC assembly must be fitted in chassis (not on extender card)

c. Monitor Link L with respect to ⏚ 2B with scope set to 5V per division.

d. Connect Load resistor across the 4808 output terminals.

e. Connect the DVM across the Load resistor and select AC 1kV range on DVM.

f. Set 4808 Power ON.

g. On 4808 select AC 1kV Range and adjust OUTPUT ◇ keys for 90V on the OUTPUT display. Select 10kHz range and set frequency to 4kHz. Set OUTPUT ON.

h. Increment demanded voltage and check that 'Scope goes to zero volts when the DVM indicated between 108V and 112V. Select output OFF.

WARNING

CALIBRATOR POWER MUST BE OFF WHEN CHANGING R84. LETHAL VOLTAGES ARE PRESENT!

j. If outside limits set in (h.) reselect R84 and repeat from step (f.).

k. When correct operation occurs solder in R84 break Link L and replace Link J.

4.6.4 Return to Use

Refit top ground/guard shield and top cover.

4.7 QUIESCENT CURRENT ADJUSTMENT - CURRENT/OHMS ASSEMBLY or CURRENT ASSEMBLY

(Refer to Layout Drawing 480614 Page 11.8-1)

To allow a measurement of quiescent current in the power amplifier stage, its power supply lines are broken and a 0.1Ω resistor inserted in series with each 22V supply line. The voltage developed across either of these resistors gives a current measurement. The quiescent current is set by adjustment of R23 on the Current/Ohms Assembly.

4.7.1 Test Equipment Required

a. Digital Voltmeter (any Datron Autocal voltmeter)

b. Two 2.5-watt resistors, 0.1Ω, 10%, wire wound (Welwyn W21 or equivalent)

4.7.2 Initial Conditions

Top cover removed.
Top ground/guard assembly removed.

4.7.3 Procedure

a. Switch the 4808 Power OFF.

b. Break the 22V supply connections to the Voltage-to-Current converter power stage by removing connector J1 from the In-guard power supply pcb.

c. Re-make each 22V supply connection from its female pin on the freed J1 connector to its corresponding male pin on the In-guard power supply pcb, using one 0.1Ω resistor in series with each supply line (Red and Brown wires).

d. Connect the digital voltmeter across one of the 0.1Ω resistors fitted in step (c.).

e. Switch 4808 Power ON. Select AC Current, 1Amp Range, ensure OUTPUT OFF.

CAUTION

In the following step (f), use a thin insulated screwdriver.

f. Carefully adjust R23 on I/Ω assembly for a digital voltmeter reading of 10mV ±1mV (equivalent to 100mA through the 0.1Ω resistor).

g. Switch 4808 Power OFF.

h. Disconnect and remove both 0.1Ω resistors and the digital voltmeter from J1. Reconnect J1 to the In-guard Power Supply pcb pins.

4.7.4 Return to Use

Refit top ground/guard assembly and top cover.

4.8 COMPLIANCE ADJUSTMENT - CURRENT/OHMS ASSEMBLY or CURRENT ASSEMBLY

(Refer to Layout Drawing 480614 Page 11.8-1)

Ensure that the Quiescent Current Adjustment Procedure has been completed (*Section 4.7*).

In the following procedure a DVM is used to measure output current as a voltage developed across a load resistor. Series resistance is then added to one of the power leads to establish a compliance voltage. The change in current output due to compliance is measured and an adjustment made to bring the instrument within manufacturer's specification.

4.8.1 Test Equipment Required

a. Digital Multimeter fitted with AC Volts Ranges. (e.g. Datron Instruments model 1281).

b. Test leads, (each containing a 22.1Ω resistor).

c. One 2.5-watt load resistor of 0.10Ω, 10%, Wire Wound. (Welwyn W21 or equivalent).

d. A 1.4Ω resistor to introduce compliance voltage.

4.8.2 Initial Conditions

Remove top cover.
Remove top ground/guard assembly.

4.8.3 Procedure

a. Connect the 0.1Ω load resistor between the 4808 current output terminals (I+/I-).

b. HF adjustment Select ACI, 1A full range output at 5kHz. Select OUTPUT ON.

c. With the DVM, measure the AC voltage across the load and note the reading. Set OUTPUT OFF.

d. Introduce the 1.4Ω compliance resistor in series with the I+ lead. Set OUTPUT ON (Test should be done in less than 5 minutes to avoid overheating). Use the DVM to measure the AC voltage across the 0.1Ω load and note the reading.

e. Remove compliance resistor. If there is a change of reading >10μV between (c.) and (d.) adjust R10 to reduce the change of reading to <10μV. After each adjustment of R10 repeat (c.) to (e.).

f. LF Adjustment Complete above procedure, leaving the 4808 as selected (ACI, 1A Full Range), but change frequency to 500Hz and limit to 5μV.

g. If change of reading in (d.) is >5μV adjust R31.

h. If an adjustment was made to R31 repeat complete procedure from (b.) until no further adjustments are required.

j. Output OFF, disconnect load resistor.

4.8.4 Return to Use

Replace top ground/guard assembly and top cover.

4.9 COMMON MODE NULL ADJUSTMENTS

(Refer to Diagram 400996 Page 11.10-1)

The procedure ensures that after replacement of Outguard Power Supply, Mains (Line) transformer or Mother Assembly, any power supply noise breakthrough on the Lo or Guard terminals is adjusted to a minimum. Resistor R12 on the Outguard Power Supply Assembly (accessible through a hole in the top ground shield) is adjusted to minimize the voltage between Lo and Ground. On the Mother Assembly (accessible through a hole in the bottom ground shield) R25 is adjusted to minimize noise between Guard and Ground.

4.9.1 Test Equipment Required

Oscilloscope (with AC input and sensitivity to 100mV/div).

4.9.2 Initial Conditions

Remove top and bottom covers.
Ensure all guard/ground screws are correctly tightened.

4.9.3 Procedure

a. Set 4808 to AC 10V range with Output OFF.

b. Ensure that the OUTPUT display is 0.000,00 V with local guard selected.

c. Connect the oscilloscope AC input to the 4808 Guard terminal and the oscilloscope Ground to the 4808 Ground terminal.

d. Locate R12 on the Outguard Power Supply assembly (accessible through the hole in the top ground/guard assembly)

e. Select OUTPUT ON and adjust the oscilloscope controls to obtain the line related noise waveform.

f. Without touching the top ground/guard assembly, adjust R12 for minimum waveform amplitude.

g. Select Remote Guard and obtain a noise waveform.

h. Locate R25 on the Mother pcb assembly through the hole in the bottom ground/guard assembly

j. Without touching the bottom ground assembly, adjust R25 for minimum waveform amplitude.

k. Repeat procedure from step (b.) to step (j.) until minimum waveform amplitude is obtained.

l. Select OUTPUT OFF. Disconnect the oscilloscope.

4.9.4 Return to Use

a. Refit top cover.

b. Refit bottom cover.

4.10 SENSE AMPLIFIER ZEROS

(Refer to Layout Drawing 400844 Facing Page 11.7-1)

The sense amplifier, situated on the AC Assembly, is provided with access holes located in the top ground/guard shield. In the following procedure the reading and adjustment steps are always taken with the 4808 OUTPUT ON and at one-tenth of the selected Full Range value.

4.10.1 Test Equipment Required

Digital voltmeter
(e.g. Datron Instruments model 1281 or 1271).

4.10.2 Initial Conditions

Remove top cover only.

4.10.3 Procedure

a. Connect the DVM Hi to TP5 on the AC Assembly (accessible via the hole in the upper guard shield). Connect its Lo to the 4808 Lo terminal. On the DVM select the DC 10V range with filter in.

b. On the 4808 select the AC 100V range, set 10V and 1kHz output. Select OUTPUT ON and adjust R122 for a DVM reading of less than 200μV.

c. On the 4808 select the AC 10V range, 1V output. Select OUTPUT ON.

d. Note the DVM reading.

e. On the 4808 select the 1V range, 100mV output. Select OUTPUT ON.

f. Note the DVM reading.

g. Adjust R107 on the AC assembly to set both (d.) and (f.) readings to less than 200μV.

h. Repeat procedure from (b.) to (g.) until readings are correct and the difference between all ranges is less than 400μV taking polarity into account.

j. Disconnect the DVM.

4.10.4 Return to Use

Refit top cover.

PART 2

TECHNICAL DESCRIPTIONS

SECTION 5 PRINCIPLES OF OPERATION

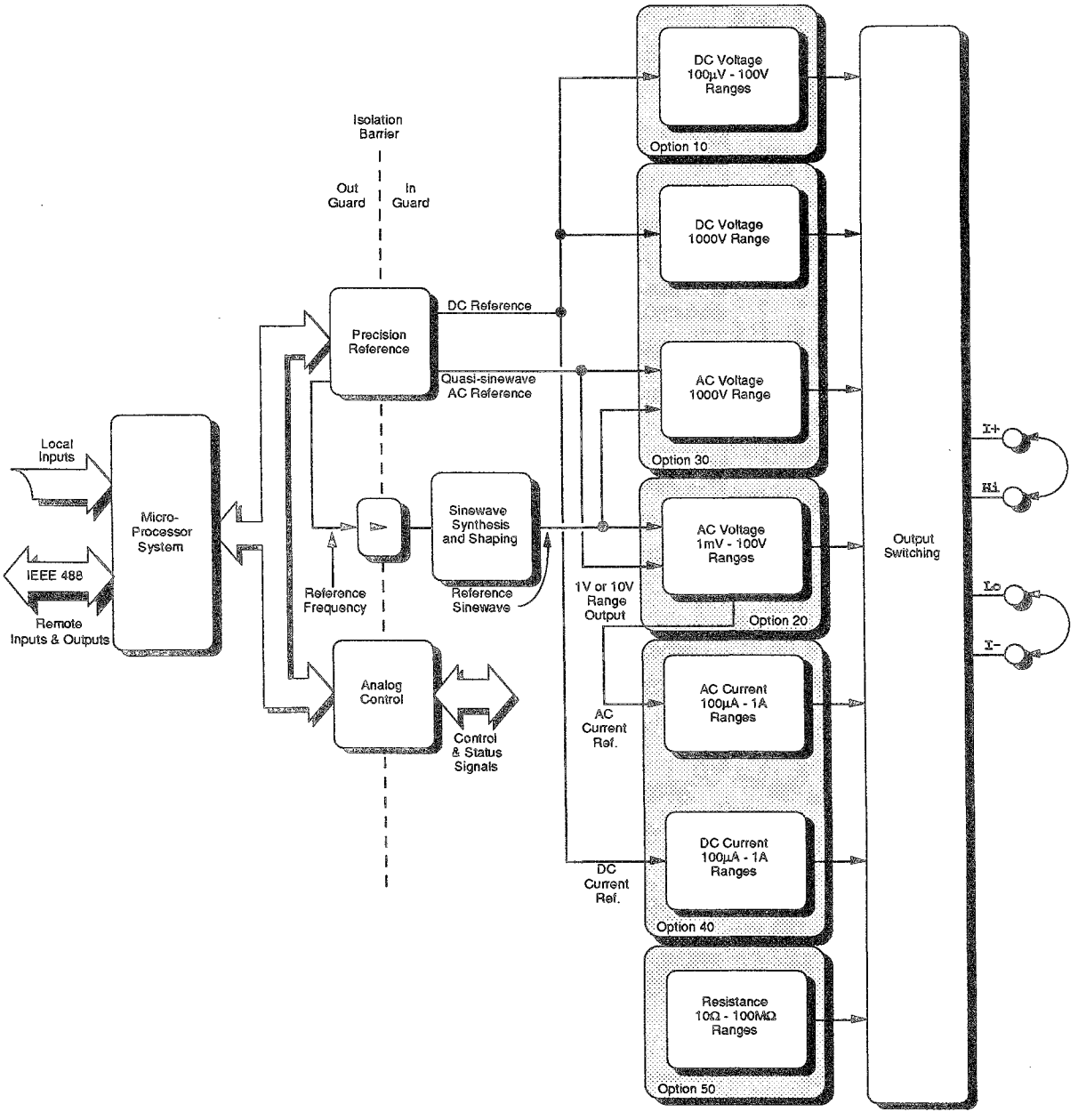


FIG. 5.1 4808 SIMPLIFIED BLOCK DIAGRAM

5.1 BLOCK DIAGRAMS

5.1.1 SIMPLIFIED BLOCK DIAGRAM

Figure 5.1 illustrates the general functions and signal flow within the 4808.

5.1.2 GENERAL DESCRIPTION

The Datron 4808 Autocal Multifunction Standard mainframe contains just a microprocessor system and IEEE-488 interface. To provide any useful functions, Option 10 and/or Option 20 must be installed as a minimum.

Option 10:	DC Voltage function to ±200V.
Option 20:	AC Voltage function to 200V.
Option 30:	Integral 1000V amplifier for AC Voltage and/or DC Voltage functions. (Requires either Option 10, Option 20 or both.)
Option 40:	Current converter to provide DC Current and AC Current functions. (DC Current capability requires Option 10, AC Current capability requires Option 20.)
Option 50:	Resistance function. (Requires Option 10 or Option 20.)
Option 60:	DC Current and/or AC Current range extension to 11A. This option includes the Datron 4600 Transconductance Amplifier and all necessary cabling. (Requires Option 40.)

For DC and AC amplitude control, an adjustable precision reference is derived from a pre-conditioned zener diode.

For AC outputs, the calibrator frequency is synthesized using a crystal-controlled oscillator as a frequency reference.

5.1.3 FUNCTIONAL BLOCK DIAGRAMS

Figures 5.2 (Digital, Control and References), *5.3* (DC/Ω) and *5.4* (AC) break the main functional divisions into smaller blocks.

They can be thrown clear of the handbook to provide a functional overview; they also form an index to other sections of Part 2.

5.2 INPUTS

The microprocessor accepts inputs from two main sources:

- The front panel keyboard provides local control inputs.
- The IEEE 488 bus system provides remote control inputs.

5.3 DIGITAL OUTPUTS

The microprocessor system outputs digital information to five main areas:

- The front panel displays provide local outputs for monitoring and control.
- The IEEE 488 bus system provides remote outputs.
- The precision reference generator produces an accurate DC reference for output-amplitude control. Sensed DC outputs are scaled and compared against the DC reference directly. Sensed AC outputs are scaled and compared against a 'quasi-sinewave' reference, whose peak value is set by the DC reference.
- The frequency synthesizer and sinewave oscillator together determine the frequency and purity of the AC output sinewave signal.
- Various decoders control function and range selection, internal processes and status monitoring.

5.4 PRECISION REFERENCE

(Fig. 5.2)

5.4.1 AMPLITUDE REFERENCE

The circuits produce a DC reference voltage which can be set between 0V and ±20V for DC outputs, and between +0.126V and +2.794V for AC outputs. The value of the reference is set by the value on the left-hand OUTPUT display, modified in software by range scaling and calibration corrections.

For DC, the range-scaled sense voltage is compared directly with the reference - the resulting error controls the DC output value directly. For AC outputs it determines the amplitude of the 'quasi-sinewave', a stepped waveform which is used as the AC amplitude reference. This operates in the error sensing loop, having a shape whose crest factor closely approaches that of a true sinewave.

The circuitry is divided into four main areas:

a. The period division comparator, outside guard, consists of a binary counter and comparator, both effectively of 25 bits. The counter is driven by a crystal-controlled clock; the comparator being set by latched data from the microprocessor system.

   When the binary count matches the data set in the latches, the comparator produces a switching pulse (reset). The counter fills to overflow point, at which the comparator produces a second pulse (set). Thus accurate mark-period timing is generated.

b. The switching integrator receives the pulses across guard. They are used to drive solid-state divider switches, chopping the output from a very stable 20V DC Master Reference. The resulting square wave is very accurately defined, both in mark-period ratio and amplitude. Integration of the square wave, by an active low-pass filter with high rejection at the chopping frequency, generates the DC Reference voltage.

c. For DC outputs, the selected output polarity controls a switch which inverts the DC Reference for negative outputs.

d. For AC outputs, a negative version of the DC reference is generated by inversion. Both positive and negative versions are passed to the quasi-sinewave generator, which sets the positive and negative inputs to a potential divider, whose centre-tap is tied to reference common.

   The outputs from the divider are selected in ten equal time-steps by digital logic, the ratios being selected so as to produce a periodic signal of quasi-sinusoidal form. The Crest Factor of this signal (Peak value divided by RMS value) is 1.397, close to that for a pure sinewave. The RMS ratio of sinewave to quasi-sinewave is stored during calibration, and reapplied as a correction during normal use.

   Because the amplitude of the quasi-sinewave depends on the value of the DC Reference voltage, its settling time to a stable value is determined by the 7-pole DC reference filter.

   For accurate sine/quasi-sine RMS comparison, it is important that both the quasi-sinewave steps and the comparator sequence are synchronized to zero-crossing points in the sensed output sinewave. This is ensured by:

   (a) including the divide-by-ten logic of the quasi-sinewave generator as part of the range-divider chain for the frequency synthesizer,

   (b) feeding the quasi-sinewave frequency to the comparator to synchronize the ten-step sequence which controls the RMS comparison process.

5.4.2 FREQUENCY REFERENCE

When the 4808 is operating in AC function, its internal frequency reference is derived from the 13-bit counter in the Precision Reference out-guard circuitry. The counter is tapped at 16kHz, which is fed directly to the synthesizer to establish the frequency of the VCO oscillation.

For users who wish to lock the output frequency of the 4808 to an external frequency source, a phase-locked loop ensures that the 16kHz reference frequency phase is tied to that of the external Reference Frequency. With correct frequency selection on the front panel, this ensures that the 4808 output frequency locks to the external reference frequency.

This function is performed in the External Reference Frequency Buffer.

5.5 ANALOG CONTROL

(Fig. 5.2)

The analog circuitry is controlled by data held in a 48-bit in-guard latch. The microprocessor regularly updates the latch contents, using the serial link to pass the data (through opto-isolators) across the isolation barrier. Certain analog status signals are returned to the microprocessor, also using the serial link.

5.6 DC VOLTAGE OUTPUTS

(Fig. 5.3)

5.6.1 LOW VOLTAGE - 100µV TO 10V RANGES

5.6.1.1 Power Delivery

The basic DC range of the 4808 is 10V (19.999,999V FS). The 10V range output is derived from a buffered 'Error' amplifier, which compares the sensed output directly with the DC Reference.

For the 1V range, the DC reference is attenuated by 10:1 before being applied to the error amplifier. The error amplifier output is buffered before being applied to the I+ and I- terminals.

For the 100mV range, the 1V DC buffer output signal is reduced by a passive 10:1 attenuator before passing to the Hi and Lo terminals. The I+ and I- terminals are not used.

The 100mV attenuator also serves the 100µV, 1mV and 10mV ranges. Output values on these ranges are set purely by scaling the DC reference in software, and the consequent reduction in output resolution available is matched by the resolution of the OUTPUT display.

5.6.1.2 Sensing

On the 1V and 10V ranges, the input from the Hi and Lo (sense) terminals is applied to the error amplifier.

For the millivolt ranges and the 100µV range, there is no remote sensing. To complete the sense feedback, the 1V DC buffer output is applied directly to the error amplifier, which is configured as for the 1V range.

5.6.2 HIGH VOLTAGE - 100V RANGE

The 10V range signal is applied to the 100V power amplifier, which drives the output terminals directly from the VMOS output stage. The sensed signal is attenuated before being applied to the error amplifier.

5.7 AC VOLTAGE OUTPUTS

(Fig. 5.4)

5.7.1 SINEWAVE SYNTHESIS AND SHAPING

To control AC outputs, the frequency synthesizer and quadrature oscillator together generate a reference sinewave of stable amplitude and high purity.

5.7.1.1 Frequency Synthesis

The user-demanded frequency is related to frequency range selection, and is expressed as a binary number 'n' by the microprocessor. It is passed into guard together with binary-coded frequency-range data, to control the frequency of the synthesizer.

The binary counter in the reference divider is synchronized to the 4.096MHz master crystal-controlled clock. This counter outputs a 16kHz frequency reference signal to the synthesizer, where it is divided by two to 8kHz.

In the synthesizer, binary subdivisions of 'n' switch the capacitors of a voltage-controlled oscillator, adjusting its relaxation time-constant so as to cover five possible frequency bands within each frequency range. The VCO output frequency is divided by 'n', then phase-compared with the 8kHz reference. The integrated output from the phase comparator controls the charge and discharge current of the capacitors in the VCO. Thus the VCO frequency is adjusted to: n x 8kHz.

The frequency range data is decoded and used to define division ratios in a series of frequency dividers, which act on the output from the VCO. The result is the user-selected frequency, to an accuracy of 100ppm.

5.7.1.2 Sinewave Shaping

The quadrature oscillator is approximately tuned to the user-selected frequency by the binary word 'n', together with the decoded frequency range data, which combine to switch its circuit constants. The oscillator output is applied to a second phase comparator, and referred to the synthesizer frequency. The comparator output adjusts the oscillator frequency to that of the synthesizer.

The quadrature oscillator feedback is conditioned to ensure that its unity loop gain and its 360° loop phaseshift occur together; only at a specific amplitude, and at the synthesized frequency.

The oscillator output passes as reference sinewave to the VCA.

5.7.2 VOLTAGE-CONTROLLED AMPLIFIERS

The output from the quadrature oscillator is applied to two cascaded voltage-controlled amplifiers. The gain of the second of these (the 1V buffer) is adjusted in coarse steps; the gain of the first being adjusted in response to the error between the scaled output amplitude, and that of the quasi-sinewave reference.

The settling curve of the 7-pole filter in the precision reference divider is imposed on the 1V buffer slew rate, by using the filter's DC reference output to control the coarse gain. This signal is changed into a 10-bit word by an analog-to-digital converter, whose digital output adjusts the input resistance of the 1V buffer in steps of 1000ppm of Full Scale. As the 1V buffer is part of the error loop, this adjustment injects an undesirable scaling into the loop. Therefore, to correct the loop gain, the same 10-bit word is used to apply inverse scaling to the error signal from the comparator, before it reaches the first VCA.

5.7.3 LOW VOLTAGE - 1mV TO 10V RANGES

5.7.3.1 Power Delivery

On the 1V range, the output from the 1V buffer is passed to the I+ and I- terminals directly.

For the 10V range, the 10V amplifier (a X10 amplifier on the Power Amplifier assembly) is inserted between the 1V buffer and the I+ and I- terminals.

For the millivolt ranges, the 1V buffer output signal is reduced by switched, passive attenuators before being output via the Hi and Lo terminals.

5.7.3.2 Sensing

On the 1V range, the input from the Hi and Lo (sense) terminals is applied to the non-inverting input to the 1V/10V sense amplifier, which acts as a voltage follower.

For the 10V range, the sense amplifier is configured as a divide-by-ten inverter.

For the millivolt ranges, there is no remote sensing. To complete the sense feedback, the 1V buffer output is input directly into the sense amplifier, which is a configured as for the 1V range.

5.7.3.3 Sine/Quasi-Sine RMS Comparator

The output sinewave is sensed and scaled to 1V levels before being applied to the comparator, which compares it with the reference quasi-sinewave to generate a DC signal whose value represents the output RMS error.

In a strict sense, this circuit does not compare RMS values directly. Instead, it compares the magnitudes of the mean-squares of its two inputs, but if these are equal, then the RMS values are equal. The error loop gain is virtually linear, due to the scaling applied to the error amplifier.

A cycling sequence is continuously imposed, each cycle having a duration of ten quasi-sinewave periods. During the first cycle:

a. the reference quasi-sinewave is first squared and integrated as an analog DC signal (REF), which is memorized in a sample-and-hold circuit;

b. the sensed sinewave input is squared, the (REF) value is subtracted, and the result is integrated and memorized as the DC (SIG) signal in a second sample-and-hold circuit;

c. the DC (SIG) value is output as the mean-square AC error signal.

On subsequent cycles, the (REF) value is also subtracted from the squared quasi-sinewave, so that both (REF) and (SIG) signals converge to steady states as the 4808 output reaches the demanded voltage.

The mean-square AC error signal is passed through the scaled error amplifier to control the VCA.

5.7.4 HIGH VOLTAGE - 100V RANGE

The high voltage loop uses much of the low voltage circuitry; the only differences being in the power amplification to the range voltages, and the attenuation of the sensed output down to 1V range levels.

5.7.4.1 Power Delivery

On the 100V range, the 100V amplifier (on the Power Amplifier assembly) is included in the output path from the 1V buffer to the I+ and I- terminals.

5.7.4.2 Sensing

The 1V/10V sense amplifier is not used on the 100V range. Instead, a separate inverting sense amplifier reduces the sensed sinewave by a ratio of 100:1.

5.8 1000V RANGES

5.8.1 DC 1000V RANGE

(Fig. 5.3)

5.8.1.1 Power Delivery

An AC voltage-amplifier/rectifier system is employed to transform the DC Reference levels up to the high voltages required for the DC 1000V range.

The error voltage, which results from comparison between the scaled sense voltage and the DC Reference, controls the amplitude of a 16kHz AC signal output from a DC modulator. The modulated signal drives the HF step-up transformer via the 100V AC Power Amplifier. A high voltage rectifier and elliptical filter convert the AC transformer output into the DC voltage output. Output polarity is determined by a changeover switch, inserted between the rectifier and the filter.

5.8.1.2 Sensing

The sensed signal is reduced to DC Reference levels by an extensively-guarded precision attenuator, before being applied to the error amplifier.

5.8.2 AC 1000V RANGE

(Fig. 5.4)

5.8.2.1 Power Delivery

The output from the AC 1V Buffer is pre-amplified by the 1kV error amplifier, before being applied to the 100V power amplifier. The 100V amplifier output is transformed up by 1:6, then passed to the I+ and I- terminals. The error amplifier receives feedback from the transformer secondary.

To cover the full frequency range, two transformers with a frequency overlap are employed. The HF transformer is selected as frequency is increased above 3kHz, but the LF transformer is used as frequency is reduced below 3.3kHz. A second feedback loop from the LF transformer primary only, eliminates any saturation of its magnetic circuit.

5.8.2.2 Sensing

The amplifier used to sense the 100V range is also employed for the 1000V range. Although the basic amplifier is common to both, each range has its own input attenuator and feedback ratio. On the 1000V range this ratio is 550:1, and software scales the reference divider digital input to set the quasi-sinewave to values which at full scale are equivalent to 1100V RMS. The amplifier output is compared to the quasi-sinewave in the RMS comparator, the resulting error signal controlling the output from the VCA.

5.9 DC/AC CURRENT OUTPUTS

5.9.1 DC CURRENT

(Fig. 5.3)

The DC Reference is switched to drive a voltage-to-current converter (this converter is the same current amplifier that is used for the AC Current function).

The various ranges are selected by digital control signals from the microprocessor system. The converter shunts are switched into the output circuit to scale the current.

5.9.2 AC CURRENT

(Fig. 5.4)

The ACI Reference signal is obtained by activating either the AC 10V range (used for the 1mA, 10mA and 100mA ranges), or the AC 1V range (100µA and 1A ranges). This is switched to drive a voltage-to-current converter, followed by a current amplifier. Range selection is the same as for DC current output.

5.9.3 10A CURRENT RANGE

(Fig 5.3, 5.4)

If the 4808 is fitted with Option 30 (the resistance and current option), then it has the capability of slave mode control over the model 4600 Autocal Transconductance Amplifier, extending the AC and DC Current functions to effectively include a 10A range, controlled from the front panel or IEEE-488 interface of the 4808. An analog bus to the model 4600 carries the reference voltages (either DC or AC) which the 4600 will 'convert' to an output current, while a digital bus carries status and control signals between the 4600 and the 4808.

5.10 RESISTANCE OUTPUTS

(Fig. 5.3)

Eight fixed precision resistors, in a decade range (from 10Ω to 100MΩ) are switched to the output terminals. The resistors are fully floating, being selected by relays under the control of digital signals from the microprocessor system.

5.11 DATRON 'AUTOCAL'

Precision components are used in all critical locations. Individual analog corrections for frequency-response, gain and offset errors are not applied. Instead, the accumulated errors are measured during calibration, and stored digitally in non-volatile memories.

In subsequent use, characteristic equations are applied to the stored errors to generate software corrections, which are then used to modify the reference divider ratios and so compensate for the accumulated analog errors.

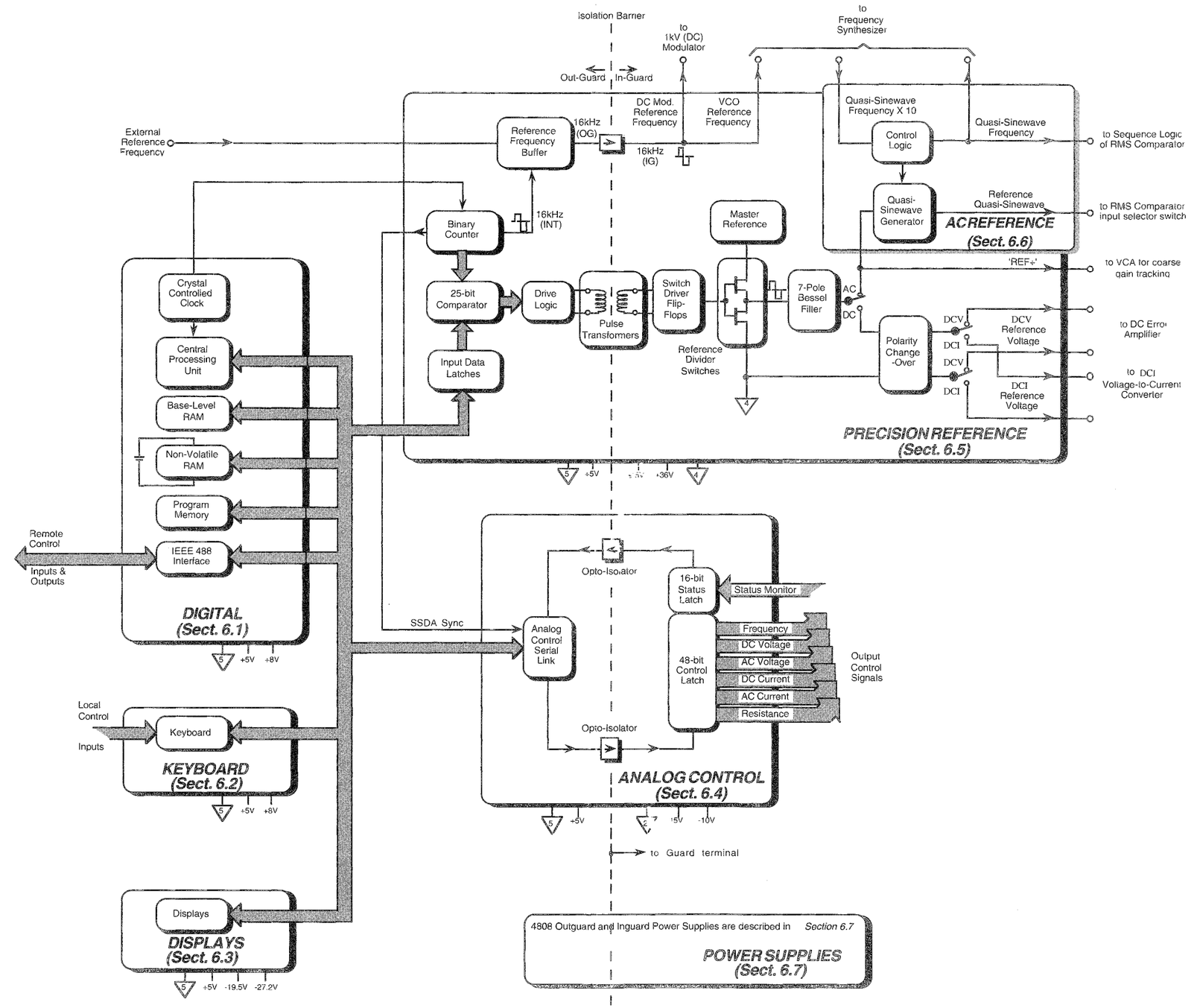


FIG. 5.2 4808 BLOCK DIAGRAM - DIGITAL, CONTROL AND REFERENCES

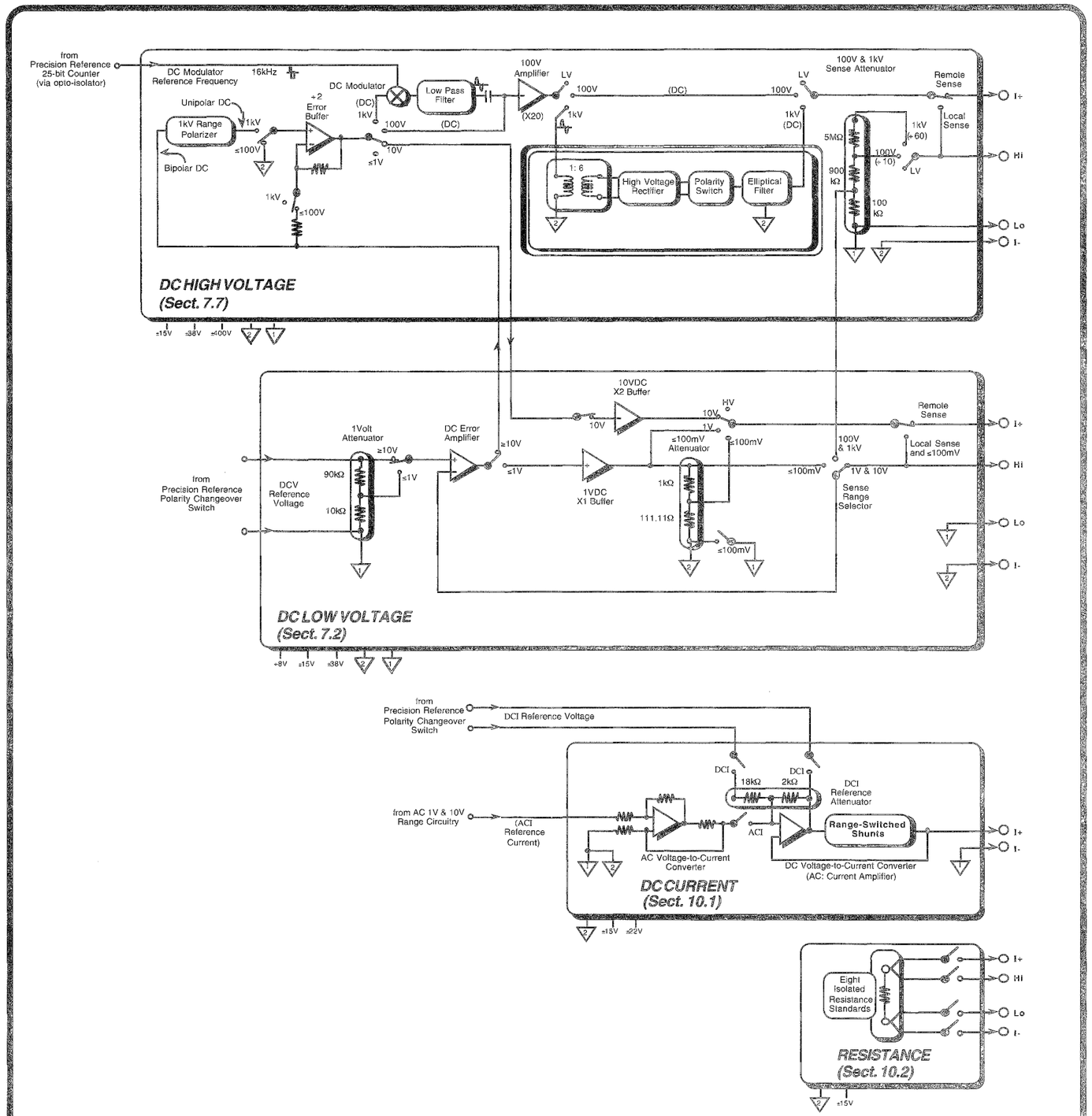


FIG. 5.3 4808 BLOCK DIAGRAM - DC OPERATION

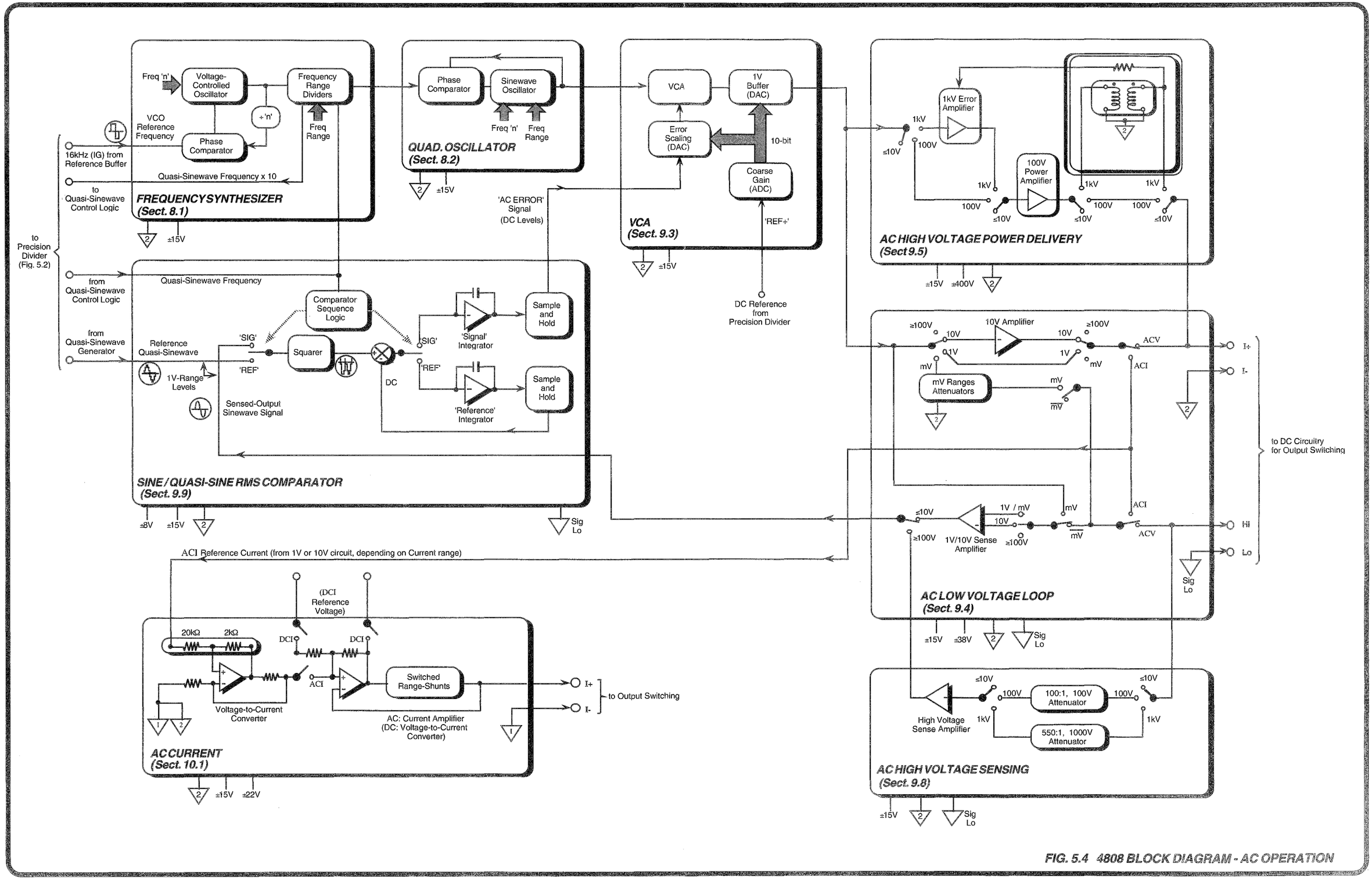


FIG. 5.4 4808 BLOCK DIAGRAM - AC OPERATION

SECTION 6 DIGITAL CIRCUITS; REFERENCE CIRCUITS; POWER SUPPLIES

6.1 DIGITAL

The circuits described in this sub-section perform the following functions:

- Central processing, with supporting memory, for management of instrument operation.
- Storage of calibration constants in non-volatile memory.
- Generation of Master clocks, with clock-waveform shaping.
- Address decoding to generate control signals.
- Controlled power-up and power-down of digital circuits.
- Servicing IRQs from asynchronous sources.
- Interfacing the instrument to the IEEE 488 bus.

The functions are performed by circuits located mainly on the Digital Assembly (480796). Master Clock generation, synchronization and division is carried out by circuits on the Analog Interface Assembly (480648).

Fig. 6.1 shows the arrangement and main interconnections of the central digital circuits.

6.1.1 GENERAL

The instrument is managed by a 6802-series microprocessor system, under the control of an operating program held in 52k bytes of EPROM. All front and rear panel controls provide direct inputs to the system, except for the Power ON/OFF switch and Reset key. The system ensures that the processor reverts to a safe state on power-up and power down.

Work space and stack is provided by 2k bytes of random-access memory (RAM). A further 8k bytes of CMOS RAM act as a non-volatile memory to hold calibration constants, powered by a back-up Lithium battery when the instrument is turned off.

6.1.1.1 Synchronous Operation

The operating program manipulates the internal circuitry by activating control signals, providing peripheral decoders with specific address/data combinations. The program is run at a 680kHz cycle frequency, derived from the instrument's 4.096MHz master crystal oscillator.

6.1.1.2 Asynchronous Operation

Any key operation (other than the Reset or Display keys), or one of two internal conditions, will initiate an asynchronous interrupt (IRQ) which suspends the CPU's current task. The CPU absorbs the new instructions, rearranges its schedule to conform to the demanded new configuration, then continues with the interrupted task until it is completed. Finally it returns to the initial operation of the amended schedule and proceeds synchronously.

Three main sources of interrupt are used:

- Remote Command via the Digital Interface
- Keyboard Command
- Real-time Clock Pulses (8ms intervals)

The CPU identifies the source by polling the data bus each time it receives an IRQ interrupt.

6.1.1.3 Output Generation

From user inputs of output value, frequency, error and calibration constants, the CPU computes a binary value to a resolution of 25 bits. This is used to adjust the mark/period ratio of the Reference Divider switch which ultimately controls the Working Reference Voltage for the output analogue circuitry.

6.1.1.4 Display Refresh

The vacuum fluorescent displays are continuously refreshed by cycling through character data stored in a separate display-image RAM. To alter the display the processor merely alters the contents of the RAM.

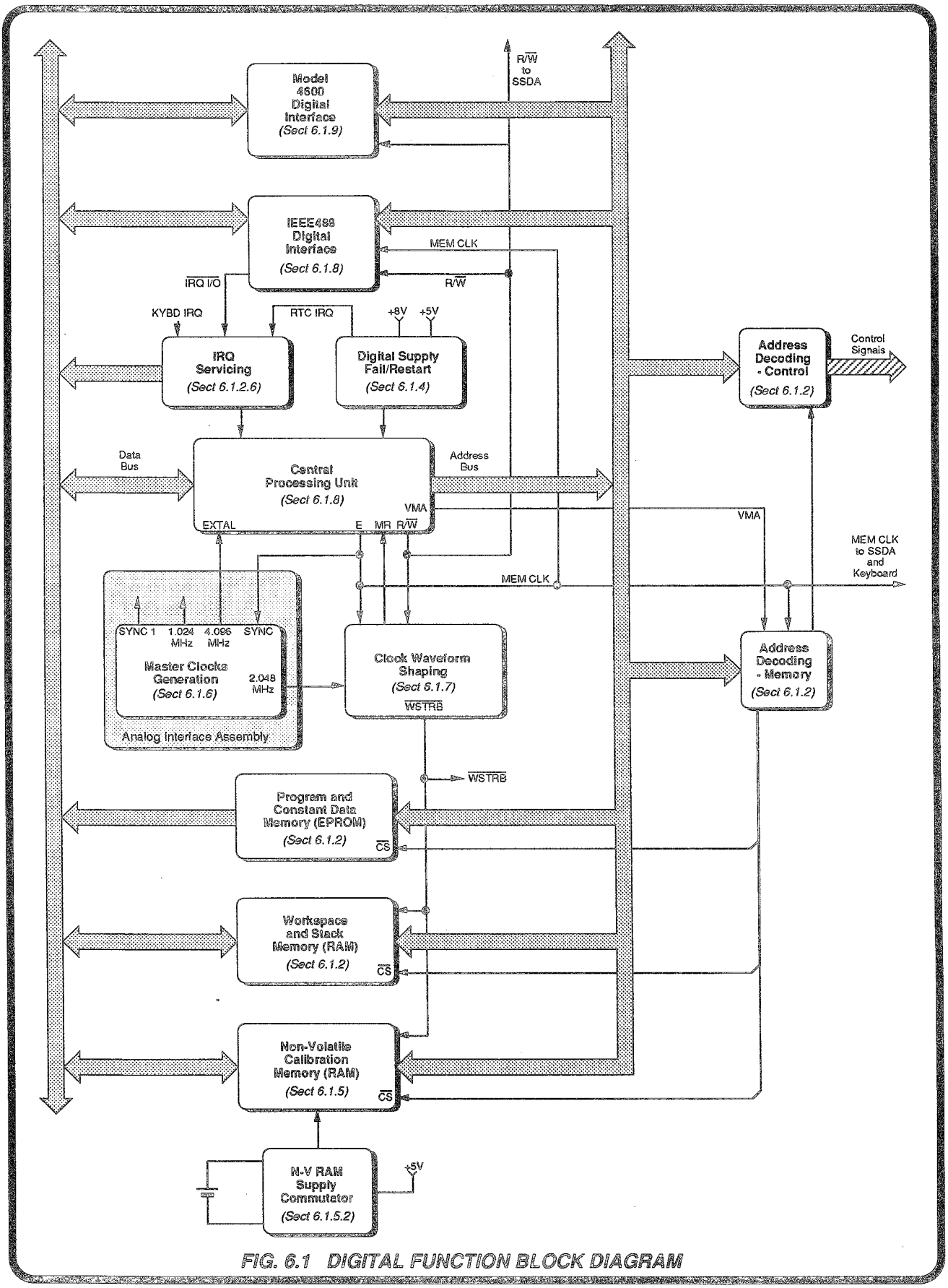


FIG. 6.1 DIGITAL FUNCTION BLOCK DIAGRAM

6.1.2 CENTRAL PROCESSOR and PROCESSOR MEMORY

(Circuit Diagrams 430796 Pages 11.2-2/3)

A 6802 microprocessor (M34), together with its memory, controls communication throughout the whole instrument.

6.1.2.1 Memory

The memory can be split into four main areas, the microprocessor's on-chip RAM not being used:

- **Program Memory** (M18) - defines and controls the operational functions of the whole instrument system.
- **Constant Data Memory** (held in EPROM with the Program Memory) - stores fixed factors used in processing; such as the key mapping tables, and the instrument specification tables that are used in **SPEC** Mode.
- **Non-Volatile Calibration Memory** (M23) - stores all the calibration constants used to correct each output value, which are determined during the 'Autocal' cycle.
- **Volatile Operating Memory** (M22) - used for volatile data storage such as computation results and present output value. This memory is also used for scratch pad operations.

Separate memory is used for special purposes, such as the Display Image RAM M16 (which is synchronously loaded but asynchronously read); the storage areas in the IEEE 488 GPIA (M29) and the Keyboard Interface (U201 on Display Assembly); and the Memory Address decoder PROM (M3). These are described in later sub-sections.

6.1.2.2 Central Processing Unit

(Circuit Diagram 430796 Page 11.2-2)

The MC6802 (M34) is a monolithic 8-bit microprocessor, with interrupt and clock-stretching facilities. It is driven by a single phase 4.096MHz square wave generated by the Master Clock X1 in the Analogue Interface Assembly. (This clock synchronizes the reference divider switch with the processor cycle).

6.1.2.3 Address and Data Lines

Address lines $A_{15\text{-}11}$ are decoded as chip-select signals for the RAM/ROM circuit, lines $A_{13\text{-}Ø}$ are connected to the instrument address bus. Data lines $D_{7\text{-}Ø}$ are linked to the instrument data bus.

6.1.2.4 E, MR and MEMCLK

The 4.096MHz clock input at M34-39 (EXTAL) is divided by four and used as output at M34-37 (E). Although the natural frequency of E is 1.024MHz, the action of the waveform shaping input to M34-3 (MR) reduces it to approx. 680kHz as MEM CLK when certain peripheral devices are accessed (IEEE 488 interface, Analogue Interface and Display assemblies).

6.1.2.5 $\overline{\text{NMI}}$

The internal switch S1 provides a non-maskable hardware interrupt which has two functions.

- With the external CALIBRATION switch set to RUN, $\overline{\text{NMI}}$ initializes the processor system.
- With the CALIBRATION switch set to ENABLE, $\overline{\text{NMI}}$ clears the non-volatile calibration memory (M23) before initializing the processor system.

6.1.2.6 $\overline{\text{IRQ}}$

Any one of three asynchronous Interrupt Request signals are able to activate the maskable IRQ input at M34-4:

- **RTC IRQ** is a real-time clock occuring every 8ms to provide timing information for the processor's monitoring facility.
- **KYBD IRQ** occurs each time a front panel key is pressed. (Note: Not the **Reset** or **Display** keys).
- $\overline{\text{IRQ IO}}$ occurs when the IEEE 488 Interface has a transaction to communicate to the processor.

D1, D2 and Q1 constitute a DTL OR-gate to isolate the IRQ inputs. On receipt of Logic-Ø on pin 4, M34 stores its register contents in stack RAM, saving the current processor environment, and vectors to IRQ service addresses FFF8 and FFF9.

The IRQ Service Routine addresses M51 and M52, setting Logic-Ø at M52-9 which enables the tristate buffers M36 and M37 (at M36-1 and 15, M37-15). This sets IRQ data bits D_5, D_6 and D_7 on the data bus so that the processor can identify the source of the IRQ and select the appropriate sub-routine to service the interrupt request.

The IRQ inputs are released as part of the service sub-routine, and after its completion, the processor recovers its environment from stack RAM and proceeds with the interrupted operation.

6.1.2.7 Software Interrupt

The 6802 will also recognise Opcode 3F on the data bus as an interrupt request ('Implied' addressing mode). This code is hard-wired via R9, R10 and AN3 onto the data bus so that if the CPU tries to access a non-available address, the floating bus will be pulled to 3F, initiating the software interrupt. The CPU vectors to FFFA and FFFB, whose contents cause the 6802 to re-initialize the system.

6.1.2.8 Read-Write Line R/$\overline{\text{W}}$

The processor sets the R/$\overline{\text{W}}$ line to Logic-1 when it is in Read state, and Logic-Ø when it has data to write into the addressed device.

The R/$\overline{\text{W}}$ signal is passed only to the SSDA on the Analogue Interface assembly, and to the IEEE 488 GPIA (M29). All other devices which require read-write control, operate from the $\overline{\text{RD STRB}}$ and $\overline{\text{WRT STRB}}$ signals generated from R/$\overline{\text{W}}$ by M49/50.

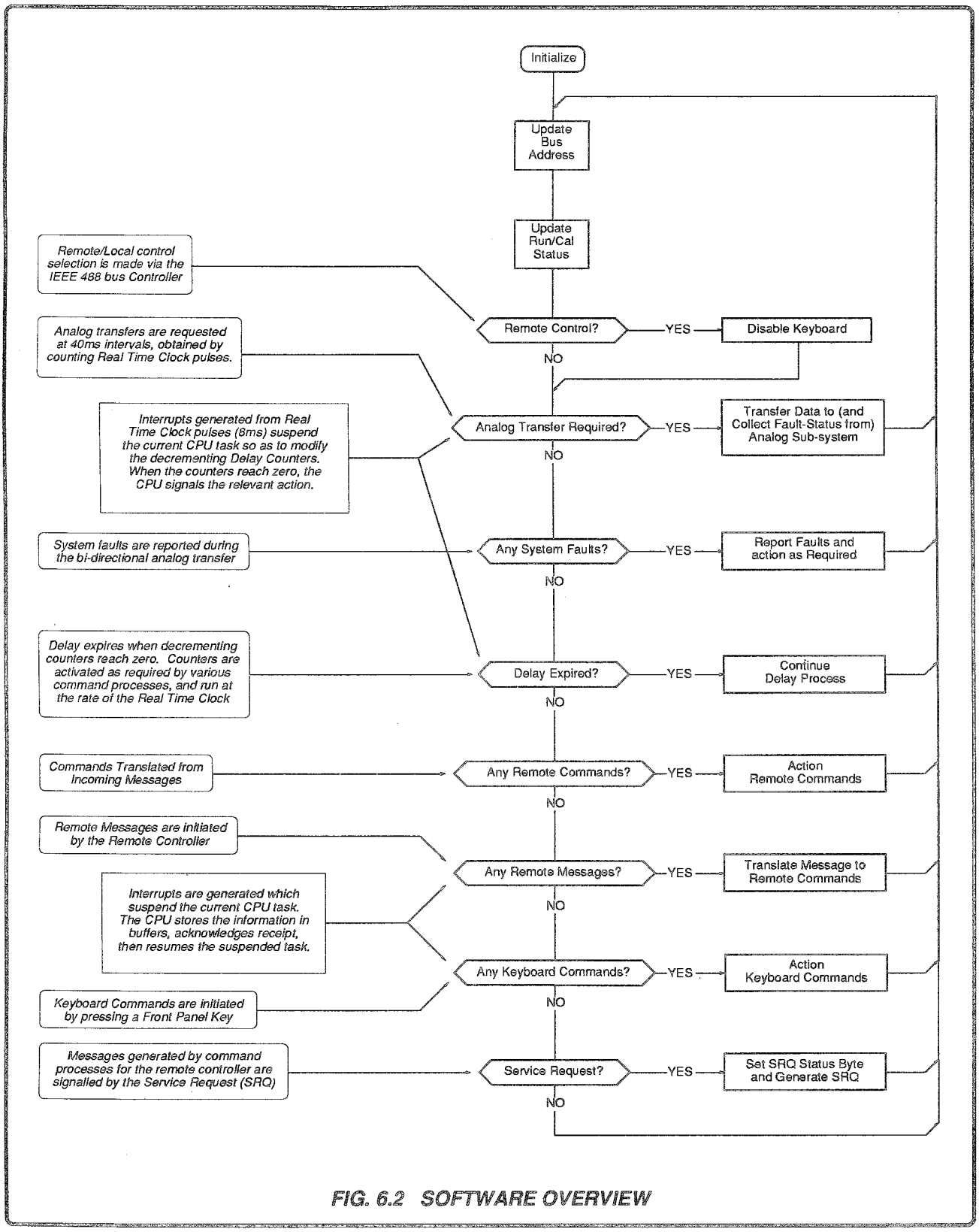


FIG. 6.2 SOFTWARE OVERVIEW

6.1.3 SOFTWARE OVERVIEW

The software management organization is shown in *Figure 6.2.* The machine cycle progresses through the task schedule as illustrated, being interrupted by the demands of activities dependent on real time, and those dedicated to local and remote commands. Real time and command interrupts suspend the current activity of the processor so that the immediate task can be serviced. The processor then resumes the suspended task and continues with the programmed routine, accounting for any alterations introduced by the interrupt.

6.1.4 DIGITAL SUPPLY: FAIL/RESTART CIRCUITRY

Power-up, restart and shut-down of the digital circuitry are performed in a controlled sequence to safeguard against both hardware and software failures. The Safety Monitor ('Watchdog' - *Section6.4.6*) maintains a continuous surveillance of the software management, and shuts down the instrument in the event of a failure either in the digital control circuits or in software management.

6.1.4.1 Power-up Sequence

(Circuit Diagram 430796 Page 11.2-2)

Power-on is first sensed by the Supply Fail Detector circuit. This draws its supplies from the +8V DC unregulated supply, which is the first of the power supplies to rise to a working level. The comparator circuit of M28 has a nominal threshold of +7.1V, above which a good working level of the +5V DC supply is assured.

As the +8V supply rises, but still below +7V, M28-2 follows until the Zener D6 avalanches, when it is held at +2.45V. At this level M28-3 voltage is less than 1V, so M28-1 remains at 0V holding the 'D' input of M8-5 at Logic-Ø and M7-3 at Logic-1. Thus M8 and M9 are held in reset, initiating and maintaining the following states:

a. M8-2 ($\overline{Q}$) at Logic-1, PWR ON RST active. This signal is fed to the Display assembly, holding the keyboard encoder U201 in reset, and disabling the LED cathode driver decoder U203.

b. M6-4 at Logic-Ø, $\overline{\text{PWR ON RST}}$ active. This signal holds the microprocessor M34 in reset state. The VMA output at M34-5 is held at Logic-Ø, disabling address decoder M3, setting all M3 address outputs to Logic-1.

c. The Logic-Ø of $\overline{\text{PWR ON RST}}$ also holds the IEEE 488 GPIA M29 *(page 11.2-4)* in reset. It is also fed to the Analog Interface assembly where it holds the SSDA M44 in reset.

When the +8V supply rises above about +7.1V, M28-3 voltage rises above the +2.45V on M28-2, so M28-1 rises to place a Logic-1 both on M8-5 (D input) and M7-1. M7-3 thus falls to Logic-Ø, removing the resets from 14-bit counter M9 and restart flip-flop M8. So M8 is enabled to receive its clock from M9, which itself starts to count its own 2.048MHz clocks.

At full count, 8ms after M9 is enabled, M9-3 clocks M8. As M8 'D' input is already at Logic-1, this is clocked to M8-1 (Q), with Logic-Ø to M8-2 ($\overline{Q}$). The PWR ON RST and $\overline{\text{PWR ON RST}}$ signals revert to their inactive states, and start-up proceeds:

a. **PWR ON RST at Logic-Ø:**

On the Display assembly, enables keyboard encoder U201 and LED cathode driver decoder U203.

b. **$\overline{\text{PWR ON RST}}$ at Logic-1:**

i. Removes reset from CPU M34, allowing the software to initialize; and also removes the reset from the IEEE bus controller M29 *(page 11.2-4).*

ii. Removes the reset from the SSDA M44 on the Analog Interface assembly.

c. **M8-1 to Logic-1:**

i. Provides an enabling input to M10-1 (See Non-Volatile RAM - *Section 6.1.5*).

ii. Triggers monostable M53-4. This monostable has a relaxation period of 470ms, during which time it holds the $\overline{\text{FP RST}}$ output at Logic-Ø. On the Reference Divider assembly this allows the Watchdog circuits to reset. *(See Section 6.4.6)*

iii. Enables the 'Real-Time Clock' IRQ via M7-13 and flip-flop M8-10. The actions of M9 and M8 interrupt the software routine every 8ms. 'RTC IRQ' sets five external states onto lines D_{4-0} of the Data bus (M36 and M37), and forces the CPU to observe them.

Address decoder M51-5 is normally held at Logic-1, so the Logic-1 at M7-11 and M8-10 allows M9-3 clock to affect the RTC IRQ output at M8-13. For so long as the +8V supply holds above +7.1V, M9 continues cycling through its full count, clocking M8-11 to initiate the RTC IRQ at 8ms intervals.

The CPU terminates each RTC IRQ service sub-routine by addressing M51, pulsing M51-5 (M7-12) to Logic-Ø (Real-time clock reset 'RTC RST). M7-11 and M8-10 are pulsed to Logic-1, resetting M8-13 (RTC IRQ) to Logic-Ø. At the next full count of M9; M8-13 is once again clocked to Logic-1, initiating another RTC IRQ.

Pulses from M9-3 regularly clock the binary state of M8-5 through to M8-1, monitoring the supply status. When running normally, M8-5 and M8-1 are both at Logic-1. If the supply fails, M8-5 reverts to Logic-Ø, but M7-1 at Logic-Ø provides a fast reset setting M8-4 to Logic-1 without waiting for the next clock pulse. M7-3 also resets the 8ms counter to zero count at M9-11.

6.1.4.2 CPU Re-start

(Circuit Diagram 430796 page 11.2-2)

Memory addressing by the CPU is monitored by logic in programmable logic array M3.

In a valid addressing sequence the CPU control and address decode signals are:-

VMA (M34-5) = Logic-1
E (M34-37) = Logic-1
and
one M3 output (M3-13, -14, -16, -17 or -18) = Logic-Ø

For an incorrect addressing sequence the CPU control and address decode signals would be:

VMA (M34-5) = Logic-1
E (M34-37) = Logic-1
and
all M3 outputs (M3-13, -14, -16, -17 or -18) = Logic-1

This situation indicates that the CPU is attempting to access memory locations which do not exist in the 4808, and is most likely the result of a software failure. This condition is detected by the logic in M3, resulting in M3-19 (INV ADDR_L) being set to a Logic-Ø. Via M7-2, this sets M7-3 to a Logic-1 which:-

- Resets counter M9 to zero and flip-flop M8 (M8-4)
- Forces M8-1 to Logic-Ø. This forces M7-11 to a Logic-1, resetting M8 (M8-10) and removing an enable from M10-1. *(See Non-Volatile RAM Section 6.1.5)*
- Forces M8-2 to Logic-1. This change:

  Resets the CPU by M34-40 to Logic-Ø. VMA is forced to Logic-Ø which in turn causes M3-19 to go to a Logic-1, removing the reset from M9-11 and M8-4.

  Makes PWR ON RST and $\overline{\text{PWR ON RST}}$ signals active, thus resetting the other software-controlled areas.

After 8ms from CPU reset, flip-flop M8-3 is triggered from clock M9. M8-1 and M8-2 change state and the start-up sequence proceeds again.

6.1.5 NON-VOLATILE RAM

6.1.5.1 'NV INHIBIT' Signals

(Circuit Diagram 430796 pages 11.2-2/3)

Chip-select to the non-volatile memory M23 is inhibited during power-up, re-start and power-down operations, by the logic signal $\overline{\text{NV INHIBIT}}$ being set to Logic-Ø. During normal running this signal reverts to Logic-1. With the $\overline{\text{NV INHIBIT}}$ signal at Logic-1 (M10-4) during normal running; write access to the NV RAM is available, but only enabled if the calibration security keyswitch on the rear panel is set to ENABLE. The NAND logic gates M10, used to control the inhibit, remain powered from the RAM standby supply after power-down.

Conditions for normal running are as follows:

- Supply fail detector circuit provides a Logic-1 (supplies valid) output to opto-coupler M11. This action causes its optically-coupled transistor to conduct and hold M10-2 at Logic-1.
- M10-8 is held at Logic-1 (to +5V via R6).
- M10-1 is held at Logic-1 by flip flop M8-1.

The above conditions ensure a Logic-1 output from M10-10, the $\overline{\text{NV INHIBIT}}$ signal.

During power-up, $\overline{\text{NV INHIBIT}}$ is held active until the power supplies have settled and the CPU has gained control of memory:

> The input to M10-8 is delayed on the +5V supply by the time-constant C8, R6. Also, the input to M10-1 is held at Logic-Ø by flip-flop M8-1 until the CPU reset is removed.

At power-down, or in the event of a supply failure, $\overline{\text{NV INHIBIT}}$ becomes active before +5V supply fails:

> The first indication of supply failure is made by supply fail detector M28 output going to Logic-Ø. This cuts off the opto-coupler M11 which takes M10-2 to Logic-Ø. M10-8/12/13 are held at Logic-1 by the +5V supply, thus M10-9 is taken to Logic-1 and M10-10 to Logic-Ø ($\overline{\text{NV INHIBIT}}$ active).

In the event of a CPU reset, the $\overline{\text{NV INHIBIT}}$ is made active for the period of reset by the switching action of M8-1 and M10-9.

6.1.5.2 Supply Commutator

(Circuit Diagram 430796 page 11.2-3)

This circuit provides the non-volatile RAM M23 with a battery-driven standby supply when the instrument is in the power-down condition. It also ensures continuity of supply during the change-over period between normal (line) operation and standby, minimizing battery current leakage.

In the power-down condition, the battery powers M10 and M23, returning from battery common (TP13) via D7 and R60. The battery common is isolated from the general common 5A by transistor Q2, which is cut-off.

During power-up, M28 is powered from the +8V supply before the +5V supply voltage becomes established. As long as the +5V supply voltage is less than the battery voltage, Q3-4 is biased negatively, and Q3 is unbalanced in favour of heavy conduction through Q3-6. M28-5 is held low, and M28-6 high as the +5V supply voltage increases, so M28-7 remains at Common-5A potential, and opto-coupler M39 is not energized. Q2 stays off, maintaining isolation of the battery supply from Common-5B. M10 and M23 remain powered from the battery.

As the +5V supply voltage increases, D7 cathode potential rises, reducing Q3-4 bias, reaching zero when the supply voltage is equal to the battery voltage (less than 10mV is developed across R60).

When the +5V supply voltage exceeds the battery voltage, Q3 becomes biased in favour of heavy conduction through Q3-2, pulling M28-6 low and reversing the differential input to M28. M28-7 rises to the +8V rail and energizes the opto-coupler M39, which switches Q2 on, connecting common-5A to the battery common. M10 and M23 are now powered from the +5V supply and the standby battery is isolated by reverse-biased diode D7.

During power down, Q3 compares the +5V supply against the battery, switching Q2 off via M28 and M39 when the +5V supply voltage falls below the battery voltage, and the non-volatile RAM supply commutates to standby battery. Alternatively, Q2 is switched off by failure of the +8V supply to M28 if this occurs before the +5V supply voltage falls below the battery voltage.

Eventually the +5V and +8V supplies both fall to zero, the battery provides the supply to the non-volatile RAM, and battery common is isolated from Common-5A by Q2.

6.1.6 MASTER CLOCK GENERATION

(Circuit Diagram 430648 page 11.3-3)
(Refer to Fig. 6.3 for waveforms)

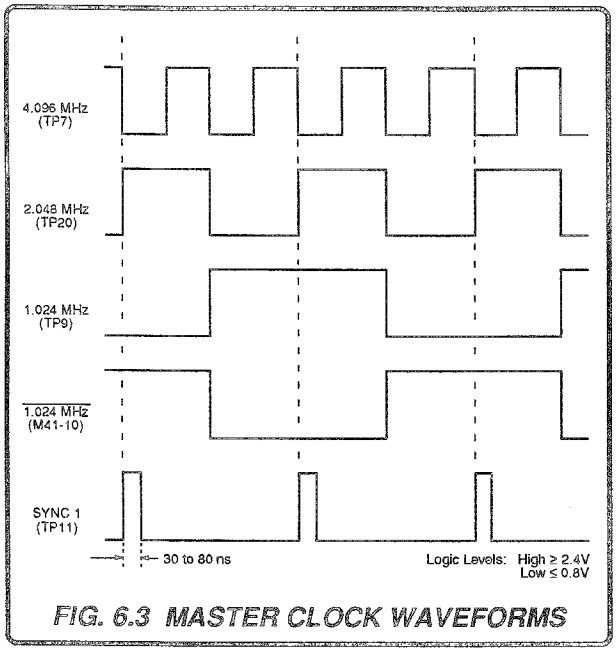


FIG. 6.3 MASTER CLOCK WAVEFORMS

The master clock generator is based on crystal oscillator X1 which provides a precision 4.096MHz squarewave reference frequency output.

The primary frequency of 4.096MHz is divided by JK flip flop stages M41, both of which are connected to toggle when clocked. The first division stage is synchronized at its reset input, M41-3, to the memory clock via flip-flop M42. This ensures correct phasing of the 2.048MHz squarewave output from M41-14.

M41-11 and M41-10 outputs provide complementary 1.024MHz and $\overline{1.024MHz}$ squarewaves respectively. Monostable M40, which is triggered at 2.048MHz from M41-15, provides the positive-going 2.048MHz synchronizing pulses, SYNC1.

6.1.7 CLOCK WAVEFORM GENERATION

(Circuit Diagrams 430796 page 11.2-2 and 430648 page 11.3-3)

NB: As the circuit locations in *Fig 6.4* are clearly marked, and as there are no duplicate designators in the circuits, this description does not refer to a component's location except where necessary.

NOTE: To avoid confusion, the terms 'high' and 'low' are used to replace 'Logic-1' and 'Logic-Ø' respectively in the following description.

The crystal oscillator on the Analog Interface Assembly provides a 4.096MHz Master Clock signal (X1-8) for the whole instrument. This drives the 6802 CPU at M34-39 (EXTAL) — M34-38 not being connected. M41 divides 4.096MHz to generate a 2.048MHz clock for the Memory Clock Stretching Circuit (M35/M49).

The CPU (M34) divides the EXTAL input internally by 4 and outputs the result as E (Enable) at M34-37, to act as a 'Phase 2' Memory Clock for the SSDA on the Analog Interface and the keyboard controller on the Display assembly.

If M34-3 (MR-Memory Ready) was permanently held at +5V, the E signal would be 1.024MHz. But in the 4808, a 'stretching' circuit (M35/M49) doubles the Logic High (+5V) time of E by switching MR to Logic Low (0V) for part of the cycle. This is shown on Fig.6.4.

The frequency of E is thus reduced to approximately 680kHz, with 1µs available for data access to the SSDA, Keyboard Controller, IEEE GPIA and memory.

6.1.7.1 Memory Clock Stretching Circuit

(Fig. 6.4)

The action of M35 and M49 is dependent upon the finite propagation time between clocks at M35-1/M35-6 and Q output at M35-15. When M34-3 (MR) is +5V; M34-37 (E) is toggled by alternate positive-going edges of the 4.096MHz clock, with a propagation delay of approximately 80ns. Also, the 4.096MHz signal is divided by 2 in M41, resulting in 2.048MHz signal whose negative-going edges clock M35. M35 cascade action is controlled by the condition of the Memory Clock (E) and affected by its own propagation times.

6.1.7.2 Shaping Action

(Figs. 6.4 and 6.5)

At T1 and T2: The 4.096MHz clock edge at T1 causes E to rise from low to high at T2. As M35-10 is also high, MR changes from high to low at T2, holding E high. M35 pin state is 4 and 10 high, 9, 12 and 16 low.

At T3: The 2.048MHz falling edge clocks M35, and M35-9 rises to high awaiting the next clock edge (not until T5). M35-10 also remains high, so MR is held low and E stays high.

At T4: MR is still low, so the 4.096MHz clock has no effect on E, and E is stretched.

At T5: MR returns to high when the Logic-1 on M35-9 is clocked as a Logic-Ø to M49-4. This allows the 6802 to toggle E at the next effective clock edge.

At T6: The rising edge of the 4.096MHz clock causes E to fall to low, setting up M35-4 to low, M35-12 and 16 to high. (M35-9 is already high.)

At T7: M35-10 is toggled to high, but as M49-5 is now low, MR remains high to allow E to be toggled at the next effective processor clock edge (not until the next T1). Also at T7, M35-15 is clocked to low to set M35-9 ready for the next (T3) clock edge. The circuit is now set up to its initial (pre-T1) condition so the action repeats.

Note: A remote possibility exists, that a severe disturbance could upset the synchronization of the 'E' signal with the 2.048MHz clock. To guard against this, M42 acts as a monostable to provide negative reset pulses into M41-3. Under all normal conditions, these will occur when M41 is already toggled in its reset state.

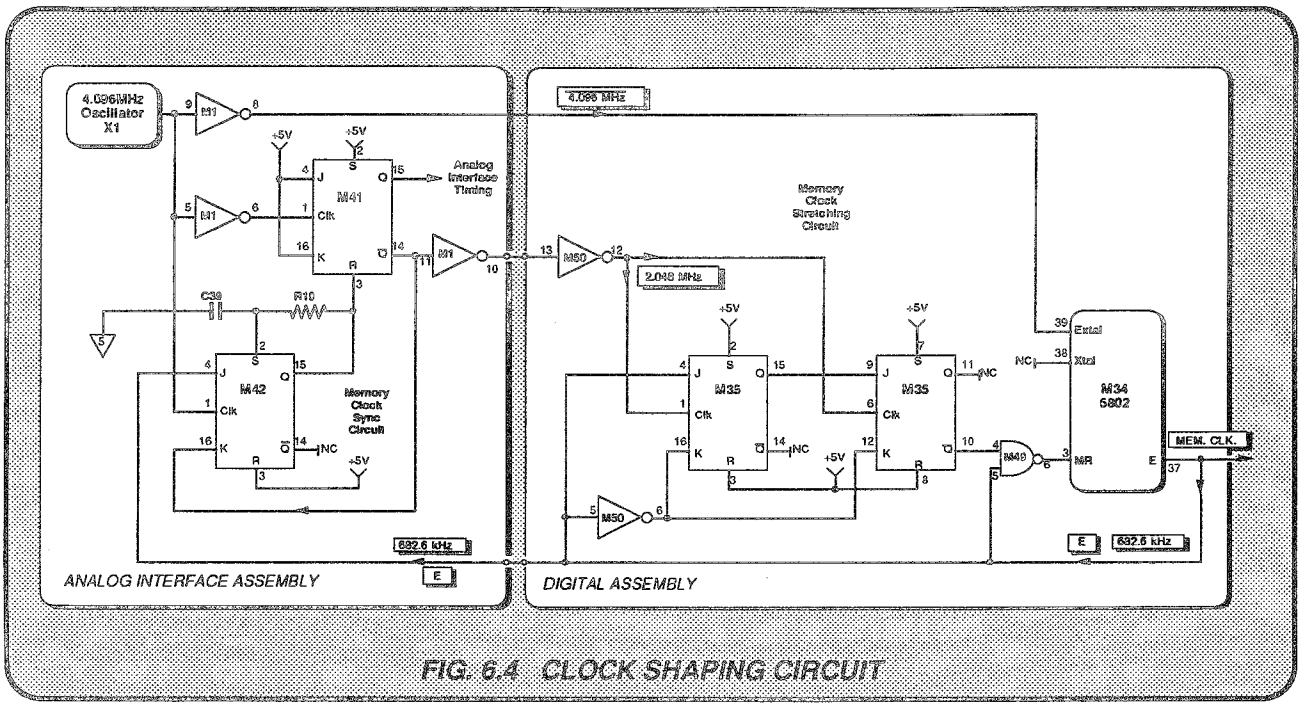
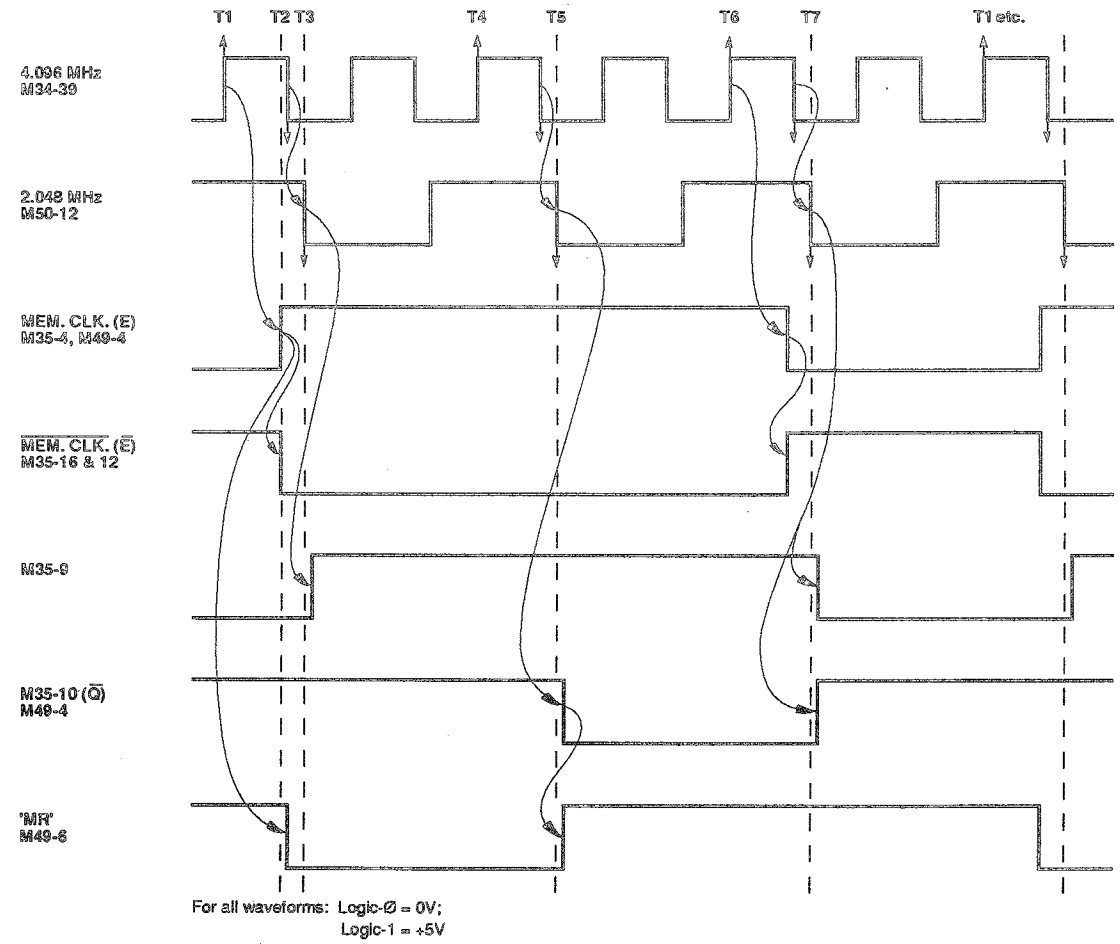


FIG. 6.4 CLOCK SHAPING CIRCUIT



For all waveforms: Logic-Ø = 0V;
Logic-1 = +5V

FIG. 6.5 CLOCK SHAPING WAVEFORMS

6.1.8 IEEE 488 DIGITAL INTERFACE

(Circuit Diagram 430796 Page 11.2-4)

The IEEE Interface circuitry is located on the bottom right-hand corner of the Digital PCB (viewed from the front of the instrument). M29, M40, M47 and M48 execute and decode interface functions, and transfer data input/output.

The General Purpose Interface Adaptor (GPIA) M29, is software-driven by the 6802 CPU, as part of its normal function. M29 is addressed at CS by $\overline{\text{XIOBBD}}$ from M51, and its internal registers are accessed by A_0, A_1 and A_2 from the address bus.

The GPIA is clocked by Memory Clock E, with read or write control direct from the processor R/W signal at M29-5; and at instrument power-on, the signal $\overline{\text{PWR ON RST}}$ from the Restart Generator circuit (M6-4) initializes M29 at M29-19.

Information is passed between M29 and the CPU (M34), via the data bus D_0-D_7. The address switch data is linked to D_0-D_6 by tristate buffers M47. During initialization and at subsequent intervals, the state of M29-4 (ASE) changes from +5V to 0V, enabling M47. The status of the address switches on the 4808 rear panel is transferred into M29 via M47 and the data bus for comparison with the received address.

M40 and M48 are bidirectional bus-driver arrays. The drivers for bus management lines: IFC, ATN and REN are permanently held in Receive state, and the SRQ driver in Transmit state. The EOI line driver is switched from Receive to Transmit by M29-28 ($T/\overline{R}1$) changing from 0V to +5V as required by M29. M29-27 ($T/\overline{R}2$) is normally held at 0V for reception of system data via DIO_{1-8} bus lines, and set to +5V for instrument data to be sent over the bus.

Some system controllers output excessive noise along the REN line. To avoid spurious switching of M29 between Local and Remote control states, the noise is filtered by R58 and C31.

Difficulty has been experienced with certain controllers in that NDAC can transfer data on to the bus too early. Resistor R62 and capacitor C7 slow down the transitions of NDAC to overcome this problem.

M29-40 ($\overline{\text{IRQ}}$) is used to inform the CPU when certain states occur. In particular, the $\overline{\text{IRQ IO}}$ signal is generated at each byte-transfer over the bus, whether the byte is sent or received. Additionally, $\overline{\text{IRQ IO}}$ is activated whenever certain specific commands are received, e.g: 'DAC', 'SPA', and changes between Remote and Local Status.

When the CPU receives $\overline{\text{IRQ IO}}$, it addresses M29's 'Interrupt' Status Register, then M29 identifies the reason via the instrument data bus.

For further information refer to 'Getting Aboard the 488 Bus' published by Motorola, or the appropriate device data sheets.

6.1.9 MODEL 4600 DIGITAL INTERFACE

(Circuit Diagram 430796 Page 11.2-3)

The processor communicates with the external Datron 4600 Transconductance Amplifier using 9 signals in the digital bus. Eight signals are controlled by the processor using the PIA M26, which drives the digital bus via the bus buffer M25. The signal IDIGBUSON is driven from +5V (*circuit diagram 430604 page 11.16-4*) so that the model 4600 may detect that the 4808 is turned on.

The data on the digital bus IAD0 to IAD4 is bi-directional so model 4600 control data can be written from the model 4808, and status information read back. Writing occurs when signal $\overline{\text{IWR}}$ pulses low and reading occurs when the signal $\overline{\text{IRD}}$ pulses low. When $\text{IA}/\overline{\text{D}}$ is low, they are in data mode as described, when high, they are in address mode. The address mode is used during a write or read to determine which address is to be written or read. The 4600 latches the address on lines IAD0 to IAD4 when $\text{IA}/\overline{\text{D}}$ is high and $\overline{\text{IWR}}$ pulses low. All subsequent writes and reads are to this address until another address is latched. The 4600 uses only addresses 0,1,2 and 3. The remaining addresses 4 to 31 are reserved for future expansion.

The processor reads the 4600 status registers each 40ms to check for malfunctions, that the analog bus is connected, and the status of the on/off keys. The digital bus is reset by driving both $\overline{\text{IWR}}$ and $\overline{\text{IRD}}$ low, either by the processor or M24 (ie BARK DEL (OG) is set).

6.2 KEYBOARD

(Circuit Diagram 400994 Page 11.1-1 and Circuit Diagram 400993 Page 11.1-2 and 11.1-3)

The circuitry described in this section performs the following functions:

- Provides front-panel operator control of instrument Output, Function, Range and Mode circuitry, by push-button keys. Key operation is detected internally and transferred to the CPU via the instrument data bus.
- Indicates the present instrument state by means of LEDs fitted in the keys.
- Generates audible warning of errors, failures, and high voltage at the Output Terminals.
  (Also see Circuit Diagram 430648 Page 11.3-3)

In addition a pushbutton switch sets instrument Power ON and OFF *(refer to Section 6.7)* and a 'Reset' key provides a hardware reset for the safety monitor (Watchdog) circuits *(refer to Section 6.4)*. The circuitry is located on the Display PCB Assembly (*400993*) and the Switch PCB Assembly (*400994*), linked to the CPU by control signals and the data bus.

6.2.1 KEY and LED MATRICES

(Circuit Diagram 400994 Page 11.1-1)

The keys are electrically arranged in an 8 x 7 matrix and the LEDs in the keys are electrically arranged in an 8 x 4 matrix as shown in the circuit diagram. These key and LED matrixes, which are situated on both halves of the Switch PCB Assembly, are connected to each other and to the Display PCB assembly via a ribbon cable.

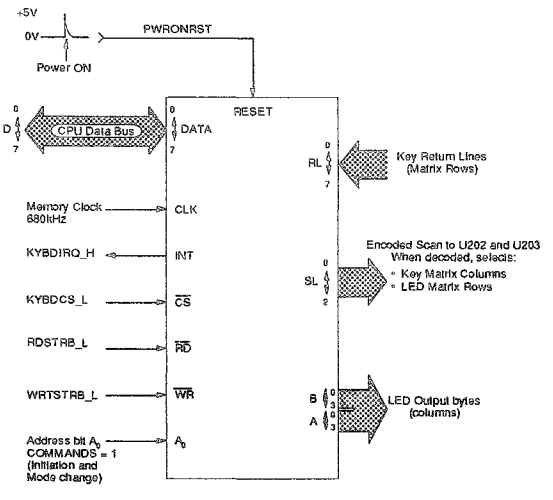


FIG. 6.6 U201 INTERFACE (P8279) - SIMPLIFIED SCHEMATIC

6.2.2 PROGRAMMABLE INTERFACE U201

(Fig 6.6 and Circuit Diagram 400993 Page 11.1-2 and 11.1-3)

U201, a P8279 keyboard/display controller, interfaces the keyboard and LEDs to the instrument data bus. It is addressed by KYBDCS_L from the Digital assembly, to chip-select CS which enables commands or data to flow via the data bus at D_{0-7}. The CPU sets address A_0 to Logic-Ø for data flow; but for programming the interface for mode change or during initialization, A_0 is set to Logic-1.

6.2.2.1 Read/Write Control

The WRTSTRB_L signal from the Digital assembly is applied to WR on U201. Data or Command is input to U201 from the CPU data bus during WR low and CS low, and is latched on the WR positive- going edge.

The RDSTRB_L signal from the Digital assembly is applied to U201 RD. Data is output from U201 on to the data bus during RD low and CS low.

6.2.2.2 U201 Initialization

Switching power on to the instrument causes U201 to be cleared by the PWRONRST pulse from the Digital assembly. The interface is then programmed during initialization as follows:

a. Clock divider set to 'divide by eight': The memory clock (E) at approximately 680kHz is divided by 8 to give an internal clock frequency of 85kHz.

b. An inherent division by 16 reduces the scan clock to 5kHz giving a scan cycling frequency of 333Hz.

c. Encoded Keyboard Scan:
The scan output from SL_{3-0} is a 4-bit count.
SL_3 is not used; SL_{2-1} scans U203, SL_{2-0} scans U202.

d. Keyboard Mode:
The internal keyboard RAM is programmed as FIFO, input being routed via RL_{7-0} return lines. Two-key lockout is employed with debounce.

e. Display Mode:
- Eight character left entry for the LED display.
- Inter-digit blanking: all 1's on B_{0-3} and A_{0-3} between digits.

6.2.2.3 U201 Reprogramming

The frequency **Store** key and the 13 dual ◇ keys have a reprogrammable function. When one of these keys is pressed, U201 is reprogrammed into Scanned Sensor Mode. When released, U201 reverts to Encoded Keyboard Scan ⩓ Mode.

6.2.3 SCAN DECODING

The encoded scan output from U201 (approximately 333Hz cycle frequency at SL_{2-0}) is decoded by U202 to energize each key-matrix column line once every scan cycle. SL_{2-1} scan outputs are also decoded by U203A to energize each LED-matrix cathode driver once in every scan cycle for a period of two digits.

6.2.4 KEY SELECTION

The keys are electrically grouped within a matrix of 8 rows of 7 (Note that the Reset and Display keys are not part of this matrix). This does not conform to their physical grouping on the front panel. Each of the eight return lines RL_{0-7} defines a matrix row, whose seven elements are scanned by U202 (Low active).

The keyboard memory RAM in the P8279 (U201) is an image of the key matrix, internally synchronized to the SL_{2-0} column scan, and receiving row inputs from RL_{0-7}. It thus stores the state of each of the 55 keys. The use of 2-key lockout rejects two or more simultaneous contacts. Any single key depression is debounced, initiating the interrupt KYBDIRQ_H to the CPU which then interrogates the keyboard image RAM in the P8279.

The next action depends upon the key's function:

a. ◇ key pressed:

   i. U201 is reprogrammed into Scanned - Sensor mode for as long as the key is pressed, the CPU acting on the key information.

   ii. If a single ∧ or ∨ key is held down for longer than half a second, the display enters 'auto ◇' mode, running at about 3 digits per second.

   iii. When the key is released, U201 is returned to Encoded Keyboard Scan mode.

b. 'Store' key pressed:

   i. U201 is reprogrammed into Scanned - Sensor mode for as long as the key is pressed, the CPU acting on the key information.

   ii. If an F1 to F5 key is pressed while Store is held down, the appropriate frequency memory location is accessed, and the output frequency is reset to the value in the memory.

   iii. When the Store key is released, U201 is returned to Encoded Keyboard Scan mode.

c. Any other key pressed (but not Reset or Display):

   i. U201 remains in Encoded Scan mode; the scan continues as the CPU is acting on the key information.

   ii. KYBDIRQ_H interrupts are generated only by the low-going edges of the key contact pulses, so U201 remains sensitive to subsequent key depressions.

6.2.5 KEY LED OPERATION

After performing the change requested by the key depression, the CPU changes the bit-patterns stored in U201 internal display RAM. As this is scanned internally in synchronism with the decoded outputs of U203A, each output byte of B_{0-3} / A_{0-3} drives the row of LEDs accessed by U203A output lines.

The bit-pattern of the byte selects the LEDs to be lit in that matrix row:

B_{0-3} / A_{0-3} bits at: Logic-1 = LEDs unlit;
Logic-Ø = LEDs lit.

During changes of output between successive bytes, all the lines from B_{0-3} / A_{0-3} are set to Logic-1 to avoid spurious LED flashes.

The eight power drivers in U206 drive the LED anodes, from a +5V supply regulated by U207. Darlington drivers U202 - U205 drive the LED cathodes.

6.2.6 AUDIBLE WARNING BUZZER

There are two reasons for an audible warning from the calibrator:

- When the instrument enters High Voltage State (>110VDC or >75VRMS). A 4kHz tone is used, pulsed as described in the User's Handbook.
- When an inappropriate selection is attempted, or if any FAIL or Error message is displayed. For this purpose a single 500Hz 'Beeper' pulse is generated.

6.2.6.1 High Voltage State Alarm Control

(Circuit Diagram 400993 Page 11.1-1)

U203B and U209 act as a control latch for the warning buzzer. With ALARM_L at Logic-1 (+5V) U209 remains unchanged; but with ALARM at Logic-Ø (0V) the state of U209 depends on the condition of the A_0 line:

A_0 at Logic-1: the buzzer sounds a tone.
A_0 at Logic-Ø: the buzzer is silent.

The latch is operated at CPU speed. Two ALARM_L pulses are used for each burst of sound. The first, with A_0 at Logic-1, starts the burst; the second, with A_0 at Logic-Ø, ends it.

The waveforms and truth table in *Fig.6.7* illustrate the action of the latch.

During POWER ON initialization, the combination of ALARM_L at Logic-Ø and A_0 at Logic-Ø is applied to U203B to force power-up in the disabled condition.

The 4kHz HF TONE signal at U209-8 originates in the Precision Divider counter which is situated on the Analog Interface Assembly. *(Refer to Circuit Diagram 430648 page 11.3-2).*

The 500Hz LF TONE signal at U209-12 remains at Logic-Ø unless the 'Beeper' in the Analog Interface assembly is switched. *(See section 6.2.6.2).*

Note that A_0 may be used for other purposes when ALARM_L is at Logic-1, but this will not affect the buzzer state.

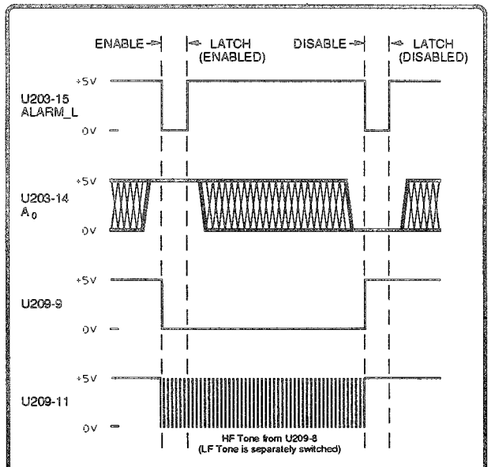
6.2.6.2 'Beeper' Control

(Circuit Diagrams400993 Page 11.1-1and Circuit Diagram 430648 page 11.3-3)

The Alarm Control circuitry on the Display assembly is overridden for Beeper control. During a 'Beep', the HF TONE signal is inhibited, and the LF TONE signal at U209-12 is enabled to control the buzzer output.

On the Analog Interface assembly *(page 11.3-3)* the Beeper consists of a monostable timer and NAND logic. Unless a requirement arises for a 500Hz warning, the $\overline{\text{BEEP}}$ signal is at Logic-1. Thus M55-3 is at Logic-Ø, so M54-5 at Logic-1 inhibits the LF TONE signal, M54-4 remaining at Logic-Ø. M54-8 is at Logic-Ø enabling the 4kHz HF TONE, which is passed to the Display assembly at U209-8 *(page 11.1-1)*.

When required, a single 'Beep' is originated by the CPU pulsing M34-3 *(page 11.3-1)* to Logic-Ø. This is the $\overline{\text{BEEP}}$ signal applied to the monostable M55-2. M55-3 rises to Logic-1 for approx. 150ms until the monostable times out, then reverts to Logic-Ø. M54-8 is at Logic-1 during this period, inhibiting the HF tone and setting M54-11 to Logic-1. This is passed to U209-8 on the Display assembly, where it ensures that U209-13 is at Logic-Ø to override any High Voltage alarm. M54-5 at Logic-Ø enables the 500Hz LF TONE signal to pass via M54-4 to U209-12 on the Display assembly *(see page 11.1-1)*. As U209-13 is held at Logic-Ø during the beep, the buzzer produces 150ms of audible 500Hz output.



U203/U209 Truth Table

U203-15 (ALARM_L)	U203-14 (A_0)	U203-12	U203-11	U209-9	BUZZER
Ø	Ø	1	Ø	1	DISABLED
Ø	1	Ø	1	Ø	ENABLED
1	X	Ø	Ø	NO CHANGE	NO CHANGE

Ø = 0V; 1 = 5V; X = Either 1 or Ø

FIG. 6.7 BUZZER CONTROL LATCH ACTION

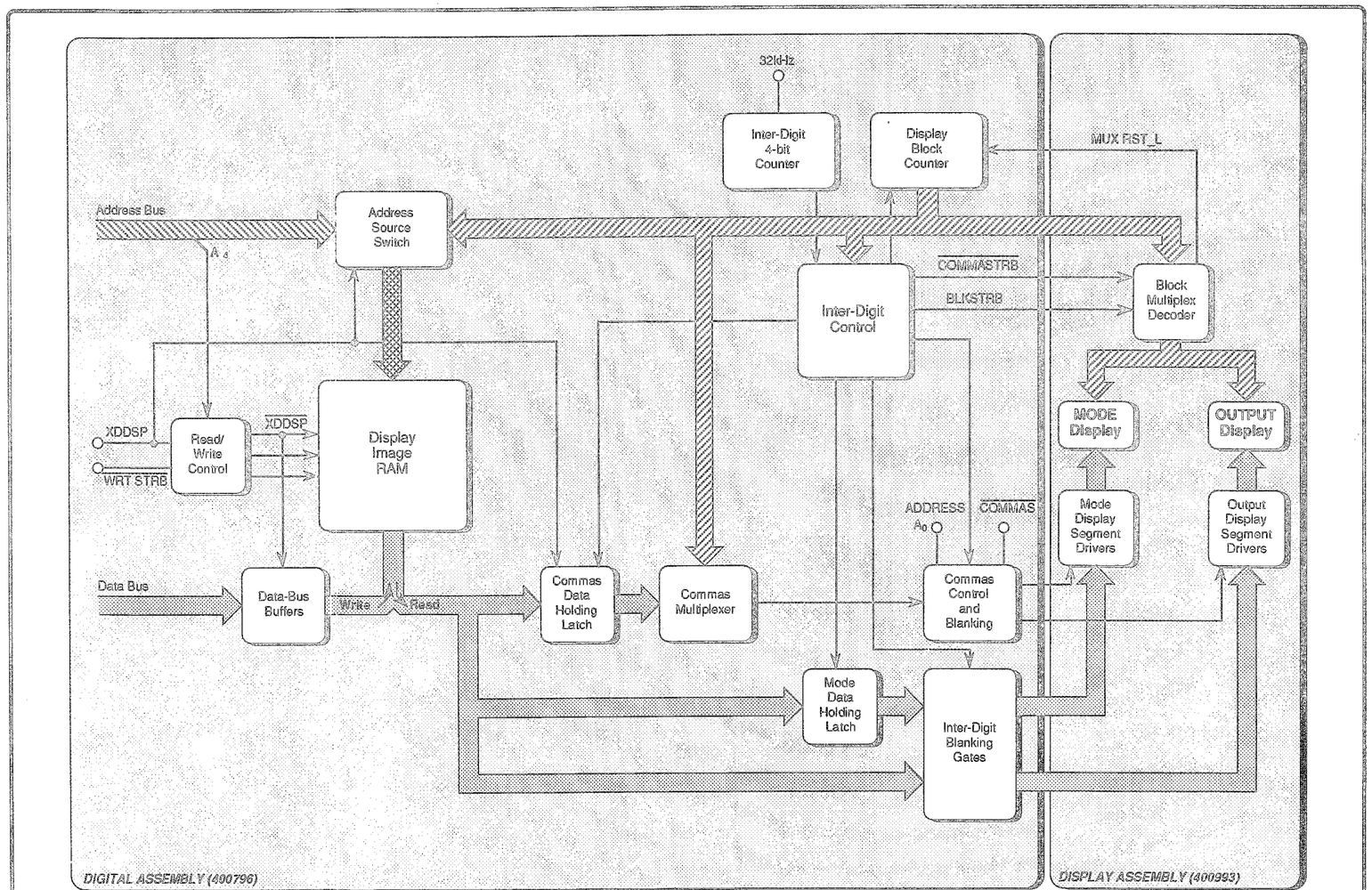


FIG. 6.8 MODE AND OUTPUT DISPLAYS - FUNCTIONAL BLOCK DIAGRAM

6.3 DIGITAL DISPLAYS

The circuits described in this section perform the following functions:

- Storage of display data in a Display Image RAM, updated under CPU control.
- Generation of multiplex count which selects segment data from the RAM, and energizes the appropriate digital blocks in synchronism.
- Distribution of negative supplies to energize the vacuum-fluorescent displays.

Part of the Digital assembly (480796) houses the display multiplexer, which includes the display image RAM, the interdigit and multiplex counters, and control circuitry.

The two vacuum-fluorescent displays, the block multiplex decoder and segment drivers are located on the Display assembly (400993). The block diagram of *Fig.6.8* shows the arrangement and main interconnections of the display circuitry.

6.3.1 GENERAL

(Fig.6.8)

The purpose of the Display Image RAM is to accept and store current display data, which is read out to drive the display segments. The Display Block Counter generates a 4-bit count at 2kHz which scans the 11 digit-blocks of both displays in parallel. The same count scans the RAM, selecting segment information for each block in turn. As there are two displays, and therefore two RAM bytes to read for each block, the 'MODE' display data is first entered into a holding latch during the inter-digit blanking period at the start of the time-slot for its block.

To update the displayed characters, the CPU writes into the RAM at high speed (680 kHz), using signal XDDSP to connect the Address bus through the Address Source Switch to the RAM. XDDSP also connects the Data Bus to the RAM through the Data Bus Buffers, writing the new segment data into the selected RAM Address. The high speed of the transfer, compared with the much slower scanning speed in Read mode, avoids spurious effects appearing on the displays.

Each RAM address contains only 8 bits, but there are nine segments in each display block. Comma-segment information is therefore not written into its normal block address in the RAM, but stored as a bit in a separate 'Commas' byte, which holds the data for all eight blocks having a comma. The byte is read out into a Commas Data Holding Latch, once every block-scan cycle, and then selected for display by a Commas Multiplexer 8-into-1 switch.

6.3.2 STATIC CONDITIONS

(Circuit Diagram 400993 Page 11.1-2)

All vacuum fluorescent display digit/block grids and all the segment anodes are driven from the +5V supply. They are connected to this supply by conduction of the grid and anode drivers in U105, U106, U107 and U108.

When not energized, all grids and anodes are pulled to approximately -34V by 100kΩ resistors connected to the -VDISP supply. The -VDISP supply is generated by voltage doubler circuit D102 - D105/C113 - C115 which is driven from the filament driver U110.

To energize a particular digit/block (simultaneously on both displays), the multiplex decoder causes the relevant grid driver to turn on, lifting the two grids to +5V.

At the same time, the two sets of data (for the characters to be displayed in the two blocks) are extracted from the Display Image RAM, and applied to the segment anode drivers.

6.3.3 WRITE MODE

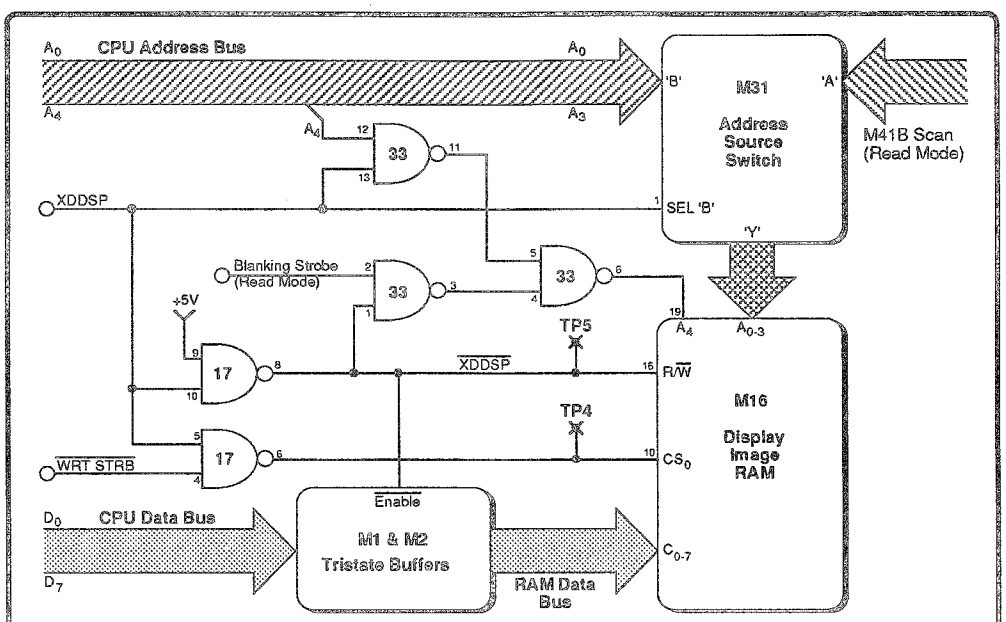


FIG. 6.9 RAM ACCESS - WRITE MODE LOGIC

Whenever the CPU is programmed to update a display (eg. for Range, Function, Mode or Value change) it sets address decode XDDSP to Logic-1 with each byte of data to be transferred. This causes M31 and M33 to select the CPU address lines A_{4-0} which are mapped directly to the RAM address input lines A_{4-0}. The RAM is placed into its write mode by signal XDDSP at Logic-Ø (M17-8, TP5, M16-16).

The RAM M16 is divided into two sections, using the address bit A_4 to differentiate between OUTPUT and MODE display images. When the CPU is loading the RAM with OUTPUT display data, it sets A_4 to Logic-1, passing to set M16-19 (A_4) input to Logic-1. MODE display and COMMAS images are written into M16 with A_4 at Logic-Ø (M33-4 and 13 at Logic-1 in write mode). (In Read mode M16-19 is again used to differentiate between the two image sections).

The signal XDDSP (M17-8) enables the tri-state buffers M1 and M2, connecting the CPU data bus to M16 data input/output lines D_{0-7}. With each byte of display data, the CPU also generates the write strobe signal WRT STRB. This is combined with XDDSP (M17-6, M16-10, TP4) to enable M16 internal Input/Output tri-state buffers to accept the data byte (chip select CS_0). Once the display data has been loaded into the RAM, the CPU returns XDDSP to Logic-Ø and the RAM reverts to Read mode.

6.3.4 READ MODE

Unless the CPU has data to update, the signal XDDSP remains at Logic-Ø, to hold the display multiplexer circuitry in Read mode. The RAM data bus is isolated from the CPU data bus by tri-state buffers M1/M2, and M16 is chip-selected in read mode by M17-6 and M17-8 at Logic-1.

6.3.4.1 Display Scan Address Interlacing

(Circuit Diagram 430796 Page 11.2-1)

M31-1 (SEL) at Logic-Ø causes the RAM to be addressed from the display block scan, mapping M41B outputs: Q4B, Q3B, Q2B, Q1B to RAM address input lines: A_0, A_3, A_2, A_1 respectively. This bit-rotation interlaces the extraction of display data, in synchronism with the interlaced block selection by the Display assembly Scan decoder.

6.3.4.2 Block Multiplex Decoding

(Circuit Diagram 400993 Page 11.1-2 and Figs. 6.11)

The 4-bit Block scan output MUX A_{3-0} from the multiplex scan counter M41B (Digital assembly) is used at $DATA_{4-1}$ input to U101 (on the Display assembly, which decodes it into an active-low 16-line scan S_{15-0}.

To strobe the commas, M3 output S_6 generates the signal COMMA STRB, and its When the count reaches output S_{13}, feedback from this ouput via the MUX RESET_L signal terminates the scan cycle by resetting M41B on the Digital assembly. Count 6 of the multiplex count is decoded at U113-6 to produce the COMMASTRB_L signal, which is fed back to the Digital assembly to control the latching of comma information from the display RAM into a holding register (*see Section 6.3.4.7*).

Eleven of U101's outputs sequentially drive the display grids (both displays in parallel) via level shifters in U105 and U106. As can be seen from *Fig. 6.11*, the interlacing is used to avoid consecutive activation of adjacent blocks.

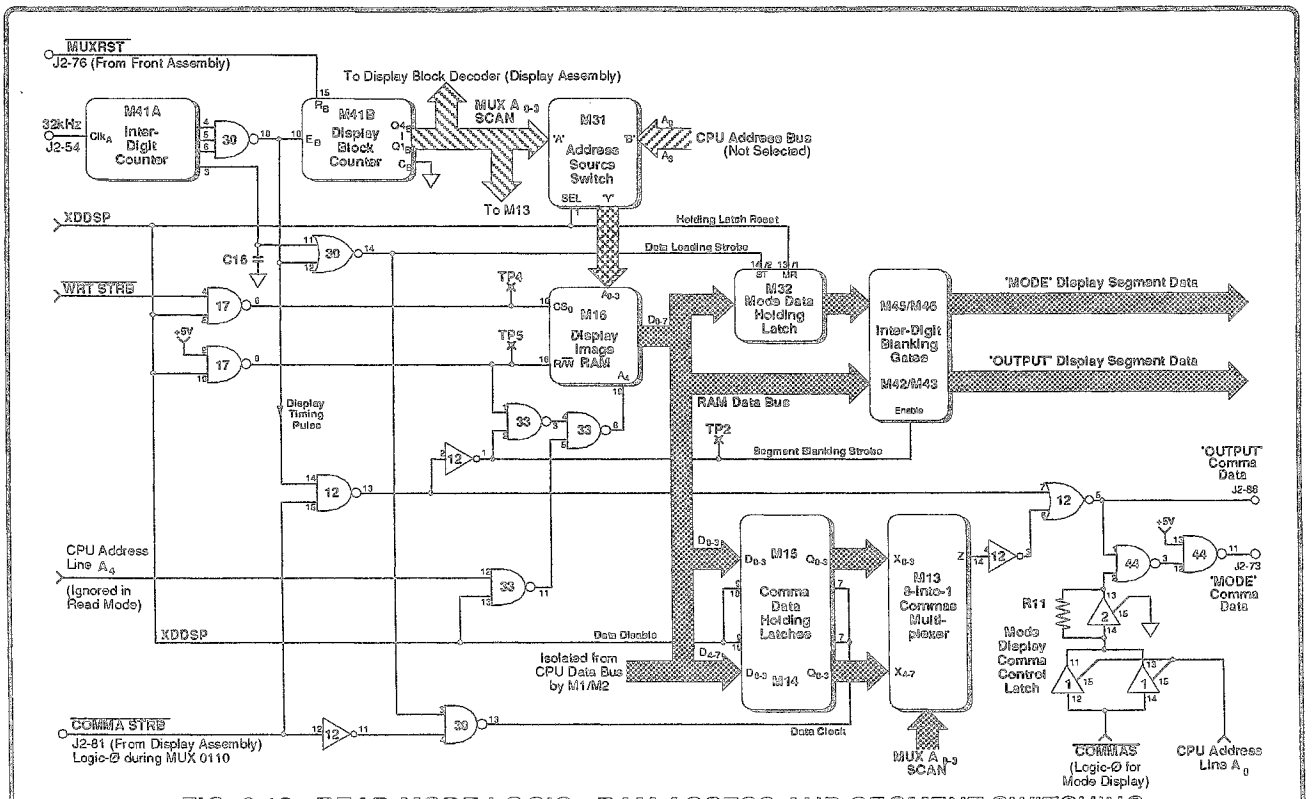


FIG. 6.10 READ MODE LOGIC - RAM ACCESS AND SEGMENT SWITCHING

6.3.4.3 Display Data Selection

(Circuit Diagram 430796 Page 11.2-1)

When the processor writes display data into the Display Image RAM, the A_4 input is used to select the MODE or OUTPUT display data storage area *(see para 6.3.3 and Fig. 6.11)*. In Read mode also, A_4 is set to Logic-1 to read OUTPUT display data, and to Logic-Ø for MODE or COMMA data.

For an alpha-numeric display block, 18 bits of data could be required:

One byte - OUTPUT display block segments;
One byte - MODE display block segments;
Two bits - COMMAS (one for each display).

The problem of transferring two bytes of data along the single-byte RAM data bus is overcome by strobing each MODE display segment byte into a holding latch (M32), during the first 30µs of its block selection time-slot. The MODE display section of the RAM is selected by setting its A_4 input to Logic-Ø for this 'Inter-digit' period, during which the inter-digit blanking gates, (M42/43, M45/46), set all the segment lines going to the Display assembly to Logic-Ø (segments OFF).

COMMA data is stored in the Display Image RAM as a separate byte *(refer to Section 6.3.4.6)*.

MUX A_{3-0} SCAN A_3 A_2 A_1 A_0 / U101 DATA $_{4-1}$ Input D_4 D_3 D_2 D_1 / M16 A_{3-0} input (Display Image RAM -Digital Assembly) A_0 A_3 A_2 A_1	U101 Output 'S' Low Active (Display Assembly)	Display Block Grid Energized, or Signal Selected (for both displays simultaneously)
0 0 0 0	S_0	A1
0 0 0 1	S_1	A3
0 0 1 0	S_2	A5
0 0 1 1	S_3	A7
0 1 0 0	S_4	A9
0 1 0 1	S_5	A11
0 1 1 0	S_6	Not Used
0 1 1 1	S_7	Not Used
1 0 0 0	S_8	A2
1 0 0 1	S_9	A4
1 0 1 0	S_{10}	A6
1 0 1 1	S_{11}	A8
1 1 0 0	S_{12}	A10
1 1 0 1	S_{13}	$\overline{\text{MUX RESET}}$
1 1 1 0	S_{14}	Not included in cycle ($\overline{\text{MUX RESET}}$ at S_{13})
1 1 1 1	S_{15}	

FIG. 6.11 DISPLAY SCAN SEQUENCES

6.3.4.4 Display Timing

(Fig. 6.12)

Read mode is driven by a 32kHz square wave (Waveform 'A', generated from the 13-bit counter in the Analog Interface Assembly M15-11), used as clock for a 4-bit counter (M41A). The three most significant bits are combined at M30-10 to produce Waveform B, the display master-timing pulse, used also for inter-digit blanking.

The following example explains how the display data is set up for the next display block in sequence, during the 62.5µs of the display timing pulse.

Example

Initial State: M41B count has already reached 1001, and the block-4 grids of both displays are energized *(Fig.6.11)*.

The OUTPUT display data for block 4 is selected in the Display Image RAM (M16) to drive the segment anodes for a figure '6', which appears on the OUTPUT display.

Block 4 of the MODE display is showing a figure '3', and the data for this is being output from the MODE display Holding Latch (M32). The data held in M16 for the next byte (Block 6 of both displays) is:

OUTPUT display	-	Figure '8'
MODE display	-	Figure '7'

Block Changeover: The next block is selected during the display master timing pulse *(Fig. 6.12, Waveform B)*.

a. The negative-going leading edge triggers the scan counter (M41B) whose output advances to 1010 (block 6). On the Display Assembly, U101 de-energizes A_4 grids and energizes A_6 grids.

b. For the duration of the Display Master Timing Pulse (Logic-Ø at M12-14), the A_4 input to M16 is set to Logic-Ø as A_{3-0} inputs are advanced to 0101. MODE display data for figure '7' is loaded onto the RAM data bus as follows:

   i. M17-6 at Logic-1 selects M16 at M16-10,

   ii. M17-8 at Logic-1 holds M16 in Read mode,

   iii. RAM address A_{4-0} = 00101 reads MODE display block 6 data onto the RAM data bus (M1/M2 isolates from the CPU data bus),

   iv. M30-14 at Logic-1 strobes the byte into M32 during the 30µs of Waveform D, then returns to Logic-Ø leaving figure '7' data latched at M32 output.

   v. M12-1 at Logic-Ø blanks the two displays by setting M45/M46/M42/M43 outputs to Logic-Ø, regardless of their inputs from M32 and the RAM data bus.

c. The positive-going edge of Waveform B lifts the RAM A_4 input (M16-19) to Logic-1, addressing the OUTPUT display section of memory. A_{3-0} is still at 0101, selecting block 6 display data (in our example a figure '8') which it loads on to the RAM data bus.

   The end of the master timing pulse also releases the blanking by enabling gates M42/M43/M45/M46, so the data for both MODE and OUTPUT displays are now delivered to the anode drivers on the Display assembly.

   This condition persists for 437.5µs until the next master timing pulse, when Waveforms B and C repeat the process for the next block of stored display data.

At any time during the cycle, the CPU may force Write mode. This will not disturb the scan from M41B, but XDDSP will reset M32 outputs to Logic-Ø (M32-1/13). However, the speed of byte transfer from the CPU ensures that the data being transferred is not visible on the displays. Subsequently, each block will be driven by its new stored data.

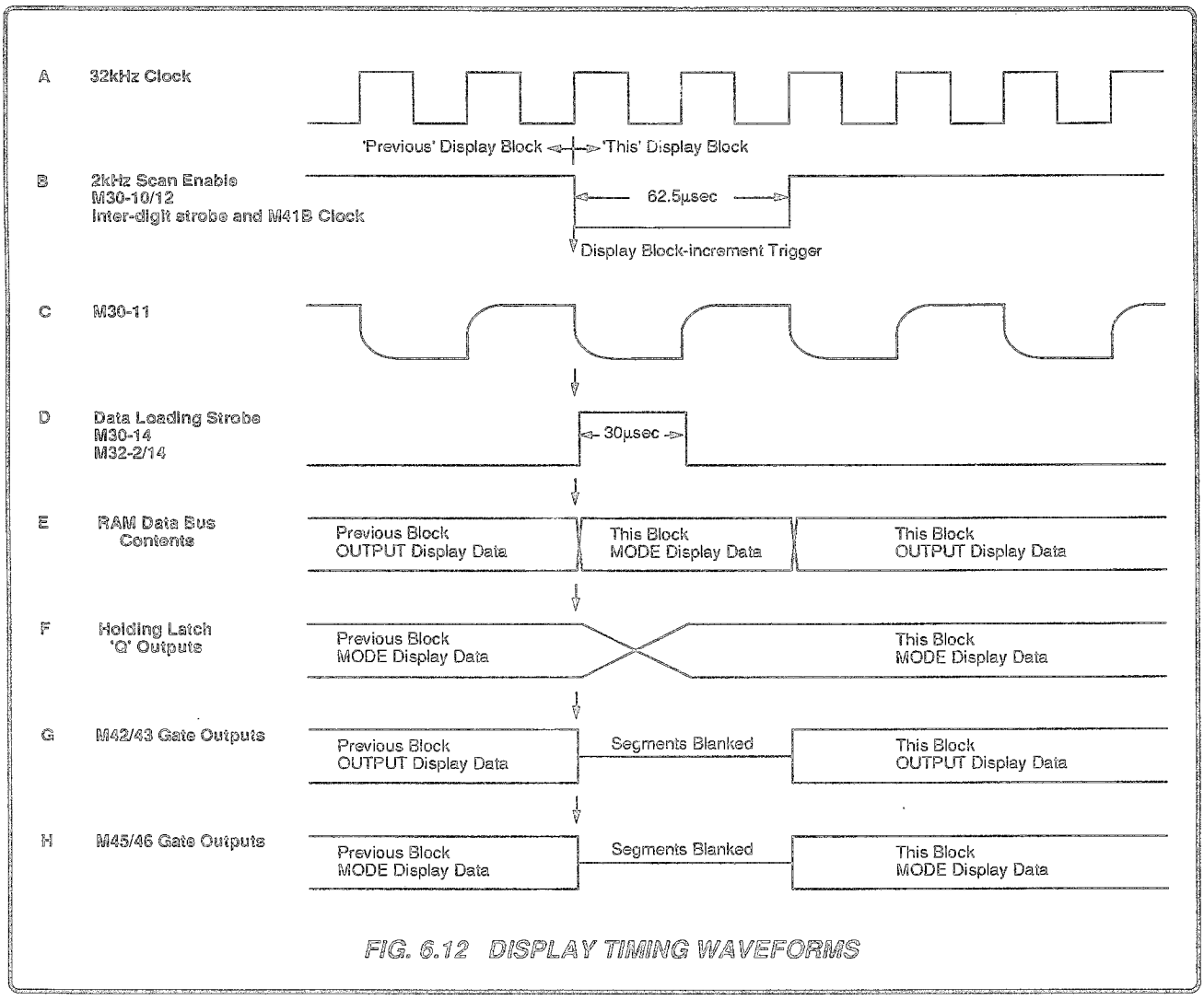


FIG. 6.12 DISPLAY TIMING WAVEFORMS

6.3.4.5 Display Segment Drive

(Circuit Diagram 400993 Page 11.1-2)

The strobed segment signals from the Digital Assembly are input to the Display assembly on J102 and J103. These are already synchronized to their blocks by the 4-bit block scan MUX A_{3-0} within the Digital assembly.

For each block in sequence, the appropriate segment bit-pattern is set at the input to the segment anode drivers in U106, U107 and U108. The correct block grid is simultaneously switched to +5V by its grid driver, lighting the appropriate digit. For bits at Logic-Ø the anode drivers remain off.

The above action proceeds for both displays simultaneously. The grid driver energizes its corresponding block grid on both displays, at the same time as the anode drivers are loaded with the correct block bit-pattern for their own display.

During change-over between blocks, all segment inputs at Logic-1 are returned to Logic-Ø by the inter-digit blanking strobes M42/43/45/46 on the Digital assembly. This turns off the drive transistors and blanks the display. The high scan frequency and persistence of the operator's vision prevents the blanking being observed on the display.

6.3.4.6 Comma Logic

(Circuit Diagram 430796 Page 11.2-1)
(Figs. 6-10 and 6.13)

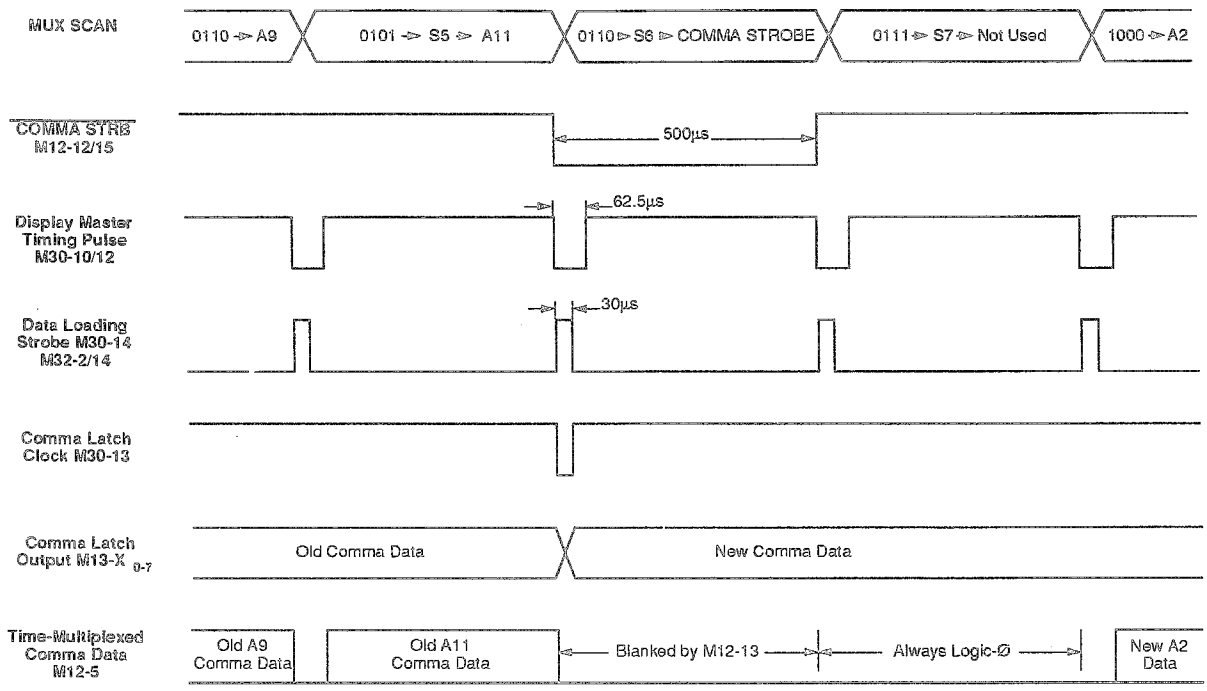


FIG. 6.13 COMMA LOGIC - TIMING WAVEFORMS

The comma is the ninth segment (*i*) in each of the numerical display blocks. It cannot fit into a block's byte in memory, as there are only eight bits per byte. But all the comma information can be stored in a single byte of memory in the RAM (RAM address 01100). This is possible although there are nine numerical blocks, because the ninth block never requires a comma. Legend blocks A_{10} and A_{11} do not have a segment *i*.

The RAM COMMA data is updated by the CPU in Write mode, and is read out (as though it were another display block) by M41B scan 0110 during the master display pulse (Waveform B sets RAM A_4 input to Logic-Ø). The same MUX combination 0110 is decoded at U113-6 on the Display assembly to generate the $\overline{\text{COMMA STRB}}$ signal (COMMASTRB_L on the Display assembly).

Thus for the duration of the MUX combination 0110, the COMMA data is on the RAM data bus, but the blanking gates prevent it reaching segments *a* to *h*.

6.3.4.7 Comma Drive Multiplexing

The $\overline{\text{COMMA STRB}}$ signal is inverted and combined with the Data Loading Strobe at M30-13 as a Logic-Ø pulse, whose positive-going edge clocks the comma data into latches M14/15, approximately 30µsec after it has been loaded on to the RAM data bus. The permanently-enabled ouputs from these latches are input as X_{0-7} into the 8-into-1 multiplexer M13 during a complete MUX scan until the next COMMA STRB signal.

The block-multiplex scan from M41B selects the correct X input to synchronize with activation of its display block grid. This is output from M13-14 (Z), into blanking gates M12.

Comma information is blanked during $\overline{\text{COMMA STRB}}$, and by inter-digit blanking during display-block change-over (M12-7).

The Comma drive line from M12-5 to the front panel, via J2-88, controls the segment *i* anode driver for the OUTPUT display.

If commas are required on the MODE display (e.g. in 'Spec' operating mode +Lim or -Lim) they will always be in the same display blocks as the OUTPUT display. When this mode is selected, the CPU pulses the COMMAS line to Logic-Ø at the same time as Address line A_0 goes to Logic-1. Tristate buffer outputs M1-11 and 13 go to +5V, setting M2-13 output to +5V (Logic-1). Outputs M1-13 and M1-11 go tristate when the COMMAS line returns to Logic-1, leaving M2-13 latched to +5V by the positive feedback action of R11. So M44-2 enables the comma data to the MODE display segment driver, via J2-73, to copy the OUTPUT display commas on to the MODE display.

When MODE display commas are not required, Logic-Ø (0V) is set on A_0 with COMMAS signal at Logic-Ø. Thus M2-13 latches to Logic-Ø and M44-2 disables the flow of comma data to the MODE display.

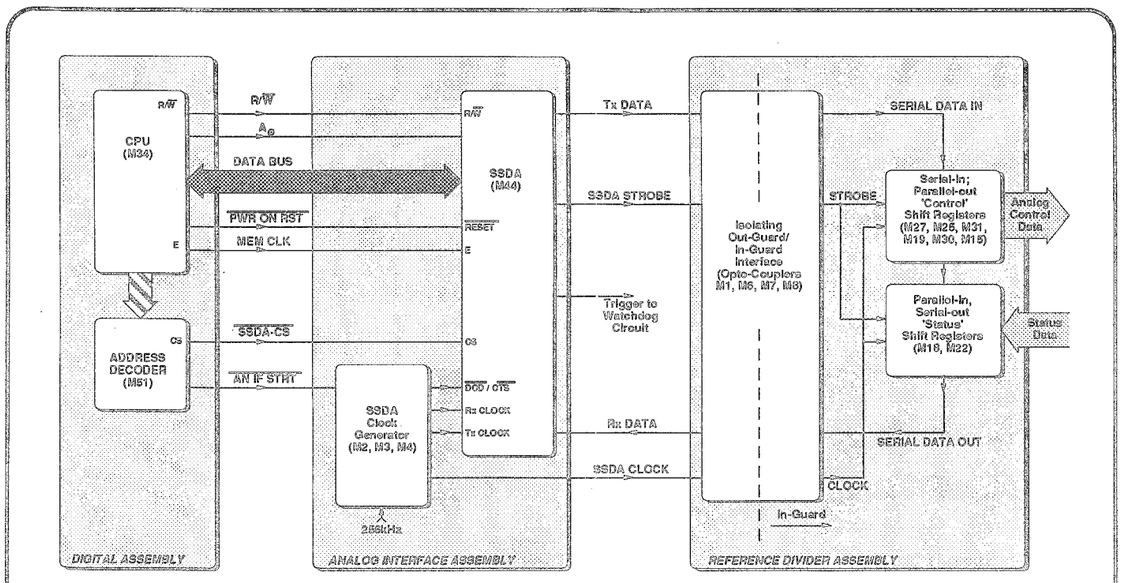


FIG. 6.14 SERIAL DATA LINK - SIMPLIFIED FUNCTIONAL BLOCK DIAGRAM

6.4 ANALOG CONTROL INTERFACE

The circuitry described in this section performs the following functions:

- Provides a two-way interface via a serial data link between out-guard digital processing and in-guard analog control circuitry on the reference divider assembly *(see Fig. 6.14)*.

- Monitors the CPU operation, serial transfer, digital supply failure and restart operations (watchdog), imposing a controlled safety default condition if there is a danger of losing digital control of the analog functions.

A manual reset of the safety monitor is provided on the front panel *(see Fig. 6.17)*.

6.4.1 GENERAL

Safety and Control information is input from Digital *(Circuit Diagram 480796)* and Front *(Circuit Diagram 400993)* Assemblies to out-guard circuits located on the Analog Interface Assembly *(Circuit Diagram 480648)*, processed and transferred across the 'Guard' isolation barrier to in-guard circuits in the Reference Divider Assembly *(Circuit Diagram 480652)*. After further processing in the Reference Divider Assembly, safety and control information is output to the following assemblies:

- Sine Source Assembly *(Circuit Diagram 480446)*
- AC Assembly (*Circuit Diagram* 400844)
- PA Assembly (*Circuit Diagram* 480618)
- DC Assembly (*Circuit Diagram* 480536)
- Current *(Circuit Diagram 401008)*, Ohms *(Circuit Diagram 401047)* or Current/Ohms Assembly *(Circuit Diagram 480614)*
- High Voltage Assembly *(Circuit Diagram 480537)*

Certain selected 'Status' signals, originating in the analog assemblies, are returned to the CPU during the data transfer. Thus, the data link forms a continuous loop, as shown in *Fig.6.14*.

6.4.2 SERIAL DATA TRANSFER

(Circuit Diagrams: 430796 Page 11.2-2, 430648Page 11.3-3, 430652 Pages 11.4-4 and 11.4-5 and Fig. 6.14))

A bi-directional serial data link passes information across the guard isolation screen; passing CPU commands to control the in-guard analog circuitry, and returning critical status signals from the guarded circuits back to the CPU.

The link is managed by a synchronous serial data adaptor (SSDA) which, having first been loaded with three bytes of control instructions by the microprocessor; transmits the resultant 24-bit word across guard one bit at a time, via its Tx DATA channel.

The 48 bits necessary to control the analog circuitry thus require two successive 24-bit transmissions.

Simultaneously with each 24-bit transmission, the SSDA receives a 24-bit word via its Rx DATA channel, enabling the CPU to parity-check its returned data, and obtain the status of the analog functions.

6.4.2.1 The Transfer Cycle
(Fig. 6.14)

The CPU uses an address-code signal $\overline{\text{ANI/F STRT}}$ (Analog Interface Start) to initiate each 24-bit shift, by triggering a separate clock generator (M2, M3, M4) which produces a burst of 24 clocks per shift. Data is clocked in a serial string through a continuous loop comprising:

- the 48-bit, serial in/parallel out, analog control shift register;
- the 16-bit, parallel in/serial out, status shift register;
- back to the SSDA receiver (Rx DATA).

The serial data string is correctly located after two 24-bit shifts, so then the SSDA generates a strobe pulse which:

a. Transfers the data present in the serial data string of the six 8-bit analog-control shift registers (M27, M25, M31, M19, M30, M15) into their enabled parallel output registers and onto the analog control bus.

   When the strobe ends, further transfer is disabled and the registers' output data is latched.

b. Injects the status data at each of the 8-bit parallel inputs of the two status shift registers (M18, M22) into corresponding locations in the serial data string.

   When the strobe ends, the parallel inputs to the status registers are disabled.

After the strobe pulse, the CPU initiates a further circulation of serial data (including the status data), in order to obtain the status data and return the analog control bits to the SSDA Rx DATA register for parity checking by the CPU.

This extra (confirmatory) circulation requires three more 24-bit shifts, so a complete data transfer consists of five shifts. If no error is detected, the SSDA provides a trigger-enable to allow updates to prevent activation (BARK) of the watchdog circuits.

If an error is detected on the first transfer, the CPU activates a second complete transfer, and then a third if an error is detected on the second. If the error persists after the third transfer, the trigger-enable is withheld, and the instrument will shut down under the control of the 'Watchdog' safety monitor.

All interfacing between out-guard and in-guard circuits is achieved using electrically-isolating opto-couplers.

6.4.2.2 Data Transfer Organization
(Fig. 6.15)

Data is transferred serially via the SSDA, control registers and status registers as directed by the CPU.

The exchange of data between the CPU and SSDA is made in bytes of 8 bits on the instrument data bus, each exchange comprising three bytes (24 bits) of parallel data.

The shifts of serial data through the in-guard circuit are synchronized by clocks which are controlled from the CPU, and the SSDA Rx return registers are cleared when read by the CPU.

Once the in-guard serial data is correctly positioned at the inputs to the control registers, the SSDA generates a strobe which enables its transfer to the parallel outputs of the control registers. The same strobe enables injection of the data on the parallel inputs of the status registers into the serial data string.

The transfer operation requires five serial data shifts, each of three bytes, through the registers. During this operation: the control registers are loaded with bytes of new data (ND); the status registers are loaded with new status data (NS); and the whole of the ND and NS data is returned to the CPU, which:

a. verifies that the analog control bits of the serial data string return to the SSDA Rx DATA register without error. This indicates that at least, the correct bit pattern was applied to the analog control register inputs at the time the strobe was generated.

b. acts upon the status data received.

6.4.2.3 Transfer Sequence

The sequence of events in the transfer operation is as follows, referring to *Fig. 6.15*:

a. Three bytes of new data, ND1, ND2 and ND3 are loaded into the SSDA transmitter registers; this data is destined for control registers D1, D2 and D3. The SSDA receiver registers were cleared when last read by the CPU.

b. A burst of 24 clock pulses, initiated by the CPU, shifts all data three bytes to the right. After the shift is completed, the transmitter registers are loaded with new data bytes ND4, ND5 and ND6 (destined for control registers D4, D5 and D6). During this period, no transfers are made between the serial data string and the parallel control or status registers.

c. A second burst of 24 clock pulses again shifts all data three bytes to the right. New data bytes ND1 to ND6 are now correctly positioned in control registers D1 - D6. After completion of the shift, three dummy bytes are loaded into the transmitter registers. Old data in the receiver register is ignored.

d. With new data bytes ND1 to ND6 correctly located, the SSDA generates a strobe pulse. This pulse:

   i. latches the 48 bits of bytes ND1 to ND6 at the parallel outputs of control registers D1 to D6;

   ii. enables the parallel inputs of status registers S1 and S2, loading two new status bytes NS1 and NS2 and clearing old data OD5 and OD6 from the registers.

e. A third burst of 24 clocks again shifts all data three bytes to the right. The CPU reads bytes NS1, NS2 and ND1 from the SSDA receiver registers (the CPU may take immediate action on NS returns). After the shift is complete, new data bytes ND1, ND2 and ND3 are re-loaded into the transmitter registers.

f. A fourth burst of 24 clocks again shifts all data three bytes to the right. The CPU reads bytes ND2, ND3 and ND4 from the receiver registers. After the shift is complete, new data bytes ND4, ND5 and ND6 are re-loaded into the transmitter registers.

g. A fifth burst of 24 clocks again shifts all data three bytes to the right. Bytes ND5 and ND6 are read from the receiver registers. The CPU has now read all new data and status bytes and the transfer sequence ends. If an error is detected between new data transmitted and new data received, the transfer process is repeated; three attempts are allowed before a fault condition is declared.

6.4.3 SYNCHRONOUS SERIAL-DATA ADAPTOR

(Circuit Diagram 430648 Page 11.3-3)

6.4.3.1 SSDA Initialization

When power supplies are first switched on or an external reset signal EXT RST is applied, the signal $\overline{\text{PWR ON RST}}$ (Power On Reset) is held at Logic-Ø for approximately 8ms.

During this period, the SSDA is latched in a reset condition to prevent erroneous output transitions at its Tx and Rx interfaces; the internal transmit registers are inhibited to prevent the loading of data from the data bus and the SSDA strobe output is held at Logic-1.

After $\overline{\text{PWR ON RST}}$ returns to Logic-1; the instrument state is initialized by the firmware program. This routine clears the latches, registers and SSDA strobe.

6.4.3.2 Parallel Data Input From CPU

The conditions for parallel data on the data bus to be accepted by the SSDA are as follows:

a. Chip-select $\overline{\text{SSDA CS}}$ at Logic-Ø.

b. Read/Write command $\overline{\text{R/W}}$ at Logic-Ø. This controls the direction of data flow via the Data Bus through the SSDA input/output port. When $\overline{\text{R/W}}$ is at Logic-Ø, data on the Data Bus is written into a selected register within the SSDA.

c. The memory clock 'MEM CLK' 682.6kHz square wave synchronizes the SSDA operating cycle to that of the CPU.

With register address bit A_0 at Logic-1 and input conditions present as above, the SSDA accepts data from the data bus into a 3-byte internal FIFO register. The data is entered over several MEM CLK cycles and stored in the FIFO register in readiness for serial transmission from the SSDA.

When the address bit A_0 is at Logic-Ø, data transferred into the SSDA are recognised as programming instructions. The SSDA is programmed as part of the initialization routine. For details of 'Control Byte' operation, refer to Motorola 6852 data sheet.

6.4.3.3 Parallel Data Output to CPU

The conditions for data to be read back from the SSDA on to the data bus are as follows:

- Chip-select $\overline{\text{SSDA CS}}$ at Logic-Ø.
- Read/Write command $\overline{\text{R/W}}$ at Logic-1.
- Memory clock, MEM CLK, present.

The data read from the SSDA may be from one of two sources, selection being made by address bit A_0:

- With A_0 at Logic-1, received data from the serial data input FIFO is transferred to the data bus.
- With A_0 at Logic-Ø, the CPU reads an internal SSDA status register.

6.4.3.4 Serial Data Transmission

Serial data transmission is controlled by the $\overline{\text{CTS}}$ (clear to send) input to the SSDA. Transmission is inhibited by $\overline{\text{CTS}}$ at Logic-1, and enabled when $\overline{\text{CTS}}$ is set to Logic-Ø by the CPU address-code signal $\overline{\text{ANI/F STRT}}$. The first serial bit is transmitted by the negative transition of the first full positive Tx clock pulse (256 kHz) after $\overline{\text{CTS}}$ has been set to Logic-Ø. $\overline{\text{CTS}}$ is held at Logic-Ø by the $\overline{\text{ANI/F STRT}}$ latch for the duration of 24 full Tx clock pulses, thus enabling the serial shift transmission of the 24 data bits from the Tx Data FIFO in the SSDA.

6.4.3.5 Serial Data Reception

Serial data is received by the SSDA, controlled by the $\overline{\text{DCD}}$ (data carrier detect) level and clocked by Rx CLOCK. $\overline{\text{DCD}}$ is common to the transmit control $\overline{\text{CTS}}$ so that transmission to, and reception from the serial/parallel shift registers is synchronous. Both Rx CLOCK and Tx CLOCK have the same frequency but Rx CLOCK is inverted with respect to the latter. The first bit arriving at its Rx DATA input is clocked into the SSDA Receive FIFO register on the positive transition of the first full Rx clock after $\overline{\text{DCD}}$ is set to Logic-Ø.

6.4.4 SSDA CLOCK GENERATION

Serial data is transmitted and received in bursts of 24 data bits. Three clocks are used to time the flow of bits, ensuring that:

- Data has time to settle before being clocked along the shift registers.
- The first Rx data sample is taken before it is lost by the first bit-shift.
- Subsequent Rx data has time to settle before being sampled by the SSDA.
- Exactly 24 bits are shifted in each burst.

6.4.4.1 SSDA, Tx and Rx Clock Action *(Fig. 6.16)*

The three clocks are derived from the 256 kHz square wave output from the 13-bit counter. The 256 kHz squarewave is used directly as the signal 'Tx CLOCK' into the SSDA. *(Refer to Circuit Diagram 430648 Page 113-2 - M15-14).*

After $\overline{\text{CTS}}$ is set to Logic-Ø, the negative transition of the first full positive pulse triggers the first serial Tx data bit setup. *(Refer to Fig. 6.16 Waveforms G and H).*

'Rx CLOCK' is an inverted version of the 256kHz squarewave. After $\overline{\text{DCD}}$ is set to Logic-Ø, the positive transition of the first full Rx clock cycle triggers the SSDA. The SSDA thus samples the first Rx data bit before the SSDA clock triggers the shift registers. *(Fig. 6.16 Waveforms K and J).*

'SSDA CLOCK' is also an inverted version of the 256kHz squarewave. The inversion allows approximately 2ms of data setup time for all serial data bits prior to clocking the data along the shift registers. SSDA CLOCK is gated at M2-3 by the action of M3-12 to ensure that the first Rx data is sampled before it is lost by the first bit-shift. 24 clock pulses are counted by M4, allowing 24 bits to be shifted before resetting the Analog Interface Start latch M2-11 (TP3) to Logic-1. *(Refer to Fig. 6.16 Waveform I).*

6.4.4.2 SSDA Clock Circuitry *(Circuit Diagram 430648 Page 113-3)*

The following paragraphs describe the action of the SSDA clock generator circuitry.

The action of the SSDA clock generator is initiated by the command $\overline{\text{ANI/F STRT}}$ from the CPU. This occurs after the parallel data has been loaded into the SSDA transmit registers from the data bus. The Logic-Ø pulse of $\overline{\text{ANI/F STRT}}$ sets flip-flop M2-10/11 to give a Logic-Ø at TP3 which then:

- Sets the D input level of flip-flop M3-5
- Removes 'SET' to enable shift register M3 at M3-6 and M3-8
- Removes 'RESET' to enable counters M4 at M4-7 and M4-15. *(Refer to Fig. 6.16 Waveforms A and C).*

At the next rising edge of the inverted 256 kHz (Rx CLOCK) from M43-8 after $\overline{\text{ANI/F STRT}}$, the shift register M3 is clocked but only M3-1 'Q' output changes state to Logic-Ø. This is applied to the SSDA $\overline{\text{CTS}}$ and $\overline{\text{DCD}}$ inputs, thus releasing the inhibits on the SSDA transmit and receive registers. *(Refer to Fig. 6.16 Waveforms D and E).*

At the next (second) rising edge of the clock to M3, M3-12 changes to Logic-1. This allows NAND M2-3 to pass 256 kHz clock pulses via buffer M5-12 to the Reference Divider Assembly to shift the serial data string along the analog-control and status registers. *(Refer to Fig. 6.16 Waveforms D, F and I).*

The 256 kHz clock at NAND M2-3 is applied to the 4-bit up-counter clock input at M4-1, each rising edge causing the counter to increment by 1.

The divide-by-16 output M4-6 is applied to enable M4 at its M4-10 input ; the falling edge occurring at count-16 and incrementing the second counter to produce, at M4-11, a Logic-1 output. Later, at count-24, M4-6 changes again to Logic-1, and together with M4-11 output, gives a Logic-Ø from NAND M2-4, causing the following actions:

a. Flip-flop M2-12 is reset to give Logic-1 at TP3.

b. The Logic-1 at TP3 sets shift register M3 to give:

   i. Logic-1 at M3-1, thus inhibiting $\overline{DCD}$ and $\overline{CTS}$;
   ii. Logic-Ø at M3-12, disabling NAND M2-3 and thus stopping any further SSDA clocks.

c. The Logic-1 at TP3 resets the up-counters M4 causing:

   i. the counter outputs to fall to Logic-Ø, inhibiting further counting;

   ii. NAND M2-5 to rise to Logic-1, re-setting flip-flop M2-12 to prepare for the next $\overline{ANI/F\ STRT}$ input. *(Refer to Fig. 6.16 Waveforms I, B, C, E and F).*

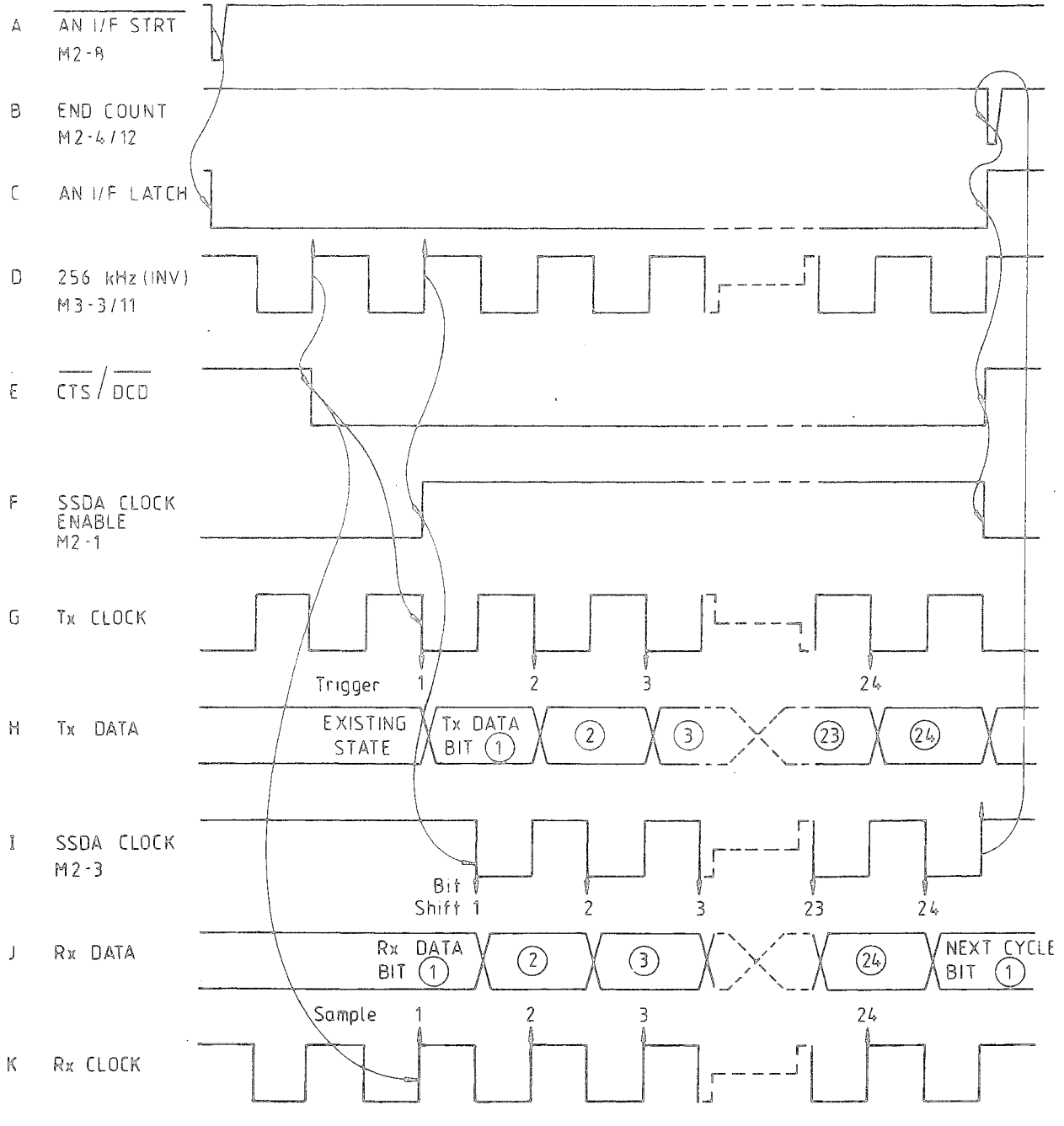


FIG. 6.16 SSDA CLOCK GENERATOR WAVEFORMS

6.4.5 SERIAL/PARALLEL CONVERTER

(Circuit Diagram 430652 Pages 11.4-4 and 11.4-5)

Serial control data transmitted from the SSDA (Analog Interface Assembly), together with their control signals (SSDA strobe and SSDA clock), enter the Reference Divider Assembly via the Mother Assembly.

The data and signals cross the isolation barrier through opto-isolators M6, M7 and M8 into guard.

Serial control and status data is returned out of guard to the SSDA receiver via opto-isolator M1.

6.4.5.1 Logic Levels

The nominal logic levels (Logic-1 = +5V, Logic-Ø = 0V) used in the out-guard SSDA circuits, are offset at the opto-isolator outputs to:

Logic-1 = -10V Logic-Ø = -15V

and level-shifted for the in-guard circuitry to:

Logic-1=0V Logic-Ø = -15V

6.4.5.2 Serial-In/Parallel-Out Control-Data Convertors

Six 8-bit serial shift registers M27, M25, M31, M19, M30 and M15 each have latchable parallel outputs. Their serial "D" inputs and "Q's" outputs are cascaded to form a single 48-bit serial shift register. M27 receives 'serial data in' from M8 via the level-shifting buffer M36-4, and M15 passes serial data on to the Parallel-in/Serial-out Status-Data converters.

6.4.5.3 Parallel-In/Serial-Out Status-Data Converters

Two 8-bit serial shift registers M18 and M22 each have parallel inputs. M18 serial "Ds" input accepts serial data from M15; M18 "Q8" output is cascaded to M22 "Ds" input; and M22 "Q8" output delivers SERIAL DATA OUT to buffer M11-11 and back to the SSDA via M1 opto-isolator.

M18 and M22 thus form a 16-bit serial shift register whose 16 parallel inputs' states can be inserted into the serial data string.

6.4.5.4 Serial Data Cycling

The serial data, organized into five blocks of three bytes *(Refer to Section 6.4.2.2)*, is accompanied by synchronized bursts of 24 clocks. The output from opto-coupler M7 is buffered via level-shifter M36-2 and then inverted at M14-6. The timing of the positive clock edges allows all bits of serial data (distributed throughout the shift registers) to stabilize before being clocked on.

After the CPU has generated two bursts of data and clock pulses, the serial control data has shifted into the correct positions in control registers M27, M25, M31, M19, M30 and M15. So before the third burst of three bytes, the SSDA produces a strobe which writes the control data into their parallel outputs. Simultaneously, the strobe also fills the 16-bit serial register of M18 and M22 with the status data present on their parallel inputs.

When the strobe ends, further transfers between serial and parallel registers are disabled. The new control data remains latched in the parallel control registers, and the new status data is in the serial status register ready for shifting to the SSDA Rx DATA register through guard.

The control and status bits in the registers are then circulated by three further bursts of clock pulses, until the CPU has read both the new status data and all the control data that were written by the strobe. Verification that the returned control data is identical to the transmitted data, ends the transfer.

If after three attempts, the returned data does not match the transmitted data; the CPU omits to re-trigger monostable M10 in the Reference Divider Assembly. M10 times out and allows the signal $\overline{\text{BARK DEL}}$ to go to Logic-Ø, disabling the 48 control data outputs by 'tri-stating' the registers M27, M25, M31, M19, M30 and M15.

6.4.5.5 Parallel Control-Data Outputs and Status-Data Inputs

The data latched in M27, M25, M31, M19, M30 and M15 outputs control the operation of the Analog circuitry. The effects are therefore described in the sub-sections relevant to their destinations.

As this is a multi-purpose converter, designed for use in more than one model of instrument, some of the control and status lines are not used.

6.4.6 SAFETY MONITOR (WATCHDOG)

(Fig.6.17)

6.4.6.1 Watchdog Signals

The watchdog circuits continuously monitor the CPU/SSDA functional process. Detection of a processor malfunction by the watchdog results in the following actions:

a. BARK. This signal:

   i. removes the drive from the primary of the High Voltage (1kV) transformer,
   ii. disables the 400V Power Supply, and
   iii. disconnects the Current Assembly output from the instrument output terminals.

b. $\overline{\text{BARK}}$. This is returned as a status bit to the CPU via the SSDA to signal a failure.

c. **BARK DELAYED.** This occurs 47ms after BARK and disconnects the AC Voltage Power and Sense circuits from the instrument output terminals.

d. $\overline{\text{BARK DELAYED}}$. This signal disables the registers of the serial/parallel data converters.

6.4.6.2 Effects at Power-on

The watchdog outputs are manipulated by the power-on reset circuits as follows:

- BARK DELAYED and $\overline{\text{BARK DELAYED}}$ are held active for 80ms from power-on and then are allowed revert to the inactive state only after two SSDA strobes have been detected.
- BARK is forced active until CPU/SSDA functioning has been verified; the latter must occur within 470ms of power-on.
- $\overline{\text{BARK}}$ is held inactive for 470ms from power-on, after which it provides a FAIL message to the CPU.

6.4.6.3 Effects after 'Reset'

Operation of the Reset control on the front panel provides a further 100ms period for the CPU/SSDA functional process to settle, during which time the watchdog circuits must verify correct functioning before their outputs are reset.

6.4.6.4 Watchdog Trip Action

The watchdog is tripped if the system fails to transmit analog-control updates to the analog circuitry. The updates are of two types:

- Transfer of 'Output value' data via the Analog Interface comparators,
- Transfer of analog switching data via the SSDA every 40ms.

The CPU generates pulses at 8ms intervals to verify that the correct output value has been latched into the Analog Interface comparators. These pulses are allowed to pass into guard only if the SSDA verifies that the analog switching data is being transferred normally at 40ms intervals. Once in guard, the pulses prevent the watchdog flip-flops from generating their four BARK output signals, by re-triggering a monostable (M10-4: 18ms) to hold it in its unstable state.

If two or more pulses are missing, M10 releases the hold, and the watchdog flip-flops 'Bark', activating the safety circuitry. They will be missing if the output value comparators are incorrectly updated; if the SSDA fails to generate 'Transmit' pulses for a period exceeding 470ms; or if the CPU crashes.

6.4.7 WATCHDOG CIRCUITRY

6.4.7.1 Out-Guard Watchdog

(Circuit Diagrams 430648 Pages 11.3-1 to 11.3-4 and 430652 Pages 11.4-1 to 11.4-6)

The CPU verifies the validity of each serial-interface transfer by giving the SSDA an instruction to generate a 'Watchdog Enable' trigger. This $\overline{\text{W.DOG ENABLE SET}}$ pulse (M44-7 on *page 11.3-3*), triggers watchdog-enabling monostable M29-11 *(page 11.3-1)*.

$\overline{\text{W.DOG ENABLE SET}}$ triggering and retriggering extends the natural (470ms) unstable state of M29 indefinitely. Unless the retriggers fail, the M29-9 output ($\overline{\text{W.DOG ENABLE}}$) remains at Logic-Ø. Absence of $\overline{\text{W.DOG ENABLE SET}}$ retriggers, for longer than 470ms, allows M29-9 to restabilize to Logic-1.

$\overline{\text{W.DOG ENABLE}}$ is inverted at M43-3 and applied to NAND gate M46-12 *(page 11.3-4)*.

During each successful processor cycle, the CPU addresses M51-9 (Digital Assembly *page 11.2-2*). The resulting low active pulses at 8ms intervals are inverted, and gated with WRT STRB to generate the active-low signal $\overline{\text{W.DOG}}$ at M49-11.

$\overline{\text{W.DOG}}$ travels via the Mother Assembly to the Analog Interface Assembly to be gated with the $\overline{\text{W.DOG ENABLE}}$ signal at NAND M46 *(page 11.3-4)*. The resulting signal at M46-13, W.DOG, consists of positive-going pulses at 8ms intervals when the CPU/SSDA system is working normally, or a Logic-1 level if the SSDA fails.

The W.DOG signal travels via the Mother Assembly to be passed into guard on the Reference Divider Assembly (Opto-coupler M9 on *page 11.4-5*).

6.4.7.2 In-Guard Watchdog

(Circuit Diagram 430652 Page 11.4-5)

NOTE:

The operating levels of the in-guard CMOS circuits are negatively displaced as follows (nominal voltages):

- Opto-coupler output circuits

  Logic-1: -10VDC Logic-Ø: -15VDC

- Digital CMOS circuits

  Logic-1: 0V Logic-Ø: -15VDC

Level-shifter M36 carries out the interfacing between these two levels.

The 'W.DOG' signal is opto-coupled into guard by M9. During normal operation: the W.DOG in-guard positive-going pulses, at 8ms intervals, keep re-triggering the monostable M10-4 to give a continuous Logic-Ø at M10-7. The 18ms unstable state of M10 allows for one pulse to be absent, but if two or more pulses are missing, M10 resets, taking M10-7 to Logic-1.

The logic level from M10-7 is connected directly to the set input of flip-flop M13-6. With the reset input to M13-4 held at Logic-Ø during normal operation, the output conditions of M13-1 and M13-2 are as follows:

- Set input M13-6 = Logic-Ø (no fault);
  M13-1 (Q) = Logic-Ø - BARK not active
  M13-2 (Q) = Logic-1 - $\overline{\text{BARK}}$ not active
- Set input M13-6 = Logic-1 (malfunction);
  M13-1 (Q) = Logic-1 - BARK active
  M13-2 (Q) = Logic-Ø - $\overline{\text{BARK}}$ active

The action of M13-2 changing to Logic-Ø triggers the monostable M10-11 which has a relaxation time of 47ms. After 47ms, M10-9 output clocks flip-flop M13-11 to give the command BARK DEL from M13-13 and $\overline{\text{BARK DEL}}$ from inverter M14-12.

6.4.7.3 Power-On Reset

(Circuit Diagram 430652 Page 11.4-5)

When power is first applied, the build-up of the 15V supply forces shift register M37 Set inputs to Logic-Ø, but its Reset inputs are held at Logic-1 by the charging action of R122/C7.

So M37 is forced into reset state for about 80ms:

- M37-2 imposes Logic-1 at M13-8 Set input.
- M37-1 at Logic-Ø holds M10 inactive at M10-3, thus preventing random triggering at M10-4 from erratic W.DOG inputs, as the SSDA/CPU functions start up. 'Q' output M10-7 holds M13-6 Set input at Logic-1.

Also, the Reset inputs M13-4 and M13-10 are held at Logic-1 for a period of 470ms from power-on by the signal $\overline{\text{FP RST}}$, generated by the power-on reset action of M53 on the Digital Assembly. *(page 11.2-2).*

Therefore, the Set/Reset inputs M13-8/M13-10, initially both at Logic-1, force M13-13 output to Logic-1 to give active BARK DELAYED and $\overline{\text{BARK DELAYED}}$ outputs.

The Set/Reset inputs M13-6 and M13-4, also initially at Logic-1, force:

- M13-1 to Logic-1 (Active BARK), and
- M13-2 to Logic-1 (Non-active $\overline{\text{BARK}}$).

The output states of M37 (M37-1 = Logic-Ø, M37-2 = Logic-1) remain unchanged after the 80ms time constant at M37 Reset inputs, but then M37-11 is free to be triggered from the SSDA strobe input. Two strobe inputs must occur before M37-1 clocks to Logic-1 and M37-2 to Logic-Ø. M13-13 now changes to Logic-Ø, making BARK DELAYED and $\overline{\text{BARK DELAYED}}$ inactive, and the inhibit is removed from M10-3.

The outputs M13-1 and M13-2 remain unchanged until M10-7 falls to Logic-Ø by the clocking action of pulses on the W.DOG input. This must occur before M13-4 returns to Logic-Ø (at 470ms from power-on) for BARK to be made inactive, otherwise BARK remains active and $\overline{\text{BARK}}$ is set to Logic-Ø, producing a fail status bit which is passed to the CPU.

6.4.7.4 Malfunction

(Fig 6.17)

Any malfunction which introduces one of the following conditions will cause the watchdog to bark:

a. CPU WRT STRB fails at Logic-Ø.

b. M51 on the Digital Assembly does not receive the address to activate M51-9.

c. Failure of transmission of bursts of the $\overline{\text{W.DOG ENABLE SET}}$ pulses from the SSDA to M29 (The SSDA is not transferring serial data).

d. The SSDA Strobe is not triggering M37.

e. W.DOG pulses are not triggering M10.

As well as these failures the CPU is informed, via SSDA Status byte transfer, of certain analog malfunctions. Subsequent CPU action can include deliberate activation of the watchdog by omitting to address M51 as in (b) above.

6.4.7.5 Reset

Once the watchdog has 'Barked' it can be reset, if the malfunction has cleared, by pressing the Reset control on the front panel.

The Reset input to the watchdog circuit, $\overline{\text{FP RST}}$, is active for 100ms after pressing the Reset key. (M53-9 on Digital Assembly *page 11.2-2*). During this period, the Reset inputs at M13-4 and M13-10 are held at Logic-1, allowing the correct pulse inputs from the processor and SSDA to hold M13-6 at Logic-Ø, and to reset BARK DEL at M13-13 to Logic-Ø. The watchdog will not reset if the malfunction persists.

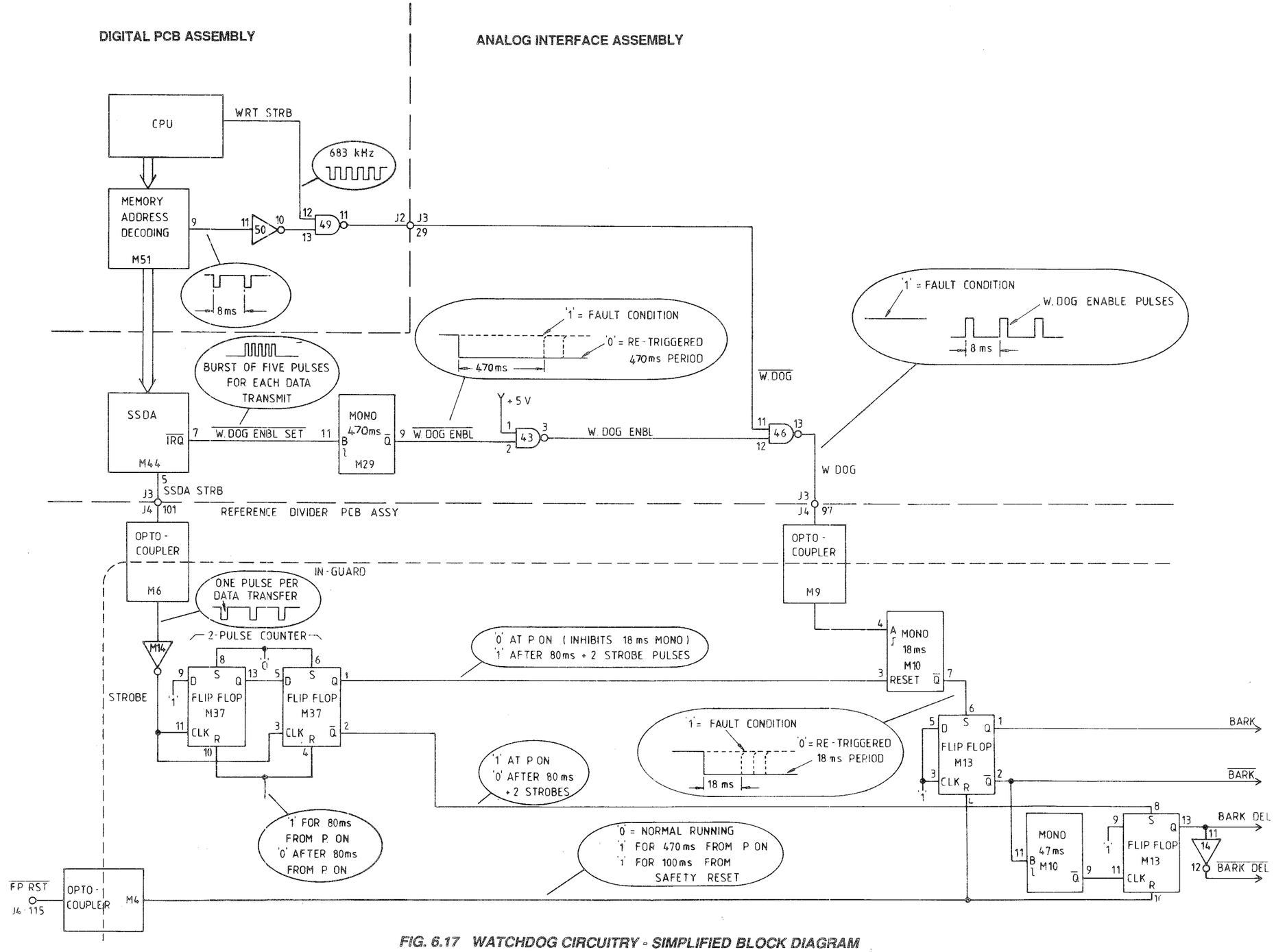


FIG. 6.17 WATCHDOG CIRCUITRY - SIMPLIFIED BLOCK DIAGRAM

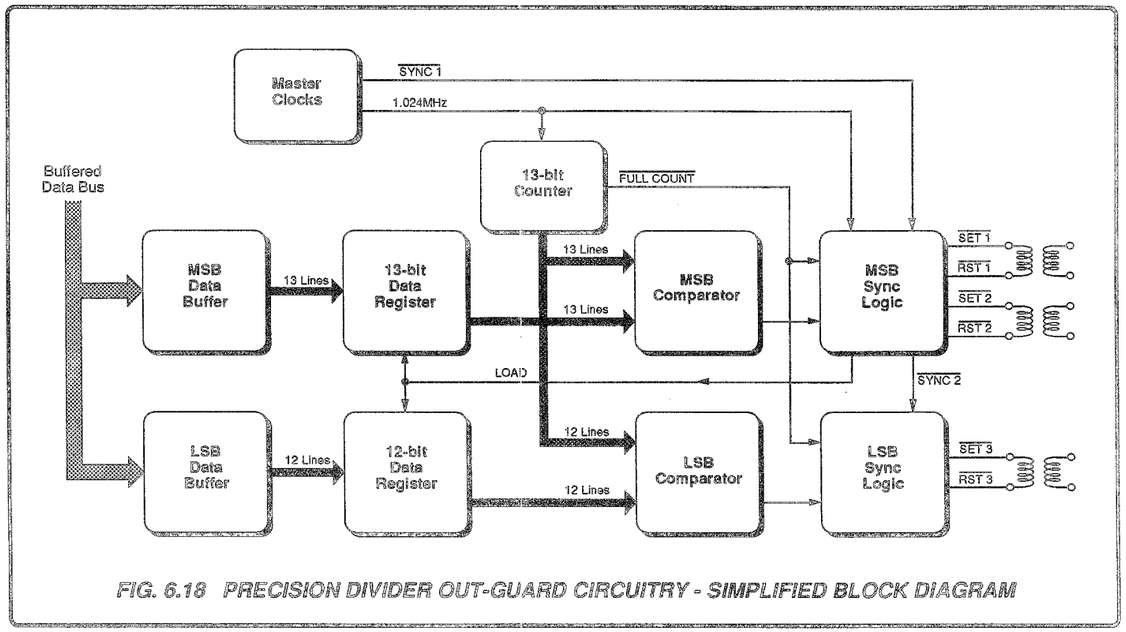


FIG. 6.18 PRECISION DIVIDER OUT-GUARD CIRCUITRY - SIMPLIFIED BLOCK DIAGRAM

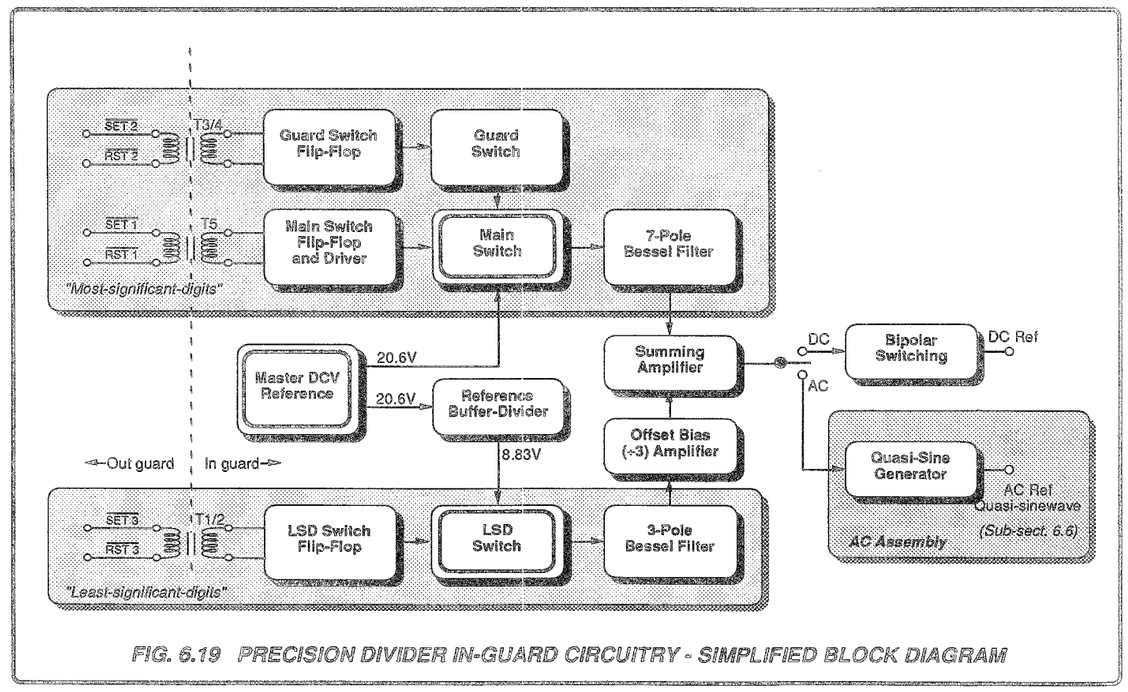


FIG. 6.19 PRECISION DIVIDER IN-GUARD CIRCUITRY - SIMPLIFIED BLOCK DIAGRAM

6.5 PRECISION DIVIDER

The out-guard circuitry described in this section performs the following functions:

- Receives and latches the demanded output value from the CPU in the form of a 25-bit word.
- Generates a continuous 13-bit up-count from the 1.024MHz Master Clock (8ms count cycle).
- Compares the 13-bit count with the 13 most-significant bits of the 25-bit word, generating 'Set' and 'Reset' pulses. These are transferred into guard to trigger the 'Most Significant' JFET switch in the Reference Divider.
- Compares the 12 most-significant bits of the count with the 12 least-significant bits of the 25-bit word, generating 'Set' and 'Reset' pulses. These are transferred into guard to trigger the 'Least-Significant' JFET switch in the Reference Divider.

The out-guard circuitry is located on the Analogue Interface Assembly.

The in-guard circuitry performs the following functions:

- Provides a Master Reference Voltage (20.6V) which is chopped by the 'Most Significant' JFET switch to generate a square-wave, whose Mark/Period ratio is controlled by the 13 most-significant bits of the 25-bit word. A 7-pole Bessel filter smooths the square-wave to provide a DC voltage, whose value varies directly as the Mark/Period ratio of the MSB square-wave.
- Provides a Buffered Reference Voltage (8.83V) which is chopped by the 'Least-Significant' JFET switch to generate a square-wave, whose Mark/Period ratio is controlled by the 12 least-significant bits of the 25-bit word. A 3-pole Bessel filter smooths the square-wave to provide a DC voltage, whose value varies directly as the Mark/Period ratio of the LSB square-wave.
- Conditions the two DC voltages produced by the Bessel filters, delivering them via full 4-wire connections to be summed on either the DC assembly (for DC output selections) or on the AC assembly (for AC outputs) as a DC 'Working Reference'.

  The value of this reference voltage is accurately proportional to the value demanded by the CPU's 25-bit word. For DC outputs, with polarity changeover switching, it can have values between +20V and -20V (including zero); but as a reference for AC outputs, its value lies between +0.126V and +2.79V.
- For AC outputs only, the in-guard circuitry digitally generates a stepped AC reference voltage whose peak value is equal to the DC Working Reference Voltage. This gives the Sense/Reference Comparator *(described in sub-section 9.9)* the considerable advantage of comparing AC Sense against AC Reference. (If AC were compared with DC, small DC off-sets would magnify and lead to 'DC turnover' errors). The AC waveform is constructed in ten steps by a digitally controlled switching network. It has been given the name 'Quasi-Sinewave".

The in-guard circuitry is located on the Reference Divider Assembly.

6.5.1 PRECISION DIVIDER COMPARATORS

(Circuit Diagram No. 430648 Pages 11.3-1 to 11.3-4)

6.5.1.1 General

(Figs. 6.18 and 6.19)

The comparators are designed as a means of translating a binary word into the accurately defined Mark/Period ratio of a square-wave. The ratio of the square-wave's average value to its peak value subsequently defines the division ratio applied to the Master Reference, and must be adjustable at high resolution.

The required decimal resolution translates into a 25-bit binary word, each bit needing to exert control of the division ratio. A single comparator of this length would require more than 30 million clocks to scan, which at sensible clock frequencies would occupy several seconds. To filter out the resultant chopping frequency would require large and expensive components, and force unrealistic operational time constraints.

In the Datron Precision Divider, the 25-bit word is split into two parts (13 most-significant bits - MSB; 12 least-significant bits - LSB), allowing a scan-cycling frequency as high as 125Hz to be achieved.

Both MSB and LSB comparators are scanned concurrently by the same 13-bit counter, forming two separate square-waves. These act on two separate reference divider switches and filters to generate separate DC voltages which are then recombined, giving the required resolution.

In summary, the two comparators translate information from the CPU into time-related pulses which control mark/period switching in the reference divider. One comparator operates on the thirteen most-significant bits of CPU data; the other deals with the twelve least-significant bits. The comparators operate concurrently, cycling continuously at 125Hz, taking 8ms per full count.

At the start of each 8ms counting period, each comparator generates a SET pulse to start its reference divider 'Mark' element. Then after precisely-measured delay times, each generates a RESET pulse to terminate the 'Mark', and start the 'Space'. At each 8ms full-count, the clock resets and continues up-counting from zero.

6.5.1.2 Comparator Operation

(Fig. 6.18)

The MSB and LSB Data Buffers are periodically loaded and latched with binary 'Demanded Output Value' data under the control of the CPU.

At the end of each comparator counting cycle, the 13-bit counter $\overline{\text{FULL COUNT}}$ output enables the generation of set pulses $\overline{\text{SET1}}$, $\overline{\text{SET2}}$ and $\overline{\text{SET3}}$ by the MSB and LSB 'Sync Logic' circuits.

FULL COUNT also generates the LOAD command. This writes the data, currently latched in the buffers, into working data latches which form the 13-bit and 12-bit Data Registers, updating the earlier 'Demanded Output Value' which is resident in the comparator.

The MSB and LSB comparators translate this binary data into 'RESET' pulses, whose time relationships to the 'SET' pulses are established by the value of their binary words.

6.5.1.3 13-Bit (MSB) Comparator

(Circuit Diagram No. 430648 Page 11.3-2)

The 13 binary outputs of the up-counter scan the 13 Exclusive-OR elements of the MSB Comparator. With the least-significant bit at 512kHz, and the most-significant at 125Hz, the 8ms scan time thus divides into 8192 time elements, each of 977ns.

Each time element has a unique binary code, incrementing by one bit on its predecessor. When this coincides with the bit-pattern set in the data register, the comparator provides an output pulse to the MSB sync logic. The latter generates reset pulses $\overline{\text{RST1}}$ and $\overline{\text{RST2}}$ in synchronism with the signal SYNC1 (2.048MHz).

6.5.1.4 12-Bit (LSB) Comparator

(Circuit Diagram No. 430648 Page 11.3-1)

This functions in the same manner as the MSB comparator, but scanning only twelve bits over the same 8ms counting period, thus accommodating 4096 time elements of 1954ns for each binary increment.

SYNC2 pulses, generated in the MSB Sync Logic circuitry at half the rate of SYNC1, synchronize the $\overline{\text{RST3}}$ output from the LSB Sync Logic.

6.5.2 COMPARATOR CIRCUIT ACTION

6.5.2.1 Input Data Latches

(Circuit Diagram 430648 Pages 11.3-1 and 11.3-2)

The input buffered data latches M31 to M34 and M37 to M39 receive 27 data bits in four bytes from the buffered data bus. Latches are selected by signals REF DIV 1, 2, 3 or 4 from the memory address decoding on the digital pcb. Data is clocked to the 'Q' outputs of the latches on the positive-going edge of $\overline{\text{WRT STRB}}$.

Data from the input latches is used as follows:

25 bits form a data word to the comparator registers M47, M48, M49 (part), M51 and M52. The remaining 3 bits from the data latches are used for separate functions:

a. M34-5 triggers monostable M29 (part), whose Q output is inverted and buffered to provide the control $\overline{\text{UPD (OG)}}$ used in the relay drive logic for analog switching.

b. M34-4 (EXT FREQ SEL) selects between the internal 16kHz synchronizing frequency and the 16kHz output from the External Frequency Input Buffer.

c. M34-3 ($\overline{\text{BEEP}}$) triggers the Beeper monostable M55, which is activated to draw attention to display messages.

6.5.2.2 13-Bit Counter

(Circuit Diagram 430648 Page 11.3-2)
(Refer to Fig 6-20 for Waveforms)

The counter consists of three 4-bit binary counters M15, M16, M17 and J-K flip flop M42 (half dual package). The squarewave outputs from the counter are on 13 binary-coded lines, the first (least-significant) being a 512kHz squarewave, the others successively divided in frequency to the most significant output of 125Hz.

Bit 1 is provided by J-K flip flop M42, which toggles on each falling edge of the 1.024MHz clock to give 512kHz Q and $\overline{Q}$ outputs. These outputs are used as follows:

a. The two complementary 'Q' outputs together provide the least-significant input to the 13-bit comparator;

b. The Q output controls the counting rate of M15, synchronizes M16 and M17, and is used in the gating of $\overline{\text{FULL COUNT}}$.

Counters M15, M16 and M17 are cascaded as a 12-bit counter and are synchronously clocked by the 1.024MHz. M15 can count only when its count-enable input M15-7 is set to Logic-1 by the Q output of M42.

As M42 output is at 512kHz, clocking of M15 occurs on the rising edge of alternate 1.024MHz clocks, thus giving outputs of 256, 128, 64 and 32kHz squarewaves from M15.

Counter M16 is enabled by the carry output from M15 together with 512kHz from M42 at the count-enable pins M16-10 and M16-7 respectively, thus giving outputs of 16, 8, 4 and 2kHz squarewaves from M16.

Counter M17 functions in a similar manner to give outputs of 1kHz, 500, 250 and 125Hz squarewaves.

The 2µs-long 'Carry' output from M17 occurs at the end of the 125Hz output when all counter outputs are at Logic-1. The carry output is NANDed with M42Q output to give the 1µs-long logic command $\overline{\text{FULL COUNT}}$. The counting cycle resets and continues, starting from bit 1.

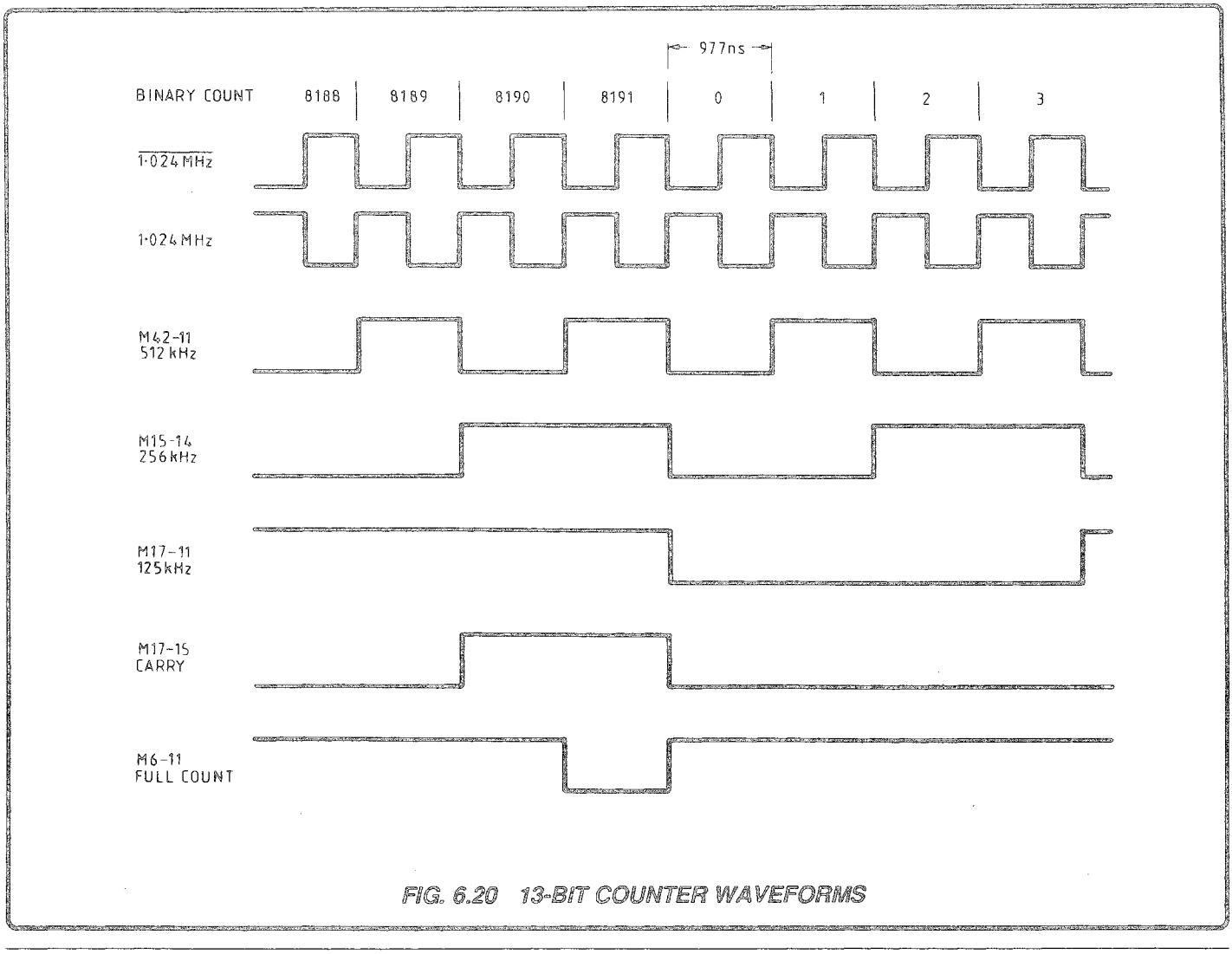


FIG. 6.20 13-BIT COUNTER WAVEFORMS

6.5.2.3 13-Bit Comparator Action

(Circuit Diagram 430648 Page 11.3-2)

The 13-bit comparator provides a Logic-1 output at TP12 whenever a coincidence occurs between the following two sets of data:

a. Data set in registers M47, M48 and M49-1;
b. Data from 13-bit counter M42, M15, M16 and M17.

Twelve exclusive-OR elements M25, M26, M27 and three NOR gates of M12 are used to detect a coincidence. The data in the registers is preset by the CPU, while that presented by the 13-bit counter cycles through every binary combination possible on 13 lines.

Two coincident inputs to an exclusive-OR gate provide a Logic-Ø to the 12-input NOR gates M24/M23; full coincidence in bits 2 to 13 is shown by a Logic-Ø at NAND M13-6. Coincidence at bit 1 is shown by Logic-Ø at M12-13 and M12-4 (M12 acting as an exclusive-OR gate) as follows:

M12 INPUT PINS			OUTPUT PINS		
6	11	9/12	4	13	
0	1	0	0	0	Only 4 input combinations available
0	1	1	1	0	
1	0	0	0	1	
1	0	1	0	0	

A BUSY signal is generated by the comparator at NAND M50-13 (TP2) when the 13-bit counter approaches full count. Bits 8 to 13 are at Logic-1 for the period of 125µs preceding the end of the counter cycle *(see Fig. 6-21)*. The $\overline{\text{BUSY}}$ level is applied to the M49 D-input at pin 9 and is synchronously clocked through as the signal $\overline{\text{REF BUSY}}$ to buffer M45-2 by 1.024MHz.

As described earlier, the demanded output value is defined by the CPU to a resolution of 25 bits, contained in four data bytes. The time needed for the 4-byte transfer could allow the latches to contain spurious data until they were fully loaded, and an inaccurate parity could be registered with the counter still running. The counter must not be interrupted, as its full count defines the 'period' of the mark/period ratio used to control the division of the reference voltage. It is therefore necessary to reduce the loading time, which is achieved by double-latching the data.

When the CPU has data to load into the input data latches, it first interrogates the comparator by enabling buffers M45 using the signal $\overline{\text{REF DIV RD}}$. The $\overline{\text{REF BUSY}}$ signal at Logic-1 (M45-3) indicates to the CPU that enough time is available to load the latches (at least 125µs remain before the LOAD pulse occurs). If the $\overline{\text{REF BUSY}}$ signal is at Logic-Ø, the CPU waits until it returns to Logic-1 again.

When the $\overline{\text{REF BUSY}}$ signal is at Logic-1, the CPU loads the data by first carrying out four transfers of one byte each into the seven quad buffer latches M31 to M34, and M37 to M39. Each byte's destination is addressed by one of the chip-select signals $\overline{\text{REF.DIV.1}}$ to $\overline{\text{REF.DIV.4}}$, which enables the selected buffer latches. The data is latched by the $\overline{\text{WRT STRB}}$ signal.

Once the full 25-bit word has been latched into the buffers, it is available as a single word at the data inputs of the comparator latches M47, M48, M49, M51 and M52. The CPU again interrogates the comparator by $\overline{\text{REF DIV RD}}$, and five of the elements of M45 buffer the five most-significant data bits back to the CPU. If parity with the transmitted data is confirmed, the CPU takes no action. When the counter times out, the $\overline{\text{FULL COUNT}}$ signal is clocked through to M14-6 by SYNC 2 as the $\overline{\text{LOAD}}$ signal, and the new data is transferred into the comparator latches.

If the data latched in the buffers is not as transmitted, the CPU initiates the FAIL 4 message procedure to the operator.

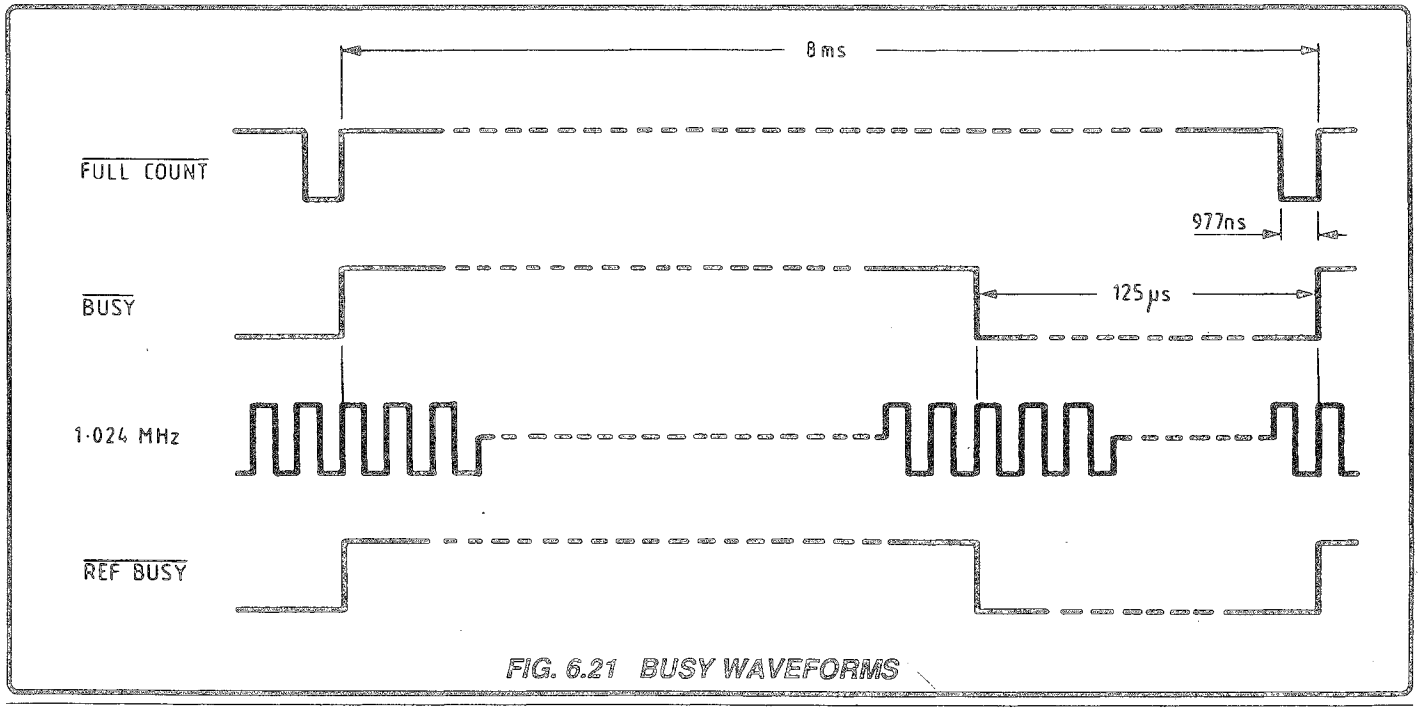


FIG. 6.21 BUSY WAVEFORMS

6.5.2.4 'Most Significant Bits' SYNC Logic

(Circuit Diagram 430648 Page 11.3-2) (Refer to Fig. 6.22 for Waveforms)

This circuit, M14, M6, M7 and M8, provides the following signals: $\overline{\text{SYNC 2}}$, LOAD, $\overline{\text{SET1}}$, $\overline{\text{SET2}}$, $\overline{\text{RST1}}$ and $\overline{\text{RST2}}$.

$\overline{\text{SYNC 2}}$ is obtained by NAND gating 1.024MHz and SYNC1 to give a synchronizing pulse at half the rate of SYNC1.

The LOAD pulse enables the 13-bit comparator registers, and is generated at M14-6 at the end of the counter's full-count output. $\overline{\text{FULL COUNT}}$ sets the D input M14-2 and the level is clocked, inverted, from M14-6 by the next two $\overline{\text{SYNC 2}}$ pulses that occur.

The inverse of LOAD is used to time the pulse $\overline{\text{SET1}}$ by NOR-gating at M7-4 with 1.024MHz. The M7-4 pulse is NAND-gated with SYNC1 to provide $\overline{\text{SET1}}$ from M8-1. The pulse $\overline{\text{SET2}}$, which occurs 977ns before $\overline{\text{SET1}}$, is obtained by gating the signal $\overline{\text{FULL COUNT}}$ with 1.024MHz at NOR M7-10 and then NAND- gating at M8-10 with SYNC1.

Reset pulse generation *(see Fig. 6.23)* is initiated by a Logic-1 level at TP12. This can occur at any one of the 8192 binary counts of the 13-bit counter, its actual time slot depending on the binary count at which the coincidence occurs.

The coincidence level at TP12 is NAND gated at M6-8; M6-10 being at Logic-1 for all binary counts except 8191. The Logic-Ø at M6-8 is NOR-gated at M7-1 with 1.024 MHz, this is then used to select the next SYNC1 pulse via NAND M8-4 to provide the pulse $\overline{\text{RST1}}$.
The coincidence level at TP12 is used to set the D input at flip-flop

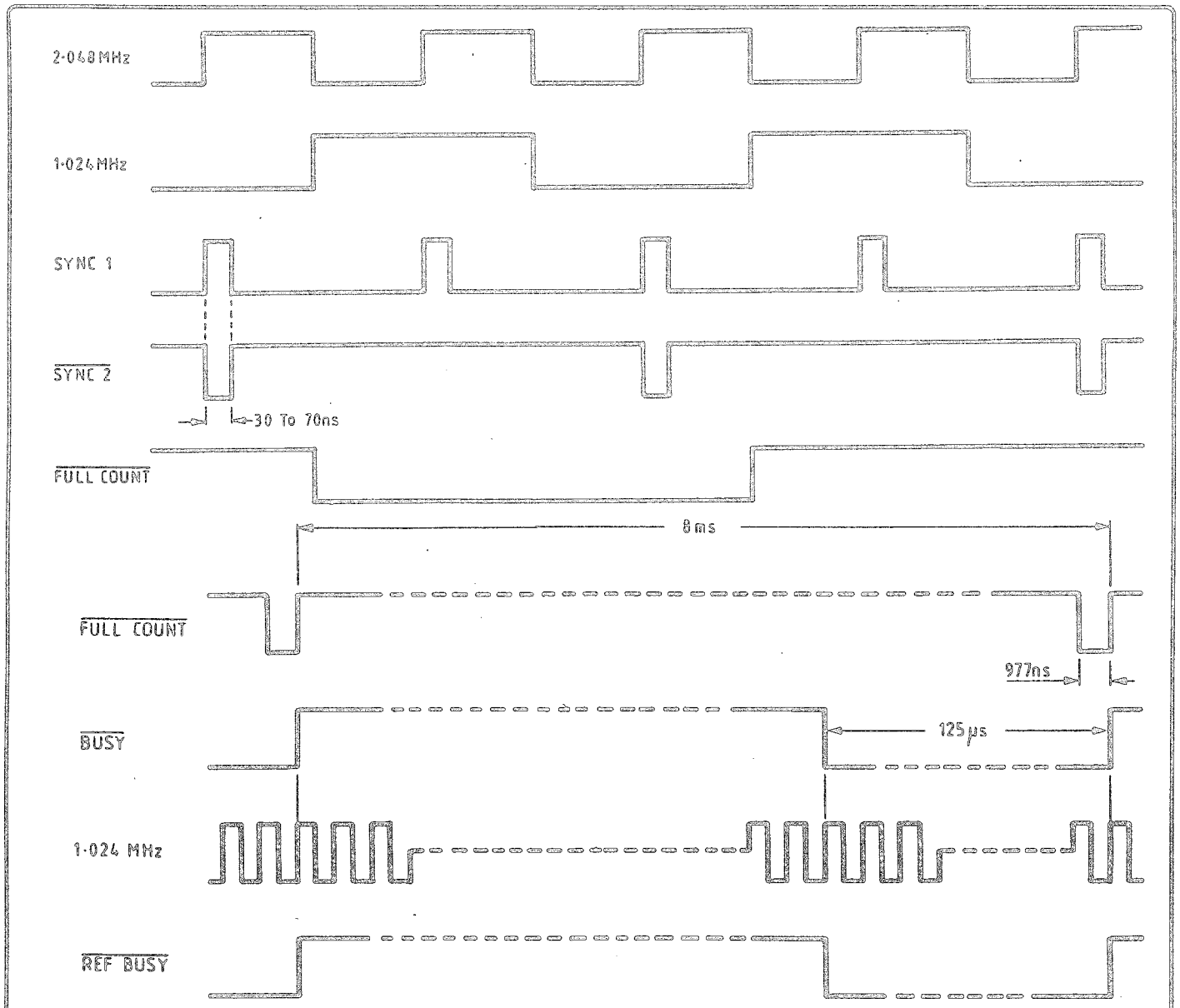


FIG. 6.22 MSB SYNC LOGIC WAVEFORMS

M14-12. This level is clocked to NAND M6-5 by the next $\overline{\text{SYNC 2}}$ pulse. NAND input M6-4 is at Logic-1 except when LOAD is active, thus M14-9 output is inverted at M6-6 to be NOR-gated with 1.024MHz at M7-13. This is then used to select the next SYNC1 pulse via NAND M8-10 to provide the pulse $\overline{\text{RST2}}$.

The pulse-timing example given in *Fig.6.23* shows the generation of $\overline{\text{RST1}}$ and $\overline{\text{RST2}}$ when coincidence occurs in the comparator at binary count = 0 (waveforms in continuous lines).

Coincidence occuring at binary count 1 causes $\overline{\text{RST1}}$ and $\overline{\text{RST2}}$ to increment in time by 977ns with respect to the $\overline{\text{SET1}}$ and $\overline{\text{SET2}}$ pulses (waveforms in broken lines).

$\overline{\text{RST1}}$ and $\overline{\text{RST2}}$ are generated with the same relationship in time to the comparator coincidence when the latter occurs in any binary count time slot from 0 to 8190 (inclusive).

Note that as the comparator word increments in value, $\overline{\text{RST1}}$ and $\overline{\text{RST2}}$ increment in time after $\overline{\text{SET1}}$ and $\overline{\text{SET2}}$, which remain stationary with respect to $\overline{\text{FULL COUNT}}$ and LOAD. $\overline{\text{RST1}}$ and $\overline{\text{RST2}}$ are inhibited when coincidence occurs at binary count 8191 to allow for the re-loading of the input registers at the end of the counter cycle. The inhibit is performed by the level of $\overline{\text{FULL COUNT}}$ going to Logic-Ø and NAND M6-10, preventing $\overline{\text{RST1}}$ being generated; and by flip-flop M14-5 output going to Logic-Ø for the period of the load pulse, inhibiting $\overline{\text{RST2}}$.

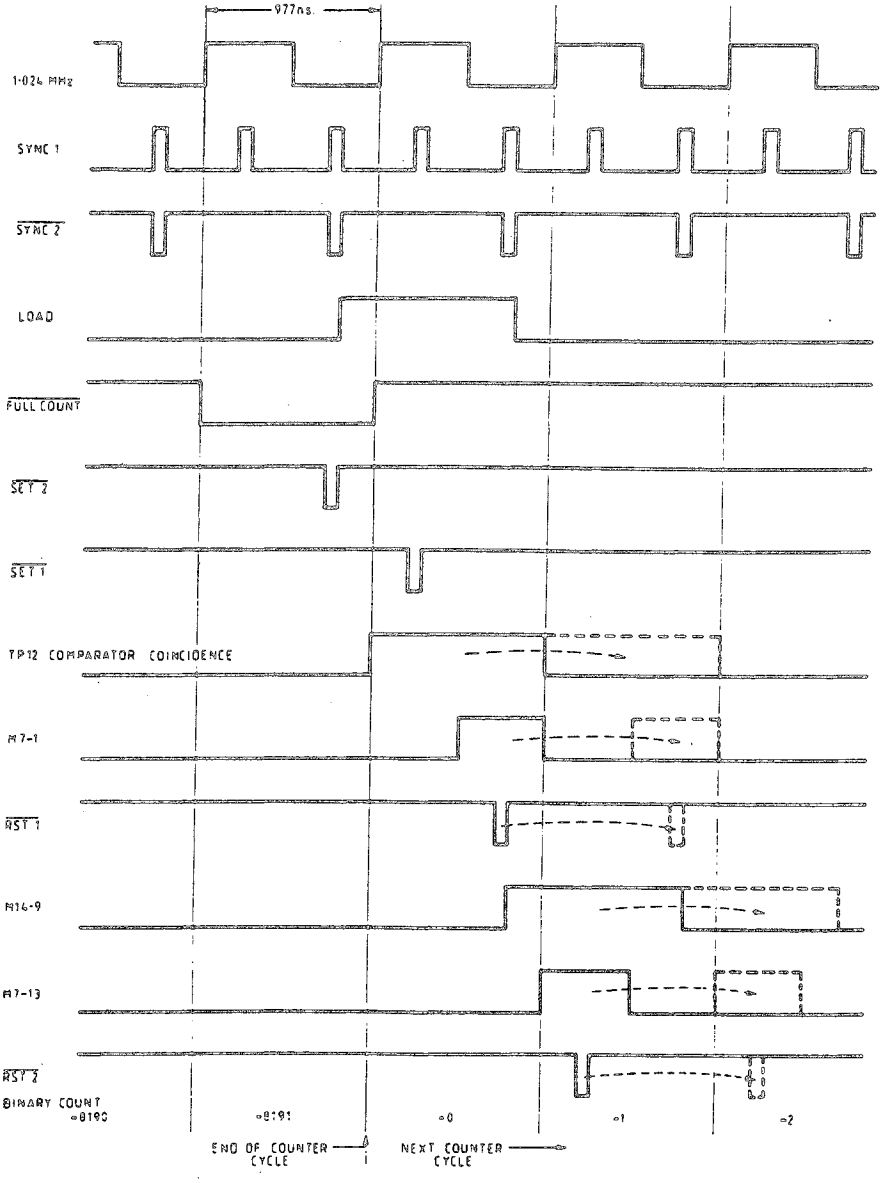


FIG. 6.23 MSB SET/RESET PULSE GENERATION

6.5.2.5 12-Bit Comparator Action

(Circuit Diagram 430648 Page 11.3-1)

This functions in an identical manner to the 13-bit comparator previously described. Twelve exclusive-OR gates, M19, M20 and M21, receive the 12-bit binary output from the common counter and compare these bits with the data in the data registers.

The least-significant bit changes at a rate of 256kHz, and the most-significant bit at 125Hz. Coincidence occurring in any of the 4096 binary-count time slots available in the comparator cycle is shown as a Logic-Ø at TP5 for a period of 1954ns.

6.5.2.6 'Least Significant Bits' SYNC Logic

(Refer to Fig. 6.24 for Waveforms)

The timing of $\overline{\text{SET3}}$ is controlled by the $\overline{\text{FULL COUNT}}$ pulse from the 13-bit counter. The inverted $\overline{\text{FULL COUNT}}$ at M43-6 is gated with the inverted $\overline{\text{SYNC 2}}$ from M43-11 to give, at M46-1, $\overline{\text{SET3}}$.

The comparator coincidence logic level is inverted to Logic-Ø at M12-1; M12-2 being at Logic-Ø except when $\overline{\text{FULL COUNT}}$ is low. The waveform at M12-1 lasts for 1954ns and therefore allows two consecutive $\overline{\text{SYNC 2}}$ pulses to be gated to M46-4 ($\overline{\text{RST3}}$).

This condition exists for all $\overline{\text{RST3}}$ timings except at the binary count of 4095; in this instance, the $\overline{\text{FULL COUNT}}$ pulse occurs after the gating of the first $\overline{\text{SYNC 2}}$ pulse, sets M12-2 to Logic-1 and so prevents the second pulse appearing at $\overline{\text{RST3}}$. In practice, the second pulse of $\overline{\text{RST3}}$ has no operational significance.

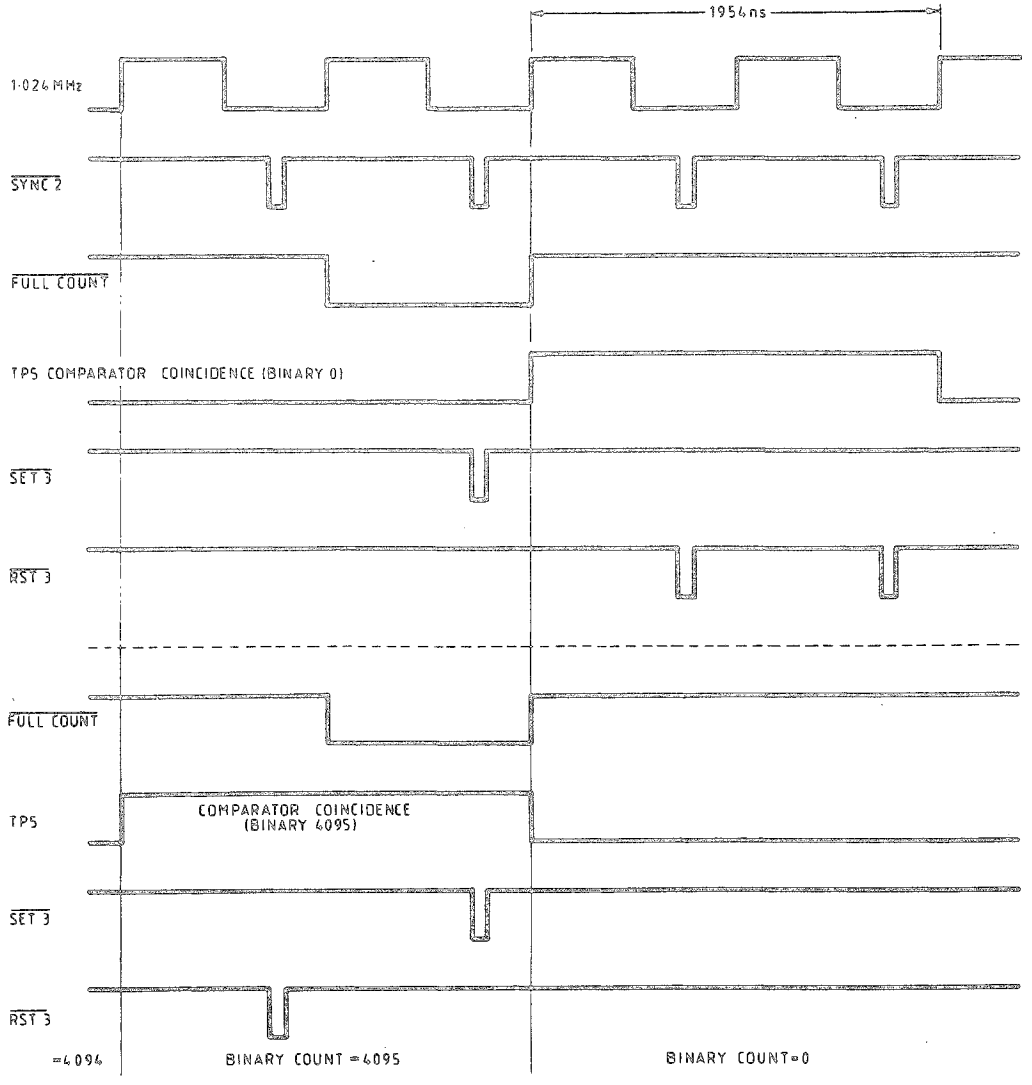


FIG. 6.24 LSB SET/RESET PULSE GENERATION

6.5.3 REFERENCES and REFERENCE DIVIDER

(Circuit Diagrams 430652 Pages 11.4-1 to 11.4-6)
(Refer also to Fig. 6.19)

The set and reset pulses from the precision divider comparators control the timing of JFET switches, which in turn chop the Master Reference voltages.

The chopped references are filtered to generate two voltages whose levels are proportional to the MSB and LSB squarewaves' mark:period ratio (duty cycle). These MSB and LSB voltages are conditioned, and transferred to the AC Assembly by full 4-wire sensed connection where they are summed at a star-point to generate a Working Reference: 'REF+Ve'. The output voltage increments at high resolution (0.03ppm: approx. 0.6μV), with a maximum possible range of adjustment of 0-20V.
The high resolution associated with the full 13-bit count and a 20V reference is advantageous for DC outputs. Such resolution, however, is not strictly necessary for the accuracies associated with AC outputs; and also the 1V Range is the basic AC range, all other ranges employing either attenuation or amplification.

For AC outputs, therefore, the working reference is reduced to a range from 0.126V to 2.79V by software. This results in a reduction of the maximum mark:period ratio of the chopping waveform to about 0.14.

6.5.4 MASTER REFERENCE

(Reference PCB Assembly on Circuit Diagram DC430652 Page 11.4-1)

The Master Reference determines the fundamental long- and short-term stability of the whole calibrator. It is a separate PCB, mounted on the Reference Divider Assembly, which generates an ultra-stable output voltage of approximately 20.6V.

This PCB module is assembled, pre-conditioned and tested by Datron Instruments as a single entity, and there is therefore no method of repairing or testing it without specialized test equipment and processes. If a fault is suspected on the Reference PCB Assembly , contact your nearest Datron Service Center.

6.5.5 REFERENCE BUFFER-DIVIDER

(Circuit Diagram 430652 Page 11.4-2)

R80 and R81 drop the 20.6V Master Reference voltage (V Ref) to +8.83V. M23/Q40 is a voltage-follower providing +8.83V with respect to Common-4 at the star-point TP11 to supply the Least-Significant Digit switch.

6.5.6 LEAST-SIGNIFICANT-DIGITS SWITCHING

(Fig.6.26)

6.5.6.1 Switch Driver

$\overline{SET3}$ and $\overline{RST3}$ pulses from the LSB Comparator in the Analog Interface Assembly are transferred into guard via pulse transformers T1 and T2, whose centre-tapped secondaries are balanced about Common-4 0V (T1) and +9V (T2).

Q5-Q8 form a fast bistable using emitter-coupled logic, to switch TP1 between +9V (mark) and +20V (space). During the "Mark" time after $\overline{SET3}$ pulse, Q29 and Q30 are switched ON, connecting LKA to +9V Ref. Q1-Q4 have the same bistable action as Q5-Q8, switching Q31 off during the "Mark" period by -11V at TP2, thus disconnecting LKA from Common-4 (0V). During the "Space" time after $\overline{RST3}$ pulse, Q29 and Q30 disconnect LKA from +9V Ref, and Q1-Q4 switch Q31 on, connecting LKA to Common-4 (0V). *Fig.6.26* illustrates this action.

6.5.6.2 JFET Switch and 3-Pole Filter

The combined action of the switch FETs alternately provides charging current for the 3-pole filter (during "mark") and discharging current (during 'space'). Two JFETs in parallel (Q29 and Q30) are necessary to equalize the charging and discharging time-constants by matching the "ON" resistances. This preserves linearity of the filter output voltage over the full range of mark/period ratios applied via the set and reset pulses.

The 3-pole filter has the advantage of not being in series with the DC output signal. The 125Hz ripple content is reduced to a level which is acceptable within the overall instrument specification. The filter output is buffered by voltage-follower M16.

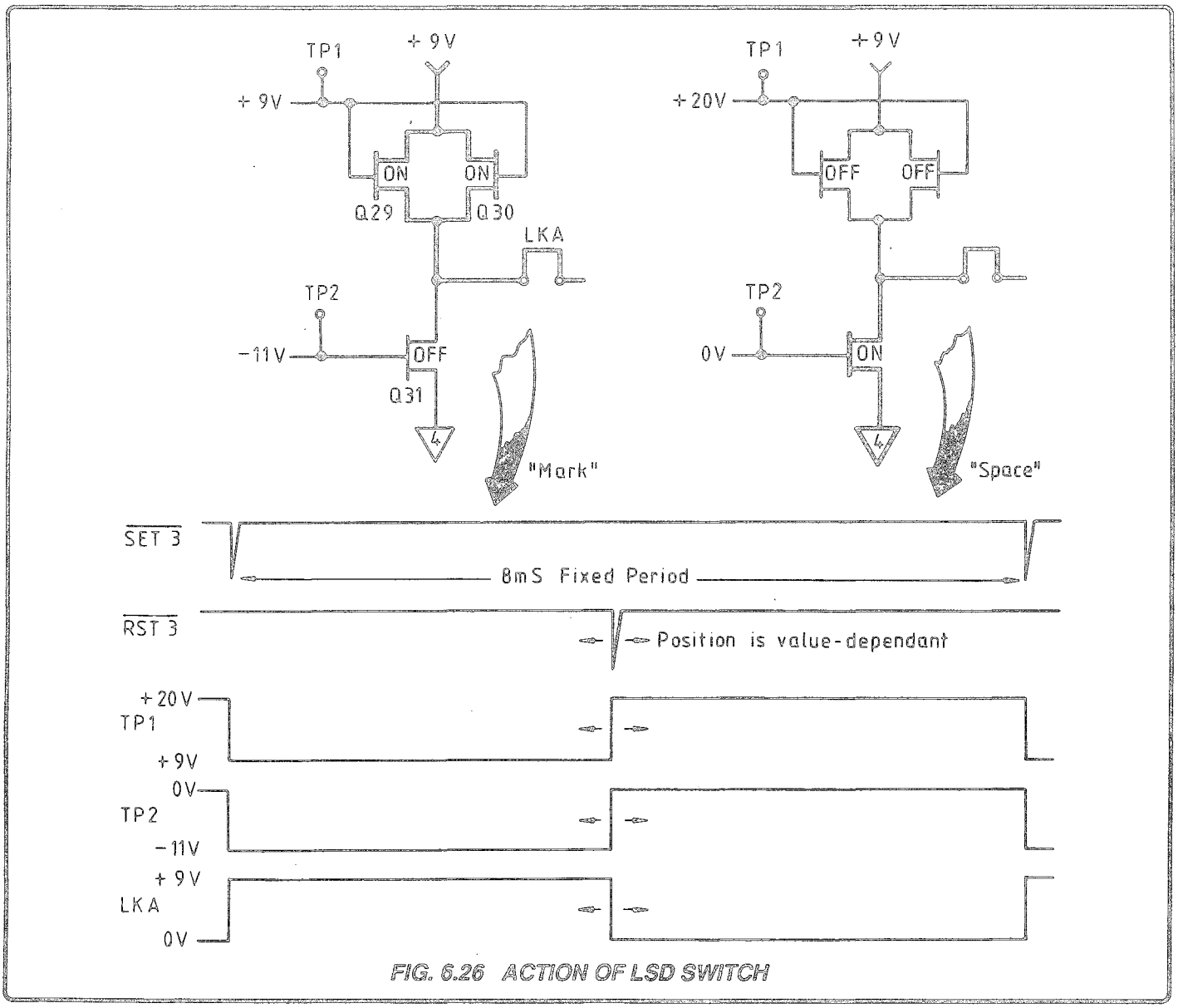


FIG. 6.26 ACTION OF LSD SWITCH

6.5.6.3 Offset Bias Amplifier

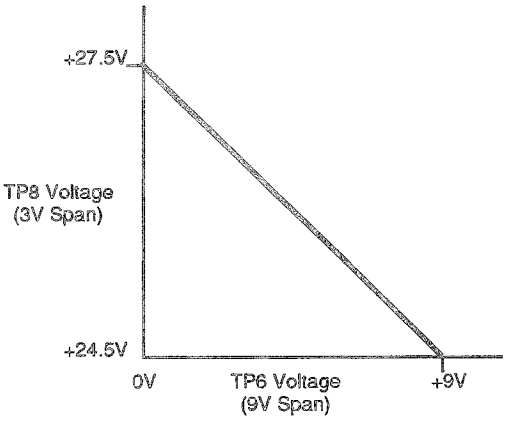
M20 performs a dual role:

a. Its gain is set to 1/3 by R65/R64

b. Its output is level-shifted to provide an offset bias for summing (this allows the summed output to have a negative zero offset).

Also a small thermal coefficient zero correction is factory-preset (D10/R85).

M20 transfer function is approximately as shown.



The actual values are as set digitally in software, affecting the mark:period ratio of the J-FET switches, using stored calibration constants.

6.5.7 MOST-SIGNIFICANT-DIGITS SWITCHING

(Circuit Diagram No. 430652 Page 11.4-1)

The large reference voltage (20.6V) and the need for higher resolution makes the MSB Switching circuitry more complex than for LSB; but the principle is the same: the set and reset pulse-timing adjusts the mark:period ratio of the square wave fed to the filter.

The arrangement used for the MSB switching satisfies two essential requirements:

a. The charge and discharge path resistances for the 7-pole filter must be closely matched.

b. The leakage current of the path switched off must be minimal.

Requirement (a) demands that the matched devices used in both paths are of the same type (P-channel JFETs have approximately 10 times the "on" resistance of N-channel types). But without the voltage standoff and leakage current shunt created by the guard switch, the pinch-off gate voltage for one of the paths would be high enough to generate gate-leakage current in excess of requirement (b).

A description of the Main and Guard Switch action is given overleaf.

6.5.8 MAIN and GUARD SWITCHES

(Circuit Diagram 430652 Page 11.4-1 and Fig. 6.27)

Refer to *Fig. 6.27*, in which only the Space to Mark (SET) state transfer a-b-c is shown.

The Mark to Space (RESET) transfer is symmetrical c-b-a.

The switch driver flip-flops establish the voltage shown at TP3, TP4 and TP5 as controlled by the set and reset pulses. The drivers are ECL fast bistables, but note that Q19 and Q20 are included in the main switch driver as a level-shifter for Q32/Q35.

6.5.8.1 Switch Timing

(Fig. 6.27)

$\overline{SET1}$ pulse is delayed by 0.5µs after $\overline{SET2}$ pulse, and $\overline{RST2}$ is delayed by 0.5µs after $\overline{RST1}$.

$\overline{SET2}$ and $\overline{RST2}$ pulses control the timing of Q36, Q33, Q34 and Q37 in the main switch (TP4 and TP5).

$\overline{SET1}$ and $\overline{RST1}$ pulses turn Q35 and Q32 on and off (TP3). Because of the 0.5µs delays, Q35 and Q32 conduct only during the time that Q36 and Q33 are also conducting.

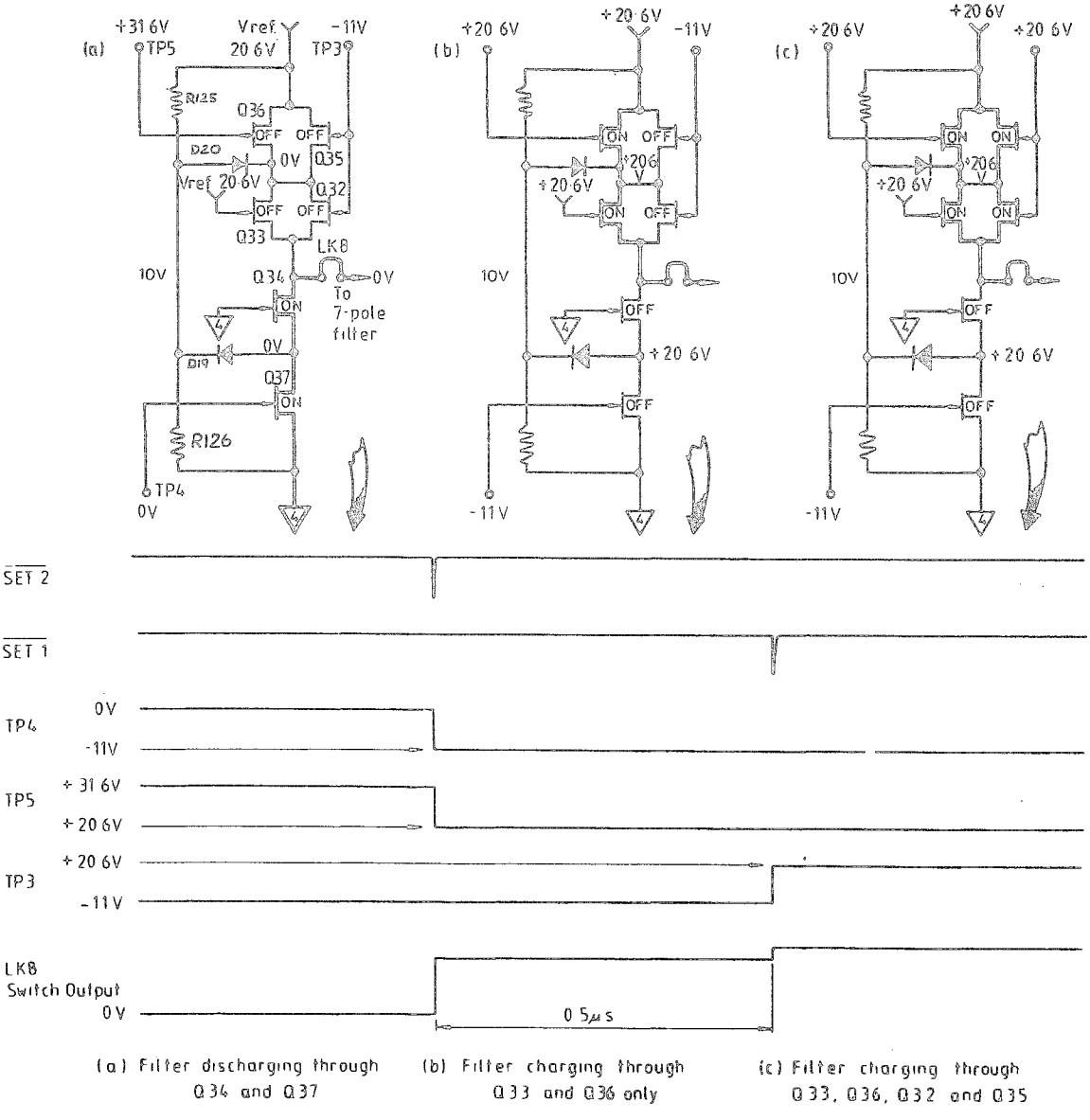


FIG. 6.27 ACTION OF MAIN AND GUARD SWITCHES (MSD)

6.5.8.2 Filter Discharge Path

In *Fig. 6.27(a)* the switches are in "space" state:

> Q37 and Q34 are turned on by TP4 at 0V, to provide the filter discharge path.
> Q33 and Q36 are turned off by TP5 at +31.6V
> Q32 and Q35 are turned off by TP3 at -11V

The filter discharges via resistor R79 and FETs Q34 and Q37. During both Mark and Space periods, R79 (78.7kOhms) is a major determinant of the 7-pole filter charge and discharge currents. Because in 'space' state the 'On' resistances of Q34 and Q37 (3Ω-5Ω each) are very small in comparison, the potential at link B can be regarded as zero when considering the effects of the other switching voltages.

Reverse leakage currents in JFET junctions are normally of the order of a few picoamps unless the junction voltages are much in excess of 20V. To control leakage effects from the four JFETs which are turned off, the cathode of diode D20 is connected to the common junction of the four devices. Its anode is returned to the junction of R125 and R126, close to +10V.

The reverse leakage characteristics for a J108 FET (Q35 and Q32) are generally several times heavier than for a J174 (Q36 and Q33). This means that in this switch, the leakage currents via Q35 and Q32 out of the common junction are 4-5 times greater than those entering via Q36 and Q33.

The net leakage out of the junction holds D20 slightly in forward bias, so that its cathode cannot rise above about +10.3V when the four FETs are turned off in 'space' state. Thus D20 guards the 'buffer' FETs Q33 and Q32 from the effects of the relatively high voltage on Q36 gate. The effects of the buffer FETs' own leakages on the voltage at the filter input can be regarded as negligible, because Q33 leakage currents towards LKB are virtually balanced by those away via Q32.

6.5.8.3 Filter Charge Path

To preserve linearity over the full range of Mark:Period ratios, the filter charging path time constant must closely match that of the discharge path. Q35 and Q32 are factory-selected to form a matched set with Q34 and Q37, all J108 N-channel FETs (the 'on' resistance of P-channel FETs in a true complementary switch would be much higher, of the order of 30Ω-40Ω). Nevertheless, to avoid high voltages being developed across Q35/Q32 when changing between states (causing excessive leakage), P-channel FETs are employed. Q36/Q33 are switched on before (and switched off after) Q35/Q32.

Fig. 6.27(b) shows this intermediate state after $\overline{\text{SET2}}$ and before $\overline{\text{SET1}}$, and *Fig. 6.27(c)* illustrates the fully-conducting state after $\overline{\text{SET1}}$. Note that for descriptive purposes, the second step on LKB waveform is heavily exaggerated, and is not readily viewed on an oscilloscope. The slightly longer charging time-constant during this half micro-second, due to the higher resistance of Q36/Q33, is not sufficient to disturb the linearity of the filter in excess of specification.

The voltage between TP4 and LKB during 'mark' state is some 31 volts. In the absence of D19, an adverse voltage distribution could cause excessive reverse leakage in Q37. D19 controls the distribution by limiting the voltage at its cathode to about +10V, constraining Q37 source-gate voltage to a tolerable 20.5V.

6.5.9 7-POLE FILTER

(Circuit Diagram 430652 Page 11.4-1)

M26, M28, M32, Q41 and Q42, together with associated capacitors and resistors, form a 7-pole Bessel filter in three active elements; providing approximately 135dB of attenuation at the 125Hz switching frequency and increasing at a rate of 140dB/decade. This allows sufficient bandwidth to avoid excessive settling time while reducing the output ripple to within instrument specification. Q41 and Q42 source-followers provide input bias currents for M26 and M28 from the 15V supplies, and buffer the line from bias-current effects. M32 bias-current effects are insignificant.

The '+Ve SUMMING AMP' filter output DC voltage (TP13), is fed to a buffer amplifier for subsequent summing with the output from the Least-Significant Switch offset-bias amplifier. R101 and C51 prevent any spike remnants from the chopper-stabilized buffer amplifier being fed back into the filter.

6.5.10 SUMMING AMPLIFIER

(Circuit Diagram 430652 Page 11.4-3)

6.5.10.1 '+VE SUMMING AMP' Buffer

M33, M34 and Q44 buffer the '+Ve SUMMING AMP' voltage output from the 7-pole filter (this is proportional to the Mark/Period ratio of the 13 most-significant bits of the binary word which defines the instrument output value demand).

M33 is a high-gain, chopper-stabilized integrator with a bandwidth of approximately 10Hz, and Q44 provides additional bandwidth for rejection of HF common-mode noise.

M35, D14, D15, Q48 and Q49 generate boot-strapped supplies to preserve full dynamic-range linearity. Q46 and Q47 establish 3mA constant-current drives for D14 and D15.

The whole amplifier acts as a voltage-follower, M34/Q45 providing the output drive, buffering the output of M33 and Q44. The output 'Hi O/P' is delivered to the DC assembly via RL2 for positive DC outputs, or via RL1 if the output is to be negative. For AC outputs, it is always delivered to the AC assembly via RL2 (RL1 being permanently de-energized for AC ranges). The output is sensed either in the DC or AC assembly to account for the volts-drops in the connecting circuit. The sense feedback voltage 'Hi SENSE' is applied to the inverting input of the whole buffer via R98.

For a zero count in the MSB comparator, the filter output voltage is approximately +3.2mV, and a full count of 8191 would produce +20.6V. These are the voltages which are developed at the buffer output.

6.5.10.2 '-VE SUMMING AMP' Buffer

M38, M39 and Q51 buffer the '-Ve SUMMING AMP' voltage output from the Offset Bias Amplifier derived from the 3-pole filter (this is proportional to the Mark/Period ratio of the 12 least-significant bits of the binary word which defines the instrument output value demand).

The dynamic range of the filter output voltage was originally defined by the Reference Buffer (8.83V) for efficient operation of the FET switching circuitry.

It was scaled in the Offset Bias Amplifier to give +27.5V for an LSB comparator count of zero (from approx. +1.1mV at TP6), and +24.5V for a full count of 4095 (from +8.83V at TP6). It now needs to be scaled down so that it has correct proportionality to the '+Ve SUMMING AMP' dynamic range.

R99 and R100 attenuate the '-Ve SUMMING AMP' input voltage by a factor of 0.8545×10^{-3}. At zero count, +27.5V is reduced to +23.5mV, and at full count +24.5V reduces to +20.9mV. These are the extremes of voltage developed at the buffer output.

The whole amplifier acts as a voltage-follower, but without bootstrapped supplies (the small input voltage dynamic range of approx. 2.5mV does not warrant it). Otherwise the circuit is identical to the '+Ve SUMMING AMP'. M39/Q52 provide the output drive, buffering the output of M38 and Q51.

The output 'Lo O/P' is delivered to the DC assembly via RL2 for positive DC outputs, or via RL1 if the output is to be negative. For AC outputs, it is always delivered to the AC assembly via RL2 (RL1 being permanently de-energized for AC ranges).

The feedback voltage, sensed in the DC or AC assembly, is returned via the appropriate relay, and applied to the inverting input of the whole buffer via R127.

6.5.10.3 Summing

On the DC or AC assembly, the outputs from the two buffers are summed by defining the 'Lo O/P' level as 'Reference Common' (Common-1 for DC, Common-2C for AC), and the 'Hi O/P' level as 'REF+Ve'. Thus at any instant, the voltage developed as 'REF+Ve' with respect to 'Reference Common' will always be 'Hi O/P' minus 'Lo O/P', at their current values.

The reference voltages and reference division ciruitry are chosen to allow for software calibration adjustments, so the summing span overlaps the possible required span of 0V to 19.999999V at both extremes:

With an overall 25-bit count of zero in the comparators, REF+Ve is +3.2mV minus +23.5mV, a negative overlap of 20.3mV.

At overall full count, REF+Ve is +20.6V minus +20.9mV, approximately +20.58V.

6.5.10.4 Bipolar Reference Switching

Relays RL1 and RL2 are used in DC ranges for polarity reversal. However, this is not necessary for AC operation, for which RL1 is un-energized, and RL2 is energized, outputs from the summing buffers being fed to the AC assembly via RL2.

6.5.10.5 DC and AC References

For DC operation, the summed DC reference is applied to the Error Amplifier directly *(refer to page 11.5-1)*, but for AC operation, the DC reference is applied to a voltage divider which is used to provide a 'Quasi-sinewave' AC reference signal. The generation of this signal is described in *Section 6.6.*

6.6 AC REFERENCE - THE QUASI-SINEWAVE

6.6.1 AC-to-AC SENSE/REF COMPARISON

In the Sense/Reference comparator, a considerable advantage is gained by comparing AC with AC. (If AC sense were compared with DC reference, small DC offsets would be magnified, leading to 'DC turnover' errors). The AC waveform used as reference is constructed in ten steps by a digitally controlled switching network, based on the DC reference as its peak value. It has been given the name 'Quasi-Sinewave".

To drive the VCA, the comparator produces a DC error signal which is proportional to the difference in 'Mean Square' values, and is driven to zero by the action of the Output-Sense loop. At zero error the RMS value of the comparator's sense input has thus been adjusted by the loop to be equal to the RMS value of its reference input.

On the 1V Range there is neither amplification nor attenuation in the Output-Sense loop. The quasi-sinewave is designed so that with the 1V Range selected, its RMS value is equal to the voltage demanded on the front panel OUTPUT display, (with small, controlled adjustments for calibration).

On higher ranges, decades of amplification are switched in to set the output to the demanded voltage. Switched decades of attenuation reduce the sensed sinewave back to the 1V-Range level for comparison with the quasi-sinewave.

For millivolt ranges, the instrument output terminals are not within the output/sense loop. Instead, the AC 1V output from the 1V buffer is sensed internally and applied to the comparator to complete the loop. The AC 1V signal is reduced to the selected millivolt range levels at the terminals by precise, passive, decade attenuators.

On current ranges, the current reference is derived from either the closed 1V or 10V Range Output/Sense loop.

Therefore on all ranges the Output/Sense loop gain is driven to a magnitude of 1, so that the VCA and the comparator both operate at 1V Range levels.

6.6.2 DC REFERENCE - SCALING for AC

The Reference Divider hardware is common to both DC and AC outputs. On DC ranges, the basic voltage range is the 10V Range, with 100% overrange at Full Scale. In these cases the full span of reference values is employed, generating the resolution necessary to accommodate the DC accuracy available.

The same analog accuracy is not available for AC, so the high resolution is not necessary. Moreover, the linearity of the analog circuitry is improved by using a smaller dynamic range in the reference circuits. So for AC outputs the 1V Range is the basic range, and the software scales its demanded value accordingly.

The sensed output is compared against the quasi-sinewave, whose characteristics match those of the sensed sinewave. To construct the quasi-sinewave, the DC reference voltage needs to be set as its peak value.

The software imposes the scaling factors which establish the reference voltage at the peak value of the quasi-sinewave. Thus the full span of the 25-bit comparator, and hence the possible dynamic range of the DC reference, are realized only on DC ranges and at times when the Reference Divider itself is being calibrated.

Before initial calibration, the maximum obtainable reference voltage for AC is slightly greater than 2.8V, and the minimum is slightly less than 125mV. This overlaps the peak voltages of the quasi-sinewaves corresponding to the maximum and minimum values of sensed output; giving a margin for accurate calibration from digital gain factors held in the non-volatile calibration memory.

6.6.3 DC REFERENCE - VOLTAGE VALUES for AC

As mentioned earlier, the DC Reference is used to establish the amplitude of the quasi-sinewave. When the 1V AC Range is selected, the reference is set to the peak value of the quasi-sinewave, which is 1.397 times the demanded RMS (sinewave) voltage output of the instrument. In normal use, therefore, the reference voltage is adjusted by front panel OUTPUT display selections; between 125.7mV (for 0.9V selection) and 2.79V (for 1.999999V selection), plus or minus any user-calibration corrections.

On higher and lower AC ranges, analog range switching in the sense amplifiers scales the sense voltages for comparison with the same RMS voltage span of quasi-sinewaves.

6.6.4 REFERENCE INVERTER

(Circuit Diagram 400844 page 11.7-2)

The quasi-sinewave is derived by a specific form of D-A converter, selecting voltages from a divider network. Because negative values are required, the divider is strung between positive and negative reference voltages. The unity-gain Reference Inverter generates the negative reference 'REF-Ve' by inverting 'REF+Ve'.

M1, M2 and Q1 perform the inversion. M2 generates the bandwidth necessary for amplitude switching operations, while chopper-stabilized integrator M1 removes DC offsets, always referring the inverter output to Common-2C. To compensate for RMS value changes in the quasi-sinewave (due to switching errors arising from frequency changes), feedback from the quasi-sinewave is applied via R1, C4, R4 and C5. Q1 provides the output drive to the quasi-sinewave generator.

6.6.5 QUASI-SINEWAVE GENERATOR

(Circuit Diagram 400844 page 11.7-3)

The SYNC Ø input to M11-15 RESET, if set to Logic-1, would disable the Quasi-sinewave sequence counter M11. The facility is not required in this application so J7-49 is unconnected on the Mother assembly *(Circuit Diagram 430604 Page 11.16-2)*. M11-15 is thus pulled down to logic-Ø by R40 to enable the quasi-sinewave for both AC Voltage and AC Current functions.

The quasi-sinewave is generated at a frequency determined by the Frequency Synthesizer 100Hz-4kHz output (*para 8.1.3.3* describes the synthesis), clocking the decade counter M11 via J7-50. This continuously recycles M11 in ascending count through $Q_{\emptyset}$ to Q_9, ten clocks constituting one cycle of the quasi-sinewave, so the quasi-sinewave runs at a frequency of between 10Hz and 400Hz. The carry C_{out} of M11 returns to the Synthesizer via J7-51 to be selected as the reference frequency for the 100Hz (10-330Hz) frequency range.

With increase of frequency range, the difference between the frequencies of output and quasi-sinewave increases in decade steps. As the comparison of sense and quasi-sinewave signals is performed at mean-square DC levels, this difference theoretically does not matter, so long as the signal is at an exact multiple of the quasi-sinewave frequency. However, to achieve optimum operation of the Sense/Reference comparator, each zero crossing of the quasi-sinewave is synchronized to coincide with a sense-signal zero crossing.

Synchronization is achieved by the clock input to M9, which controls the timing of the quasi-sinewave switches M8 and M14. Using the same clocks, M11 and M10 transit times prevent the data from arriving at M9 'D' inputs until the data already established there by the previous clock pulse has been latched at its outputs. Thus data ripples through M11 and M9 at successive clock pulses.

The ripple delays the data by one clock period and would, if left uncorrected, put the switching out of sequence. The arrangement of the connections between M11 outputs and M9 data inputs, combines appropriate outputs so as to correct the switching pattern. The table in *Fig. 6.28* demonstrates the rotation of 1 clock period; the quasi-sinewave steps being labelled at M9 inputs and outputs.

The quasi-sinewave is output to the transfer switching input to the Sig/Ref comparator at M16-1. The action of the transfer switch is described in *Section 9.5*.

A second output is filtered and fed back as compensation to the Reference Invertor as described earlier *(para 6.6.4)*.

Step	0	1	2	3	4	5	6	7	8	9
M11 Output at Logic-1:	Q_9	$Q_\varnothing$	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7	Q_8
M10 Output pin at Logic-1:	4	11	-	11	4	10	3	-	3	10
M9 Output pin at Logic-1:	O_1	O_4	O_5	O_4	O_1	O_2	$O_\varnothing$	O_3	$O_\varnothing$	O_2
Switch Energized M8 pin: / M14 pin:	5 / -	6 / -	13 / -	6 / -	5 / -	- / 5	- / 6	- / 13	- / 6	- / 5
Step Voltage fed to M16-1:	+0.42	+1.16	+1.397	+1.16	+0.42	-0.42	-1.16	-1.397	-1.16	-0.42

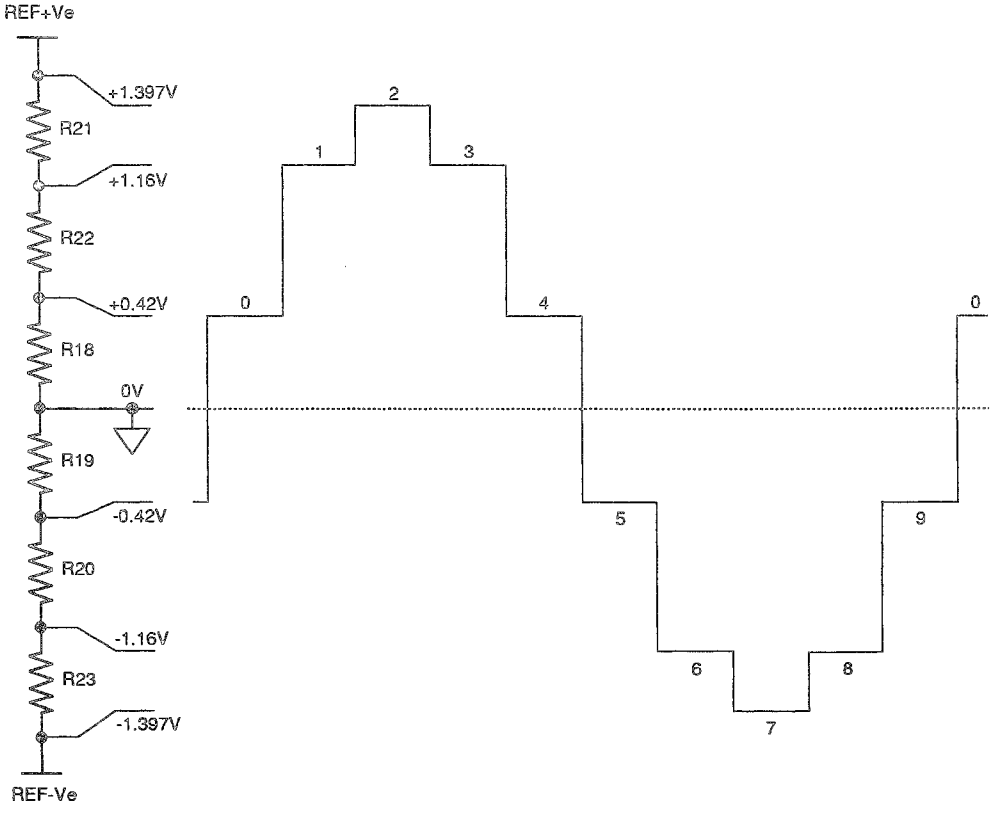


FIG. 6.28 QUASI-SINEWAVE GENERATION

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6.7 POWER SUPPLIES

The circuits described in this section perform the following functions:

- Line power switching, fusing, filtering, voltage selection and transformation.
- Main digital supply generation and distribution (Outguard).
- Display voltage supply generation.
- In-guard stabilized supply generation for Common-2 and Common-4 circuitry.

A simplified power-distribution block diagram appears at *Fig. 6.29*.

The power input module is mounted on the rear panel. The mains (line) transformer is located in the rear section of the instrument, close to the In-guard and Out-guard Power Supply assemblies.

(For details of location and attachment, refer to *Section 3*; and *Section 11, page 11.0-1*).

6.7.1 LINE POWER DISTRIBUTION

(Circuit Diagram 430830 Page 11.17-2)
(Fig.6.29)

The single phase line supply enters via a 3-pole input cable at the rear of the instrument. The cable connector plugs into a power input module which contains a fuse, filter and line voltage selector pcb. (For details of fuse values and operating voltage selection refer to the *User's Handbook, Section 2*).

Both 'line' and 'neutral' rails are filtered by a low-pass LC network before being fed through the instrument to the two-pole 'Power' switch on the front panel.

The switched supply is fed back into the power input module, to the voltage selector pcb, which configures the line transformer primary circuit as determined by the user. Power for the air circulation fan is provided directly from the power input module.

All line transformer secondaries are electrostatically decoupled from the primaries by a ground screen between the windings. The secondaries which supply the Common-2 and Common-4 in-guard circuits are decoupled by an additional screen which is connected to the instrument guard.

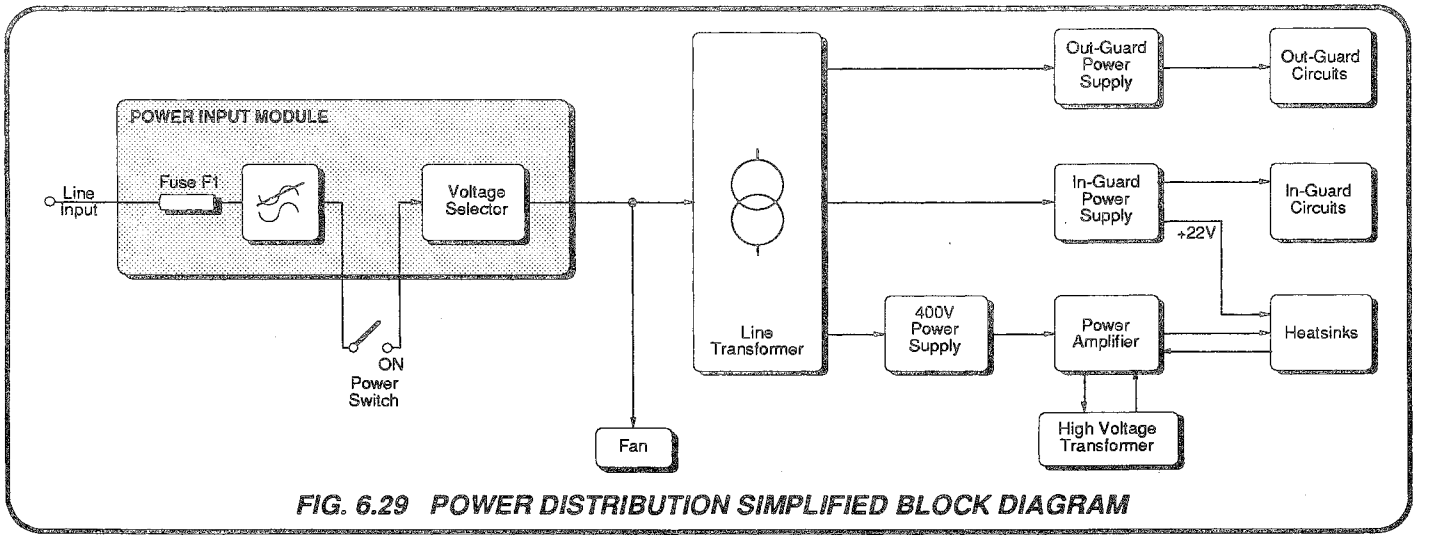

FIG. 6.29 POWER DISTRIBUTION SIMPLIFIED BLOCK DIAGRAM

6.7.2 OUT-GUARD POWER SUPPLIES

(Circuit Diagram 400996 Page 11.10-1)

6.7.2.1 Digital Main Supply

This circuit provides:

- +8V unregulated supply for the Front and Digital assemblies.
- +5V regulated supply for out-guard digital circuits.

6.7.2.2 +8V Unregulated Supply

This is taken directly from full-wave rectifier D101, D102 via fuse F101 (rated at 4A).

6.7.2.3 +5V Regulated Supply

The output voltage is controlled by series regulator Q102, Q103. Load current is sensed by R1 in the base-emitter circuit of Q101, which provides short circuit current limiting by turning on and thereby reducing the base drive in Q102 and Q103 if the load current exceeds approximately 2A. The 2.45V zener D104 provides the reference voltage for comparator U101 at U101-3. The output voltage is sensed between the +5V and DIG COMMON rails on the Mother assembly, and divided down to reference potential at U101-2. R106 and R109 ensure that regulation persists even if the sense links are disconnected.

U101 output drives current sink Q104 whose collector current controls Q102 and Q103 conduction. If the +5V rail voltage falls due to loading, Q104 collector current increases, increasing Q102 and Q103 conduction to restore the rail voltage. Zener D105 prevents the positive excursion of the +5V rail in the event of regulator breakdown. Zener D103 restricts positive excursions of Q104 base voltage, and hence the maximum base current in Q102 and Q103. C102 and C103 give a controlled fast response to reduce the effects of transients on the +5V rail.

PTC thermistor R112 protects the power supply from high ground-leakage currents, notably in the external circuits of the IEEE 488 bus system. R112 presents a minimum of 80Ω between the digital common line and ground; this resistance increasing with increasing ground-leakage current.

6.7.2.4 Display Supply

The vacuum fluorescent displays on the Front Panel Assembly require a low-voltage (6.7V rms typical) AC filament supply centred around -24V with respect to Digital Common. This AC supply is generated from -VFIL_HI (-20V) and -VFIL_LO (-28V) by U110 on the Display Assembly *(Circuit Diagram 400993 Page 11.1-2)*.

-VFIL_HI and -VFIL_LO are generated from a split secondary winding on the line transformer by 25V positive voltage regulator U102 and 8V negative voltage regulator U103 respectively. The positive output of U102 is connected to the +5V out-guard supply so that its negative output sits at -20V and the negative output of U103 sits at -28V.

6.7.2.5 Common Mode Null

This circuit provides a line-hum cancelling (bucking) output to the instrument guard network. For adjustments refer to *Section 4.9*.

6.7.3 IN-GUARD POWER SUPPLIES

(Circuit Diagram 430554 Pages 11.11-1 and 11.11-2)

6.7.3.1 In-Guard Common-2 Supplies

The general 15V supply for the analog circuitry is provided by three integrated-circuit regulators *(page 11.11-1)* as follows:

- +15V from M2
  Because of the high current taken from this supply, the regulator power dissipation is shared. The rectifier output is first regulated to +18.5V by Q1, Q3 and D9; and then to +15V by M2.
- -15V from M1
  This is a mirror image of the positive supply.
- -10V from M6
  Derived from the -15V supply.

The supply is protected by 3.15A fuses F3 and F4 at the bridge rectifier output.

The 8V supply for the Sine-Source assembly is provided by two integrated-circuit regulators M8 and M9 *(page 11.11-2)*. The supply is protected by 1A fuses F5 and F6 at the bridge rectifier output. Chokes L7 and L9 attenuate HF transients on the AC input.

6.7.3.2 ±22V Current Option Supply

This provides +22V and -22V unregulated power outputs to the PS/I Heatsink assembly. Both supplies are protected at 4A by fuses F1 and F2. The 22V common return is maintained close to the common-2 return potential by resistor R1.

6.7.3.3 Reference Divider Common-4 Supplies
(Circuit Diagram 430554 Pages 11.11-2)

This circuit provides +36V, +15V and -15V regulated outputs to the Reference Divider in-guard circuits. The +36V supply is also used to power the +20V Master DC Reference.

Two secondary windings of the line transformer are used, and inter-supply transients are reduced by the special coupling arrangements of common-mode choke L10. The rectified output from bridge W4 is series-regulated by M3 to produce the +36V supply. R2/R3 sense the output voltage.

D11 and M4 reduce the +36V to generate the +15V regulated supply.

The -15V supply is provided by bridge W3 and regulator M7.

6.7.3.4 ±38V Common-2 Supply
(Circuit Diagrams 430653 Page 11.12-1 and 430604 Page 11.16-5)

The ±38V regulated supply is used for two purposes:

- to power the 10V Amplifier in the Power Amplifier assembly;
- to provide a lower positive source voltage to reduce dissipation on the Power Amplifier assembly, when negative voltages are being output on the 100V DC Range (refer to *sub-section 7.8.3.4).*

It is plugged into the Mother assembly in the rear compartment next to the Heatsinks.

The mains (line) transformer 40VRMS secondary centre tap is referred to Common-2 on the Mother assembly. It provides a variable AC output by R25 on the Mother assembly to balance line-induced voltages on the guard screens. The 40V is rectified, filtered and smoothed on the Mother assembly before being passed to the regulator at approx. 50VDC.

On the ±38V Power Supply assembly the output voltage is controlled by series regulators Q2 and Q1. As the regulator is symmetrical, only the positive side is described.

The output voltage is divided by R26 and R25 to provide a sense signal for comparator M1, which is powered by a local shunt regulator D8/R16/C8. The 2.45V reference for the comparator is derived by D6/R23 from the comparator supply.

M1 output drives Q8 whose collector voltage controls Q6 and hence Q2 conduction. If the +38V rail voltage falls due to loading, Q8 collector voltage rises, increasing Q5 and Q6 conduction to restore the rail voltage.

Load current is sensed by R24 in the base-emitter circuit of Q5, which is normally cut off unless the load current exceeds 170mA. At this point Q5 conducts and pulls down the base of Q6, setting a hard current limit.

Zener diode D2 turns Q5 hard on in the event of an output short circuit, providing a rapid reponse to catastrophic failure in the power amplifier circuitry. As the output voltage falls below +22V, D2 arrests the fall on Q5 base, switching Q5 hard on and turning Q6 and Q2 off. This leaves D2, R8 and R9 controlling the output current, which falls to less than 500µA.

When the load is removed, the conduction of Q5 via R26/R25 is insufficient to hold Q6 cut off, especially as Q8 is also cut off by the comparator. So Q2 is allowed to conduct, the output voltage rises until first D2, and then Q5, cut off and the output voltage is restored to comparator control.

The ±38V output is taken through wired-in fuses F1 and F2. These merely protect the PCB tracking in the event of an output short-circuit. The output voltages are protected from reverse polarity by D1 and D2 on the Mother assembly.

6.7.3.5 ±38V Supply Failure
(Circuit Diagram 430618 Page 11.9-4)

The ±38V output voltage is monitored in the Power Amplifier assembly. The monitor is described in *Section 7, para 7.8.6.3.*

6.7.3.6 ±400V Common-2 Supply

This is described in *Section 7, paras 7.8.5 and 7.8.6.4.*

SECTION 7
DC VOLTAGE OUTPUTS - AMPLITUDE CONTROL SYSTEM

7.1 INTRODUCTION

When DC Voltage Function is selected, a relay (RL2) on the Reference Divider assembly feeds the output of the summing amplifier into the DC assembly as DC Ref (Hi and Lo), the value of which represents the demanded output voltage and polarity. The DC Voltage circuitry selects the required range, from switching data transmitted into guard via the Serial Data Link. The selected range circuit generates the demanded voltage at the output terminals. Output switching and protection are provided.

7.1.2 DC VOLTAGE SYSTEM BLOCK DIAGRAM

The DC Voltage Amplitude Control System is briefly described in *Section 5*, and illustrated in the Block diagram of *Fig. 5.3*. DC Voltage Ranges up to 100V are described in *Section 5.6*, and the DC 1000V Range in *Section 5.8.1*; at block diagram level.

7.1.3 CIRCUIT OPERATION

The circuits described in this section perform the following functions:

- Buffer the DC Ref voltage (-20V to +20V) and provide output voltages to the instrument terminals, on the 10V DC Range.
- Amplify the DC Ref voltage providing output voltages:

  -200V to +200V on 100V Range
  -1100V to +1100V on 1000V Range

- Attenuate the DC Ref voltage and provide output voltages between -2V and +2V on the 1V DC Range.
- Further attenuate the 1V Range voltages and provide output voltages:

  -200mV to +200mV on 100mV Range
  -20mV to +20mV on 10mV Range
  -2mV to +2mV on 1mV Range
  -200µV to +200µV on 100µV Range.

- On the 10V Range, sense the output voltage (at the load in Remote Sense), making continuous, direct comparisons in a closed negative-feedback loop with the DC Ref voltage input from the Precision Divider. The comparison generates an 'error' voltage which corrects the output voltage.
- On the 1V Range, sense the output voltage at 1V Range levels, comparing the sensed voltage with the attenuated DC Ref input, and correcting the output as on the 10V Range.
- On the 100V Range, sense the output voltage at 100V levels, and reduce the sensed voltage to 10V levels. Compare the attenuated voltage with the DC Ref input from the Reference Divider and correct the output voltage as on the 10V Range.
- On ranges below 1V; sense the 1V Buffer output at 1V Range levels, correcting its output as on the 1V Range.
- On the 1000V Range, provide a VCA drive from the Error Amplifier to a DC Modulator for the high voltage amplification circuits. Attenuate the sensed output voltage, comparing the attenuated voltage with the DC Ref input at 10V Range levels, and correcting the output as on the 10V Range.
- Provide switching of DC Voltage Output, Range, Guard and Sense, under the control of signals from the Analog Control Interface.
- Sense excess currents in the output circuit, providing a $\overline{\text{LIM ST}}$ status signal to the CPU via the Analog Control Interface.
- Sense High Voltage State (at approx. >130V) on the PHI (I+) output line, providing a $\overline{\text{HV ST}}$ signal to the CPU via the Analog Control Interface.

Many of the circuits described in this section are located on the DC PCB assembly. The major exceptions are as follows:

10V Range Buffer stage	-	Power Amplifier assembly.
100V Amplifier	-	Power Amplifier assembly and Heatsink assemblies.
1000V Range output circuits	-	LF and HF transformer assemblies and the High Voltage assembly.
Function Switching	-	Current/Ohms assembly.
Output Filtering	-	Terminal Board assembly.

7.2 LOW VOLTAGE LOOPS

(Fig. 7.1)

The 10V range is regarded as the basic DC range of the instrument, because it uses the full 20V Reference, suffering no overall voltage attenuation nor amplification in its output loop. However, it does require power amplification at dissipations which preclude its positioning within the thermal shield, so its output buffer is located on the Power Amplifier assembly. This factor complicates the routing of its signals.

The 1V range loop is more direct; its buffer is located on the DC assembly, and there are fewer circuit elements to describe in its path. For reasons of simplicity, therefore, the 1V range is chosen for this description of the basic DC output loop.

The descriptions in *Section 7.2.1* and *Section 7.3* concentrate on the signal path of the 1V Range loop; from the polarity switch in the Precision Divider, out to the 'Power' terminals, and back to the 'Sense' input of the Error Amplifier.

For descriptions of the alterations to the 1V loop to accommodate the other DC voltage ranges, refer to the following sub-sections:

100mV Range	*7.4*
100µV to 10mV Ranges	*7.5*
10V Range	*7.6*
100V Range	*7.8*
1kV Range	*7.9*

On the circuit diagrams in *Section 11*, all relay contacts are shown with their relays in the unactivated condition .

7.2.1 1V RANGE SUMMARY

The low voltage loop and routing are illustrated in the simplified diagram of *Fig. 7.1*. Switching contacts are shown in positions set for the 1V Range.

DC Ref is variable between -20V and +20V referred to common-1, and the 1V attenuator provides voltages between -2V and +2V. The Error Amplifier and 1V Buffer are connected to form a voltage-follower when I+ is connected to Hi (in either local or remote sense).

The output from the 1V Buffer is connected directly to the I+ terminal via power switching, the sense feedback returning from the Hi terminal, via sense switching, to the Error Amplifier inverting input. The sensed output voltage is adjusted by the feedback until it equals the attenuated DC Ref Value, i.e. for zero differential input to the Error Amplifier.

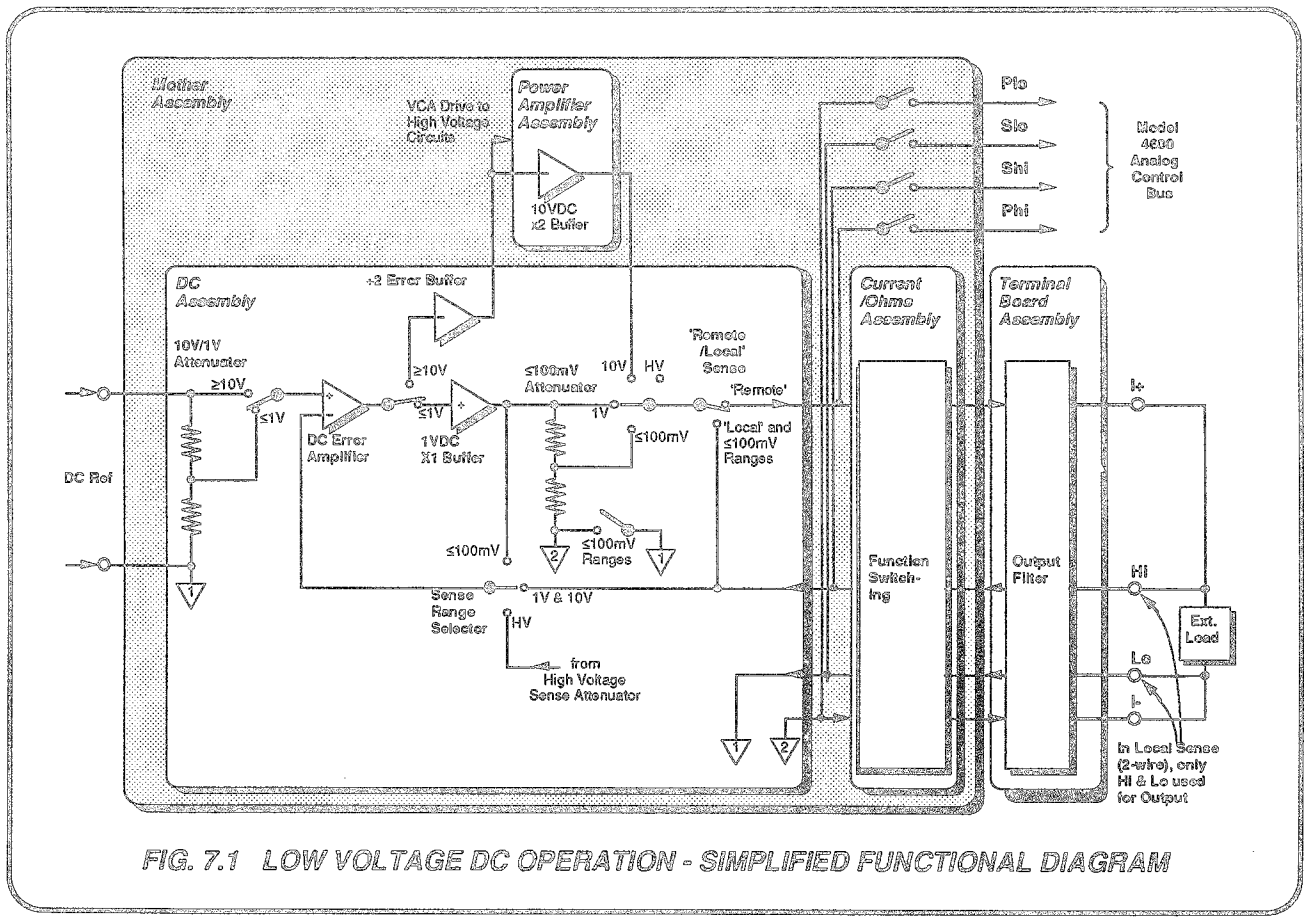

FIG. 7.1 LOW VOLTAGE DC OPERATION - SIMPLIFIED FUNCTIONAL DIAGRAM

7.3 DC 1V LOOP

7.3.1 REFERENCE DIVIDER ASSEMBLY

(Circuit diagram 430652 Page 11.4-3)

For positive outputs, the positive DC Reference PHI(REF), PLO(REF), SHI(REF) and SLO(REF) pass via energized relay RL2, to be output as a 4-wire sensed connection into the DC assembly. The four lines are routed out at J4 pins 9, 10, 11 and 12 into the Mother assembly. For negative outputs, energized relay RL1 configures the lines to give a negative DC reference.

7.3.2 DC ASSEMBLY

(Circuit diagram 430536 Page 11.5-1)

The DC Reference enters at J5 pins 1, 2, 3 and 4. On DC Voltage ranges, RL18 connects the power and sense lines to the two star-points TP2 and TP3. TP3 is the signal Common-1 point, to which all instrument DC voltage sense inputs are referred.

For the 1V and lower ranges, RL16-5/4 connects the output of the 1V attenuator to the non-inverting input of the Error Amplifier. (On the 10V and higher ranges, RL16-8/9 connects the full DC Reference to the Error Amplifier.)

7.3.3 ERROR AMPLIFIER

The DC Ref Voltage from the Reference Divider is applied to two amplifiers: M21 is a high-gain chopper-stabilized integrator of approximately 10Hz bandwidth, Q5 provides additional bandwidth for rejection of HF common-mode noise. M20 provides additional gain and output drive, through a transient-suppressing diode clamp circuit.

The whole amplifier is bootstrapped by M22, D48, D49, Q6, Q7 and Q10. Q8/Q9 provide 1.4mA constant-current drives for D48/D49 over the range of BS-Common variation (-20V to +20V on the 10V and higher ranges). Power for the bootstrapped amplifier is obtained originally from the ±38V supply; used also to power the 10V Buffer in the PA assembly, referred to Common-2.

Extensive screening and filtering is used to eliminate the effects of the chopping spikes at inputs and output of M21.

7.3.4 1V BUFFER

On the 1V and lower ranges the error amplifier output is applied to the 1V Buffer, via the closed contacts 10/11 of energized relay RL16. A current amplifier M23 is chosen, as the buffer has to drive the external load directly via the output switching, output lines and external leads. It also drives the 100mV Attenuator on the 100µV - 100mV ranges.

M23 is powered by a separate, individually filtered, 8V supply *(refer to pages 11.5-4 and 11.11-2)*. Its input and output are protected by back-to-back zener diodes.

The output from the 1V buffer is connected, via contacts 12/7 of energized relay RL3, to the '1V+10V+100V' PHI(DCV) star point.

7.3.5 RANGE SWITCHING

On the 1V and 10V ranges the 1V+10V+100V star point is decoupled to Common-2A by C28 via contacts 2/3 of energized relay RL4.

Relay RL5 is energized on the 1V and 10V ranges; and after passing through the back-to-back contacts RL5-8/9, which cancel their own thermal EMFs, the 1V+10V+100V signal is renamed 'PHI(DCV)'.

7.3.6 OUTPUT SWITCHING

(Circuit Diagram 430536 Page 11.5-2)

The PHI(DCV) output and other connections from the Range relays *(Page 11.5-1)* are passed to the instrument output terminals via several relay contacts which provide switching for Remote or Local Sense, Remote or Local Guard, and Output On/Off.

The output does not travel directly to the terminals from the DC assembly, as further switching is required. If Option 40 or 50 is fitted, function changes switch the terminal lines on the Current/Ohms assembly. If neither Option 40 nor 50 is fitted, a Current/Ohms Link PCB (Part No. 410288) is fitted in place of the Current/Ohms assembly. This PCB provides direct connections for the signals, on their route to the instrument terminals *(para 7.3.8.1.)*

7.3.6.1 DCV/ACV Switching

For DC voltage ranges, relays RL10 and RL11 are energized. The PHI(DCV) line from the range relays passes via RL10 contacts, TP8, 1A fuse F6, and RL15 contacts (if output is set ON); to the PHI(V) line at J5-19. For DC voltage outputs, the four ACV lines at J5-25/26/29/30 are disconnected by relays in the AC assembly.

In Remote Sense, the power return line PLO(DCV) is linked via RL11 contacts, 1A fuses F4 and F3, relay RL14 and RL15 contacts to J5-23 as PLO(V). PLO(DCV) is held close to Common-2A by R56/C30 *(page 11.5-1)*, being protected against excessive departure from Common-2A potential by the back-to-back 3V zeners D13 and D25.

The voltage developed across R56 by the output current is monitored by comparator M13 *(page 11.5-2)*.

7.3.6.2 Output On/Off.

Because the DCV and ACV lines are separately switched, a single independent 4-pole relay RL15 can be used to set output on and off. Thus the lines at J5-19/20/23/24 carry either DCV or ACV signals to and from the output terminals.

Where ACV and DCV join, the power lines change their names to PHI(V) and PLO(V).

7.3.6.3 Remote Sense Switching.

When Remote Sense is not selected, two-wire outputs to external loads can only be connected from the Hi and Lo terminals (a relay on the Mother assembly disconnects the I+ terminal). Relay contacts RL14-9/8 connect PHI(DCV) to SHI(DCV), and RL14-3/2 connect PLO(DCV) to SLO(DCV). Relay contact RL14-5/4 is open, severing the connection to the I- terminal.

In Remote Sense relay RL14 is energized, removing the connections between the power and sense lines, and RL14-5/4 reinstates the link from PLO(DCV) to the I- terminal. This gives full 4-wire sensing at the external load.

7.3.6.4 Remote Guard Switching

The front panel 'Guard' terminals are permanently connected to the internal guard shields via J5-15/16 and J5-11/12. With 'Remote Guard' selected, the direct connection between Guard and Lo is severed by the open contact of energized relay RL17. R121 damps any high frequency resonance in the combined internal and external guard circuits; C62 reducing HF noise on the millivolt ranges. With Remote Guard off, RL17 connects the guards to PLO(V) via PTC thermistor R97, which also assists in reducing millivolt noise.

7.3.7 OUTPUT PROTECTION

Two circuits are described in the following paragraphs:

- The DC Overcurrent Detector, sensing the current flowing in the PLO(DCV) return line and sending a signal to the status-reporting logic if the DC current exceeds approx. 28.5mA.

  On the 100V and 1kV DC ranges the 'LIM DET' signal is sent, but on the 10V DC and lower ranges the '$\overline{\text{LIM ST}}$' signal is made active.

- The Overvoltage Detector provides an indication to the CPU that the output voltage is in 'High Voltage State', ie. the '$\overline{\text{HV ST}}$' signal is activated if the output DC or peak AC voltage is greater than 110V. If the instrument has not been programmed into High Voltage State, then an anomaly exists, and remedial action is taken by the CPU.

The results of activating the overcurrent detector are described later in *sub-section 7.12.7.*

7.3.7.1 DC Overcurrent Detection

On DC voltage ranges of 1V and higher, the current taken by the instrument load develops a voltage across resistor R56 *(page 11.5-1)*, which is applied to the resistor chain R31/R30/R36 *(page 11.5-2)*. On 100mV and lower ranges R56 is shorted out by relays RL2-5/4 *(page 11.5-1)*, RL11-2/5 and 11/8, and RL14-2/3 *(page 11.5-2)*.

M13 is an open-collector comparator wired to detect excessive voltages across R30/R36 (R31 is the common bias resistor). Diodes D17 and D18 set the reference potential at M13-3 (for positive outputs) to approx. +285mV; and at M13-6 (negative outputs) to approx. -285mV. Under normal operation, when the output current is less than 25mA, both halves of M13 are held in the open-collector state.

When the output current through R56 exceeds approximately 28.5mA, the voltage across it exceeds 285mV and one of the halves of M13 switches its output to the negative rail (analog logic-Ø). Diode D52 conducts, pulling M10-6 and M10-9 to logic-Ø:

LIM DET Activation:

On the 10V and lower DC ranges, M10-5 is permanently held at logic-1 disabling M10-6, so the overcurrent signal has no effect on M10-4, which is held at logic-1 and D3 remains in reverse bias. The LIM DET signal is not activated.

On the 100VDC or 1kVDC range, M10-6 is enabled by M10-5 at logic-Ø, so the overcurrent signal sets M10-4 to logic-Ø and LIM DET is activated at logic-1.

$\overline{\text{LIM ST}}$ Activation:

In this case the effect of the 100VDC and 1kVDC signals is reversed, and M10-9 is sensitized to the DC overcurrent signal only on the 10V and 1V ranges, when M10-8 is at logic-Ø. For excessive DC output currents, M10-10 sets D9 cathode to logic-Ø pulling the $\overline{\text{LIM ST}}$ line to its logic-Ø active state.

The AC 1kV Overcurrent Detector receives no input on DC ranges, as no current passes through the sensing resistors R107 and R108.

7.3.7.2 High Voltage Status Detector ('Overvoltage')

In order to provide information to the CPU so that it can decide whether the High/Low voltage state is as demanded, the voltage level on the PHI(V) line (TP8) is monitored and compared against a reference. The detector senses DC levels for DC voltage outputs, or peak levels for AC voltage outputs.

M17 is a dual comparator whose hysteresis is set to ±1.22V. As long as the voltage on the PHI(V) line remains within approx. ±125V, the division ratio of M16 keeps the input to M17-5/9 within the ±1.22V hysteresis, and M17-12/7 remains at logic-1 (0V).

The PHI(V) voltage at TP8 is applied via R83 and R62 to M16-2, which is referred to Common-2B, M16-3 being connected directly to this common. Resistors R61 and R68 apply feedback to M16, setting its gain to -0.0098. C29, C31 and R63 ensure that any transient switching spikes do not activate the comparator. The output from M16-6 is compared with ±1.22V in comparator M17.

The open-collector comparator M17 is wired to detect excessive voltages at M16 output (R69 is the common bias resistor). Diodes D26 and D27 set the reference potential at M17-10 (for positive outputs) to +1.22V, and at M17-4 (negative outputs) to -1.22V. Under normal operation in low voltage state, the output voltage lies between -110V and +110V, and M16 output is between -1.07V and +1.07V. Both halves of M17 are thus held in the open-collector state.

If the DC PHI(V) voltage exceeds 125V (or for an AC peak corresponding to a sinewave RMS exceeding 90V), either M17-7 or M17-12 pulls towards logic-Ø. Current source Q2 permits only 3mA to flow in M17 output circuit, so the voltage input to D6 cathode and M12-11 (B trigger) suffers a negative-going trigger edge.

a. Effect of Overvoltage on DC Voltage Ranges

For DC outputs the 'Q' output of M12 is permanently held at logic-1 by $\overline{\text{DC FNCT}}$ at M12-13 set to logic-Ø, so the effect of the negative-going transition at M12-11 is suppressed. However, diode D6 conducts, pulling the $\overline{\text{HV ST}}$ line at J5-105 to logic-Ø (-15V). This is passed to the CPU, via the status register in the reference divider and the serial data interface.

The CPU is now aware that the DC output voltage exceeds 110V. The CPU has to make a decision, as to whether the programmed output voltage and the detected state are compatible. If High Voltage state has not been commanded, a fault is assumed and FAIL 2 message is presented on the MODE display.

b. Effect of Overvoltage on AC Voltage Ranges

For AC outputs the $\overline{\text{DC FNCT}}$ signal is inactive at logic-1, so M12-13 at logic-1 removes the reset. Monostable M12 is set to produce a logic-1 at its $\overline{Q}$ output (M12-9) unless its B input at M12-11 is edge-triggered negatively. In 'Low Voltage State' conditions no trigger is given, so M12-9 remains at logic-1, D7 and D6 are reverse-biassed and the $\overline{\text{HV ST}}$ line remains at the logic-1 level of 0V.

When the comparator output switches to logic-Ø, D6 conducts instantaneously to obtain the earliest possible reaction to the overvoltage. But as this is a peak value, the $\overline{\text{HV ST}}$ signal would revert to logic-1 without monostable M12. M12 produces a logic-Ø (-15V) pulse of 140ms duration, which forward-biasses D7, and the $\overline{\text{HV ST}}$ line transmits a logic-Ø pulse of 140ms duration. Successive positive or negative peaks of overvoltage retrigger the monostable, maintaining its $\overline{Q}$ output (and thus the $\overline{\text{HV ST}}$ signal) at logic-Ø.

7.3.8 ROUTING to the TERMINALS

The power and sense lines from J5-20/24 connect to the model 4600 analog bus via relays RL2 and RL3. When the 10A range is selected, these relays are closed and the front panel terminals isolated using relays on the Current/Ohms Assembly. Four wire sense is used, and the 4808 drives the analog bus with a -10V to +10V signal that the 4600 will convert to a -10A to +10A signal. The 4808 guard is transferred to the analog bus by the changeover relay RL4. The analog bus also contains a grounded signal ANABUSON which is used by the 4600 to detect that the 4808 is connected to the analog bus.

7.3.8.1 Current, Ohms or Current/Ohms Assembly

(Circuit Diagram 401008 page 11.8-6, Circuit Diagram 401047 page 11.8-8 or Circuit Diagram 430614 page 11.8-1 respectively)

With a voltage range selected, relays RL8 and RL9 on the Current or Current/Ohms assembly are un-energized as shown. On the Ohms or Current/Ohms assembly, relays RL24 and RL25 are also un-energized. Voltage Output relay RL23 is energized; connecting PHI(V) to J8-8/9 as 'PHI', and PLO(V) to J8-16/17 as 'PLO'.

PHI and PLO pass into the Mother assembly via at J8-25 and J8-29 respectively.

If no Current, Ohms or Current/Ohms assembly is fitted, a Link PCB (Part No. 410288) is fitted in its place. This shorts:

J8-25 [PHI(V)] to J8-8/9 [PHI],
J8-29 [PLO(V)] to J8-16/17[PLO].

These connections do not involve any switching.

7.3.8.2 Mother Assembly

(Circuit Diagram 430604 page 11.16-1)

PHI and PLO enter at J8-8/9 and J8-16/17 respectively.

PLO passes through the common mode choke L1 via J23-3 and then J26-4 as 'I-' to the Terminal Board assembly.

PHI is switched by relay RL1. If Remote Sense is not selected, RL1 is un-energized as shown; disconnecting PHI from the I+ terminal circuit, and shorting it to the sense SHI input line. When in Remote Sense, RL1 is energized and PHI passes through the common mode choke L1 via J23-1 and J26-1, and as 'I+' to the Terminal Board assembly.

7.3.8.3 Terminal Board Assembly

(Circuit Diagram 400995 page 11.17-3)

I+ and I- are filtered and passed to the front panel terminals. Ferrite bead E1 and C2 protect the internal circuitry from the effects of HF pickup in the external circuit.

7.3.9 1V LOOP - OUTPUT SENSING

7.3.9.1 Terminal Board Assembly

(Circuit Diagram 400995 page 11.17-3)

If Remote Sense is selected, the front panel sense terminals Hi and Lo are connected externally to I+ and I- respectively at the load. The sensed voltage is filtered by E2 and C3 to reject external HF pickup. Except on the 1000V Range, a signal ('R-', 'R+') originates as 'TERM FILTER' in the Reference Divider to energize relay K1, which introduces capacitor C1 to augment this HF rejection.

7.3.9.2 Mother Assembly

(Circuit Diagram 430604 page 11.16-1)

Lo passes through the common mode choke and directly to the Current assembly at J8-18 as SLO.

Hi also passes through the choke and enters the Current assembly as SHI at J8-10. However, if Remote Sense is not selected, it is shorted to PHI by relay RL1 for two-wire connection. RL1 is energized from the REM SENSE +ve and -ve lines from the DC assembly.

7.3.9.3 Current Assembly; Ohms Assembly or Current/Ohms Assembly

(Circuit Diagram 401008 page 11.8-6; Circuit Diagram 401047 page 11.8-8 or Circuit Diagram 430614 page 11.8-1 respectively)

With a voltage range selected, relays RL8 and RL9 on the Current or Current/Ohms assembly are un-energized as shown. On the Ohms or Current/Ohms assembly, relays RL24 and RL25 are also un-energized. RL23 is energized; connecting SHI into the Mother assembly as 'SHI(V)' via J8-26, and connecting SLO via J8-30 as 'SLO(V)'.

If no Current, Ohms or Current/Ohms assembly is fitted, a Link PCB shorts:

J8-10 [SHI] to J8-26 [SHI(V)],
J8-18 [SLO] to J8-30 [SLO(V)].

The connections involve no switching.

7.3.9.4 DC Assembly

(Circuit diagram 430536 Page 11.5-2)

In normal 4-wire operation (Remote Sense selected) with OUTPUT 'ON' on the 1V and 10V Ranges, relays RL10, RL11, RL14 and RL15 are energized.

SHI(V) enters from the Mother assembly at J5-20 and is passed directly through RL15 and RL10 contacts, 1A fuse F2, and to the range relays as SHI(DCV).

SLO(V) travels via RL15 and RL11 contacts to the range relays as SLO(DCV).

With Remote Sense not selected, relay RL14 is unenergized.
RL14-9/8 short SHI(V) to the power Hi output PHI(V).
RL14-2/3 short SLO(V) to the power Lo output PLO(V).

Refer to Page 11.5-1.

SLO(DCV) is referred to Reference Common-1. SHI(DCV) passes to the contacts 8/9/10/11 of energized 1V+10V range relay RL4, and via R77 to the inverting input of the Error Amplifier.

N.B. Although the relays are referred to above as 'energized' and 'un-energized', this is not strictly true as polarized relays are used to dispense with the power needed to hold the relays in.

This distinction is not significant to the present text, but is discussed later in *Section 7.11* where the relay logic is detailed.

7.4 100mV RANGE

The 1V Attenuator and 1V Buffer are connected into the circuit as for the 1V range. Relays RL1 and RL2 are energized. The output from the 1V buffer is connected to the star point at TP5 by RL1-7/12, and RL2-5/4 connects the Common-2 star point, at the base of the 100mV Attenuator, to Reference Common-1. Thus the 100mV Attenuator is connected across the 1V Buffer output.

The TP5 starpoint is connected directly to the Error Amplifier inverting input via RL2-9/8 and R77, completing the sense feedback. The Error Amplifier adjusts the voltage at TP5 until the error is reduced to zero; the TP5 voltage thus converges to that of the attenuated DC Ref at RL16-4.

The output of the 100mV Attenuator, at the TP6 star point, is therefore one hundredth of the DC Ref voltage, and can be varied between -200mV and +200mV. Note that the full DC Reference voltage resolution is available, so that the 100mV range resolution remains at $7^1/2$ digits. This is reflected in the resolution of the OUTPUT display on the instrument front panel.

The 100mV Attenuator output passes through RL2-2/3/10/11 to join the PHI(DCV) line. On ranges below 1V the Remote Sense relay RL14 *(page 11.5-2)* cannot be energized; so with DC Voltage and Output ON selected, the 100mV range output is routed via RL14-9/8 and the SHI(V) line on towards the Hi terminal on the front panel for 2-wire connection.

The other connection to the load returns via the Lo terminal, arriving at the DC assembly as SLO(V), referred to Common-1 *(page 11.5-1)*. Contacts 2 and 3 of unenergized Remote Sense relay RL14 connect the SLO(V) line to the PLO(DCV) line, and through the overcurrent sense resistor R56 to Common-2A. However, no overcurrent sensing is available on ranges below 1V, as R56 is shorted by the RL2-5/4 connection between Common-1 and Common-2A at the base of the 100mV Attenuator, and the contacts of the energized RL11 and un-energized RL14 *(page 11.5-2)*.

N.B. Although the relays are referred to above as 'energized' and 'un-energized', this is not strictly true as polarized relays are used to dispense with the power needed to hold the relays in.

This distinction is not significant to the present text, but is discussed later in *Section 7.11* where the relay logic is detailed.

7.5 100µV - 10mV RANGES

These ranges use the same relay settings as 100mV Range, so the output voltages remain at 1/100 of the DC Ref voltages. The differences lie in the spans of DC Ref voltages used.

To achieve the correct DC Ref span, the appropriate scaling is computed digitally and the 4-byte binary words set in the 13-bit and 12-bit comparator latches of the Analog Interface. The DC Ref spans are scaled as follows:

10mV Range	-	-2V to +2V
1mV Range	-	-200mV to +200mV
100µV Range	-	-20mV to +20mV

Because of this scaling, the resolution available on these ranges is reduced in proportion to the scaling ratio. The displayed output resolution is automatically adjusted according to range selection:

10V, 1V and 100mV Ranges	-	7½ digits
10mV Range	-	6½ digits
1mV Range	-	5½ digits
100µV Range	-	4½ digits

7.6 DC 10V LOOP

7.6.1 DC REF. and ERROR AMPLIFIER

(Circuit diagram 430536 Page 11.5-1)

The DC Ref signal is derived as for the 1V range, entering the DC assembly at the same pins: J5 pins 1, 2, 3 and 4. Relay RL18 again connects the power and sense lines to the two star-points TP2 and TP3, TP3 being the signal Common-1 point.

On this range, RL16-8/9 connects full DC Ref to the non-inverting input of the Error Amplifier, which operates as for the 1V range, except that the span of voltages is now the full -20V to +20V.

7.6.2 DC ÷2 ERROR BUFFER M14

(Circuit diagram 430536 Page 11.5-1)

The Error Amplifier output is blocked from the 1V Buffer by the open contacts 10/11 of RL16. Instead, it is connected by RL6-6/4 as input to M14.

For the 10V and 100V ranges, M14 is connected as an inverting ÷2 line buffer by the un-energized relay RL6-6/4 and 11/13. For the 10V range, M14 output passes to the Power Amplifier assembly via J5-73 and the Mother assembly.

7.6.3 10V BUFFER (Power Amplifier Assembly)

(Circuit Diagram 430618 pages 11.9-1 and 11.9-2)

The discrete, complementary, 10V Range buffer-amplifier is a dual-purpose circuit, generating power to the output terminals for both DC and AC functions.

As it provides the full output current, it is located on the Power Amplifier assembly so that the heat from its power stage can be developed outside the thermally-shielding Chassis assembly, and dissipated by forced-air cooling from the fan. Its output is fed back to the DC or AC assembly for range and output switching, as the 'DC10V+100V' signal.

The output from the line buffer M14 on the DC assembly (the signal 'DC 10V+100V+1kV ERROR') enters the PA assembly at J9-40, passing to the input of the 10V Power Amplifier via DC/AC selector relay RL4-11/13 and 10V selector RL3-9/13. The signal is attenuated by R171 and R124 in a ratio of 4.17:1. So a positive full range DC Ref signal of +10V from the Reference Divider appears at J9-40 as -5V, and is further attenuated by R171/R124 to approximately -1.2V across R124, which refers it to Common-2B. The amplifier is best regarded as having separate DC and AC paths.

7.6.3.1 DC Path

The DC path is blocked by C56; M17 is the DC input buffer, connected as an integrator with diode clamping. M19 operates as an inverter in open loop, so applies high DC gain to the output from M17 on M19-2, referred to Common-2C by R112.

The output from M19 drives both halves of the symmetrical, inverting, discrete power amplifier through current-limiters Q21 and Q24, and is buffered by emitter-followers Q22 and Q23. Common-emitter devices Q27 and Q29 form a voltage amplifier, driving the complementary output stage Q32 and Q33. Resistors R119 and R120 set the gain of the discrete stages to approx. 4.5.

The forward amplification contains three inversions, negative DC feedback being applied to M17 inverting input by R122, defining an overall gain of 10 in conjunction with input resistor R123.

For DC range selections, the DC error signal is applied at M17-2, is amplified by 10 and output at TP11 via the low DC resistance of L8. The forward voltage gain, from the output of the Error Amplifier to the output of the 10V Buffer, is thus of the order of 1.2. This is more than sufficient to support the specified output current, when corrected to the demanded output voltage by the sense feedback to the Error Amplifier.

In AC operation, the effect of the DC path is to sense and correct the DC offsets throughout the whole AC amplifier, referring the output to Common-2A at M17-3.

7.6.3.2 AC Path

The AC path is blocked by the integrator M17, but is applied to the non-inverting input of M19 through the coupling capacitor C56. M19 operates in open loop, applying its output to the discrete power amplifier (see *para 7.6.3.1* above).

The amplifier AC gain is also set to 10 by R122 and R123, the circuit time constants being selected to allow overall instrument output operation over the full frequency range of 10Hz to 1MHz.

7.6.3.3 Overload Detection

The $\overline{\text{10V FLAG}}$ line, connected to D71 cathode, is pulled up to 0V (in-guard logic-1) by 7.2kΩ (*See page 11.9-5* - R154 in parallel with R38). An Error OL message results from this line being driven to logic-Ø by Q34. During DC operation, relay RL8 is un-energized, configuring the collector loads of emitter-followers Q32 and Q33 as low-pass filters. This de-sensitizes the overload detector and the overload limiters Q28 and Q30 from the effects of transient currents.

Overload detector Q31 reaches Vbe threshold when the DC current value in R139 and R141 exceeds approximately 35mA. Similarly, Q34 detects currents in R147 and R149. In either case, Q34 conducts, pulling diode D71 cathode down to -15.7V. This drives the $\overline{\text{10V FLAG}}$ line to logic-Ø, so the status message is returned to the CPU via the SSDA serial interface, and the 'Error OL' message is displayed.

This does not preclude further increase in output current, but under these conditions the instrument accuracy specification is not guaranteed.

During AC operation, relay RL8 is energized, the filter is removed, and the Overload Detector is adjusted to operate as a peak current detector. R172/R141 and R173/R147 cause the $\overline{\text{10V FLAG}}$ to activate for RMS values of output sinewave current in excess of approximately 80mA.

7.6.3.4 Overload Limiting

If the DC output current increases to approximately 39mA, the current in either R139 or R149 causes the Vbe threshold of Q28 or Q30 to be exceeded, shunting the base current of the corresponding voltage amplifier. Thus the output drive to the final stage is limited.

In AC operation, if the RMS output current increases to approximately 100mA, the peaks of current cause the Vbe threshold of Q28 or Q30 to be exceeded. The output drive to the final stage is limited at this level.

7.6.3.5 Output Protection

The output current passes through the combination of R144 and L8. At DC and low frequency AC, the inductor provides a low output impedance, whereas at high frequencies the resistor stabilizes the amplifier when driving capacitive loads.

7.6.3.6 10V Buffer Output

For DC and AC 10V ranges, relay RL3 is energized.

For DC, RL4 is un-energized, so the 10V Buffer output passes via RL3-8/4 and RL4-4/6 as the 'DC 10V+100V' signal, J19-19/20 to the Mother assembly, and thence to the DC assembly.

For AC, RL4 is energized, diverting the 10V Buffer output via RL4-4/8 as the 'AC 10V+100V' signal, and out at J19-15/16 via the Mother assembly to the AC assembly.

7.6.3.7 10V Amplifier Power Supplies

M17 and M19 are supplied from ±15V Common-2A rails, but the discrete amplifier receives power from the ±38V supply, which is also used for the Error Amplifier on the DC assembly.

7.6.4 RANGE SWITCHING (DC Assembly)

(Circuit Diagram 430536 Page 11.5-1)

The DC 10V+100V signal enters the DC assembly from the Mother assembly at J5-37/38, and R73/L6 filter out any spikes picked up in transit. Relay RL4 is energized, shorting the high voltage resistor R67, so the signal goes directly through the 1Amp fuse F1 to the 1V+10V+100V star-point.

7.6.5 REMAINDER OF THE 10V LOOP

From this point, the 10V range loop follows the same path as the 1V loop, both outwards to the I+ and I- terminals and back to the Error Amplifier inverting (sense) input. Of course, on the 10V range, the returning sense signal is compared with the full DC Ref voltage, rather than the attenuated DC Ref for the 1V range. *(Refer to sub-section 7.3; from para. 7.3.6 onwards).*

7.7 DC HIGH VOLTAGE LOOPS

The instrument includes two high voltage DC ranges. The 100V ranges extends from -200V to +200V full scale, the 1000V range from -1100V to +1100V full scale.

The simplified block diagram of *Fig. 7.2* illustrates the high voltage DC circuit arrangement and signal flow. Details of the 100V and 1000V ranges are described in *Sub-sects. 7.8 and 7.9*.

7.7.1 HIGH VOLTAGE DELIVERY

Both ranges employ the same referencing arrangement used for the 10V DC Range, but the techniques necessary to generate high voltages differ from those in the low voltage loops:

- For the 100V Range, a VMOS circuit amplifies the ±20V Reference directly, as a DC signal, powered from a separate ±400V supply. The 100V range voltages are passed back via the range switching circuitry in the DC assembly to be output from the instrument as for the low voltage ranges.
- For the 1000V Range, the DC reference is first converted to a 16kHz AC signal, amplified in the same 100V amplifier, then stepped up to 1000V range voltages through a separate transformer. Subsequent high voltage rectification, filtering and polarity-switching converts the AC output from the transformer secondary into a DC voltage. A separate line conveys the 1kV range voltage back to the DC assembly for range switching and output from the instrument.

7.7.2 HIGH VOLTAGE SENSING

A guarded high-voltage switched precision attenuator reduces the DC sense voltage from the Hi and Lo terminals to Reference levels. The attenuated sense voltage is compared with the DC Ref voltage, their difference being used as an error signal to correct the range output level.

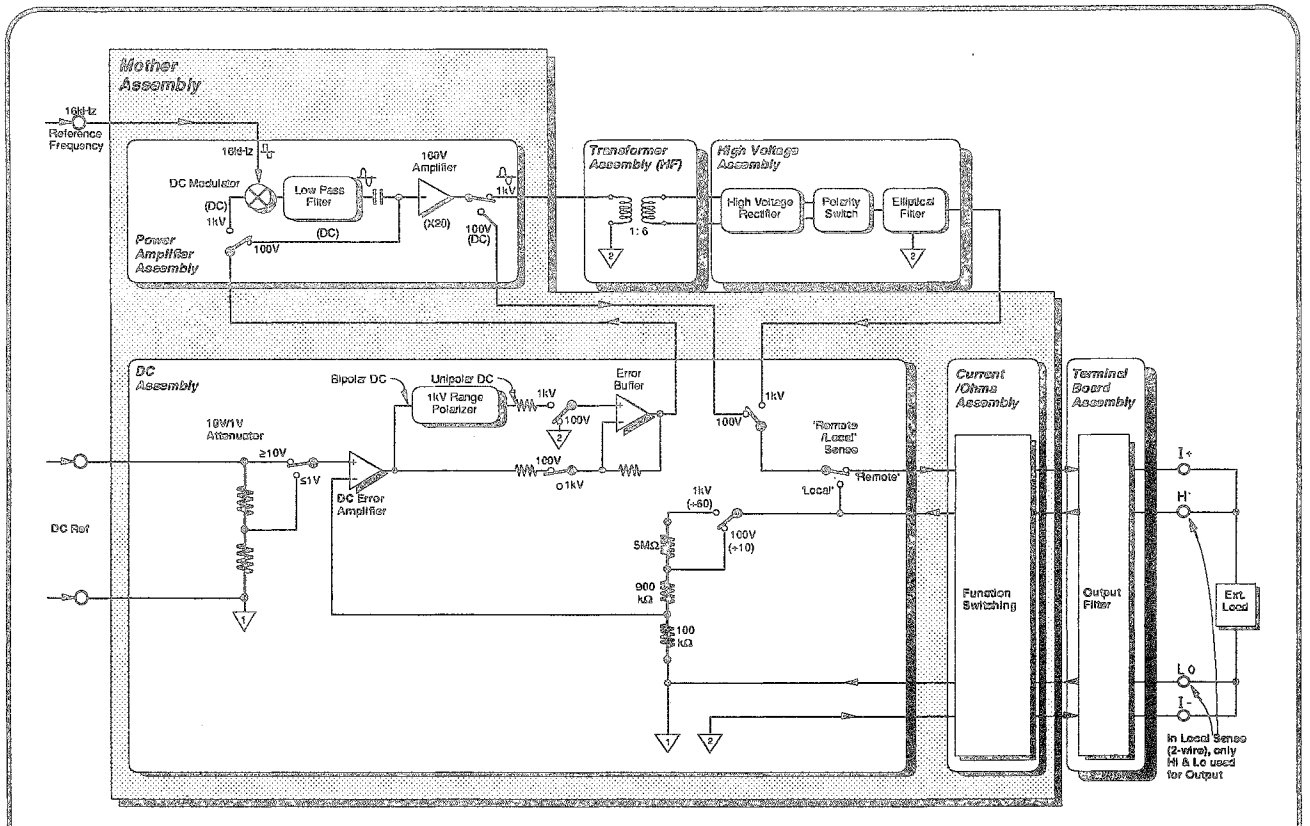

FIG. 7.2 DC HIGH VOLTAGE LOOP - SIMPLIFIED BLOCK DIAGRAM AND ROUTING

7.8 100V RANGE

7.8.1 INTRODUCTION

The '10V+100V+1000V DC ERROR' signal, generated by the ÷2 DC Error Buffer in the DC assembly, enters the Power Amplifier as for the 10VDC range; but the 10V Amplifier is bypassed for the high voltage ranges.

On the 100V range, the signal is switched directly into the 100V Amplifier, where it is scaled up by a factor of -20, the amplifier output being delivered via the 'DC 10V+100V' line to the PHI(DCV) line on the DC assembly. Thereafter the output is transferred to the instrument terminals as for the 10V range.

7.8.2 100V RANGE POWER ROUTING

7.8.2.1 DC Reference and Error Amplifier

(Circuit diagram 430536 Page 11.5-1)

The DC Ref signal is derived as for the 1V range, entering the DC assembly at the same pins: J5 pins 1, 2, 3 and 4. Relay RL18 again connects the power and sense lines to the two star-points TP2 and TP3, the latter being the signal Common-1 point.

On the 100V range, RL16-8/9 connects the full DC Reference to the non-inverting input of the Error Amplifier, which operates as for the 1V range, except that the span of voltages is now the full -20V to +20V.

7.8.2.2 DC ÷2 Error Buffer M14

The Error Amplifier output is blocked from the 1V Buffer by the open contacts 10/11 of RL16. Instead, it is connected by RL6-6/4 as input to M14.

For the 10V and 100V ranges, M14 is connected as an inverting ÷2 line buffer by the un-energized relay RL6-6/4 and 11/13. For the 100V range, M14 output passes to the Power Amplifier assembly via J5-73 and the Mother assembly.

7.8.2.3 Power Amplifier and Output Routing

(Circuit Diagram 430618 page 11.9-2 and 11.9-3; and Circuit Diagram 430536 page 11.5-1)

'DC Error' enters the Power Amplifier assembly at J9-40 (refer to page 11.9-2). Relay RL3 is un-energized, shorting the 10V Amplifier input; and RL4 is un-energized, routing the DC Error signal to the 100V Amplifier as signal '100V I/P' *(page 11.9-3)*.

Energized relay contacts RL2-8/4 apply the signal to the Gain Stage, which provides drive to the power amplifiers in the positive and negative heat sinks, via J3-12 and J3-11. The single-ended output from the heatsinks at J3-9 passes via R89, L7 and relay RL2-13/9 (RL2 energized), to RL3-6 *(page 11.9-2)*, and onto the 'DC 10V+100V' line via RL4-4/6, R174 and J9-19/20.

On the DC assembly *(page 11.5-1)*, the signal is routed to the PHI(DCV) line as for the 10V range.

7.8.3 100V AMPLIFIER

(Circuit Diagram 430618 page 11.9-3)

The 100V amplifier is in three stages:

- Gain Stage: this is similar to the first stage of the 10V amplifier, but with a different distribution of gain.
- Driver Stage: providing most of the gain, this stage runs from a regulated 400V supply.
- **Buffer Output Stage:** complementary MOSFET circuits, located on the positive and negative heatsinks, provide a single-ended output with the required voltage swing, at low impedance.

  The voltage gain for the whole 100V amplifier is set at 100 by the input resistors R74/R71 and the feedback resistor R88.

The 100V amplifier is also used for 100V AC outputs, and on the DC and AC 1000V ranges to drive the step-up transformer. For this reason the following description is applicable to both DC and AC signal processing, and will be referred to in the sub-sections dealing with those functions and ranges.

7.8.3.1 Input to Gain and Driver Stages

(Circuit Diagram 430618 pages 11.9-2 and 11.9-3)

The DC ERROR signal enters the PA assembly at J9-40, passing to the input of the 100V Power Amplifier via relays RL4-11/13 and RL2-8/4. It is referred to common 2B by developing a voltage across R72.

7.8.3.2 DC Offset Correction

M10 is the DC offset integrator, with diode clamping. It provides a DC input to the non-inverting input of the voltage gain amplifier M8, controlling its DC offset. This is similar to the arrangement in the 10V Amplifier.

7.8.3.3 Signal Processing

M8 is a high speed hybrid amplifier operating as an inverter. With link LKD normally made, its stage gain is approximately 2.5, frequency compensated by C18 and C72. It operates from the 15V Common-2B supplies, but its signal output is converted into a current by Q10 and Q8; allowing its mean DC voltage for AC signals to reach the -400V levels required to operate the driver MOSFET output circuit. Diodes D44, D43 and D36 prevent negative latch-up.

Voltage Regulator M21 sets its pin 1 to +12V. Common-emitter buffer Q10 drives the capacitance of Q8 source-gate from the output of M8, forming a cascode current generator. The drain of p-channel MOSFET Q8 passes the signal current to the mirror Q12/Q11 at voltages close to the negative 400V rail.

The current-mirror output transistor Q11 is also in cascode with its associated MOSFET Q9. Emitter resistor R53 defines the current in Q9, the ratio R52/R53 setting the mirror's current gain.

MOSFETs are inherently capacitive, so measures are taken to nullify the effects, on slew rate, of the capacitive currents between Q9 electrodes. The cascode arrangement ensures that any source-gate and source-drain capacitive currents join the main flow of source current and have little effect on slew rate.

The Miller feedback of the drain-gate capacitance has the greatest effect on slew rate, generating AC currents between anti-phase electrodes which normally pass into the input circuit. In this arrangement, Q13 diverts these currents back into the cascode current, while maintaining a standing bias of about 4 volts between gate and source. These measures minimize the reduction of Q9 operating bandwidth.

R51 and D42 provide Q13 operating bias, and D51 protects the bias circuit. The high-power resistor R49 refers the bias circuit to Common-2, and C26 stabilizes the base-emitter bias of Q13. Zener diode D39 protects the MOSFET from source-gate voltage breakdown.

7.8.3.4 Driver Regulator

At Full Scale on the 100V AC range, the output from the driver is 200V RMS. This requires Q9 drain to provide a peak-to-peak voltage swing approaching 600 Volts, as there is no voltage gain in the heatsink power amplifiers. The positive supply which provides Q9 current therefore needs special regulation.

The ±400 volt supply is at this point unregulated, so can contain line ripple and level variations, this noise level being critical to the output performance. To define a stable supply voltage, a DC restoration circuit is employed as a trough detector, maintaining a level about 5V below the most negative excursions of the ripple.

At power-up, 75V zener D57 allows a rapid charge of reservoir capacitors C49 and C59, until the charge reduces D57 voltage below the avalanche level. When D57 cuts-off, R100 provides a charge path of 1MΩ, giving a time constant of approximately 10 seconds. The smoothed voltage across C49/C59 is divided by R101, R86 and R87; so a small voltage is dropped across R101, and Q20 gate is held about 5V below the +400V(2)B line voltage. The N-channel source-follower Q20 thus provides a quiet, low-impedance DC supply voltage.

Zener diodes D60 and D61 divide the voltage across C49 and C59, so that their breakdown voltages are not exceeded. The 10V zener D54 protects the TMOS gate/source from excessive voltages.

The opto-coupler M16 permits the 400V supply to be switched off, allowing D56 to assume forward bias, thus connecting the rail to the +38V supply. This facility is made available to reduce the voltage across R65, and hence its continuous power loading, when the instrument is delivering a DC output of negative polarity. M16 is turned off for AC and positive DC outputs, by the 'POSITIVE' signal from the processor being set to logic-1 (0V). Thus M16-6 is isolated from M16-5, and the +400V rail out of the regulator remains energized. For negative DC outputs, the cathode of the LED in M16 is pulled to logic-Ø (the POSITIVE signal being set to -15V on M16-3 - see *page 11.9-5*); the LED emits, and M16-6/5 shorts out D54 turning Q20 off. The total supply voltage for negative outputs is then limited to 438V.

At HF, inductor L6 appears as a current source, increasing the impedance of Q9 drain load with frequency to compensate for capacitive loading. It has the advantage of not increasing the net power dissipated in the stage; any active current source would have significant output capacitance. The 12-watt resistor R65 is the main resistive drain load for Q9.

7.8.3.5 Driver Output

The driver develops its output voltage, which can involve peak-to-peak AC swings of up to 600V, across the load resistor R65. Zener diode D41 is included to clamp the output in the event of the heatsinks being disconnected. This is normally held below avalanche by the current passing through a series bias buffer (Q8) in the Positive Heatsink assembly, via J3-11 and J3-12.

The main frequency compensation is performed by C12. This could have been connected to the drain of Q9, but the output line slew rate is sensitive to capacitive loading. Instead it is connected via J2-7, to a low impedance point in the Negative Heatsink assembly which follows the driver output voltage swing.

7.8.4 100V POWER AMPLIFIER

(Circuit Diagrams 430637 page 11.13-1 and Circuit Diagram 430539 page 11.13-2)

The 100V power amplifier stage is split between the Positive and Negative Heatsink assemblies. The driver output voltage is connected into the Positive assembly, and the frequency compensation feedback is derived in the Negative assembly.

The whole circuit is a complementary, single-ended push-pull amplifier with unity voltage gain. To achieve the full 300V peak voltage output, two MOSFET source-followers are connected in cascode, for each polarity, in a totempole arrangement.

To obtain the required peak current levels, each source-follower consists of two MOSFETs in parallel. In all, therefore, eight MOSFET devices are used.

On 100V ranges, the output currents are such as to bias the amplifier in class A, but on 1000V ranges the output currents impose class AB conditons. Crossover distortion is minimized by a regulated bias, generated by a Vgs multiplier (M1 in the Positive Heatsink assembly).

Power for the amplifier is provided by the same ±400V supply that serves the driver circuit. To minimize internal temperature by improving efficiency, overall power loss is reduced by regulation only where required. Thus only the driver stage is regulated, allowing the power amplifier to take power directly from the unregulated supply. Being source-followers, the ripple on their 400V rail is not transmitted.

7.8.4.1 Positive Heatsink Assembly

(Circuit Diagram 430637 Page 11.13-1)

N-channel MOSFETs Q1 and Q2 are connected in parallel, as are Q3 and Q4. All devices are matched for power dissipation and threshold voltage for an even dissipation of approximately 400W between the two heatsinks. All gate-source potentials are limited by 10V zeners.

The input voltage from the driver is present at J3-11 and J3-12. Most of the driver load current passes through the bias buffer Q8, and the voltage developed across Q8/R21 is applied to the bias control R10. The Vgs multiplier M1/Q8 acts as a high gain shunt regulator, generating a bias of between 5V and 9V, set by R10. The regulator's own bias chain of Q9, D8, and Q5 (which is connected as a diode) responds to the temperature of the heatsink to compensate for the temperature coefficients of the MOSFETs.

The 'DRIVE-' voltage at J3-11 is transferred directly to the negative heatsink input via J1-7 (*Circuit Diagram 430539 page 11.13-2*).

The 'DRIVE+' voltage at J3-12 is buffered by Q7 and applied to the gates of Q3 and Q4. In the event of an output short-circuit, Q6 detects the output current as a voltage across R14, imposing a hard limit of 1.5A by reducing the signal voltage at the input to the MOSFET gates.

The series gate resistors R5 and R6, together with their associated drain-gate capacitances, form the dominant pole of the amplifier. Damping resistor R19 with ferrite bead FB1, prevent local oscillations in emitter-follower Q7.

Q1 and Q2 act as buffers to provide a bootstrapped supply for the output devices Q3 and Q4, splitting the overall power dissipation to four points of application to the heatsink. The gates of Q1 and Q2 receive their drive from the output line, obtained via the divider R16/R22/R23/R15. Capacitors C10 and C13 decouple any noise on the 400V rail; C11 and C12 correct any lag which may be generated by C10 and C13. C5 and C6 control the division ratio at HF, swamping any stray capacitance.

The drains of Q3 and Q4 are shorted together, and connected via J1-5 by a 10nF capacitor to the corresponding point in the Negative Heatsink, completing an AC bootstrap (BS). The gates of Q3/Q4 (J1-1) and Q1/Q2 (J1-4) are similarly linked to their corresponding points in the negative heatsink. This ensures that AC swings in both polarities are identical.

The combined output from the Positive and Negative Heatsinks is transmitted back to the Power Amplifier assembly via the screen of the input connection.

7.8.4.2 Negative Heatsink Assembly

(Circuit Diagram 430539 Page 11.13-2)

This is virtually a mirror image of the Positive Heatsink circuit. However, because the P-channel MOSFETs are operating closer to their maximum voltage rating, they are further protected by Zener diodes which limit their drain-gate potentials.

The HF swamp capacitors are not required, as the whole circuit is AC-bootstrapped to corresponding points in the Positive Heatsink assembly, via C1, C2 and C4.

HF compensation for the driver and output stages is derived at low impedance from the junction of R2 and D12. It feeds back via J2-7 to the driver output circuit, through C12 in the Power Amplifier assembly, to avoid capacitively loading the driver output line.

7.8.4.3 Over-Temperature Detection

The two NTC thermistors in each heatsink circuit are part of a bridge network which detects excessive temperatures on the heatsinks. The action of the bridge is described in *Section 7.12.9*.

7.8.4.4 100V Output Connection

DANGER!
FOR GUARDING PURPOSES, THE OUTPUT FROM THE HEATSINKS IS TRANSMITTED BACK TO J3-9 OF THE POWER AMPLIFIER ASSEMBLY ALONG THE SCREEN OF THE INPUT CABLE. THE VOLTAGES ON THIS SCREEN ARE POTENTIALLY LETHAL. UTMOST CAUTION SHOULD BE EXERCISED WHEN WORKING IN THEIR VICINITY.

7.8.4.5 Heatsink Removal

The 100V Amplifier can work with the heatsinks removed, because of the clamp diode (D41 on *page 11.9-3*) in series with the driver load. If they are removed, however, J3-9 and J3-11 in the disconnected socket of J3 must be connected together, to maintain the feedback. In this condition, the gain falls due to loading of the driver by resistors in the DC or AC assembly.

7.8.5 POWER SUPPLIES AND PROTECTION

Three main power supplies are employed in the Power Amplifier:

- ±15V Common-2 in-guard supply.
  This is used for all low voltage applications, including the switching and functional logic. For the most part the logic conforms to the standard: logic-Ø = -15V; logic-1 = 0V.
- ±38V Common-2 supply.
  Required mainly for the 10V Power Amplifier, but also for negative DC outputs in the 100V Amplifier driver, this supply is generated on the separate 38V Power Supply assembly *(Circuit Diagram 430653 page 11.12-1)*. Part of the supply circuit is situated on the Mother Assembly.
- ±400V Power Supply.
  The 100V Power Amplifier used for the 100V and 1000V ranges, for both DC and AC outputs. The line transformer secondary output is rectified and smoothed on the Mother assembly, and the main regulator circuitry for the driver stage is contained on the Power Supply / Current Heatsink. The power output stage of the 100V Amplifier receives unregulated 400V supply. Extensive protection is incorporated.

7.8.5.1 ±38V Supply

(Circuit Diagram 430653 Page 11.12-1)

The line (mains) transformer secondary centre tap is referred to Common-2 on the Mother assembly after passing through the ±38V Power Supply assembly. This secondary also provides an AC output for the 'Common Mode Null' balancing circuit.

A single bridge rectifier on the Mother assembly provides both positive and negative raw supplies for the foldback regulator in the ±38V Power Supply assembly. The ±38V supply circuit is described in *Section 6.7, para 6.7.3.4.*

7.8.5.2 ±400V Transformation/ Rectification

(Circuit Diagram 430604 Page 11.16-5)

The mains (line) transformer secondary centre tap is referred to Common-2 on the Mother assembly. The secondary is switched with the secondary for the 38V supply, to allow a lower voltage to drive the 100V power amplifier for servicing purposes. Under operational conditions in the 4708, this switch, which is situated prominently on the Mains Transformer assembly, is set to the 400V position.

A single bridge rectifier on the Mother assembly uses series diodes to achieve the high peak inverse voltage performance required for the 400V supply.

After smoothing, and part-loading by a bleeder resistor chain (the bleeder resistors also balance the voltages across the capacitors); the rectifier output is passed via J31, to provide both positive and negative raw supplies for the foldback regulator in the PS/I Heatsink assembly.

7.8.5.3 400V Current Control

(Circuit Diagram 430540 Page 11.13-3)

When the 400V supply is enabled, the LEDs in opto-isolators M1 and M2 are conducting, allowing their opto-transistors to be energized. As the circuits for both polarities are otherwise symmetrical, only the positive circuit is described.

Zener Diode D8 protects the source-gate circuit of level-shifter Q3. This N-channel MOSFET supplies a current of 1.4mA, as defined by Q8, to the current-monitor reference zener diode D7. This current is available only if the 400V supply is enabled by M1, otherwise Q4 base is pulled down by D1/R9, Q4 conducting via D7 so Q9 is pinched off.

Under normal operating conditions the Power Amplifier supply current is drawn through the P-channel MOSFET Q9, which is held in conduction by R8, R12 and D2. The current is sensed by the parallel combination of resistors R17 and R32. Although the peaks of the current taken by the power amplifier can reach 1.4A, the mean value is less than 0.5A. Ripple currents making up the difference are smoothed by the main reservoir capacitors C31 and C22 on the Power Amplifier assembly *(page 11.9-3)*.

For mean currents more than approximately 0.5A (in particular for output short-circuits); the voltage sensed across R17/R32, subsequently divided by the attenuator R10/R9, exceeds the threshold of Q4/D7. Q4 conducts to pass current into R8, reducing the drive to Q9 gate, so the +400V(2)B voltage at D5 anode falls. When the voltage dropped by Q9 rises to 56V, zener D5 conducts and pulls Q4 base down, further reducing the drive to Q9 gate. This cumulative action is slowed only by the time constant of the combination R34/C15, so that both voltage and current on the +400V(2)B line are simultaneously closed down.

With a persistent 400V overload, the circuit cannot recover naturally from this 'foldback' mode. However, the 400V voltage is monitored. If the 400V monitor senses a failure, a status bit is passed back to the CPU via the SSDA serial link. The CPU makes three attempts to reinstate correct operation by removing the PA bias while restarting the supply via the 400V enable line. If after the third attempt the voltage does not recover, the CPU assumes that a hardware fault is present, so displays the 'FAIL 7' message.

7.8.5.4 100V Current Sense and 1kV Overvolts Detector

(Circuit Diagram 430618 Page 11.9-6)

This detector circuitry is used only for AC High Voltage ranges, and is described with the AC Voltage Amplitude Control system in *Section 9*. However, as the 400V supplies pass through the circuit for DC high voltage ranges, it is mentioned at this point.

The 400V(2)B lines enter the Power Amplifier assembly from the PS/I Heatsink at J1-8/6 and are filtered by L1 and L2 before being applied across two neon lamps LP1 and LP3. These lamps are visible from the top and rear of the instrument when the PA board is exposed, indicating that a dangerous voltage is present.

The 400V(2)B lines pass on to power the driver stage of the 100V amplifier, where the voltage is regulated as described in *sect. 7.8.3.4*. The 400V(2)C lines supply the power amplifier in the Positive and Negative Heatsinks.

On the AC 100V range, the current in each of these lines is used as an analog of the load placed on the amplifier. (On the 1000V ranges, any overload is sensed by an AC or DC overcurrent detector in the DC assembly.) On the AC 1000V Range, the voltage applied to the primary of the step-up transformer is fed via a resistor to the detector at M2-5/9. The '100V AC' line is set to logic-Ø (-15V) only when the 100V AC range is selected.

7.8.6 POWER AMPLIFIER POWER SUPPLY MONITORS

(Circuit Diagram 430618 Page 11.9-4)

All three power supply voltages: ±15V, ±38V, and ±400V; are monitored using similar comparators to initiate individual 'FAIL' messages. In addition, if either the ±400V or the ±15V monitor circuit detects a low power supply voltage, the ±400V supply is disabled.

7.8.6.1 Comparator Supply Protection

To ensure that failure of either the ±15V or the ±38V supply does not remove the power from the three comparators, these two sources are 'OR'ed by D5, D6, D15 and D16 (the ±38V supply being ballasted by R1 and R15) to provide the V+ and V- supply to the Quad op-amp M3. In nine of the possible sixteen states of failure of these two supplies, power will still be applied to the comparators. The maximum values of V+ and V- are limited to +16V and -16V by zener diodes D7 and D14.

7.8.6.2 ±15V Monitor

Zener diode D29 is the 2.45V reference for the ±15V comparator. It is ballasted by R27 to V+, and its +2.45V above the -15V rail is applied to the non-inverting input of M3c. The +15V to -15V supply is divided by R29/R30/R33, generating a voltage +2.50V above the -15V rail at the inverting input to M3c under normal operating conditions. Thus the output at M3c-7 remains at the negative (V-) rail, holding D28 in forward bias, and the 15V(2) FAIL line at J9-108 is held at Logic-Ø (-15V).

If the voltage between the ±15V supply rails falls to less than 29.4V, the voltage across R30/R33 falls to less than the reference 2.45V. The output at M3c-7 changes state to the V+ rail, reverse-biassing D28, so the 15V(2) FAIL line is pulled to logic-1 (0V) by R28.

The logic levels on the 15V(2) FAIL line pass via the Mother assembly to the Parallel/Serial status registers in the Reference Divider assembly (M18-5 on *page 11.4-4*). During each control data transfer, the SSDA also passes the condition of the status registers back across guard to be read by the CPU. When the 15V(2) FAIL line switches to logic-1 due to a ±15V failure, this is detected by the CPU which produces the FAIL 9 message on the MODE display.

The ±15V monitor output line also gives an input to the 400V enable logic *(Section 7.12.5)*. The effect of a ±15V failure is to disable the 400V(2)B regulated supply via D26 conduction and J1-3 at logic-1.

7.8.6.3 ±38V Monitor

The action is similar to the ±15V monitor, but because of the higher voltage, the divider between the +38V and -38V lines is balanced by two 10kΩ droppers in each line. Without Q5, the 2.45V zener bias current would affect the sensing level. By employing Q5 as a voltage follower, D25 bias current can pass directly to the V- rail and still be referred to the R25/R26 junction. The Vbe drops in Q5 cancel one another out, so the zener and the sensor R25/R32 are referred to the same potential.

In normal operation the voltage across the 715Ω of R25/R32 is approximately 2.62V, in excess of the 2.45V of D25.

If the 76V between the +38V and -38V rails falls below 71V, the voltage at M3b-2 falls below that at M3b-3, and the output at M3b-1 changes state from -V to +V. The action of D22 and the 38V(2) FAIL line are the same as for the ±15V monitor.

7.8.6.4 ±400V Monitor

The ±400V Monitor is in two mirrored halves, each dealing with its own polarity of the supply, so only the positive half is described.

Zener D9 provides the +2.45V reference on the non-inverting input at M3d-12. The divided +400V is sensed across R16 at a normal operating voltage of +3.27V (referred to common-2C) and applied to the inverting input at M3d-13, thus setting the output at M3d-14 to the -V rail voltage. D20 is reverse-biassed so the 400V(2) FAIL voltage is pulled to logic-Ø (-15V) by R7.

If the +400V supply fails by falling below +300V, the voltage across R16 falls below the +2.45V reference and the M3d-14 output switches to the +V rail voltage. D20 conducts, pulling the 400V(2) FAIL line at J9-106 to logic-1.

In normal 400V operation R31 is shorted by the 400V/50V switch on the Mains (line) transformer, via the 'Lo SUPPLY A' and 'Lo SUPPLY B' lines. When the switch is set to 50V, the Lo SUPPLY A line is connected to -15V, effectively disabling the monitor output by holding the 400V(2) FAIL line at logic-Ø.

The output line gives an input via D3 to the 400V enable logic (described in *Sub-section 7.12.5*). Its effect is as for a ±15V failure.

7.9 1000V RANGE

7.9.1 INTRODUCTION

7.9.1.1 Power Signal Processing

Method

The 1000V DC Range obtains its high voltages by using the 100V power amplifier to drive an AC signal into the primary of a step-up transformer. The AC signal is derived by modulating a 16kHz reference with the DC ERROR signal.

Error Signal Conditioning

The '10V+100V+1000V DC ERROR' signal is pre-conditioned by the VCA Drive circuitry in the DC assembly, before it enters the Power Amplifier. The 10V Amplifier is bypassed.

High AC Voltage Generation

The modulated 16kHz signal is passed from the DC modulator into the 100V Amplifier, where it is scaled up by a factor of -100, the amplifier output being delivered via the 'OUTPUT' line to the HF Transformer assembly.

Rectification and Output

The stepped-up secondary voltage is rectified and filtered in the High Voltage assembly:

- A constant-current source acts as a shunt to sustain the current drawn from the high-voltage secondary winding through the bridge rectifier. Polarity is switched with respect to common-2 via the LC-filtered ±38V common-2 supplies. Positive polarity output is referred to -38V at zero output, to overlap with negative polarity output referred to +38V. The overlap allows digital calibration constants to be used to align zero voltage output in both polarities to the same calibrated zero.
- The main output filter is placed in the output line. This is a low-pass filter with a high rejection at 16kHz, reducing the ripple voltage to within specification limits.
- The output voltage is fed out through the Range switch on the DC assembly, where it is subject to Remote Sense and Output On/Off switching, before being passed to the I+ terminal by the same route as for low voltage ranges. High voltage status is detected on the DC assembly as described in *para 7.3.7.2* for the 1V Range.
- The external current is sunk into common-2 via the overcurrent detector, which warns the control processor when the output current exceeds approximately 28.5mA *(see para 7.3.7.1)*. On the 1000V range the processor will switch the output off on receipt of the overcurrent signal from the overcurrent detector.

7.9.1.2 Sense Loop

Sense Attenuation

The sensed output voltage from the Hi and Lo terminals is reduced down to 'DC Ref' levels by a guarded precision attenuator on the DC assembly, and then applied to the inverting input of the Error Amplifier:

- The Lo terminal and Sense Attenuator Lo are both referred to Common-1 (DC Ref Lo). The attenuator is dual-purpose, being used for both 100V and 1000V ranges. The Hi sense voltage is divided in the Sense Attenuators by 10 (100V Range) or 60 (1000V Range).
- The attenuated output is compared against DC Ref Hi in the Error Amplifier, modifying its output to the VCA Drive.
- The 10V Bootstrap, in addition to supplying the Error Amplifier, also buffers DC Ref Hi as reference for the VCA Drive circuit.

Error Conditioning

The bipolar DC error voltage between the buffered DC Ref Hi and the Error Amplifier output is converted by a switched precision rectifier in the 'VCA Drive', to provide a suitable unipolar control signal for the DC modulator. The buffered output from the rectifier becomes the '10V+100V+1000V DC ERROR' signal which adjusts the amplitude of the 1000V Range outputs.

Loop Action and Reference Scaling

The Sense loop thus stabilizes the 1000V Range DC output to a value which is 60 times the DC Ref voltage, this value being determined by the division ratio of the precision sense attenuator. The DC Ref voltage is scaled digitally so that Full Scale of 20V corresponds to 1100V on the OUTPUT display and at the output terminals.

7.9.2 1000V RANGE POWER ROUTING

7.9.2.1 DC Reference and Error Amplifier

(Circuit diagram 430536 Page 11.5-1)

The DC Ref signal is derived as for the 1V range, entering the DC assembly at the same pins: J5 pins 1, 2, 3 and 4. Relay RL18 again connects the power and sense lines to the two star-points TP2 and TP3, the latter being the signal Common-1 point.

On the 1000V range, RL16-8/9 connects the full DC Reference to the non-inverting input of the Error Amplifier, which operates as for the 1V range, except that the span of voltages is now the full -20V to +20V.

The Error Amplifier output is blocked from the 1V Buffer by the open contacts 10/11 of RL16. Instead, it passes as input to M15-5. The error signal is conditioned by the VCA Drive circuit M15/M14 and passed to the line buffer at M14-5. For the 1000V range, M14 is connected as a non-inverting line buffer by contacts 8/4 and 9/13 of energized relay RL6. M14-7 output passes to the Power Amplifier assembly via J5-73 and the Mother assembly.

7.9.2.2 Power Amplifier Routing

(Circuit Diagrams: 430618 pages 11.9-2 and 11.9-3)

'DC Error' enters the Power Amplifier assembly at J9-40 *(refer to page 11.9-2)*. Relay RL3-9/11/13 remains un-energized, shorting across the 10V Amplifier input. The DC Error signal is routed via link LK.W and TP14 to the 1kV DC Modulator at R78. The route to the 100V Amplifier input as signal '100V I/P' via RL4-11/13 is blocked by the open contacts 8/4 of unenergized relay RL2 *(page 11.9-3)*.

The output from the modulator is a 16kHz AC signal at TP15 whose amplitude is determined by the value of the DC Error signal. With RL1 unenergized on the 1kV DC Range, this AC signal passes via RL1-11/13 contacts to the '1kV ERROR O/P' line.

Contacts RL2-6/4 *(page 11.9-3)* apply the signal to the Gain Stage, which provides drive to the power amplifiers in the positive and negative heat sinks, via J3-12 and J3-11. The single-ended output from the heatsinks at J3-9 passes via the OUTPUT line to the 1kV ENABLE relay contacts RL6-8/9 *(page 11.9-2)*. RL6 is energized, and RL7 is unenergized on the DC 1kV Range, so the OUTPUT line is connected to J5-3 (PA assembly) and out as a direct link to the High Frequency Transformer assembly.

7.9.2.3 High Voltage Assembly - Routing

(Circuit Diagram 430537 page 11.14-1)

The high voltage output from the secondary of the HF transformer is input to the High Voltage assembly between J2-1/2 and J2-8/9. After rectification, polarity switching and filtering, the DC 1kV signal is output via J1-2/3 to pin L on the Mother assembly, where it is again filtered before passing to the DC assembly on J5-33/34.

7.9.2.4 DC Assembly - Power and Sense Routing

(Circuit Diagram 430536 page 11.5-1)

On the DC assembly, the DC 1kV signal line is fused at 1A by F5, and the signal is routed through RL7-5/4. At this point the voltage is also used to energize the attenuator guard network R15 etc. It is routed to the PHI(DCV) line through RL7-10/11, then out to the I+ terminal and back from the Hi terminal on the SHI(DCV) line as for the 1V range. The current returning from the I- terminal is sunk into common-2 via the overcurrent detector R56 *(see para 7.3.7.1)*.

SHI(DCV) is range switched on to the HV attenuator R17 etc. by RL7-8/9, the reduced voltage being taken off through RL9-10/11 and applied to the inverting input of the Error Amplifier.

7.9.3 VCA DRIVE CIRCUITRY

(Circuit Diagram 430536 page 11.5-1)

The attenuated sense signal is applied to the inverting input of the Error Amplifier via RL9-10/11. This bootstrapped, high gain circuit compares the sense signal with DC Ref. When both are equal; the output at M20-6, the bootstrap common BS at TP1, DC Ref Hi and the sense signal are all at the same level. Therefore the differential input to the error buffer-comparator M15 is zero at M15-6/5.

The second M15 stage acts as a bipolar-unipolar switch which adapts the bi-polar action of the Error Amplifier to the unipolar sensitivity of the DC modulator:

- With the front panel **Output on+** LED lit, the POSITIVE control signal is at logic-1 (0V). FET Q1 conducts, setting the M15-3 non-inverting input to zero volts, so the amplifier inverts the input at M15-2.
- Alternatively, if the **Output on-** LED is lit the POSITIVE signal is at logic-Ø (-15V), cutting off Q2. M15-3 follows the M15-7 voltage, so the amplifier acts as a voltage follower.

The gain from M15-7 to the I+ terminal is approx. x2000. R87 and C40 at the Error Amplifier input; and R40, C21 on the first stage of M14; provide frequency compensation for the overall loop.

For the 1000V range, the second M14 stage is connected as a non-inverting line buffer by contacts 8/4 and 9/13 of activated relay RL6. The output from M14-7 passes to the Power Amplifier assembly via J5-73 and the Mother assembly.

7.9.3.1 Action of VCA Drive Circuitry

If a user increases a positive OUTPUT display value, the positive DC Ref Hi voltage will increase (this is a demand to increase a positive output voltage). The polarity switch inverts the positive input from M15-7, so M15-1 feeds a negative output to M14. This is inverted at M14-1 and then buffered by voltage follower action at M14-7. It is passed via the Mother assembly to the DC modulator on the Power Amplifier assembly as an increasing positive DC signal.

In the case of an increasing negative OUTPUT display value, the negative DC Ref Hi value will increase negatively. But now the POSITIVE signal is at logic-Ø (-15V), so the output from M15-7 is not inverted and remains negative as for positive outputs. The action of M14 is not altered, so an increasing positive signal is sent to the DC modulator as before.

In both of the above cases the signal sent to the DC modulator is increasing positively, and this will result in an increasing 16kHz amplitude input to the 100V Amplifier. All polarity information is lost, so has to be re-inserted after rectification of the step-up transformer output, by the polarity switch in the High Voltage assembly.

7.9.4 DC MODULATOR

7.9.4.1 16kHz Derivation

(Circuit Diagrams:430648 page 11.3-2; 430652 page 11.4-5; 430618 pages 11.9-5 /11.9-2)

The 13-bit counter in the Analogue Interface generates 16kHz at pin 14 of M16 *(page 11.3-2)*. This is transferred into guard through opto-isolator M3 on the Reference Divider *(page 11.4-5)*. The 16kHz square wave, switching between logic-1 = 0V and logic-Ø = -15V, enters the Power Amplifier assembly on J9-61 *(page 11.9-5)*.

Providing the 1kV range is selected, and the 'PA CLAMP' signal is at logic-Ø (-15V), the full 15V p-p squarewave passes via M6-4 and M9-10 to inverter Q41 *(page 11.9-2)*.

7.9.4.2 DC Error Signal Processing

(Circuit Diagram 430618 page 11.9-2)

The modulator operates by alternately charging the low-pass filter formed by R83, C83 and C84 via the series switch Q39, and discharging it through Q40.

The 16kHz MOD DRIVE squarewave alternates between logic-1 (0V) and logic-Ø (-15V). After inversion in Q41, the signal at its collector switches between the +15V and -15V rails. Positive half-cycles of the MOD DRIVE signal make Q41 conduct, switching Q40 off and Q39 on, so the DC Error voltage charges the filter. For negative half-cycles the conditions are reversed and the filter is discharged to Common-2.

The DC Error signal is always positive, due to the polarity switch on the DC assembly. Its amplitude depends on the difference between the conditioned output voltage and the DC Ref Value, but is limited to +12V by D75.

The filter reduces the 32kHz and higher harmonic content of the squarewave, while passing 16kHz with little distortion. Its output is buffered by source-follower Q42, before being AC-coupled to the 100V Amplifier by a high pass filter (formed mainly by C86 with the approx. 400Ω input resistance of the amplifier).

The near-sinusoidal 16kHz signal input to the 100V Amplifier has an amplitude which is proportional to the value of the DC Error signal, so it acts as an AC analog of the difference between the normalized instrument DC output voltage and the value of the DC Ref voltage. It is based on a mean of 0V, and is passed as the '1kV ERROR O/P' signal via RL1-11/13 and RL2-6/4 into the Gain Stage of the 100V Amplifier *(page 11.9-3)*.

7.9.5 100V AMPLIFIER

(Circuit Diagram 430618 page 11.9-3 - For description refer to Subsections 7.8.3 and 7.8.4)

This operates as for the 100V range, but in this case the DC path simply maintains the zero offset of the AC signal, which is amplified along the AC path. The output signal 'OUTPUT' is fed from J3-9 to relay RL6 contacts *(page 11.9-2)* for application to the step-up transformer.

7.9.6 '1kV ENABLE' RELAY RL6

(Circuit Diagram 430618 page 11.9-2*)*

Relay RL6 allows the OUTPUT signal from the 100V Amplifier to energize the HF step-up transformer, providing the following conditions are met:

- **The $\overline{\text{1kV}}$ Signal is at Logic-Ø:**
  This is a processor-controlled signal, set to logic-Ø when the instrument output is switched on, in the 1000V range.
- The Watchdog has NOT 'Barked'.
- The '1kV ENABLE' Switch S1 on the Power Amplifier assembly is set to 'ENABLE'.
  S1 is situated below the left-hand ejector lever (viewed from the front of the instrument), facing the rear. It allows the high voltage to be switched off for servicing purposes.

A red LED glows when all other conditions are met.

When RL6 is closed, the OUTPUT signal from the 100V Amplifier is switched through to the contacts of RL7.

7.9.7 LF/HF TRANSFORMER SELECTION

The two transformers are separately located, their secondaries being connected into the High Voltage assembly. The HF transformer is selected when RL7 is unenergized, its primary being returned to Common-2C. RL7 is energized to select the LF transformer.

For the 16kHz signal used with the 1000V DC Range, the HF transformer is selected by RL7 being unenergized.

7.9.8 HIGH VOLTAGE TRANSFORMER AND RECTIFIER

(Circuit Diagram No. 430537 page 11.14-1).

For the 1000V DC Range, the HF transformer gives a step up ratio of 1:6.17. This ratio generates secondary voltage outputs large enough to provide DC outputs from the instrument of 1100V. The AC relays RL2 and RL3 in the High Voltage assembly remain un-energized for the 1000V DC range, but the DC relay RL4 is energized, applying the HF transformer secondary voltage to the rectifier bridge via RL4-5/4 and RL4-2/3.

The rectifier bridge uses two series diodes in each arm. Each diode is current-rated at 1A, with a p.i.v. of 1.5kV.

N.B. The transformer secondary and bridge rectifier are not directly referred to any common. This allows the rectifier output to float so that it may be used for either polarity.

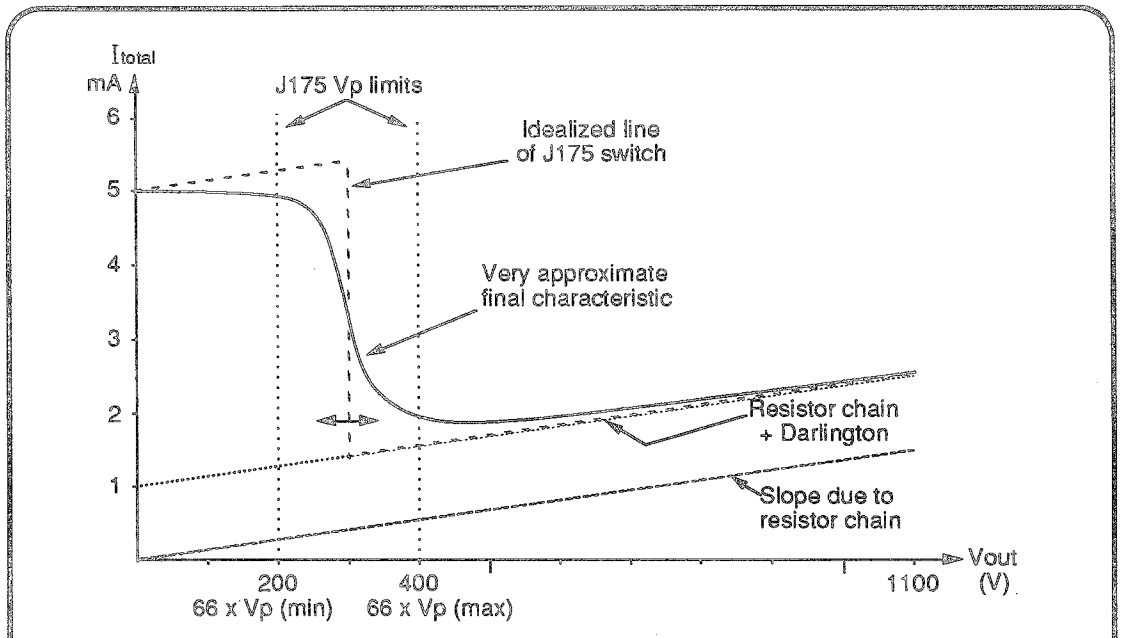

FIG. 7.3 ACTION OF CONSTANT-CURRENT SOURCE

7.9.9 CONSTANT-CURRENT ASSEMBLY

(Circuit Diagram 430563 page 11.14-2).

7.9.9.1 Constant-Current Source.

Q1-12 form a series Darlington chain, connected across the bridge rectifier output as a constant-current source, having two functions:

- It maintains conduction in diode bridge D56-D63 under no-load conditions.
- At higher voltages, D15-D17 limit Q11 base voltage to +2.4V, limiting the series current in R11, with Q13 pinched off. At lower voltages Q13 conducts, shunting R11 with 170-180Ω (R10 plus Q13 'On' resistance which falls to approx 125Ω), and increasing the discharge current. The approximate shape of the overall characteristic is shown in *Fig. 7.3*.

NB: Note that the minimum voltage applied across the constant-current source is 38V. Even at zero output voltage and current, the diode bridge generates 38V to back off the positive or negative 38V connected to RL3.

7.9.9.2 Overvoltage Detection

Zener diodes D1 - D13 form a series chain across the High Voltage supply. When the voltage exceeds 1440V this chain conducts, lifting D13 cathode and driving opto-isolator M1. M1 collector falls, turning on Q14, whose collector voltage rises to provide a 'LIM DET' logic-1 (0V) output at pin 5. This signal travels from the High Voltage assembly at J1-14, via the Mother assembly, to the Power Amplifier assembly at J9-69.

The operation of the LIM DET circuitry and subsequent action is described in *Section 7.12*.

7.9.10 POLARITY SWITCHING

(Circuit Diagram 430537 page 11.14-1)

Double-pole relay RL5 performs the polarity-reversal. With RL5 un-energized as shown the output filter is connected to rectifier positive, and the -38V Common-2 supply is connected to rectifier negative. During zero calibration, the -38V is backed off to give a true zero output by an output from the rectifier.

Relay RL5 is controlled by the Exclusive-NOR gate M4-2, under the influence of the CPU's 'POSITIVE' and 'PA CLAMP ON' signals from the serial data-link parallel output registers. When negative outputs are selected, providing the PA is not clamped; RL5 is energized, the output filter is connected to rectifier negative, and the +38V Common-2 supply is connected to rectifier positive. Again, the +38V is backed off by an output from the rectifier for all negative outputs, including zero.

The requirements which decide the use of the Exclusive-NOR function are discussed in *sub-section 7.12.4*.

7.9.11 OUTPUT FILTERING

The high voltage output is filtered in three stages:

a. L3, R1, C1 and C2 together form a 2-pole low-pass filter, which attenuates 16kHz by approximately 30dB and 32kHz by approximately 42dB.

b. L4, L5 and their associated capacitors form a 5-pole filter with elliptical characteristics, attenuating by at least 60dB above 16kHz.

c. The final stage is formed by R10, with C1, R84 and R85 on the Mother assembly (*Circuit Diagram 430604 page 11.16-1*). This provides further attenuation of approximately 30dB at 16kHz and 36dB at 32kHz.

7.9.12 1kV DC OVERCURRENT

The overcurrent detector on the DC assembly operates on the 1000V Range identically as on the 1V Range. Refer to *para 7.3.7.1*.

7.9.13 1kV and 100V SENSE ATTENUATION

(Circuit Diagram 430536 page 11.5-1)

Both ranges' output voltages are sensed on the SHI(DCV) line and reduced to 10V Range levels in the same guarded attenuator.

The 1000V Range output is developed across the full attenuator via relay RL7-8/9 contacts, and the guard chain is driven from the DC 1kV line via RL7-5/4.

The 100V output enters the attenuator at the tapping between R85 and R101 via RL8-9/8 contacts, the corresponding guard voltage being applied to the Guard chain via RL8-4/5.

The output tapping is common to both ranges, taken at the 900kΩ/100kΩ junction of R101. Thus the 1000V DC Range voltages are attenuated by 60:1, the 100V DC Range voltages by 10:1. The reduced output from the Sense attenuator is applied to the inverting input of the Error Amplifier.

Each junction between adjacent elements of the attenuator has its own guard screen. To eliminate leakage while providing an effective guard, a separate attenuator steps the power output voltage on the PHI(DCV) down to the correct voltage for each junction's guard screen.

The Sense attenuator sinks into Common-1, the 'reference' common to which the Error Amplifier and the 10V/1V attenuator are also referred. The guard attenuator sinks into Common-2, the general analog power common.

7.10 LOGIC CONTROL OF DC OUTPUTS

Two main aspects of analog control functions can be considered:

a. The effects of the controls on the analog circuitry, which are discussed elsewhere in the descriptions of the relevant circuits;

b. The methods of implementing the control logic, which have been developed to use the minimum number of control signals. It is also required to dissipate as little energy as possible inside the heat-shielding chassis assembly, to avoid temperature effects on the accuracy of the analog circuits themselves.

7.10.1 LOGIC LEVELS

In general, the analog control logic operates between 0V and -15V, with Logic-1 = 0V, and Logic-Ø = -15V. These levels are set originally at the serial/parallel control data latches in the Reference Divider assembly as outputs from the serial data link, and are accepted by the parallel/serial status data latches as inputs to the link back to the CPU. Some special control signals are passed into guard via opto-isolators, also in the Reference Divider, operating between -10V and -15V. These are subsequently adjusted to the normal control logic levels.

7.10.2 HEAT REDUCTION

Two methods are used to ensure that the energy dissipated by the relays is minimized:

- Use of bistable latching relays.
- Use of an 'Update' signal;

7.10.2.1 Update Considerations

For some heat-sensitive environments within the chassis assembly, polarized bistable latching relays are used which only require actuation, and hold on without a solenoid supply. Where relays need hold-on energization, they are usually tied to 0V or +15V on one side, and controlled on the other by the uncommitted collector of an inverting Darlington driver. Thus when the input to the driver is logic-1, the relay is held energized by its -15V output; and when the driver input is logic-Ø, its output is high impedance, releasing the relay.

For some relays it is necessary to hold the full actuating voltage across the solenoid for the whole time that it is energized. But where periodic updating will not cause difficulties, a relay is held on between 0V and -15V, raising the 0V side to +15V to actuate it during an update,. Such relays have a secure hold-on voltage of approximately 12V, but require 20V or more to pull them in.

At intervals of 40ms (typically - depending on the priorities of the CPU's program), the CPU generates a data transfer across the serial interface, and an 'Update' signal is passed into guard by the CPU via an opto-isolator (M4 in the Reference Divider - *page 11.4-5*). This serves two purposes:

- It is mainly provided to ensure no delay in transferring important status data back to the CPU;
- It is available when it is required to update the analog state of the instrument functions, as demanded by reversionary modes or user inputs.

After passing into guard, the update signal is named '$\overline{\text{UPD(IG)}}$'

7.11 DC ASSEMBLY RELAY DRIVES AND LOGIC

7.11.1 INTRODUCTION

(Circuit Diagrams 430536 page 11.5-3 and 430668 page 7-23).

The analog circuitry is mainly controlled by low-thermal relays, many contacts being fitted back-to-back to further reduce temperature effects. For the fastest response, the output relay RL15 is not latched, but can trip out quickly if the power supply fails, removing any output voltage from the terminals.

The rest of the relays are latched, allowing hold-on without power, to reduce the internal temperature at their contacts. As they are polarized they require a bipolar actuating drive, which is provided by 'Tristate' relay drivers and a bias amplifier.

7.11.1.1 Latched Bistable Relays

(Circuit Diagram 430536 page 11.5-3).

As can be seen from the circuit diagram on *page 11.5-3*, the relays are strung out between the output of their bias amplifier (-7.5V approx. at M1-2) and the drive outputs from the Clamp assembly.

The bias amplifier M1 is a frequency-compensated voltage follower, buffering the tapping of attenuator R4/R5, to hold one side of each relay permanently at -7.5V. The relay drivers on the Clamp assembly can provide outputs at 0V or -15V when enabled by the $\overline{\text{UPD(IG)}}$ pulse, but return to tristate when disabled. A relay is therefore driven to one or the other of its bistable states during update, then latched in the chosen state when the driver output returns to open-circuit.

All the latched relays operate in the same polarity sense: when its driver output updates at logic-1 (0V), the relay latches to select its nominal function; for a logic-Ø (-15V) update, the function is deselected. In the analog circuit diagrams, the relay contacts are shown in their deselected state, equivalent to the un-energized state of a conventional non-latching relay. For consistency, in the analog descriptions relays are referred to as being 'energized' or 'unenergized'.

7.11.1.2 'Tristate' Relay Drivers

(Circuit Diagram 430668 page 7-23).

The relay drivers (M1, M2, M3 on the Clamp assembly) are octal 'Tristate' buffers. Each chip is served by two inverted enable inputs on pins 1 and 19 (four buffers - half the chip - per enabling input).

Whenever a switching command has been received, the CPU performs a control data transfer and the $\overline{\text{UPD(IG)}}$ line from J5-104 is pulsed to -15V for 50ms.

The switching logic places a logic-1 (0V) on the input of selected drivers, and logic-Ø (-15V) on those whose function is not selected. Because all the buffers are non-inverting, during the update pulse a driver selects its function by setting its output voltage to 0V, or deselects by pulling its output voltage to -15V.

7.11.2 CLAMP ASSEMBLY

(Circuit Diagrams 430536 page 11.5-3 and 430668 page 7-23).

On the DC Relay Drive Logic circuit diagram *(page 11.5-3)* the Clamp assembly is shown in block form. Also, the pcb pin numbers correspond to the pin numbers of the buffer chips: J7, J8 and J9 being the connections to M1, M2 and M3 respectively. For signals crossing the block from left to right, the output of each non-inverting buffer is drawn opposite its input, so the function remains unchanged as it crosses the block. As a further aid to identification, the pins of any one buffer are numbered so that the input and output numbers add up to 20.

7.11.2.1 $\overline{\text{UPD(IG)}}$ Distribution

As the $\overline{\text{UPD(IG)}}$ signal is distributed as the enable to many buffers, it is itself buffered before being fanned out. So the four $\overline{\text{UPD(IG)}}$ connections at the top of the block are inputs to four buffers (M1) which are permanently enabled by J7-19 at -15V. The outputs of two of these buffers are brought out to J7-5 and J7-7 which are not connected (and not shown on the circuit diagram).

The input at J7-11 emerges from the Clamp assembly at J7-9 to operate the driver for the non-latching relay RL15 (at M2-6). The fourth input at J7-17 emerges at J7-3, and is reconnected as the fanned-out enable to the other buffers on the assembly *(Fig. 7.4)*.

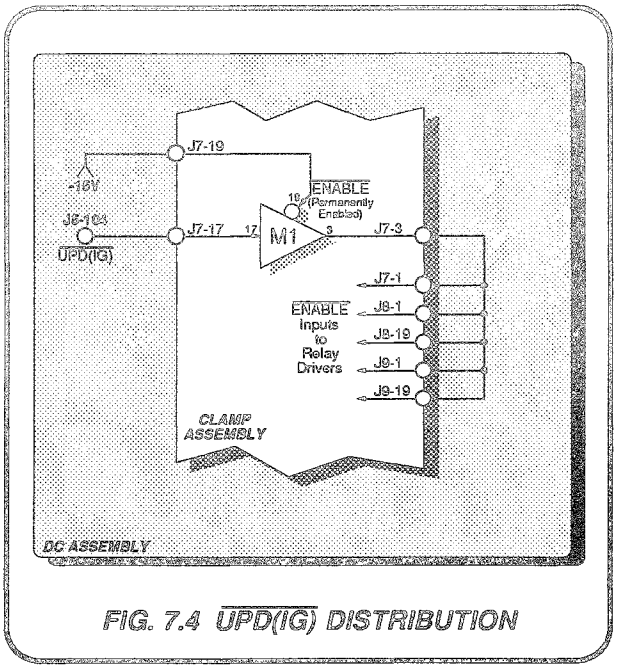

FIG. 7.4 $\overline{\text{UPD(IG)}}$ DISTRIBUTION

7.11.2.2 Buffer Clamping

(Circuit Diagram 430668 page 11.5-5).

Some versions of the 40244 octal buffer are protected against SCR avalanche if the output voltage exceeds the rail voltage, but some are not. Each buffer drives a relay solenoid, and is switched on and off by the update enable. Because the inductance of the relay coil can generate a back EMF in excess of the rail voltage, a clamp circuit guards against the possibility of SCR breakdown.

On the Clamp assembly Q1-Q4 form two power supplies, each delivering a regulated voltage of a diode-drop less than the rail voltage ('+VE CLAMP' and '-VE CLAMP'). A diode connected from the buffer output to each of the clamp lines allows the output voltage to rise to, but not exceed, the rail voltage *(see Fig. 7.5)*.

Where two parallel buffers drive two relays, the clamp diodes are omitted from one buffer output (e.g. M2-9 and M2-7 are joined on the DC assembly between J8-9 and J8-7, so both are clamped).

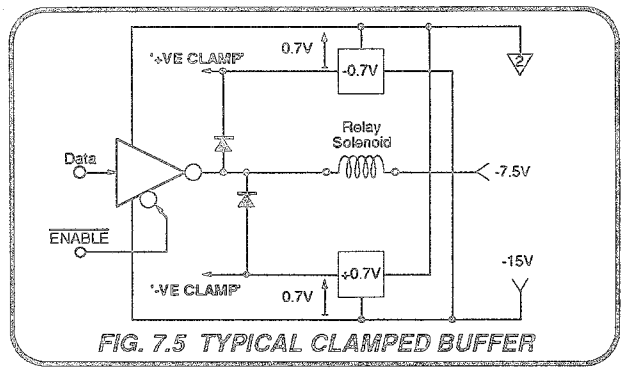

FIG. 7.5 TYPICAL CLAMPED BUFFER

7.11.3 DC ASSEMBLY SWITCHING LOGIC

(Circuit Diagram 430536 page 11.5-3).

The analog-control signals are transferred into guard on the Reference Divider assembly, and latched as 'Q' outputs in the Serial/Parallel Data Converter. Offset positive logic is employed (Logic-Ø = -15V, Logic-1 = 0V) for the signals entering the DC assembly via J5 from the Mother assembly. For general analog control considerations refer to *Sect. 7.10*.

7.11.3.1 Range Switching Logic

Range control data is input as a 3-bit code on DCRØ, DCR1 and DCR2 lines. The bit-pattern is decoded by M4 to select the correct range relays. As the 100µV, 1mV, 10mV and 100mV ranges all use the same analog circuitry, only one bit-combination (DCR2) is required for these four ranges. The resulting five combinations are listed in Table 4.1, which shows the states of M6 'Q' output pins and the relays energized for each range.

Note that deselection of DC function sets each DCR(2-Ø) to logic-1. The M6 'Q' outputs all fall to logic-Ø, deselecting all range relays except RL1, RL2, RL3 and RL16, which are selected by DCR2 being at logic-1.

7.11.3.2 Function and Output Switching Logic

Output voltages pass through the DC assembly on all AC and DC ranges. RL15 connects SHi, SLo, PHi and PLo to the instrument's Hi, Lo, I+ and I- terminals. Four signals control this relay:

OFF at logic-Ø when Output is selected ON.
BARK DEL at logic-Ø unless the watchdog has tripped.
$\overline{\text{AC FNCT}}$ at logic-Ø if AC Function is selected, or
DC FUNCT at logic-1 if DC Function is selected.

Under these conditions M4 pins 1 and 2 are set to logic-1, M4-9 is at logic-Ø; M4 pins 3, 4 and 5 are at logic-Ø, M4-6 is at logic-1. So M2-2 is driven positive, and as M2-3 is biassed at about -4.75V, then M2-1 goes to approximately -12V. During the update pulse J7-9 goes to -15V, so M2-7 goes to +15V. RL15 is thus actuated by some 27V, but after the $\overline{\text{UPD(IG)}}$ pulse is terminated, M2-7 returns to 0V and RL15 is held on. If AC and DC are both deselected, or if the output is set to OFF, or if the Watchdog barks; the -12V at M2-1 reverts to approximately +11.5V. If the $\overline{\text{UPD(IG)}}$ pulse is not present, the voltage across RL15 falls through zero and RL15 is de-energized. If it is present, only approximately 4.5V is connected across RL15, which is insufficient to hold the relay on. Under these conditions the instrument terminals are disconnected from the output.

Relays RL10 and RL18 are selected when DC voltage has been commanded, providing that the Watchdog has not barked. With DC FNCT at logic-1, M4-11/13 are at logic-Ø. If the Watchdog has not barked then BARK DEL is logic-Ø at M14-12. As a result of both these conditions, M4-10 is at logic-1 and both relays RL10 and RL18 are selected. RL10 connects the PHI(DCV) and SHI(DCV) line to the PHI(V) and SHI(V) lines respectively, RL18 connects the DC Ref output from the Reference Divider to the DC Error Amplifier input.

Relay RL11 connects the power and sense Lo lines back to their respective commons. Thus when RL10 and RL18 are selected for DC voltage outputs, so is RL11. But in Current Function it is also required to tie the Local Guard to Common-2. This also is done by selecting RL11. With Current selected, the $\overline{\text{I FNCT}}$ signal is at logic-Ø so M3-13 is at logic-1 and RL11 is selected.

The Remote Sense Relay RL14 is also selected by the $\overline{\text{I FNCT}}$ signal, as well as by the front panel selection of remote sense. These are combined at OR-gate M10-3, before selecting RL14 directly via its buffer. RL14 removes the local sense short between the power and sense lines at both Hi and Lo signal levels. For Current Function this has negligible effect on the DC assembly, but the REM SENSE '+' and '-' signals are also passed out to RL1 on the Mother assembly *(Circuit Diagram 430604 page 11.16-1)*. Although remote sense is not selectable for DC or AC Current ranges, it is necessary to route the current output to the I+ and I- terminals on the front panel. RL1 on the Mother assembly is energized to do this. (For Local Sense on voltage ranges, RL1 routes the power Hi line to the Hi terminal instead of I+). REM GU selects the Remote Guard relay RL17 via its buffer.

The HIGH I LIMIT and AC 1kV RANGE signals are concerned with the AC 1kV Overcurrent Detector circuit. The signals operate their relays RL12 and RL13 directly through their buffers. *Section 9* discusses their effects. The effects of control signals '1kVDC', '100VDC', $\overline{\text{DC FNCT}}$ ' and 'POSITIVE' are discussed in the descriptions of the analog circuitry at their destinations.

7.12 PA ASSEMBLY LOGIC AND RELAY DRIVES

(Circuit Diagrams 430618 Pages 11.9-4 and 11.9-5)

The CMOS logic operates between the levels 0V and -15V, with logic-1 = 0V, and logic-Ø = -15V. Relays are tied to +15V on one side, and controlled on the other by the uncommitted collector of an inverting Darlington driver. Thus when the input to the driver is at logic-1, the relay is energized by 15V; and when it is at logic-Ø, its output is high impedance, releasing the relay.

7.12.1 DC RANGE SWITCHING

(Page 11.9-5)

The three inputs DCRØ, DCR1 and DCR2 carry the DC range switching information, and are decoded by M7a as follows:

	M7a inputs			M7a outputs		
	E	B	A	Q2	Q1	QØ
Range Select	DCR2	DCR1	DCRØ			
1000V	0	0	0	0	0	1
100V	0	0	1	0	1	0
10V	0	1	0	1	0	0
1V	0	1	1	0	0	0
100mV	1	0	0	0	0	0
10mV	1	0	0	0	0	0
1mV	1	0	0	0	0	0
100µV	1	0	0	0	0	0
Deselect DC	1	1	1	0	0	0

7.12.2 AC RANGE SWITCHING

(Page 11.9-5)

The three inputs ACRØ, ACR1 and ACR2 carry the AC range switching information, and are decoded by M7b as follows:

	M7b inputs			M7b outputs		
	E	B	A	Q2	Q1	QØ
Range Select	ACR2	ACR1	ACRØ			
1000V	0	0	0	0	0	1
100V	0	0	1	0	1	0
10V	0	1	0	1	0	0
1V	0	1	1	0	0	0
100mV	1	0	0	0	0	0
10mV	1	0	1	0	0	0
1mV	1	1	0	0	0	0

7.12.3 FUNCTION AND RANGE LOGIC

DCV Logic

When un-energized, relay RL4 selects the DC ERROR signal in preference to the AC 1V signal, as input to the Power Amplifier when DC Voltage function is selected. When un-energized, Relay RL8 reduces the permissible overload on the output of the 10V Amplifier, also when DC Voltage is selected.

When 'DC' is selected on the front panel, both DC FNCT (J9-70) and $\overline{\text{I FNCT}}$ (J9-72) signals are at logic-1. Under these conditions both inputs to NAND M6-12/13 are at logic-1, so M6-11 is at logic-Ø and both relays RL4 and RL8 are un-energized. For all other function selections DC FNCT is at logic-Ø, so M6-11 is at logic-1 to energize both relays.

AC & DC 10V Range Logic

On the DC 10V Range only, the input to M6-1 is logic-Ø; and on the AC 10V Range only, the input to M6-2 is logic-Ø. Logic-1 occurs at M6-3 to operate relay RL3 only when either the AC or DC 10V range is commanded.

AC & DC 100V Range Logic

The input to Q12-8 is logic-1 only when the DC 100V range is selected, and the input to Q12-9 is logic-1 only on the AC 100V range. Either input gives logic-1 at M12-10, so relay RL2 operates only when the AC or DC 100V range is commanded.

AC 100V Range Logic

A '$\overline{\text{100V AC}}$' signal is also passed to activate the 100V Current Sense circuit *(see page 11.9-6)*, only on the AC 100V Range.

DC 100V Range Logic

The decoded DC 100V Range signal at M7a-5 is also connected to the cathode of D31. On other ranges the diode conducts to pull the DC INPUT CLAMP signal to logic-Ø (Off), but on the DC 100V Range D31 releases the line so that the PA CLAMP ON signal can set it to logic-1 (On).

AC & DC 1000V Range Logic

The $\overline{\text{1kV}}$ signal enters the Power Amplifier at J9-32. It is at logic-Ø only when AC or DC 1000V Range is commanded by the CPU, with the OUTPUT set ON. 'BARK' enters at J9-66, and is at logic-Ø only if the watchdog has not detected a failure *(see Sect. 6)*. With both inputs to M4-8/9 at logic-Ø the output at M4-10 is logic-1 which lights the internal warning LED D70. Relay RL6 is energized if the internal 1kV ENABLE switch on the PA assembly is set to its normal operating position of ENABLE. This allows the AC drive to be passed to the step-up transformers (16kHz signal in the case of the DC 1kV Range, to the HF transformer).

For other ranges, or if the watchdog barks, RL6 is de-energized, removing the AC drive to the step-up transformers. LED D70 is also de-energized.

AC 1000V Range Logic

The input to M13-3 is logic-1 to energize relay RL1 only when the AC 1000V range is commanded. A 'AC 1kV RANGE' signal is also passed to the DC assembly to select the overload sense resistor.

DC 1000V Range Logic

Although the combination of the universal $\overline{\text{1kV}}$ Range signal and the AC 1kV signal is used to define the DC 1kV circuitry, two extra facilities are required for the DC 1kV Range. The 16kHz REF FREQ signal has to be switched to the DC modulator. For negative outputs on the 100V Range the 100V Amplifier positive rail is reduced to +38V instead of the +400V supply, so this has to be restored to +400V for the AC signals on the 1kV Range. For these applications the decoded DC 1kV signal at M7a-4 is used as input to M4-6 and M6-6.

(Continued overleaf)

The REF FREQ signal enters at J9-61 and is enabled at M6-5 by the 1kV Range decode on M6-6. Provided that the PA CLAMP ON signal is Off (ie. at logic-Ø), the 16kHz 'MOD DRIVE' signal is passed to the 1kV DC Modulator *(see page 11.9-2)*.

The POSITIVE signal entering at J9-41 is input to M4-5 and the 1kV Range decode is input to M4-6. If a negative output on the 100V Range is commanded, then both inputs are at logic-Ø. The output at M4-4 is logic-1 and M15 causes the LED in M16 to conduct by pulling M16-3 to logic-Ø. The photo-transistor of M16 conducts *(see page 11.9-3)*, placing a short circuit between the source and gate of Q20, which turns off the +400V supply to the 100V Amplifier driver stage. Q9 conduction causes D56 to conduct, so for negative outputs on the 100V Range the positive rail for the driver is sourced from the +38V supply.

On the DC 1kV Range the +400V supply is required to deal with the AC signal being amplified, so M4-6 at logic-1 inhibits the disabling photo-coupler; M13-15 being open-collector. The same inhibition results for positive outputs on the DC 100V Range (when the +400V is needed to power the driver stage) by M4-5 at logic-1.

7.12.4 'PA CLAMP ON' SIGNAL

PA CLAMP ON is applied before the 1kV DC control loop is broken by the 1kV line, and released when the loop is restored. It is also required on entry into and exit from the 100V DC Range. Other ranges are 'don't care' states.

7.12.4.1 DC 1000V Range Clamp

When the DC 1000V Range is selected, but Output is set Off, the drive is removed from the input to the step-up transformer. The High Voltage assembly polarity relay RL5, in the positive position, connects -38V to the base of the Constant Current chain at Pin 2. The other end of the chain is connected, via the instrument output lines, to the head of the 1kV sense attenuator on the DC assembly. The attenuator output is fed to the inverting input of the Error Amplifier.

Under these conditions, the Error Amplifier 'sees' a negative voltage at the Output terminals, and would drive heavily into saturation on its positive side to correct the output. This would occur regardless of the size of the positive DC Ref voltage being applied on its non-inverting input. When the positive Output was reset to On, the power circuitry could generate a massive swing which would result in catastrophic failure. A similar (but polarity-reversed) effect could be present for negative DC Output selections.

This excess loop gain is removed by reversing the position of the polarity switch during the time that the output is turned off, so that the Error Amplifier sees a positive voltage and backs off toward zero. The logic to reverse the polarity is driven by the PA CLAMP ON and POSITIVE signals, employing an exclusive-NOR gate.

In the High Voltage assembly, M2-4 feeds the driver for the polarity changeover relay RL5. The inputs at M4-5 and M4-6 are POSITIVE and PA CLAMP ON respectively.

The required reversal conditions are satisfied as shown:

Selected Commands	'POSITIVE'	PA CLAMP ON	M2-4 State	RL5 State	Nominal Output Polarity
-VE-O/P ON	Ø	Ø	1	Energized	-ve
-VE-O/P OFF	Ø	1	Ø	Un-energized	+ve
+VE-O/P ON	1	Ø	Ø	Un-energized	+ve
+VE-O/P OFF	1	1	1	Energized	-ve

The PA CLAMP ON signal at logic-1 also disables the 16kHz MOD DRIVE signal to the DC Modulator.

7.12.5 '400V ENABLE' LOGIC

The '400V(2) OFF' signal from the CPU is normally at logic-Ø for voltage ranges; but after a 'FAIL 7' message indicates a 400V supply failure, it is toggled three times, attempting to restore the supply.

Thus in normal operation, BARK is logic-Ø and the PSI OFF signal from M11-4, also logic-Ø, is input to M1-1/6 *(page 11.9-4)*. M1 consists of six inverting drivers, each with uncommitted-collector output (as used for the relay drivers). M1-1 at logic-Ø allows M1-2 to be pulled to logic-1 by AN1-1/2, or to logic-Ø by M1-14. In the lower chain with four inversions, M1-14 is also open-collector, if a 400V or 15V failure has not been detected by the monitors.

Thus for normal operation M1-2 is pulled to logic-1 and the 'ENABLE 400V-' line from M1-15 is held at logic-Ø (-15V). With the 'ENABLE 400V+' line it energizes the opto-isolator LEDs in the 400V power supply (PS/I heatsink *page 11.13-3*).

A failure of either the 400V or 15V supply pulls M1-3 to logic-1, disabling the 400V supply by setting the ENABLE 400V- line to logic-1. If the +15V or -15V rail collapses, the opto-isolator current is cut off in any case, due to zener D24.

7.12.6 'BIAS OFF' LOGIC

On the 100V or 1000V ranges, after receiving a 400V FAIL signal from the monitor, the CPU attempts three times to restore the 400V supply. The foldback current limiting for the supply (in the PS/I heatsink) prevents reinstatement if an overload persists. Thus it is necessary to remove the overload if the supply is to be restored. This is done by setting the BIAS OFF line to logic-Ø (-15V), cutting off Q10 *(page 11.9-3)* and removing the output drive.

The three attempts are made by toggling the 400V(2) OFF line (described in *sub-section 7.12.5*). Each time the supply is enabled, R6 and C1 hold the BIAS OFF signal at logic-Ø for about 1ms to allow the supply to build up before the load is reapplied.

After three unsuccessful attempts, the CPU assumes a permanent hardware fault and holds the 400V(2) OFF signal at logic-1.

7.12.7 'LIM ST' LOGIC

This status signal is passed back to the CPU via the SSDA serial link to indicate that certain limits have been exceeded. The LIM ST signal entering the Reference Divider at J4-76 *(page 11.4-4)* can be activated to logic-Ø by any one of nine detectors, as illustrated in the simplified diagram of *Fig. 7.6.*

7.12.7.1 'LIM DET'

The LIM DET signal output from the Power Amplifier at J9-67 *(page 11.9-5)* can result from the LIM DET signal setting the latch M5a. LIM DET is associated with the high voltage ranges, and can be activated by:

- **DC Assembly** *(page 11.5-1/2)*
  AC 1kV Overcurrent Detector
  DC Overcurrent Detector (100V & 1000V DC ranges)
- High Voltage Assembly (Constant Current Source)
  DC 1kV Overvoltage Detector
- Power Amplifier Assembly
  AC 100V Overcurrent Detector
  AC 1000V Overvoltage Detector

  (These two combine to generate the 100V FLAG, which is NORed with 'DC FNCT' before becoming LIM DET.)

NOT100V FLAG is initiated by the AC 100V Overload Detector or AC 1000V Overvoltage Detector *(page 11.9-6)*, whenever the 400V supply current peaks are excessive, or the AC 1kV Range drive voltage to the primary of the step-up transformer is excessive.

The LIM DET logic-1 is immediately transferred via M12-3 as the signal 'I LIM 100V AMP' to the gate of Q14 *(page 11.9-3)*. Q14 conduction reduces the 100V amplifier input to zero, so if the overload is external the LIM DET signal should revert to logic-Ø.

7.12.7.2 'LIM ST' Generation

The latch M5a is set by logic-1 on pin 6, for as long as LIM DET remains at logic-1. Its 'Q' output activates LIM ST via M4-3 to inform the CPU. It also reinforces and latches I LIM 100V AMP. LIM ST is also activated if the overload signal 10V FLAG from the 10V Amplifier is at logic-Ø when in AC 10V Range.

Other detectors which can provide the LIM ST signal are:

- DC Assembly *(page 11.5-1/2)*
  DC Overcurrent Detector (1V & 10V DC ranges)
- **Sine-Source Assembly (Constant Current Source)**
  AC 1V Buffer Overcurrent Detector
- **Current/Ohms Assembly**
  DC and AC Current ranges Overvoltage Detector

7.12.7.3 CPU Response

On receipt of the LIM ST signal, the CPU initiates a series of clock pulses on the 'I LIM RST' line via the SSDA and Reference Divider, so that M5a can be reset as soon as the LIM DET signal clears to logic-Ø, M5a 'D' input being strapped to logic-Ø (-15V). The CPU also displays the 'Error OL' message.

If the LIM DET line has cleared to logic-Ø, the 100V Amplifier input is reinstated by M5a being reset. Furthermore, if the overload was temporary, the LIM DET line remains at logic-Ø, and normal operation resumes. The CPU is informed by LIM ST at logic-1, so the I LIM RST pulses are discontinued, and the Error message is removed.

For a persistent overload, the detectors operate again — the cycle repeating until user action is taken to remove the overload. The Error message continues to be displayed. If the overload is an internal fault, it is likely that another protection circuit will have detected it and taken its own action.

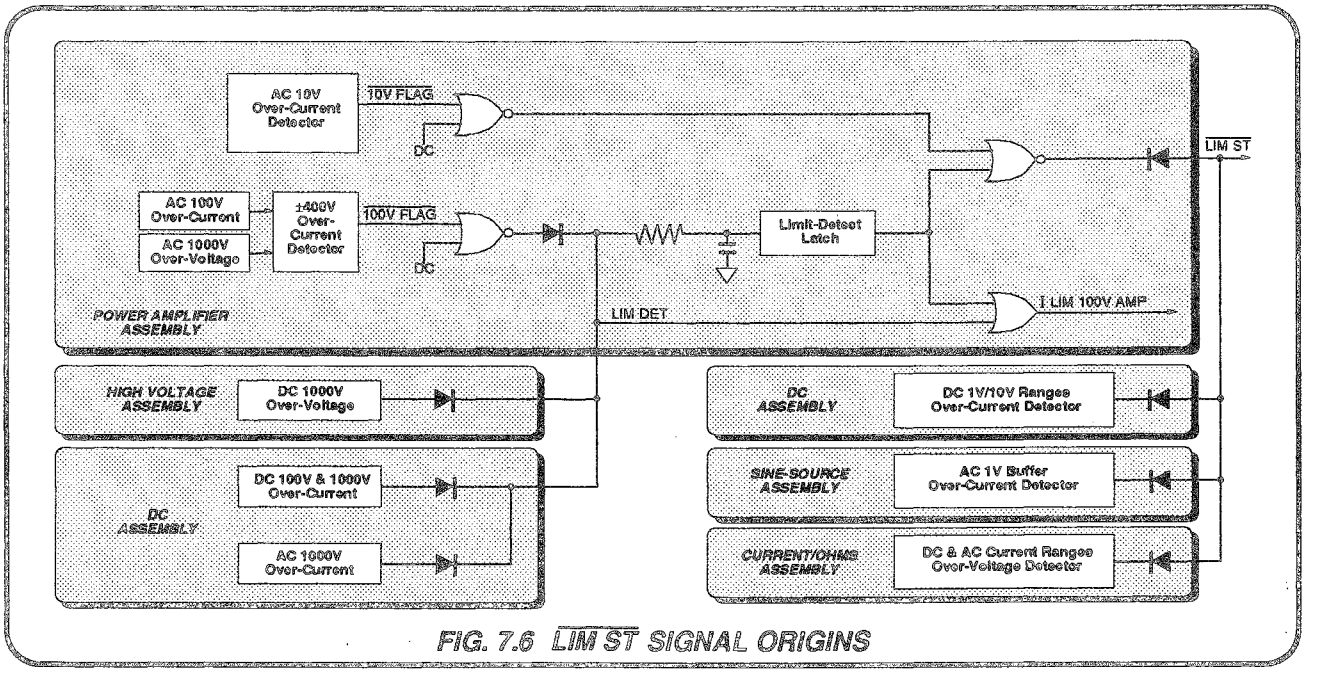

FIG. 7.6 LIM ST SIGNAL ORIGINS

7.12.8 'LF', '$\overline{LF}$' and '1kV GAIN'

These are signals used to control the gain and compensation of the AC 1kV amplifiers, *(Refer to section 9.7)*.

The 'LF' signal is set to logic-1 by the CPU via the SSDA serial link and Reference Divider latches, when the AC 1000V range and the 100Hz or 1kHz frequency ranges are selected. It is inverted as '$\overline{LF}$' at M11-12, and then inverted as buffered 'LF' at M11-10.

'FREQ RØ' is also CPU-controlled. It is set to logic-1 when either the 1kHz or 100kHz frequency range is selected.

'$\overline{LF}$' and 'FREQ RØ' are combined at M6-10 to give the '1kV GAIN' signal, which is at logic-Ø only when the 100kHz range is selected. (The software prevents the 1MHz range being selected on the 1000V range).

7.12.9 THERMISTOR COMPARATOR

Two NTC thermistors situated in different positions on each PA heatsink are part of a bridge network which detects excessive temperatures on the heatsinks.

The reference arm of the bridge is formed by R165 and AN9-7/10 in parallel, both in series with AN9-6/11.

The sense arm has four parallel sections, each consisting of one section of AN9 in series with one of the NTC thermistors. Four null detectors are used (M22 and M23), each comparing the voltage at the reference arm junction with that at the junction of one of the sections (TEMP +R/-R/+F/-F).

At 25°C each thermistor resistance is 10kΩ. The bridge is unbalanced in favour of open-collector outputs from the four comparators, pulled up to Common-2 by AN2-3/4 and AN2-5/6. Q36 is therefore cut off, and the 'OVERTEMP' signal at J9-31 is at logic-Ø (-15V).

If one of the chip temperatures exceeds 100°C, its thermistor resistance falls to the extent that the bias on its null detector is reversed. The null detector output is taken low to -15V, Q36 conducts and the OVERTEMP signal goes to logic-1.

The OVERTEMP status signal is passed to one of the Reference Divider status registers, *(page 11.4-4)*, where for safety reasons it is pulled-up by a 1MΩ section of AN2. The CPU reacts to the logic-Ø signal by displaying the 'FAIL 1' message, and forcing a recovery sequence:

OUTPUT OFF
Reference Divider ramp to zero
Remote Sense OFF
Analog Control 'OFF' bit set
Analog Control '1kV' line disabled
Display and Keyboard locked

After approximately 1 minute, the CPU defaults the instrument to the normal 'OUTPUT OFF' state in the selected ranges with output set to zero. The FAIL 1 message is removed, and the user is at liberty to try another attempt.

Under normal power-up conditions, with the Power Amplifier assembly plugged in and Q36 cut off, AN2-7/8 holds the line more negative than -14V (logic-Ø). If the Power Amplifier is removed, no over-temperature information is available from the heatsinks. In this event, the OVERTEMP signal rises to logic-1, indicating failure.

SECTION 8
AC VOLTAGE OUTPUTS - FREQUENCY CONTROL SYSTEM

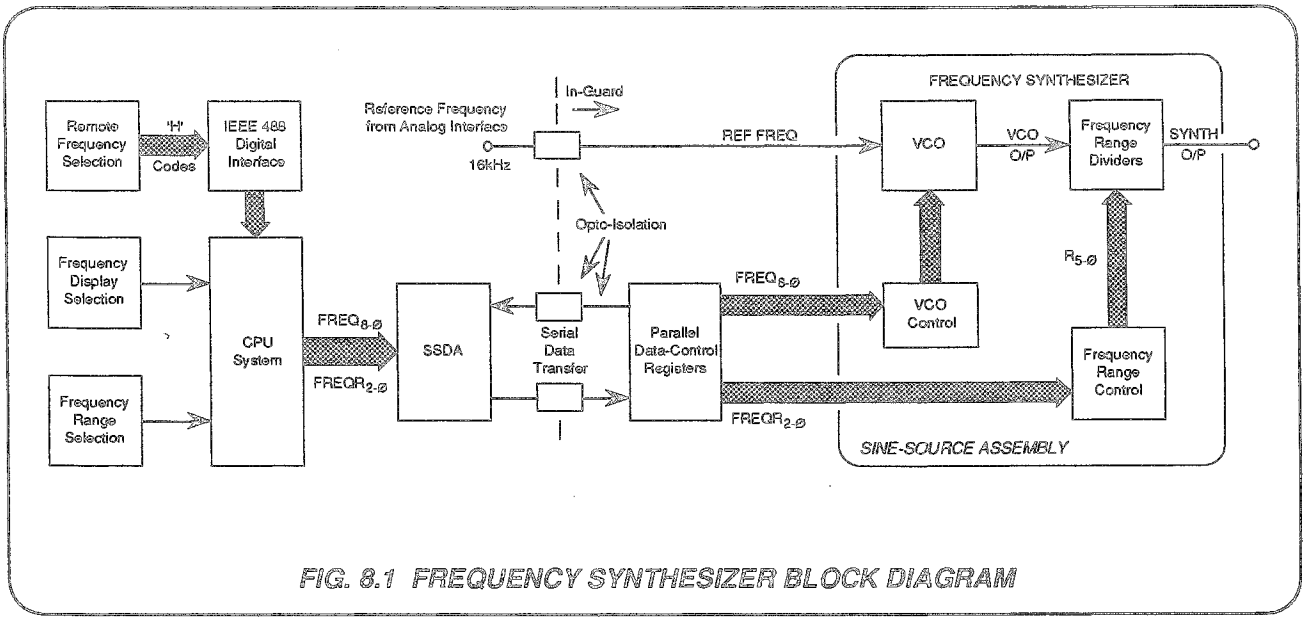

FIG. 8.1 FREQUENCY SYNTHESIZER BLOCK DIAGRAM

8.1 DIGITAL FREQUENCY SYNTHESIZER

(Fig. 8.1)

8.1.1 GENERAL

Users normally set the operating frequency by a combination of 'FREQUENCY RANGE' and 'FREQUENCY' display selections. These are memorized by the CPU and translated into two binary control words:

'FREQ $R_{2-Ø}$'
: A three-bit word, five of whose codes represent the five frequency ranges.

'$FREQ_{8-Ø}$'
: A nine-bit word whose value 'n' defines the chosen frequency with respect to the selected frequency range.

Users can select a frequency by means other than pressing a FREQUENCY RANGE key and setting a frequency on the display; for example by using 'Store' or the IEEE 488 digital interface. But regardless of the selection method, the CPU will always compute the two binary words, which then synthesize the selected frequency in the Sine-Source Assembly.

Both words are passed into guard via the SSDA, and latched at the outputs of the Reference Divider Parallel Control registers. A 16kHz reference frequency is also taken into guard, to be divided by two to 8kHz in the Sine-Source assembly.

After entering the Sine-Source assembly, $FREQ_{8-Ø}$ effectively multiplies the 8kHz reference by a factor 'n' to determine the frequency of a Voltage Controlled Oscillator (VCO). The VCO frequency (signal 'VCO O/P') is input into a series of frequency dividers, whose ratios are set by FREQ $R_{2-Ø}$. The division ratios are chosen so as to make the dividers generate the Frequency Synthesizer output signal ('SYNTH O/P') at the user-selected frequency.

The purpose of the synthesizer is to provide an accurate frequency reference for the quadrature sinewave oscillator. The oscillator is approximately tuned by selection of circuit constants using the combination of 'FREQ $R_{2-Ø}$' and '$FREQ_{8-Ø}$'.

'SYNTH O/P' acts as the reference in the phase comparator of a Phase-Locked Loop, controlling the frequency of the main Quadrature Sinewave Oscillator to an accuracy determined by the crystal oscillator.

8.1.2 VOLTAGE CONTROLLED OSCILLATOR

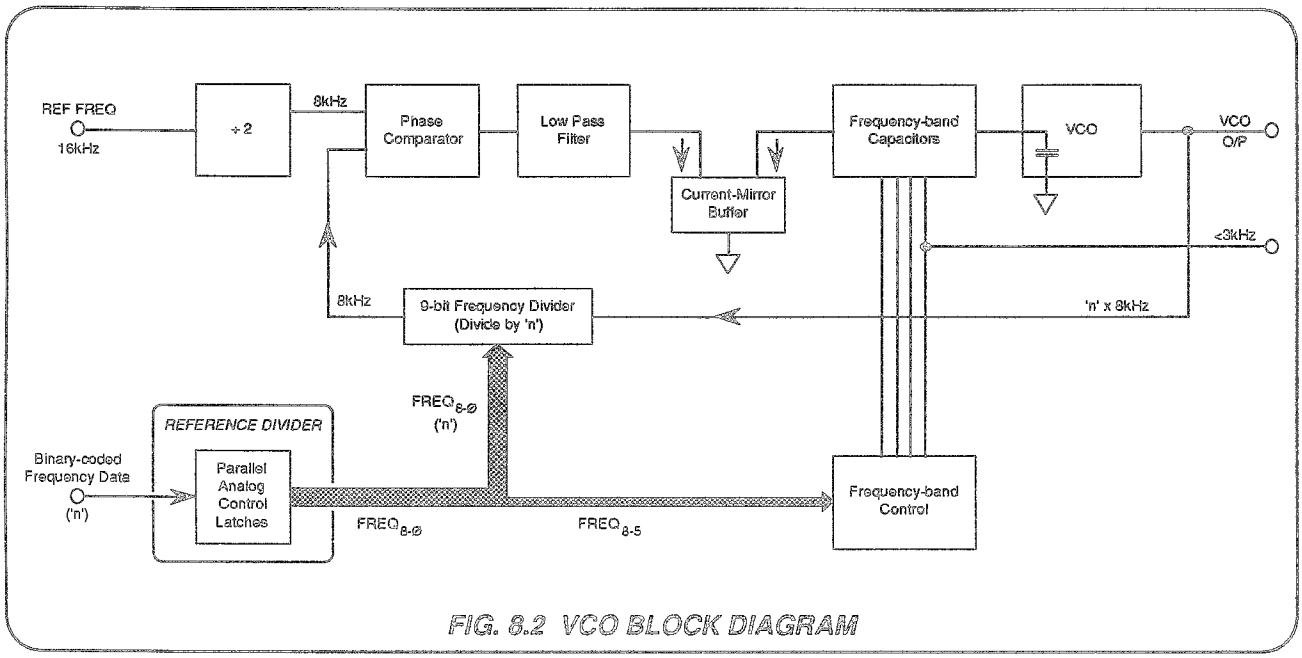

FIG. 8.2 VCO BLOCK DIAGRAM

8.1.2.1 Generation of 16kHz Reference

(Circuit Diagrams 430648 page 11.3-2, 430652 page 11.4-5 and 430446 page 11.6-4)

The 16kHz (INT) signal originates at M16-14 in the Analog Interface *(page 11.3-2)* and is buffered as '16kHz(OG)' *(page 11.3-1)*. On the Reference Divider at J4-104, it passes into guard via opto-isolator M3 *(page 11.4-5)*, gating with 'DISABLE REF FREQUENCY' and 'BARK' in M24, filtered by R86/C38 to reduce harmonics from the transmission path, and is sent via the Mother Assembly to J6-53 on the Sine-Source Assembly *(page 11.6-4)*.

Schmitt-trigger M14 inverts the 16kHz into a symmetrical squarewave, which is then applied as clock to M13a, a bistable connected to divide by two. The resulting 8kHz squarewave is taken as the reference frequency for phase comparator M12. Note that in this configuration the SIG input of M12 is used for the reference, and the divided VCO output signal is applied to the REF input. This is necessary to provide the correct sense in the phase control element M50, because of the inversion of integrator M11.

8.1.2.2 Squarewave Generation by the VCO

The VCO is a discrete-component ECL relaxation oscillator generating an output of frequency 'n' x 8kHz. Its natural frequency is dependent on:

- the value of capacitor C2 (or C2 plus one of C3 - C6),
- the value of its continuous discharge current through the phase control element (current mirror M50), and
- the value of its charging current through Q2 on alternate half cycles (4.7mA).

Consider C2 fully discharged. Q4 is off; so all the 4.7mA from Q6 passes through Q5. The collector voltage of Q4 is close to the positive rail, buffered by Q7 and R9 to hold Q5 on. Also, as Q3 is turned off by Q4 collector voltage, Q2 is turned on by its emitter, passing 4.7mA into C2 and the current mirror M50.

Capacitor C2 charges until Q4 turns on. Cumulative Schmitt action passes the fall at Q4 collector to the base of Q5, ensuring a rapid transition between states; so the 4.7mA is transferred from Q5 to Q4. Q3 turns on, its emitter falling quickly to cut Q2 off, so the charging path to C2 etc. is interrupted.

M50 continues to discharge C2, whose voltage falls slowly until Q4 starts to cut off again. The cumulative action is repeated to turn Q2 on, recharging C2. The cycle of charge and discharge continues, generating 'VCO O/P' squarewaves at buffer Q12 emitter.

8.1.2.3 Coarse Frequency Control

(Circuit Diagram 430446 Page 11.6-4, and Fig. 8.2)

At any time, only one of the capacitors C3, C4, C5 and C6 can be connected in parallel with C2, by conduction of its associated transistor. This splits the frequency range of the VCO into five bands, governed by the four most-significant bits of the frequency control word $FREQ_{8-0}$ acting on M8. The association is shown in *Table 8.1*; note that the VCO frequency bands quoted in the table are correct only because the VCO is under the fine control of comparator M12, within the phase-locked loop.

$FREQ_{8-5}$ bits 8 7 6 5	Range of 'n' Values	M8 O/Ps at Logic-1	C2-C6 Selection	VCO Frequency Band (kHz)
0 0 0 0	10 to 31	$X_{\varnothing}$	C2 & C6	80 to 248
0 0 0 0	32 to 63	X_1	C2 & C5	256 to 504
0 0 0 0	64 to 127	X_{3-2}	C2 & C4	512 to 1016
0 0 0 0	128 to 255	X_{7-4}	C2 & C3	1024 to 2040
0 0 0 0	256 to 500	NONE	C2 only	2048 to 4000

TABLE 8.1 COARSE FREQUENCY CONTROL

8.1.2.4 Fine Frequency Control

(Circuit Diagram 430446 Page 11.6-4, and Fig. 8.2)

In the following description, capacitors C3, C4, C5 and C6 are ignored, but references to C2 should be read as including the appropriate additional capacitor.

The VCO output is fed back to M12 phase comparator via M9 and M13b, which are connected to act as a 9-bit frequency divider. Because the divider is controlled by $FREQ_{8-\varnothing}$, the VCO output frequency is always divided by 'n' before being applied to the REF input of the comparator. The output from the comparator will only be zero if the frequency fed back to M12-6 is 8kHz (ie. the VCO frequency is n x 8kHz), and in phase with the 8kHz REF FREQ at M12-3 (TP14).

The output from M12 is integrated by M11 to drive a DC current into the current mirror M50, which has a gain of two, its output current being drawn from the charge on C2. During the half-cycles of the VCO oscillation when C2 is being charged, the mirror obtains its current from Q2 conduction.

The phase control loop seeks to phase-lock the two inputs to the comparator. If they are in phase, the comparator output is at high impedance ('TRISTATE'). In this condition the integrator capacitors C16 and C18 have no charge or discharge path, so M11's extremely high gain maintains their charge, and thus the voltage at TP6. M11 supplies the input current for M50, the mirror continues to draw the same discharge current from C2, so the frequency of VCO oscillation remains constant. Thus the loop stabilizes only when the frequency divided by 'n' from the VCO output is in phase with (and therefore at the same frequency as) the reference 8kHz.

In stable operation, therefore, the loop maintains VCO oscillations at n x 8kHz, and the feedback dividers reduce this frequency by a factor of 'n' to 8kHz.

Any disturbance in the loop will generate corrections to restore zero phase difference at the inputs of M12. Frequency deviations are therefore detected at an early stage as phase changes, giving a measure of 'phase advance' correction.

8.1.2.5 'INHIBIT' (VCO Off)

The VCO can be switched off by a logic-1 of 0V at the base of Q11 (INHIBIT signal). This originates in the CPU system, setting FREQ $R_{2-\varnothing}$ code to 111 (a non-existent 'R7' range) when AC functions are deselected. It also resets the ÷2 flip-flop M13a, so that no reference frequency is passed into the phase comparator.

8.1.2.6 VCO Supply Rail Protection

To prevent VCO oscillations appearing on the 15V power rails, which also supply the integrator M11 and current mirror M50, the positive rail is heavily decoupled, regulated by Q8, and all devices whose currents are likely to disturb the rails are supplied through constant current sources (Q1, Q6, Q9 and Q13).

8.1.2.7 VCO Output

The VCO, M11 and M50 operate from the 15V supplies. M12, M9 and the frequency dividers which follow the VCO, all operate from the in-guard logic supplies of +0V and -15V. The VCO output from Q12 emitter is therefore limited by D1 to logic supply levels. A re-conversion back to 15V levels is accomplished at the input to the integrator M11, as TP31 pulses are negative at M11 input.

D1 is a Schottky hot carrier diode of reverse capacitance approx. 2pF. This avoids distorting the high frequency output squarewaves (for 1MHz output, the VCO oscillates at 4MHz).

The output is fed through R12 to avoid loading the VCO, and as 'VCO O/P' to the frequency dividers at M5-9 *(page 11.6-5)*.

8.1.3 FREQUENCY RANGE DIVIDERS

(Fig 8.3)

As mentioned earlier in *para 8.1.1*, the purpose of the synthesizer is to provide an accurate frequency reference for the quadrature sinewave oscillator. The VCO frequency (signal 'VCO O/P') is input to a series of frequency dividers, whose ratios are set by 'FREQ $R_{2-\varnothing}$', so as to make the dividers generate the selected frequency as 'SYNTH O/P'. FREQ $R_{2-\varnothing}$ is a three-bit word, five of whose codes represent the five frequency ranges.

A second purpose is to clock the Quasi-Sinewave Generator in synchronism with the synthesizer output (and hence with the main quadrature sinewave oscillator output). The synthesizer frequency is a multiple of the Quasi-Sine frequency, except on the 100Hz frequency range, where they are both at the same frequency. Thus the divider ratios are also chosen to generate the correct frequencies for the quasi-sinewave clock, for each frequency range selected.

8.1.3.1 Divider Ratios

(Circuit Diagram 430446 Page 11.6-5)

Binary/BCD Divider M5 is set for binary division by fixing M5-2 and M5-10 at Logic-Ø. Conversely, M1 is set for decimal division by fixing M1-2 and M1-10 at Logic-1.

BCD counter M2 is set to count up, by fixing M2-10 at Logic-1. Its $\overline{\text{CARRY OUT}}$ signal at M2-7 is at 1/10 of its clock frequency, and its Q1 output on M2-6 is at half its clock frequency. Flip-flop M4a is connected to divide its clocks by two.

Multiplexer M6 selects the appropriate source frequency to clock the Quasi-Sinewave generator. In particular, on the 100Hz Range it selects the $\overline{\text{CARRY OUT}}$ from M2, which is subsequently divided by 10 in the quasi-sinewave counter, and returned via J6-51 to be used as SYNTH O/P.

8.1.3.2 Ratio Selection by Frequency Range
(Fig. 8.3 and Table 8.2)

The frequency range selection word FREQ $R_{2\text{-}Ø}$ is decoded by M29 into five range lines $R_{4\text{-}Ø}$. These lines perform the following functions:

a. Switch ranges in the quadrature sinewave oscillator by relays RL1-RL8 selection of integrator capacitors *(page 11.6-1)*;

b. Switch ranges in the Cosine Squarer output filter *(page 11.6-2)*;

c. Adjust the division ratios of Frequency Range Dividers M5 and M1 *(page 11.6-5)* for range R_4 (1MHz Range),

d. Select appropriate outputs from the Frequency Range Dividers *(page 11.6-5)*; and

e. The INHIBIT line turns off the VCO for non-AC functions.

Functions (a) and (b) are described later in *Section 8.2*. In this description we are concerned mainly with functions (c) and (d).

Table 8.2 shows how frequency range switching derives the synthesizer output frequencies by selecting the appropriate outputs from the dividers. Note that except for the 1MHz Range R_4, the ratios of individual dividers are not altered.

On the 100Hz Range $R_Ø$ the overall division ratio of 8000 is achieved as for the 1kHz Range, but with a further division by 10 in the quasi-sinewave counter M11 on the AC Assembly.

On the 1MHz Range, R_4, the division ratio of M5 is changed from 8 to 4. The DP_A inputs M5-5 and M5-6 are primed to Logic-1 and Logic-Ø respectively, whereas on all other ranges the priming is reversed. Range R_4 also alters the division ratio of M1 from 10 to 25, by changing its priming bit-pattern, to correct the quasi-sinewave frequency; but as the synthesizer output is taken through M10-4/3 from M5 output, the adjustment to M1 does not affect the SYNTH O/P frequency.

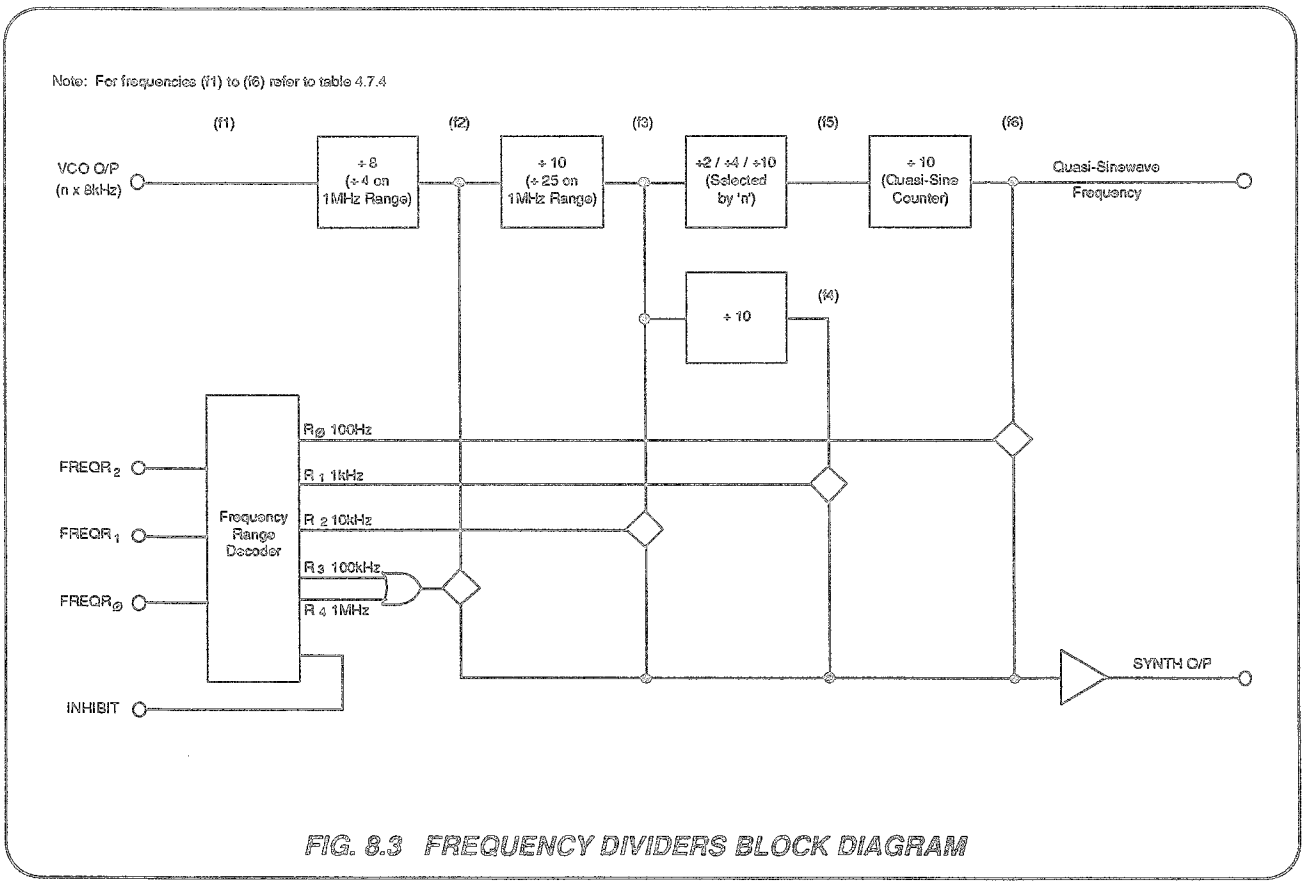

FIG. 8.3 FREQUENCY DIVIDERS BLOCK DIAGRAM

FREQ. RANGE	FREQUENCY DISPLAY Hz	VCO OUTPUT (n × 8kHz) kHz	OVERALL DIVISION RATIO	RELEVANT DIVIDER RATIOS M5	M1	M2	M11* (AC PCB)	QUASI-SINE CLOCK FREQUENCIES (J6-50)*	SYNTHESIZER OUTPUT (J6-52)
100Hz (R0)	10-63 64-127 128-330	80-504 512-1016 1024-2640	8000	8 8 8	10 10 10	10 10 10	10 10 10	Hz 100-630 640-1270 1280-3300	Hz 10-63 64-127 128-330
1kHz (R1)	0.30k-0.63k 0.64k-1.27k 1.28k-3.30k	240-504 512-1016 1024-2640	800	8 8 8	10 10 10	10 10 10		kHz 1.5-3.15 1.6-3.175 1.28-3.3	Hz 300-630 640-1270 1280-3300
10kHz (R2)	3.0k-6.3k 6.4k-12.7k 12.8k-33.0k	240-504 512-1016 1024-2640	80	8 8 8	10 10 10			kHz 1.5-3.15 1.6-3.175 1.28-3.3	kHz 3.0-6.3 6.4-12.7 12.8-33.0
100kHz (R3)	30k-63k 64k-127k 128k-330k	240-504 512-1016 1024-2640	8	8 8 8				kHz 1.5-3.15 1.6-3.175 1.28-3.3	kHz 30-63 64-127 128-330
1MHz (R4)	0.30M-1.00M	1200-4000	4	4				kHz 1.2-4.0	kHz 300-1000

* Quasi-sine counter M11 on the AC Assembly divides VCO output at all frequencies, but contributes to SYNTH O/P only on the 100Hz Frequency Range.

TABLE 8.2 SYNTHESIZER OUTPUT - DIVISION RATIOS

8.1.3.3 Frequency Synthesis for the Quasi-Sinewave Generator

(Fig. 8.3 and Table 8.3)

The 100Hz frequency range uses the quasi-sinewave counter as a divider in deriving its SYNTH O/P frequency. Although not a direct component of the frequency of the SYNTH O/P signal on other ranges, the quasi-sinewave frequency is deliberately derived in the synthesizer, so that the zero-crossings of its waveform can be synchronized at a time when the main sinewave is also crossing zero. (The main sinewave, of course, can be at a high multiple of the quasi-sinewave frequency.)

The quasi-sinewave frequency is held to a maximum of 330Hz (400Hz on the 1MHz range), to limit errors due to high harmonics. The 1MHz frequency range contains only one frequency band, but the other four ranges are each divided into three bands, corresponding to the three most significant bits of the frequency word $FREQ_{8,\emptyset}$.

Table 8.3 illustrates the way that the three bands affect the quasi-sine frequencies. Note that division ratios of 2, 4 or 10, by M2 and M4a, are selected by $FREQ_6$, $FREQ_7$ and $FREQ_8$ at M6 pins 11, 10 and 9 respectively. Frequency range $R_\emptyset$ at M7-2 ensures that on the 100Hz range, the divide-by-10 output of M2 is always selected, regardless of the state of these three bits.

To ensure that the Divide-by-2 outputs of M2 and M4a are locked into the correct phase for quasi-sinewave generation, a synchronizing signal 'CHOP LOCK' is derived from the quasi-sinewave counter '$Q_\emptyset$' output, entering at J6-75. Following DC-restoration from 8V supplies to the normal 0V/-15V logic supplies by C20/D3/R15/M7, the signal is applied to M4a SET input, and M2 RESET input.

For all frequency ranges, the '100-5kHz' quasi-sinewave generator clock is passed to the AC Assembly via J6-50 and the Mother Assembly. This output is level-shifted by Q42, to the 8V supplies which are used in the quasi-sinewave generator circuitry.

The quasi-sinewave generator reset signal '$SYNC_\emptyset$(IG)' (which was transferred into Guard by M2 on the Reference Divider), is input to the Sine-Source Assembly on J6-48 to be similarly level-shifted by M43, before being passed to the AC Assembly via J6-49. This signal, however, is not used on this instrument.

For other details of the quasi-sinewave generator refer to *Section 6.6.*

FREQ. RANGE	FREQUENCY DISPLAY Hz	FREQUENCIES SYNTHESIZED IN SINE-SOURCE ASSEMBLY				QUASI-SINE FREQUENCY (& J7-51) Hz	OUTPUT FREQUENCY Hz
		VCO OUTPUT (n x 8kHz) kHz	DIVIDER RATIOS for QUASI-SINEWAVE M5 M1 M2 M4a	OVERALL DIVISION RATIO	QUASI-SINE CLOCK FREQUENCY (J7-50)		
100Hz (RØ)	10-63 64-127 128-330	80-504 512-1016 1024-2640	8 10 10 – 8 10 10 – 8 10 10 –	800 800 800	Hz 100-630 640-1270 1280-3300	10-63 64-127 128-330	10-63 64-127 128-330
1kHz (R1)	0.30k-0.63k 0.64k-1.27k 1.28k-3.30k	240-504 512-1016 1024-2640	8 10 2 – 8 10 2 2 8 10 10 –	160 320 800	kHz 1.5-3.15 1.6-3.175 1.28-3.3	150-315 160-317.5 128-330	0.30k-0.63k 0.64k-1.27k 1.28k-3.30k
10kHz (R2)	3.0k-6.3k 6.4k-12.7k 12.8k-33.0k	240-504 512-1016 1024-2640	8 10 2 – 8 10 2 2 8 10 10 –	160 320 800	kHz 1.5-3.15 1.6-3.175 1.28-3.3	150-315 160-317.5 128-330	3.0k-6.3k 6.4k-12.7k 12.8k-33.0k
100kHz (R3)	30k-63k 64k-127k 128k-330k	240-504 512-1016 1024-2640	8 10 2 – 8 10 2 2 8 10 10 –	160 320 800	kHz 1.5-3.15 1.6-3.175 1.28-3.3	150-315 160-317.5 128-330	30k-63k 64k-127k 128k-330k
1MHz (R4)	0.30M-1.00M	1200-4000	4 25 10 –	1000	kHz 1.2-4.0	120-400	0.30M-1.00M

TABLE 8.3 QUASI-SINEWAVE FREQUENCY DERIVATION IN FREQUENCY SYNTHESIZER

8.1.3.4 Synthesizer Frequency Analysis

Table 8.4 is provided to allow a complete analysis of the frequencies to be found in the divider circuitry. In part, it duplicates figures from *tables 8.2 and 8.3*.

FREQ. RANGE (NOM)	FREQUENCY DISPLAY Hz	VCO DIVISOR 'n'	f1 VCO OUTPUT (n × 8kHz) kHz	f2 M5 OUTPUT (f1 – 8) kHz	f3 M1 OUTPUT (f2 – 10) kHz	f4 M2 OUTPUT (f3 – 10) Hz	f5* M6 OUTPUT (M6-3) Hz			f6 J6-51 INPUT (f5 – 10) Hz
							M6 Input Channels and Division Ratios			
							$X_{\emptyset}$ (f3 – 2)	X_1 (f3 – 4)	$X_{2\text{-}7}$ (f3 – 10)	
100Hz (RØ)	10-63 64-127 128-330	10-63 64-127 128-330	80-504 512-1016 1024-2640	10-63 64-127 128-330	1.0-6.3 6.4-12.7 12.8-33.0	100-630 640-1270 1280-3300			100-630 640-1270 1280-3300	[10-63] [64-127] [128-330]
1kHz (R1)	0.30k-0.63k 0.64k-1.27k 1.28k-3.30k	30-63 64-127 128-330	240-504 512-1016 1024-2640	30-63 64-127 128-330	3.0-6.3 6.4-12.7 12.8-33.0	[100-630] [640-1270] [1280-3300]	1500-3150	1600-3175	1280-3300	150-315 160-317.5 128-330
10kHz (R2)	3.0k-6.3k 6.4k-12.7k 12.8k-33.0k	30-63 64-127 128-330	240-504 512-1016 1024-2640	30-63 64-127 128-330	[3.0-6.3] [6.4-12.7] [12.8-33.0]	100-630 640-1270 1280-3300	1500-3150	1600-3175	1280-3300	150-315 160-317.5 128-330
100kHz (R3)	30k-63k 64k-127k 128k-330k	30-63 64-127 128-330	240-504 512-1016 1024-2640	[30-63] [64-127] [128-330]	3.0-6.3 6.4-12.7 12.8-33.0	100-630 640-1270 1280-3300	1500-3150	1600-3175	1280-3300	150-315 160-317.5 128-330
1MHz (R4)	Hz 0.30M-1.00M	'n' 150-500	kHz 1200-4000	(f1 – 4) kHz [300-1000]	(f2 – 25) kHz 12-40	(f3 – 10) Hz 1200-4000			1200-4000	Hz 120-400

TABLE 8.4 SYNTHESIZER DIVIDERS - FREQUENCY ANALYSIS

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8.2 QUADRATURE SINEWAVE OSCILLATOR

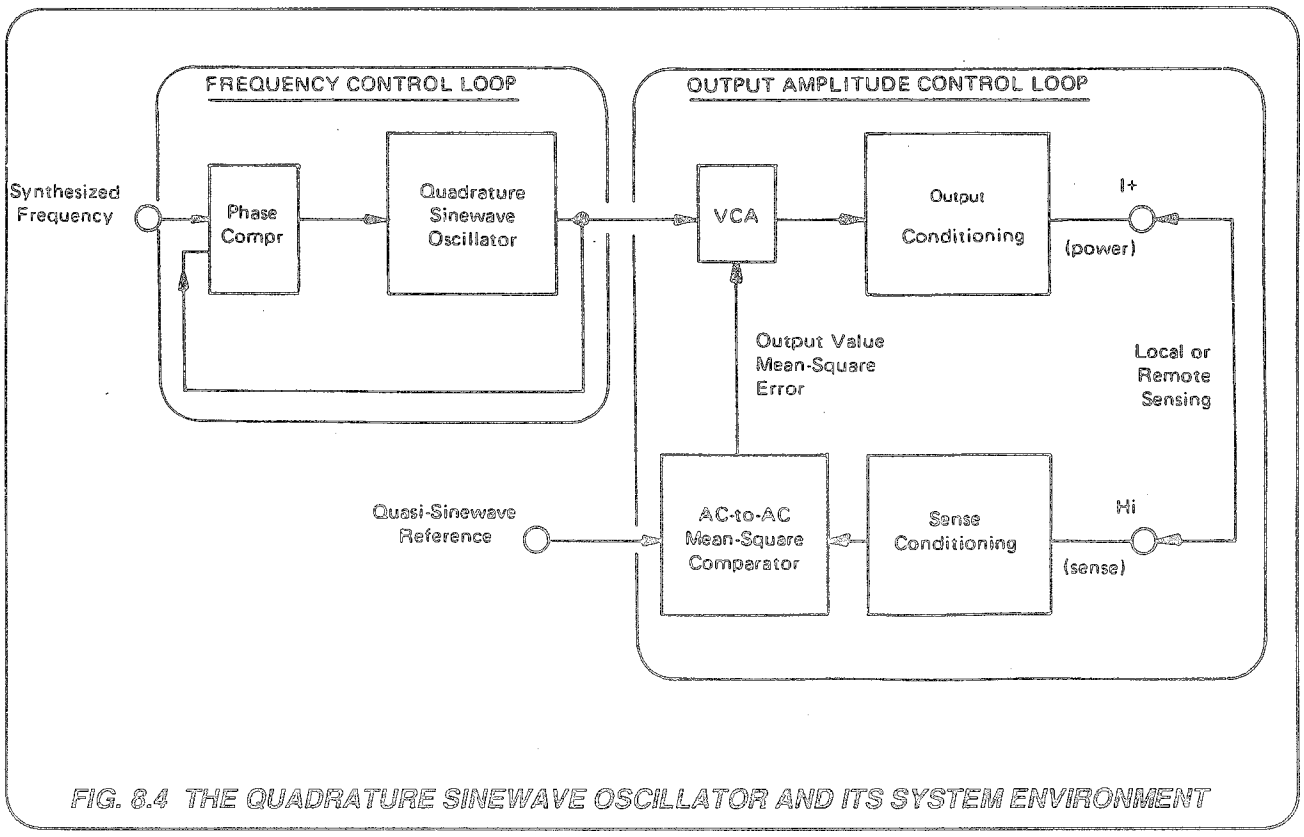


FIG. 8.4 THE QUADRATURE SINEWAVE OSCILLATOR AND ITS SYSTEM ENVIRONMENT

8.2.1 PURPOSE and ENVIRONMENT

(Fig. 8.4)

The purpose of the oscillator is to define the amplitude-stability, purity and frequency of the sinusoidal output of the instrument on all ranges. Its output is of sufficient constant amplitude to drive the subsequent signal-conditioning circuitry.

After originating in the oscillator, the sinewave amplitude is accurately defined in two output- sense loops, using a low-distortion VCA as control element. The sinewave is set close to its demanded value by analog conditioning in the output circuits.

The output voltage is sensed, attenuated to its 1V Range equivalent, then its mean-square value is compared against that of the quasi-sinewave reference. The difference is converted into a DC error voltage which corrects the output by adjusting the VCA gain.

As the purity and amplitude-stability of the output sinewave depend substantially upon its source, a high quality oscillator is necessary. A 'quadrature' (dual-integrator) circuit is chosen for two main reasons:

- This arrangement allows extensive phase and amplitude controls to be applied, to establish the required high specification.
- Its natural frequency can be easily programmed by electrical selection of its component values.

The oscillator is approximately tuned by selection of circuit constants using the two CPU-derived binary words '$FREQ\ R_{2\text{-}\emptyset}$' and '$FREQ_{8\text{-}\emptyset}$'. These also accurately define the crystal-sourced frequency of the Digital Frequency Synthesizer output, to which the oscillator is phase-locked. Thus the output sinewave frequency accuracy is held to 100ppm.

8.2.2 SIMPLE QUADRATURE OSCILLATOR

8.2.2.1 Basic Circuit

(Fig. 8.5)

The circuit consists of two RC integrators and an inverter, connected in a positive feedback loop. The nominal phase-shift around the loop is 360° (actually 720°: 270° in each integrator, 180° in the inverter).

Assuming perfect integrators, matched components and an inverter gain of exactly -1, this circuit will undergo stable oscillation at a frequency given by:

$$w = 1/R.C$$

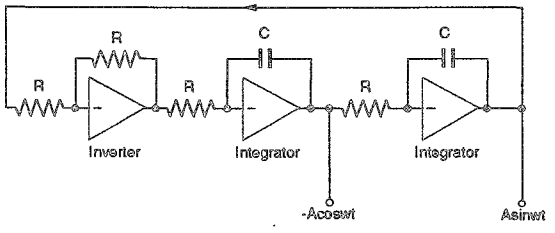


FIG. 8.5 BASIC QUADRATURE OSCILLATOR

8.2.2.2 Inadequacies of the Basic Circuit

(Figs. 8.5 and 8.6)

For an unrefined practical implementation of the basic circuit, the loop gain and phase response would be as shown in *Fig. 8.6.*

The two main conditions for stable oscillation at constant amplitude are: exactly unity loop gain, and exactly 360° (or multiple of 360°) of loop phase-shift; so the circuit of *Fig. 8.5* clearly does not satisfy these conditions. Without some attempt to control gain and phase, the loop would be either over- or under-damped, so oscillations would either die away or increase in amplitude until limited by the supply rails.

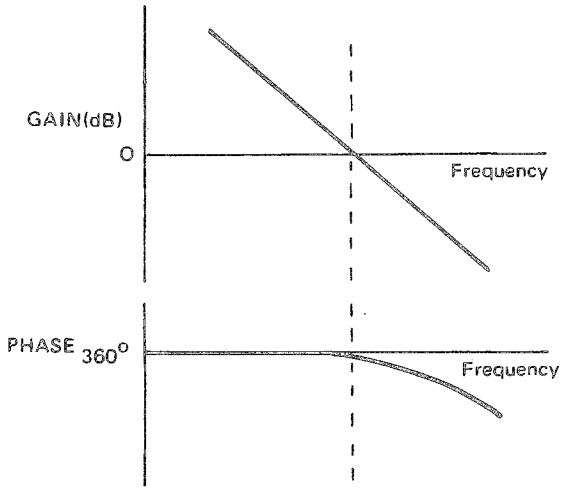


FIG. 8.6 GAIN AND PHASE RESPONSE OF PRACTICAL CIRCUIT

8.2.3 PRACTICAL QUADRATURE OSCILLATOR

(Fig. 8.7)

The method chosen to refine the simple circuit corrects the loop phase-shift to exactly 360° using a feedback signal. Furthermore, it is arranged that this signal is correct only at a given output amplitude, so the amplitude of stable oscillation is defined. In *Fig. 8.7* the correction circuit is added.

8.2.3.1 Phase Correction

The loop phase is corrected by introducing a small cosine term (B.cosωt) to be summed with the sine feedback (A.sinωt) at the input to the inverter. The resultant output of the inverter is thus given by:

$$V(t) = -(A.\sin\omega t + B.\cos\omega t)$$
$$= M.\sin(\omega t + \phi) \quad \text{------ } 1$$

where $M = \sqrt{(A^2 + B^2)}$

and $\sin\phi = B/M;$

$\cos\phi = A/M.$

Hence $\phi = \tan^{-1}(B/A).$

and for B«A: $\phi \approx B/A$ ------ *2*

The ϕ term represents an additional phase shift in the inverter, which by suitable scaling can be made equal to the phase error in the basic oscillator loop. Scaling is achieved by multiplying A.cosωt by the DC amplitude error (A^2-I_{REF}), as described opposite.

8.2.3.2 Constant Amplitude Control

The above method of phase correction plays its part in controlling the output amplitude. With both sine and cosine terms available, a DC analog of the sinusoidal output amplitude can be obtained utilizing the identity:

$$\sin^2\omega t + \cos^2\omega t = 1.$$

Equal-amplitude sine and cosine outputs are squared in 4-quadrant multipliers. Their squares are summed to generate amplitude feedback in the form:

$$A^2.\sin^2\omega t + A^2.\cos^2\omega t$$

$$= A^2(\sin^2\omega t + \cos^2\omega t)$$

$$= A^2.$$

This method therefore expresses the square of the output amplitude as a DC current analog, from which is subtracted a constant DC reference current 'I_{REF}'.

The difference current 'A^2-I_{REF}' is taken as the amplitude error, which defines the fraction 'B' of the cosine term to be fed back to the inverter as 'B.coswt'.

In a perfect oscillator, this 'cos' feedback would be driven to zero. But in any practical circuit, some small remnant of B.coswt persists at the correct loop phase-shift, correcting the loop gain to within the stability specification.

Acting thus together, the combined feedbacks correct both loop gain and phase simultaneously. The method of amplitude correction prevents the appearance of AC components in the amplitude error signal, thus avoiding unacceptable levels of harmonic distortion due to the cosine multiplier.

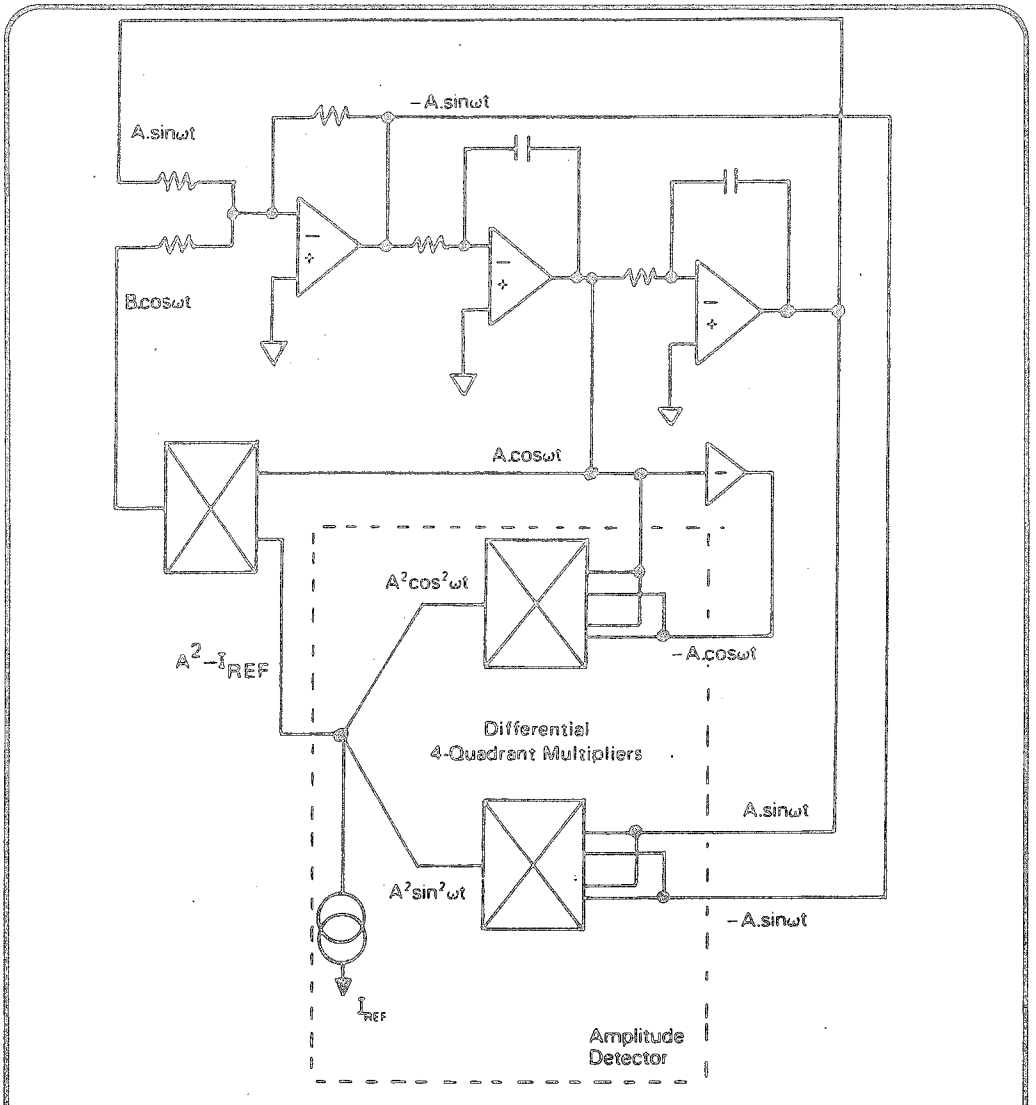


FIG. 8.7 CORRECTED QUADRATURE OSCILLATOR

8.2.4 FREQUENCY CONTROL

Section 8.1 describes frequency generation in the Frequency Synthesizer. Binary control words computed by the CPU represent user-selections of FREQUENCY RANGE and FREQUENCY. These adjust frequency division ratios in the feedback circuit of a phase-locked loop, and division ratios in subsequent frequency dividers, to set the Synthesizer output signal 'SYNTH O/P' to the selected frequency. Stability and accuracy are assured by a crystal-sourced reference of 16kHz.

8.2.4.1 Coarse Adjustment

The Sinewave Oscillator is already approximately tuned to the selected frequency by the two binary control words, which select from weighted values of integration capacitance and resistance:

- **Frequency ranges** are selected by control word FREQ R_{2^0}, which controls relays to change the values of integrator capacitance.
- **Frequencies within a range** are selected by the control word $FREQ_{8^0}$, which controls FETs to change the values of integrator resistance.

8.2.4.2 Fine Adjustment

(Fig. 8.8)

The oscillator's output is converted into a squarewave and applied as 'signal' to the phase comparator of a second phase-locked loop. The Synthesizer output signal 'SYNTH O/P' is input as reference frequency to the same comparator. The difference is integrated to produce a DC phase error signal, which is applied to control the gain of the inverter stage of the oscillator.

It can be shown that the actual operating frequency is a function of the inverter gain. In the frequency domain, the oscillator loop transfer function is given by:

$$G \times (\omega_\phi/s) \times (\omega_\phi/s)$$

where G is the inverter gain,
ω_ϕ is the unity-gain frequency
$s = j.\omega$, where ω is the actual frequency of operation.

For stable oscillation, the loop transfer function must equal $1\angle 0$.

$$\text{Hence } G.\omega_\phi^2/s^2 = 1\angle 0$$

$$\text{Therefore } G.\omega_\phi^2 = j^2.\omega^2 = -1.\omega^2$$

$$\text{and } \omega = -\omega_\phi.G^{1/2}$$

Thus by adjusting the gain of the inverter, the phase error signal from the comparator exerts fine control of the oscillator frequency. This phase-locks the oscillator to the Frequency Synthesizer.

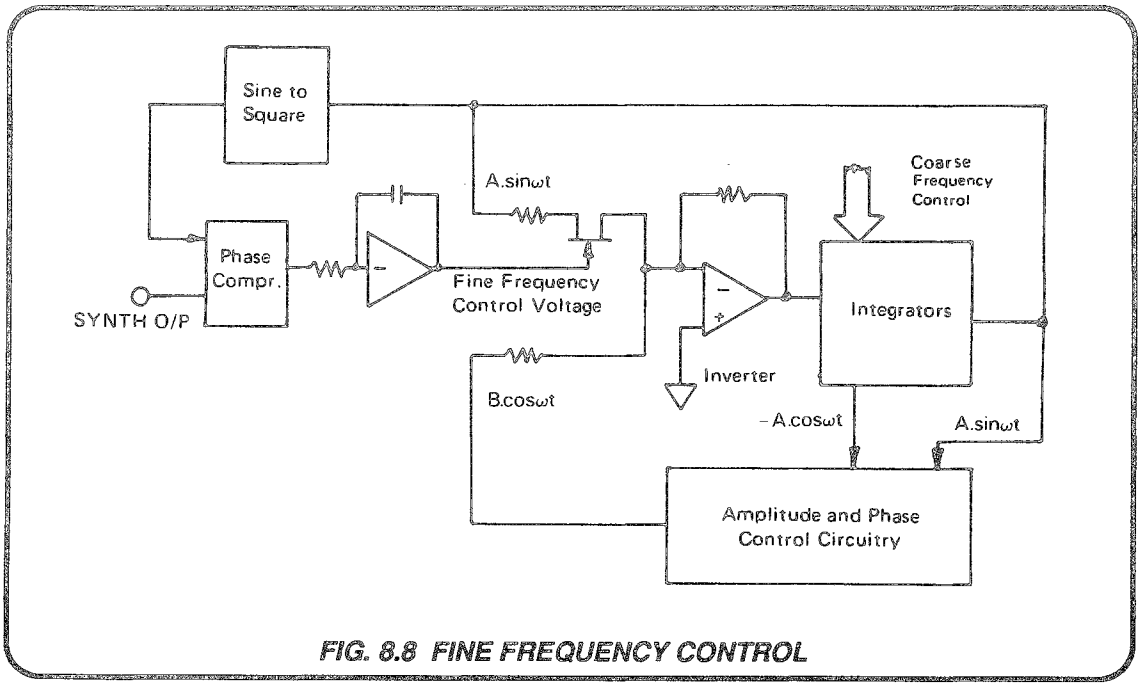


FIG. 8.8 FINE FREQUENCY CONTROL

8.2.5 OSCILLATOR OUTPUT

The A.sinωt signal is inverted and buffered out to provide the drive to the output loop VCA. The buffer feedback resistors are positive TC thermistors which compensate for the TC of the VCA input FETs *(refer to section 9)*.

8.2.6 MAIN INTEGRATORS

(Circuit Diagram 430446 page 11.6-1)

The cascaded integrators consist of M19 and M30 together with their input resistors and feedback capacitors. Both circuits are identical in operation, although some slight differences in implementation exist. Adjustments to the natural oscillation frequency are made by switching the integrator time constants.

8.2.6.1 Frequency Range Switching

The feedback capacitors are selected by the binary control word '$FREQ_{R2\text{-}\phi}$'. This is decoded into five lines $_{R4\text{-}\phi}$ *(page 11.6-5)*, each representing a frequency range. The capacitors for R_4 (1MHz) are fixed, one other set being added in parallel when its range is selected. Relays RL1 to RL8 perform the switching.

8.2.6.2 Frequency Increments

The integrator input resistors are connected in a binary-weighted ladder network, the total input resistance depending on the pattern of FET conduction. Each FET is turned on by its corresponding binary digit in the frequency control word $FREQ_{0\text{-}\phi}$ (appearing as $A_{3\text{-}\phi}$ and $B_{3\text{-}\phi}$ at the FET gates).

The least-significant bits, representing low frequencies, control the highest-value resistors at the base of the ladder. The most-significant bits, which represent the highest frequencies, control the lowest-value resistors at the top.

Any user-selected frequency in a given frequency range is thus represented by a bit-pattern in the control word, which is repeated in the FET conduction pattern and resistance selection at the input of both integrators.

8.2.6.3 Slew Rate and Protection

Emitter-followers at the outputs of the integrator operational amplifiers allow the high slew-rates necessary to be achieved, by buffering any loading effects. The diode clamp networks between output and input prevent latch-up by imposing unity-gain feedback when output peaks exceed approximately 5V.

8.2.6.4 Output Offset Control

The amplitude detector circuit squares the outputs from both integrators. It is therefore important that their DC offset voltages are not included in the squaring computation.

The 'Cosine' offset is removed by adjustment of R50 at the non-inverting input of M30, and the 'Sine' offset by R49 at the input of inverter M15. This latter adjustment removes the combined offsets of M15 and M19. (At manufacture, and after any replacement of major board components, the controls are iteratively adjusted for minimum AC fundamental component in the DC amplitude control signal 'V_G' at link 'B'.)

8.2.7 INVERTER STAGE

The inverter completes the positive feedback loop of the basic oscillator. The very high bandwidth device used for M15 is compensated by C27, and its TO8 case is grounded.

As mentioned earlier, its DC input offset is adjusted by R49 to null the sine DC offset.

8.2.7.1 Gain Control

The inverter has three inputs:

a. A.sinωt from the second integrator, the basic oscillator feedback loop.

b. B.cosωt from the Amplitude correction loop.

c. 'FREQ ERROR', a DC current which alters the inverter's input resistance (and hence its gain) by controlling FET conduction, phase-locking the oscillator to the synthesizer output frequency *(refer to para 8.2.4.2)*.

Inputs (a) and (b) [A.sinωt and B.cosωt] are summed as currents at the inverting input. The amplitude of the B.cosωt signal is determined by the action of the amplitude control loop, described in *sections 8.2.8 and 8.2.9*.

Input (c) controls the gain of the inverter. The A.sinωt is applied via two input resistors R28 and R41 in series. R28 is shunted by the two FETs of Q29, whose the source-drain resistance is altered by the 'FREQ ERROR' current via current-mirrors M16 and M18.

Two FETs in series are required for the amplitude levels reached by A.sinωt. R41 is selected to account for differing 'on' resistances of different batches of FETs. This input circuit is a scaled-down version of that employed for the VCA in the main output loop, details of which appear in *Section* 9. A description of the action of the frequency tracking loop follows at *para 8.2.7.2*.

8.2.7.2 Frequency Tracking - General

As stated in *para 8.2.4.2*, the oscillator's output is applied to the comparator of a phase-locked loop. The Synthesizer output is input as reference frequency to the same comparator. The phase-difference pulse train from the comparator is integrated to produce a DC phase error signal, which is applied to control the gain of the inverter stage of the oscillator. This exerts fine control of the oscillator frequency, tracking the Synthesizer frequency.

8.2.7.3 Tracking Comparator

(Circuit Diagram 430844 Page 11.7-6)

After buffering and invertion by M47 on the Sine-source Assembly *(page 11.6-1)*, the oscillator A.sinwt output is passed to the AC Assembly via J6-45 and J7-45.

On the AC Assembly, the sinewave is converted into a squarewave by Schmitt bistable Q32/Q33, and level-shifted to logic supply levels of 0V and -15V by D25/Q28. Q28 provides a current-limited load for maximum gain, while D24 and D25 prevent voltage saturation of Q32. Q23 buffers the resulting squarewave into the phase comparator input at M30-6.

The slower zero-crossings at the lowest frequencies could be susceptible to HF noise, so this is filtered, on the 100Hz frequency range only, by Q27 and C48.

The 'SYNTH O/P' squarewave, at the demanded frequency, is transmitted from the Sine-source Assembly at low (1V Full Range) level. This holds the maximum slew rate to a value which avoids inducing interference in other internal circuits. Q20 and Q21 amplify the signal to the CMOS logic levels of 0V and -15V required by the comparator input at M30-3.

Note that current steering is used between Q32 and Q33, and between Q20 and Q21. Also, a constant current source Q22 provides Q23 emitter current. These measures prevent the fast switching edges in the schmitt and amplifier circuits from injecting spikes into the supply rails.

Phase-comparator output M30-5 consists of positive pulses (0V) when the oscillator lags the synthesizer, or negative (-15V) when the oscillator leads. When both are in phase, M30-5 is at high impedance.

At integrator M31 input, zener diode D30 holds the non-inverting input at -6.4V; so for in-phase signals into the comparator, the inverting input seeks the same level. The integrator tends to hold its voltage level (with very slight drift due to capacitor leakage but limited to -9.8V by D32/D33). When the oscillator output lags the synthesizer output, the positive-going comparator pulses are integrated to drive M31-6 slowly more negative. When the phase of the oscillator leads, the integrator output becomes more positive.

The phase control loop seeks to phase-lock the two inputs to the comparator. If they are in phase, the comparator output is at high impedance ('TRISTATE'). In this condition the integrator capacitors C53 and C56 have no charge or discharge path, so M31's extremely high gain maintains a constant charge on the capacitors. The constant voltage on Q37 base maintains a constant 'FREQ ERROR' current.

Q37 appears to be an open-collector amplifier. However, its collector current passes via J7-44 and J6-44, into the two current-mirrors at the input to the oscillator inverter on the Sine-source Assembly *(page 11.6-1)*, and thence to the -15V rail.

With constant input current, the mirrors continue to draw the same output current from the AN4 bias network for Q29, so the frequency of the dual-integrator oscillator remains constant. Thus the loop stabilizes only when the oscillator frequency is in phase with (and therefore at the same frequency as) the Frequency Synthesizer output.

The overall action is for a lagging oscillator (frequency lower than the synthesizer) to increase the DC current flowing into the two current mirrors, and vice-versa if the oscillator leads. The two inputs to the comparator are in phase when the sinewave output from the oscillator is at the synthesizer frequency.

Any disturbance in the loop will generate corrections to restore zero phase difference at the inputs of M30. Frequency deviations are therefore detected at an early stage as phase changes, giving a measure of 'phase advance' correction.

8.2.8 SINEWAVE AMPLITUDE DETECTOR

The method of amplitude measurement relies on the identity '$\sin^2wt+\cos^2wt = 1$' to convert AC output signals from the oscillator into a representative DC signal.

Squaring Asinwt and Acoswt:

$$A^2\sin^2wt = (A^2 - A^2\cos2wt)/2,$$
$$A^2\cos^2wt = (A^2 + A^2\cos2wt)/2,$$

The AC waveforms of $A^2\cos2wt$ and $A^2\sin2wt$ are inverted versions of each other, at twice the original frequency, and both are symmetrical about the DC mean value of $A^2/2$.

By summing the two, the AC waveforms are eliminated, leaving a DC signal, A^2, representing the square of the amplitude.

In the Amplitude Detector, the Vsin and Vcos outputs from the oscillator are squared electronically and summed as a differential current I^2. This is compared with a constant DC reference current I_{REF} to generate the error current ($I^2 - I_{REF}$), which is used to derive an amplitude error voltage 'V_G'. This is filtered and passed to the Amplitude Control circuits *(page 11.6-1)*.

V_G is driven to zero by the action of the amplitude control loop, so that $I^2 - I_{REF} = 0$, and thus $I^2 = I_{REF}$. The loop therefore stabilizes only when the two are equal, and at a constant amplitude.

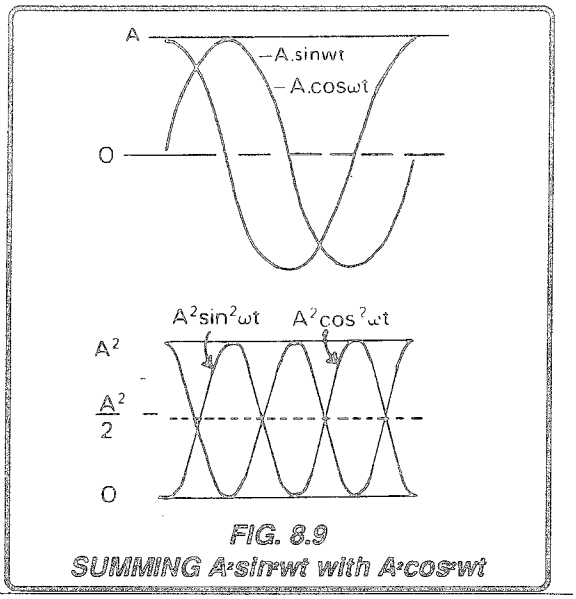


FIG. 8.9
SUMMING A²sin²wt with A²cos²wt

8.2.8.1 Squaring Circuit Inputs

(Circuit Diagram 430446 Page 11.6-1)

Vcos and Vsin are squared independently in a pair of differential four-Quadrant multipliers, each with two identical differential inputs.

The Sine Squarer receives Vsinwt from the second integrator M30 (Q44 emitter), and -Vsinwt from the main inverter (M15-11).

As +Vcoswt is the only natural cosine output from the oscillator, the -Vcoswt signal is derived by inversion in M31. These are both fed as inputs to the Cosine Squarer.

8.2.8.2 Cosine Squarer

(Circuit Diagram 430446 Page 11.6-2)

Isolating the Cosine circuit alone as an example, there are two differential inputs. One is applied across M34 pins 13 and 16, and the other across pins 6 and 10.

The multiplying action of the squaring circuitry relies on the exponential transconductance between a transistor's base voltage and its emitter-collector current:

$$I_c \text{ is proportional to } \exp(V_{be})$$
$$\text{so } V_{be} \text{ is proportional to } \mathrm{Ln}(I_c)$$

The difference between the currents in M34-1 and M34-14 collectors is linearly proportional to Vcoswt (due to M34 emitter resistors AN15). The currents are drawn from the supply through Q55 (which is connected as two matched diodes), but because of the exponential transconductance, Q55 base-emitter voltages increase logarithmically with increase of emitter current. Therefore the differential voltage at Q56 and Q57 bases due to Q55 emitter currents is logarithmic:

$$(V_{Q55\text{-}4} - V_{Q55\text{-}3}) \text{ is proportional to } \mathrm{Ln}(V.\mathrm{coswt})$$

The difference between the currents in M34-9 and M34-7 collectors is also linearly proportional to Vcoswt (due to other M34 emitter resistors AN15). But each collector current is divided between the two halves of the dual transistor in its collector circuit, regulated both by the dual transistor's exponential transconductance, and by its logarithmic differential base voltage.

The combined effect of these two factors is similar to the mathematical operation of multiplying by adding logarithms: a term is produced in each Q56 and Q57 collector current, proportional to the linear product of the two input voltages.

By cross coupling the collectors of Q56 and Q57 as shown, other constant terms are suppressed, and the difference between the currents drawn from AN15-7/8 and AN16-9/10 is proportional to:

$$\mathrm{Vcoswt} \times \mathrm{Vcoswt}$$

The inputs are equal, so the differential output current is proportional to $V^2\cos^2 wt$.

8.2.8.3 Sine Squarer

The Sine Squarer behaves in the same way, producing a differential current in its collector loads proportional to $V^2\sin^2 wt$.

8.2.8.4 Cos², Sin² and I_{REF} Summing

In this application, the currents from both Sine and Cosine Squarers are combined in common loads. The voltages developed across the loads will therefore also differ by an amount proportional to the expression $V^2\cos^2 wt + V^2\sin^2 wt$. Thus if a reference current was not superimposed, and utilizing the well-known identity '$\sin^2 + \cos^2 = 1$', a DC voltage would exist between TP9 and TP10 (TP9 positive), equal to:

$$KV^2(\cos^2 wt + \sin^2 wt) = KV^2$$

where 'K' is a constant at constant temperature, dependent upon identical circuit values in both squarers, and 'V' is the amplitude of both sine and cosine outputs from the oscillator.

However, a reference current is superimposed. The DC current I_{REF} is drawn through the 1kohm load AN15 by M40 (pin 2), reducing the positive value of TP9 voltage to ($KV^2 - KV_{REF}$) with respect to TP10. (The reference current is established at a value which includes the scaling factor 'K', by D26 and R91. The value of R91 for correct oscillator amplitude is determined at manufacture). M34 is connected as a diode to compensate for M40 V_{be} temperature drift.

Voltage $K(V^2 - V_{REF})$ is applied to the input of M35a, the unity-gain Summing Amplifier. M35a is connected to remove any common mode present at its input, so at TP11, $K(V^2 - V_{REF})$ is referred to common 2A. At this point it can be recognized as the Amplitude Error Voltage. Moreover, the amplitude loop adjusts the oscillator outputs to drive the error voltage to zero, so the action of the loop also drives V^2 to equal V_{REF}.

8.2.8.5 Filtering

Because components cannot be matched exactly, some small differences can exist between the $\sin^2$ and $\cos^2$ terms. Such differences appear in V_G as the fundamental and second harmonics of the oscillator frequency. These are limited by filtering in the filter formed by M35b and its associated circuit.

It would be possible to set a single low-pass bandwidth for all ranges, but as this would need to filter down to 20Hz for the 100Hz range, it would also impose inconveniently long settling times for the higher frequency ranges. The low-pass bandwidth of the filter is therefore switched between frequency ranges by the $R_{4\text{-}\beta}$ signals decoded from FREQ $R_{2\text{-}\beta}$ in the synthesizer *(page 11.6-5)*.

The frequency range signals select the appropriate feedback components, by conduction of only one FET from Q47-Q52 per range. (Q48 is not used).

The filter output is the oscillator amplitude DC error signal 'V_G', limited to a maximum of approximately 6V by the action of back-to-back clamp diodes D24 and D25. V_G passes via link B to the 'Amplitude Control' circuitry *(see page 11.6-1)*. The value of V_G determines the fraction, and its polarity the phase, of the V.coswt signal which is to be added to V.sinwt at M15 input.

8.2.9 AMPLITUDE CONTROL IMPLEMENTATION

(Circuit Diagram 430446 Page 11.6-1)

Before describing the control circuitry, it is useful to review the various controls imposed on the oscillator *(see Figs. 8.4 and 8.7)*:

a. Frequency control by phase-locked loop to the frequency of the synthesizer output (albeit with a constant phase lag). This is effected by controlling the gain of the inverter stage of the oscillator. (Input resistance of M15 is changed by adjusting the conduction of FETs Q29.)

b. Phase control to establish exactly 360° loop phase-shift by injecting a small amount of Vcosωt into the oscillator inverter input (via R29).

c. Amplitude control by adjusting the sense and amplitude of V.cosωt added to V.sinωt, so that the loop gain is exactly unity at 360° loop phase-shift, at a constant output amplitude, and at the synthesizer frequency. (M23 gain is adjusted by varying the attenuation of its input signal, using FETs $Q41_a$ and $Q41_b$.)

Amplitude error is corrected by adding a controlled fraction of either Vcosωt or -Vcosωt to the Vsinωt feedback being applied to the main inverter M15. A push-pull control circuit is employed in order to adjust both amplitude and sense. Vcosωt is input from Q31 emitter to R71, and its inverse is input to R70 from the output of M31, (which also provides the -Vcosωt input for the cosine squarer).

8.2.9.1 V.cosωt Amplifier - M23

M23 is connected as a summing VCA, with a fixed feedback resistor R53. Vcosωt and -Vcosωt are applied to opposite ends of its balanced input resistor chain R71, R65, R64 and R70. The center of the chain is the virtual ground of M23, so if the 'on' resistances of $Q41_a$ and $Q41_b$ are equal, the balance is not disturbed and M23 output voltage is zero.

When the Loop-gain Error is zero ($V_G = 0V$), the static conditions set approx. -3V bias on both FETs (depletion mode) to reduce crossover distortion. The FET gates are also bootstrapped by M24 and M25 to half the AC voltage between source and drain.

The DC conditions are:

$Q41_a$	Q46 emitter	- -0.75V
	M26 I_{in}	- 150µA
	M26 I_{out}	- 300µA
	$Q41_a$ V_{gs}	- -1.5V
$Q41_b$	M32-6	- 0V
	Q45 emitter	- -0.75V
	M27 I_{in}	- 150µA
	M27 I_{out}	- 300µA
	$Q41_b$ V_{gs}	- -1.5V

Amplitude Error:

	M23-6	- zero

The Amplitude Error adjusts the 'on' resistance of $Q41_a$ and $Q41_b$ differentially, due to the inverter M32 in the side feeding $Q41_b$. In the case of a positive V_G of about 0.5V:

$Q41_a$	Q46 emitter	- -0.25V
	M26 I_{in}	- 50µA
	M26 I_{out}	- 100µA
	$Q41_a$ V_{gs}	- -0.5V (more conduction)
$Q41_b$	M32-6	- -0.5V
	Q45 emitter	- -1.25V
	M27 I_{in}	- 250µA
	M27 I_{out}	- 500µA
	$Q41_b$ V_{gs}	- -2.5V (less conduction)

The output voltage at M23-6 is in the same phase as Vcosωt, increasing with larger amplitude error.

For a negative V_G, M23-6 output voltage assumes the same phase as the -Vcosωt signal, increasing with larger amplitude error.

Transistors Q45 and Q46 act as voltage-to-current converters to drive the 'x2' current mirrors M27 and M26. Voltage reference diodes D20 and D22 provide the crossover bias. D21 and D23 provide clamping when Q45 and Q46 bases are driven positive, preventing V_{be} breakdown.

M23 output (now recognized as 'B.cosωt') is summed with the basic oscillator feedback (Vsinωt) at the main inverter input (M15-5). When the amplitude is correct, and the loop phase is exactly 360°, M23 output is zero and does not inject any 'cos' component into the loop.

If the loop gain or phase is in error, then the squarers' output current is not equal to the reference current, V_G is not zero, and a small amount of cos component is fed into the loop. This adjusts the loop phase and gain to correct the oscillator amplitude.

8.3 EXTERNAL FREQUENCY LOCK

The External Frequency Lock allows the instrument output to be synchronized with an external reference frequency of either 1MHz or 10MHz (a tolerance of ±1% on these frequencies is specified).

The main use envisaged for this facility is for a user to improve on the ±100ppm frequency accuracy of the instrument, by locking the internal frequency synthesizer to a customer's own frequency standard.

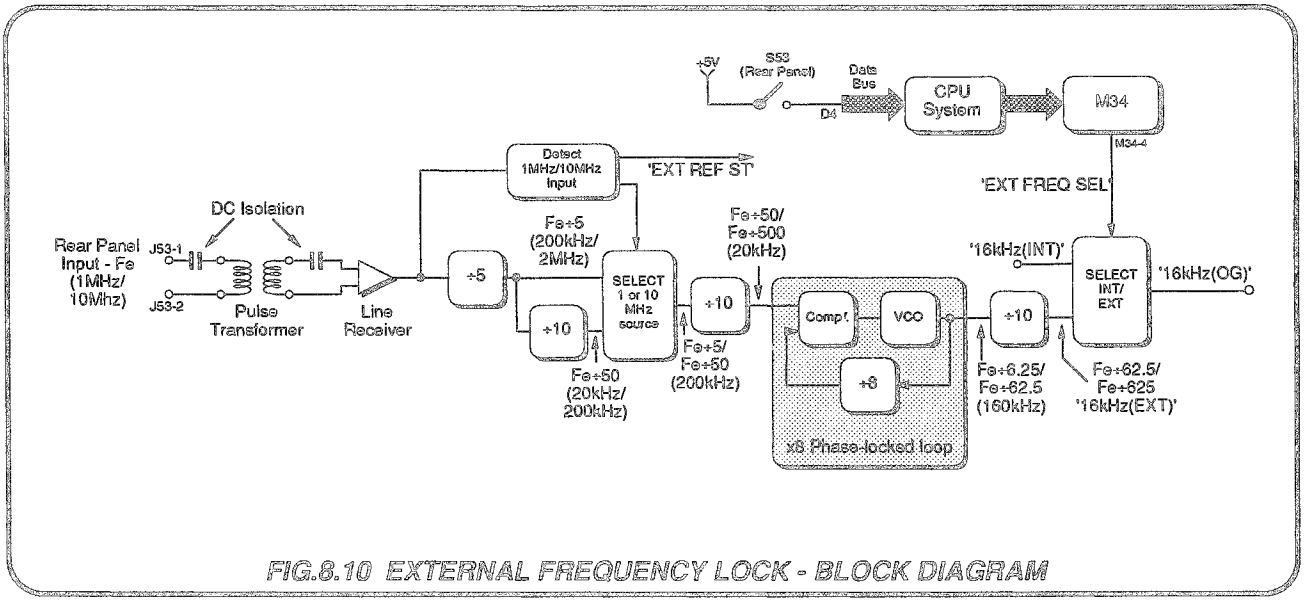


FIG.8.10 EXTERNAL FREQUENCY LOCK - BLOCK DIAGRAM

8.3.1 INTRODUCTION

The output sinewave frequency is synthesized in the Sine-Source assembly, normally synchronized to an internally-generated reference frequency of 16kHz. To lock the output to an external reference, it is necessary only to divide the frequency of the reference down to 16kHz and use this instead of the internal reference. The circuitry described in this sub-section is shown in block form in *Fig. 8.10* and carries out the following functions:

- Isolates, limits and buffers the input reference signal to TTL levels.
- Divides the input frequency 'Fe' by 5 and then by 10 *(Fig. 8.10)*.
- Detects whether the Fe is 1MHz or 10MHz; from this it sets the selector to choose either its ÷5 or ÷50 input, to give an output of 200kHz. The detector sets the status signal 'EXT REF ST' to Logic-1 whenever either of the two signals is present.
- Divides the selector output by 10, then multiplies by 8 in a phase-locked loop, finally dividing by 10 again to 16kHz to give the signal '16kHz(EXT)'.
- Selects either '16kHz(INT)' or '16kHz(EXT)' in response to the position of the Rear Panel switch S53, and to the presence of a 1MHz or 10MHz External Reference signal. The selected signal '16kHz(OG)' is transferred into guard by opto-isolator M3 on the Reference Divider assembly, and thence as 'REF FREQ' to the digital frequency synthesizer on the Sine Source assembly.

8.3.2 EXT REF SIGNAL INPUT

(Circuit Diagrams: 430830 Page 11.17-2; 430604 Page 11.16-4; 430648 Page 11.3-4.)

The External Reference signal of 1MHz or 10MHz enters the instrument via pins 1 (Hi) and 2 (Lo) of Rear-Panel connector J53 on the Interconnection assembly *(page 11.17-2)*. It is transferred via J18 and J3 on the Mother assembly *(page 11.16-4)* to the buffer input circuit on the Analog Interface assembly *(page 11.3-4)*.

C59 and R1 remove any DC components of the signal; and R15, D1 and D2 limit its excursions to approximately ±0.7V before it is applied to the pulse transformer T1.

The output from T1 drives line receiver M9, C62 setting the DC offset to zero, and R16 providing some noise-immunity.

8.3.3 DIVISION CHAIN

8.3.3.1 '÷5' and '÷10' Counters M11

The line receiver output at TP24 clocks the ÷5 section of M11 counter. Its frequency is reduced to either 200kHz (for 1MHz input) or 2MHz (10MHz input), and this signal is used to clock the second (÷10) section of M11. This section (and the other two ÷10 counters M28) is connected as a 'bi-quinary' divider to establish a symmetrical mark/space ratio. The frequency at M11-13 is either 20kHz (for 1MHz input) or 200kHz (10MHz input). The outputs from both counters are fed to the dual 4 into 1 line selector M18, which always chooses the 200kHz signal.

8.3.3.2 'EXT FREQ SEL'

When S53 on the rear panel is closed to select External Reference, +5V from S53 enters the Digital assembly at J2-25 *(page 11.2-2)*, setting line D2 on the Data bus to Logic-1 each time that M36 is enabled by any IRQ (ie. every 8ms in response to the internal signal RTC IRQ *para 6.1.2.6*). The CPU passes the information to the External Reference Buffer on the Analog Interface assembly via the Precision Divider Input Data Latches. The state of S53 is repeated at M34-4 *(page 11.3-1)* and input to M18-2 (B) to set M18 outputs.

8.3.3.3 1MHZ/10MHz Detector M10

The state of the other input to M18 at M18-14 'A' depends on the frequency of the external reference signal at TP24, which is used to clock M10-2 'B'. Each positive-going edge triggers the first (330ns) monostable, initially setting M10-13 to Logic-1 *(Fig. 8.11)*.

If the frequency is 1MHz, M10-13 times out and returns to Logic-Ø before the next 1MHz trigger arrives, thus providing a train of negative-going triggers for the second (5.7µs) monostable at M10-9. The first negative-going edge sets M10-12 to Logic-Ø, but in this case each succeeding retrigger arrives before the monostable has timed out, and so M10-12 remains at Logic-Ø. The output from M10-12 drives M18 control input M18-14 (A).

If the frequency is 10MHz, M10-13 (330ns) cannot time out before the next retrigger arrives at M10-2, so it remains at Logic-1. No negative edges appear at M10-9 to trigger M10-12 to Logic-Ø, so the control input to M18-14 remains at Logic-1 as shown in *Fig 8.11*.

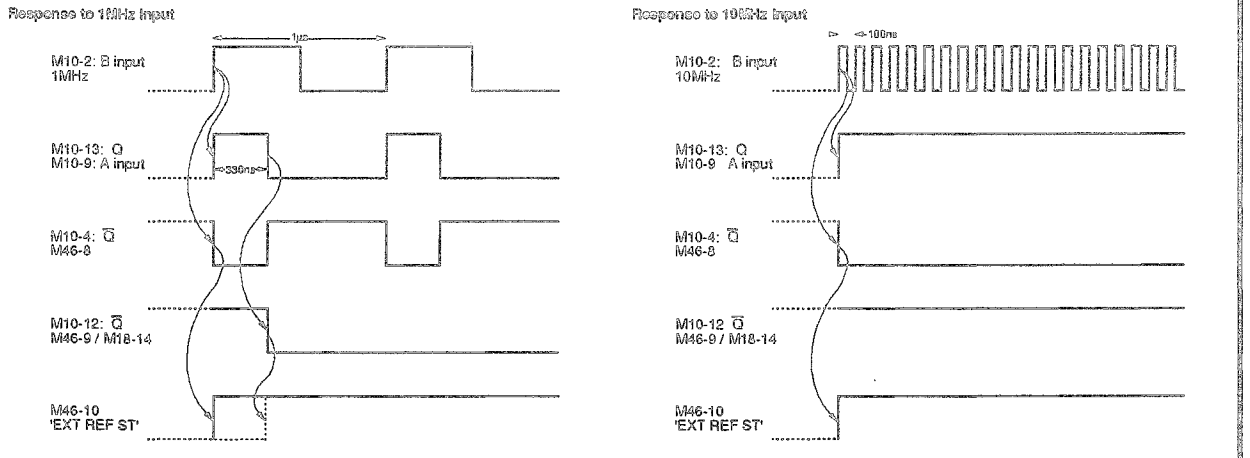


FIG. 8.11 1MHz/10MHz DETECTOR WAVEFORMS

8.3.3.4 M18 Frequency Selections

The input sources to M18-10/11/12/13 are switched to M18-9 according to the following table. The *italicized* frequencies cannot be obtained because it is frequency which controls the A input to M18:

Reference Frequency	'EXT FREQ SEL' M18-2 (B)	1/10MHz Detect. M18-14 (A)	Source Transferred	M18-12 Frequency	M18-13 Frequency
1MHz	1	Ø	M18-12 (2C2)	200kHz	*20kHz*
10MHz	1	1	M18-13 (2C3)	*2MHz*	200kHz
No Input, or 10MHz (and Not Selected)	Ø	1	M18-11 (2C1)	0V	0V
1MHz (and Not Selected)	Ø	Ø	M18-11 (2C0)	0V	0V

8.3.3.5 Further Division of M18 Output

The 200kHz output from M18-9 is divided by a further ÷12.5 before it becomes the signal '16kHz EXT'. This is achieved in three stages:

÷10 (M28-3); x8 (PLL); ÷10 (M28-13).

The x10 dividers are connected as bi-quinary counters to maintain the symmetrical squarewave.

8.3.3.6 PLL Frequency Multiplier

The Phase-Locked Loop is formed by M30 and M53. The VCO oscillates at a frequency which when divided by 8 (M53-11) phase-locks to the 20kHz present at TP25. At this frequency (160kHz) the error voltage across C30 is a very low amplitude ripple balanced about 0V DC.

The loop can be regarded as a simplified version of the synthesizer VCO, described in *para 8.1.2.4*. The VCO output is low-pass filtered, then buffered and inverted by Q1 which drives the final ÷10 counter.

8.3.4 INT/EXT Reference Selection

The 16kHz (EXT) signal output from M28-13 is a symmetrical squarewave phase-locked to the External Reference frequency at TP27. It is passed into the same selector (M18) which carries out the 1MHz/10MHz and INT/EXT selection of the divided signal input. The 16kHz (INT) signal is also applied to M18. In this case the other half of the dual selector is employed.

The 16kHz(EXT)REF signal from TP27 is input via M18-3 and M18-4, while the 16kHz(INT) signal goes to M18-5 and M18-6. Switching between 1MHz and 10MHz (M18-14) has no effect, as the output at M18-7 selects shorted input lines. The INT/EXT switching by EXT FREQ SEL (M18-2) selects between the two pairs of shorted inputs to give the 16kHz (OG) output from M18-7. This is buffered via M5-6, J3-104 *(page 11.3-1)* and the Mother assembly to the Sine Source assembly at J6-53 *(page 11.6-4)*.

8.3.5 'EXT REF ST' (M46)

If no external reference signal is present, both M10 monostables remain permanently in their relaxed (timed-out) state. Thus M10-4 and M10-12 are at Logic-1, both inputs to NAND M46 are Logic-1, so its output (EXT REF ST) is at Logic-Ø. For signal frequencies of 1MHz or 10MHz one of the inputs to M46 is at Logic-Ø, so EXT REF ST goes to Logic-1.

M46 output is returned to the CPU, being sensed on the data bus line D4 at each RTC IRQ (M37-13 *page 11.2-2*), so the CPU knows whether an external reference signal is present or not. It also knows when S53 is selected, and issues the 'Error EF' message on the MODE Display if S53 is selected but no external reference signal is present. This warns the user that with the external reference facility selected, the VCO in the Reference Buffer is free-running in the absence of a locking signal, and is still the reference for synthesis of the instrument output frequency. The output is thus unlocked both from the user's sync source and from the internal crystal oscillator. This is normally because no external reference has been connected to J53 on the rear panel!

SECTION 9 AC VOLTAGE OUTPUTS - AMPLITUDE CONTROL SYSTEM

9.1 INTRODUCTION

This complex system generates the whole range of AC voltage outputs, as defined by its inputs. For the AC Current function, an AC voltage is derived from the internal voltage amplitude loop on the 1V or 10V range to act as an accurate reference. Thus the following description applies also to the generation of that reference.

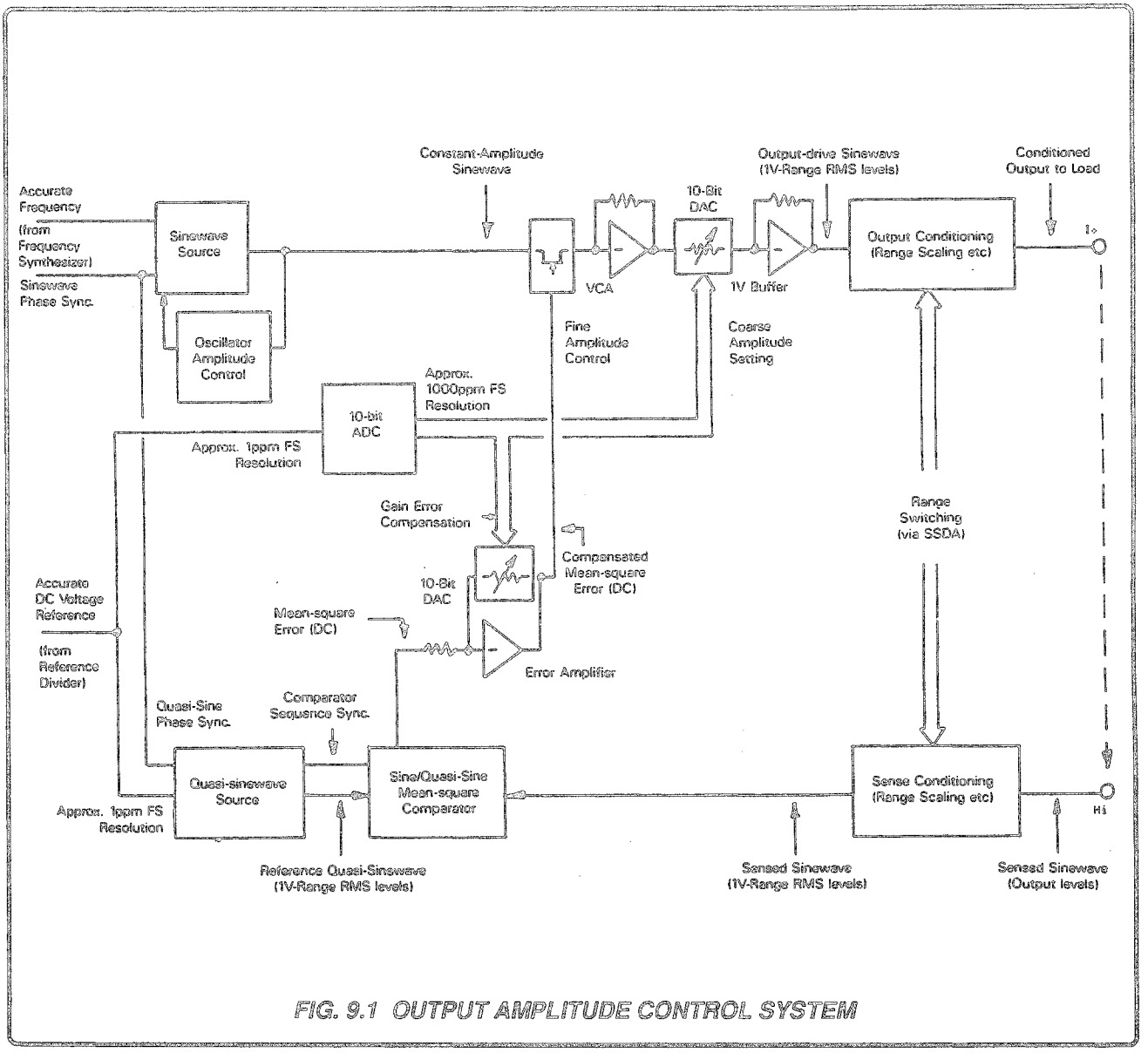


FIG. 9.1 OUTPUT AMPLITUDE CONTROL SYSTEM

Feature of Output	*Controlling Element*	*Controlling Input to Loop*
Frequency:	Frequency Synthesizer (Crystal-Sourced)	Constant-amplitude sinewave from Quadrature Oscillator
Sinewave Purity:	Quadrature Oscillator	Constant-amplitude sinewave
Voltage Range:	Processor, via SSDA and Control Latches	Ranging Signals
Coarse Amplitude:	Reference Divider	Accurate DC Reference Voltage (Resolution reduced to approx. 1000ppm FS by 10-bit DAC)
Fine Amplitude:	Reference Divider and Quasi-sinewave Generator	Quasi-sine RMS value at resolution of approx. 1ppm FS

9.2 AC VOLTAGE AMPLITUDE CONTROL SYSTEM - BLOCK DIAGRAM

(Fig. 9.1)

The system elements are described individually in the five sub-sections from *9.3 to 9.7*. The system block diagram at *Fig. 9.1* throws clear of the handbook, so that it can be used for reference when reading these descriptions.

9.2.1 FREQUENCY/WAVESHAPE CONTROL

Sinewave sourcing is the subject of *sub-sections 8.1* (Frequency Synthesizer) *and 8.2* (Quadrature Oscillator). The result is a high-purity sinewave of constant 1.9V amplitude, input to the VCA.

9.2.2 OUTPUT RANGING

The microprocessor passes Voltage and Current range selections into guard via the serial data link as described in *sub-section 6.4*.

This range information is held in the Analog Control latches in the Reference Divider Assembly, providing signals to the Output and Sense conditioning circuitry.
Their effects are described in *sub-sections 9.4 to 9.6*.

9.2.3 COARSE AMPLITUDE SETTING

The 1V Buffer also acts as a coarse amplitude control within each range. The value of its input resistance is adjusted to control its gain, which is incremented in steps of approximately 1000ppm of Full Scale by a 10-bit digital-to-analog converter.

The increments are defined by a 10-bit analog-to-digital converter, which responds to the accurate DC Reference voltages generated by the Reference Divider. The value of the 'DC Ref' voltage is proportional to the values set on the front panel OUTPUT display, as described in *sub-section 6.5*.

This coarse adjustment of output amplitude allows the fine control element (the VCA) to operate within a small dynamic range, minimizing introduced distortion and thus maintaining the high purity of the output sinewave. The operation of the coarse amplitude control is described in *sub-section 9.3*.

9.2.4 FINE AMPLITUDE CONTROL

9.2.4.1 Error Loop

The output amplitude is controlled within the coarse increments by an 'error' loop. The output is sensed at the load for 4-wire connections, or at an internal point in the forward path when 2-wire connection is selected (or imposed).

The sensed output is reduced to 1V Range RMS levels by the Sense Conditioning circuitry (as described in *sub-sections 9.4 and 9.6*), and its mean-square value is compared with that of the Reference Quasi-sinewave. The difference between the two values is expressed as a DC error, and fed to control the gain of the VCA.

Because the coarse amplitude control adjusts the error loop gain, and the error itself results from comparison with an amplitude analog, the gain of the error loop would not naturally be constant. Compensation is therefore applied to the error to reduce the loop gain in synchronism with increasing increments of coarse amplitude. (The Error Amplifier feedback resistance is reduced by a second DAC in step with the coarse amplitude ADC. The result is that the loop gain, and therefore the loop dynamics, are virtually linear.)

Details of VCA operation and error compensation are described in *sub-section 9.3*.

9.2.4.2 Mean-Square Comparator

When a value is set on the OUTPUT Display, it describes the RMS value of the output. From the displayed value the Reference Divider generates an accurate DC Reference voltage (stepping in increments of approximately 1ppm of Full Scale), which results in a quasi-sinewave whose peak voltage has the same value. (Thus at 1V Full Range output, the DC Reference voltage and the quasi-sinewave peak voltage are both 1.397V.)

The Crest Factor for any wave is defined as its Peak value divided by its RMS value. For a pure sinewave the figure is $\sqrt{2}$ (say 1.414), whereas the quasi-sinewave crest factor is 1.397. So for the same RMS value of 1V Full Range output, the quasi-sinewave input to the comparator has a peak value of 1.397V, against the sense feedback peak of 1.414V. The comparison is between mean-square rather than RMS values, but when the mean-square difference is zero, so is the RMS difference.

Generation of DC Reference voltage and Quasi-sinewave are described in *Section 6*.

9.2.4.3 Synchronization

The comparator is based on a sequence of squaring, integration, sampling and subtraction. Its operation and accuracy rely heavily on the synchronism of sinewave and quasi-sinewave, each state-change in the sequence occurring at zero-crossings of both waveforms. Thus both waveforms synchronize to clocks from the synthesizer, even when the sinewave is at a multiple of the quasi-sinewave frequency. The comparison sequence cycles once every ten quasi-sinewave periods.

9.3 VOLTAGE CONTROLLED AMPLIFIERS

(Circuit Diagram 430446, page 11.6-3)

The circuits described in this section perform the following functions:

- Modify the output of the Sine Source by coarsely tracking the gain of the output amplitude to the requested output voltage, providing stepped coverage of the instrument's dynamic range.
- Provide smooth adjustment of gain, within the coarse steps, in response to error signals from the Sine/Quasi-Sine Comparator.
- Impose the settling rate of the true analog DC reference voltage on both the coarse gain adjustment and the mean-square error (AC AMPL ERROR) scaling.
- Sense excess currents in the output buffer, providing a $\overline{\text{LIM ST}}$ signal to the CPU via the analog control interface.

All the circuits described in this section are located on the Sine Source Assembly. On the circuit diagram, two voltage-controlled amplifiers are shown:

- The 1 Volt Buffer (M45, M46 and the discrete output amplifier). Its input resistance is controlled by the DAC M43.
- The main VCA M48/Q88, whose input resistance is determined by the FET chain Q76 and Q77.

For a general description of the Output Amplitude Control System refer to *sub-sections 9.1 and 9.2*.

9.3.1 GENERAL

(Fig. 9.2)

The main VCA receives a constant amplitude sinewave input from the Quadrature Oscillator (*Section 8*). Its gain is controlled by an error voltage, which is obtained by comparing the sensed sinewave output of the instrument with the reference quasi-sinewave.

The 1 Volt Buffer is included in the output signal path on all voltage and current ranges. It also acts as a VCA, since its input resistance is controlled by its 10-bit Digital-to-Analog Converter. The DAC receives its binary input from an Analog-to-Digital Converter, whose numerical output tracks the user's output demand, in increments of size approximately 1000ppm of full scale.

It is also necessary to ensure that the rate of coarse gain adjustment tracks the settling-time characteristics of the DC Reference filter. To achieve this, the ADC is controlled by the level of the DC Reference voltage. The filtered reference's settling time is thus imposed on the ADC digital output, and hence on the 1V Buffer gain adjustments.

For reasons given in *sub-section 9.1*, it is also necessary to compensate the output loop gain error synchronously with the coarse gain steps. The tracking ADC therefore drives a second DAC, which selects values of feedback resistor in the Error Amplifier. This increments the output-amplitude error loop gain, modifying the AC AMPL ERROR signal which originated in the mean-square comparator.

The tracking ADC and its DACs ensure that the loop has the fastest possible settling time for any selected frequency.

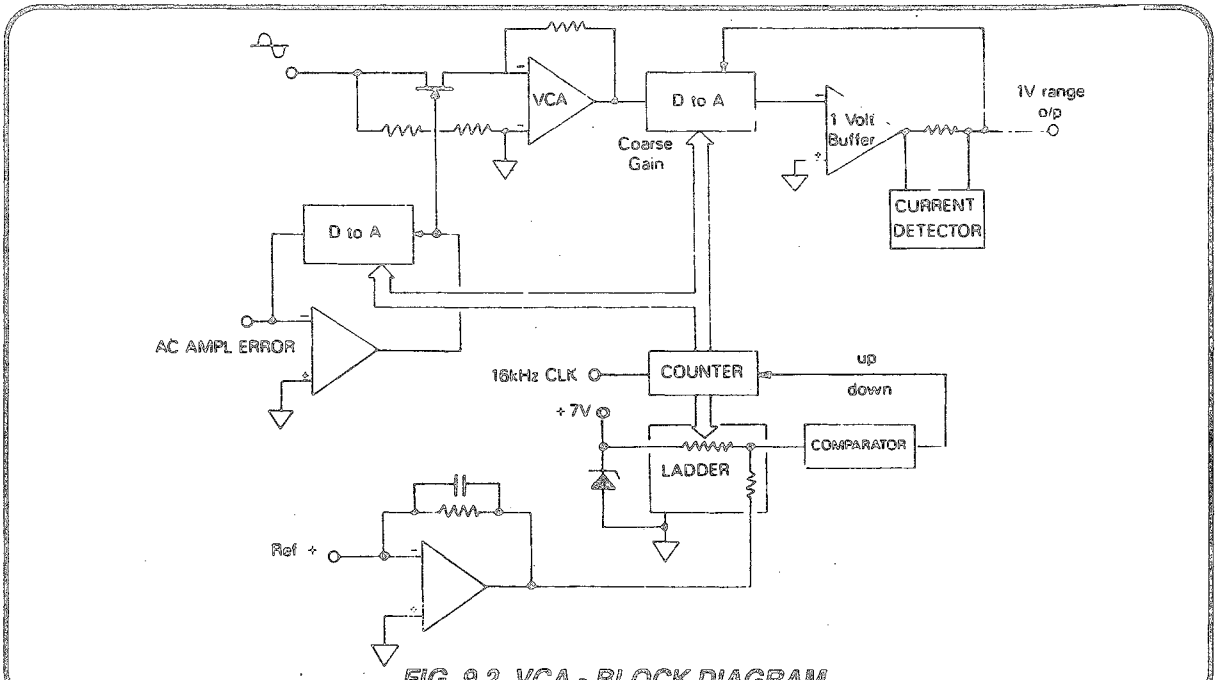


FIG. 9.2 VCA - BLOCK DIAGRAM

9.3.1 VCA AND 1V BUFFER

The VCA and 1V Buffer combine in cascade to modify the amplitude of the sinewave output from the sine oscillator, accurately covering the instrument's dynamic range *(see Section 9.1 and 9.2)*. The eventual output from the 1V Buffer (AC 1V FR) forms the instrument's basic 1V AC range.

The VCA gain is adjusted by the 'AC AMPL ERROR' signal, scaled by M41 and M42. The coarse gain scaling of the 1V buffer derives from the DC Reference voltage 'Ref+'.

9.3.1.1 Main Voltage-controlled Amplifier

(Circuit Diagram 430446 Pages 11.6-1 & 11.6-3).

The Sine Oscillator output from ÷2 buffer M47 *(page 11.6-1)* is emitter-followed by Q75 to the VCA FET input chain Q76/Q77 *(page 11.6-3)*. These dual FETs are enclosed with M47 PTC feedback resistors R136 and R137, in a metal heatsink. The matched FETs Q76/Q77 ($R_{DS\ (ON)}$ within 1%) form the variable gain element for the low input-offset amplifier M48, to provide distortion-free and linear control of gain.

Each FET gate is current-bootstrapped from the divider AN18, to maintain a linear relationship between gain and input voltage. C106 and C117 drive the chain at HF. The center of the FET chain is also bootstrapped, M44 ensuring precise AC tracking. Resistors R143 and R135 divide and limit the maximum input resistance, preventing the gain from falling to zero.

The thermal linking to M47 feedback resistors compensates for the FET chain temperature coefficient. The inertia of the heatsink's thermal time-constant also prevents gain modulation due to draughts.

The DC signal 'AC AMPL ERROR' is scaled and then fed to each gate by transistors Q78 to Q81, which have low collector capacitance. The voltage control element formed by these transistors adjusts the DC gate voltages of the FETs in the chain, and hence the input resistance of the VCA.

M48 output is emitter-followed and passed through DC-isolating (and AC-compensating) capacitors C121 and C122 into M43, the 1V buffer DAC.

9.3.1.2 The 1V Buffer

The buffer consists of a voltage follower with hard current limiting. Amplifiers M45 and M46 buffer the Class A power stage from the capacitance of the input DAC. The first buffer M45 has extremely high DC gain, rolling off at HF due to the feedback of C108. It removes the input DC offsets of M46.

M46 controls the buffer's AC performance; C112 ensures that the non-inverting input appears as a virtual AC ground at HF, allowing source-follower Q74 to develop the AC input across R159.

The discrete output stage provides class A current amplification, avoiding any cross-over distortion particularly at HF. Power transistor Q93 is provided with load and quiescent currents, from constant-current source Q94 (70mA) and constant-current sink Q86 (140mA). *Refer to Fig. 9.3.*

With zero input conditions Q94 is saturated, limiting the quiescent current at 70mA. Only the small bias current for Q92 flows in R144, so the output voltage is just +Vb.

The input signal to Q92 controls Q93, allowing a small signal transistor with good HF performance to adjust the large output currents flowing in R144.

Voltage amplifier Q92 conduction falls during positive half-cycles of input, reducing Q93 conduction. The quiescent current still flows in Q94, but part is now diverted through the output circuit via R144, R112 and L7.

During negative half-cycles of input; Q92 conduction increases, so Q93 conducts more heavily, drawing its extra (load) current through R144, and its quiescent current from Q94. The emitter of Q92 also attempts to go negative, drawing current directly from the load. The combined currents flow into the current sink, so Q86 must be able to sink 70mA quiescent + 70mA load.

In the output line, inductor L7 and resistor R112 provide phase compensation for capacitive loading at HF.

If any components in the discrete amplifier are changed, re-adjustment of gain (using M48 feedback resistor R149) may be necessary.

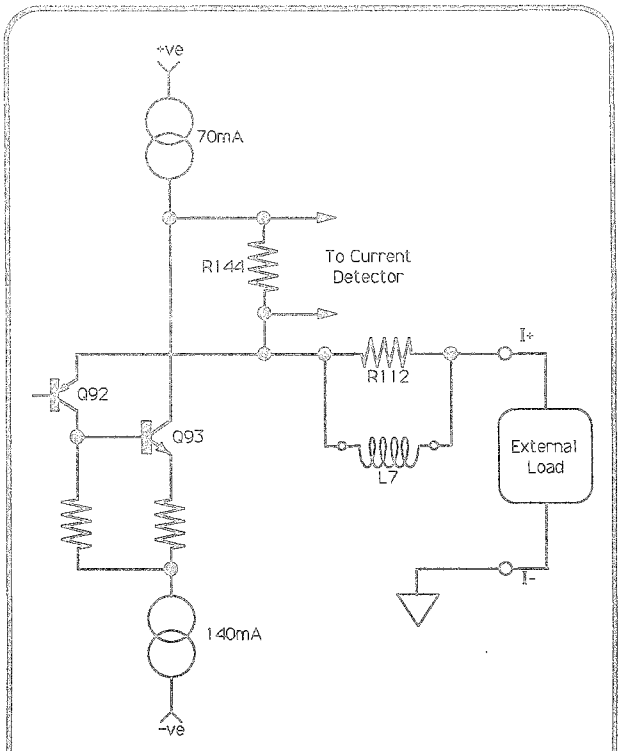


FIG. 9.3 1V BUFFER - OUTPUT STAGE

9.3.1.3 Current Detector

Except for a small bias current, all output current from the discrete buffer stage flows in R144, so the current level can be detected by sensing the differential voltage across it. This sense voltage rides on the output voltage; thus to capture it, the current detector is bootstrapped to the AC 1V output.

High-speed dual comparator M49 forms the basis of the Current Detector circuit. Its supplies are bootstrapped via TP29 to the junction of R144 and R112 in the 1V Buffer output. Q82 and Q84 provide constant current drive to 6.2V Zeners D40 and D41, with Q83 and Q85 providing the regulation for the bootstrapped rails at TP35 and TP36.

The comparator latching levels are set by dividers R151/R152 and R153/R154, their values allowing for bias current error in R144. The comparator's output is open-collector when the peak voltage across R144 is less than the positive or negative latch level. Line drivers Q90 and Q91 are cut off, so the $\overline{\text{LIM ST}}$ line at J6-70 is pulled to +15V by AN2 in the Reference Divider *(page 11.4-4)*.

When the level is exceeded in either polarity, then either M49a or M49b output goes negative. This turns Q90 and Q91 on, pulling the $\overline{\text{LIM ST}}$ line to -15V (in-guard logic-Ø). The signal is passed to the CPU via the serial data link.

This limit is set much lower than the hard current limit of the buffer. If exceeded, the instrument displays 'Error OL', described in *Section 2* (Fault Diagnosis). In overload at 35-40mA, a built-in margin of safety allows the instrument to meet most of its specifications.

9.3.2 ADC - DAC TRACKING

As mentioned earlier, it is necessary to track the coarse gain stepping rate to the settling time imposed by the DC Reference filtering. A tracking Analog-to-Digital Converter (ADC) is used to synchronize stepping, ensuring the fastest possible settling time at the selected frequency.

To set circuit conditions for the required output within a range, the gain of the main VCA is set in response to fine amplitude information, in the form of an error signal from the Sine/Quasi-Sine comparator. For constant output amplitude loop gain, the error loop gain also needs to track the coarse amplitude stepping.

For an outline of the Output Amplitude Control System, refer to the descriptions in *sub-sections 9.1 and 9.2*.

9.3.2.1 Use of 'REF+'

(Circuit Diagram 430446 page 11.6-3)

The ADC requires a voltage input which tracks the value of instrument AC output demanded by the user, with settling times imposed by the Reference filter. The DC 'REF+' voltage exhibits these characteristics, so is used in this circuit to determine the numerical value of the ADC binary output.

'REF+' originates in the Reference Divider and is used to set the peak value of the quasi-sinewave in the AC assembly. Its value ranges from +0.126V at 9% of Full Range, through +1.397V at Full Range, to +2.794V at Full Scale.

REF+ is input to the Sine-Source assembly at J6-57 and J6-56, then applied to amplifier M41b, which is connected to remove any common mode present at its input. Thus at TP47, M41b output is referred to Common-2A.

Capacitors C99, C130 and C131 filter any HF pickup from the reference voltage, and M41b scales up the DC voltage levels by a factor of 2.43, to:

9% of Full Range:	-0.306V,
Full Range:	-3.395V,
Full Scale:	-6.789V.

A fixed positive version of this Full Scale value is also generated (Q66/D30/D31) as a reference for the tracking ADC M38 at M38-27.

9.3.2.2 Tracking ADC M38

(Fig.9.4)

M38 is a 'System DAC' which can be employed either in 'READ' or 'WRITE' mode. WRITE mode is not used for this function.

In READ mode the binary count can be output continuously from the ten pins DB_{9-0}. An internal 10-bit counter is clocked at 16kHz into pin 9 via level shifters Q53 and Q54. The counter can be controlled by two level-sensitive inputs: CONT 1 and CONT 2 (logic-1 = +5V; logic-Ø = 0V) as follows:

CONT 1	CONT 2	Effect on Count
Ø	Ø	not used
Ø	1	Incremented
1	Ø	Decremented
1	1	Frozen

An internal 12kΩ reference resistor and switched resistor ladder form a divider between pin 27 (V_{REF}) and pin 1 (R_{FB}). Their junction is brought out to pin 2 (OUT 1). *(See Figs. 9.4 and 9.5.)*

The ladder is switched by the 10-bit counter. At zero count it is open-circuit; as the count is increased the ladder resistance reduces in inverse proportion, until at full count of 2^{11} - 1 (corresponding to the instrument Full Scale output), it reaches its minimum of 12kΩ.

At Full Scale (FS) the M41b output voltage is -6.789V, into R_{FB}, and the fixed reference into V_{REF} is the positive version of this input, so at FS the OUT 1 voltage is balanced at zero.

For instrument output values below FS, the negative M41b output voltage is linearly reduced, so that the OUT 1 voltage tends to increase positively. By feeding an external comparator which drives the CONT 1 and CONT 2 counter controls, the OUT 1 voltage is used to provide automatic control of the count itself. In the case of a reduced output demand, a lower count is required to increase the resistance of the ladder, resetting OUT 1 to the zero balance.

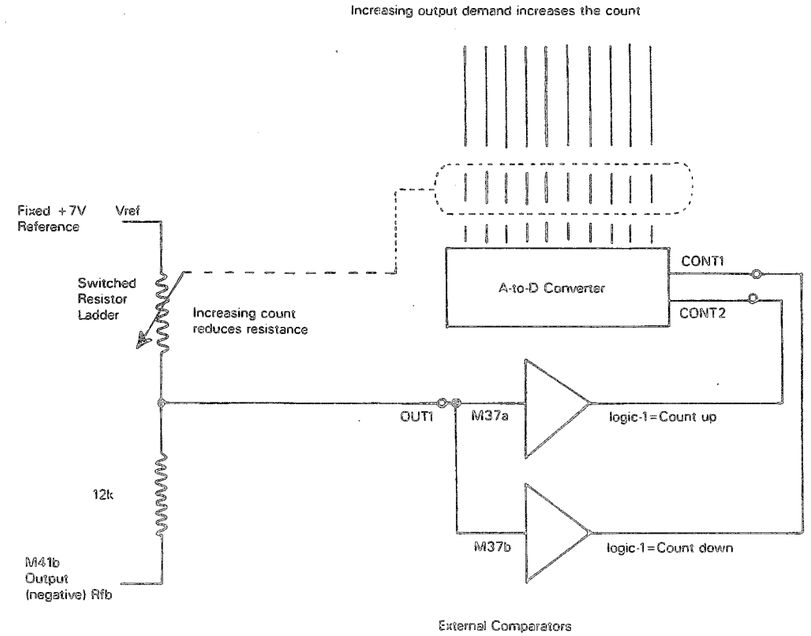


FIG. 9.4 SIMPLIFIED DIAGRAM OF TRACKING ANALOG-TO-DIGITAL CONVERTER

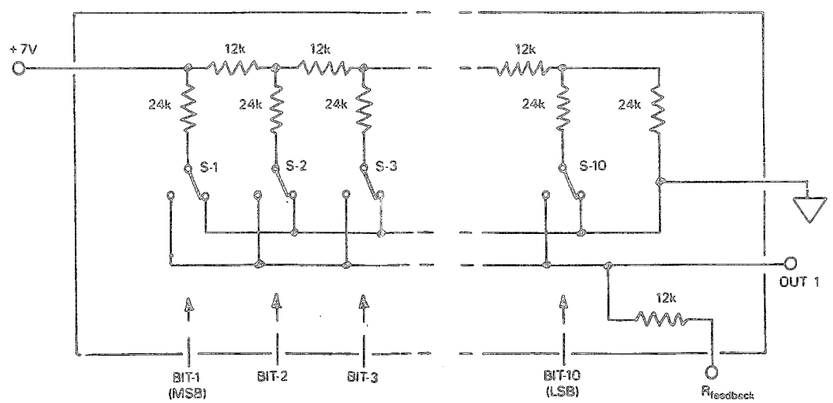


FIG. 9.5 A-D TRACKING - R/2R NETWORK

9.3.2.3 Window Comparator

M37 is a high-speed dual comparator, which accepts OUT 1 as its input voltage, and controls the M38 counter via its CONT 1 and CONT 2 inputs. The 'Counter Freeze' condition of M38, resulting from both CONT inputs being at logic-1, allows hysteresis bias to be applied the comparator to create a 'Dead Band' window.

Each of the two outputs of M37 responds to its input in the same way: high impedance when its non-inverting input is more positive than its inverting input, and pulled low when the inverting input is more positive (uncommitted-collector).

M37a is connected as a non-inverting device, but M37b inverts its input. OUT 1 is input to both circuits. Both inputs are biassed by approximately 15mV to generate the dead-band hysteresis: M37a by R96/R98, R37b by R100/R101.

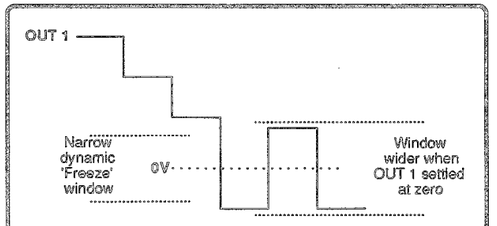


FIG. 9.6 WINDOW COMPARATOR ACTION

9.3.2.4 Action for OUT 1 = Zero

Because of the bias, both M37 outputs are pulled low when the voltage at OUT 1 is zero. The inverting level-shifters Q67 and Q68 are both cut off by -15V on their gates, so CONT 1 and CONT 2 are at logic-1. M38 is thus put in the 'Freeze' condition, so its 10-bit output value is held.

In this condition, M36-12 and M36-13 inputs are both at -15V, so M36-10 is also -15V. R99 is therefore placed in parallel with R100, increasing the bias on M37b. The bias on M37a is also increased by Q69 being cut off, placing AN11 and R97 in parallel with R96. The 'Freeze' window is therefore widened, to improve the comparator's noise rejection. *(Refer to Fig. 9.6.)*

9.3.2.5 Action when OUT 1 Voltage Changes

When a user demands a new (greater) output from the instrument, REF+ increases as the Reference filter settles, and the OUT 1 voltage becomes more negative. The bias on M37b is eroded and finally exceeded, so M37-7 is placed at high impedance, pulled up to Common-2C by AN13. Q67 conducts setting CONT 1 to logic-Ø, which increments the count to step up the gain in the 1V Buffer.

Simultaneously, M36-12 is set to 0V (in guard logic-1). M36-10 rises from -15V to 0V, switching R99 to shunt R101 instead of shunting R100. Q69 conducts, switching R97 to shunt R98 instead of shunting R96. The bias levels shift back to 15mV, narrowing the hysteresis window.

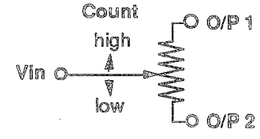
If the user had demanded a lower output, OUT 1 would have become more positive, exceeding M37a bias. CONT 2 would have fallen to logic-Ø, decrementing the counter and reducing the 1V Buffer gain. The effect on the comparator bias would be the same as for the incrementing case.

As the counter changes its numerical value, M38's internal resistance ladder is switched to back-off the OUT 1 voltage. When REF+ finally settles, the OUT 1 voltage once again enters (and widens) the comparator's dead band, The count freezes, and the 1V Buffer gain remains constant.

Thus the OUT 1 voltage remains close to zero as the comparator and tracking ADC have a sensitive response to the variations of REF+; but once settled, the wider hysteresis window prevents the comparator from responding to noise.

9.3.2.6 10-bit Digital-to-Analog Converters

M42 and M43 binary inputs are identically connected, so they both behave in the same way:



For low counts the resistance between Vin and O/P 1 is large, and small between Vin and O/P 2. The condition is incrementally reversed as the count increases to high values.

M43
As we have seen; an increase in user output demand increases the DC Reference voltage REF+, so a higher ADC count results. This reduces the resistance between M43 pin 15 (Vin) and pin 1 (O/P 1), and increases the resistance between Vin and O/P 2; increasing the gain of the 1V Buffer and thus increasing the instrument output. This is the stepped coarse gain adjustment referred to in *sub-section 9.2.*

M42
M42 has a different function. The fine adjustment of output value is incorporated in the 'Gain Error Loop', in which the output sinewave and quasi-sinewave are compared. This comparison generates the 'AC AMPL ERROR', to be used in controlling the VCA gain.

The error loop thus also passes through the 1V Buffer, and the effect of an increase in ADC count would be to increase the error loop gain, possibly overloading the VCA input FETs. This is prevented by reducing the gain of the error amplifier M41a, using M42 to track the steps of the coarse gain adjustment.

With an increase of the ADC count, M41a feedback is increased, as the resistance between M42 pins 15 and 1 is reduced. This reduces the error loop gain to compensate for the increase due to M43. Thus the fine gain remains virtually constant over the full span of coarse gain adjustment.

9.4 AC LOW VOLTAGE LOOP

The circuits described in this section perform the following functions:

- Connect the VCA (1V buffer) output to the instrument's terminals to provide the AC 1V Range: 0.09V to 2V.
- Amplify the VCA output voltages and connect to the terminals for the AC 10V Range: 0.9V to 20V.
- Passively attenuate the basic AC 1V range voltages to provide the millivolt range outputs:
  9mV to 200mV on the AC 100mV Range
  0.9mV to 20mV on the AC 10mV Range
  90µV to 2mV on the AC 1mV Range
- Sense the voltages at the output terminals (or at the load in Remote Sense) and scale the signal to the 1V RMS Full-Range level for comparison with the quasi-sinewave.
- Provide switching of AC voltage output, Range, Guard and Sense, under the control of signals from the Analog Control Interface.
- Detect excess currents in the output circuit, providing a status signal to the CPU via the Analog Control Interface.
- Detect excess voltages on the PHi (I+) output line, providing a status signal to the CPU via the Analog Control Interface.
- Switch the generated 10V range to the model 4600 analog control bus, as described in section 7.3.8. For clarity, these connections have been omitted from Fig 9.7

The circuits in this section are located as follows:

Millivolt attenuator & sensing:	AC Assembly.
Power amplification:	Power Amplifier Assembly.
Output control:	DC Assembly.
Output Terminals:	Mother Assembly and Terminal Board.

A simplified block diagram of the low voltage loop and routing appears in *Fig. 9.7.*

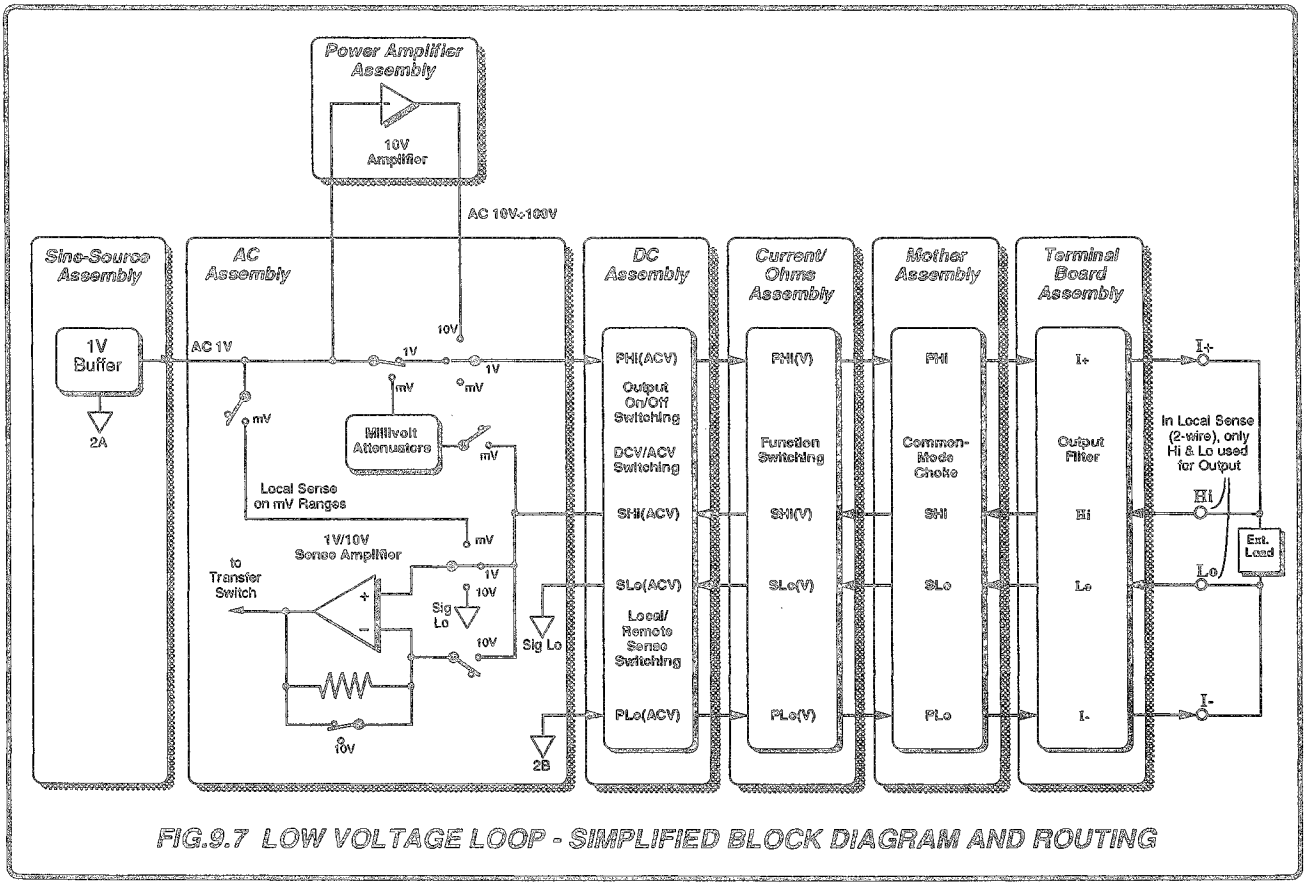


FIG.9.7 LOW VOLTAGE LOOP - SIMPLIFIED BLOCK DIAGRAM AND ROUTING

9.4.1 GENERAL

The following description follows the 1V range path from the VCA buffer to the Sine/Quasi-Sine Comparator (at the input of the transfer switch M16). The 10V and millivolts outputs and sense conditioning are included, the outputs also being sourced from the 1V Buffer.

On the circuit diagrams, the relay contacts are shown in the un-activated condition.

For High Voltage output and High Voltage sense attenuation refer to *Sections 9.5 and 9.6*.

9.4.2 1V LOOP - POWER DELIVERY

9.4.2.1 Sine-Source Assembly

(Circuit diagram 430446 Page 11.6-3)

The 1V Buffer *(page 11.6-3)* is described in *sub-section 9.3*, as part of the output amplitude control circuitry. Its output sinewave, signal 'AC 1V' ranging between 0.09V and 2V RMS is fed out of the Sine-Source assembly on J6-41, via the Mother assembly, and input to the AC assembly on J7-41 *(page 11.7-1)*.

9.4.2.2 AC Assembly

(Circuit diagram 400844 Page 11.7-1)

With the 1V Range selected, relays RL7 (1V) and RL19 (1kV) are energized, but relays RL4, 5, 6, 17, 18 and 20 are not. Therefore the AC 1V signal is passed directly out of the AC assembly via RL7, fuse F1, RL19 and fuse F2 to become the Power-Hi signal 'PHI(ACV)' at J7-27.

The power common 'PLO(ACV)' is sourced from the in-guard Common-2 supply at the star-point Common-2B, passing out via the energized contacts of AC Voltage selector relay RL10, to J7-31.

PHI(ACV) and PLO(ACV) travel via the Mother assembly to the DC assembly at J5-25 and J5-29 respectively *(Page 11.5-2)*.

9.4.2.3 DC Assembly

(Circuit diagram 430536 Page 11.5-2)

Output Switching

The PHI and PLO (ACV) connections are passed to the instrument output terminals via several relay contacts which provide switching for Remote or Local Sense, Remote or Local Guard, and Output On/Off.

If Option 40 or 50 is fitted, the terminal lines are switched for function changes on the Current/Ohms assembly. When neither Option 40 nor Option 50 is fitted, a Current/Ohms Link PCB (Part No. 410288) is fitted in place of the Current/Ohms assembly. This PCB provides direct connections for the signals, on their route to the instrument terminals.

ACV/DCV Switching

For AC voltage outputs, relays RL10 and RL11 are un-energized. The PHI(ACV) line for the 1V range bypasses the 1kV Range current sensing resistors R107 and R108, via contacts 7/10 of the un-energized relay RL13. It then passes directly via TP8, 1A fuse F6, and RL15 contacts (if output is set ON); to the PHI(V) line at J5-19.

When in Remote Sense, the power return line PLO(ACV) is linked from J5-29, via 1A fuses F4 and F3, RL14 and RL15 contacts to become PLO(V) at J5-23.

(For DC voltage outputs, the four ACV lines at J5-25/26/29/30 are disconnected by the Range relays and the ACV relay RL10 in the AC assembly).

9.4.2.4 Connections to the Terminals

(Section 7)

The PHI(V) and PLO(V) lines are routed to the I+ and I- terminals on the front panel exactly as for DC 1V Range outputs.

Descriptions of the processing and routing can be found in the following sub-sections of *Section 7*:

Output On/Off:	*7.3.6.2*
Remote Sense:	*7.3.6.3*
Remote Guard:	*7.3.6.4*
Overvoltage Detection:	*7.3.7.2*
Output to Terminals:	*7.3.8*

9.4.3 AC 1V LOOP - OUTPUT SENSING

The SHI(V) and SLO(V) lines are routed from the Hi and Lo terminals on the front panel exactly as for DC 1V Range outputs. The processing and routing back to the DC assembly is described in *Section 7, sub-sections 7.3.9.1 to 7.3.9.3*.

9.4.3.1 DC Assembly

(Circuit diagram 430536 Page 11.5-2)

In normal 4-wire operation (Remote Sense selected) with OUTPUT 'ON' on the AC 1V Range, relays RL14 and 15 are energized; RL10 and 11 are un-energized.

SHI(V) enters from the Mother assembly at J5-20, passing directly through RL15 contacts, TP9 and R98, to J5-26 as SHI(ACV).

SLO(V) travels via RL15 contacts and TP10 to J5-30 as SLO(ACV).

With Remote Sense not selected, relay RL14 is unenergized:
RL14-9/8 short SHI(V) to the power Hi output PHI(V).
RL14-2/3 short SLO(V) to the power Lo output PLO(V).

SHI(ACV) and SLO(ACV) are routed from J5-26 and J5-30 via the Mother assembly to the AC assembly.

9.4.3.2 AC Assembly

(Circuit diagram 430844 Page 11.7-1)

SLO(ACV) passes via the energized contact of the AC Voltage selector relay RL10, to be referred to the Sine/Quasi-Sine comparator transfer switch common 'SIG LO'.

With the 1V Range selected, relay RL19 ($\overline{1kV}$) contacts are closed, so SHI(ACV) appears at RL19-11 as 'SENSE Hi'.
(Refer to the circuit diagram on *page 11.7-2.*)

With the 1V Range selected, relay RL8 (1V) is energized, thus SENSE Hi is applied to the non-inverting input of the Sense Amplifier via R126. RL14 is un-energized as shown, so the inverting input via R115 is referred to SIG LO.

RL3 ($\overline{100V+1kV}$) is energized, connecting the Sense Amplifier output to the Sine/Quasi-Sine comparator transfer switch M16-11 *(page 11.7-3)*. The amplifier is described in *sub-section 9.4.4.*

9.4.4 AC 1V SENSE AMPLIFIER

(Circuit Diagram 430844 page 11.7-2)

The same amplifier is used on the 10V, 1V, 100mV, 10mV and 1mV AC Ranges. Its main purpose is to buffer the sense voltage, providing a high impedance input, low DC offset and flat frequency response.

On the AC 1V and millivolt ranges it is connected as a voltage-follower, sensing always being carried out at the 1V level. The 1V Range sense signal originates at the load in remote sense, or in the DC assembly in local sense.

For the millivolt ranges the 'AC 1V' drive signal to the millivolt attenuators is sensed directly *(see sub-section 9.4.5)*.

On the AC 10V range an inverting configuration is employed. The circuit divides by 10, scaling the sense signal down to 1V range levels, for input to the Sine/Quasi-Sine comparator.

Separate arrangements are made for attenuation and scaling on the 100V and 1kV AC ranges. These are described in *Section 9.6.*

9.4.4.1 General Arrangement

A discrete amplifier is used to provide the required slew rate up to 1MHz, all time constants being set well above 1MHz, with the first pole above 5MHz. It is configured into its follower circuit by relay switching.

Relays RL8, RL12 and RL3 are all energized on the 1V range. Relays RL11, RL13, RL14, RL15 and RL16 remain un-energized as shown in the diagram.

Dual JFET Q41 is a unity gain buffer in totem pole configuration. It drives the input protection diodes D37-D40, D44-D47; the screen on Q40 inverting input; and the bootstrap buffer Q46. The total input capacitance is thus reduced to 1-1.5pF.

The differential input amplifier, dual FET Q40, has low input capacitance and low input current. Q36 provides constant-current drive to Q40 and the bootstrapped followers Q38/Q39. R107 permits initial DC input-offset cancellation. The stage gain is low.

Emitter-followers Q34 and Q35 buffer the high-impedance low-gain FET stage, driving a differential signal into the high gain voltage amplifier Q29/Q30. This arrangement has the advantage of placing all the gain in one stage. The single-ended drive to Q31 output stage is taken from Q30 collector.

Q24 and Q25 form a current mirror to equallize the collector currents of Q29 and Q30, preventing signal injection into the sense amplifier power rails.

L6 and L7 isolate the amplifier power rails from the 15V supply at HF. C50 is the main frequency-response compensation capacitor, providing smooth roll-off, with unity gain at around 5MHz.

On the 1V Range, the output from Q31 is returned at low impedance, as 100% negative feedback to the amplifier input, via the closed contacts of RL12-8/14.

9.4.5 MILLIVOLT LOOP

(Circuit Diagram 400844 pages 11.7-1 and 11.7-2)

The basic 1V loop is extended by inserting a switched, passive, attenuator network. The switching circuit connects the selected millivolt output via RL4-13/9 and RL19-11/8 directly to the SHI(ACV) line, not 'PHI'. Thus only the two front panel Sense Hi and Lo terminals are used to connect to the load.

The software forces Remote Sense OFF in the millivolt ranges. Except for a series resistor (R154) on the 1mV range, the AC 1V signal is connected directly to the input of the Sense Amplifier via RL11-4/5 at RL8-13. The amplifier circuit remains permanently in its non-inverting configuration for all three millivolt ranges, so local sensing is carried out at 1V range levels.

Thus the output value at the terminals depends on both the calibrated value of the AC 1V signal and the division ratio of the attenuator. In addition to the 1V range calibration, each millivolt range is also 'Autocalibrated' separately *(refer to User's Handbook Section 8)*.

9.4.5.1 Millivolt Attenuators

(Fig. 9.8)

The AC 1V signal is diverted from its 1V range route by contacts 13/11 of un-energized relay RL7, and applied to the attenuator network.

The fixed chain (formed by R120 in series with the parallel combination of R112B and R110) is permanently connected between RL7-11 and the Common-2 star-point. Three levels of attenuation are achieved by switching R112A and R118. Relay RL5 is energized for the 10mV range only, RL6 for the 100mV range.

The three arrangements are shown in *Fig. 9.8*.

On the 1mV range, the series resistor R154 is connected between RL7-11 and the Sense Amplifier input via RL11-5, but it is shorted on the 10mV and 100mV ranges by the closed contacts of RL5 and RL6 respectively.

Relay RL4 is energized on all millivolt ranges. The attenuator output is passed out via RL4-8/9 and RL19-11/8 to the SHI(ACV) line. C89 defines the specified bandwidth, filtering noise at HF.

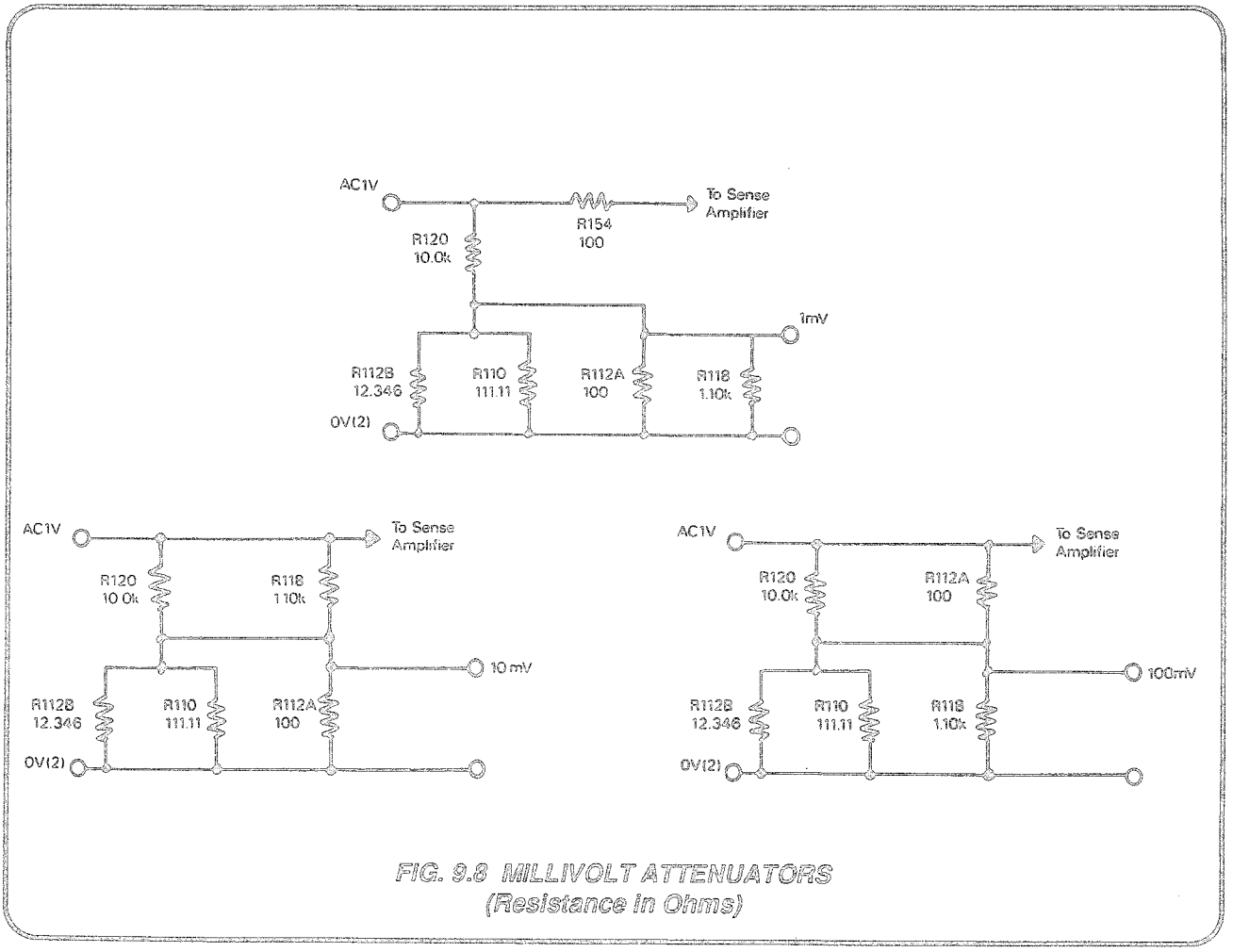


FIG. 9.8 MILLIVOLT ATTENUATORS (Resistance in Ohms)

9.4.6 10V LOOP

(Circuit Diagrams: 430446 page 11.6-3; 430618 page 11.9-1 and 11.9-2; and 400844 page 11.7-1)

As noted in *sub-section 9.4.1*, the 1V Buffer is part of the power delivery system for all ranges. On the 10V range its output (AC 1V) passes via J6-41 from the Sine-Source assembly and into the Power Amplifier assembly (PA) at J9-36 *(page 11.9-2)*.

The AC1V signal is amplified by a factor of 10 in the inverting 10V Power Amplifier, whose output is placed on the 'AC 10V+100V' line. This 10V range signal returns to the AC assembly at relay contacts RL17-13/4. It passes through RL19-2/5 to the PHI(ACV) line at J7-27.

The 10V range outputs then follow the same route (to and from the output terminals) as the 1V signals. Whether in Remote Sense or not, the sensed voltages return via the SHI(ACV) line to the same Sense Amplifier used for 1V range signals.

With 10V range selected, the sense amplifier has an inverting gain of 0.1, returning the signal to the 1V Range levels required by the Sine/Quasi-Sine comparator.

9.4.7 10V POWER AMPLIFIER

(Circuit Diagram 430618 page 11.9-2)

The AC 1V signal enters the PA assembly at J9-36, passing to the input of the 10V Amplifier via relays RL4-9/13 and RL3-9/13. It is referred to Common-2B by developing a voltage across R124.

The amplifier has already been described for the DC 10V Range; in this text, the effects on the 10V AC Range of its separate DC and AC paths are considered below.

9.4.7.1 DC Path

The DC path is blocked by C56; M17 is the DC input amplifier, connected as an integrator with diode clamping. M19 operates as an inverter in open loop, so applies high DC gain to the output from M17 on M19-2.

The output from M19 drives both halves of the symmetrical, inverting, discrete power amplifier through current-limiters Q21 and Q24, and is buffered by emitter-followers Q22 and Q23. Common-emitters Q27 and Q29 form a voltage amplifier, driving the complementary output stage Q32 and Q33. Input and feedback resistors R119 and R120 set the gain of the discrete stages to approximately 4.5.

The forward amplification contains three inversions, DC negative feedback being applied to M17 inverting input by R122, defining an overall gain of 10 in conjunction with input resistor R123.

The DC path senses and corrects the DC offsets throughout the whole AC amplifier, referring the output to Common-2A at M17-3.

9.4.7.2 AC Path

The AC path is blocked by the integrator M17, but is applied to the non-inverting input of M19 through the coupling capacitor C56. M19 operates in open loop, applying its output to the discrete power amplifier *(see 9.4.7.1 above)*.

The amplifier AC gain is also set to 10 by R122 and R123, the circuit time constants being selected to allow overall instrument output operation over the full frequency range of 10Hz to 1MHz.

9.4.7.3 Power Supplies

M17 and M19 are supplied from ±15V common-2A rails, but the discrete amplifier receives power from the ±38V supply.

9.4.7.4 Overload Detection

The $\overline{\text{10V FLAG}}$ line, connected to TP12, is pulled up to 0V (in-guard logic-1) in the Reference Divider assembly *(page 11.4-4)* by AN2-9/1 (1MΩ). The Error OL message results from this line being driven to logic-Ø.

RL8 is energized for the AC 10V Range, so overload detector Q31 reaches Vbe threshold on output current peaks, when the RMS value in R139/R172 and R141 exceeds approximately 80mA. Similarly, Q34 detects peak currents in R147 and R149/R173. In either case, the conduction of Q34 pulls TP12 down to -15.7V. The $\overline{\text{10V FLAG}}$ line is driven to logic-Ø, so the status message is returned to the CPU via the SSDA serial interface, and the Error OL message is displayed.

This does not preclude further increase in output current, but the accuracy specification is not guaranteed.

9.4.7.5 Overload Limiting

If the RMS output current increases to approximately 100mA, the peaks of current cause the Vbe threshold of Q28 or Q30 to be exceeded, shunting the base current of the corresponding voltage amplifier. This hard-limits the output drive to the final stage.

9.4.7.6 Output Protection

The output current passes through the combination of R144 and L8. At low frequencies the inductor provides a low output impedance, whereas at high frequencies the resistor stabilizes the amplifier when driving capacitive loads.

9.4.8 10V SENSE AMPLIFIER

(Circuit Diagram 400844 page 11.7-2)

9.4.8.1 General

A common sense amplifier is used for the 10V, 1V, 100mV, 10mV and 1mV Ranges. Its main purpose is to buffer the sense voltage, providing a high impedance input, low DC offset and flat frequency response.

The operation of the Sense Amplifier for the AC 1V and millivolt ranges, is described in *para 9.4.4.1*. For these ranges it is connected as a voltage-follower.

The AC millivolt ranges' outputs are simply the AC 1V range after passive attenuation; these levels are not sensed directly. The AC 1V signal is sensed before attenuation.

On the 10V range an inverting configuration is employed. The circuit divides by 10, scaling the sense signal down to 1V range levels, for input to the Sine/Quasi-Sine comparator.

Separate arrangements are made for attenuation and scaling on the 100V and 1kV ranges. These are described in *sub-section 9.6*.

9.4.8.2 10V Range Configuration

On the 10V Range, relays RL14 and RL3 are both energized. Relays RL8, RL11, RL12, RL13, RL15 and RL16 remain un-energized as shown in the diagram.

The 'SENSE HI' signal is routed to the inverting input of the amplifier through the closed contacts of RL14 and resistor R115. With relays RL8 and RL11 not energized, the non-inverting input is referred to SIG LO.

The output from Q31 is returned via R121 as negative feedback to the amplifier input, the contacts of RL12-8/14 being open.

Thus the circuit is configured as an inverting amplifier, resistors R115 and R121 scaling the sense signal down by a factor of 10. Extensive screening is employed at the amplifier's virtual ground, bootstrapped by buffers Q46 and Q41 to follow the virtual-common potential. This reduces the input capacitance, which is further compensated by feedback capacitor C60.

9.5 AC HIGH VOLTAGE LOOPS

The instrument includes two high voltage AC ranges. The 100V ranges extends from 9V to 200V full scale, the 1000V range from 90V to 1100V full scale.

Circuit Diagrams 400844 *page 11.7-1* and 430618 *page 11.9-1* together illustrate the high voltage AC circuit arrangement and indicate signal flow. The details of the 100V and 1000V ranges are described in *sub-sections 9.6 and 9.7*.

9.5.1 AC HIGH VOLTAGE DELIVERY

Both ranges employ the same precision sinewave oscillator and VCA arrangement used for the 1V AC Range, but the techniques necessary to generate high voltages differ from those in the low voltage loops:

- On the 100V range, the AC 1V signal is switched directly into the 100V Amplifier, where it is scaled up by a factor of 100, the amplifier output being delivered via the 'AC 10V+100V' line to the PHI(ACV) line on the AC assembly.
- For the 1000V range the DC Reference is scaled in software, so that the AC 1V signal Full Scale value represents 1100V output. The signal is routed through extra stages of amplification before being applied to the 100V Amplifier, whose output now drives one of two 1:6 step-up transformers (LF or HF). The power-amplifier gain on the 1000V range is controlled by feedback from the transformer secondary, into the input of the 1000V Error Amplifier. The 'AC 1kV' line transfers the transformer output to the AC assembly, where it is switched onto the PHI(ACV) line.

9.5.2 AC HIGH VOLTAGE SENSING

Guarded high-voltage precision attenuators reduce the AC sense voltage from the Hi and Lo terminals to 1V Range levels. The attenuated voltage is compared with the quasi-sinewave voltage, their mean-square difference being used as an error signal to correct the range output level by controlling the gain of the VCA.

9.6 AC 100V RANGE

9.6.1 INTRODUCTION

(Circuit Diagram 430618 page 11.9-1)

The AC 1V signal, generated by the 1V Buffer in the Sine-Source assembly, enters the Power Amplifier as for the 10V range; but the 10V Amplifier is bypassed for the high voltage ranges.

On the 100V range, the signal is switched directly into the 100V Amplifier, where it is scaled up by a factor of 100, the amplifier output being delivered via the 'AC 10V÷100V' line to the PHI(ACV) line on the AC assembly. Thereafter the output is transferred to the instrument terminals as for the 10V range.

9.6.2 AC 100V RANGE POWER ROUTING

(Circuit Diagrams: 430618 pages 11.9-2 and 11.9-3; 400844 page 11.7-1)

'AC 1V' enters the Power Amplifier assembly at J9-36 *(page 11.9-2)*. Relay RL3 is un-energized, shorting the 10V Amplifier input; and RL4 is energized, routing the AC 1V signal to the 100V Amplifier as '100V I/P' *(page 11.9-3)*.

Relay contacts RL2-8/4 apply the signal to the Gain Stage, which provides drive to the power amplifiers in the positive and negative heat sinks, via J3-12 and J3-11. The single-ended output from the heatsinks at J3-9 passes via R89, L7 and relay RL2-13/9, to RL3-6 *(page 11.9-2)*, and onto the 'AC 10V+100V' line via RL4-4/8.

On the AC assembly *(page 11.7-1)*, the signal is routed to the PHI(ACV) line as for the 10V range.

9.6.3 100V AMPLIFIER

The AC 1V signal enters the PA assembly at J9-36, passing to the input of the 100V Power Amplifier via closed relays RL4-9/13 and RL2-8/4. It is referred to Common-2B by developing a voltage across R72.

The 100V Amplifier is described in *Section 7.8*, which deals with the 100V DC outputs.

The description is sub-divided as follows:

9.6.4 POWER SUPPLIES AND PROTECTION

The power supplies and protection for the 100V Amplifier are also described in *Section 7.8.*

The description is sub-divided as follows:

7.8.5 Power Supplies and Protection Introduction
7.8.5.1 ±38V Supply (The 38V supply circuit is also described in Section 6.7, para 6.7.3.4.)
7.8.5.2 ±400V Transformation and Rectification
7.8.5.3 400V Current Control
7.8.5.4 100V Current Sense and 1kV Overvolts Detector (This detector circuitry is used only for AC High Voltage ranges, and is therefore described in sub-sections 9.6.4.1 and 9.7.6.1 below).

7.8.6 PA Power Supply Monitors
7.8.6.1 Comparator Supply Protection
7.8.6.2 ±15V Monitor
7.8.6.3 ±38V Monitor
7.8.6.4 ±400V Monitor

9.6.4.1 100V Current Sense

(Circuit Diagram 430618 Page 11.9-6)

The 400V(2)B lines enter the Power Amplifier assembly from the PS/I Heatsink at J1-8/6 and are filtered by L1 and L2 before being applied across two neon lamps LP1 and LP3. These lamps are visible from the top and rear of the instrument when the PA board is exposed, indicating that a dangerous voltage is present.

The 400V(2)B lines continue on to power the driver stage of the 100V amplifier, where the voltage is regulated as described in *para 7.8.3.4.*

The 400V(2)C lines supply the power amplifier in the Positive and Negative Heatsinks. On the 100V range, the current in each of these lines is used as an analog of the load placed on the amplifier. (On the 1000V range, any overload is sensed by a series detector in the DC assembly.)

The '$\overline{\text{100V AC}}$' line is set to logic-1 (0V) only when the 100V range is selected. Driver Q7 pinches off the FET switch Q6, removing the short from R37, thus allowing the overload detector to operate. In normal use, links LKB and LKC are not connected. Their test purpose is to allow the current mirrors Q1 and Q3 to be powered without the level-shifters Q2 and Q4.

Most of the positive output current for the heatsinks passes through the series combination of R34 and D27, the negative currents through R9 and D4. As both positive and negative circuits are symmetrical, only the positive circuit is described.

Current mirror Q3 diverts approx. 1.8% of the positive supply current into the level-shifter Q4, R36 and into the common reistor R37. Similarly Q1 draws current out of R37. Under no terminal load conditions these two currents are balanced, even if the output voltage is high.

Any AC output load current from the power amplifier is reflected by ripple currents in both positive and negative supplies. The net instantaneous current flowing in R37 alternates in synchronism with the output cycles, its amplitude increasing as the load current increases. So the amplitude of the alternating voltage across R37 is an analog of the output load current, and can be compared against a scaled reference voltage.

A window comparator is formed from the two halves of M2 and the voltage across R37 is applied to both halves. The outputs at M2-12 and M2-7 are uncommitted. Each half is biassed by 2.45V in the correct polarity, provided by the reference zeners D9 and D17 in the 400V Monitor circuit. Unless any voltage peak across R37 exceeds this level, both M2 outputs will be pulled to 0V by R20.

The '$\overline{\text{100V FLAG}}$' line (TP2) therefore remains at logic-1.

Any peak greater than 2.45V overcomes the bias on one half, causing its output to fall to -15V, resulting in the $\overline{\text{100V FLAG}}$ line being pulled to logic-Ø. This signal sets limit detector latch M5a *(page 11.9-5)*, as described in *para 7.12.7.1.*

9.7 AC 1000V RANGE

9.7.1 INTRODUCTION

(Circuit Diagram 430618 page 11.9-1)

The AC 1V signal, generated by the 1V Buffer in the Sine-Source assembly, enters the Power Amplifier as for the 10V range; but the 10V Amplifier is bypassed for the high voltage ranges.

On the 1000V range, the signal is switched via the 1kV x2 Amplifier and 1kV Error Amplifier, before being applied to the 100V Amplifier.

The 100V Amplifier output is stepped up to 1000V Range levels by one of two (LF or HF) transformers, whose secondary voltage is delivered via the 'AC 1kV' line to the PHI(ACV) line on the AC assembly. Thereafter the output is transferred to the instrument terminals as for the 10V range.

9.7.2 1000V RANGE POWER ROUTING

(Circuit Diagrams: 430618 pages 11.9-2 and 11.9-3; 400844 page 11.7-1; 430537 page 11.14-1)

'AC 1V' enters the Power Amplifier assembly at J9-36 *(page 11.9-2)*. Relay RL3 is un-energized, shorting the 10V Amplifier input; and RL1 is energized, routing the AC 1V signal to the 1000V Amplifier chain.

Energized relay contacts RL1-8/4 apply the signal to the Gain x2 Stage, whose output is summed with error feedback, providing drive to the 1kV Error Amplifier.

The 1kV Error Amplifier output is passed as '1kV ERROR O/P' via relay RL1-9/13 to the 100V Amplifier *(page 11.9-3)*. It is input through the contacts of un-energized relay RL2-6/4.

The output from the heatsink at J3-9 is transferred directly, as the 'OUTPUT' signal, to the '1kV ENABLE' relay contacts RL6-8 and RL6-9 *(page 11.9-2)*. Relay RL7 determines whether the LF or HF transformer assembly is to be used, the OUTPUT signal being applied to the appropriate primary winding.

The secondaries of both transformers are connected into the High Voltage assembly *(page 11.14-1)*. Relay RL2 or RL3 selects the appropriate output to be passed on to the AC assembly, via J1-28 and J1-22, as the AC 1kV signal.

The AC 1kV signal is also applied as the negative 'Error' feedback to the 1000V amplifier system. It passes through R138 and R155 on the PA assembly *(pages 11.9-1 and 11.9-2)*, to be summed at the inverting input of M18a-2. A single net inversion is present around this loop.

On the AC assembly *(page 11.7-1)*, the AC 1kV signal is routed by the contacts of energized relay RL20, and through fuse F2 to the PHI(ACV) line at J7-27.

9.7.3 1kV POWER AMPLIFIER

(Circuit Diagram 430618 page 11.9-1)

Amplification to a maximum of 1100V is in four stages:

1. Gain x2 Stage: the AC 1V signal is HF-boosted and amplified. For the 1000V range the DC Reference is scaled in software, so that the AC 1V signal Full Scale value represents 1100V output.
2. **1kV Error Amplifier:** the Gain x2 Stage output is summed with error feedback from the secondary of the step-up transformer.
3. **100V Amplifier:** possessing a gain of 100, the output from its heatsinks drives one of two (LF or HF) step-up transformers.
4. **Step-up Transformer:** a ratio of 1:6.6 (LF) or 1:6.17 (HF) allows sufficient gain in the system to provide a maximum RMS output of 1100V.

The frequency response of the amplifier is matched to the step-up transformer in use. The 'LF' signal into the amplifier is at logic-1 (0V) only when the 1kV range, and either the 100Hz or the 1kHz frequency range, is selected.

9.7.3.1 Gain x2 Stage

(Circuit Diagram 430618 page 11.9-2)

The AC 1V signal is routed via relay RL1-8/4 to be developed across resistor R160. It is filtered by R162/C30 and applied to the non-inverting input of M15.

The feedback divider generates the x2 gain in M15; R159 and C67 providing HF lift to compensate the step-up transformer responses. FET Q35 adds C68 on the 100Hz and 1kHz frequency ranges, activated by the LF signal at logic-1, to boost the lift.

Output from the x2 stage is applied to the 1kV Error Amplifier via its input resistors R156/R95.

9.7.3.2 1kV Error Amplifier

The input resistance to M18a is split between R156 and R95 to allow the saturation detector to reduce the gain in the event of transformer saturation.

At the inverting input of M18a the signal input is summed with the AC 1kV negative feedback signal, output from the selected transformer secondary. The resulting error signal is amplified by the two stages of M18.

On the 100kHz frequency range, the maximum voltage available from the instrument is 750V. A tapping on the HF step-up transformer secondary reduces the maximum output to this level. The signal '1kV GAIN' is thus set to logic-Ø only on the 100kHz range, cutting off FET Q19 and restoring adequate loop gain.

The second stage, M18b, adjusts the bandpass of the amplifier to match the selected step-up transformer:

100Hz and 1kHz ranges:
Q26 connects C58 and R126 across the input resistor R97; relay RL5 shorts R48, connecting C34 and R93 directly across the feedback resistor R92, also shorting C38 in the output line.

10kHz and 100kHz ranges:
Q26 connects C57 and R125 across the input resistor R97; relay RL5 shorts R47, connecting C33 and R94 directly across the feedback resistor R92, and leaves C38 dominant in the output line.

These measures give the necessary loop compensation for each transformer.

When the 1000V range is selected the amplifier output drives the 100V Amplifier via RL1-9/13 as the '1kV ERROR O/P' signal.

9.7.4 100V AMPLIFIER

This operates as for the 100V range, but its output signal 'OUTPUT' is fed directly to relay RL6 contacts for application to the step-up transformer.

The 100V Amplifier is described in *Section 7.8*, which deals with the 100V DC outputs.

The description is sub-divided as follows:

7.8.3 100V Amplifier Introduction
7.8.3.1 Input to Gain and Driver Stages
7.8.3.2 DC Offset Correction
7.8.3.3 Signal Processing
7.8.3.4 Driver Regulator
7.8.3.5 Driver Output

7.8.4 100V Power Amplifier
7.8.4.1 Positive Heatsink Assembly
7.8.4.2 Negative Heatsink Assembly
7.8.4.3 Over-Temperature Detection
7.8.4.4 100V Output Connection
7.8.4.5 Heatsink Removal

9.7.5 STEP-UP TRANSFORMER CIRCUITRY

9.7.5.1 '1kV ENABLE' Relay RL6

Relay RL6 allows the OUTPUT signal from the 100V Amplifier to energize a step-up transformer, providing the following conditions are met:

The $\overline{\text{1kV}}$ signal is at logic-Ø:
This is a processor-controlled signal, set to logic-Ø when the instrument AC output is switched on, in the 1000V range.

The watchdog has not 'Barked'.

On the PA assembly, the '1kV ENABLE' switch S1 is set to 'ENABLE'.
S1 is situated below the left-hand ejector lever (viewed from the front of the instrument), facing the rear of the instrument. It allows the high voltage to be switched off for servicing purposes. A red LED glows when all other conditions are met.

When RL6 is closed, the OUTPUT signal from the 100V Amplifier is switched through to the contacts of RL7.

9.7.5.2 LF/HF Transformer Selection

Relay RL7 is activated by the 'LF' signal, applying the 100V amplifier output to the HF step-up transformer for the 10kHz and 100kHz frequency ranges, and to the LF transformer for the 100Hz and 1kHz ranges.

The two transformers are separately located, their secondaries being connected into the High Voltage assembly. The HF transformer is selected when RL7 is un-energized, its primary being returned to Common-2C. RL7 is energized to select the LF transformer, whose primary current is sensed by the Saturation Detector.

9.7.5.3 Saturation Detector

To obtain the required performance, the LF transformer core is constructed from a material with high remanence. It is possible for the 1kV range to be deselected when the core is magnetized, and subsequently reselected in the same sense, with resultant saturation.

The Saturation Detector circuit is activated by sensing any excess primary current in R114, associated with the loss of reactance. It progressively removes the signal input to M18b during half cycles of the appropriate sense until the core recovers, then automatically returns to its quiescent mode.

The dual amplifier M20 is biassed by R115-R118 to approximately 1V on each input. Under normal operating conditions, the unsaturated core reactance holds R114 current down, so the voltage developed across R114 is insufficient to overcome the bias. The output from both amplifiers is of negative polarity, both diodes D58 and D59 are reverse-biassed, and FET Q18 is cut off by its gate being pulled down to -15V.

When the core saturates, the current in R114 rises rapidly and its voltage exceeds the bias on one of the detector amplifiers. One diode conducts, forcing Q18 into conduction; so the signal feed to M18a is shorted, the current in the transformer core is reduced to zero, and Q18 is cut off again.

On the next half-cycle the current is reversed, so saturation is reduced. If the core saturates on successive half-cycles, they again activate the detector with further reduction. The process continues until the core remains unsaturated over the full dynamic range of the primary current, when the detector becomes inactive.

9.7.6 POWER SUPPLIES AND PROTECTION

The power supplies and protection for the 100V Amplifier are described in *Section 7.8.*

The description is sub-divided as follows:

7.8.5 Power Supplies and Protection Introduction
7.8.5.1 ±38V Supply (The 38V supply circuit is more fully described in Section 6.7, para 6.7.3.4.)
7.8.5.2 ±400V Transformation and Rectification
7.8.5.3 400V Current Control
7.8.5.4 100V Current Sense and 1kV Overvolts Detector (This detector circuitry is used only for AC High Voltage ranges, and is therefore described in sub-sections 9.6.4.1, and 9.7.6.1 below).

7.8.6 PA Power Supply Monitors
7.8.6.1 Comparator Supply Protection
7.8.6.2 ±15V Monitor
7.8.6.3 ±38V Monitor
7.8.6.4 ±400V Monitor

9.7.6.1 AC 1kV Overvoltage Detector

(Circuit diagram 430618 Page 11.9-6)

On the 1000V Range the primary voltage of the step-up transformer in use is fed as 'AC OVERVOLTAGE DRIVE' from RL6-4/13 *(page 11.9-2)*, via R176 and a screened lead, to the M2 comparator input *(page 11.9.6)*. (The operation of the comparator is described for the 100V Current Sense application in *Section 9.6, para 9.6.4.*) On the 1000V Range, Q6 shorts the 100V overcurrent sense resistor R37; Q6 gate is driven by $\overline{\text{100V AC}}$ at logic-1.

The HF (1:6.17) step-up transformer primary voltage is divided by R176 and R180 (i.e. by 1/116), but for the LF (1:6.6) transformer R181 shunts R180 (increasing the division ratio to 1/124.5), activated by the $\overline{\text{LF}}$ signal and Q43. The result is that overvoltage is detected on the HF transformer primary at approximately 305V, but on the LF transformer primary at approximately 285V. Taking the step-up ratios into account, the 1kV Overvolts Detector trips at LF or HF for the same secondary voltage: approximately 1880V peak, 1330V RMS. This in turn activates the $\overline{\text{100V FLAG}}$ signal as on the 100V Range.

9.7.6.2 AC 1kV Overcurrent Detector

(Circuit Diagram 430536 Page 11.5-2)

For the AC 1000V range, so as to protect the step-up transformers, overloads are detected directly in the output lines to the terminals. For this range only, resistance is inserted in the PHI(ACV) line in the DC assembly. The voltage across the resistance is rectified and compared against a reference. If the voltage is excessive, the comparator generates a LIM DET signal. At higher frequencies, where the internal and external connections to the load will draw extra capacitive current, part of the resistance is short circuited.

The 'AC 1kV RANGE' signal enters at J5-102 *(page 11.5-3)*. This is at logic-1 to energize relay RL13, only if the 1000V range is selected. RL13 removes the short from R107 and R108.

The 'HIGH I LIMIT' signal enters at J5-98 *(also on page 11.5-3)*. When the 1000V range is selected, this is at logic-1 only for the 10kHz and 100kHz frequency ranges. It energizes relay RL12, shorting R108, so that higher currents are required to trip the LIM DET signal. As frequency increases, so do the currents taken by the capacitance of the internal tracking and wiring; R107 is compensated by C45 and C49 to bypass this extra capacitive loading.

A diode-bridge rectifies the voltage developed across the selected resistor(s). The voltage is limited to 10V by D31, and resistor R84 sets the trip current level for the opto-isolator M19.

The isolator operates from the 5 volts between -10V and -15V. In normal operation M19 output at M19-6 is open-collector so Q4 does not conduct. When the output current is sufficient to trip M19, Q4 emitter is pulled low and so Q4 conducts, its collector current being drawn through R79.

M18 is a switch which under no-overload conditions is biassed by R79 to +15V; and with its output at -15V, its non-inverting input is set to approx. -2V. When Q4 conducts, its collector is pulled down close to the -15V rail voltage. This is applied to the inverting input of M18, whose output reverses to +15V providing a positive trigger edge to M12-4.

For AC outputs the $\overline{\text{DC FNCT}}$ signal is inactive at logic-1, M12-3 at logic-1 removes the reset which is present for all DC voltage ranges. Monostable M12 is set to produce a logic-Ø at its Q output (M12-6) unless its A input at M12-4 is edge-triggered positively. In normal conditions no trigger is given, so M12-6 remains at logic-Ø, D10 is unbiassed and the LIM DET line remains at the logic-Ø level of -15V.

When M18 output reverses to +15V, M12-6 produces a logic-1 (0V) pulse of 1ms duration, which forward-biasses D10, so the LIM DET line transmits a logic-1 pulse of 1ms duration. Successive positive or negative peaks of overcurrent retrigger the monostable, maintaining its Q output (and thus the LIM DET signal) at logic-1.

9.8 AC HIGH VOLTAGE SENSING

(Circuit Diagram 400844 Pages 11.7-1 and 11.7-2)

The SHI(ACV) signal, returned from the terminals via the Current and Output Control assemblies, enters the AC assembly as for the 10V range; but the 1V/10V Sense Amplifier is bypassed for the high voltage ranges.

On these ranges, the signal is switched into one of two guarded attenuators, both housed in the Attenuator/Cage assembly plugged directly into the AC assembly. Each attenuator is a separate resistor chain which acts as the input resistor to the inverting amplifier M32. The output of the amplifier is passed to the Comparator Transfer switch.

9.8.1 100V SENSE AMPLIFIER

The SHI(ACV) signal passes through the contacts of energized relays RL19 and RL15, and is applied via the four pins of J1 into the 100V attenuator chain. The attenuator consists of four 25kΩ 0.1% resistors in series. To eliminate leakage, each junction between the resistors is guarded, the guards being taken to equivalent voltage points on a chain of four capacitors, C64 to C67. The capacitive chain is also driven from the sense signal. The attenuator acts as the input resistor for the 100V/1000V Sense Amplifier M32.

Relay RL13 is un-energized on this range, so R124 acts alone as the feedback resistor, producing an amplifier gain of 1/100. The sense signals are thus reduced to 1V range levels. The amplifier output is routed through the contacts of un-energized relay RL3 as the comparator 'SIG' input, to transfer switch M16-11 *(page 11.7-3)*.

9.8.2 1000V SENSE AMPLIFIER

The SHI(ACV) signal is blocked by the contacts of un-energized relay RL15, but RL16 is energized, applying SHI(ACV) as the '1kV SENSE' signal via link LK1 into the 1000V attenuator chain. The chain has ten 50kΩ 1% resistors in series, which combine to form the input resistance for M32. The guards are taken to equivalent voltage points on a chain of eight capacitors, C70 to C77, again driven from the sense signal.

Relay RL13 is energized on the 1000V range, so R123 and R124 act in parallel as the feedback resistance, giving a gain of 1/550. The sense signals are thus reduced to 1V range levels (the 1000V range FS voltage is 1100V; the equivalent 1V range FS voltage is 2V). The amplifier output passes to the transfer switch as on the 100V range.

9.9 SINE/QUASI-SINE RMS COMPARATOR

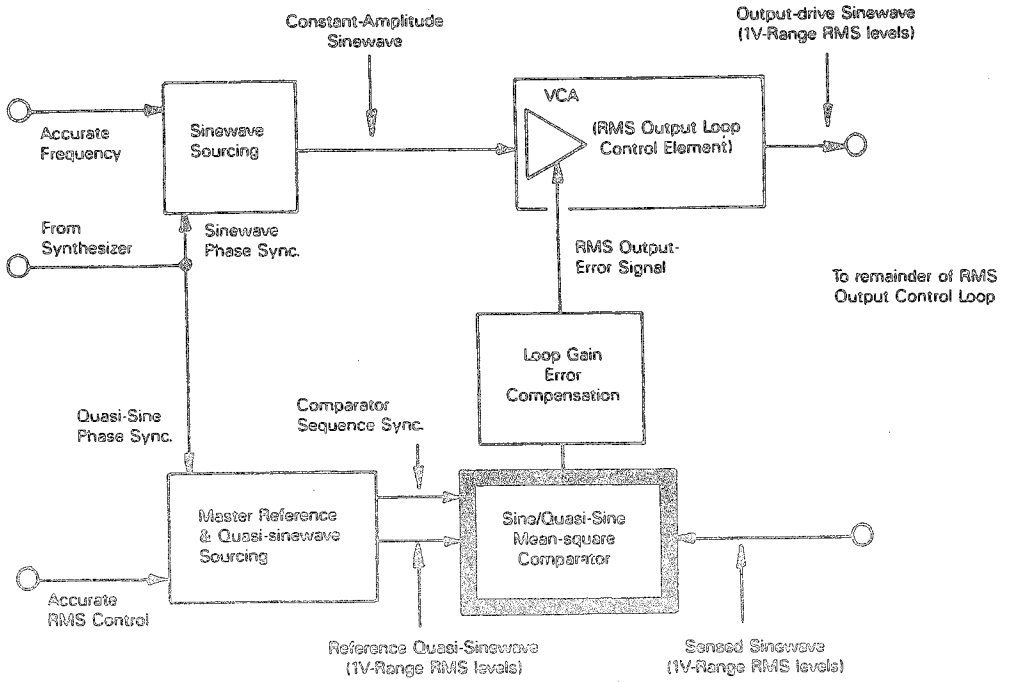


FIG. 9.9 THE SINE/QUASI-SINE COMPARATOR AND ITS SYSTEM ENVIRONMENT

9.9.1 PURPOSE AND ENVIRONMENT

(Fig. 9.9)

The VCA acts as the control element of the Fine Amplitude Control Loop, having variable gain which is adjusted to change the output value.

The main purpose of the comparator, in conjunction with the coarse amplitude control, is to cause the output RMS value to track the value set on the front panel OUTPUT display. It generates a DC error voltage which adjusts the VCA gain.

Because it is part of the fine amplitude control loop, the comparator also corrects output RMS changes due to loading and other disturbances, within the instrument specification.

The Comparator receives two analog inputs:

a. The reference quasi-sinewave whose RMS value is set by the value on the OUTPUT Display, and is also modified by stored calibration data *(sub-section 6.6)*.

b. The sensed and conditioned output sinewave, which is compared against the reference quasi-sinewave *(sub-sections 9.4 and 9.5)*.

The Comparator output is the DC error voltage resulting from the difference between the mean-square values of the two inputs. As the VCA gain (and hence the output RMS level) is adjusted, the RMS value of the comparator's sense input approaches that of the reference, and the error voltage is driven towards zero. The output value stabilizes when the RMS values of the two inputs are equal.

The buffered DC error signal output from the comparator is adjusted in approximately 1000ppm FS steps by the action of the Coarse Amplitude DAC, to give a virtually constant loop gain. The effects are described in *sub-section 9.3*.

9.9.2 IMPLEMENTATION

Both inputs are scaled to 1V Range levels and compared in an Integration/Sample-and-Hold system. They are sequentially steered through a common squaring circuit into separate 'REF' (Reference^2) and 'SIG' (Reference^2 *minus* Sense^2) averaging integrators.

A capacitor and voltage follower samples and holds the settled REF integrator voltage. It generates a DC 'REF^2' signal which is subtracted from the AC 'SIG^2' signal. The result is applied to the SIG integrator, then another sample-and-hold circuit generates the 'AC ERROR' signal from the integrator's output.

'AC ERROR' is thus a DC analog of the difference between the 'mean-square' values of the two inputs. It is buffered and applied to the VCA via the Error Amplifier.

9.9.3 METHOD OF COMPARISON

(Figs. 9.10 and 9.11)

The comparator is based on a ten-state recycling sequence of squaring, integration, sampling and subtraction. Operation and accuracy rely heavily on synchronization between sine and quasi-sine.

At relevant points in the following description, reference is made to a specific output frequency of 500Hz (1kHz Range), as an example to clarify the following points:

a. As the output sinewave frequency is varied, the quasi-sinewave tracks an exact sub-multiple of its frequency; except on the 100Hz Range, where both are at the same frequency. In our example at 500Hz, the quasi-sinewave has half the output frequency. The various relationships between output and quasi-sinewave frequencies for different frequency ranges are detailed in *Section 8, Table 8.3*.

b. The duration of each comparison cycle is always equal to ten quasi-sinewave periods (here 40ms), and each of the 'C' periods persists for one quasi-sinewave period (for 500Hz output - 4ms). This effect can be observed using an oscilloscope, say at TP46.

c. Using this specific case also gives a point of reference for examination of the circuit waveforms using an oscilloscope.

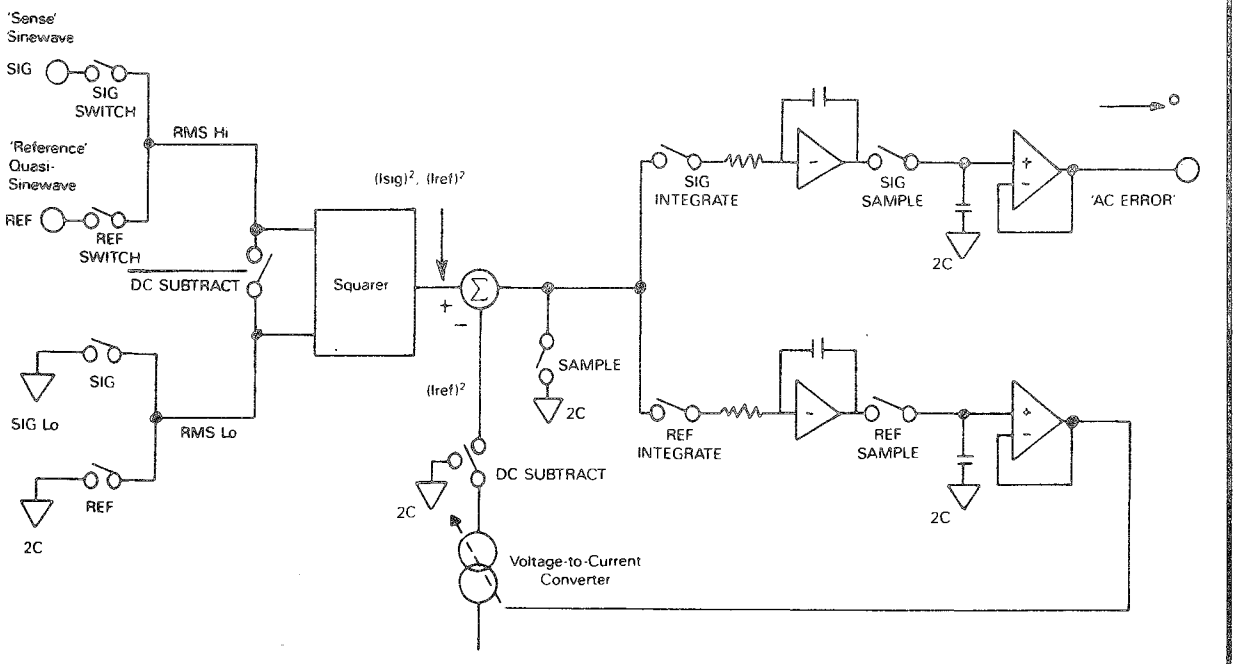


FIG. 9.10 SINE/QUASI-SINE COMPARATOR - BLOCK DIAGRAM

9.9.3.1 The Comparator Sequence

(Figs. 9.10 and 9.11)

The table in *Fig. 9.11* shows the conduction patterns of the switches in the block diagram of *Fig. 9.10*, within a complete sequence cycle. The cycle is broadly divided into two similar patterns ('REF' and 'SIG'), each occupying five quasi-sinewave periods. The cycle repeats continuously.

In the following analysis, the effects of the closed switches are described; all other switches are open.

'X' indicates that switch is closed	COMPARATOR CYCLING PERIODS									
	C 1	C 2	C 3	C 4	C 5	C 6	C 7	C 8	C 9	C Ø
STATES	REFERENCE PATTERN					SENSE (SIG) PATTERN				
(a) Squarer input	quasi-sine			zero		sine			zero	
(b) REF SWITCH	X	X	X							
(c) REF INTEGRATE	X	X	X	X						
(d) REF SAMPLE					X					
(e) SIG SWITCH						X	X	X		
(f) SIG INTEGRATE						X	X	X	X	
(g) SIG SAMPLE										X
(h) DC SUBTRACT	X	X	X			X	X	X		
(j) $\overline{\text{DC SUBTRACT}}$				X	X				X	X
(k) REF SWITCH					X					X
(l) REF SWITCH	COMMON-2C					SIG LO				2C

FIG. 9.11 SINE/QUASI-SINE COMPARATOR - SEQUENCE CYCLE

Periods C1, C2 and C3

a. REF SWITCH is closed to input the quasi-sinewave to the squarer.
b. REF INTEGRATE steers the squarer output current into the Reference Integrator.
c. DC SUBTRACT allows $Iref^2$ to be drawn from the summing junction.
d. RMS Lo has been connected to common 2C since the start of CØ in the previous period, in preparation for REF squaring.

The quasi-sinewave is squared, and the result is output as a current (at twice the input frequency) into the summing junction. The DC current $Iref^2$ is subtracted at the junction, and the residue goes to charge the Reference Integrator capacitor.

(Note that every time that OUTPUT OFF is selected, REF and SIG integrator capacitors are discharged, driving both 'AC ERROR' and '$Iref^2$' to zero. During the first REF integration when OUTPUT ON is next selected, $Iref^2$ remains at zero so the integrator capacitors start charging from zero.)

Period C4

a. REF SWITCH is opened, removing the input to the squarer.
b. DC SUBTRACT is opened, subtraction ceases.
c. DC SUBTRACT closes to input a hard zero to the squarer.
d. REF INTEGRATE remains closed, allowing the squarer and integrator to settle.
e. RMS Lo remains connected to Common-2C until the integrator has settled.

The REF integrator remains in its integrating (on) condition during period C4, to ensure that any energy stored in the squarer during C1 to C3 is acquired.

DC subtraction during period C4 would generate an error, as full subtraction was already applied during period C1. DC SUBTRACT is therefore turned off by transferring the source of $Iref^2$ from the summing junction to Common-2.

Period C5

a. REF INTEGRATE opens, stopping the integrator action.
b. SAMPLE closure forces the squarer output to a hard zero, to nullify any leakage effects in the integrator switch.
c. REF SAMPLE closes, and current from the integrator op-amp charges the sampling capacitor to the integrator capacitor voltage.
d. RMS Lo is switched from the Ref Common-2C to the Sense SIG Lo in preparation for SIG squaring.

As the sampling capacitor changes its charge, its voltage-follower drives the voltage-to-current converter to change the DC subtraction current. The new $Iref^2$ is sourced from Common-2 during this period, but during the next SIG and REF integration periods, it will be subtracted from the squarer output current at the summing junction.

Periods C6 to CØ

As can be seen from *Fig. 9.11*, the closure pattern is repeated for SIG squaring, integration and sampling. The SIG circuit action is identical to REF, except that:

a. the squarer input is now the sensed sinewave.
b. the subtraction current has been set to a new value during period C5. This does not change again until period C5 of the next cycle.
c. During period CØ, the 'AC ERROR' output from the SIG sample-and-hold voltage follower is changed, updating the VCA gain via the Error Buffer and Error Amplifier.
d. RMS Lo was switched from Common-2C to SIG Lo during period C5 in preparation for SIG squaring. It remains connected to SIG Lo during the squaring periods C6, C7 and C8, and also during period C9 for the Sig Integrator settling. At Period CØ it is reconnected to Common-2C in preparation for REF squaring.

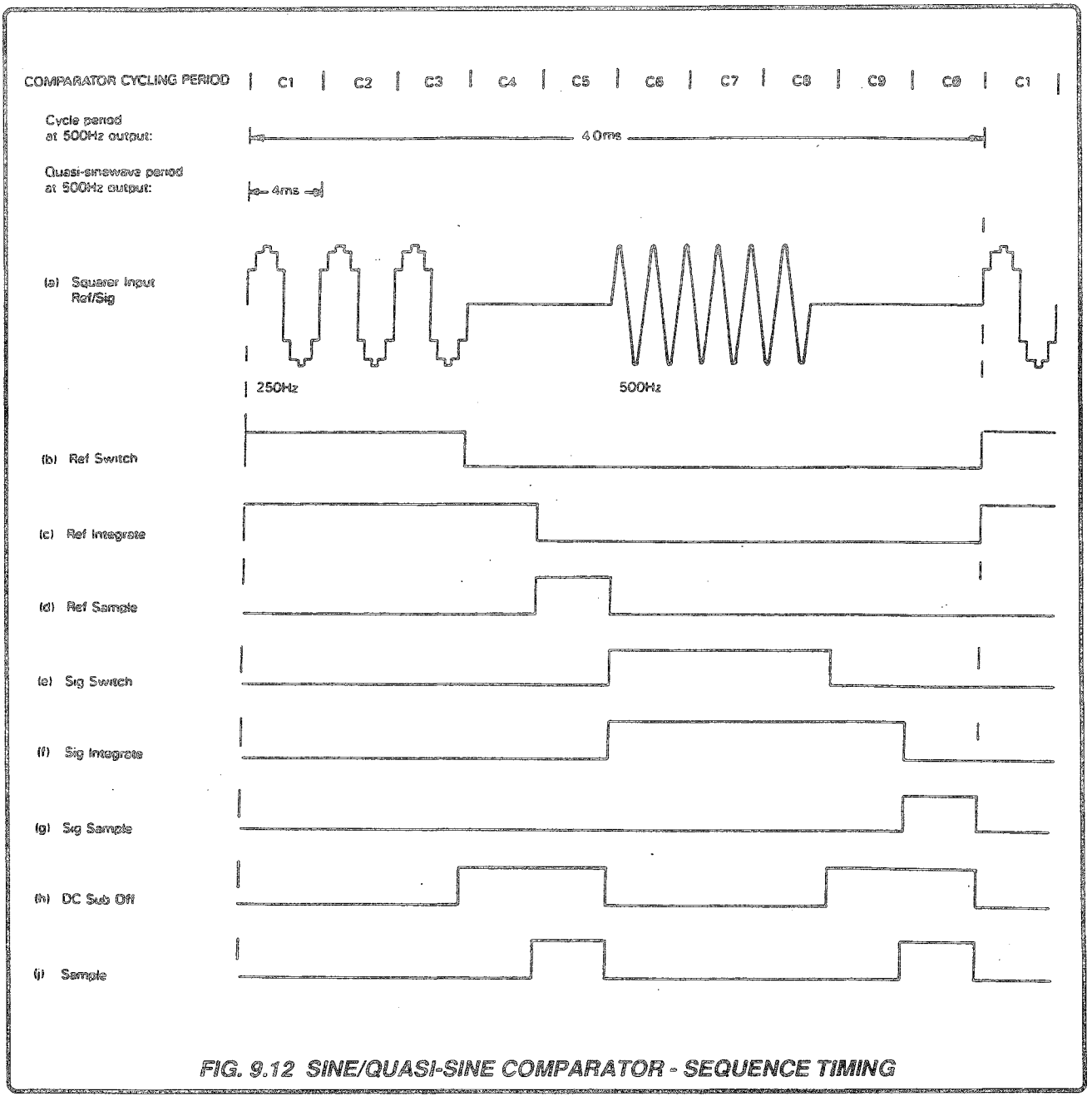


FIG. 9.12 SINE/QUASI-SINE COMPARATOR - SEQUENCE TIMING

9.9.3.2 Comparator Action

The sequence described in 9.9.3.1 is necessarily simplified. When a new output demand changes the amplitude of the quasi-sinewave, a few sequence cycles are required to stabilize the conditions of the Ref integrator, Sig integrator, subtraction current and AC ERROR output. The circuit must also respond to demands for reduced output in addition to those for increases.

The comparator forms part of the output amplitude control loop, ultimately affecting the output voltage and hence the sensed voltage input to the squarer as 'SIG'. As the sequence recycles, the mean-square value of the SIG input sinewave will approach that of the REF quasi-sinewave, and as it does so the AC ERROR output must approach a steady-state value.

The squarer output current has an AC component in its waveform, but $Iref^2$ being subtracted at the summing junction is a DC current. In the settled condition, $Iref^2$ is driven on successive cycles to balance the quasi-sinewave REF^2 AC current (being applied to its integrator) about zero. The final level of $Iref^2$ is just sufficient to be self-sustaining.

Meanwhile, the sensed SIG^2 current approaches the REF^2 value, and the same $Iref^2$ is a DC analog of the quasi-sinewave mean-square voltage. In the output loop, the VCA is driven until the instrument output (and sensed SIG input) is at the correct level just to generate a self-sustaining 'AC ERROR'.

In the comparator, $Iref^2$ is subtracted from both SIG^2 and REF^2 currents. This maintains the AC AMPL ERROR as an analog of the difference between the quasi-sinewave and the output sinewave mean-square voltages (when the latter is reduced by sense conditioning to 1V Range levels). Thus when the sensed SIG input voltage approaches the quasi-sinewave REF voltage (mean-square values), the AC ERROR approaches stability and the system settles.

A further complication: a bias is applied to the squaring circuit to avoid distortion by maintaining permanent conduction. The bias is controlled by the value of the positive reference voltage, and a bias current is superimposed on the subtraction current. These factors will be discussed later during the circuit analysis.

9.9.4 COMPARATOR CONTROL LOGIC

(Circuit Diagram 400844 page 11.7-3)

The Comparator operating cycle originates at M15, which is a 10-bit sequencing counter, clocked at the quasi-sinewave frequency by the carry-out from M11-12.

The SYNC Ø input to M15 RESET is a decoded address, whose function at logic-1 is to disable counters M11 and M15, inhibiting operation of the comparator and generation of the quasi-sinewave. In this instrument, SYNC Ø is held permanently at logic-Ø, enabling both quasi-sinewave and comparator for AC Voltage and Current functions.

The clock continuously recycles M15 in ascending count through $Q_Ø$ to Q_9, ten clocks (ie ten quasi-sinewave periods) constituting one cycle of the comparator sequence. Only one 'Q' output is at logic-1 (+8V) at a time, the remainder being at logic-Ø (-8V).

With increase of frequency range, the difference between the frequencies of sensed sinewave and reference quasi-sinewave increases in decade steps. As the comparison is performed at mean-square levels, this frequency difference does not matter, so long as the sinewave is at an exact multiple of the quasi-sinewave frequency. However, to optimize the operation of the Sense/Reference comparator, the zero crossings of the quasi-sinewave are synchronized to occur coincident with a sinewave zero crossing, and all comparator state changes are also synchronized to sinewave zero-crossings.

Synchronization is achieved by clocking M17 so that all the analog switching data changes simultaneously. Thus data is latched from M17 'D' inputs to its permanently-enabled outputs, one complete quasi-sinewave period after it was clocked through M15. This ensures that the transit times of M15, M18 and M20 do not affect synchronism with the quasi-sinewave zero-crossing.

The data is thus strobed through M15 and M17, being delayed by one clock period. This does not affect the operation of the comparator, although it must be accounted for when observing waveforms on an oscilloscope.

The sequence, as described earlier in *sub-section 9.9.3*, begins with REF SWITCH connecting the quasi-sinewave to the squarer input during period C1. The logical origin of the comparator switch state during C1 corresponds to M15-2 (Q1 output) at logic-1; but because of the data delay its actual timing is coincident with the Q2 output of M15-4 at logic-1.

9.9.5 COMPARATOR TIMING LOGIC

(Fig. 9.13)

The comparator timing waveforms for the sequence are illustrated in *Fig. 9.13*. To highlight the data delay, the main waveforms are grouped into two blocks: 'REF' and 'SIG', each headed by the states of the comparator cycle. *Line (b)* shows which of M15 (Q) outputs is at logic-1 during each of the states. It can be seen that the effects of M15 output states are delayed by 1 clock period, in the translation to comparator states.

9.9.5.1 Squarer Commons Switching

['REF' and 'SIG' waveforms (d) and (k)]

Waveform (c) shows the variation of M15-12 (Cout). *Waveforms (d) and (k)* are the direct results of Cout inputs to M17 after the translation by one clock shift (note the inversion at M20-10).

During states CØ to C4, *waveform (d)* at logic-1 connects the squarer common (RMS Lo) to Common-2 at M16-4 for quasi-sinewave squaring; whereas during states C5 to C9, *waveform (k)* connects RMS Lo to SIG Lo at M16-8 for sensed sinewave squaring. In both cases, the appropriate common is connected one period ahead of the squarer input, and disconnected at the end of the integrator settling time.

9.9.5.2 Squarer Input Switching

['REF SW' and 'SIG SW' waveforms (e) and (l)]

M15 outputs Q1 to Q3 are 'OR' gated at M18-6 and applied as D2 input to M17. The result is to generate the REF SW *waveform (e)* at M17-7.

REF SW connects the quasi-sinewave as input to the squarer by M16-13 only during states C1 to C3.

Similarly, SIG SW waveform (l), logically derived from M15 outputs Q6 to Q8, is at logic-1 only during states C6 to C8, inputting the sensed sinewave as input to the squarer by M16-12.

9.9.5.3 Integration and Sample Switching

['INT' and 'SAMPLE' waveforms (f) and (h)]

At any instant, the comparator is either sampling or integrating. The INT waveform is thus the inverse of the SAMPLE waveform.

SAMPLE

M15 outputs QØ and Q5 are 'OR' gated at M18-9 and applied as D3 input to M17. The result is to generate the SAMPLE *waveform (h)* at M17-10.

Therefore, for CØ and C5 only, SAMPLE provides two enabling inputs to AND gates M13 at M13-2 and M13-5. It also places a hard zero on the squarer output by M7-5 *(page 11.7-4)* when this is disconnected from both integrator inputs. With both input and output at zero volts, any offsets are removed in preparation for the subsequent squaring and integration sequence.

INT

The 'SAMPLE' output of M18-9 is inverted at M20-4, applying logic-1 to the D1 input of M17 for the whole of the cycle except for CØ and C5. The INT output at M17-5 is *waveform (f)*, which enables M13-1 and M13-13.

REF INT

INT is 'AND-gated' with REF *waveform (d)* at M13-11 to generate the 'REF INT' *waveform (g)*, which is at logic-1 only during periods C1 to C4. During this time M7-12 *(page 11.7-4)* at logic-1 connects the squarer output to the REF Integrator input.

SIG INT

INT is 'AND-gated' with SIG *waveform (k)* at M13-10 to generate the 'SIG INT' *waveform (m)*, which is at logic-1 only during periods C6 to C9. During this time M7-6 *(page 11.7-4)* at logic-1 connects the squarer output to the SIG Integrator input.

REF SAM

'SAMPLE' is 'AND-gated' with SIG *waveform (k)* at M13-4 to generate the 'REF SAM' *waveform (j)*, which is at logic-1 only during state C5. During this time driver M6-1 at logic-1 causes FET Q2 to conduct *(page 11.7-4)*, connecting the REF Integrator output to the REF Sample-and-Hold input.

SIG SAM

'SAMPLE' is 'AND-gated' with REF *waveform (d)* at M13-3 to generate the 'SIG SAM' *waveform (n)* which is at logic-1 only during state CØ. During this time driver M6-7 at logic 1 causes FET Q3 to conduct *(page 11.7-4)*, connecting the SIG Integrator output to the SIG Sample-and-Hold input.

9.9.5.4 DC Subtraction

['DC SUBTRACT OFF waveform (p)]

Subtraction is required only when either input is being applied to the squarer. As REF SW and SIG SW already exist, it remains only to provide an OR function to join them. The analog circuits need an inverted waveform, so a NAND gate is used. For loading purposes two elements of M20 are connected in parallel: REF SW and SIG SW are combined as *waveform (p)* at M20-3 and M20-11.

Squarer Input Short

When at logic-1 during C4-C5 and C9-CØ, M7-13 places a hard short between RMS Hi and RMS Lo; otherwise the short is released.

Subtraction Current Control

During C1 to C3 and C6 to C8, DC SUBTRACT OFF at logic-Ø cuts off D8 *(page 11.7-4)*, allowing Q6 to draw subtraction current through D6, D5 and R54. When at logic-1, D8 conducts and sets D5 and D6 in reverse bias, diverting the subtraction current.

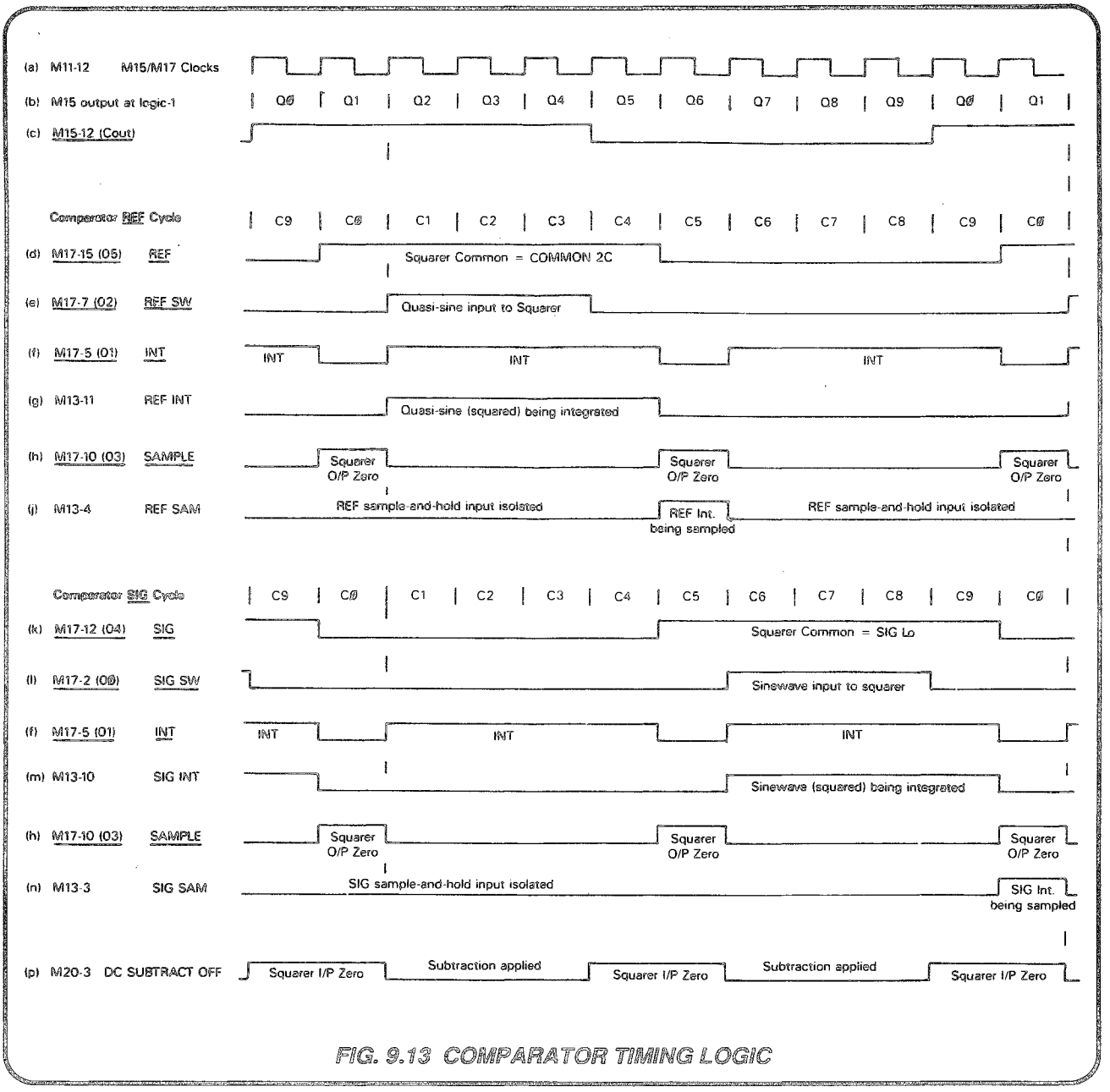


FIG. 9.13 COMPARATOR TIMING LOGIC

9.9.6 SQUARE LAW DETECTOR CIRCUIT

(Circuit Diagram 400844 Page 11.7-4 and DC400842 Page 11.7-8)

The basic action of the squaring circuitry is the same as is used for $\sin^2$ and $\cos^2$ in the Sinewave Oscillator amplitude loop, but there are some differences in detail *(refer to sub-section 8.2)*.

The Square detector is biassed in such a way that it is permanently turned on, to improve bandwidth and permit control of gain scaling. Its differential output voltage at Q109 and Q110 collectors is proportional to the square of its input voltage, divided by the bias voltage. The bias is derived from the DC version of the demanded signal level REF+ve, the DC output from the reference divider.

Thus the transfer proportionality of the signal magnitude is given by:

$$\text{Vout is proportional to } \text{Vin}^2 / \text{Vbias}$$

but as Vbias is derived from REF+ve,

$$\text{Vin} / \text{Vbias is a constant: k,}$$

and the instantaneous squarer gain is:

$$\frac{d(\text{Vout})}{d(\text{Vin})} = \frac{d(\frac{k\text{Vin}^2}{\text{Vin}})}{d(\text{Vin})} = 2k$$

Thus the basic gain equation has no amplitude or frequency components, so is constant over a wide bandwidth and dynamic range. The squarer therefore has a fast response at all signal levels.

The bias is applied as currents to Q116 and Q117 emitter circuits. The transistors in the array of M22 are all used as current generators.

9.9.6.1 Bias Control

The input to Reference Amplifier M24 is the positive DC REF +ve voltage, which varies between approximately 0.14V and 2.8V, depending on the output value selection.

M24 output voltage rises until M22-9 pulls enough current through R50 to reduce M24-3 to zero. The other transistors in M22 act as current mirrors, so their collector currents are defined by the REF +ve voltage and the resistance of R50.

Thus bias current is applied to Q116 and Q117 in direct proportion to the REF +ve voltage, which is an accurate analog of the demanded output value.

9.9.6.2 Current Driver

The 'SIG²' and 'REF²' current outputs from the square detector develop a differential voltage input between the collectors of Q109 and Q110, to the current driver M103. This amplifier generates a single-ended current drive to the integrators.

M103-7 drives current out through R113 and R118 to the integrators while M103-1 cupplies voltage feedback to maintain TP9 node at very near common 2 potential while maintaining high output impedance to the integrators.

Differential input variations between the collectors of Q110 and Q109, due to 'SIG²' and 'REF²' outputs from the Square Detector are translated to single ended currents into and out of the junction at TP9. The current difference passes through R118 to R148 during SIG INT states, and to R149 during REF INT states.

At other times, when both of the integrator input switches M7-8/9 and M7-11/10 are open, the 'SAMPLE' waveform closes M7-4/3 to pass any difference current to Common-2C. (During the SAMPLE periods, DC SUBTRACT OFF is zeroing the Square Detector input RMS Hi anyway, by shorting to RMS Lo via M7-2/1 - *page 11.7-4*.)

Resistors R118, R148 and R149 are of very low value compared with the output impedance at TP9, so the driver compliance is high.

9.9.6.3 Output Amplitude Loop - LF Gain Reduction

On the 100Hz Frequency range the gain around the output amplitude loop needs to be less than on other ranges. This compensate for the longer integration times at lower frequencies.

Adjustment is in two stages, using dual open-collector comparator M105:

a. For 100Hz Range selection
The '100Hz' logic signal input to M105-2 is derived in the frequency systhesizer and is at logic-1 when 100Hz range is selected. M105-1 is pulled up by R115 and Q108 conducts connecting R116 across R113, reducing the gain of the M103 voltage to current converter.

b. For frequency selections below 32Hz
The '>31Hz' signal input to M21 is also generated in the Synthesizer.

Similar comparator action provides further loop gain reduction for frequencies of 31Hz and below. Both Q107 and Q108 are on to switch in both R116 and R116 across R113.

9.9.7 GENERATION OF THE DC SUBTRACTION CURRENT

9.9.7.1 'REF' Integration

The integrator circuit is very basic. Feedback for M12 is by C25, but the input resistance is formed by R149, R35 and the output impedance of the Current Driver, which is heavily predominant. The current from the driver is virtually unaffected by R35 and R149.

M7-11/10 conducts for periods C1 to C4 (REF INT). During C1 to C3 the REF SW waveform inputs the quasi-sinewave to the squarer, and during C4 the squarer settles to its zero input.

The REF^2 output from the driver is an AC current, which for a constant quasi-sinewave amplitude is integrally charge-balanced about zero due to the DC subtraction, at twice the quasi-sinewave frequency. C25 therefore receives equal positive and negative charge during each cycle of quasi-sinewave, so the mean voltage at M12-1 does not change.

A discharge path for C25 is provided by Q5/R30. The 'INT HOLD' signal at J7-46 is logic-1 when the instrument is in 'OUTPUT OFF' condition, discharging both REF and SIG integrators. For so long as the output remains 'ON', the INT HOLD signal stays at logic-Ø, and the integrators are never discharged other than by the action of their inputs.

9.9.7.2 'REF' Sample-and-Hold

Q2 conducts during each 'REF SAM' period, when the charge on C25 has settled for the cycle. M12 drives C12 to the voltage on C25, and the voltage follower M4 passes the same voltage as 'REF ERROR' on to the REF V to I Converter.

Q2, C12 and M4 are low-leakage devices and M4 input circuit is screened, at low impedance, to the sampled voltage. Thus the 'Droop' is specified as less than 20μV during the 'Hold' part of the cycle when Q2 is not conducting.

9.9.7.3 'REF' V to I Converter

The circuit of M19 and Q6 converts the DC voltage output of M4 into the subtraction current. A second function is to draw an extra DC current which compensates for the bias control currents.

The DC 'REF ERROR' voltage from M4-6 is divided by R37/R31 and applied to the non-inverting input of M19. A second input results from the DC bias current drawn by M22-14, defined by the 'REF+ve' voltage and the two resistors AN2-10/7 and R141.

M19 drives FET Q6, which draws current via Q110 emitter, R54, D5 and D6. The current is sunk into Common-2C via R47, R38 and AN2-12/5, and into the -15V supply via the M22-14/12 bias circuit.

Capacitor C34 filters out any HF transients remaining from the switching edges of REF SAMPLE, and D7 protects against positive excursions of Q6 gate.

In the simplified diagram of *Fig. 9.10*, the subtraction current is shown as being sourced by the summing junction. In reality, it is taken from Q110 emitter for three main reasons:

a. The Current Driver input bias is removed, allowing a zero-offset reference.

b. The control bias for the squarer is compensated at the earliest opportunity, reducing the required dynamic range of the driver.

c. Q110 emitter voltage remains virtually constant for all squarer inputs.

Relocating the subtraction point does not affect the essential action of the square detector and driver, because of the current-mirror action of the driver.

Subtraction is valid only during times when a quasi-sinewave or sensed sinewave is being input to the Square Detector. Thus for periods C1 to C3 and C6 to C8, diode D8 is held in reverse bias by the signal 'DC SUBTRACT OFF' at logic-Ø. During periods C4, C5, C9 and CØ, the signal is at logic-1, so D8 conducts and reverse-biases D5 and D6. The subtraction current passed by Q6 is then diverted through D8 from M20-11/3, the 'DC SUBTRACT OFF' parallel NOR gates' output being at logic-1 *(page 11.7-3)*.

When an operator selects a different output value, the result is a change in amplitude of the quasi-sinewave. This unbalances the integrator input, so C25 charges to a different mean voltage at the output of M12. The DC subtraction current change takes place over a few comparator cycles until balance is restored, when C25 and C12 will have charged to a new voltage.

9.9.8 'AC ERROR' SIGNAL GENERATION

9.9.8.1 Integration and Sampling Circuit

The SIGNAL Integration and Sample-and-Hold circuitry is identical to the REF arrangement described in *Section 9.9.7.* Moreover, the SIGNAL Integrator M12 is the other half of a matched pair with the REF Integrator.

The difference lies in the timing. Switch M7-6 allows current to pass into the SIG integrator only during periods C6 to C9, so it is the SIGNAL (sensed sinewave)^2 current minus the (DC REF)^2 subtraction current which is integrated.

The integrator voltage is sampled and output as the 'AC ERROR' DC voltage *(sub-sections 9.2.4 and 9.9.2)*, into the output amplitude control loop.

9.9.8.2 Output Amplitude Loop Action

Consider the case of 'OUTPUT OFF'

a. The quasi-sinewave has an amplitude determined by the 'OUTPUT' display value:

b. The quasi-sinewave is squared and appears as a current in R35 during periods C1-C4, but because Q5 is conducting, the REF integrator capacitor C25 is discharged. Thus the DC subtraction current is effectively zero (it is actually sufficient to cancel the DC current in R35 due to the squarer bias).

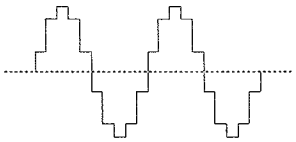
c. The AC ERROR signal voltage is zero, as Q4 conduction prevents any charge on the SIG integrator capacitor C26. Also, the output amplitude is zero, hence the sensed output applied to the squarer is zero.

Therefore during periods C6-C9 the current in R35 is zero.

Now consider the case when OUTPUT is switched ON, with the OUTPUT display set to the minimum value of 9% of range:

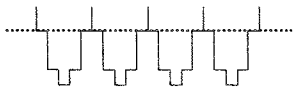
As the quasi-sinewave is already present, it is squared into a negative-going waveform in R35.

Quasi-Sinewave Input



During the first comparator cycle, this appears as a voltage at TP9 thus:

(Quasi-Sinewave)^2

Zero Reference 

The standing bias on the Ref. V to I Converter has immediately set the (quasi-sinewave)^2 to an approximate zero mean.

The (quasi-sinewave)^2 current is integrated across C25, resulting in a positive 'REF ERROR' voltage after period C5, and hence a positive subtraction current in R35. The effect of the current can be seen in the TP9 voltage waveform: an increase of (quasi-sinewave)^2 amplitude is accompanied by a positive shift as its mean value seeks coincidence with zero.

After a few comparator cycles the current in R35 becomes charge-balanced about zero, the DC subtraction current stabilizing to a steady-state value.

Meanwhile, during the 'SIG' sections of the comparator cycle, the positive subtraction current is integrated across C26. A negative 'AC ERROR' voltage is generated, which increases the instrument output voltage via the VCA. This increase is detected by the sense feedback circuits. After squaring, the result is an AC current in R35, whose mean level begins to offset the effect of the subtraction current on the SIG integrator.

After a few comparator cycles, the AC SIG^2 mean current and the DC subtraction current are equal and opposite, so the current fed through R35 into the integrator is charge-balanced about zero. The integrator capacitor C26 is thus being charged and discharged by the same amount during each half-cycle of output (SIG^2 current being at twice the output frequency), so the AC ERROR voltage stabilizes.

Fig. 9.14 illustrates three stages in the process of increasing output from zero; observing the current in R35 (ie. the voltage at TP9), the 'AC ERROR' signal, and the output sinewave. The waveforms are not to scale.

Stage 1.
This is the first cycle that the quasi-sinewave starts to charge C25. During period C6 a non-zero subtraction current is applied to the SIG integrator, resulting in a non-zero value of 'AC ERROR', starting at CØ as the integrator voltage is sampled. This causes the instrument sinewave output to rise from zero.

Stage 2.
On the next cycle the subtraction current imposes a positive shift on the R35 waveform during C1-C3 and C6-C8. The squared quasi-sinewave does not change in amplitude, but it is more equally balanced about zero, so the next increase in subtraction current will not be so great.

During C6-C8 the sinewave is being applied to the squarer, so TP9 exhibits its squared waveform shifted positively by the subtraction current. A smaller increase in 'AC ERROR' and output sinewave results, as the AC input to the SIG integrator is more equally balanced about zero.

Stage 3.
In this state the loop has stabilized. The squared quasi-sinewave and sensed sinewave are both charge-balanced about zero, the subtraction current and 'AC ERROR' have reached constant values, and the instrument output is stable.

9.9.8.3 'AC ERROR' V-to-I Converter

(Circuit Diagram 400844 page 11.7-6)

To avoid noise pick-up, the AC ERROR voltage is converted into a current, for transmission to the Error Amplifier on the Sine-Source Assembly. One half of M3 is used as a unity-gain inverting buffer, and the other as a voltage-to-current converter. The relay RL1 is not fitted, so M3-7 is linked directly to the test switch S1 'NORM' terminal.

At M3-7 the DC 'AC ERROR' voltage is inverted and used to drive the current converter via AN1-3/12.

The current in AN1-4/13 is mirrored by the current in AN1-11/6 (AC AMPL ERROR), which is sourced in the Sine-Source Assembly by M41a, the Error Amplifier (*Circuit Diagram 430446 page 11.6-3*).

As the AC ERROR signal DC voltage is varied by the comparator, the current in M41a input resistance also varies, and is converted into a varying voltage at M41a-1. This voltage is used to control the main voltage-controlled amplifier M48 via Q71.
For further information about the VCA, refer to *Section 9.3*.

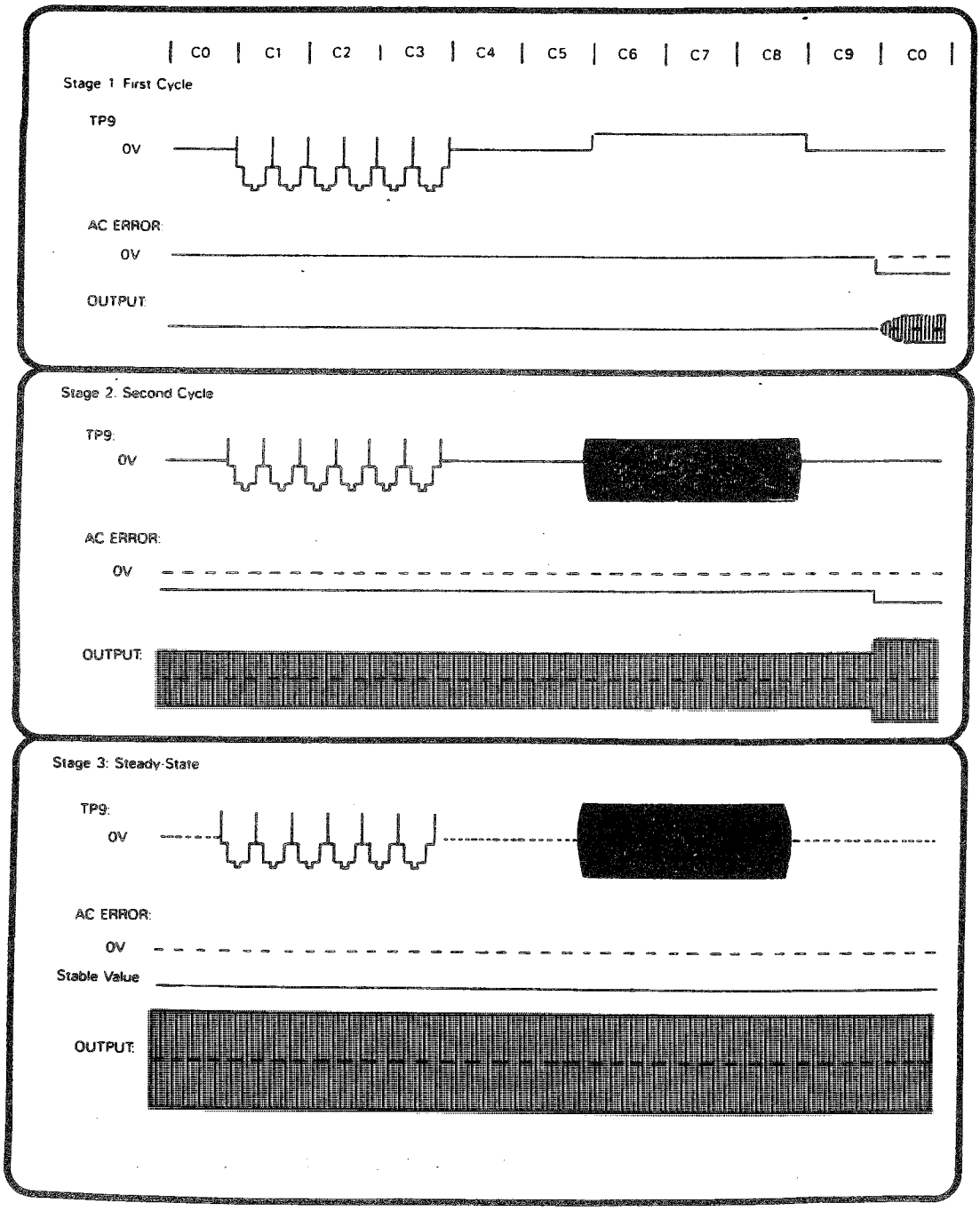


FIG. 9.14 THREE STAGES OF OUTPUT BUILD-UP FROM ZERO

9.10 LOGIC CONTROL OF AC OUTPUTS

The general aspects of analog control functions are discussed earlier in *sub-section 7.10*, subdivided as follows:

7.10.1 Logic Levels

7.10.2 Heat Reduction
7.10.2.1 Update Considerations

The AC signals are routed through the DC assembly on their way to the terminals and back; for the 10V, 100V and 1000V ranges they are amplified in the Power Amplifier assembly. The signals are subject to digital controls incorporated in those assemblies.

Descriptions of the controls in the DC and PA assemblies are indexed in *sub-sections 9.10.1 and 9.10.2*, below.

9.10.1 DC ASSEMBLY - LOGIC AND RELAY DRIVES

(Circuit Diagram 430536 Page 11.5-3)

The AC voltage output and sense signals pass through the DC assembly, and are affected by the analog control signals present there.

The effects of the control logic on the DC assembly are detailed in *Section 7*, subdivided as indexed, except for the 'HIGH I LIMIT' and 'AC 1kV RANGE' Logic.

As these two signals are activated only on the AC 1kV Range, their effects are described in *sub-section 9.7.6* (but reference is also made to relays 12 and 13 in *para 9.4.2.3)*.

7.11.1 Introduction
7.11.1.1 Latched Bistable Relays
7.11.1.2 'Tristate' Relay Drivers

7.11.2 Clamp Assembly
7.11.2.1 UPD(IG) Distribution
7.11.2.2 Buffer Clamping

7.11.3 DC Assembly Switching Logic
7.11.3.1 DC Range Switching Logic
7.11.3.2 Function and Output Switching Logic

9.10.2 PA ASSEMBLY - LOGIC AND RELAY DRIVES

(Circuit Diagram 430618 Page 11.9-5)

The extensive switching needed to control the many modes of operation of the Power Amplifier assembly, is described earlier in *Section 7.12*. The subjects are subdivided as listed below:

7.12.1 DC Range Switching
7.12.2 AC Range Switching
7.12.3 Function and Ranging Logic
7.12.4 'PA CLAMP ON' Signal
7.12.5 '400V ENABLE' Logic
7.12.6 'BIAS OFF' Logic

7.12.7 '$\overline{\text{LIM ST}}$' Logic
7.12.7.1 'LIM DET'
7.12.7.2 '$\overline{\text{LIM ST}}$' Generation
7.12.7.3 CPU Response

7.12.8 'LF', '$\overline{\text{LF}}$' and '1kV GAIN'
7.12.9 Thermistor Comparator

9.10.3 AC ASSEMBLY LOGIC AND RELAY DRIVES

(Circuit Diagrams 400844 Page 11.7-5)

The analog control signals are transferred into guard on the Reference Divider assembly, and latched as 'Q' outputs in the Serial/Parallel Data Converter. Offset positive logic is used:

logic-Ø = -15V, logic-1 = 0V.

The signals enter the AC assembly via J7 from the Mother assembly.

M28 and M29 are inverting, open-collector Darlington drivers. The relay-drive logic places a logic-1 (0V) on the input of the selected drivers and logic-Ø (-15V) on those not required. A selected driver operates its relay by pulling its output to -14V.

Whenever a switching command has been received, the CPU performs a control-data transfer and the $\overline{\text{UPD(IG)}}$ line from J7-53 is pulsed to logic-Ø for 50ms. Q19 is turned on, applying +15V to the relays connected to its collector. The selected relays are thus energized by 30V, but after the $\overline{\text{UPD(IG)}}$ pulse has ended Q19 turns off, and they are held on by the -12.6V between -1.4V at the cathode of D20 and -14V at the selected driver output. This method reduces the heat, generated locally by energized relay solenoids, in the relay contacts.

FETs Q42 and Q43 damp the coils of RL12 and RL13; diodes D59 and D60 isolate parts of the printed circuit to these relays, which are sensitive to power-common breakthrough when they are deselected. D55 and D56 are overswing diodes.

9.10.3.1 Range Switching

(Page 11.7-5)

Range control data is input as a 3-bit code on ACR_0, ACR_1 and ACR_2 lines. The bit-pattern is decoded to '1 of 8' by M25, to energize the correct relays for the selected range. In this instrument only eight of the M25 'Q' outputs are connected. The resulting variants are listed in *Table 9.1* against range selections.

9.10.3.2 $\overline{\text{AC FNCT}}$ and $\overline{\text{I FNCT}}$ Logic

(Page 11.7-5)

In addition to its primary function of controlling AC Voltage range switching, the AC assembly logic also needs to respond to AC Current range selections if Option 40 is fitted; because the AC voltage reference for the Current assembly is generated by the Voltage circuitry. For this purpose the two signals $\overline{\text{AC FNCT}}$ and $\overline{\text{I FNCT}}$ are used.

$\overline{\text{AC FNCT}}$ is at logic-Ø only when AC Voltage output is selected, holding M25-11 'D' input at logic-Ø, and energizing relays RL2 and RL10. This connects the star-point at Common-2B to the PLO(ACV) line (J7-31) and SIG LO to the SLO(ACV) line (J7-32) *(page 11.7-1)*. The bit-patterns controlling the voltage range switching are shown on *Table 9.1*.

$\overline{\text{I FNCT}}$ is at logic-Ø only when Current output is selected, holding M25-11 'D' input at logic-Ø, and energizing relays RL2 and RL9. This connects the ACI REF lines (J7-69 to J7-72) to the ACV lines *(page 11.7-1)*. The 10V range output is used as reference for the 100mA, 10mA and 1mA Current ranges, but the 1V range output is used for the 100µA and 1A ranges. The bit-patterns controlling the current range switching are also shown on *Table 9.1*.

The signals $\overline{\text{AC FNCT}}$ and $\overline{\text{I FNCT}}$ are never at logic-Ø at the same time in normal operation. The only time they are at logic-1 together is when all outputs from the Control Data latches in the Reference Divider are 'Tristated'. 'DCI' ensures that RL2 and RL9 cannot be energized by selection of DC Current ranges.

9.10.3.3 'AC Zero'

For zero output, the lines from the voltage generators to the I+ and I- terminals are disconnected by deselection of the ranges, and a hard short is placed across the output lines by RL18.

The $ACR_{2\text{-}0}$ code is '1,1,1'. This sets M25-4 to logic-1 (energizing relay RL18) and all other M25 range outputs to logic-Ø (the resultant bit-pattern is shown in Table 9.1). Thus all ranges are deselected, but relays RL2 (ACV and ACI), RL3 (AC Low Voltage Output), RL10 (ACV) and RL19 ($\overline{\text{1kV}}$) remain energized. Relay RL18 connects the PLO(ACV) star-point of Common-2B to the PHI(ACV) line.

9.10.3.4 'BARK DELAYED'

The 'BARK' signal does not affect the AC assembly relays. However, if the Watchdog is activated, the CPU imposes OUTPUT OFF conditions and forces the Precision DC Reference to ramp down to zero, so the PHI REF voltage also falls to zero.

All outputs from the Control Data latches in the Reference Divider *(page 11.4-4)* are 'Tristated' by the 'BARK DELAYED' signal. This allows the pull-up resistors (AN4 and AN5) to become effective.

The $\overline{\text{AC FNCT}}$ and $\overline{\text{I FNCT}}$ are pulled to logic-1, and the $ACR_{2\text{-}0}$ code is '1,1,1'. This imposes 'AC Zero' conditions on the analog circuit, but RL2, RL9 and RL10 are also de-energized. So the DC precision reference is disconnected from the input to the quasi-sinewave generator; the ACI(REF) is disconnected from the input to the AC Current circuitry, and the Sense and Power Lo lines are disconnected from the sense amplifiers.

Function Note [1]	Range	Range Code $ACR_{2\ 0}$ ACR_2 ACR_1 ACR_0			M25 Output at Logic-1 'Q'	Pin	Relays Energized [° = Energized] 2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
AC Volts	1000V	0	0	0	Q0	3	°								°			°			°				°
	100V	0	0	1	Q1	14	°								°					°		°		°	
$\overline{\text{AC FNCT}}$ at Logic-0,	10V	0	1	0	Q2	2	°	°							°				°			°		°	
	1V	0	1	1	Q3	15	°	°				°	°		°		°							°	
$\overline{\text{IFNCT}}$ at Logic-1)	100mV	1	0	0	Q4	1	°	°	°		°				°	°	°							°	
	10mV	1	0	1	Q5	6	°	°	°	°					°	°	°							°	
	1mV	1	1	0	Q6	7	°	°							°	°	°							°	
	Any	1	1	1	Q7	4	°	°							°								°	°	
AC Current $\overline{\text{AC FNCT}}$ at Logic-1,	100μA 1A	0	1	1	Q3	15	°	°				°	°	°				°						°	
$\overline{\text{IFNCT}}$ at Logic-0)	1mA 10mA 100mA	0	1	0	Q2	2	°	°						°					°			°		°	

Note[1] In normal operation, unless the SAFETY message is displayed; either $\overline{\text{AC FNCT}}$ or $\overline{\text{I FNCT}}$, but not both, will be at Logic-0.

TABLE 9.1 AC ASSEMBLY SWITCHING LOGIC

SECTION 10 CURRENT OUTPUTS AND RESISTANCE

10.1 DC AND AC CURRENT

The circuits described in this sub-section perform the following functions:

- Divide the DC reference voltage by 10 to (-2V to +2V).
- Generate a DC output current whose value varies directly as the reduced value of the DC reference Voltage.
- Convert the ACI Reference Voltage into an AC reference current, having a high-impedance source.
- Generate an output current whose value varies directly as the value of the AC reference current.
- Provide switching of the DC or AC Current Range and Output, under the control of the Analog Control Interface.
- Sense excess output (compliance) voltage, providing a status signal to the CPU via the Analog Control Interface.

The voltage-to-current converter is located on the Current or Current/Ohms assembly, providing five DC and five AC ranges of current output. The full range values are 1A, 100mA, 10mA, 1mA and 100µA, extending to 100% overrange, for both DC and AC Current. The output is drawn from the instrument I+ and I- terminals; the Hi and Lo terminals not being used.

10.1.1 VOLTAGE-TO-CURRENT CONVERTER

Fig. 10.1 shows the basic arrangement. A DC or AC reference voltage is developed across R1 between the output and the inverting input of the high-gain amplifier. Its output connects to its other input by a 'shunt' network, part of which carries the output current.

The combined feedback forces the differential input to zero. This adjusts the current in the positive feedback path until the full value of the reference develops across the path. For example in *Fig. 10.1* no current flows in R2, so all of VRef is develops across Rs. The values of VRef and 'shunt' Rs determine the current flowing in the external circuit. Rs is switched to select the range, and VRef is varied to set the output current within the range.

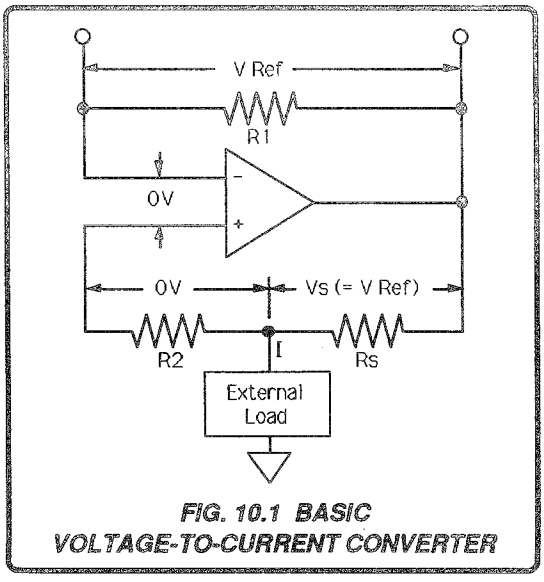


FIG. 10.1 BASIC VOLTAGE-TO-CURRENT CONVERTER

10.1.2 AC CURRENT GENERATOR

(Circuit Diagrams 430614 Page 11.8-1 and 430540 Page 11.13-3)

Because a return path is needed for the output current, a 'compliance' signal voltage appears between the I+ and I- terminals. The magnitude of this voltage is specified in the User's Handbook, and the specification is met by floating the input to the output amplifier.

On the DC ranges the floating DC reference is input directly into the output amplifier, which therefore acts as a voltage to current converter in the style of *Fig. 10.1*. Resistors R44 and R45 provide 10:1 attenuation, to set the 'VRef' to 1/10 of the reference value.

For AC ranges the ACI Reference is buffered from the output amplifier in a two-stage circuit. A fixed voltage-to-current conversion stage is followed by a range-switchable current amplifier (the latter is the voltage-to-current converter for DC ranges). The combination is simplified at *Fig. 10.2*.

In the figure, the AC Reference voltage is applied via two resistors R1 and R3 to both inputs of the first stage. It is arranged for the resistor values to conform to:

$$\frac{R2}{R1} = \frac{R4}{R3}$$

so the output impedance of the stage is virtually infinite, and its output 'floats'.

The second stage is a current amplifier, receiving the output current of the fixed stage to generate a voltage across R5. This voltage is repeated across R6, whose value is range-switched. Any resistor Rs does not affect the output, carrying no current. The current amplifier supplies are bootstrapped to improve common mode rejection.

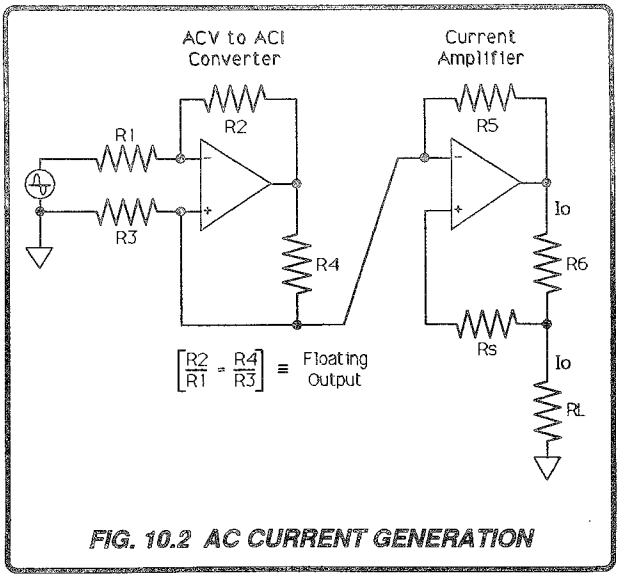


FIG. 10.2 AC CURRENT GENERATION

10.1.3 DC AND AC REFERENCE - SOURCING AND SCALING

The DC output currents are bipolar, directly controlled within each range by the ±20V reference voltage (REF) from the Reference Divider. On DC ranges, REF is divided by 10 in the input attenuator. For the 1mA,10mA and 100mA ranges, the ±2V full scale span is available across the selected range shunt.

To optimize component choice and minimize the relay count, software further divides the DC reference by 10 for the other two ranges. On the 1A Range a full scale span of ±200mV can be applied across its 0.1Ω shunt, and for the 100µA Range the ±200mV can be applied across the combined shunt resistance of 1000Ω assigned to the 1mA Range.

The AC output currents are controlled within each range by the value and frequency of the ACI(REF) voltage. This reference voltage is generated by the circuitry used for AC voltage ranges: the 10V Range for the 1mA, 10mA and 100mA ranges; but the 1V Range for the 100µA and 1A ranges. Thus the same shunt values and switching relays can be used for both AC and DC current outputs. The highest frequency available is 5kHz.

10.1.4 DC CURRENT REFERENCE '(REF)'

(Circuit Diagrams 430652 Page 11.4-3 and 430614 Page 11.8-1)

The (REF) signal is the main DC reference for the whole instrument. It is sourced in the Reference Divider on J4-9/10/11/12 *(page 11.4-3)* as a 4-wire output, which enters the Current/Ohms assembly from the Mother assembly on J8-1/2/3/4 *(page 11.8-1)*. Relay RL7 is activated for DC Current Ranges, so the PHI(REF) and PLO(REF) levels are sensed at TP3 and TP4 respectively.

(REF) is divided by R43/R44, so 1/10 of (REF) is developed across R43, and applied between the inverting input of the V-I converter and the output of the Darlingtons on the PS/I heatsink at J19-7 (one of the relay contacts RL1-2/3 or RL1-10/11 is always made).

10.1.5 AC CURRENT REFERENCE 'PHI (ACI REF)'

(Circuit Diagrams 400844 Page 11.7-1.and 430614 Page 11.8-1)

On the 100µA and 1A ranges, the AC 1V Range circuit provides the 2V RMS Full Scale reference; on the 1mA, 10mA and 100mA ranges the AC 10V Range circuit provides 20V RMS at Full Scale.

On the AC assembly *(Page 11.7-1)*, for T' function, RL9 is energized and RL10 is not. The reference voltage for the current generator is derived from the PHI (ACV) and PLO (ACV) signals; and sensed at the input to the Current or Current/Ohms assembly. The sensed ACI REF is returned to the appropriate connections on the 1V/10V Sense Amplifier. The 4-wire connections are made via J7, pins 69 to 71, to the same pins of J8 on the Current/Ohms assembly.

The AC preamplifier M8 divides the reference voltage by 10, so the RMS voltage applied to R43 is the same as the DC voltage applied for corresponding range and output settings.

10.1.6 RANGE SELECTION

Fig. 10.3 shows two Range configurations of the current amplifier. In each case V Ref is 10% of the reference voltage. The polarity of the solenoid current of bistable latching relay RL1 determines which state is selected. Solenoid current is not required for hold-on, only to change state.

The voltage across the I+ and I- terminals is fully compliant up to 3V DC or RMS. Each range has resistance in series with the I+ terminal to enhance stability for reactive loads.

10.1.6.1 1A Range

(Refer to Fig. 10.3a)

Relay RL1 closes contacts 8/9, 11/10 and opens contacts 2/3. Relays RL2, 3, 4, and 5 are not energized. The only output current path passes through the 0.1Ω shunt R80. Thus in the positive feedback path all of VRef is developed across R80, and no current flows in R79, R8, R9 or R10. As V Ref is scaled to 100mV DC or RMS Full Range, the full range output current in R80 is: 100mV/0.1Ω = 1A.

10.1.6.2 100mA, 10mA, and 1mA Ranges

(Refer to Fig. 10.3b)

Relay RL1 is activated so that contact RL1-3/2 is closed, contacts RL1-10/11 and 8/9 are open. One relay from RL2, 3 and 4 is energized by range, RL5 is also energized on the 10mA and 100mA ranges for extra HF filtering. All currents now avoid the 0.1Ω shunt, passing instead through the 10Ω shunt R79. R79 is mounted with R80 on a separate heatsink assembly, plugged into the main Current or Current/Ohms assembly (refer to the Layout Drawing, *page 11.8-1* for alternative versions).

On the 100mA range, VRef is scaled to 1V DC or RMS Full Range, so the full range current flowing through R79 to the I+ terminal via RL3-14/8 is: 1V/10Ω = 100mA.

For the 10mA range, R8 (90.00Ω) is included in the current path, so the full range output current is reduced to 10mA. 900.0Ω (R9) is added on the 1mA range.

10.1.6.3 100µA Range

(Refer to Fig. 10.3b)

The hardware is switched as for the 1mA range, but either the DC REF voltage is scaled in software to 1V full range, or the ACI REF voltage is obtained, as for the 1A range, from the AC 1V range circuitry. Thus VRef is scaled to 100mV DC or RMS Full Range, and the full range output current is 100µA.

10.1.6.4 10A Range

The 10A range can be selected only if a Model 4600 amplifier is connected to the instrument by the digital and analog control busses. The 4600 converts an input voltage to an output current, so operation of the 4808 in 10A range is more appropriate to the discussion of DC and AC Voltage *(sections 6.1.9 and 7.3.8)*.

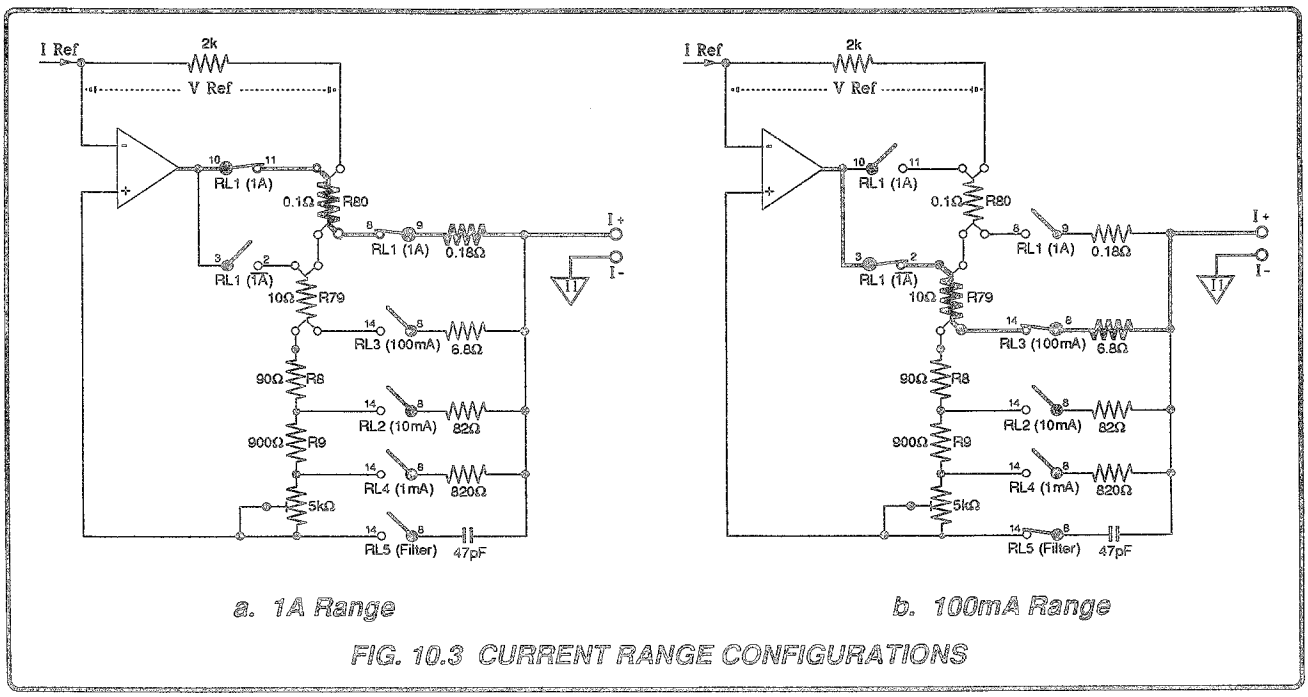


FIG. 10.3 CURRENT RANGE CONFIGURATIONS

10.1.7 DC VOLTAGE-TO-CURRENT CONVERSION

The value of the REF input sets the output current value, scaled for range as described earlier. REF is coupled: Hi (TP3) to the output, and Lo (TP4) to the inverting input through R44.

The conversion amplifier is in two sections: a voltage preamplifier on the Current assembly *(page 11.8-6)* or Current/Ohms assembly *(page 11.8-1)*, and a power amplifier on the PS/I Heatsink assembly *(page 11.13-3)*. The latter is also drawn, for convenience, on *page 11.8-1 and page 11.8-6*.

The whole amplifier is also used as the Current Amplifier for AC output currents. In that case it is preceded by the AC preamplifier M8 (*sub-section 10.1.9*).

10.1.7.1 Voltage Preamplifier

M3, M4 and Q6 form a high-gain, chopper-stabilized voltage amplifier. M3, itself a chopper-stabilized amplifier of high gain and approximately 10Hz bandwidth, trims the input offset of Q6, which provides the bandwidth necessary to pass the signal frequencies and reject common-mode noise.

M4 contributes additional gain and drives the high-current output stage via link TLE. Its load, consisting of R26, R23 and R28 shunted by Q7 in the Heatsink assembly, is supplied with a constant current by Q9, D6 and Q11. Additional frequency compensation is provided by C43 and R81.

The supplies to Q6 and M3 are bootstrapped by M7 for common-mode rejection, also linearizing the preamplifier's dynamic response. Extensive screening and filtering is employed to eliminate the effects of the chopping spikes at the inputs and output of M3.

10.1.7.2 High Current Output Stage

(Circuit Diagram 430614 Page 11.8-1 or 401008 page 11.8-6, and Circuit Diagram 430540 Page 11.13-3)

The main current amplifier and temperature-sensing driver load (Q7) are located on the PS/I Heatsink assembly. The quiescent current 'SET I_Q' adjustment is situated on the Current or Current/Ohms assembly.

10.1.7.3 Temperature Compensation

Transistor Q7, thermally attached to the heatsink and in parallel with R26, R23 and R28 on the Current or Current/Ohms assembly, acts as the load for the preamp buffer. As the heatsink temperature increases, Q7 conduction increases, reducing the drive to the current amplifier. This compensates for increased intrinsic quiescent current in the two Darlington output devices.

10.1.7.4 Quiescent Current Adjustment

FET Q9 acts as constant 1.4mA ballast for the 3.3V zener diode D6, which sets the voltage across R27 to approx. 2.6V. This establishes the collector current in Q11, generating a constant current in the buffer load.

The voltage across the load is supplied to the PS/I heatsink as drive for the high-current amplifier. The tapping at J8-110 sets the base conduction level of Q7 on the heatsink, which in turn sets the level of its collector conduction, adjustable by R23. This therefore adjusts the quiescent current in the output devices Q1 and Q2.

10.1.7.5 Power Amplifier

Darlington emitter-followers Q1 and Q2 form the power output amplifier, current-limited by Q5 and Q6. The bias is set to provide some 100mA of quiescent current, which reduces the output resistance of the stage, improving the dynamic response of the output current. This also suppresses any tendency for the drive from the preamp buffer to fluctuate for output currents around zero; as the drive voltage must slew through approximately 1.3V after switching one device off before the other is switched on. The current shunts complete the feedback and output circuits, the output current being fed to the I+ terminal via protection circuitry and output switching.

10.1.8 AC VOLTAGE-TO-CURRENT CONVERSION

10.1.8.1 AC Voltage-to-Current Converter M8

(Circuit Diagram 430614 Page11.8-1 or 401008 page 11.8-6)

The reference voltage PHI(ACI REF) is applied to the inverting input of M8 via resistor R45, with R46 as feedback resistor. Similarly R47 and R48 are connected on the non-inverting side. The 18MΩ resistors R82 and R83 shunt R47 to allow compliance adjustment by R31. R86 refers the input to Common-I1, the main 'signal' common.

10.1.8.2 Current Amplifier

The output AC current from the converter, flowing through R48 to restore M8 input virtual-common, passes via R85 into the Current Amplifier feedback resistor R43. It generates a reference AC voltage between the output of the whole Current Amplifier and its inverting input. This is reflected on its non-inverting side by the current flowing through the range-switched output 'shunts'.

The whole amplifier is also used as the Voltage-to-Current Converter for DC output currents (*sub-section 10.1.8*). The Preamplifier and Output sections have the same operation as in the DC case.

10.1.9 OUTPUT PROTECTION

Diodes D18 and D19 are 5V, 5 Watt zeners, placing an absolute limit on the excursions of output voltage. The output compliance specification is valid only up to 3V DC or RMS at the output terminals. Nevertheless, occasions may arise when a user overloads the circuit by attempting to drive current into open circuit (e.g. by disconnecting from a load with OUTPUT ON). In this case D18 and D19 protect any voltage-sensitive load by limiting the output voltage to 5V. But before the voltage reaches this limit, the overvoltage protection circuit generates the $\overline{\text{LIM ST}}$ signal.

10.1.9.1 Guard Buffers

M1 guards out the leakage of D18 and D19 in normal operation, and protects against other leakage, by maintaining the output screens and shields around the output circuitry at the output potential. In addition to its bootstrap function, M7 also acts as a buffer for guards around the amplifier input, thus preventing any common-mode disturbances from affecting the performance of the main amplifier.

10.1.9.2 Overvoltage Detection

The output guard buffer M1 drives the overvoltage detection circuit. M15 divides the output voltage by two and acts as an inverting full-wave rectifier, accommodating AC and both polarities of DC. The full-wave rectified voltage at M15-14 thus increases negatively as the output voltage increases, charging C32 to its mean value at M15-10. M15-9 is biassed to -2.2V, so M15-8 reverse biasses D10 unless the terminal voltage exceeds 4.8V RMS, when M15-8 swings to the negative rail and pulls the $\overline{\text{LIM ST}}$ line to -15V (logic-Ø).

The diode D10 is part of a diode-OR gate, linking $\overline{\text{LIM ST}}$ to the $\overline{\text{LIM ST}}$ line, which enters the Reference Divider at J4-76. The CPU receives the $\overline{\text{LIM ST}}$ status signal via the SSDA serial interface, and if at logic-Ø presents the 'Error OL' message on the MODE display. If in the 100mA or 1A range, the Output is turned off and the DC precision reference is ramped to zero, to limit the power developed as heat within the instrument. Other sources and the effects of the $\overline{\text{LIM ST}}$ signal are described in *sub-section 7.12.7.*

10.2 RESISTANCE

10.2.1 INTRODUCTION

Eight standard resistors are mounted on the Ohms or Current/ Ohms Assembly, each being part of a combination whose total resistance is factory-adjusted to a value close to nominal. They are 4-wire connected to the instrument terminals by range-selection relays. Nominal values are 10Ω, 100Ω, 1kΩ, 10kΩ, 100kΩ, 1MΩ, 10MΩ and 100MΩ.

10.2.2 RESISTOR CIRCUITS

10.2.2.1 4-Wire Connection Symmetry.

(Circuit Diagram No. 430614 Page 11.8-3 or 401047 page 11.8-8).

For any given resistor combination, the connections on the Hi side are made through contacts of the same relays used for the Lo side, except for the 'Ω OUTPUT' relays RL24 and RL25. This ensures that both sides of each resistor connect to the front panel terminals through the same number of similar thermal connections.

To achieve the low leakage required for the Megohm ranges, particularly for the 100MΩ range, a further relay RL17 is used to isolate the parallel leakage paths of the lower range circuits.

The use of latching relays eliminates the heating effect from their solenoids. But it is important that all non-thermal relay contacts are made back-to-back to cancel thermal effects. Thus only the connections to non-latching relays RL24 and RL25 actually need to be back-to-back, although most others are.

This symmetrical, 4-wire arrangement transfers the stability and accuracy of each resistor to the front panel terminals.

10.2.2.2 4-Wire Junctions and Pre-set Trimming.

R63, R64, R65 and R72 are 4-wire resistors, so for 10Ω-10KΩ selections the 4-wire junction is at the standard resistor itself. These resistors are parallel-trimmed. R62, R74, R73 and R71 are two-wire resistors. For these higher resistance values, 100KΩ, 1MΩ, 10MΩ and 100MΩ, series trimming is used and the 4-wire junctions enclose the series chain.

Trimming resistors are selected and adjusted in the factory, in a carefully-controlled environment, against traceable standards.

10.2.3 METHODS OF CALIBRATION

10.2.3.1 Routine Autocalibration

The nominal value of each standard resistor is labelled below its RANGE key. When the key is pressed, the OUTPUT display does not show nominal; but instead gives the value measured at its most recent calibration. This is the main criterion for many users, rather than having the resistor internally trimmed to nominal. So routine recalibration consists of accurately measuring the resistor value and setting the display to read that measured value, without removing the instrument covers *(refer to User's Handbook Section 8)*. The factor which corrects the nominal value to the measured value is stored in non-volatile RAM on the Digital assembly.

During recalibration, if a user enters a value on the OUTPUT display which is outside the span of the calibration memory, the instrument displays "Error 6". As any resistor drift is normally just a fraction of the span, "Error 6" appears only when an erroneous value is entered, (eg. if a resistor's value has been changed by the stress of an overload).

10.2.3.2 Internal Adjustment

A severe overload can alter a resistor's value, possibly taking it out of its calibration memory span. To restore the value to one which can be entered from the front panel, each resistor combination includes an internal trimmer *(para 10.2.2.2)*. A procedure for adjustment of the trimmers is given in *sub-section 1.4*, but this should be limited to values less than about 50ppm outside tolerance. If a resistor is found to be more than ±50ppm outside its tolerance, it is likely to be unserviceably damaged, so it is advisable to have such a resistor tested or replaced by an agent of Datron Instruments.

10.2.4 USE OF 'Remote Sense' KEY

10.2.4.1 4-wire/2-wire Display Values.

In Ω function, selection of Remote Sense mode (Key LED lit) displays the measured value for the 4-wire connection, but with the Remote Sense LED unlit, the 2-wire value is displayed.

10.2.4.2 Two-wire Connections.

To avoid the intrusion of extra thermal voltages, no additional switching is employed for selection of 2-wire connections. Users are recommended to connect only to the Hi/Lo terminals, so the 2-wire mode should be recalibrated at these terminals.

10.2.5 OHMS ZERO

With Ω function selected, pressing the zero key on the front panel closes the contacts of relay RL16. This provides a true 4-wire short, the existing resistor remaining connected.

If the Rem sense LED is lit, the displayed value is zero and cannot be calibrated; but if unlit, the resistance of the short plus internal wiring can be measured and entered on the display, using four-wire measurement at the Hi and Lo terminals. Subsequently, each time the 'Zero' key is pressed in 'Ω' function with the Rem sense key LED unlit, this entered value will be displayed.

10.3 FUNCTION SWITCHING.

10.3.1 OUTPUT CONNECTIONS - FUNCTION ROUTING

(Circuit Diagram 430614 Pages 11.8-1 and 11.8-3 or 401008 page 11.8-6 or 401047 page 11.8-8)

The PHI, PLO, SHI and SLO connections are routed via the Current, Ohms or Current/Ohms assembly, and it is there that they are switched between functions. The outputs of the three functions V, I and Ω are switched by separate relays onto the terminal lines *(Fig 10.4)*:

Voltage Outputs

Relays RL8 and RL9 are de-energized as shown on *pages 11.8-1 or 11.8-6 as applicable*. Relays RL24 and RL25 are de-energized as shown on *pages 11.8-3 or 11.8-8 as applicable*.The DC or AC Voltage Power and Sense connections to the DC assembly are routed out to the I+, I-, Hi and Lo terminals via latching relay RL23 closed contacts.

NB If neither Option 40 nor Option 50 is fitted, the Current/Ohms Link pcb is fitted in its place to make direct connection from the DC assembly to the terminals *(Section 3)*.

Current Outputs

Relay RL23 contacts are latched open, and if Option 50 (Ohms function) is fitted relays RL24 and RL25 are un-energized. Relays RL8 and RL9 are energized to connect the output from the selected shunt to the PHI and PLO lines only.

Resistance

Relay RL23 contacts are latched open, and if Option 40 (Current function) is fitted relays RL8 and RL9 are un-energized. Relays RL24 and RL25 are energized to connect the selected standard resistor to the four PHI, PLO, SHI and SLO lines, regardless of the state of Remote/Local switching. To avoid the intrusion of extra thermal voltages, no additional switching is employed for selection of 2-wire connections.

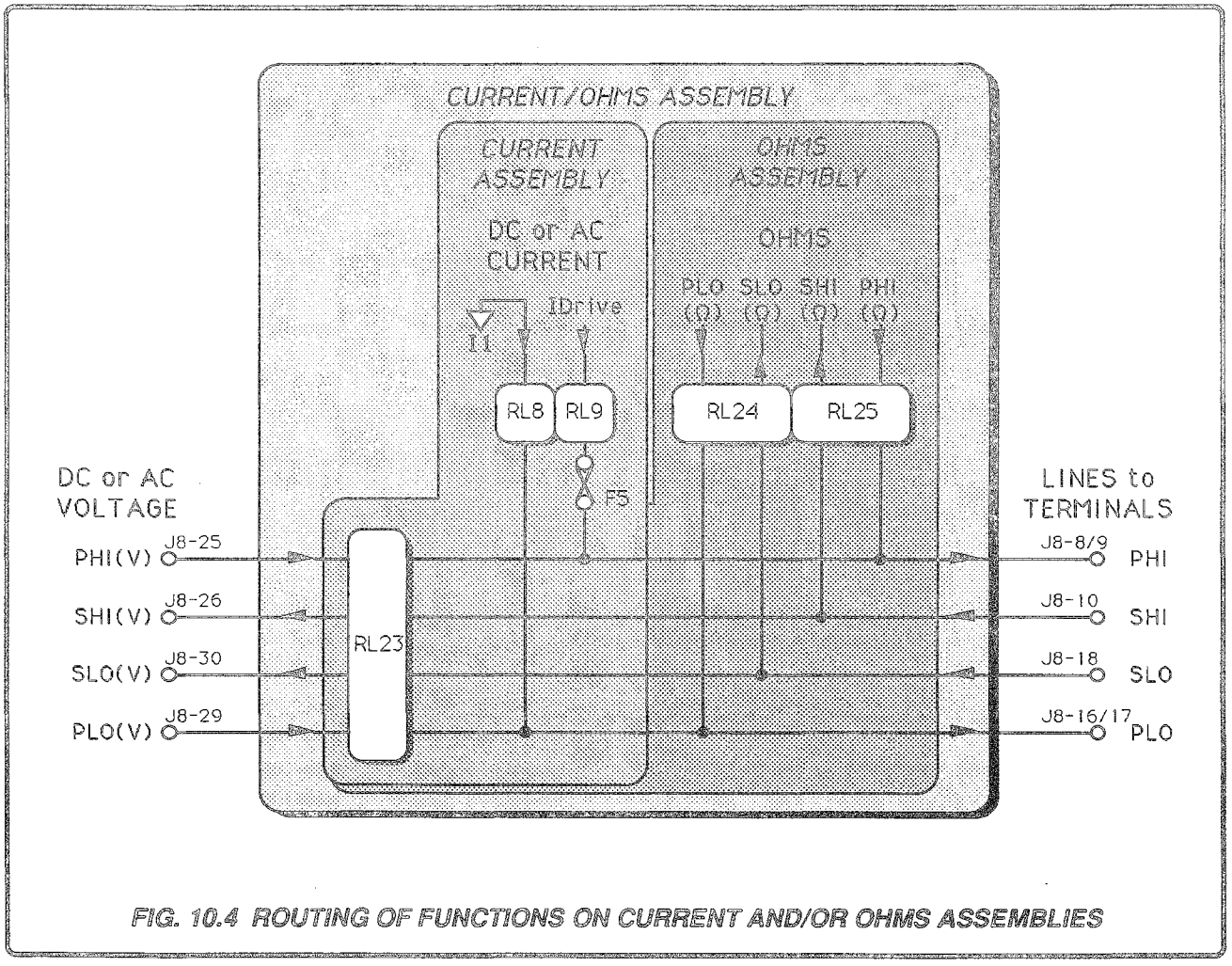


FIG. 10.4 ROUTING OF FUNCTIONS ON CURRENT AND/OR OHMS ASSEMBLIES

10.4 CURRENT AND/OR OHMS ASSEMBLY ANALOG CONTROL

10.4.1 INTRODUCTION

(Circuit Diagram 430614 Page 11.8-2 or 401008 page 11.8-7 or 401047 page 11.8-9)

10.4.1.1 Control Signals

The analog control signals are transferred into guard on the Reference Divider assembly, and latched as 'Q' outputs in the Serial/Parallel Data Converter. Offset positive logic is used:

logic-Ø = -15V, logic-1 = 0V.

The signals enter the Current, Ohms or Current/Ohms assembly via J8 from the Mother assembly.

10.4.1.2 Types of Relays

Guarded Reed Relays
Relays RL2, 3, 4 and 5 are guarded reed relays activated and held on by 15V.

24V Relays
Relays RL 8, 9, 24 and 25 are 24V relays, activated during the 50ms $\overline{\text{UPD(IG)}}$ pulse by approx. 30V, but held on by 15V.

Polarized Relays
Relays RL1, 7, 10, 11, 12, 13, 14, 16, 17, 18, 19, 20, 23 and 26 are 6V latching relays, activated by approx. 7.5V; between M10-13 at -7.5V and either 0V or -15V from the drive output of the clamp assembly. These relays, strung out between the output of their bias amplifier (M10) and the Clamp assembly, are activated only during the 50ms $\overline{\text{UPD(IG)}}$ pulse. They are polarized bistable relays, which require no hold-on power.

10.4.2 LATCHING RELAYS AND CLAMPING

The Ohms and DC Current circuitry is mainly controlled by low-thermal relays, many contacts being fitted back-to-back to reduce temperature effects. For the fastest response, the output relays RL8, 9, 24 and 25 are not latched, but can trip out quickly if the power supply fails, removing any sensitive circuitry from the terminals.

All the other Ohms relays, the AC/DC Current changeover relays, 1A Range relay, and Voltage output relay are latched; allowing hold-on without power, to minimize the internal temperature at their contacts. As they are polarized they need a bipolar actuating drive, which is provided by 'Tristate' relay drivers and a bias amplifier.

10.4.2.1 Latched Bistable Relays

As can be seen from the circuit diagrams, the relays are strung out between the output of their bias amplifier (-7.5V at M10-13) and the drive outputs from the Clamp assembly.

The bias amplifier M10 is a frequency-compensated voltage follower, buffering the tapping of attenuator AN5/R97. So one side of each relay is held permanently at -7.5V. The relay drivers on the Clamp assembly can provide outputs at 0V or -15V when enabled by the $\overline{\text{UPD(IG)}}$ pulse, but return to tristate when disabled. A relay is therefore driven to one or the other of its bistable states during update, then magnetically latched in the chosen state when the driver output returns to open-circuit.

All the latched relays except RL17 operate in the same polarity sense: when its driver output updates at logic-1 (0V), the relay latches to select its nominal function; for a logic-Ø (-15V) update, the function is deselected. For RL17 these conditions are reversed. In the analog circuit diagrams, the relay contacts are shown in their deselected state, equivalent to the un-energized state of a conventional non-latching relay. In the analog descriptions relays may be referred to as being 'energized' or 'un-energized'.

10.4.2.2 'Tristate' Relay Drivers

(Circuit Diagram 430669 Page 11.8-5).

The relay drivers (M1 and M3 on the Clamp assembly) are octal 'Tristate' buffers. Each chip is served by two inverted enable inputs on pins 1 and 19 (four buffers - half the chip - per enabling input).

Whenever a switching command has been received, the CPU performs a control data transfer and the $\overline{\text{UPD(IG)}}$ line from J8-60 is pulsed to -15V for 50ms.

Generally, the switching logic places a logic-1 (0V) on the input of selected drivers, and logic-Ø (-15V) on those whose function is not selected. Because all the buffers are non-inverting, during the update pulse a driver selects its function by setting its output voltage to 0V, deselecting by pulling its output voltage to -15V. The driver serving RL17 (M3-15/5) performs in reverse, J13-15 being pulled to logic-Ø to allow selection of the lower resistance ranges.

10.4.3 CLAMP ASSEMBLY

(Circuit Diagrams 430614 Page 11.8-2 or 401008 Page 11.8-7 or 401047 Page 11.8-9; and 430669 Page 11.8-5).

On the Current, Ohms and Current/Ohms Relay Drive Logic circuit diagrams the Clamp assembly is shown in block form only. Also, the pcb pin numbers correspond to the pin numbers of the buffer chips: J14 and J15 being the connections to M1 and M3 respectively. For signals crossing the block from bottom to top, the output of each non-inverting buffer is drawn opposite its input, so the function remains unchanged as it crosses the block. As a further aid to identification, the pins of any one buffer are numbered so that the input and output numbers add up to 20.

10.4.3.1 $\overline{\text{UPD(IG)}}$ Distribution

As the $\overline{\text{UPD(IG)}}$ signal is distributed as the 'enable' to 16 buffers, it is itself buffered by M16 at M16-3 before being fanned out. So the four $\overline{\text{UPD(IG)}}$ connections at the left of the block are inputs to four sets of four buffers.

10.4.3.2 Buffer Clamping

(Circuit Diagram 430669 Page 11.8-5).

The 40244 octal buffer can be sourced from several manufacturers. Some variants are protected against SCR avalanche if the output voltage were to exceed the rail voltage, but some are not. Each buffer drives its output into the solenoid of a relay, and is switched on and off by the update enable. The self inductance of the solenoid can generate back EMFs well in excess of the rail voltage, so to guard against the possibility of catastrophic failure, it was decided to provide external protection in the form of a clamp circuit.

On the Clamp assembly Q1, Q2, Q3 and Q4 form two power supplies, each delivering a regulated voltage of a diode-drop less than the rail voltage, called '+VE CLAMP' and '-VE CLAMP'.

A diode connected from the buffer output to each of the clamp lines allows the output voltage to rise to the rail voltage but not to exceed it *(see Fig. 10.5)*.

10.4.3.3 BCD - Decimal Decoder M2

The function of M2 is to decode the octal Ohms Ranging signal $R\Omega_{2\text{-}\emptyset}$ with the Ω ZERO signal, providing switching information for individual relays. To provide flexibility for other applications, the inputs and decoded outputs for M2 are taken out to pins of J18, the outputs being linked back to selected pins of J13 and J14. These connections are shown on *page 11.8-2 and 11.8-9*.

Refer to *sub-section 10.4.6* and *Table 10.3* for a discussion of the M2 decode and resultant relay operation.

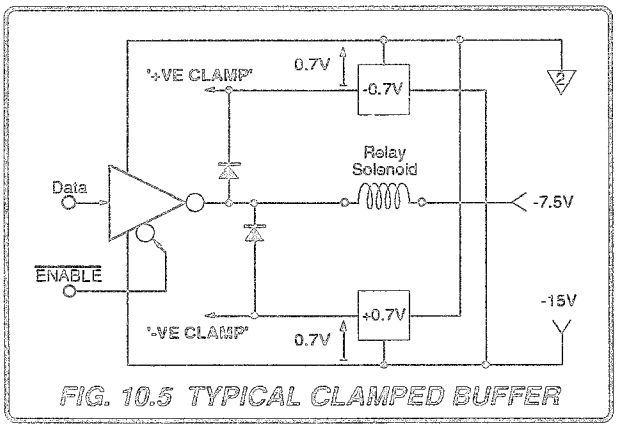


FIG. 10.5 TYPICAL CLAMPED BUFFER

10.4.4 V, I AND Ω FUNCTION SWITCHING

10.4.4.1 Function Relays

The Function relays are located at top right of the circuit diagram on *page 11.8-2, 11.8-7 and 11.8-9.*

RL8 and RL9 on *page 11.8-2 or 11.8-7*, when energized, select the Current function.

RL24 and RL25 on *page 11.8-2 or 11.8-9* select the Ohms function.

RL23 connects the Voltage outputs to the instrument terminals.

For the analog connections refer to *sub-section 10.3.*

10.4.4.2 Voltage Output

Selection of the DC or AC Voltage function at the front panel also deselects Current and Ohms functions in software. The $\overline{\text{I FNCT}}$ and Ω FNCT signals are set to logic-1, and decoded by M17-8, M16-10 and M16-11 to set the V OUTPUT signal to logic-1. This activates relay RL23, connecting the voltage output lines to the front panel terminals.

The $IR_{2\text{-}Ø}$ code is '1,1,1', setting only M6 'Q7' (pin 4) output to logic-1. Thus the Current range relays RL2, RL3 and RL4 are all un-energized. If Option 40 (Current function) is fitted, relays RL8 and RL9 are un-energized, disconnecting the current output and shorting it to the current common-I1. RL1 is latched in the 1A position, selecting R79 in preference to R80; and RL5 connects the 10mA/100mA filter.

Since $\overline{\text{I FNCT}}$ is at logic-1, the DCI and ACI signals are at logic-Ø; relays RL7 and RL26 are un-energized, disconnecting the DC and AC references from the current circuitry. *(Refer to Circuit Diagram 430844 Pages 11.7-1 and 11.7-5)*

In the AC assembly , the logic-1 $\overline{\text{I FNCT}}$ signal (J7-86) de-energizes RL9. This disconnects the ACI REF lines (J7-69 to J7-72) from the ACV lines. Thus the voltage to current converter (M8 on the Current or Current/Ohms assembly) receives no input voltage, and so no current is generated. $\overline{\text{AC FNCT}}$ connects the ACV lines only for voltage ranges.

10.4.4.3 Current and Ohms Function Switching

The function selection logic is included later in the descriptions at *sub-sections 10.4.5 and 10.4.6.*

10.4.5 CURRENT SWITCHING LOGIC

(Circuit Diagram 430614 Page 11.8-2 or 401008 Page 11.8-7)

10.4.5.1 'I OUTPUT' Relays RL8 and RL9

Whenever a switching command has been received, the CPU performs a control-data transfer and the $\overline{\text{UPD(IG)}}$ line from J8-60 is pulsed to logic-Ø for 50ms. Q1 and Q7 remain cut off until the pulse arrives. The pulse turns Q1 and Q7 on, applying +15V to the relays connected to Q1 collector.

Any selected relays are thus energized by 30V, but after the $\overline{\text{UPD(IG)}}$ pulse has ended they are held on by the 13.3V between -0.7V at the cathode of D2 and -14V at the selected driver (M20) output. This method reduces the local heat, generated by energized relay solenoids, in the relay contacts.

The $\overline{\text{I FNCT}}$ and OFF signals are decoded so that RL8 and RL9 are energized only when the Current function has been selected and Output is ON.

(i.e. RL8/9 are energized if M16-4 [$\overline{\text{OFF}}$•I FNCT] = logic-1).

10.4.5.2 'DCI' and 'ACI' Relays RL26 and RL7

The $\overline{\text{I FNCT}}$, BARK and DC I signals are decoded so that RL7 and RL26 can be energized only when the Current function has been selected and the Watchdog has not 'BARK'ed.

Under these conditions; if DC Current is chosen, then the DC I signal is at logic-1, so M9-10 is also at logic-1 and RL7 closes its contacts to apply the DC Reference 'REF' to its voltage-to-current converter. If AC Current is chosen; DC I is at logic-Ø, so M9-9 goes to logic1 and RL26 closes its contact. This connects the output from its voltage-to-current converter M8 to the input of its current amplifier.

Function	Signals						Relays Activated	
							Current, Ohms or Current/Ohms Assembly as applicable RL8 RL24 RL23 RL7 RL26 RL9 RL25 (Latching Relays - * = Pin 1 at Logic-1)	AC Assembly RL9 RL10 RL2 RL2
	OFF	BARK	$\overline{\text{I FNCT}}$	$\overline{\Omega\text{ FNCT}}$	DCI	$\overline{\text{AC FNCT}}$		
DCI	Ø	Ø	Ø	1	1	1	* *	
ACI	Ø	Ø	Ø	1	Ø	1	* *	*
DCV	Ø	Ø	1	1	Ø	1	*	
ACV	Ø	Ø	1	1	Ø	Ø	*	*
Ω	Ø	Ø	1	Ø	Ø	1	*	

TABLE 10.1 CURRENT/OHMS ASSEMBLY - FUNCTION LOGIC

10.4.5.3 Current Range Relays RL1, 2, 3, 4 and 5

M12 is a Darlington open-collector inverting driver array. The relay drive logic places a logic-1 (0V) on the input of the selected drivers and logic-Ø (-15V) on those not required. A selected driver operates its relay by pulling its output to -14V.

The octal Current Ranging signal $IR_{2\text{-}Ø}$ is decoded by M6 to provide four individual outputs for Range relays:

Range	M6 Relay Output		Reference Source DC	AC
1A	Q2	RL1	-2V to +2V	1V Range
100mA	Q3	RL3	-20V to +20V	10V Range
10mA	Q4	RL2	-20V to +20V	10V Range
1mA	Q5	RL4	-20V to +20V	10V Range
100µA	Q5	RL4	-2V to +2V	1V Range

The Q3 and Q4 decoded outputs for the 100mA and 10mA ranges are ORed at M17-6 to operate RL5, which introduces HF filter capacitor C49 on both these ranges.

RL1 is a bistable latching relay with a single operating solenoid. A logic-1 at pin 1 switches the 1A range on, and a logic-Ø switches it off. Normally pin 1 is floating on open collector, so the relay remains latched in one bistable state with its solenoid un-energized. During the 50ms $\overline{UPD(IG)}$ pulse, non-inverting buffer M1 on the Clamp assembly is enabled, allowing the M6 Q2 state to change RL1 over (if programmed), before the $\overline{UPD(IG)}$ pulse ends.

10.4.5.4 Current Zero-Output

DC Current Zero

The DC Current output can be continuously incremented between its negative and positive Full-Scale outputs. Thus zero output can be selected by operator-adjustment of the 'REF' value using the 'OUTPUT' keys, or pressing the 'Zero' key, which ramps REF to zero. The zero value is corrected during Routine Autocalibration.

AC Current Zero

For AC zero output, as each range operates only between 9% and 200% of nominal, zero cannot be selected by adjustment of the OUTPUT keys. The AC zero is normally obtained by using the 'Zero' key which, through software, disconnects the lines from the current generator to the I+ and I- terminals.

The 'OFF' signal is set to logic-1, and the $IR_{2\text{-}Ø}$ code is 'Ø,Ø,Ø'. This sets all M6 outputs to logic-Ø, so the Current Range relays RL2,RL3 and RL4, and the filter relay RL5, are all un-energized, and RL1 latches in the $\overline{1A}$ position (R79 is selected in preference to R80).

Relays RL8 and RL9 are de-energized by the OFF signal, to open-circuit the I+ and I- terminals, and short the current amplifier output to common-I1. While setting OFF to logic-1, the CPU also forces the Precision DC Reference to ramp down to zero, so the AC reference voltage also falls to zero, and the current generator has no input. Thus the high current amplifier is not trying to produce an output current, and will not be damaged.

Function	Range	Range Code $IR_{2\text{-}Ø}$ IR_2	IR_1	$IR_Ø$	M6 Output Pins Q2 2	Q3 15	Q4 1	Q5 6	Q7 4	Relays Activated RL1 1+ 12- (Latching)	RL1 1- 12+	RL2	RL3	RL4	RL5	RL8 RL9
V or Ω	N/A	1	1	1					1		*				*	
DCI or ACI	100µA	1	Ø	1				1			*			*		*
	1mA	1	Ø	1				1			*			*		*
	10mA	1	Ø	Ø			1				*	*			*	*
	100mA	Ø	1	1		1					*		*		*	*
	1A	Ø	1	Ø	1					*						*
ACI ZERO	Any	Ø	Ø	Ø							*					

TABLE 10.2 CURRENT RANGING LOGIC

10.4.6 RESISTANCE SWITCHING LOGIC

(Circuit Diagram No. 430614 Page 11.8-2 or 401047 Page 11.8-9).

10.4.6.1 Output Switching.

Whenever a switching command has been received, the CPU performs a control-data transfer and the $\overline{\text{UPD(IG)}}$ line from J8-60 is pulsed to logic-Ø for 50ms. Q1 and Q7 remain cut off until the pulse arrives. The pulse turns Q1 and Q7 on, applying +15V to the relays connected to Q1 collector.

Any selected relays are thus energized by 30V, but after the $\overline{\text{UPD(IG)}}$ pulse has ended they are held on by the 13.3V between -0.7V at the cathode of D2 and -14V at the selected driver (M20) output. This method reduces the local heat, generated by energized relay solenoids, in the relay contacts.

The $\overline{\Omega\ \text{FNCT}}$, BARK and OFF signals are decoded so that RL24 and RL25 are energized only when the Ohms function has been selected, Output is ON and the Watchdog has not barked.
(i.e. If M16-9 [$\overline{\text{OFF}}$•Ω FNCT•$\overline{\text{BARK}}$] = logic-1, RL24 and RL25 are energized).

10.4.6.2 Range Switching

Range control data is input as a 3-bit code on $\Omega R_{Ø}$, ΩR_1 and ΩR_2 lines. The bit-pattern is decoded by M2 in the Clamp assembly to activate the correct relay(s) for the selected range. The resulting variants are listed in *Table 10.3* against range selections.

Relay RL17 is activated to connect the lower Ohms (<1MΩ) ranges to the output line only when the Megohm ranges are not activated. This reduces the parallel leakage *(para 10.2.2.1)*. NOR gate M19-6 combines the signals which will activate RL17; bearing in mind that the polarized RL17 connections between its driver and the -7.5V rail are the reverse of all the other latching relays. Thus it closes its contacts when M19-6 is at logic-Ø (-15V), not logic-1 (0V).

The signal states which cause RL17 to close its contacts are:

	$\overline{\Omega\ \text{FNCT}}$	- logic-1 (Ohms function not selected)
or	**Ω R2**	- logic-Ø (10Ω, 100Ω, 1kΩ, or 10kΩ selected)
or	**Ω ZERO**	- logic-1 (Ohms Zero selected)
or	**J18-1**	- logic-1 (Clamp assembly M2 Q4 at logic-1 - 100kΩ range selected)

10.4.6.3 Ohms Zero.

The $\overline{\Omega\ \text{FNCT}}$ and Ω ZERO signals are NORed by M19-10 and inverted by M17-12 so that RL16 is activated either when the Ohms function has been selected and the Zero Key has been pressed, or at times when the Ohms function is not selected.

Range	Range Code ($\Omega R_{2\text{-}Ø}$) ΩR_2	ΩR_1	$\Omega R_Ø$	M2 'Q' Output (Clamp Assembly)	Relays Activated (All latching relays)	
10Ω	Ø	Ø	Ø	QØ	RL13)	
100Ω	Ø	Ø	1	Q1	RL10)	
1kΩ	Ø	1	Ø	Q2	RL14)	
10kΩ	Ø	1	1	Q3	RL12)	Each relay selects when
100kΩ	1	Ø	Ø	Q4	RL11)	pin 1 = Logic-1 (0V)
1MΩ	1	Ø	1	Q5	RL20)	
10MΩ	1	1	Ø	Q6	RL19)	
100MΩ	1	1	1	Q7	RL18)	
Ω Zero	(All Range relays deselected)				RL16	Relay selects when pin 1 = Logic-1 (0V)
Ranges <1MΩ (excluding Ω Zero)					RL17	Relay selects when pin 12 = Logic-1 (0V)

TABLE 10.3 OHMS RANGING LOGIC

10.4.7 DEFAULT AND STATUS LOGIC

10.4.7.1 'OFF'

The OFF signal is combined with the $\overline{\text{I FNCT}}$ and $\overline{\Omega \text{ FNCT}}$ signals to ensure that when the instrument OUTPUT OFF key is pressed, the selected function's circuitry is disconnected from the terminals. For Current outputs, RL8 and RL9 disconnect the terminals from the current output; and for Resistance, RL24 and RL25 disconnect the standard resistor.

10.4.7.2 'BARK'

The BARK signal is combined with the $\overline{\Omega \text{ FNCT}}$ and DC I signals to ensure that when the Watchdog barks, the selected function is disabled. For DC Current outputs, RL7 disconnects the REF signal from the High-current V-to-I converter; for AC Current outputs, RL26 disconnects the drive from the AC reference V-to-I converter to the High current amplifier; and for Resistance, RL24 and RL25 disconnect the standard resistor.

The effects of '$\overline{\text{BARK DELAYED}}$' follow after 47ms.

10.4.7.3 '$\overline{\text{BARK DELAYED}}$'

If the Watchdog is activated, the BARK signal is generated, and 47ms later all outputs from the Control Data latches in the Reference Divider are 'Tristated' by the '$\overline{\text{BARK DELAYED}}$' signal. On the Current, Ohms or Current/Ohms assembly, this allows the pull-up resistors (AN1) and pull-down resistors (AN3) to become effective. At the same time the BARK DELAYED signal sets a -15V pulse on the $\overline{\text{UPD(IG)}}$ line for 1.5 seconds (M41 on *page 11.4-5*), to ensure that the latching relays on the DC and Current, Ohms or Current/Ohms assemblies will respond to the default state.

The full effect of the default is that relays RL5, RL16, RL17 and RL23 are activated, the remainder are not:

The Current and Ohms circuits are disconnected from the terminals, but relay RL23 connects the Power and Sense lines from the DC assembly to the terminals. However, on the DC assembly the same default has disconnected the voltage output from the lines.

The Current ranges are deselected, but relay RL5 holds the HF filter in circuit.

All Ohms standard resistors are deselected as well as disconnected from the terminals; the 4-wire Ohms-Zero short is activated, but is also isolated from the instrument terminals by RL24 and RL25.

As the Watchdog detects certain malfunctions in processor or Analog Control transfer operation, the default is a safe holding state, and subsequent changes will depend on the reaction of the CPU to the event. The Watchdog is described in *sub-section 6.4.6*.

10.4.7.4 '$\overline{\text{I/}\Omega \text{ ST}}$'

The $\overline{\text{I/}\Omega \text{ ST}}$ line at J8-98 is pulled down to -15V (logic-Ø) for as long as the Current/Ohms assembly is fitted in the instrument. This state is passed back via the Reference Divider (J4-68) and the SSDA serial link to the CPU (Circuit Diagram 430652 *page 11.4-4*). Thus the CPU recognizes that the Current/Ohms assembly is fitted, and can operate the appropriate programs.

DATRON INSTRUMENTS FAILURE REPORT.

Please complete all sections and return with your instrument.

Company: .....

Division: ..... Department/Mail Stop .....

User, Name: ..... Telephone ..... Ext .....

Serial number: .....

Datron Return Authorisation number ..... Date of failure .....

Brief description of fault: .....

.....

.....

.....

.....

Fault details:

is the fault present on all ranges? Yes ☐ No ☐ Not Applicable ☐

if no describe: .....

is the fault present on all functions? Yes ☐ No ☐ Not Applicable ☐

is the fault: Permanent ☐ Intermittent ☐

if intermittent under what conditions does the fault re-appear .....

.....

Does the instrument pass 'self test?' Yes ☐ No ☐

Any fail/error message displayed:

Now: Yes ☐ No ☐ if yes describe .....

.....

At the time of fault: Yes ☐ No ☐

if yes describe .....

.....

Prior to fault: Yes ☐ No ☐

if yes describe .....

.....

Is the instrument used on I.E.E.E 488 bus? Yes ☐ No ☐

Is the instrument normally enclosed in a rack? Yes ☐ No ☐

Approximate ambient temperature .....

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