MODEL 650
MAINTENANCE MANUAL

Manual Revision 9/88
Manual Part Number: 1300-00-0420

Scans
By
Artek Media

Artek Media
1042 Plummer Cir. SW
Rochester, MN 55902

www.artekmedia.com

"High resolution scans of obsolete technical manuals"

If your looking for a quality scanned technical manual in PDF format please visit our WEB site at www.artekmedia.com or drop us an email at manuals@artekmedia.com and we will be happy to email you a current list of the manuals we have available.

If you don't see the manual you need on the list drop us a line anyway we may still be able to point you to other sources. If you have an existing manual you would like scanned please write for details, This can often be done very reasonably in consideration for adding your manual to our library.

Typically the scans in our manuals are done as follows;

1) Typed text pages are typically scanned in black and white at 300 dpi.
2) Photo pages are typically scanned in gray scale mode at 600 dpi
3) Schematic diagram pages are typically scanned in black and white at 600 dpi unless the original manual had colored high lighting (as is the case for some 70's vintage Tektronix manuals).

If you purchased this manual from us (typically through our Ebay name of ArtekMedia) thank you very much. If you received this from a well-meaning "friend" for free we would appreciate your treating this much like you would "share ware". By that we mean a donation of at least $5-10 per manual is appreciated in recognition of the time (a manual can take as much as 40 hours to reproduce, book, link etc.), energy and quality of effort that went into preserving this manual. Donations via PayPal go to: manuals@artekmedia.com or can be mailed to us the address above.

Thanks

Dave & Lynn Henderson
Artek Media

WARRANTY

Wavetek warrants that all products manufactured by Wavetek conform to published Wavetek specifications and are free from defects in materials and workmanship for a period of one (1) year from the date of delivery when used under normal operating conditions and within the service conditions for which they were furnished.

The obligation of Wavetek arising from a Warranty claim shall be limited to repairing, or at its option, replacing without charge, any product which in Wavetek's sole opinion proves to be defective within the scope of the Warranty. In the event Wavetek is not able to modify, repair or replace non-conforming defective parts or components to a condition as warrantied within a reasonable time after receipt thereof, Buyers shall be credited for their value at the original purchase price.

Wavetek must be notified in writing of the defect or nonconformity within the Warranty period and the affected product returned to Wavetek's factory or to an authorized service center within (30) days after discovery of such defect or nonconformity.

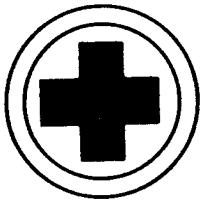
For product warranties requiring return to Wavetek, products must be returned to a service facility designated by Wavetek. Buyer shall prepay shipping charges, taxes, duties and insurance for products returned to Wavetek for warranty service. Except for products returned to Buyer from another country, Wavetek shall pay for return of products to Buyer.

Wavetek shall have no responsibility hereunder for any defect or damage caused by improper storage, improper installation, unauthorized modification, misuse, neglect, inadequate maintenance, accident or for any product which has been repaired or altered by anyone other than Wavetek or its authorized representative and not in accordance with instructions furnished by Wavetek.

Exclusion of Other Warranties

The Warranty described above is Buyer's sole and exclusive remedy and no other warranty, whether written or oral, is expressed or implied. Wavetek specifically disclaims the implied warranties of merchantability and fitness for a particular purpose. No statement, representation, agreement, or understanding, oral or written, made by an agent, distributor, representative, or employee of Wavetek, which is not contained in the foregoing Warranty will be binding upon Wavetek, unless made in writing and executed by an authorized Wavetek employee. **Under no circumstances shall Wavetek be liable for any direct, indirect, special, incidental, or consequential damages, expenses, losses or delays (including loss of profits) based on contract, tort, or any other legal theory.**

SAFETY FIRST



Protect yourself. Follow these precautions:

- Don't touch the outputs of the instrument or any exposed test wiring carrying the output signals. This instrument can generate hazardous voltages and currents.
- Don't bypass the power cord's ground lead with two-wire extension cords or plug adaptors.
- Don't disconnect the green and yellow safety-earth-ground wire that connects the ground lug of the power receptacle to the chassis ground terminal (marked with ⏚ or ⚠).
- Don't hold your eyes extremely close to an rf output for a long time. The normally nonhazardous low-power rf energy generated by the instrument could possibly cause eye injury.
- Don't plug in the power cord until directed to by the installation instructions.
- Don't repair the instrument unless you qualify and know how to work with hazardous voltages.
- Pay attention to the **WARNING** statements. They point out situations that can cause injury or death.
- Pay attention to the CAUTION statements. They point out situations that can cause equipment damage.

WARNING

DO NOT RECHARGE, SHORT CIRCUIT, DISASSEMBLE, OR APPLY HEAT TO THE LITHIUM BATTERY INSIDE THE 650. VIOLATING THIS RULE COULD RELEASE POTENTIALLY HARMFUL LITHIUM. OBSERVE POLARITY WHEN YOU REPLACE THE BATTERY.

CAUTION

The 650 can deliver up to 12½ watts of output power. Always keep the output signal levels within the power range of your load.

WARNING

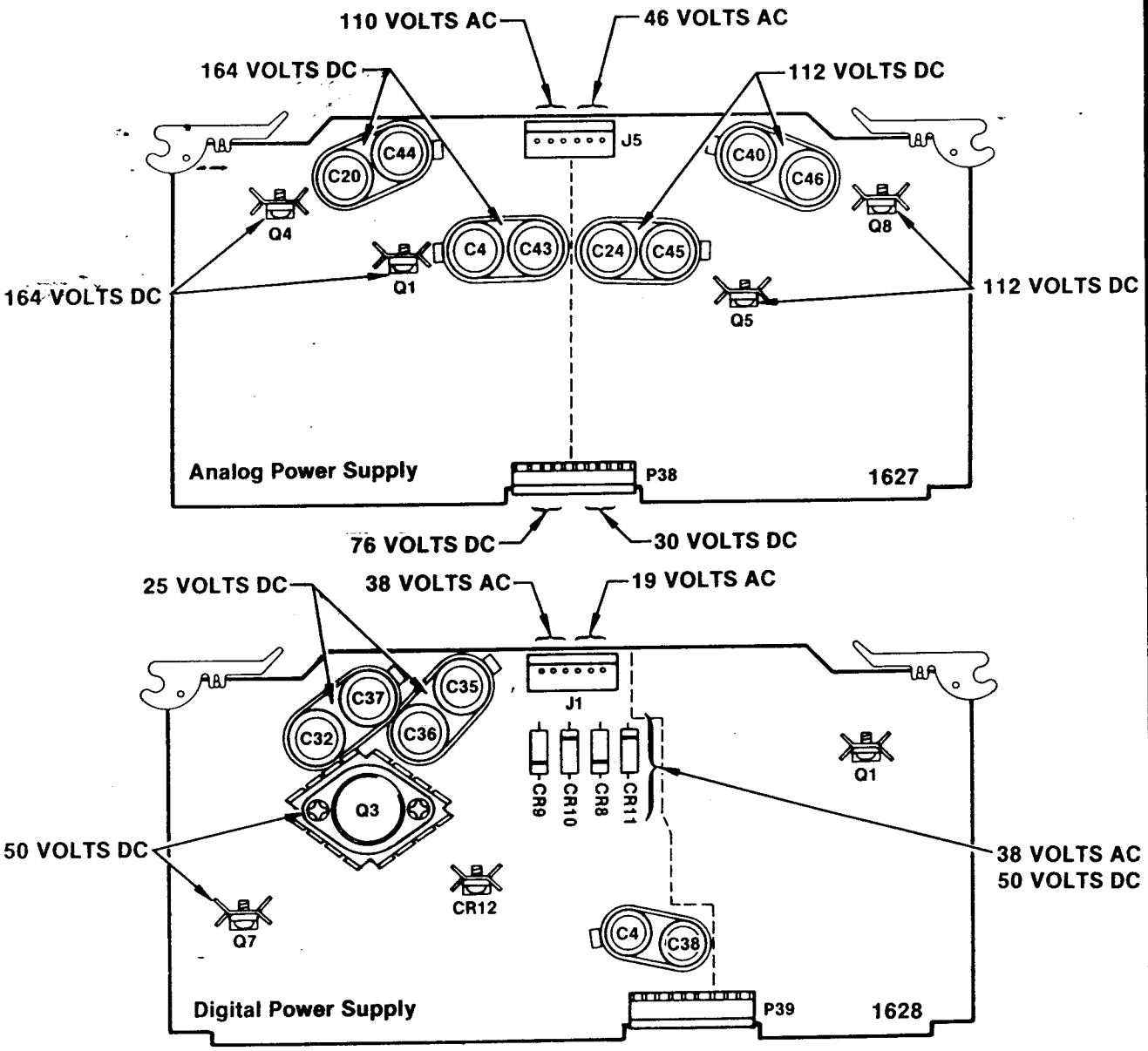
DANGEROUS POWER SUPPLIES
LETHAL VOLTAGES — HIGH CURRENTS — HOT HEATSINKS

DO NOT ATTEMPT TO REPAIR THE POWER SUPPLIES UNLESS YOU KNOW HOW TO WORK SAFELY WITH HIGH VOLTAGE, HIGH CURRENT, AND HIGH POWER.

WEAR SAFETY GLASSES AT ALL TIMES — DEFECTIVE CAPACITORS CAN EXPLODE.

CAPACITORS REQUIRE 40 SECONDS TO DISCHARGE.

USE AN EXTERNAL FAN TO COOL ANY SUPPLY OPERATED OUTSIDE THE 650 CHASSIS.



CONTENTS

CHAPTER 1

INTRODUCTION

1.1 SPECIFICATIONS

Instrument specifications are located in section 1 of the Model 650 Operator's Manual.

1.2 TOOLS AND TEST EQUIPMENT

You must have the following equipment to test, troubleshoot, calibrate and repair the 650.

Basic Equipment. You must have the following equipment for the procedures in the following sections:

Phase Measurement

Wavetek Model 601 Switching System Master Chassis
Wavetek Model 603 Switching System Front Panel
Wavetek Model 621 Switching System Phase Detector Module

Signal Sources

Wavetek Model 271 12MHz Pulse/Function Generator
Wavetek Model 178 Programmable Waveform Synthesizer
Wavetek Model 650 2MHz Variable Phase Synthesizer

CHAPTER 2

THEORY OF OPERATION

Section	Function
2.1 System Overview	Tells what the 650 does, how phase accumulation works, and what hardware performs each major function.
2.2 Input Board Set 2.3 MicroProcessor/S&H Board 2.4 Phase Engine Board 2.5 Phase Accumulator Board 2.6 RAM Board 2.7 DAC/Output Board 2.8 Ref/Cal Board	Lists the board functions, provides a block diagram to the circuit level, and describes individual circuits.
2.9 Power Supplies	Explains circuit operation of the switching power supplies.

See section 4 for wiring diagrams and schematics.

2.1 SYSTEM OVERVIEW

Section	Why You Should Read the Section
2.1.1 What Does the 650 Do?	You need to know what the 650 can do before you can understand how it works. Therefore, this section first describes phase synthesis, then lists all the other capabilities that support it.
2.1.2 How Does Phase Accumulation Work?	You need to understand phase accumulation before you study the circuits that perform it. Therefore, this section first describes this important concept, then shows how the 650 uses it to sweep frequency and phase.
2.1.3 What Does Each Board Do?	You need to know what each board does so you can relate the 650's functions to the circuits that perform them. Therefore, this section provides a system block diagram that shows all the boards and lists the functions each one performs.

2.1.1 What Can the 650 Do?

This section describes phase synthesis and lists all the 650 capabilities that support it. Knowing what the 650 can do will help you understand how it works.

Phase Synthesis. The Model 650 Variable Phase Synthesizer generates multiple waveforms at controlled phase angles. Each channel's output signal maintains an absolutely fixed and precisely controllable phase relationship with the output signals of the other channels. Phase accuracy holds for fixed frequency, swept frequency, and swept phase operation. Digital generation of the signals guarantees fixed accuracy across the entire range of frequency and phase.

Support Capabilities. The additional capabilities listed below support the 650's primary role as a phase synthesizer and enable it to serve both phase and non-phase applications.

Category	Capabilities		
Non-Sweep Modes	Continuous Triggered Burst	Sync Gated Async Gated Phase Lock	Waveform Hold AM
Sweep Choices	Frequency Sweep Phase Sweep Both Sweep Sequential Sweep	Hold Sweep Linear Sweep Log Sweep	Sine Sweep Random Sweep AM/FM/PM
Frequency/Phase/ Both Sweep Modes	Continuous Sweep with Auto Reset Continuous Sweep with Auto Reverse Triggered Sweep with Auto Reset Triggered Sweep with Auto Reverse Triggered Sweep/Hold with Trig Reset/Hold		Triggered Sweep/Hold with Trig Reverse/Hold Sequential with Triggered Steps Sequential with Continuous Stepping Sequential with Triggered Single Pass
Channel Control	Sine, Triangle, Square, Ramp, DC Waveforms Output Impedance Waveform Amplitude	Waveform Offset Square Wave Duty Cycle Phase Control Frequency Multiplication	Amplitude Modulation Sync Output Delta Frequency Ramp Duty Cycle
Triggering	Internal External	Front Panel GPIB	
Modulation	Frequency Modulation Phase Modulation	Amplitude Modulation Combined (FM/PM)	
Shift Keying	Synchronous Frequency Shift Keying (S-FSK) Asynchronous Frequency Shift Keying (A-FSK) Asynchronous Multiple Frequency Shift Keying Asynchronous Multiple Phase Shift Keying		
Sweep Progress	Screen Sweep Monitor	Sweep Horizontal Out	Sweep Marker
Unit Control	Front Panel	GPIB	MATE (optional)
Memory	25 Stored Instrument Setups		Lost-Power Instrument Setup
Maintenance	Self-Calibration		Self-Test

2.1.2 How Does Phase Accumulation Work?

This section describes phase accumulation, then shows how the 650 uses it to sweep frequency and phase. Read this section to learn the basics of this important concept so you can better understand the circuits that perform it.

Basic Concept. Figure 2-1 shows a simplified block diagram of the phase synthesis circuits. To generate a fixed-frequency waveform, the phase engine loads a phase value (such as 0.9°) into the frequency control register of the phase accumulator. The adder then accumulates phase by repeatedly adding this phase value to the total in the summing register. The accumulating phase total sequentially addresses the storage locations of the waveform RAM. As you can see, the phase accumulator actually serves as a RAM address generator.

Because the RAM stores the waveform as a series of digital amplitudes, the RAM output, when applied to the digital-to-analog converter, produces a stairstep waveform. Filtering removes the stairsteps and produces a smooth output.

The address-generation rate of the phase accumulator remains constant at 10MHz. This gives a fixed amount of time between additions for the phase engine to load new values, if any, in the frequency and phase control registers. Because the address generation rate remains fixed, the phase accumulator determines the frequency of the output waveform by jumping over intermediate RAM addresses. The size of the phase value in the frequency control register determines the size of the jumps.

RAM Memory. For simplicity, figure 2-1 shows a sine wave stored as five points. In reality, the 650 stores the waveform as 8192 points. This resolution allows great latitude in skipping steps before the output signal suffers. Output resolution decreases only for extremely wide and fast sweeps.

Waveform Changes. To change a channel's output waveform, the 650 simply loads a new waveshape in the RAM. Each channel can produce a different waveform without affecting phase coherence between channels.

Equivalent Addresses. The "equivalent addresses" shown with the RAM make the example easy to follow. In actual operation, the phase engine loads the registers with adjusted values that produce real RAM addresses instead of the equivalent addresses shown.

DAC/Filter. The digital-to-analog converter converts the digital amplitude values emerging from the RAM into a stair-step waveform. The 2MHz output filter removes the 10MHz clock frequency and its harmonics to produce a smooth analog waveform.

Simple Examples. Follow the table for each example to see how the values loaded in the frequency and phase control registers produce the fixed frequency, swept frequency, and swept phase outputs shown.

Swept Phase Illustration. The swept phase illustration shows three snapshots in the leftward progression of a sine wave. The wave begins in the position shown in the top figure. The middle figure shows it after it jumps 90° to the left, and the bottom one shows it after another jump 90° to the left. In actual operation, these large jumps would consist of thousands of very small jumps that would produce a smooth sweep.

Realistic Example. The phase engine actually loads a phase value (such as 0.9°) into the frequency control register. The phase value accumulates in the summing register at the fixed clock rate (10MHz for the 650). This phase accumulation controls addressing of the RAM memory and therefore the frequency of the waveform. To see more realistically how this phase accumulator technique works, assume a phase value of 0.9° and a clock rate of 10MHz:

$$\frac{0.9°}{\text{step}} \times \frac{10 \times 10^6 \text{ steps}}{1 \text{ second}} \times \frac{1 \text{ cycle}}{360°} = \frac{9 \times 10^6 \text{ cycles}}{360 \text{ seconds}} = 25 \text{ kHz output.}$$

$$\frac{360°}{\text{cycle}} \times \frac{1 \text{ step}}{0.9°} = 400 \text{ discrete steps in each cycle of a 25 kHz output}$$

Next, assume a phase value of 9° and a clock rate of 10MHz:

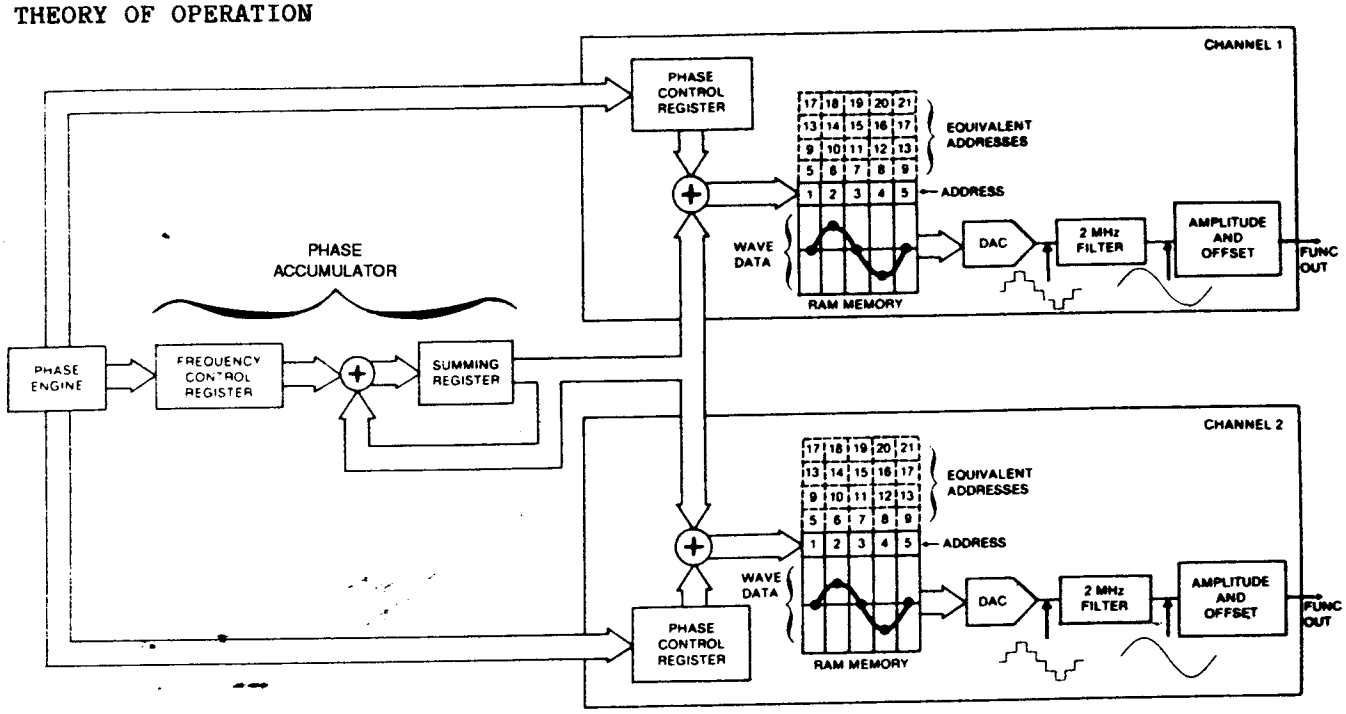
$$\frac{9°}{\text{step}} \times \frac{10 \times 10^6 \text{ steps}}{1 \text{ second}} \times \frac{1 \text{ cycle}}{360°} = \frac{90 \times 10^6 \text{ cycles}}{360 \text{ seconds}} = 250 \text{ kHz output}$$

$$\frac{360°}{\text{cycle}} \times \frac{1 \text{ step}}{9°} = 40 \text{ discrete steps in each cycle of a 250 kHz output}$$

Main Menu. When you enter a frequency in the main menu, the 650 loads the non-changing phase value that will produce that fixed frequency into the frequency control register.

Sweep Menu. When you enter START and STOP frequencies in the sweep menu, the 650 converts these into the incrementing series of phase values that it loads successively into the frequency control register as the sweep progresses. All channels sweep frequency simultaneously. Similarly, when you enter different START and STOP phases for each channel in the sweep menu, the 650 converts these into a separate series of incrementing values for each channel, then loads these series successively into the phase control registers of the channels as the sweeps progress. Each channel sweeps phase independently.

Channel Menu. When you use the channel menu to select a waveform for a channel, the 650 loads that waveform into the channel's RAM. Similarly, when you enter an amplitude and voltage offset for the waveform, the 650 loads these values into the channel's amplitude and offset circuits. Finally, when you enter a fixed phase shift for a channel, the 650 loads the value that will produce that shift into the channel's phase control register.

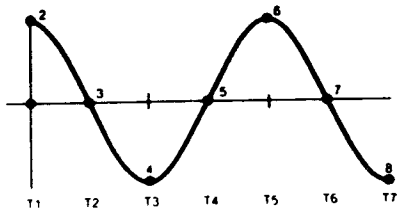


FIXED FREQUENCY, FIXED PHASE EXAMPLE

Freq Ctrl Reg		Sum Register Old		Sum Register New		Phase Ctrl Reg		RAM Adr		Time
1	+	0	=	1	+	1	=	2	at	T1
1	+	1	=	2	+	1	=	3	at	T2
1	+	2	=	3	+	1	=	4	at	T3
1	+	3	=	4	+	1	=	5	at	T4
1	+	4	=	5	+	1	=	6	at	T5
1	+	5	=	6	+	1	=	7	at	T6

↑ Fixed Frequency ↑ Fixed Phase (90°)

FIXED FREQUENCY

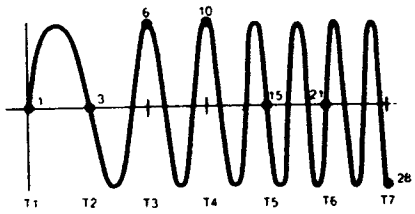


SWEPT FREQUENCY, FIXED PHASE EXAMPLE

Freq Ctrl Reg		Sum Register Old		Sum Register New		Phase Ctrl Reg		RAM Adr		Time
1	+	0	=	1	+	0	=	1	at	T1
2	+	1	=	3	+	0	=	3	at	T2
3	+	3	=	6	+	0	=	6	at	T3
4	+	6	=	10	+	0	=	10	at	T4
5	+	10	=	15	+	0	=	15	at	T5
6	+	15	=	21	+	0	=	21	at	T6

↑ Swept Frequency ↑ Fixed Phase (0°)

SWEPT FREQUENCY



SWEPT PHASE, FIXED FREQUENCY EXAMPLE

Freq Ctrl Reg		Sum Register Old		Sum Register New		Phase Ctrl Reg		RAM Adr		Time
1	+	0	=	1	+	1	=	2	at	T1
1	+	1	=	2	+	2	=	4	at	T2
1	+	2	=	3	+	3	=	6	at	T3
1	+	3	=	4	+	4	=	8	at	T4
1	+	4	=	5	+	5	=	10	at	T5
1	+	5	=	6	+	6	=	12	at	T6

↑ Fixed Frequency ↑ Swept Phase

SWEPT PHASE

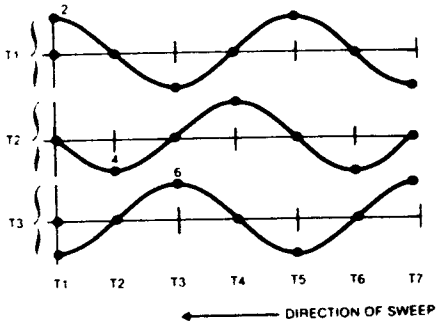


Figure 2-1. How the 650 Generates Phase-Coherent Waveforms

2.1.3 What Does Each Board Do?

This section provides a system block diagram that shows all the boards of the 650 and lists the functions each one performs. Study this diagram so you can relate the 650's functions to the circuits that perform them.

Diagram Explanation. Figure 2-0 shows the system block diagram for the 650. Data and signal processing flows from the keyboard/GPIB inputs at the left to the signal outputs at the right. The blocks of text list the major functions of each board.

2.2 INPUT BOARD SET (1473, 1474)

(Refer to figure 2-0.)

2.3 MAIN MICROPROCESSOR/SAMPLE AND HOLD BOARD (1531)

(Refer to figure 2-0.)

2.4 PHASE ENGINE BOARD (1625)

(Refer to figure 2-0.)

2.5 PHASE ACCUMULATOR BOARD (1383)

Major Function. The phase accumulator board determines the basic output frequency of all channels by generating a series of addresses that sweep through the waveforms stored in the RAMs on the RAM boards.

SUBFUNCTION	ACTIVE PHASE ACC BOARD CIRCUITS	SECTION
Sweep/Waveform Hold via the Hold Input Connector	Hold Input	2.5.4
Sweep Hold via [Hold/Resume] key or the GPIB bus	Control Processor Interface Hold Input	2.5.3 2.5.4
Master/Slave Operation	External Sync Logic Phase Sync and Phase Clear Connectors	2.5.6 2.5.6
[Main] CONT, TRIG, A-GATE, S-GATE, and PHSLK Modes [Sweep] Modes 1-29	Mode Control Logic External Sync Logic Acc Sync Logic Phase Accumulator	2.5.5 2.5.6 2.5.7 2.5.1
[Main] BURST Mode	Control Processor Interface Mode Control Logic External Sync Logic Acc Sync Logic Phase Accumulator	2.5.3 2.5.5 2.5.6 2.5.7 2.5.1
Control by Main MicroP Board (over the GPIO bus)	Control Processor Interface	2.5.3
Control by Phase Engine Board (over the phase engine bus)	Phase Engine Interface (bus address decoder/mode latches)	2.5.2

INFORMATION IN THIS SECTION		
INFORMATION	FUNCTION	LOCATION
Block Diagram	Shows data and control flow, circuit interaction, and related boards.	Figure 2-0
Sync and Control Logic Figure	Shows how the sync and control logic circuits generate the five major phase accumulator control signals.	Figure 2-0
Circuit Description Text	Individually describes the operation of each phase accumulator circuit.	Sections 2.5.1 to 2.5.7
Signal Description Table	Describes the function and action of each phase accumulator board signal. Alphabetical by signal name.	Table 2-0

RELATED INFORMATION IN OTHER SECTIONS		
INFORMATION	FUNCTION	LOCATION
GPIO Bus Figure	Shows how the main µP board controls the phase accumulator board over the GPIO bus.	Figure 2-0 in section 2.3
ΦENG Bus Figure	Shows how the phase engine board controls the phase accumulator board over the ΦENG bus.	Figure 2-0 in section 2.4

2.5.1 Phase Accumulator Circuit

Function. Generate a series of increasing addresses by repeatedly adding a small phase increment to a running total.

Components. A and B phase increment registers, an adder, and a phase summing register.

Operation. The phase increments in the A/B registers determine the frequency of the output signal. In operation, the phase accumulator adds the phase increment in register A or B to the current address in the phase summing register to produce a new and larger address. This new address addresses the waveform RAMs and calls up another point further along on the waveform stored in the RAM.

For a fixed-frequency output signal, the phase engine holds a fixed value in one of the phase increment registers. This value, repeatedly added to the value in the phase summing register at the fixed rate of 10MHz, makes the summing register address the waveform RAMS in equal steps and therefore produces a fixed-frequency output. Large phase increments produce higher frequencies by making the phase summing register step through the RAM (at 10MHz) with fewer, but larger, steps. Lower phase increments produce lower frequencies by stepping through the RAM (at 10MHz) with more, but smaller, steps.

For a swept-frequency output signal, the phase accumulator loads the phase increment registers with a series of larger and larger phase increments as the sweep progresses. In step-by-step operation, the phase accumulator adds the address increment in register A to the total in the summing register while the phase engine simultaneously loads the next larger address increment into the B register. Then, the control logic switches the registers and adds the new increment in the B register to the total in the summing register while the phase engine loads the next value in the series into the A register. The rate of increase of the series determines the rate and linearity of the sweep.

Although the phase accumulator sends a 16-bit address to the RAMs, it accepts and adds 40-bit phase increment values to allow extremely precise frequency control.

The following table shows how the phase engine uses the A and B registers to produce the operating modes.

TO IMPLEMENT THESE MODES:	THE PHASE ENGINE LOADS:
All Main (Non-Sweeping) Modes (CONT/TRIG/GATE/BURST/PHSLK)	An unchanging value in one register.
CONT/TRIG Frequency Sweep Modes (1-6)	A series of slowly incrementing values into alternating registers.
Frequency-Shift-Keyed Modes (7-8)	The base value in one register and the keyed value in the other register.
Frequency Sequence Modes (9-11)	A series of values from an internal table into alternating registers.
Frequency Modulation Modes (12, 29)	A series of values, each determined by the voltage level of an external signal, into alternating registers.

2.5.2 Phase Engine Interface Circuit

Function. Lets the phase engine board control the phase accumulator board.

Operation. The phase engine controls the phase accumulator by sending bytes of data over the ΦENG bus. The phase engine interface circuit accepts these bytes and loads them into the appropriate registers. The registers determine the operating mode, the burst count, and the output frequency.

U4. Address decoder U4 selects the register to receive the data on the data bus (see figure 2-0, phase engine bus). To load a register, the phase engine first puts data and an address on the ΦENG bus, then strobes U4 with line FSTB/. The FSTB/ strobe causes the particular Y output selected by the address to strobe and clock the data bus data into the register controlled by that Y output. In addition to loading registers, three of U4's Y outputs also serve as control signals for the sync and control logic.

U5, U6. To make the phase accumulator board operate in a given mode, the phase engine loads various bit patterns in sweep mode latches U5 and U6. The latched outputs of U5 and U6 then make the sync and control logic generate the specific control signals required by the selected operating mode. Figure 2-0, sync and control logic, shows how the outputs of U5 and U6 affect the sync and control logic and contains a table that lists the bit pattern for each mode.

2.5.3 Control Processor Interface Circuit

Function. Accepts the hold-sweep, resume-sweep, and reset-status-line-IOST4/ commands from the main μP board; returns the burst-complete response to it.

U2A. Flip-flop U2A converts the BURST END pulse into a held signal level so that the main µP does not have to monitor status line IOST4/ continuously. Selecting the [Main] BURST mode will pull D of U2A low and allow the BURST END pulse to set status line IOST4/ low. After the main µP has processed the burst-complete response, it resets U2A with the Y0 output of U3.

U2B. Flip-flop U2B converts the sweep hold/resume commands into a line level for the hold input circuit.

U3. Address decoder U3 converts the GPIO addresses into the sweep hold, sweep resume, and reset status line commands.

2.5.4 Hold Input Circuit

Function. Accepts all hold requests and sends a hold signal to the proper circuit.

		HOLD INPUT CIRCUIT SIGNALS	
TYPE OF HOLD	SOURCE	INPUTS	OUTPUTS
Sweep Holds (Frequency or Phase)	GPIB Bus	µPHOLD/ low	15D Out high
	[Hold/Resume] Key	µPHOLD/ low	15D Out high
	Hold Input Connector	Hold Input low	15D Out high
Waveform Hold	Hold Input Connector	Hold Input low	16A Q/ low

U15BC, U16A. NAND gates U15BC, flip-flop U16A, and HOLDEN determine the function of the Hold Input connector. HOLDEN low makes Hold Input hold frequency or phase sweeps by routing the hold signal through gate U15B to the phase engine. HOLDEN high makes Hold Input hold waveforms by allowing the hold signal to set Q/ of U16A low. ACCHOLD/ allows the phase engine board to apply a waveform hold.

U15D. Gate U15D accepts frequency and phase hold commands from either the main µP board or the Hold Input connector and sends them to the phase engine board.

U17B. Gate U17B either allows the ΦACCCLK clock line to run at 10MHz or holds it low, depending on the state of Q/ of U16A. If the clock runs, the system generates output waveforms point by point. Stopping the clock stops address generation and holds the waveform at the point reached when the hold was applied. Releasing the hold allows waveform generation to resume from the held point.

U11A, U17A. Buffers U11A and U17A put identical clock signals ΦACCCLK and BACCCLK on two lines for distribution to the mode, sync, and accumulator circuits. Fan-out limits prevent the use of just one clock line.

2.5.5 Mode Control Logic Circuit

Major Function: Generates the ΦACCCLR/ signal for the phase accumulator.

Secondary Function: Generates the LΦOVFL, LΦOVFL/, and the SELINCLK signals for the other control circuits; accepts the CLEAR/ signal from the external sync logic circuit.

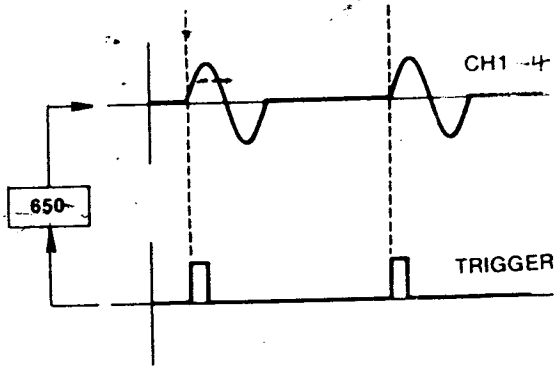
SIGNAL	FUNCTION
ΦACCCLR/	Clears the Φ summing register. Low stops generation of output waveforms; high allows generation of output waveforms.
ΦOVFL	Positive going 0.1μsec pulse generated whenever the phase accumulator adder reaches the highest address supplied to the waveform RAM (360° point of the stored waveform).
LΦOVFL	Positive-going 0.1 μsec pulse formed by synchronizing ΦOVFL to ΦACCCLK. Used by the external sync logic.
LΦOVFL/	Inverse of LΦOVFL. Used by the external sync logic.
SELINCLK	Either ΦACCCLK or LΦOVFL, as selected by INCLK/. Used by the acc sync logic.
CLEAR/	Allows the external sync logic or the phase engine to generate a ΦACCCLR/ and clear the phase summing register.

Operation. The phase engine sends the bit patterns shown in figure 2-0 (sync and control logic) to the phase accumulator to make the mode control logic generate the following five versions of ΦACCCLR/:

MODE	ACTION OF ΦACCCLR/
[Main] CONT, PHSLK [Sweep] Modes 1-29	Stays high continuously (the phase engine handles triggered sweeps).
[Main] TRIG	Steps high when TRIGGER steps high, then steps low on the next ΦOVFL.
[Main] A-GATE	Steps high when TRIGGER steps high, then steps low when TRIGGER steps low.
[Main] S-GATE	Steps high when TRIGGER steps high, then steps low on the first ΦOVFL after TRIGGER steps low.
[Main] BURST	Steps high when TRIGGER steps high, then steps low when RCO (burst counter carry) steps low.

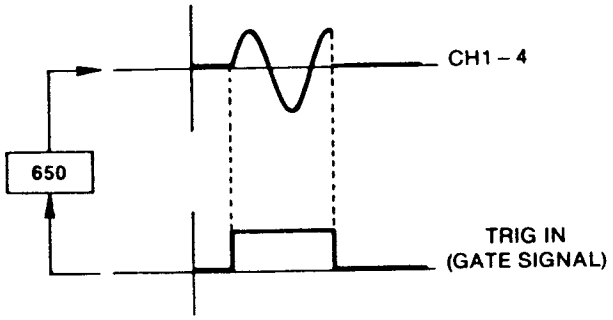
CONT, PHSLK, and All [Sweep] Modes. ΦACCCLR/ stays high continuously. Circuit Setup: CONT/ low holds flip-flop U13A cleared (Q/ output high) to block clearing of the phase summing register by the burst counter or flip-flop U7A. AGATE low disables gate U14B to prevent clearing of the phase summing register by the TRIGGER line. Operation: Holding ΦACCCLR/ high allows the phase accumulator to run continuously and generate a continuous output waveform. The phase engine board handles triggering of the triggered sweep modes.

TRIG Mode. ΦACCCLR/ steps high when TRIGGER steps high, then steps low on the next ΦOVFL. Circuit Setup: TGATE/ low (through U12C, U12B, and U13B) allows gate U14C to pass the output pulses of flip-flop U7A.

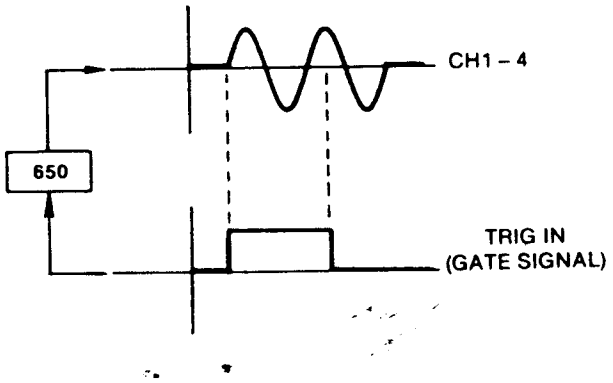


Operation: Stepping TRIGGER high clocks flip-flop U13A and sets output Q/ high. Rippling this high through gates U14D and U14A sets ΦACCCLR/ high and begins output waveform generation. When the waveform reaches the 360° point, ΦOVFL will shift high, causing flip-flop U7A to generate a high-going pulse. This pulse will pass through gate U14C and preset the Q/ output of flip-flop U13A low. Rippling this low through gates 14D and 14A sets ΦACCCLR/ low and stops output waveform generation.

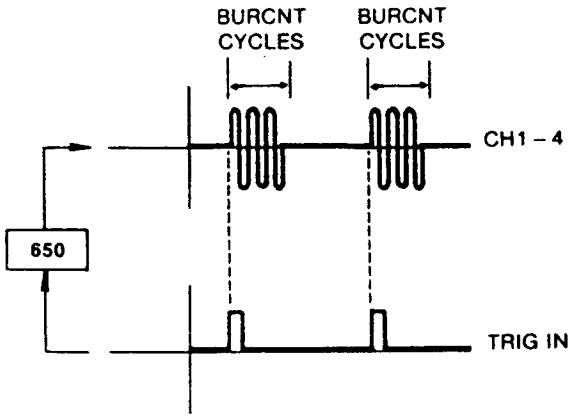
A-GATE Mode. ΦACCCLR/ steps high when TRIGGER steps high, then steps low when TRIGGER steps low. Circuit Setup: AGATE high lets gate U14B pass the TRIGGER signal. Operation: A low TRIGGER prevents signal generation by holding ΦACCCLR/ low through U14B and U14A. Stepping TRIGGER high releases the Φ summing register and begins waveform generation. Returning TRIGGER to low immediately clears the Φ summing register and stops the output waveform in mid-cycle.



S-GATE Mode. ΦACCCLR/ steps high when TRIGGER steps high, then steps low on the first ΦOVFL after TRIGGER steps low. Circuit Setup: SGATE high lets TRIGGER clear flip-flop U7A, and CONT/ high lets TRIGGER clock flip-flop U13A. Operation: Stepping TRIGGER high clocks flip-flop U13A and sets output Q/ high. Rippling this high through gates U14D and U14A sets ΦACCCLR/ high and begins output waveform generation. Stepping TRIGGER low releases the clear on flip-flop U7A and enables ΦACCCLK to clock the next positive-going pulse of ΦOVFL through to Q of U7A. Gate U14C converts this positive-going pulse to a negative going pulse that resets Q/ of flip-flop U13A to low. Rippling this low through gates 14D and 14A sets ΦACCCLR/ low and stops the output waveform at its 360° point.



BURST Mode. $\overline{\Phi ACCCLR}$/ steps high when TRIGGER steps high, then steps low when RCO (burst counter carry) steps low. Circuit Setup: BURST/ low lets LΦOVFL clock the burst counter, TGATE/ high lets the burst counter clear flip-flop U13B, and CONT/ high lets flip-flop U13A accept TRIGGER signals.



The phase engine sets up the mode control logic for burst operation as follows: First, it puts 65535 minus the Burst Count on the ΦENG data bus (for a burst of 100 cycles, 65435 would appear on the bus). Second, it loads this modified burst count into the internal register of the burst counter by pulling line Y1 (BC/) low via the address bus. The modified burst count immediately transfers from the internal register to the counter register because ΦACCCLR/ holds CLOAD/ low between bursts. Finally, when the operator selects BURST from the main mode menu, the phase engine loads the burst bit pattern into the mode latches.

The mode control logic controls the burst as follows: With the TRIGGER line low, output Q/ of flip-flow U13A stays low and holds ΦACCCLR/ low through gates U14D and A. When TRIGGER steps high, Q/ of U13A steps high, ΦACCCLR/ steps high, and the phase accumulator starts running. Flip-flop U7B generates pulse LΦOVFL at the end of each complete cycle of the output waveform. This pulse clocks input CCK of the burst counter, which begins counting up from the modified burst count loaded into its counter register. Output RCO/ steps low when the count reaches 65535 and back high when the count reaches 00000. RCO/ stepping low clears flip-flop U13B, which enables gate U14C. Flip-flop U7A produces pulses identical to the LΦOVFL pulses from flip-flop U7B. When the LΦOVFL pulse from U7B steps the count to 00000, the same pulse from U7A passes through gate U14C and presets flip-flop U13A. This sets Q/ low which, in turn, pulls ΦACCCLR/ low and stops generation of the output waveform.

2.5.6 External Sync Logic Circuit

Function. Synchronizes the output waveforms of interconnected 650 units.

System Interconnection. The synchronized group consists of a master and several slaves. The Phase Clear connector of the master connects to the Phase Clear connectors of all the slaves. The Phase Sync connector of the master connects to the Phase Sync connectors of all the slaves. The 10 MHz Ref connector of the master connects to the 10 MHz Ref connectors of all the slaves. The last slave has a 50 ohm termination at the 10 MHz Ref input.

Unit Configuration. To determine the configuration of each 650, the operator selects INDEPN, MASTER, or SLAVE in the [Utility] CONFIG menu. The front panel sends the operator's choice over the optolink to the main µP board, the main µP sends it over the GPIB bus to the phase engine board, and the phase engine sends it over the ΦENG data bus (as bits 8 and 9) to the phase accumulator board. Bits 8 and 9 appear at the output of the sweep mode latches as the MASTER EN and SLAVE EN lines.

System Operation. All units, whether master or slave, generate ΦOVFL, a pulse that occurs each time the adder of the phase accumulator reaches the highest address in the address generation cycle. This address represents the end (or 360° point) of the waveforms stored in the RAM board RAMs.

The master 650 converts ΦOVFL into a phase-sync pulse. The phase-sync pulse travels out Phase Sync of the master and into Phase Sync of all the slaves. Each slave compares the master phase-sync pulse to its internal sync pulse. If the pulses do not match, the slave generates a phase-clear pulse. The phase-clear pulse travels out Phase Clear of the out-of-sync slave and into Phase Clear of all the other slaves and the master. The phase-clear pulse resets the phase accumulator addresses of all units (master and slaves) to 0.

Unit Master Operation. Setup: MASTER EN line high, SLAVE EN line low.

Function 1: Generate phase-sync pulses for all the slaves. MASTER EN high allows NAND gate U48A to convert the LΦOVFL signal into the phase-sync signal. Phase-sync consists of a series of negative-going 0.1 µsec pulses. SLAVE EN low holds flip-flop U46A cleared (Q low) to keep the master-sync signal from passing through U50A, U46A, and U48B and out the Phase Clear connector.

Function 2: Accept a phase-clear pulse from any slave. MASTER EN high and SLAVE EN low makes OR gate 49B generate a high and enable the equivalent AND gate shown in dotted lines (U48BC, U50BC). This enables a phase-clear pulse from any slave to enter the Phase Clear connector and propagate through the gates to generate a CLEAR/ pulse and clear the master unit.

Unit Slave Operation. Setup: MASTER EN line low, SLAVE EN line high.

Function 1: Generate phase clear pulses. MASTER EN low holds the output of gate U48A continuously high so that exclusive-OR gate U50A can compare the phase-sync pulses from the master to the slave's internal LΦOVFL/ signal. If the signals don't match, a varying width pulse will appear at the output of gate U50A. Flip-flop U46A (enabled by SLAVE EN high) converts the mismatch pulse into a 0.1 µsec pulse. U48B converts this signal into a negative-going phase-clear pulse for this slave, all other slaves, and the master.

Function 2: Accept phase clear pulses. MASTER EN high and SLAVE EN low makes OR gate 49B generate a high and enable the equivalent AND gate shown in dotted lines (U48BC, U50BC). Enabling this gate allows a phase-clear pulse generated by this slave or any other slave to propagate through and clear this slave.

Unit Independent (Single-Unit) Operation. Setup: Both MASTER EN and SLAVE EN low.

Function 1: Do not generate or accept phase-sync pulses. MASTER EN low disables gate U48A to stop generation of phase-sync pulses. SLAVE EN low holds flip-flop U46A cleared to block acceptance of phase-sync signals.

Function 2: Do not generate or accept phase clear pulses. SLAVE EN low holds flip-flop U46A cleared to block generation of phase-clear pulses. MASTER EN low and SLAVE EN low makes OR gate 49B generate a low. This signal disables the equivalent AND gate shown in dotted lines (U48BC, U50BC) and stops acceptance of phase clear pulses.

2.5.7 Acc Sync Logic Circuit

Function. Generates the AINC/ and BINC/ signals for the phase increment registers of the phase accumulator.

Operation. The complementary AINC/ and BINC/ signals make the registers accept and deliver data as follows:

AINC/ Low — Register A sends current data to the adder, while
BINC/ High — register B takes new data from the phase engine data bus.

AINC/ High — Register A takes new data from the phase engine data bus, while
BINC/ Low — register B sends current data to the adder.

The components of the acc sync logic circuit perform the following functions:

U45B. Flip-flop U45B synchronizes register switching to the ΦACCCLK.

U45A. Flip-flop U45A synchronizes register switching to either the ΦACCCLK or the LΦOVFL signal, as selected by the multiplexer formed by gates U8A-D. All modes except sweep mode 7, SYNC-FSK, use ΦACCCLK.

U44. Data selector U44 selects the signal that will control AINC/ and BINC/. The "active" register feeds data to the adder, while the "inactive" register can, if required by the mode, receive new data from the phase engine.

INCSEL 10	SELECTS SIGNAL	IN ORDER TO
LL	TRIGGER	Make the TRIGGER signal select the active/inactive register. Modes: SYNC-FSK (7) and ASYNC-FSK (8).
LH	BINC	Make the phase engine directly select the active/inactive register by setting line BINC.
HL	43B-Q	Make the register currently receiving data from the phase engine send that data to the adder as soon as the phase engine finishes loading it. AINCO/ clearing Q to low says register A just received the last 16 bits of its 40-bit load; BINCO/ setting Q to high says B just received the last 16 bits of its 40-bit load. Modes: All main and sweep modes use this signal except SYNC-FSK (7), ASYNC-FSK (8), and EXTR-SEQUENCE (9).
HH	43A-$\overline{Q}$	Make the register that last received data from the phase engine send that data to the adder, but not until directed to by the TRIGGER or SWPCLK signal, as selected by ACCSEQ and gates U47A-D. Modes: EXTR-SEQUENCE (9). The ACCSEQ signal selects TRIGGER for mode 9.

Table 2-0. Signal Functions of the Phase Accumulator Board

ACCHOLD/	Sweep mode latch line 10. Allows the phase engine to hold the waveform by stopping the ΦACCCLK. Low applies hold; high releases it.
ACCCLK	10MHz system reference clock supplied by the ref/cal board.
ACCSEQ	Sweep mode latch line 1. Allows the phase engine to choose either TRIGGER or SWPCLK as the signal that will cause the last-loaded phase increment register to send its data to the adder. ACCSEQ low chooses TRIGGER; high chooses SWPCLK.
AGAC/	Sweep mode latch line 3. Asynchronous gate asynchronous clear control line. The phase engine sets this line low for the main A-GATE mode so that TRIGGER can immediately clear the Φ summing register, rather than wait for the output waveform to reach 360°.
AGATE	Sweep mode latch line 4. The phase engine sets this line high for the main A-GATE mode so that the TRIGGER signal can directly clear the Φ summing register.
AINC2/	Output Y2 of the ΦENG address bus decoder. Strobes the most significant 8 bits of the phase increment from the ΦENG data bus into U33 of the A register.
AINC/	Major control signal. Low directs the A phase increment register to send its stored phase increment to the adder.
AINC1/	Output Y3 of the ΦENG address bus decoder. Strobes the middle 16 bits of the phase increment from the ΦENG data bus into U38 and U28 of the A register.
AINC0/	Output Y4 of the ΦENG address bus decoder. Two functions: 1) Strobes the least-significant 16 bits of the phase increment from the ΦENG data bus into U18 and U23 of the A register, and 2) tells the acc sync logic circuit that the phase engine has completed loading the A register.
BACCCLK	Major control signal. Switched version of ACCCLK. This 10MHz clock synchronizes operation of the sync and control logic. Also called ΦACCCLK.
BC/	Output Y1 of the ΦENG address bus decoder. Strobes the burst count on the ΦENG data bus into the burst counter's internal register.
BINC	Sweep mode latch line 12. Allows the phase engine to directly select the phase increment register that will add its phase increment to the Φ summing register.

Table 2-0. Signal Functions of the Phase Accumulator Board

BINC/	Major control signal. Low directs the B phase increment register to send its stored phase increment to the adder.
BINC2/	Output Y5 of the ΦENG address bus decoder. Strobes the most significant 8 bits of the phase increment from the ΦENG data bus into U34 of the B register.
BINC1/	Output Y6 of the ΦENG address bus decoder. Strobes the middle 16 bits of the phase increment from the ΦENG data bus into U39 and U29 of the B register.
BINC0/	Output Y7 of the ΦENG address bus decoder. Two functions: 1) Strobes the least-significant 16 bits of the phase increment from the ΦENG data bus into U19 and U24 of the B register, and 2) tells the acc sync logic circuit that the phase engine has completed loading the B register.
BURST/	Sweep mode latch line 2. Low for main BURST mode operation. Allows the burst counter to count the number of complete output waveform cycles.
BURSTCOMP/	Board output signal line. The control processor interface sets this line low to tell the main μP that the phase accumulator has finished generating the requested number of output cycles.
CLEAR	Sweep mode latch line 15. Allows the phase engine to clear the phase summing register as required. For example, the phase engine pulses this line high to clear the phase summing register when the operator changes from sweep mode 12 to 13, from 24 to 23, and from 1 to 0.
CLEAR/	Output of external sync logic circuit. Clears the phase summing register.
CONT/	Sweep mode latch line 7. Low for all the sweep modes and for the main CONT and PHSLK modes. Blocks generation of ΦACCCLR pulses so that the phase accumulator can run free.
Hold In	Rear-panel BNC input for sweep or waveform holds (see HOLDEN). Low applies, high releases the hold.
HOLDEN	Sweep mode latch line 11. Allows the phase engine to select the function of the Hold In connector. [Utility] CONFIG WAVFM sets HOLDEN high for waveform hold, [Utility] CONFIG SWEEP sets HOLDEN low for sweep hold.

Table 2-0. Signal Functions of the Phase Accumulator Board

HOLD REQ	Board output signal line. The hold input circuit sends the hold request signal to the phase engine board. High requests the phase engine to hold the current frequency or phase sweep.
INCLK/	Sweep mode latch line 0. Chooses either ΦACCCLK or LΦOVFL as the signal that controls when the phase increment registers swap their add/load functions. The SYNC-FSK sweep mode uses LΦOVFL; all other main and sweep modes use ΦACCCLK.
INSEL1 INSEL0	Sweep mode latch lines 13 and 14. Allows the phase engine to select one of four phase increment register control lines. The control lines determine 1) which register will drive the adder while the other gets new data and 2) when the registers will swap functions. LL lets the TRIGGER line choose the adding register, LH lets the phase engine select the adding register with the BINC line, HL makes the most recently loaded register add immediately, and HH makes the most recently loaded register add when directed to by TRIGGER or SWPCLK.
LΦOVFL	Positive-going 0.1 µsec pulse formed by synchronizing ΦOVFL to ΦACCCLK. Used by the external sync logic.
MASTER EN	Sweep mode latch line 8. Determines the function of the 650 in a group of synchronized units. MASTER EN high and SLAVE EN low makes the unit a master. Both lines low make it independent (single unit operation).
µPHOLD/	Internal output of control processor interface circuit. Low indicates a sweep hold request from the front panel or GPIB bus.
MODE/	Output Y0 of the ΦENG address bus decoder. Two functions: 1) Strobes the bits on the ΦENG data bus into the sweep mode latches and 2) presets the Q output of flip-flop 43A to an initial state of 1.
ΦACCCLK	Major control signal. Switched version of ACCCLK. This 10MHz clock synchronizes operation of the sync and control logic. Also called BACCCLK.
ΦACCCLR/	Major control signal. Clears the Φ summing register. Pulsing this line low clears the register; holding it low stops generation of output waveforms.
ΦOVFL	Major control signal. Positive-going 0.1µsec pulse generated whenever the phase accumulator adder reaches the highest address supplied to the waveform RAM (360° point of the stored waveform).

Table 2-0. Signal Functions of the Phase Accumulator Board

Phase Sync	Rear-panel BNC input/output. Synchronizes the output waveforms of interconnected 650 units. Consists of a series of 100 nsec negative-going pulses.
Phase Clear	Rear-panel BNC input/output. Synchronizes the output waveforms of interconnected 650 units. 100 nsec negative-going pulse.
SLAVE EN	Sweep mode latch line 9. Determines the function of the 650 in a group of synchronized units. SLAVE EN high and MASTER EN low makes the unit a slave. Both lines low make it independent (single unit operation).
SWPCLK	Input signal supplied by the ref/cal board. SWPCLK's frequency depends on sweep mode (1-29), sweep function (linear, log, sine, random), and sweep compensation (on or off). One cycle of SWPCLK takes slightly more time than the phase engine needs to calculate and load the next phase increment of the sweep. Non-linear and compensated sweeps require more calculation time and therefore have lower SWPCLK frequencies than linear and non-compensated sweeps.
TGATE/	Sweep mode latch line 6. The phase engine sets this line low to disable the burst counter for the main TRIG, A-GATE, and S-GATE modes.
TRIGGER	Input signal supplied by the ref/cal board. Controls the TRIG, A-GATE, S-GATE, and BURST modes. A TRIGGER signal can come from any of these sources: internal trigger generator, Trig In BNC connector, front panel [Manual Trigger] key, or the GPIB bus.

2.6 RAM BOARD (1458)

Major Function. Stores the waveshape and controls the phase of two independent output channels.

	Waveform RAM	2.6.6
Generate Waveforms Add Fixed Phase Offset Sweep Phase	Control Logic Phase Accumulator Interface Phase Offset Register Adder Waveform RAM RAM Output Buffer	2.6.1 2.6.3 2.6.5 2.6.4 2.6.6 2.6.7

INFORMATION IN THIS SECTION		
INFORMATION	FUNCTION	LOCATION
Block Diagram	Shows data flow, circuit control, and related boards.	Figure 2-0
Circuit Description Text	Individually describes the operation of each RAM board circuit.	Sections 2.6.1 through 2.6.7
Signal Description Table	Describes the function and action of each RAM board signal. Alphabetical by signal name.	Table 2-0

INFORMATION IN OTHER SECTIONS		
INFORMATION	FUNCTION	LOCATION
ΦENG Bus Figure	Shows how the phase engine board controls the phase accumulator board over the ΦENG bus.	Figure 2-0 in section 2.4

2.6.1 Control Logic Circuit

Function. Lets the phase engine control the data processing circuits of the RAM board.

Components. Address decoders U7 and U8, NAND gates U9 and U10, and flip-flops U11, U12, and U13.

U7, U8. Address decoders U7 and U8 form the phase engine interface. All the Y outputs of each decoder stay high. The phase engine pulses them low one at a time by placing an address on the ΦENG address bus, then strobing the ΦSTBO/ line of the bus low. The resulting pulse on the selected Y output either controls circuits directly through gates or indirectly through the D flip-flops.

U10A, UI0B. Gates U10A and U10B allow the phase engine to load a waveform into RAM1 (with the RAM1WRITE/ signal), into RAM2 (with the RAM2WRITE/ signal), or into both RAMs simultaneously (with the RAMWRITE/ signal). These signals strobe the waveform amplitudes byte-by-byte from the RAM data input buffers into the waveform RAMs.

U11A. Flip-flop U11A allows the phase engine to turn RDATACLK off (to load waveforms), then back on (to generate output signals).

U11B. Flip-flop U11B allows the phase engine to control the RAM data bus. Signal RAMOE/ makes the RAM data bus either accept data from the data input buffers (load new waveform) or send data to the output buffers (generate output signals). Complimentary signal RAMOE disables the outputs of the data input buffers during output signal generation.

U9C, U10C. Gates U9C and U10C allow the phase engine to load a phase value into the channel 1 offset register (with the RAM1OFST/ signal), into the channel 2 offset register (with the RAM2OFST/signal), or into both RAMs simultaneously (with the RAMOFST/ signal). Flip-flops U12A, U12B, U13A, and U13B synchronize the loading with RADRSCLK.

2.6.2 RAM Data Input Buffer Circuit

Function. The RAM data input buffer lets the phase engine load sine, triangle, and ramp waveshapes into the waveform RAMs.

Components. D-Type flip-flops U23, U25, and U34.

Operation. The phase engine loads a waveform as a series of individual amplitude bytes, one for every addressable location in the RAM. To load one byte, the phase engine first latches that byte into the RAM data input buffers. Next, it loads the address of the RAM location that will store that byte into the phase offset register. Finally, it strobes the byte from the input buffer to the RAM.

The RAM data input buffer consists of 74ALS574 D-type edge-triggered flip-flops. Setting the OC/ line low makes the Q outputs deliver data to the

RAM. Setting OC/ high makes the outputs assume the high-Z state. A positive-going clock pulse clocks the bit present at the D input to the corresponding Q output.

2.6.3 Phase Accumulator Interface Circuit

Function. Stores each address generated by the RAM board. This lets the RAM board generate the next address while the adder processes the old one.

Components. D-Type flip-flops U5 and U6.

Operation. During waveform generation, the phase accumulator interface reads the output of the phase accumulator board each time RADDRSCLK steps high. The output of the phase accumulator interface then remains fixed for use by the adder for the rest of the RADDRSCLK cycle. During waveform loading, RAMOE/ pulls the OC/ line high to make the Q outputs assume the high-Z state. With the outputs high-Z, resistor networks RN1 and RN2 pull the adder input lines BACC3-15 high.

2.6.4 Adder Circuit

Function. Adds the address in the phase offset register to the address in the phase accumulator and places the total in the RAM address register.

Components. U14-U17, U26-U29 (adder) and D-type flip-flops U18, U19, U30, U31 (RAM address register).

Operation. The adders continously sum their inputs and present the result at their outputs. The RAM address register reads the output of the adders each time RADDRSCLK steps high. The output of the RAM address register then remains fixed for use by the RAM memories for the rest of the RADDRSCLK cycle.

2.6.5 Phase Offset Register Circuit

Function. Lets the phase engine either give a fixed phase offset (such as 35°) to the channel output signal or phase sweep the channel output signal.

Components. D-type flip-flops U1 through U4.

Fixed Phase Operation. The operator specifies a fixed phase by pressing [Channel], then PHASE, then entering a phase in degrees. The phase engine applies this phase by loading a fixed address in the phase offset register, then repeatedly adding it to the addresses delivered by the phase accumulator.

Swept Phase Operation. The operator specifies a phase sweep by pressing [Sweep], then PHASE, then following the menus to specify the type of phase sweep and its parameters. To apply a phase sweep, the phase engine puts a new and larger address in the phase offset register before each add cycle, then adds this address to the next address from the phase accumulator board.

2.6.6 Waveform RAM Circuit

Function. Stores the waveshape of the channel's output signal. The RAM puts out 12-bit digital bytes that represent amplitudes along the stored waveform.

Components. U20 and U21 (channel 1 or 3), and U32 and U33 (channel 2 or 4).

Operation. Each channel's RAM consists of two 8192-word x 8-bit CMOS chips that store the waveform as 12-bit amplitude values distributed across 8192 addresses. The phase engine loads sine, triangle, and ramp waveshapes in the waveform RAM. For square waves, the phase engine loads a sine in the RAM, then has the DAC/output board convert it to a square wave.

The RAM's OE/ line controls the mode of the data output line: L to read data out, H to write data in. Pulling the WE/ line low writes data into the currently addressed word.

2.6.7 RAM Output Buffer Circuit

Function. Stores each digital amplitude called from the RAM memories. This lets the control logic call the next amplitude from the RAMs while the DAC/output board processes the old one.

Components. D-type flip-flops U22, U24, U35.

Operation. RDATACLK clocks the values through at 10MHz.

Table 2-0. Signal Functions of the RAM Board

DATAON/	Output Y0 of address decoder U8. Negative-going pulse. Turns RDATACLK on for output signal generation.
DATAOFF/	Output Y1 of address decoder U8. Negative-going pulse. Turns RDATACLK off during RAM waveform loading.
RAM1OFST/	Output Y0 of address decoder U7. Negative-going pulse. Latches a new phase offset value into the channel 1 phase offset register. Flip-flops U13B and U13A synchronize the actual latching of the new value with RADRSCLK (10MHz). This lets the phase engine load a new offset value for every address processed, as required by phase sweeps.
RAM2OFST/	Output Y1 of address decoder U7. Negative-going pulse. Latches a new phase offset value into the channel 2 phase offset register. Flip-flops U12B and U12A synchronize the actual latching of the new value with RADRSCLK (10MHz). This lets the phase engine load a new offset value for every address processed, as required by phase sweeps.
RAMOFST/	Output Y2 of address decoder U7. Negative-going pulse. Simultaneously latches a new phase offset value into both the channel 1 and channel 2 phase offset registers.
RAMON/	Output Y2 of address decoder U8. Negative-going pulse. Sets the outputs of flip-flop U11B to RAMOE/ low and RAMOE high.
RAMOFF/	Output Y3 of address decoder U8. Negative-going pulse. Sets the outputs of flip-flop U11B to RAMOE/ high and RAMOE low.
RAMOE/ RAMOFF/	Complimentary outputs of flip-flop U11B. Three functions: 1) Configures the RAM data output bus to accept data from the RAM data input buffers or to read data to the RAM output buffers. 2) Enables the outputs of the RAM data input buffers for loading waveforms into the RAMS and disables them during output signal generation. 3) Enables/disables the outputs of the phase accumulator interface for signal generation/waveform loading.

Table 2-0. Signal Functions of the RAM Board

RAM1WRITE/	Output Y3 of address decoder U7. Negative-going pulse. Writes a new 12-bit amplitude data word from the channel 1 RAM data input buffer into the channel 1 waveform RAM (U32 and U33).
RAM2WRITE/	Output Y4 of address decoder U7. Negative-going pulse. Writes a new 12-bit amplitude data word from the channel 2 RAM data input buffer into the channel 2 waveform RAM (U20 and U21).
RAMWRITE/	Output Y5 of address decoder U7. Negative-going pulse. Simultaneously writes the same 12-bit amplitude data word from both RAM data input buffers into both channel waveform RAMs (U20, U21, U32, and U33).
RDATA/	Output Y6 of address decoder U7. Negative-going pulse. The positive-going edge of the pulse latches the 12-bit waveform amplitude word currently on the phase engine data bus into the RAM data input buffers.

2.7 DAC/OUTPUT BOARD (1467)

Major Function. Converts the stream of digital amplitudes from the RAM board into an analog signal, then processes it for output.

SUBFUNCTION	CIRCUITS RESPONSIBLE	SECTION
Convert D-to-A	TTL/ECL Translator DAC Data Latches Waveform DAC	2.7.1 2.7.2 2.7.3
Remove 10MHz from Waveform	6-Pole Filter	2.7.4
Convert Sine Wave to Variable Duty Cycle Square Wave	Square Shaper Square Wave Symmetry DAC	2.7.5 2.7.6
Control the Amplitude of the Output Signal	XY Multiplier Amplitude Control	2.7.7 2.7.8
Provide Signal Offset and Final Amplication	Output Amplifier	2.7.9
Provide Output Impedance and Attenuation	Attenuator	2.7.10
Provide Output Protection	Output Protection	2.7.11
Provide Internal Signals for Calibration and Test	Cal Mux Channel Select	2.7.12
Control Relays	Relay Drive Buffer	2.7.13
Generate the Sync Out Signal	Square Shaper	2.7.5

INFORMATION IN THIS SECTION		
INFORMATION	FUNCTION	LOCATION
Block Diagram	Shows data flow, circuit control, and related boards.	Figure 2-0
Circuit Description Text	Individually describes the operation of each DAC/Output board circuit.	Sections 2.7.1 through 2.7.12

INFORMATION IN OTHER SECTIONS		
INFORMATION	FUNCTION	LOCATION
ΦENG Bus Figure	Shows how the phase engine board compensates amplitude over the Φbus.	Figure 2-0 in section 2.4

2.7.1 TTL to ECL Translator Circuit

Function. Converts the 10MHz system clock (ACCCLK) and the 12-bit waveform amplitudes sent by the RAM board from TTL (0V/+5V) to ECL (-1V/-2V) voltage levels.

Operation. For a triangle waveform, the LSB (D0) clocks at 5MHz and the MSB (D11) clocks at 1.2KHz.

RN1-RN4. Resistor networks RN1 through RN4 convert bits D0 through D8 of each amplitude byte from TTL to ECL voltage levels. Although the resistor networks produce inexact ECL voltage levels, the DAC data latches can easily handle the slight variations.

U26. Level-translator U26 converts the system clock from TTL to precise ECL voltage levels. ACCCLK requires precise conversion because it controls presentation of the amplitude byte to the waveform DAC. Although MSB amplitude bits D9-D11 do not need precise level conversion, converting them through U26 eliminates the need for more resistor networks.

2.7.2 DAC Data Latch Circuit

Function. Synchronizes the level transitions of the individual bits of the amplitude byte.

Operation. The data byte present on the inputs of D flip-flops U1 and U2 transfers to the Q outputs only when ACCCLK (10MHz) steps from low to high. U1 and U2 ignore their inputs for the rest of the clock cycle. Resistor networks RN5 and RN6 rapidly pull the released outputs to -5V to further synchronize the level transitions.

2.7.3 Waveform DAC Circuit

Function. Converts the digital amplitude bytes into a stair-step analog waveform.

Operation. Because ACCCLK holds each input byte fixed for 100 nseconds, the output waveform has steps 100 nseconds wide.

R41. Potentiometer R41 adjusts the voltage level (threshold voltage) at which the DAC recognizes state changes at the input terminals. A DAC input terminal does not jump immediately to the voltage level for its new state, but instead follows a transition curve with a very steep slope. R41 puts the threshold voltage in the linear center of the curve, rather than at the non-linear ends. To understand the importance of the threshold setting, consider the change from 0111 to 1000. If the MSB changes before the other bits, the DAC sees this sequence: 0111 → (1111) → 1000. The temporary state (in parentheses) causes a high-voltage spike on the DAC output. Centering the threshold voltage eliminates such spikes. The calibration procedure tells how to set R41.

R4. Potentiometer R4 sets the output impedance of the DAC. The calibration procedure sets it to 66.67 ohms.

2.7.4 Six-Pole Filter Circuit

Function. Removes the voltage stair-steps from the output waveform of the DAC.

Operation. The low-pass filter passes frequencies below 2MHz (the specified output frequency range of the 650), but rolls off sharply above 2 MHz to remove the 10MHz system clock frequency riding on the waveform. The 6 poles give the filter a sharp roll-off rate.

U4-U5. Amplifiers U4 and U5 each have a gain of 2.6 (1 + 750Ω/464Ω) and three poles at 2MHz. Capacitors C* and C** control the gain vs frequency response of the filter. C* (in parallel with C11) controls the flatness of the filter response curve, while C** (in parallel with C17) controls the sharpness of the knee. Flattening the curve reduces the amount of correction the auto calibration program must apply at each frequency. The calibration procedure tells how to set these capacitors and shows their effect on the response curve.

R84. Potentiometer R84 sets the output amplitude of the filter. The calibration procedure sets R84 to a value that gives a 1kHz sine wave a known amplitude (10Vrms measured at the Func Out connector, rather than at the output of the filter). The auto calibration program then uses this known starting point to build correction curves for other amplitudes and frequencies.

2.7.5 Square Shaper Circuit

Function.. The square shaper converts the sine wave into a square wave with a variable duty cycle. The square wave symmetry DAC determines the duty cycle of the square wave.

Front Panel Control. To choose sine or square, press [Channel], then FUNC, then SINE or SQUARE.

Operation. Voltage comparator U18 compares SYMV (a DC voltage that controls the duty cycle) to FILTOUT (the sine wave emerging from the six-pole filter). Whenever the sine wave voltage exceeds SYMV, output OUTB switches low. See figure 2-0 (duty cycle waveforms). OUTA is the inverse of OUTB.

Signal OUTA (U18). Transistors Q4 and Q5 and resistors R57 and R58 convert OUTA into the 50Ω-impedance, TTL-level Sync Out signal. Relay K8, if present, allows the MATE option to turn the sync signal on and off.

Signal OUTB (U18). Transistor Q3, amplifier U20, and the XY multiplier, output amplifier, and 50Ω attenuator circuits convert OUTB into the square wave output waveform of the channel. OUTB turns Q3 on and off. The state of Q3 makes the precision current source (consisting of the ±10VR supplies and 1% resistors R88 and R59) deliver either of two fixed precise current levels to amplifier U20. These precise currents make U20 deliver a square wave with equally precise positive and negative amplitudes (4.4V p-p at TP10).

Q2. Transistor Q2 turns off the square shaper during sine wave generation to eliminate radiation of square wave noise into other circuits. RLY6, the same signal that makes relay K6 switch to a sine wave, also turns on transistor Q2. Q2, when on, holds the output of U20 low (-2.2V at TP10).

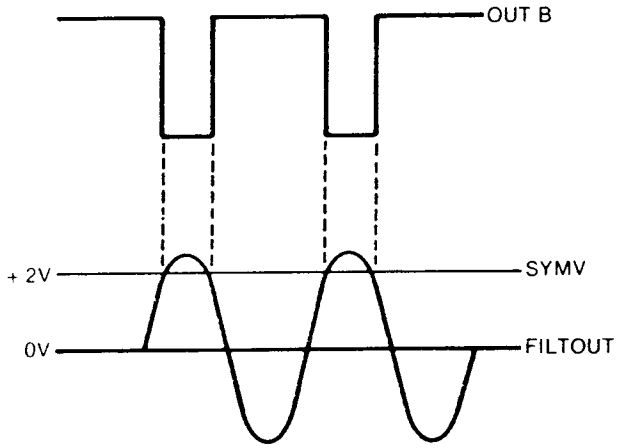
2.7.6 Square Wave Symmetry DAC Circuit

Function. The square wave symmetry DAC determines the duty cycle of the square wave generated by the square shaper circuit.

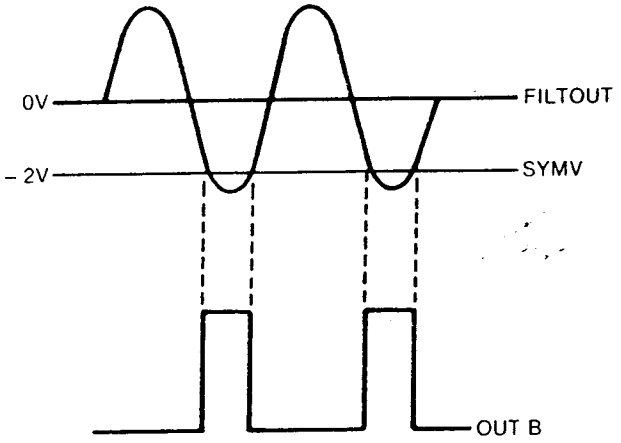
Front Panel Control. To enter a duty cycle, press [Channel], then SHIFT, then DUTY, then enter any duty cycle (in 1% increments) between 20% and 80%.

Operation. The front panel board sends the duty cycle to the main microprocessor board. The main microprocessor sends it over the GPIO bus to square wave symmetry DAC U11 on the DAC/output board. U11 converts the duty cycle into differential analog currents, amplifier U14A converts the currents to an analog voltage, and amplifier U14B offsets and scales the voltage to produce SYMV for the square shaper circuit.

SYMV TP6	MENU DUTY	SQUARE WAVE STAYS HIGH	LOW
+2V	80%	80%	20%
0V	50%	50%	50%
-2V	20%	20%	80%



80% DUTY CYCLE



20% DUTY CYCLE

Figure 2-0. Duty Cycle Waveforms

2.7.7 XY Multiplier Circuit

Function. Determines the amplitude of the output signal.

Operation. Relay K6 selects either the output of the six-pole filter or the square shaper for amplitude adjustment. Amplifier U6 inverts the signal to provide differential (180° out of phase) inputs to dual-channel linear multiplier U7. Running U7 differentially reduces distortion of the amplified signal. The AMPLCTRL signal (+0.3 to +3.0V at pin 1 of U7) determines the amount of amplification. Zener diodes CR1 and CR2 drop the +/-15V supply voltages down to +/-12V for U7's power supply inputs. Amplifier U8 inverts the CH1 output signal for addition to the CH2 output signal; amplifier U9 buffers the summed signal for delivery to the output amplifier circuit.

2.7.8 Amplitude Control Circuit

Function. Combines the effects of the three signals that can control the amplitude of the output waveform to produce one signal (AMPLCTRL) for the XY multiplier circuit.

SIGNAL	DESCRIPTION
AM In	Allows an external signal (connected to the rear-panel AM In connector) to amplitude-modulate the output waveform.
AMPL	Allows the operator to control the waveform amplitude. The front panel board sends the digital amplitude entered in the channel amplitude menu to the main microprocessor board, which generates the DC voltage level AMPL.
PHASE ENG DATA BUS	Allows the phase engine board to correct frequency-dependent amplitude errors caused by non-linearities in the output circuits. The phase engine sends correction factors (previously generated by the auto-calibration program) over the phase engine data bus to DAC U19 to correct frequency-dependent gain errors point-by-point as waveform generation proceeds.

Front Panel Control. To enter an amplitude, press [Channel], then AMPL, then enter an amplitude voltage.

Operation. Scaling by the +10V REF and the resistor network makes every 0.3V of AMPL (at TP4) produce a 5Vp-p increase in the output waveform.

U19. DAC U19 converts the data on the phase engine data bus into an amplitude correction for each point of the output waveform. Figure 2-0 (structure and operation of the phase engine bus) shows how the phase engine uses the data bus and the CSTB0/ and CSTB1/ signals (shown as CSTB/ on the DAC/output board schematic) to load a different amplitude correction value in each output channel. The DAC has a compensation range of +/-12.5%.

2.7.9 Output Amplifier Circuit

Function. Adds DC voltage offset and amplifies the signal up to 50Vp-p.

Front Panel Operation. To enter an offset, press [Channel], then OFFSET, then enter an offset voltage.

Operation. The output amplifier consists of very high slew rate wideband differential amplifier U25, associated transistors Q13-Q18, and voltage regulators VR1 and VR2. The output amplifier inverts the signal.

Gain Calibration. Manual calibration step 5 sets the gain (R119/[R92+R93]) of the output amplifier. Gain calibration requires an input signal with a known precise amplitude, a gain variation control, and a way to measure the output. For manual calibration step 5, the square shaper circuit provides the known reference input signal, R93 varies the gain from 5.4 to 7.5, and an external DVM measures the output amplitude at the rear-panel Func Out BNC connector. Calibration step 5 (called square wave amplitude adjust) has the operator adjust R93 until the output signal equals 10.0vrms. This corresponds to a gain of about 6.5.

Offset. Offset refers to the centerline DC offset voltage of the output waveform. Signal OFST (from the main microprocessor board) offsets the output by the amount specified in the channel menu.

U25, Q13-Q18. Zeners CR11 and CR12 reduce the ±38VDC supply voltages to ±15VDC for operational amplifier U25. The operating current used by U25 to keep the inverting (-) input at 0 volts varies according to the amplitude of MULT OUT, the applied input signal. The varying operating current develops corresponding varying voltages across resistors R120 and R124, which, in turn, drive transistors Q14 and Q17. The output of Q14 drives parallel transistors Q13/Q15 to produce the positive half of an output cycle, while Q17 drives Q16/Q18 to produce the negative half of an output cycle.

R133. Potentiometer R133 (on the output of U25) controls the aberrations (overshoot) and rise time of the output signal. Manual calibration step 7 tells how to set R133.

VR1 and VR2. Voltage regulators VR1 and VR2 limit the output current to 625 ma.

2.7.10 Attenuator Circuit

Function. Provides output switching, impedance, and attenuation.

Front Panel Control. To switch the output on/off and select either 0 or 50 ohm impedance, press [Channel], then SHIFT, then OUTPUT, then OFF, ON-0 ohm, or ON-50 ohm. To control attenuation, see paragraph K3 below.

Why Does the 650 Use Attenuation? Although the 650 can produce output voltages over a 1000-to-1 range (when the operator selects 50 ohm output impedance), the XY multiplier and output amplifier circuits work best (most linear) only over a 10-to-1 range (between 25V and 2.5V). Operating in the linear region of these circuits reduces the amount of amplitude correction the auto-calibration feature must add at each point of the waveform. The attenuator circuit lets the 650 produce an output voltage range of 1000-to-1 and, at the same time, operate the XY multiplier and output amplifier over only a 10-to-1 range.

To accomplish this, the main microprocessor board puts the output voltage entered in the channel menu into one of three subranges (25mV to 249mV, 250mV to 2.499V, or 2.5V to 25V). It then makes the output amplifier deliver 2.5V to 25V regardless of the range, and makes the attenuator divide this voltage by ten or a hundred to get the amplitude entered in the menu. For example, if the operator enters 1V in the menu, the output amplifier generates 10V and the attenuator divides it by 10 to get 1V at the output. The operator doesn't know about the attenuator because the main microprocessor automatically switches in the attenuation required for whatever voltage appears in the channel menu.

What About 0Ω Output Impedance? The 0 ohm output impedance shorts out the attenuator. Therefore, if the operator selects 0 ohm, the 650 limits its output to a single 100-to-1 amplitude range of 25V to 0.25V. Operating over this range makes the XY multiplexer and output amplifier operate in somewhat non-linear regions and forces the auto-calibration feature to apply larger correction factors to keep the output linear.

Component Descriptions. The attenuator consists of relays K1-K3, K5, and various precision resistors. One side of all the relay coils connects to +5V; therefore, a relay energizes when the appropriate Q output of U13 (the relay drive buffer) steps low. The schematic shows relays unenergized.

K1. Relay K1 allows the operator to turn the output on/off and also provides output overload protection. The channel menu controls K1 directly; the output protection circuit controls K1 indirectly. OFF in the channel menu opens K1; either ON-0 ohm or ON-50 ohm closes it. If the output protection circuit detects an overload, it opens K1 by disabling U13, the relay drive buffer.

K2. Relay K2 selects either 0 ohm or 50 ohm output impedance. The channel menu controls it directly. ON-0 ohm energizes the coil; ON-50 ohm de-energizes it.

K3, K5. Relays K3 and K5 control attenuation. Note that K3 requires energizing to add -20dB, while K5 requires non-energizing to add -20dB. To operate K3 and K5, first select an offset of 0V ([Channel] OFFSET 0 [Execute]). Second, select a voltage range from the Func Out column of table 2-0. Third, enter a voltage within that range in the channel menu ([Channel] AMPL ## [Execute]). The relays will operate as shown in table 2-0.

K7. Relay K7 connects the output amplifier to the ref/cal board to calibrate offset voltage, peak voltage, and phase.

Table 2-0. Operation of the Attenuation Relays

HIGH VOLTAGE OUTPUT AMP VOLTAGE RANGE	RELAY K3			RELAY K5			TOTAL (K3+K5) ATTENUATION	VOLTAGE AT Func Out BNC (as entered in channel menu)
	U13 P16	K3 COIL	K3 ATTN	U13 P13	K5 COIL	K5 ATTN		
2.5V ↔ 25V	H	NE	0dB	L	E	0dB	0dB (V/1)	2.5V ↔ 25.0V
2.5V ↔ 25V	L	E	-20dB	L	E	0dB	-20dB (V/10)	0.25V ↔ 2.499V
2.5V ↔ 25V	L	E	-20dB	H	NE	-20dB	-40dB (V/100)	0.025V ↔ 0.249V

E = Energized, NE = Not Energized

2.7.11 Output Protection Circuit

Function. Protects against internal and external current and voltage overloads.

Functional Schematic. Figure 2-0 gives a functional schematic of the output protection circuit.

Window Comparator. Operational amplifiers U24C and D form a window voltage comparator that continuously checks the output voltage and current.

Window Limits. Voltage regulator VR1 and resistors R107 and R108 determine the upper voltage limit of the window comparator. As long as the current through VR1 stays less than 625ma, the voltage at pin 2 stays fixed at about 37V. R108 and R107 divide the range between +37V and -5V down to an upper limit of +3V at pin 11 of U24D. Similarly, VR2, R109, and R153 divide the range between -37V and +5V down to a lower limit of -3V at pin 8 of U24C. Therefore, any output of the voltage monitor circuit that exceeds the window limits of +3V and -3V will trip output protection.

Overcurrent Detector. VR1's impedance increases when the current through it exceeds 625ma. An overcurrent therefore pushes the voltage at VR1-pin 2 toward ground. Because R107 connects to -5V, pushing the voltage of VR1-pin 2 to ground pushes U24D's + input negative. This action forces U24D's output negative and trips output protection. Similarly, an overcurrent through VR2 pushes the - input of U24C positive. This action forces U24C's output negative and trips output protection. Tripping output protection opens output relay K1 and disconnects any external short circuit or current source.

Voltage Monitor. Resistors R111, R113, R114, and relay K4 divide the output voltage down to the +3V/-3V range of the window comparator. Selecting an output impedance of 50 ohms and an output voltage between 0 and 2.499V opens relay K4. With K4 open, 1/10 of the Func Out voltage appears across R111 (110K) and 9/10 appears across both R114 (1Meg) and the comparator inputs. Selecting an output impedance of 50 ohms and an output voltage of 2.500 or greater closes relay K4. With K4 closed, 9/10 of the Func Out voltage appears across R111 (110K) and 1/10 appears across both R113 (12K) and the comparator inputs. For 0 ohms output impedance, K4 stays closed for all output voltages.

If the output of the voltage divider exceeds +3V, the output of U24D will swing negative and trip output protection. Likewise, if the voltage comparator output drops below -3V, the output of U24C will swing negative and trip output protection. Tripping output protection opens the output relay and disconnects any external source of high voltage. Diodes CR8 and CR9 limit the output swing of the voltage comparator to protect U24C and U24D.

Component/Signal Descriptions. The following paragraphs discuss the operation of U24 and the OE/, IOST6/, IOBS/, and MSTRST/ signals.

U24A. Operational amplifier U24A acts as a flip-flop that remembers the status of output protection. Capacitor C68 lets U24C or U24D develop a negative-going pulse at pin 4 of U24A. Because this pulse exceeds -2.2V (the voltage at pin 5 that holds U24A in the untripped state), U24A's output swings positive and U24A switches to the tripped state.

Output OE/. Output OE/ opens output relay K1 when the output protection circuit trips. OE/ controls the output enable line of U13, the relay drive buffer. With no overload, OE/ stays low and lets the main microprocessor control the relays through U13. An overload switches OE/ high, disables the relay drive buffer, and opens all the relays, including K1, the output relay.

Output IOST6/. Status line IOST6/ tells the main microprocessor the status of the output protection circuit. High indicates untripped; low indicates tripped. Each the DAC/output board has an IOST6/ line; they all connect together and feed back to the main microprocessor board as a single line.

Input IOBS/. Board select line IOBS/ lets the main microprocessor board reset the output protection circuit. Pulling IOBS/ low pulls U24A-pin 5 from +2.2V (tripped level) down to about 0.7V. Because U24A-pin 4 stays at 0.9V (except during trip pulses), pulling U24A-pin 5 down to 0.7V makes U24A's output swing negative and switches U24A to the untripped state.

Input MSTRST/. Master reset line MSTRST/ lets the main microprocessor board reset the output protection circuit. The main microprocessor board generates a master reset on power-up and also when you press the [Reset] PARAMS key.

2.7.12 Cal Mux Channel Select

Function. Lets the main microprocessor board connect any of eight internal DAC/output board signals to the ref/cal board for calibration and self testing.

Operation. Using the GPIO address bus, the main microprocessor board makes address decoder U10 latch the data on GPIO data bus lines IODT0-3 into U17's D-type flip-flops. Output lines Q1-2 of U17 connect to the address inputs of multiplexer U15. The latched data on these address lines selects one of the eight multiplexer inputs for connection to the ref/cal board.

Latched output bit Q5 of U17 (input IODT3) controls relay K4 in the output protection circuit. K4 turns the output protection circuit on and off. The next section tells why U13, the relay drive buffer, cannot control relay U4.

2.7.13 Relay Drive Buffer

Function. Lets the main microprocessor board operate relays K1-K3 and K5-K7 on the DAC/output board.

Operation. Using the GPIO address bus, the main microprocessor board makes address decoder U10 latch the data on GPIO data bus lines IODT1-3 and 5-7 into U13's D-type flip-flops. A low at any latched (Q) output of U13 turns the relay connected to that output on. A low at the OE terminal (pin 1) enables U13 and lets it control the relays, while a high forces all the outputs to a high impedance state.

Effect of an Output Overload. When the output protection circuit detects an overload, it steps the OE/ signal high. Stepping OE/ high forces U13's outputs to their high impedance state, which opens all the relays, including K1. Opening relay K1 disconnects the output amplifier from the Func Out connector.

Relay K4. U13 does not control relay K4 (part of the output protection circuit). Instead, U13 in the cal mux channel select circuit controls K4.

2.8 REFERENCE/CALIBRATION BOARD (1615)

(Refer to figure 2-0.)

2.9 SWITCHING POWER SUPPLIES (1627, 1628)

The 650 contains the following switching power supplies:

BOARD NAME	SUPPLY NAME	OUTPUT NAME	OUTPUT CURRENT	VOLTAGE LIMITS (VDC)
ANALOG POWER SUPPLY BOARD (1627)	±38VDC	+38VDC	3A	+36.8 to +39.2
		-38VDC	3A	-36.8 to -39.2
	±15VDC	+15VDC	2A	+14.5 to +15.5
		-15VDC	2A	-14.5 to -15.5
DIGITAL POWER SUPPLY BOARD (1628)	±5VDC	+5VDC	10A	+4.9 to +5.1
		-5VDC	2A	-4.9 to -5.1
	ISO+5VDC	+5VDC	1A	+4.9 to +5.1

2.9.1 Functional Circuit Description

Because the ±38VDC, ±15VDC, ±5VDC, and ISO+5VDC switching power supplies all work basically the same, this section describes only the ±38VDC supply. Figure 2-0 redraws the ±38VDC schematic to make the major functions easier to see. The following text keys its circuit descriptions to the numbered functions on the schematic.

Function. Supplies ±38VDC power to the output amplifiers of each channel.

Basic Circuit. Components U1, Q1, L1, C11, and CR6 form the basic switching power supply circuit. U1 generates a 30kHz square wave that drives the gate of FET transistor Q1. Q1 switches ≃60 volts from the input filter capacitors through to inductor L1. L1 absorbs most of the applied voltage to limit the charging current flow to output filter capacitor C11. When Q1 removes the input voltage, L1 discharges through CR6. C11 discharges continuously through the external load. U1 controls the output voltage by adjusting the width (Q1 on-time) of the applied voltage pulses.

(1) SWITCHING FREQUENCY CONTROLLER

R4 and C6 determine the oscillator frequency for both U1 and U2. The resulting 30kHz sawtooth waveform appears across C6.

(2) POWER SWITCHER

R1 biases Q1 off (+). U1 turns Q1 on by pulling its gate less positive through R1, R2, and CR5. Zener diode CR5 shifts the bias voltage down to protect U1's switching transistor. Zener diode CR23 protects field-effect transistor Q1 by limiting its gate-source voltage to 15 volts.

(3) VCC POWER

C5 provides VCC power to U1 and U2. During power-up, the input filter capacitors charge C5 through R3. After power-up, diode CR8 charges C5. C7 decouples high frequency and EMI at U1.

(4) DEAD-TIME CONTROLLER

C8 and R64 prevent power-up current surges. At the first application of power, C8 acts as a direct short because it contains no charge. Therefore, the entire +5V reference voltage initially appears at the DTC pin and makes U1 restrict the charging pulse to its minimum width. As C8 charges through R64, the voltage at DTC drops to 0V and allows the charging pulse to expand to its operating width.

(5) CURRENT LIMITER

Normal Operation. A voltage directly proportional to the output current appears across R10. Because the output voltage sensor holds R10's output (R11) side fixed at 38V, voltage variations due to current changes appear entirely on R10's input (CR22) side. R11 and R12 provide the reference voltage for the - input of error amplifier 2, while R10, CR22, R8, and R9 provide the current dependent voltage for the + input. Only output currents in excess of 3 amps can generate enough voltage across R10 to overcome the fixed 0.6V forward drop across diode CR22. Overcoming CR22's drop pulls the 2+ input below the 2- reference and makes U1 reduce the width of the charging pulse.

Operation During Power-Up. During power-up, reverse current flow from ground through R9, R8, and R70 to the -38V input filter capacitors disables current limiting by holding the B+ input low. As the +38V line rises toward 38 volts, the increasing forward current from the +38V line through CR22, R8, and R9 eventually swamps out the reverse flow and enables current limiting.

(6) OVER-VOLTAGE PROTECTOR

Components R13, CR9, and R15 connect from +38V to -38V and monitor both outputs of the supply. If the total output voltage (76 volts) rises above 82 volts, zener diode CR9 will conduct, current will flow through R15, and the resulting voltage will turn on Q2. Silicon-controlled rectifier Q2 will then remain on and hold +38V and VCC shorted to ground through CR8, R14, and CR10.

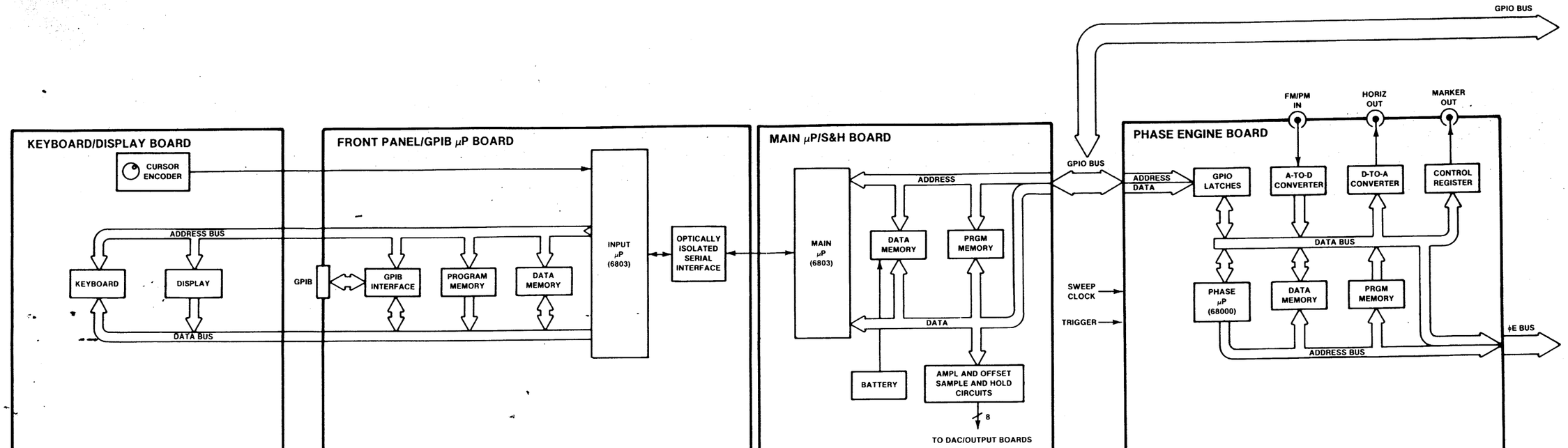
(7) OUTPUT VOLTAGE SENSOR

Error amplifier 1 of U1 monitors the output voltage. R6 provides the reference voltage, while R16 and R17 divide the output voltage down to the range of the reference voltage. Feedback components C9 and R5 make the voltage monitoring amplifier insensitive to 60Hz voltage variations.

THIS
PAGE
LEFT
BLANK

SCANS
By
Artek Media

Figure 2-0



GIVES CONTROL OF THE 650 TO THE OPERATOR.

Keyboard. Allows operator to:
- Step through menu trees
- Choose operating modes
- Enter parameter values
- Control cursor position

Display. Provides operator with this status and control information:
- Menus
- Operating modes
- Parameters
- Error messages
- Cursor position
- Parameter monitors
- Listen buffer
- SRQ buffer
- GPIB address

Cursor Encoder. Allows operator to continuously vary numerical values.

INTERFACES BOTH OPERATOR INPUT AND GPIB INPUT TO THE 650.

GPIB Interface. Electrically interfaces the GPIB bus to the Input μP.

Input μP. Performs the input interfacing function.
Operator interfacing:
- Operates menu trees.
- Checks keyboard-entered parameters/modes against limits.
- Displays error messages for non-legal commands.

GPIB bus interfacing:
- Strips parameters/modes from GPIB command strings.
- Checks GPIB-entered parameters/modes against limits.
- Loads listen and SRQ buffers.

Loads legal parameters/modes into pending commands register.
Executes (sends to Main μP) pending commands.
Transmits cursor knob/arrow changes to Main μP board.

Data (RAM) Memory. Stores this material:
- Pending parameters/modes until operator/GPIB requests execution.
- Listen buffer (all commands received from GPIB bus).
- SRQ buffer (defective commands from GPIB bus).
- Display viewing angle and backlight setting.

Program (ROM) Memory. Stores the front-panel operating system:
- Menus and menu trees
- Numeric parameter limits
- Operating mode restrictions
- List of GPIB commands for operator reference
- Error messages

Serial Interface. Optically isolates the front panel and the GPIB bus from the waveform generation boards.

SERVES AS A CENTRAL SYSTEM CONTROLLER.

Main μP. Performs these functions:
- Sets up the instrument for manual calibration.
- Develops auto-cal correction factors.
- Develops quick-cal correction factors.
- Develops master-slave correction factors.
- Sends frequency-dependent correction factors to the phase engine board.
- Receives modes and raw parameters from Input μP.
- Adds correction factors to parameters to compensate for amplitude, offset, and duty cycle errors.
- Distributes corrected parameters to other boards.
- Runs the complete self-test procedure.
- Runs individual troubleshooting routines.
- Sends hardware status messages to Input μP.

Data (RAM) Memory. Stores this battery-protected material:
- "Stored Settings" instrument setups
- Quick-calibration correction factors
- Auto-cal correction factors for:
  - Amplitude errors
  - Offset errors
  - Square wave duty cycle errors
  - Frequency-dependent gain errors
  - Frequency-dependent phase errors

Program (ROM) Memory. Stores the chassis operating system:
- Parameter/mode handling and distribution program
- Manual calibration instrument setups
- Auto-calibration program
- Quick-calibration program
- Self-test/troubleshooting routines
- Self-test limits

Amplitude/Offset Sample/Hold Circuit. Generates amplitude and offset control voltages for DAC/Output boards.

DIGITALLY GENERATES ALL FREQUENCY AND PHASE SWEEPS.

Phase μP. Performs these functions:
- Accepts sweep instructions/parameters from Main μP.
- Loads frequency control registers on ΦACC board.
- Loads burst count register on ΦACC board.
- Loads phase offset registers on RAM boards.
- Loads waveforms in RAMs on RAM boards.
- Processes front panel Hold/Resume sweep commands.
- Compensates for frequency-dependent gain/phase errors.
- Processes **FM/PM In** signals.
- Generates **Horiz Out** signal.
- Generates **Marker Out** signal.
- Controls operation of ΦACC and RAM boards.
- Self-tests phase engine board.

Data (RAM) Memory. Stores this material:
- Sweep parameters
- Copy of all data sent to other boards
- Currently active sweep loop routine
- Auto-cal correction factors for frequency-dependent gain/phase errors (received from Main μP board)
- Operator-entered frequency sequence data
- Operator-entered phase sequence data

Program (ROM) Memory. Stores the entire phase engine operating program:
- Data handling routines
- Input/output signal processing routines
- 63 sweep loop routines
- Self-test routines
- Error compensation routines

Figure 2-0, Part 1
650 System Block Diagram

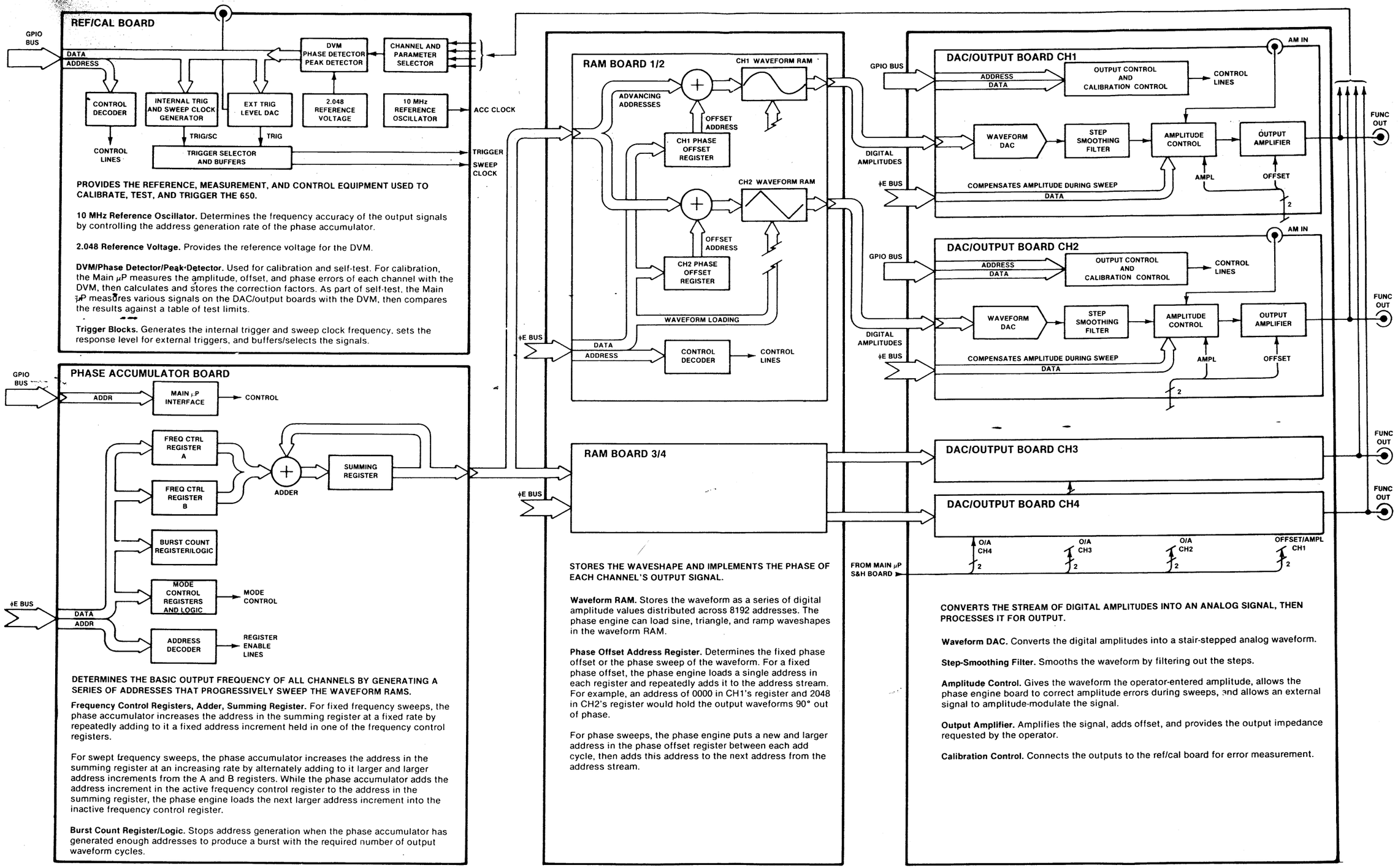


Figure 2-0, Part 2
650 System Block Diagram

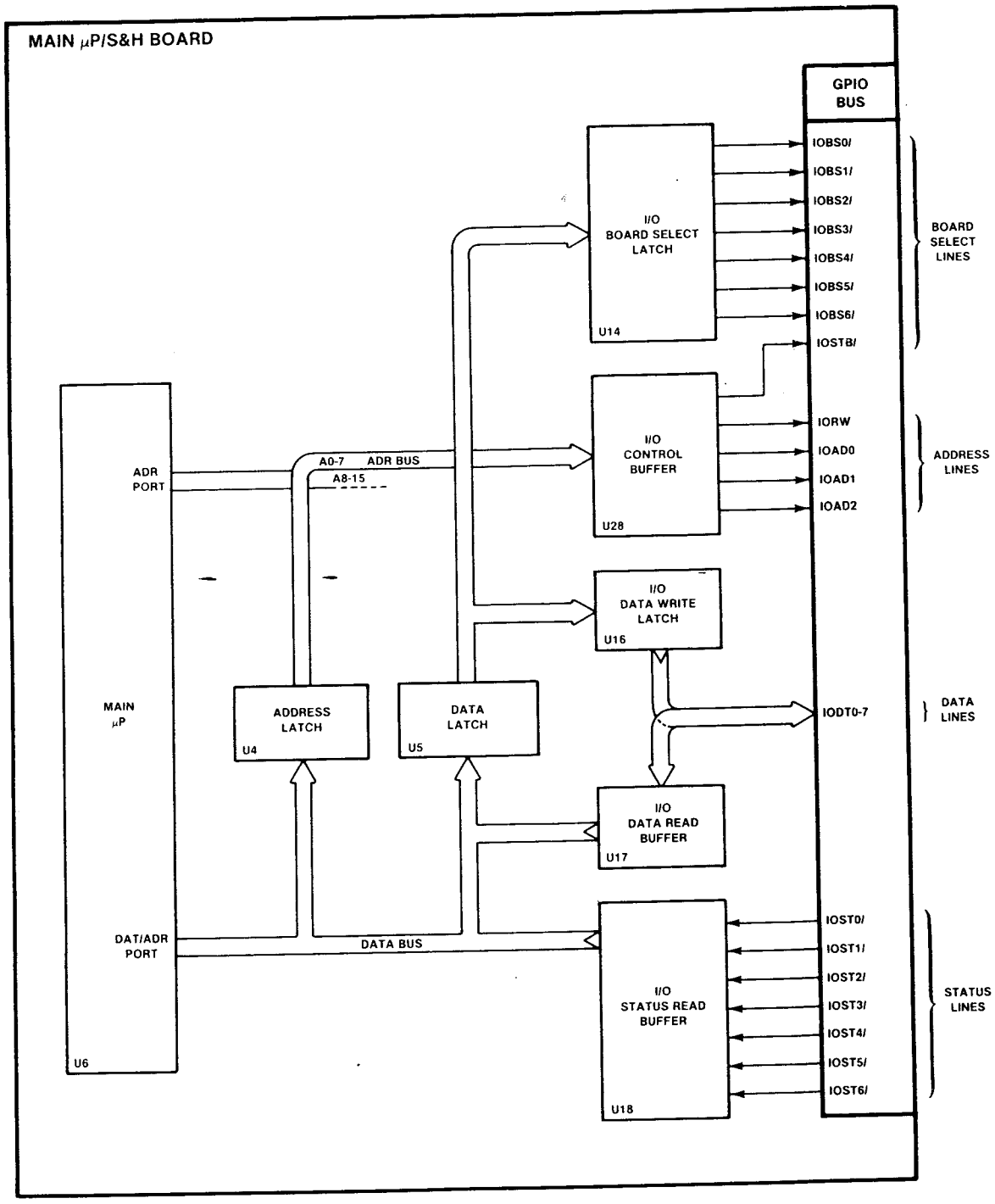
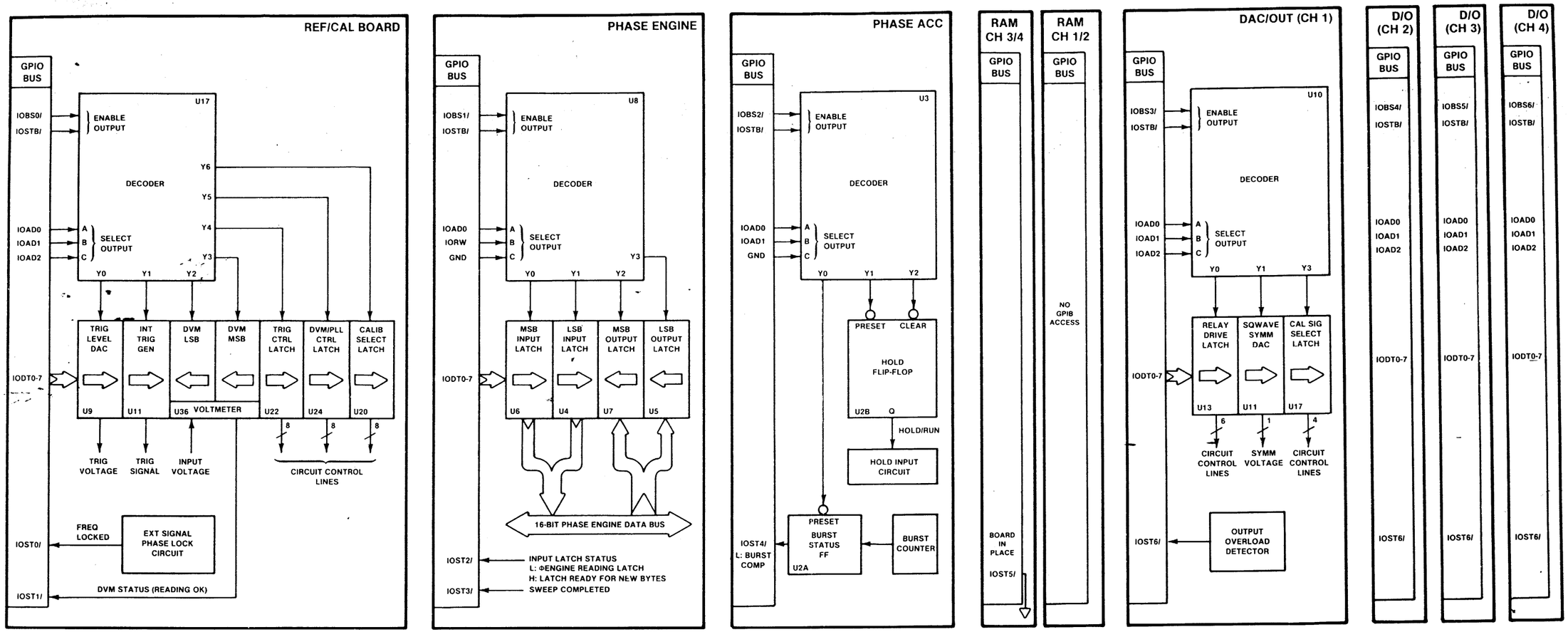


Figure 2-0, Part 1
GPIO Bus Block Diagram



LINE NAME	FUNCTION
IOBS#/	Input/Output Board Select Lines
IOSTB/	Input/Output Strobe Line
IORW	Input/Output Read/Write Line
IOAD#	Input/Output Address Lines
IODT#/	Input/Output Data Lines
IOST#/	Input/Output Status Lines
/	Identifies low-true signals.

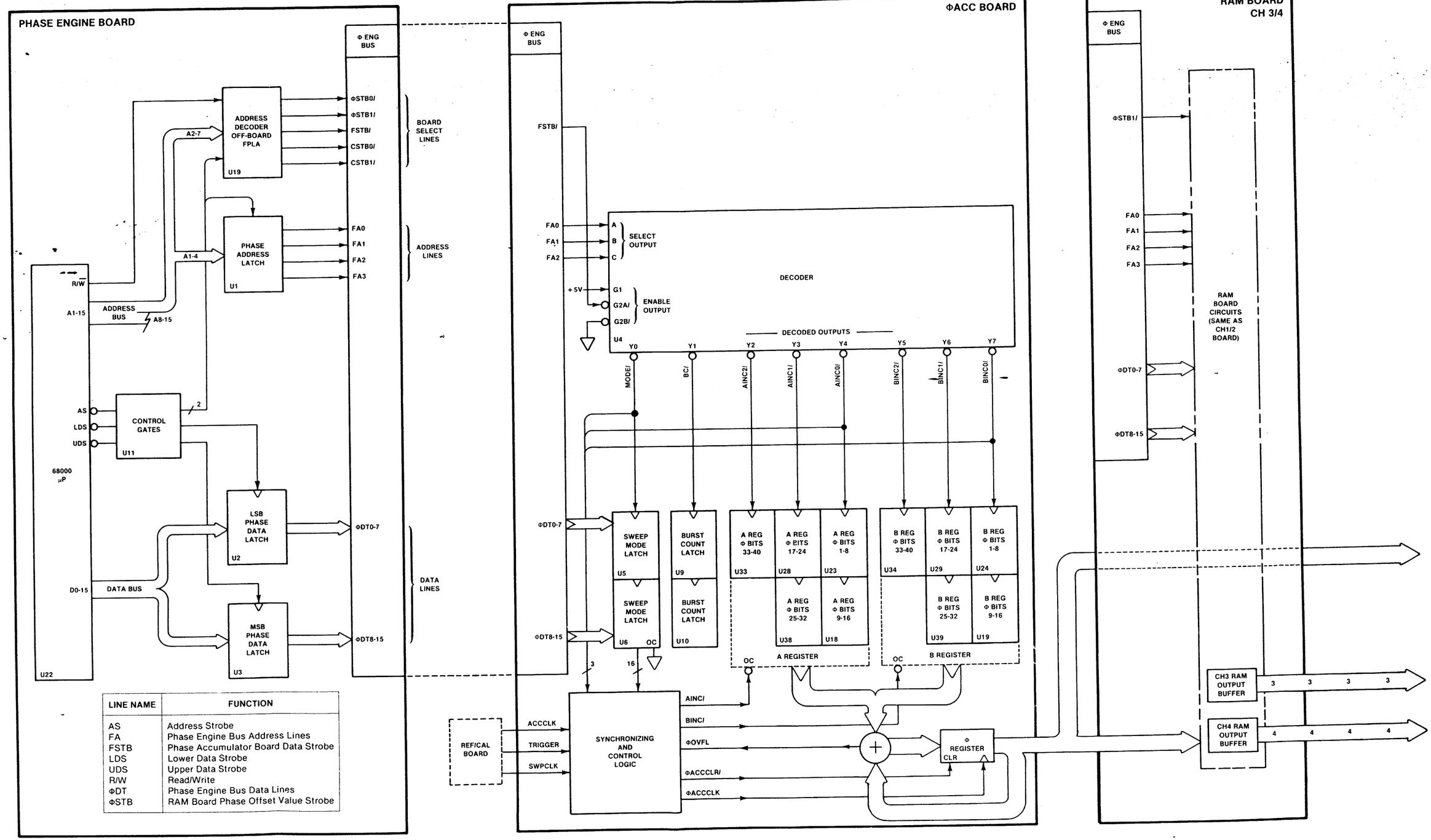
REF/CAL BOARD ADDRESS-DECODED FUNCTION LINES				
LINE	ACTION	CONTENTS OF BYTE	FROM	TO
Y0	Reads	Ext trigger trip level	IODT bus	Trigger level DAC
Y1	Reads	Start/stop command	IODT bus	Internal trigger generator
Y2	Writes	LSB of DVM reading	DVM	IODT bus
Y3	Writes	MSB of DVM reading	DVM	IODT bus
Y4	Reads	Trigger control bits	IODT bus	Control signal latch
Y5	Reads	DVM/PLL control bits	IODT bus	DVM latch
Y6	Reads	Relay control bits	IODT bus	Calibrate select latch

PHASE ENGINE BOARD ADDRESS-DECODED FUNCTION LINES				
LINE	ACTION	CONTENTS OF BYTE	FROM	TO
Y0	Reads	Commands/Data	IODT bus	MSB in latch
Y1	Reads	Commands/Data	IODT bus	LSB in latch
Y2	Writes	Commands/Data	MSB out latch	IODT bus
Y3	Writes	Commands/Data	LSB out latch	IODT bus

PHASE ACCUMULATOR BOARD ADDRESS-DECODED FUNCTION LINES	
LINE	FUNCTION
Y0	Sets status line IOST4/ (Q of flip-flop U2A) high (burst not complete).
Y1	Sets HOLD flip-flop (U2B) to "resume sweep" state.
Y2	Sets HOLD flip-flop (U2B) to "hold sweep" state.

DAC/OUTPUT BOARD ADDRESS-DECODED FUNCTION LINES				
LINE	ACTION	CONTENTS OF BYTE	FROM	TO
Y0	Reads	Relay control bits	IODT bus	Relay drive latch
Y1	Reads	Symmetry level	IODT bus	Square wave symmetry DAC
Y3	Reads	Signal select bits	IODT bus	Calibrate signal select latch

Figure 2-0, Part 2
GPIO Bus Block Diagram



LINE NAME	FUNCTION
AS	Address Strobe
FA	Phase Engine Bus Address Lines
FSTB	Phase Accumulator Board Data Strobe
LDS	Lower Data Strobe
UDS	Upper Data Strobe
R/W	Read/Write
ΦDT	Phase Engine Bus Data Lines
ΦSTB	RAM Board Phase Offset Value Strobe

Figure 2-0, Part 1
Phase Engine Bus Block Diagram

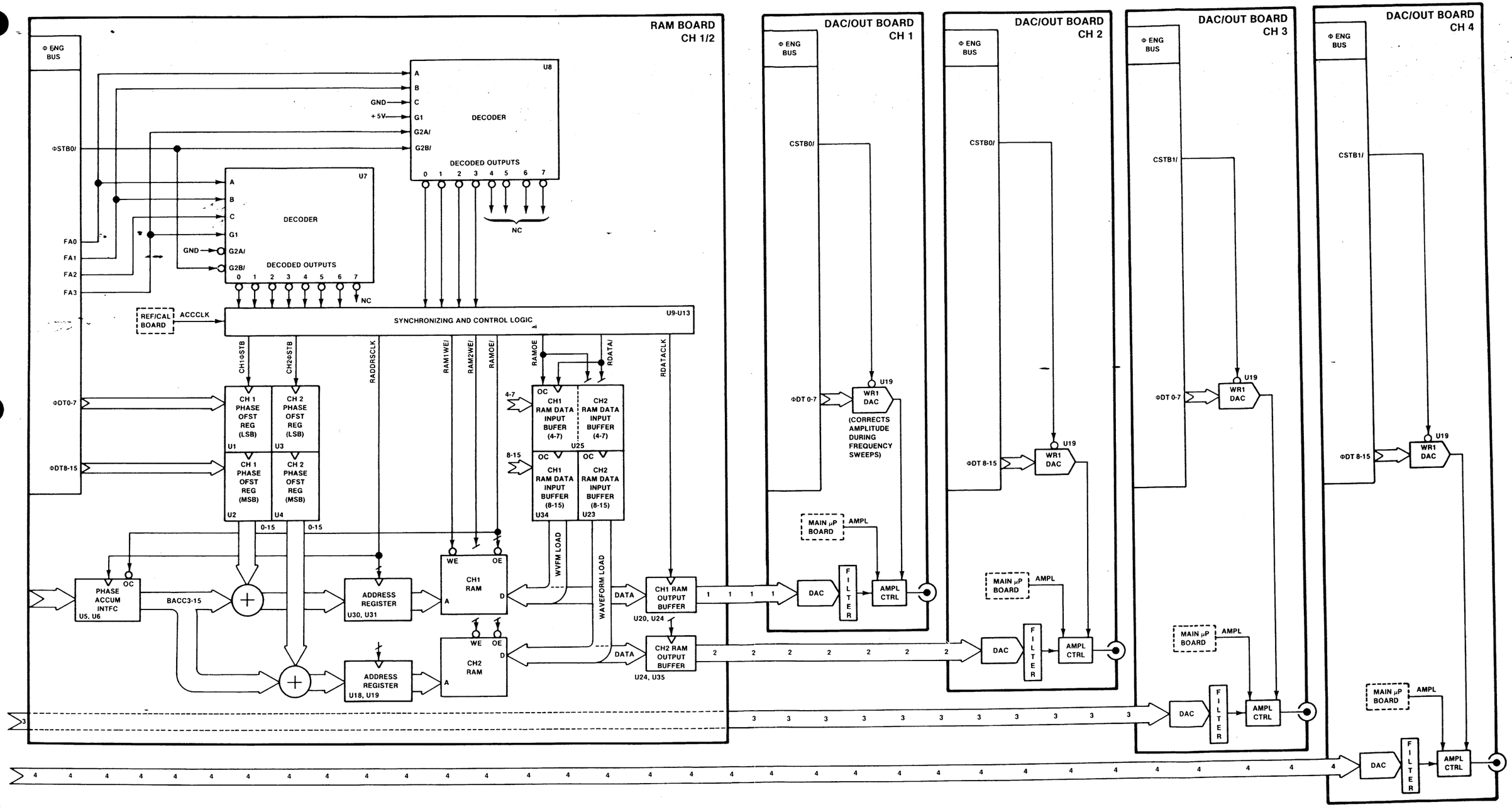


Figure 2-0, Part 2
Phase Engine Bus Block Diagram

BLANK

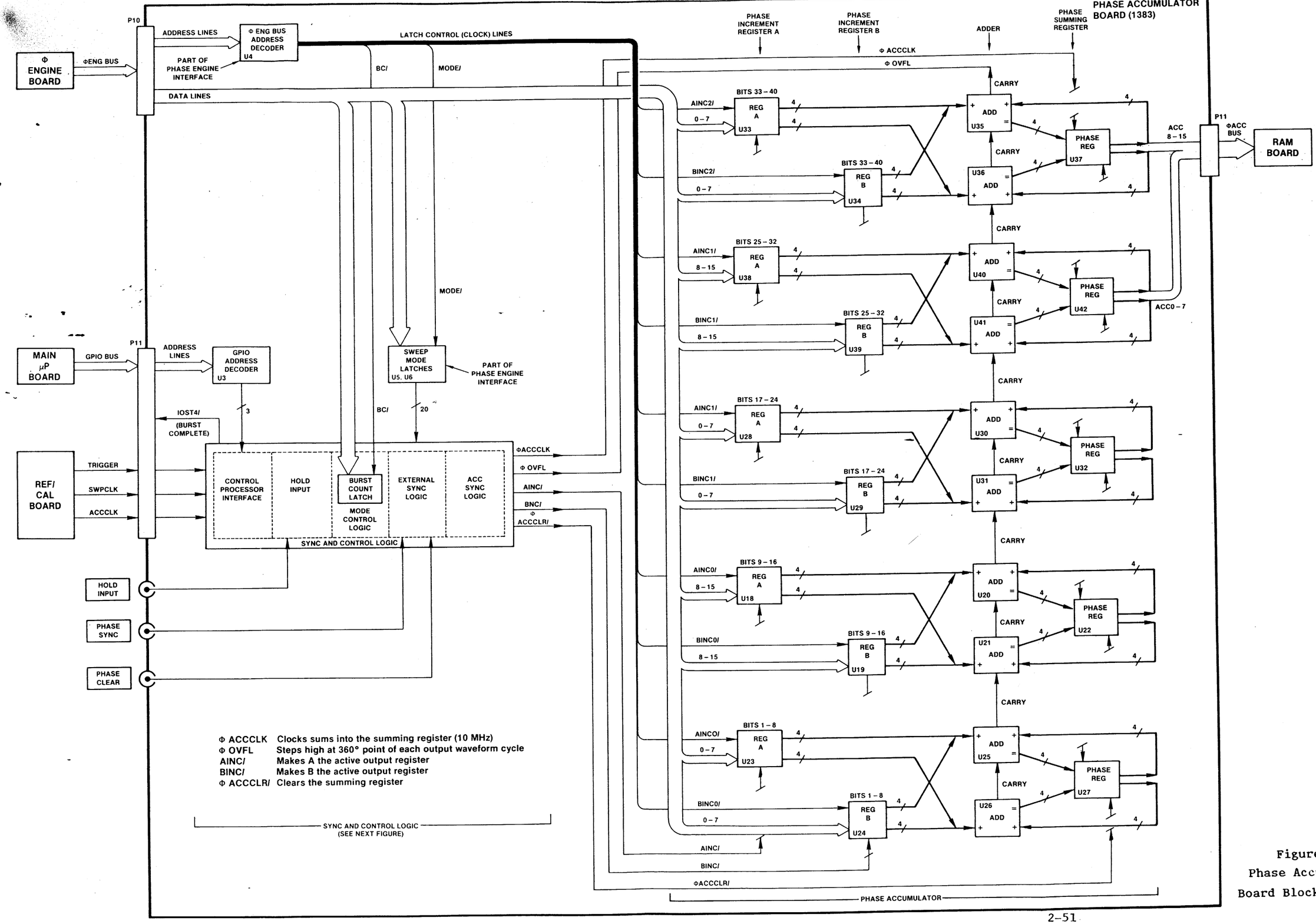


Figure 2-0
Phase Accumulator
Board Block Diagram

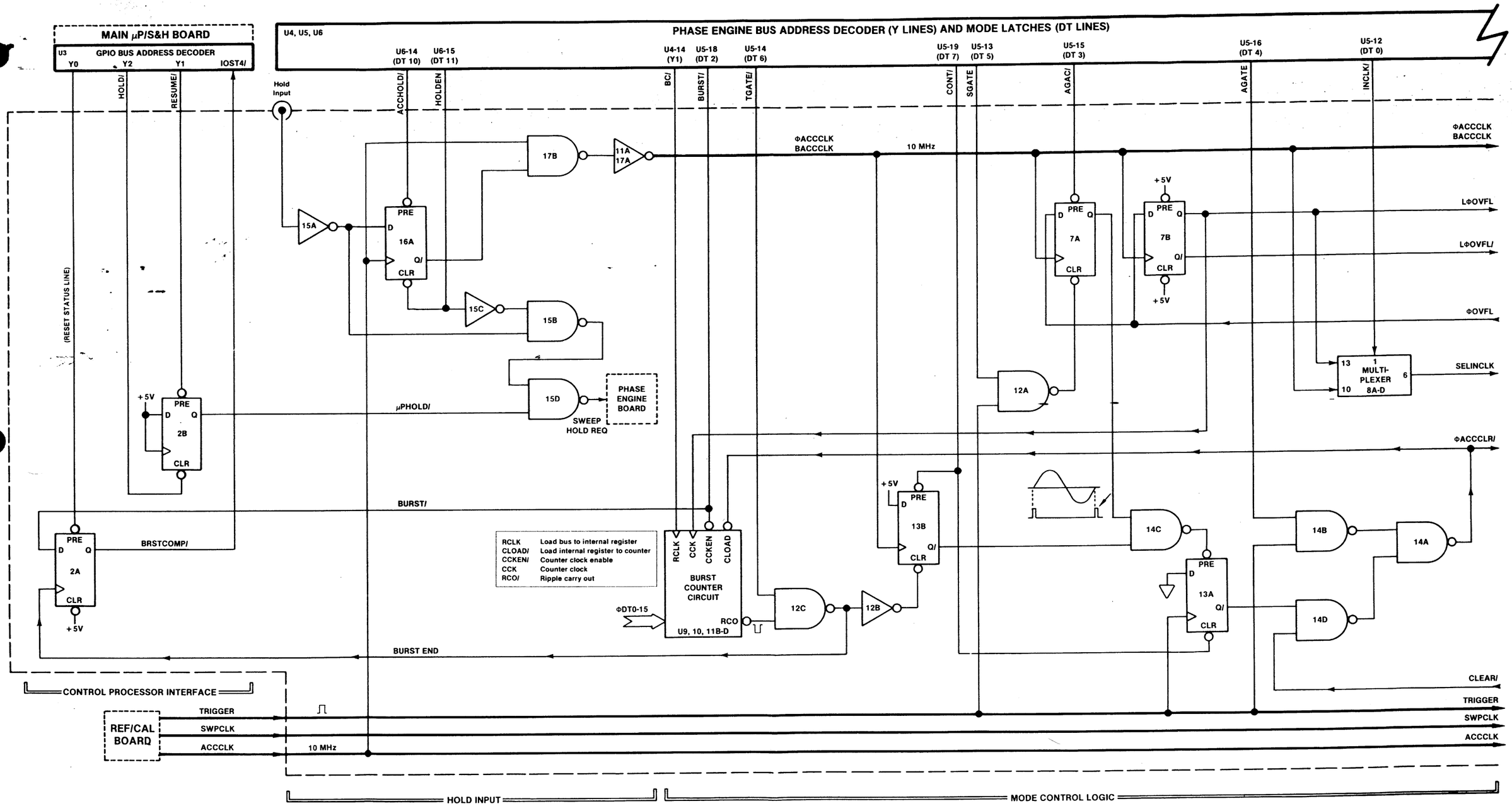
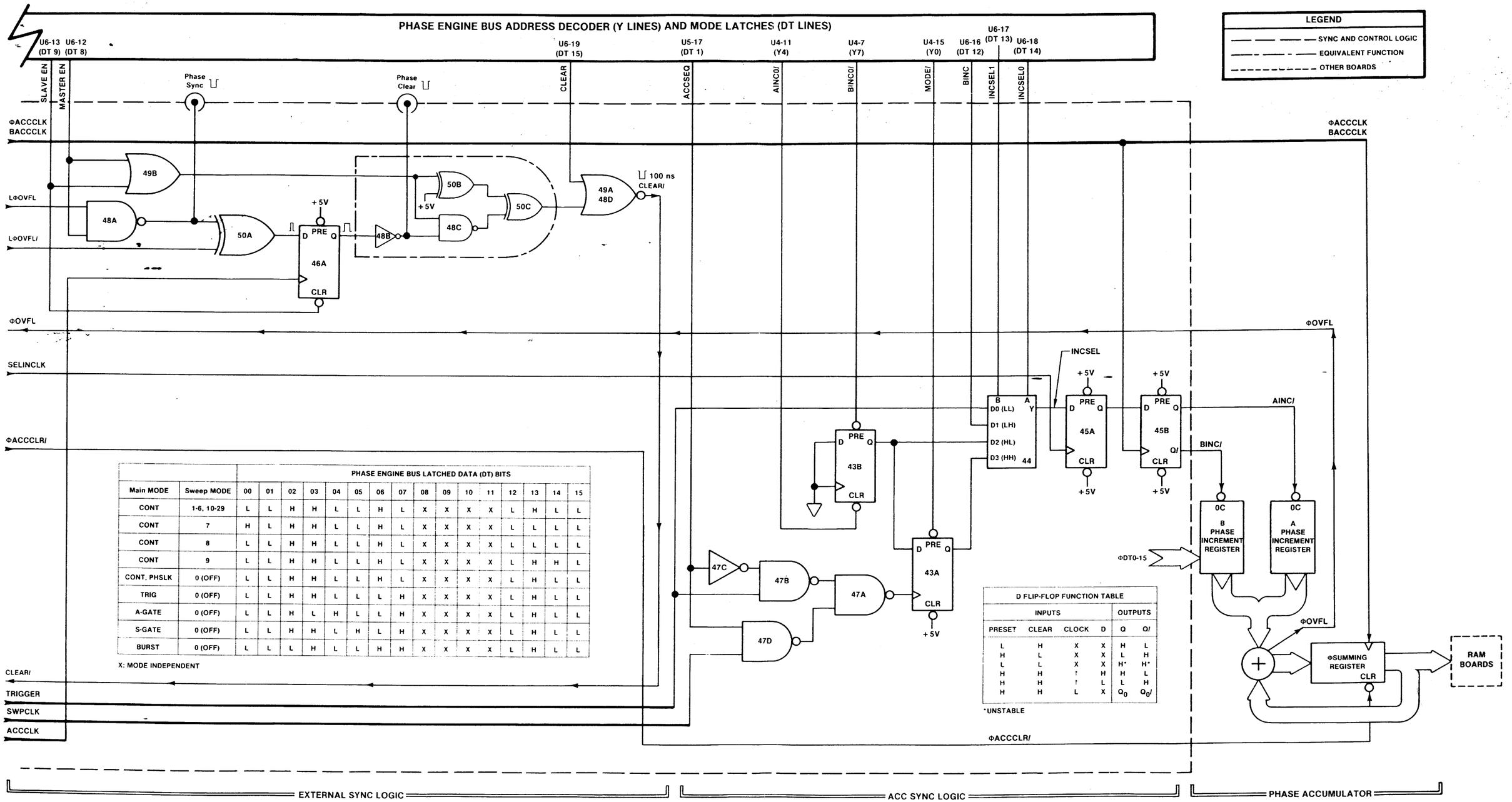


Figure 2-0, Part 1
Phase Accumulator Board
Sync and Control Logic



		PHASE ENGINE BUS LATCHED DATA (DT) BITS															
Main MODE	Sweep MODE	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15
CONT	1-6, 10-29	L	L	H	H	L	L	H	L	X	X	X	X	L	H	L	L
CONT	7	H	L	H	H	L	L	H	L	X	X	X	X	L	L	L	L
CONT	8	L	L	H	H	L	L	H	L	X	X	X	X	L	L	L	L
CONT	9	L	L	H	H	L	L	H	L	X	X	X	X	L	H	H	L
CONT, PHSLK	0 (OFF)	L	L	H	H	L	L	H	L	X	X	X	X	L	H	L	L
TRIG	0 (OFF)	L	L	H	H	L	L	L	H	X	X	X	X	L	H	L	L
A-GATE	0 (OFF)	L	L	H	L	H	L	L	H	X	X	X	X	L	H	L	L
S-GATE	0 (OFF)	L	L	H	H	L	H	L	H	X	X	X	X	L	H	L	L
BURST	0 (OFF)	L	L	L	H	L	L	H	H	X	X	X	X	L	H	L	L

X: MODE INDEPENDENT

D FLIP-FLOP FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	Q/
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	Q_0/

*UNSTABLE

Figure 2-0, Part 2
Phase Accumulator Board
Sync and Control Logic

REF/CAL BOARD
ACCCLK
P16
P17
ACCCLK
U9A
RADDRSCLK
U9B
RDATACLK
DATAON/
DATEN
PRE
D
Q
U11A
Q/
CLR
ΦENG ADDRESS BUS
ADDRESS DECODER
Y0
Y1
Y3
Y2
U8
FA0-3
ΦSTB0
DATAOFF/
RAMOFF/
RAMON/
PRE
U11B
RAMOE/
RAMOE
RDATA/
RDATA/
Y6
Y4
Y5
Y3
RAM2WRITE/
RAMWRITE/
RAM1WRITE/
U10A
U10B
RAM2WE/
RAM1WE/
ADDRESS DECODER
U7
Y1
Y2
Y0
RAM2OFST/
RAMOFST/
RAM1OFST/
U9C
U10C
R2OFST
R1OFST
+5V
+5
U12B
U12A
U13B
U13A
CH2ΦSTB
CH1ΦSTB
CONTROL LOGIC
PHASE ENGINE BOARD
ΦENG DATA BUS
ΦDT0-7
ΦDT8-15
CH1 PHASE OFST REG (LSB)
CH2 PHASE OFST REG (LSB)
CH1 PHASE OFST REG (MSB)
CH2 PHASE OFST REG (MSB)
U1
U3
U2
U4
0-15
CH1ΦSTB
CH2ΦSTB
RADDRSCLK
RAM1WE/
RAM2WE/
RAMOE/
RAMOE
RDATA/
RDATACLK
4-7
8-15
CH1 RAM DATA INPUT BUFFER (4-7)
CH2 RAM DATA INPUT BUFFER (4-7)
U25
CH1 RAM DATA INPUT BUFFER (8-15)
CH2 RAM DATA INPUT BUFFER (8-15)
U34
U23
4-15
WAVEFORM LOAD
PHASE ACCUMULATOR BOARD
ΦACC BUS
PHASE ACCUM INTFC
U5, U6
OC
BACC3-15
U26-U29
U14-U17
ADDRESS REGISTER
U30, U31
U18, U19
CH1 RAMS
U32, U33
CH2 RAMS
U21, U20
WE
OE
A
D
DATA
CH1 RAM OUTPUT BUFFER
CH2 RAM OUTPUT BUFFER
U24, U35
U22, U24
DA0-11
DB0-11
1
2
P16
CH1 DAC/OUTPUT BOARD
CH2 DAC/OUTPUT BOARD

Figure 2-0
RAM Board Block Diagra

DAC/OUTPUT BOARD (1467)

P19

MSTRST/ — IOST6/

MAIN μP BOARD

GPIO BUS

ADDRESSES

U10 ADDRESS DECODER

Y0 Y3 Y1

DATA

RELAY DRIVE BUFFER U13 OE

CAL MUX CHANNEL SELECT U17

WRI SQWV SYM DAC U11, U14

SYMV

7 1 3

RELAY COILS (SEE TABLE)

P21

OFST

AMPL

Φ ENGINE BOARD

ΦE BUS

(DATA ONLY)

ΦDT0 – 7 (CH 1 AND 3)
ΦDT8 – 15 (CH 2 AND 4)

AMPLITUDE CONTROL U19, U21

+10VR

AM IN — AM

AMPLCTRL

±I LIMIT REFS

OUTPUT PROTECTION U24, Q7, Q8, K4

SINE

±10VR

RAM BOARD

DAC BUS

P19

DAΦ-11

TTL/ECL TRANS-LATOR U26, RN1, 2

DAC DATA LATCHES U1, U2

ACCCLK

WAVEFORM DAC U3

6-POLE FILTER U4, U5

SQUARE SHAPER U18, U20 Q2 – Q5

K6

XY MULTIPLIER U6 – U9

OUTPUT AMPLIFIER U25, Q13 – Q18

50Ω ATTENUATOR K3, K5

50Ω K2 0Ω 100K

K1

FUNC OUT

K7

CHXAC

P21

REF/CAL BOARD

ACCCLK +10VR −10VR

K8 (MATE OPTION)

JUMPER (NO MATE OPTION)

SYNC OUT

÷10

U15

FUNCTEST

FUNCTEST/10

OFSTTEST

MULTTEST

AMPLTEST

SYMVTEST

FILTEST

DACOUTTEST

CALIBRATION MUX

ADDRESS LINES

CHXDC

OFST 10K

MULTOUT 1K

AMPLCTRL 1K

SYMV 1K

FILTOUT 1K

DACOUT 1K

3 3 3

ARTEK MEDIA

Signature Not Verified

Digitally signed by ARTEK MEDIA
DN: cn=ARTEK MEDIA, o=DC Henderson, c=US
Date: 2005.01.25 09:43:16 -06'00'

RELAY FUNCTION TABLE

U17 PIN	U13 PIN	RELAY COIL	RELAY FUNCTION
—	14	K1	TURNS OUTPUT AT FUNC OUT BNC ON/OFF
—	15	K2	SELECTS 0Ω/50Ω OUTPUT IMPEDANCE
—	16	K3	TURNS – 20 dB ATTENUATION ON/OFF
18	—	K4	SELECTS MONITORING RANGE OF OUTPUT PROTECTION CIRCUIT
—	13	K5	TURNS – 40 dB ATTENUATION ON/OFF
—	17	K6	SELECTS SQUARE/SINE WAVE (U13 – 17 ALSO TURNS SQUARE SHAPER ON/OFF)
—	18	K7	TURNS OUTPUT AMPLIFIER SIGNAL FEED TO REF/CAL BOARD ON/OFF
—	19	K8	TURNS SYNC OUT ON/OFF (MATE OPTION ONLY)

Figure 2-0
DAC/Output Board Block Diagram

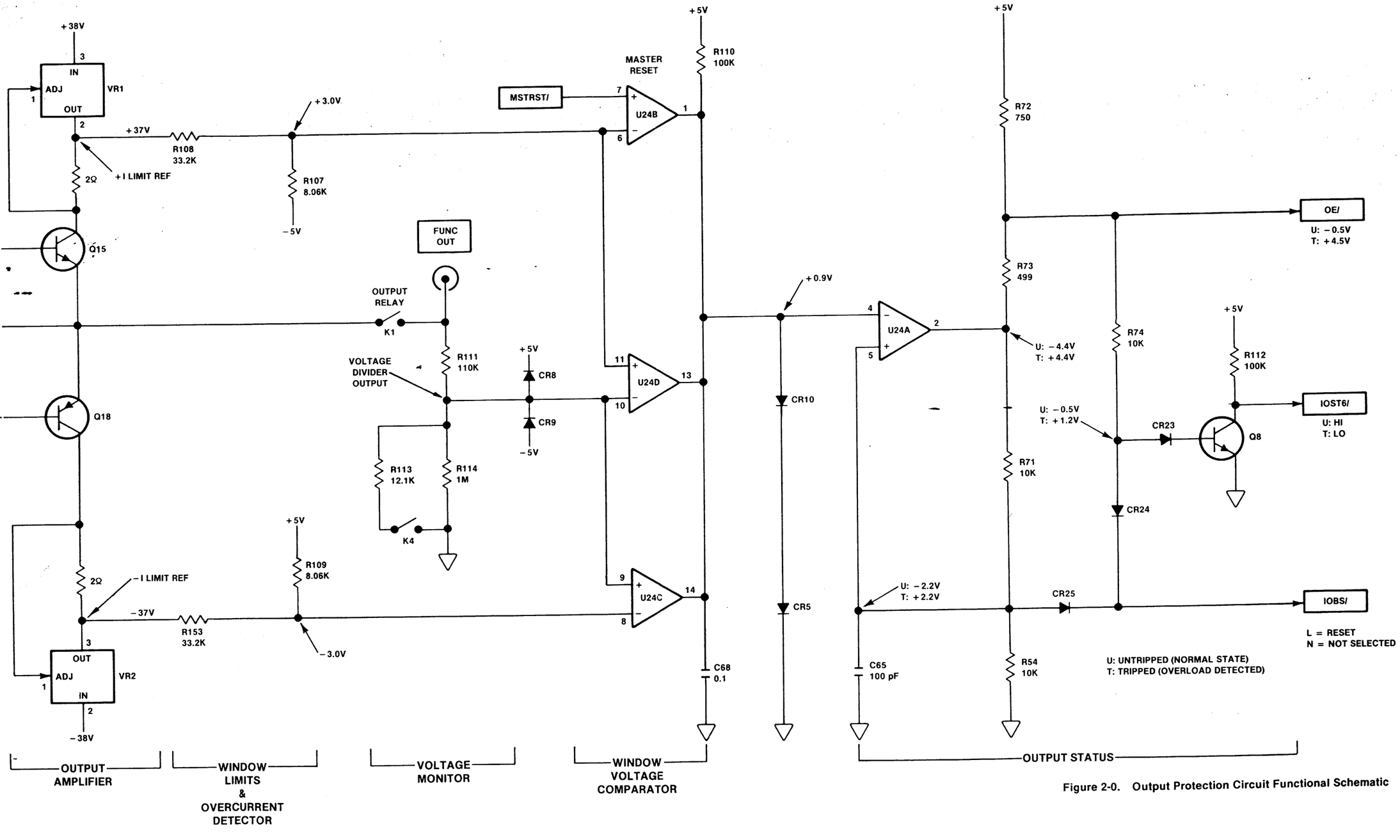


Figure 2-0. Output Protection Circuit Functional Schematic

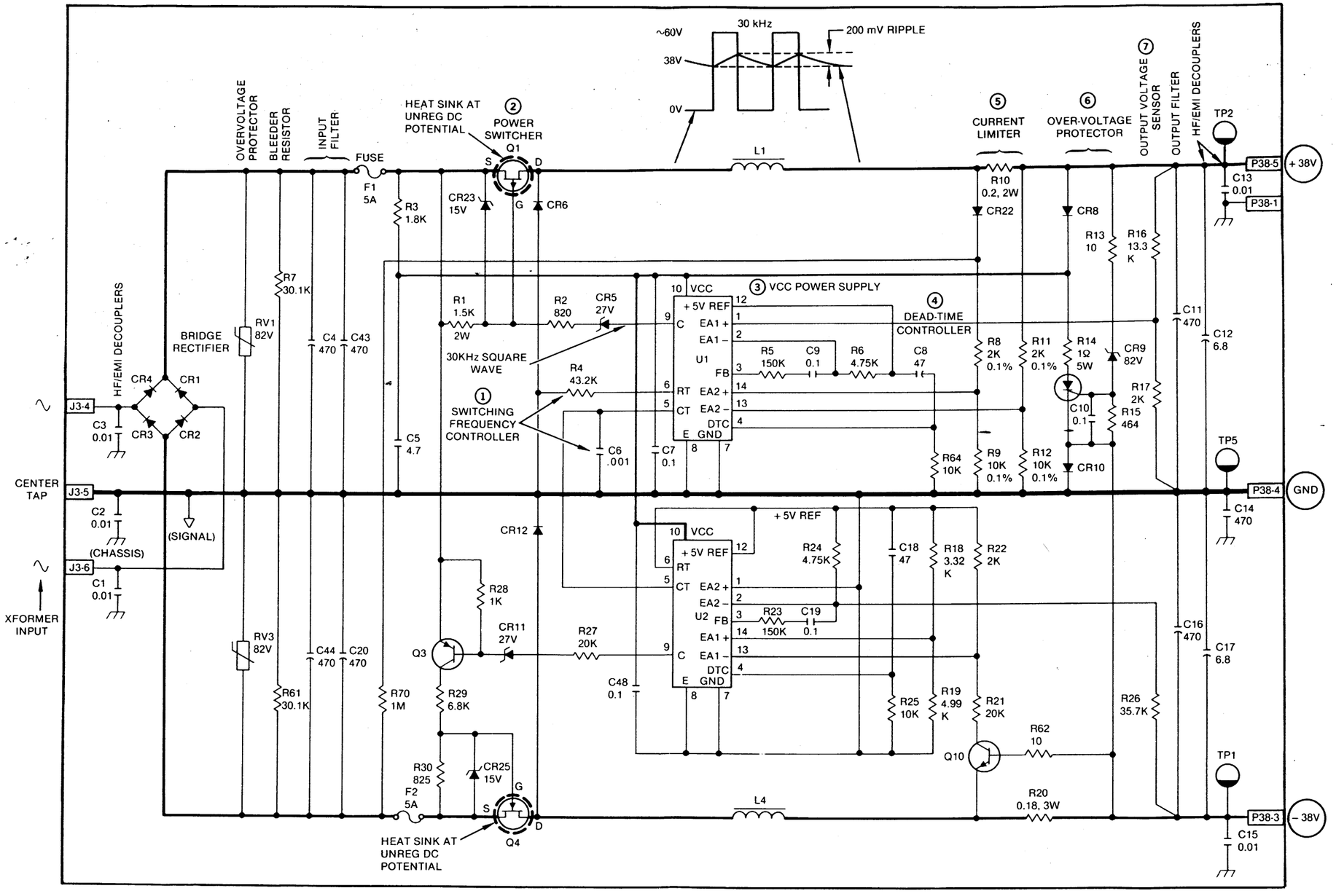


Figure 2-0
Switching Power Supply
Functional Schematic

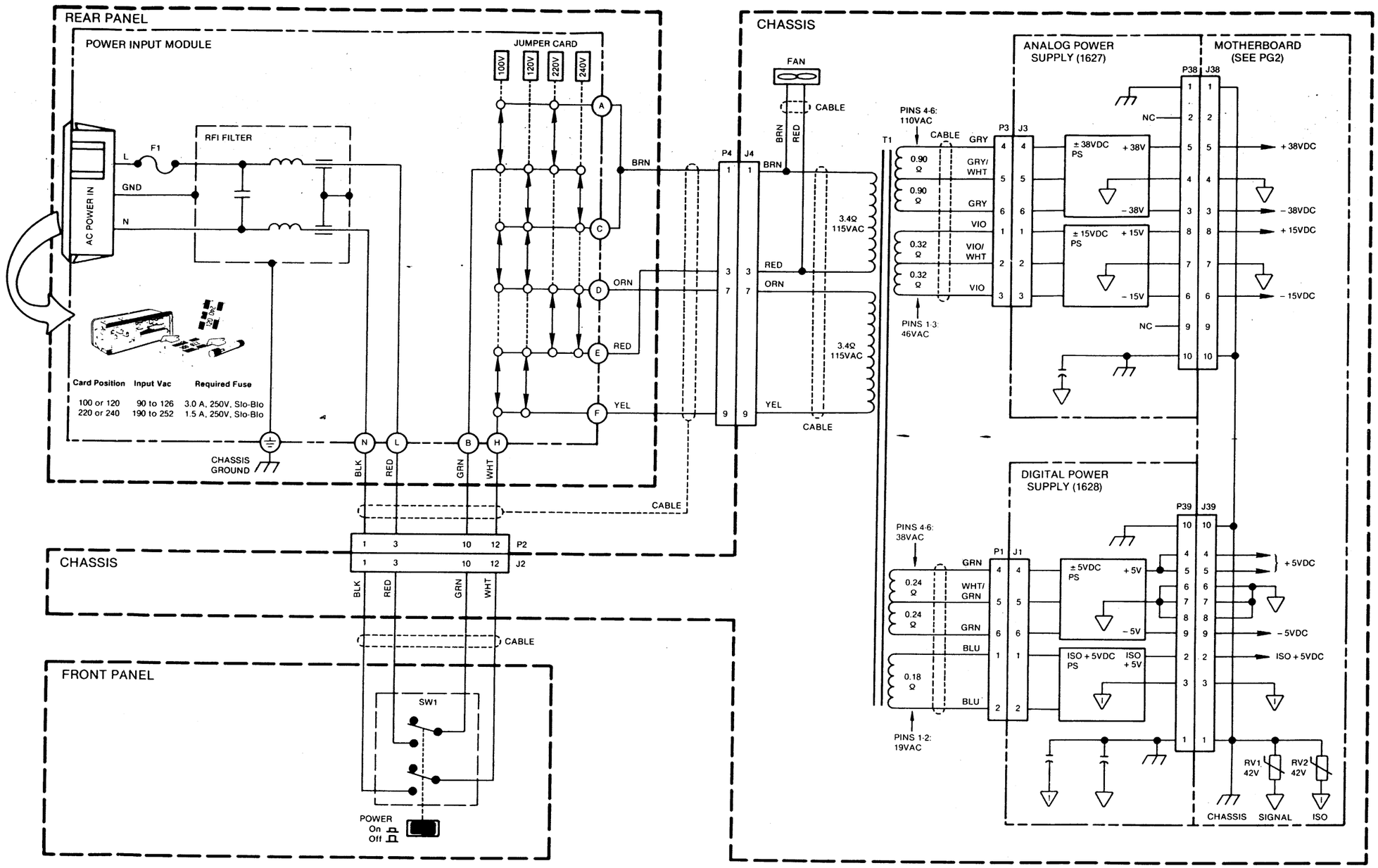


Figure 2-0, Part 1
Power Distribution Diagram

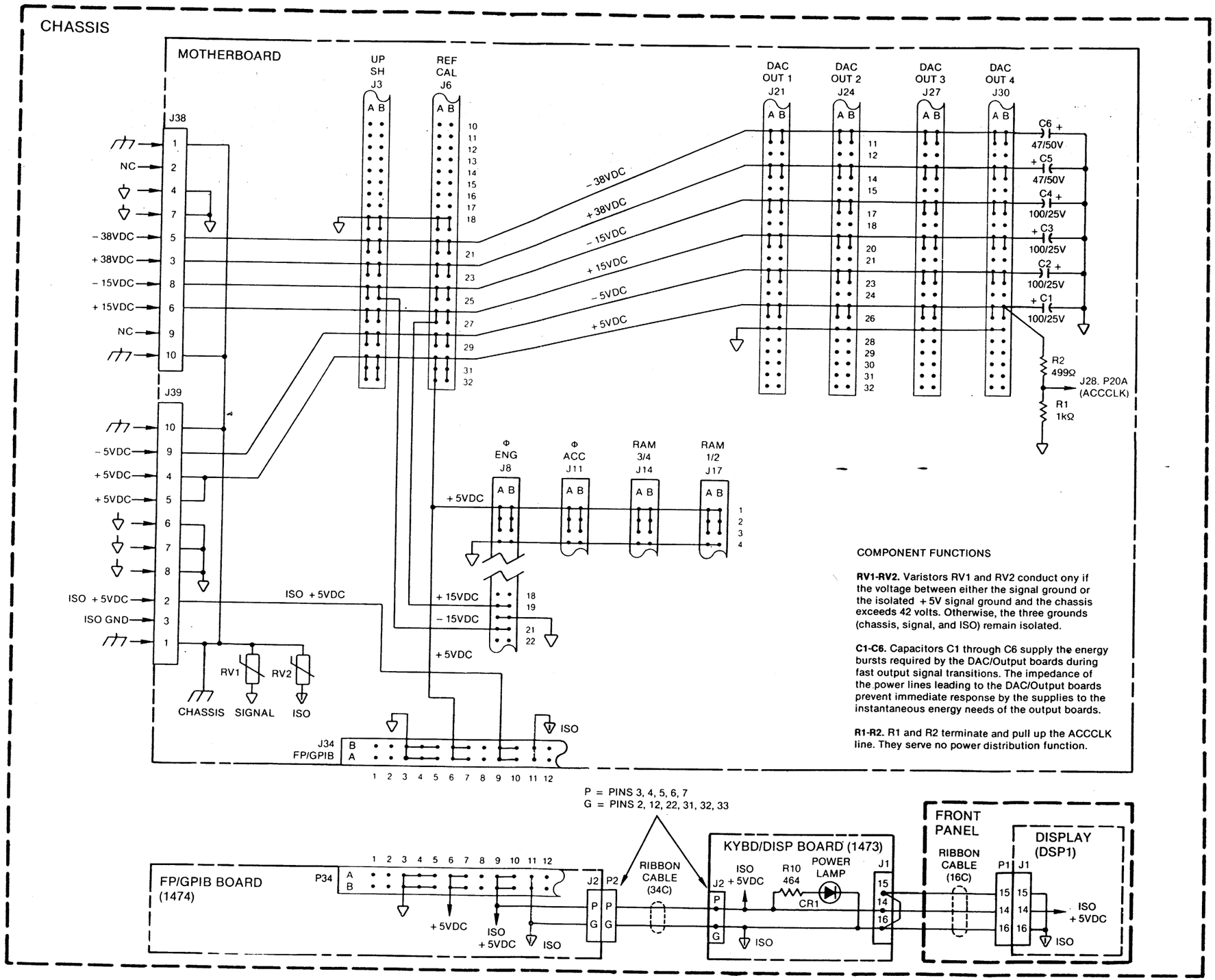


Figure 2-0, Part 2
Power Distribution Diagram

CHAPTER 3

PERFORMANCE VERIFICATION PROCEDURES

CHAPTER OVERVIEW

3.1 QUICK FUNCTIONAL CHECK

(See Section 2.7 in Operation Manual)

3.2 COMPLETE PERFORMANCE VERIFICATION

Does the 650 meet all the specifications? Use the tests and test equipment described in this section to find out.

Test Equipment Required. Table 3-0 lists the complete set of test equipment needed to fully verify 650 performance, while table 3-0 gives the specific instruments needed for each test.

Test Numbering. Complete performance verification consists of channel tests (repeated on each channel) and system tests (performed once per 650). Each test breaks down into parts numbered as follows:

Output Channel Tests TT.C.X.X	System Tests TT.X.X	Numbering Range
Test Number----------TT	Test Number--TT	TT = 4 through 40
Channel Under Test------C		C = 1, 2, 3, 4
Test Part----------X	Test Part--------X	X = As required
Subtest Part----------X	Subtest Part------X	X = As required

More Information. Section 3.4, factory performance verification, shows the results of the factory automated version of these tests.

TEST SUMMARY

Software Version Test. Reads the version number of the software.

Quick Functional Check. Verifies that each channel has the correct Func Out and Sync Out outputs at power on.

Quick Cal Check. Verifies proper calibration of the internal reference voltage source.

Reference Input/Output. Three functions: 1) Verifies the frequency accuracy of the internal reference clock. 2) Verifies that the 650 can detect a signal at 10MHz Ref In, turn off the internal REF clock, and operate from an external reference signal. 3) Verifies that the 10MHz Ref Out signal meets TTL level specifications.

Internal Voltage Reference. Measures the accuracy of the internal calibration voltage reference.

Output On/Off; 0/50 Ohm Impedance. Verifies correct operation of the output impedances and on/off controls of all channels.

Function Check at 600Hz, 10Vp-p. Verifies that each channel allows selection of the SINE, TRIANG, RAMP, SQUARE, and DC functions and that each function operates correctly.

Sine Amplitude and Offset Accuracy. Verifies that sine wave amplitude and offset meet specifications across the 0db range for all channels.

Sine Amplitude Accuracy at 50Vp-p. Verifies that each channel can deliver 0.5 ampere into a 50 ohm load and still maintain the maximum peak-to-peak output voltage.

Square Amplitude and Offset Accuracy. Verifies that the square wave amplitude and offset meet specifications across the 0db range for all channels.

DC Voltage Accuracy. Verifies DC voltage accuracy for each channel.

DC Current Load Test. Verifies that each channel can deliver 0.5 ampere into a 50 ohm load and still maintain the maximum DC output voltage.

Attenuator Accuracy. Verifies the accuracy of the output attenuator of each channel.

Phase Check. Verifies the phase accuracy and quick cal effectiveness for each channel.

Sine Frequency Response. Verifies that each channel's sine wave amplitude deviation remains within limits from 10Hz to 20kHz.

Sine Distortion. Verifies that each channel's sine wave meets purity specifications (limited second and third harmonics).

Spurious Level. Verifies that the worst-case spur of each channel falls below the specified limit.

Rise/Fall Time and Aberrations. Verifies that each channel's square wave rise/fall times and positive/negative aberrations meet specifications.

Square Wave Symmetry. Verifies the duty cycle set-ability and accuracy of each channel's square wave.

AM Input. Verifies that each channel's AM input operates and has the correct modulation drive levels.

Sync Out. Verifies that each channel's sync signal meets TTL level limits.

Main Generator Mode. Verifies that the main generator modes operate correctly at a phase setting of 0°.

Burst Count. Tests the set-ability and accuracy of the burst counter at the maximum trigger frequency.

External Phase Lock. Verifies that the 650 can phase lock to an external reference signal applied to Trig In.

Programmable Trigger Level. Verifies operation and accuracy of the trigger level DAC circuitry.

Internal Trigger. Verifies the frequency accuracy of the internal trigger synthesizer.

Marker Output Level. Three functions: 1) Verifies set-ability and accuracy of the marker frequency. 2) Verifies that the Marker Out levels meet TTL requirements. 3) Indirectly verifies proper operation of the phase marker.

Sweep Time. Verifies sweep time accuracy.

Sweep Modes. Verifies proper operation of the sweep modes associated with the Trig In, Marker Out, and Horiz Out connectors.

FM/PM Input. Verifies that an external dc voltange source can frequency modulate the 650.

Hold In. Verifies that a TTL signal applied to the Hold In connector can control frequency sweep and waveform output.

Stored Settings. Verifies that the 650 can store and recall setups and that the memory backup battery works.

Self Diagnostics. Verifies that self test can test the 650 circuits and that none have defects.

Table 3-0. Test Equipment Required for Complete Performance Verification

Equipment	Recommended
Analyzer, Spectrum	HP8568A
Counter, Universal	HP5334A
Detector, Peak/Phase	Wavetek Phase Detection System Wavetek 601 Switching System Main Chassis Wavetek 603 Switching System Control Panel* Wavetek 621 Phase Detector Module
DMM, Thermal True RMS	Fluke 8506A
Generator, Pulse/Function	Wavetek 271*
Oscilloscope	Tektronix 7854 Waveform Calculator
Plug-In, Vert, Programmable	Tektronix 7A16P
Plug-In, Horz, Programmable	Tektronix 7B90P
Supply, Power, Programmable	Keithley 230
Synthesizer, Waveform	Wavetek 178*

Terminations and Attenuators	Specifications
Termination A	50 ohm, 2W, 2%
Termination B (Precision*)	50 ohm, 2W, 0.1%
Termination C (Precision*)	50 ohm, >12.5W, 0.1%
Attenuator 1	50 ohm, 5X, 2W
Attenuator 2	50 ohm, 10X, 12.5W

*NOTES

A GPIB instrumentation computer can replace the Wavetek 603 control panel.

Any inaccuracy in the precision terminations will cause measurement errors. Either connect trimmer resistors in parallel and adjust the resistance to precise values, or measure the inaccuracy of the termination and scale the test readings accordingly.

The Wavetek 178 waveform synthesizer provides high frequency accuracy. The Wavetek 271 pulse/function generator provides the pulse function.

Table 3-0. Test Equipment Required for Each Test

---REQUIRED EQUIPMENT---

No.	Test Name	Type	SPECT ANZR	COUNTER	PHSEDET621	DMM	FUNCGEN271	SCOPE	PWR SUPPLY	WVFM SYN178	TERMA	TERMB	TERMC	ATTN1	ATTN2
4.	Software Version Test	S	.	.	.	.	.	.	.	.	.	.	.	.	.
5.	Quick Functional Check	C	.	o	.	o	.	.	.	.	.	.	.	.	.
6.	Quick Cal (3.5Vacrms) Check	S	.	.	.	o	.	.	.	.	.	.	.	.	.
7.	Reference Input/Output	S	.	o	.	.	.	o	.	o	o	.	.	.	.
8.	Internal Voltage Reference (2.048Vdc)	S	.	.	.	o	.	.	.	.	.	.	.	.	.
9.	(No Test)	-	.	.	.	.	.	.	.	.	.	.	.	.	.
10.	(No Test)	-	.	.	.	.	.	.	.	.	.	.	.	.	.
11.	Output ON/OFF; 0/50 Ohm Impedance	C	.	.	.	o	.	.	.	.	.	o	.	.	.
12.	Function Check at 600Hz, 10Vp-p	C	.	.	.	o	.	.	.	.	.	o	.	.	.
13.	Sine Amplitude and Offset Accuracy	C	.	.	.	o	.	.	.	.	.	.	.	.	.
14.	Sine Amplitude Accuracy at 50Vp-p	C	.	.	.	o	.	.	.	.	.	.	o	.	.
15.	Square Amplitude and Offset Accuracy	C	.	.	.	o	.	.	.	.	.	.	.	.	.
16.	DC Voltage Accuracy	C	.	.	.	o	.	.	.	.	.	.	.	.	.
17.	DC Current Load	C	.	.	.	o	.	.	.	.	.	.	o	.	.
18.	Attenuator Accuracy	C	.	.	.	o	.	.	.	.	.	o	.	.	.
19.	(No Test)	-	.	.	.	.	.	.	.	.	.	.	.	.	.
20.	(No Test)	-	.	.	.	.	.	.	.	.	.	.	.	.	.
21.	Phase Check	C	.	.	o	o	.	.	.	.	.	o	.	.	.
22.	Frequency Response (Sine)	C	.	.	.	o	.	.	.	.	.	.	.	.	.
23.	Sine Distortion	C	o	.	.	.	.	.	.	.	.	.	.	o	.
24.	Spurious Level	C	o	.	.	.	.	.	.	.	.	.	.	.	.
25.	Rise/Fall and Aberrations	C	.	.	.	.	.	o	.	.	o	.	.	.	o
26.	Square Wave Symmetry	C	.	o	.	.	.	.	.	.	o	.	.	.	.
27.	AM Input	C	.	.	.	o	.	.	o	.	.	.	.	.	.
28.	Sync Out	C	.	.	.	o	.	o	.	.	o	.	.	.	.
29.	Main Generator Mode	S	.	o	.	o	o	.	.	.	o	.	.	.	.
30.	Burst Count	S	.	o	.	.	.	.	.	.	o	.	.	.	.
31.	External Phase Lock	S	.	o	.	.	.	.	.	o	o	.	.	.	.
32.	Programmable Trigger Level	S	.	.	.	o	.	.	o	.	.	.	.	.	.
33.	Internal Trigger	S	.	o	.	.	.	.	.	.	.	.	.	.	.
34.	Marker Output Level	S	.	.	.	o	.	.	.	.	o	.	.	.	.
35.	Sweep Time	S	.	o	.	.	.	.	.	.	o	.	.	.	.
36.	Sweep Modes	S	.	o	.	o	.	.	o	o	o	.	.	.	.
37.	FM/PM Input	S	.	o	.	.	.	.	o	.	o	.	.	.	.
38.	Hold In	S	.	o	.	o	.	.	o	.	o	.	.	.	.
39.	Stored Settings	S	.	.	.	.	.	.	.	.	.	.	.	.	.
40.	Self Diagnostics	S	.	.	.	.	.	.	.	.	.	.	.	.	.

TEST 4: SOFTWARE VERSION TEST

Purpose Read the version number of the software.

Equipment None

Setup Turn 650 power on.

Results Power-up screen displays: "WAVETEK MODEL 650 (V2.1)"

TEST 5: QUICK FUNCTIONAL CHECK

Purpose Verify that each channel has the correct Func Out and Sync Out outputs at power on.

Equipment Counter, DMM.

Setup

Test 5.C.1
CNTR: Function Frequency
650: RESET PARAMETERS CHANNEL(1-4) OUTPUT ONZERO EXECUTE.
Connect 650 Channel (1-4) Sync Out to counter.

Test 5.C.2
DMM: Func Vac
650: RESET PARAMETERS CHANNEL(1-4) OUTPUT ONZERO EXECUTE.
Connect 650 Channel (1-4) Func Out to DMM.

Test 5.C.3
DMM: Func Vdc
650: RESET PARAMETERS CHANNEL(1-4) OUTPUT ONZERO EXECUTE.
Connect 650 Channel (1-4) Func Out to DMM.

Limits
5.C.1 1000Hz ±1%
5.C.2 1.768Vacrms ±1%
5.C.3 0Vdc ±0.150

Results

	PARAMETER	LOLIMIT	READING	HILIMIT	UNIT
5.C.1	SYNC OUT	990	CNTR	1010	Hz
5.C.2	FUNC OUT	1.750	DMM	1.785	Vacrms
5.C.3	FUNC OUT	-0.150	DMM	0.150	Vdc

TEST 6: QUICK CAL (3.5Vacrms) CHECK

Purpose Verify proper calibration of the 650's internal reference voltage source. To calibrate this reference, see step 2 (quick cal amplitude adjust) in the calibration procedure.

Equipment DMM

Setup DMM: Func Vac, Range Auto
650: RESET PARAMETERS CHANNEL 1 AMPLITUDE 9.9 OUTPUT ONZERO, EXECUTE. Connect 650 CH1 Func Out to DMM.

Procedure Press the [Quick Calibrate] key, then take the reading.

Limits Calibration Limits: 3.5Vacrms ±0.1%
Operation Limits: 3.5Vacrms ±0.5%

Results	PARAMETER	±0.5% LOLIMIT	READING	±0.5% HILIMIT	UNIT
6.1	3.5Vacrms	3.4825	DMM	3.5175	Vacrms

TEST 7: REFERENCE INPUT/OUTPUT

Purpose 1) Verify the frequency accuracy of the internal reference clock.
2) Verify that the 650 can detect a signal at 10MHz Ref In, turn off the internal REF clock, and operate from the external reference signal.
3) Verify that the 10MHz Ref Out signal meets TTL hi/lo level specifications.

Equipment Counter, DMM, 178, oscilloscope, termination (50 ohm, 2W, 2%).

Setup

Test 7.1
CNTR: Function Frequency 'A'.
650: Connect 650 10 MHz Ref Out to counter, terminate at counter with 50 ohm, 2W, 2% termination.

Tests 7.2 and 7.3
CNTR: Function Frequency 'A'.
178: Reset, Frequency per test 7.X, Function Sine, Amplitude 0.25Vp-p, Rear Output On, Execute.
Connect signal source 178 Func Out to 650 10MHz Ref In.
Connect 650 10MHz Ref Out to counter. Terminate at counter with 50 ohm, 2W, 2% termination.

Tests 7.4 and 7.5
650: Connect 10 MHz Ref Out to Scope Channel 1. Terminate with 50 ohm, 2W, 2% termination.

Limits Reference Out: 10MHz ±5ppm.
Reference In: Lock to external clock of 10MHz ±1%, 0.5Vp-p signal.
Ref Out TTL Levels: 0.0 < LO < 0.4Vdc, 2.4 < HI < 5Vdc into 50 ohm.

Results	FREQ OF REF IN	LOLIMIT	READING	HILIMIT	UNITS
7.1	No Input	9,999,950	CNTR	10,000,050	Hz
7.2	9.9 MHz	9,899,951	CNTR	9,900,050	Hz
7.3	10.1 MHz	10,099,950	CNTR	10,100,051	Hz
7.4	TTL HI	2.4	SCOPE	5.0	Vdc
7.5	TTL LO	0.0	SCOPE	0.4	Vdc

TEST 8: INTERNAL CALIBRATION VOLTAGE REFERENCE (2.048Vdc)

Purpose: Measure the accuracy of the internal calibration voltage reference.

Equipment: DMM

Setup:
DMM: Func Vdc
650: RESET PARAMETERS
Connect 650 2.048v Out directly to DMM (no termination).

Limits: 2.04Vdc ±1%

Results

	PARAMETER	LOLIMIT	READING	HILIMIT	UNIT
8.1	2.04	2.020	DMM	2.060	Vdc

TEST 11: OUTPUT ON/OFF; 0/50 OHM IMPEDANCE

Purpose . Verify correct operation of the output impedances and on/off controls of all channels.

Equipment DMM, Termination (50 ohm, 2W, 0.1%)

Comment Any inaccuracy in the 50 ohm termination will cause a measurement error. Therefore, you must measure the inaccuracy, then scale the voltage readings accordingly. Also, the way you connect the termination and coaxial cable to the 650 and the DMM can cause error.

Setup
650: RESET PARAMETERS, AMPLITUDE 2.5Vp-p, OUTPUT (setting per test 11.C.X), EXECUTE.
DMM: Function Vacrms
Connect 650 CH1-4 Func Out to DMM terminated with 50 ohm, 2W, 0.1% termination.
See Output Setting for test specific setup.

Limits
11.1 0.884 ±0.5%
11.2 0.884 ±0.5%
11.3 0.000 +0.01, -0
11.4 0.884 ±0.5%
11.5 1.768 ±0.5%

Results	OUTPUT SETTING	LOLIMIT	READING	HILIMIT	UNIT
11.C.1	Z=0, Output On (use external 50 ohm term)	0.879	DMM	0.888	Vrms
11.C.2	Z=50, Output On (use external 50 ohm term)	0.879	DMM	0.888	Vrms
11.C.3	Z=0, Output Off	0.000	DMM	0.010	Vrms
11.C.4	Z=0, Output On (no external termination)	0.879	DMM	0.888	Vrms
11.C.5	Z=50, output on (no external termination)	1.758	DMM	1.778	Vrms

TEST 12: FUNCTION CHECK AT 600Hz, 10Vp-p

Purpose Verify that each channel allows selection of the SINE, TRIANG, RAMP, SQUARE, and DC functions and that each function operates correctly.

Equipment: DMM, 50 ohm, 2W, 0.1% termination.

Comment Any inaccuracy in the 50 ohm termination will cause a measurement error. Therefore, you must measure the inaccuracy, then scale the voltage readings accordingly. Also, the way you connect the termination and coaxial cable to the 650 and the DMM can cause error.

Setup

Test 12.C.X.X
DMM: Function Vac
650: FREQUENCY 600 MODE CONTINUOUS CHANNEL (1-4) FUNCTION (per test 12.C.X.1) PHASE 0 AMPLITUDE 10 OUTPUT ON-50 EXECUTE. Connect Channel (1-4) Func Out to DMM. Terminate with 50 ohm, 2W, 0.1% termination.

Test 12.C.5
DMM: Function Vdc
650: FREQUENCY 600 MODE CONTINUOUS CHANNEL (1-4) FUNCTION (test 12.C.X.1) PHASE 0 AMPLITUDE 10 OUTPUT ON-50 EXECUTE. Connect Channel (1-4) Func Out to DMM. Terminate with 50 ohm, 2W, 0.1% termination.

Limits

SINE Ampl	10Vp-p	±0.5%
TRIANG Ampl	10Vp-p	±0.5%
SQUARE Ampl	10Vp-p	±0.5%
RAMP Ampl	10Vp-p	±0.5%
DC (0Vdc)	0Vdc	±10mVdc
Offset	0Vdc	±150mVdc

Results	FUNCTION (Vrms)	LOLIMIT	READING	HILIMIT	UNIT
12.C.1.1	Sine (3.536)	3.516	DMM	3.556	Vrms
12.C.1.2	Offset	-0.150	DMM	0.150	Vdc
12.C.2.1	Triangle (2.886)	2.870	DMM	2.902	Vrms
12.C.2.2	Offset	-0.150	DMM	0.150	Vdc
12.C.3.1	Square (5)	4.973	DMM	5.027	Vrms
12.C.3.2	Offset	-0.150	DMM	0.150	Vdc
12.C.4.1	Ramp (2.886)	2.870	DMM	2.902	Vrms
12.C.4.2	Offset	-0.150	DMM	0.150	Vdc
12.C.5	DC (0Vdc)	-0.010	DMM	+0.010	mVdc

TEST 13: SINE AMPLITUDE AND OFFSET ACCURACY

Purpose Verify that sine wave amplitude and offset meet specifications across the 0db range for all channels.

Equipment DMM

Comment The particular function and amplitude chosen will cause small changes in offset voltage. Because the sine and square waves have slightly different internal signal paths, test 15 tests for square wave amplitude and offset accuracy. Auto Cal measures the gain and offset errors of the signal path, then corrects those errors during operation. To see if Auto Cal works, the test points below include the calibration points used by the 650.

Setup

Test 13.C.X.1
DMM: Function Vacrms
650: RESET, FREQUENCY 600, CHANNEL (1-4), FUNCTION SINE, AMPLITUDE (per test 13.C.X.1), OUTPUT ONZERO EXECUTE.
Connect 650 CH1-4 Func Out to DMM.

Test 13.C.X.2
DMM: Function Vdc
650: RESET, FREQUENCY 600, MODE TRIGGERED, CHANNEL (1-4), FUNCTION SINE, AMPLITUDE (per test 13.C.X.1), OUTPUT ONZERO EXECUTE.
Connect 650 CH1-4 Func Out to DMM.

Limits

13.C.X.1	Vp-p	±0.5%
13.C.X.2	Ovdc	±0.15 Vdc

Results

	AMP SETTING (Vrms)	LOLIMIT	READING	HILIMIT	UNIT
13.C.1.1	2.5Vp-p (.884)	0.880	DMM	0.888	Vrms
13.C.1.2	Offset 0	0.150	DMM	0.150	Vdc
13.C.2.1	5.0Vp-p (1.768)	1.759	DMM	1.777	Vrms
13.C.2.2	Offset 0	0.150	DMM	0.150	Vdc
13.C.3.1	7.5Vp-p (2.652)	2.639	DMM	2.665	Vrms
13.C.3.2	Offset 0	-0.150	DMM	0.150	Vdc
13.C.4.1	10.0Vp-p (3.536)	3.518	DMM	3.554	Vrms
13.C.4.2	Offset 0	-0.150	DMM	0.150	Vdc
13.C.5.1	12.5Vp-p (4.419)	4.397	DMM	4.441	Vrms
13.C.5.2	Offset 0	-0.150	DMM	0.150	Vdc
13.C.6.1	15.0Vp-p (5.303)	5.276	DMM	5.330	Vrms
13.C.6.2	Offset 0	-0.150	DMM	0.150	Vdc
13.C.7.1	17.5Vp-p (6.187)	6.156	DMM	6.218	Vrms
13.C.7.2	Offset 0	-0.150	DMM	0.150	Vdc

13.C.8.1	20.0Vp-P (7.071)	7.036	DMM	7.106	Vrms
13.C.8.2	Offset 0	-0.150	DMM	0.150	Vdc
13.C.9.1	22.5Vp-P (7.955)	7.915	DMM	7.995	Vrms
13.C.9.2	Offset 0	-0.150	DMM	0.150	Vdc
13.C.10.1	25.0Vp-P (8.839)	8.795	DMM	8.883	Vrms
13.C.10.2	Offset 0	-0.150	DMM	0.150	Vdc

TEST 14: SINE WAVE AMPLITUDE ACCURACY AT 50Vp-p

Purpose Verify that each channel can deliver 0.5 amp into a 50 ohm load and still maintain the maximum peak-to-peak output voltage.

Equipment DMM, termination (50 ohm, 12.5W minimum, 0.1%).

Comment Any inaccuracy in the 50 ohm termination will cause a measurement error. Therefore, you must measure the inaccuracy, then scale the voltage readings accordingly. Also, the way you connect the termination and coaxial cable to the 650 and the DMM can cause error.

Setup

DMM: Function Vacrms.

650: RESET, FREQUENCY 600, CHANNEL (1-4), FUNCTION SINE AMPLITUDE 50, OUTPUT ONZERO, EXECUTE.
Connect 650 Channel (1-4) Func Out to DMM. Terminate with 50 ohm, 12.5W, 0.1% termination.

Limits 17.678 ±0.5%

Results	SETTING	LOLIMIT	READING	HILIMIT	UNIT
14.C.1	50Vp-p (17.678)	17.590	DMM	17.766	Vrms

TEST 15: SQUARE AMPLITUDE AND OFFSET ACCURACY

Purpose Verify that the square wave amplitude and offset meet specifications across the Odb range for all channels.

Equipment DMM

Comment Because the square and sine waves have slightly different internal signal paths, test 13 tests for sine wave amplitude and offset accuracy. Auto Cal measures the gain and offset errors of the signal path, then corrects those errors during operation. To see if Auto Cal works, the test points below include the calibration points used by the 650.

Determine DC offset and amplitude for the square wave by measuring the positive peak and the negative peak voltage levels. Subtract the peak values to get the amplitude; average the peak values to get the offset. Set the 650 to MODE TRIGGERED and PHASE to +90°/-90° to measure the respective positive and negative peaks.

Setup DMM: Function Vdc
650: RESET, MODE TRIGGERED, CHANNEL (1-4), FUNCTION SQUARE, AMPLITUDE (per test 15.C.X.1), OUTPUT ONZERO, EXECUTE.
Connect 650 Channel (1-4) Func Out to DMM.

Limits

15.C.X.1	Vp-p ±0.5%
15.C.X.2	0Vdc ±0.15 Vdc

Results

	AMP SETTING	LOLIMIT	READING	HILIMIT	UNITS
15.C.1.1	AMPL 2.5	2.488	DMM	2.513	Vp-p
15.C.1.2	Offset 0	-0.150	DMM	0.150	Vdc
15.C.2.1	AMPL 5.0	4.975	DMM	5.025	Vp-p
15.C.2.2	Offset 0	-0.150	DMM	0.150	Vdc
15.C.3.1	AMPL 7.5	7.463	DMM	7.538	Vp-p
15.C.3.2	Offset 0	-0.150	DMM	0.150	Vdc
15.C.4.1	AMPL 10.0	9.950	DMM	10.050	Vp-p
15.C.4.2	Offset 0	-0.150	DMM	0.150	Vdc
15.C.5.1	AMPL 12.5	12.438	DMM	12.563	Vp-p
15.C.5.2	Offset 0	-0.150	DMM	0.150	Vdc
15.C.6.1	AMPL 15.0	14.925	DMM	15.075	Vp-p
15.C.6.2	Offset 0	-0.150	DMM	0.150	Vdc
15.C.7.1	AMPL 17.5	17.413	DMM	17.588	Vp-p
15.C.7.2	Offset 0	-0.150	DMM	0.150	Vdc
15.C.8.1	AMPL 20.0	19.900	DMM	20.100	Vp-p
15.C.8.2	Offset 0	-0.150	DMM	0.150	Vdc

15.C.9.1	AMPL 22.5	22.388	DMM	22.613	Vp-p
15.C.9.2	Offset 0	-0.150	DMM	0.150	Vdc
15.C.10.1	AMPL 25.0	24.875	DMM	25.125	Vp-p
15.C.10.2	Offset 0	-0.150	DMM	0.150	Vdc

TEST 16: DC VOLTAGE ACCURACY TEST

Purpose Verify DC voltage accuracy for each channel.

Equipment DMM

Setup DMM: Function Vdc.
650: RESET, CHANNEL (1-4), FUNCTION DC, OFFSET (per test 16.C.X), OUTPUT ONZERO, EXECUTE.
Connect 650 Channel (1-4) Func Out to DMM.

Limits ±0.3% ±10mVdc

Results	DC OFFSET	LOLIMIT	READING	HILIMIT	UNITS
16.C.1	25	24.915	DMM	25.085	Vdc
16.C.2	20	19.930	DMM	20.070	Vdc
16.C.3	15	14.945	DMM	15.055	Vdc
16.C.4	10	9.960	DMM	10.040	Vdc
16.C.5	5	4.975	DMM	5.025	Vdc
16.C.6	0	-0.010	DMM	+0.010	Vdc
16.C.7	-5	-5.025	DMM	-4.975	Vdc
16.C.8	-10	-10.040	DMM	-9.960	Vdc
16.C.9	-15	-15.055	DMM	-14.945	Vdc
16.C.10	-20	-20.070	DMM	-19.930	Vdc
16.C.11	-25	-25.085	DMM	-24.915	Vdc

TEST 17: DC CURRENT LOAD TEST

Purpose Verify that each channel can deliver 0.5 amp into a 50 ohm load and still maintain the maximum dc output voltage.

Equipment DMM, termination (50 ohm, 12.5W minimum, 0.1%).

Comment Any inaccuracy in the 50 ohm termination will cause a measurement error. Therefore, you must measure the inaccuracy, then scale the voltage readings accordingly. Also, the way you connect the termination and coaxial cable to the 650 and the DMM can cause error.

Setup

DMM: Function Vdc.
650: RESET, CHANNEL (1-4), FUNCTION DC, OFFSET (per test 17.C.X), OUTPUT ONZERO, EXECUTE.
--- Connect the 650 Channel (1-4) Func Out to the DMM. Terminate with 50 ohm, 12.5W minimum, 0.1% termination.

Limits ±0.5% ±10mVdc

Results	SETTING	LOLIMIT	READING	HILIMIT	UNIT
17.C.1	25.0	24.865	DMM	25.135	Vdc
17.C.2	-25.0	-25.135	DMM	-24.865	Vdc

TEST 18: ATTENUATOR ACCURACY

Purpose Verify the accuracy of the output attenuator of each channel. This test tests the 0dB, 20dB, and 40dB attenuator ranges by measuring the voltage accuracy of three AC signals.

Equipment DMM, termination (50 ohm, 2W, 0.1%)

Comment Any inaccuracy in the 50 ohm termination will cause a measurement error. Therefore, you must measure the inaccuracy, then scale the voltage readings accordingly. Also, the way you connect the termination and coaxial cable to the 650 and the DMM can cause error.

Setup
DMM: Function Vacrms
650: RESET, CHANNEL (1-4), AMPLITUDE (per test 18.C.X), OUTPUT ON-50 EXECUTE.
Connect 650 Channel (1-4) Func Out to DMM. Terminate with 50 ohm, 2W, 0.1% termination.

Limits

18.C.1	±0.5% ±2mVdc
18.C.2	±0.5% ±2mVdc
18.C.3	±0.5% ±2mVdc

Results

	AMPLITUDE (Vp-p, Vrms, dB)	LOLIMIT	READING	HILIMIT	UNIT
18.C.1	10.0, 3.5360, 0	3.5163	DMM	3.5557	Vacrms
18.C.2	1.0, 0.3536, 20	0.3498	DMM	0.3574	Vacrms
18.C.3	0.1, 0.0354, 40	0.0332	DMM	0.0376	Vacrms

TEST 20: 180° PHASE VERIFICATION PROCEDURE

Purpose Verify the phase accuracy between two sine waveforms 180° out of phase.

Equipment Power combiner (shown in figure 3-1), HP 3580A or similar spectrum analyzer, one matching pair of equal length (4 feet maximum) BNC cables.

Comment For this test you will sum two equal amplitude signals that are 180° out of phase to obtain the desired result of zero volts. A mismatch in signal amplitudes or BNC cable lengths will give an erroneous reading. To eliminate an amplitude mismatch, an adjustable resistor network (power combiner) sums the two input signals. The output is then measured with a spectrum analyzer. Any voltage at the fundamental frequency not caused by amplitude or cable length differences is the error signal amplitude. The phase error is determined by subtracting the output signal level from the input signal level (table 3-1).

Setup

650: AMPLITUDE (10 Vp-p), FREQUENCY (any desired frequency), FUNCTION (sine), PHASE (0 degree), OUTPUT ON-0Ω impedance. Connect 650 Channel (1-4) Func Out as shown.

SA: Measure Fundamental ATTENUATION +10dB, RESOLUTION BANDWIDTH 10 Hz, CENTER FREQUENCY to match Model 650 frequency, FREQUENCY SPAN 0 Hz, ATTENUATION VERNIER max cw, SWEEP TIME 2 s/div.

Procedure Set Model 650 channel under test to 0°. Use analyzer course and fine frequency adjustments to center the display on the screen. Use the input sensitivity control to set the positive peak of the display at the top line of the anaylzer. This is now the 0 dB reference. Set the Model 650 channel under test to 180°, which should reduce the display signal. Adjust the power combiner for minimum output level, then increase resolution by setting the analyzer attenuator to -10 dB. Readjust the power combiner level to minimum and read the level relative to the 0 dB line. Use table 3-1 to determine the phase error.

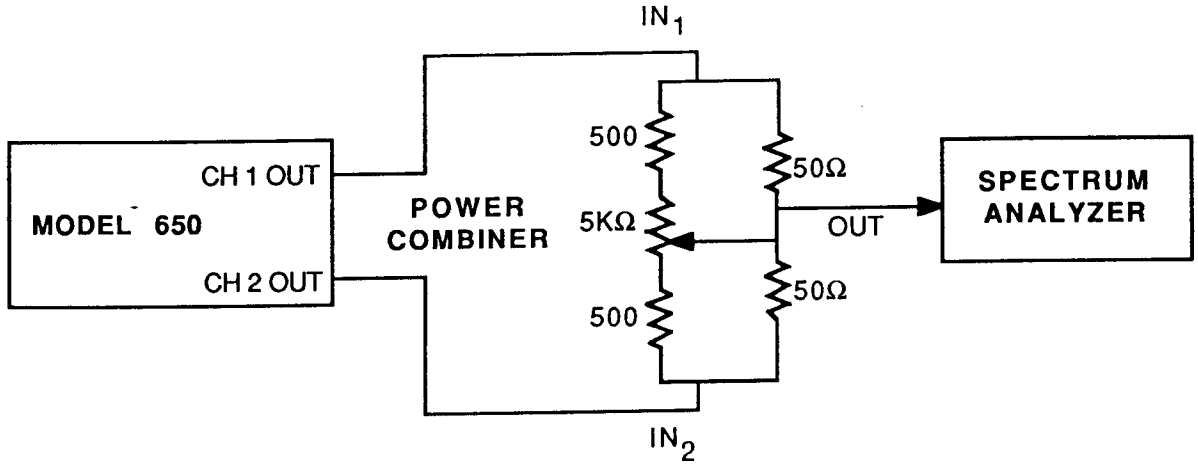


Figure 3-1. 180° Phase Verification Setup

Table 3-1. Phase Error Interpolation

DB	Phase error IN DEGREES	DB	Phase error IN MILLI-DEGREES	DB	Phase error IN MILLI-DEGREES	DB	Phase error IN MILLI-DEGREES
-40	1.15	-60	114.59	-80	11.46	-100	1.15
-41	1.02	-61	102.13	-81	10.21	-101	1.02
-42	0.91	-62	91.02	-82	9.10	-102	0.91
-43	0.81	-63	81.12	-83	8.11	-103	0.81
-44	0.72	-64	72.30	-84	7.23	-104	0.72
-45	0.64	-65	64.44	-85	6.44	-105	0.64
-46	0.57	-66	57.43	-86	5.74	-106	0.57
-47	0.51	-67	51.19	-87	5.12	-107	0.51
-48	0.46	-68	45.62	-88	4.56	-108	0.46
-49	0.41	-69	40.66	-89	4.07	-109	0.41
-50	0.36	-70	36.24	-90	3.62	-110	0.36
-51	0.32	-71	32.30	-91	3.23	-111	0.32
-52	0.29	-72	28.78	-92	2.88	-112	0.29
-53	0.26	-73	25.65	-93	2.57	-113	0.26
-54	0.23	-74	22.86	-94	2.29	-114	0.23
-55	0.20	-75	20.38	-95	2.04	-115	0.20
-56	0.18	-76	18.16	-96	1.82	-116	0.18
-57	0.16	-77	16.19	-97	1.62	-117	0.16
-58	0.14	-78	14.43	-98	1.44	-118	0.14
-59	0.13	-79	12.86	-99	1.29	-119	0.13
60	0.11	-80	11.46	-100	1.15	-120	0.11

TEST 21: PHASE CHECK

Purpose Verify the following for each channel:
1) phase accuracy, and — Tests 21-1, 2, 3, 4
2) quick cal effectiveness. — Tests 21-5, 6, 7, 8

Equipment DMM, Wavetek 621 phase detector, two terminations (50 ohms, 2W, 0.1%, one per channel)

Setup
1) Connect DMM, 621, 650, and terminations per figure 3-2, the test 21 connection diagram.
2) Run 650 Auto-Cal as follows: Utility CAL START.

Comment Phase Accuracy Tests. Tests 21-2 through 21-4 use channel 1 as a reference to measure the phase errors of channels 2 through 4, while test 21-1 uses channel 2 as a reference to measure the phase error of channel 1. Each test measures the phase error of its channel at thirteen frequencies from 500Hz to 2MHz. To determine the phase error at each frequency, you must take four measurements, then make a calculation:

DMM A = +90° Direct Reading (ref ch to 621 ref, tst ch to 621 tst)
DMM B = +90° Swapped Reading (ref ch to 621 tst, tst ch to 621 ref)
DMM C = -90° Direct Reading
DMM D = -90° Swapped Reading

CHC FRQ X 90° Phase Error = [(A+B)-(C+D)]/4 (unscaled)

Setting the 650 to ±90° and swapping the reference/test channel leads eliminates the phase errors caused by the test setup. Relay 6 in the 621 phase detector swaps the leads automatically.

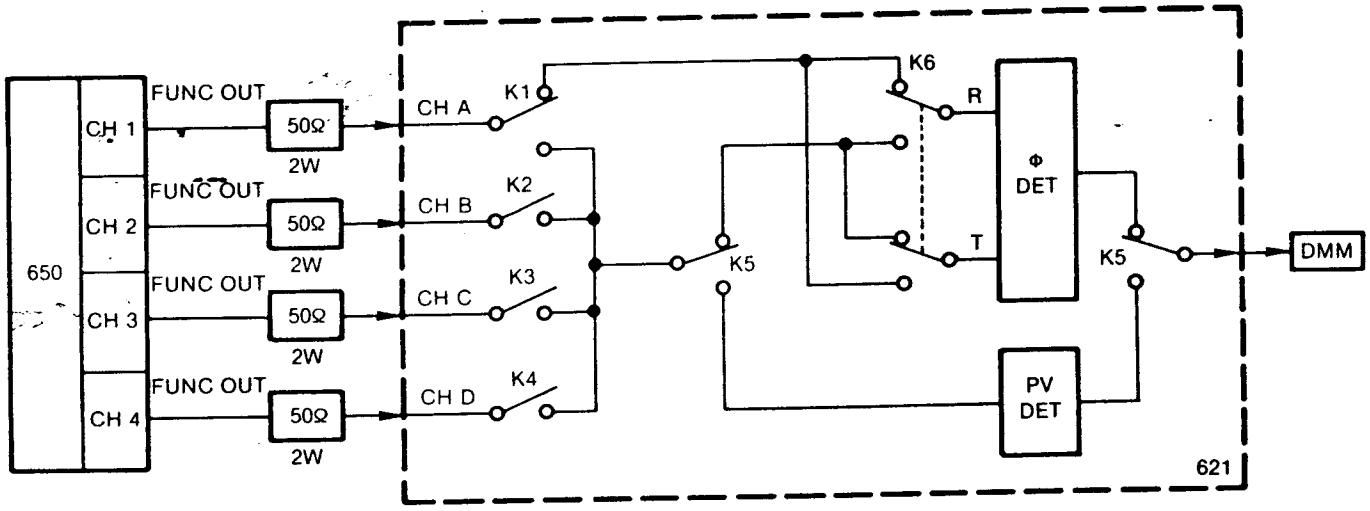
Because the 621 delivers less than 1V per degree of error, the above formula requires a scaler to convert the result to degrees. To develop the scaler, you use the above procedure to determine the phase error at 90° and at 91°, then calculate the scaler as follows:

CHC Scaler = 1/(CHC 91° Phase Error - CHC 90° Phase Error)

The actual (scaled) formula that you will use to calculate phase error at each frequency looks like this:

CHC FRQ X 90° Phase Error = (CHC Scaler) x ([(A+B)-(C+D)]/4)

Comment Quick Cal Effectiveness Tests. Tests 21-5 through 21-8 measure the ability of the quick calibrate feature to optimize the phase error of each channel for the current 650 setup and environment. The test procedure matches that of tests 1 through 4, with the following exceptions: 1) you do not have to recalculate the channel scalers, 2) you determine phase error at only three frequencies per channel, and 3) you press the Quick Calibrate key before each reading.



NOTES

Make all signal paths equal length.
50Ω termination resistances must fall within ±0.1% of each other.
All relays shown in open position.

Figure 3-2. Test 21 Connection Diagram

TEST 21-1: PHASE CHECK (Channel 1 Phase Measured in Rererence to Channel 2)

Setup

DMM: Function Vdc
621: Set relays as described below.
650: RESET PARAMS, Channel Number 1, Channel AMPL 4, SHIFT OUTPUT ON-0, Channel Number 2, Channel AMPL 4, SHIFT OUTPUT ON-0 EXECUTE. Set main frequency and each channel's phase as described below.

Procedure

STEP	650 TEST CHAN	SET TCHAN PHASE	650 REFN CHAN	SET RCHAN PHASE	621 RELAY STATES 1	2	3	4	5	6	SET 650 MAIN FREQUENCY	READ DMM
1	CH1	+91°	CH2	0°	O	C	O	O	O	O	1000 Hz	A
2	CH1	+91°	CH2	0°	O	C	O	O	O	C	1000 Hz	B
3	CH1	-89°	CH2	0°	O	C	O	O	O	O	1000 Hz	C
4	CH1	-89°	CH2	0°	O	C	O	O	O	C	1000 Hz	D
5	Calculate: CH1 91° Phase Error = ((A+B)-(C+D))/4											
6	CH1	+90°	CH2	0°	O	C	O	O	C	O	1000 Hz	E
7	CH1	+90°	CH2	0°	O	C	O	O	O	C	1000 Hz	F
8	CH1	-90°	CH2	0°	O	C	O	O	O	O	1000 Hz	G
9	CH1	-90°	CH2	0°	O	C	O	O	O	C	1000 Hz	H
10	Calculate: CH1 90° Phase Error = ((E+F)-(G+H))/4											
11	Calculate: CH1 Scaler = 1/(CH1 91° Phase Error - CH1 90° Phase Error)											
12	Repeat steps 13-17 for each test frequency specified below.											
13	CH1	+90°	CH2	0°	O	C	O	O	O	O	Per 21.1.X	I
14	CH1	+90°	CH2	0°	O	C	O	O	O	C	Per 21.1.X	J
15	CH1	-90°	CH2	0°	O	C	O	O	O	O	Per 21.1.X	K
16	CH1	-90°	CH2	0°	O	C	O	O	O	C	Per 21.1.X	L
17	Calculate: CH1 90° FRQ X Phase Error = (CH1 Scaler) x (((I+J)-(K+L))/4)											

Test	Frequency	Test	Frequency
21.1.1	500.000 Hz	21.1.8	100.000kHz
21.1.2	1.000kHz	21.1.9	200.000kHz
21.1.3	2.000kHz	21.1.10	500.000kHz
21.1.4	5.000kHz	21.1.11	1.000MHz
21.1.5	10.000kHz	21.1.12	1.500MHz
21.1.6	20.000kHz	21.1.13	2.000MHz
21.1.7	50.000kHz		

Results

The results follow test 21-8.

TEST 21-2: PHASE CHECK (Channel 2 Phase Measured in Reference to Channel 1)

Setup
DMM: Function Vdc
621: Set relays as described below.
650: RESET PARAMS, Channel Number 1, Channel AMPL 4, SHIFT OUTPUT ON-0, Channel Number 2, Channel AMPL 4, SHIFT OUTPUT ON-0 EXECUTE. Set main frequency and each channel's phase as described below.

Procedure

STEP	650 TEST CHAN	SET TCHAN PHASE	650 REFN CHAN	SET RCHAN PHASE	621 RELAY STATES 1	2	3	4	5	6	SET 650 MAIN FREQUENCY	READ DMM
1	CH2	+91°	CH1	0°	O	C	O	O	O	O	1000 Hz	A
2	CH2	+91°	CH1	0°	O	C	O	O	O	C	1000 Hz	B
3	CH2	-89°	CH1	0°	O	C	O	O	O	O	1000 Hz	C
4	CH2	-89°	CH1	0°	O	C	O	O	O	C	1000 Hz	D
5	Calculate: CH2 91° Phase Error = ((A+B)-(C+D))/4											
6	CH2	+90°	CH1	0°	O	C	O	O	O	O	1000 Hz	E
7	CH2	+90°	CH1	0°	O	C	O	O	O	C	1000 Hz	F
8	CH2	-90°	CH1	0°	O	C	O	O	O	O	1000 Hz	G
9	CH2	-90°	CH1	0°	O	C	O	O	O	C	1000 Hz	H
10	Calculate: CH2 90° Phase Error = ((E+F)-(G+H))/4											
11	Calculate: CH2 Scaler = 1/(CH2 91° Phase Error - CH2 90° Phase Error)											
12	Repeat steps 13-17 for each test frequency specified below.											
13	CH2	+90°	CH1	0°	O	C	O	O	O	O	Per 21.2.X	I
14	CH2	+90°	CH1	0°	O	C	O	O	O	C	Per 21.2.X	J
15	CH2	-90°	CH1	0°	O	C	O	O	O	O	Per 21.2.X	K
16	CH2	-90°	CH1	0°	O	C	O	O	O	C	Per 21.2.X	L
17	Calculate: CH2 90° FRQ X Phase Error = (CH2 Scaler) x (((I+J)-(K+L))/4)											

Test	Frequency	Test	Frequency
21.2.1	500.000 Hz	21.2.8	100.000kHz
21.2.2	1.000kHz	21.2.9	200.000kHz
21.2.3	2.000kHz	21.2.10	500.000kHz
21.2.4	5.000kHz	21.2.11	1.000MHz
21.2.5	10.000kHz	21.2.12	1.500MHz
21.2.6	20.000kHz	21.2.13	2.000MHz
21.2.7	50.000kHz		

Results The results follow test 21-8.

TEST 21-3: PHASE CHECK (Channel 3 Phase Measured in Reference to Channel 1)

Setup
- DMM: Function Vdc
- 621: Set relays as described below.
- 650: RESET PARAMS, Channel Number 1, Channel AMPL 4, SHIFT OUTPUT ON-0, Channel Number 3, Channel AMPL 4, SHIFT OUTPUT ON-0 EXECUTE. Set main frequency and each channel's phase as described below.

Procedure

STEP	650 TEST CHAN	SET TCHAN PHASE	650 REFN CHAN	SET RCHAN PHASE	621 RELAY STATES 1	2	3	4	5	6	SET 650 MAIN FREQUENCY	READ DMM
1	CH3	+91°	CH1	0°	O	O	C	O	O	O	1000 Hz	A
2	CH3	+91°	CH1	0°	O	O	C	O	O	C	1000 Hz	B
3	CH3	-89°	CH1	0°	O	O	C	O	O	O	1000 Hz	C
4	CH3	-89°	CH1	0°	O	O	C	O	O	C	1000 Hz	D
5	Calculate: CH3 91° Phase Error = ((A+B)-(C+D))/4											
6	CH3	+90°	CH1	0°	O	O	C	O	O	O	1000 Hz	E
7	CH3	+90°	CH1	0°	O	O	C	O	O	C	1000 Hz	F
8	CH3	-90°	CH1	0°	O	O	C	O	O	O	1000 Hz	G
9	CH3	-90°	CH1	0°	O	O	C	O	O	C	1000 Hz	H
10	Calculate: CH3 90° Phase Error = ((E+F)-(G+H))/4											
11	Calculate: CH3 Scaler = 1/(CH3 91° Phase Error - CH3 90° Phase Error)											
12	Repeat steps 13-17 for each test frequency specified below.											
13	CH3	+90°	CH1	0°	O	O	C	O	O	O	Per 21.3.X	I
14	CH3	+90°	CH1	0°	O	O	C	O	O	C	Per 21.3.X	J
15	CH3	-90°	CH1	0°	O	O	C	O	O	O	Per 21.3.X	K
16	CH3	-90°	CH1	0°	O	O	C	O	O	C	Per 21.3.X	L
17	Calculate: CH3 90° FRQ X Phase Error = (CH3 Scaler) x (((I+J)-(K+L))/4)											

Test	Frequency	Test	Frequency
21.3.1	500.000 Hz	21.3.8	100.000kHz
21.3.2	1.000kHz	21.3.9	200.000kHz
21.3.3	2.000kHz	21.3.10	500.000kHz
21.3.4	5.000kHz	21.3.11	1.000MHz
21.3.5	10.000kHz	21.3.12	1.500MHz
21.3.6	20.000kHz	21.3.13	2.000MHz
21.3.7	50.000kHz		

Results The results follow test 21-8.

TEST 21-4: PHASE CHECK (Channel 4 Phase Measured in Reference to Channel 1)

Setup. DMM: Function Vdc
621: Set relays as described below.
650: RESET PARAMS, Channel Number 1, Channel AMPL 4, SHIFT OUTPUT ON-0, Channel Number 4, Channel AMPL 4, SHIFT OUTPUT ON-0 EXECUTE. Set main frequency and each channel's phase as described below.

Procedure

STEP	650 TEST CHAN	SET TCHAN PHASE	650 REFN CHAN	SET RCHAN PHASE	621 RELAY STATES 1	2	3	4	5	6	SET 650 MAIN FREQUENCY	READ DMM
1	CH4	+91°	CH1	0°	O	O	O	C	O	O	1000 Hz	A
2	CH4	+91°	CH1	0°	O	O	O	C	O	C	1000 Hz	B
3	CH4	-89°	CH1	0°	O	O	O	C	O	O	1000 Hz	C
4	CH4	-89°	CH1	0°	O	O	O	C	O	C	1000 Hz	D
5	Calculate: CH4 91° Phase Error = ((A+B)-(C+D))/4											
6	CH4	+90°	CH1	0°	O	O	O	C	O	O	1000 Hz	E
7	CH4	+90°	CH1	0°	O	O	O	C	O	C	1000 Hz	F
8	CH4	-90°	CH1	0°	O	O	O	C	O	O	1000 Hz	G
9	CH4	-90°	CH1	0°	O	O	O	C	O	C	1000 Hz	H
10	Calculate: CH4 90° Phase Error = ((E+F)-(F+H))/4											
11	Calculate: CH4 Scaler = 1/(CH4 91° Phase Error - CH4 90° Phase Error)											
12	Repeat steps 13-17 for each test frequency specified below.											
13	CH4	+90°	CH1	0°	O	O	O	C	O	O	Per 21.4.X	I
14	CH4	+90°	CH1	0°	O	O	O	C	O	C	Per 21.4.X	J
15	CH4	-90°	CH1	0°	O	O	O	C	O	O	Per 21.4.X	K
16	CH4	-90°	CH1	0°	O	O	O	C	O	C	Per 21.4.X	L
17	Calculate: CH4 90° FRQ X Phase Error = (CH4 Scaler) x (((I+J)-(K+L))/4)											

Test	Frequency	Test	Frequency
21.4.1	500.000 Hz	21.4.8	100.000kHz
21.4.2	1.000kHz	21.4.9	200.000kHz
21.4.3	2.000kHz	21.4.10	500.000kHz
21.4.4	5.000kHz	21.4.11	1.000MHz
21.4.5	10.000kHz	21.4.12	1.500MHz
21.4.6	20.000kHz	21.4.13	2.000MHz
21.4.7	50.000kHz		

Results The results follow test 21-8.

TEST 21-5: PHASE CHECK (Auto-Cal Effectiveness for Channel 1)

Setup

DMM: Function Vdc
621: Set relays as described below.
650: RESET PARAMS, Channel Number 1, Channel AMPL 4, SHIFT OUTPUT ON-0, Channel Number 2, Channel AMPL 4, SHIFT OUTPUT ON-0 EXECUTE. Set main frequency and each channel's phase as described below.

Procedure

STEP	650 TEST CHAN	SET TCHAN PHASE	650 REFN CHAN	SET RCHAN PHASE	621 RELAY STATES 1	2	3	4	5	6	SET 650 MAIN FREQUENCY	READ DMM
1	Repeat steps 2-6 for each frequency specified below. For each step, first set the frequency and phase, then press Quick Calibrate, then read the DVM.											
2	CH1	+90°	CH2	0°	O	C	O	O	O	O	Per 21.1.X	I
3	CH1	+90°	CH2	0°	O	C	O	O	O	C	Per 21.1.X	J
4	CH1	-90°	CH2	0°	O	C	O	O	O	O	Per 21.1.X	K
5	CH1	-90°	CH2	0°	O	C	O	O	O	C	Per 21.1.X	L
6	Using the CH1 Scaler derived in part 21-1, calculate: CH1 90° FRQ X Phase Error = (CH1 Scaler) x (((I+J)-(K+L))/4)											

Test	Frequency
21.1.14	1.000MHz
21.1.15	1.500MHz
21.1.16	2.000MHz

Results The results follow test 21-8.

TEST 21-6: PHASE CHECK (Auto-Cal Effectiveness for Channel 2)

Setup:
DMM: Function Vdc
621: Set relays as described below.
650: RESET PARAMS, Channel Number 1, Channel AMPL 4, SHIFT OUTPUT ON-0, Channel Number 2, Channel AMPL 4, SHIFT OUTPUT ON-0 EXECUTE. Set main frequency and each channel's phase as described below.

Procedure

STEP	650 TEST CHAN	SET TCHAN PHASE	650 REFN CHAN	SET RCHAN PHASE	621 RELAY STATES 1	2	3	4	5	6	SET 650 MAIN FREQUENCY	READ DMM
1	Repeat steps 2-6 for each frequency specified below. For each step, first set the frequency and phase, then press Quick Calibrate, then read the DVM.											
2	CH2	+90°	CH1	0°	O	C	O	O	O	O	Per 21.2.X	I
3	CH2	+90°	CH1	0°	O	C	O	O	O	C	Per 21.2.X	J
4	CH2	-90°	CH1	0°	O	C	O	O	O	O	Per 21.2.X	K
5	CH2	-90°	CH1	0°	O	C	O	O	O	C	Per 21.2.X	L
6	Using the CH2 Scaler derived in part 21-2, calculate: CH2 90° FRQ X Phase Error = (CH2 Scaler) x (((I+J)-(K+L))/4)											

Test	Frequency
21.2.14	1.000MHz
21.2.15	1.500MHz
21.2.16	2.000MHz

Results: The results follow test 21-8.

TEST 21-7: PHASE CHECK (Auto-Cal Effectiveness for Channel 3)

Setup

DMM: Function Vdc
621: Set relays as described below.
650: RESET PARAMS, Channel Number 1, Channel AMPL 4, SHIFT OUTPUT ON-0, Channel Number 3, Channel AMPL 4, SHIFT OUTPUT ON-0 EXECUTE. Set main frequency and each channel's phase as described below.

Procedure

STEP	650 TEST CHAN	SET TCHAN PHASE	650 REFN CHAN	SET RCHAN PHASE	621 RELAY STATES 1	2	3	4	5	6	SET 650 MAIN FREQUENCY	READ DMM
1	Repeat steps 2-6 for each frequency specified below. For each step, first set the frequency and phase, then press Quick Calibrate, then read the DVM.											
2	CH3	+90°	CH1	0°	O	O	C	O	O	O	Per 21.3.X	I
3	CH3	+90°	CH1	0°	O	O	C	O	O	C	Per 21.3.X	J
4	CH3	-90°	CH1	0°	O	O	C	O	O	O	Per 21.3.X	K
5	CH3	-90°	CH1	0°	O	O	C	O	O	C	Per 21.3.X	L
6	Using the CH3 Scaler derived in part 21-3, calculate: CH3 90° FRQ X Phase Error = (CH3 Scaler) x (((I+J)-(K+L))/4)											

Test	Frequency
21.3.14	1.000MHz
21.3.15	1.500MHz
21.3.16	2.000MHz

Results The results follow test 21-8.

TEST 21-8: PHASE CHECK (Auto-Cal Effectiveness for Channel 4)

Setup

DMM: Function Vdc
621: Set relays as described below.
650: RESET PARAMS, Channel Number 1, Channel AMPL 4, SHIFT OUTPUT ON-0, Channel Number 4, Channel AMPL 4, SHIFT OUTPUT ON-0 EXECUTE. Set main frequency and each channel's phase as described below.

Procedure

STEP	650 TEST CHAN	SET TCHAN PHASE	650 REFN CHAN	SET RCHAN PHASE	621 RELAY STATES 1	2	3	4	5	6	SET 650 MAIN FREQUENCY	READ DMM
1	Repeat steps 2-6 for each frequency specified below. For each step, first set the frequency and phase, then press Quick Calibrate, then read the DVM.											
2	CH4	+90°	CH1	0°	O	O	O	C	O	O	Per 21.4.X	I
3	CH4	+90°	CH1	0°	O	O	O	C	O	C	Per 21.4.X	J
4	CH4	-90°	CH1	0°	O	O	O	C	O	O	Per 21.4.X	K
5	CH4	-90°	CH1	0°	O	O	O	C	O	C	Per 21.4.X	L
6	Using the CH4 Scaler derived in part 21-4, calculate: CH4 90° FRQ X Phase Error = (CH4 Scaler) x (((I+J)-(K+L))/4)											

Test	Frequency
21.4.14	1.000MHz
21.4.15	1.500MHz
21.4.16	2.000MHz

Results The results follow test 21-8.

Phase Accuracy Test Results for CH1-4 (Tests 21-1, 2, 3, and 4)

Results	FREQUENCY	LOLIMIT	Calculation	HILIMIT	UNIT
	CHANNEL SCALER			1.500	
21.C.1	500.0 Hz	-0.0050	PHASE ERROR	+0.0050	Deg
21.C.2	1.0kHz	-0.0050	PHASE ERROR	+0.0050	Deg
21.C.3	2.0kHz	-0.0300	PHASE ERROR	+0.0300	Deg
21.C.4	5.0kHz	-0.0300	PHASE ERROR	+0.0300	Deg
21.C.5	10.0kHz	-0.1000	PHASE ERROR	+0.1000	Deg
21.C.6	20.0kHz	-0.1000	PHASE ERROR	+0.1000	Deg
21.C.7	50.0kHz	-0.1000	PHASE ERROR	+0.1000	Deg
21.C.8	100.0kHz	-0.1000	PHASE ERROR	+0.1000	Deg
21.C.9	200.0kHz	-0.5000	PHASE ERROR	+0.5000	Deg
21.C.10	500.0kHz	-0.5000	PHASE ERROR	+0.5000	Deg
21.C.11	1.0MHz	-2.0000	PHASE ERROR	+2.0000	Deg
21.C.12	1.5MHz	-2.0000	PHASE ERROR	+2.0000	Deg
21.C.13	2.0MHz	-2.0000	PHASE ERROR	+2.0000	Deg

Quick Cal Test Results for CH1-4 (Tests 21-5, 6, 7, and 8)

Results	FREQUENCY	LOLIMIT	Calculation	HILIMIT	UNIT
21.C.14	1.0MHz	-1.0000	PHASE ERROR	+1.0000	Deg
21.C.15	1.5MHz	-1.0000	PHASE ERROR	+1.0000	Deg
21.C.16	2.0MHz	-1.0000	PHASE ERROR	+1.0000	Deg

TEST 22: FREQUENCY RESPONSE, SINE

Purpose - Verifies that each channel's sine wave amplitude deviation remains within limits from 10Hz to 20kHz.

Equipment DMM

Setup
DMM: Function VACrms
650: RESET, FREQUENCY (per test 21.C.X), CHANNEL (1-4), FUNCTION SINE, AMPLITUDE 10, OUTPUT ONZERO, EXECUTE.
Connect 650 Channel (1-4) Func Out to DMM.

Limits 22.C.1 to 22.C.6 3.535Vrms ±0.5%

Results	FREQUENCY	LOLIMIT	READING	HILIMITS	UNITS
22.C.1	10.0Hz	3.516	DMM	3.556	Vrms
22.C.2	100.0Hz	3.516	DMM	3.556	Vrms
22.C.3	1000.0Hz	3.516	DMM	3.556	Vrms
22.C.4	5000.0Hz	3.516	DMM	3.556	Vrms
22.C.5	10000.0Hz	3.516	DMM	3.556	Vrms
22.C.6	20000.0Hz	3.516	DMM	3.556	Vrms

Results	PARAMETER	LOLIMIT	READING	HILIMIT	UNIT
23.C.1	1 kHz				
23.C.1.1	FUND PWR	-2.00	SPEC ANA	NONE	dBm
23.C.1.2	WORST HARM		2 or 3		nd/rd
23.C.1.3	HARM PWR		SPEC ANA		dBm
23.C.1.4	FUND-HARM	-90	FUND-HARM	-60	dBc
23.C.2	2 kHz				
23.C.2.1	FUND PWR	-2.00	SPEC ANA	NONE	dBm
23.C.2.2	WORST HARM		2 or 3		nd/rd
23.C.2.3	HARM PWR		SPEC ANA		dBm
23.C.2.4	FUND-HARM	-90	FUND-HARM	-60	dBc
23.C.3	5 kHz				
23.C.3.1	FUND PWR	-2.00	SPEC ANA	NONE	dBm
23.C.3.2	WORST HARM		2 or 3		nd/rd
23.C.3.3	HARM PWR		SPEC ANA		dBm
23.C.3.4	FUND-HARM	-90	FUND-HARM	-60	dBc
23.C.4	10 kHz				
23.C.4.1	FUND PWR	-2.00	SPEC ANA	NONE	dBm
23.C.4.2	WORST HARM		2 or 3		nd/rd
23.C.4.3	HARM PWR		SPEC ANA		dBm
23.C.4.4	FUND-HARM	-90	FUND-HARM	-60	dBc
23.C.5	20 kHz				
23.C.5.1	FUND PWR	-2.00	SPEC ANA	NONE	dBm
23.C.5.2	WORST HARM		2 or 3		nd/rd
23.C.5.3	HARM PWR		SPEC ANA		dBm
23.C.5.4	FUND-HARM	-90	FUND-HARM	-50	dBc
23.C.6	50 kHz				
23.C.6.1	FUND PWR	-2.00	SPEC ANA	NONE	dBm
23.C.6.2	WORST HARM		2 or 3		nd/rd
23.C.6.3	HARM PWR		SPEC ANA		dBm
23.C.6.4	FUND-HARM	-90	FUND-HARM	-50	dBc
23.C.7	100 kHz				
23.C.7.1	FUND PWR	-2.00	SPEC ANA	NONE	dBm
23.C.7.2	WORST HARM		2 or 3		nd/rd
23.C.7.3	HARM PWR		SPEC ANA		dBm
23.C.7.4	FUND-HARM	-90	FUND-HARM	-50	dBc

TEST 23: SINE DISTORTION

Purpose — Verify that each channel's sine wave meets purity specifications by measuring the power levels of the 2nd and 3rd harmonics with reference to the fundamental frequency.

Equipment — HP8568A spectrum analyzer, attenuator (50 ohms, 5X, 2W).

Comment — Calibrate the spectrum analyzer before running this test. The spectrum analyzer will store its correction factors. You will enable these correction factors during this test.

Setup

Test 23.C.1.X to 23.C.7.X, (frequency range 1kHz to 50kHz)

650: RESET PARAMS, FREQUENCY (per tests 23.C.1-6), CHANNEL (1-4), AMPLITUDE 2.828, OUTPUT ONFIFTY, EXECUTE.
Connect 650 Channel (1-4) Func Out to spectrum analyzer left input through the 50 ohm, 5X, 2W attenuator.

SA: Measure Fundamental PRESET, ATTENUATION 30dB, REFERENCE LEVEL 0dB, MIXER LEVEL (shift ',') -30dB, LEFT INPUT, CORRECTION FACTORS ON, CENTER FREQUENCY (per tests 23.C.1-13), FREQUENCY SPAN (per tests 23.C.1-13), MARKER NORMAL, PEAK SEARCH.

Measure Harmonics CENTER FREQUENCY (per tests 23.C.1-13) * HARMONIC (2 or 3), FREQUENCY SPAN (per tests 23.C.1-13) * HARMONIC (2 or 3) * 0.1, MARKER NORMAL, PEAK SEARCH.

Test 23.C.8.X to 23.C.13.X, (frequency range 100KHz to 2MHz)

650: RESET PARAMS, FREQUENCY (per tests 23.C.7-13), CHANNEL (1-4), AMPLITUDE 2.828, OUTPUT ONFIFTY, EXECUTE.
Connect 650 Channel (1-4) Func Out to spectrum analyzer right input.

SA: Measure Fundamental PRESET, ATTENUATION 40dB, REFERENCE LEVEL 20dB, MIXER LEVEL (shift ',') -30dB, RIGHT INPUT, CORRECTION FACTORS ON, CENTER FREQUENCY (per tests 23.C.1-13), FREQUENCY SPAN (per tests 23.C.1-13), MARKER NORMAL, PEAK SEARCH.

Measure Harmonics CENTER FREQUENCY (per tests 23.C.1-13) * HARMONIC (2 or 3), FREQUENCY SPAN (per tests 23.C.1-13) * HARMONIC (2 or 3) * 0.1, MARKER NORMAL, PEAK SEARCH.

Limits
≤10kHz: -60dBc
≤100kHz: -50dBc
≤2MHz: -40dBc

Results	Parameter	LOLIMIT	READING	HILIMIT	UNIT
23.C.8	200 kHz				
23.C.8.1	FUND PWR	9.00	SPEC ANA	NONE	dBm
23.C.8.2	WORST HARM		2 or 3		nd/rd
23.C.8.3	HARM PWR		SPEC ANA		dBm
23.C.8.4	FUND-HARM	-90	FUND-HARM	-40	dBc
23.C.9	500 kHz				
23.C.9.1	FUND PWR	9.00	SPEC ANA	NONE	dBm
23.C.9.2	WORST HARM		2 or 3		nd/rd
23.C.9.3	HARM PWR		SPEC ANA		dBm
23.C.9.4	FUND-HARM	-90	FUND-HARM	-40	dBc
23.C.10	1.0 MHz				
23.C.10.1	FUND PWR	9.00	SPEC ANA	NONE	dBm
23.C.10.2	WORST HARM		2 or 3		nd/rd
23.C.10.3	HARM PWR		SPEC ANA		dBm
23.C.10.4	FUND-HARM	-90	FUND-HARM	-40	dBc
23.C.11	1.2 MHz				
23.C.11.1	FUND PWR	9.00	SPEC ANA	NONE	dBm
23.C.11.2	WORST HARM		2 or 3		nd/rd
23.C.11.3	HARM PWR		SPEC ANA		dBm
23.C.11.4	FUND-HARM	-90	FUND-HARM	-40	dBc
23.C.12	1.5 MHz				
23.C.12.1	FUND PWR	9.00	SPEC ANA	NONE	dBm
23.C.12.2	WORST HARM		2 or 3		nd/rd
23.C.12.3	HARM PWR		SPEC ANA		dBm
23.C.12.4	FUND-HARM	-90	FUND-HARM	-40	dBc
23.C.13	2.0 MHz				
23.C.13.1	FUND PWR	9.00	SPEC ANA	NONE	dBm
23.C.13.2	WORST HARM		2 or 3		nd/rd
23.C.13.3	HARM PWR		SPEC ANA		dBm
23.C.13.4	FUND-HARM	-90	FUND-HARM	-40	dBc

TEST 24: SPURIOUS LEVEL

Purpose - Verify that the worst-case spur of each channel falls below the specified limit.

Equipment HP8568A spectrum analyzer

Comment The 650 could produce absolutely pure sine waves if spurious frequencies (called spurs) did not mix with and distort the main frequency. Test 24 finds the frequency and measures the amplitude of each spur to make sure none can cause significant distortion.

Test 24.C.1 looks for unexpected spurs across the band 0.10MHz to 2.75MHz. Test 24.C.2 looks for a likely spur at 0.909MHz (caused by a specific hardware defect). Test 24.C.3 looks for a likely spur at 10MHz (caused by leakage of the 10MHz reference clock).

Each test (Band, 0.909MHz, and 10MHz) first measures the level of the fundamental frequency, then measures the level of the spur, then calculates the separation between the two levels. The level of the spur must fall at least -50dBc (dB referenced to carrier) below the level of the fundamental frequency.

Setup All Tests

SA: Before running this test, calibrate the spectrum analyzer and enable the correction factors.

Band Test TEST 24.C.1: BAND TEST

650: RESET, FREQUENCY 1.5E6, CHANNEL (1-4), AMPLITUDE 2.828, OUTPUT ONFIFTY, EXECUTE.
Connect 650 Channel (1-4) Func Out to spectrum analyzer right input.

SA: PRESET, REFERENCE LEVEL 20dB.

Test 24.C.1.1: Measure Fundamental Power (FUND PWR)

SA: CENTER FREQUENCY 1.5MHz, FREQUENCY SPAN 2.5MHz, MARKER NORMAL, PEAK SEARCH ON.

Test 24.C.1.2 (Step 1): Search 0.10MHz-1.40MHz for Worst-Case Spur

SA: CENTER FREQUENCY 0.75MHz, FREQUENCY SPAN 1.3MHz, MAX HOLD ON (allow 8 seconds minimum to construct worst-case spur), PEAK SEARCH ON (read spur power level), MARKER FREQUENCY (read spur frequency).

Test 24.C.1.2 (Step 2): Search 1.60MHz-2.75MHz for Worst-Case Spur

SA: CENTER FREQUENCY 2.175MHz, FREQUENCY SPAN 1.15MHz, MAX HOLD ON (allow 8 seconds minimum to construct worst-case spur), PEAK SEARCH ON (read spur power level), MARKER FREQUENCY (read spur frequency).

Test 24.C.1.2 (Step 3): Report Worst-Case Spur (SPUR LVL @ ##MHz)

Examine the spurs from part A and B above, select the worst one, and report it as follows: SPUR LVL @ ##MHz: -##.#dBm.

Limits FUND/SPUR HI LIMIT: -50dBc

Results	PARAMETER	LOLIMIT	READING	HILIMIT	UNIT
24.C.1	FREQ: 1.5 MHz				
24.C.1.X	FUND PWR	12.0	SPEC ANA		dBm
24.C.1.X	SPUR LVL @ ##MHz		SPEC ANA		dBm
24.C.1.X	FUND/SPUR		CALC	-50	dBc
24.C.2	FREQ: 1.818181818 MHz				
24.C.2.X	FUND PWR	12.0	SPEC ANA		dBm
24.C.2.X	SPUR LVL @ 0.909MHz		SPEC ANA		dBm
24.C.2.X	FUND/SPUR		CALC	-50	dBc
24.C.3	FREQ: 2.0 MHz				
24.C.3.X	FUND PWR	12.0	SPEC ANA		dBm
24.C.3.X	SPUR LVL @ 10MHz		SPEC ANA		dBm
24.C.3.X	FUND/SPUR		CALC	-50	dBc

Test 24.C.1.3: Calculate FUND/SPUR Separation

Calculate the separation between fundamental power (FUND PWR) and the worst-case spur (SPUR LVL):

FUND/SPUR = SPUR LVL - FUND PWR

Example: If FUND PWR = 13.7dBm and SPUR LVL = -46.8dBm, then FUND/SPUR = -46.8dBm - 13.7dBm = -60.5dBc. The worst-case spur therefore lies -60.5dBc below the main frequency.

0.909MHz Test

TEST 24.C.2: 0.909MHz SPUR TEST

650: RESET, FREQUENCY 1.8181818MHz, CHANNEL (1-4), AMPLITUDE 2.828, OUTPUT ONFIFTY, EXECUTE.
Connect 650 Channel (1-4) Func Out to spectrum analyzer right input.

SA: PRESET, REFERENCE LEVEL 20dB.

Test 24.C.2.1: Measure Fundamental Power (FUND PWR)

SA: CENTER FREQUENCY 1.8181818 MHz, FREQUENCY SPAN 2MHz, NORMAL MARKER ON, PEAK SEARCH ON.

Test 24.C.2.2: Measure Spur Level (SPUR LVL @ 0.909MHz)

SA: CENTER FREQUENCY 0.909090909MHz, FREQUENCY SPAN 100kHz, MAX HOLD ON (allow 5 seconds minimum to construct worst-case spur), PEAK SEARCH ON.

Test 24.C.2.3: Calculate FUND/SPUR Separation

Calculate the separation between fundamental power (FUND PWR) and the spur level (SPUR LVL):

FUND/SPUR = SPUR LVL - FUND PWR

10MHz Test

TEST 24.C.3: 10MHz SPUR TEST

650: RESET, FREQUENCY 2MHz, CHANNEL (1-4), AMPLITUDE 2.828, OUTPUT ONFIFTY, EXECUTE.
Connect 650 Channel (1-4) Func Out to spectrum analyzer right input.

SA: PRESET, REFERENCE LEVEL 20dB.

Test 24.C.3.1: Measure Fundamental Power (FUND PWR)

SA: CENTER FREQUENCY 2 MHz, FREQUENCY SPAN 100kHz, NORMAL MARKER ON, PEAK SEARCH.

Test 24.C.3.2: Measure Spur Level (SPUR LVL @ 10MHz)

CENTER FREQUENCY 10MHz, FREQUENCY SPAN 100kHz, MAX HOLD ON (allow 5 seconds minimum to construct worst-case spur), PEAK SEARCH ON.

Test 24.C.3.3: Calculate FUND/SPUR Separation

Calculate the separation between fundamental power (FUND PWR) and the spur level (SPUR LVL):

FUND/SPUR = SPUR LVL - FUND PWR

TEST 25: RISE/FALL TIME AND ABERRATIONS

Purpose Verify that each channel's square wave rise/fall times and positive/negative aberrations meet specifications.

Equipment Oscilloscope with plug-ins, attenuator (50 ohm, 10X, 12.5W minimum), termination (50 ohm, 2W, 2%).

Setup

Test 25.C.1

650: RESET, FREQUENCY 1E6, CHANNEL (1-4), FUNCTION SQUARE, AMPLITUDE 10, OUTPUT ONFIFTY, EXECUTE.
Connect 650 Channel (1-4) Func Out to oscilloscope vertical amplifier channel 1 input. Use a 50 ohm, 10X, 12.5W (minimum) attenuator in series with a 50 ohm, 2W, 2% termination.

Scope: 7A16P Vertical Channel 1, Coupling DC, Volts/Div 0.2. 7B90P Horizontal Slope '-', Trigger Mode p-p, Trigger Source Internal, Trigger Coupling DC, Time/Division 200nsec.

Test 25.C.2

650: RESET, FREQUENCY 1E6, CHANNEL (1-4), FUNCTION SQUARE, AMPLITUDE 25, OUTPUT ONFIFTY, EXECUTE.
Connect 650 Channel (1-4) Func Out to oscilloscope vertical amplifier channel 1 input. Use a 50 ohm, 10X, 12.5W (minimum) attenuator in series with a 50 ohm, 2W, 2% termination.

Scope: 7A16P Vertical Channel 1, Coupling DC, Volts/Div 0.5. 7B90P Horizontal Slope '-', Trigger Mode p-p, Trigger Source Internal, Trigger Coupling DC, Time/Division 200nsec.

Limits

25.C.X.1	Risetime < 75nsec
25.C.X.2	Falltime < 75nsec
25.C.X.3	Pos.Aber < 5%
25.C.X.4	Neg Aber < 5%

Results

	AMPLITUDE	LOLIMIT	READING	HILIMIT	UNITS
25.C.1	10Vp-p				
25.C.1.1	Risetime	20	SCOPE	75	nsec
25.C.1.2	Falltime	20	SCOPE	75	nsec
25.C.1.3	Pos Aberr	0	SCOPE	5	%
25.C.1.4	Neg Aberr	0	SCOPE	5	%
25.C.2	25Vp-p				
25.C.2.1	Risetime	20	SCOPE	75	nsec
25.C.2.2	Falltime	20	SCOPE	75	nsec
25.C.2.3	Pos Aberr	0	SCOPE	5	%
25.C.2.4	Neg Aberr	0	SCOPE	5	%

TEST 26: SQUARE WAVE SYMMETRY (1KHz and 1MHz)

Purpose: Verify the duty cycle set-ability and accuracy of each channel's square wave.

Equipment: Counter, termination (50 ohm, 2W, 2%).

Comment: This test measures the period and pulse width of the square wave with the counter, then calculates DUTYCYCLE% from the following algorithm:

DUTYCYCLE% = (Positive Pulse Width/Period)*100%

Setup: CNTR: Function PERIOD for first reading, Function PULSE WIDTH for second reading.

650: RESET, FREQUENCY (per test 26.C.1-6), CHANNEL (1-4), FUNCTION SQUARE, AMPLITUDE 10, DUTYCYCLE (per test 26.C.1-6), OUTPUT ONFIFTY, EXECUTE.
Connect 650 Channel (1-4) Func Out to counter. Terminate with a 50 ohm, 2W, 2% termination.

Limits: DUTY SETTING ±3%, ±15nsec

	FREQ/DUTY	LOLIMIT	READING	HILIMIT	UNITS
26.C.1	1kHz, 20%	16.999	CALC	23.001	%
26.C.2	1kHz, 50%	46.999	CALC	53.001	%
26.C.3	1kHz, 80%	76.999	CALC	83.001	%
26.C.4	1MHz, 20%	15.500	CALC	24.500	%
26.C.5	1MHz, 50%	45.500	CALC	54.500	%
26.C.6	1MHz, 80%	75.500	CALC	84.500	%

TEST 27: AM INPUT

Purpose Verify that each channel's AM input operates and has the correct modulation drive levels.

Equipment DMM, power supply.

Comment The test applies an external DC level to the AM In connector of the test channel, then measures the ACvrms value of the sine wave at the Func Out connector.

Setup

DMM: FUNCTION VAcrms.
PS: Volts (per test 27.C.1-6)
650: RESET, CHANNEL (1-4), AMPLITUDE 0, OUTPUT ONZERO, EXECUTE. Connect 650 Channel (1-4) Func Out to DMM. Connect power supply to 650 Channel (1-4) AM In.

Limits ±15%

Results	AM In (Vdc)	LOLIMIT	READING	HILIMIT	UNITS
27.C.1	0	-0.23	DMM	0.23	Vrms
27.C.2	1	2.85	DMM	3.86	Vrms
27.C.3	2	6.01	DMM	8.13	Vrms
27.C.4	3	9.02	DMM	12.20	Vrms
27.C.5	4	12.02	DMM	16.26	Vrms
27.C.6	5	15.03	DMM	20.33	Vrms

TEST 28: SYNC OUT

Purpose - Verify that each channel's sync signal meets TTL level limits.

Equipment DMM, scope with plug-ins, termination (50 ohm, 2W, 2%).

Setup

Test 28.C.1.1

650: RESET, MODE TRIGGERED, CHANNEL (1-4), PHASE -90, EXECUTE. Connect the 650 channel (1-4) Sync Out to the DMM. Terminate with a 50 ohm, 2W, 2% termination.

DMM: FUNCTION Vdc

Test 28.C.1.2

650: RESET, MODE TRIGGERED, CHANNEL (1-4), PHASE +90, EXECUTE. Connect the 650 Channel (1-4) Sync Out to DMM. Terminate with a 50 ohm, 2W, 2% termination.

DMM: FUNCTION Vdc

Limits

28.C.1.1 -0.005Vdc < SYNC LO < +0.400Vdc

28.C.1.2 +2.4Vdc < SYNC HI < +5.0Vdc

	PARAMETER	LOLIMIT	READING	HILIMIT	UNIT
28.C.1.1	Sync Lo Level	-0.005	DMM	0.400	Vdc
28.C.1.2	Sync Hi Level	2.4	DMM	5.0	Vdc

TEST 29: MAIN GENERATOR MODE TEST

Purpose · Verify that the main generator modes operate correctly at a phase setting of 0°.

Equipment DMM, counter, signal source 271, termination (50 ohm, 2W, 2%).

Setup

Test 29.1
650: RESET, FREQUENCY 2E3, EXECUTE.
Connect 650 Channel 1 Sync Out to Counter. Terminate with 50 ohm, 2W, 2% termination.
CNTR: Function FREQUENCY

Test 29.2
DMM: Function ACrms
650: RESET, FREQUENCY 2E3, MODE TRIGGERED, CHANNEL 1, OUTPUT ONZERO, EXECUTE.
Connect 650 Channel 1 Func Out to DMM.

Test 29.3
650: RESET, FREQUENCY 2E3, MODE TRIGGERED, CHANNEL 1, OUTPUT ONZERO, EXECUTE.
Connect 650 Channel 1 Sync Out to Counter. Connect signal source 271 to Trig In. Terminate with a 50 ohm, 2W, 2% termination.
CNTR: Function FREQUENCY
271: RESET (sets frequency to 1kHz), FUNCTION SQUARE, OUTPUT ON, EXECUTE

Test 29.4
650: RESET, FREQUENCY 2E3, MODE SYNCGATE, EXECUTE.
Connect 650 Func Out to DMM.
DMM: Function VACrms

Test 29.5
650: RESET, FREQUENCY 2E3, MODE SYNCGATE, EXECUTE.
Connect 650 Channel 1 Sync Out to Counter. Connect signal source 271 to Trig In. Terminate with a 50 ohm, 2W, 2% termination.
CNTR: Function FREQUENCY.
271: RESET, FUNCTION DC, OFFSET 2, OUTPUT ON, EXECUTE.

Test 29.6
650: RESET, FREQUENCY 2E3, MODE SYNCGATE, EXECUTE.
Connect 650 Channel 1 Func Out to DMM. Connect Signal Source 271 to Trig In. Terminate with 50 ohm, 2W, 2% termination.
DMM: Function VAC rms
271: RESET, FUNCTION SINGLE PULSE, PULSE WIDTH 250 uSec, UPPER LEVEL 3, LOWER 0, OUTPUT ON, EXECUTE.

Test 29.7

650: RESET, FREQUENCY 2E3, MODE ASYNCGATE, EXECUTE
Connect 650 Channel 1 Func Out to DMM. Connect Signal Source 271 to Trig In. Terminate with 50 ohm, 2W, 2% termination.

DMM: Function VAC rms

271: RESET, FUNCTION SINGLE PULSE, PULSE WIDTH 250 uSec, UPPER LEVEL 3, LOWER 0, OUTPUT ON, EXECUTE.

Test 29.8

650: RESET, FREQUENCY 2E3, MODE BURST, CHANNEL 1, OUTPUT ONFIFTY, EXECUTE.
Connect 650 Channel 1 Func Out to Counter. Terminate with 50 ohm, 2W, 2% termination.

CNTR: Function TOTALIZE. Set trigger level to 1.5 Vdc.

Limits

29.1 2kHz ±5%
29.2 0Vac, -0, +0.10Vac
29.3 1kHz ±2%
29.4 0Vac, -0, +0.10Vac
29.5 1.768Vac ±1%
29.6 1.25Vac ±10%
29.7 0.884Vac ±10%
29.8 2 counts ±0 counts

Results	MODE	PARAMETERM	LOLIMIT	READING	HILIMIT	UNITS
29.1	CONT	FREQUENCY	1900	CNTR	2100	Hz
29.2	TRIG	QUIESCENT		DMM	0.1	Vacrms
29.3	TRIG	FREQUENCY	980	CNTR	1020	Hz
29.4	S-Gated	QUIESCENT		DMM	0.1	Vacrms
29.5	S-Gated	GATED	1.75	DMM	1.79	Vacrms
29.6	S-GATE	1 CYCLE	1.13	DMM	1.37	Vacrms
29.7	A-GATE	CYCLE/2	0.79	DMM	0.97	Vacrms
29.8	BURST	COUNT(2)	2	CNTR	2	EVENTS

TEST 30: BURST COUNT

Purpose Test the set-ability and accuracy of the burst counter at the maximum trigger frequency.

Equipment Counter, termination (50 ohm, 2W, 2%).

Setup

650: RESET, FREQUENCY 2E5, MODE BURST, BURST COUNT (per test 29.X), CHANNEL 1, FUNCTION SQUARE, PHASE 90, AMPLITUDE 10, OUTPUT ONFIFTY, EXECUTE.
Connect 650 Channel 1 Func Out to counter input. Terminate with 50 ohm, 2W, 2% termination.
Press the Manual Trigger key (or send a group execute trigger over the GPIB bus) to trigger the burst.

CNTR: FUNCTION TOTALIZE, TRIG LEVEL 1.5 Vdc

Procedure Trigger 650, wait for the burst to complete, then set counter to TOTALIZE STOP. Record reading and reset counter (clear reading).

Limits ±0 counts

Results	SETTING	READING	UNIT
30.1	1	1	EVENTS
30.2	2	2	EVENTS
30.3	4	4	EVENTS
30.4	8	8	EVENTS
30.5	16	16	EVENTS
30.6	32	32	EVENTS
30.7	64	64	EVENTS
30.8	128	128	EVENTS
30.9	256	256	EVENTS
30.10	512	512	EVENTS
30.11	1024	1024	EVENTS
30.12	2048	2048	EVENTS
30.13	4096	4096	EVENTS
30.14	8192	8192	EVENTS
30.15	16384	16384	EVENTS
30.16	32768	32768	EVENTS
30.17	65535	65535	EVENTS

TEST 31: EXTERNAL PHASE LOCK

Purpose - Verify that the 650 can phase lock to an external reference signal applied to Trig In.

Equipment Counter, signal source 178, termination (50 ohm, 2W, 2%).
Note: Step 3 requires a GPIB instrumentation computer.

Comment The 650 can phase lock to an external 40Hz to 2Mhz signal. The 650 first measures the signal's frequency, then selects the correct configuration for the PLL filter, then programs a corresponding output frequency. Part 1 of this test uses the GPIB command MONITORFREQ? to verify that the 650 can measure the reference signal frequency, part 2 verifies that the 650 can generate a phase-locked output signal, and part 3 verifies that the 650 will generate a display error message and an SRQ upon signal removal.

Setup

CNTR: FUNCTION FREQUENCY, TRIGGER LEVEL 1.5Vdc.
178: RESET, FREQUENCY (per test 31.X), FUNCTION SQUARE, AMPLITUDE 5, REAR FUNC OUT ON, EXECUTE.
650: RESET, MODE PHASELOCK, EXECUTE.
Connect signal source 178 rear FUNC OUT to Trig In. Connect 650 Channel 1 Sync Out to counter. Terminate with 50 ohm, 2W, 2% termination.
Configure the 650 SRQMASK to get an SRQ for phase lock loss.

Procedure

1) Set the frequency of the external signal (per test 31.X).
2) Wait 4 seconds for the 650 to lock to the external signal.
3) Read the measured frequency with the GPIB command MONITORFREQ?.
4) Measure the Sync Out frequency.
5) Remove the external signal.

Limits

31.C.1 Lock Time: <4sec
Monitor Frequency: REF FREQ ±3%

31.C.2 Frequency Accuracy: REF FREQ ±0.1%

31.C.3 Locked/Unlocked: Removing signal unlocks PLL.

Results	SETTING/SOURCE	LOLIMIT	READING	HILIMIT	UNIT
31.1.1	40Hz/MONITOR	38.800	CNTR	41.200	Hz
31.1.2	SYNC OUT	39.960	CNTR	40.040	Hz
31.1.3	PLL NO LOCK (EXT. SIGNAL REMOVED) PASS/FAIL				
31.2.1	475Hz/MONITOR	460.750	CNTR	489.250	Hz
31.2.2	SYNC OUT	474.530	CNTR	475.480	Hz
31.2.3	PLL NO LOCK (EXT. SIGNAL REMOVED) PASS/FAIL				
31.3.1	990Hz/MONITOR	960.300	CNTR	1019.700	Hz
31.3.2	SYNC OUT	989.010	CNTR	990.990	Hz
31.3.3	PLL NO LOCK (EXT. SIGNAL REMOVED) PASS/FAIL				

31.4.1	1.1kHz/MONITOR	1.067	CNTR	1.133	kHz
31.4.2	SYNC OUT	1.099	CNTR	1.101	kHz
31.4.3	PLL NO LOCK (EXT. SIGNAL REMOVED) PASS/FAIL				
31.5.1	4.4kHz/MONITOR	4.268	CNTR	4.532	kHz
31.5.2	SYNC OUT	4.396	CNTR	4.404	kHz
31.5.3	PLL NO LOCK (EXT. SIGNAL REMOVED) PASS/FAIL				
31.6.1	9.9kHz/MONITOR	9.603	CNTR	10.197	kHz
31.6.2	SYNC OUT	9.890	CNTR	9.910	kHz
31.6.3	PLL NO LOCK (EXT. SIGNAL REMOVED) PASS/FAIL				
31.7.1	10.1kHz/MONITOR	9.797	CNTR	10.403	kHz
31.7.2	SYNC OUT	10.090	CNTR	10.110	kHz
31.7.3	PLL NO LOCK (EXT. SIGNAL REMOVED) PASS/FAIL				
31.8.1	44.9kHz/MONITOR	43.553	CNTR	46.247	kHz
31.8.2	SYNC OUT	44.855	CNTR	44.945	kHz
31.8.3	PLL NO LOCK (EXT. SIGNAL REMOVED) PASS/FAIL				
31.9.1	99.9kHz/MONITOR	96.903	CNTR	102.897	kHz
31.9.2	SYNC OUT	99.800	CNTR	100.000	kHz
31.9.3	PLL NO LOCK (EXT. SIGNAL REMOVED) PASS/FAIL				
31.10.1	100.1kHz/MONITOR	97.097	CNTR	103.103	kHz
31.10.2	SYNC OUT	100.000	CNTR	100.200	kHz
31.10.3	PLL NO LOCK (EXT. SIGNAL REMOVED) PASS/FAIL				
31.11.1	1MHz/MONITOR	0.970	CNTR	1.030	MHz
31.11.2	SYNC OUT	0.999	CNTR	1.001	MHz
31.11.3	PLL NO LOCK (EXT. SIGNAL REMOVED) PASS/FAIL				
31.12.1	2MHz/MONITOR	1.940	CNTR	2.060	MHz
31.12.2	SYNC OUT	1.998	CNTR	2.002	MHz
31.12.3	PLL NO LOCK (EXT. SIGNAL REMOVED) PASS/FAIL				

TEST 32: PROGRAMMABLE TRIGGER LEVEL

Purpose Verify operation and accuracy of the trigger level DAC circuitry.

Equipment DMM, power supply.

Comment The positive and negative trigger levels used by this test force the DAC trigger level circuitry to respond to complimentary binary bit patterns.

Because this test puts the 650 in the gated mode with no trigger voltage, the Func Out connector will not produce an output until the trigger voltage applied to the Trig In connector reaches the trigger level.

Procedure Use the power supply to apply a starting voltage of ±2.9V to the Trig In connector. Change the voltage slowly until the 650 produces an output waveform.

Setup

DMM: Function Vacrms.
PS: Volts, Current limiting ≤2ma.
650: RESET, MODE SYNCGATE, CHANNEL 1, AMPLITUDE 10, OUTPUT ONZERO, EXECUTE.
Connect power supply output to Trig In.
Connect 650 channel 1 Func Out to DMM.

Limits Trig level accuracy ±0.3V

Results

	T-LVL/SLOPE	LOLIMIT	READING	HILIMIT	UNITS
32.1	+3.4/POS	3.1	DMM	3.7	Vdc
32.2	-3.3/POS	-3.6	DMM	-3.0	Vdc
32.3	-3.3/NEG	-3.6	DMM	-3.0	Vdc

TEST 33: INTERNAL TRIGGER

Purpose Verify the frequency accuracy of the internal trigger synthesizer. The internal trigger can generate triggers from 2.5mHz to 200kHz.

Equipment Counter

Setup
650: RESET, FREQUENCY 200E3, MODE TRIGGERED, TRIGGERSOURCE INTERNAL, TRIGGERFREQ (per test 33.X), EXECUTE.
Connect 650 Channel 1 Sync Out to frequency counter.
CNTR: Function Frequency, Trigger Level 1.25V

Limits Frequency Accuracy: ±0.1%

	SETTING	LOLIMIT	READING	HILIMIT	UNIT
33.1	156.00 kHz	155.84400	CNTR	156.15600	kHz
33.2	78.10 kHz	78.02190	CNTR	78.17810	kHz
33.3	39.10 kHz	39.06090	CNTR	39.13910	kHz
33.4	19.50 kHz	19.48050	CNTR	19.51950	kHz
33.5	9.77 kHz	9.76023	CNTR	9.77977	kHz
33.6	4.88 kHz	4.87512	CNTR	4.88488	kHz
33.7	2.44 kHz	2.43756	CNTR	2.44244	kHz
33.8	1.22 kHz	1.21878	CNTR	1.22121	kHz
33.9	610.00 Hz	609.39000	CNTR	610.61000	Hz
33.10	305.00 Hz	304.69500	CNTR	305.30500	Hz
33.11	152.00 Hz	151.84800	CNTR	152.15200	Hz
33.12	76.30 Hz	76.22370	CNTR	76.37630	Hz
33.13	38.10 Hz	38.06190	CNTR	38.13810	Hz
33.14	19.10 Hz	19.08090	CNTR	19.11910	Hz
33.15	9.54 Hz	9.53046	CNTR	9.54954	Hz
33.16	4.77 Hz	4.76523	CNTR	4.77477	Hz
33.17	2.38 Hz	2.37762	CNTR	2.38238	Hz
33.18	1.19 Hz	1.18881	CNTR	1.19119	Hz

TEST 34: MARKER OUTPUT LEVEL

Purpose 1) Verify set-ability and accuracy of the marker frequency.
2) Verify that the Marker Out levels meet TTL requirements.
3) Indirectly verify proper operation of the phase marker.

Equipment DMM, termination (50 ohm, 2W, 2%).

Setup DMM: Function Vdc.
650: RESET, SWEEPMODE FREQ-CONT-RST, STARTFREQUENCY 1000, STOPFREQUENCY 1000, EXECUTE.
Connect 650 Marker Out to DMM. Terminate with 50 ohm, 2W, 2% termination.

Procedure Set [Sweep] FREQ MARKER to the frequencies given below in 34.1 and 34.2.

Limits FREQ ACCUR ±0.00001%
TTL LEVELS -0.005Vdc < LO < 0.400Vdc
2.4Vdc < HI < 5.0Vdc

Results	MARKER FREQ	LOLIMIT	READING	HILIMIT	UNITS
34.1	999.9999Hz	2.4	DMM	5.0	Vdc
34.2	1000.0001Hz	-0.005	DMM	0.400	Vdc

TEST 35: SWEEP TIME

Purpose Verify sweep time accuracy.

Equipment Counter, termination (50 ohm, 2W, 2%).

Setup CNTR: Function Period, Trigger Level 1.25 V, Execute.
650: RESET, SWEEPMODE FREQCONTRST, SWEEPTIME .01 SWEEPCOMP OFF, EXECUTE.
Connect 650 Marker Out to counter. Terminate with 50 ohm, 2W, 2% termination.

Limits ±0.1%, ±100usec.

Results	SETTING	LOLIMIT	READING	HILIMITS	UNIT
35.1	0.01sec	9.8900	CNTR	10.1100	msec

TEST 36: SWEEP MODES

Purpose Verify proper operation of the sweep modes associated with the Trig In, Marker Out, and Horiz Out connectors.

Equipment DMM, counter, power supply, signal source 178, termination (50 ohm, 2W, 2%).

Setup

Test 36.1 through 36.5
CNTR: Function Frequency
DMM: Function Vdc
650: RESET, CHANNEL 1, OUTPUT ONZERO, SWEEPMODE FREQTRIGHOLDRST, SWEEPTIME .01, SWEEPCOMP OFF, EXECUTE.
NOTE: You will need to press the Manual Trigger key or send a group execute trigger over the GPIB bus for tests 36.3 and 36.5.
--- Connect 650 Channel 1 Func Out to the counter and Horiz Out to the DMM.

Test 36.6 through 36.7
CNTR: Function Frequency
PS: DC volts (TTL levels per test 36.X)
650: RESET, CHANNEL 1, OUTPUT ONZERO, SWEEPMODE FREQSYNCFSK, SWEEPTIME .01, SWEEPCOMP OFF, EXECUTE.
Connect power supply output to 650 Trig In.
Connect 650 Channel 1 Func Out to counter.

Test 36.8 through 36.9
CNTR: Function Frequency
PS: DC volts (TTL levels per test 36.X)
650: RESET, CHANNEL 1, OUTPUT ONZERO, SWEEPMODE FREQASYNCFSK, SWEEPTIME .01, SWEEPCOMP OFF, EXECUTE.
Connect power supply output to 650 Trig In.
Connect 650 Channel 1 Func Out to Counter.

Test 36.10
CNTR: Function Frequency
178: RESET, FUNCTION SQUARE, AMPLITUDE 5, REAR FUNC OUT ON, EXECUTE.
650: RESET, CHANNEL 1, OUTPUT ONZERO, SWEEPMODE FREQSEQEXT, SWEEPTIME .01, SWEEPCOMP OFF, EXECUTE.
Connect Signal Source 178 Func Out to 650 Trig In.
Connect 650 Marker Out to counter and terminate with 50 ohm, 2W, 2% termination.

Test 36.11
CNTR: Function Frequency
650: RESET, CHANNEL 1, OUTPUT ONZERO, SWEEPMODE FREQSEQCONT, SEQUENCELIMIT 99, SWEEPTIME .1, SWEEPCOMP OFF, EXECUTE.
Connect 650 Marker Out to counter and terminate with 50 ohm, 2W, 2% termination.

Limits:		
	36.1	1kHz ±0.1%
	36.2	0Vdc ±0.1Vdc
	36.3	10kHz ±0.01%
	36.4	10Vdc ±5%
	36.5	1kHz ±0.1%
	36.6	1kHz ±1%
	36.7	10kHz ±1%
	36.8	1kHz ±1%
	36.9	10kHz ±1%
	36.10	1kHz ±0.1%
	36.11	990Hz ±0.1%

Results	SWPMODE/PARAMETER	LOLIMIT	READING	HILIMIT	UNIT
36.1	(5)/START FREQ	0.999	CNTR	1.001	kHz
36.2	(5)/HORZ OUT	-0.10	DMM	0.10	Vdc
36.3	(5)/STOP FREQ	9.999	CNTR	10.001	kHz
36.4	(5)/HORZ OUT	9.50	DMM	10.50	Vdc
36.5	(5)/START FREQ	0.999	CNTR	1.001	kHz
36.6	(7)/SYNC FSK (TTL LO @ TRIG IN)	0.990	CNTR	1.010	kHz
36.7	(7)/SYNC FSK (TTL HI @ TRIG IN)	9.900	CNTR	10.100	kHz
36.8	(8)/ASYNC FSK (TTL LO @ TRIG IN)	0.990	CNTR	1.010	kHz
36.9	(8)/ASYNC FSK (TTL HI @ TRIG IN)	9.900	CNTR	10.100	kHz
36.10	(9)/MARKER FREQ (TRIG FREQ: 1kHZ)	0.999	CNTR	1.001	kHz
36.11	(10)/MARKER FREQ	0.989	CNTR	0.991	kHz

TEST 37: FM/PM INPUT

Purpose Verify that an external dc voltage source can frequency modulate the 650. (This test indirectly verifies operation of phase modulation.)

Equipment Counter, power supply, termination (50 ohm, 2W, 2%).

Comment A modulation voltage of -1V to +1V will fully modulate the output signal between the programmed start and stop frequency values. Pressing Reset PARAMS sets the start frequency to 1kHz and the stop frequency to 10kHz. This test uses modulation voltages of ±0.96Vdc (instead of ±1.00Vdc) to verify that modulation of the output signal does not peak before ±1.00Vdc.

Setup

CNTR: Function Frequency
PS: Volts (per test 37.X), current limiting ≤2ma.
650: RESET, CHANNEL 1 OUTPUT ONFIFTY, SWEEPMODE BOTHEXTMOD, EXECUTE.
Connect 650 Channel 1 Func Out to counter and terminate with 50 ohm, 2W, 2% termination.
Connect power supply output to 650 FM/PM In.

Limits

START VOLTAGE	-0.961Vdc ±5%
START FREQUENCY	1175Hz, ±216Hz
STOP VOLTAGE	+0.961Vdc ±5%
STOP FREQUENCY	9825Hz, ±216Hz

Results

	FM/PM In	LOLIMIT	READING	HILIMITS	UNIT
37.1	-0.961Vdc	0.959	COUNTER	1.391	kHZ
37.2	+0.961Vdc	9.609	COUNTER	10.041	kHZ

TEST 38: HOLD IN

Purpose. Verify that a TTL signal applied to the Hold In connector can control frequency sweep and waveform output.

Equipment DMM, counter, power supply, termination (50 ohm, 2W, 2%).

Procedure Testing frequency sweep hold requires the following timing control:

1) Set the 650 sweep time to 2 seconds
2) Trigger the sweep
3) Wait one second
4) Make the power supply deliver a TTL low to Hold In
5) Measure the CH1 Sync Out frequency
6) Verify that the sweep has reached 50% of the range programmed

Testing waveform hold requires the following timing control:

1) Set the 650 frequency to 0.5 Hz
2) Set the output waveform to a RAMP with 10V amplitude
3) Trigger the output
4) Wait one second
5) Make the power supply deliver a TTL low to Hold In
6) Measure the CH1 Func Out voltage
7) Verify that the ramp has reached 50% of the 10V amplitude

Setup

Test 38.1

CNTR: Function Frequency

650: RESET, SWEEPMODE FREQTRIGHOLDRST, SWEEPTIME 2, TRIGGERSOURCE EXTERNAL, EXECUTE.
Connect 650 CH1 Sync Out to counter and terminate with 50 ohm, 2W, 2% termination.
Connect power supply output to Hold In.

Test 38.2

DMM: Function Vdc

650: RESET, FREQUENCY 0.5, MODE TRIGGERED, HOLDINPUT WAVEFORM, CHANNEL 1, FUNCTION RAMP, AMPLITUDE 10, OUTPUT ONZERO, EXECUTE.
Connect 650 CH1 Func Out to DMM.
Connect power supply output to Hold In.

Limits

38.1	5.50kHz ±10%
38.2	5.00Vdc ±10%

Results

	SETTING	LOLIMIT	READING	HILIMIT	UNIT
38.1	HOLD SWEEP	4.95	CNTR	6.05	kHz
38.2	HOLD RAMP	4.50	DMM	5.50	Vdc

TEST 39: STORED SETTINGS

Purpose Verify that the 650 can store and recall setups and that the memory backup battery works. This battery protects the stored setups and auto calibration data against power loss.

Equipment None.

Comment A setup includes all the operating settings of the Main, Channel, Sweep, and Trigger keys, but not those of the GPIB or Utility keys.

When the 650 stores a setup, it also generates and stores a check sum with the setup. Then, when the operator or a GPIB computer recalls the setup, the 650 generates a new check sum and compares it to the stored check sum. If the sums differ, the 650 generates a screen error message and (if the SRQMASK equals 7) an SRQ.

Procedure For the automated factory test, the instrumentation computer sets the SRQMASK to 7, sends a command string of 25 identical setups, turns the power off/on, then recalls all 25 setups. The setup stored in all 25 locations consists of [Reset] PARAMS plus [Main] MODE TRIG.

For bench testing, use this procedure to store and recall setups:

STORE
1) Give the 650 a setup.
2) Press Stored Settings STORE.
2) Key in a storage location number.
4) Press Execute to store the setup.

RECALL
1) Press Stored Settings RECALL.
2) Key in storage location number.
3) Press Execute to recall setup.

Store from 1 to 25 setups, turn the power off/on, then recall each setup. If the front panel displays no error messages, then the stored setups and the battery work.

Setup 650: Storing: RESET, MODE TRIGGERED, STORESETTING (1-25), EXECUTE.
Recalling: RESET, SRQMASK 7, MODE TRIGGERED, RECALLSTORESETTING (1-25), EXECUTE.
Connect test system GPIB cable to 650.

Limits Store and recall 25 setups with no errors.

TEST 40: SELF DIAGNOSTICS

Purpose Verify that self test can test the 650 circuits and that none have defects.

Equipment None.

Setup Remove all rear-panel cables.

Procedure Press Utility TEST START.

Results Self test takes 2-4 minutes, depending on the number of channels in the 650. If it finds a defect, it will display an error message and stop. If if finds no defects, it will display PASSED ALL TESTS.

3.3 FACTORY PERFORMANCE VERIFICATION

Do you want Wavetek to run the complete performance verification for you?

We will:
1) Calibrate your 650
2) Run the complete performance verification procedure
3) Provide you with a printout of the test results

If you want factory calibration and test, follow this procedure:

1) Call us at (619) 279-2200 and ask for customer service. Our service representative will ask for your name, telephone number, company name, and equipment type. Tell the representative you want 650 calibration and customer data performance verification.

2) Pack and ship the 650. If possible, use the original packing material and boxes. If you use inadequate materials, you'll have to pay to repair any shipping damage because carriers won't pay claims on incorrectly packed equipment.

Performance Verification Data. Our automated test set will generate a report like the following for your 650. The letters UUT in the report refer to the 650 (unit under test).

MODEL 650 ACCEPTANCE

PROCESS STEP: CUSTOMER DATA
PRINTOUT CONTAINS: ALL DATA
TEST SPECIFICATIONS: PUBLISHED
UUT SERIAL #: 6370286
OPTIONS INSTALLED: NO OPTIONS
OPERATOR CALIB.#: 116
DATE: 02/04/87

4.0 SOFTWARE VERSION CHECK

4.1 U.U.T. VERSION RESPONSE: WAVETEK MODEL 650 (V2.1)

5.0 QUICK FUNCTIONAL CHECK

5.1 -- CHANNEL 1

	PARAMETER	LOLIMIT	READING	HILIMIT	UNIT	STATUS
5.1.1	Sync FREQ	990	1000.0	1010	Hz	PASS
5.1.2	Sine AMPL	1.750	1.7712	1.785	Vrms	PASS
5.1.3	Sine OFST	-.150	-.0011	.150	Vdc	PASS

5.2 CHANNEL 2

5.2.1	Sync FREQ	990	1000.0	1010	Hz	PASS
5.2.2	Sine AMPL	1.750	1.7707	1.785	Vrms	PASS
5.2.3	Sine OFST	-.150	-.0007	.150	Vdc	PASS

6.0 QUICK CAL (3.5Vacrms) CHECK

	PARAMETER	LOLIMIT	READING	HILIMIT	UNIT	STATUS
6.1	3.500Vrms	3.4825	3.50081	3.5175	Vrms	PASS

7.0 REFERENCE INPUT / OUTPUT

	PARAMETER	LOLIMIT	READING	HILIMIT	UNIT	STATUS
	(REFIN)		(REFOUT)			
7.1	NO INPUT	9999950	10000023	10000050	Hz	PASS
7.2	9900000	9899951	9900000	9900050	Hz	PASS
7.3	10100000	10099950	10100000	10100051	Hz	PASS
7.4	TTL HI	2.4	2.51	5.0	Vdc	PASS
7.5	TTL LO	.0	.23	.4	Vdc	PASS

8.0 INTERNAL VOLTAGE REFERENCE (2.048 Vdc)

	PARAMETER	LOLIMIT	READING	HILIMIT	UNIT	STATUS
8.1	2.04vdc	2.020	2.0449	2.060	vdc	PASS

11.0 OUTPUT ON/OFF; 0/50 OHM IMPEDANCE

11.1 CHANNEL 1

	PARAMETER	LOLIMIT	READING	HILIMIT	UNIT	STATUS
11.1.1	Z=0,OUTPUT ON (LOAD= 50ohm)	.879	.8837	.888	Vrms	PASS
11.1.2	Z=50,OUTPUT ON (LOAD= 50ohm)	.879	.8848	.888	Vrms	PASS
11.1.3	OUTPUT OFF	.000	.0010	.010	Vrms	PASS
11.1.4	Z=0,OUTPUT ON (NO LOAD)	.879	.8862	.888	Vrms	PASS
11.1.5	Z=50,OUTPUT ON (NO LOAD)	1.758	1.7705	1.778	Vrms	PASS

11.2 CHANNEL 2

	PARAMETER	LOLIMIT	READING	HILIMIT	UNIT	STATUS
11.2.1	Z=0,OUTPUT ON (LOAD= 50ohm)	.879	.8828	.888	Vrms	PASS
11.2.2	Z=50,OUTPUT ON (LOAD= 50ohm)	.879	.8830	.888	Vrms	PASS
11.2.3	OUTPUT OFF	.000	.0010	.010	Vrms	PASS
11.2.4	Z=0,OUTPUT ON (NO LOAD)	.879	.8851	.888	Vrms	PASS
11.2.5	Z=50,OUTPUT ON (NO LOAD)	1.758	1.7701	1.778	Vrms	PASS

12.0 FUNCTION CHECK AT 600Hz, 10Vp-p

12.1 CHANNEL 1

	PARAMETER	LOLIMIT	READING	HILIMIT	UNIT	STATUS
12.1.1.1	SINE 3.536	3.516	3.5366	3.556	Vrms	PASS
12.1.1.2	OFFSET	-.15	.015	.15	Vdc	PASS
12.1.2.1	TRIANGLE 2.886	2.870	2.8880	2.902	Vrms	PASS
12.1.2.2	OFFSET	-.15	.003	.15	Vdc	PASS
12.1.3.1	SQUARE 5	4.973	5.0000	5.027	Vrms	PASS
12.1.3.2	OFFSET	-.15	.071	.15	Vdc	PASS
12.1.4.1	RAMP 2.886	2.870	2.8879	2.902	Vrms	PASS
12.1.4.2	OFFSET	-.15	.004	.15	Vdc	PASS
12.1.5	DC 0	-.010	-.0007	.010	Vdc	PASS

12.2 CHANNEL 2

12.2.1.1	SINE 3.536	3.516	3.5318	3.556	Vrms	PASS
12.2.1.2	OFFSET	-.15	.014	.15	Vdc	PASS
12.2.2.1	TRIANGLE 2.886	2.870	2.8842	2.902	Vrms	PASS
12.2.2.2	OFFSET	-.15	.001	.15	Vdc	PASS
12.2.3.1	SQUARE 5	4.973	4.9873	5.027	Vrms	PASS
12.2.3.2	OFFSET	-.15	.024	.15	Vdc	PASS
12.2.4.1	RAMP 2.886	2.870	2.8841	2.902	Vrms	PASS
12.2.4.2	OFFSET	-.15	.003	.15	Vdc	PASS
12.2.5	DC 0	-.010	-.0014	.010	Vdc	PASS

13.0 SINE AMPLITUDE & OFFSET ACCURACY

13.1 CHANNEL 1

	PARAMETER	LOLIMIT	READING	HILIMIT	UNIT	STATUS
	(Vp-p : Vrms)					
13.1.1.1	(2.5),(.884)	.880	.8864	.888	Vrms	PASS
13.1.1.2	OFFSET 0	-.15	.000	.15	Vdc	PASS
13.1.2.1	(5),(1.768)	1.759	1.7715	1.777	Vrms	PASS
13.1.2.2	OFFSET 0	-.15	.004	.15	Vdc	PASS
13.1.3.1	(7.5),(2.652)	2.639	2.6553	2.665	Vrms	PASS
13.1.3.2	OFFSET 0	-.15	.007	.15	Vdc	PASS
13.1.4.1	(10),(3.536)	3.518	3.5402	3.554	Vrms	PASS
13.1.4.2	OFFSET 0	-.15	.011	.15	Vdc	PASS
13.1.5.1	(12.5),(4.419)	4.397	4.4238	4.441	Vrms	PASS
13.1.5.2	OFFSET 0	-.15	.013	.15	Vdc	PASS
13.1.6.1	(15),(5.303)	5.276	5.3070	5.330	Vrms	PASS
13.1.6.2	OFFSET 0	-.15	.017	.15	Vdc	PASS
13.1.7.1	(17.5),(6.187)	6.156	6.1907	6.218	Vrms	PASS
13.1.7.2	OFFSET 0	-.15	.019	.15	Vdc	PASS
13.1.8.1	(20),(7.071)	7.036	7.0754	7.106	Vrms	PASS
13.1.8.2	OFFSET 0	-.15	.023	.15	Vdc	PASS
13.1.9.1	(22.5),(7.955)	7.915	7.9572	7.995	Vrms	PASS
13.1.9.2	OFFSET 0	-.15	.025	.15	Vdc	PASS
13.1.10.1	(25),(8.839)	8.795	8.8402	8.883	Vrms	PASS
13.1.10.2	OFFSET 0	-.15	.029	.15	Vdc	PASS

13.2 CHANNEL 2

13.2.1.1	(2.5),(.884)	.880	.8850	.888	Vrms	PASS
13.2.1.2	OFFSET 0	-.15	.001	.15	Vdc	PASS
13.2.2.1	(5),(1.768)	1.759	1.7709	1.777	Vrms	PASS
13.2.2.2	OFFSET 0	-.15	.004	.15	Vdc	PASS
13.2.3.1	(7.5),(2.652)	2.639	2.6553	2.665	Vrms	PASS
13.2.3.2	OFFSET 0	-.15	.007	.15	Vdc	PASS
13.2.4.1	(10),(3.536)	3.518	3.5420	3.554	Vrms	PASS
13.2.4.2	OFFSET 0	-.15	.008	.15	Vdc	PASS
13.2.5.1	(12.5),(4.419)	4.397	4.4246	4.441	Vrms	PASS
13.2.5.2	OFFSET 0	-.15	.012	.15	Vdc	PASS
13.2.6.1	(15),(5.303)	5.276	5.3078	5.330	Vrms	PASS
13.2.6.2	OFFSET 0	-.15	.014	.15	Vdc	PASS

13.2.7.1	(17.5),(6.187)	6.156	6.1921	6.218	Vrms	PASS
13.2.7.2	OFFSET 0	-.15	.017	.15	Vdc	PASS
13.2.8.1	(20),(7.071)	7.036	7.0782	7.106	Vrms	PASS
13.2.8.2	OFFSET 0	-.15	.019	.15	Vdc	PASS
13.2.9.1	(22.5),(7.955)	7.915	7.9604	7.995	Vrms	PASS
13.2.9.2	OFFSET 0	-.15	.023	.15	Vdc	PASS
13.2.10.1	(25),(8.839)	8.795	8.8437	8.883	Vrms	PASS
13.2.10.2	OFFSET 0	-.15	.025	.15	Vdc	PASS

14.0 SINEWAVE AMPLITUDE ACCURACY AT 50 Vp-p

14.1 CHANNEL 1

	PARAMETER	LOLIMIT	READING	HILIMIT	UNIT	STATUS
	(Vp-p : Vrms)					
14.1.1	(50),(17.678)	17.590	17.6290	17.766	Vrms	PASS

14.2 CHANNEL 2

14.2.1	(50),(17.678)	17.590	17.6320	17.766	Vrms	PASS

15.0 SQUARE AMPLITUDE & OFFSET ACCURACY

15.1 CHANNEL 1

	PARAMETER	LOLIMIT	READING	HILIMIT	UNIT	STATUS
15.1.1.1	AMPL 2.5	2.488	2.5064	2.513	Vp-p	PASS
15.1.1.2	OFFSET	-.15	-.004	.15	Vdc	PASS
15.1.2.1	AMPL 5	4.975	5.0089	5.025	Vp-p	PASS
15.1.2.2	OFFSET	-.15	-.006	.15	Vdc	PASS
15.1.3.1	AMPL 7.5	7.463	7.5088	7.538	Vp-p	PASS
15.1.3.2	OFFSET	-.15	-.008	.15	Vdc	PASS
15.1.4.1	AMPL 10	9.950	10.0069	10.050	Vp-p	PASS
15.1.4.2	OFFSET	-.15	-.009	.15	Vdc	PASS
15.1.5.1	AMPL 12.5	12.438	12.5073	12.563	Vp-p	PASS
15.1.5.2	OFFSET	-.15	-.010	.15	Vdc	PASS
15.1.6.1	AMPL 15	14.925	15.0052	15.075	Vp-p	PASS
15.1.6.2	OFFSET	-.15	-.011	.15	Vdc	PASS
15.1.7.1	AMPL 17.5	17.413	17.5061	17.588	Vp-p	PASS
15.1.7.2	OFFSET	-.15	-.012	.15	Vdc	PASS
15.1.8.1	AMPL 20	19.900	20.0082	20.100	Vp-p	PASS
15.1.8.2	OFFSET	-.15	-.013	.15	Vdc	PASS
15.1.9.1	AMPL 22.5	22.388	22.5034	22.613	Vp-p	PASS
15.1.9.2	OFFSET	-.15	-.012	.15	Vdc	PASS
15.1.10.1	AMPL 25	24.875	25.0027	25.125	Vp-p	PASS
15.1.10.2	OFFSET	-.15	-.011	.15	Vdc	PASS

15.2 CHANNEL 2

15.2.1.1	AMPL 2.5	2.488	2.5011	2.513	Vp-p	PASS
15.2.1.2	OFFSET	-.15	-.003	.15	Vdc	PASS

15.2.2.1	AMPL 5	4.975	5.0002	5.025	Vp-p	PASS
15.2.2.2	OFFSET	-.15	-.003	.15	Vdc	PASS
15.2.3.1	AMPL 7.5	7.463	7.4978	7.538	Vp-p	PASS
15.2.3.2	OFFSET	-.15	-.005	.15	Vdc	PASS
15.2.4.1	AMPL 10	9.950	9.9978	10.050	Vp-p	PASS
15.2.4.2	OFFSET	-.15	-.006	.15	Vdc	PASS
15.2.5.1	AMPL 12.5	12.438	12.4898	12.563	Vp-p	PASS
15.2.5.2	OFFSET	-.15	-.005	.15	Vdc	PASS
15.2.6.1	AMPL 15	14.925	14.9861	15.075	Vp-p	PASS
15.2.6.2	OFFSET	-.15	-.004	.15	Vdc	PASS
15.2.7.1	AMPL 17.5	17.413	17.4837	17.588	Vp-p	PASS
15.2.7.2	OFFSET	-.15	-.004	.15	Vdc	PASS
15.2.8.1	AMPL 20	19.900	19.9877	20.100	Vp-p	PASS
15.2.8.2	OFFSET	-.15	-.004	.15	Vdc	PASS
15.2.9.1	AMPL 22.5	22.388	22.4810	22.613	Vp-p	PASS
15.2.9.2	OFFSET	-.15	-.005	.15	Vdc	PASS
15.2.10.1	AMPL 25	24.875	24.9775	25.125	Vp-p	PASS
15.2.10.2	OFFSET	-.15	-.007	.15	Vdc	PASS

16.0 DC VOLTAGE ACCURACY, FUNCTION DC

16.1 CHANNEL 1

	PARAMETER	LOLIMIT	READING	HILIMIT	UNIT	STATUS
	(OFFSET Vdc)					
16.1.1	25.0	24.915	24.9772	25.085	Vdc	PASS
16.1.2	20.0	19.930	19.9817	20.070	Vdc	PASS
16.1.3	15.0	14.945	14.9857	15.055	Vdc	PASS
16.1.4	10.0	9.960	9.9907	10.040	Vdc	PASS
16.1.5	5.0	4.975	4.9946	5.025	Vdc	PASS
16.1.6	.0	-.010	-.0013	.010	Vdc	PASS
16.1.7	-5.0	-5.025	-4.9976	-4.975	Vdc	PASS
16.1.8	-10.0	-10.040	-9.9945	-9.960	Vdc	PASS
16.1.9	-15.0	-15.055	-14.9898	-14.945	Vdc	PASS
16.1.10	-20.0	-20.070	-19.9860	-19.930	Vdc	PASS
16.1.11	-25.0	-25.085	-24.9829	-24.915	Vdc	PASS

16.2 CHANNEL 2

16.2.1	25.0	24.915	24.9792	25.085	Vdc	PASS
16.2.2	20.0	19.930	19.9828	20.070	Vdc	PASS
16.2.3	15.0	14.945	14.9876	15.055	Vdc	PASS
16.2.4	10.0	9.960	9.9907	10.040	Vdc	PASS
16.2.5	5.0	4.975	4.9946	5.025	Vdc	PASS
16.2.6	.0	-.010	-.0029	.010	Vdc	PASS
16.2.7	-5.0	-5.025	-5.0002	-4.975	Vdc	PASS
16.2.8	-10.0	-10.040	-9.9977	-9.960	Vdc	PASS
16.2.9	-15.0	-15.055	-14.9951	-14.945	Vdc	PASS
16.2.10	-20.0	-20.070	-19.9908	-19.930	Vdc	PASS
16.2.11	-25.0	-25.085	-24.9853	-24.915	Vdc	PASS

17.0 DC VOLTS TEST (+/-25 Vdc) TERMINATED INTO 50 ohms

17.1 CHANNEL 1

	PARAMETER	LOLIMIT	READING	HILIMIT	UNIT	STATUS
	(OFFSET Vdc)					
17.1.1	25.0	24.865	24.9058	25.135	Vdc	PASS
17.1.2	-25.0	-25.135	-24.9134	-24.865	Vdc	PASS

17.2 CHANNEL 2

17.2.1	25.0	24.865	24.9189	25.135	Vdc	PASS
17.2.2	-25.0	-25.135	-24.9282	-24.865	Vdc	PASS

18.0 ATTENUATOR ACCURACY

18.1 CHANNEL 1

	PARAMETER	LOLIMIT	READING	HILIMIT	UNIT	STATUS
	(Vp-p,Vrms,db)					
18.1.1	(10,3.536,0)	3.516	3.5358	3.555	Vrms	PASS
18.1.2	(1,.3536,20)	.3498	.35334	.3574	Vrms	PASS
18.1.3	(.1,.0354,40)	.0332	.03535	.0376	Vrms	PASS

18.2 CHANNEL 2

18.2.1	(10,3.536,0)	3.516	3.5286	3.555	Vrms	PASS
18.2.2	(1,.3536,20)	.3498	.35307	.3574	Vrms	PASS
18.2.3	(.1,.0354,40)	.0332	.03531	.0376	Vrms	PASS

21.0 PHASE CHECK

CHANNEL 1 PHASE MEASURED IN REFERENCE TO CHANNEL 2

	FREQ SETTING	LOLIMIT	READING	HILIMIT	UNIT	STATUS
	SYSTEM_SCALAR		1.3676	1.500		PASS
21.1.1	500.000 Hz	-.0050	.0009	.0050	Deg	PASS
21.1.2	1.000 kHz	-.0050	.0011	.0050	Deg	PASS
21.1.3	2.000 kHz	-.0300	.0007	.0300	Deg	PASS
21.1.4	5.000 kHz	-.0300	.0036	.0300	Deg	PASS
21.1.5	10.000 kHz	-.1000	.0069	.1000	Deg	PASS
21.1.6	20.000 kHz	-.1000	.0038	.1000	Deg	PASS
21.1.7	50.000 kHz	-.1000	.0025	.1000	Deg	PASS
21.1.8	100.000 kHz	-.1000	.0077	.1000	Deg	PASS
21.1.9	200.000 kHz	-.5000	.0136	.5000	Deg	PASS
21.1.10	500.000 kHz	-.5000	.0386	.5000	Deg	PASS
21.1.11	1.000 MHz	-2.0000	-.0155	2.0000	Deg	PASS
21.1.12	1.500 MHz	-2.0000	.0956	2.0000	Deg	PASS
21.1.13	2.000 MHz	-2.0000	.1218	2.0000	Deg	PASS

QUICK CAL PHASE ACCURACY TEST

21.1.14	1.000 MHz	-1.0000	.0460	1.0000	Deg	PASS
21.1.15	1.500 MHz	-1.0000	.0264	1.0000	Deg	PASS
21.1.16	2.000 MHz	-1.0000	.0522	1.0000	Deg	PASS

CHANNEL 2 PHASE MEASURED IN REFERENCE TO CHANNEL 1

	FREQ SETTING	LOLIMIT	READING	HILIMIT	UNIT	STATUS
	SYSTEM_SCALAR		1.3671	1.500		PASS
21.2.1	500.000 Hz	-.0050	-.0012	.0050	Deg	PASS
21.2.2	1.000 kHz	-.0050	-.0010	.0050	Deg	PASS
21.2.3	2.000 kHz	-.0300	-.0007	.0300	Deg	PASS
21.2.4	5.000 kHz	-.0300	-.0031	.0300	Deg	PASS
21.2.5	10.000 kHz	-.1000	-.0060	.1000	Deg	PASS
21.2.6	20.000 kHz	-.1000	-.0015	.1000	Deg	PASS
21.2.7	50.000 kHz	-.1000	.0072	.1000	Deg	PASS
21.2.8	100.000 kHz	-.1000	-.0009	.1000	Deg	PASS
21.2.9	200.000 kHz	-.5000	-.0142	.5000	Deg	PASS
21.2.10	500.000 kHz	-.5000	-.0295	.5000	Deg	PASS
21.2.11	1.000 MHz	-2.0000	.0021	2.0000	Deg	PASS
21.2.12	1.500 MHz	-2.0000	-.0973	2.0000	Deg	PASS
21.2.13	2.000 MHz	-2.0000	-.1356	2.0000	Deg	PASS

QUICK CAL PHASE ACCURACY TEST

21.2.14	1.000 MHz	-1.0000	.0648	1.0000	Deg	PASS
21.2.15	1.500 MHz	-1.0000	-.0686	1.0000	Deg	PASS
21.2.16	2.000 MHz	-1.0000	.0458	1.0000	Deg	PASS

22.0 FREQUENCY RESPONSE, SINE

22.1 CHANNEL 1

	FREQUENCY	LOLIMIT	READING	HILIMIT	UNIT	STATUS
22.1.1	10 Hz	3.516	3.5392	3.556	Vrms	PASS
22.1.2	100 Hz	3.516	3.5394	3.556	Vrms	PASS
22.1.3	1000 Hz	3.516	3.5384	3.556	Vrms	PASS
22.1.4	5000 Hz	3.516	3.5389	3.556	Vrms	PASS
22.1.5	10000 Hz	3.516	3.5393	3.556	Vrms	PASS
22.1.6	20000 Hz	3.516	3.5395	3.556	Vrms	PASS

22.2 CHANNEL 2

22.2.1	10 Hz	3.516	3.5365	3.556	Vrms	PASS
22.2.2	100 Hz	3.516	3.5403	3.556	Vrms	PASS
22.2.3	1000 Hz	3.516	3.5393	3.556	Vrms	PASS
22.2.4	5000 Hz	3.516	3.5398	3.556	Vrms	PASS
22.2.5	10000 Hz	3.516	3.5402	3.556	Vrms	PASS
22.2.6	20000 Hz	3.516	3.5403	3.556	Vrms	PASS

23.0 SINE DISTORTION

23.1 CHANNEL 1

	PARAMETER	LOLIMIT	READING	HILIMIT	UNIT	STATUS
23.1.1	1 kHz					
23.1.1.1	FUND PWR	-2.00	-1.00	.00	dbm	PASS
23.1.1.2	WORST HARM		3.0		rd	
23.1.1.3	HARM PWR		-74.8		dbm	
23.1.1.4	FUND - HARM	-90	-73.8	-60	dbc	PASS
23.1.2	2 kHz					
23.1.2.1	FUND PWR	-2.00	-.80	.00	dbm	PASS
23.1.2.2	WORST HARM		3.0		rd	
23.1.2.3	HARM PWR		-74.6		dbm	
23.1.2.4	FUND - HARM	-90	-73.8	-60	dbc	PASS
23.1.3	5 kHz					
23.1.3.1	FUND PWR	-2.00	-.90	.00	dbm	PASS
23.1.3.2	WORST HARM		3.0		rd	
23.1.3.3	HARM PWR		-74.0		dbm	
23.1.3.4	FUND - HARM	-90	-73.1	-60	dbc	PASS
23.1.4	10 kHz					
23.1.4.1	FUND PWR	-2.00	-1.00	.00	dbm	PASS
23.1.4.2	WORST HARM		3.0		rd	
23.1.4.3	HARM PWR		-72.9		dbm	
23.1.4.4	FUND - HARM	-90	-71.9	-60	dbc	PASS
23.1.5	20 kHz					
23.1.5.1	FUND PWR	-2.00	-1.00	.00	dbm	PASS
23.1.5.2	WORST HARM		3.0		rd	
23.1.5.3	HARM PWR		-72.3		dbm	
23.1.5.4	FUND - HARM	-90	-71.3	-50	dbc	PASS
23.1.6	50 kHz					
23.1.6.1	FUND PWR	-2.00	-1.00	.00	dbm	PASS
23.1.6.2	WORST HARM		2.0		nd	
23.1.6.3	HARM PWR		-68.4		dbm	
23.1.6.4	FUND - HARM	-90	-67.4	-50	dbc	PASS
23.1.7	100 kHz					
23.1.7.1	FUND PWR	-2.00	-1.10	.00	dbm	PASS
23.1.7.2	WORST HARM		2.0		nd	
23.1.7.3	HARM PWR		-68.7		dbm	
23.1.7.4	FUND - HARM	-90	-67.6	-50	dbc	PASS
23.1.8	200 kHz					
23.1.8.1	FUND PWR	9.00	9.60	.00	dbm	PASS
23.1.8.2	WORST HARM		3.0		rd	
23.1.8.3	HARM PWR		-60.7		dbm	
23.1.8.4	FUND - HARM	-90	-70.3	-40	dbc	PASS
23.1.9	500 kHz					
23.1.9.1	FUND PWR	9.00	9.70	.00	dbm	PASS

23.1.9.2	WORST HARM		2.0		nd	
23.1.9.3	HARM PWR		-56.1		dbm	
23.1.9.4	FUND - HARM	-90	-65.8	-40	dbc	PASS
23.1.10	1 MHz					
23.1.10.1	FUND PWR	9.00	9.80	.00	dbm	PASS
23.1.10.2	WORST HARM		3.0		rd	
23.1.10.3	HARM PWR		-47.1		dbm	
23.1.10.4	FUND - HARM	-90	-56.9	-40	dbc	PASS
23.1.11	1.2 MHz					
23.1.11.1	FUND PWR	-2.00	10.10	.00	dbm	PASS
23.1.11.2	WORST HARM		3.0		rd	
23.1.11.3	HARM PWR		-46.0		dbm	
23.1.11.4	FUND - HARM	-90	-56.1	-40	dbc	PASS
23.1.12	1.5 MHz					
23.1.12.1	FUND PWR	-2.00	10.20	.00	dbm	PASS
23.1.12.2	WORST HARM		3.0		rd	
23.1.12.3	HARM PWR		-46.7		dbm	
23.1.12.4	FUND - HARM	-90	-56.9	-40	dbc	PASS
23.1.13	2 MHz					
23.1.13.1	FUND PWR	-2.00	8.90	.00	dbm	PASS
23.1.13.2	WORST HARM		3.0		rd	
23.1.13.3	HARM PWR		-47.7		dbm	
23.1.13.4	FUND - HARM	-90	-56.6	-40	dbc	PASS

23.2 CHANNEL 2

	PARAMETER	LOLIMIT	READING	HILIMIT	UNIT	STATUS
23.2.1	1 kHz					
23.2.1.1	FUND PWR	-2.00	-1.00	.00	dbm	PASS
23.2.1.2	WORST HARM		3.0		rd	
23.2.1.3	HARM PWR		-70.9		dbm	
23.2.1.4	FUND - HARM	-90	-69.9	-60	dbc	PASS
23.2.2	2 kHz					
23.2.2.1	FUND PWR	-2.00	-.80	.00	dbm	PASS
23.2.2.2	WORST HARM		3.0		rd	
23.2.2.3	HARM PWR		-71.0		dbm	
23.2.2.4	FUND - HARM	-90	-70.2	-60	dbc	PASS
23.2.3	5 kHz					
23.2.3.1	FUND PWR	-2.00	-.90	.00	dbm	PASS
23.2.3.2	WORST HARM		3.0		rd	
23.2.3.3	HARM PWR		-70.4		dbm	
23.2.3.4	FUND - HARM	-90	-69.5	-60	dbc	PASS
23.2.4	10 kHz					
23.2.4.1	FUND PWR	-2.00	-1.00	.00	dbm	PASS
23.2.4.2	WORST HARM		3.0		rd	
23.2.4.3	HARM PWR		-69.9		dbm	

23.2.4.4	FUND - HARM	-90	-68.9	-60	dbc	PASS
23.2.5	20 kHz					
23.2.5.1	FUND PWR	-2.00	-1.00	.00	dbm	PASS
23.2.5.2	WORST HARM		3.0		rd	
23.2.5.3	HARM PWR		-68.6		dbm	
23.2.5.4	FUND - HARM	-90	-67.6	-50	dbc	PASS
23.2.6	50 kHz					
23.2.6.1	FUND PWR	-2.00	-1.00	.00	dbm	PASS
23.2.6.2	WORST HARM		3.0		rd	
23.2.6.3	HARM PWR		-69.0		dbm	
23.2.6.4	FUND - HARM	-90	-68.0	-50	dbc	PASS
23.2.7	100 kHz					
23.2.7.1	FUND PWR	-2.00	-1.10	.00	dbm	PASS
23.2.7.2	WORST HARM		2.0		nd	
23.2.7.3	HARM PWR		-68.0		dbm	
23.2.7.4	FUND - HARM	-90	-66.9	-50	dbc	PASS
23.2.8	200 kHz					
23.2.8.1	FUND PWR	9.00	9.60	.00	dbm	PASS
23.2.8.2	WORST HARM		2.0		nd	
23.2.8.3	HARM PWR		-63.1		dbm	
23.2.8.4	FUND - HARM	-90	-72.7	-40	dbc	PASS
23.2.9	500 kHz					
23.2.9.1	FUND PWR	9.00	9.60	.00	dbm	PASS
23.2.9.2	WORST HARM		2.0		nd	
23.2.9.3	HARM PWR		-53.4		dbm	
23.2.9.4	FUND - HARM	-90	-63.0	-40	dbc	PASS
23.2.10	1 MHz					
23.2.10.1	FUND PWR	9.00	9.70	.00	dbm	PASS
23.2.10.2	WORST HARM		3.0		rd	
23.2.10.3	HARM PWR		-46.8		dbm	
23.2.10.4	FUND - HARM	-90	-56.5	-40	dbc	PASS
23.2.11	1.2 MHz					
23.2.11.1	FUND PWR	-2.00	10.00	.00	dbm	PASS
23.2.11.2	WORST HARM		3.0		rd	
23.2.11.3	HARM PWR		-45.9		dbm	
23.2.11.4	FUND - HARM	-90	-55.9	-40	dbc	PASS
23.2.12	1.5 MHz					
23.2.12.1	FUND PWR	-2.00	10.10	.00	dbm	PASS
23.2.12.2	WORST HARM		3.0		rd	
23.2.12.3	HARM PWR		-46.5		dbm	
23.2.12.4	FUND - HARM	-90	-56.6	-40	dbc	PASS
23.2.13	2 MHz					
23.2.13.1	FUND PWR	-2.00	9.20	.00	dbm	PASS
23.2.13.2	WORST HARM		2.0		nd	

23.2.13.3 HARM PWR		-47.0		dbm	
23.2.13.4 FUND - HARM	-90	-56.2	-40	dbc	PASS

24.0 SPURIOUS

CHANNEL 1

	PARAMETER	LOLIMIT	READING	HILIMIT	UNIT	STATUS
24.1.1	FREQ: 1.5 Mhz					
24.1.1.1	FUND PWR	12	13.7		dbm	PASS
24.1.1.2	SPUR LVL @ 2.5 Mhz		-46.8		dbm	
24.1.1.3	FUND-SPUR		-60.5	-50	dbc	PASS
24.1.2	FREQ: 1.818181818 Mhz					
24.1.2.1	FUND PWR	12	12.8		dbm	PASS
24.1.2.2	SPUR LVL @ .909 Mhz		-42.4		dbm	
24.1.2.3	FUND-SPUR		-55.2	-50	dbc	PASS
24.1.3	FREQ: 2 Mhz					
24.1.3.1	FUND PWR	12	12.2		dbm	PASS
24.1.3.2	SPUR LVL @ 10 Mhz		-61.4		dbm	
24.1.3.3	FUND-SPUR		-73.6	-50	dbc	PASS

CHANNEL 2

24.2.1	FREQ: 1.5 Mhz					
24.2.1.1	FUND PWR	12	13.7		dbm	PASS
24.2.1.2	SPUR LVL @ 2.5 Mhz		-44.2		dbm	
24.2.1.3	FUND-SPUR		-57.9	-50	dbc	PASS
24.2.2	FREQ: 1.818181818 Mhz					
24.2.2.1	FUND PWR	12	13.0		dbm	PASS
24.2.2.2	SPUR LVL @ .909 Mhz		-45.3		dbm	
24.2.2.3	FUND-SPUR		-58.3	-50	dbc	PASS
24.2.3	FREQ: 2 Mhz					
24.2.3.1	FUND PWR	12	12.5		dbm	PASS
24.2.3.2	SPUR LVL @ 10 Mhz		-55.4		dbm	
24.2.3.3	FUND-SPUR		-67.9	-50	dbc	PASS

25.0 RISE / FALL & ABERRATIONS

25.1 CHANNEL 1

	PARAMETER	LOLIMIT	READING	HILIMIT	UNIT	STATUS
25.1.1	10 Vp-p					
25.1.1.1	Risetime	20	44.7	75	nsec	PASS

25.1.1.2 Falltime	20	40.0	75	nsec	PASS
25.1.1.3 Pos aberr	0	1.2	5	%	PASS
25.1.1.4 Neg aberr	0	1.0	5	%	PASS
25.1.2 25 Vp-p					
25.1.2.1 Risetime	20	43.2	75	nsec	PASS
25.1.2.2 Falltime	20	36.4	75	nsec	PASS
25.1.2.3 Pos aberr	0	1.3	5	%	PASS
25.1.2.4 Neg aberr	0	1.2	5	%	PASS

25.2 CHANNEL 2

25.2.1 10 Vp-p					
25.2.1.1 Risetime	20	45.8	75	nsec	PASS
25.2.1.2 Falltime	20	41.4	75	nsec	PASS
25.2.1.3 Pos aberr	0	1.1	5	%	PASS
25.2.1.4 Neg aberr	0	1.1	5	%	PASS
25.2.2 25 Vp-p					
25.2.2.1 Risetime	20	44.7	75	nsec	PASS
25.2.2.2 Falltime	20	36.6	75	nsec	PASS
25.2.2.3 Pos aberr	0	1.3	5	%	PASS
25.2.2.4 Neg aberr	0	2.5	5	%	PASS

26.0 SQUAREWAVE SYMMETRY

CHANNEL 1

	FREQ,SYM	LOLIMIT	READING	HILIMIT	UNIT	STATUS
26.1.1	1 kHz : 20	16.999	21.5149	23.001	%	PASS
26.1.2	1 kHz : 50	46.999	50.7753	53.001	%	PASS
26.1.3	1 kHz : 80	76.999	80.8963	83.001	%	PASS
26.1.4	1 MHz : 20	15.500	22.3000	24.500	%	PASS
26.1.5	1 MHz : 50	45.500	51.0001	54.500	%	PASS
26.1.6	1 MHz : 80	75.500	80.5002	84.500	%	PASS

CHANNEL 2

26.2.1	1 kHz : 20	16.999	20.5253	23.001	%	PASS
26.2.2	1 kHz : 50	46.999	50.2645	53.001	%	PASS
26.2.3	1 kHz : 80	76.999	80.3251	83.001	%	PASS
26.2.4	1 MHz : 20	15.500	21.4000	24.500	%	PASS
26.2.5	1 MHz : 50	45.500	50.5001	54.500	%	PASS
26.2.6	1 MHz : 80	75.500	79.6002	84.500	%	PASS

27.0 AM INPUT

27.1 CHANNEL 1

	AM IN Vdc	LOLIMIT	READING	HILIMIT	UNIT	STATUS
27.1.1	0	-.23	.018	.23	Vrms	PASS
27.1.2	1	2.85	3.663	3.86	Vrms	PASS
27.1.3	2	6.01	7.279	8.13	Vrms	PASS
27.1.4	3	9.02	10.875	12.20	Vrms	PASS

27.1.5	4	12.02	14.482	16.26	Vrms	PASS
27.1.6	5	15.03	18.101	20.33	Vrms	PASS
27.2.		CHANNEL 2				
27.2.1	0	-.23	.002	.23	Vrms	PASS
27.2.2	1	2.85	3.797	3.86	Vrms	PASS
27.2.3	2	6.01	7.557	8.13	Vrms	PASS
27.2.4	3	9.02	11.297	12.20	Vrms	PASS
27.2.5	4	12.02	15.051	16.26	Vrms	PASS
27.2.6	5	15.03	18.818	20.33	Vrms	PASS

28.0 SYNC OUT

28.1 CHANNEL 1

	PARAMETER	LOLIMIT	READING	HILIMIT	UNIT	STATUS
28.1.1.1	SYNC LO	-.005	-.0008	.400	Vdc	PASS
28.1.1.2	SYNC HI	2.4	2.60	5.0	Vdc	PASS
28.2		CHANNEL 2				
28.2.1.1	SYNC LO	-.005	-.0008	.400	Vdc	PASS
28.2.1.2	SYNC HI	2.4	2.52	5.0	Vdc	PASS

29.0 MAIN GENERATOR MODE TEST

	MODE/PARAMETER	LOLIMIT	READING	HILIMIT	UNIT	STATUS
	(UUT FREQ:2Khz)					
29.1	CONT/FREQ	1900	2000.0	2100	Hz	PASS
29.2	TRIG/QUIESCENT		.002	.10	Vrms	PASS
29.3	TRIG / FREQ	980	986.7	1020	Hz	PASS
	TRIG SOURCE: 1 Khz SQUAREWAVE					
29.4	S-GATE/QUIESCENT		.000	.10	Vrms	PASS
29.5	S-GATE / GATED	1.75	1.772	1.79	Vrms	PASS
	TRIG SOURCE 2Vdc					
29.6	S-GATE / 1 CYCLE	1.13	1.244	1.37	Vrms	PASS
	TRIG SOURCE: 1 Khz SINGLE PULSE, PULSE WIDTH 250 usec					
29.7	A-GATE / CYCLE/2	.71	.785	.97	Vrms	PASS
	TRIG SOURCE: 1 Khz SINGLE PULSE, PULSE WIDTH 250 usec					
29.8	BURST / COUNT(2)	2	2	2		PASS

30.0 BURST COUNT

	BURST COUNT	READING	STATUS
30.1	1	1	PASS
30.2	2	2	PASS
30.3	4	4	PASS
30.4	8	8	PASS
30.5	16	16	PASS
30.6	32	32	PASS
30.7	64	64	PASS
30.8	128	128	PASS
30.9	256	256	PASS
30.10	512	512	PASS
30.11	1024	1024	PASS
30.12	2048	2048	PASS
30.13	4096	4096	PASS
30.14	8192	8192	PASS
30.15	16384	16384	PASS
30.16	32768	32768	PASS
30.17	65535	65535	PASS

31.0 EXTERNAL PHASE LOCK

	SETTING/SOURCE	LOLIMIT	READING	HILIMIT	UNIT	STATUS
31.1.1	40Hz/MONITOR	38.800	40.0000	41.200	Hz	PASS
31.1.2	SYNC OUT	39.960	39.9999	40.040	Hz	PASS
31.1.3	PLL_NO_LOCK (EXT. SIGNAL REMOVED)					PASS
31.2.1	475Hz/MONITOR	460.750	475.0594	489.250	Hz	PASS
31.2.2	SYNC OUT	474.530	475.0001	475.480	Hz	PASS
31.2.3	PLL_NO_LOCK (EXT. SIGNAL REMOVED)					PASS
31.3.1	990Hz/MONITOR	960.300	990.0990	1019.700	Hz	PASS
31.3.2	SYNC OUT	989.010	990.0003	990.990	Hz	PASS
31.3.3	PLL_NO_LOCK (EXT. SIGNAL REMOVED)					PASS
31.4.1	1.1kHz/MONITOR	1.067	1.1001	1.133	kHz	PASS
31.4.2	SYNC OUT	1.099	1.1000	1.101	kHz	PASS
31.4.3	PLL_NO_LOCK (EXT. SIGNAL REMOVED)					PASS
31.5.1	4.4kHz/MONITOR	4.268	4.4053	4.532	kHz	PASS
31.5.2	SYNC OUT	4.396	4.4000	4.404	kHz	PASS
31.5.3	PLL_NO_LOCK (EXT. SIGNAL REMOVED)					PASS
31.6.1	9.9kHz/MONITOR	9.603	9.9010	10.197	kHz	PASS
31.6.2	SYNC OUT	9.890	9.9000	9.910	kHz	PASS
31.6.3	PLL_NO_LOCK (EXT. SIGNAL REMOVED)					PASS
31.7.1	10.1kHz/MONITOR	9.797	10.1010	10.403	kHz	PASS
31.7.2	SYNC OUT	10.090	10.1000	10.110	kHz	PASS
31.7.3	PLL_NO_LOCK (EXT. SIGNAL REMOVED)					PASS

31.8.1	44.9kHz/MONITOR	43.553	44.8833	46.247 kHz	PASS
31.8.2	SYNC OUT	44.855	44.9000	44.945 kHz	PASS
31.8.3	PLL_NO_LOCK (EXT. SIGNAL REMOVED)				PASS
31.9.1	99.9kHz/MONITOR	96.903	99.8004	102.897 kHz	PASS
31.9.2	SYNC OUT	99.800	99.9000	100.000 kHz	PASS
31.9.3	PLL_NO_LOCK (EXT. SIGNAL REMOVED)				PASS
31.10.1	100.1kHz/MONITOR	97.097	100.0000	103.103 kHz	PASS
31.10.2	SYNC OUT	100.000	100.1000	100.200 kHz	PASS
31.10.3	PLL_NO_LOCK (EXT. SIGNAL REMOVED)				PASS
31.11.1	1MHz/MONITOR	.970	1.0000	1.030 MHz	PASS
31.11.2	SYNC OUT	.999	1.0000	1.001 MHz	PASS
31.11.3	PLL_NO_LOCK (EXT. SIGNAL REMOVED)				PASS
31.12.1	2MHz/MONITOR	1.940	2.0000	2.060 MHz	PASS
31.12.2	SYNC OUT	1.998	2.0000	2.002 MHz	PASS
31.12.3	PLL_NO_LOCK (EXT. SIGNAL REMOVED)				PASS

32.0 PROGRAMMABLE TRIGGER LEVEL TEST

	TRIG LVL/SLOPE	LOLIMIT	READING	HILIMIT	UNIT	STATUS
32.1	3.4 POS	3.1	3.47	3.7	Vdc	PASS
32.2	-3.3 POS	-3.6	-3.42	-3.0	Vdc	PASS
32.3	-3.3 NEG	-3.6	-3.45	-3.0	Vdc	PASS

33.0 INTERNAL TRIGGER TEST

	SETTING	LOLIMIT	READING	HILIMIT	UNIT	STATUS
33.1	156.00 kHz	155.84400	156.003764	156.15600	kHz	PASS
33.2	78.10 kHz	78.02190	78.096391	78.17810	kHz	PASS
33.3	39.10 kHz	39.06090	39.100723	39.13910	kHz	PASS
33.4	19.50 kHz	19.48050	19.499918	19.51950	kHz	PASS
33.5	9.77 kHz	9.76023	9.770410	9.77977	kHz	PASS
33.6	4.88 kHz	4.87512	4.879794	4.88488	kHz	PASS
33.7	2.44 kHz	2.43756	2.439915	2.44244	kHz	PASS
33.8	1.22 kHz	1.21878	1.219962	1.22122	kHz	PASS
33.9	610.00 Hz	609.39000	609.977320	610.61000	Hz	PASS
33.10	305.00 Hz	304.69500	304.990188	305.30500	Hz	PASS
33.11	152.00 Hz	151.84800	151.992131	152.15200	Hz	PASS
33.12	76.30 Hz	76.22370	76.294110	76.37630	Hz	PASS
33.13	38.10 Hz	38.06190	38.100921	38.13810	Hz	PASS
33.14	19.10 Hz	19.08090	19.101460	19.11910	Hz	PASS
33.15	9.54 Hz	9.53046	9.539099	9.54954	Hz	PASS
33.16	4.77 Hz	4.76523	4.769545	4.77477	Hz	PASS
33.17	2.38 Hz	2.37762	2.380118	2.38238	Hz	PASS
33.18	1.19 Hz	1.18881	1.190058	1.19119	Hz	PASS

34.0 MARKER OUTPUT LEVEL TEST

	SETTING	LOLIMIT	READING	HILIMIT	UNIT	STATUS
34.1	999.9999	2.4	2.66	5.0	Vdc	PASS

34.2	1000.0001	-.005	.0012	.400	Vdc	PASS

35.0 SWEEP TIME

	SETTING	LOLIMIT	READING	HILIMIT	UNIT	STATUS
35.1	.01sec	9.8900	9.97569	10.1100	mSEC	PASS

36.0 SWEEP MODES

	MODE / PARAMETER	LOLIMIT	READING	HILIMIT	UNIT	STATUS
36.1	(5) / START FREQ	.999	1.0000	1.001	kHz	PASS
36.2	(5) / HORZ Vdc	-.10	.003	.10	Vdc	PASS
36.3	(5) / STOP FREQ	9.999	10.0000	10.001	kHz	PASS
36.4	(5) / HORZ Vdc	9.50	10.023	10.50	Vdc	PASS
36.5	(5) / START FREQ	.999	1.0000	1.001	kHz	PASS
36.6	(7) / SYNC FSK (TTL Lo @ TRIGIN)	.990	1.0000	1.010	kHz	PASS
36.7	(7) / SYNC FSK (TTL HI @ TRIGIN)	9.900	10.0000	10.100	kHz	PASS
36.8	(8) / ASYNC FSK (TTL Lo @ TRIGIN)	.990	1.0000	1.010	kHz	PASS
36.9	(8) / ASYNC FSK (TTL HI @ TRIGIN)	9.900	10.0000	10.100	kHz	PASS
36.10	(9) / MARKER FREQ (TRIG FREQ: 1kHz)	.999	1.0000	1.001	kHz	PASS
36.11	(10) / MARKER FREQ	.989	.9900	.991	kHz	PASS

37.0 FM/PM INPUT

	FM_PM IN	LOLIMIT	READING	HILIMIT	UNIT	STATUS
37.1	-.9609 vdc	.959	1.1871	1.391	kHz	PASS
37.2	.9609 vdc	9.609	9.8234	10.041	kHz	PASS

38.0 HOLD IN

	ACTION/PARAMETER	LOLIMIT	READING	HILIMIT	UNIT	STATUS
38.1	HOLD/SWEEP FREQ	4.95	5.500	6.05	kHz	PASS
38.2	HOLD/RAMP Vdc	4.50	4.994	5.50	Vdc	PASS

39.0 STORED SETTINGS

39.1 STORING AND RECALLING 25 STORESETTINGS

PASSED STORESETTINGS TEST

40.0 SELF DIAGNOSTICS

PASSED SELF DIAGNOSTICS TEST