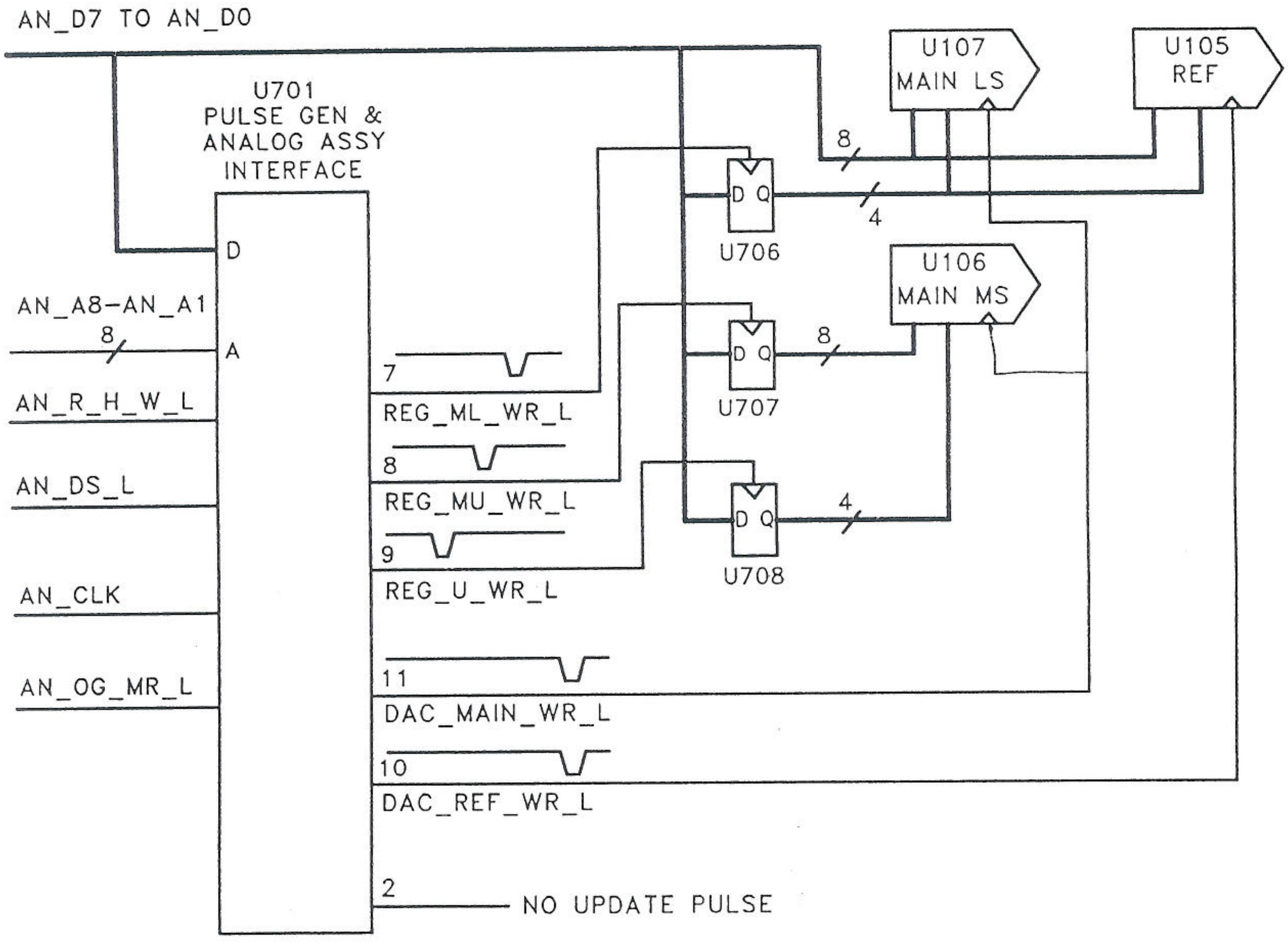
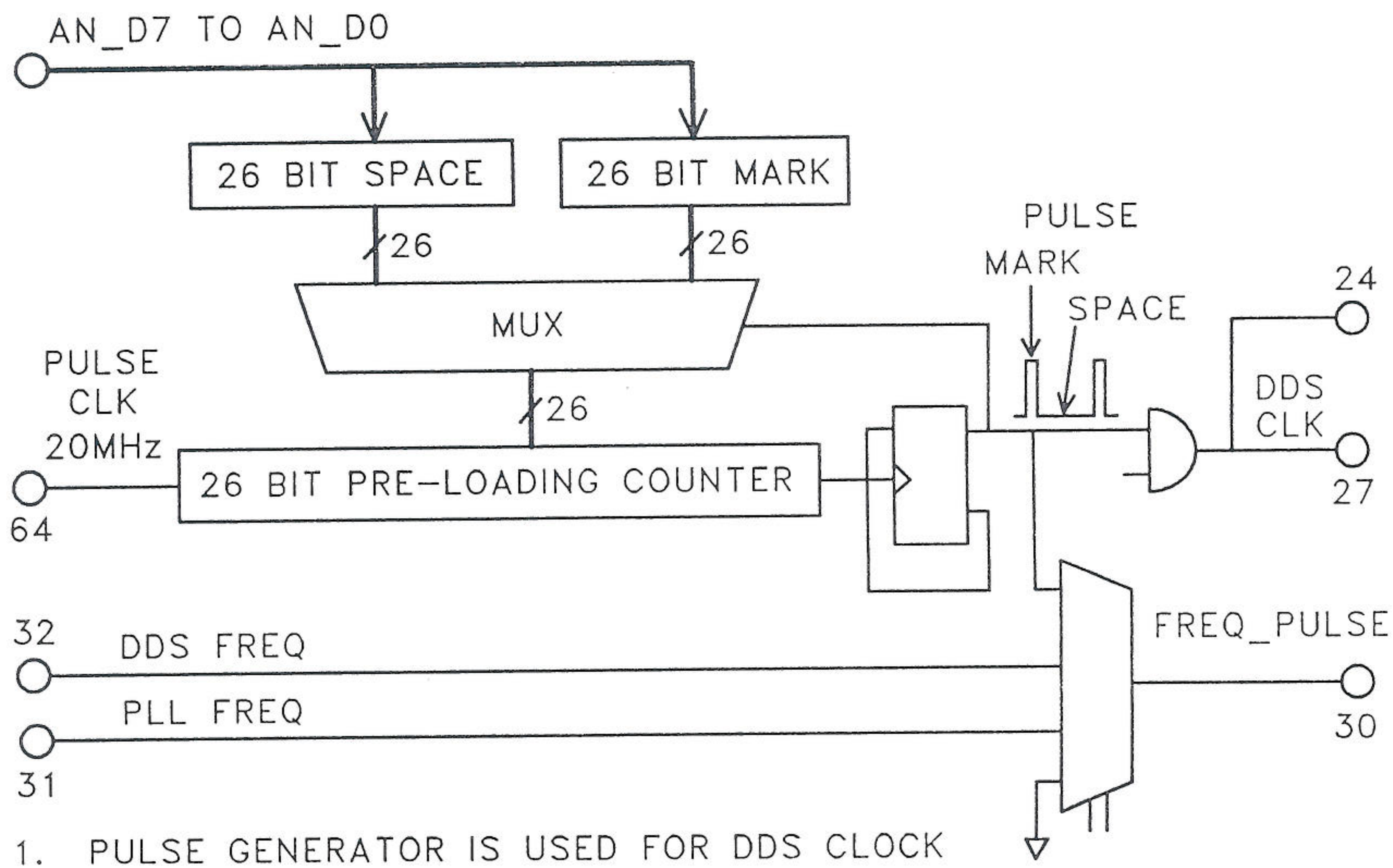


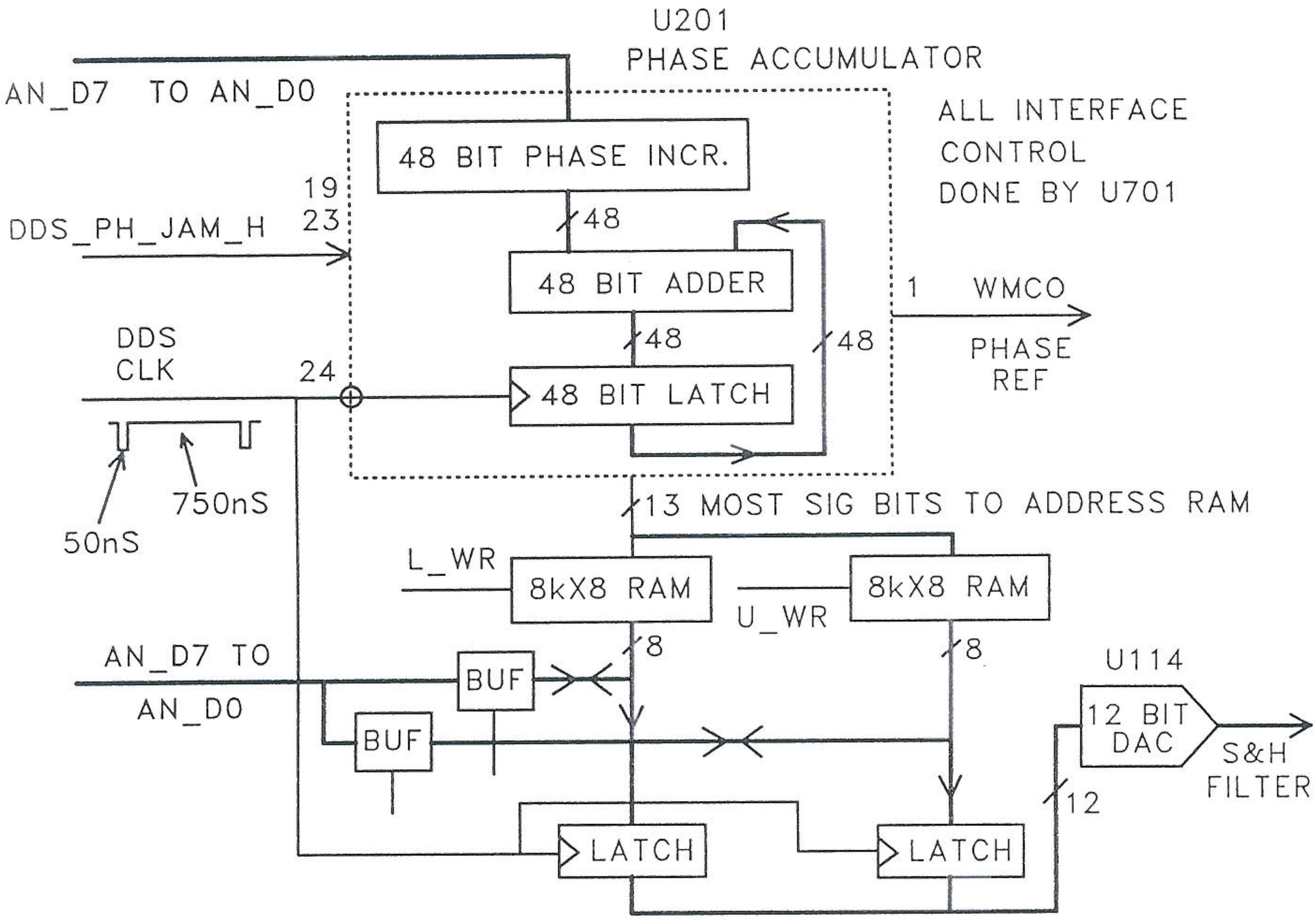
ANALOG ASSY – DAC CONTROL



1. PULSE GENERATOR IS USED FOR DDS CLOCK
2. ACTEL DEVICE SELECTS FREQ_PULSE SOURCE

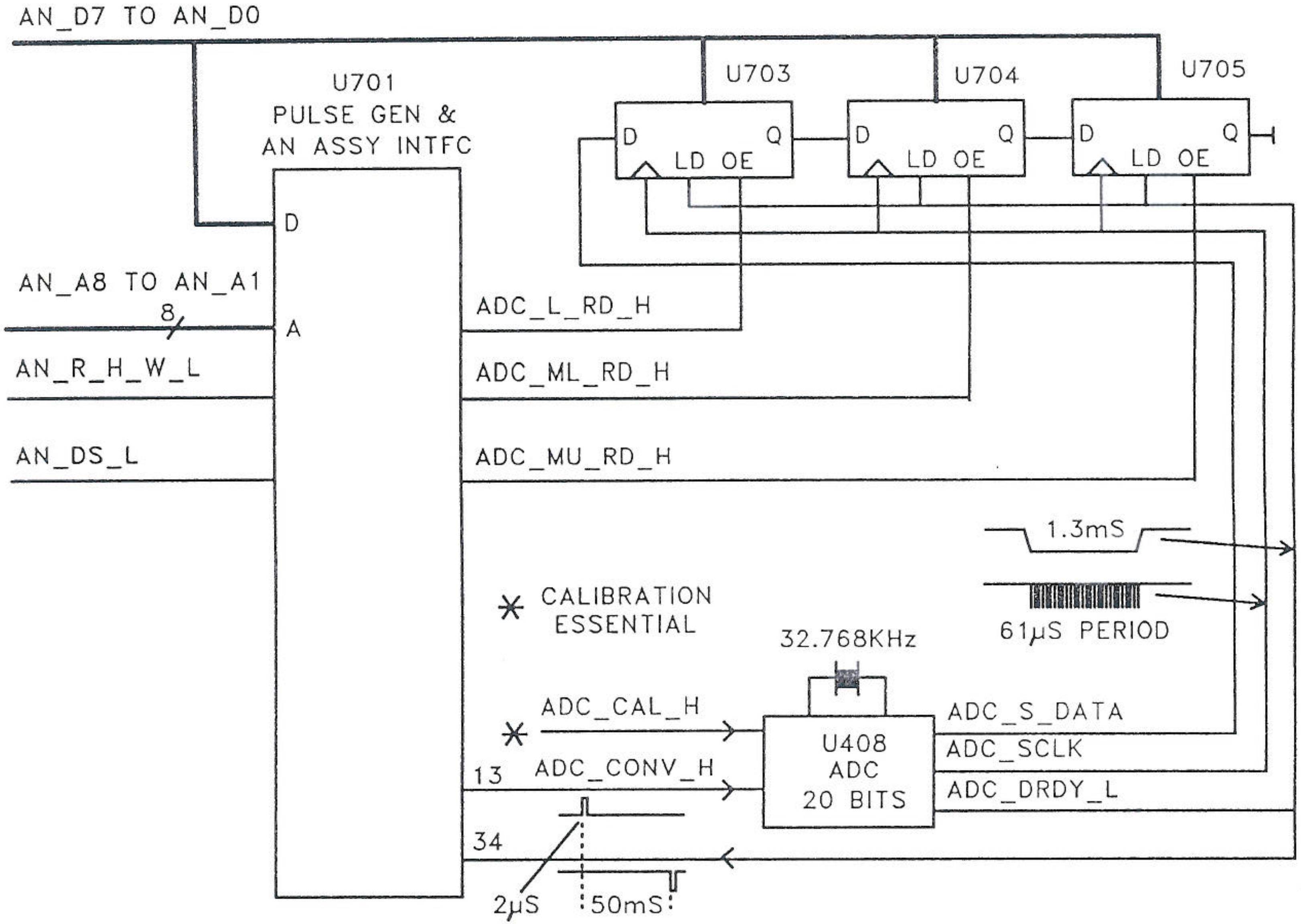
ANALOG ASSY – U701 INTERNALS

PULSE COUNTER & PULSE/FREQ SELECTION

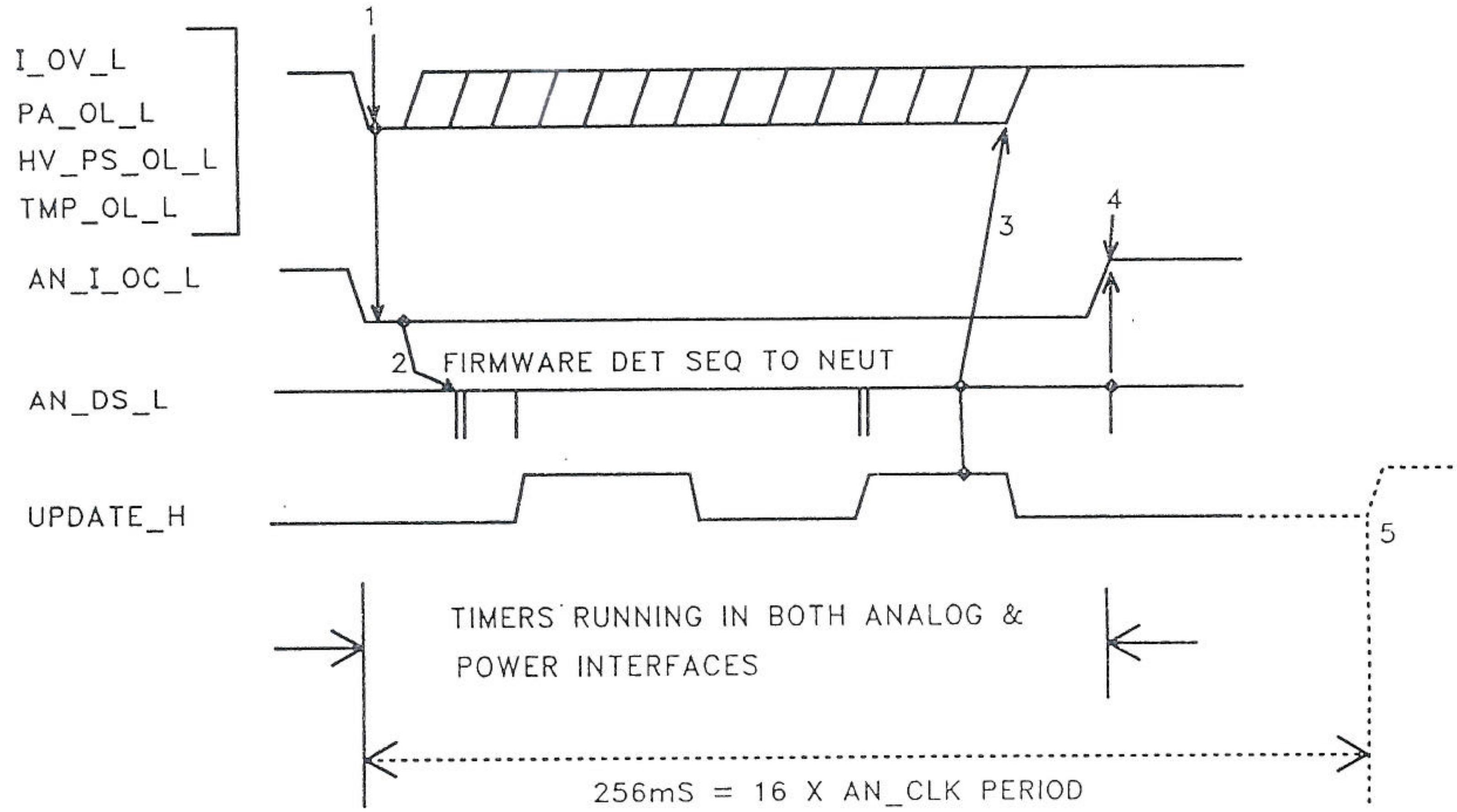


ANALOG ASSY – DDS DIGITAL

A27



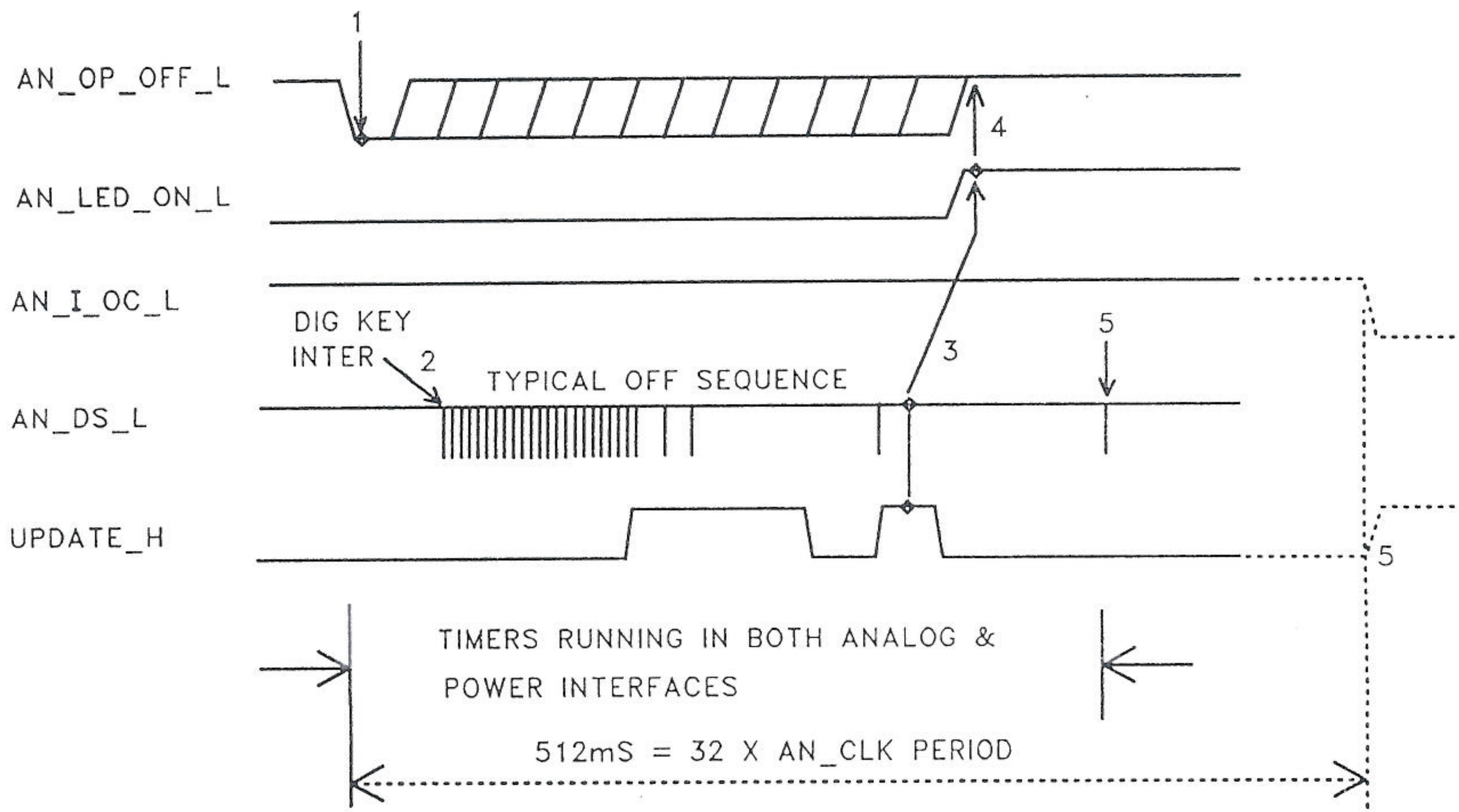
ANALOG ASSY ADC INTERFACE



1. DETECTOR INPUT IS SET AND LATCHED INTERNALLY TO REQUEST INTERRUPT
2. FIRMWARE DETECTOR OFF SEQUENCE TO NEUTRAL
3. NEUTRAL STATE CLEARS DETECTOR SIGNAL
4. FIRMWARE CLEARS INTERRUPT TO RESET TIMERS BEFORE TIME-OUT
5. IF INTERRUPT FAILS TO CLEAR - ALL CONTROL BITS FORCED TO NEUTRAL ON TIME-OUT

POWER ASSY DETECTORS & FAULT SEQUENCE

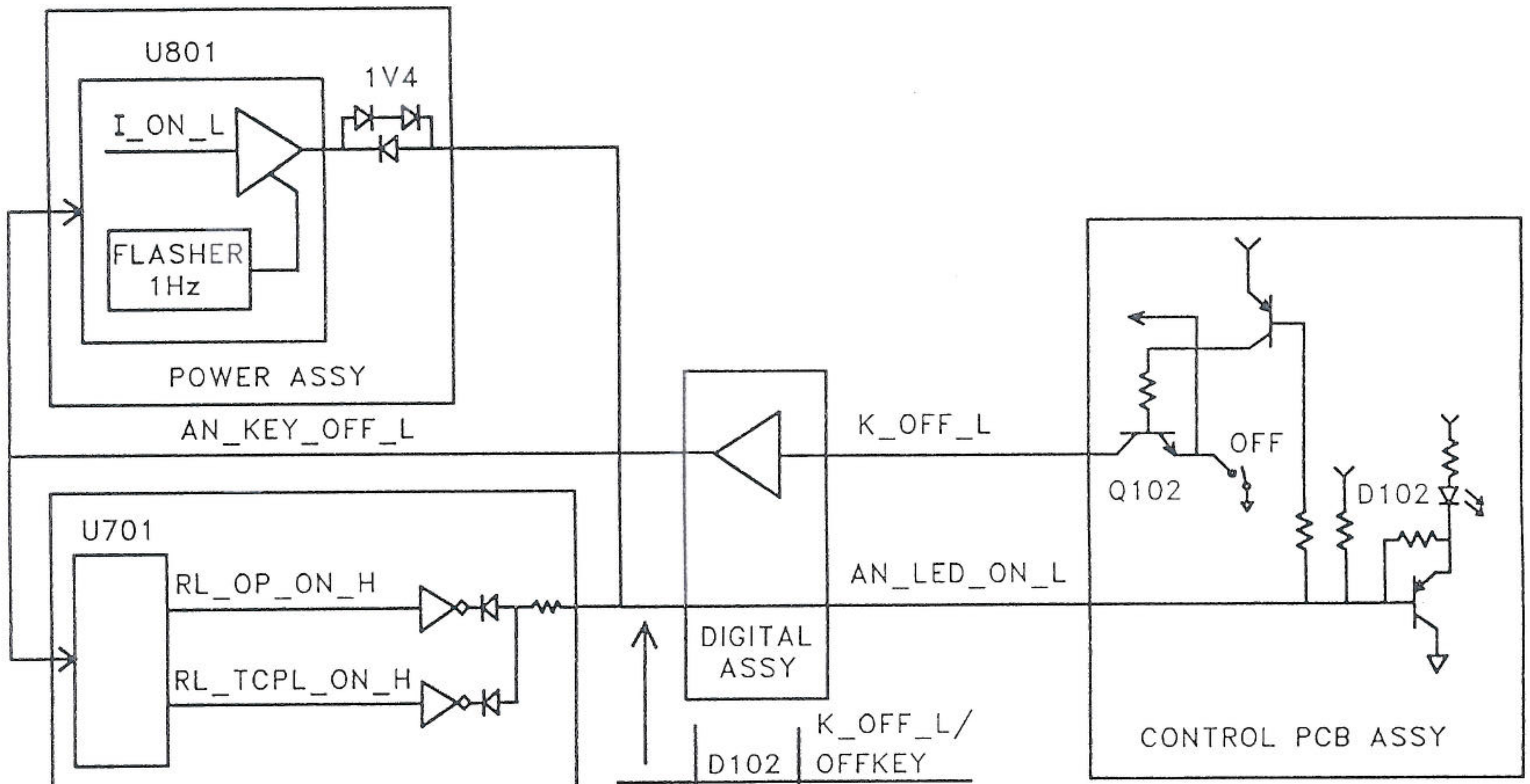
A29



1. OFF KEY PRESSED WITH OUTPUT LED ON. AN_OP_OFF_L LATCHED INTERNALLY
2. FIRMWARE NORMAL SEQUENCE TO NEUTRAL (OFF) FROM KEY INTERRUPT
3. OUTPUT LED GOES OFF IN NEUTRAL
4. AN_OP_OFF_L CLEARS IF KEY STILL PUSHED
5. FIRMWARE CLEARS LATCHED AN_OP_OFF_L TO RESET TIMERS
6. IF LATCHED AN_OP_OFF_L FAILS TO CLEAR – ALL CONTROL BITS FORCED TO NEUTRAL ON TIME-OUT

POWER & ANALOG ASSY – OFF KEY INTERLOCK

A30



	D102	K_OFF_L/ OFFKEY
5V0	OFF	INHIBIT
3V6	OFF	ENABLE
0V6	ON	ENABLE

1. LED IS ON DRIVEN FROM ANALOG OR POWER ASSEMBLIES IF OUTPUT IS ON.
2. LED IS FLASHED BY POWER INTERFACE (U801) IF HIGH VOLTAGE PATH SELECTED BY FIRMWARE.
3. AN_LED_ON_L HAS THREE LEVEL LOGIC SO THAT K_OFF_L CAN GO LOW WHEN THE OUTPUT IS ON.

ON LED CONTROL & OFF KEY INTERLOCK

ADDRESS	D15-D8	D7-D0	TIME-OUT
FFFFFF - FFFC00	processor internal peripherals		0 waits
FFFBFF - C20000	--- unused area ---		processor BERR TIME-OUT
C1FFFF - C10000	peripheral decode area U207		processor CS1
C0FFFF - C04000	EEPROM_L hi (protected by CAL_EN_L)	EEPROM_L lo	processor CS1
C03FFF - C00000	EEPROM_L hi (not protected by CAL_EN_L)	EEPROM_L lo	processor CS1
BFFFFF - 830000	--- unused area ---		processor BERR TIME-OUT
82FFFF - 820000	-----	SGEN_L	stretched by U204
81FFFF - 810000	DISP_MEM_L hi	DISP_MEM_L lo	U301 DTACK
80FFFF - 800000	DISP_REG_L hi	DISP_REG_L lo	U301 DTACK
7FFFFF - 600000	C2_CE1_L	C2_CE2_L	processor CS0
5FFFFF - 400000	C1_CE1_L (PROM1_L when BOOT_EN_L is low	C1_CE2_L	processor CS0 0 waits)
3FFFFF - 340000	--- unused area ---		processor BERR TIME-OUT
33FFFF - 300000	RAM_L hi	RAM_L lo	0 waits
2FFFFF - 240000	--- unused area ---		processor BERR TIME-OUT
23FFFF - 200000	PROM3_L hi	-----	0 waits
1FFFFF - 100000	--- prom expansion area ---		processor BERR TIME-OUT
1BFFFF - 080000	PROM2_L hi (CARD1 when BOOT_EN_L is low	PROM2_L lo	0 waits processor CS0)
07FFFF - 000000	PROM1_L hi (CARD1 when BOOT_EN_L is low	PROM1_L lo	0 waits processor CS0)

The IO area is further decoded by U207.

Processor CS0 & CS1 are setup by the firmware to introduce three wait clock cycles (total select 380ns typical).

DISP_MEM_L and DISP_REG_L can only be accessed as words not bytes.

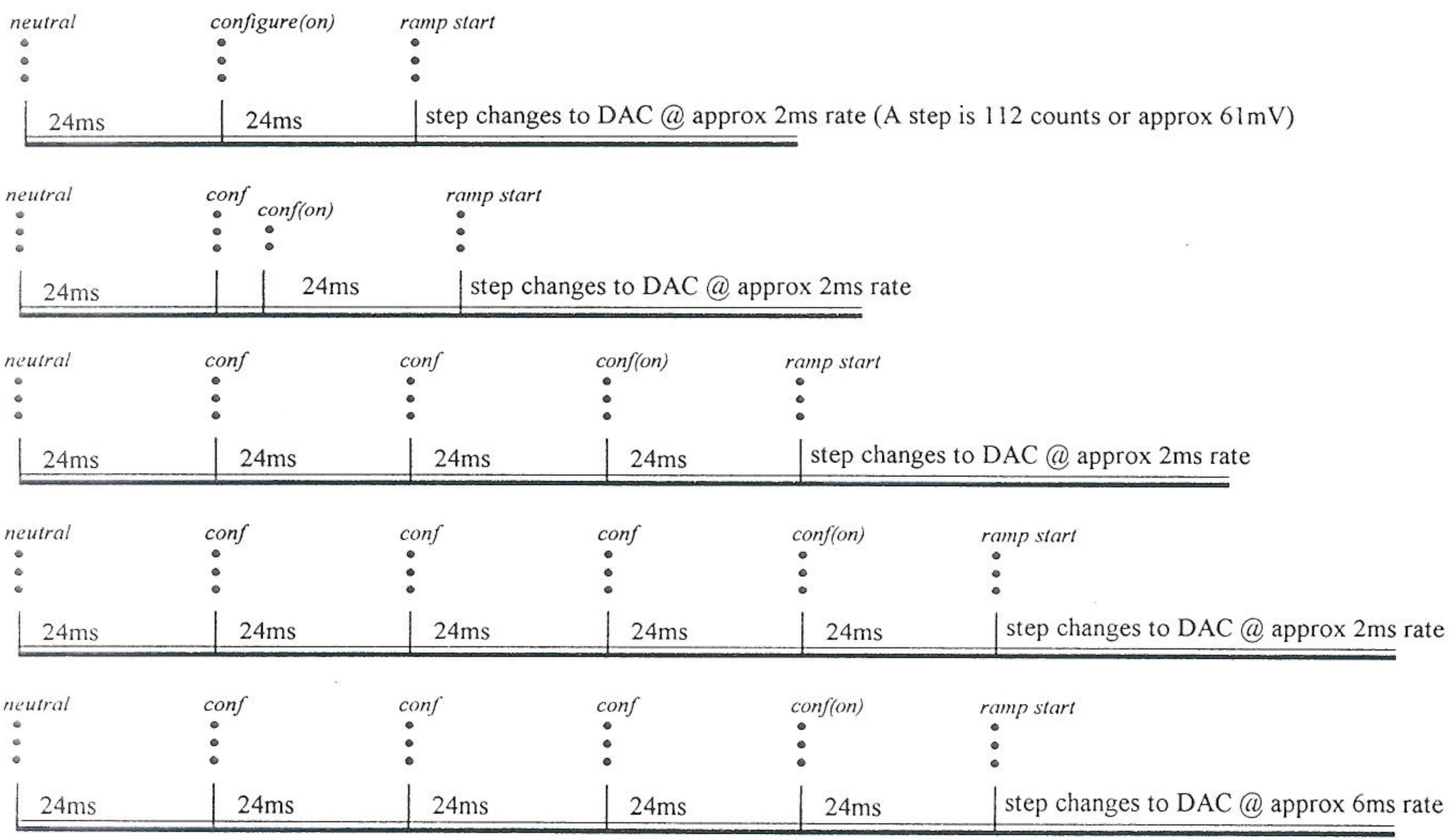
Flash & EEPROM are protected during power down by driving RD_L low . R206 also acts as a pull down.

ADDRESS	D15-D8	D7-D0	TIME-OUT
C1FFFF - C1E000	GPIA	----	processor CS1
C1DFFF - C1C000	-----	RTC DATA	processor CS1
C1BFFF - C1A000	-----	RTC ADDR	processor CS1
C19FFF - C18000	-----	RD_KEY	processor CS1
C17FFF - C16000	-----	RD_WHL	processor CS1
C15FFF - C14000	WR_CNTRL	-----	processor CS1
C13FFF - C12000	-----	RD_STAT2	processor CS1
C11FFF - C10000	RD_STAT1 hi	RD_STAT1 lo	processor CS1

address offset	device	write	read
001		REG A [47:40]	
003		REG A [39:32]	
005		REG A [31:24]	
007		REG A [23:16]	
009		REG A [15:8]	
00B		REG A [7:0]	
00D			
00F		REG A [47:0]	
011		REG B [47:40]	
013		REG B [39:32]	
015		REG B [31:24]	
017		REG B [23:16]	
019		REG B [15:8]	
01B		REG B [7:0]	
01D			
01F		REG B [47:0]	
021		REG C [47:40]	
023		REG C [39:32]	
025		REG C [31:24]	
027		REG C [23:16]	
029		REG C [15:8]	
02B		REG C [7:0]	
02D			
02F		REG D [47:0]	
031		REG D [47:40]	
033		REG D [39:32]	
035		REG D [31:24]	
037		REG D [23:16]	
039		REG D [15:8]	
03B		REG D [7:0]	
03D			
03F	DDS PHASE ACCUMULATOR U201	REG MA [47:0]	
041		REG MA [47:40]	
043		REG MA [39:32]	
045		REG MA [31:24]	
047		REG MA [23:16]	
049		REG MA [15:8]	
04B		REG MA [7:0]	
04D			
04F		REG MA [47:0]	
051		REG MB [47:40]	
053		REG MB [39:32]	
055		REG MB [31:24]	
057		REG MB [23:16]	
059		REG MB [15:8]	
15B		REG MB [7:0]	
05D			
05F		REG MB [47:0]	
061		MODE	
063			
065			
067			
069			
06B			
06D			
06F		IRST	
071		PCLK [15:8]	
073		PCLK [7:0]	
075		PCLK [15:8]	
077		PCLK [7:0]	
079		PCLK [15:8]	
07B		PCLK [7:0]	
07D		PCLK [15:8]	
07F		PCLK [7:0]	

0h820000 + address offset	device	write	read
081	ANALOG ASSY. CONTROL BITS. ANALOG CONTROLLER U701	A CLR (ONLY WR BEFOE UPDATES)	
083		AR D 5 & 6 CLR (ONLY WR AFTER RD)	AR (STATUS)
085		A5	A5
087		A6	A6
089		A1 - U807	A1 - U808
08B		A2 - U803	A2 - U804
08D		A3 - U805	A3 - U806
08F		A4 - U801 (LATCHES A1-A6 & P1-P4)	A4 - U802
091			
093			
095		DAC REF [11:8] - U105	
097		DAC REF [7:0] - U105	
099		DAC MAIN [28:24] - U106	
09B		DAC MAIN [23:16] - U106	
09D		DAC MAIN [11:8] - U107	
09F		DAC MAIN [7:0] - U107	
0A1		COUNT MARK [25:24]	
0A3		COUNT MARK [23:16]	
0A5		COUNT MARK [15:8]	
0A7		COUNT MARK [7:0]	
0A9		COUNT SPACE [25:24]	
0AB		COUNT SPACE [23:16]	
0AD		COUNT SPACE [15:8]	
0AF		COUNT SPACE [7:0]	
0B1			
0B3			ADC [19:16] - U705
0B5			ADC [15:8] - U704
0B7			ADC [7:0] - U703
0B9			
0BB			
0BD			
0BF			
0C1	POWER ASSY. CONTROL BITS. POWER CONTROLLER U801	P CLR (ONLY WR BEFOE UPDATES)	
0C3			PR (STATUS)
0C5			
0C7			
0C9		P1	P1
0CB		P2	P2
0CD		P3	P3
0CF		P4	P4
0D1			
0D3			
0D5			
0D7			
0D9			
0DB			
0D5			
0DF			
0E1			
0E3			
0E5			
0E7			
0E9			
0EB			
06D			
0EF			
0F1			
0F3			
0F5			
0F7			
0F9			
0FB			
0FD			
0FF			

9000 SEQUENCED CHANGES TO ANALOG SUBSYTEM
On Sequences



Applicable ranges:

300mV DC,
Thermocouple, Level

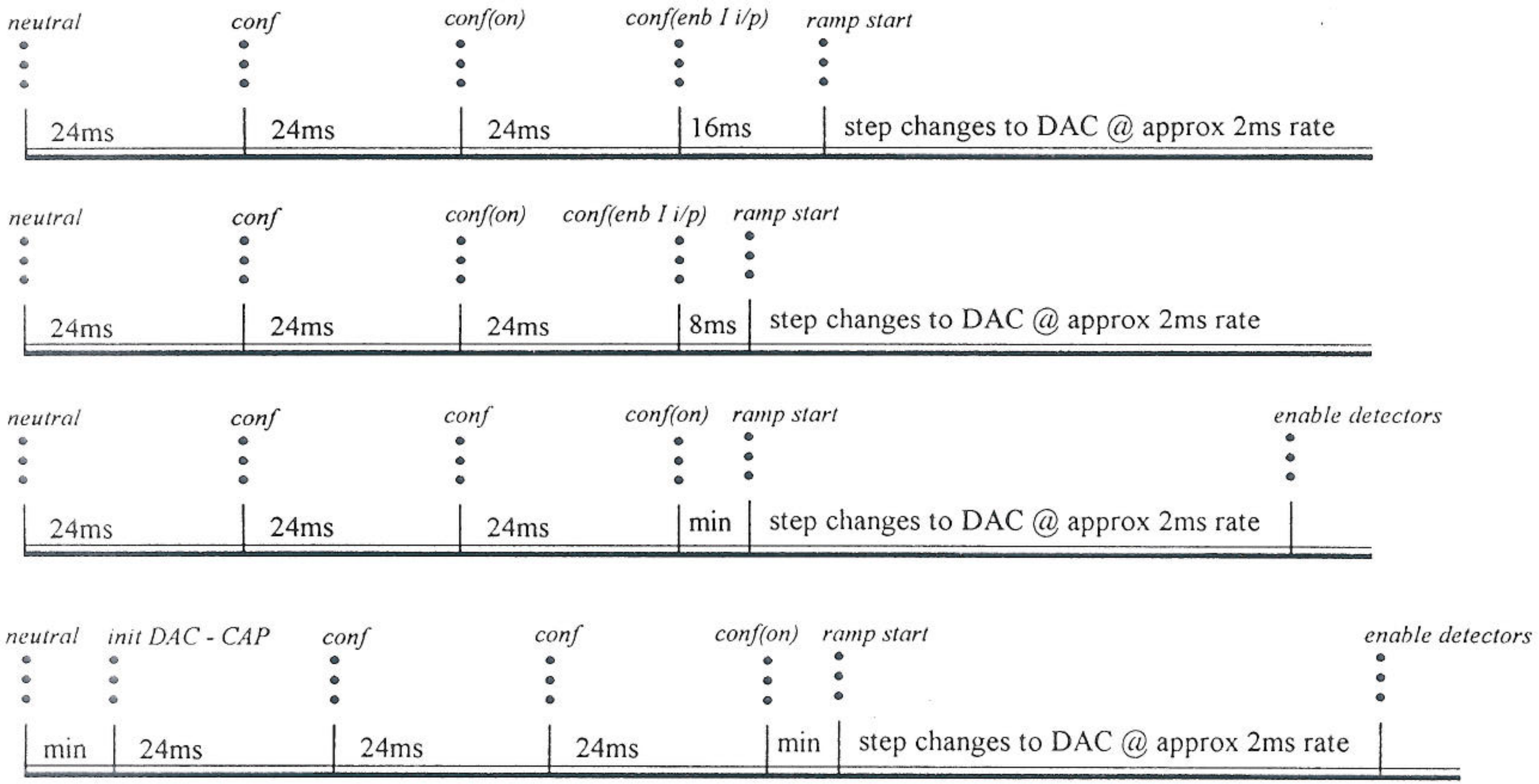
3V DC
300mV AC, 3V AC

30V DC
30V AC, 100V AC

300V DC
300V AC

1kV DC
1kV AC

9000 SEQUENCED CHANGES TO ANALOG SUBSYTEM
On Sequences (contd.)



Applicable ranges:

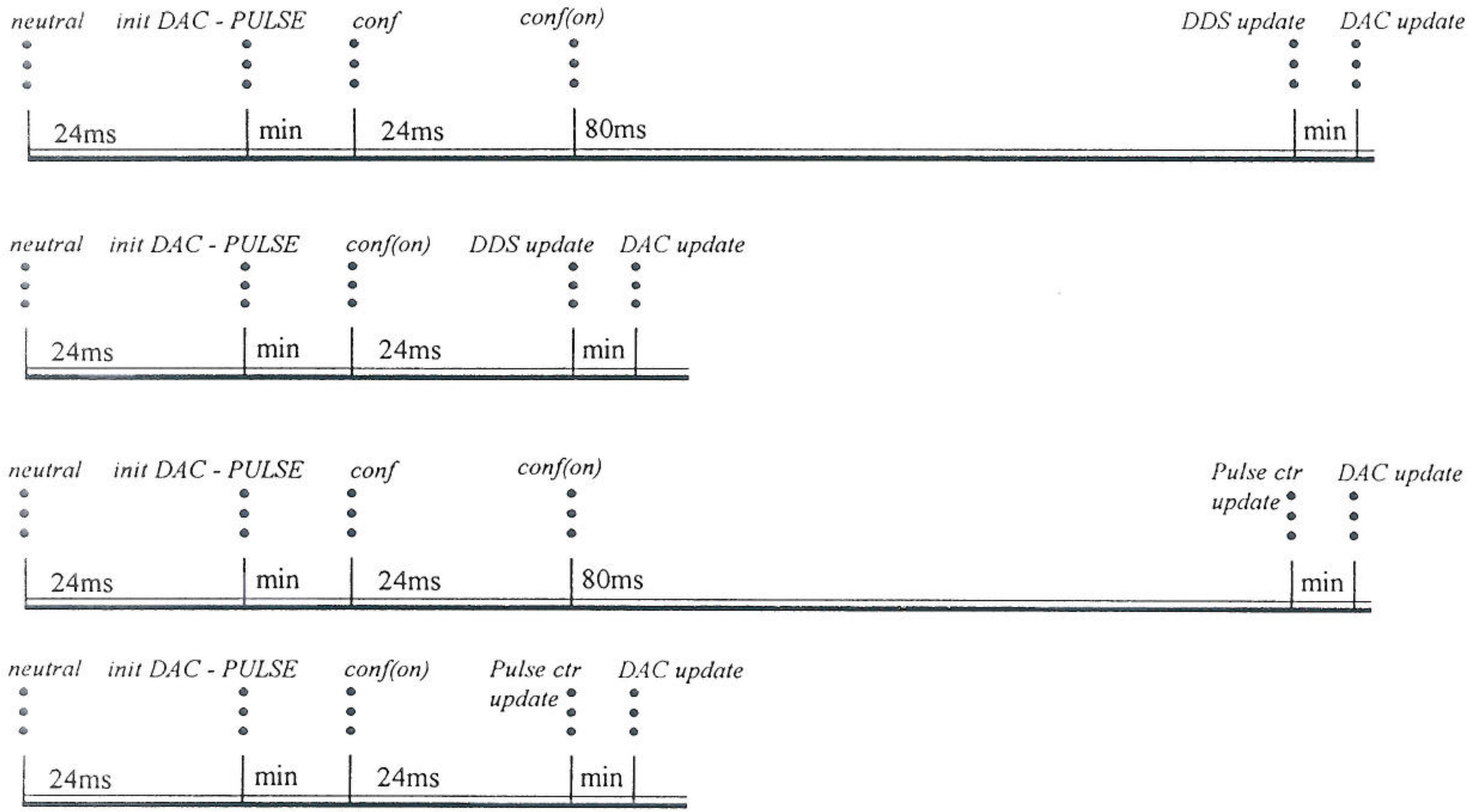
All DC and AC current ranges except 20A DC

20A DC

all OHMS ranges PRT

all CAPACITANCE ranges

9000 SEQUENCED CHANGES TO ANALOG SUBSYTEM
On Sequences (contd.)



Applicable ranges:

Frequency (High Volts)

Frequency (Low Volts)

Pulse (High Volts)

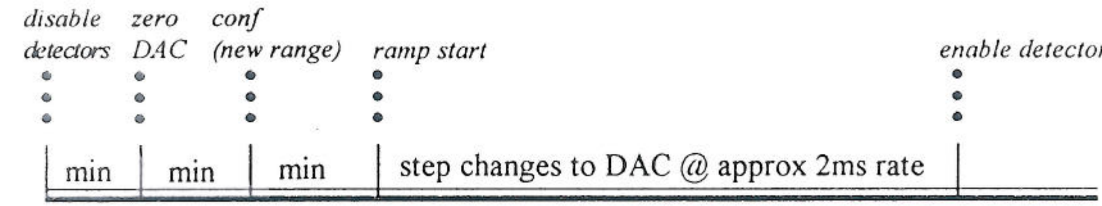
Pulse (Low Volts)

A38

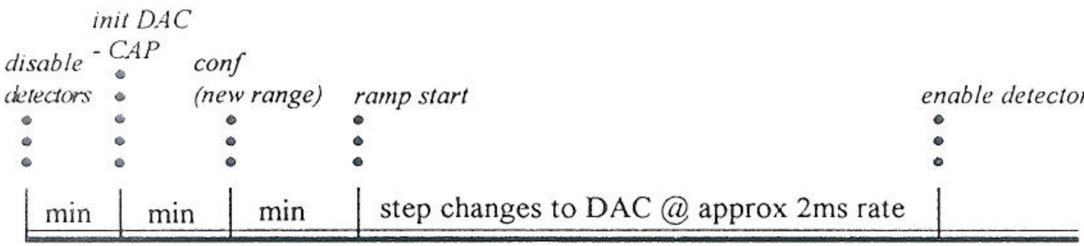
9000 SEQUENCED CHANGES TO ANALOG SUBSYTEM

Special Range Change Sequences

Applicable ranges:



All OHMS and COND ranges

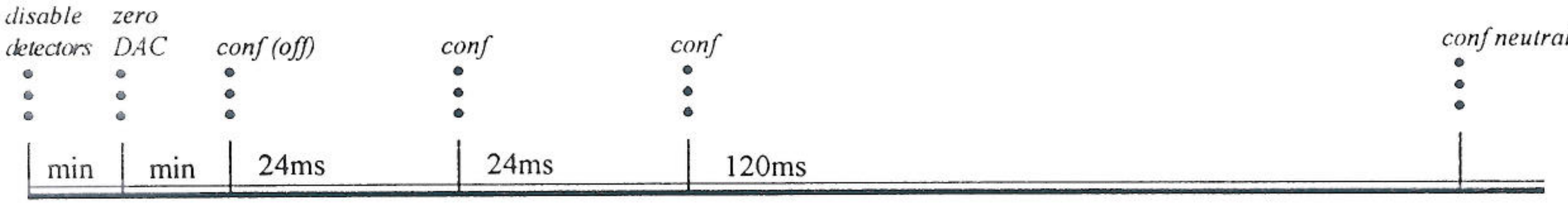


All CAP ranges

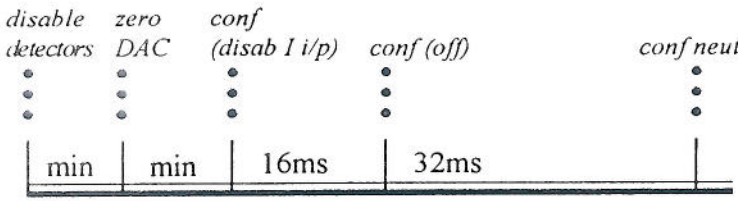
9000 SEQUENCED CHANGES TO ANALOG SUBSYTEM

Off Sequences

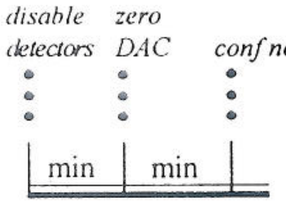
Applicable ranges:



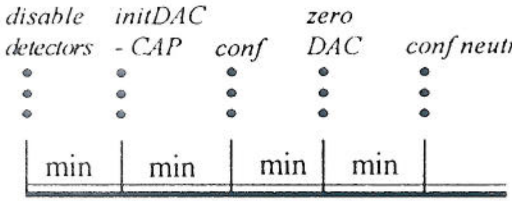
All DCV and ACV ranges, Level



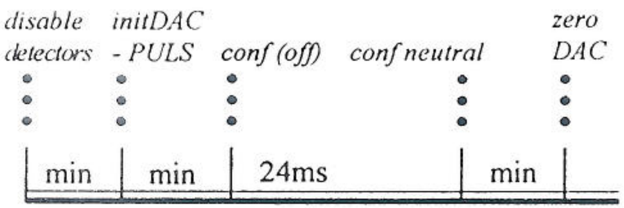
All DCI and ACI ranges



All ranges in OHMS, COND, PRT, and Thermocouple

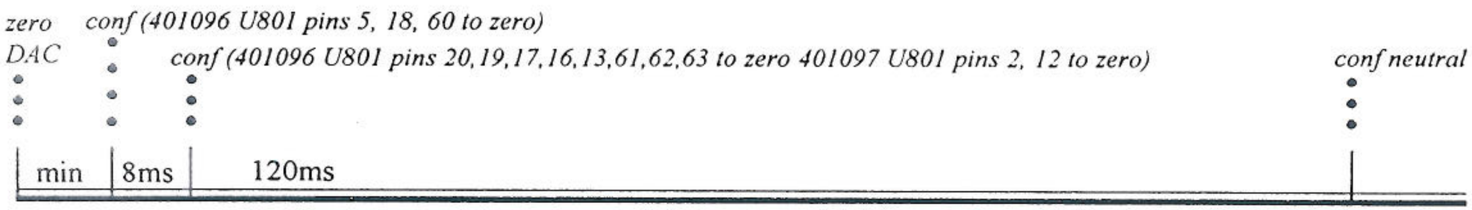


All CAP ranges



Frequency and Pulse

9000 SEQUENCED CHANGES TO ANALOG SUBSYTEM
Hardware Fault Off Sequence



There are three actions that follow the completion of this sequence;-

1. No apparent effect, if the cause is an 'off timeout' and the output state is Off.
2. An error is reported to the user for which a corrective action is possible.
3. If the output state is Off and not 'off timeout' a FATAL error is reported, via a watchdog trip, with message numbers in the range 9503, 9506 to 9509.

FUNCTIONAL DESCRIPTION OF THE 9000 ANALOGUE PCB

U101 is the main voltage reference for all AC and DC voltage and current functions. R103 attenuates the nominal 6.95V reference down to 6.5536. R103 also provides a 2.5V tapping for the ADC reference. U102 provides a buffer from the relatively high impedance of R104 to generate the positive reference. It also in conjunction with R105 provides the precision inverter to generate the negative reference of the same magnitude. U108 switches between the different polarities of reference and is driven by DAC_ REF_ NEG_ L. U113 selects whether a DC reference of the appropriate polarity or the DDS O/P is driven into the I/P of the composite DAC. U113 also selects source of reference for the DDS system. The two options are either the nominal reference, of the appropriate polarity, or the output of the composite DAC. This feature is incorporated so that when in high voltage DC functions the reference to the DDS system and hence the O/P is altered by the composite DAC. For all AC voltage and current functions the DDS is always driven from a static reference and the composite DAC is used to scale the AC voltage. The line used to determine whether an AC or DC reference is applied to the composite DAC is DAC_ DDS_ H_ REF_ L. This line is taken low when in DC functions and high when in all AC functions. DAC_ DDS_ DC_ HV_ H is used to select the reference for the DDS system. In all functions other than the 300 and 1000V DC ranges, this line is held low. The appropriate AC or DC reference coming from pins 15 and 2 of U113, then enters U115. This dual four way multiplexer is used to select the source of input and output for the composite DAC. This feature is provided so that not only can the composite DAC provide a precision linear AC or DC voltage source, but it can also be used as a precision divider for any voltage fed into it. This latter characteristic is used in the impedance functions. In all voltage functions DAC_F0_H and DAC_ F1_ H are held low to select the zero channel of the multiplexer. This causes the reference to be fed into U103. This amplifier is configured as a follower with a small transistor buffer on the output and is used to drive both U107, the trim DAC, U106, the main DAC, and also to provide a reference for the pulse circuitry.

The composite DAC deserves a more detailed explanation. The requirements of the composite DAC are to give 16 or 17 bit linearity which is approximately 10 ppm, a stability of 20 ppm/year, and a T/C of less than 5 ppm/degrees centigrade. This seems like a relatively simple requirement that could be fulfilled by an off the shelf 16 bit DAC. Unfortunately, very few 16 or even 18 bit DACs have true 16 bit linearity. Hence the solution, in fine Datron tradition, is to use relatively low accuracy, but high stability parts, and to measure the errors and take them out in a software characterisation. The DAC used here has one LSB non-linearity guaranteed. This is approximately 250 ppm which is obviously wildly out from what we require. The way in which we achieve the superior linearity performance is to step U106 through each of its 4096 codes and to measure it via U405 and R413 and into the self test set at a gain of 0.5. We used the ADC U408 to measure this. This is a sigma delta converter and has extremely good linearity performance, guaranteed to no worse than 7 ppm. Once the linearity errors of U106 have been measured they can then be compensated with an appropriate adjustment from U107, usually referred to as the trim DAC. R120 and R121 form a resistive summer with the trim DAC contributing only a 274th of that which the main DAC contributes. This allows the trim DAC to make an equivalent 15 bits of correction to the main DAC if required. There is no need to characterize U107 because its contribution is divided by 274, this means that its 1 LSB of non-linearity would cause only 1 ppm non-linearity in the final composite DAC output. This is insignificant. It can also be observed that U108 pin 15 connects into the summing point of the composite DAC output. This is so that a very small offset voltage can be injected through R143. The reason for this is that in DC functions a unipolar DAC that went only from zero to plus full scale would not allow zero offsets in the following gain stages to be calibrated out. This offset is only injected in DCV and DCI.

When in ACV or impedance functions the line RL_ RGC_ H_ EXP_ L is driven high. This switches the output of the offset DAC via R149 onto the input of U103. The purpose of this is to trim out the offset of U103 because this would be unacceptable in impedance functions.

If further information is required on the operation and concepts behind the composite DAC, then the document "20 Bit Composite DAC for DAD65" should be referred to, as this contains an extensive explanation of the ideas and implementation of this technique.

The output of the composite DAC is switched through U115. For everything other than impedance functions this goes into U103. To drive the line DAC_OUT_1 which is fed to the power board for the 30V and 100V ranges and also to the low voltage amplifier for the 300mV and 3V ranges.

U105 usually referred to as the offset DAC is used primarily in self test to generate tickle currents to stimulate the impedance function during selftest. The only other function of it as previously mentioned is to provide an offset trim for U103.

THE DDS SUB-SYSTEM

Direct digital synthesis is a means of generating sine waves of varying frequency whilst maintaining the same clock frequency and hence making the filtering far easier. The idea behind this technique is that a sine wave is loaded in to a look-up table, in this case consisting of U202 and U203. These are a pair of static RAMs which are 8 bits wide and 8K in length. They are always used in parallel, this allows 16 bits of data for the 8,192 locations of storage. U207 and U208 are bi-directional buffers through which the data is loaded into the RAMs and also can be read back from them. U204 and U205 are fast 8 bit latches which means that the relatively slow undefined edges which come out of the RAMs can be re-sync'd and clocked cleanly into the DDS DAC. U201 is the chip that controls all of this and is a 48 bit phase accumulator.

The DDS data is clocked out of the rams via U204 and U205 at 1.25MHz. This data then enters U114, the DDS DAC. As with the other DACs, this is a current output device and therefore has an inverting buffer directly on the output of it. U116 is an AD843. This is a fast bipolar device. U117 is a 200MHz current buffer. This device is in place so that when the sampling gate U119 switches and applies a new voltage onto C115, the sampling cap, the substantial transient currents can be handled relatively well. U119 is a very fast DMOS switch. DDS_ SMPL_ L, is the sample line which drives U119. This is a 1.25MHz waveform which goes active low and enables the gate for only 50 nS . The sampler is in place because U114, the DDS DAC is in fact a relatively slow device and when the output of it is looked at substantial gliches, lasting 500 nS or 600 nS appear on the output of it. By using U119 to sample this output 750 nS after the DAC is updated a relatively accurate level can be achieved and the gliches can be avoided. R130 and C136 provide a high frequency filter to remove the worst of the sharp high frequency edges which would severely upset the following op-amps if they were left. U120 and its surrounding components form a salen-key filter which provides a 2 pole role off at 350KHz. This filter also gives a gain of 1.38. The output of this filter is still unipolar at this point, but by summing this signal with the reference on pin 2 of U118, the DC offset can be removed to provide an AC signal on pin 6 of U118 with no more than 60mV of DC offset. R124, L102 and C125 form the second half of the filtering giving another 2 pole role off at 350KHz. U121 provides a buffer so that this relatively sensitive node does not have to run all over the board and be susceptible to pick-up and loading due to stray capacitance.

THE SELF TEST CIRCUITRY

This instrument has an extensive self-test capability with multiplexers allowing nodes throughout the circuit to be selected and driven into U407. U406 allows a gain of x2, x1, x0.5 or x0.2 to be selected, and this voltage is then driven into U408, the ADC.

FREQUENCY & PULSE

All pulse wave forms of varying marked space are generated by U701, the Actel chip, the actel chip which has a dual counter for this purpose. These counters are clocked from Y701, a 20MHz crystal with an absolute uncertainty of 25ppm. When in pulse functions the Actel chip drives the output circuitry via FREQ_PULSE_H. This line drives directly into U509 which is another fast DMOS switch. This switch selects either the high pulse level or the low pulse level of TP503 and TP504 respectively and then drives the output via a 51ohm resister. The high and low levels for pulse are derived by using the composite DAC in a rather different way. The main DAC is used to control the high level of the pulse and the trim DAC is used to control the low level of the pulse. These 2 DACs enter the pulse circuitry via VH_SET and VL_SET. The two parts of U507 are used to make the previously unipolar DAC outputs into bipolar signals. U505 and 506 are used to buffer the output of this IC. These levels are then fed directly onto the switching inputs of U509. Because U509 can only stand 21 volts maximum between it's power supplies, D513, D514 and the associated transistor buffers are used to provide the reduced power supplies of +12V, -7V.

SELF TEST SUMMARY

Test A01_001

This test measures the main reference on TT101. The self test circuitry causes a approximate -1% loading of the nominal 6.5536V. This does not show up in the internally measured value because any loading of the main reference will cause an equal ratio loading of the ADC reference. The components tested by this measurement are U101 and R104. The ADC gain is -0.2.

Test A01_002

This test measures the positive buffered reference via TT102. The components tested here are U102 and the switching of U108. The ADC gain is -0.2.

Test A01_003

This test measures the negative buffered reference via TT102. The components tested are U102 and the switching of U108. The ADC gain is -0.2.

Test A01_004

This measures the positive reference on DAC_REF_V. This is the point where the main AC or DC reference enters the composite DAC. The components tested are U113, U115, U103 and Q101, Q102. The ADC gain is -0.2.

Test A01_005

This measures the negative reference on DAC_REF_V. The components tested are as A01_004. The ADC gain is -0.2.

Test A01_006

This test measures the main DAC zero on VH_SET. The components tested are U106, U110 and U111. The limits on this test are dominated by the self test input offset. In practice if it is measured with an external volt meter the offset on this point should be less than 30uV (see maths test A01.M01). The ADC gain is -2.

Test A01_007

This test measures the positive full scale via VH_SET. The components tested are U106, U110 and U111. The ADC gain is -0.2.

Test A01_008

This test measures the negative full scale via VH_SET. The components tested are U106, U110 and U111. The ADC gain is -0.2.

Tests A01_009 to Test A01_020

This group of 12 tests measures the linearity of the main DAC, U106. Each bit is measured individually starting with the MSB and ending with the LSB. The ADC gain is -0.5.

Test A01_021

This test measures the trim DAC zero via VL_SET. The components tested are U107 and U112. The ADC gain is -2.

Test A01_022

This test measures the positive full scale via VL_SET. The components tested are U107 and U112. The ADC gain is -0.2.

Test A01_023

This test measures negative full scale via VL_SET. The components tested are U107 and U112. The ADC gain is -0.2.

Tests A01_024 to A01_035

This group of tests measures the linearity of the trim DAC, starting with the MSB, ending with the LSB. The new componants tested are U107. The ADC gain is -0.5.

Test A01_036

This test measures positive full scale of the composite DAC via DAC_OUT_1. The components tested are U115 and U103. The ADC gain is -0.2.

Test A01_037

This test measures negative full scale via DAC_OUT_1. The components tested are U115 and U103. The ADC gain is -0.2.

Test A01_038

This test measures positive full range via DAC_OUT_1. This test measures no previously un-tested circuitry and is included purely to give a reference for later comparative mathematical tests. The ADC gain is -0.2.

Test A01_039

This test measures negative full range via DAC_OUT_1. As with the previous test, this measures no new circuitry and is included purely to give a reference for future comparative mathematical tests. The ADC gain is -0.2.

Test A01_040

This test measures the zero offset of the composite DAC. This tests the zero offset of U103. The ADC gain is -2.

Test A01_041

This test measures the contribution of the trim DAC to the composite DAC output via DAC_OUT_1. The componants tested are the ratio of R120 to R121.

Test A01_042

This test measures the gain of the x 0.75 self test buffer. The componants tested comprises R413 and U405. The ADC gain is -0.5.

Test A01_043

This test checks the zero offset of the offset DAC via TT103. The componants tested are U105 and U109. The ADC gain is -2.

Test A01_044

This test measures positive full scale of the offset DAC via TT103. The componants tested are U105 and U109. The ADC gain is -0.2.

Tests A01_045 to A01_056

This group of tests measures the linearity of the offset DAC, starting with the MSB, ending with the LSB. The componants tested are U105 and U109. The ADC gain is -0.5.

Test A01_057

This test measures the offset zero of the DDS DAC via TT107. The new circuitry tested is U113, U112, U114, U116 and U117. For this test DAC_DDS_DC_HV_H is taken low to select the main reference into U112. The ADC gain is -2.

Test A01_058

This test measures positive full scale out of the DDS DAC via TT107. The componants tested are U113, U112, U114, U116 and U117. The ADC gain is -0.2.

Test A01_059

This test measures negative full scale out of the DDS DAC via TT107. The componants tested are U113, U112, U114, U116 and U117. The ADC gain is -0.2.

Tests A01_060 to A01_071

This group of tests measures the linearity of the DDS DAC via TT107, starting with the MSB, ending with the LSB. The componants tested are U114 and U116. The ADC gain is -0.5.

Test A01_072

This test measures zero coming out of the sample and hold and salen key filter of the DDS sub-system via TT108. The new circuitry tested is U119, U120, D103, D104. The ADC gain is -2.

Test A01_073

This test measures positive full scale via TT108. Because of the gain of 1.38 in the salen key filter the nominal output voltage will be 6.5536V x 1.38. The componants tested are U119, U120, D103, D104. The ADC gain is -0.2.

Test A01_074

This measures negative full scale out of the salen key filter on TT108. As with the previous test, because of the gain of 1.38, the nominal output voltage will be 6.5536V x 1.38. If any problems are encountered with test A01_073 and test A01_074, this may well be due to an anomaly in the power supplies derived from D103 and D104. The componants tested are U119, U120, D103, D104. The ADC gain is -0.2.

Test A01_075

This measures the routing of the composite DAC O/P into the DDS DAC via U113 pins 6 and 7. The componants tested are U113. The ADC gain is -0.2.

Test A01_076

This measures the routing of the DDS DAC O/P through U113 pins 2 and 3 and U115 pins 4 and 8 into the composite DAC I/P via DAC_REF_V. The componants tested are U113, U118, D121, R125. The ADC gain is -0.2.

Test A01_077

This measures the DC offset of the DDS sub-system with 0x800 jammed on the O/P of the DDS DAC through the composite DAC via DAC_REF_V. The componants tested are U119. The ADC gain is -2.

Test A01_078

This measures the DC offset of the DDS sub-system with a 50Hz sine wave on the O/P of the DDS DAC via the composite DAC on DAC_REF_V. The ADC incorperates a digital comb filter at 50Hz and 60Hz so it completely rejects the AC componant of the waveform and just measures the DC offset. The componants tested are U119. The ADC gain is -0.2.

Test A04_001

This measures the DC offset of the self test circuitry when in *-2 gain by selecting the reference zero from the power PCB, (U406 pin 9 on the power board). The componants tested are U406, U407. The ADC gain is obviously -2.

Test A04_002

This measures the DC offset of the self test circuitry when in *-2 gain by selecting the reference zero from the power PCB, (U406 pin 9 on the power board). This test equates directly to Z1 in the polarity characterization. The ADC gain is obviously -2.

Test A04_003

This measures the DC offset of the self test circuitry when in *-0.5 gain by selecting the reference zero from the power PCB, (U406 pin 9 on the power board). This test equates directly to Z2 in the polarity characterization. The componants tested are U406. The ADC gain is obviously -0.5.

Test A04_004

This measures the DC offset of the self test circuitry when in *-0.5 gain including the *0.75 buffer by selecting the O/P of the main and trim DACs to 0x001, this 1bit is just the right amount to cancel the offset injected by R143. The componants tested are U405, U504. This test equates directly to Z3 in the polarity characterization. The ADC gain is -0.5.

Test A04_005

This measures the DC offset of the *-0.75 buffer, by selecting *-0.5 gain including the *0.75 buffer and driving the main and trim DACs to 0x001, this is the same DAC setting as test A04_005. This test equates directly to Z4 in the polarity characterization. The componants tested are U405, U504. The ADC gain is -0.5.

Test A04_006

This measures the mean level of the 150Hz DDS O/P by selecting the *0.75 buffer and driving a 12V pk-pk sine wave into it. The *0.75 buffer is configured as a half wave rectifier. This test equates directly to the 150Hz point in the ACLF flatness characterization. The ADC gain is -0.5.

Test A04_007

This measures the mean level of the 50Hz DDS O/P by selecting the *0.75 buffer and driving a 12V pk-pk sine wave into it. The *0.75 buffer is configured as a half wave rectifier. This test equates directly to the 50Hz point in the ACLF flatness characterization. The ADC gain is -0.5.

Test A05_001

This measures the control voltage of U502 on TT501 when running the Phase Locked Loop on the 200KHz - 800KHz range at 200KHz. The componants tested are U501, U502, U503, U504. The ADC gain is -0.2.

Test A05_002

This measures the control voltage of U502 on TT501 when running the Phase Locked Loop on the 200KHz - 800KHz range at 800KHz. The ADC gain is -0.2.

Test A05_003

This measures the control voltage of U502 on TT501 when running the Phase Locked Loop on the 800KHz - 3.2MHz range at 800KHz. The componants tested are U501, U502, U503, U504. The ADC gain is -0.2.

Test A05_004

This measures the control voltage of U502 on TT501 when running the Phase Locked Loop on the 800KHz - 3.2MHz range at 3.2MHz. The componants tested are U501, U502, U503, U504. The ADC gain is -0.2.

Test A05_005

This measures the control voltage of U502 on TT501 when running the Phase Locked Loop on the 3.2MHz - 10MHz range at 3.2MHz. The componants tested are U501, U502, U503, U504. The ADC gain is -0.2.

Test A05_006

This measures the control voltage of U502 on TT501 when running the Phase Locked Loop on the 3.2MHz - 10MHz range at 10MHz. The ADC gain is -0.2.

Test A05_007

This measures the pulse Hi Limit on TT502 at +6V. The componants tested are U507, U508, Q505. The ADC gain is -0.2.

Test A05_008

This measures the pulse Hi Limit on TT502 at -6V. The componants tested are U507, U508, Q505. The ADC gain is -0.2.

Test A05_009

This measures the pulse Lo Limit on TT502 at +6V. The componants tested are U507, U508, Q506. The ADC gain is -0.2.

Test A05_010

This measures the pulse Lo Limit on TT502 at +6V. The componants tested are U507, U508, Q506. The ADC gain is -0.2.

Test A05_011

This measures the pulse Hi Limit on FREQ_PULSE at +6V with the circuitry running at 50Hz with a 66666:1 mark space ratio. The componants tested are U509. The ADC gain is -0.2.

Test A05_012

This measures the pulse Lo Limit on FREQ_PULSE at -6V with the circuitry running at 50Hz with a 1:66666 mark space ratio. The componants tested are U509. The ADC gain is -0.2.

Test A05_013

This measures the average of the pulse waveform on FREQ_PULSE while running a 50Hz square wave. The componants tested are U509. The ADC gain is -0.2.

Test A09_001

This measures the 300mV range zero at V_I_DRV. The componants tested are U901, U902, U904, U905. The ADC gain is -2.

Test A09_002

This measures the +300mV full range at V_I_DRV. The componants tested are U901, U902, U904, U905. The ADC gain is -2.

Test A09_003

This measures the -300mV full range at V_I_DRV. The componants tested are U901, U902, U904, U905. The ADC gain is -2.

Test A09_004

This measures the 3V range zero at V_I_DRV. The componants tested are U901, U902, U904, U905. The ADC gain is -2.

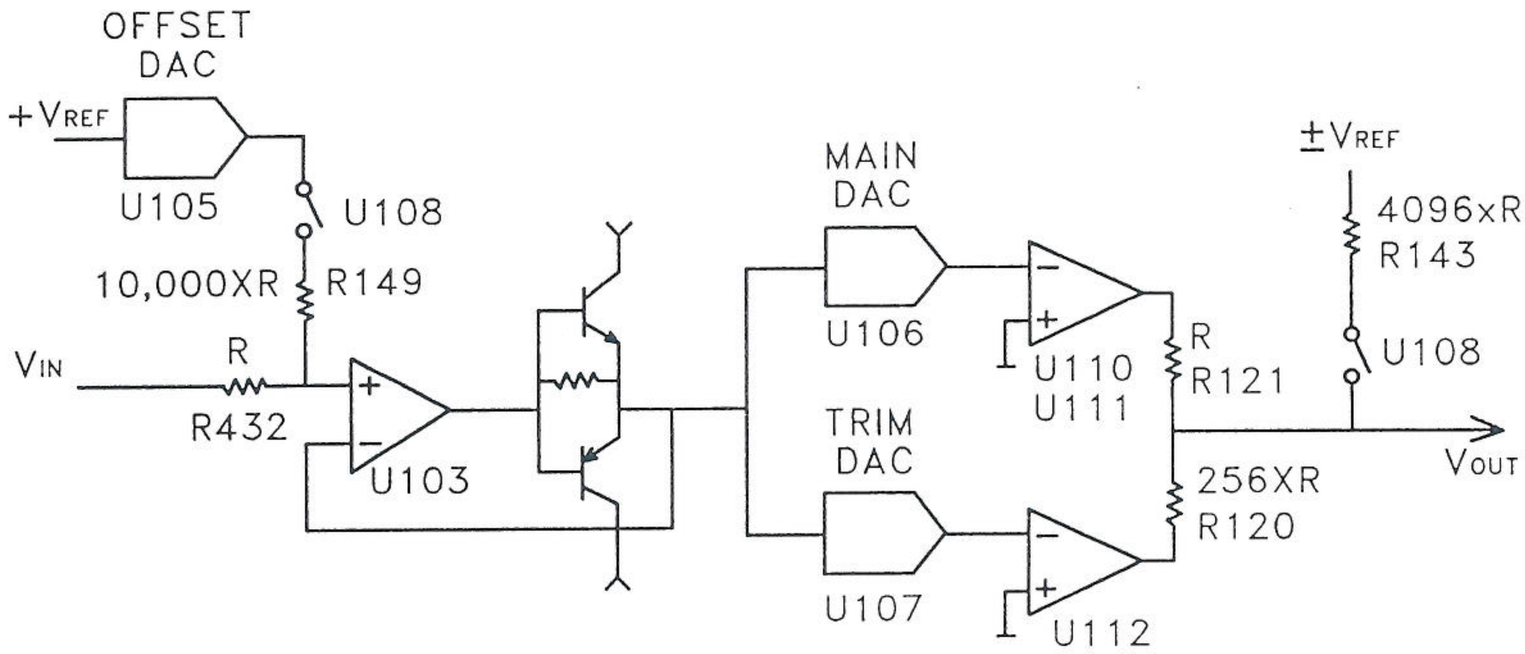
Test A09_005

This measures the +3V full range at V_I_DRV. The componants tested are U901, U902, U904, U905. The ADC gain is -0.5.

Test A09_006

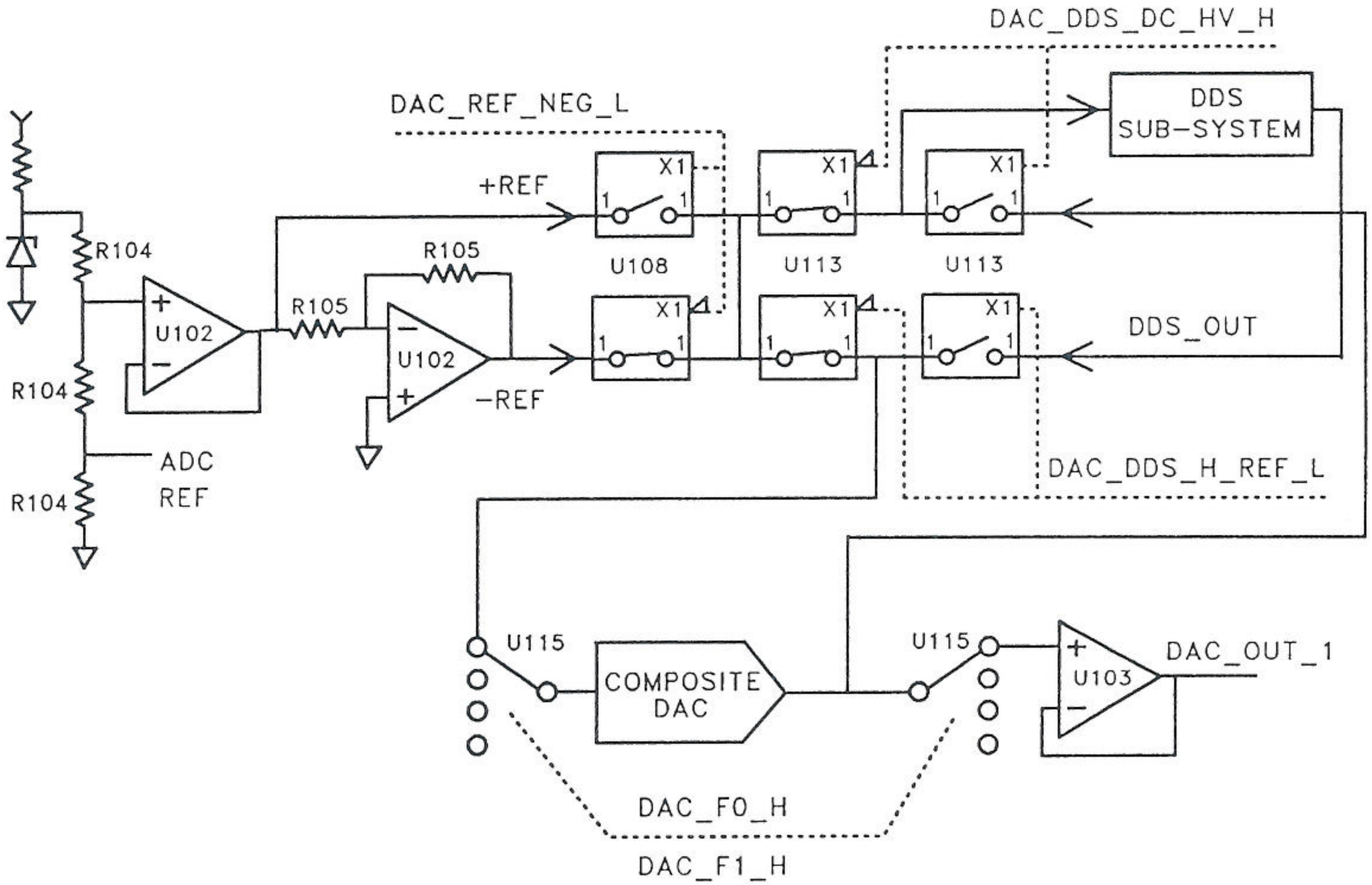
This measures the -3V full range at V_I_DRV. The componants tested are U901, U902, U904, U905. The ADC gain is -0.5.

COMPOSITE DAC



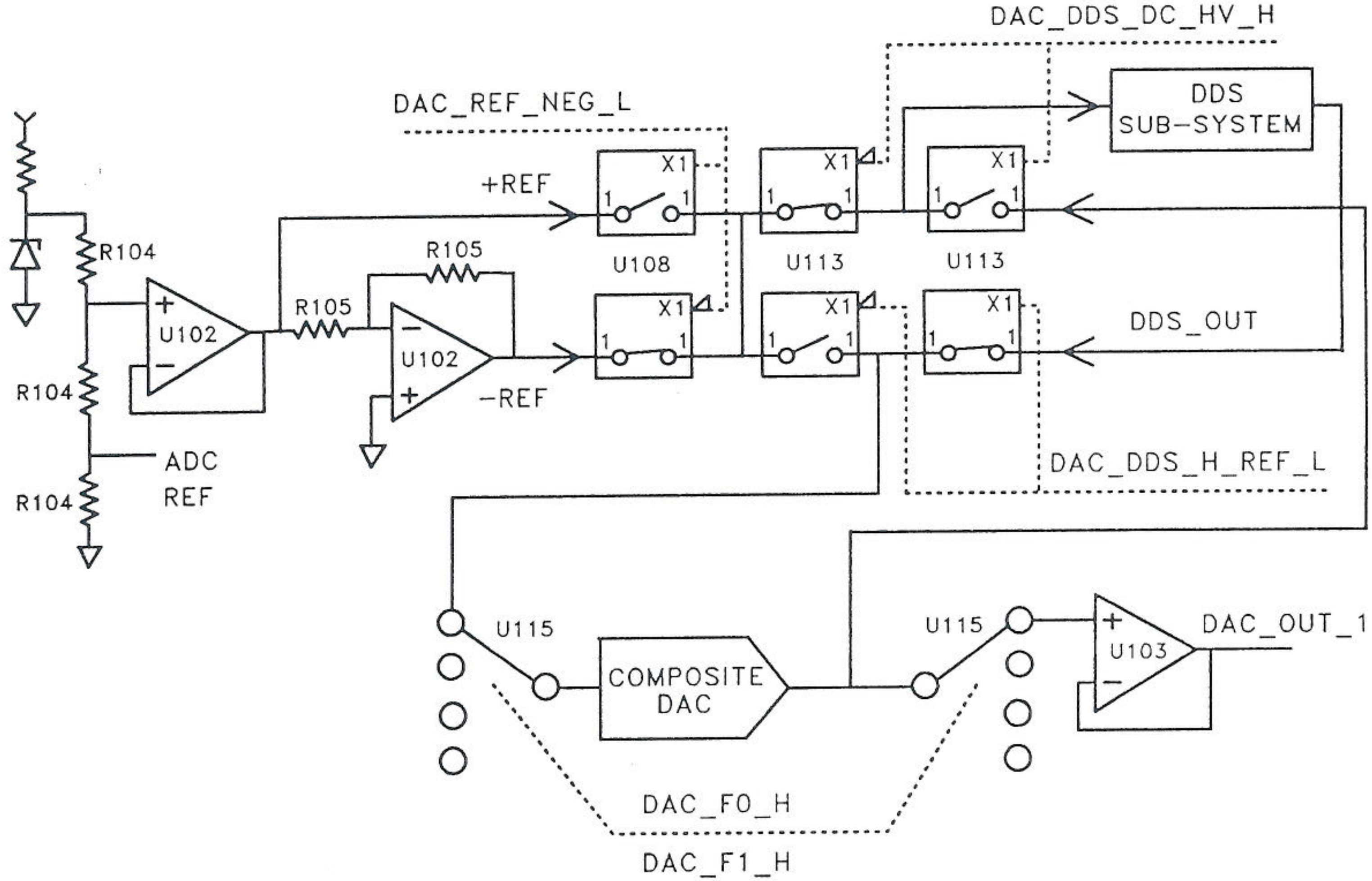
SOURCE SWITCHING

FOR DCI 300uA ⟶ 20A AND DCV 300mV, 3V, 30V



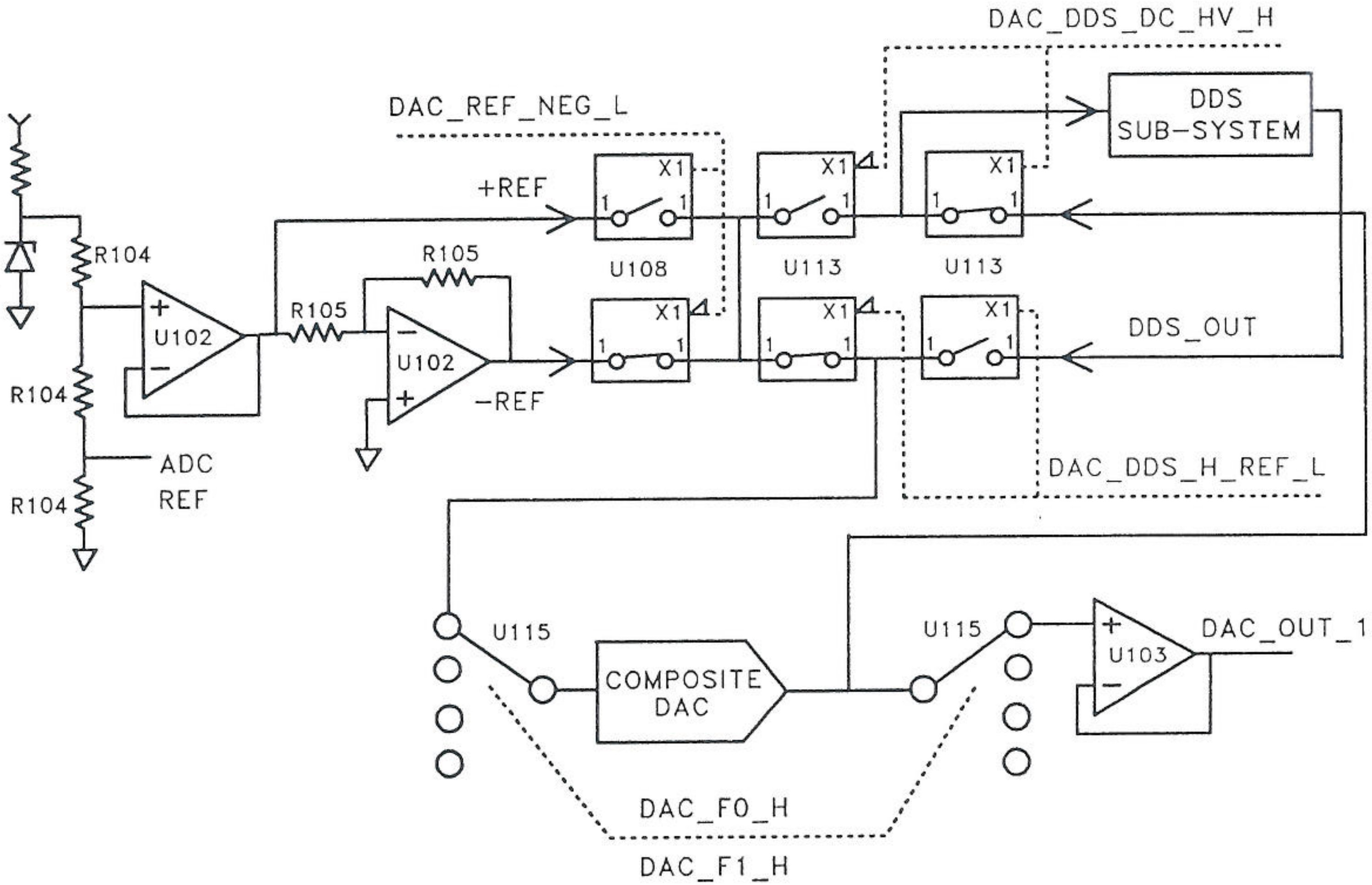
SOURCE SWITCHING

FOR ACI 300uA ⟶ 20A AND ACV 300mV ⟶ 1KV



SOURCE SWITCHING

FOR DCV 300V AND 1KV



Characterization and Usage of 20bit DAC For DAD65

Explanation of the 20bit DAC

All values are requested as a gain ratio (floating point between 0.0 and 1.0) with all range gain corrections (including frequency) and zero corrections already applied. The level of calculation required for a given change in output is not excessive (5 floating point calculations) and should take no more than 1mS.

The characterization measures the Gain errors of the Main and Trim DACs and the Zero of the composite DAC, and then measures and stores the output value of the Main DAC at 4096 points. These values are converted to volts by a standard algorithm that is used on all A-D conversions (assume ADC 0x00000 = -2.5V ADC 0xFFFFF = +2.5V) and stored in floating point format. The values in the Lookup table at position 0x000 and 0xFFF are of particular significance and are given the identifiers Vmin and Vmax respectively, to clarify the examples below. After the linearity characterization the ADC is recalibrated internaly for maximum accuracy and a series of zero measurements taken on various pathways and gain settings. From these measurements the offset errors of the selftest circuitry can be calculated. The final stage is, using the previous errors, to measure and derive cal. corrections for the absolute zero offset and relative gain difference due to flipping the DAC Reference polarity.

On request of a gain (GainRequest) the first step is to apply the polarity dependant offset and gain corrections and then to scale this value relative to Vmin and Vmax (the output extremes of the DAC). Then the previously measured MainGain and MainZero corrections are applied to this to convert it to an integer value (Main) between 0x000 and 0xFFF, this corresponds to the DAC output nearest to the requested value. This value is then adjusted slightly depending on the DAC setting (e.g.:- at an output of more than 0xEF4 2bits are added, at less than 0x10C 2bits are subtracted, there are 3 other evenly spaced correction levels in between e.g.:- +1, 0, -1) this correction is applied because the Trim DAC can only correct the output of the Main DAC by decreasing the voltage at full scale and can only correct by increasing the voltage at Zero. This tweaked version of Main is then used to acquire the nearest output value from the Lookup table. The value returned from the Lookup table is subtracted from the Vrequest hence giving the difference that the Trim DAC has to correct for. This figure then has the TrimGain factor applied to it. This floating point value is then converted to a 12bit integer and has the nominal Trim offset applied to it (the nominal Trim offset is the same value that is sent to the Main DAC) before sending the Trim value to the Trim DAC and the previously calculated value of Main to the Main DAC.

NomFR = +2.5V, ADCnomFS = +5V, ADCbias = -2.5V, NomOffset = 0.00753V.

Note: Unless otherwise stated the pathway for the DAC Characterization is Chrt.

Conversion of ADC readings to Volts.

ADCbitsize = ADCnomFS / 1048576 (1048576 is 2 to the power of 20)
V = ADCreturn * ADCbitsize + ADCbias

Linearity Characterization of the DAC

The DAC now has overall 20 Bit resolution, this is achieved by only having 4 bits overlap between the two DACs. There are various measurements to be taken on initial characterization of the DAC to give Gain and Zero figures for both Main and Trim DACs and also the Linearisation Lookup table for the Main DAC. These constants are derived by the following steps.

All the derived constants of the DAC characterization are in floating point format.
All readings taken should be an average of 4 and converted to volts as above.
If not specified the Trim DAC is always set to the same value as the Main DAC.

1. Trigger ADC internal gain cal. against it's own Ref.

2. Find Gain of Main DAC.

```
MainGain = NomFR/( Reading(Main=0xFFF ) - Reading( Main=0x000 ) )
If ( MainGain < 1.007 OR MainGain > 1.027 ) Error 4501, "Limits: main DAC gain"
```

3. Find Zero offset of the composite Main and Trim DACs.

```
MainZero = Reading( Main=0x000 ) * MainGain
If ( MainZero > 0.0004 OR MainZero < -0.0016 ) Error 4502, "Limits: composite DAC zero"
```

4. Find Gain of Trim DAC.

```
Main = 0x800.
TrimGain = NomFR/( Reading( Trim=0xFFF ) - Reading( Trim=0x000 ) )
If ( TrimGain > 307 OR TrimGain < 205 ) Error 4503, "Limits: trim DAC gain"
```

6. Fill Lookup table.

```
For ( n=0; n<4096; n++ )
        {
        Lookup[n] = Reading( Main = n, Trim = n );
        If ( n>0 )
                {
                bitcheck = Lookup[n] - Lookup[n-1];
                If  ( bitcheck > (NomFR / 2048) OR bitcheck < 0.0 )
                                                        Error 4505, "Limits: main DAC linearity"
                /*      The above line checks the DAC to plus or minus 1bit          */
                }
        }
```

7. On Linearity Error fill the Lookup table with Default values.

```
defaultval = -0.0006
defaultstep = NomFR / 4095

For ( n=0; n<4096; n++ )
        {
        Lookup[n] = defaultval;
        defaultval += defaultstep;
        }
```

Polarity Characterization of the DAC

1. Trigger ADC internal gain cal. against it's own Ref.

2. Measure Zeros For Polarity Characterization.

Z1 = Reading(Chrt_zpg2, Main = 0x000, Trim = 0x000) (A04.002)
If (Z1 > 1e-3 OR Z1 < -1e-3) Error 4507, "Limits: gain of 2 zero"

Z2 = Reading(Chrt_zpg05 , Main = 0x000, Trim = 0x000) (A04.003)
If (Z2 > 700e-6 OR Z2 < -700e-6) Error 4508, "Limits: gain of 0.5 zero"

Z3 = Reading(Chrt_opg05 , Main = 0x001, Trim = 0x001) - Z2 (A04.004)
If (Z3 > 1e-3 OR Z3 < -1e-3) Error 4509, "Limits: DAC output zero"

Z4 = Reading(Chrt_Pos , Main = 0x001, Trim = 0x001) - Z2 (A04.005)
If (Z4 > 1.5e-3 OR Z4 < -1.5e-3) Error 4510, "Limits: 0.75 buffer zero"

Z5 = (Z4 - (Z3 * -0.75) + Z2)

3. Measure DAC Zeros and Full Ranges to Derive Corrections.

scale = -5.33333333

PosZero = (Reading(Chrt_ppg2, Main = 0x000, Trim = 0x000) - Z1) / scale
If (PosZero > 1e-3 OR PosZero < 200e-6) Error 4511, "Limits: DAC posative zero"

NegZero = (Reading(Chrt_npg2, Main = 0x000, Trim = 0x000) - Z1) / scale
If (NegZero > -200e-6 OR NegZero < -1e-3) Error 4512, "Limits: DAC negative zero"

PosFR = Reading(Chrt_Pos, Main = 0xFFF, Trim = 0xFFF) - Z5
If (PosFR > -2.443969 OR PosFR < -2.46853) Error 4513, "Limits: DAC posative FR"

NegFR = Reading(Chrt, Main = 0xFFF, Trim = 0xFFF) - Z5
If (NegFR > 2.46853 OR NegFR < 2.443969) Error 4514, "Limits: DAC negative FR"

GainFactor = ((PosFR - PosZero) / (NegFR - NegZero)) * -1
If (GainFactor > 1.005 OR GainFactor < 0.995) Error 4515, "DAC ±FR Ratio Failure"

PosZero = PosZero / (Vmax - Vmin)

NegZero = (NegZero / (Vmax - Vmin)) / -GainFactor

Phil Harbord **13 MAY 93**

Conversion of GainRequest to Main and Trim DAC Outputs.

The following steps are required to convert an absolute ratio request (0 to 1.0) to two 12bit integers for the DACs. Any Gain, Flatness, Offset constants for a given range are assumed to be applied to GainRequest prior to calling this routine.

Bit = NomFR / 4095

The constant Bit is the voltage value of one bit on either DAC if scaled to full range.

Vmax = Lookup[0xFFF]
Vmin = Lookup[0x000]

GainRequest = 0.0 to 1.0

1. If (Polarity = Pos) GainRequest = GainRequest - PosZero

2. If (Polarity = Neg) GainRequest = (GainRequest - NegZero) * GainFactor

3. Vrequest = (GainRequest * (Vmax - Vmin)) + Vmin

4. Calculate the Bit code for the Main DAC, also the Lookup table code.

   Main = (Vrequest * MainGain - MainZero) / Bit

5. Apply Scale dependant Adjustment to Main.

   Main = Main + ((Main - 2048) / 890)   Integer division.
   If Main exceeds the bounds 0 to 4095 then correct it to the nearest boundary (eg: -2 becomes 0)

6. Extract the DAC output voltage from the Lookup table.

   Output = Lookup[Main]

7. Calculate the error correction required from the Trim DAC to bring the output to the requested value.

   Vtrim = (Vrequest - Output) * TrimGain

8. Calculate the Bit code required for the Trim DAC.

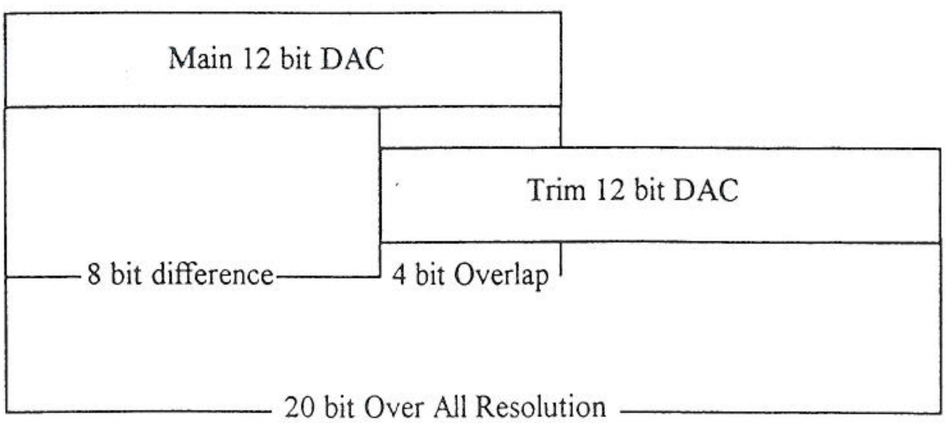
   Trim = (Vtrim / Bit) + Main

9. Output calculated values to the DACs

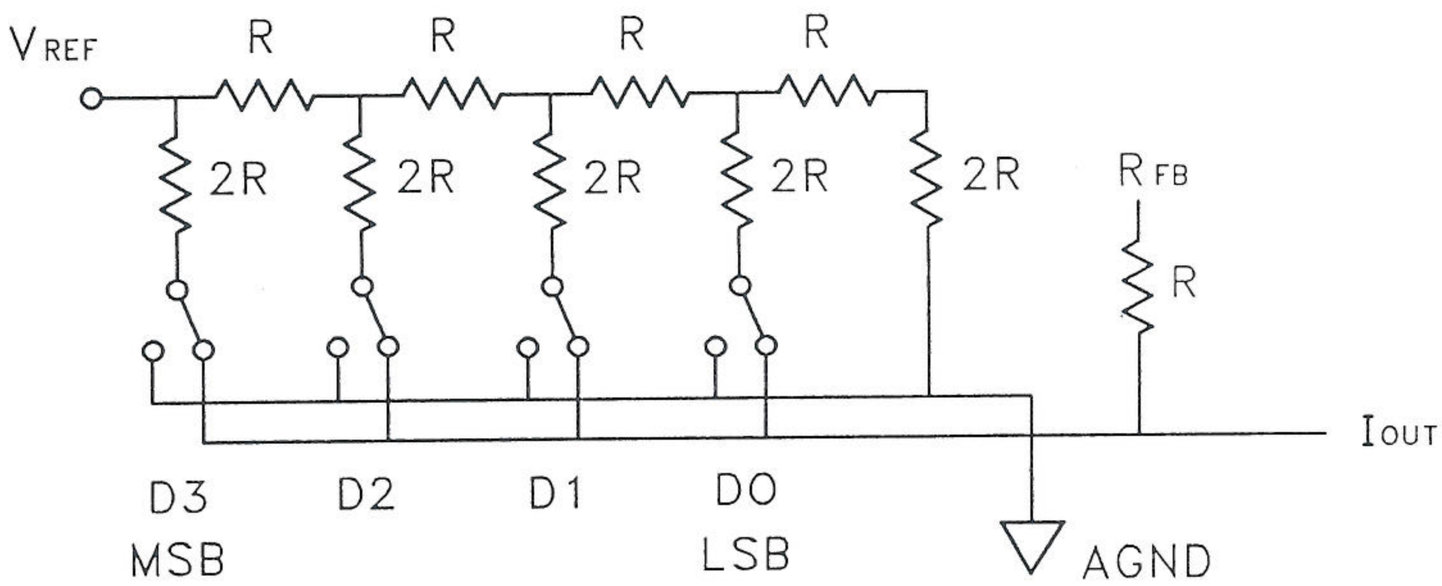
   Send Main to the Main DAC.
   Send Trim to the Trim DAC.

The variables used are of the type specified below.

static float PosZero, NegZero, GainFactor, MainGain, MainZero, TrimZero ;
signed int Main, Trim, Offset ;
float Bit, Output, Vtrim, Vrequest, OffsetBitVal, Z1, Z2, Z3, Z4, Z5, PosFR, NegFR, Scale ;



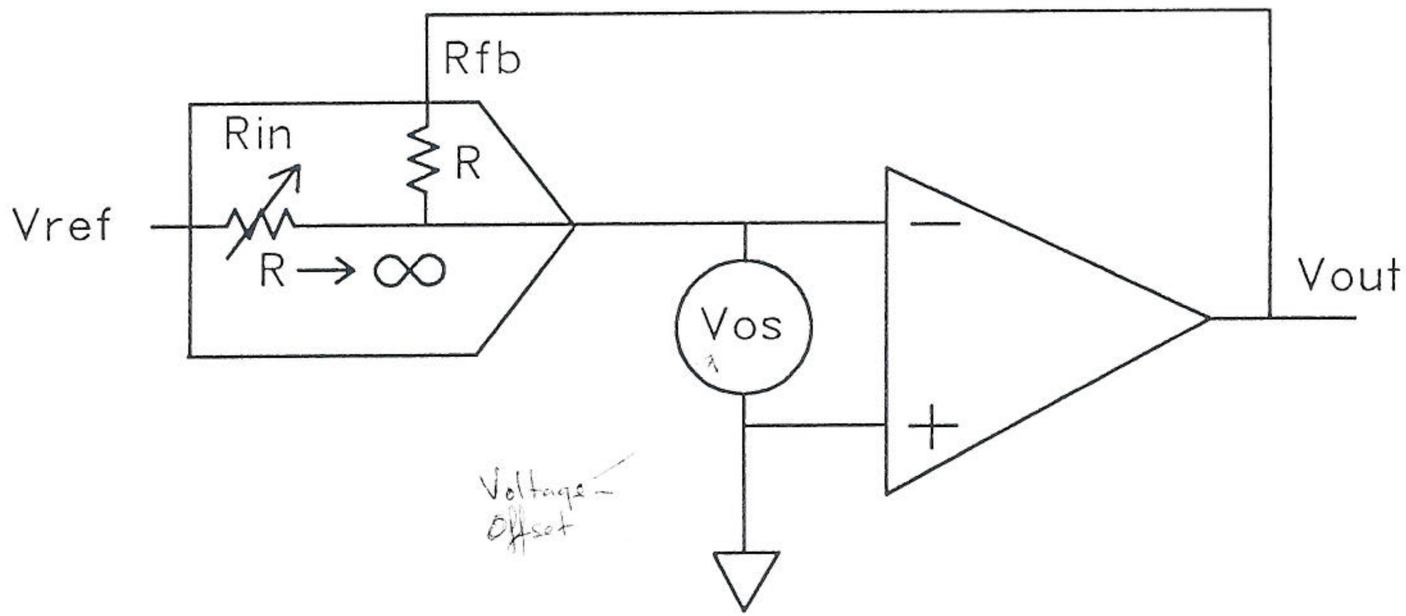
R, 2R LADDER DAC



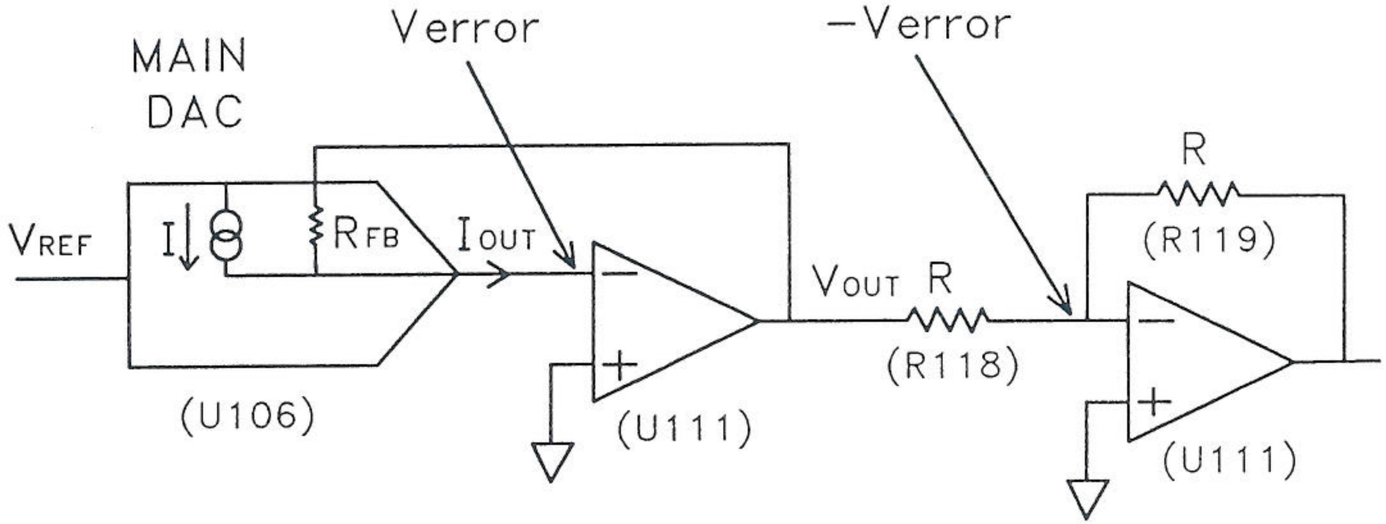
DAC SENSITIVITY TO AMPLIFIER OFFSET VOLTAGE

IF Vref = 0 AND Rin = R THEN Vout = Vos*2

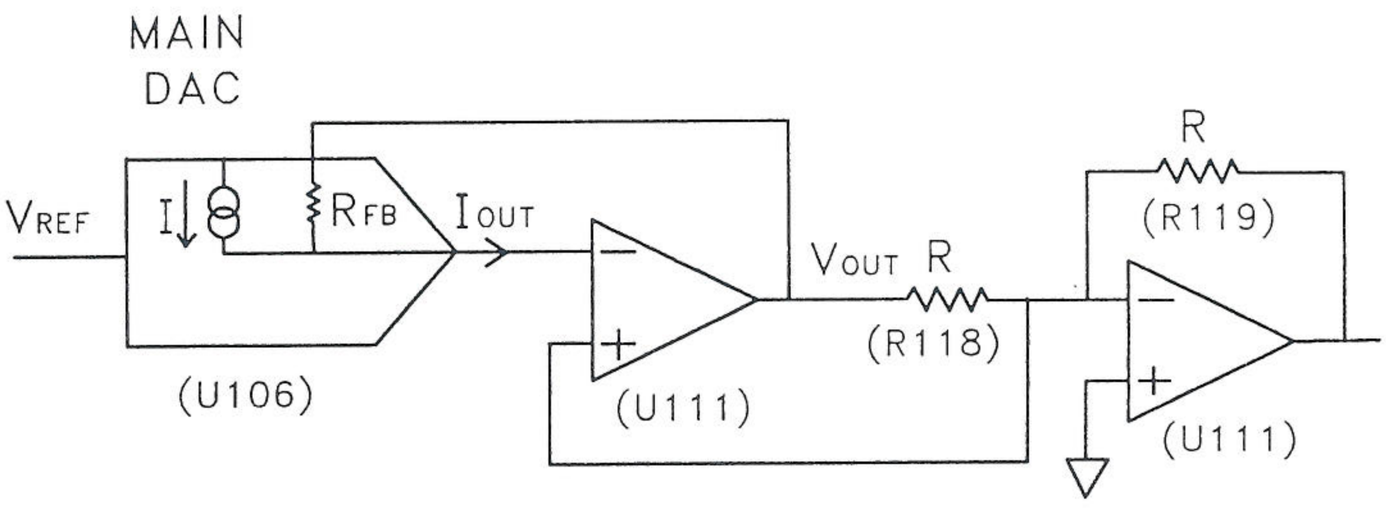
IF Vref = 0 AND Rin = ∞ THEN Vout = Vos



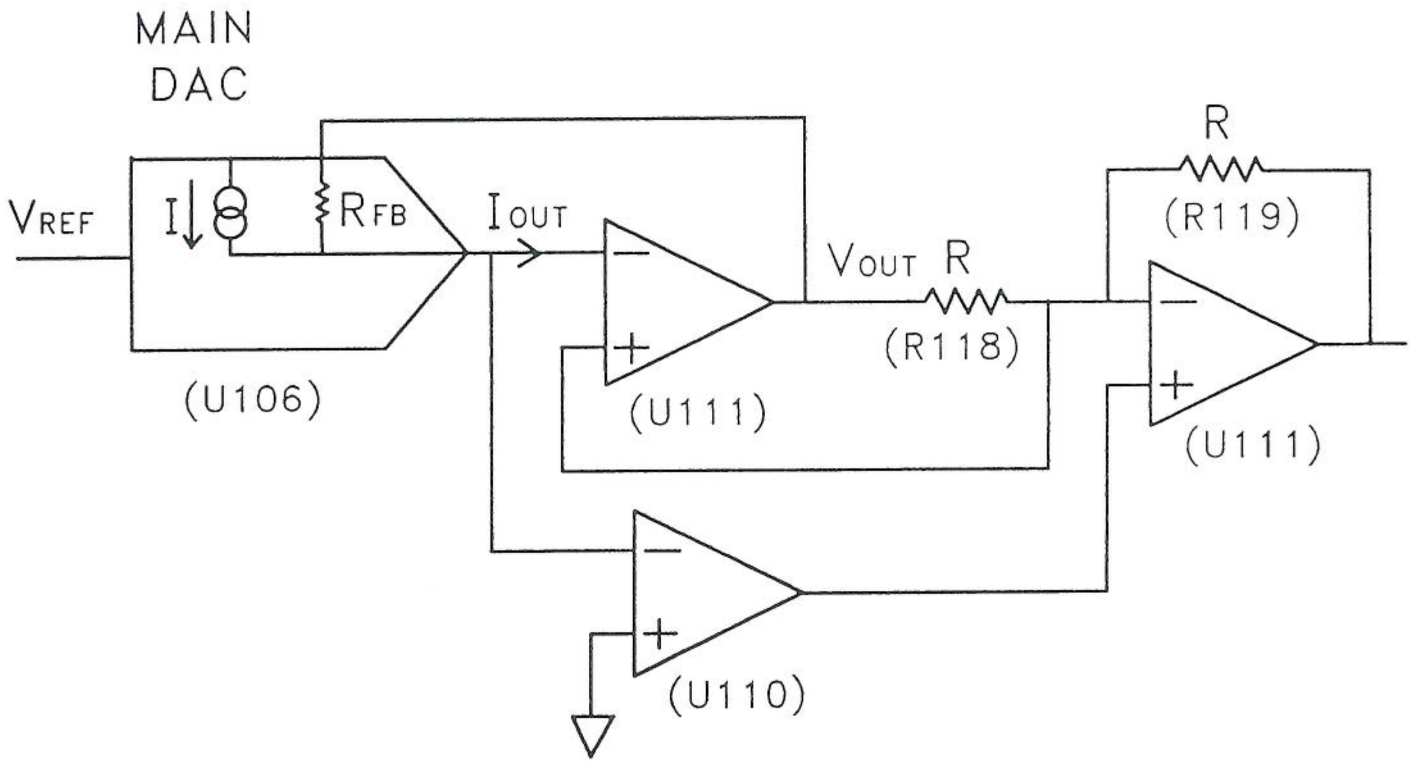
MAIN DAC AMP 1



MAIN DAC AMP 2

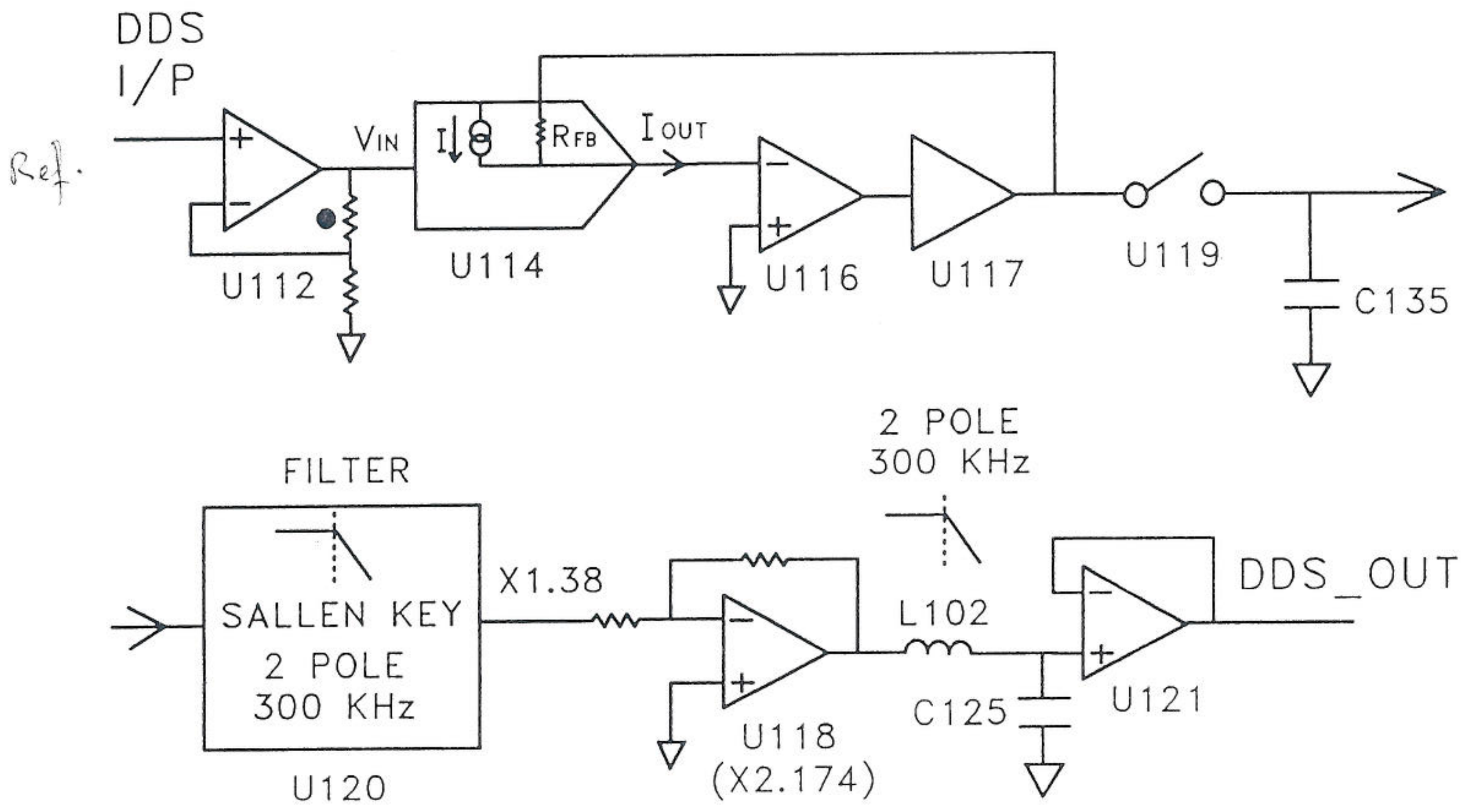


MAIN DAC AMP 3

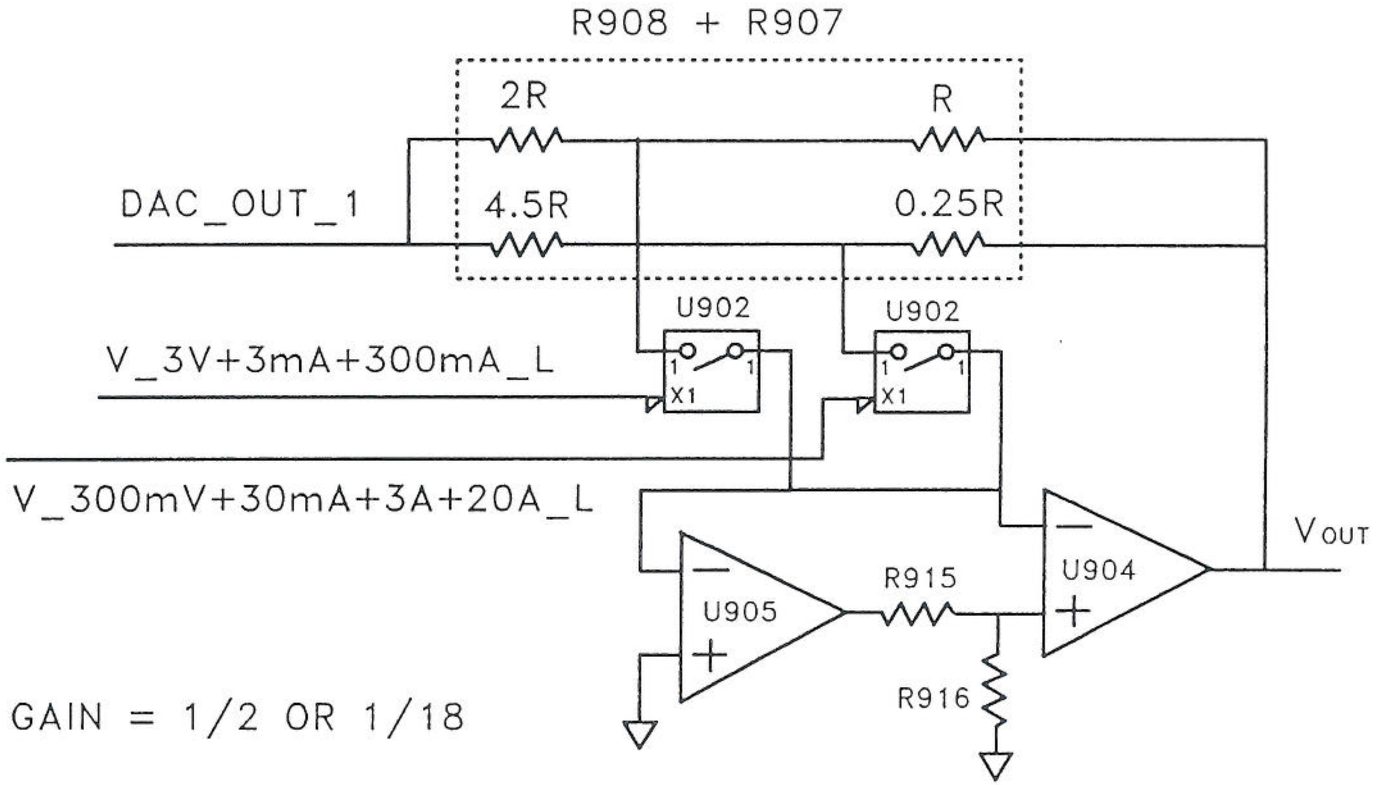


P3

DDS SUB-SYSTEM

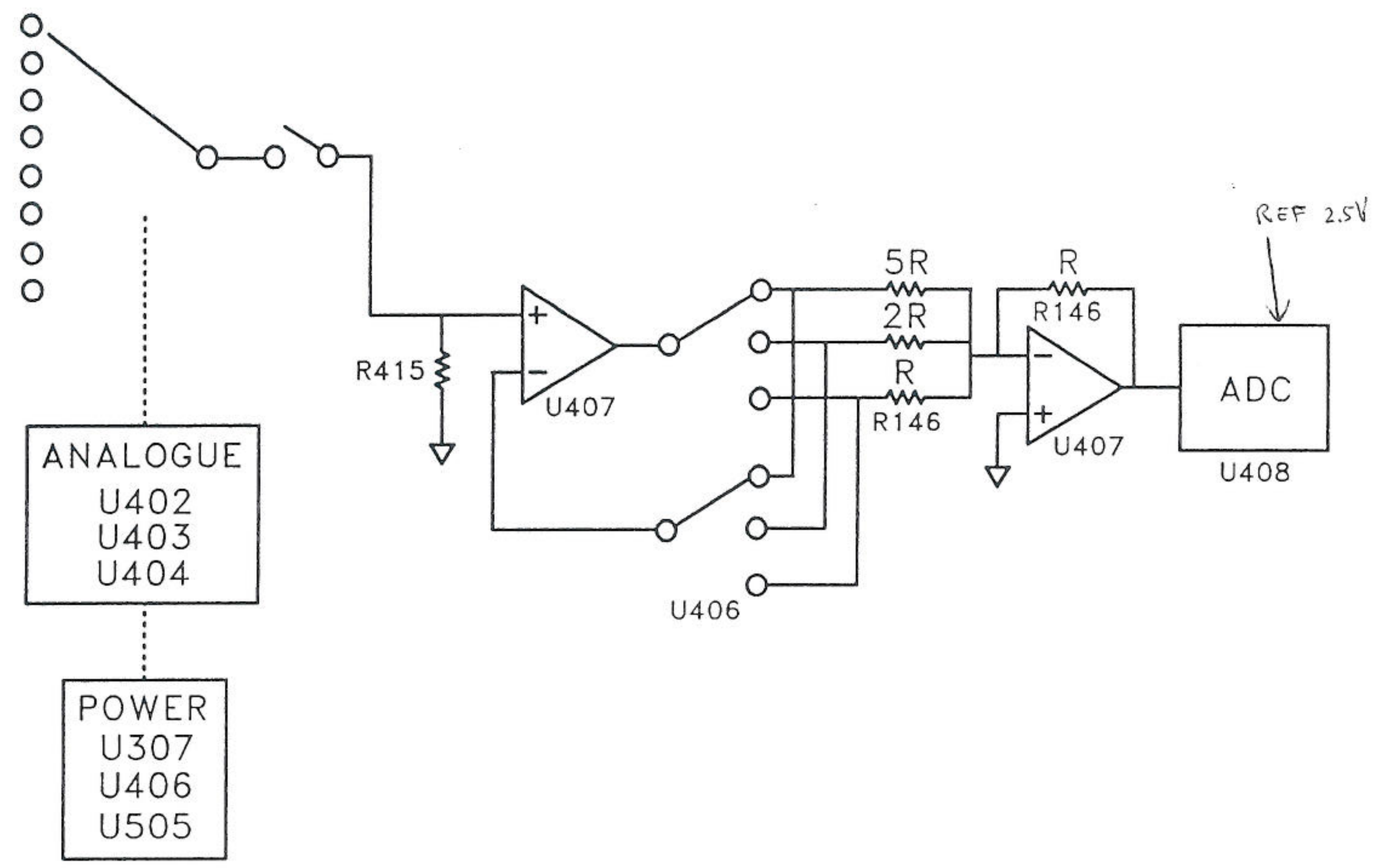


LV OUTPUT AMP



GAIN = 1/2 OR 1/18

SELF TEST


ANALOGUE
U402
U403
U404
POWER
U307
U406
U505
R415
U407
U406
5R
2R
R
R146
R
R146
U407
REF 2.5V
ADC
U408

Control of the Main DAC for Pulse and Frequency

Conversion of VLHigh and VLLow to DAC Codes for Pulse and Freq Functions.

The conversion of the high and low voltage request levels to two 12bit binary codes is very straight forward as both levels use the same conversion algorithm, this is achieved as follows.

BitsPerVolt = 4095 / -13.1072 (eg: (2^12) / (2 * 6.5536))

1. Convert VLHigh to Main.

   Main = 2048 + VLHigh * BitsPerVolt

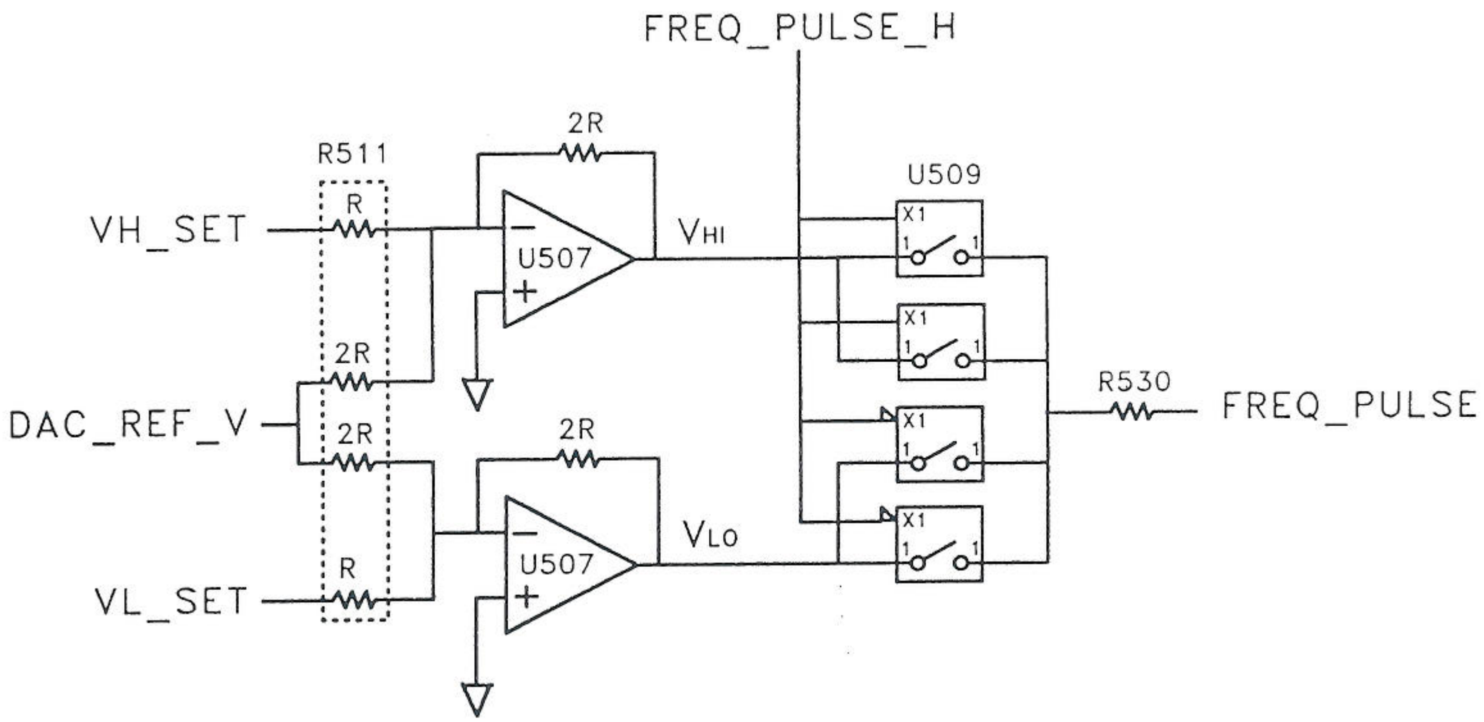
2. Convert VLLow to Trim.

   Trim = 2048 + VLLow * BitsPerVolt

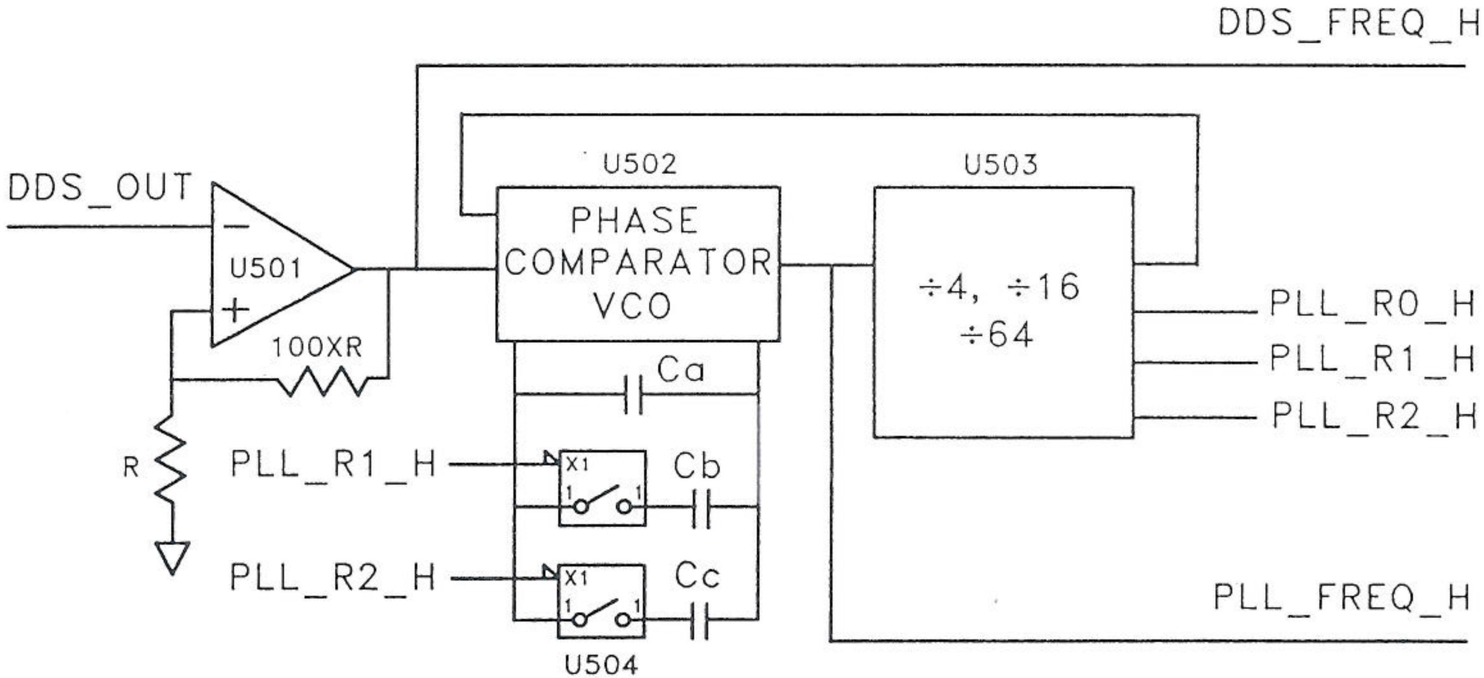
3. Send Values to DACs.

   Send Main to Main DAC.
   Send Trim to Trim DAC.

FREQUENCY + PULSE OUTPUT STAGE



FREQUENCY PHASE LOCKED LOOP



	0.5Hz → 200KHz	200KHz → 800KHz	800KHz → 3.2MHz	3.2MHz → 10MHz
PLL_R0_H	X	1	1	1
PLL_R1_H	X	0	1	1
PLL_R2_H	X	0	0	1
DDS FREQ	0.5Hz → 200KHz	50KHz → 200KHz	50KHz → 200KHz	50KHz → 156.25KHz
CAP		Ca+Cb+Cc	Ca+Cb	Ca

LF AC Characterization

This characterization is intended to remove a systematic error in the DDS sub-system. The idea is to drive the *0.75 selftest buffer with the DDS output via the composite DAC at 50Hz and 150Hz and measure the DC offset in both cases. Then the *0.75 selftest buffer is switched into a precision half wave rectifier using TST_ACV_L and used to measure the same frequencies. This effectively measures the flatness error between the above 2 frequencies and also removes DC offsets which may vary slightly with frequency. Now an error term Max_Error can be derived which is the maximum error that this particular effect can cause, how ever low the output frequency. The correction is applied to both ACV and ACI functions if the requested frequency is below 152.6Hz (1.25MHz / 8192).

OffsetDAC = 0x800
All measurements are an average of 32 readings.

Measurement of LF AC Flatness

1. Load DDS look up table with a sine wave.

2. Set Char_ac pathway.

3. OffsetA = (MainDAC = 0xA5B, TrimDAC = 0xA5B, DDS_Freq = 150Hz)

4. OffsetB = (MainDAC = 0xA5B, TrimDAC = 0xA5B, DDS_Freq = 50Hz)

5. Set Char_lfac pathway.

6. ReadingA = (MainDAC = 0xA5B, TrimDAC = 0xA5B, DDS_Freq = 150Hz)

7. ReadingB = (MainDAC = 0xA5B, TrimDAC = 0xA5B, DDS_Freq = 50Hz)

8. If (ReadingA > -0.5 OR ReadingB > -0.5)
```
{
Max_Error = 0
Errror 4521, "LF AC Chrctn impossable: default set"
/*    Do not abort the characterization this is an acceptable result    */
}
```

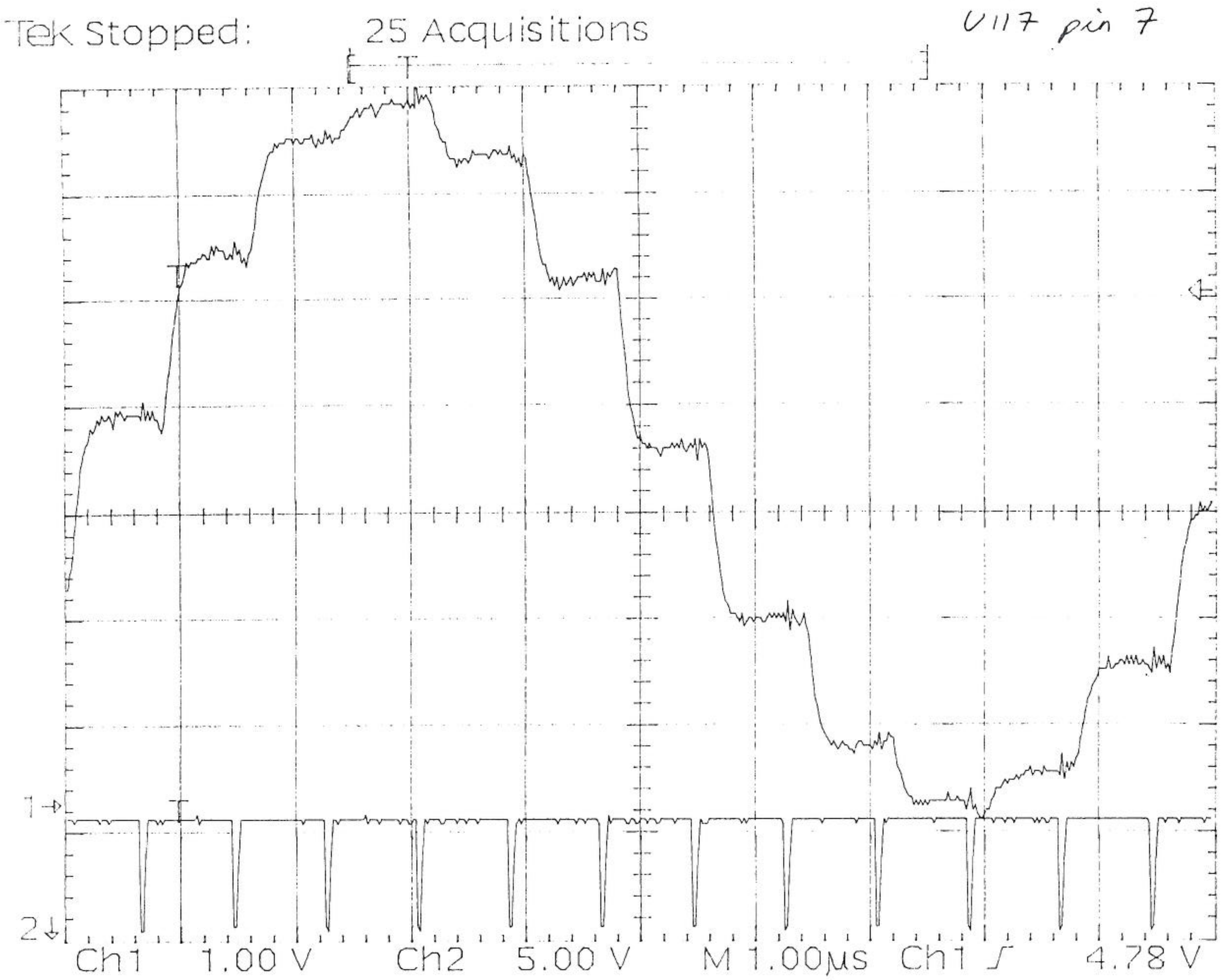
9. Max_Error = (((ReadingB - (OffsetB * 0.5)) / (ReadingA - (OffsetA * 0.5))) -1) * 1.52513

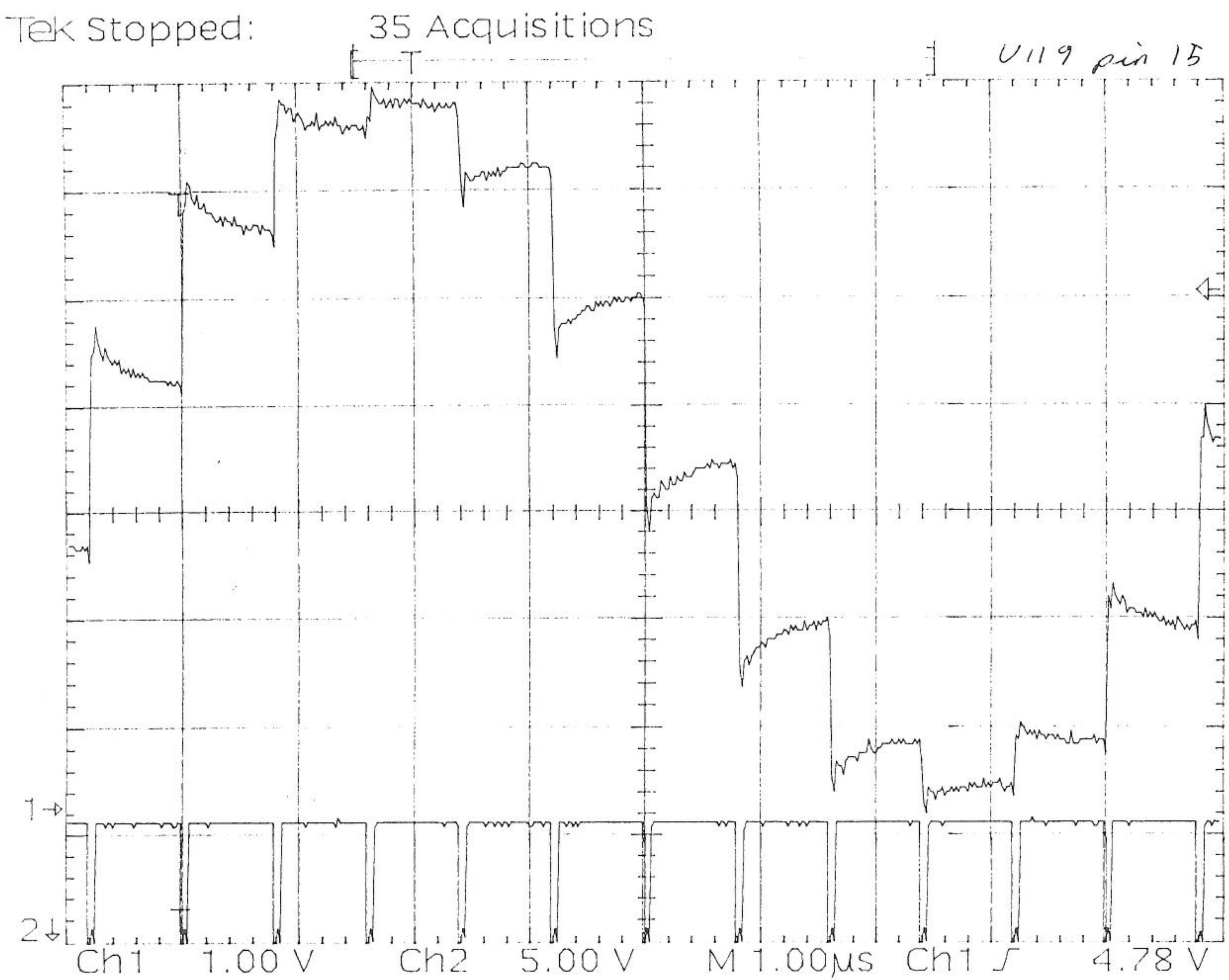
10. If (Max_Error > 0.001 OR Max_Error < -0.001)
```
{
Max_Error = 0
Errror 4522, "Excess LF AC flatness"    Abort
}
```

Application of LF AC Correction.

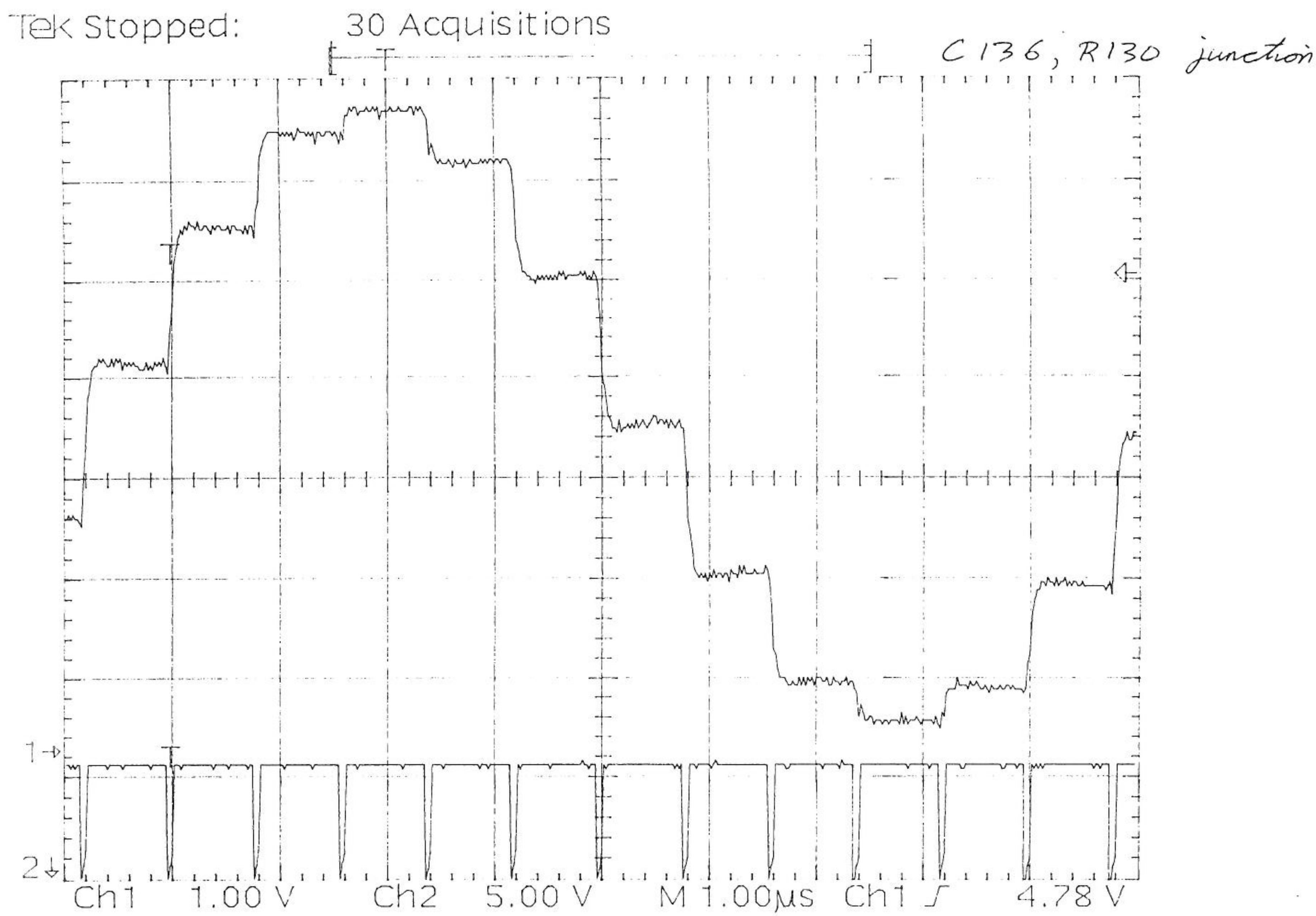
1. if (Frequest < 152.6)
```
{
LF_Correction = 1 + ( ( 1 - ( Frequest / 152.6 ) ) * Max_Error )
GainRequest = GainRequest * LF_Correction
}
```

The above correction should be applied to the GainRequest after all cal. corrections have been done. It is important that the correction is applied after the point were GainRequest is read back for calibration purposes (the Actual value of the cal pair).

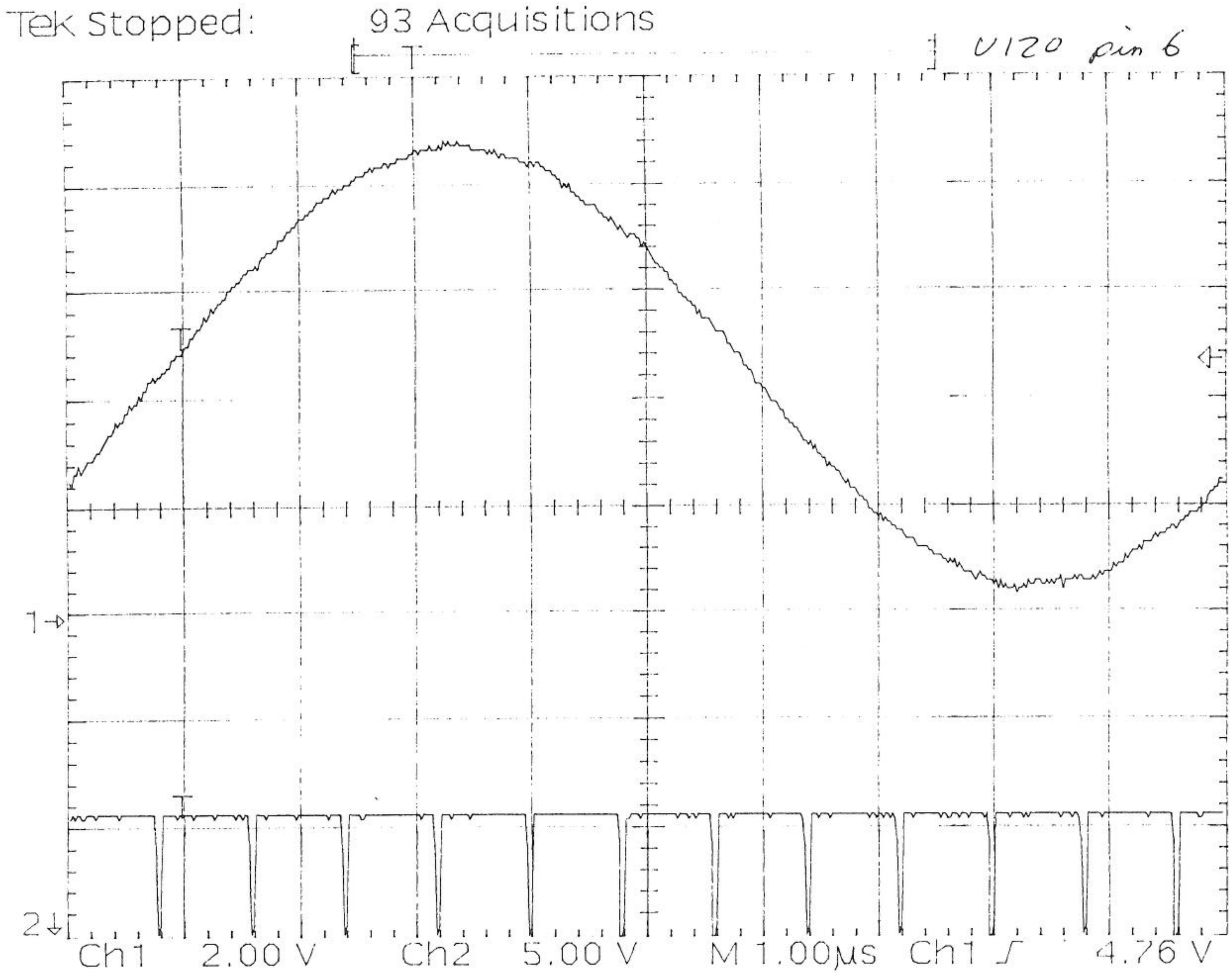

Tek Stopped:
25 Acquisitions
U117 pin 7
Ch1 1.00 V
Ch2 5.00 V
M 1.00µs
Ch1 ∫ 4.78 V

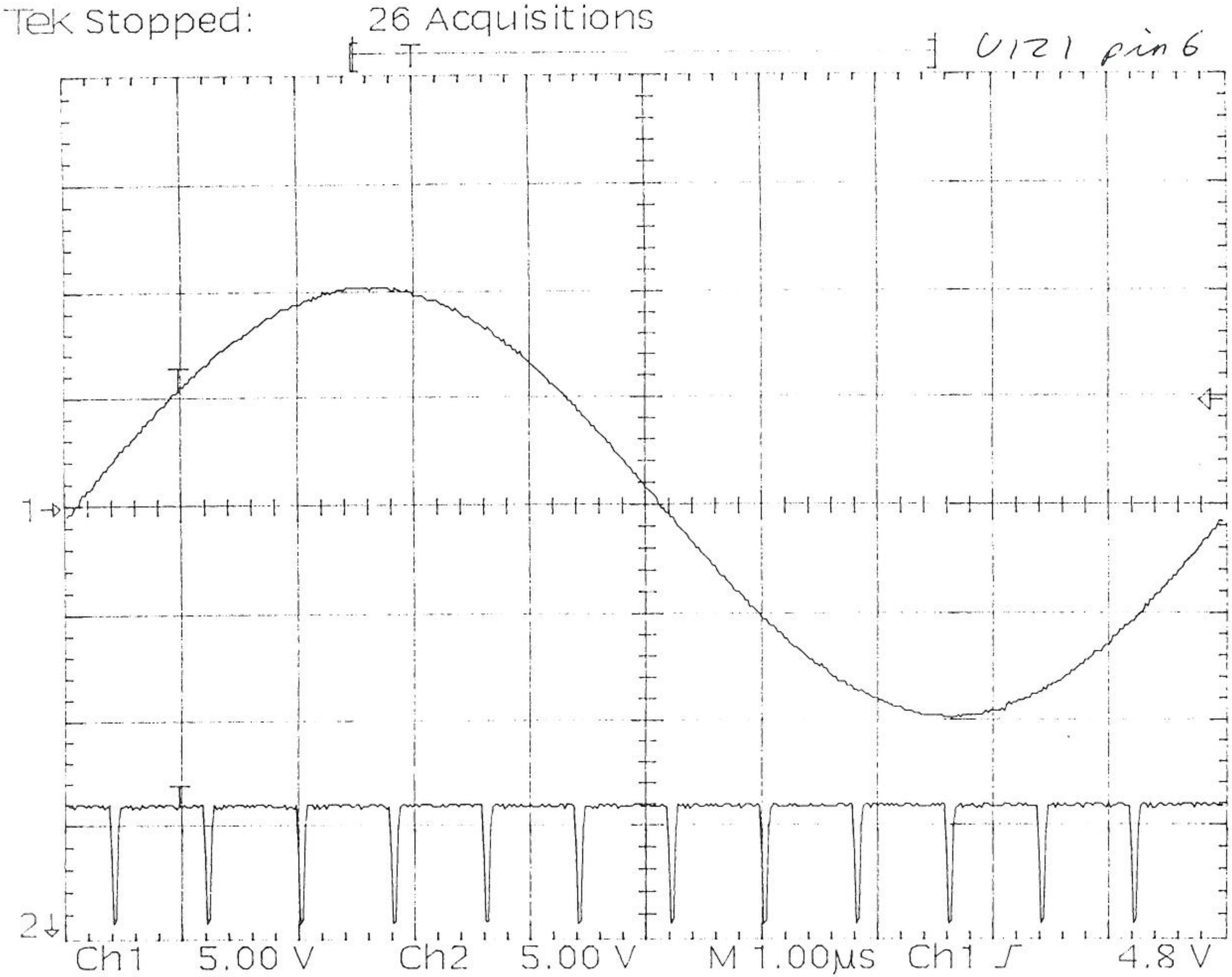


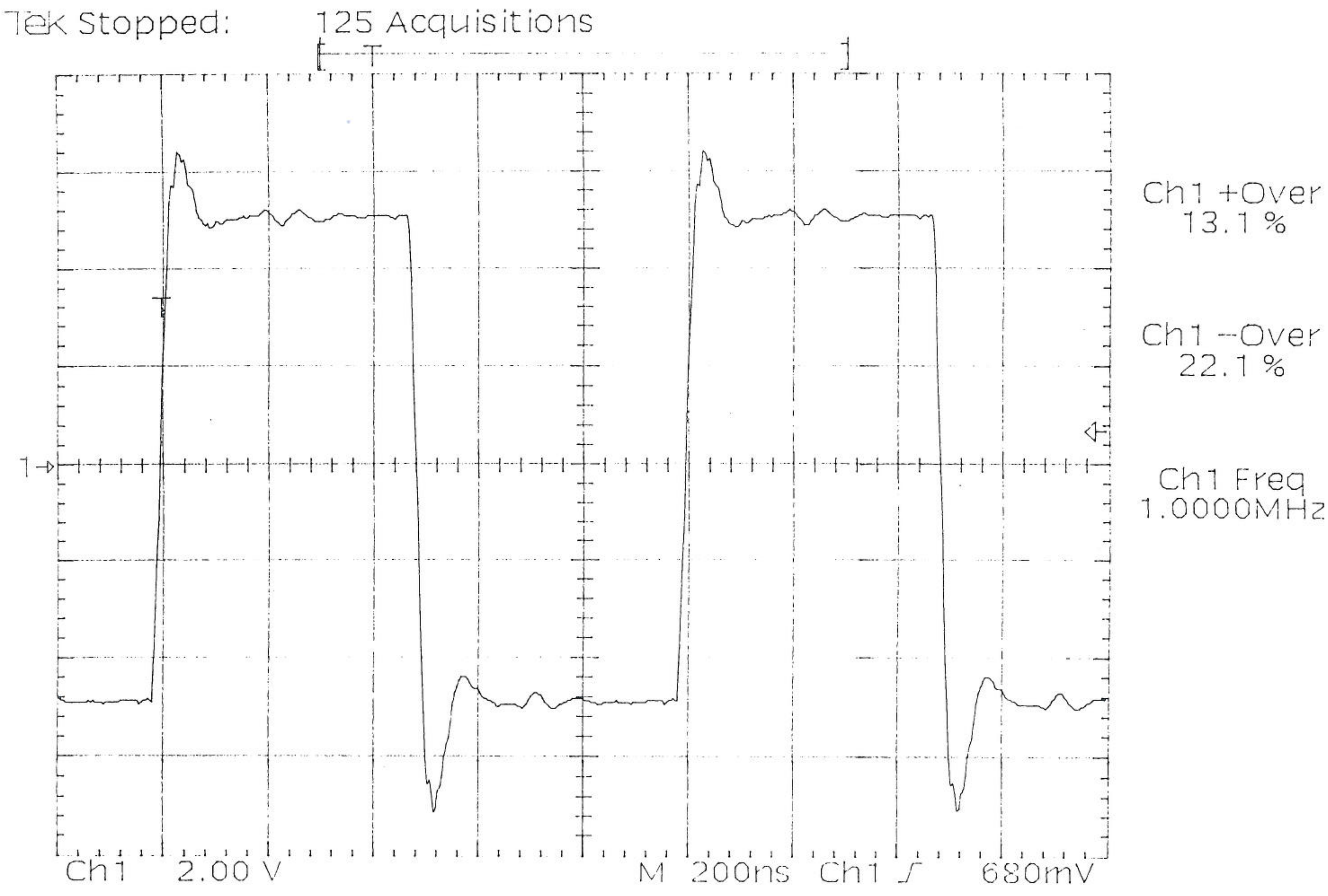
Tek Stopped: 35 Acquisitions
U119 pin 15
1
2
Ch1 1.00 V Ch2 5.00 V M 1.00µs Ch1 ∫ 4.78 V

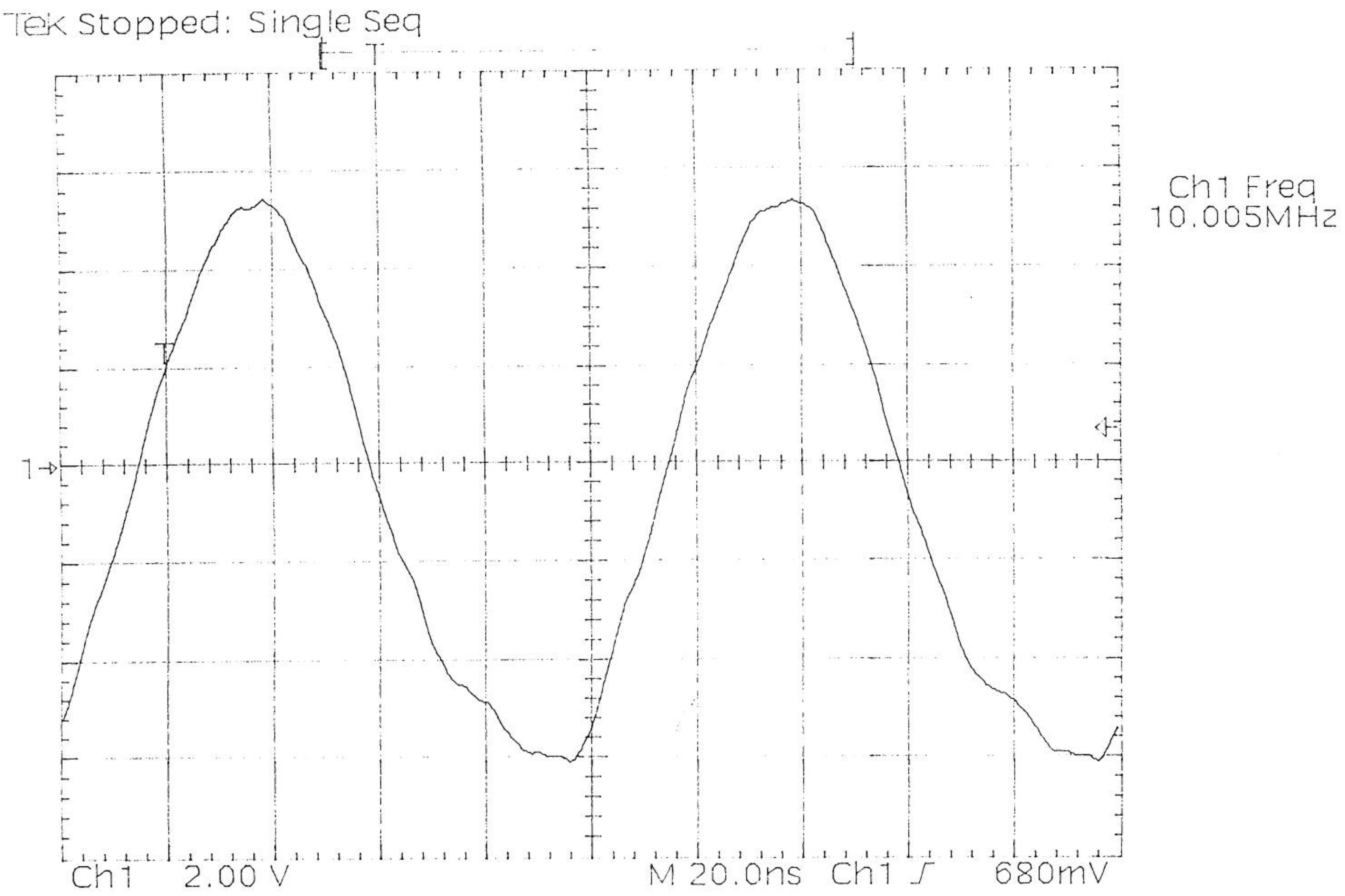


Tek Stopped:
30 Acquisitions
C136, R130 junction
1
2
Ch1 1.00 V
Ch2 5.00 V
M 1.00μs
Ch1 ∫ 4.78 V


Tek Stopped:
93 Acquisitions
U120 pin 6
1
2
Ch1 2.00 V
Ch2 5.00 V
M 1.00µs Ch1 ∫ 4.76 V


Tek Stopped:
26 Acquisitions
U121 pin 6
Ch1 5.00 V
Ch2 5.00 V
M 1.00µs
Ch1 ∫ 4.8 V


Tek Stopped: 125 Acquisitions
Ch1 +Over
13.1 %
Ch1 −Over
22.1 %
Ch1 Freq
1.0000MHz
Ch1 2.00 V
M 200ns Ch1 ∫ 680mV


Tek Stopped: Single Seq
Ch1 Freq
10.005MHz
Ch1 2.00 V
M 20.0ns Ch1 ∫ 680mV

ACTIVE Z (RES. F'N)

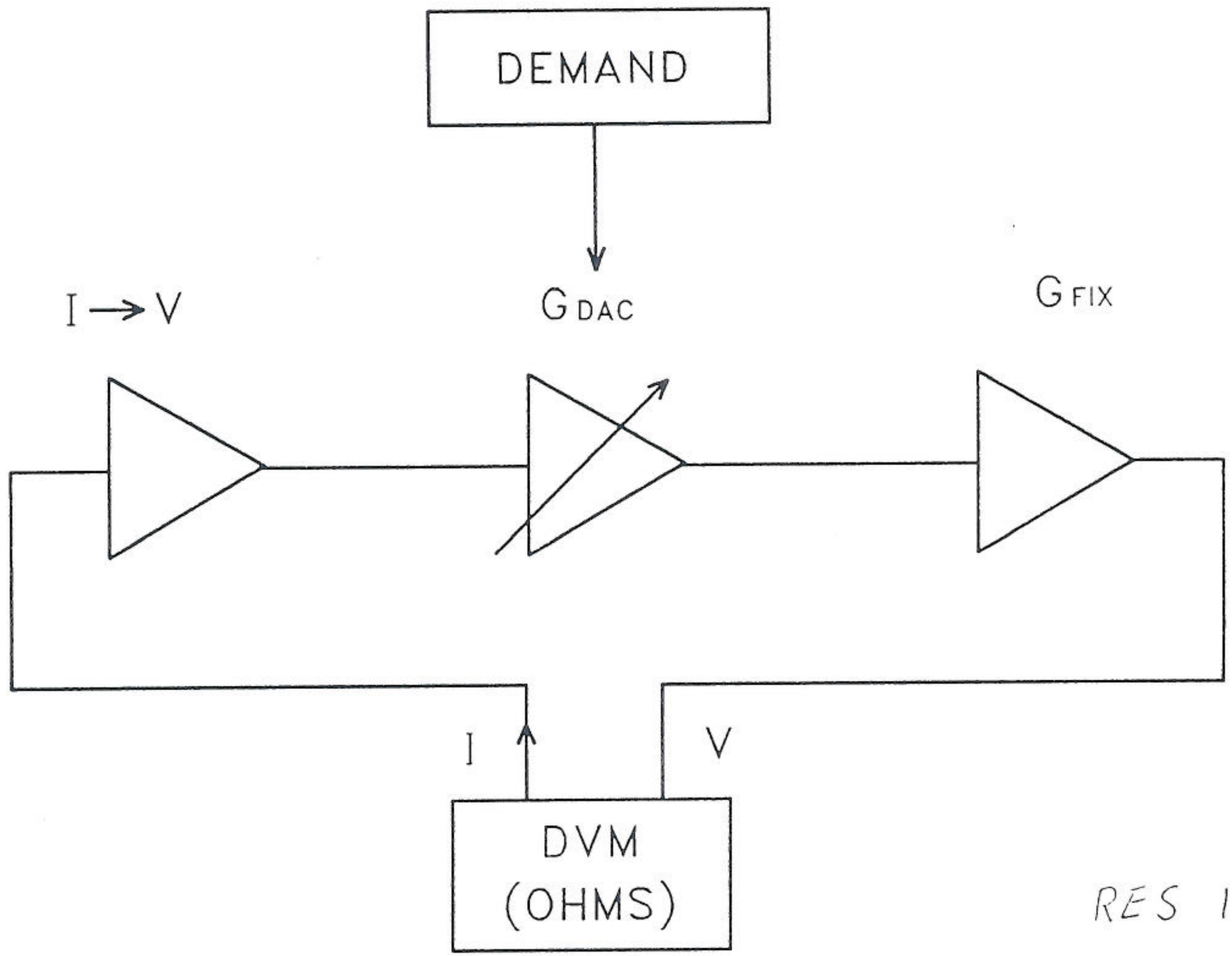
CAP FUNCTION

SELF CAL

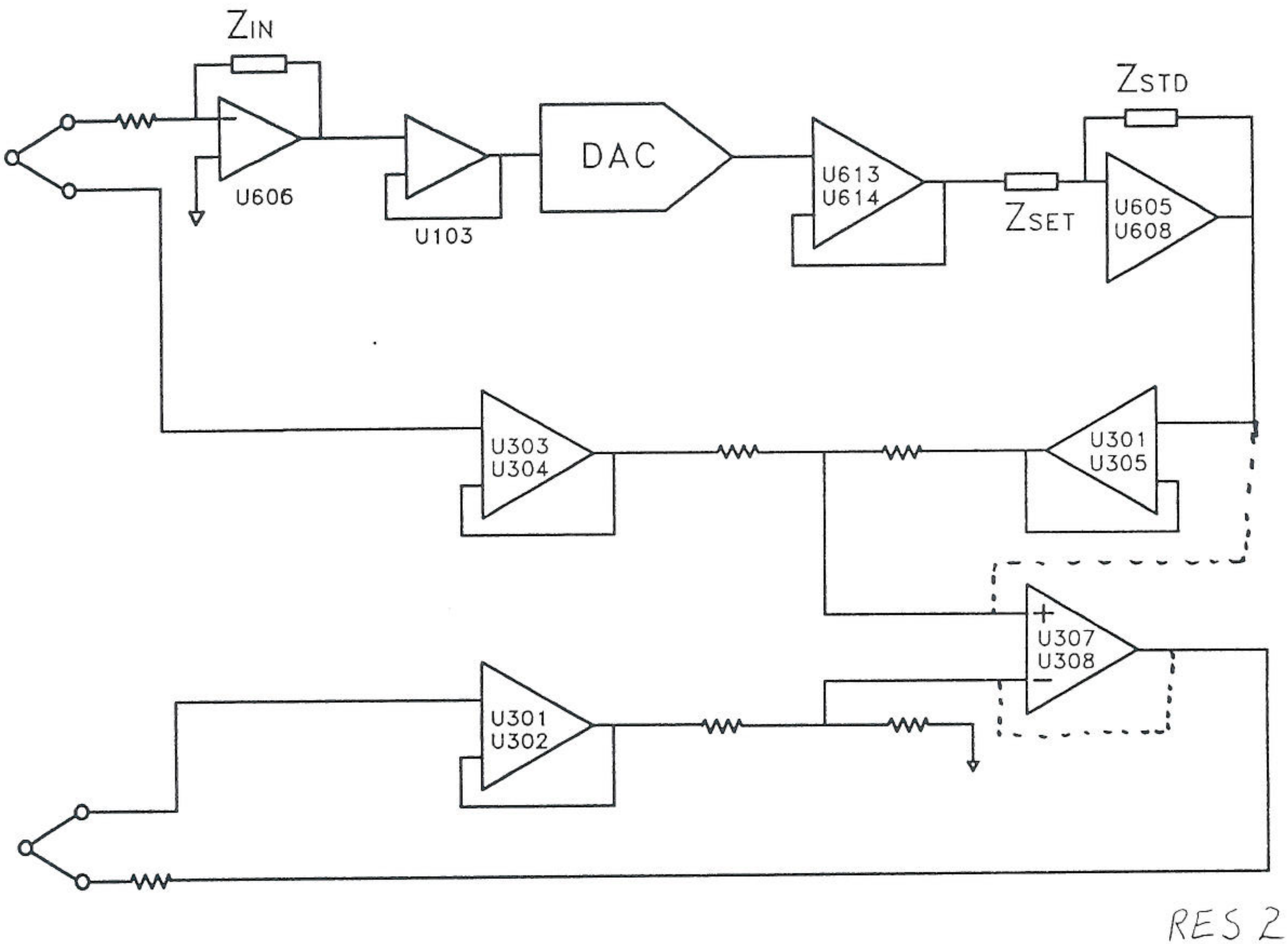
SELF TEST

FAULT FINDING

THIS MORNING'S AGENDA

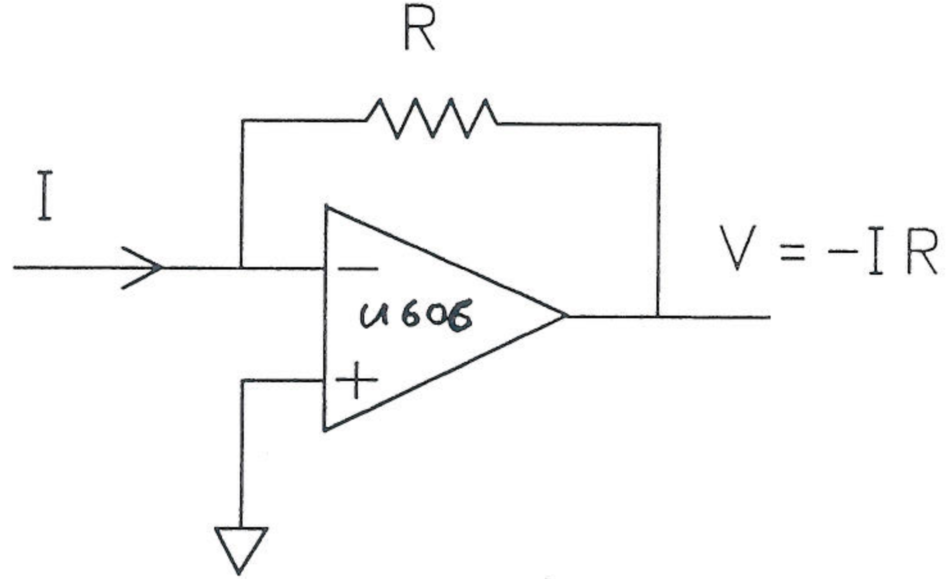


RES 1



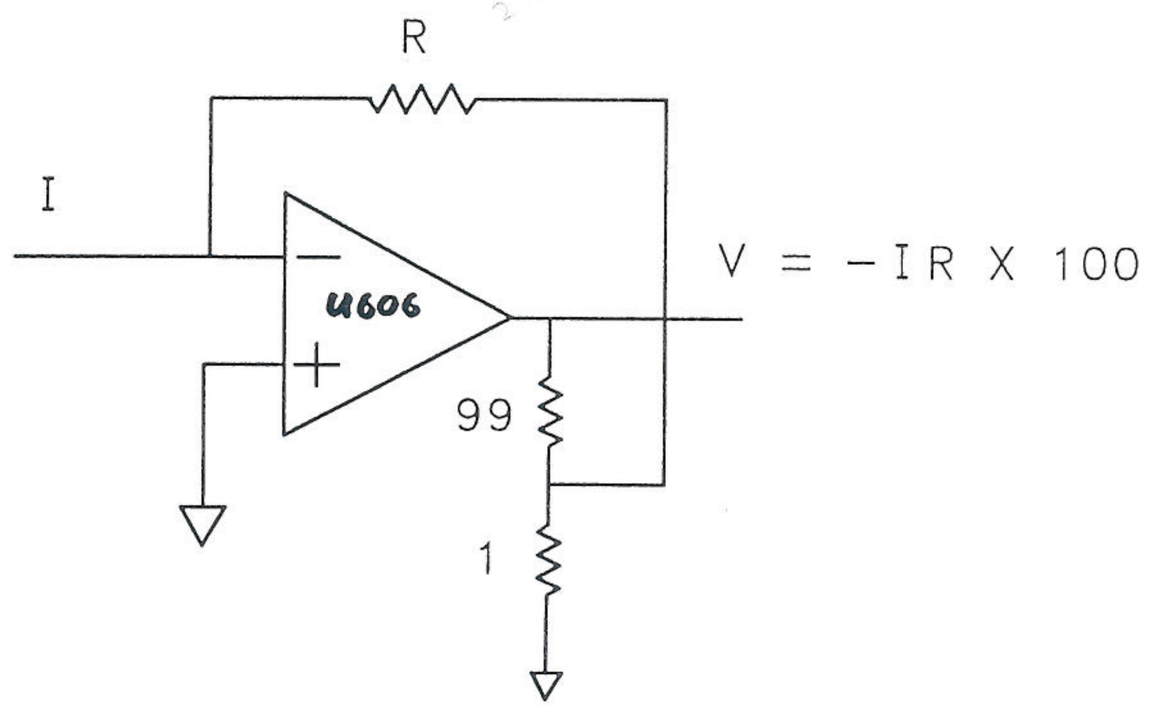
ACTIVE Z COMPLETE SYSTEM

C21



CURRENT → VOLTS CONVERTER

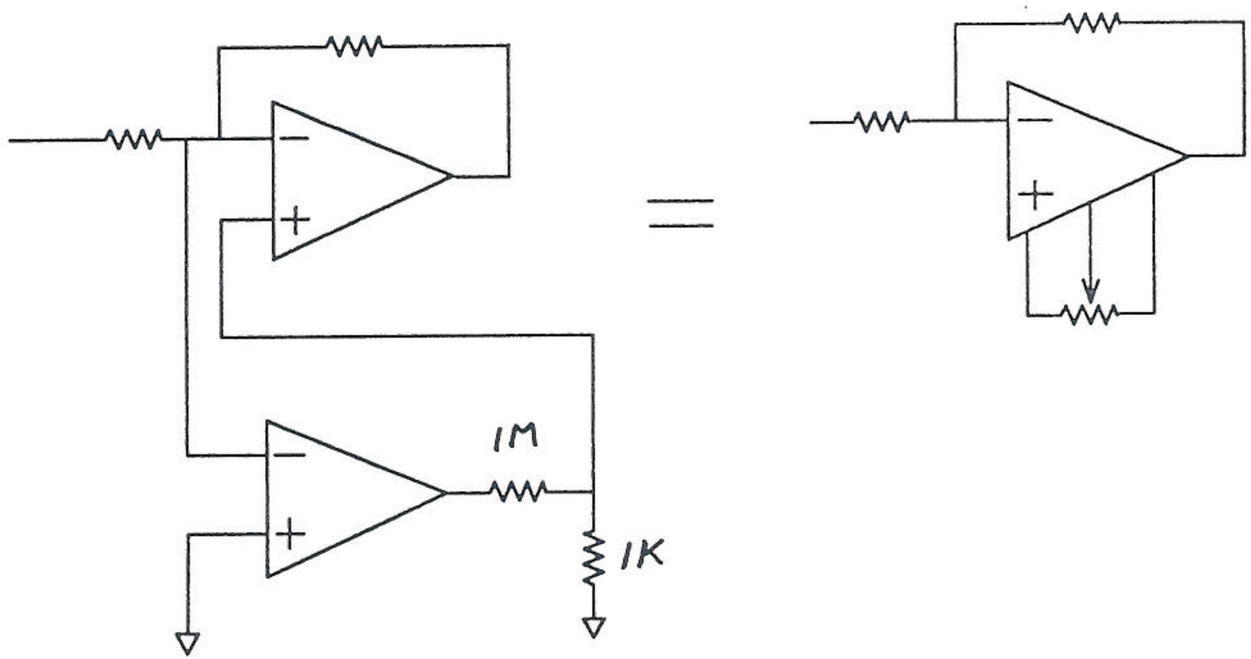
RES 3



LOW CURRENT ⟶ VOLTS CONVERTER

RES 4

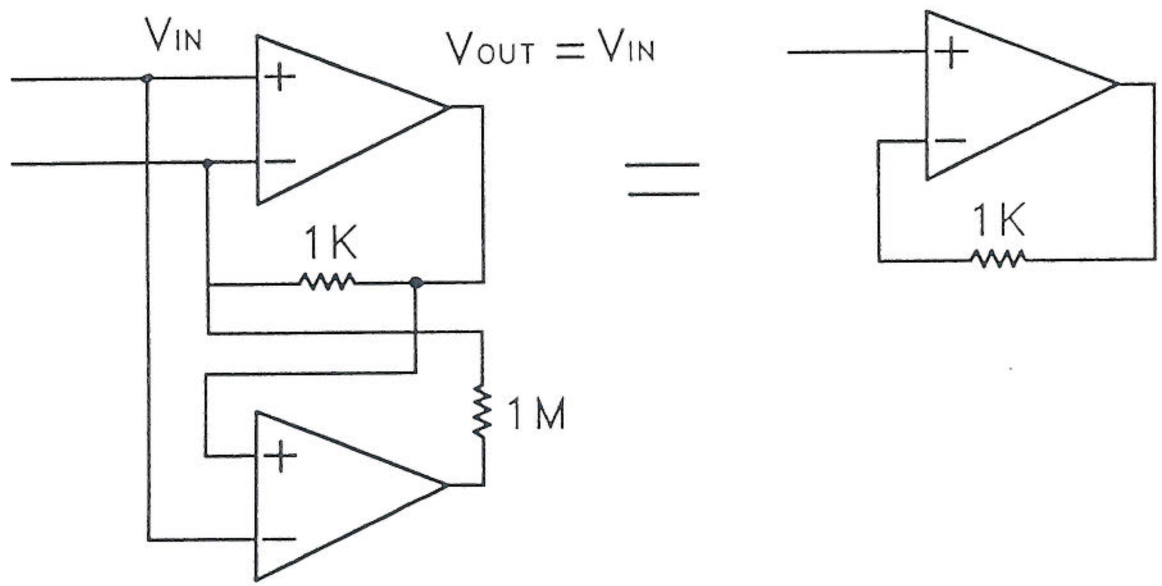
C10



INVERTING CHOPPER STABILISATION

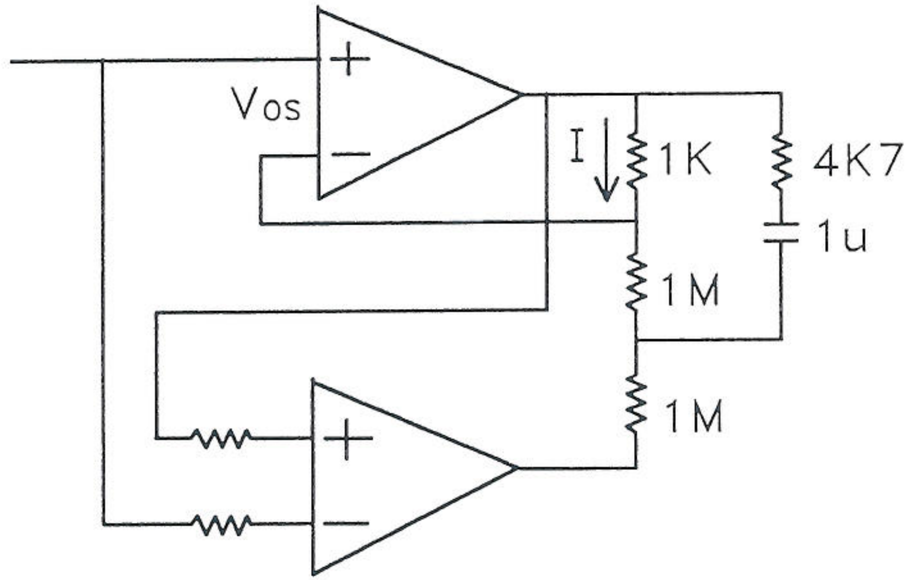
RES 5

C23



PRINCIPLE OF
FOLLOWING CHOPPER STABILISATION

RES 6 C24

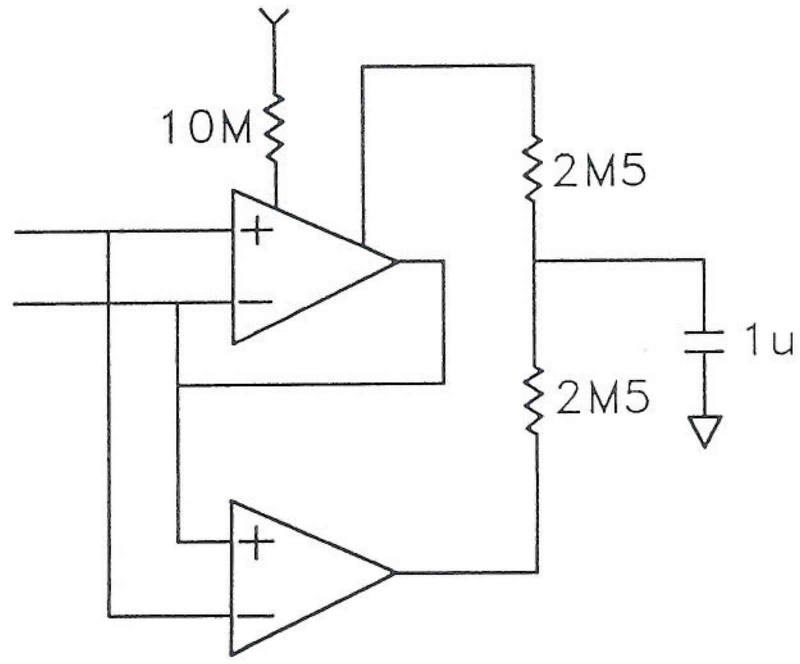


$$I = \frac{V_{os}}{1K}$$

PRACTICAL FOLLOWER + CHOPPER STABILISATION

RES 7

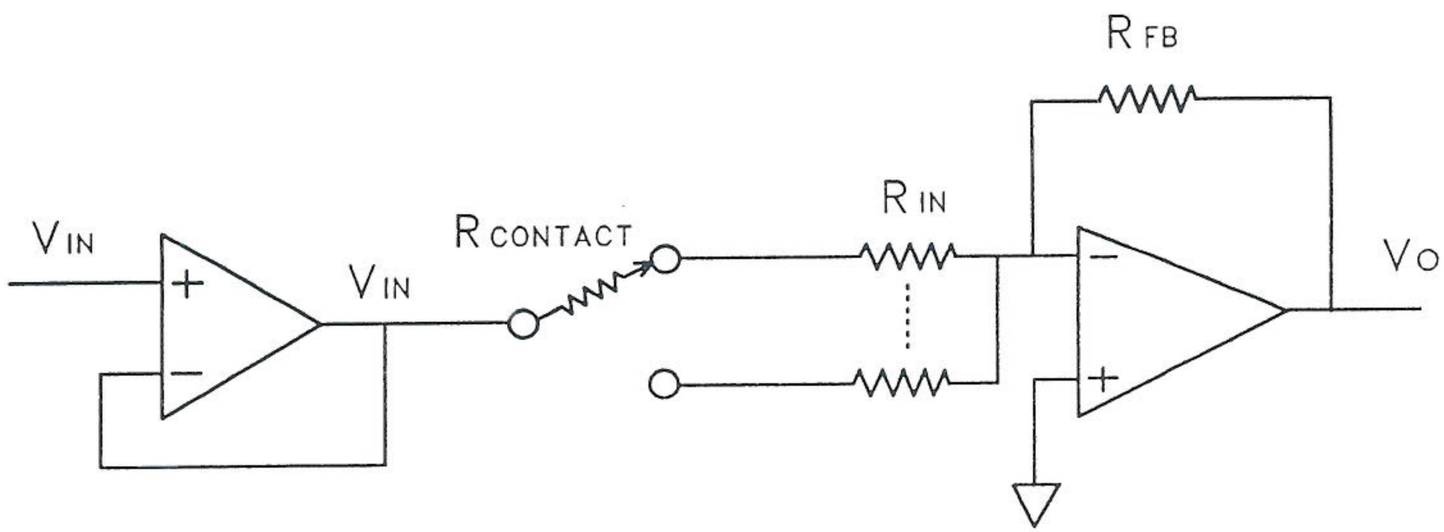
C25



ALTERNATIVE APPROACH TO FOLLOWER

RES 8

C26

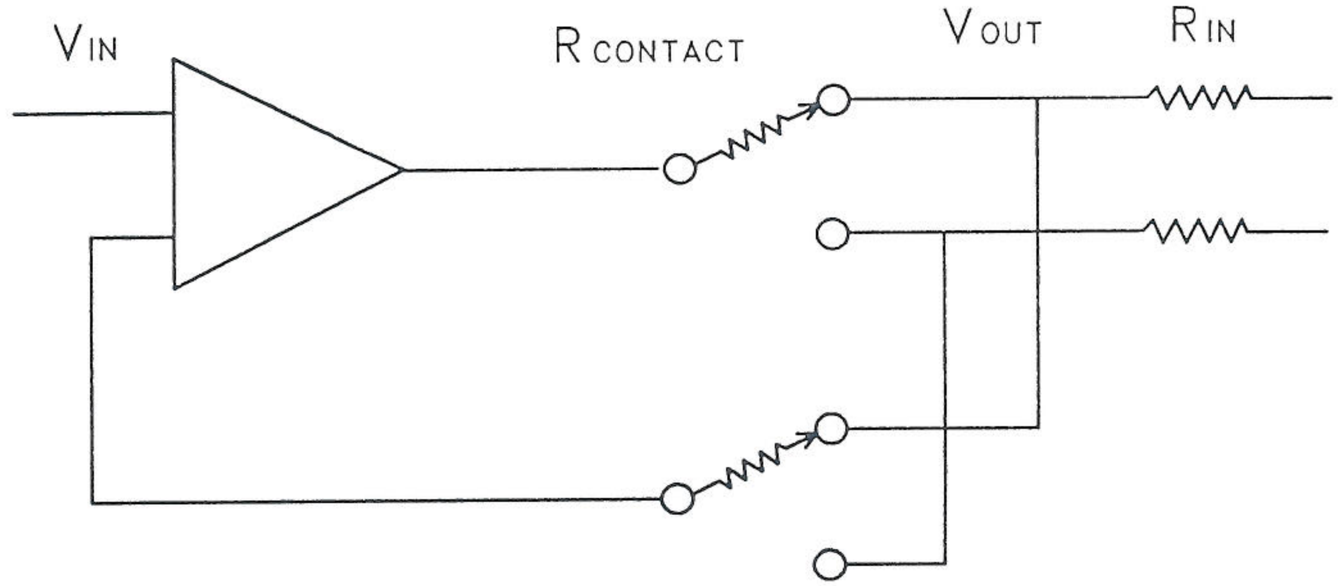


I WANT $V_O = \frac{R_{FB}}{R_{IN}} (V_{IN})$

I GET $V_O = \frac{R_{FB} (V_{IN})}{R_{IN} + R_{CONTACT}}$

SWITCH PROBLEMS

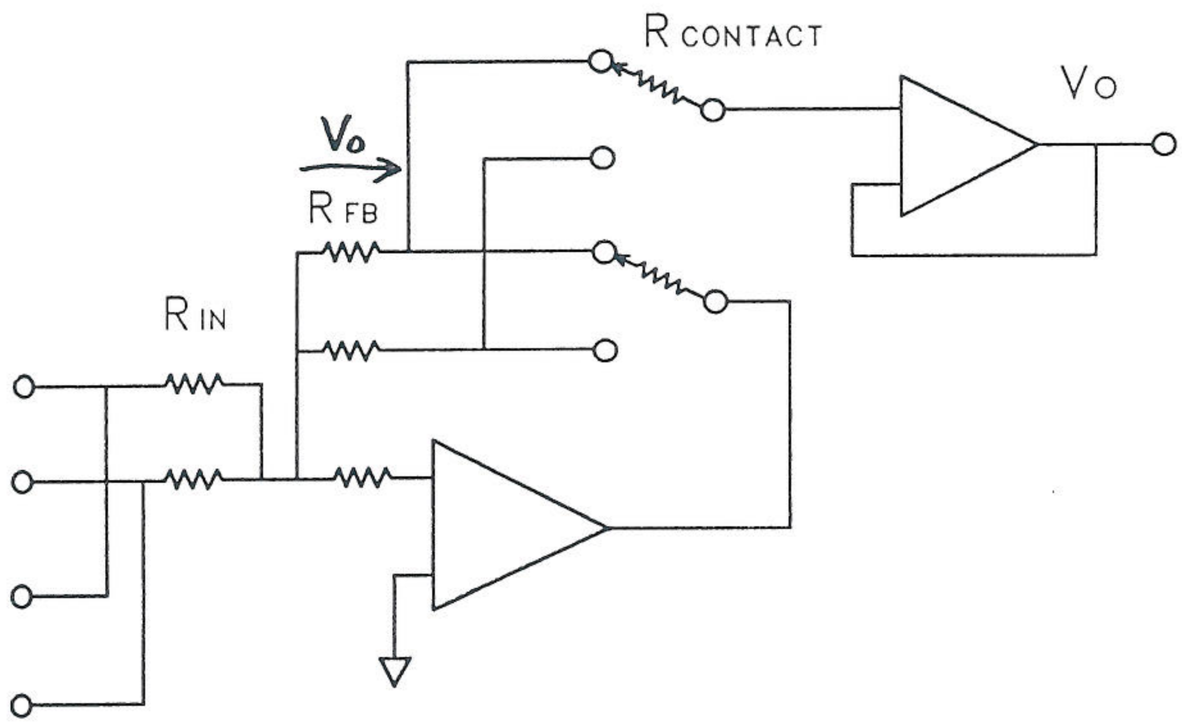
RES 9



NO SWITCH PROBLEM

RES 10

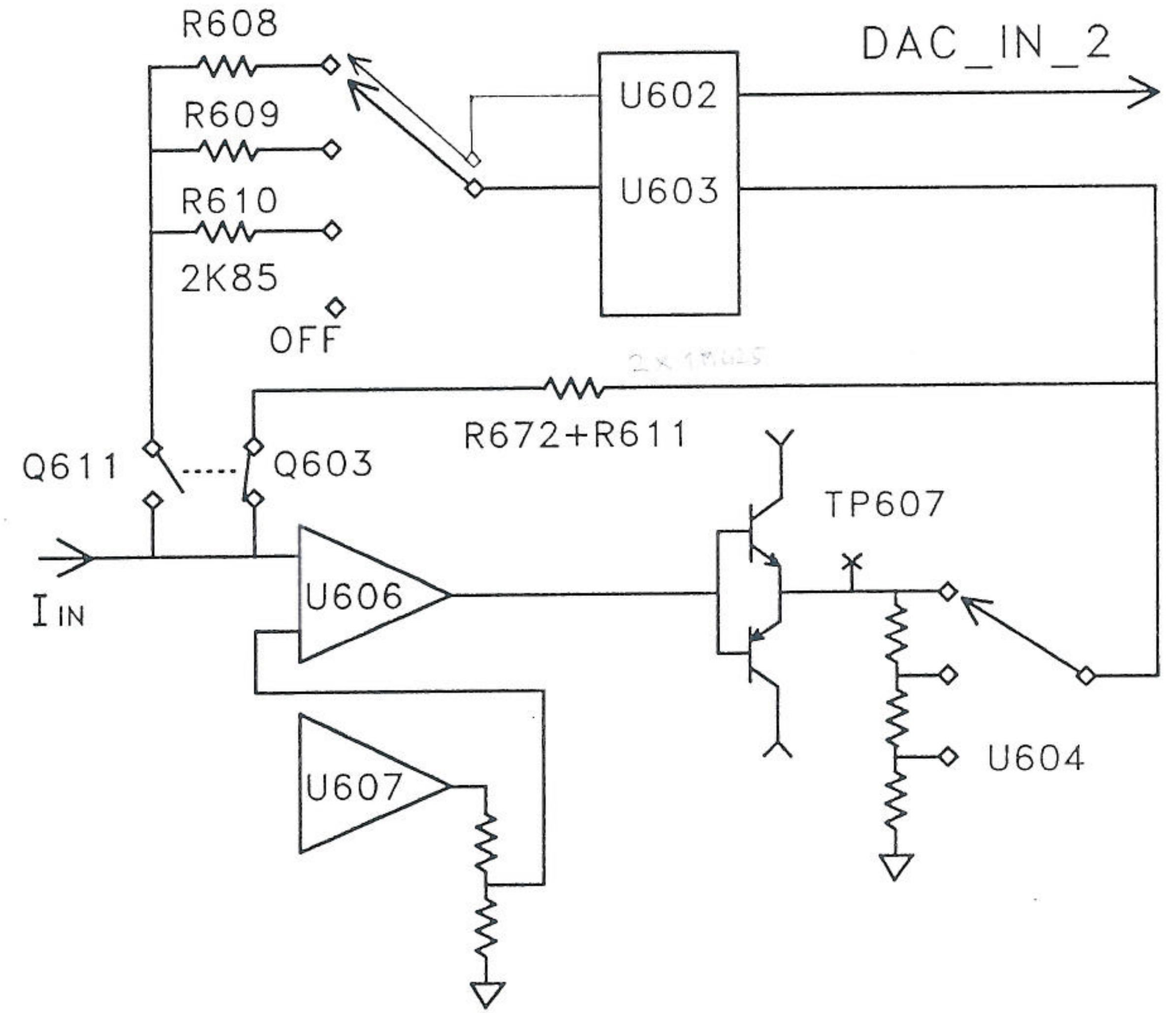
C7



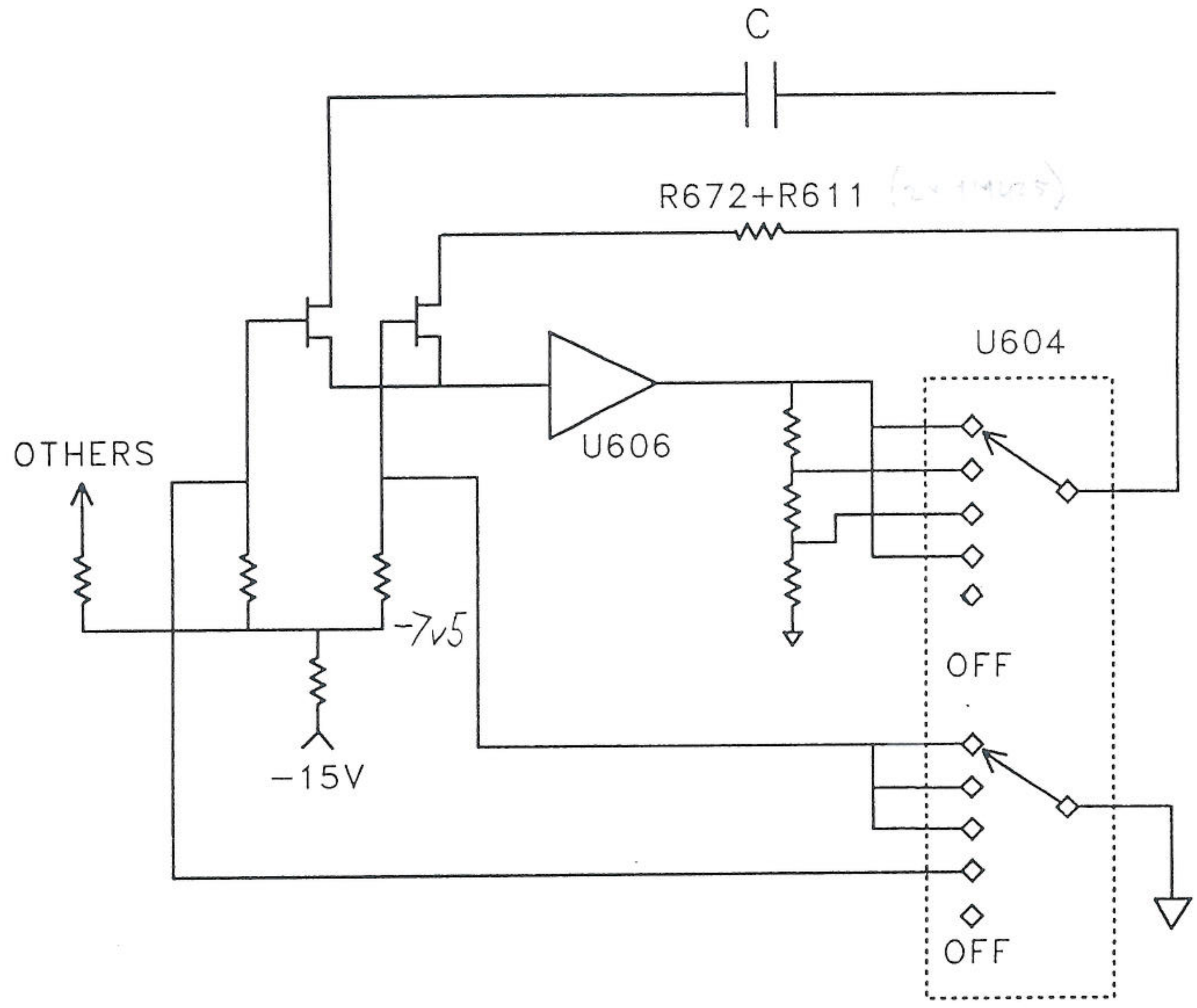
SWITCH IN FEEDBACK

RES 11

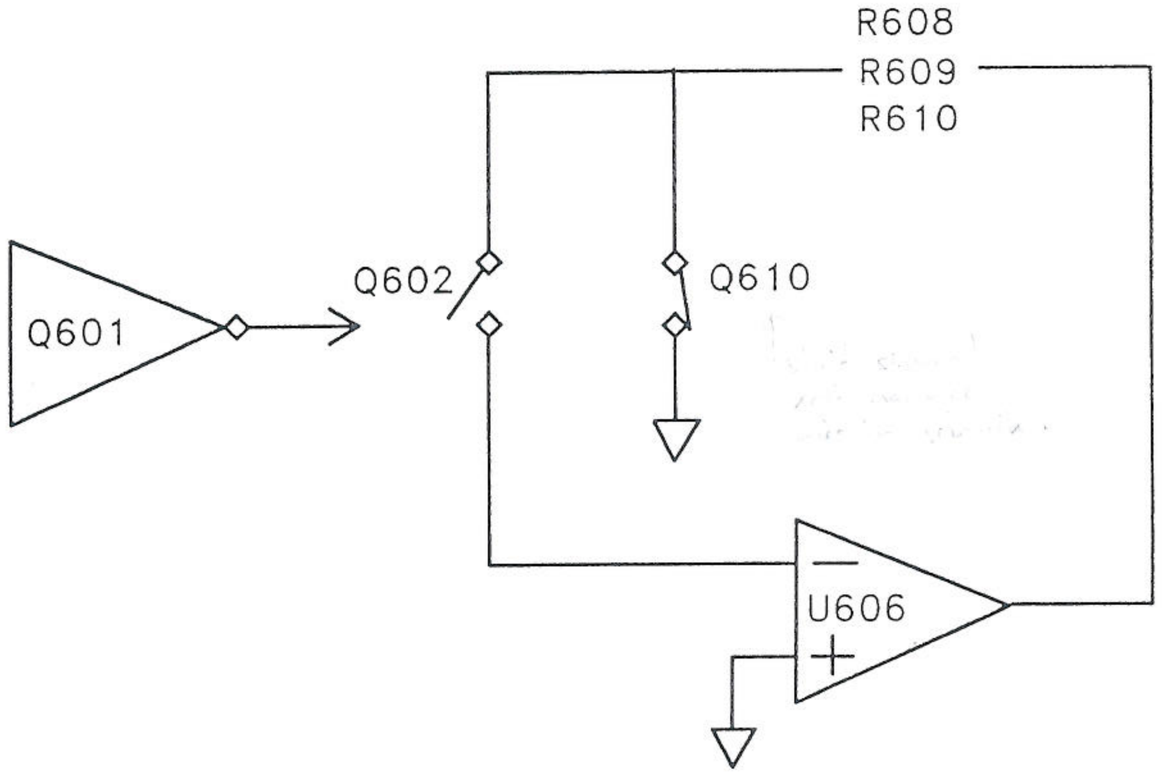
C8



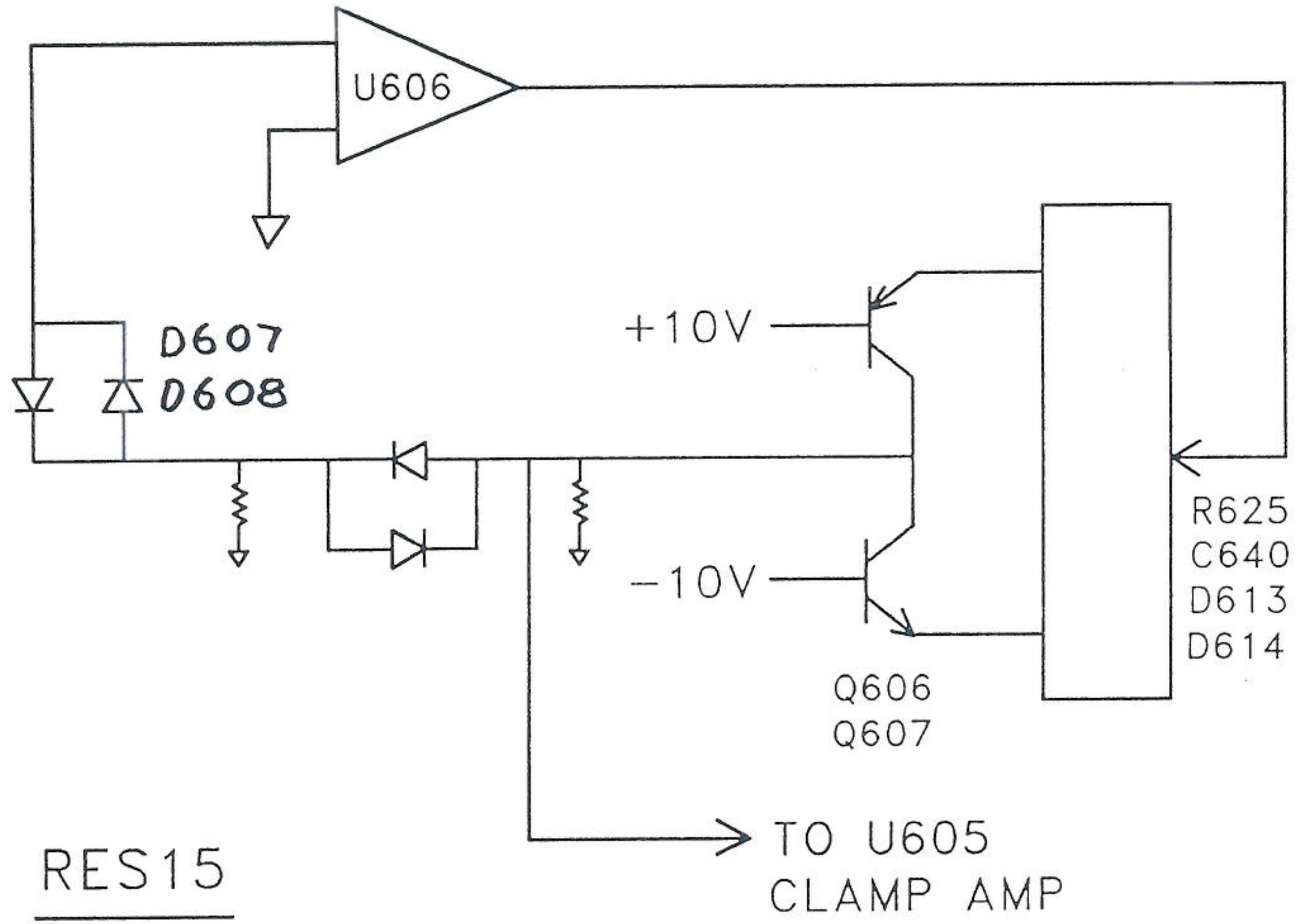
RES12 - PRACTICAL ARRANGEMENT



RES13 *FET SWITCHING*



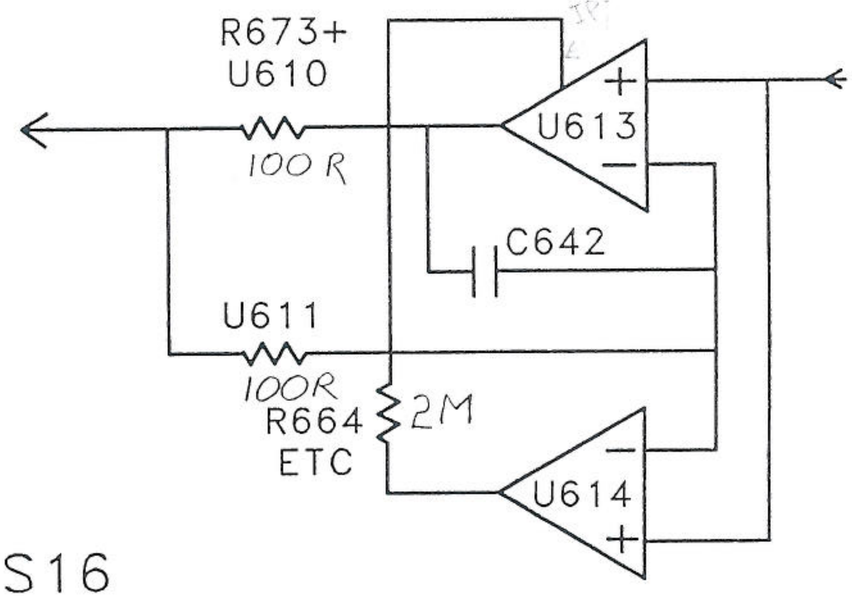
RES14 *LEAKAGE REDUCTION*



RES15

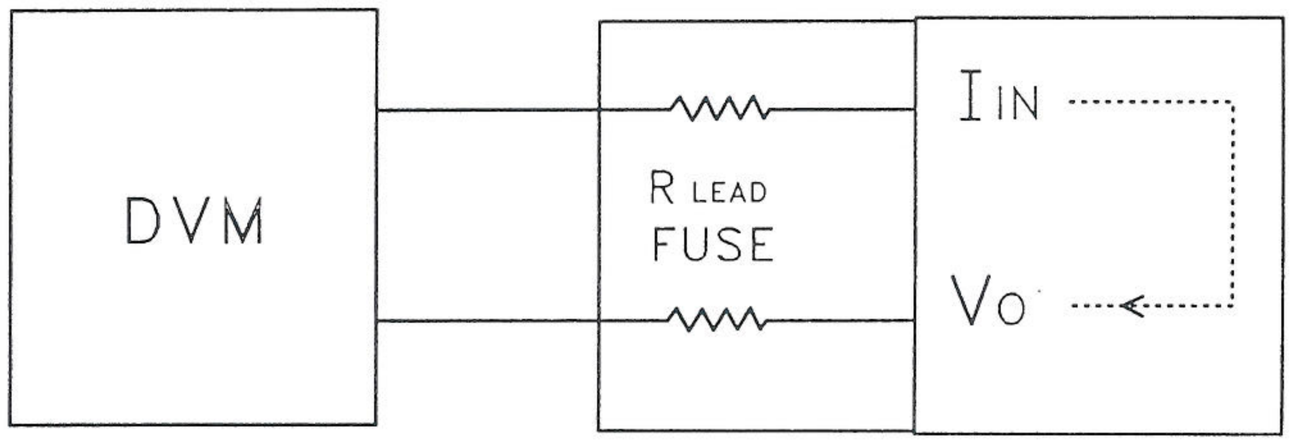
OPERATION OF VOLTAGE LIMIT

C35



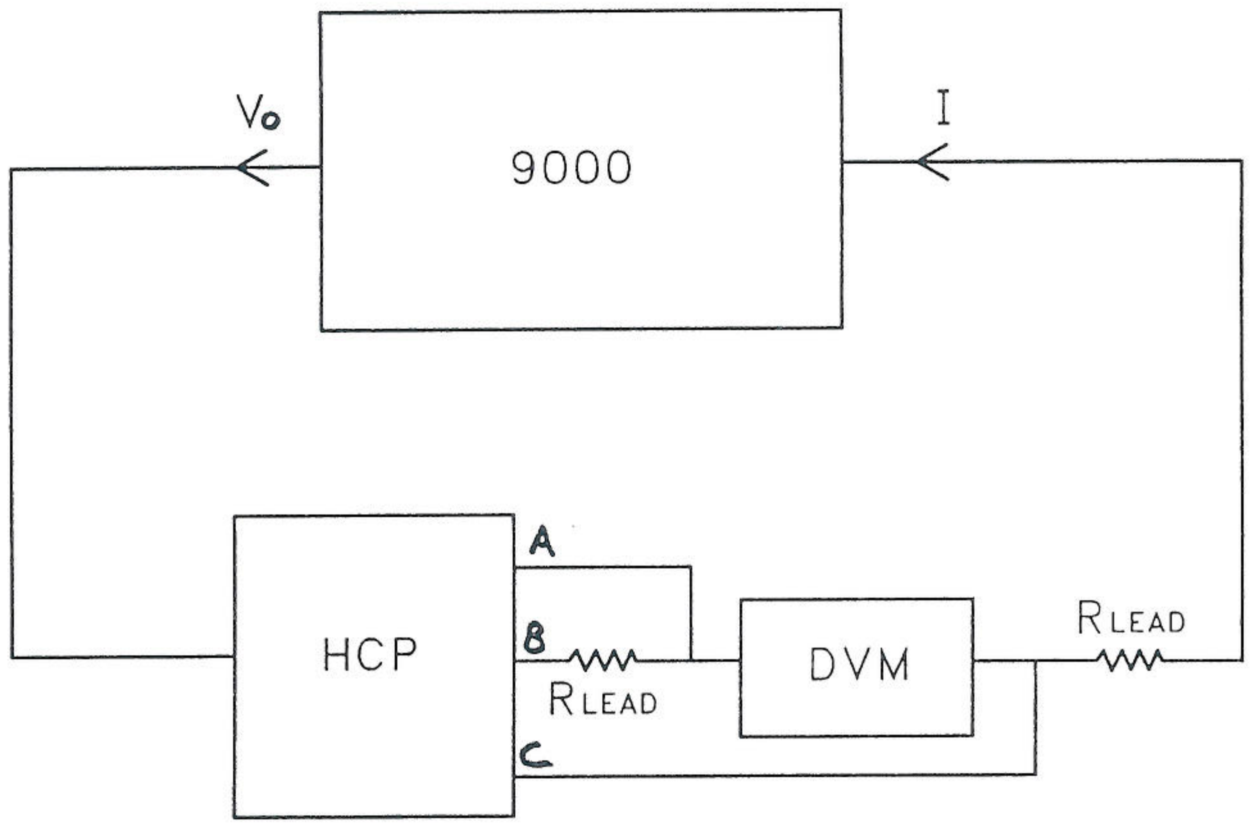
RES16

OFFSET REMOVAL OF U613



PROBLEM :– DVM MEASURES TOO MANY OHMS!

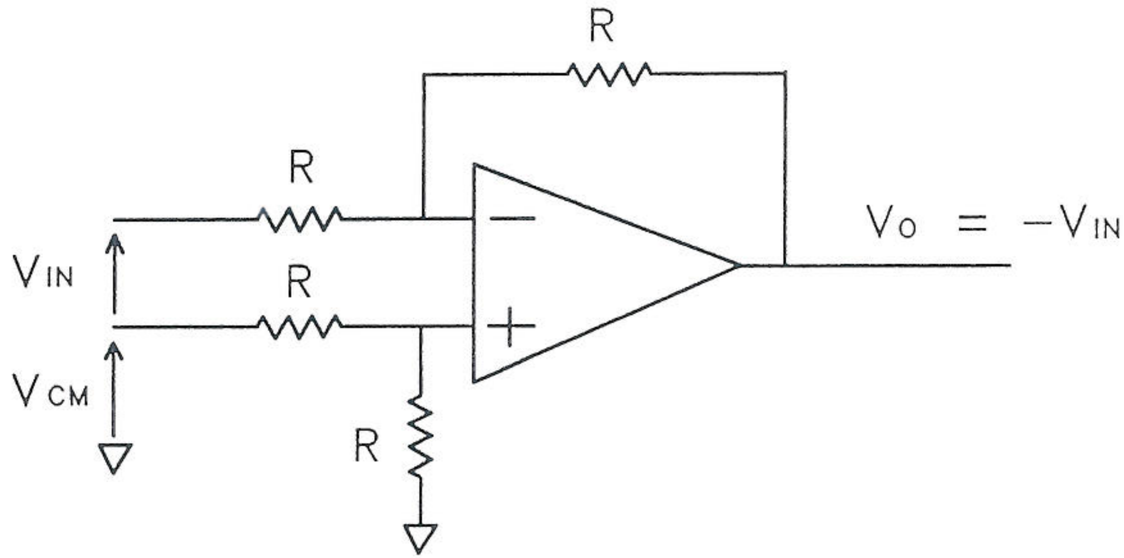
RES 17



CONCEPT OF LEAD IMPEDANCE COMPENSATION

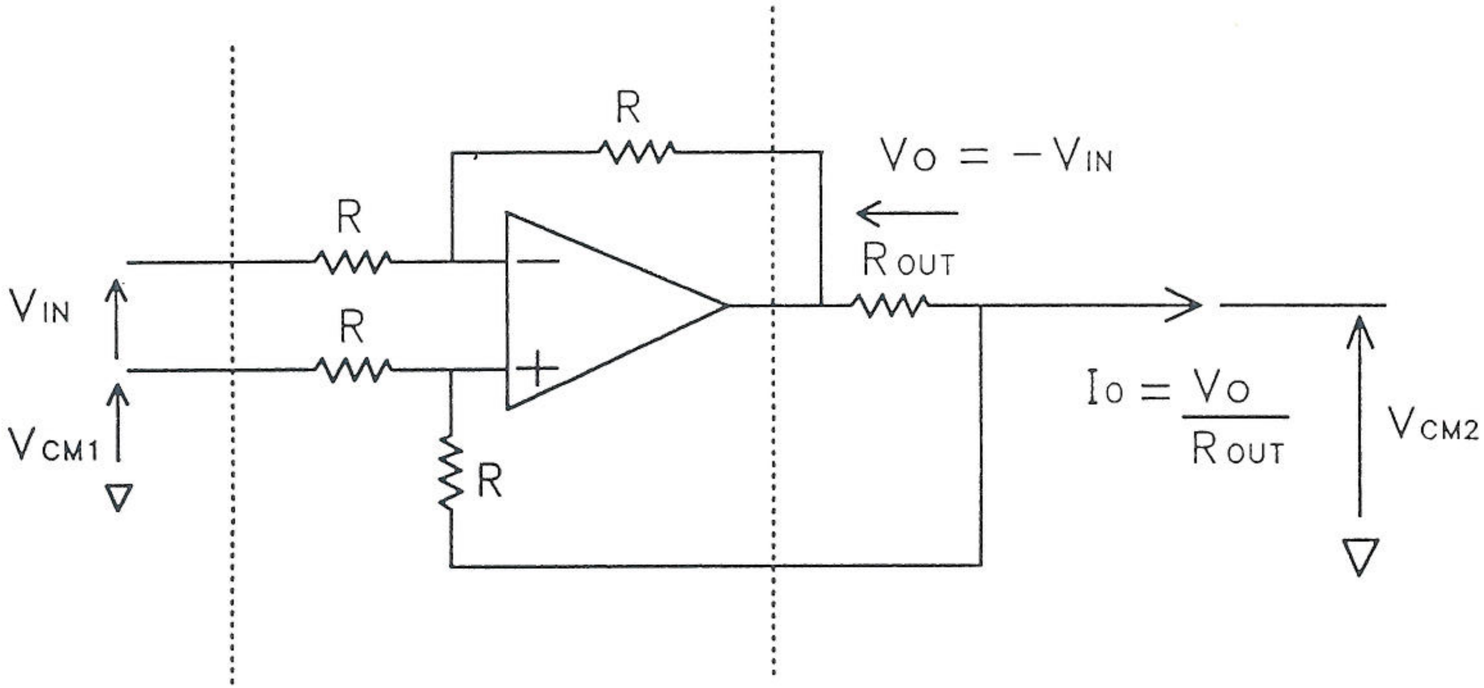
RES 18

C15



DIFFERENTIAL AMPLIFIER

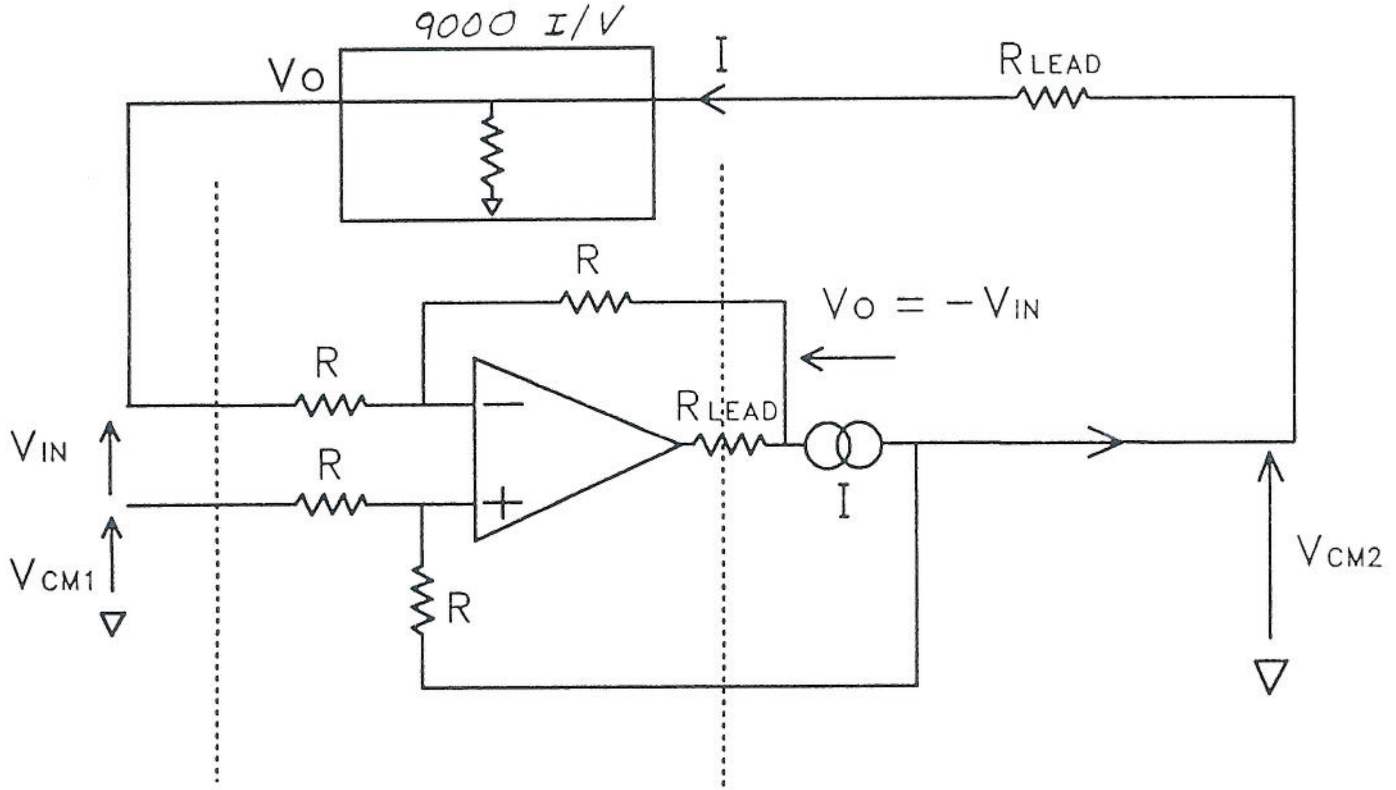
RES 19



HOWLAND CURRENT PUMP

RES 20

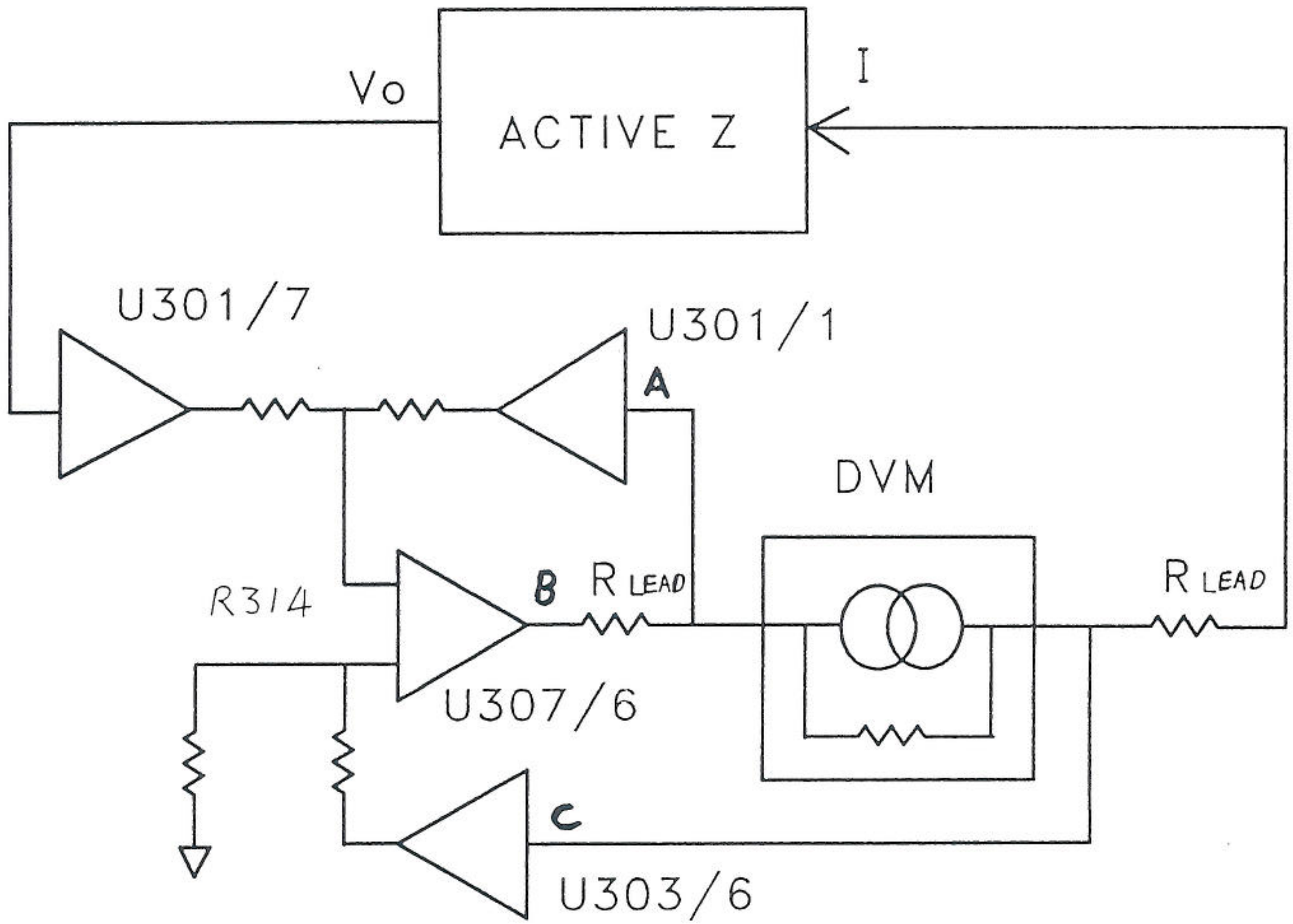
C14



HOWLAND CURRENT PUMP

RES 22

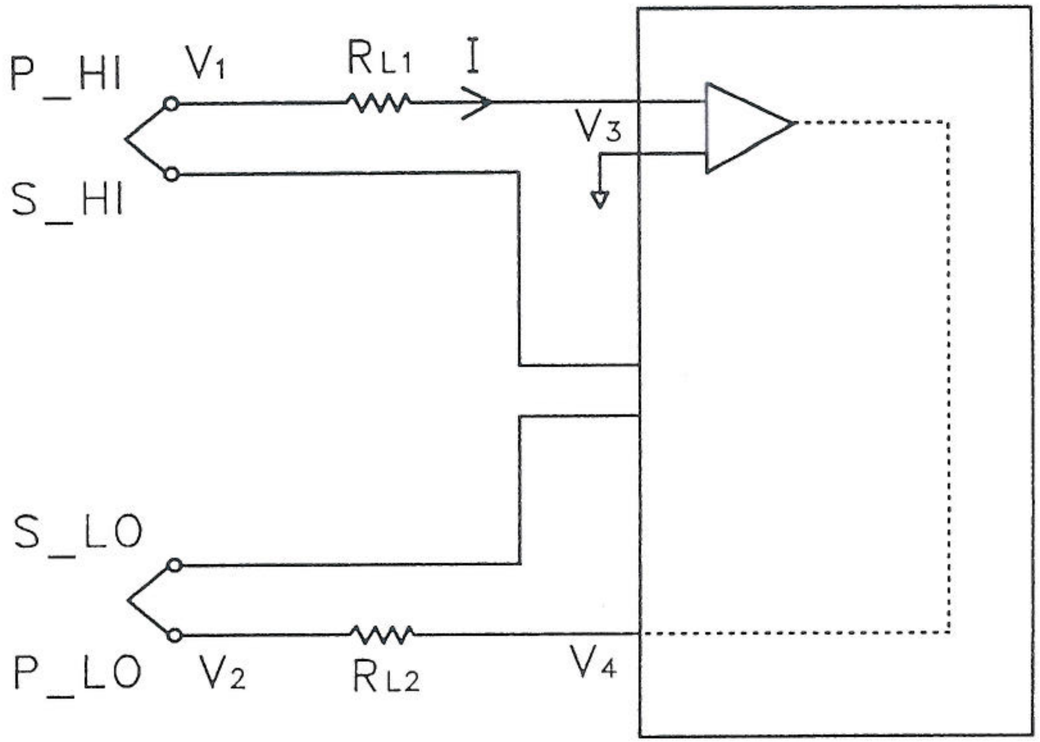
C22



THE FIX : A 4WIRE SENSE

RES 23

C12

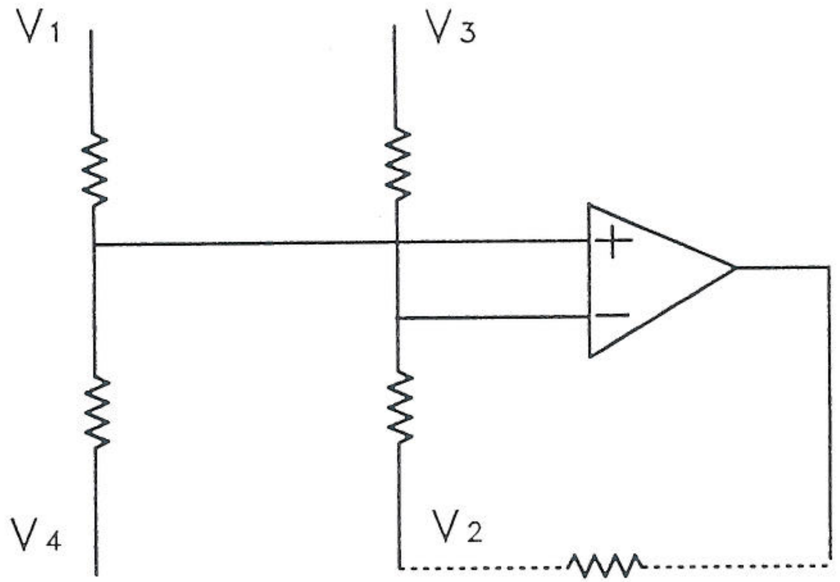


$$ERROR = I(R_{L1} + R_{L2})$$

THE LEAD PROBLEM

RES 24

C16

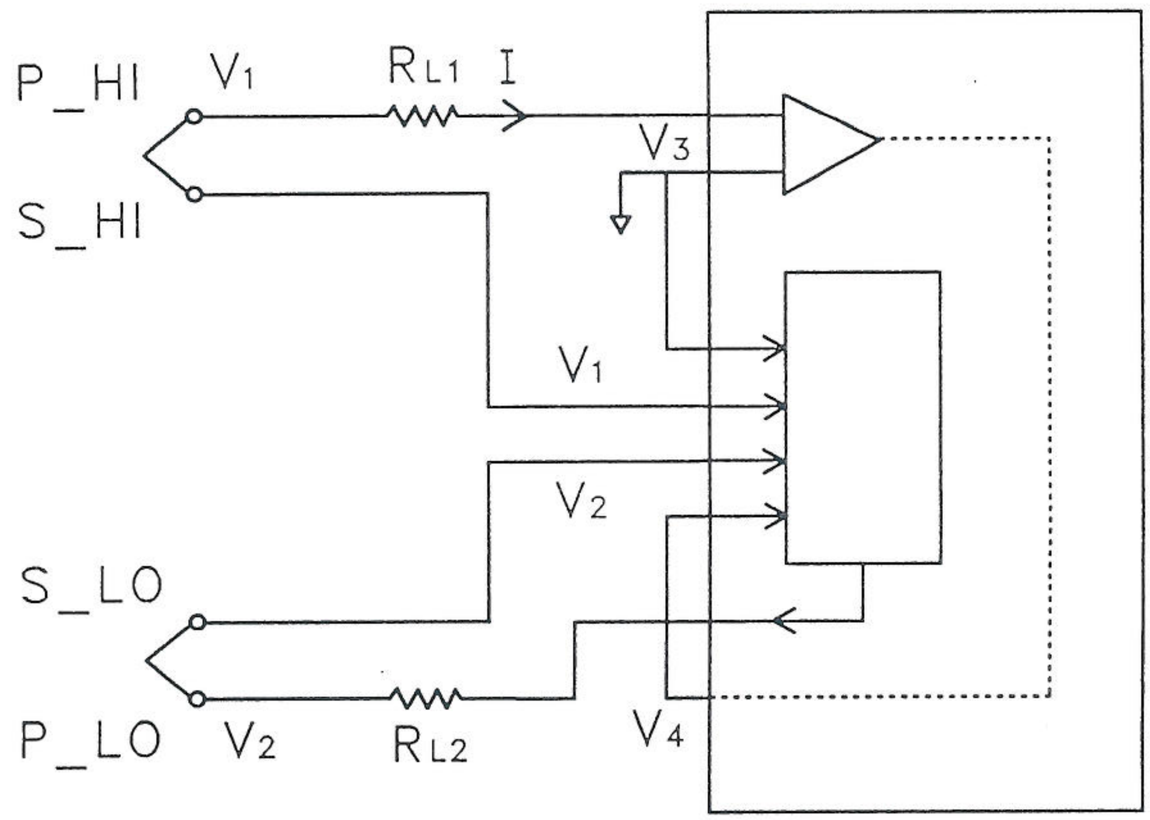


$V_1 + V_4 = V_2 + V_3$ [TP303 − TP301

SO $V_1 - V_2 = V_3 - V_4$ = TP304 − TP305]

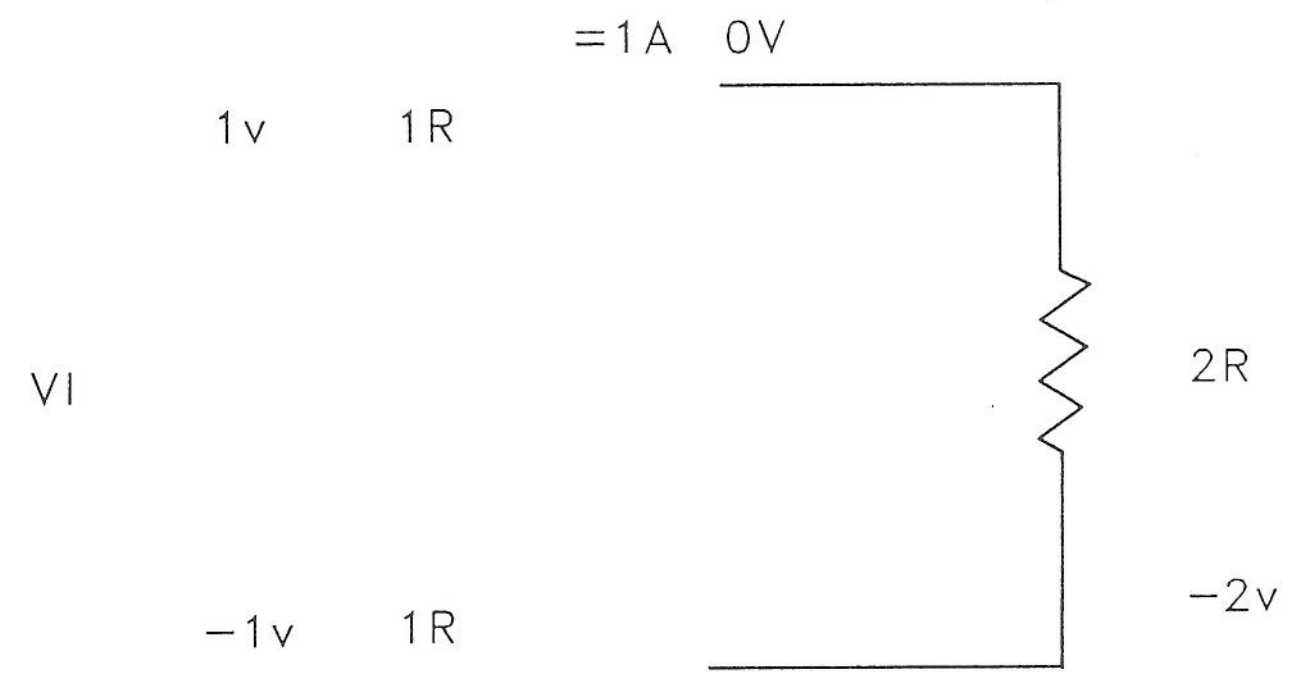
RES 25

LEAD Z SOLUTION



RES 26

C18



$$V_1 - V_2 = V_3 - V_4$$

$$1v - V_2 = 0 - -2v$$

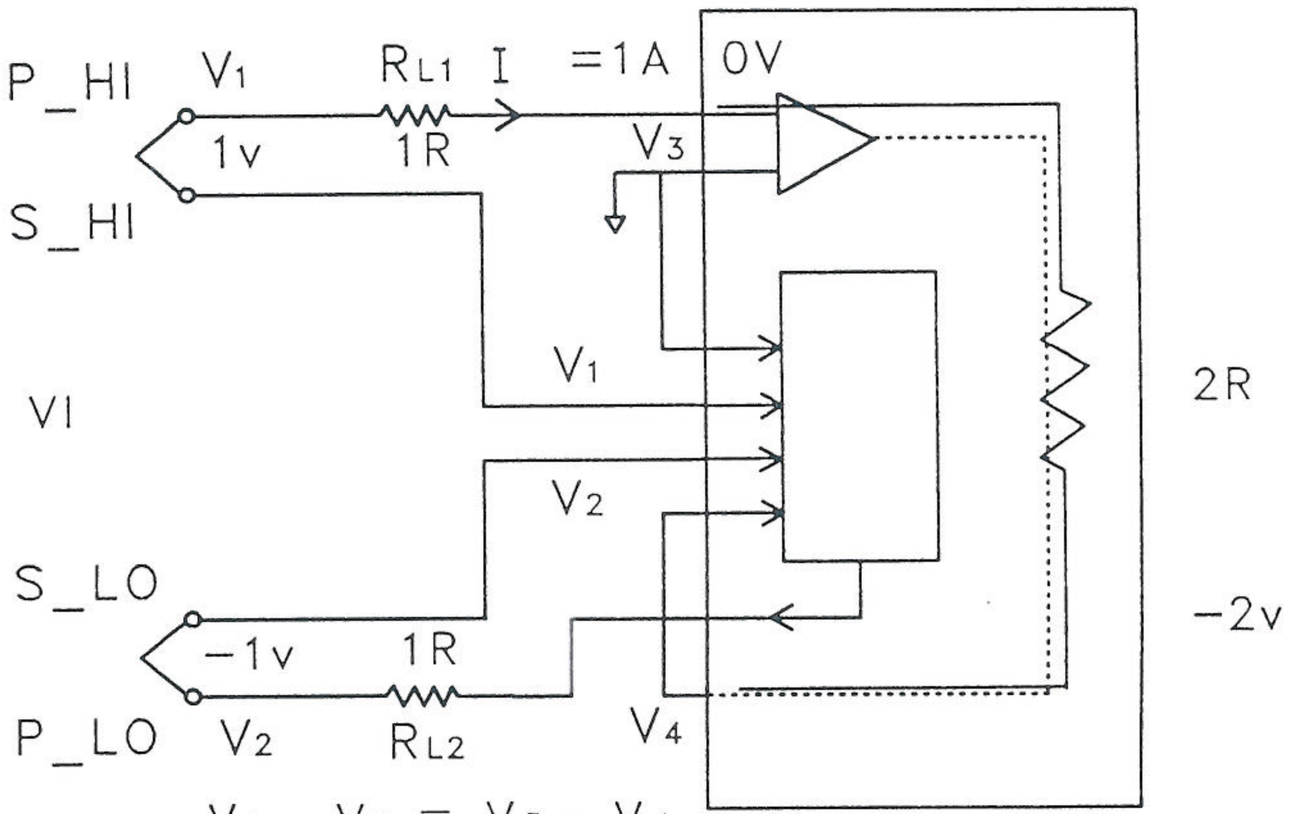
$$1v - 2v = V_2 = -1v$$

$$\text{SO } V_1 - V_2 = 2v$$

RES 27

C19

LEAD Z SOLUTION



$V_1 - V_2 = V_3 - V_4$

$1v - V_2 = 0 - -2v$

$1v - 2v = V_2 = -1v$

SO $V_1 - V_2 = 2v$

RES 26+
RES 27

V_1 = RGC_S_POS

= TP303

V_2 = RGC_S_NEG

= TP301

V_3 = 0V (VIRTUAL EARTH)

= TP304

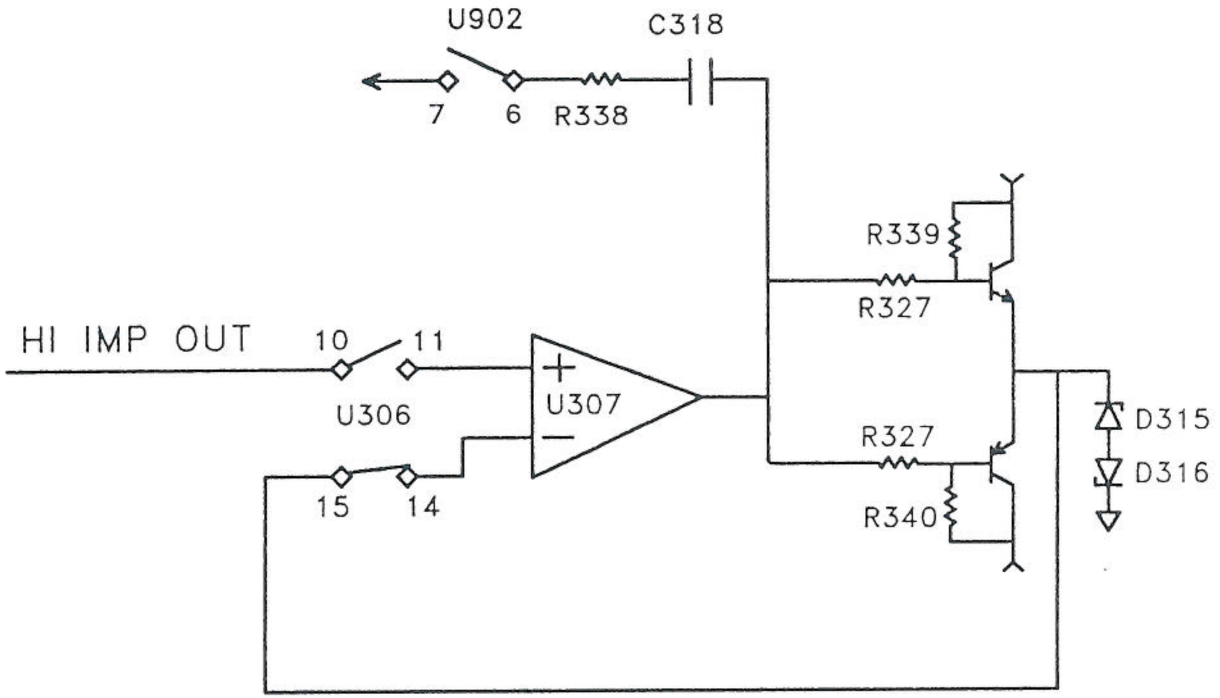
V_4 = HI_IMP_OUT

= TP305

[TP303 − TP301 = TP304 − TP305]

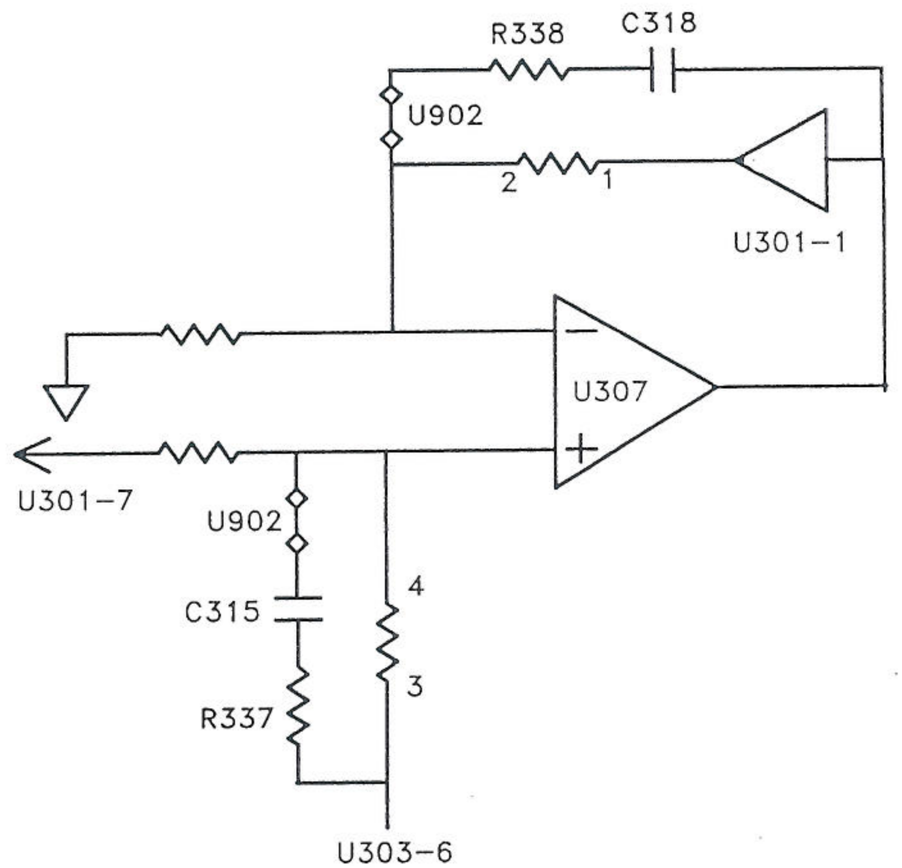
RES 28

C20



SIMPLIFIED BUFFER

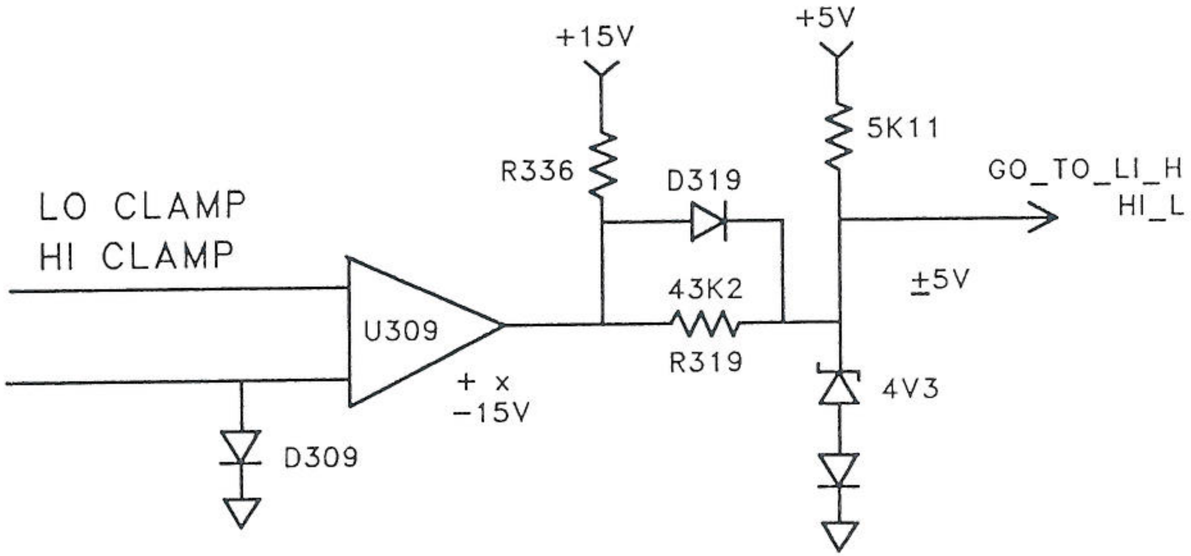
RES29



DIFF AMP FILTERING VIA U902

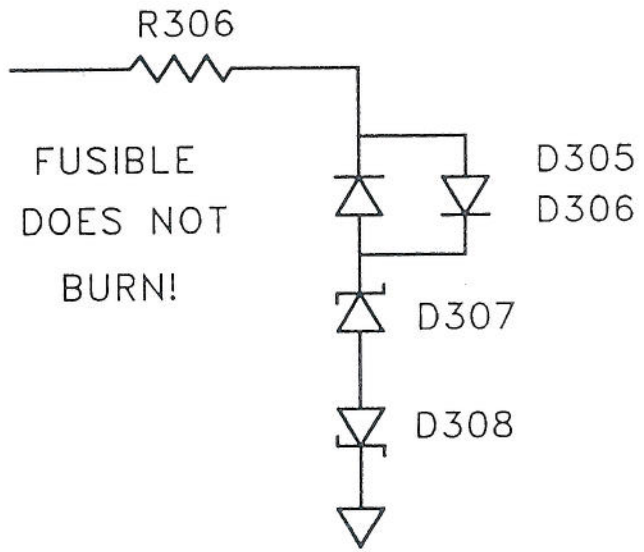
RES30

C51

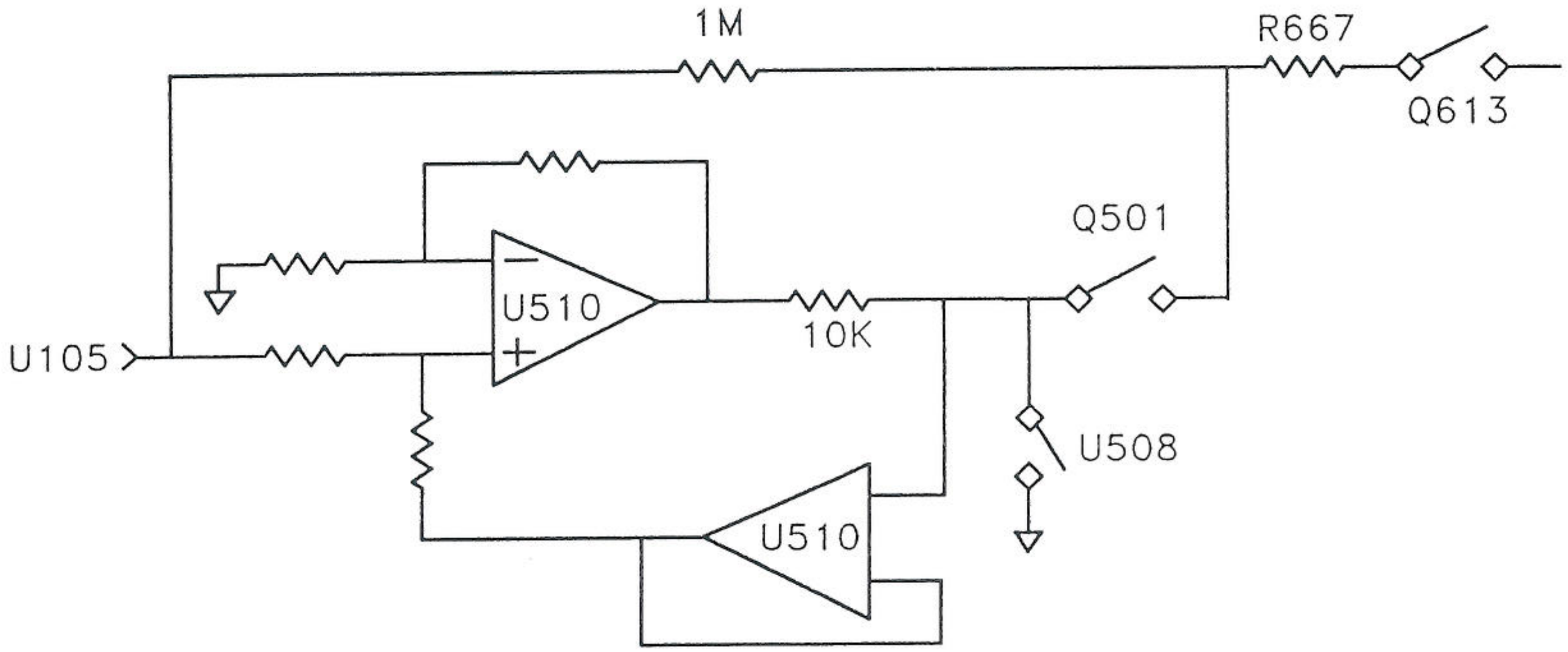


SIMPLIFIED CLAMP

RES31



SENSOR PROTECTION   RES32



CURRENT TICKLE

RES32

C54

! EQUATIONS !

$$\text{IMPEDANCE} \propto \frac{1}{C}$$

$$It = Q = CV$$

IF C GETS BIGGER
IMPEDANCE REDUCES

CAP1