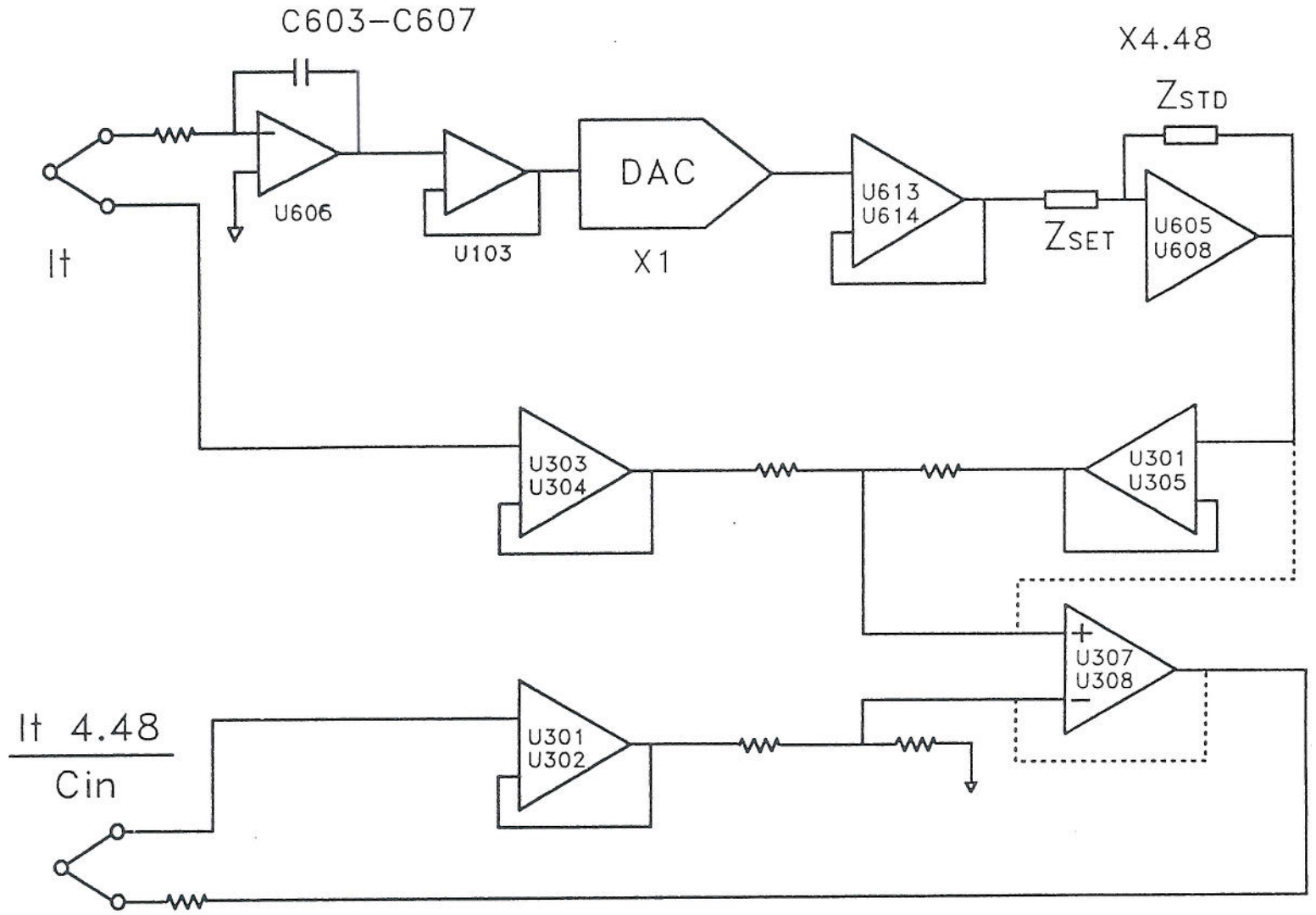


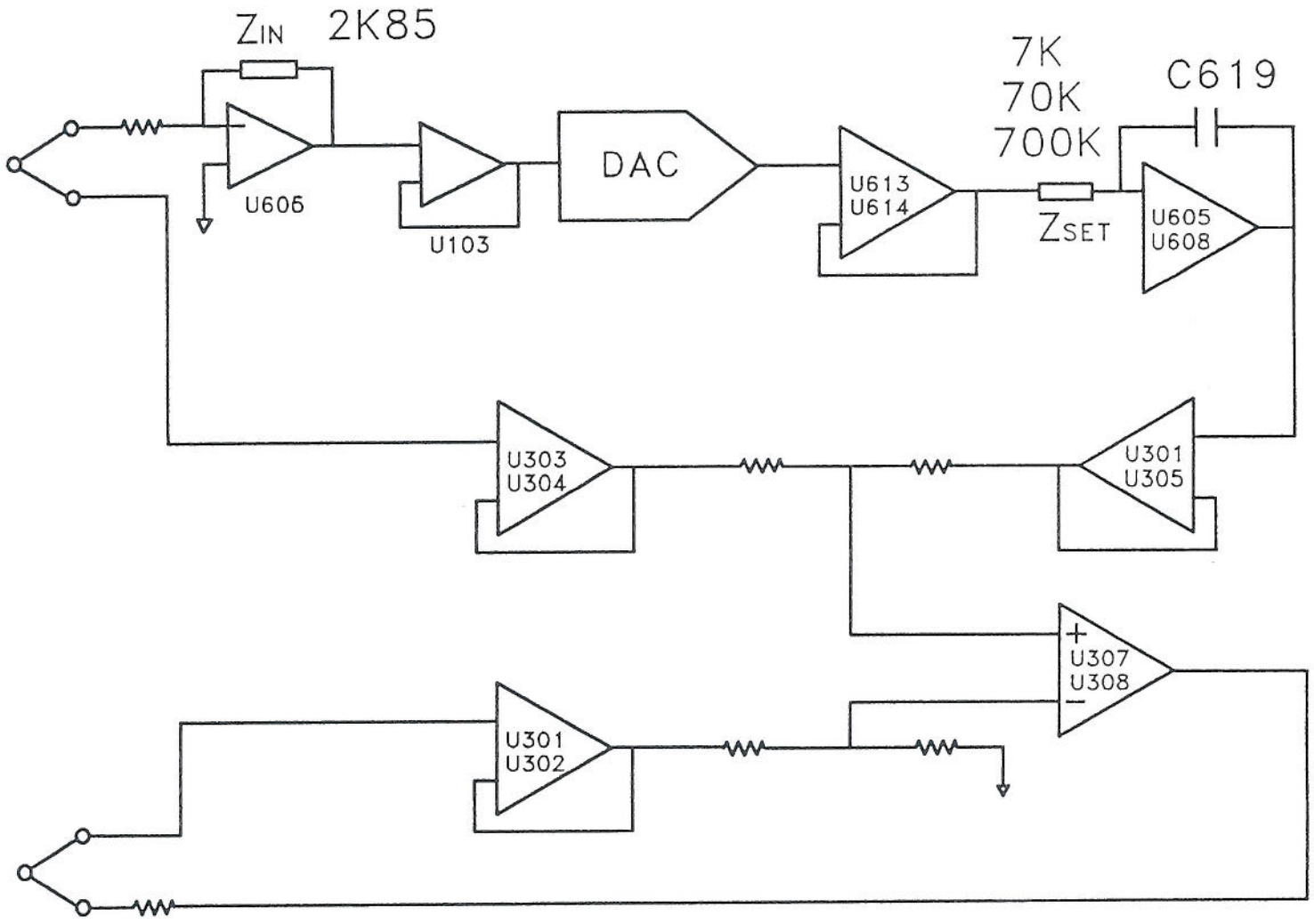
$$C = \frac{Cin}{4.48}$$

ACTIVE C COMPLETE SYSTEM

CAP2

–TO 40μF

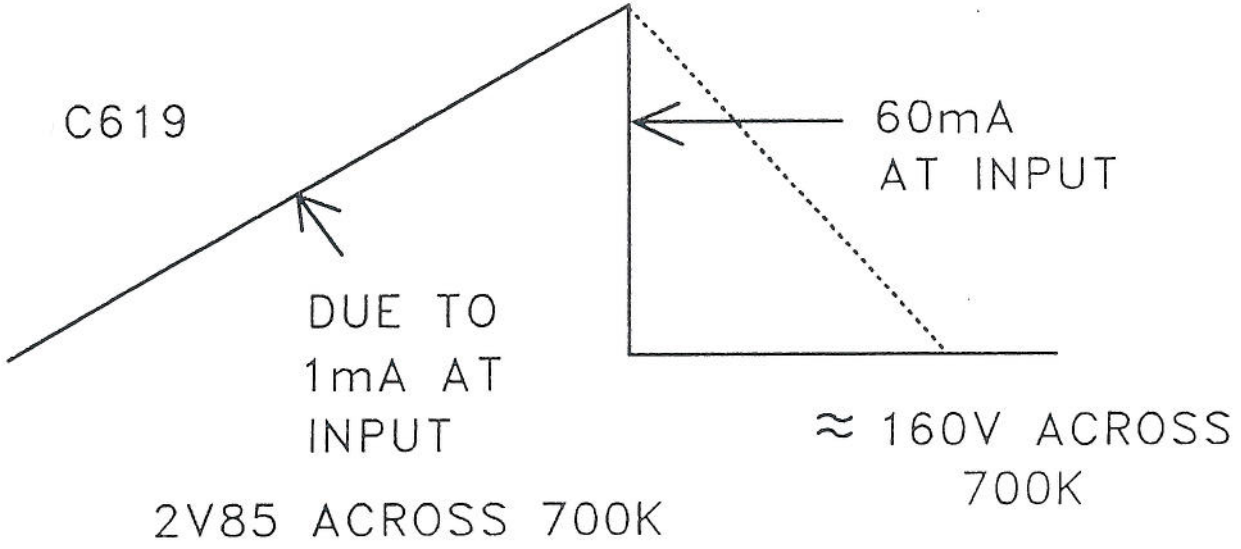
C56



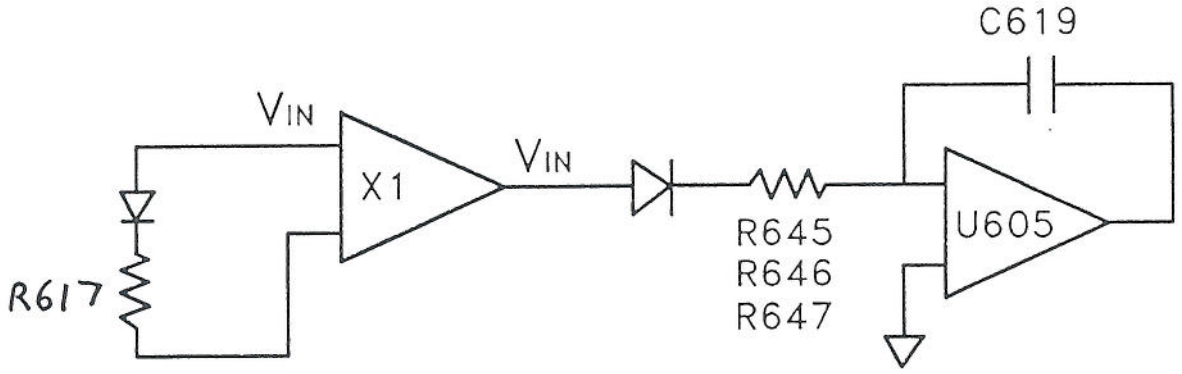
$$C = \frac{C619}{0.407} \times 10^{0,1,2}$$

ACTIVE C COMPLETE SYSTEM

40µF – 40mF CAP3

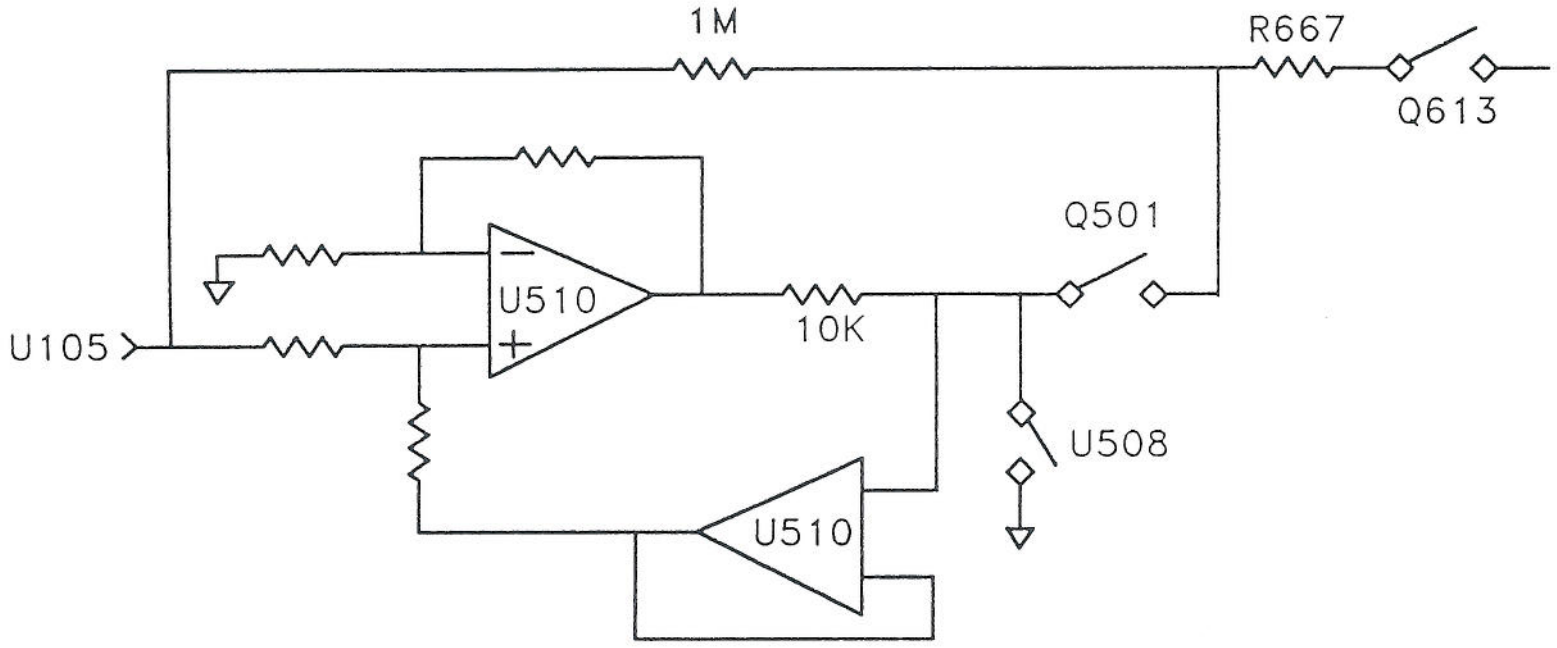


FAST DISCHARGE PROBLEM CAP4



CAP 5

POSITIVE CLAMP IN CAP >40μF



CURRENT TICKLE

SCφ

C54

STAGE 1 – CALIBRATE R (4950)

STAGE 2 – IR = V (INTERNAL)

STAGE 3 – It = CV

$$\frac{\cancel{I}R}{\cancel{I}t} = \frac{\cancel{V}}{C\cancel{V}} \quad \text{SO} \quad C = \frac{t}{R}$$

C is calibrated – no offsets
I & V do not matter!

Notes – 1. STAGE 2&3 can be repeated at any time (5)
2. SELECTING CAP CAUSES STAGE 2&3 – hence delay, O/P turns on & off, etc.
3. IF R is wrong then C is also wrong.

SELF CAL OF CAP

SC1

REMOVE / THERMISTOR CONNECTOR
REPLACE

HEAT THERMISTOR

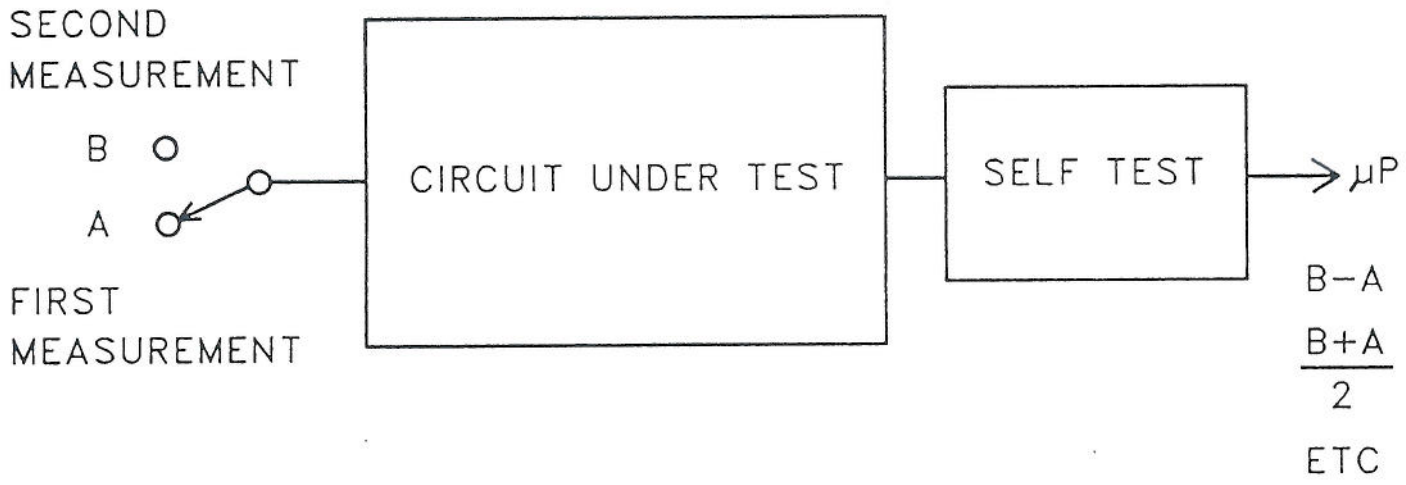
CAL. ANY HI OHMS RANGE $\geqslant$40K,
WITH O/P = TARGET.

+
SELECT
CAP

FORCING CAP SELF CALS

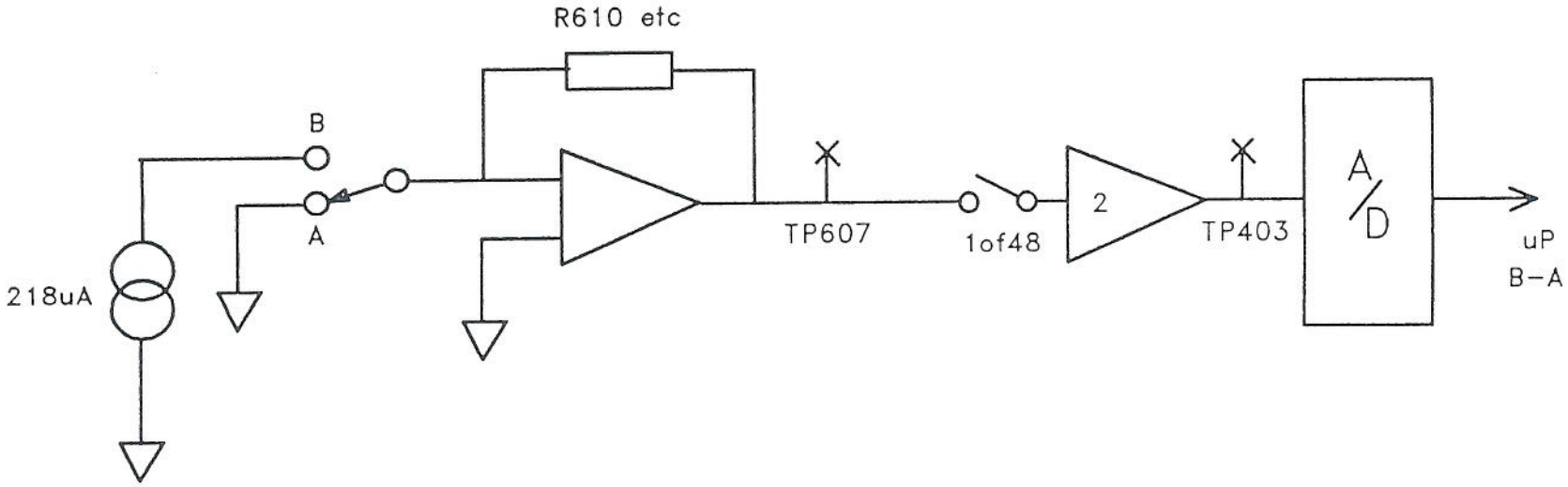
SC2

C62



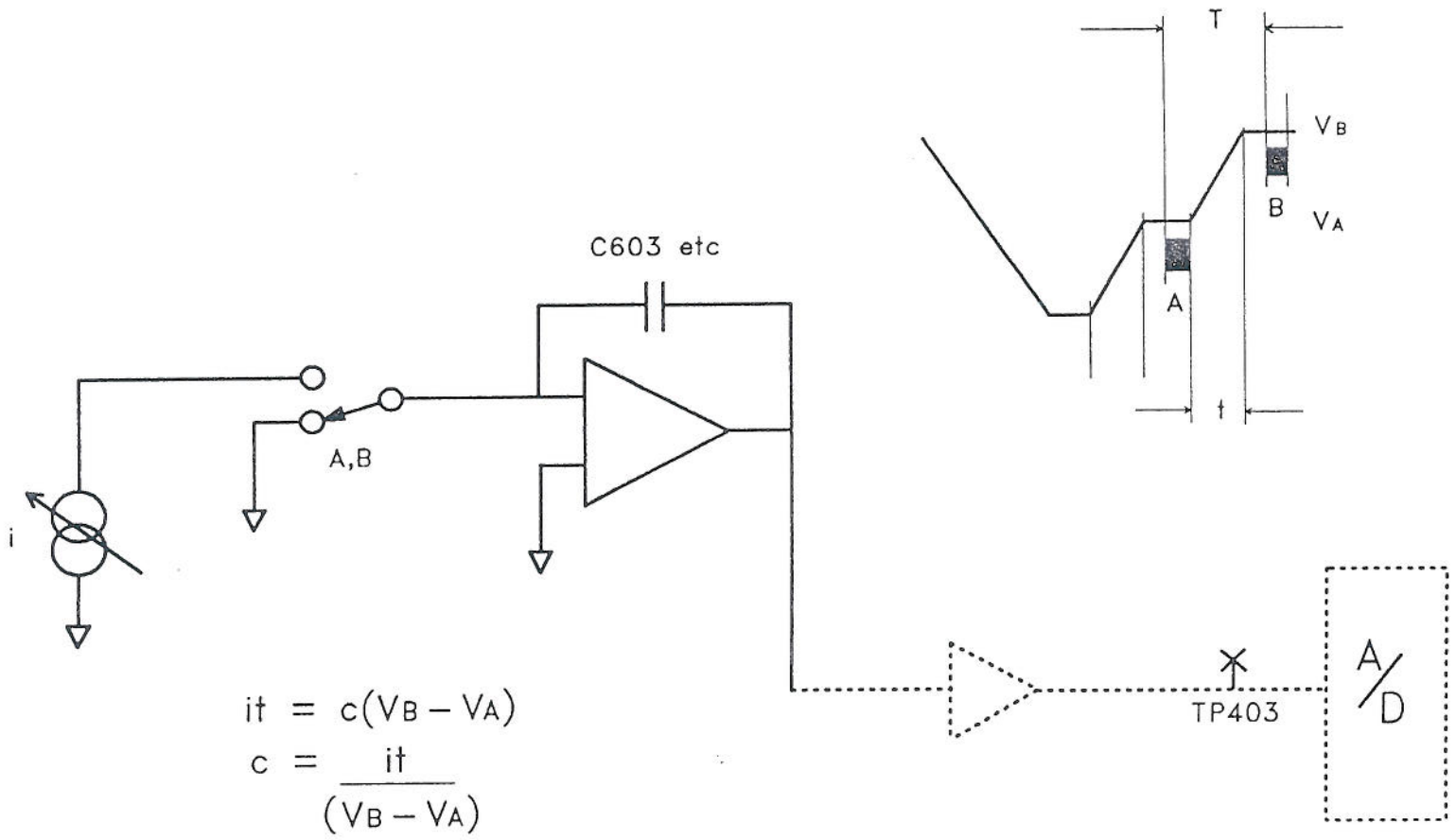
SELF TEST PRINCIPLE

ST ϕ



SELF TEST A06.002

ST 1

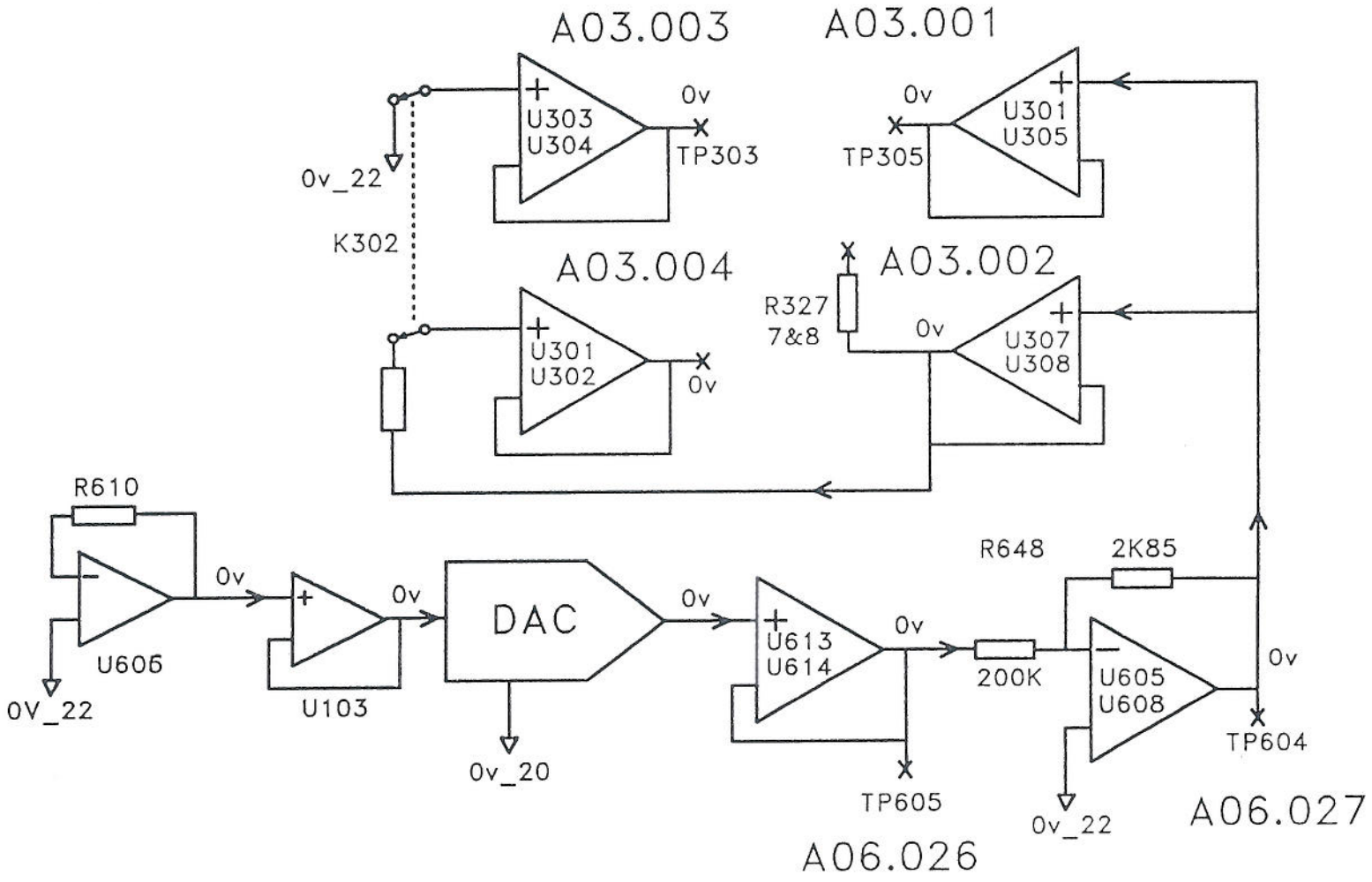


$$it = c(V_B - V_A)$$

$$c = \frac{it}{(V_B - V_A)}$$

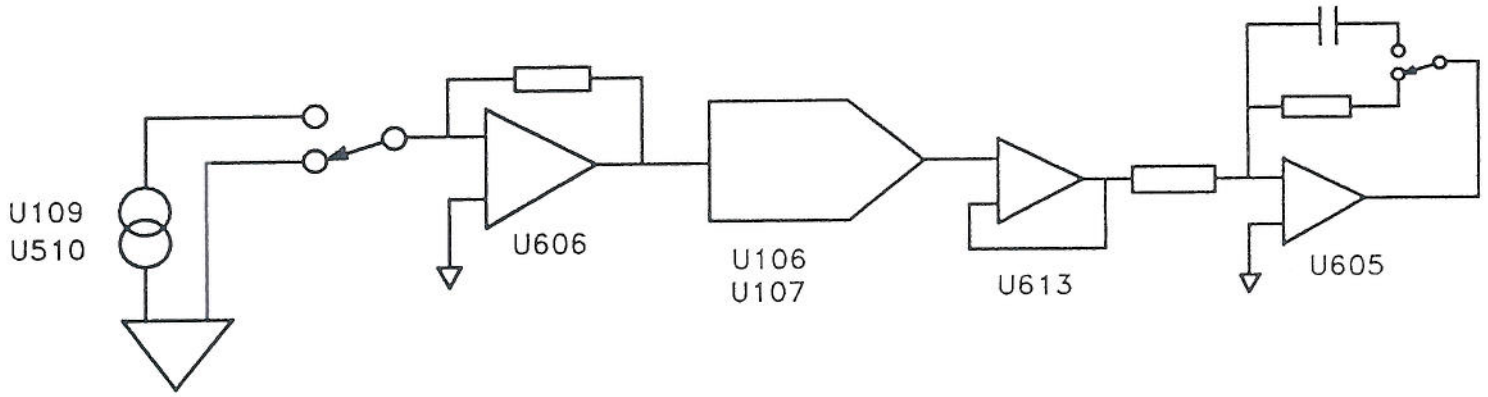
SELF TEST A06.020

ST2



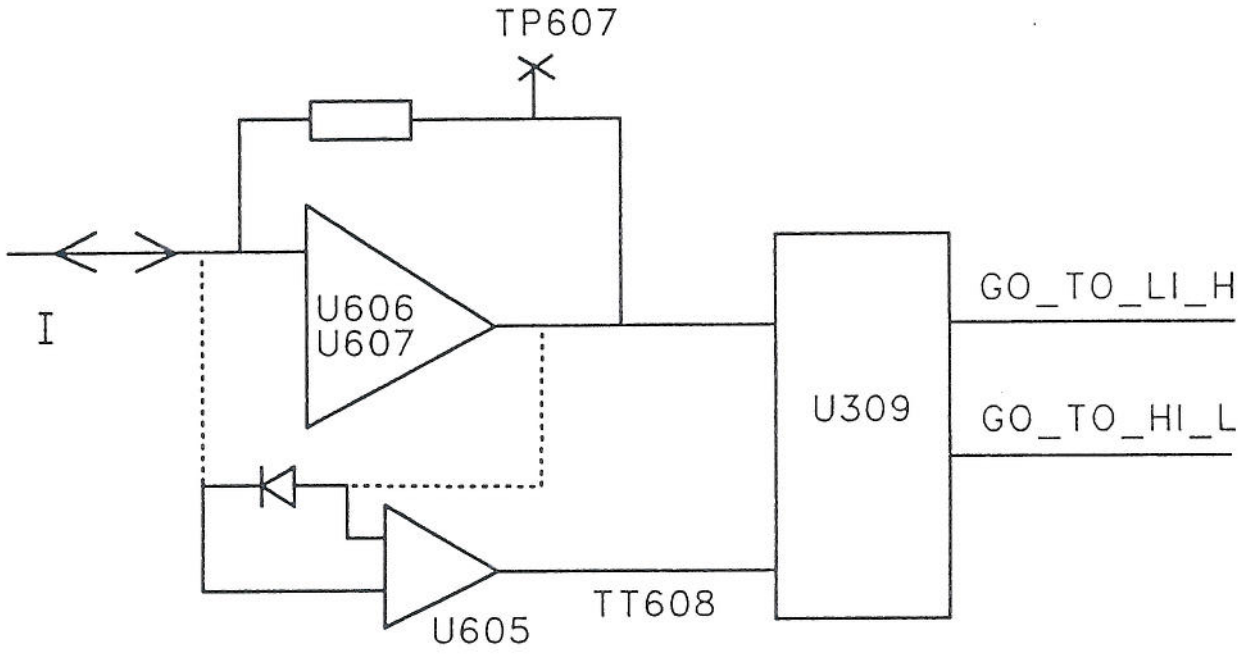
Diag 1. SELF TESTS.

ST3



SELF TESTS A06.028 to A06.036

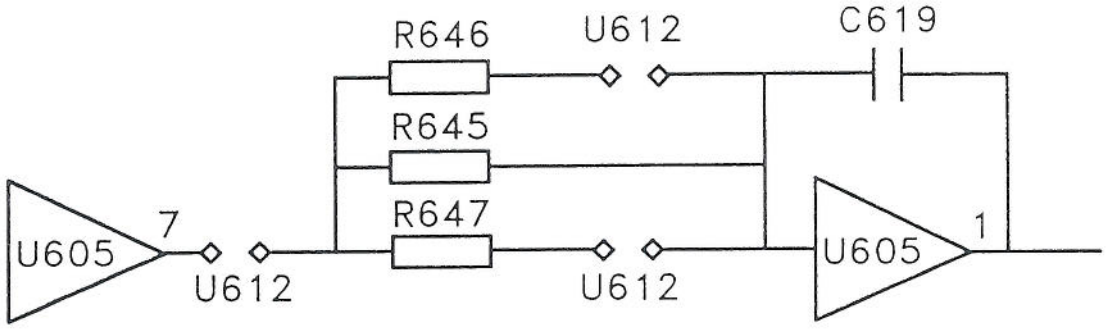
ST 4



SELF TESTS A03.011 TO A03.018
+A06.041

ST5

C63



SELF TESTS

A06.042

A06.043

SEE ALSO

CAP4,

CAP5

ST6

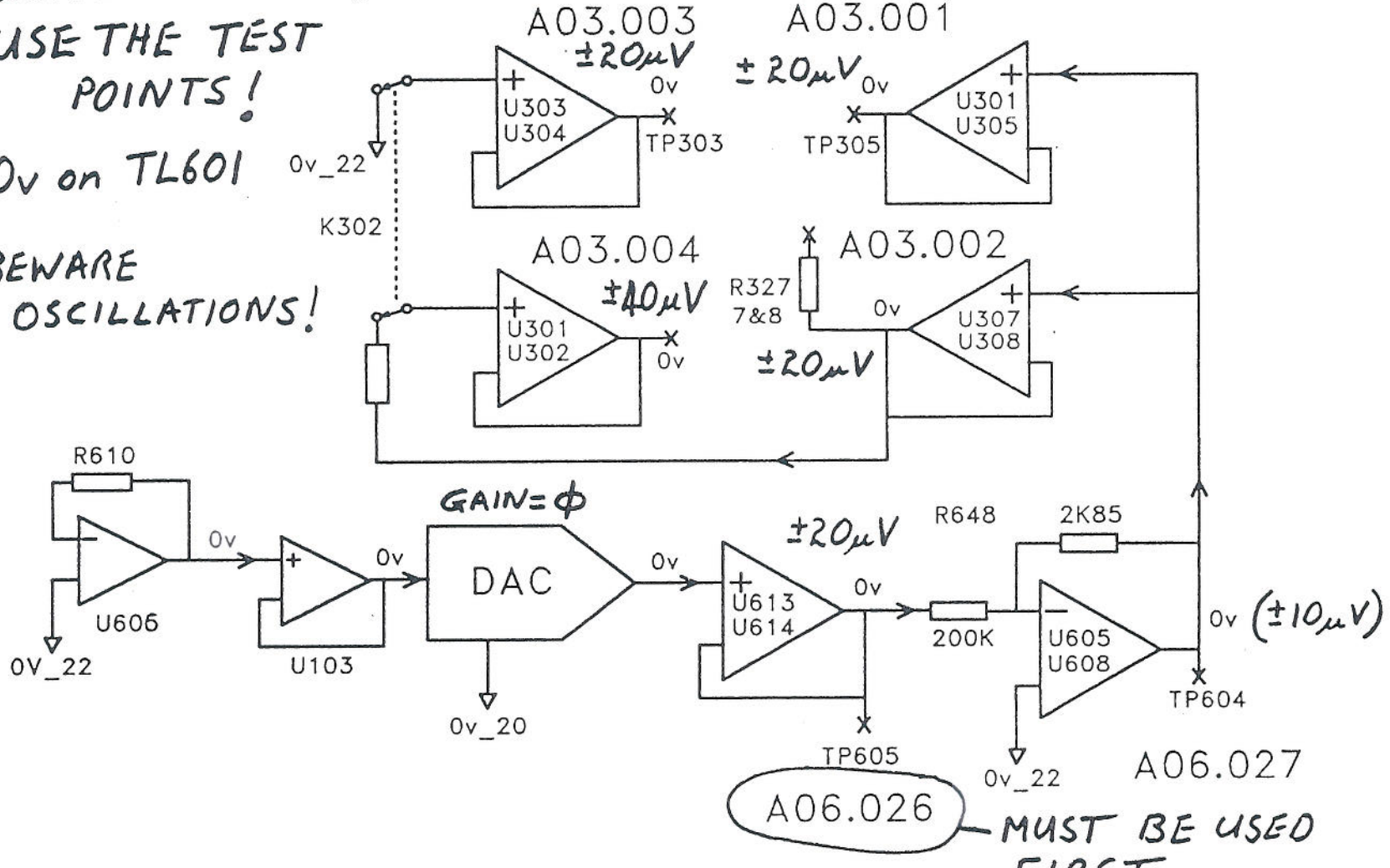
C64

BEWARE THERMALS!

1). USE THE TEST POINTS!

2) Ov on TL601

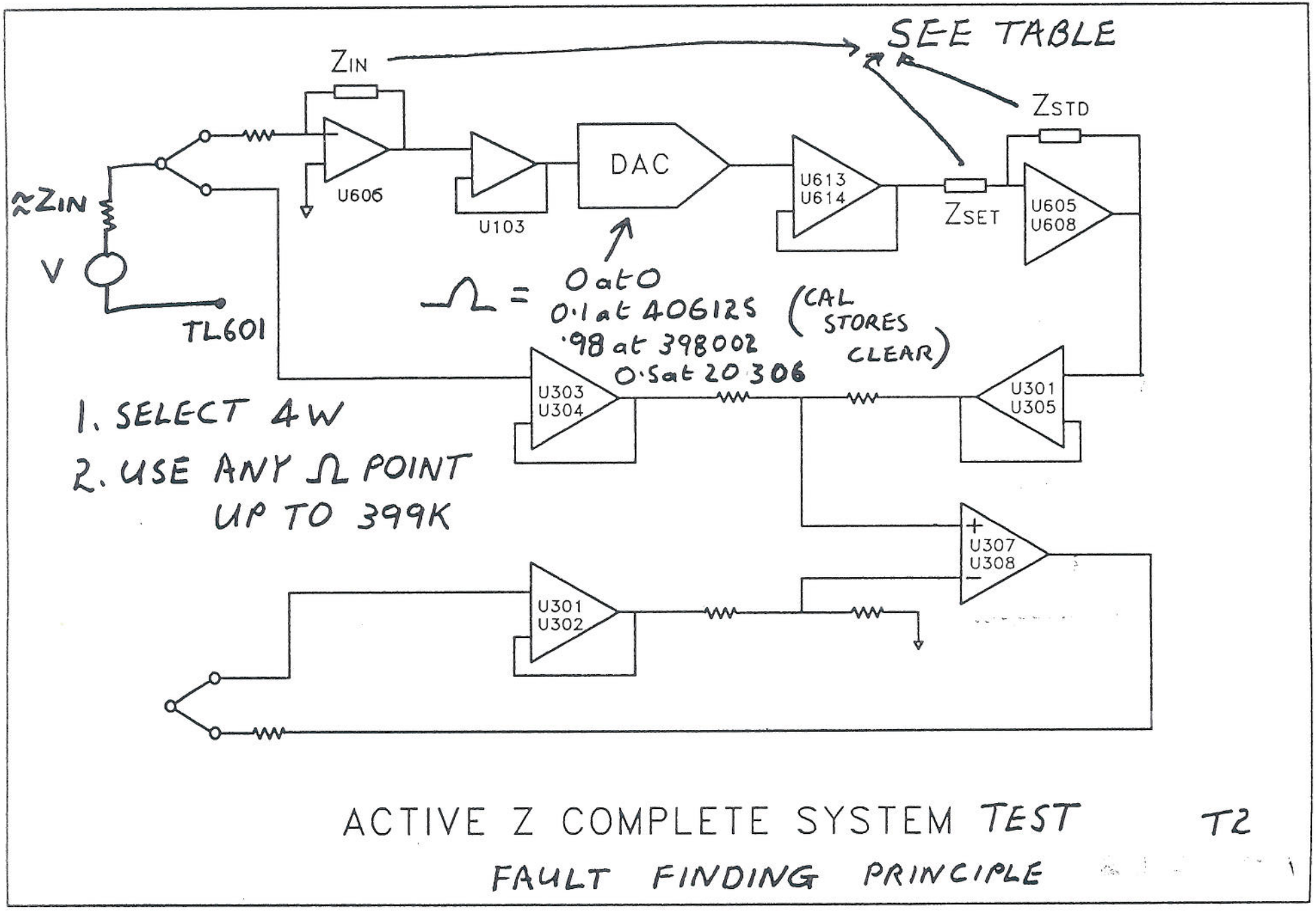
3) BEWARE OSCILLATIONS!



ZERO TESTS.

FAULT FINDING

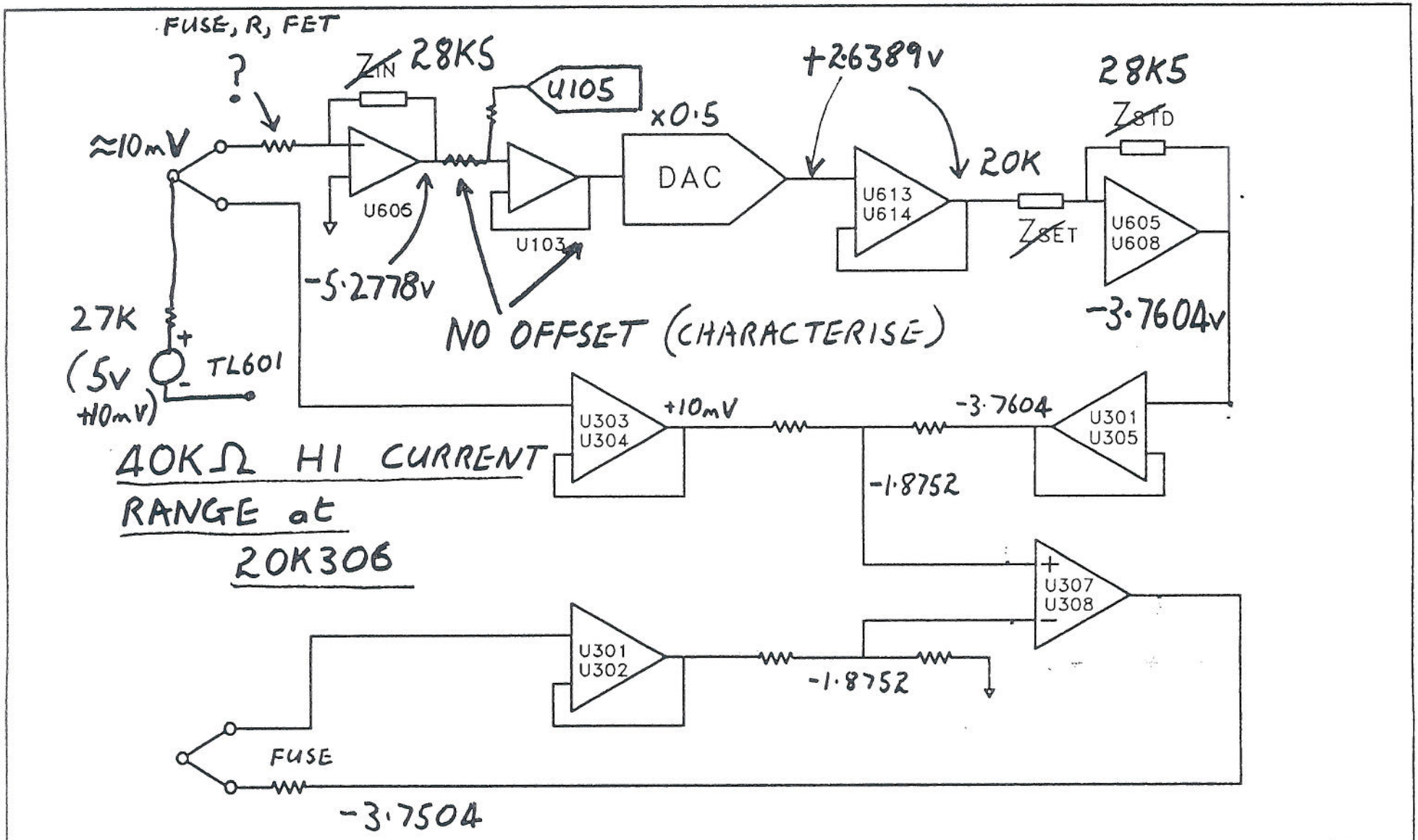
T1



ACTIVE Z COMPLETE SYSTEM TEST

T2

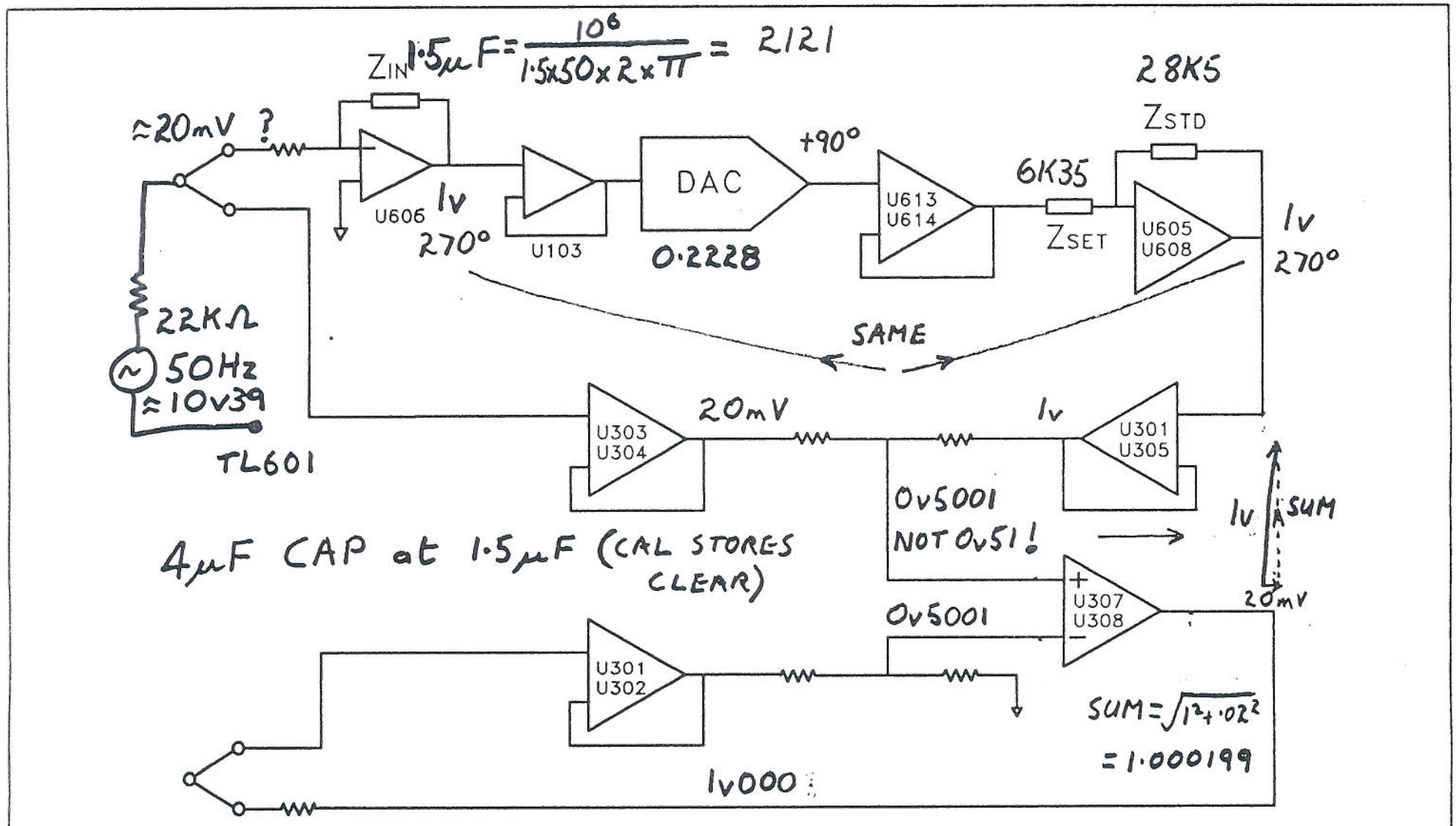
FAULT FINDING PRINCIPLE



EXAMPLE ACTIVE Z COMPLETE SYSTEM TEST

T3

FAULT FINDING

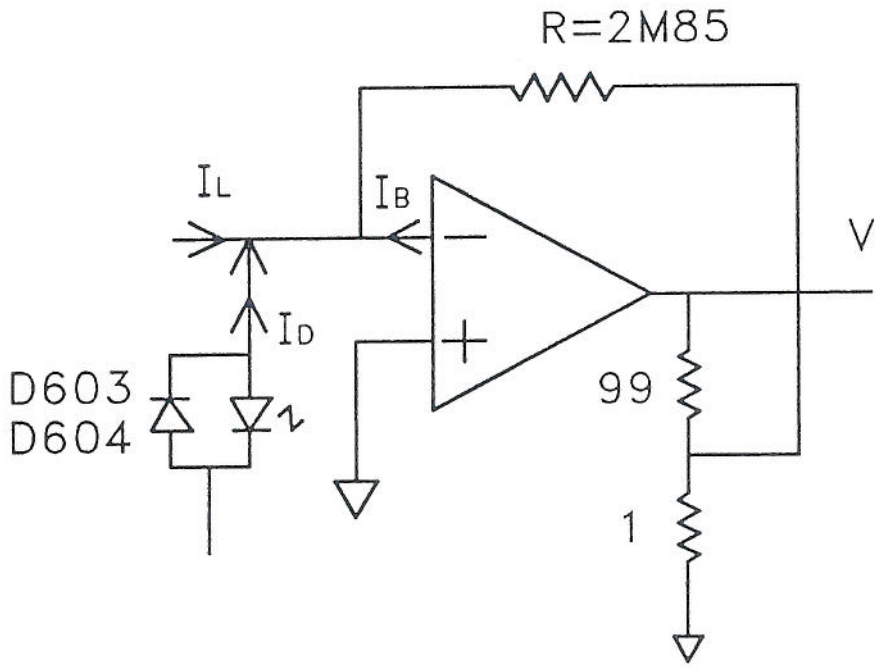


ACTIVE Z COMPLETE SYSTEM TEST

CAPACITANCE

T4

BEWARE I_D DUE TO LIGHT!



SELECT 400M LI
O/P ON
OR A06.014

$V = -IR \times 100$
$= (I_L + I_B) \times 100$
$= 10pA \times 2M85 \times 100$
$= 2.85mV$

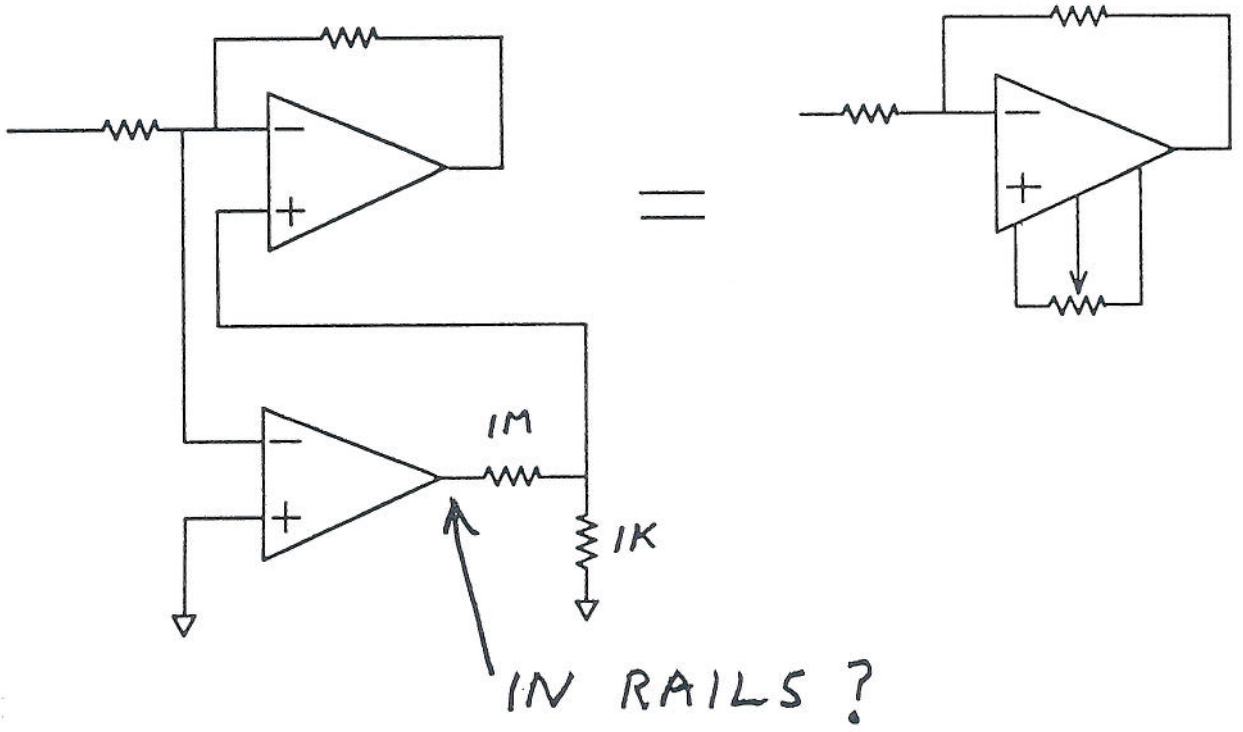
LOW CURRENT ⟶ VOLTS CONVERTER

I_{BIAS} TEST (≈A06.014)

(BOARD, U605, U607,) RELAYS

T5

C60



INVERTING CHOPPER

CHECKING

T6

OHMS & CAP Self Test Descriptions

A06,001
Check zero of composite amp U602 and U607.
Input = OFF Feedback = R610
If fails, check TP607 WRT TL401 (<50uV). Used for maths, establishing offset voltages.

A06,002 to A06,013
These tests all apply zero (A) then INPUT (B).

The result is (B-A). Input is from U109 via 'TICKLE' (zero for A06.012 is in fact +1.1nA).

The table below gives the inputs and expected outputs on TP607 WRT TL401, with the resistor under test circuit designator.

Test	Input "Curtickle"	TP607	Resistor	Volts to A/D (TP403)	Notes
A06.002	+218uA	-0.622V	R610	+1.245V	
A06.003	-218uA	+0.622V	R610	- 1.245V	
A06.004	+21.8uA	-0.622V	R609	+1.245V	
A06.005	-21.8uA	+0.622V	R609	- 1.245V	
A06.006	+35.09uA	-10V	R608	+2.00V	(1)
A06.007	-35.09uA	+10V	R608	- 2.00V	(1)
A06.008	+2u18uA	-6.22V	R611 +R672	+1.245V	
A06.009	-2u18uA	+6.22V	R611 +R672	- 1.245V	
A06.010	+218nA	-6.22V	R611+R672+R668/5	+1.245V	(2)
A06.011	-218nA	+6.22V	R611+R672+R668/5	-1.245V	(2)
A06.012	+35.2nA	-10V	R611+R672+R668/1	+2.00V	(3)
A06.013	-34.1nA	+9.7V	R611+R672+R668/1	-1.94V	(3)
A06.014	0nA	0V	R611+R672+R668/1	0V	(4)

Notes
(1) Checks amp swings +/- also.
(2) Note use of divider R668 Pin 5.
(3) Checks clamp D607, D608 leakages are low.
(4) Bias current test in MATHS.

A06.015 to A06.019 are "Spares"

A06.020 to A06.024 - Capacitance Tests

These tests all force TP607 to the negative rail. A current is then applied and removed to bring TP607 to a linear region (Measurement A). A current is then applied and removed to further charge the capacitor under test (Measurement B). (B-A) gives the voltage change on the capacitor due to I x t (current multiplied by time). From CV=It the value of C is known in Self Cal. In Self Test we just utilise the voltage change B-A. To see the waveforms use a digital scope and the REPEAT TEST button. See ST 2 for sketch of a typical waveform on TP607.

Test	Input "Curtickle"	Time	=Vcap (TP607)	to A/D (TP403)	TP403 Finishes at Nominally	C under test
A06.020	-144nA	0.1s	7.868	1.574	-0.94	C603
A06.021	1.44µA	0.1s	8.52	1.7	-1.2	C604
A06.022	1.964µA	0.5s	6.68	1.3345	-0.43	C605
A06.023	19.2µA	0.5s	6.4	1.3375	-0.46	C606
A06.024	207µA	0.3s	6.22	1.245	-0.4	C607
A06.025	Does not exist					

A06.026 - A03.004

These tests check a series of composite amplifiers, most of which are followers, U608 + U605 being the only exceptions. The main DAC is forced to zero gain and the resulting outputs are measured as a "gross failure" check. The MATHS facility is used to establish the real offset of each amplifier.
Diagram 2 is a sketch of the chain to indicate the signal paths and pick-off points for each test.

Test	Amps offset	Picked Off At
A06.026	U613+U614+DAC	TT605
A06.027	U605+U608	HI_IMP_OUT
A03.001	U301+U305+A06.027	TT304
A03.002	U307+U308+A06.027	TT302
A03.003	U303+U304	TT303
A03.004	U301+U302+A03.002+A06.027	TT301

A06.028 - A06.033

After test A03.004 we are certain that the preamp U606 can swing ±10V and that all other amplifiers are probably working as they have a good zero. It remains to check that all gains subsequent to the preamp are within limits. DC paths are used to check Ohms gain, but this is unfortunately not possible for capacitance gains, and we have to resort to the ramping technique used previously.
All tests go -/+ve on TP607.

Test	Checks	Vp/p	Vp/p on	V Final on TP403
A06.028	Establish preamp span	12.45	TP607	+1.245
A06.029	R648 28k5/20k	17.74	TP604	-1.77

At this point 3 tests are inserted to check followers for swing capability. Setup as A06.029.

A03.005	U301/U305	17.74	TP305	-1.77
A03.006	U307/U308	17.74	TP302	-1.77
A03.007	U301/U302	17.74	TP301	-1.77

Test	Checks	Vp/p	Vp/p on	V Final at TP403
A06.030	R648 28k5/200k	1.77	TP604	-177mV
A06.031	R648 2k85/20k	1.77	TP604	-177mV
A06.032	R648 285k/200k	17.7	TP604	-1.77
A06.033	R648 6k35/28k5	6.68	TP604	-0.4

Test A06.033 is similar to A06.022. The DAC exactly compensates for the gain in R648 of 285k5 / 6k35 and is set to 6.35 / 28.5 or 0.222807.

Both the DAC and U605/U608 invert so the waveform on TP604 is exactly the same as on TP607.

A06.034 to A06.036

Tests A06.034 to A06.036 check R648 700k, 70k, 7k respectively. The same remarks apply which introduced checks A06.020 to A06.024.

Test	Input "Curtickle"	Volts TP607	R648	Current C619	Time	(B-A) Volts C619	TP403 (B-A) Volts	TP403 Ends at.
A06.034	24µA	6.84	700k	0.977µA	1.13s	-1.08	+0.22	+2V
A06.035	24µA	6.84	70k	9.77µA	0.5s	-4.88	+0.977	+0.25
A06.036	12.05µA	3.42	7k	48.85µA	0.1s	-4.91	+0.981	+0.25

A03.011 to A03.018

It is now required to check the error lines GO_TO_LI_H and GO_TO_HI_L in all possible states. The test setup is exactly as A06.006 except that the input volts (and hence TP607) are raised.

Test	TP607	GO_TO_LI_H	GO_TO_HI_L
A03.011	>10V	0	0
A03.012	10V	0	1
A03.013	1.0V	0	1
A03.014	0.4V	1	1
A03.015	-0.4V	1	1
A03.016	-1.0V	0	1
A03.017	-10V	0	1
A03.018	<-10V	0	0

Note:- 1 = +5V, 0 = 0V

Note that the input HI_CLAMP comes from the middle of the clamp circuit and a fault in this will cause failure(s) in these tests. (LO_CLAMP is direct from TP607). It is the correct operation of the clamp circuit which causes HI_CLAMP to exceed "one diode drop" and hence change GO-TO_HI_L. There are no A/D measurements in the above tests.

A06.041

Test A06.041 repeats the setup of A03.011 and A03.018, but U605/7 is monitored via TT608. This is the output of the clamp circuit. The limits are set very wide, but typically expect 1.0 to 1.4 volts to be indicated as a result on the display. The input to U605 is a ±0.7v in turn seen across D609 and D610 when the clamp conducts, and this has a gain of 1 to the A/D input TP403.

A06.042-A06.043

Tests A06.042 and A06.043 use the output of U605 as in test A06.041 above. This output was originally used to discharge C619 via R647, R646 and R645 in 400µF, 4mF and 40mF ranges. We can only test the first two, as the 40mF takes far too long to attain an accurate result. The waveforms are similar to those described in the introduction to A06.020 to A06.024. The input to U605/7 is obtained by making the clamp circuit Q606, Q607 etc conduct, with TP607 at more than ±10v.

Test	Resistor	I Nominal	Time	(A-B) on TP604	(A-B) on TP403
A06.042	R647	60µA	0.5sec	3.0	0.6
A06.043	R646	12µA	1.0sec	1.2	0.24

MATHS TESTS

Test	Source	Limits	Possible Fault if Fail
A06.M01	A06.007+A06.006	0±0.0027	Clamp Serious Level Fault
A06.M02	A06.009+A06.008	0±0.002	R611+R672 Fault
A06.M03	A06.010+A06.011	0±0.002	R668 Fault + R611 & R672
A06.M04	A06.013+A06.012	0±0.006	R668 Fault, R611 + R672, Ground Offset, U105 Non Linearity. (Note 1)
A06.M05	A06.014-A06.001	0±0.0057	U606, U607 Q611, Q613, Q602, Q604, Q614 Ibias or Igate
A06.M06	A06.026-A06.001	0±0.0004	OFFSET U613/U614 (Note 2)
A06.M07	A06.027-A06.026	0±0.0004	OFFSET U605/U608
A03.M01	A3.001-A06.001	0±0.00015	OFFSET U307/U308
A03.M02	A3.002-A06.027	0±0.00015	OFFSET U301/U305
A03.M03	A3.003-A06.001	0±0.00020	OFFSET U303/U304
A03.M04	A3.004-A03.001	0±0.0001	OFFSET U302/U301 (Note 3)
A06.M08	A06.029/A06.030	10±0.03	R648 20k/200k RATIO (Note 4)
A06.M04	A06.029/A06.031	10±0.03	R648 28k5/2k85 RATIO
A06.M10	A06.029/A06.032	1±0.004	R648 285k/28k5 RATIO (Note 5)
A06.M11	A06.042/A06.043	2.75+1.5-0.75	CAP DISCHARGE RATE - U605 etc R647, R646

NOTES:-

1. U105 can give unequal ± o/p at these low levels. A swap with U107 can help. Early boards had U105/2 to ST401. This was changed by ECO to ST402. A 'cut and link' is required.

2. Serious ground current errors can cause failures - check 0V_20 WRT 0V_22A.
3. Very early models require an ECO to join K302/9 to 0V_22 and K302/2 to RGC_P_NEG via 100k.
4. Switch errors can also cause faults - an O/C drive is most likely.
5. If A06.M08 fails, this test will fail as well.
6. Note factory limits are usually 0.75 x Nominal and customer limits are 2 x Nominal.

CIRCUIT DESCRIPTION - POWER PCB.

HIGH VOLTAGE OUTPUT.

All output voltages greater than 3.2V ac/dc are produced by amplification of DAC output signals on the power pcb. ALL range amplifiers are non-inverting.

30V AC/DC (401096 sht 2 & 401097 sht 9)

These ranges are produced by x5 amplification of the DAC_OUT_1 signal from the main DAC. It is input via U901 (analog) on the HV_IP net. The attenuator R247 defines the performance of the 30V amplifier and sufficient precision is obtained without any additional measurement loops. In 30V ac/dc ranges, the voltage amplifier main power supplies HV_PS_POS and HV_PS_NEG are at +/-70V respectively (unregulated). Discrete stages Q201 through Q212 form the actual amplifying stage with R247 and U204 'closing the loop' to the required gain and precision.

Complementary current mirrors Q209/Q217 mirror the current in the output devices, and thus the voltage developed across R262 & R263 is a measure of output current. U206/R265/R266 provide three discrete levels of overload detection for various ranges. For 30V ac/dc the detector is at its most sensitive setting (upper switch of U206 ON).

When not in use, the discrete stages are disabled by turning off the V/I stage Q201 (and thus all following stages). This is done by taking U204-3 to +15V with HV_IP_ON_H.

The output devices are biassed to class A/B by the U205/Q205 shunt regulator, temperature compensated by Q204 (mounted on h/s in close proximity to output devices). Bias is set by demanding 3.3VAC/1kHz and adjusting R208 for 240mVDC across R218 with no external load. This must be verified before any further fault-finding is attempted. (If set too low, oscillation will occur due to loss of bandwidth in output followers. Too high and output capability will be reduced and in extreme cases may result in thermal runaway of output devices).

Q202/Q203/C209 form an 'active smoothing' circuit for the cascode amplifier stage positive supply. This stage has no rejection whatsoever to noise/ripple present at the 'cold' end of its load resistor, so a clean supply is essential.

Q208/Q212 are protected in the short term by Q207/Q211 which limit drain current to approx. 600mA peak.

100V AC (401096 sht 2)

30V description applies except:-

a) HV amp PSU raised to +/-200V (protected).

b) Gain increased from x5 to x17 (by K202).

c) Cascode stage load resistor and other biasing w/w resistors increased to suit higher supplies (by K201).

Again , sufficient precision is obtained without recourse to any additional measurement loops.

300V DC (401096 shts 1 & 2)

Basic output is produced by feeding an appropriately scaled trapezoid waveform from the DDS to the 30V amplifier input via the HV_IP net. The VPA is configured as for the 30V range except that the overcurrent detector sensitivity is lowered (both U206 switches ON).

The amplified trapezoid is ac-coupled to the HFTX primary, the secondary driving a diode voltage doubler/filter arrangement with built-in polarity switching.

Having produced the basic output power at approximately the right level, (this open-loop gain is trimmable via an FSV on the analog pcb.), an outer loop is used to fine trim the output to req'd ppm levels. The 300V/1kV attenuator assy sits between doubler output and ground, and in the 300V range has a ratio of 51:1. Output of the attenuator is compared to the DAC_OUT_1 signal in error integrator U104. U104 output is amplified by approx x5 in the control amplifier and used to 'tweak' the earthy end of the floating voltage doubler to close the loop.

The control amp input is monitored for overdrive (indicating loss of feedback in the loop). Excessive corrections trigger the overcurrent 'etector via D119/D120 and the CA_OVDRV net.

1kV DC (401096 shts 1 & 2)

As 300V DC except:-

a) PA configured as for 100V AC wrt gain, power supplies, and biasing components.

b) Overcurrent detector to least sensitive level. (U206 lower switch ON).

c) Attenuator assy ratio changes to 176:1 (by K109).

300V AC (401096 shts 1 & 2)

Here the 30V amp is used via one of two 1:10 step-up transformers. The LFTX T101 is used for 40Hz to 3kHz outputs and the HFTX for frequencies higher than 3kHz (max = 30kHz). Since the transformers have significant performance imperfections, a non-precision feedback loop consisting of R137/R138/R139 attenuator and error amp U104 is used to reduce the effects of:-

a) Distortion due to core effects @ low freq end of each transformers span.

b) Flatness errors-these are substantial with the LFTX in particular due to resonances.

c) Output Z effects. These again are large with the LFTX due to high winding resistance and leakage inductance.

The gain of this inner loop is approx 11 and is set by R136/R139. Output/input gain is approx 51:1, set by R138/R139.

Overcurrent detector sensitivity is medium (both switches of U206 ON) for LF freqs and low (U206 lower switch ON) for HF freqs.

The inner feedback loop still does not provide the necessary precision so a further outer control loop with high gain is required to bring performance to ppm levels. This works by comparing the output from the 300V/1kV precision attenuator assy (51:1) with the AC reference input on DAC_OUT_1. This is achieved by complementary matched precision rectification of both input signal and attenuated output. The rectifier outputs are summed and integrated in U108 to control a varible gain buffer U109 so as to bring the two signals to the same mean amplitude, thus closing the control loop and stabilising the gain of the system to ppm levels. Performance of this system relies heavily on signal purity as regards the input signal since the loop is vulnerable to mean-sense errors. These impact on flatness, particularly around 1.5 to 3kHz. For this reason, flatness spec tends to be wider than 30/100V AC ranges.

1kV AC (401096 shts 1 & 2)

As 300V AC except:-

a) PA config'd as for 100V AC wrt gain, power supplies & biasing components.

b) Overcurrent det to lowest sensitivity (U206 lower switch ON) for all freqs.

c) Attenuator assy & inner non-precision attenuator both change to 176:1 (by K109).

+/-70/200V PSU switch and Display PSUs (401096 sht 5)

Power mosfets Q505/Q508 are fully enhanced when the HV_PS_ON_H line is taken high to raise the normally +/-70V supplies to +/-200V. Average drain currents are monitored by Q503/Q506 and an error flag HV_PS_OL_L is produced if either exceeds approx 200mA. Software then removes the enabling signal and forces neutral state. The +/-70V supplies are not monitored for overcurrent.

+/-70V and +/-200V (switched by Q505/Q508) are diode-ORed to produc the PA supplies HV_PS_POS and HV_PS_NEG.

Q511 circuit produces -22V regulated from the -70V rail to power the display (not overcurrent protected).

Q512 circuit produces +12V regulated for the display backlight inverter. It can be shutdown for standby by LCD_BL_ON_L going high. The +12V supply is not overcurrent protected.

DC HV Control Amp (401096 sht 1)

This block operates fron +/-70V supplies and when not in use has its input grounded via R119. When the input of U105 is driven, The load resistor on U105 output causes differentials in the supply rails to the op-amp. These currents pass to mirrors on the +/-70V rails (via cascodes Q101/Q105). Mirror ratios are 1:1 and the output voltage is developed across R121, to be buffered by Q103/Q108 which are in turn biassed into class A/B by D107/D108. Gain of this discrete section is approx 4.

Overall feedback is applied to U105 inverting input via R132/R133 to set the closed-loop gain to approx 4.9 .

A degree of protection is provided by ballast resistors R115/R127 in the +/-70V rails.

LF Pulse Range (401096 sht 2 & 401097 sht 9)

For pulse outputs at freqs of 1kHz and lower, and peak amplitude of more than +/-6V, the pulse system output is routed via U901 (analog) to the 30V amplifier before passing to the output. Configuration is identical to 30V AC/DC cases and up to 60V ptp is available.

R201/C244 slow the fast edges from the pulse output stage to prevent overshoot and ringing of the PA.

HIGH VOLTAGE & POWER SUPPLIES
SELF-TEST DESCRIPTION

P05.001 - Tests +5V PSU via R546. Inst state = NEUTRAL.

P05.002 - Tests +15V PSU via R541. Inst state = NEUTRAL.

P05.003 - " -15V " " " " " "

P05.004/P05.005 - Tests high-I +/-7.5V supplies via R546.

P05.006 - Tests -22V PSU via R545. Inst state = NEUTRAL.

P05.007 - " +70V " " R532/R533/R534. Inst state = NEUTRAL.

P05.008 - " -70V " " R535/R536/R537. " " " .

P05.009 - " +200V " " R532/R533/R534. Inst state = NEUTRAL except:-
a) HV_PS_ON_H is taken HIGH (to enable +/-200V).
b) Relay K202 is energised (to protect R247).

P05.010 - Tests -200V PSU via R535/R536/R537. Inst state = as for P05.009.

P02.001 - Tests 30Vamp positive swing via R250/R251 - main DAC = +FS.

P02.002 - " " zero output " " " - " " = ZERO.

P02.003 - " " negative swing " " " - " " = -FS.

P02.004 - " " inverting input with main DAC = ZERO.

NOTE - The following tests involve 100V/300V/1kV operation. Remember there is no warning beeper in self-test mode.

P02.005 - As P02.001 except PA config'd for 100V AC range. To prevent overstressing of w/w resistors in PA, pathway exists only for duration of test.

P02.006 - As P02.002 except PA config'd for 100V AC range.

P02.007 - As P02.005 except main DAC = -FS.

P02.008 - As P02.004 except PA config'd for 100V AC range.

P01.001 - Output of DC HV error amp U104 @ +FS on 300V DC range via R111
---
and EA_TST.

P01.002 - Output of DC HV control amp @ +FS on 300V DC range via R102/R142
---
and CA_TST.

P01.003 - Output of 300V DC system @ +FS via R102/R142 and VHV_AMP_TST.

P01.004 - Check inverting input of error amp U104 @ +FS via VHV_ATT_TST.

P01.005 - As P01.001 except main DAC = -FS.

P01.006 - As P01.002 " " " " .

P01.007 - As P01.003 " " " " .

P01.008 - As P01.004 " " " " .

P01.009 - As P01.002 except done @ +FS on 1kV DC range.

P01.010 - As P01.003 " " " " " " " " .

P01.011 - As P01.004 " " " " " " " " .

P01.012 - As P01.002 " " " -FS " " " " .

P01.013 - As P01.003 " " " " " " " " .

P01.014 - As P01.004 " " " " " " " " .

The remaining tests check that the HVAC VCA control port voltage is "within bounds", inferring locking of the outer measurement loop. (via AC_HV_TST).

P01.015 - 320V/40Hz
P01.016 - 320V/3kHz
P01.017 - 320V/3.1kHz
P01.018 - 320V/30kHz
P01.019 - 1050V/40Hz
P01.020 - 1050V/3kHz
P01.021 - 1050V/3.1kHz
P01.022 - 1050V/10kHz
P01.023 - 500V/20kHz
P01.024 - 330V/30kHz

Math Tests

These can only be viewed via the self-test print-out facility, and only ever appear on the screen if they fail. Even so, the constituent test results are not shown on screen, so a full printout is necessary to chase any math test failures.

The four range configurations are checked for +/-FS gain and input offset. The equations used in the math tests are given below:-

P02.M01 - 30V amp input offset. A01.040-P02.004

P02.M02 - 30V amp gain pos. (P02.001-P02.002)/(A01.036-A01.040)

P02.M03 - 30V amp gain neg. (P02.003-P02.002)/(A01.037-A01.040)

P02.M04 - 100V amp input offset. A01.040-P02.008

P02.M05 - 100V amp gain pos. (P02.005-P02.006)/(A01.036-A01.040)

P02.M06 - 100V amp gain neg. (P02.007-P02.006)/(A01.037-A01.040)

P01.M02 - 300V DC system input offset +FS. A01.036-P01.004

P01.M03 - " " " " " -FS. A01.037-P01.008

P01.M04 - " " " gain +FS. P01.003/P01.004

P01.M05 - " " " " -FS. P01.007/P01.008

P01.M06 - 1kV DC system input offset +FS. A01.038-P01.011

P01.M07 - " " " " " -FS. A01.039-P01.014

P01.M08 - " " " gain +FS. P01.010/P01.011

P01.M09 - " " " " -FS. P01.013/P01.014

HIGH VOLTAGE - SERVICING AND FAULT FINDING

Safety First

a) Never work with both hands when instrument switched on. The 9000 is more dangerous than a floating source in this respect.

b) When using self-test pathways involving high voltage configurations remember there is no warning beeper.

c) If the PA is faulty, remove the +/-200V fuses F501/F502 and work in the 30V range until the fault is cleared.

d) When F501/F502 are fitted, there is a 3.9 second RC on the main reservoirs C501/C502. Therefore wait about 20 sec before touching PCB.

e) Never switch on with U801 not present : relay and subsystem control lines will be undefined and a bad 'blow-up' will result.

Connections

Remember it is not necessary to re-connect the high-current secondaries to run the high-voltage section. Slide some thin card between the PCB lugs and transformer connections. Both star points must be screwed down as must the LFTX right-hand mounting lug. This connects the core to chassis and screens the high-voltage secondary. Electrostatic coupling and oscillation may occur if core not grounded.

Power Supplies

The display supplies (+12V & -22V) are not overcurrent protected so expect damage if these are shorted out. This usually takes out the series pass transistor and associated transzorb. The base-defining zener/diode chain may also be damaged. -22V supply damage results in blowing of the +/-70V fuses and can easily be mistaken for a PA fault. A good indication of this fault is blown +/-70V fuses and intact +/-200V fuses. Watch out for the LFTX RH mounting lug shorting to -22V track close by (especially on early units).

The +/-200V switch circuit rarely gives trouble but following any kind of PA 'blow-up' it pays to check Q505/Q508 and zeners D535/D536. Failure to do this could result in +/-200V to the PA in 30V mode which would most likely re-damage the PA. The w/w resistors and attenuator R247 would certainly be seriously overstressed by this.

Power Amp - Common Faults

a) Insulator Breakdown @ Q208/Q212

This was common and a serious problem on older units using 'Kapton' (yellow) insulators. These are now mica and the problem has gone away, but some very early units were shipped with the Kapton insulators. Once breakdown occurs, a short is formed and is permanent. Always replace insulators with the mica type for improved reliability. This is quite damaging if it occurs : R218/R237 go open and R220/R238 vaporise as a result. Other bits to check are Q208/Q212/Q505/Q508/D535/D536 & R219/R222/D207/D211. If either of the output mosfets are damaged, check also the driving follower and current limiter.

b) Noisy - Gain Stepping (Worst @ 100kHz)

Caused by Q204/heatsink interface having a DC leakage, the effective resistance being high and intermittent in value. This was seen only with Kapton and should have gone away. It causes gain variation in the main cascode stage and is best looked for at the output of the OP37. Here the full magnitude of the gain change will be seen, even at LF. At the output, the effect is diminished by the loop gain of the amplifier. This is related to dirt behind the transistor rather than breakdown and has been seen in both 30V and 100V ranges.

'Value stepping' of the cascode stage w/w load resistors has also been encountered, but more rarely than the insulator problem.

50/60Hz noise will get everywhere if the active smoothing driver supply is broken, causing noise and 'beating' problems. Check with 'scope.

Always look carefully for oscillations when chasing noise problems.

c) KWV Series Wirewounds

Only fitted to engineering models. There was a reliability problem and none were shipped. To use an engineering model for demo etc, they ought to be replaced.

d) 30V DC Offset / Linearity Problems

1) Check 3V range to ensure fault is with power board.
2) D219 to D222 leakage. Try lifting them - they are only clamps.
3) D229/D230 leakage - they can be carefully disconnected when the amplifier is ON. They prevent a relaxation oscillation which can occur when entering the range.
4) Leakage @ U203 or U406. U203 can be replaced and U406 unplugged.
5) Check for oscillation @ various levels between -32V & +32V.
6) Poor (resistive) connections @ main star points. Check also on

analog PCB.

7) R247 faulty. One unit only seen with 15ppm settling over about 20 sec to final correct value.

8) OP37 excessive bias current - seen only once - caused failure of P02 "zero" tests.

e) Oscillation or Thermal Runaway

1) Bias setting incorrect - see circuit description or test proc.

2) Thermal runaway @ full power on 1kV ranges (trips HV power supply after about 15 mins). Seen on two engineering models only and cured by replacing Q208 & Q212.

Inner HV Loops and Transformers

Will not turn on @ 1050V/40Hz - check transzorbs across TX primary coupling caps as there can be a few volts offset at the PA output, exacerbating transformer saturation problems. Slow ramp-ups are used on the 1kV AC range to reduce flux peaks at these lower frequencies. Ramp-down to 320.01V occurs for certain frequency changes for the same reason. Another clue to DC on the primaries is excessive core noise from the HF transformer.

Earlier units had LF transformers with higher leakage inductance. This caused peaking such that inner loop flatness error could be up to +30% at 3kHz. A large damping resistor is fitted to these units. The TX was improved and the resistor removed. If flatness problems persist around 2 to 3kHz (usually -500ppm'ish) on these older units then the TX /damping resistor mod should be done.

The inner AC HV loop may be 'opened' by shorting out R136.

The DC HV doubler/filter has no history of problems.

Outer HV Loops

The DC HV control amp has no history of problems and may be worked on in the neutral state. (The input is grounded by R119).

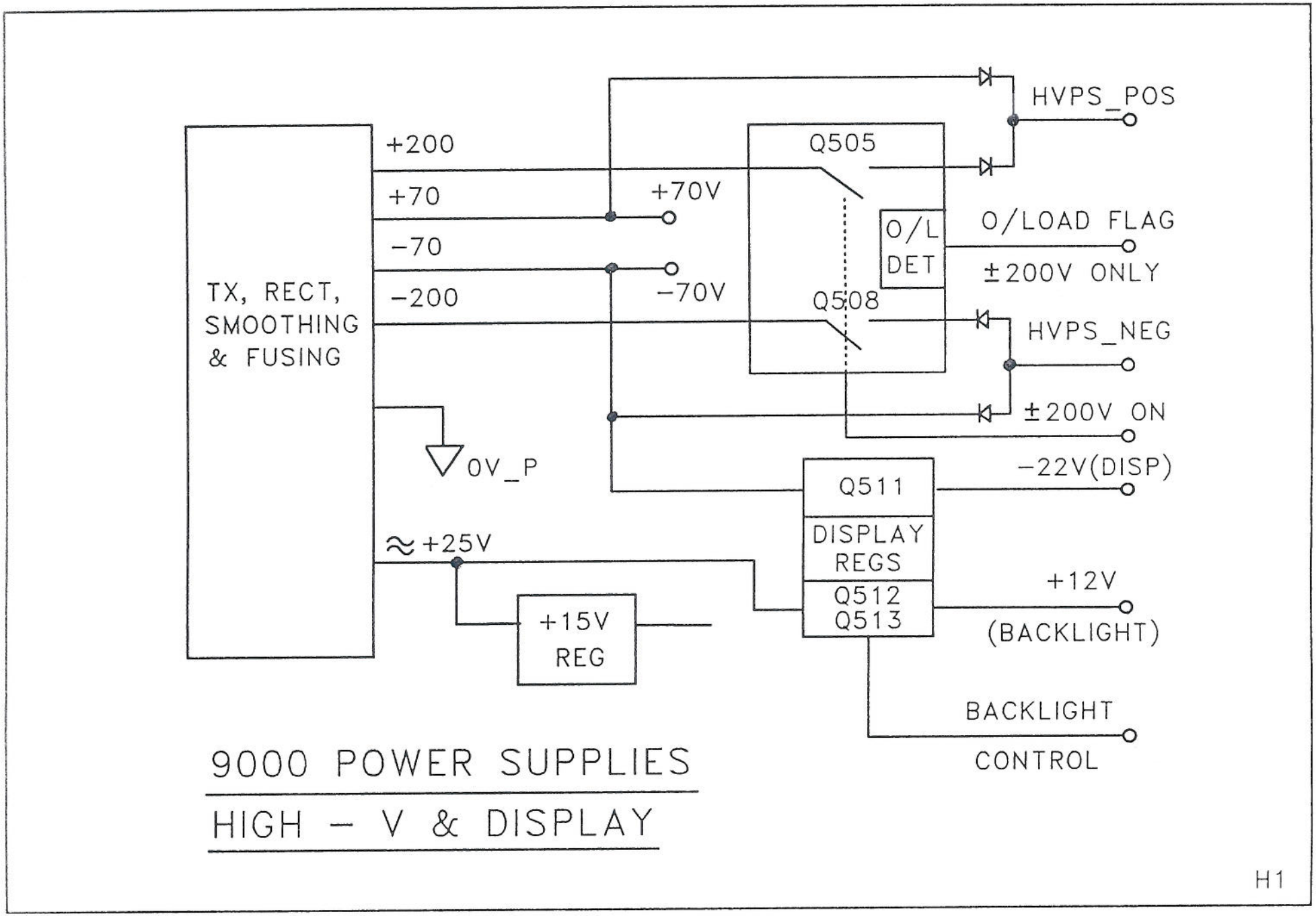
The AC HV precision rectifiers have seen some changes. Very early units with OP270's in U106 & U107 positions may have poor 300V/30kHz linearity (caused by marginal slew-limiting). They should be changed for the later types (AD712/OP271).

Excessive offset at either U106/U107/U108, diode leakage, or excessive op-amp bias currents will cause poor LF linearity.

The outer loop may be 'opened' by linking TL101. The VCA then runs at a nominal gain of 1.

Flatness problems due to PCB effects (hook) in the attenuator assy have been experienced with some non-approved suppliers' boards. Errors of up to +2000ppm @ 20kHz have been seen. The only fix is another assembly - the resistors can usually be reclaimed. C132 is for HF flatness compensation, and if of the wrong value can prevent calibration @ 330V/30kHz.

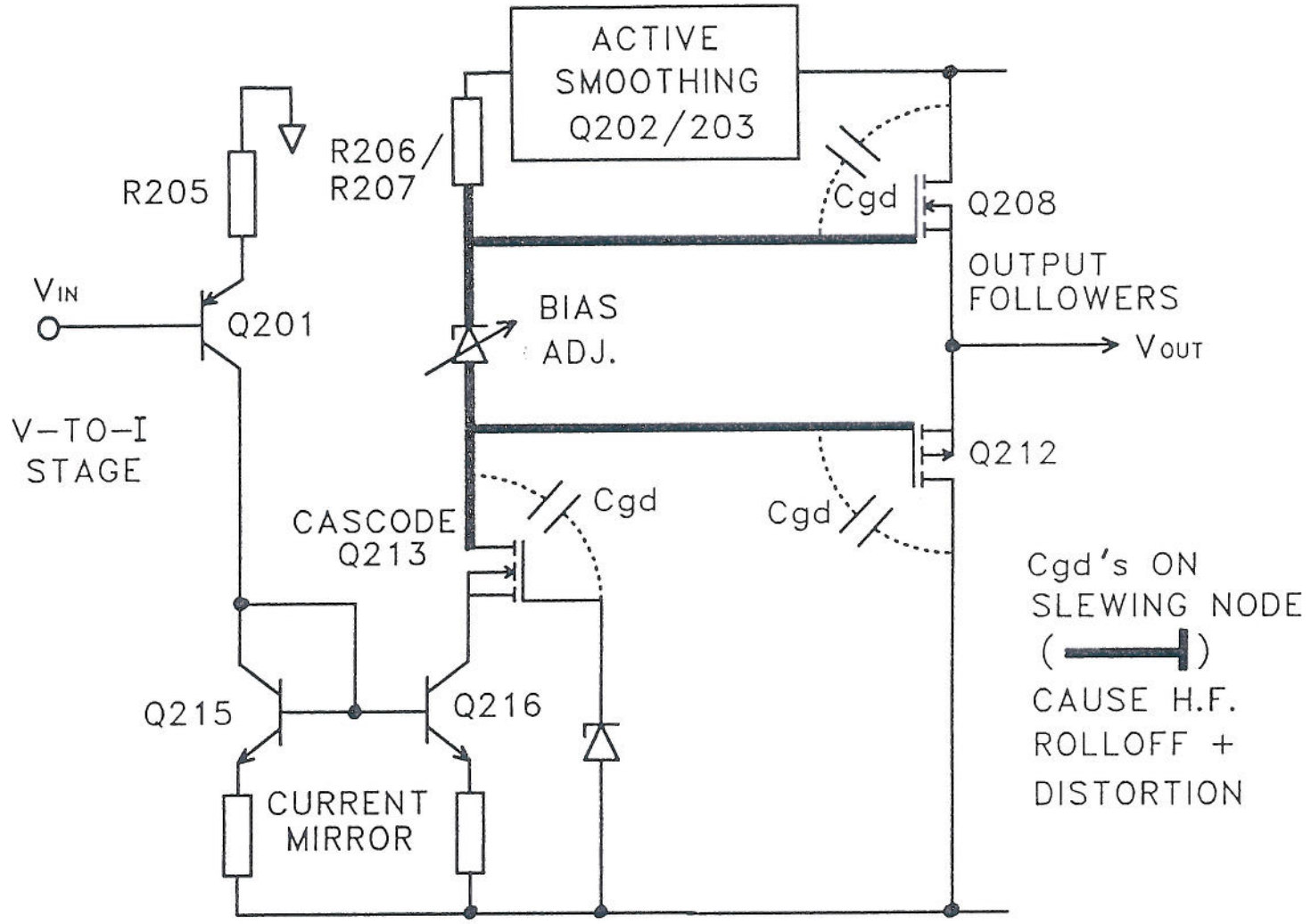
Remember the outer loop is dependent on signal purity from the analog board and within the amplifier. Excessive distortion or mean-sense error will have flatness implications. Serious errors in the inner loop will generally have second-order implications in the outer loop.



9000 POWER SUPPLIES

HIGH − V & DISPLAY

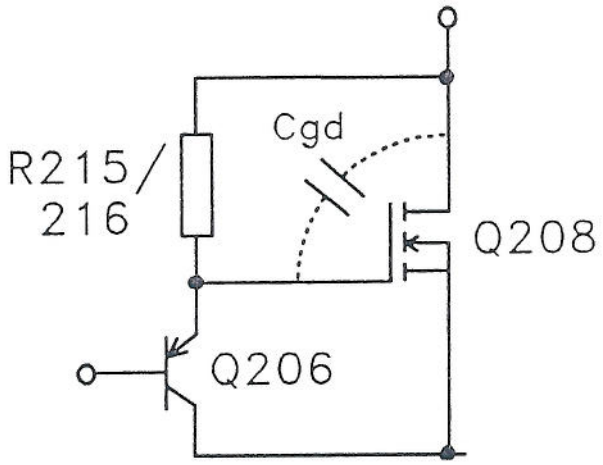
H1



VOLTAGE P.A. SIMPLIFIED

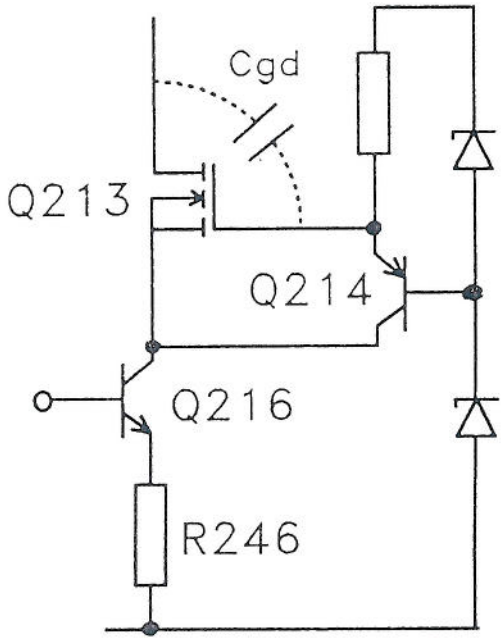
FIXING THE Cgd PROBLEMS

Q208/212



EFFECTIVE INPUT CAP VERY LOW DUE TO Q206(C)&(E) FOLLOWING BASE SIGNAL

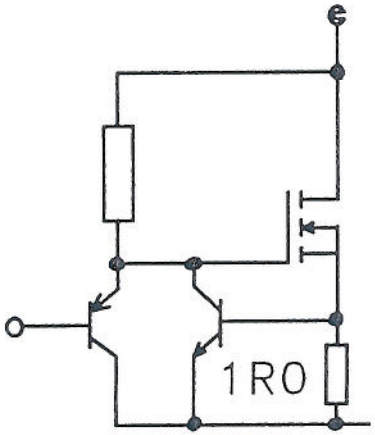
Q213



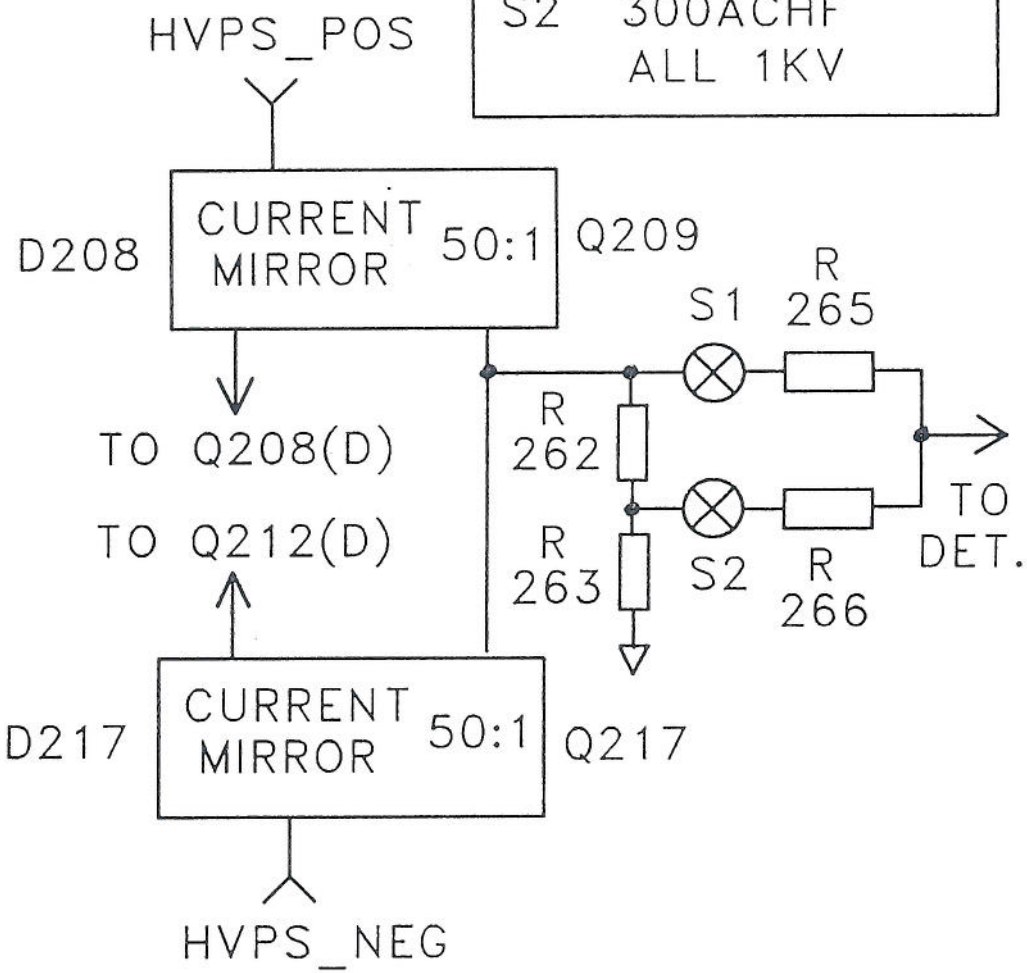
"LOST" CURRENT THRO' Cgd IS RETURNED TO Q216 BY Q214

VOLTAGE PA PROTECTION & OVERLOAD DETECTION

S1 ALL 30V/100V
S1+S2 300ACLF
300DC
S2 300ACHF
ALL 1KV



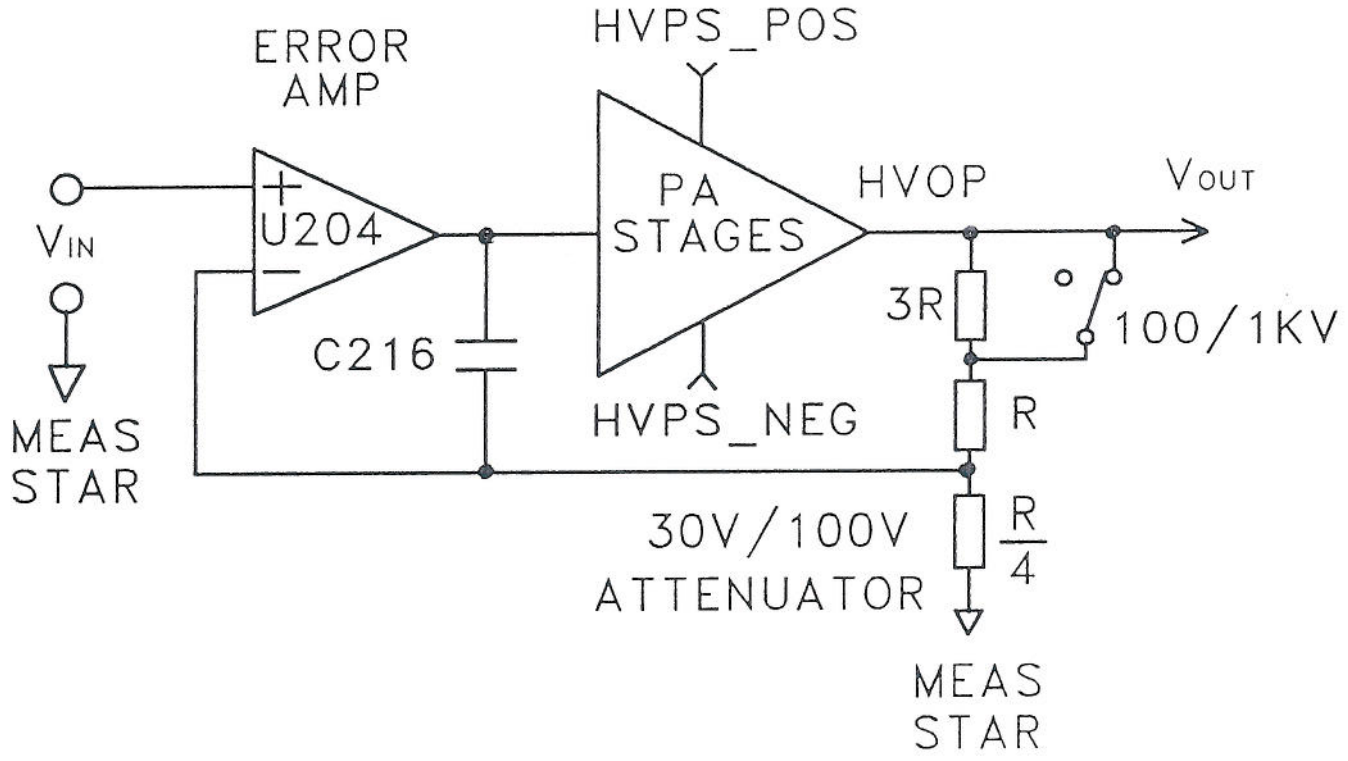
O/P STAGE
LOCAL I- LIM
=600mA



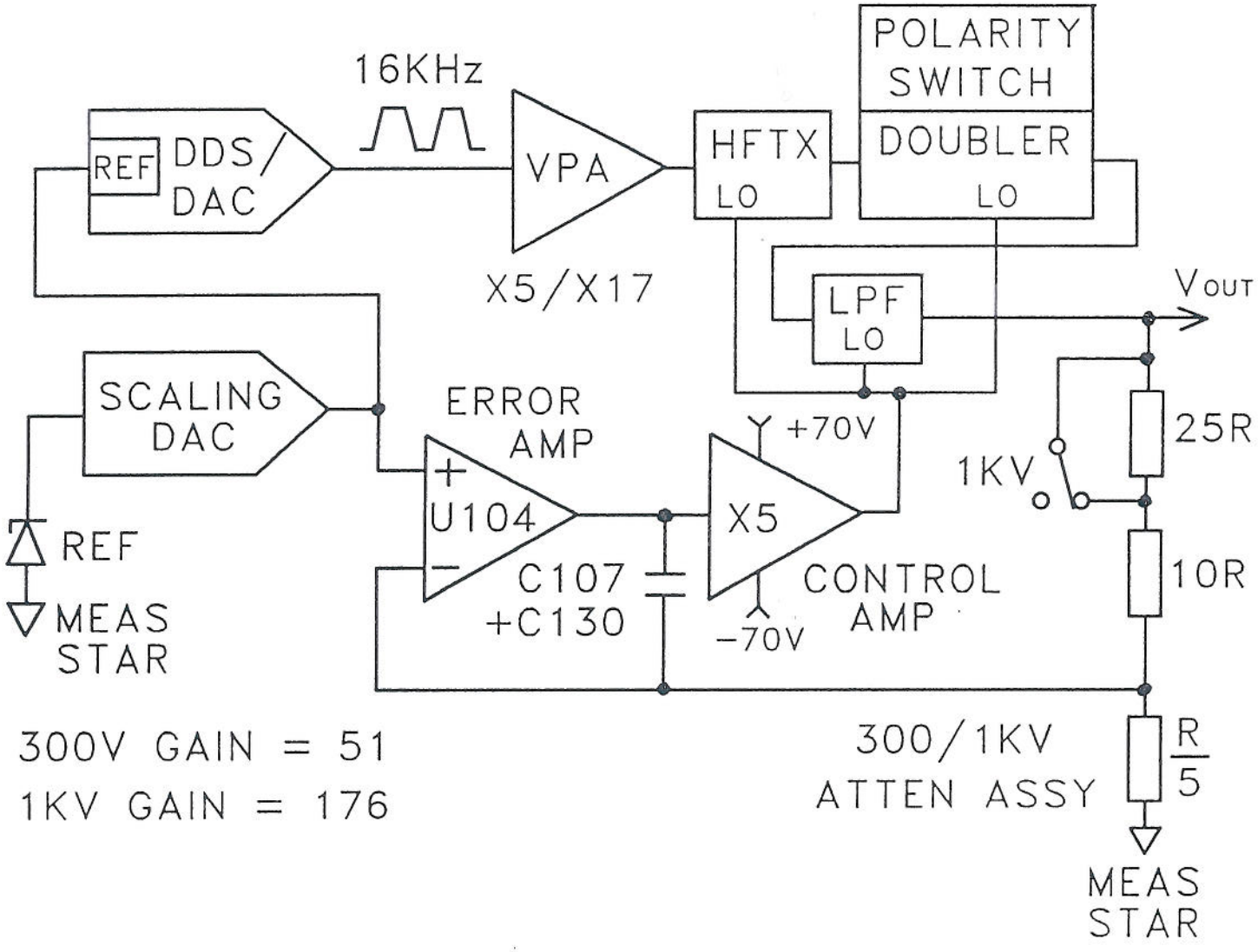
VOLTAGE PA – CLOSING THE LOOP

$$30/300V\ GAIN = \frac{R+R/4}{R/4} = 5 \qquad (\pm 70V)$$

$$100/1000V\ GAIN = \frac{R+3R+R/4}{R/4} = 17 \quad (\pm 200V)$$



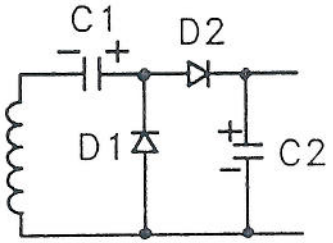
DC HIGH VOLTAGE



H6

HALF WAVE DIODE DOUBLER

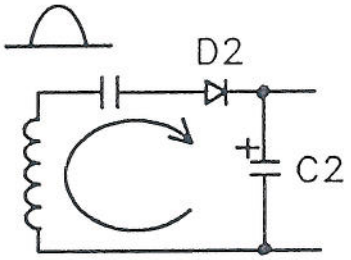
TWO USED ON OPPOSITE PHASES TO GIVE FULL WAVE DOUBLING.



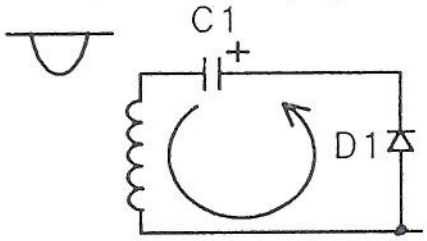
ON (+)VE 1/2 CYCLES C2 IS CHARGED VIA D2 (A)

ON (−)VE 1/2 CYCLES C1 IS CHARGED VIA D1 (B)

(A)

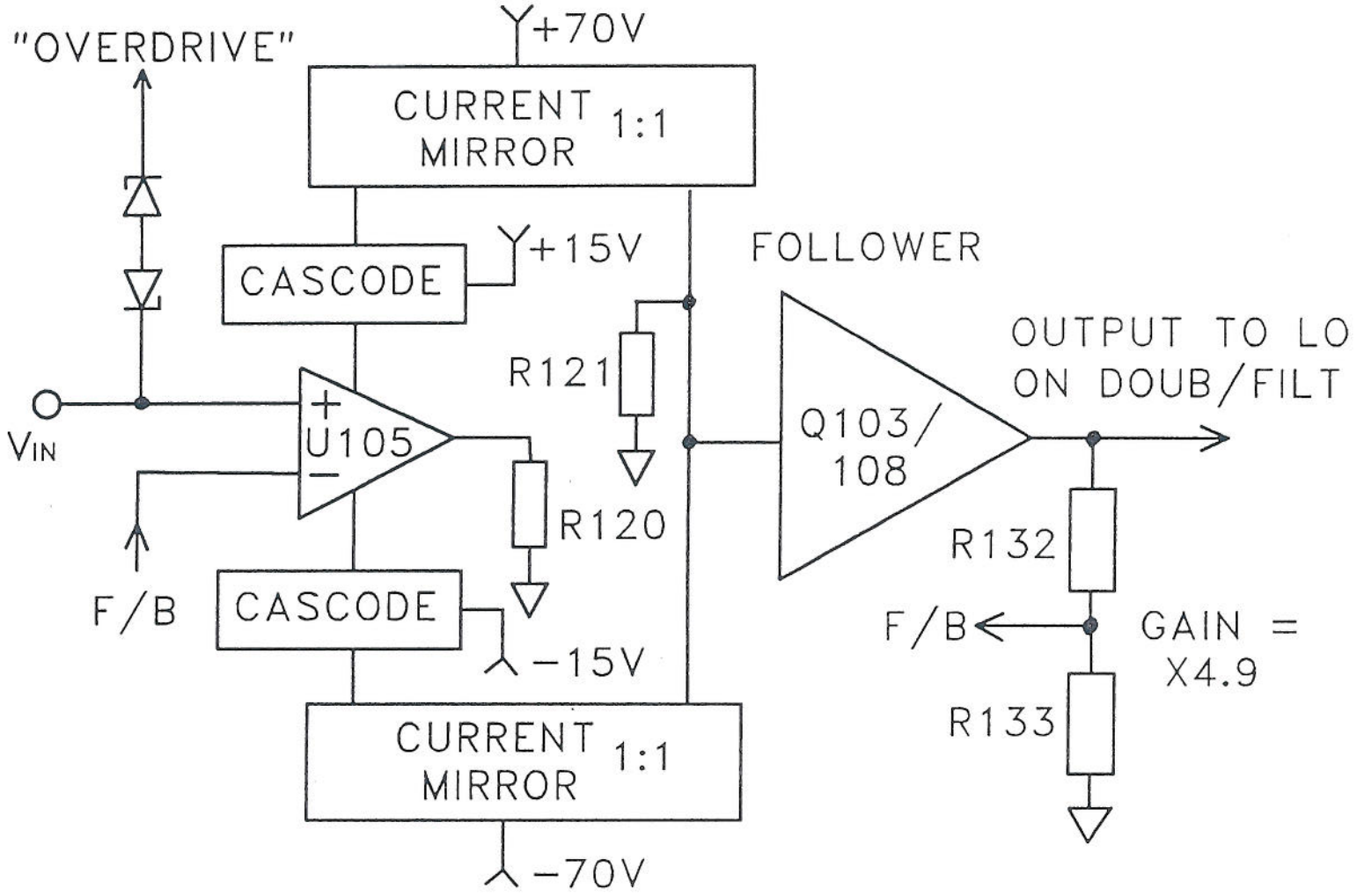


(B)



VOLTAGE DEVELOPED ACROSS C1 ON (−)VE 1/2 CYCLE ADDS TO AC SOURCE ON NEXT (+)VE 1/2 CYCLE

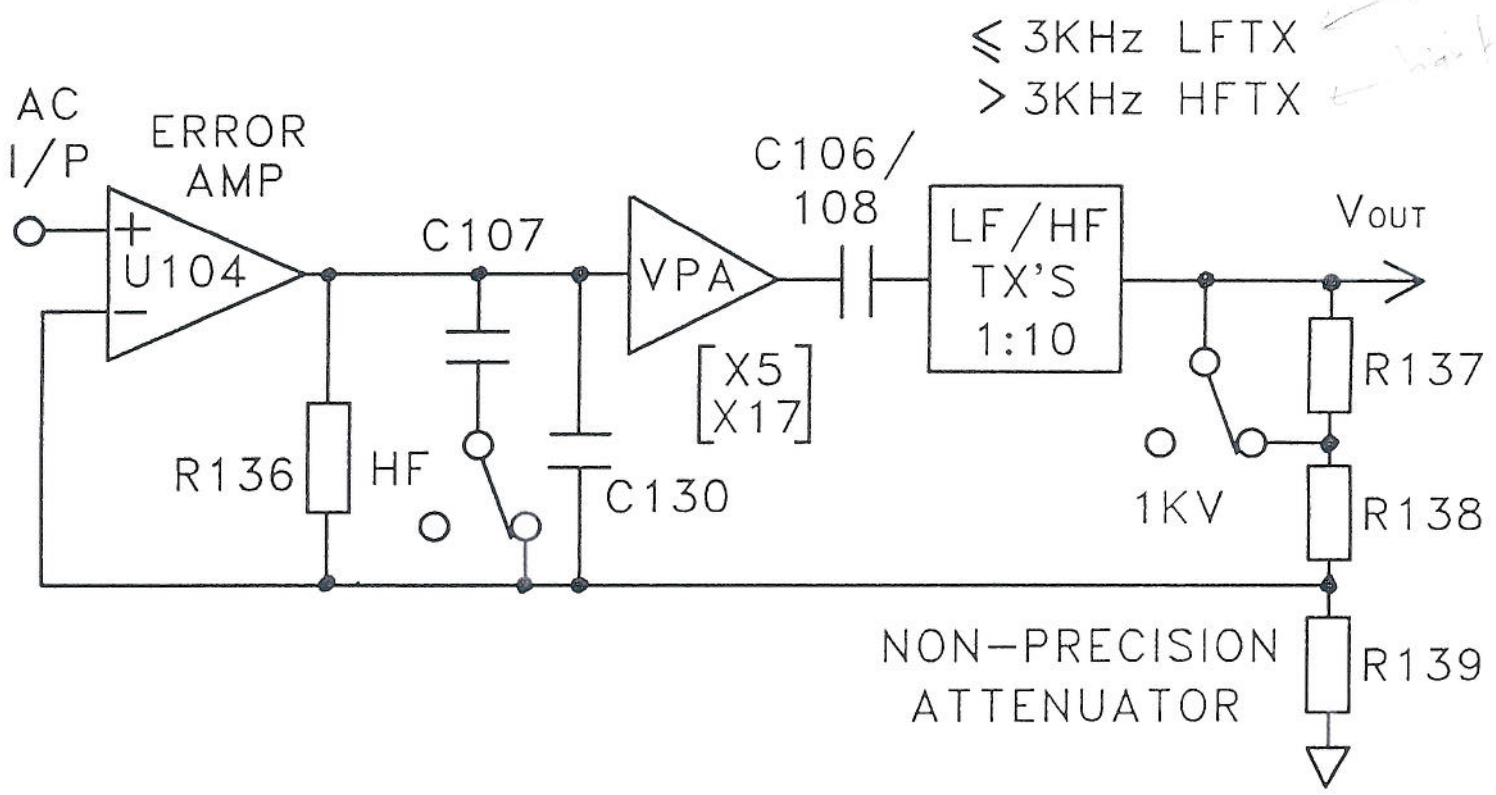
DC HV CONTROL AMP



H8

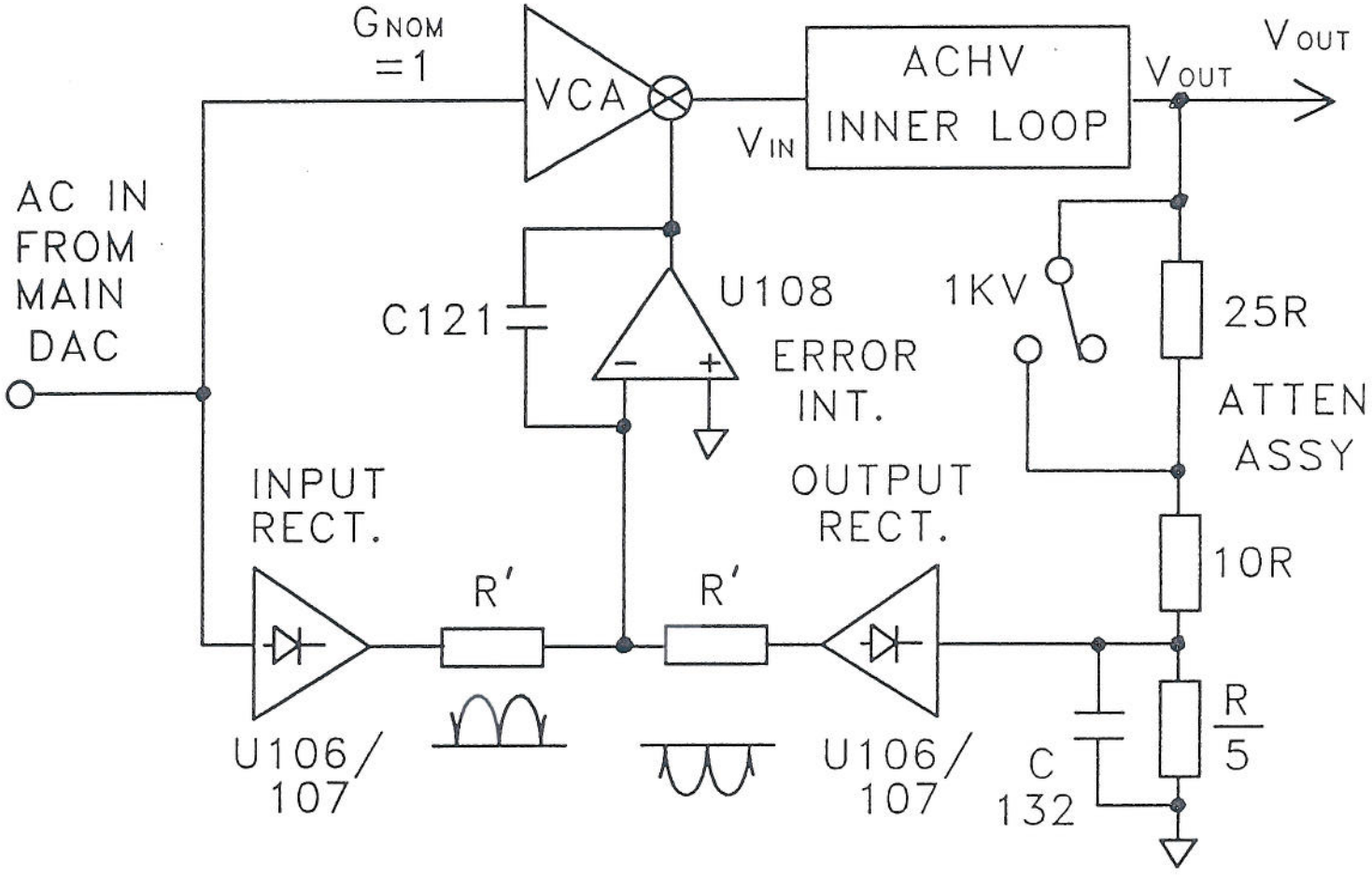
ACHV INNER LOOP

(1) PRODUCES BASIC OUTPUT POWER FOR HVAC.
(2) REDUCES DISTORTION @ LOW FREQS DUE TO TX SATURATION BY VIRTUE OF LOOP GAIN.
(3) REDUCES FLATNESS ERROR OF TX'S.



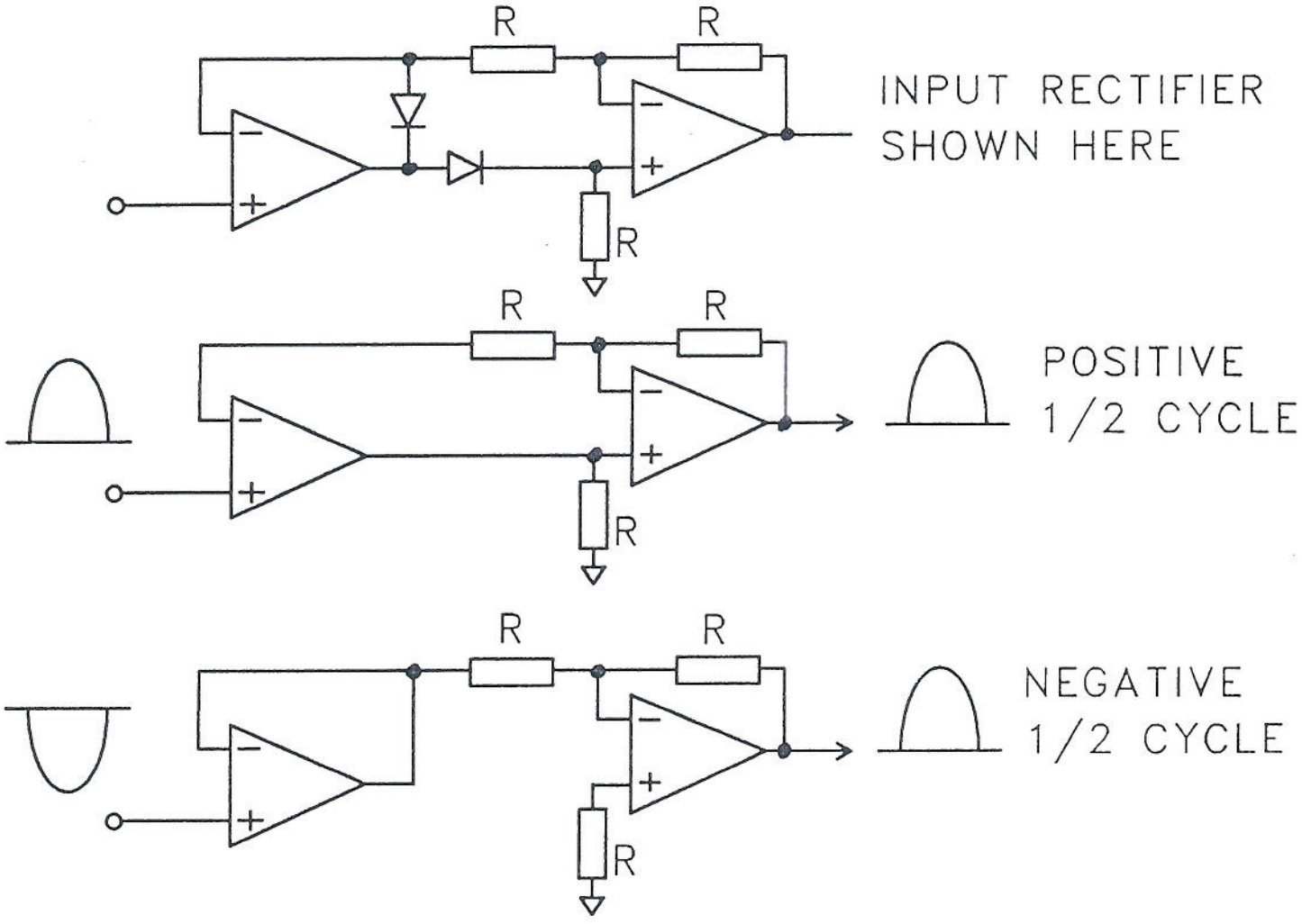
ACHV OUTER LOOP

PROVIDES FINE CONTROL OF HV GAIN TO PPM LEVELS (BY USE OF THE DCHV PRECISION ATTENUATOR IN A MEAN SENSING LOOP)



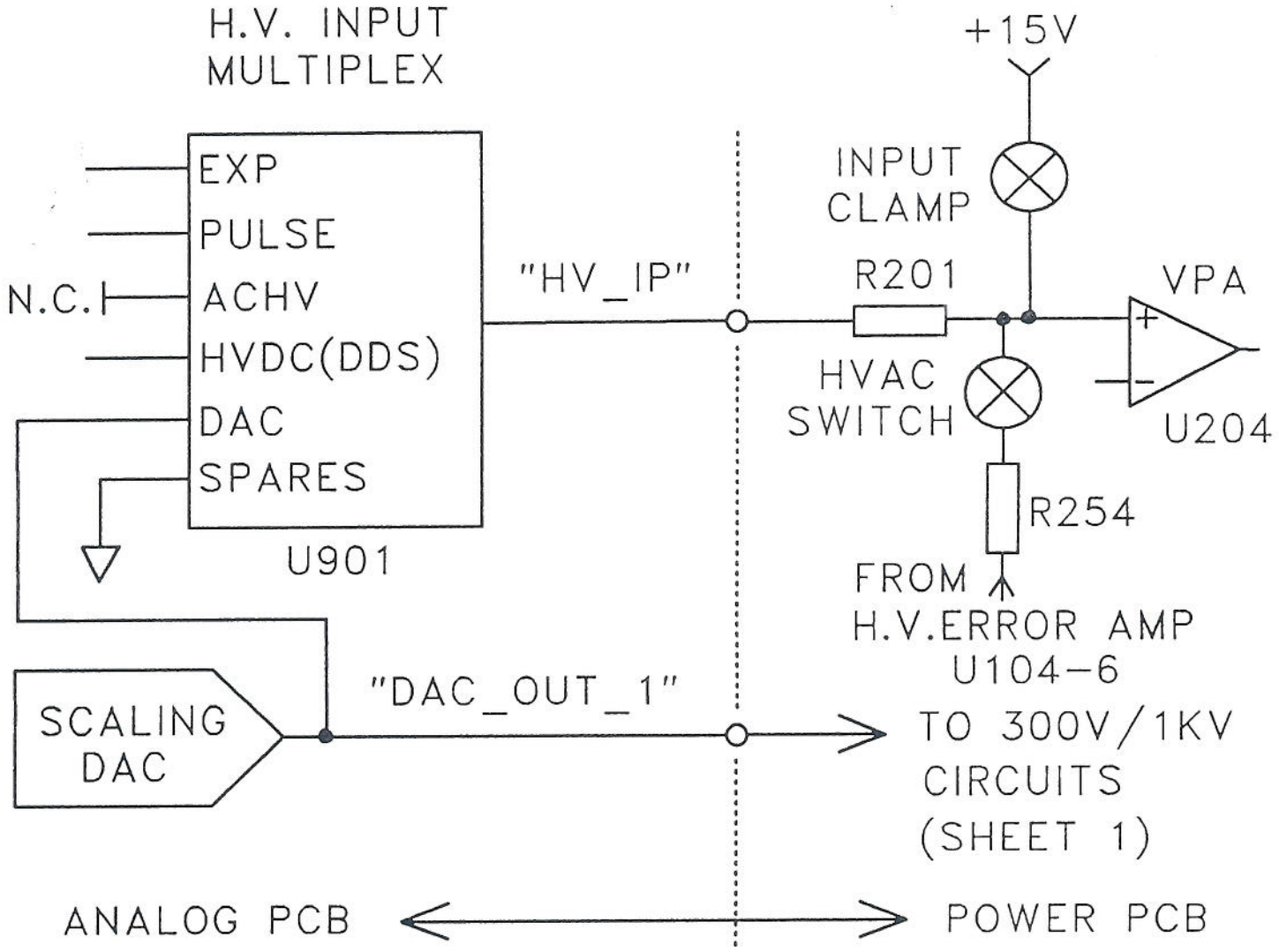
H10

PRECISION RECTIFIERS OF MEAN-SENSE HV LOOP



H11

HIGH VOLTAGE – INPUT ROUTING



H12

HIGH VOLTAGE – HARDWARE OVERVIEW

RANGE	GAIN	HVPS	OUTPUT CONTROL
30VDC	+5	±70V	NONE:DIRECT FROM P/A
300VDC	+51	±70V	DCHV CONTROL LOOP
1KVDC	+176	±200V	DCHV CONTROL LOOP
30VAC	+5	±70V	NONE:DIRECT FROM P/A
100VAC	+17	±200V	NONE:DIRECT FROM P/A
300VAC	+51	±70V	ACHV MEAN SENSE LOOP
1KVAC	+176	±200V	ACHV MEAN SENSE LOOP

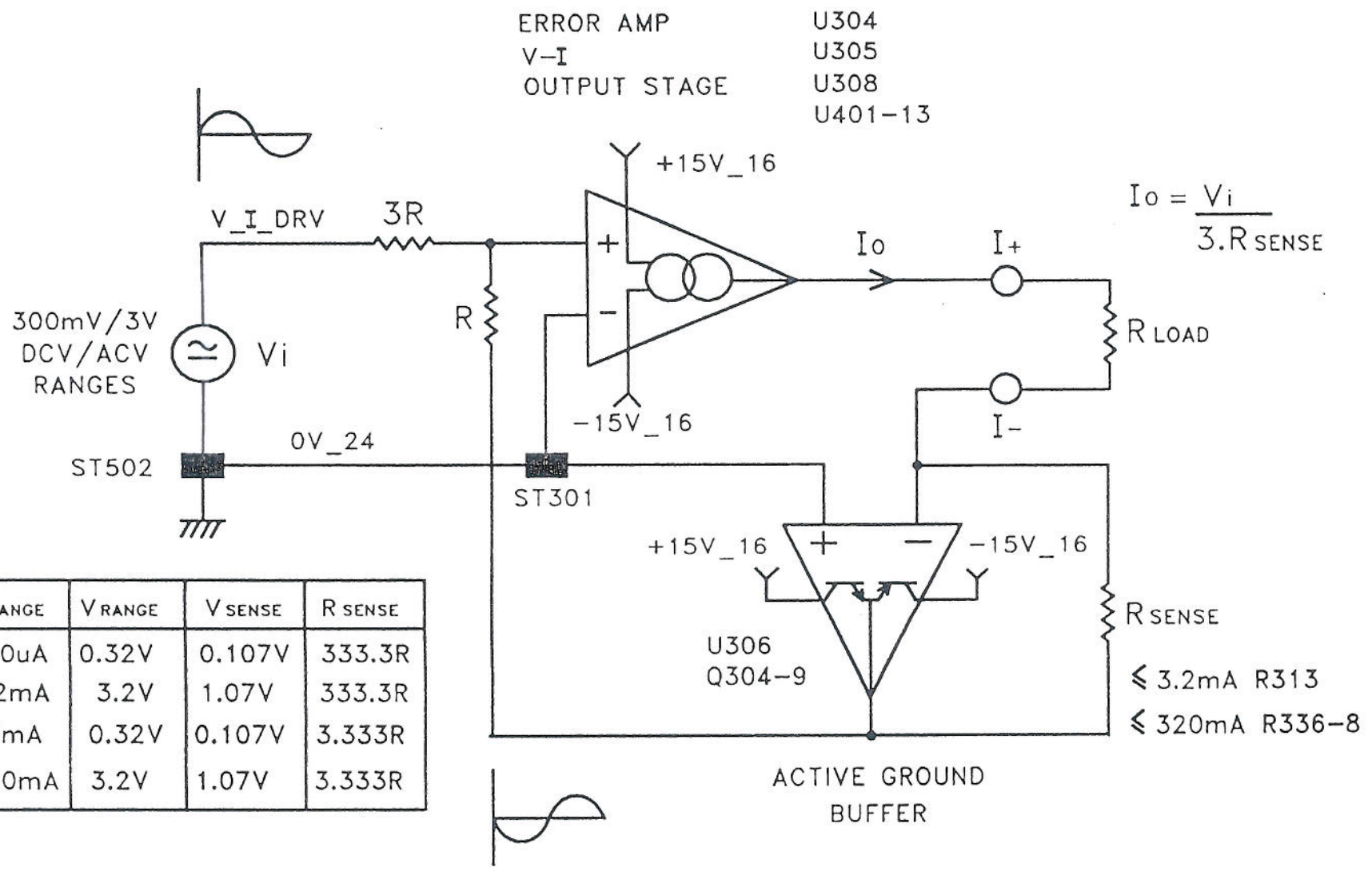
ERROR FLAGS

PA OVERLOAD – ACTIVE FOR ALL RANGES

PS OVERLOAD – ACTIVE ONLY WHEN HVPS = ±200V

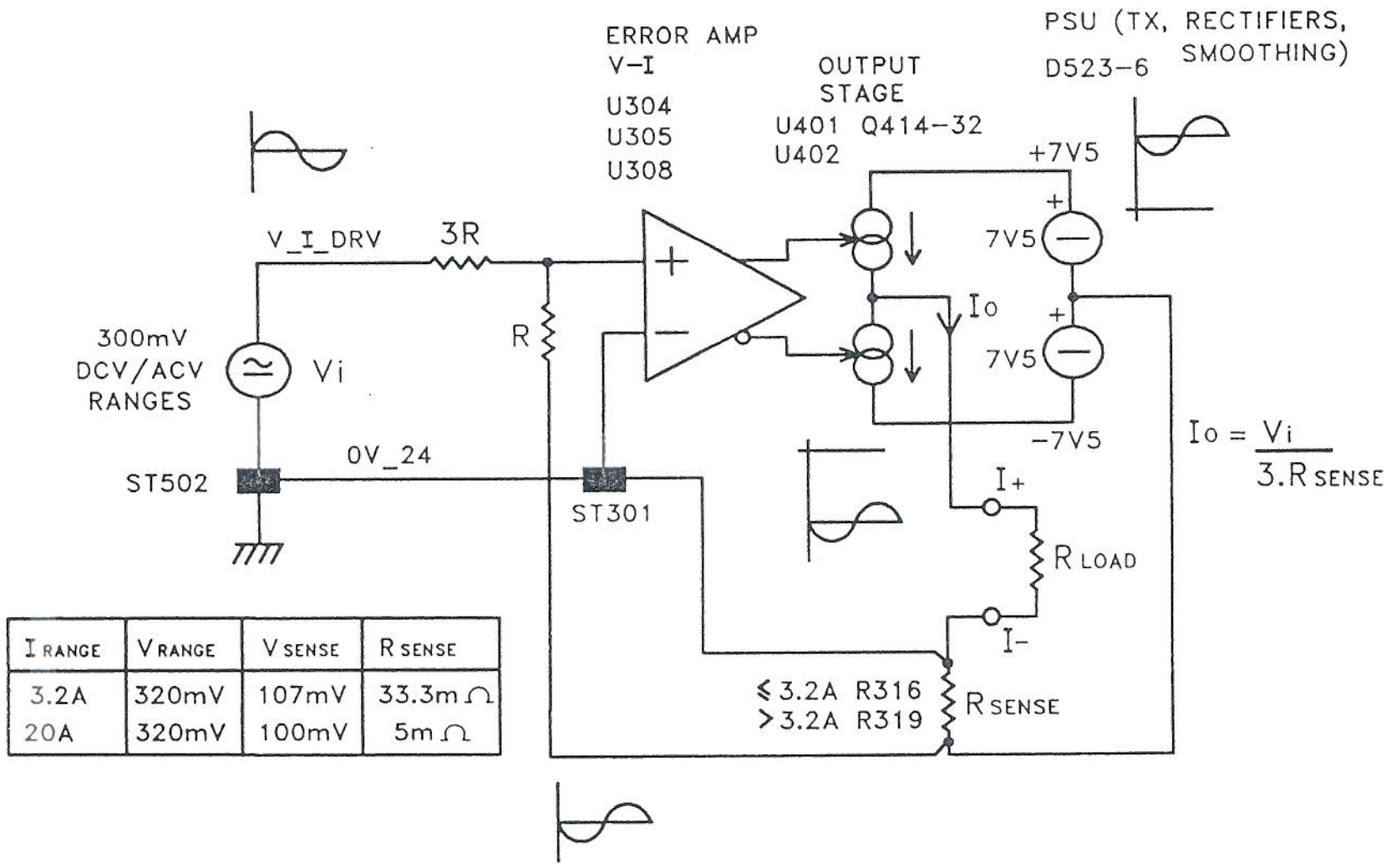
EITHER OR BOTH CAUSE A SEQUENCED SHUTDOWN TO NEUTRAL STATE.

LOW CURRENT ARCHITECTURE (⩽ 320mA)



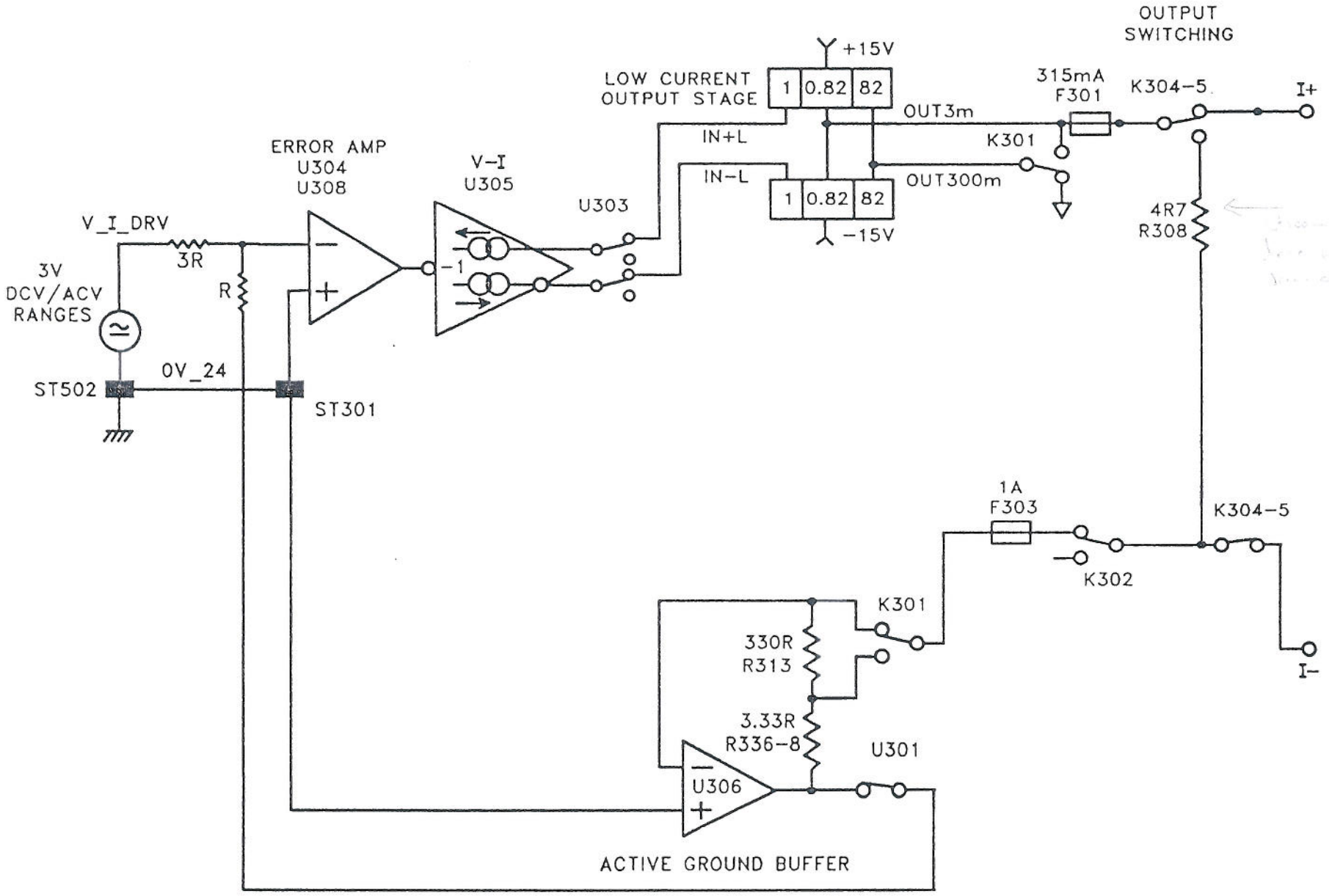
I RANGE	V RANGE	V SENSE	R SENSE
320uA	0.32V	0.107V	333.3R
3.2mA	3.2V	1.07V	333.3R
32mA	0.32V	0.107V	3.333R
320mA	3.2V	1.07V	3.333R

HIGH CURRENT ARCHITECTURE (>320mA)



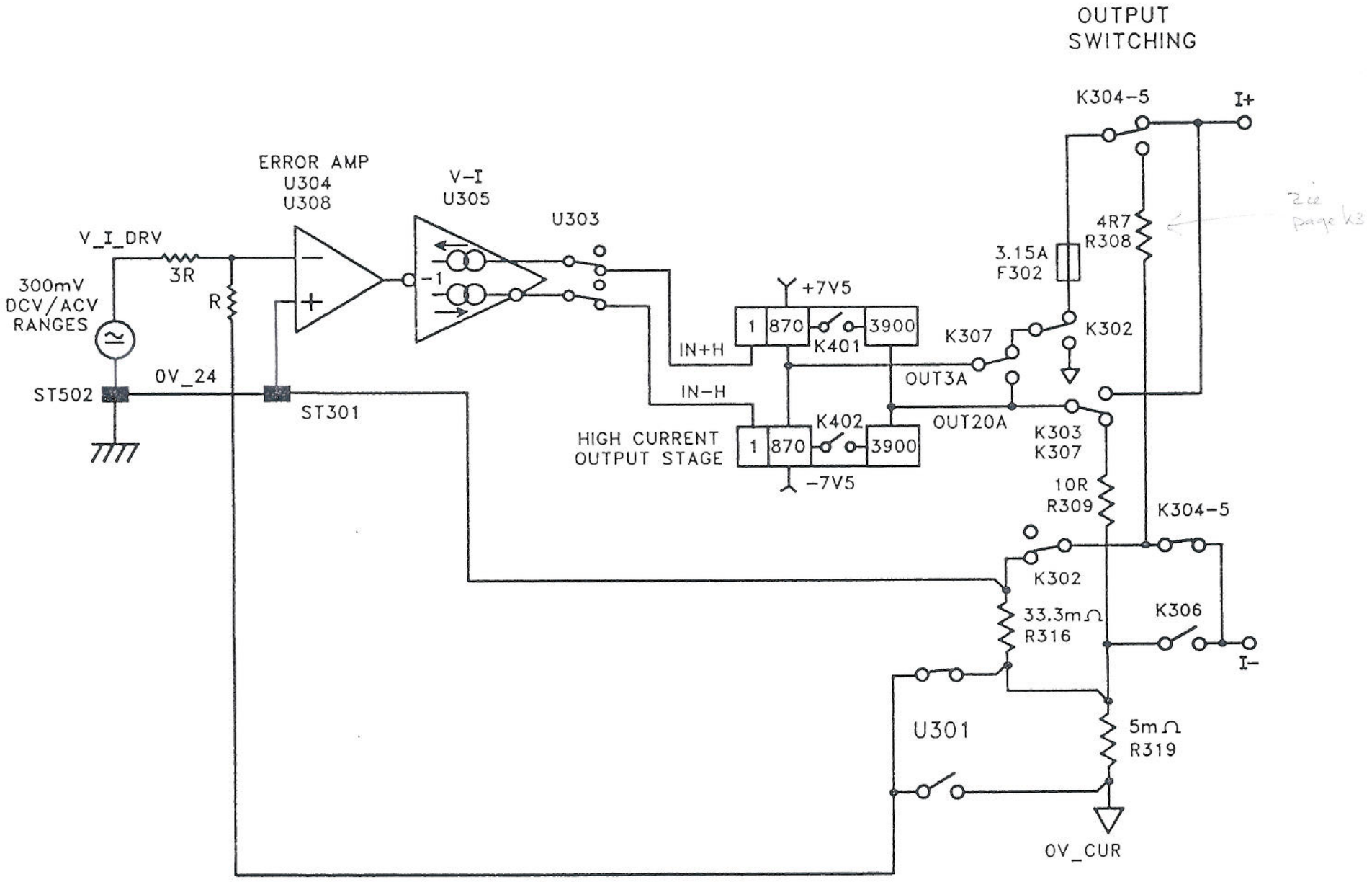
I RANGE	V RANGE	V SENSE	R SENSE
3.2A	320mV	107mV	33.3mΩ
20A	320mV	100mV	5mΩ

LOW CURRENT ARCHITECTURE AND SWITCHING – 3mA ON



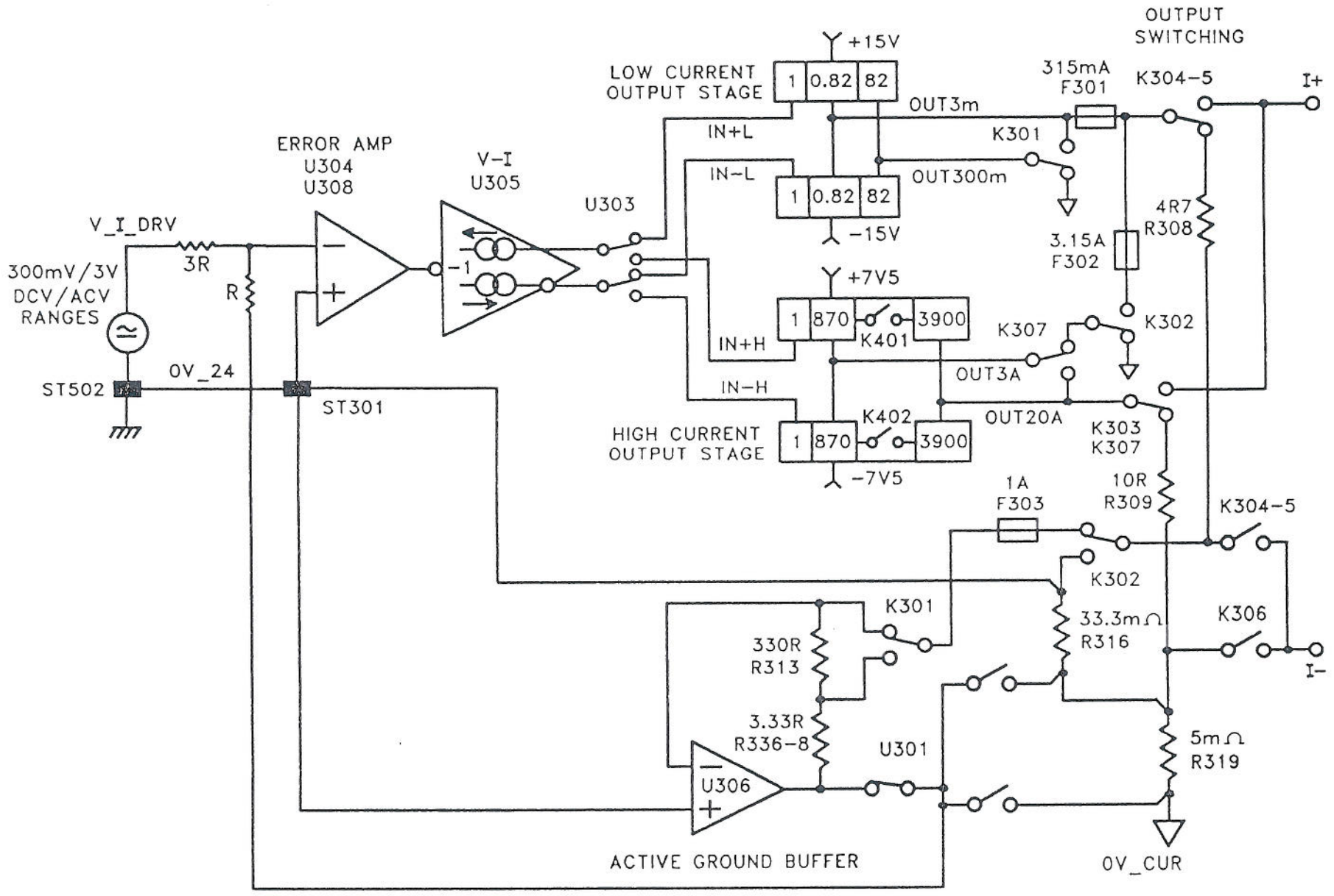
K3

HIGH CURRENT ARCHITECTURE AND SWITCHING – 3A OUTPUT ON

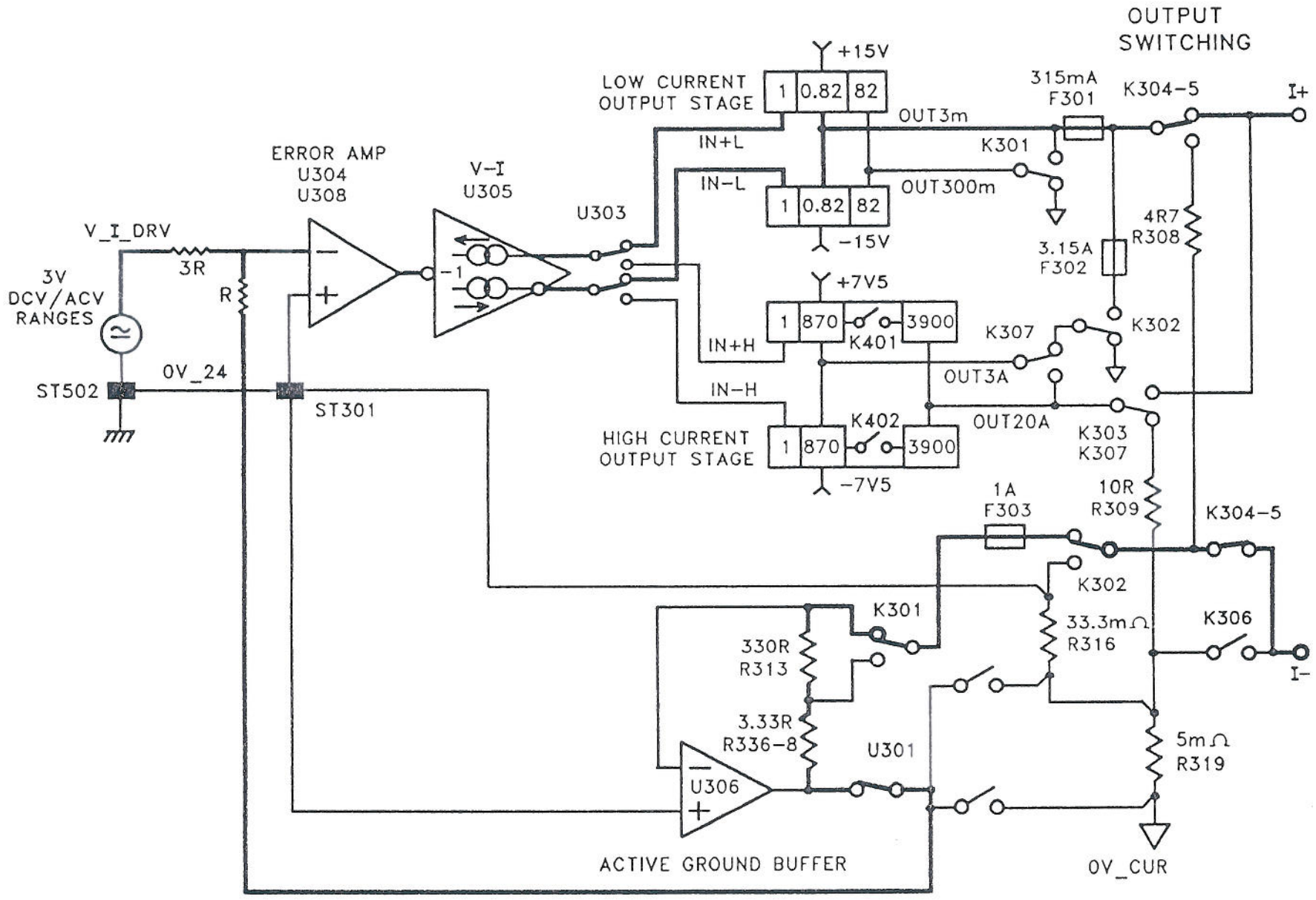


K4

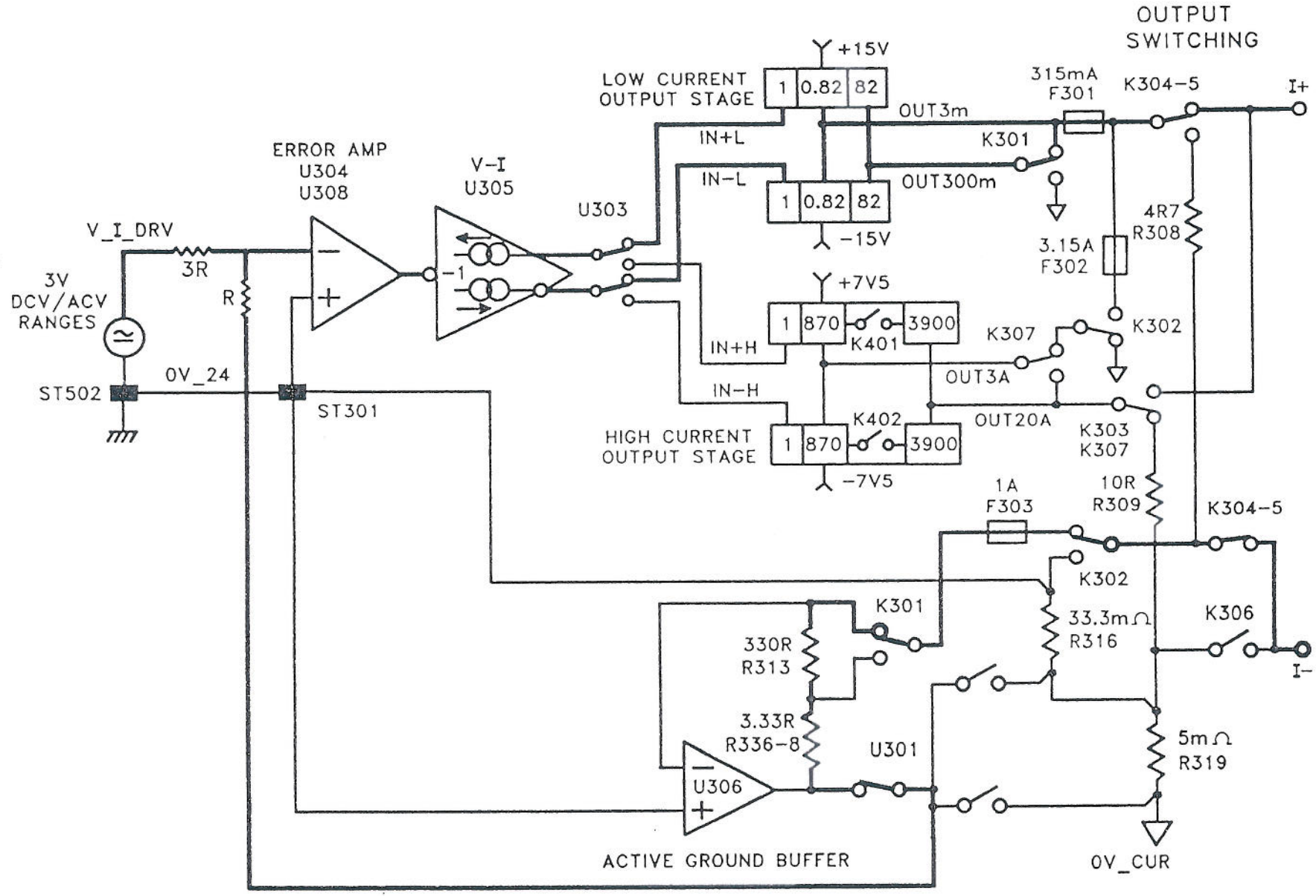
SHARED ARCHITECTURE AND SWITCHING – NEUTRAL STATE



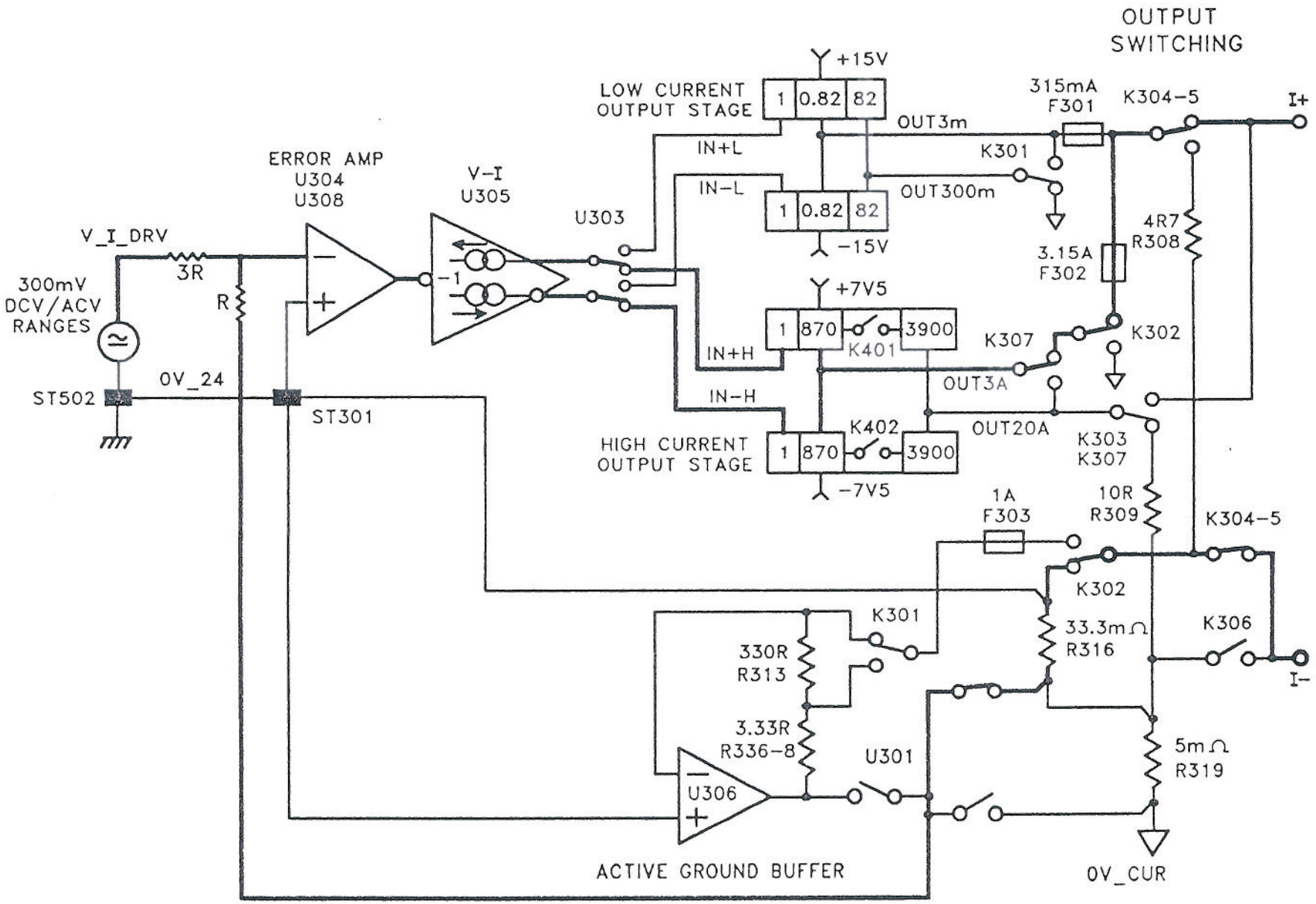
SHARED ARCHITECTURE AND SWITCHING – 3mA OUTPUT ON



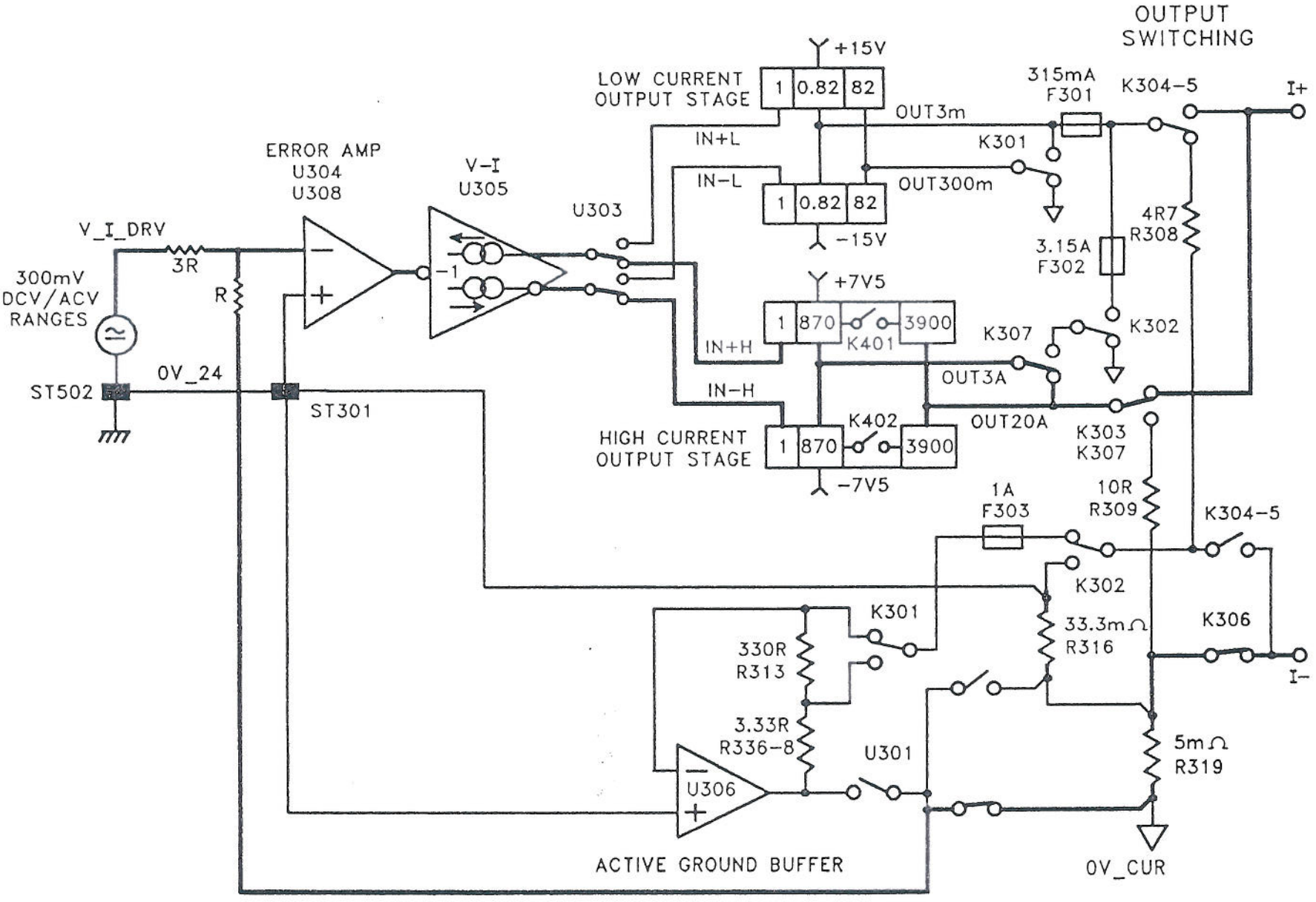
SHARED ARCHITECTURE AND SWITCHING – 300mA OUTPUT ON



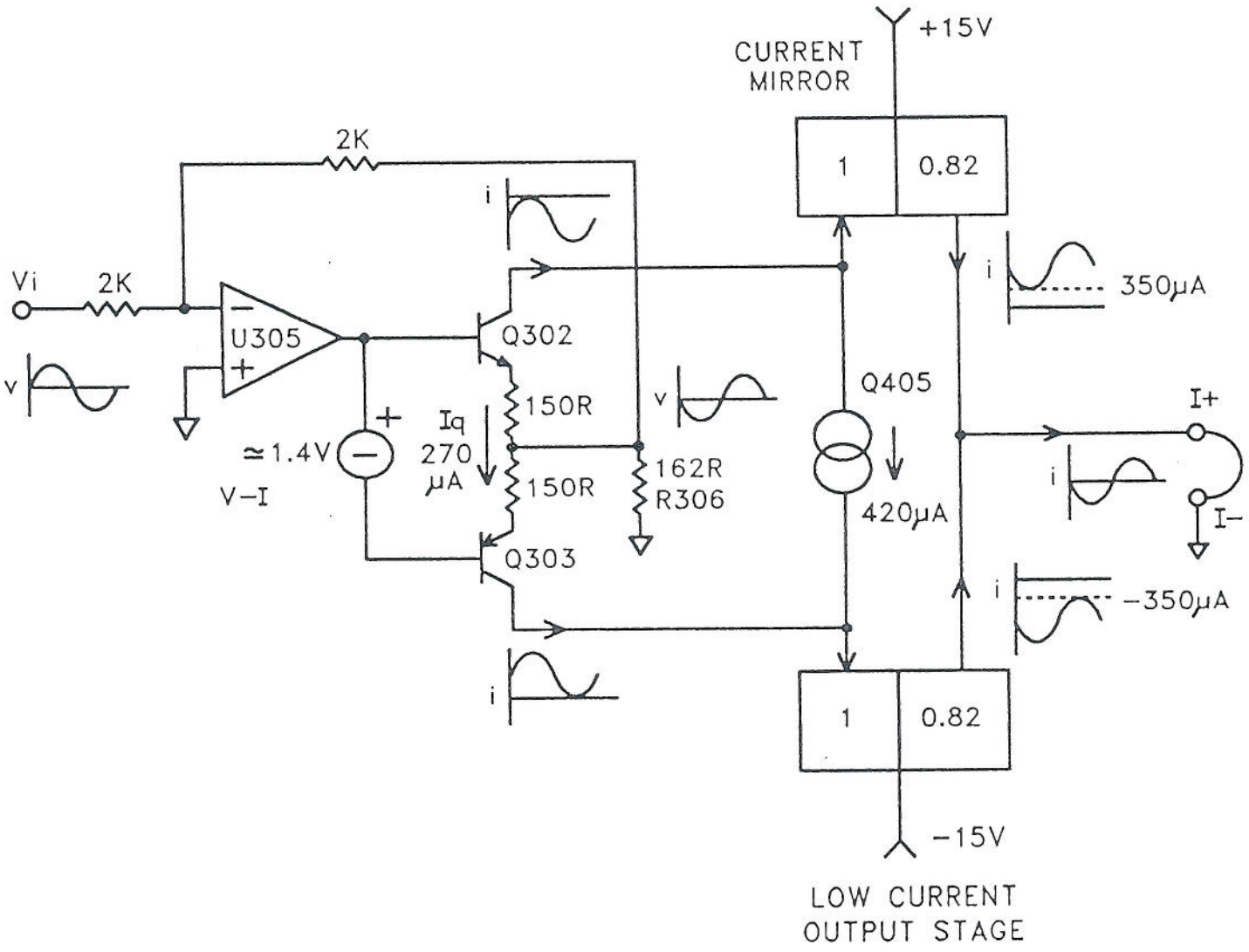
SHARED ARCHITECTURE AND SWITCHING – 3A OUTPUT ON



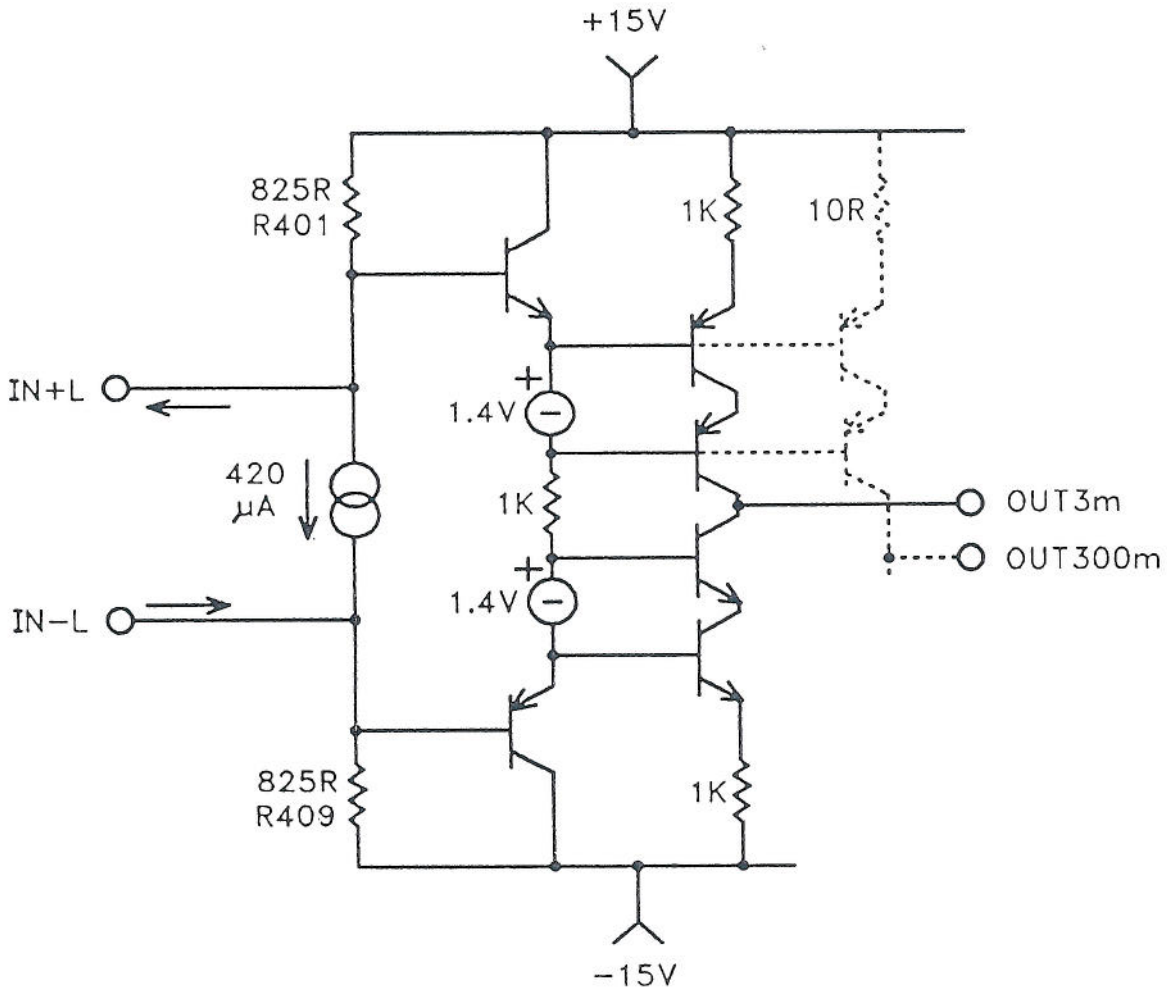
SHARED ARCHITECTURE AND SWITCHING – 20A OUTPUT ON



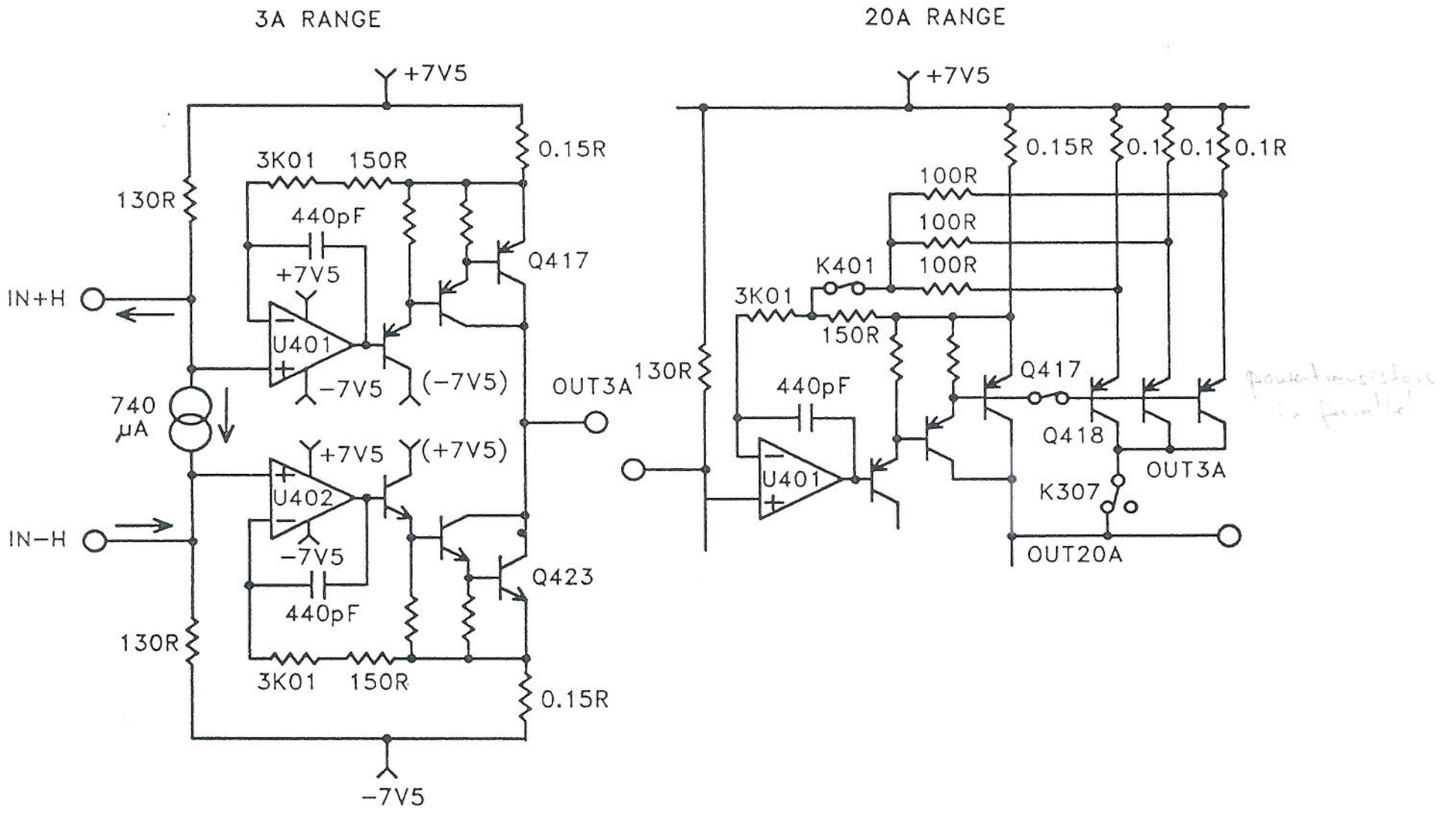
CLASS Aa OUTPUT STAGE – 3mA RANGE



LOW CURRENT OUTPUT STAGE ⩽0.32A

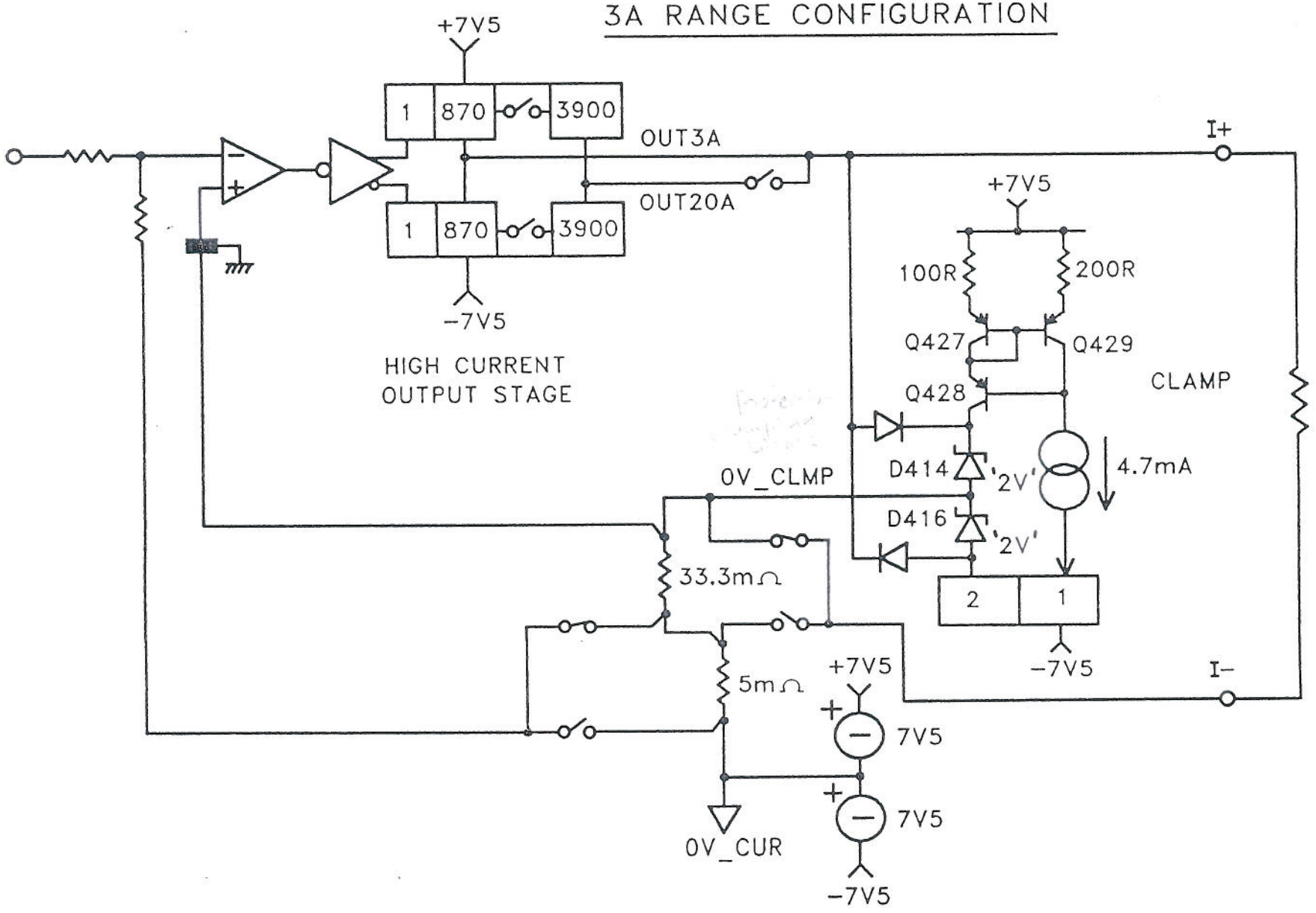


HIGH CURRENT OUTPUT STAGE >0.32A



HIGH CURRENT CLAMPING – 3A & 20A RANGES

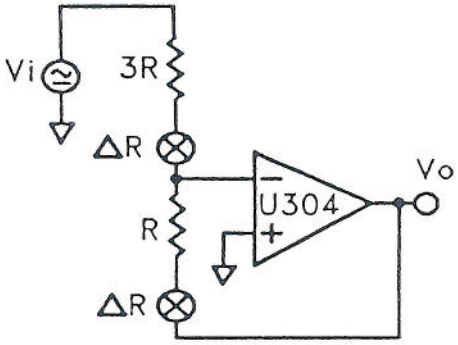
3A RANGE CONFIGURATION



K13

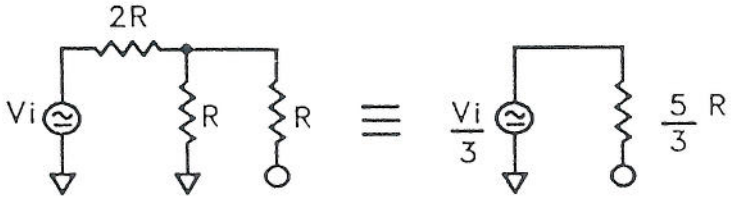
GAIN DEFINING NETWORK AND INPUT CLAMP

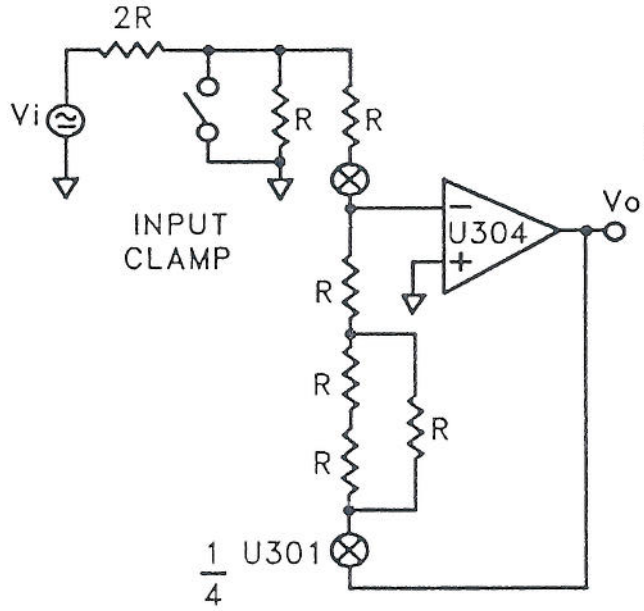
SIMPLE NETWORK



$$\frac{Vo}{Vi} = \frac{R + \Delta R}{3R + \Delta R} = \frac{1}{3}\left(1 - \frac{2}{3}\cdot\frac{\Delta R}{R}\right)$$

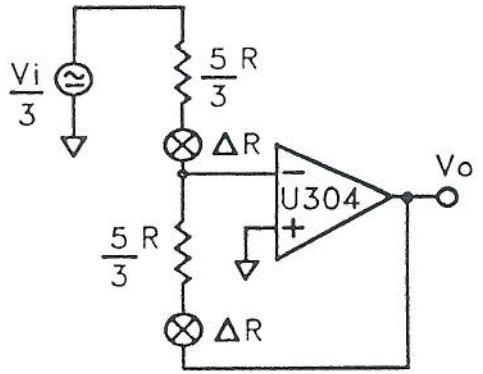
ACTUAL NETWORK





R301
(8X3K3)

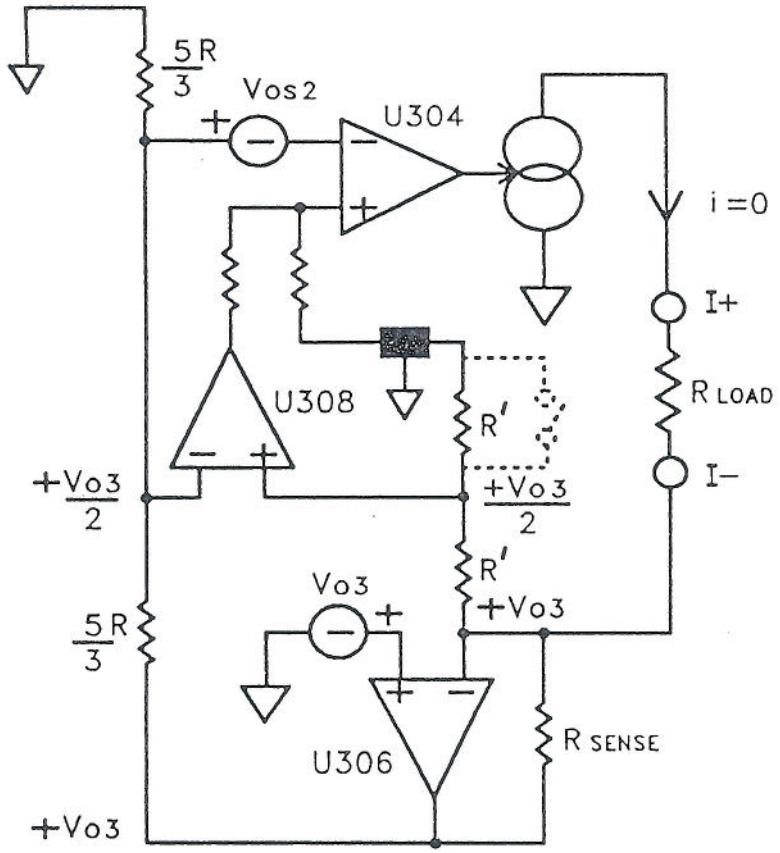
≡



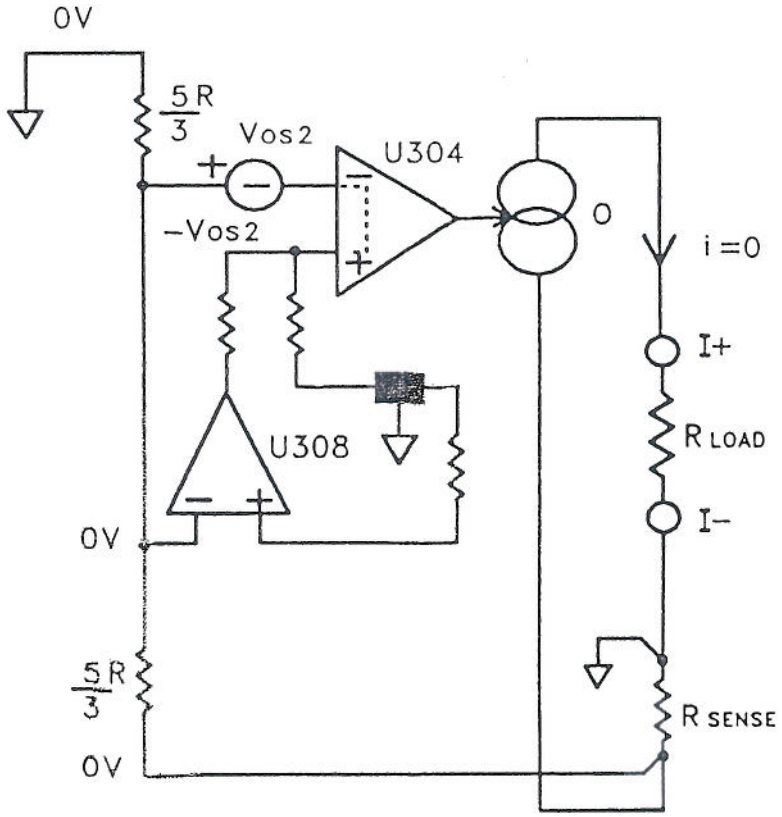
$$\frac{Vo}{Vi} = \frac{1}{3}\cdot\frac{\frac{5}{3}R + \Delta R}{\frac{5}{3}R + \Delta R} = \frac{1}{3}$$

DC STABILISATION LOOP

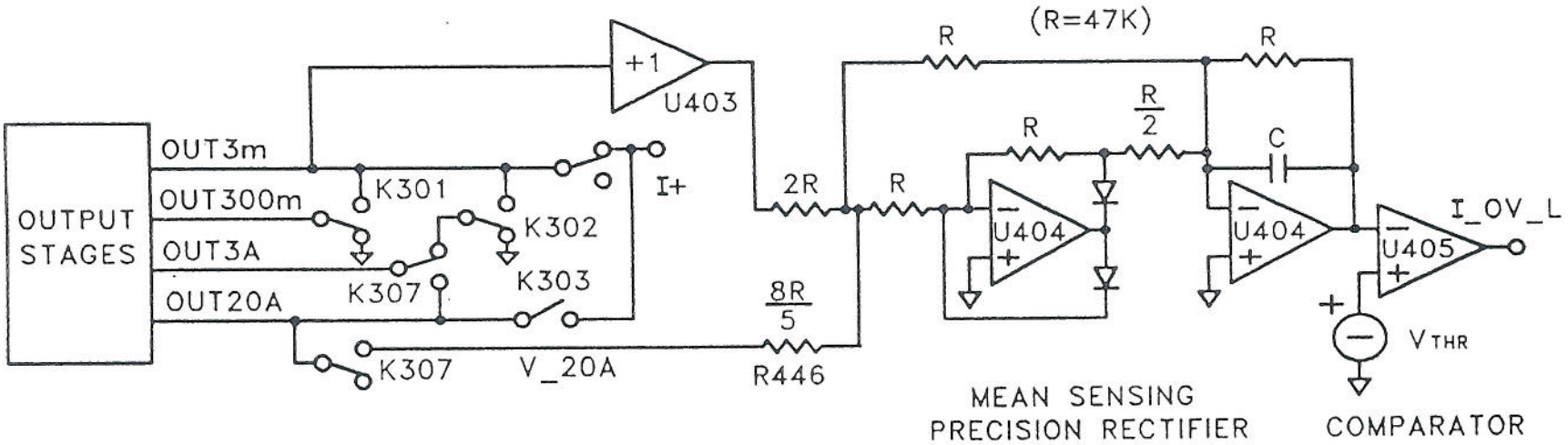
LOW CURRENT $\leqslant$ 0.32A



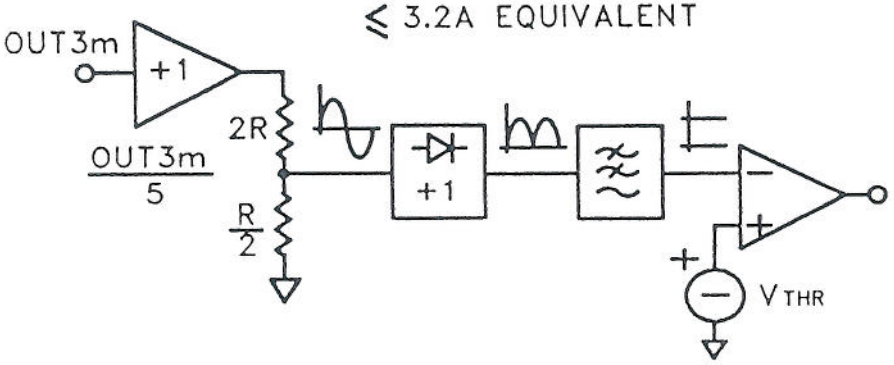
HIGH CURRENT $>$ 0.32A



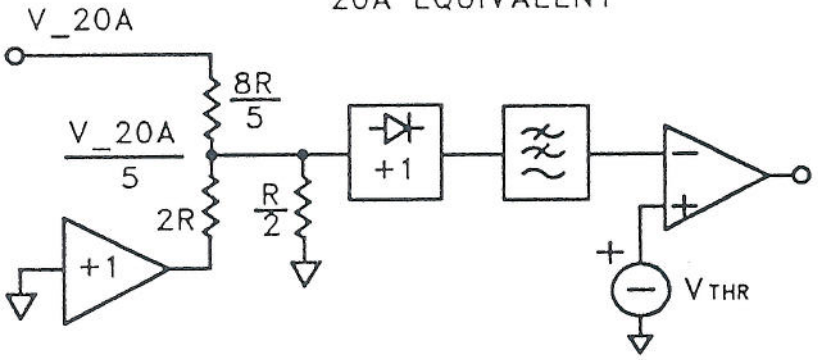
OVER VOLTAGE DETECTOR



≤ 3.2A EQUIVALENT

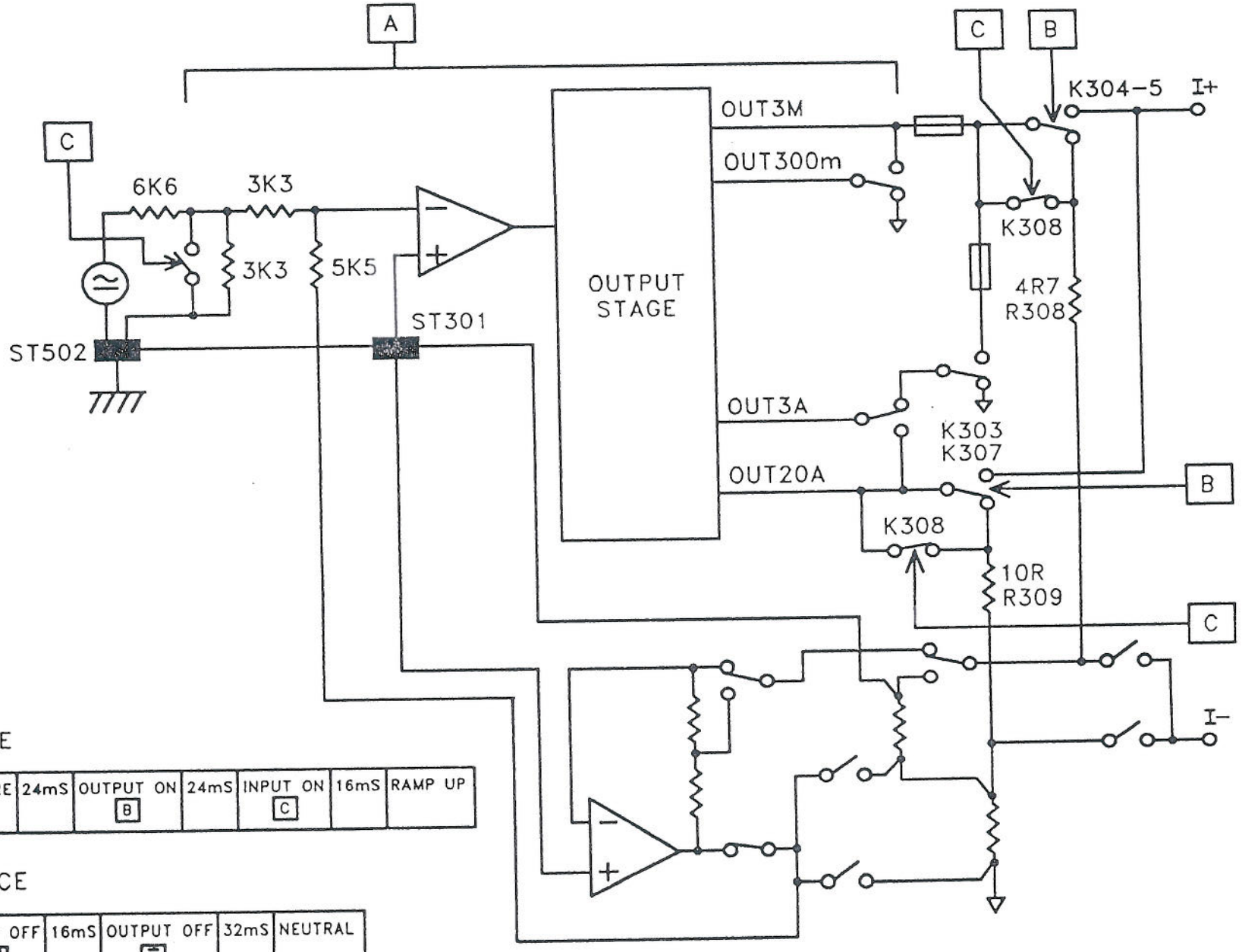


20A EQUIVALENT



	V_{DET}		V_{THR}
	DC (V_{DC})	AC (V_{RMS})	
0.32A R	5.47V_{DC}	6.07V_{RMS}	1.094
3.2A R	(2.33−0.047 Io)	(2.59−0.047 Io)	0.465
20A R	(2.32−0.015 Io)	(2.58−0.015 Io)	0.465
Tol	±10%	+14% −10%	

STATE SEQUENCING



ON SEQUENCE

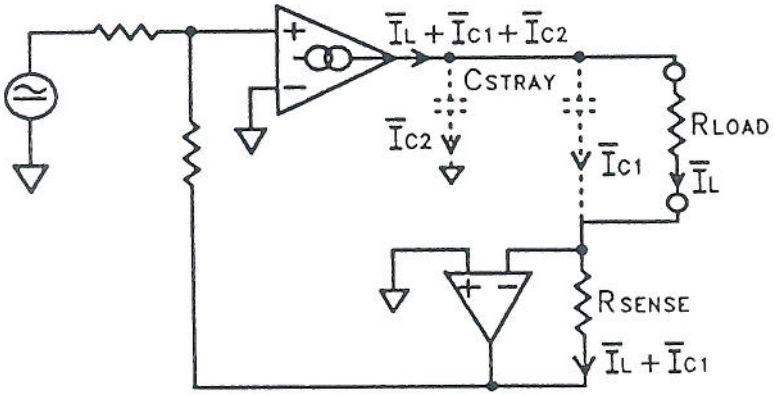
NEUTRAL	CONFIGURE [A]	24mS	OUTPUT ON [B]	24mS	INPUT ON [C]	16mS	RAMP UP

OFF SEQUENCE

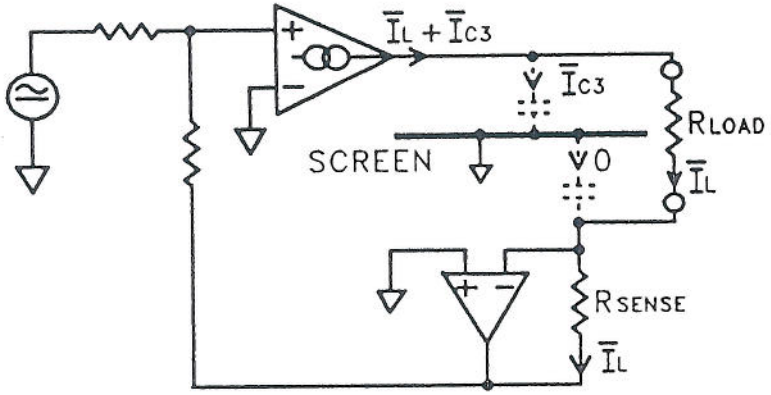
RAMP DOWN	INPUT OFF [C]	16mS	OUTPUT OFF [B]	32mS	NEUTRAL

GUARDING

WITHOUT GUARDING



WITH GUARDING



CIRCUIT DESCRIPTION - POWER PCB

CURRENT SECTION

- **Overall Loop (401096 Sht 3):**

  Precision current is provided by a V-I converter (transconductance amp) driven by the 300mV and the 3V voltage ranges. The output current is sensed via I-, on its return. As the I- point is held at ground potential a positive output current produces a negative voltage on the opposite end of the sense resistor (R316, 319, 313, 336-8). This sense voltage is compared to the input voltage via a feed back network (R301) at the error amp virtual earth input (U304). The error signal produced by the input amp is turned into a differential current by the small signal V-I converter (U305). This current is then amplified by the appropriate output stage.

  At high currents (>0.32A) the I- end of the sense resistor is held at ground potential by both earthing the sense and by floating the output stage and its power supply. At low currents (<0.32A) the I- current is fed into the virtual earth of a ground referenced inverting amp (U306) (transresistance amp).

- **Input Network and Error Amp (401096Sht3):**

  The input network (R301) provides attenuation of the input signal (x $^1/_3$), analogue switch (U301) impedance matching and a convenient point for the input clamp FET (Q301). With analogue switches, from the same chip, both in the input and the feedback networks, switch ON resistance TC is bucked out.

  C302/3 provides the dominant pole in the loop. In open loop mode (J803 pin 2 linked to 3) feedback sense is disabled and local feedback is provided around the error amp by R327 via U302.

  DC stabilization is provided by a chopper amp (U308) configured as the low frequency part of a compound amp (crossover approx 1 Hz). At high currents (>0.32A) the chopper amp compares the virtual earth (U304 pin 2) of the loop with reference ground. At low currents (<0.32A) it compares the virtual earth to half the offset voltage of the active ground butter (U306). An analogue switch (U302 pins 9-11) selects the appropriate reference voltage for the DC amp. The virtual earth is sensitve to leakage current so low bias current op amps have been used and pcb guarding employed.

- **Small Signal V-I (401096Sht3):**

  The converter (U305) is formed from an inverting amp, with switched gain (U302) and a class AB output stage. The output voltage is developed across the load resistor (R306), consequently the differential output current, via the collectors of transistors (Q302, 303), is proportional to the input voltage. Diode clamps are provided in the feedback (D308-11) to limit the output current.

- **Low Current Output Stage (401096Sht4):**

  The output stage consists of a complementary pair of dual output current mirrors (gains of 0.82 and 82) and a bias current source (Q405). The 3mA range is fed from the low gain output with the high gain output grounded. The 300mA range is fed from both outputs is parallel.

  The bias current source maintains a minimum current flow in both both current mirrors when either of the control currents falls to zero. The outputs of the current mirrors are cascoded to increase output impedance. A series RC network (R408 + C404) provides a local HF output current path.

- **High Current Output Stage (401096Sht4) and ±7V5 PSU (401096Sht5):**

  The high current output stage also consists of a complementary dual output current mirror configuration (gains of 867and 4767) with a bias current source (Q414). The 3A range topology uses one output transistor per mirror whereas the 20A range uses four output transistors per mirror, with the four emitter voltages averaged via R414, 421, 423 and R425. Two relays (K401, K402) isolate the six unused output transistors and their associated feedback signals when in the 3A range configuration.

  The ±7V5 lines are conventional unregulated supplies consisting of a transformer secondary, a bridge rectifier and a pair of reservoir caps.

  A bipolar, load bypassing, clamp is formed with two zeners (D414, 416) and two diodes (D413, 415). The two zeners are biased up with equal currents which are derived from a current source (Q433) and two current mirrors (Q427 - 432). In the 3A range configuration the clamp simply provides a parallel path to the load. In the 20A range the clamp current is injected via the top end of the 33mR shunt (R316) not via I-. This forces an output current reduction when the clamp cuts in.

- **Output Switching (401096Sht3):**

  Relays route the appropriate output to either internal loads (4R7/R308 - neutral and self test of 3mA/300mA/3A ranges, 10R/R309 - neutral and self test of 20A) the I+ terminal or the D type guarded current output. Relays route the return current from I- to the appropriate sense resistor. Fuses F301/F302 protect the 3mA, 300mA and 3A outputs. Fuse F303 with diode clamp D305/6 protects the active ground buffer.

Relay K308 maintains connection to the internal loads during the ON sequence whilst the external load is being switched in.

Analogue switch array U301 selects the appropriate feedback signal.

- **Active Ground Buffer (401096Sht3):**

The active ground buffer is configured as a ground referenced virtual earth amp. It is formed from an op amp and a class AB, unity gain, output buffer. Relay K301 selects the appropriate feedback resistor (R336-8: 300mA, R313 + 336-8: 3mA).

- **Over Voltage Detector (401096Sht4):**

The over voltage detector consists of a buffer (U403), a precision, unity gain, full wave rectifier/low pass filter (U404) and a comparitor with a switchable threshold (Q434).

The 3mA, 300mA and 3A ranges feed the detector via 'Out 3m' and the 20A range is sensed via 'V-20A'.

The response to the detector is handled via the microprocessor under normal circumstances.

FAULT FINDING - CURRENT FUNCTION

- **±7V5 Supplies:**

The ± 7V5 supplies are high energy and only current limited by the primary fuse. Always be very careful when fault finding with these supplies connected, especially:

- 3A and 20A range faults
- primary side faults

Always check for excessively hot components. The 9000 can be powered up with the ± 7V5 supplies disconnected (E501, E502). Only the 3A and 20A ranges are affected.

- **Bench Supplies:**

Fault finding on the 3A and 20A ranges is simpler with external bench supplies in place of the ± 7V5. Replace internal supplies with:

3AR:	8 - 0 - 8V @ 4A, isolated supply
20AR:	8 - 0 - 8V @ 8A, isolated supply
+8V:	connected to E504
0V:	connected to E506
-8V:	connected to E507

Power on sequence: power up 9000 (with self test disabled - middle horizontal soft key etc) wait 10 s then power up bench supply.

Power off sequence: power off bench supply wait 10 s then power off 9000.

- **Self Test:**

Factory limit full self test is always a good first pass fault check. This checks for most static functional faults like bias conditions, gains, broken loops, clamps and most of the over voltage detector thresholds. It is important to note that the 20A range over voltage detector is not checked with the self test. So if there is any doubt test this manually.

Self test pathways can be used to access machine states that are otherwise unavailable. The most useful state available is open loop with zero input signal. This state, for each hardware range allows symmetrical bias checking:

300mAR - OL - Ø	PO3.001
3mAR - OL - Ø	PO3.011
3AR - OL - Ø	PO3.014

- **Grounding Rules:**

  For earthy instruments (eg scopes) connect earth clip to either 'chassis metalwork' or TP521 (Star 2). Never connect earth clip to TP302. For floating instruments (eg Dmm) connect 'lo' to TP302 (ground 24) as a general reference.

  Due to currents between star points there can be up to 2mVrms between TP302 and TP521.

- **Open Loop Configuration:**

  The open loop mode (J803 to the right) allows functional blocks to be checked without the feedback loop confusing the issue.

  Any range can be selected in open loop mode but the current produced at the output is greater than current indicated on the display, so always select the lowest output on the hardware range of interest (eg 0.33A on 3A range) and then use a handheld Dmm as the output load to check the output current before ramping output up to the required level.

  Approximate range multipliers in open loop mode:

		Multiplier	Maximum Displayed Current
300µA/3mA	:	x 4.2	75µA/0.75mA
30µA/300mA	:	x 4.2	7.5mA/75mA
3A	:	x 1.84	1.7A
20A	:	x 1.52	6.5A

- **AC Response:**

  To check the AC loop response of the current converter use the high frequency load regulation tests to check the loop bandwidth is high enough and the maximum load inductance tests to check that the loop bandwidth is not too great. (Tests can be found in the Power board and instrument test procedures.)

- **High Frequency High Current Problems:**

  Always keep output leads short and tightly coupled (eg 2.5 mm² conductors twisted together). This will keep the resistance and inductance down. To illustrate the problem at 20A/10KHz the compliance voltage limit (0.9Vrms) is developed across a load inductance of only 0.7µH.

  Do not be fooled by the voltage waveform on the output as this will appear to be much more distorted than the actual current flowing - The amplification of the

high frequency components of the current is due to the inductive nature of the load. Check the current waveform either with a current probe, or by monitoring TP310 with your scope. The other consequence of this high frequency amplification is that if there is an oscillation, even at low level, the resultant output oscillation voltage will be large. This helps with low level oscillation detection.

- **Low Current Problems:**

  At high frequency stay capacitance can cause large measurement errors. Guarding will reduce the problem (see diagram K19).

  At low frequency, problems due to beat noise caused either by pick-up of line harmonic interference or by common mode current, from a line powered measuring instrument, finding its way back to earth via the I- of the 9000. These beats will be worst around 51, 101, 151 Hz etc. The solution to pick-up is screening. To prevent common mode current noise beating use a good quality, well guarded Dmm, eg 1271/81. Also remember battery powered instruments do not generate common mode current.

CUSTOMER QUERY ISSUES - CURRENT FUNCTION

- **Inductive Load Handling:**

  Inductive load handling is limited, especially at high current. It is adequate for reasonable leads and loads, but will not handle inductive loads like multi-turn coils used to calibrate clamp-on ammeters.

- **Over Voltage Detector Limits:**

  Due to the soft nature of the clamps and the tolerance of the detector the trip point is beyond the specified region of operation. Consequently if the output voltage is above the specified region (see Vol II spec section) and below the trip level the output current magnitude will be unreliable.

- **Normal and Guarded Output:**

  Normal output is via I+/I- terminals and guarded output via D type pin 1/I- terminal. Via lead set, yellow and black leads - normal or white and black leads - guarded.

  The guarded output is limited to 1A. This output provides a more accurate HF low current output at the lead tips.

- **Primary Specifications:**

  The ACI accuracy specified is for Rms measurement, therefore on mean sensing instruments the mean sense error must be added to the overall accuracy. Mean sense instruments are generally of much lower accuracy so the TURs are not affected significantly.

- **Low Current Output:**

  For pick-up and common mode current issues see "Fault Finding".

- **Earthed Instruments:**

  As the 9000 is earthed it will only operate properly with an isolated load.

Scope Option

Guided Tour

Contents

Scope Calibration Module.

1. Block diagram description of functional configurations.

1.1 Sine 10Hz to 250MHz.

1.1.1 Sine 10Hz to <50kHz. (49.999kHz)

The power and analogue assemblies are used to generate sine waves of a particular amplitude and required output frequency. The front terminal output relays remain open and the scope module connects to the signal HV_P_HI on the 50 way analogue ribbon connector.

This signal is routed to SIG_OUT via the LF attenuator and last stage of the HF attenuator. The final stage of the HF attenuator also acts as the output on/off relay.

The trigger output, TRIG_OUT, is driven at the same frequency as SIG_OUT by the AC coupled trigger comparator, U102, sensing HV_P_HI. Its output is routed to TRIG_OUT via the Actel device U801.

The phase of the trigger and signal may change with 9100 setting (e.g. range & frequency).

The 30MHz VCXO and HF oscillators sleep in this mode to reduce noise.

1.1.2 Sine 50kHz to <11.2MHz.

The scope DDS, U602, is used to generate a sine wave signal of the required frequency and variable amplitude. This is amplified then routed to SIG_OUT via the HF attenuator.

The amplitude level is controlled by a loop which drives the DDS reference. The DDS reference can be over driven by an external signal (0V to 2V). The peak detector on the scope HF assembly and error amplifier compare the set point from the amplitude DAC and scaling with the buffer output to complete the amplitude loop.

At lower amplitudes the DDS has an 8dB input amplifier and -8dB output attenuator to keep its reference at a sensible level. Lower amplitude is decoded by the Actel device, U801, when the latched bits driving the amplitude DAC_D11 to DAC_D8 have the binary code 0 1 0 1 or less.

The DDS is driven at 30MHz by either a 30MHz VCXO or 30MHz +-25ppm fixed oscillator. The VCXO is fitted when option 100 is fitted to the analogue assembly to maintain the frequency specification. A phase lock loop is used to lock the analog assy signal EXP_FREQ_PULSE_H at 58.59375kHz to the 30MHz required for the DDS. The 32 bit scope DDS has 6.99mHz resolution which is 0.139ppm of 50kHz, so small frequency adjustments to the analog assembly DDS are made to get the accuracy well within the 0.25ppm specification of option 100. If the fixed crystal is fitted the frequency corrections to EXP_FREQ_PULSE_H have no effect.

When EXP_FREQ_PULSE_H is used the main DAC on the analogue assembly is set for minimum frequency/pulse output amplitude as the output stage will still be active.

The trigger signal is derived from the AC coupled comparator, U603, sensing the scope DDS output. The follower Q602 is used to stop noise feeding back to the filter. It is routed to TRIG_OUT via the progammable divider (set to divide by one) and trigger selector in the Actel device U801.

The HF oscillators sleep in this mode.

1.1.3 Sine 11.2MHz to <250MHz.

A high frequency signal is generated by a mixer arrangement controlled by a phase lock loop and an amplitude loop. The signal is amplified and routed to SIG_OUT via the HF attenuator.

The output frequency is 32 times the scope DDS frequency (0.350MHz to 7.8125MHz) and adjusted by changing the scope DDS setting (and the analog assembly DDS if the VCXO is fitted). The scope DDS run at higher amplitude from its internal voltage reference as it only provides a frequency reference. The external reference is it is isolated by U807-1/2/3.

The level is set by a control loop which drives a pin attenuator on the mixer output. The peak detector and error amplifier compares the set point from the amplitude DAC with the buffer output to complete the amplitude loop.

The trigger signal is derived from the signal frequency divided by 32. It comes from the pre-scaler U303 and level shifter Q407/Q408. It is routed to TRIG_OUT via the Actel device U801. Delays in the circuitry may cause frequency dependant phase shifts between SIG_OUT and TRIG_OUT.

1.2 Square 1kHz.

The square uses the same path as the sine for 10Hz to 50kHz. The signal is generated at 1kHz only by the power and analogue assemblies.

The analog assembly DDS is loaded with a new pattern so that the base of the square is related to 0V and adjustment will be made to its peak value using the analog assembly main DAC.

The trigger is generated at 1kHz and being AC coupled should line up with SIG_OUT.

The 30MHz VCXO and HF oscillators sleep in this mode.

1.3 DC.

DC uses the same path as the sine 10Hz to 50kHz. The power and analog assemblies generate the DC signal. The LF attenuator includes a filter, C105, which is selected for higher DC voltages using the HF transformer.

The 30MHz VCXO and HF oscillators sleep in this mode.

A trigger signal at approximately 64Hz is generated within the Actel device, U801, using the clock AN_CLK.

1.4 Edge.

1.4.1 Edge 1ns/low amplitude 10ms to 89.29ns.

The edge 1ns/low amplitude output circuitry drives SIG_OUT via the HF attenuator which also provides the output on/off relay.

The repetition period of the output is determined by the scope DDS, U602, which drives through the programmable divider on the Actel device, U801. This combination gives variability in decades without introducing excessive DDS uncertainty at lower frequencies. The scope DDS clock is generated by either the 30MHz VCXO locked to EXP_FRQ_PLS_H.or the fixed crystal The DDS is set to a higher output amplitude using its internal reference.

The output amplitude is set by the amplitude DAC and scaling which drives the edge 1ns/low amplitude output stage directly.

Triggers are generated from the programmable divider output within the Actel device and routed to TRIG_OUT. Signal delay is added by a U605 to ensure that the trigger occurs before the edge.

The HF oscillators should sleep in this mode.

1.4.2 Edge 1ns/low amplitude 89.29ns to 10ns.

This mode uses the sine circuitry (11.2MHz to 100mhz) to drive the edge output circuits.

The repetition period of the output is determined by the scope DDS but the frequency is multiplied by 32 using the HF oscillators and mixer. Minimum attenuation on the mixer output is set by jamming the peak detector and error amplifier to get FS output using U503/14/15/16..

Triggers are generated from the ECL pre-scaler so occur every 32 edges of the output signal.

1.4.3 Edge 100ns/high amplitude 10ms to 10us.

This mode is similar to edge 1ns/low amplitude 10ms to 89.29ns with amplitude and repetition rate routed to the edge 100ns/high amplitude output circuitry, instead of the 1ns/low amplitude.

The HF oscillators sleep in this mode.

1.5 Markers 5.5s to 4ns.

1.5.1 Markers 5.5s to 89.29ns.

This mode uses the same configuration as edge 1ns/low amplitude 10ms to 89.29ns. The lower range is extended to 5.5 seconds by more programmable divider stages.

1.5.2 Markers 89.29ns to 8.8888ns.

This mode uses the same configuration as edge 1ns/low amplitude 89.29ns to 10ns.

1.5.3 Markers 8.8888ns to 04.000ns.

This mode uses the same configuration as sine 11.2MHz to 250MHz. It is actually a sine so the trigger point may vary compared to the other markers.

2. Circuit descriptions -sheet by sheet.

2.1 Sheet 1

Relays shown are driven from circuits on sheet 8 |The comparator U102 senses HV_P_HI to derive triggers when the analog and power assemblies are sourcing the scope module output.

2.2 Sheet 2

Signal DLY_LINE_OUT_H controls the switching of the edge 100ns/high amplitude. FEHA_NEG_L goes low to enable circuitry.

2.3 Sheet 3

Signal SLP2_H is used to enable the oscillators. The pre-scaler U303 is used to drive PLL on sheet 4. Relay K302 allows the edge 1ns/low amplitude to be driven from the sine output above 11.2MHz or DLY_LINE_OUT_H below 11.2mhz.

2.4 Sheet 4

Signal SINE_MIX_FS_L is used to get minimum attenuation from pin attenuator, hence maximum amplitude to drive edge circuitry

2.5 Sheet 5

DAC U501 is used to control amplitude of waveforms generated on the scope assembly. The most significant four bits are latched by Actel device U801 and remain static. They are clocked into DAC when the processor writes the least significant eight bits by strobing DAC_LD_L. The DAC is driven from the analog assembly reference at 8.5536V which gives a ouput between 0V and 8.5536V.

The DAC output is divided by four to drive the edge circuitry. Signal SLP3_H is high when the edge 1ns/low amplitude when not used.

2.6 Sheet 6

The DDS, U602 and filter on U60-2 are used to generate sine waves between 50kHz and 11.199MHz. The DDS has an internal reference of 1.27V on U605-8 which is enabled when switch U807-1/2/3 is open.. When U807-1/2/3 is closed the internal reference is overdriven by the amplitude control signal from the peak detector and error amplifier, DDS_AMP_CTRL. At lower amplitudes the amplifier U606 gives a gain of x2.5 to the reference level and there is a corresponding attenuation from K301-4/7. to help reduce noise effects. The diode clamps, D607 and D608, stop U602-6 going outside the range 0V to +2V. The DDS output U602-2 should always be in the range 0V to 1V.

Folower Q602 and comparator U603 generate a logic signal at the same frequency as the sine wave on REF_FREQ_H. This is used to drive the x32 PLL or programmable divider on Actel device U801-64.

The trigger output stage is a logic gate U604 which gives 1Vpk into 50R external load. The trigger source is selected by Actel device U801from:-

1 programmable divider divide by 1, 2, 20, 200 etc. to 20000000,

2 COMPL_LF_H for signals power and anlog assemblies or

3 DIV_32_TTL_L for outputs frequecies above 11.2MHz.

The programmable divider output U801-63 is delayed by U605 to ensure that the edge outputs occur later than the trigger output.

The DDS clock comes from 30MHz VCXO Y601 (which may be a fixed crytsl when option 100 is not fitted). The VCXO is phase locked to EXP_FREQ_PULSE_H at 58.59375kHz from the analog assembly. The VCXO divide by 512 and phase comparator are on Actel device U801. The fast and slow control outputs are summed and filtered at C812, which feeds back to the VCXO via amplifier U601.

The supply to the VCXO is switched by Q601 to reduce noise when the DDS is not required. D605 and D606 ensure U601 does not drive the VCXO when its power supply is switched off. SLP1_H also reduced the DDS DAC consumption by driving U602_37.

The DDS registers are written by the processor via AN_D7 to AN_D0 which are strobed by DDS_WR_L. Bytes are written in groups to fill a four byte assembly register. The assembly register is transferred to the required destination by AN_A3 to AN_A1 which are strobed by DDS_LD_L (this should be active high). The DDS clock must be present for loading to work properly.

2.7 *Sheet 7*

The self test selection signals TST_6_H to TST_0_H from the analog and power assemblies, control analog multiplexers U701 and U702.

2.8 *Sheet 8*

Actel device U801 contains the double latching for the 32 relay and control bits. The latches are written in groups of four bytes so the last write updates the control outputs. The control bits are written from data on AN_D7 to AN_D0, decoded address AN_A8 to AN_A1 and the strobe AN_DS_L. The signal AN_R_H_W_L is high to read and low to write the registers.

The signal AN_I_OC_L is an open collector interrupt line which signals the processor and other Actel devices that the detector input U801-42 has latched. Actel devices on other assemblies can drive this line. If the interrupt is ignored all Actel devices will force a safe instrument control bit state after 0.25 seconds from the interrupt line first going low. The signal AN_OP_OFF_L is pulsed low when the off key is pressed to check that the firmware services it. It will force a safe state 0.5 seconds after it is first seen if the firmware does not respond.

The signal; AN_LED_ON_L turns on the front panel red LED. It is driven low by Actel devices on other assemblies including the scope module when an output is turned on. When a high voltage control pattern is selected the power assembly Actel device will drive this signal to about 3V once per second to flash the LED off.

3. Control bit names and functions.

These names are for register bits within the Actel device U801 with the pin numbers they drive shown in brackets. They may be useful when fault finding.

3.1 *LF Attenuator Bank and Filter*

The following bits are decoded for sine 10Hz to 50kHz, DCV and square 1kHz. They control the LF Attenuator which is used only when the power and analogue assemblies are to drive the scope option output.

S1-0	ATN_LF_RL1_H	default=L	[83]
S1-1	ATN_LF_RL2_H	default=L	[31]
S1-2	ATN_LF_RL3_H	default=L	[1]
S1-3	ATN_LF_RL4_H	default=L	[80]
S1-4	ATN_LF_RL7_H	default=L	[6]
S1-5	ATN_LF_RL8_H	default=L	[5]
S1-6	ATN_LF_DCV_H	default=L	[3]
S1-7	SEL_9100_H	default=L	[2]

3.2 *HF Attenuator Bank and Output Relay*

S2-0 ATN_HF_19dB_1_H default=L [73]
H inserts 19dB attenuator 1 for sine 50kHz to 250MHz.
L attenuator 1 bypassed.

S2-1 ATN_HF_19dB_2_H default=L [34]
H inserts 19dB attenuator 2 for sine 50kHz to 250MHz.
L attenuator 2 bypassed.

The following bits are decoded to select 9.66dB attenuator and perform output on:-

		output off (default)	output on 9.66dB atten	output on no atten
S2-2	ATN_HF_9dB_IN_H [76]	L	L	H
S2-3	ATN_HF_9dB_OUT_H [77]	L	H	L

3.3 *Trigger Control*

		disabled (default)	sine 10kHz to 50kHz - IP1	output freq / 32 - IP2	prog. divider
S2-4	TRG_F0_H [no pin]	0	1	0	1
S2-5	TRG_F1_H [no pin]	0	0	1	1

S2-6 TRG_FLT_H (not used) default=L [13]
H trigger filter active
L trigger filter inactive.

S2-7 TRG_INV_H default=L [no pin]
H trigger output is inverted
L trigger output not inverted.

3.4 Edge 1ns/Low Amplitude and 100ns/High Amplitude

S3-0 FELA_MIX_H_DIV_L default=L [78]
H drives edge low amplitude from the DDS & mixer (50kHz to 11.2mhz).
L drives edge low amplitude from the programmable divider delay line.

S3-1 FELA_POS_H (do not select with NEG) default=L [30]
H configures edge low amplitude for positive output pulse.
L disables edge low amplitude positive output.

S3-2 FELA_NEG_H (do not select with POS) default=L [24]
H configures edge low amplitude for negative output pulse.
L disables edge low amplitude negative output.

S3-3 FEHA_NEG_L default=H [79]
H disables edge high amplitude negative output.
L configures edge high amplitude for negative output pulse.

S3-4 FEHA_0DB_H default=L [7]
H de-selects attenuation of edge low amplitude.
L selects -15dB attenuator for edge high amplitude negative output.

S3-5 SPARE S3_5 [8]

S3-6 SPARE S3_6 default=L [21]

S3-7 FE_TST_H default=L [no pin]
H drives edge frequency inputs high to stop noisy signal toggling and for for test.
L allows edge inputs to be driven fom selected source.

3.5 General Signal Routing.

S4-0 SINE_HF_H default=L [53]
H connects sine 50kHz to 250MHz from mixer or DDS to output circuitry.
L other functions connected to output circuitry.

S4-1 SINE_DDS_H_MIX_L default=L
H connects DDS to output circuitry for sine 50kHz to 11.2MHz.
L connects mixer to output circuitry for sine 11.2MHz to 250MHz.

S4-2 SINE_MIX_FS_L default=L [62]
H normal sine 50kHz to 250MHz amplitude loop operation.
L drives the sine 50kHz to 250MHz amplitude control loop to maximum output.

S4-3 DDS_EXT_REF_L default=H [70]
H DDS internal reference for use as frequency source without amplitude control.
L closes amplitude loop for sine 5kHz to 11.2MHz.

S4-4 NOT_FELA_H default=L [11]
H other functions connected to output circuitry.
L connects edge low amplitude to output circuitry.

3.6 *Sleep Control.*

S4-5 SLP1_H default=H [10]
H 30MHz VCXO to sleep mode.
L 30MHz VCXO enable.

S4-6 SLP2_H default=H [15]
H HF oscillators to sleep mode.
L HF oscillators enable.

S4-7 SLP3_H default=H [81]
H edge low amplitude to sleep mode.
L edge low amplitude enable.

4. Scope Actel Registers.

The scope Actel device controls the address decoding for the DDS, DAC and control bits. Read-back is only provided on the four control bit registers and the status register.

The S CLR address should be cleared in the same way as the P CLR and A CLR in the power and analogue devices. There is a spare detector and the same off key time-out and hardware go to neutral (should the common signal generation interrupt not be serviced by the processor) system as the other devices.

The programmable divider is a cascaded decade counter. The taps are selected by the programmable divider register.

4.1 Status Register

This is decoded as follows:-

SR-0 OFF_TIMEOUT_H

H output off key time-out has occurred or the hardware has gone to neutral as the interrupt was not serviced.

SR-1 S_DET_H

H detector has tripped causing interrupt and starts go to neutral time-out.

SR-2 OPT_TST_L

H option not fitted

L option fitted

4.2 Programmable Divider

Bits 3 to 0 are decoded as follows:-

	PD-3	PD-2	PD-1	PD-0
1/1 (default)	0	0	0	0
IF_CLK (64Hz)	0	0	0	1
1/2	1	0	0	0
1/20	1	0	0	1
1/200	1	0	1	0
1/2000	1	0	1	1
1/20000	1	1	0	0
1/200000	1	1	0	1
1/2000000	1	1	1	0
1/20000000	1	1	1	1

IF_CLK is used to provide a trigger output in DCV scope function.

The output of the programmable divider drives the edge circuitry via pin 63 and/or the trigger via pin 14

4.3 Control Bit Registers

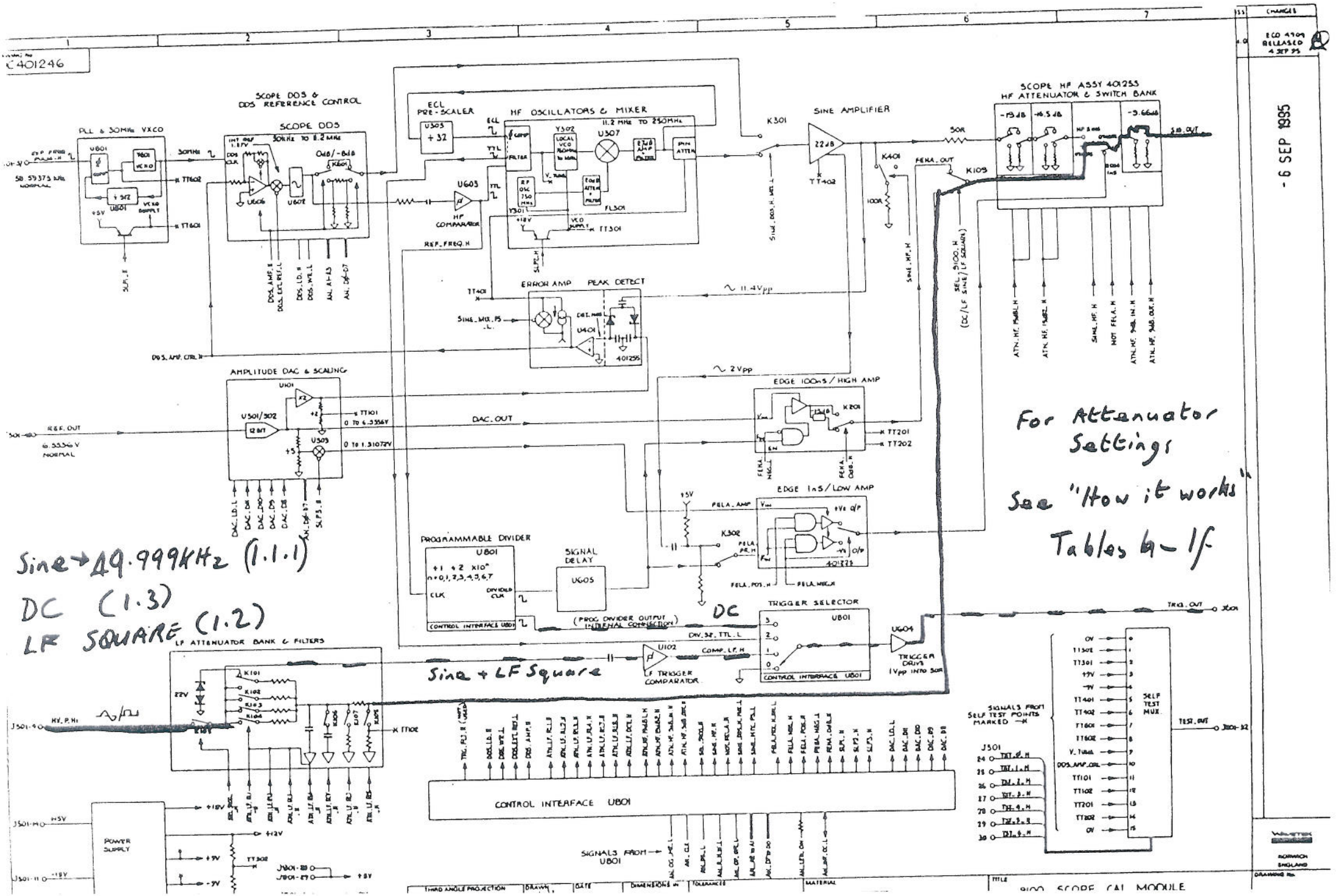
These registers are described above as S!, S2, S3 & S4. They can be written and read and are double latched so writing S4 (possibly using MOVEP.L) will change the control bits to the new state. The read is of the second latch driving the output pin levels.

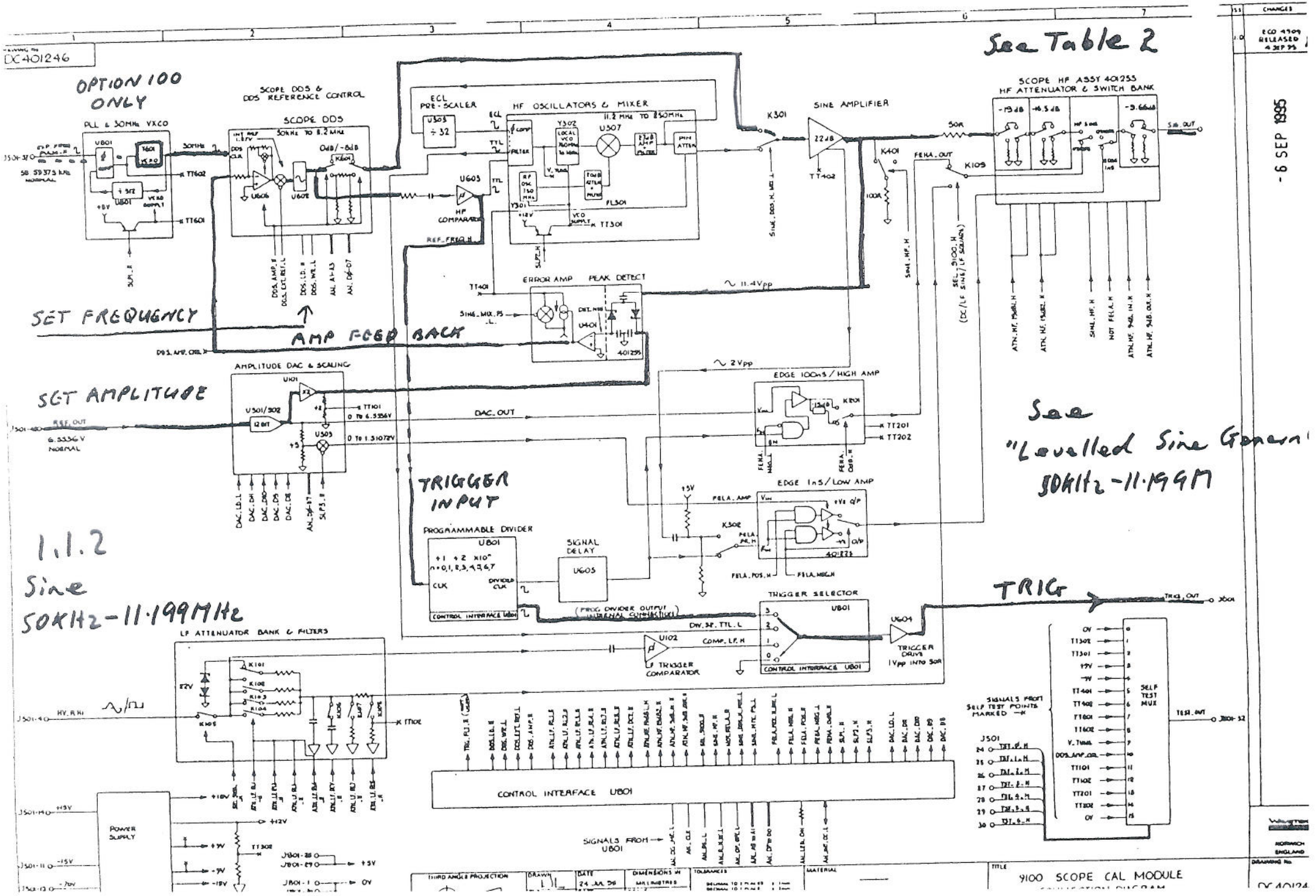
4.4 Scope DAC

This DAC is written (possibly using MOVEP.W) as a high byte containing D11 to D8 and a low byte containing D7 to D0. The high byte is latched and transferred to the DAC when the low byte is written.

4.5 DDS Registers

The DDS assembly register is used to temporarily hold values to be written to the DDS registers.


C401246
SCOPE DDS & DDS REFERENCE CONTROL
SCOPE DDS
PLL & 30MHz VXCO
ECL PRE-SCALER
HF OSCILLATORS & MIXER
11.2 MHz TO 250MHz
SINE AMPLIFIER
SCOPE HF ASSY 401255
HF ATTENUATOR & SWITCH BANK
ERROR AMP PEAK DETECT
AMPLITUDE DAC & SCALING
EDGE 100nS / HIGH AMP
EDGE 1nS / LOW AMP
PROGRAMMABLE DIVIDER
SIGNAL DELAY
TRIGGER SELECTOR
LF ATTENUATOR BANK & FILTERS
CONTROL INTERFACE U801
POWER SUPPLY
SELF TEST MUX
SIGNALS FROM SELF TEST POINTS MARKED —H
SIGNALS FROM U801
Sine → 49.999KHz (1.1.1)
DC (1.3)
LF SQUARE (1.2)
Sine + LF Square
DC
For Attenuator Settings
See "How it works"
Tables 4 – 1/-
ECO 4909 RELEASED 4 SEP 85
- 6 SEP 1985
9100 SCOPE CAL MODULE


DC401246
OPTION 100 ONLY
See Table 2
SCOPE DDS & DDS REFERENCE CONTROL
PLL & 30MHz VXCO
SCOPE DDS
ECL PRE-SCALER
HF OSCILLATORS & MIXER
SINE AMPLIFIER
SCOPE HF ASSY 401255
HF ATTENUATOR & SWITCH BANK
SET FREQUENCY
AMP FEED BACK
ERROR AMP
PEAK DETECT
SET AMPLITUDE
AMPLITUDE DAC & SCALING
EDGE 100nS / HIGH AMP
EDGE 1nS / LOW AMP
TRIGGER INPUT
PROGRAMMABLE DIVIDER
SIGNAL DELAY
TRIGGER SELECTOR
TRIG
LP ATTENUATOR BANK & FILTERS
LF TRIGGER COMPARATOR
TRIGGER DRIVE 1Vpp INTO 50R
1.1.2
Sine
50KHz-11.199MHz
See "Levelled Sine Generator"
50KHz-11.199MHz
CONTROL INTERFACE U801
POWER SUPPLY
SELF TEST MUX
SIGNALS FROM SELF TEST POINTS MARKED -H
SIGNALS FROM U801
ECO 4909 RELEASED 4 SEP 95
- 6 SEP 1995
9100 SCOPE CAL MODULE
NORWICH ENGLAND