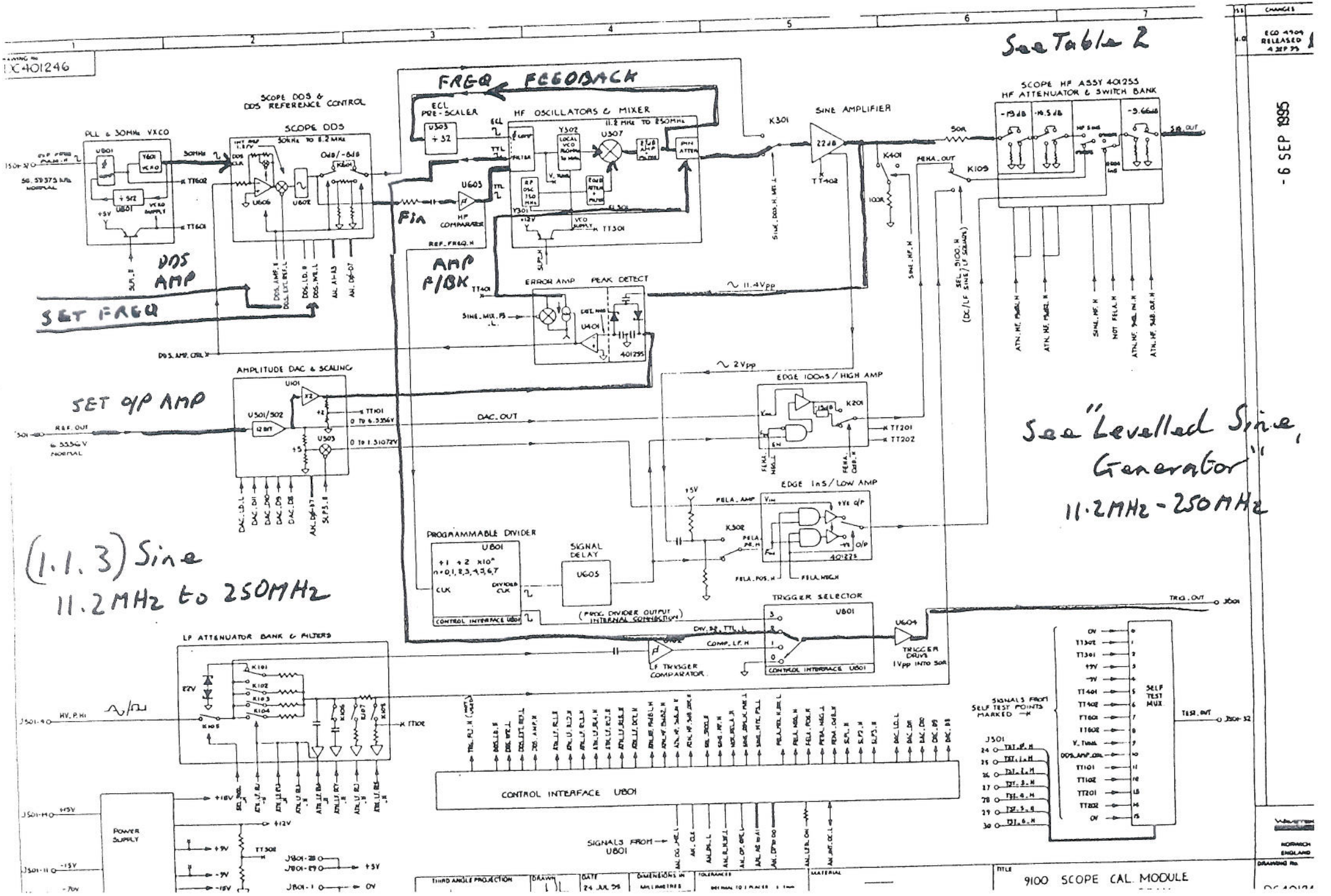
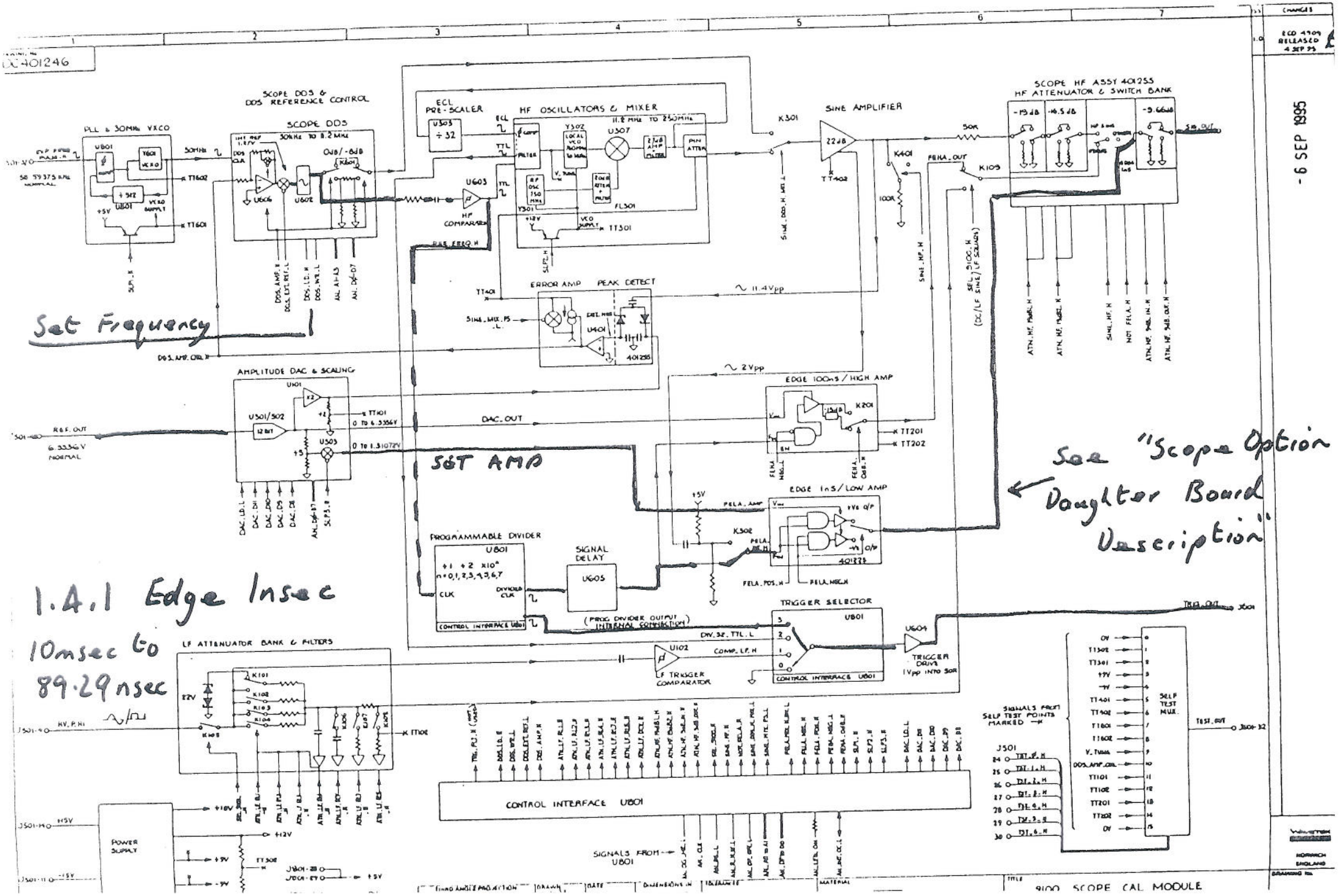
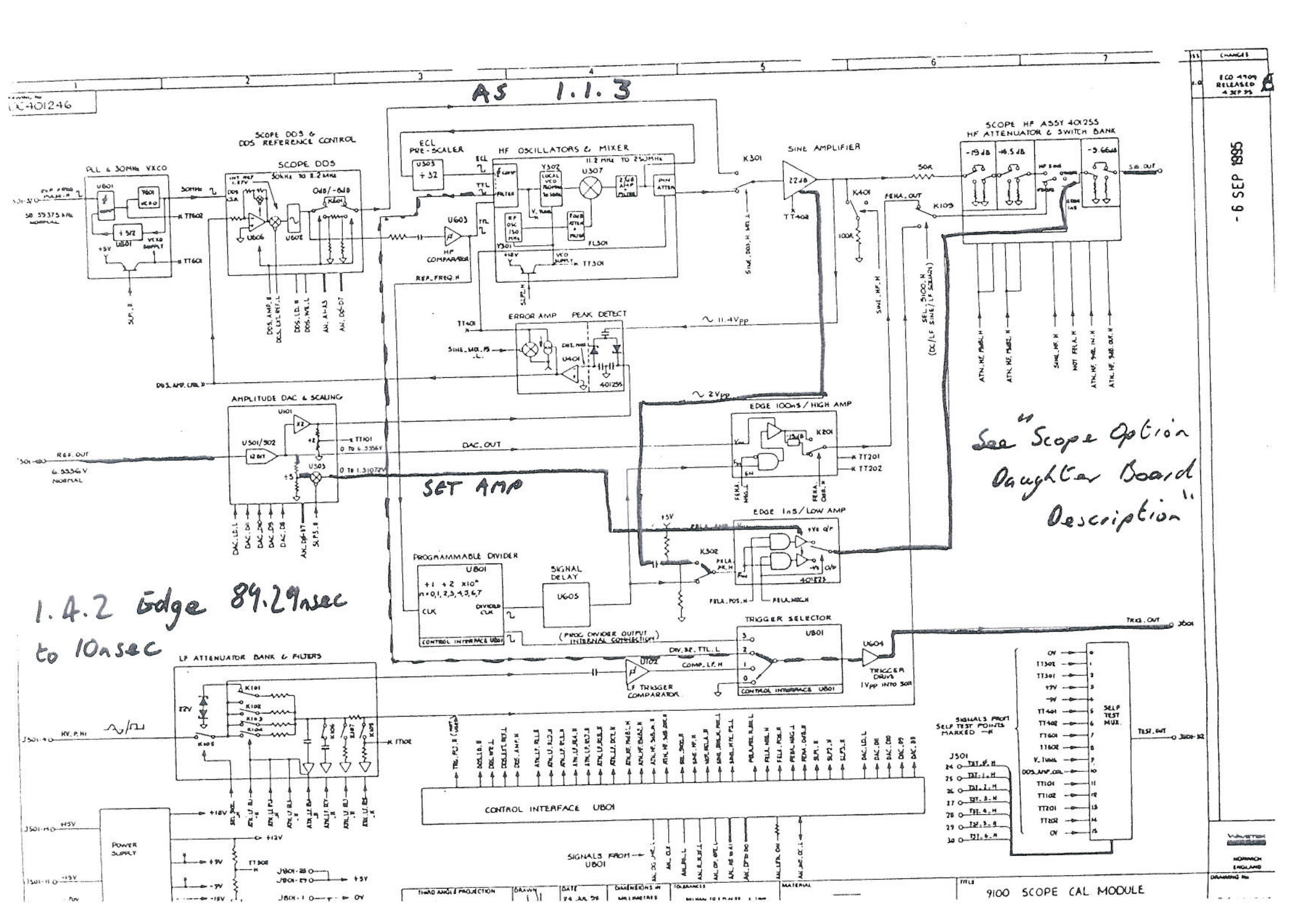
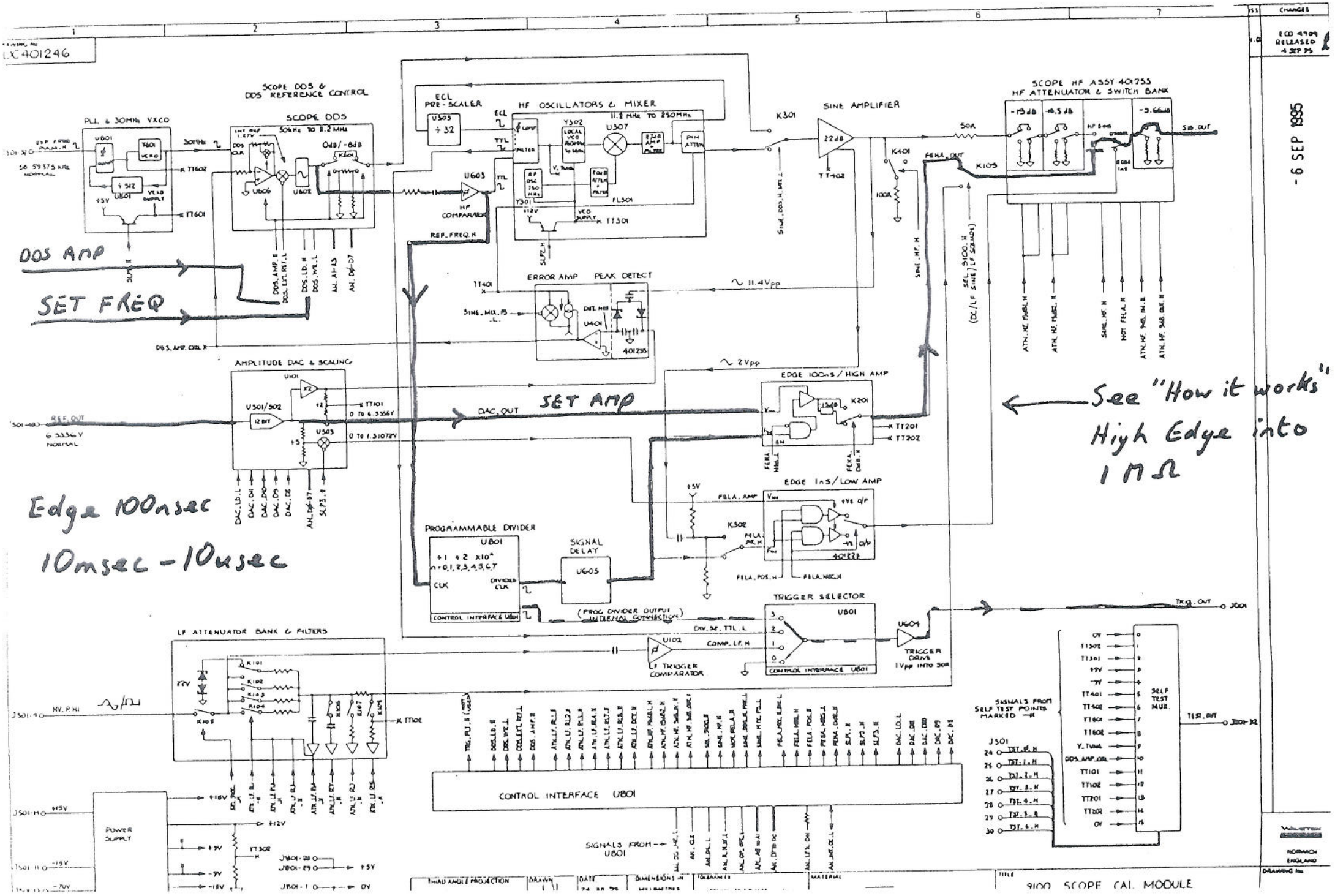

DC401246
See Table 2
FREQ FEEDBACK
SCOPE DDS & DDS REFERENCE CONTROL
SCOPE DDS
PLL & 30MHz VXCO
ECL PRE-SCALER
HF OSCILLATORS & MIXER
11.2 MHz TO 250MHz
SINE AMPLIFIER
SCOPE HF ASSY 401253
HF ATTENUATOR & SWITCH BANK
DDS AMP
SET FREQ
AMP P/BK
ERROR AMP
PEAK DETECT
AMPLITUDE DAC & SCALING
SET O/P AMP
EDGE 100nS / HIGH AMP
EDGE 1nS / LOW AMP
PROGRAMMABLE DIVIDER
SIGNAL DELAY
TRIGGER SELECTOR
LF ATTENUATOR BANK & FILTERS
CONTROL INTERFACE U801
POWER SUPPLY
SELF TEST MUX
(1.1.3) Sine
11.2MHz to 250MHz
See "Levelled Sine Generator"
11.2MHz - 250MHz
9100 SCOPE CAL. MODULE
- 6 SEP 1995


DC401246
CHANGES
ECO 4909 RELEASED 4 SEP 95
- 6 SEP 1995
SCOPE DDS & DDS REFERENCE CONTROL
PLL & 50MHz VXCO
SCOPE DDS
ECL PRE-SCALER
HF OSCILLATORS & MIXER
SINE AMPLIFIER
SCOPE HF ASSY 401255
HF ATTENUATOR & SWITCH BANK
Set Frequency
ERROR AMP PEAK DETECT
AMPLITUDE DAC & SCALING
Set AMP
EDGE 100nS / HIGH AMP
EDGE 1nS/LOW AMP
PROGRAMMABLE DIVIDER
SIGNAL DELAY
TRIGGER SELECTOR
LF ATTENUATOR BANK & FILTERS
CONTROL INTERFACE U801
POWER SUPPLY
SELF TEST MUX.
SIGNALS FROM SELF TEST POINTS MARKED →
SIGNALS FROM U801
9100 SCOPE CAL MODULE
See "Scope Option Daughter Board Description"
1.A.1 Edge Insec
10msec to 89.29nsec


AS 1.1.3
SCOPE DDS & DDS REFERENCE CONTROL
PLL & 30MHz VXCO
SCOPE DDS
ECL PRE-SCALER
HF OSCILLATORS & MIXER
SINE AMPLIFIER
SCOPE HF ASSY 401255
HF ATTENUATOR & SWITCH BANK
ERROR AMP
PEAK DETECT
AMPLITUDE DAC & SCALING
EDGE 100nS / HIGH AMP
EDGE 1nS / LOW AMP
PROGRAMMABLE DIVIDER
SIGNAL DELAY
TRIGGER SELECTOR
LP ATTENUATOR BANK & FILTERS
POWER SUPPLY
CONTROL INTERFACE U801
SELF TEST MUX
SET AMP
See "Scope Option Daughter Board Description"
1.4.2 Edge 89.29nsec to 10nsec
ECO 4909 RELEASED 4 SEP 95
- 6 SEP 1995
9100 SCOPE CAL MODULE


LC401246
CHANGES
ECO 4909 RELEASED 4 SEP 95
- 6 SEP 1995
SCOPE DDS & DDS REFERENCE CONTROL
PLL & 30MHz VXCO
SCOPE DDS
ECL PRE-SCALER
HF OSCILLATORS & MIXER
SINE AMPLIFIER
SCOPE HF ASSY 401255
HF ATTENUATOR & SWITCH BANK
DDS AMP
SET FREQ
ERROR AMP PEAK DETECT
AMPLITUDE DAC & SCALING
SET AMP
EDGE 100nS / HIGH AMP
EDGE 1nS / LOW AMP
See "How it works"
High Edge into
1 MΩ
Edge 100nsec
10msec - 10usec
PROGRAMMABLE DIVIDER
SIGNAL DELAY
TRIGGER SELECTOR
LF ATTENUATOR BANK & FILTERS
CONTROL INTERFACE U801
POWER SUPPLY
SIGNALS FROM SELF TEST POINTS MARKED —H
SELF TEST MUX.
9100 SCOPE CAL MODULE

Scope Option Daughter Board Description

The fast edge circuit is simple both in concept and implementation. The rising and falling edges are produced by two separate circuits, with the valid edge being the one that ends up at 0V. Too avoid duplication I will describe only the falling edge +ve side of the circuit.

When the falling edge is selected U101 pin 11 should have a TTL level signal on it of the same frequency as that applied to U101 pins 12,13 The level should transition between 0V and +5V and not be significantly away from either of these levels. The junction of R101, R102 is the same signal divided by 2 (0V to +2.5V). Q101 reflects this up to the +9V rail giving a differential voltage across R103 of 2.5V. This is now reflected down from the +9V rail and offset by the Q114 buffered voltage level. This level is now current buffered to R111 which should switch between 3V and 4.7V. D101 anode should sit at 4V, although this level may differ slightly between units it is the relationship between this and the voltage on R111 that should remain constant. The level on R111 will cause either Q104 or Q105 to sink all of the current produced by the current source, U102, Q106. The current source is simple enough, the controlling voltage is converted to a current though R158 by U102, this is mirrored up to the +9V rail to R160 which feeds U102 with a voltage equal to that on E107. This voltage is then converted to a higher current through R119 and sourced to the switching circuitry via Q106 collector. The voltage across R160 is also converted to a current through R159 and reflected down to the -9V rail, to be converted back to a voltage across R161 and hence feed the current source for the rising edge generator.

R158, R160 R159 (R119) R148 (over when ⌐ selected)

R161 should all have same volts when ⌐ selected

Danger points :- Q106, Q105 have gain of ≈ 20

Q112, Q111 have gain of ≈ 50

So be aware that ⌐ edge circuit needs more V_{in} (E129) to give same V_o as ⌐ circuit.

C108 has been known to leak, which makes Q106 seem to be lower gain than expected.

The transistors do get warm

9100 Scope Option - How it works.
High Edge into 1Mohm

This section describes sheet two of DC401231. The circuit has three main sections, a 50 Volt output pulse amplifier, a variable power supply with a 70 volt input and a sampler to provide feedback and control the power supply.

For test purposes, link J201 can be connected between 1and 2. This reduces the supply on the pulse circuit output to a safe 9volts, which should prevent smoke even if there is a gross fault. It is essential to get the pulse circuit and power supply working properly before making this link between 2 and 3 for normal operation.

The three sections of U201 controlled by FEHA_NEG_L turn the circuit off when the control line is high. Under this condition, the power supply output must be less than 1V. U202/6 output can drift to either rail, this does not matter.

The pulse circuit is in two halves, which are similar, so only one is described here. Current into Q201 causes it to turn on, hence turning on Q202 and then Q207. The other components are for anti-saturation, capacitive speed up and base current limiting. The design objective is for Q207 to be just starting to turn off when Q203 turns on and vice versa. This gives a good positive edge, (from minus volts up to zero) and a reasonable falling edge.

R214,215 prevent current "shoot through", if due to a switching problem, both output transistors momentarily turn on. C253 allows 200 nanoseconds of unrestricted current, to permit the negative going edge to charge C222, which shapes the pulse.

If an over current is sensed, the volts across R246 causes Q212 to turn on, sufficient to pull down the overload line, at which point the firmware will turn the output off. R246 also provides emergency pulse by pulse current limiting. If the volts across it reaches 0.9V, Q206 also turns on, and hence Q207 turns off. Note that this does not normally prevent the firmware from giving a system trip. To examine overcurrent situations requires the use of the 9V supply (or in extreme cases even less).

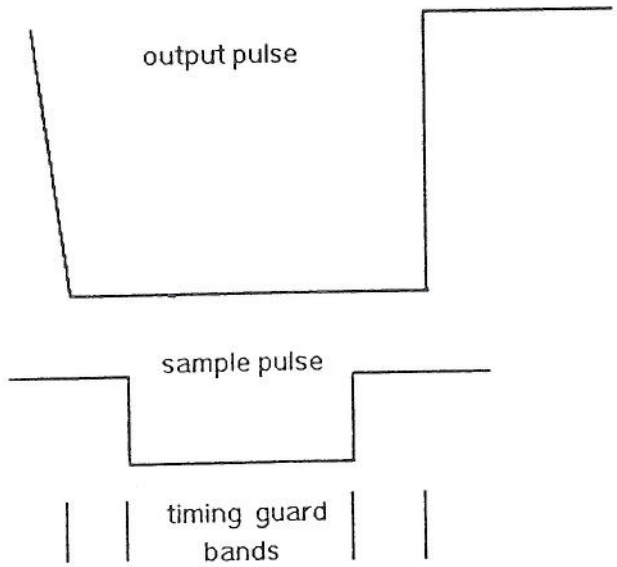
Disconnecting the firmware overcurrent detector Q212 should not be done except as a last resort. Note that in this event, if an auxilary supply, eg the 9V is not used, the current limit of the 70V power supply (Q299) may be forced to operate. The safe rule is to use the lowest possible power supply voltage where a trip is about to happen.

The power supply is conventional. Current into Q211 turns on Q210, hence Q208. R217 and Q209 is a current limit, but this only buys a little time, as it is not possible to provide enough heatsinking to last for ever. It can be tested safely by injecting volts into R228/D215 junction with the high edge function deselected, and J201 in the test position. The voltage gain is (R239+R247)/R228, or about 7.2. So 5 volts in gives about 32V out at this point after allowing for diode drops.

Note that load faults will cause overcurrent trips only when the output volts is above 4.444V. If overcurrent trips occur at say, 4V the problem is in the pulse circuit. If they occur at 48V but not at 4V then look in the output circuitry for the problem.

The next thing to check is the sample circuit, the timing of which is described below.

The pulse input is DLY_LINE_OUT_H. U205 and associated components provide two similar 5V pulses which are slightly skewed so as to allow for propogation delays in the sampler U201/1,2,3 This allows the sample pulse edges to be inside the Output pulse.



The actual sampling timing cannot be seen, as it includes the internal delay time of U201. The sample falling edge on U201/1 has to be on or to the right of the pulse falling edge, and the sample rising edge must be 300nsec before the o/p pulse starts to rise.

The output pulse is divided by twelve by R220,231,232, and buffered by U204 before sampling. U201/1 controls the sample and hold, the hold capacitor being C212, which in turn is buffered by U203. So if this is working properly, with a 9V negative supply, the output pulse should be about 7V (2V is lost in the o/p circuit) and U203/6 should be at about -0.58V. It can be seen that the objective is to sample the negative level of the output pulse, thus removing the drops present in the output stage. D214 is a fault limiter. If the sampler is not working, the circuit would tend to go to full output. If the o/p is about 15V more negative than C212 thinks it should be, D214 conducts, charging C212 and thus preventing the output from becoming uncontrolled.

When the circuit is selected and all working, with the test link in the run position, the pulse voltage is set as follows. DAC_OUT sends current towards U202 pin 3. This cannot go into the pin, and must go down R225 into U203/6. As an example, 2.85volts in causes 0.05mA. Through R225, this demands U203/6 to be -2.35volts.

2.35 times 12 gives a pulse amplitude of -28.2volts. This would require the power supply to deliver around -30 volts, and U202/6 should be at 30/7.2 = 4.6V, plus another 1.4V for the drops across D215 and across Q211, which acts as a virtual earth at 0.7V

If the procedure outlined above has been followed, and the whole circuit doesn't work, only U202 has not been tested, and this should be examined carefully. This is difficult. If utter confusion results, R256 may be fitted at 680K and R225/C211 removed. This removes the sampler from the loop, and DAC_OUT controls the power supply output voltage via U202, with a gain of around 12. In this case, U203/6 should end up nearly the same as DAC_OUT, but it has no control effect on the loop in this configuration.

Further methods are given in the Self Test section which forms an appendix to the board test procedure PT 401231 Issue 1.0

9100 Scope Calibrator Board Test Procedure

Equipment required

1.0 9100 scope cal test rig TExxxx
2.0 1281 DVM
3.0 Oscilloscope 350MHz (min) with 50ohm input. Preferably analogue type.
4.0 Frequency counter Dana 8130 TExx
5.0 50ohm through terminator Suhner 6701-01-B TExxxx
6.0 50ohm through terminator Greenpar B35X13E999X99 TExxxx
7.0 Delay Line and Mismatch TExxxx
8.0 RF millivoltmeter eg Boonton model 92E or similar
9.0 3.5 digit handheld DMM (or better).
10.0 Spectrum Analyser 50kHz to 1GHz (min).
11.0 1KΩ Test link with hook at one end and probe point at other end.

Abbreviations used

w.r.t. = with respect to
ESD = Electrostatic Discharge
I.C.T. = In Circuit Test
Ωload= Press horizontal soft key on 9100 used to change Zout of the 9100.

Notes

1.0 All faults found and their fixes should be listed on the I.C.T. test record sheet.
2.0 Observe ESD precautions throughout these tests.
3.0 As this assembly uses Surface Mount Technology any rework must be carried out by a rework operator trained in Surface Mount rework.
4.0 Scope settings are a guide and may require slight variation with board and operator preference.

Preliminary

1.0 Check visually for solder splashes, open circuits, missing components and/or orientation errors.
2.0 Check regulator heatsinks are fitted parallel; they are connected to raw power supplies and must not touch each other.
3.0 Check all relevant ECO's have been correctly implemented.
4.0 Ensure a handbag link is fitted between J201 pins 1and 2. (Pin 1 is at front)
5.0 Set the RF oscillator frequency adjustment R303 to mid-scale.
6.0 Ensure switch 7 on the rear is UP.

1.0 Procedure

1.1 Fit the unit under test to the 9100 scope cal test rig and connect four cables (output,trigger, 34way IDC,50way IDC)+ one ground strap.

Ensure the heatsink plate above Q401-4 is correctly fitted with regard to ECO issue and tightness. There must be good metal to metal contact to the standoff underneath, with adequate heat sink compound.

Switch on and hold in the centre button below the display (this disables power on self test) until the logo disappears.

Check immediately for overheating components.

Note that the output transistors Q401,402,403,404 do run quite hot (heat sink)

2.0 Self test

2.1 Select Mode, Test, enter the password (741258), then press the upper vertical soft key to enable factory limits and press the second from the top vertical soft key to enable scope cal tests.

A small ***f*** and **s** should appear in the lower right corner of the display to indicate that the factory limits and scope cal tests are selected. Run Full scope selftest.

2.2 At least one of S02.001 and S02.002 should fail, if there are any other fails, investigate and rectify before proceeding further. See appendix for self test descriptions and test details.

3.0 High (100nsec) Edge.

3.1 Tests S02.001 and S02.002 fail due to the link position of J201, which permits only a fixed 9V power supply. Connect SIG-OUT to an Oscilloscope Ch1 set to 1MΩ 2V/div, 1msec/div. Trigger from Ch1. On the 9100 UUT select AUX, EDGE, Ωload=1MΩ, 5V, 1msec, o/p ON.

If a 7V square waveform appears, then the pulse circuit is probably OK. If the UUT trips out, investigate the current limit circuitry.

3.2 Using a DVM, check that J201/3 is between -0.2V and 0V wrt D504 anode. (=0V reference point).

3.3 Increase the demanded output of the 9100 to 12V at 1KHz (=1msec) and check that the DVM reads between -10V and -30V.

{If these tests fail, check the path U204/6, (0.5V squarewave), U201/2, U203/6(-0.5V DC) is correct. Otherwise, check out U202, which under the above two conditions should try to swing rail to rail, negative for the 5V demand and positive for the 12V demand. The only other fault may be U205, which produces delayed versions of the input DLY_LINE_OUT_H. The correct delay is of the order of 300nsec}.

3.4 Turn the 9100 o/p OFF, and move the link on J201.

Manually repeat self tests S02.001 and S02.002 and ensure a pass is obtained. If not, refer to appendix.

4.0 Low (1nsec) Edge.

4.1 Connect SIG-OUT to an Oscilloscope, Ch1 set to 50Ω 0.2V/div, 10µsec/div. Connect TRIG_OUT to Ch2 set to 0.2V/div via a 50Ω terminator (item 6) or select 50Ω on the Ch2 input if available. Set the scope to trigger from Ch2. (Do not display Ch2). Set the 9100 to AUX, EDGE, (rising) Ωload=50Ω, 1V, o/p ON. The scope trace should be a -ve 100KHz square wave of 0.90V to 1.02V.

(If the scope can't be triggered, it will be necessary to trigger from Ch1 until the trigger is fixed in section 8. Note that unless otherwise stated, Ch2 is used as described here to provide a consistent trigger throughout the whole of this test procedure).

4.2 Set scope to 1µsec/div. Check that the negative voltage level is flat to within 20mV.

4.3 Set the edge to Falling by pressing the horizontal EDGE TYPE softkey. Set scope to 10µsec/div.
The scope trace should be a +ve 100KHz square wave of 0.90V to 1.02V.
Set scope to 1µsec/div. Check that the positive voltage level is flat to within 20mV.

4.4 Set the frequency to 1MHz. Set scope to 0.1µsec/div.
Check that the positive voltage level is flat to within 20mV.

4.5 Set the edge to Rising by pressing the EDGE TYPE softkey
Check that the negative voltage level is flat to within 20mV.

4.6 Set the frequency to 100Hz. Set scope to 1msec/div.
Check that the negative voltage level is flat to within 20mV.

4.7 Set the edge to Falling by pressing the horizontal EDGE TYPE softkey.
Check that the positive voltage level is flat to within 20mV.

4.8 Set the edge to Rising by pressing the EDGE TYPE softkey
Set the 9100 to 320mV, 100KHz. Set scope Ch1 to 0.1V/div, timebase 10µsec/div.
Check the O/P level is 300mV to 340mV. Turn 9100 OFF.

5.0 Amplitude functions.

5.1 On the 9100 select AUX, SQUARE, ΩLoad=1 MΩ. Use direct entry on the 9100 to set the output level to 80mV. Connect SIG_OUT to scope Ch1 set to 20mV/div, 1MΩ, timebase=200µsec/div. Turn 9100 o/p ON. Check that an output of 75 to 85mV is obtained.
Check there is no overshoot on either waveform edge greater than one line thickness on the scope.

5.2 Set the scope to 10V/div, 20µsec/div. On the 9100 select SINE, 49.9KHz, Ωload =1MΩ, 80V.
Check the oscilloscope indicates 75 to 85V. Turn 9100 OFF

6.0 50 ohm outputs.

6.1 Reduce the output on the 9100 to 3.3V, select Ωload=50Ω, o/p ON. Fit the terminator item 6 to SIG_OUT. **Do not** use the internal 50Ω of the scope! Set the scope to 1V/div.
Check for 3.1 to 3.5V on the Oscilloscope. Turn 9100 o/p OFF. Leave the 50Ω load connected.

7.0 Overload protection.

7.1 Set the 9100 to SINE, 49.9KHz, 1MΩ, 20V, turn the o/p ON, and check that the output is immediately tripped OFF. If it doesn't trip, turn it off as quickly as possible and investigate the fault, probably on the 9100 power amp overload; detector not functioning.

7.2 Select EDGE, Ωload=1MΩ, 20V, 1KHz. Turn 9100 ON, and check that the output is immediately tripped OFF. If it does not trip, turn it off as quickly as possible and investigate the fault, probably in the overload detector of the high edge circuitry.

8.0 Trigger Outputs.

8.1 Connect SIG_OUT to a scope Ch 1, 1MΩ set to 0.2V/div, 5msec/div and TRIG_OUT to Ch 2 set to 0.2V/div, 50Ω (moving terminator item 6 from Ch1 or using internal 50Ω on the Ch 2 input if available).

Set the scope to 10msec/division. Set scope to trigger from Ch2, and display Ch2.

On the 9100 select AUX, DCV, 1V, Ωload=1MΩ and turn the o/p ON.

Check scope Ch 1 indicates between 0.95 and 1.05V.

8.2 Check that TRIG_OUT logic signal, Ch2 has a period of 14.7 to 16.6mSec and is of amplitude between 0.9 and 1.1V.

8.3 On the 9100 select AUX, SINE, Ωload = 50Ω, 10KHz 5.0mV and turn o/p ON. Set scope Ch1 to 50Ω, 5mV/div, 10usec/div. The scope must be on CHOP vertical mode during this test, not ALT mode, unless the scope is digital.

Check TRIG_OUT logic signal Ch 2 is 0.9 to 1.1V wrt 0V and that the mark space is 45:55 or better ('high' for 4.5 divisions or greater).

Check Ch1 indicates between 4.8 and 6.0mV, (allowing for some noise) If there is some LF present, ensure both 9100 o/p leads go to the LEFT of the UUT. i.e. Do not put the scope on the RHS of the UUT.

Check Ch1 and Ch2 are synchronised at the same frequency.

8.4 Set scope to 2µsec/div. Return scope to ALT display. Set 9100 frequency to 49.9kHz and repeat the three checks of section 8.3 above.

8.5 On the 9100 select 10.7mV, 50.0kHz and turn output on.

Check TRIG_OUT logic signal is between 0.9 and 1.1Vpk wrt 0V (ignoring short duration overshoots) with a mark space of 35:65 or better ('high' for 3.5 divisions or greater).

Check Ch1 and Ch2 are synchronised at the same frequency.

8.6 Increase amplitude to 15mV and repeat the checks of section 8.5.

8.7 Set UUT frequency to 11.1MHz, scope to 10nsec/div, and repeat checks as in 8.5.

8.8 Set the scope to 0.5µsec/division. Set UUT frequency to 11.3MHz.

The trigger frequency should become 353.125kHz eg. period of 2.8µSec (output frequency/32). Note that there is only one positive trigger transition, at just past the centre of the 'scope display, and two negative transitions. (A further +ve transition may be seen at the extreme LHS of the scope display).

9.0 Timing Markers.

9.1 Set the 'scope to 0.2msec/div, Ch1 to 0.5V/div. On the 9100 select AUX, TIMING MARKERS, (lowest RHS vertical soft key) 1ms, o/p ON.

Check that the TRIG_OUT signal has a period of 1ms.

9.2 Connect SIG_OUT to scope Ch1 set to 0.5V/division 50Ω, timebase 20nSec/division. On the 9100 select 8.9000nsec.

Check SIG_OUT (Ch1) is 0.9V to 1.1V peak signal wrt 0V with 30:70 to 45:55 mark/space. (the waveform may look like a half wave rectified sine; measure the mark from the base of the waveform.)

Check TRIG_OUT (Ch2) is 0.9V to 1.1v peak signal wrt 0V.

9.3 On the 9100 select 8.8000nsec and check SIG_OUT (Ch1) becomes 1Vpp sinewave.

9.4 On the 9100 select 10nsec marker period, set scope to 10nSec/division. Check SIG_OUT (Ch1) period on the Oscilloscope is 10nsec.

Increase the Oscilloscope time base and 9100 period settings together by decades up to 1sec. At each decade check the Oscilloscope displays 10 cycles of signal on Ch1.

(This test can also be made using a counter. Increase the 9100 period settings by decades up to 10msec. At each decade check the counter displays between 99.99975 and 100.0025 for each setting. This should be done at least once in the sequence; the 100µsec point is recommended.)

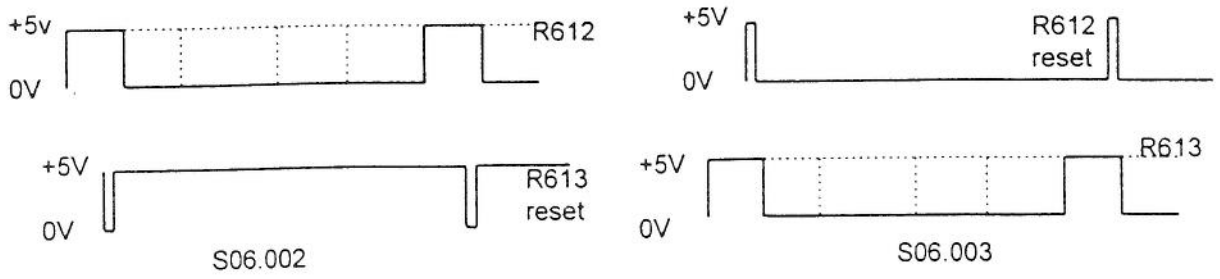
10.0 DDS Phase lock loop components

If option 100 is ***not*** fitted:-

10.1 Call up pathway S06.002 (This tests U801 and U601 and will pass if Y601 is < ±25ppm).

With a scope set to 2V/div, 20µsec/div check on R612/614junction and R613616 junction that one"active" waveform grows and collapses, and the other waveform is a narrow reset pulse.

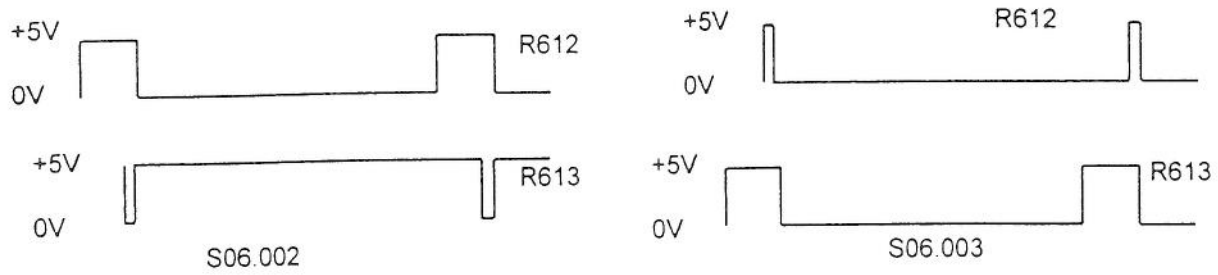
Note in waveforms below that "active" is the section before the narrow reset pulse; the reset pulse may be of the order of 50nsec, and difficult to see.



10.2 Select S06.003. (This tests U801 and U601 and will pass if Y601 is < ±25ppm). Check that the moving waveform is on the opposite channel of the scope. Should this check fail, refer to the relevant section in the Appendix.

If option 100 ***is*** fitted:-

10.3 Call up pathway S06.002. Check with a scope set to 5V/div, 20µsec/div on R612 and R613 that the waveforms are steady. This means that the "active" should be constant with only slight modulation in the width seen, and the other channel should have very short reset pulses.



10.4 Call up pathway S06.003. Check with a scope on R612 and R613 that the "active" has moved to the opposite channel and is still steady.

11.0 PLL Synthesiser Adjustment

11.1 Connect DMM to TP302 (D307(k)) wrt 0V. Select pathway S03.002. Adjust R303 fully cw. Using test link item 11 clipped to the +5V suppply, momentarily touch the probe to the LHS of C434/426. (The circuit should latch with o/p frequency up to 100MHz). Check the DMM reads 2.4V to 2.9V. Adjust R303 slowly ccw until the DVM suddenly goes more positive by nominally 0.4V to 0.5V. Note the reading, A.

Further ccw adjustment will now make the DVM decrease its reading. Continue with ccw adjustment until the DVM reading decreases by a further 0.1V.

Press REMEASURE, and ensure the self test passes with factory limits, with an error between -95% and +75%).

Touch the probe of item 11 to the LHS of C434/426 again, observing the new DVM reading.

Check the DVM reading increases by at least 0.2V when the probe is removed.

11.2 Connect an Oscilloscope Ch 1 to TL403 or TP404 and Ch 2 to TL404 or TP405. Set the scope to 5V/div, 10usec/div.

Check the scope displays waveforms similar to those in section 9 above. "Active" must occupy less than 50% of the total period.

11.3 Select "next test" S03.003 (250MHz). Check for + 7.0 to +7.6Vdc on the DMM (ensure self test passes with error of +/- 40% at factory limits).

Set scope timebase to 0.5µsec/div. Check the scope displays waveforms similar to those above. "Active" must occupy less than 50% of the total period.

11.4 If the above tests fail, due to VCO imbalance, swop the VCOs around and repeat section 11.

11.5 Transfer the DVM to TP 403 and check it reads -1.25V to -2.0V.

12.0 Off Key Signal and On LED.

12.1 The on LED can be turned on from power, analog or scope assemblies. Disconnect 50Ω load from SIG_OUT, select AUX, DCV and turn the o/p ON.

Check that the output LED is on continuously. Increase output to 32.000V and check output LED is on continuously. Increase output to 33.000V and check output LED flashes on and off once per second.

12.2 Connect a 10MΩ probe on the scope Ch1 to pin 48 of U801 on the scope board. (Pin 48 is 6 in from the RH front corner of U801). Set scope to 2V/division, 50msec/div and trigger from LINE or free run. Turn the o/p OFF and check that it pulses low for approximately 30ms.

12.3 Push the o/p OFF key again and check that no pulse occurs.

13.0 Levelling Loop Checks for DDS and PLL Section

13.1 Connect SIG_OUT to the 'scope Ch1. Set the 9100 to AUX, SINE, 5.5V, 11.1MHz, Ωload =50ohm and the scope Ch1 to 50Ω 1V/div and 0.1μsec/div. Turn the o/p ON.

The Oscilloscope should display 5.25V to 5.75V pk-pk with no obvious oscillations or aberrations.

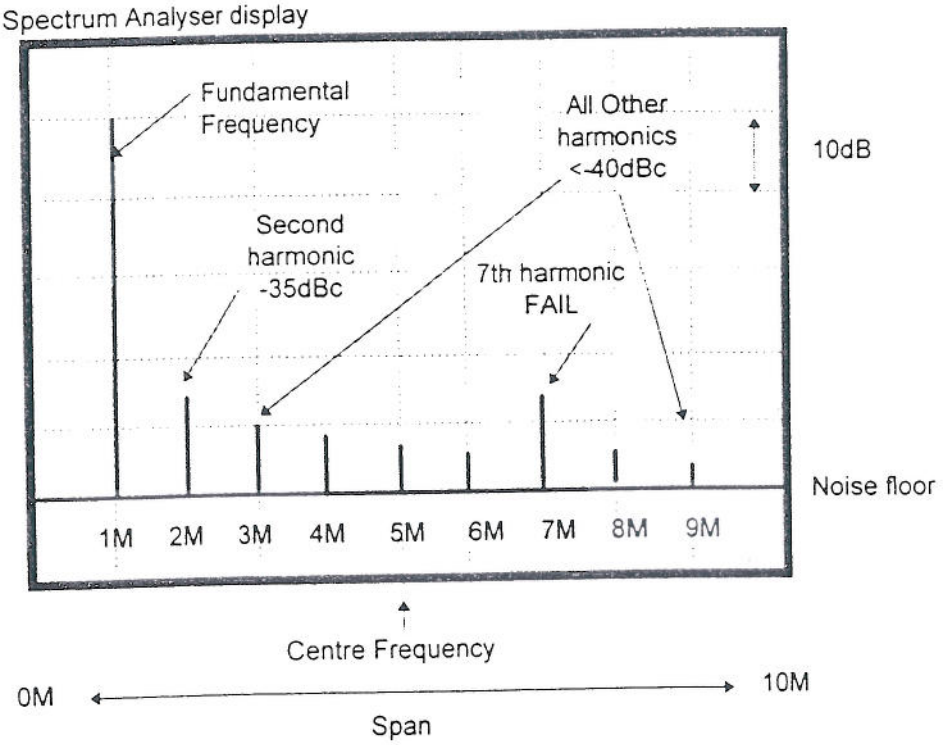
Recheck at 11.3MHz, 50MHz, 100MHz, 150MHz, 200MHz and 250MHz checking waveform cosmetics at each point. At 250 MHz, the output may have dropped to 5.00V if the UUT is uncalibrated.

13.2 Repeat with RF millivoltmeter replacing the Oscilloscope . The correct uncalibrated level should be between +18.5dBm and +19.1dBm up to 150 MHz. Some 1.0dB roll-off (10%) at 250MHz wrt 11.3MHz is to be expected in the uncalibrated state.

14.0 Harmonic Distortion and Spurii

14.1 In the following test, where possible set the spectrum analyzer for a centre frequency equal to 5 X times the 9100 output frequency with a span equal to 10 X times the 9100 output frequency. The reference (fundamental) is then 1 graticule division in from the left. (see diagram).

Example of Spectrum Analyser display



13.2 Connect SIG_OUT to a spectrum analyser and set the 9100 to SINE, 50KHz, 5.56V o/p ON. Check that the second harmonic is lower than minus 35dBc and all other harmonics lower than minus 40dBc at frequencies of 50kHz, 5MHz, 11.199MHz, 11.200MHz, 50MHz,100MHz and 250MHz. Non-harmonic spurii should be lower than minus 45dBc.

15.0 Attenuator VSWR.

15.1 Select AUX, SINE, 2V, Ωload=50Ω. Connect the output of the scope option to the delay line I/P, connect the mismatch to the delayline O/P, then connect the RF millivolt meter to the mismatch O/P.
Connect a 1281 to the analogue O/P of the millivolt meter and set it to the 10V DC range.

15.2 Set 232MHz on the 9100 and turn the O/P on. Increase the frequency by 10MHz in 1MHz steps to get a maximum reading on the 1281.
Press MATH CONFIG C LAST RDG ENTER Z LAST RDG ENTER MATH /Z -C %.

15.3 Set the frequency to 236MHz and increase by 14MHz in 1MHz steps to get the largest negative reading on the 1281. This should not exceed -7%.
Press MATH on the 1281 to reset all maths functions.

15.4 Repeat steps 15.2 to 15.3 for output amplitude of 900mV.

15.5 Repeat steps 15.2 to 15.3 for output amplitude of 300mV.

15.6 Repeat steps 15.2 to 15.3 for output amplitude of 100mV.

15.7 Repeat steps 15.2 to 15.3 for output amplitude of 30mV.

15.8 Repeat steps 15.2 to 15.3 for output amplitude of 20mV.

Appendix:-

Self Test Descriptions for 9100 'Scope Option.

The table below summarises the available tests. Following this is further description where the complexity of the test merits it. As previous practice, the test number attempts to locate by circuit sheet the location of all or most of the circuitry under test. Follow the pathway for each Self Test using the marked-up circuit diagrams labelled S07.001 to S02.002. There may be more than one circuit diagram per pathway or more than one pathway per circuit diagram.

TP403 voltage limits (the output of the Self Test on the Analogue Board) are those which would be expected in practice, and are usually equal to or tighter than the factory limit as set by the firmware. Information on the screen of the instrument is not repeated here.

Limits on the screen are sometimes mathematically calculated back to the source under test, so a technician has the volts at the start and the end of the test chain. This is always true for power supplies. Note that TP403 is inverted WRT to the origination point, and has a gain of 2, 1, ÷2 or ÷5. relative to TP 401.

TEST NUMBER	TEST DESCRIPTION	TP403 VOLTAGE LIMITS
S07.001	0v via U701/4 to establish earth problems.	-4mV to +4mV
S05.001	+12V Supply ÷ 2 , Self test ÷ 5	-1.28 to -1.12
S03.001	Oscillator +12V. Switched in by SLP2_H. Supply ÷ 2, Self test ÷ 5	-1.26 to -1.06
S05.002	+9V via U701/7 Self test ÷ 5	-1.85 to -1.61
S05.003	-9V via U701/12 Self test ÷ 5	1.61 to 1.85
S06.001	VCXOscillator +5V. Switched in by SLP1_H. Self test ÷ 5	-1.04 to -0.96
S05.004	MSB of U501 Self test ÷ 2 for all U501 tests	-1.69 to -1.59
S05.005	2SB of U501	-.847 to -.791
S05.006	3SB of U501	-.425 to -.393
S05.007	4SB of U501	-.214 to -.195
S05.008	5SB of U501	-.109 to -.096
S05.009	6SB of U501	-.056 to -.046
S05.010	7SB of U501	-.030 to -.021
S05.011	8SB of U501	-.016 to -.008
S05.012	All bits off, U501	-.003 to +.003
S04.005	HF amp Bias control -6 to -3 volts Self test ÷ 5	0.65 to 1.15
S06.002	VCXOsc. +33 ppm phase lock volts control. Self Test ÷5	-.96 to -.44
S06.003	VCXOsc. -33 ppm phase lock volts control. Self Test ÷5	-.56 to -.06
S04.001	DDS Amplitude control, max. Self Test gain =1	-2.3 to -2.0
S04.002	DDs Amplitude control, min. 8dB checks.	-1.35 to -1.15
S03.002	11.21 MHz HF Sine Phase Lock Loop control volts at lowest frequency. Self test ÷ 5	-.95 to -.35
S03.003	250 MHz HF Sine Phase Lock Loop control volts at highest frequency. Self test ÷ 5	-2 to -1.2
S04.003	15MHz HF Sine PIN diode amplitude control range at max amplitude. Self Test ÷ 5.	0.15 to 0.30
S04.004	15MHz HF Sine PIN diode amplitude control range at min amplitude. Self Test ÷ 5. (Should be -0.05 wrt S04.003)	0.10 to 0.25
S01.001	32V range DC relay check at 7Volts K105 K101 K108 are used. Self Test ÷ 5	-1.08 to -.92
S01.002	4.44V range, with extras. K107, K102, K108 in use. Slf Tst ÷ 5.	-.396 to -.372
S01.003	0.745V range. K103 and K104 introduced. Self Test gain of one.	-.8 to -.69
S01.004	14 mV range. Maximum attenuation. Only K108 in use. Self Test gain of 2.	-35mV to -25mV
S02.001	High Edge Power Supply control	-1.3 to -0.9
S02.002	High Edge Sampling Circuit.	1.1 to 1.4

S03.001 PLL Sleep Mode

If this test fails first check the path as in the diagrams. As a further test, select AC, 1V 11.21 MHz. Connect DMM to either end of R305 or R311. Reduce demanded frequency to 11.199MHz and ensure +12Vdc disappears. It should return when 11.21MHz is demanded. (The self test does not check that the power supply can be switched off.)

S06.001 30MHz VCXO Sleep Mode

If this test fails first check the path as in the diagrams. As a further test, select AC, 1V 50.1KHz.. Connect DMM to TP601. Reduce demanded frequency to 49.900kHz and ensure +5V falls to zero. It should return when 50.100kHz is demanded. (The self test does not check that the power supply can be switched off.)

S04.005 Output Amplifier Bias Loop

Connect DMM to TP401 (Q403 emitter) wrt -15V and check for +0.95 to +1.05Vdc. Note that the lower level of 0.95V is subject to a future change and may then reduce to 0.50V). (If higher than this, switch off immediately to minimise further damage and repair fault). Repeat for TP402 (Q404 emitter).

Fault finding techniques involve removing a suspect transistor and measuring it out of circuit. The control loop can be checked by checking volts wrt -15V. (TP401+TP402) = R421/R422 junction; U402/6 should be -6 to -3V wrt 0V. More than a few mV across R447or R448 indicate Q401 or Q402 respectively broken.

S06.002/3 Phase lock loop of the Voltage Controlled Crystal Oscillator.

We deviate the o/p frequency ± 33 ppm and check the control volts going into the VCXO. The test should detect failures in the phase comparator U801 or its succeeding amplifier U601.

If option 100 is NOT fitted, these tests should not fail in the factory, even though there is no controllability. The customer limits are set wide so as to guarantee a pass under all circumstances.

When option 100 is fitted, the results can still give us an assurance that all is well. Maths tests can do this for us, but these cannot be done dependant on option. S06.002-S06.003 should give around 2 to 3 volts on the displayed results. The device fitted has a nominal ±160 ppm span for 5 volts in, and we test over half of that span. Only the difference of nominally 2V on TP604 can really be trusted to give an unambiguous pass result; there are circumstances where both tests can pass even though the phase locked loop is not working at all.

If the 'scope check fails, this is probably because the combined error of the two crystals in use (possibly 50ppm) exceeds the 33ppm called up by the test.

Check each crystal as follows, using test S06.003. The input freq, TP602 must be between 58.59033MHz and 58.59326MHz. If not, providing the power supplies are between 4.75 and 5.2V, replace the crystal Y701 on the analogue board.

Check on TP603 that the frequency is between 29.99925MHz and 30.00075MHz. If this fails, providing the power supplies are between 4.75 and 5.2V, replace Y601 on the scope board.

S04.001 DDS amplitude and frequency loops

This takes the biggest step of all in terms of introducing new bits into the loop.We use the main output amp, the diode detector and the error amplifier for the first time. Note these are also used later on. The DDS in the scope option is set to 51 KHz. This is applied to the main amp, producing 11V p-p and detected from J101-13 by the diode detector on the daughter board which works with/against the demand on U101/6.

The error amp U401amplifies the error voltage and produces a DC of -1 to -2 V which is used as the reference voltage into the DDS, via DDS_AMP_CTRL. This is the point which is checked by this test.

If it all falls over, sanity can be restored by forcing the volts on R604/C601 to about 1V. This gives the DDS a minimal input reference voltage. If it has a clock and has been given a count AC volts should appear along the L601 etc filter chain. This should at least allow the DDS and main amp to be eliminated as being seriously faulty.

S04.002 is similar to the above, but 8dB gain is added before the DDS and 8dB attenuation is added after it.

DDS Section Tests

The following section describes a brief instrument test procedure for the DDS loop.

Connect 50ohm 'scope to output socket at the rear of the UUT and set to 1V/division. Connect DMM to U606-6 wrt ground. Demand 5.56Vpk-pk at 50kHz and turn output ON. Check for a nominal 5.5Vpk-pk on the scope and check no obvious oscillations or aberrations. Repeat at 11.19MHz. .

Check the 8dB DDS attenuator by reducing demand to 2.45Vpk-pk and repeating the above 50kHz test. The RF millivoltmeter should read +11.4 to +12.0dBm.

Check the output frequency with a counter on the output. The reading should be stable, quiet, and within the error spec of the main DDS crystal Y601 (± 25ppm or 0.25ppm if option 100 fitted).

S03.002/3 Lock range of the HF sine phase locked loop.

The new components introduced are mainly on sheet 3 of DC401231. Many of these are bought in modules, including the two VCOs which are the main subject of these tests. The VCO control range is about 650MHz for 15 volts, so for 250 MHz the two tests are expected to give displayed results differing by about 5V. It is possible for the VCOs to be working perfectly, and for the test to fail if there is a break in the signal path causing the output to be low or zero up to Q301 em. Inductors with shorted turns are especially hard to find. Open circuits on U303 leads have also been seen.

The signal path to check is R307 - R313, then Y302/1. If these are both OK at around 750MHz U301/1 - U302/1 - C317 - C320should be checked. U303 should be acting as a ÷32 in frequency.

A further trick is to lift R310, thus breaking the control loop. Y302/3 can then be driven externally to a suitable voltage, around 3.5V, which should give a suitable low frequency for further investigation

Note that R303 needs to be carefully set up. See section 11 in the board test procedure.

S04.003/4. HF Sine Amplitude span

Many of the previous comments for S04.001/2 apply. See drawings attached. The first test sets 11.4 Volts at the SINE_AMP_OUT line, the second sets 1.6Volts. (Both p-p) The frequency is low so as to allow any 'scope to be used and minimise measurement problems. The HF output is not measurable, but the DC on the PIN_ATN_CTRL diode control line is 0V to -2V and can be checked by the self test.

(A PIN diode is a variable attenuator. As DC current through it increases, its AC resistance drops. The AC current must be less than the DC current. Placing two diodes back to back reduces distortion. The diodes must have the same DC current in each. R324 and R327 must therefore be the same value.

The signal at 15 MHz should be attenuated between Q301 and Q303. Barring opens or shorts, the most likely fault is the control of the PIN diodes. If the signal disappears between D305 and D306, bridging them with 330R between R324 and R329 will restore sanity.

The o/p of the main amp SINE_AMP_OUT should be 11v p/p in the first test. The amplifier was checked in test S04.001, as was the diode detector. S03.002/3 checked the VCO circuit.

S01.001 to 004 Relay switching.

Using the data on the circuit diagrams attached, trace through the signal paths to find the errors at the DC levels provided by the test.

On the 9100 select AUX, Square ZOUT=1 Mohm and use the oscilloscope set to 1msec/division to check that an output is obtained accurate to within ± 5% at 20mV, 100mV, 1V, 3V, 4V, 40v and 133.4V relative to 0V. Use direct entry on the 9100 to set the output level. In each case, verify that there is no overshoot on either edge of the waveform greater than one line thickness on the oscilloscope.

On the 9100 select SINE, 49.9KHz, 3V and 100V in turn and check the oscilloscope indicates correctly, ±5%

S02.001. High Edge power supply

The circuit is set going and the power supply must get to about -32V. The PS is effectively an inverting amplifier with gain of 6.8, so its input must be +5.5V when a diode drop is added to the measured point. If this fails and S02.002 passes, check out the chain U201/7, D215, R228, R240//R247, R239, R217. Oscillations on U202/6 and U202/6 at 1.4V indicate R228 low or R239, R247//R240 very high.

S02.002 High Edge Sampler

Same conditions as above. This time the actual o/p pulse, ÷ 12 is sampled, filtered and measured. If there is a fault in the sampler, both tests may fail. The daughter board may have a relay shorted, in which case several of the S01.XXX tests will also fail.

Summary table of Scope and UUT settings with expected Results

Note: a result followed by an asterix * indicates a DVM reading

Scope Settings							9100 UUT Settings				Results	
Test No.	Ch 1 from SIG_ OUT	Z in or 10x Probe	Ch 2 from TRG_ OUT	Z in or 10x Probe	Trig ±	Time base	Function	Level	Freq/ Period	Z out	Ch1 or DVM * min	Ch2 or DVM *max
3.1	2V	1M			+ Ch1	1msec	Edge	5V	1KHz	1M	7V	
3.2							Edge	5V	1KHz	1M	-0.2V*	0V*
3.3							Edge	12V	1KHz	1M	-30V*	-10V*
4.1	0.2V	50Ω	0.2V	50Ω	+Ch2	1µsec	Edge	1V	100KHz	50Ω	0.90V-1.02V	
4.2 & 4.3	0.2V	50Ω	0.2V	50Ω	+Ch2	1µsec	Edge	1V	100KHz	50Ω	Flat	
4.4& 4.5	0.2V	50Ω	0.2V	50Ω	+Ch2	0.1µsec	Edge	1V	1MHz	50Ω	Flat	
4.6& 4.7	0.2V	50Ω	0.2V	50Ω	+Ch2	1msec	Edge	1V	100Hz	50Ω	Flat	
4.8	0.1V	50Ω	0.2V	50Ω	+Ch2	10µsec	Edge	320mV	100KHz	50Ω	0.3V to 0.34V	
5.1	20mV	1M	0.2V	1M	+Ch1	200µsec	Square	80mV	Fixed	1M	75-85mV	
5.2	10V	1M	0.2V	1M	+Ch1	20µsec	Sine	80V	49.9KHz	1M	75-85V	
6.1	1V	50Ω	0.2V	50Ω	+Ch1	20µsec	Sine	3.3V	49.9KHz	50Ω	3.1V to 3.5V	
7.1							Sine	20V	49.9KHz	1M	9100	TRIP
7.2							Edge	20V	1KHz	1M	9100	TRIP
8.1 & 8.2	0.2V	1M	0.2V	50Ω	+Ch2	5msec	DC	1V		1M	0.95V to 1.05V	0.9-1.1V@ 14.7-16.6 msec
8.3	5mV	50Ω	0.2V	50Ω	+Ch2	10µsec	Sine	5mV	10Hz	50Ω	5mV	1V
8.4	5mV	50Ω	0.2V	50Ω	+Ch2	2µsec	Sine	5mV	49.9KHz	50Ω	5mV	1V
8.5	5mV	50Ω	0.2V	50Ω	+Ch2	2µsec	Sine	10.7mV	50KHz	50Ω	10.7mV	1V
8.6	5mV	50Ω	0.2V	50Ω	+Ch2	2µsec	Sine	15mV	50KHz	50Ω	15mV	1V
8.7	5mV	50Ω	0.2V	50Ω	+Ch2	10nsec	Sine	15mV	11.1MHz	50Ω	15mV	1V
8.8	5mV	50Ω	0.2V	50Ω	+Ch2	0.5µsec	Sine	15mV	11.3MHz	50Ω	15mV	1V
9.1	0.5v	50Ω	0.2v	50Ω	+Ch2	200µsec	Markers	1V	1msec	50Ω	1V	1V
9.2	0.5V	50Ω	0.2V	50Ω	+Ch2	20nsec	Markers	1V	8.9nsec	50Ω	1V	1V
9.3	0.5V	50Ω	0.2V	50Ω	+Ch2	20nsec	Markers	1V	8.8nsec	50Ω	1V	1V
9.4	0.5V	50Ω	0.2V	50Ω	+Ch2	10nsec to 1sec	Markers	1V	10nsec to 10msec	50Ω	1V, 10 cycles	1V
10.1	2V	Probe	2V	Probe	+Ch2	20µsec	S06.002				2V	2V
10.2	2V	Probe	2V	Probe	+Ch2	20µsec	S06.002				2V	2V
10.3	2V	Probe	2V	Probe	+Ch2	20µsec	S06.002				2V	2V
10.4	2V	Probe	2V	Probe	+Ch2	20µsec	S06.002				2V	2V
11.1							S03.002				2.95V*	3.15V*
11.2	2V	Probe	2V	Probe	+Ch2	10µsec	S03.002				4V	4V
11.3	2V	Probe	2V	Probe	+Ch2	0.5µsec	S03.003				4V 7V*	4V 7.6V*
12.2	2V	Probe			Line	10msec	o/p off				low pulse	
12.3	2V	Probe			Line	10msec	o/p off				no pulse	

13.1	1V	50Ω	0.2V	50Ω	+Ch2	0.05µsec 0.05µsec 20nsec 10nsec 10nsec 5nsec 5nsec	Sine	5.5V	11.1MHz 11.3MHz 50MHz 100 MHz 150MHz 200MHz 250MHz	50Ω	5.25to 5.75V to 4.75V	1V
15.3		Delay					Sine	2V	232MHz			-7%*
15.4		line					Sine	0.9V				-7%*
15.5							Sine	0.3V	to			-7%*
15.6		+					Sine	0.1V				-7%*
15.7		Mis-					Sine	30mV				-7%*
15.8		match					Sine	20mV	250MHz			-7%*

Expanded Self Test Descriptions for 9100 'Scope Option.

The table below summarises the tests. As previous practice. the test number attempts to locate by circuit sheet the location of all. most or the start of the circuitry under test.

TP403 voltage limits (the output of the Self Test on the Analogue Board) are those which would be expected in practice, and are usually equal to or tighter than the factory limit as set by the firmware. Information on the screen of the instrument is not repeated here.

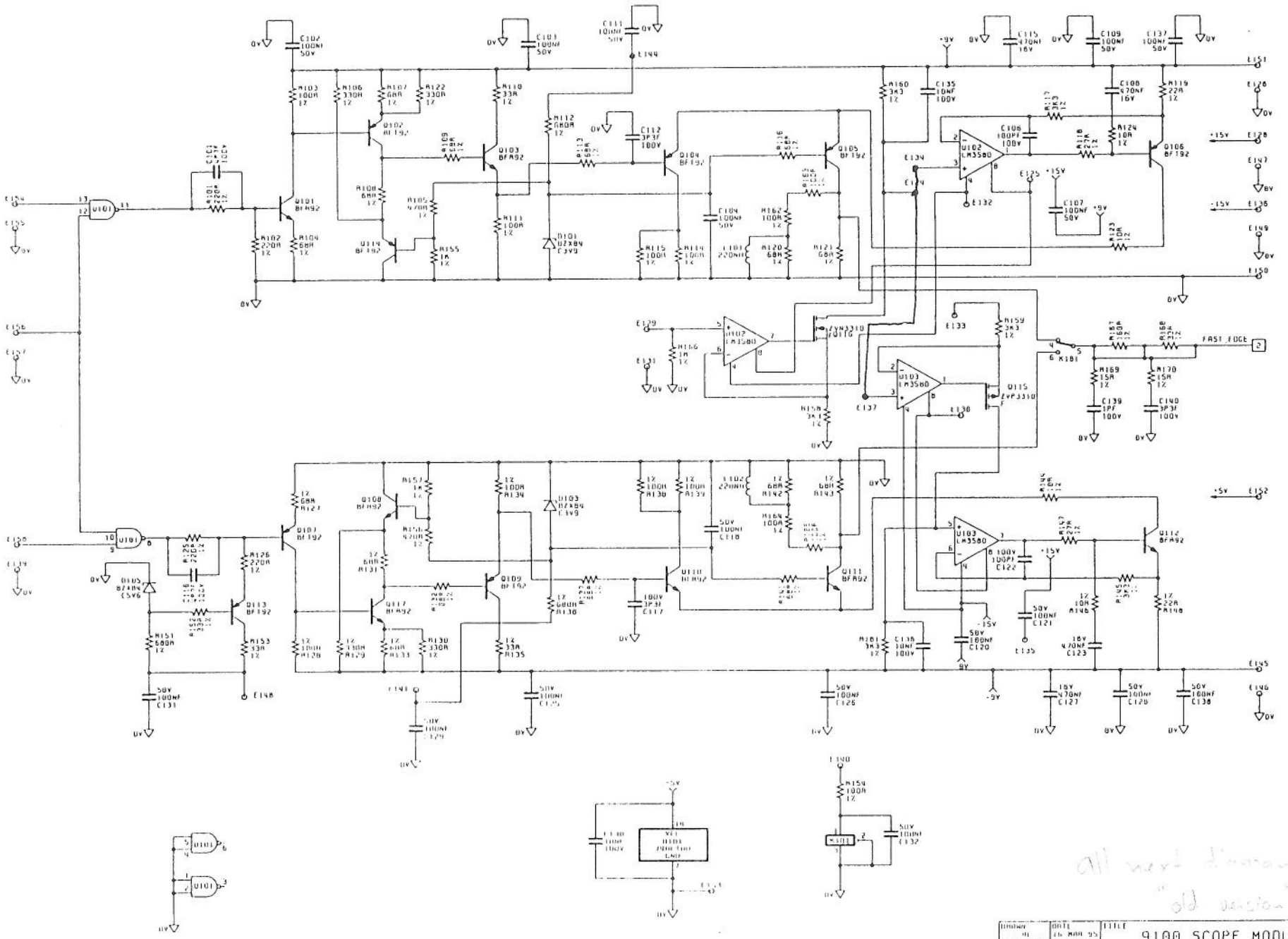
Limits on the screen are *sometimes* mathematically calculated back to the source under test. so a technician has the volts at the start and the end of the test chain. This is always true for power supplies. Note that TP403 is inverted WRT to the origination point. and has a gain of -2. -1, -0.5 or -0.2. relative to TP 401.

TEST NUMBER	TEST DESCRIPTION	POINTS ON PATH DC401231, # DC401097	TP403 VOLTAGE LIMITS
S07.001	0v via U701/4 to establish earth problems.	Chassis, U704/1. TST_OUT # TP401, U406 TP403 U408	-4mV to +4mV
S05.001	+12V Supply ÷ 2. Self test ÷ 5	+15v, U504. C505+ve. TT302,U701/5, # TP401 etc	-1.28 to -1.12
S03.001	Oscillator +12V. Switched in by SLP2_H. Supply ÷ 2. Self test ÷ 5	+12v, Q304. TP301, TT301. U701/6 # etc	-1.26 to -1.06
S05.002	+9V via U701/7 Self test ÷ 5	+15V, U505. C507.U701/7 # etc	-1.85 to -1.61
S05.003	-9V via U701/12 Self test ÷ 5	-15V. U506. C511, U701/12 # etc	1.61 to 1.85
S06.001	VCXOscillator +5V. Switched in by SLP1_H. Self test ÷ 5	+5V. Q501. TT601. U701/9 # etc	-1.04 to -0.96
S05.004	MSB of U501 Self test ÷ 2 for all U501 tests	U501, U502. U101.TT101.U702/7. # etc	-1.69 to -1.59
S05.005	2SB of U501	AS ABOVE	-.847 to -.791
S05.006	3SB of U501	AS ABOVE	-.425 to -.393
S05.007	4SB of U501	AS ABOVE	-.214 to -.195
S05.008	5SB of U501	AS ABOVE	-.109 to -.096
S05.009	6SB of U501	AS ABOVE	-.056 to -.046
S05.010	7SB of U501	AS ABOVE	-.030 to -.021
S05.011	8SB of U501	AS ABOVE	-.016 to -.008
S05.012	All bits off, U501 *The four LSBs are not tested*	AS ABOVE	-.003 to +.003
S04.005	HF amp Bias control -6 to -3 volts Self test ÷ 5	TP401&402. U402/2. TT402. U701/10. # etc Bias level set by R421,422	0.65 to 1.15

S06.002	VCXOsc. +33 ppm phase lock volts control. Valid only if option 100 fitted. Self Test ÷5	TP 602 =58.5918KHz U801/32=30.001MHz TP604, TT602 U702/4, # etc	-.96 to -.44
S06.003	VCXOsc. -33 ppm phase lock volts control. Valid only if option 100 fitted Diff=2V at TP604. Self Test ÷5	TP602 =58.5956KHz U801/32=29.999MHz TP604, TT602 U702/4, # etc	-.56 to -.06 Diff=0.4V
S04.001	DDS Amplitude control, max amplitude. Self Test gain =1	U807/8 is Low (IC ON). TP403, U702/6 # etc	-2.3 to -2.0
S04.002	DDS Amplitude control, min amplitude. 8dB attenuator checked.	U807 OFF. K601 OPERATED. TP403, U702/6 # etc	-1.35 to -1.15
S03.002	11.21 MHz HF Sine Phase Lock Loop control volts at lowest frequency. Self test ÷ 5	U405/6, U702/5 # etc	-.95 to -.35
S03.003	250 MHz HF Sine Phase Lock Loop control volts at highest frequency. Self test ÷ 5	U405/6, U702/5 # etc	-2 to -1.2
S04.003	15MHz HF Sine PIN diode amplitude control range at max amplitude. Self Test ÷ 5.	U405/6, Q405, Q406, ,TT401, U701/11 # etc	0.15 to 0.30
S04.004	15MHz HF Sine PIN diode amplitude control range at min. Self Test ÷ 5. (Should be -0.05V wrt S04.003)	U405/6, Q405, Q406, ,TT401, U701/11 # etc	0.10 to 0.25
S01.001	32V range DC relay check at Vin=7Volts K105 K101 K108 in use. TT102= Vin*(5/7) Self Test ÷ 5	HV_P_HI from DC401097,Relays K105 K101 K108, R115, R124, TT102, U702/12, # etc	-1.08 to -.92
S01.002	4.44V range, with extras. K107, K102, K108 in use. Vin=12.69V TT102= Vin*(1/6.6) Slf Tst ÷ 5	HV_P_HI from DC401097, K105, K107, K102, K108, R124, TT102, U702/12, # etc	-.396 to -.372
S01.003	0.745V range. Vin=29.68V K103 and K104 introduced. TT102= Vin*(1/39.84) Self Test gain of one.	HV_P_HI from DC401097, K105, K103, K104, K108, R124, TT102, U702/12, # etc	-.8 to -.69
S01.004	14 mV range. Vin= 29.4V Maximum attenuation, 1/2000 to TT102 Most relays OFF. Self Test gain of 2.	HV_P_HI from DC401097, K105, K108, R124, TT102, U702/12, # etc	-35mV to -25mV
S02.001	High Edge Power Supply control Self test ÷ 5	U202/6, TT201 (6V approx), U702/11, # etc	-1.3 to -0.9
S02.002	High Edge Sampling Circuit. Vout 30V squarewave is averaged and ÷12. Self test at unity gain.	Q203coll,(30Vsquare), R221 (1.25V), TT202, U702/10, # etc	1.1 to 1.4

DRAWING NO
DC401255

SS	CHANGES
1.0	ECO 4909 MEL 6456CO 21 AUG 95



all text & components "old version"

DRAWN	DATE	TITLE
ROH	22-8-95	9100 SCOPE MODULE DAUGHTER

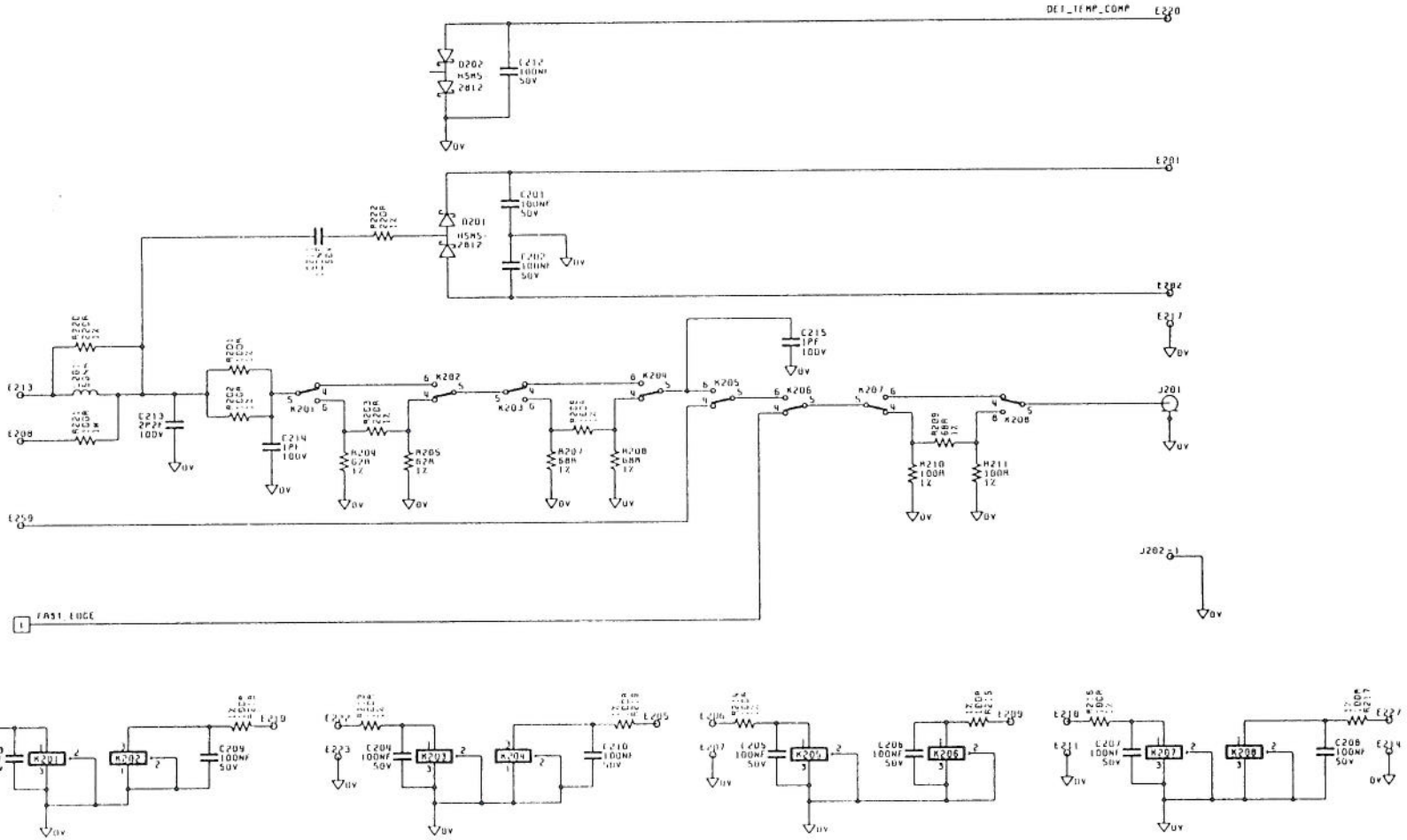
WAVETEK

DC401255

DRAWING NO
DC401255

ISS	CHANGES
..B	ECO 9909 RELEASED 21 AUG 95

31 AUG 1995



DESIGN	DATE 10 MAR 95	TITLE	9100 SCOPE MODULE DAUGHTER PCB ASSEMBLY
CHECK	DATE 22-8-95		

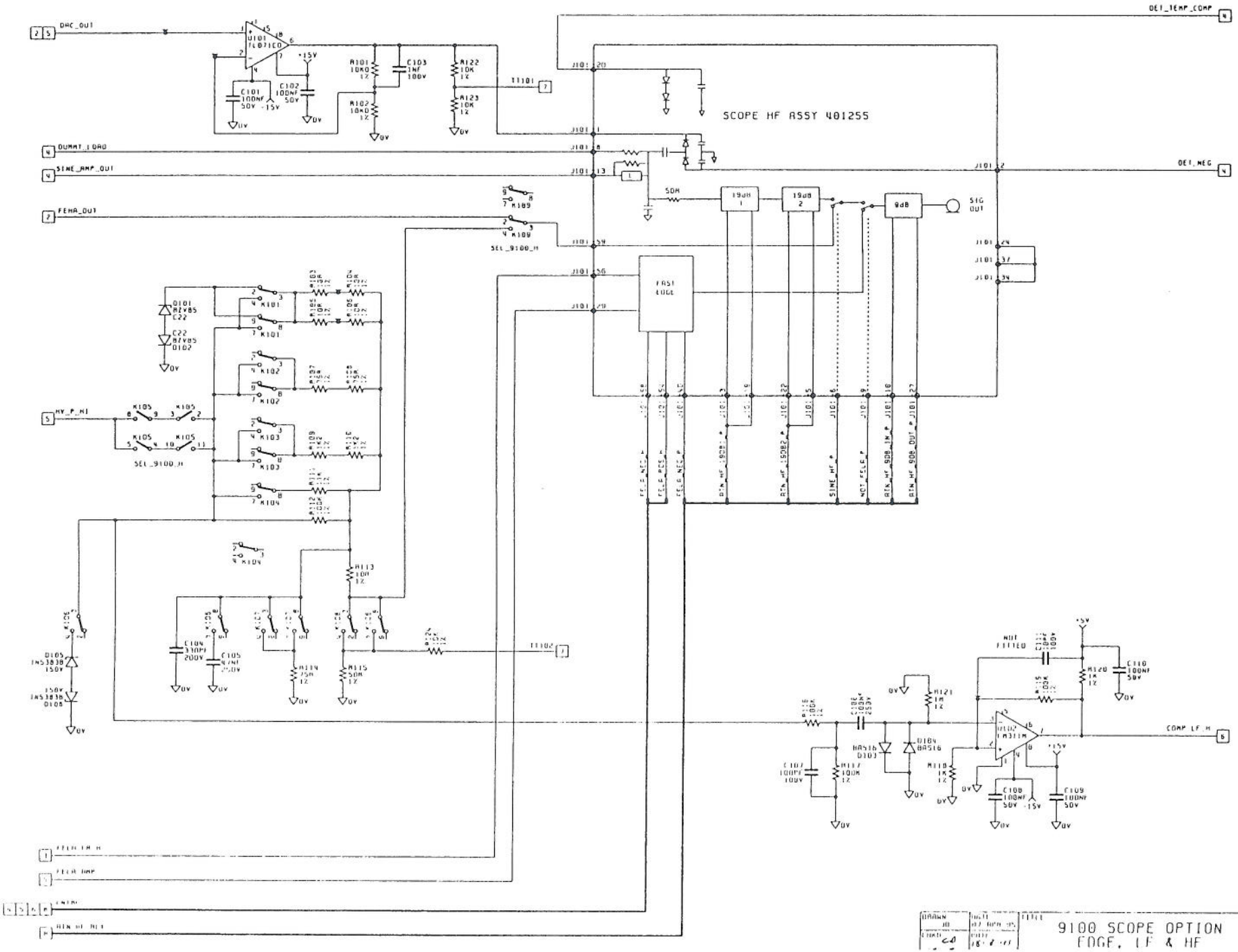
WAVETEK

DRAWING NO
DC401255

DRAWING NO
DC401231

SS	CHANGES
1.0	ECO 4309 RELEASED 18 AUG 85

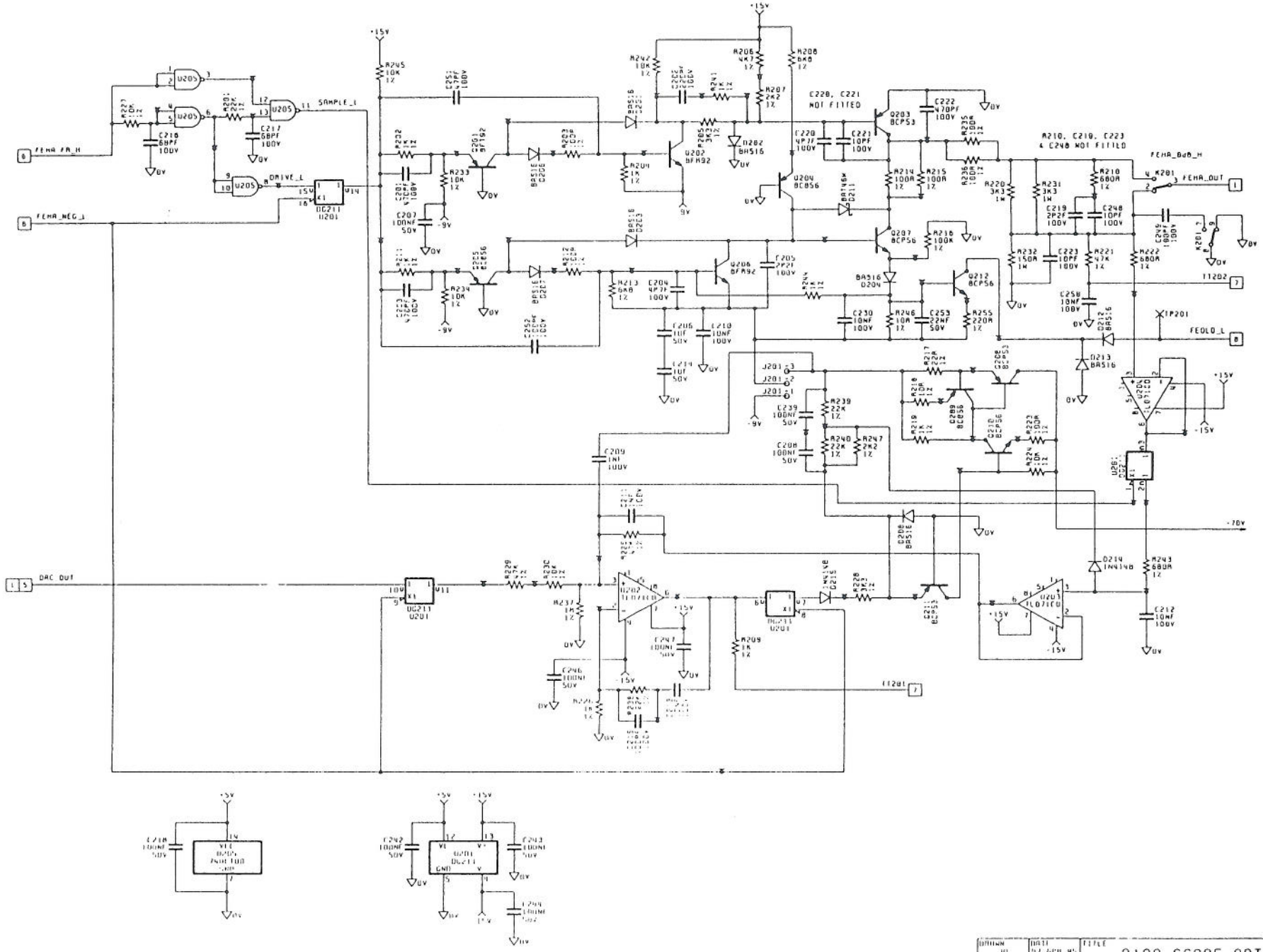
31 AUG 1995



DRAWING NO
0C401231

ISS	CHANGES
1.0	ECO 4709 RELEASED 18 AUG 95

3 1 AUG 1995



DRAWN	DATE	TITLE
JD	02 APR 95	9100 SCOPE OPTION HIGH EDGE
CHKD	DATE	

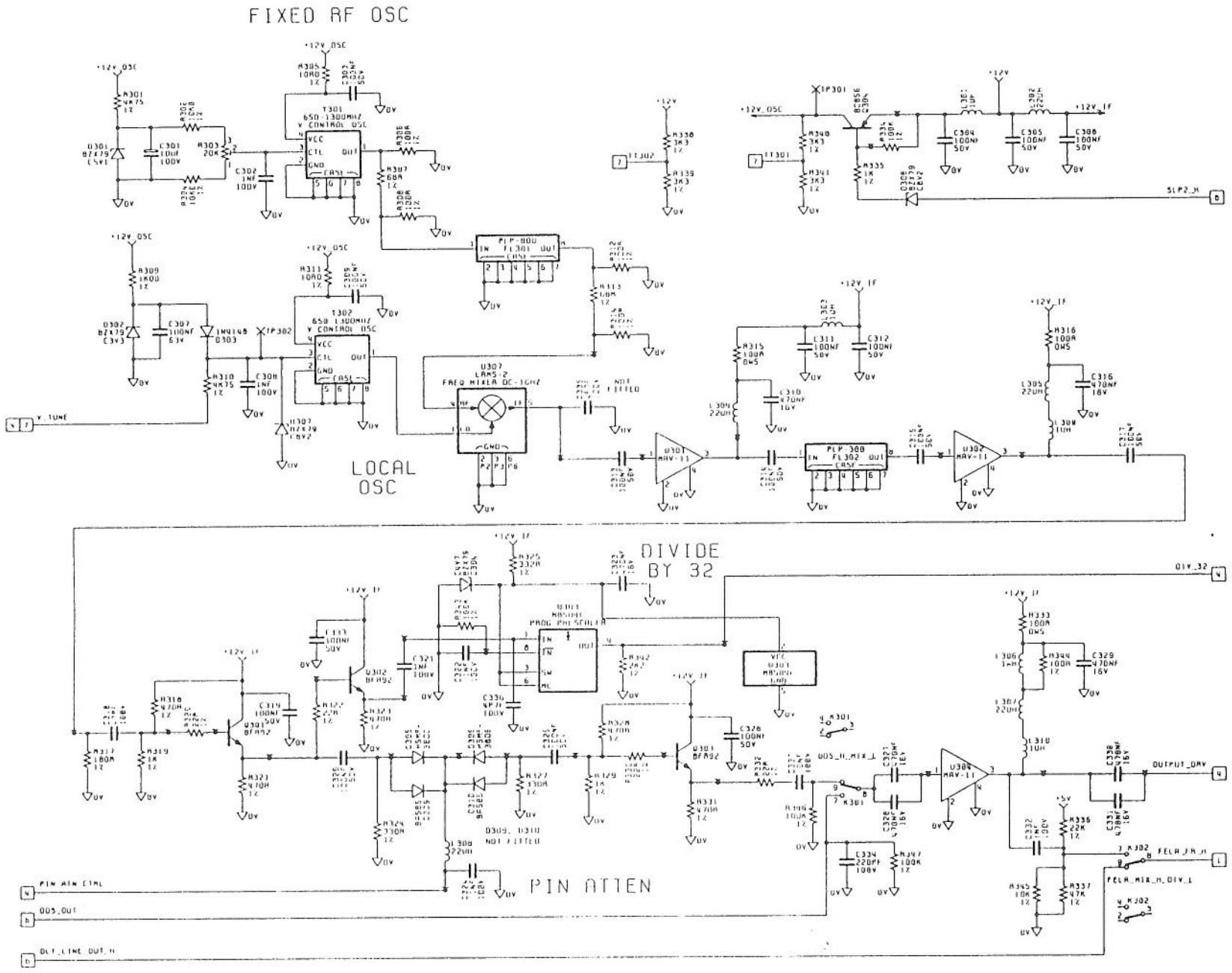
WAVETEK
SOMERSET, ENGLAND

DRAWING NO
0C401231

DRAWING NO
DC401231

	CHANGES
..0	ECO 4509 RELEASED 18 AUG 95
1.1	ECO 4563 C337, R346 & R347 ADDED TJL 20 SEP 95

21 SEP 1995

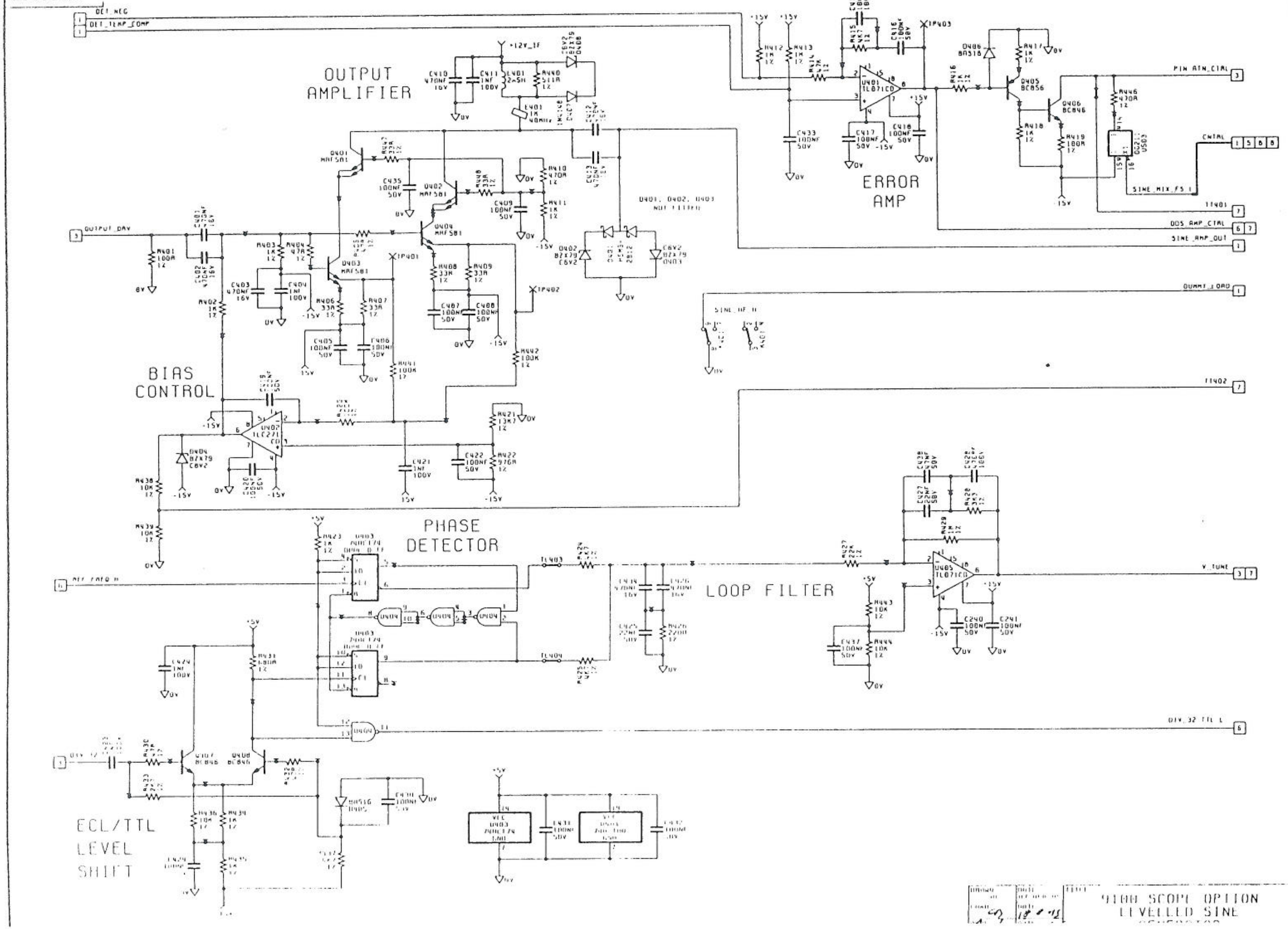


DRAWN JD	DATE 17 AUG 95	TITLE	9100 SCOPE OPTION LEVELLED SINE
CHKD TJL	DATE 18 AUG 95		

WAVETEK
WOKING, ENGLAND

DRAWING NO
DC401231

DRAWING NO
DC401231



CHANGES	
0	ECO 4909 RELEASED 18 AUG 95

3 1 AUG 1995

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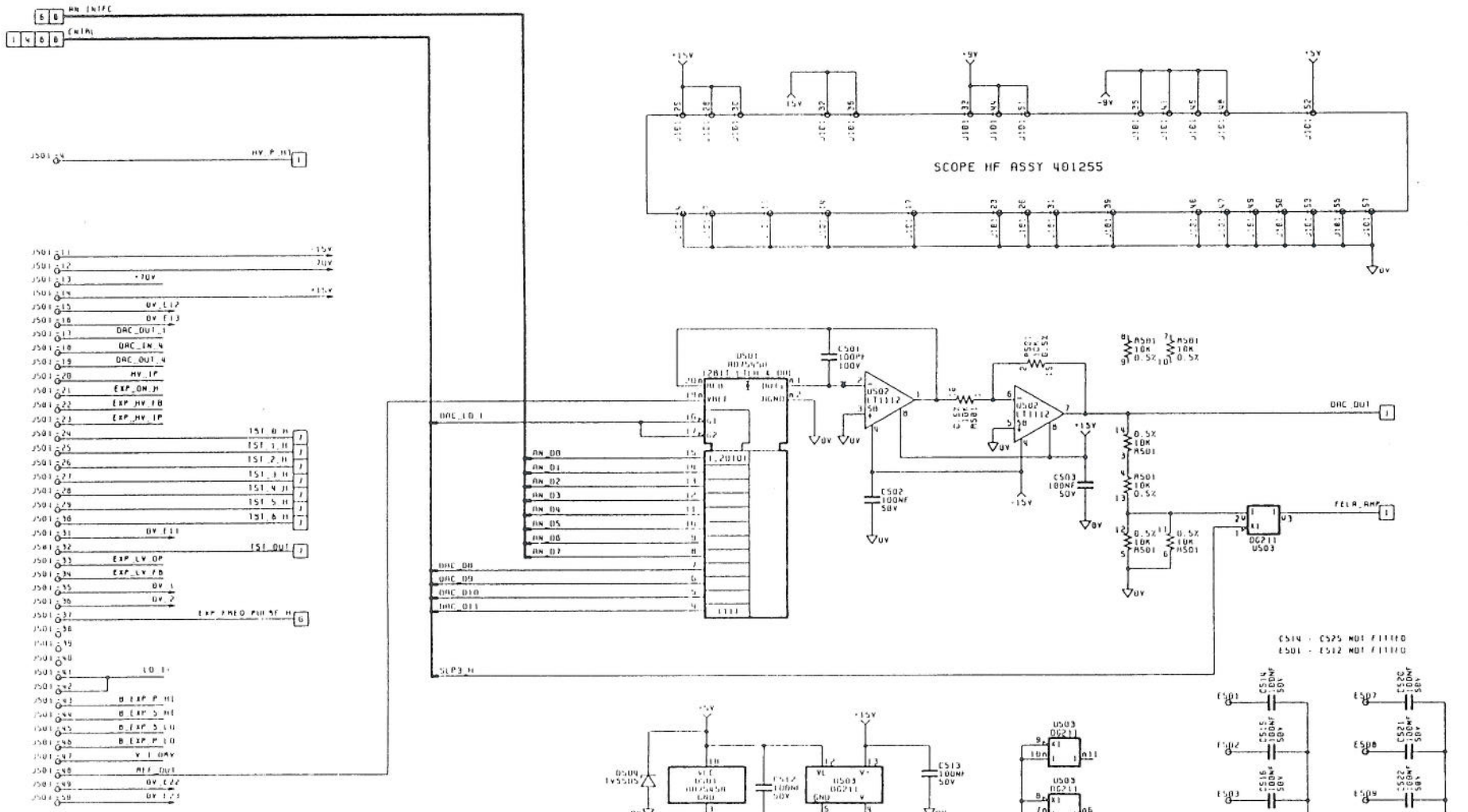
TITLE
9100 SCOPE OPTION
LEVELLED SINE

DRAWING NO
DC401231

DRAWING NO
DC401231

	CHANGES
H	ECO 4909 RELEASED 10 AUG 95

31 AUG 1995



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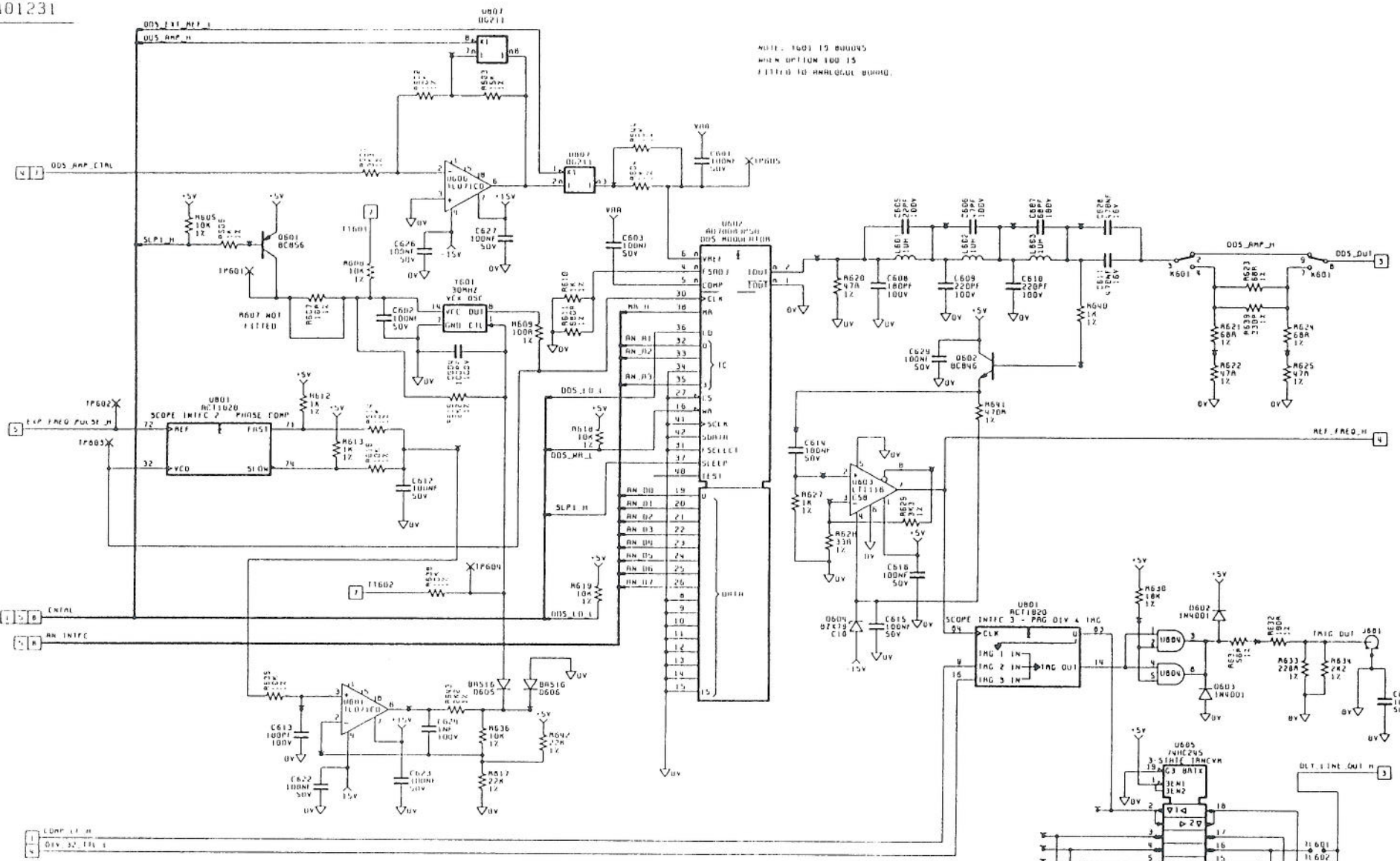
DRAWN	DATE 01 AUG 95	TITLE	9100 SCOPE OPTION 50 WAY CONN, AMPL CNTRL
CHKD	DATE 18/08/95		DRAWING NO DC401231

DRAWING NO
DC401231

SS	CHANGES
1.0	ECO 4909 REVERSED 18 AUG 95

31 AUG 1995

NOTE: T601 IS 800045 WHEN OPTION 100 IS FITTED TO ANALOGUE BOARD.



DRAWN	DATE 07 APR 95	TITLE 9100 SCOPE OPTION DDS, PLL REF
CHKD	DATE 18 AUG 95	

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SAN DIEGO, CA
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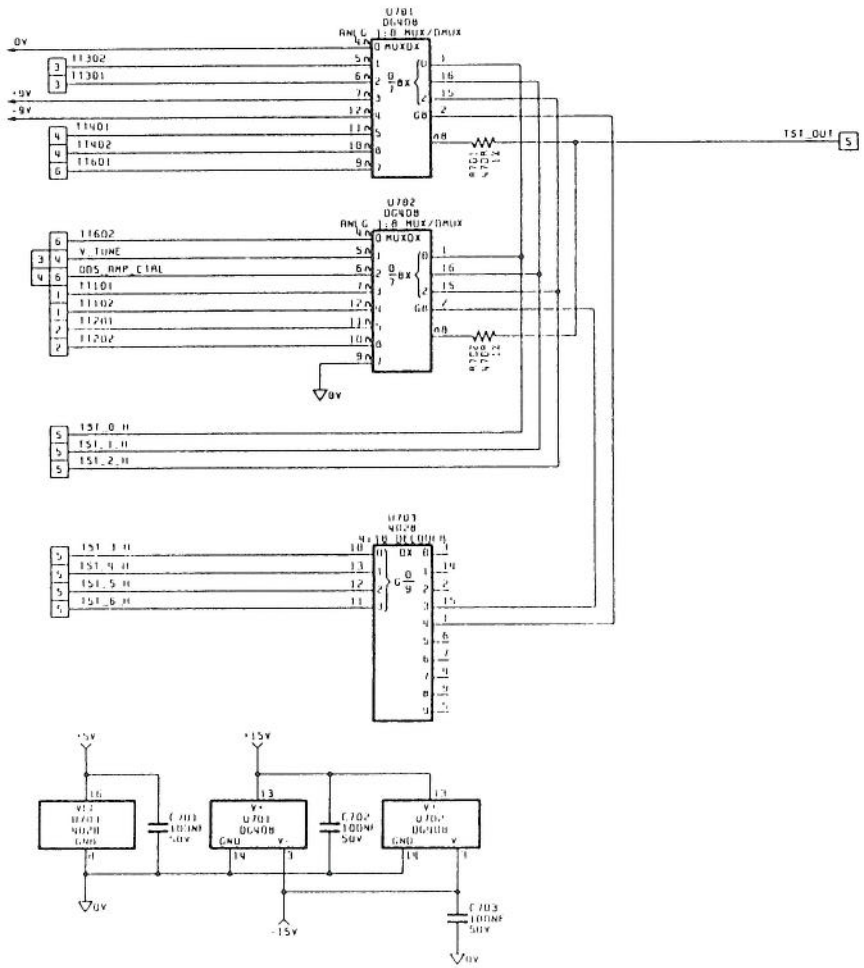
DRAWING NO
DC401231

DRAWING NO
DC401231



CHANGES	
1.0	ECO 4989 RELEASED 18 AUG 95

31 AUG 1995

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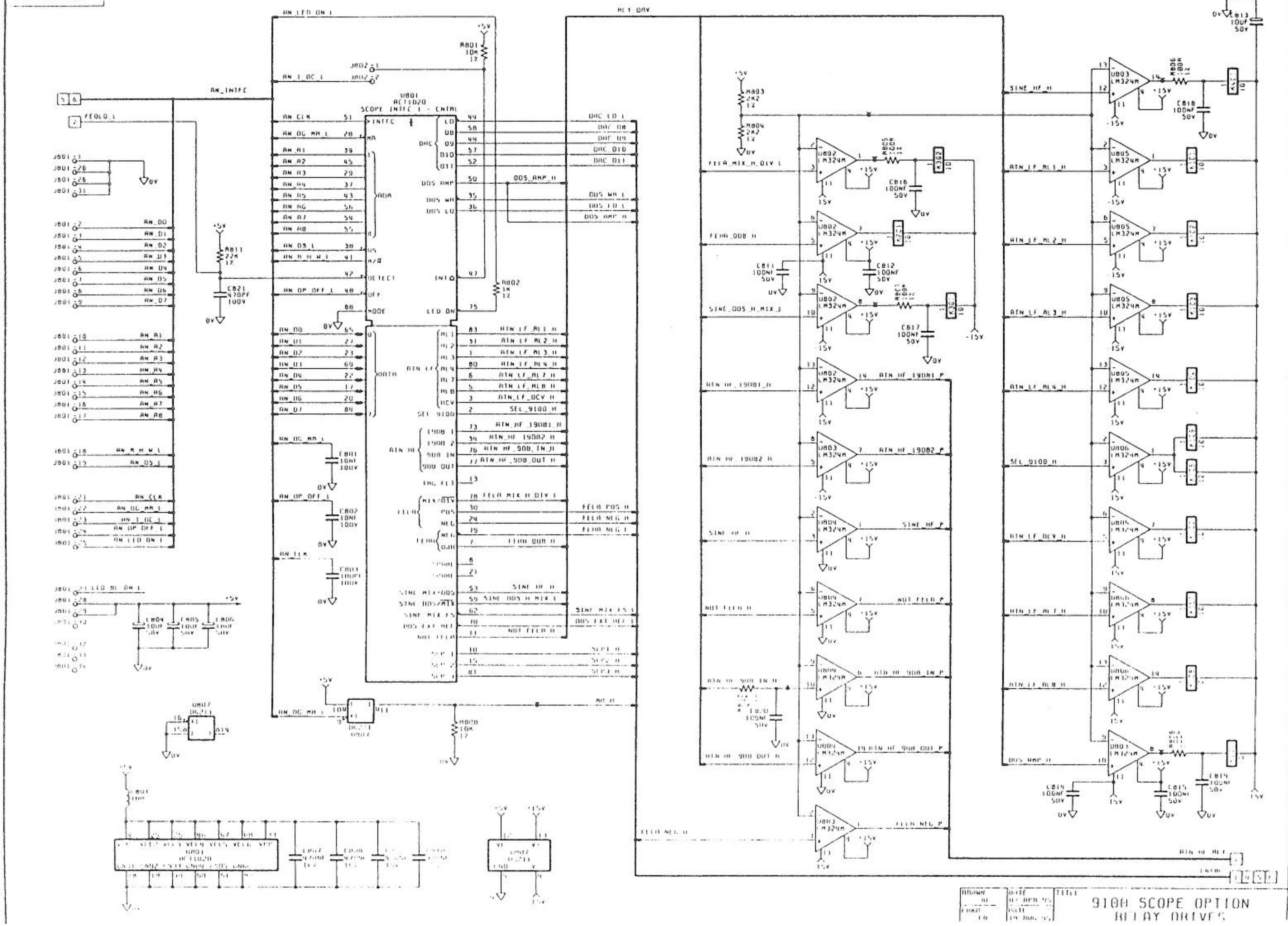
TITLE: 9100 SCOPE OPTION SELF TEST

DRAWING NO: DC401231

DRAWING NO DC401231



IS	CHANGES
1.0	ECO 4909 RELEASED 18 AUG 95
1.1	ECO 4931 C801/C802 WERE 180PF MJD 30 AUG 95

3 1 AUG 1995

WAVETEK

TITLE 9100 SCOPE OPTION RELAY DRIVES

DRAWING NO DC401231

9100 Scope Option - How it works.
DC, Square and Sine to 49.999KHz

These functions use the 9100 Hardware ranges listed below.(Column three). The waveshape for the square is changed so that it goes from zero to positive values. Care is therefore needed when measuring it! All scope option ranges are obtained by means of an internal attenuator, see sheet 1 of DC401231. The only thing to check is that the correct combination of resistors is switched in by the relays.

The table below refers to the connections made in each function. For fault finding purposes, the most useful tables are probably the ones headed **into external High Z (1 Mohm)**

The other tables will only give the correct attenuation if an external 50 ohm resistor is fitted.

Column one describes the maximum voltage into the attenuator on HV_P_HI assuming the machine is calibrated and all resistors are exact.

Column two gives the expected attenuation in dB. To convert to real numbers, divide the dB by 20 and hit 10^x on the calculator. This tells you the amount by which column one is divided., to give the value shown in Column four.

Col 5 is a reminder of the value of the load impedance required. Column 6, the attenuator resistance, is the total resistance expected between HV_P_HI and R113/Relay K108 junction. This is usually a parallel combination of R107 - R112 plus R113. R103 - R106 is for protection only, and is not an attenuator.

Column 7 is a reminder of the internal load, either nothing, 50 or 75 ohms, i.e. R114 or R115. One self test uses both. Column 8 is a list of relays which are closed for the given attenuation. Note that relay 2 in the table refers to K102 etc etc. The final column is the effective output impedance and has no faultfinding significance, except that if you load the output with this impedance you will halve the output volts and possibly overload the amplifiers!

Table 1a Ranges for LF Square, p-p to 3.336V into UUT 50 ohms

Vmax at Amplifier	Atten (dB)	9100 Hware	Vout max	Ext Load	Attenuator Resistance	Int Load	Relays Made
13.285	12.00	Square,	3.336	50	139.2+10	none	2 3 4
43.376	32.00	45Vrms	1.089	50	1932+10	none	3 4
29.30	45.99	90Vp-p	0.147	50	9900+10	none	4
44.44	66.02	note1	0.02222	50	100000+10	none	

Table 1b Ranges for LF Square, p-p to 133.4V into external High Z (1 Mohm)

Vmax at Amplifier	Atten (dB)	9100 Hware	Vout max	Ext Load	Attenuator Resistance	Int Load	Relays Made	Zout
> 133.44	0	Range1	133.44	UUT	40 + 10	none	1	50.0
44.44	0	Square,	44.44	UUT	40 + 10	none	1	50.0
12.68	9.11	45Vrms	4.444	UUT	150	75	2 7	48.74
13.285	12.00	90Vp-p	3.336	UUT	139.2 +10	50	2 3 4 8	37.45
43.376	32.00		1.089	UUT	1932+10	50	3 4 8	48.74
29.30	45.99		0.147	UUT	9900+10	50	4 8	49.97
44.44	66.02		0.02222	UUT	100000 +10	50	8	49.98

Table 1c Ranges for LF Sin, p-p to 5.56V into UUT 50 ohms

Vmax at Amplifier	Atten (dB)	9100 Hware	Vout max	Ext Load	Attenuator Resistance	Int Load	Relays Made
22.15	12.00	Sine,	5.56	50	139.2+10	none	2 3 4

88.52	32.00	32Vrms	2.222	50	1932+10	none	3 4
88.57	45.99	Vp-p	0.4444	50	9900+10	none	4
88.88	66.02		0.04444	50	100000+10	none	

Table 1d Ranges for LF Sin, p-p to 133.4V into external High Z (1 Mohm)

Vmax at Amplifier	Atten (dB)	9100 Hware	Vout max	Ext Load	Attenuator Resistance	Int Load	Relays Made	Zout
> 133.44	0	Sine 105V rms	133.44	UUT	40 + 10	none	1	50.0
88.88	0	Sine,	88.88	UUT	40 + 10	none	1	50.0
25.38	9.11	32Vrms	8.888	UUT	150	75	2 7	48.74
21.68	12.00	45Vp-p	5.444	UUT	139.2 +10	50	2 3 4 8	37.45
88.52	32.00		2.222	UUT	1932+10	50	3 4 8	48.74
88.57	45.99		0.4444	UUT	9900+10	50	4 8	49.97
88.88	66.02		0.04444	UUT	100000 +10	50	8	49.98

Table 1e Ranges for DC to 2.78V into UUT 50 ohms

Vmax at Amplifier	Atten (dB)	9100 Hware	Vout max	Ext Load	Attenuator Resistance	Int Load	Relays Made
11.07	12.00	DC	2.78	50	139.2+10	none	2 3 4
29.68	32.00	32V	0.745	50	1932+10	none	3 4
29.31	45.99		0.147	50	9900+10	none	4
29.4	66.02		0.0147	50	100000+10	none	

Table 1f Ranges forDC to 133.4V into external High Z (1 Mohm)

Vmax at Amplifier	Atten (dB)	9100 Hware	Vout max	Ext Load	Attenuator Resistance	Int Load	Relays Made	Zout
>133.44	0	DC 320V	133.44	UUT	40 + 10	none	1 6	50.0
32.0	0	DC	32.0	UUT	40 + 10	none	1	50.0
12.69	9.11	32V	4.444	UUT	150	75	2 7	48.74
10.83	12.00		2.72	UUT	139.2 +10	50	2 3 4 8	37.45
29.68	32.00		0.745	UUT	1932+10	50	3 4 8	48.74
29.31	45.99		0.147	UUT	9900+10	50	4 8	49.97
29.4	66.02		0.0147	UUT	100000 +10	50	8	49.98

D102 and D102 are for protection purposes only. If a user forgets to connect his external 50 ohms, he might get a zap. These therfore limit the maximum o/p to 22Volts

U102 and its associated bits are a comparator which drives the trigger circuit. It is AC coupled so that the square wave will drive it properly. R116 and D103, D104 protect it. C107 is an HF noise killer and R119/ R118 provide 50mV of hysterisis on early boards. This is far too much at the lowest levels of signal and was reduced to 2mV by changing R118 downwards.

Levelled Sine Generator : Circuit Description

Overview.

These circuits provide sinewave outputs from 50kHz to 250MHz at levels ranging from 20mV to 5.5V peak-to-peak. Frequencies are referred back to an onboard crystal (or to the high-accuracy crystal if this option is fitted), while pk-pk amplitude is referred back to an onboard DAC driven by the main instrument reference. User frequency demands are loaded into the DDS increment register while amplitude demands are loaded into the DAC. For all frequencies, output amplitude is controlled by a pk-pk diode detector situated at the output of the final amplifier stage. Two distinct systems are used to generate the range of output frequency required.

1) 50kHz to 11.199MHz

These frequencies are generated directly by a DDS/Filter arrangement and passed to the output amplifier at approx 0.5V pk-pk. Amplitude levelling is achieved by "pulling" the DC reference voltage of the DDS according to the output of the pk-pk detector (via a "slow" integrator/error-amp). Clock frequency to the DDS is fixed at 30MHz. An "all-in-one" DDS device is used which contains all circuitry except the output load resistor and LPF.

2) 11.2MHz to 250MHz

For this band, the DDS provides a reference frequency of 1/32 of the requested output frequency to a PLL synthesiser (after squaring by a fast comparator). Amplitude of the DDS is preset by fixing the DC reference input to it. The frequency synthesiser operates on a heterodyne principle as follows :-

A VCO running between approx 750MHz and 1GHz is mixed with a fixed oscillator running at approx 750MHz. The difference frequency is selected from the mixer output by a 300MHz LPF and amplified to the correct level to drive the output amplifier (approx 0.5V pk-pk). This IF signal passes through a PIN diode attenuator controlled by the levelling loop and also the IF signal is buffered off to drive a divide-by-32 ECL prescaler, the output of the prescaler driving the "variable" input of the PLL phase detector. Output of the phase detector passes through a LPF/error amp and drives the tuning port of the variable oscillator. A diode clamp prevents the variable oscillator frequency being pulled below the fixed oscillator frequency (this would cause the PLL to latch up if it were to occur). When not in use, the two UHF oscillators are "slept" by removing their power supplies.

Output Amplifier.

A discrete output stage is used consisting of parallel-connected cascode RF transistors running in class-A, bias being controlled by a slow integrating error amp circuit

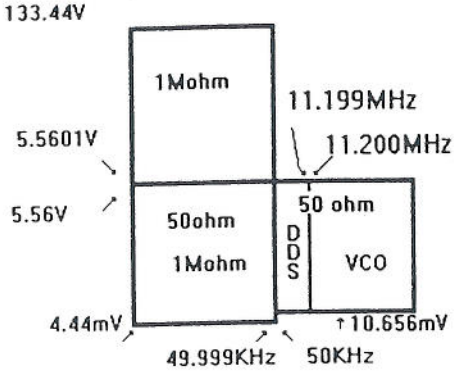
which stabilises the standing current at about 120mA. A LPF follows the output stage and is necessary to meet the harmonic distortion spec at the upper end of the frequency range. The pk-pk detector monitors the output node of this filter and thus levels the input to the final attenuator chain located on the daughter PCB.

Table 2 HF Sine ranges and Voltages

Attenuation dB	Nom Vout minimum	Nom Vout maximum	Actual Vout minimum	Actual Vout calib'n volts	Actual Vout maximum
00.00	0.805	5.700	1.0667V	2.5000V	5.5600V
9.66	0.264	1.87	0.3337V	0.9000V	1.0666V
19.04	0.09	0.636	0.1334V	0.3150V	0.3336V
28.7	0.0295	0.209	44.441mV	0.1000V	0.1333V
35.37	0.0137	0.0971	22.221mV	32.500mV	44.440mV
45.03	0.0045	0.0319	10.656mV	22.000mV	22.220mV

Notes: Zout is always 50 ohms, Zload is 50 ohms or 50Ohm terminator in parallel with UUT Zload.

Fig 1 Sine Volts Hertz Profile



9100 Scope Calibrator Board Test Procedure

Equipment required

1.0 9100 scope cal test rig TE268 or TE 269
2.0 1281 DVM
3.0 Oscilloscope 350MHz (min) with 50ohm input. Preferably analogue type.
4.0 Frequency counter Dana 8130 TE13
5.0 50ohm through terminator Suhner 6701-01-B TExxxx
6.0 50ohm through terminator Greenpar B35X13E999X99 TExxxx
7.0 Delay Line and Mismatch TE1565 and TE1564
8.0 RF millivoltmeter eg Boonton model 92E or similar
9.0 3.5 digit handheld DMM (or better).
10.0 Spectrum Analyser 50kHz to 1GHz (min).
11.0 1KΩ Test link with hook at one end and probe point at other end.
12.0 100K Test Probe, 0.2 inch tip separation

Abbreviations used

w.r.t. = with respect to
ESD = Electrostatic Discharge
I.C.T. = In Circuit Test
Ωload= Press horizontal soft key on 9100 used to change Zout of the 9100.

Notes

1.0 All faults found and their fixes should be listed on the I.C.T. test record sheet.
2.0 Observe ESD precautions throughout these tests.
3.0 As this assembly uses Surface Mount Technology any rework must be carried out by a rework operator trained in Surface Mount rework.
4.0 Scope settings are a guide and may require slight variation with board and operator preference.

Preliminary

1.0 Check visually for solder splashes, open circuits, missing components and/or orientation errors.
2.0 Check regulator heatsinks are fitted parallel; they are connected to raw power supplies and must not touch each other.
3.0 Check all relevant ECO's have been correctly implemented.
4.0 Ensure a handbag link is fitted between J201 pins 1and 2. (Pin 1 is at front)
5.0 Set the RF oscillator frequency adjustment R303 to mid-scale.
6.0 Ensure switch 7 on the rear is UP.

1.0 Procedure

1.1 Fit the unit under test to the 9100 scope cal test rig and connect four cables (output,trigger, 34way IDC,50way IDC)+ one ground strap.

Ensure the heatsink plate above Q401-4 is correctly fitted with regard to ECO issue and tightness. There must be good metal to metal contact to the standoff underneath, with adequate heat sink compound.

Switch on and hold in the centre button below the display (this disables power on self test) until the logo disappears.
Check immediately for overheating components.
Note that the output transistors Q401,402,403,404 do run quite hot (heat sink)

2.0 Self test

2.1 Select Mode, Test, enter the password (741258), then press the upper vertical soft key to enable factory limits and press the second from the top vertical soft key to enable scope cal tests.

A small *f* and **s** should appear in the lower right corner of the display to indicate that the factory limits and scope cal tests are selected. Run Full scope selftest.

2.2 At least one of S02.001 and S02.002 should fail, if there are any other fails, investigate and rectify before proceeding further. See appendix for self test descriptions and test details.

3.0 High (100nsec) Edge.

3.1 Tests S02.001 and S02.002 may fail due to the link position of J201, which permits only a fixed 9V power supply. Connect SIG-OUT to an Oscilloscope Ch1 set to 1MΩ 2V/div, 1msec/div. Trigger from Ch1. On the 9100 UUT select AUX, EDGE, Ωload=1MΩ, 5V, 1msec, o/p ON.

If a 7V square waveform appears, then the pulse circuit is probably OK. If the UUT trips out, investigate the current limit circuitry.

3.2 Using a DVM, check that J201/3 is between 28 and 38V wrt D504 anode. (=0V reference point).

3.3 Increase the demanded output of the 9100 to 12V at 1KHz (=1msec) and check that the DVM reads between --62V and -73V.

{If these tests fail, check the path U204/6, (0.5V squarewave), U201/2, U203/6(-0.5V DC) is correct. Otherwise, check out U202, which under the above two conditions should try to swing rail to rail, negative for the 5V demand and positive for the 12V demand. The only other fault may be U205, which produces delayed versions of the input DLY_LINE_OUT_H. The correct delay is of the order of 300nsec}.

3.4 Turn the 9100 o/p OFF, and move the link on J201.

Manually repeat self tests S02.001 and S02.002 and ensure a pass is obtained. If not, refer to appendix.

4.0 Low (1nsec) Edge.

4.1 Connect SIG-OUT to an Oscilloscope, Ch1 set to 50Ω 0.2V/div, 10µsec/div. Connect TRIG_OUT to Ch2 set to 0.2V/div via a 50Ω terminator (item 6) or select 50Ω on the Ch2 input if available. Set the scope to trigger from Ch2. (Do not display Ch2). Set the 9100 to AUX, EDGE, (rising) Ωload=50Ω, 1V, o/p ON. The scope trace should be a -ve 100KHz square wave of 0.90V to 1.02V.

(If the scope can't be triggered, it will be necessary to trigger from Ch1 until the trigger is fixed in section 8. Note that unless otherwise stated, Ch2 is used as described here to provide a consistent trigger throughout the whole of this test procedure).

4.2 Set scope to 1µsec/div. Check that the negative voltage level is flat to within 20mV.

4.3 Set the edge to Falling by pressing the horizontal EDGE TYPE softkey. Set scope to 10µsec/div. The scope trace should be a +ve 100KHz square wave of 0.90V to 1.02V.
Set scope to 1µsec/div. Check that the positive voltage level is flat to within 20mV.

4.4 Set the frequency to 1MHz. Set scope to 0.1µsec/div.
Check that the positive voltage level is flat to within 20mV.

4.5 Set the edge to Rising by pressing the EDGE TYPE softkey
Check that the negative voltage level is flat to within 20mV.

4.6 Set the frequency to 100Hz. Set scope to 1msec/div.
Check that the negative voltage level is flat to within 20mV.

4.7 Set the edge to Falling by pressing the horizontal EDGE TYPE softkey.
Check that the positive voltage level is flat to within 20mV.

4.8 Set the edge to Rising by pressing the EDGE TYPE softkey
Set the 9100 to 320mV, 100KHz. Set scope Ch1 to 0.1V/div, timebase 10µsec/div.
Check the O/P level is 300mV to 340mV. Turn 9100 OFF.

5.0 Amplitude functions.

5.1 On the 9100 select AUX, SQUARE, ΩLoad=1 MΩ. Use direct entry on the 9100 to set the output level to 80mV. Connect SIG_OUT to scope Ch1 set to 20mV/div, 1MΩ, timebase=200µsec/div. Turn 9100 o/p ON. Check that an output of 75 to 85mV is obtained.
Check there is no overshoot on either waveform edge greater than one line thickness on the scope.

5.2 Set the scope to 5V/div, 20µsec/div. On the 9100 select SINE, 49.9KHz, Ωload =1MΩ, 40V.
Check the oscilloscope indicates 37 to 43V. Turn 9100 OFF

6.0 50 ohm outputs.

6.1 Reduce the output on the 9100 to 3.3V, select Ωload=50Ω, o/p ON. Fit the terminator item 6 to SIG_OUT. **Do not** use the internal 50Ω of the scope! Set the scope to 1V/div.
Check for 3.1 to 3.5V on the Oscilloscope. Turn 9100 o/p OFF. Leave the 50Ω load connected.

7.0 Overload protection.

7.1 Set the 9100 to SINE, 49.9KHz, 1MΩ, 20V, turn the o/p ON, and check that the output is immediately tripped OFF. If it doesn't trip, turn it off as quickly as possible and investigate the fault, probably on the 9100 power amp overload; detector not functioning.

7.2 Select EDGE, Ωload=1MΩ, 20V, 1KHz. Turn 9100 ON. If the output trips off, perhaps after a few seconds, no further action is required. If the o/p does not trip off, touch probe item 12 between Q208 collector tab and Q212 emitter. (nearest lead to Q208collector tab). A second touch should result in a system trip.

8.0 Trigger Outputs.

8.1 Connect SIG_OUT to a scope Ch 1, 1MΩ set to 0.2V/div, 5msec/div and TRIG_OUT to Ch 2 set to 0.2V/div, 50Ω (moving terminator item 6 from Ch1 or using internal 50Ω on the Ch 2 input if available).

Set the scope to 10msec/division. Set scope to trigger from Ch2, and display Ch2.

On the 9100 select AUX, DCV, 1V, Ωload=1MΩ and turn the o/p ON.

Check scope Ch 1 indicates between 0.95 and 1.05V.

8.2 Check that TRIG_OUT logic signal, Ch2 has a period of 14.7 to 16.6mSec and is of amplitude between 0.9 and 1.1V.

8.3 On the 9100 select AUX, SINE, Ωload = 50Ω, 10KHz 5.0mV and turn o/p ON. Set scope Ch1 to 50Ω, 5mV/div, 10usec/div. The scope must be on CHOP vertical mode during this test, not ALT mode, unless the scope is digital.

Check TRIG_OUT logic signal Ch 2 is 0.9 to 1.1V wrt 0V and that the mark space is 45:55 or better ('high' for 4.5 divisions or greater).

Check Ch1 indicates between 4.8 and 6.0mV, (allowing for some noise) If there is some LF present, ensure both 9100 o/p leads go to the LEFT of the UUT. i.e. Do not put the scope on the RHS of the UUT.

Check Ch1 and Ch2 are synchronised at the same frequency.

8.4 Set scope to 2µsec/div. Return scope to ALT display. Set 9100 frequency to 49.9kHz and repeat the three checks of section 8.3 above.

8.5 On the 9100 select 10.7mV, 50.0kHz and turn output on.

Check TRIG_OUT logic signal is between 0.9 and 1.1Vpk wrt 0V (ignoring short duration overshoots) with a mark space of 35:65 or better ('high' for 3.5 divisions or greater).

Check Ch1 and Ch2 are synchronised at the same frequency.

8.6 Increase amplitude to 0.3337V and repeat the checks of section 8.5.

Set Ch1 to 1MΩ DC coupled, fit a 10x probe, touch scope Ch1 (displaying 50mV/div), to U603 pins 2 and 3 in turn. Use the VCO guard box for the probe earth connection.

Check the sine peaks exceed the square wave peak levels by at least 15mV.

Remove the probe and reconnect scope Ch1 set to 50Ω to the SIG o/p.

8.7 Set UUT frequency to 11.1MHz, scope to 10nsec/div, and repeat checks as in 8.5.

8.8 Set the scope to 0.5µsec/division. Set UUT frequency to 11.3MHz.

The trigger frequency should become 353.125kHz eg. period of 2.8µSec (output frequency/32). Note that there is only one positive trigger transition, at just past the centre of the 'scope display, and two negative transitions. (A further +ve transition may be seen at the extreme LHS of the scope display).

9.0 Timing Markers.

9.1 Connect scope Ch1 to SIG_OUT and set Ch1 to 0.5V/div, 50Ω, timebase 0.2msec/div. On the 9100 select AUX, TIMING MARKERS, (lowest RHS vertical soft key) 1ms, o/p ON.

Check that the TRIG_OUT signal has a period of 1ms.

9.2 Set scope timebase to 20nSec/division. On the 9100 select 8.9000nsec.

Check SIG_OUT (Ch1) is 0.9V to 1.1V peak signal wrt 0V with 30:70 to 45:55 mark/space. (the waveform may look like a half wave rectified sine; measure the mark from the base of the waveform.)

Check TRIG_OUT (Ch2) is 0.9V to 1.1v peak signal wrt 0V.

9.3 On the 9100 select 8.8000nsec and check SIG_OUT (Ch1) becomes 1Vpp sinewave.

9.4 On the 9100 select 10nsec marker period, set scope to 10nSec/division. Check SIG_OUT (Ch1) period on the Oscilloscope is 10nsec.

Increase the Oscilloscope time base and 9100 period settings together by decades up to 1sec. At each decade check the Oscilloscope displays 10 cycles of signal on Ch1.

(This test can also be made using a counter. Increase the 9100 period settings by decades up to 10msec. At each decade check the counter displays between 99.99975 and 100.0025 for each setting. This should be done at least once in the sequence; the 100µsec point is recommended.)

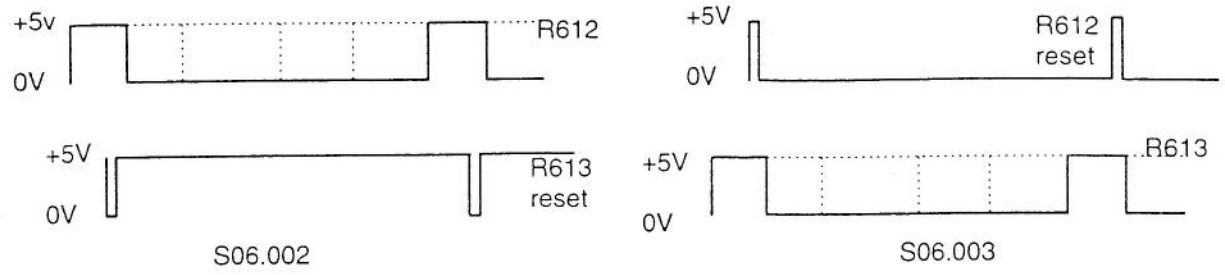
10.0 DDS Phase lock loop components

If option 100 is ***not*** fitted:-

10.1 Call up pathway S06.002 (This tests U801 and U601 and will pass if Y601 is < ±25ppm).

With a scope set to 2V/div, 20µsec/div check on R612/614junction and R613616 junction that one"active" waveform grows and collapses, and the other waveform is a narrow reset pulse.

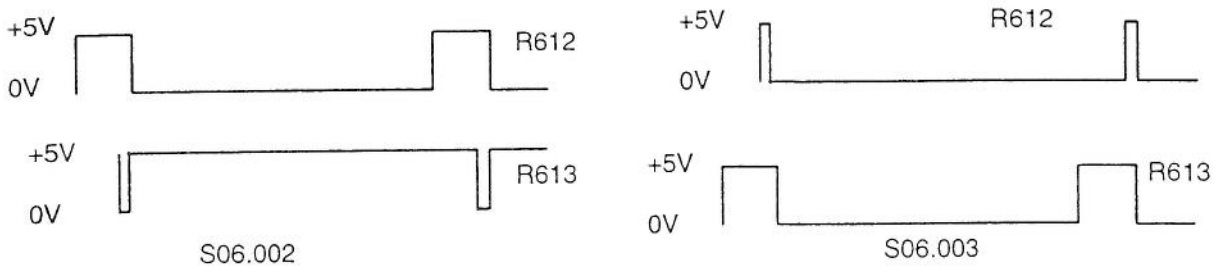
Note in waveforms below that "active" is the section before the narrow reset pulse; the reset pulse may be of the order of 50nsec, and difficult to see.



10.2 Select S06.003. (This tests U801 and U601 and will pass if Y601 is < ±25ppm). Check that the moving waveform is on the opposite channel of the scope. Should this check fail, refer to the relevant section in the Appendix.

If option 100 ***is*** fitted:-

10.3 Call up pathway S06.002. Check with a scope set to 5V/div, 20µsec/div on R612 and R613 that the waveforms are steady. This means that the "active" should be constant with only slight modulation in the width seen, and the other channel should have very short reset pulses.



10.4 Call up pathway S06.003. Check with a scope on R612 and R613 that the "active" has moved to the opposite channel and is still steady.

11.0 PLL Synthesiser Adjustment

11.1 Connect DMM to TP302 (D307(k)) wrt 0V. Select pathway S03.002. Adjust R303 fully cw. Using test link item 11 clipped to the +5V supply, momentarily touch the probe to the LHS of C434/426. (The circuit should latch with o/p frequency up to 100MHz). Check the DMM reads 2.4V to 2.9V. Adjust R303 slowly ccw until the DVM suddenly goes more positive by nominally 0.4V to 0.5V. Note the reading, A.

Further ccw adjustment will now make the DVM decrease its reading. Continue with ccw adjustment until the DVM reading has decreased from reading A by a further 0.1V.

Press REMEASURE, and ensure the self test passes factory limits, with error from -95% to +75%).

Touch the probe of item 11 to the LHS of C434/426 again, observing the new DVM reading.

Check the DVM reading increases by at least 0.2V when the probe is removed.

11.2 Connect an Oscilloscope Ch 1 to TL403 or TP404 and Ch 2 to TL404 or TP405. Set the scope to 5V/div, 10usec/div.

Check the scope displays waveforms similar to those in section 9 above. "Active" must occupy less than 50% of the total period.

11.3 Select "next test" S03.003 (250MHz). Check for + 7.0 to +7.6Vdc on the DMM (ensure self test passes with error of +/- 50% at factory limits).

Set scope timebase to 0.5µsec/div. Check the scope displays waveforms similar to those above. "Active" must occupy less than 50% of the total period.

11.4 If the above tests fail, due to VCO imbalance, swop the VCOs around and repeat section 11.

11.5 Transfer the DVM to TP 403. Check it reads -1.25V to -1.8V. (Checks 250MHz gain loop).

12.0 Off Key Signal and On LED.

12.1 The on LED can be turned on from power, analog or scope assemblies. Disconnect 50Ω load from SIG_OUT, select AUX, DCV and turn the o/p ON.

Check that the output LED is on continuously. Increase output to 32.000V and check output LED is on continuously. Increase output to 33.000V and check output LED flashes on and off once per second.

12.2 Connect a 10MΩ probe on the scope Ch1 to pin 48 of U801 on the scope board. (Pin 48 is 6 in from the RH front corner of U801). Set scope to 2V/division, 50msec/div and trigger from LINE or free run. Turn the o/p OFF and check that it pulses low for approximately 30ms.
12.3 Push the o/p OFF key again and check that no pulse occurs.

13.0 Levelling Loop Checks for DDS and PLL Section

13.1 Connect SIG_OUT to the 'scope Ch1. Set the 9100 to AUX, SINE, 5.5V, 11.1MHz, Ωload =50ohm and the scope Ch1 to 50Ω 1V/div and 0.1µsec/div. Turn the o/p ON.

The Oscilloscope should display 5.25V to 5.75V pk-pk with no obvious oscillations or aberrations.

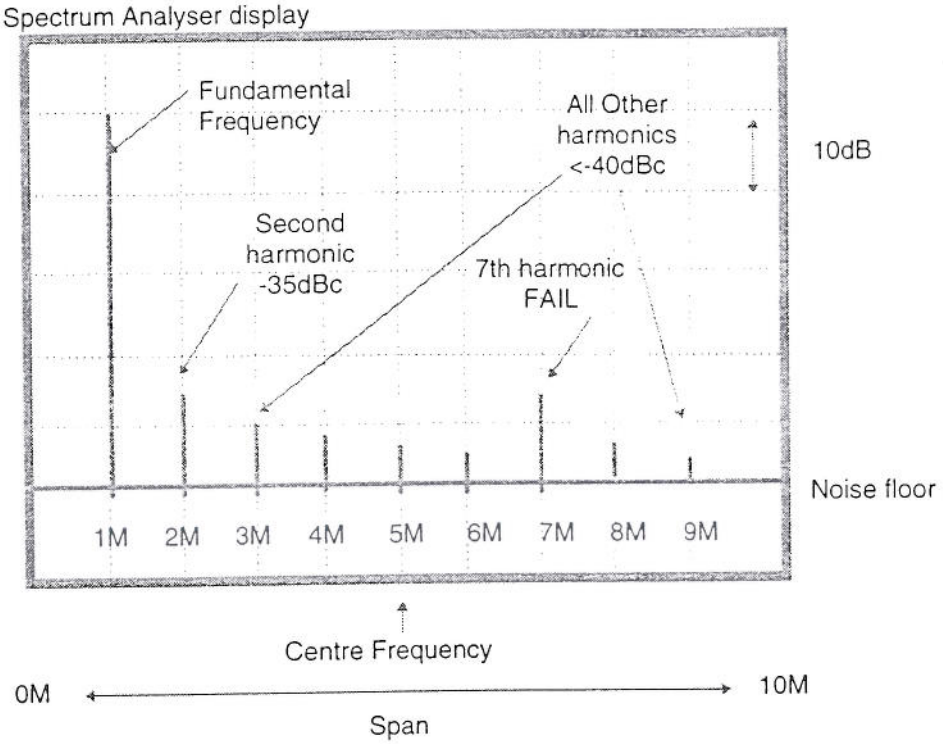
Recheck at 11.3MHz, 50MHz, 100MHz, 150MHz, 200MHz and 250MHz checking waveform cosmetics at each point. At 250 MHz, the output may have dropped to 5.00V if the UUT is uncalibrated.

13.2 Repeat with RF millivoltmeter replacing the Oscilloscope . The correct uncalibrated level should be between +18.5dBm and +19.1dBm up to 150 MHz. Some 1.0dB roll-off (10%) at 250MHz wrt 11.3MHz is to be expected in the uncalibrated state.

14.0 Harmonic Distortion and Spurii

14.1 In the following test, where possible set the spectrum analyzer for a centre frequency equal to 5 X times the 9100 output frequency with a span equal to 10 X times the 9100 output frequency. The reference (fundamental) is then 1 graticule division in from the left. (see diagram).

Example of Spectrum Analyser display



13.2 Connect SIG_OUT to a spectrum analyser and set the 9100 to SINE, 50KHz, 5.56V o/p ON. Check that the second harmonic is lower than minus 35dBc and all other harmonics lower than minus 40dBc at frequencies of 50kHz, 5MHz, 11.199MHz, 11.200MHz, 50MHz,100MHz and 250MHz. Non-harmonic spurii should be lower than minus 45dBc.

15.0 Attenuator VSWR.

15.1 Select AUX, SINE, 2V, Ωload=50Ω. Connect the output of the scope option to the delay line I/P, connect the mismatch to the delayline O/P, then connect the RF millivolt meter to the mismatch O/P.

Connect a 1281 to the analogue O/P of the millivolt meter and set it to the 10V DC range.

15.2 Set 232MHz on the 9100 and turn the O/P on. Increase the frequency by 10MHz in 1MHz steps to get a maximum reading on the 1281.

Press MATH CONFIG C LAST RDG ENTER Z LAST RDG ENTER MATH /Z -C %.

15.3 Set the frequency to 236MHz and increase by 14MHz in 1MHz steps to get the largest negative reading on the 1281. This should not exceed -7%.
Press MATH on the 1281 to reset all maths functions.

Appendix:-

Self Test Descriptions for 9100 'Scope Option.

The table below summarises the available tests. Following this is further description where the complexity of the test merits it. As previous practice, the test number attempts to locate by circuit sheet the location of all or most of the circuitry under test. Follow the pathway for each Self Test using the marked-up circuit diagrams labelled S07.001 to S02.002. There may be more than one circuit diagram per pathway or more than one pathway per circuit diagram.

TP403 voltage limits (the output of the Self Test on the Analogue Board) are those which would be expected in practice, and are usually equal to or tighter than the factory limit as set by the firmware. Information on the screen of the instrument is not repeated here.

Limits on the screen are sometimes mathematically calculated back to the source under test, so a technician has the volts at the start and the end of the test chain. This is always true for power supplies. Note that TP403 is inverted WRT to the origination point, and has a gain of 2, 1, ÷2 or ÷5. relative to TP 401.

TEST NUMBER	TEST DESCRIPTION	TP403 VOLTAGE LIMITS GUIDE
S07.001	0v via U701/4 to establish earth problems.	-4mV to +4mV
S05.001	+12V Supply ÷ 2 , Self test ÷ 5	-1.28 to -1.12
S03.001	Oscillator +12V. Switched in by SLP2_H. Supply ÷ 2, Self test ÷ 5	-1.26 to -1.06
S05.002	+9V via U701/7 Self test ÷ 5	-1.85 to -1.61
S05.003	-9V via U701/12 Self test ÷ 5	1.61 to 1.85
S06.001	VCXOscillator +5V. Switched in by SLP1_H. Self test ÷ 5	-1.04 to -0.96
S05.004	MSB of U501 Self test ÷ 2 for all U501 tests	-1.69 to -1.59
S05.005	2SB of U501	-.847 to -.791
S05.006	3SB of U501	-.425 to -.393
S05.007	4SB of U501	-.214 to -.195
S05.008	5SB of U501	-.109 to -.096
S05.009	6SB of U501	-.056 to -.046
S05.010	7SB of U501	-.030 to -.021
S05.011	8SB of U501	-.016 to -.008
S05.012	All bits off, U501	-.003 to +.003
S04.005	HF amp Bias control -6 to -3 volts Self test ÷ 5	0.65 to 1.15
S06.002	VCXOsc. +33 ppm phase lock volts control. Self Test ÷5	-.96 to -.44
S06.003	VCXOsc. -33 ppm phase lock volts control. Self Test ÷5	-.56 to -.06
S04.001	DDS Amplitude control, max. Self Test gain =1	-2.3 to -2.0
S04.002	DDs Amplitude control, min. 8dB checks.	-1.35 to -1.15
S03.002	11.21 MHz HF Sine Phase Lock Loop control volts at lowest frequency. Self test ÷ 5	-.95 to -.35
S03.003	250 MHz HF Sine Phase Lock Loop control volts at highest frequency. Self test ÷ 5	-2 to -1.2
S04.003	15MHz HF Sine PIN diode amplitude control range at max amplitude. Self Test ÷ 5.	0.15 to 0.30
S04.004	15MHz HF Sine PIN diode amplitude control range at min amplitude. Self Test ÷ 5. (Should be -0.05 wrt S04.003)	0.10 to 0.25
S01.001	32V range DC relay check at 7Volts K105 K101 K108 are used. Self Test ÷ 5	-1.08 to -.92
S01.002	4.44V range, with extras. K107, K102, K108 in use. Slf Tst ÷ 5.	-.396 to -.372
S01.003	0.745V range. K103 and K104 introduced. Self Test gain of one.	-.8 to -.69
S01.004	14 mV range. Maximum attenuation. Only K108 in use. Self Test gain of 2.	-35mV to -25mV
S02.001	High Edge Power Supply control	-1.3 to -0.9
S02.002	High Edge Sampling Circuit.	1.1 to 1.4

S03.001 PLL Sleep Mode

If this test fails first check the path as in the diagrams. As a further test, select AC, 1V 11.21 MHz. Connect DMM to either end of R305 or R311. Reduce demanded frequency to 11.199MHz and ensure +12Vdc disappears. It should return when 11.21MHz is demanded. (The self test does not check that the power supply can be switched off.)

S06.001 30MHz VCXO Sleep Mode

If this test fails first check the path as in the diagrams. As a further test, select AC, 1V 50.1KHz. Connect DMM to TP601. Reduce demanded frequency to 49.900kHz and ensure +5V falls to zero. It should return when 50.100kHz is demanded. (The self test does not check that the power supply can be switched off.)

S04.005 Output Amplifier Bias Loop

Connect DMM to TP401 (Q403 emitter) wrt -15V and check for +0.93 to +1.03Vdc. (If higher than this, switch off immediately to minimise further damage and repair fault). Repeat for TP402 (Q404 emitter). Note that this level varies down to approx 0.5V as o/p level demanded decreases.

Fault finding techniques involve removing a suspect transistor and measuring it out of circuit. The control loop can be checked by checking volts wrt -15V. (TP401+TP402) = R421/R422 junction; U402/6 should be -6 to -3V wrt 0V. More than a few mV across R447or R448 indicate Q401 or Q402 respectively broken.

S06.002/3 Phase lock loop of the Voltage Controlled Crystal Oscillator.

We deviate the o/p frequency ± 33 ppm and check the control volts going into the VCXO. The test should detect failures in the phase comparator U801 or its succeeding amplifier U601.

If option 100 is NOT fitted, these tests should not fail in the factory, even though there is no controllability. The customer limits are set wide so as to guarantee a pass under all circumstances.

When option 100 is fitted, the results can still give us an assurance that all is well. Maths tests can do this for us, but these cannot be done dependant on option. S06.002-S06.003 should give around 2 to 3 volts on the displayed results. The device fitted has a nominal ±160 ppm span for 5 volts in, and we test over half of that span. Only the difference of nominally 2V on TP604 can really be trusted to give an unambiguous pass result; there are circumstances where both tests can pass even though the phase locked loop is not working at all.

If the 'scope check fails, this is probably because the combined error of the two crystals in use (possibly 50ppm) exceeds the 33ppm called up by the test.

Check each crystal as follows, using test S06.003. The input freq, TP602 must be between 58.59033MHz and 58.59326MHz. If not, providing the power supplies are between 4.75 and 5.2V, replace the crystal Y701 on the analogue board.

Check on TP603 that the frequency is between 29.99925MHz and 30.00075MHz. If this fails, providing the power supplies are between 4.75 and 5.2V, replace Y601 on the scope board.

S04.001 DDS amplitude and frequency loops

This takes the biggest step of all in terms of introducing new bits into the loop.We use the main output amp, the diode detector and the error amplifier for the first time. Note these are also used later on. The DDS in the scope option is set to 51 KHz. This is applied to the main amp, producing 11V p-p and detected from J101-13 by the diode detector on the daughter board which works with/against the demand on U101/6.

The error amp U401amplifies the error voltage and produces a DC of -1 to -2 V which is used as the reference voltage into the DDS, via DDS_AMP_CTRL. This is the point which is checked by this test.

If it all falls over, sanity can be restored by forcing the volts on R604/C601 to about 1V. This gives the DDS a minimal input reference voltage. If it has a clock and has been given a count AC volts should appear along the L601 etc filter chain. This should at least allow the DDS and main amp to be eliminated as being seriously faulty.

S04.002 is similar to the above, but 8dB gain is added before the DDS and 8dB attenuation is added after it.

DDS Section Tests

The following section describes a brief instrument test procedure for the DDS loop.

Connect 50ohm 'scope to output socket at the rear of the UUT and set to 1V/division. Connect DMM to U606-6 wrt ground. Demand 5.56Vpk-pk at 50kHz and turn output ON. Check for a nominal 5.5Vpk-pk on the scope and check no obvious oscillations or aberrations. Repeat at 11.19MHz. .

Check the 8dB DDS attenuator by reducing demand to 2.45Vpk-pk and repeating the above 50kHz test. The RF millivoltmeter should read +11.4 to +12.0dBm.

Check the output frequency with a counter on the output. The reading should be stable, quiet, and within the error spec of the main DDS crystal Y601 (± 25ppm or 0.25ppm if option 100 fitted).

S03.002/3 Lock range of the HF sine phase locked loop.

The new components introduced are mainly on sheet 3 of DC401231. Many of these are bought in modules, including the two VCOs which are the main subject of these tests. The VCO control range is about 650MHz for 15 volts, so for 250 MHz the two tests are expected to give displayed results differing by about 5V. It is possible for the VCOs to be working perfectly, and for the test to fail if there is a break in the signal path causing the output to be low or zero up to Q301 em. Inductors with shorted turns are especially hard to find. Open circuits on U303 leads have also been seen.

The signal path to check is R307 - R313, then Y302/1. If these are both OK at around 750MHz U301/1 - U302/1 - C317 - C320should be checked. U303 should be acting as a ÷32 in frequency.

A further trick is to lift R310, thus breaking the control loop. Y302/3 can then be driven externally to a suitable voltage, around 3.5V, which should give a suitable low frequency for further investigation

Note that R303 needs to be carefully set up. See section 11 in the board test procedure.

S04.003/4. HF Sine Amplitude span

Many of the previous comments for S04.001/2 apply. See drawings attached. The first test sets 11.4 Volts at the SINE_AMP_OUT line, the second sets 1.6Volts. (Both p-p) The frequency is low so as to allow any 'scope to be used and minimise measurement problems. The HF output is not measurable, but the DC on the PIN_ATN_CTRL diode control line is 0V to -2V and can be checked by the self test.

(A PIN diode is a variable attenuator. As DC current through it increases, its AC resistance drops. The AC current must be less than the DC current. Placing two diodes back to back reduces distortion. The diodes must have the same DC current in each. R324 and R327 must therefore be the same value.

The signal at 15 MHz should be attenuated between Q301 and Q303. Barring opens or shorts, the most likely fault is the control of the PIN diodes. If the signal disappears between D305 and D306, bridging them with 330R between R324 and R329 will restore sanity.

The o/p of the main amp SINE_AMP_OUT should be 11v p/p in the first test. The amplifier was checked in test S04.001, as was the diode detector. S03.002/3 checked the VCO circuit.

S01.001 to 004 Relay switching.

Using the data on the circuit diagrams attached, trace through the signal paths to find the errors at the DC levels provided by the test.

On the 9100 select AUX, Square ZOUT=1 Mohm and use the oscilloscope set to 1msec/division to check that an output is obtained accurate to within ± 5% at 20mV, 100mV, 1V, 3V, 4V, 40v and 133.4V relative to 0V. Use direct entry on the 9100 to set the output level. In each case, verify that there is no overshoot on either edge of the waveform greater than one line thickness on the oscilloscope.

On the 9100 select SINE, 49.9KHz, 3V and 100V in turn and check the oscilloscope indicates correctly, ±5%

S02.001. High Edge power supply

The circuit is set going and the power supply must get to about -32V. The PS is effectively an inverting amplifier with gain of 6.8, so its input must be +5.5V when a diode drop is added to the measured point. If this fails and S02.002 passes, check out the chain U201/7, D215, R228, R240//R247, R239, R217. Oscillations on U202/6 and U202/6 at 1.4V indicate R228 low or R239, R247//R240 very high.

S02.002 High Edge Sampler

Same conditions as above. This time the actual o/p pulse, ÷ 12 is sampled, filtered and measured. If there is a fault in the sampler, both tests may fail. The daughter board may have a relay shorted, in which case several of the S01.XXX tests will also fail.

Summary table of Scope and UUT settings with expected Results

Note: a result followed by an asterix * indicates a DVM reading

Scope Settings							9100 UUT Settings				Results	
Test No.	Ch 1 from SIG_ OUT	Z in or 10x Probe	Ch 2 from TRG_ OUT	Z in or 10x Probe	Trig ±	Time base	Function	Level	Freq/ Period	Z out	Ch1 or DVM * min	Ch2 or DVM *max
3.1	2V	1M			+ Ch1	1msec	Edge	5V	1KHz	1M	7V	
3.2							Edge	5V	1KHz	1M	-0.2V*	0V*
3.3							Edge	12V	1KHz	1M	-30V*	-10V*
4.1	0.2V	50Ω	0.2V	50Ω	+Ch2	1µsec	Edge	1V	100KHz	50Ω	0.90V-1.02V	
4.2 & 4.3	0.2V	50Ω	0.2V	50Ω	+Ch2	1µsec	Edge	1V	100KHz	50Ω	Flat	
4.4& 4.5	0.2V	50Ω	0.2V	50Ω	+Ch2	0.1µsec	Edge	1V	1MHz	50Ω	Flat	
4.6& 4.7	0.2V	50Ω	0.2V	50Ω	+Ch2	1msec	Edge	1V	100Hz	50Ω	Flat	
4.8	0.1V	50Ω	0.2V	50Ω	+Ch2	10µsec	Edge	320mV	100KHz	50Ω	0.3V to 0.34V	
5.1	20mV	1M	0.2V	1M	+Ch1	200µsec	Square	80mV	Fixed	1M	75-85mV	
5.2	10V	1M	0.2V	1M	+Ch1	20µsec	Sine	80V	49.9KHz	1M	75-85V	
6.1	1V	50Ω	0.2V	50Ω	+Ch1	20µsec	Sine	3.3V	49.9KHz	50Ω	3.1V to 3.5V	
7.1							Sine	20V	49.9KHz	1M	9100	TRIP
7.2							Edge	20V	1KHz	1M	9100	TRIP
8.1 & 8.2	0.2V	1M	0.2V	50Ω	+Ch2	5msec	DC	1V		1M	0.95V to 1.05V	0.9-1.1V@ 14.7-16.6 msec
8.3	5mV	50Ω	0.2V	50Ω	+Ch2	10µsec	Sine	5mV	10Hz	50Ω	5mV	1V
8.4	5mV	50Ω	0.2V	50Ω	+Ch2	2µsec	Sine	5mV	49.9KHz	50Ω	5mV	1V
8.5	5mV	50Ω	0.2V	50Ω	+Ch2	2µsec	Sine	10.7mV	50KHz	50Ω	10.7mV	1V
8.6	5mV	50Ω	0.2V	50Ω	+Ch2	2µsec	Sine	15mV	50KHz	50Ω	15mV	1V
8.7	5mV	50Ω	0.2V	50Ω	+Ch2	10nsec	Sine	15mV	11.1MHz	50Ω	15mV	1V
8.8	5mV	50Ω	0.2V	50Ω	+Ch2	0.5µsec	Sine	15mV	11.3MHz	50Ω	15mV	1V
9.1	0.5v	50Ω	0.2v	50Ω	+Ch2	200µsec	Markers	1V	1msec	50Ω	1V	1V
9.2	0.5V	50Ω	0.2V	50Ω	+Ch2	20nsec	Markers	1V	8.9nsec	50Ω	1V	1V
9.3	0.5V	50Ω	0.2V	50Ω	+Ch2	20nsec	Markers	1V	8.8nsec	50Ω	1V	1V
9.4	0.5V	50Ω	0.2V	50Ω	+Ch2	10nsec to 1sec	Markers	1V	10nsec to 10msec	50Ω	1V, 10 cycles	1V
10.1	2V	Probe	2V	Probe	+Ch2	20µsec	S06.002				2V	2V
10.2	2V	Probe	2V	Probe	+Ch2	20µsec	S06.002				2V	2V
10.3	2V	Probe	2V	Probe	+Ch2	20µsec	S06.002				2V	2V
10.4	2V	Probe	2V	Probe	+Ch2	20µsec	S06.002				2V	2V
11.1							S03.002				2.95V*	3.15V*
11.2	2V	Probe	2V	Probe	+Ch2	10µsec	S03.002				4V	4V
11.3	2V	Probe	2V	Probe	+Ch2	0.5µsec	S03.003				4V 7V*	4V 7.6V*
12.2	2V	Probe			Line	10msec	o/p off				low pulse	
12.3	2V	Probe			Line	10msec	o/p off				no pulse	

13.1	1V	50Ω	0.2V	50Ω	+Ch2	0.05µsec 0.05µsec 20nsec 10nsec 10nsec 5nsec 5nsec	Sine	5.5V	11.1MHz 11.3MHz 50MHz 100 MHz 150MHz 200MHz 250MHz	50Ω	5.25to 5.75V to 4.75V	1V
15.3		Delay					Sine	2V	232MHz			-7%*
15.4		line					Sine	0.9V				-7%*
15.5							Sine	0.3V	to			-7%*
15.6		+					Sine	0.1V				-7%*
15.7		Mis-					Sine	30mV				-7%*
15.8		match					Sine	20mV	250MHz			-7%*