INSTRUCTION MANUAL

MODEL 21
11 MHz STABILIZED FUNCTION GENERATOR

WAVETEK®

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WARRANTY

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The obligation of Wavetek hereunder shall expire one (1) year after delivery and is limited to repairing, or at its option, replacing without charge, any such product which in Wavetek's sole opinion proves to be defective within the scope of this Warranty. In the event Wavetek is not able to repair or replace defective products or components within a reasonable time after receipt thereof, Buyer shall be credited for their value at the original purchase price.

Wavetek must be notified in writing of the defect or nonconformity within the warranty period and the affected product returned to Wavetek's factory or to an authorized service center within thirty (30) days after discovery of such defect or nonconformity. Shipment shall not be made without prior authorization by Wavetek.

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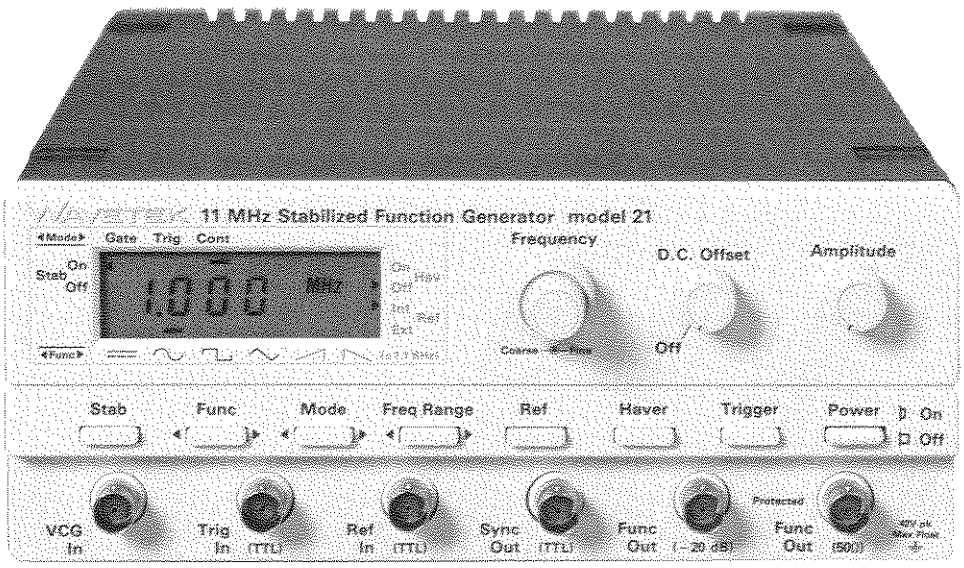


Model 21. 11 MHz Stabilized Function and Sweep Generator

SECTION 1
GENERAL DESCRIPTION

1.1 Model 21

Model 21 is a closed-loop, frequency stabilized, function generator. Both short term and long term frequency accuracies are 0.09% over its 100 μHz to 11 MHz frequency range.

Modes are continuous, triggered and gated. Output levels are to 20V peak-to-peak (10 Vp-p into 50Ω).

Waveforms are sine, triangle, square, ramp up, ramp down, haversine, havertriangle and dc. Above 1.1 kHz waveforms are analog generated; below, waveforms are digitally synthesized. Synthesized waveforms can be held at any point and continued from that point.

Synthesized output signal frequency is 1/1000 of reference clock frequency, which can be internal or external. By use of an external reference clock, the output range can be extended to ultra-low frequencies.

An LCD display shows frequency (3½ digits plus unit of measure) and annunciators that indicate selected operating modes, etc. Output is reverse power protected.

1.2 SPECIFICATIONS

1.2.1 Versatility

Waveforms

A bidirectional switch selects sine (∿), triangle (∿), square (⊓) and dc (⎓). For frequencies below 1.100 kHz ramp up (◿), ramp down (◺) and haverwaves(⩘ , ⩘) are also available.

Operational Modes

Continuous: Generator runs continuously at selected frequency.

Triggered: Generator is quiescent until triggered by external signal or manual trigger, then generates one complete waveform cycle at selected frequency.

Gated: As triggered mode, except output continues for duration of gate signal. Last waveform started is completed.

Frequency Range

100 μHz to 11 MHz in 9 overlapping decade ranges. Range switching with bidirectional switch with frequency digits; decimal and units displayed on LCD display. Each decade range capable of 1100:1 frequency change controlled by the Frequency Coarse and Fine controls.

Function Output

Waveform amplitude variable over a 20 dB range up to 20 Vp-p (10 Vp-p into 50Ω) at Function Out. Waveform also present at Function Out (-20 dB) with a fixed 20 dB attenuation relative to the Function Out for a full 40 dB of amplitude range. Peak output current is 100 mA maximum at Function Out. Source impedance of both outputs is 50Ω.

DC Offset and DC Output

Waveform offset and dc output variable with DC Offset control with off position for calibrated zero offset. Function Out is ± 10V maximum (± 5V into 50Ω) as offset or Vdc output. Signal peak plus offset limited to ± 10V (± 5V into 50Ω). DC offset plus waveform attenuated proportionately at Function Out (-20 dB).

Sync Output

TTL pulse (50% duty cycle) at generator frequency will drive 10 LS TTL loads.

VCG — Voltage Controlled Generator

Up to 1100:1 frequency change with external 0 to ± 5V signal applied to VCG IN connector. Upper and lower frequencies limited to maximum and minimum of selected range. Input impedance is 5kΩ and maximum slew rate is 0.1V/μs. VCG IN is disconnected when the Stabilizer is engaged.

Trigger and Gate

External TTL compatible signal at Trig In BNC triggers or gates generator output when generator is in trigger or gate mode. Generator triggers on positive edge of input or gates on for duration of high level input. External signal pulse width is 50 ns minimum with a maximum repetition rate of 5MHz.

Stabilizer

When selected, the generator frequency is stabilized at the displayed frequency to a crystal-controlled reference. The Stabilizer improves long term frequency stability for all durations to be equal to the 10 min. short term value.

When the stabilizer is on, the generator frequency is corrected to the displayed frequency ± 0.09% of range over the entire operating temperature range of 0 to + 50°C. The stabilizer is automatically turned off when the mode is taken out of continuous or Ext Ref. is enabled.

Display

1100 count LCD frequency display with frequency ranging units (mHz, Hz, kHz, and MHz) and decimal point. Annunciators indicate selection of waveform, stabilizer and external reference status, haverwave selection and generator mode.

External Reference

External Reference switch provides selection of internal or external control of waveform output frequency and also provides a means of holding or releasing the waveform manually, electrically or through external contact closure. External Reference connector accepts either a TTL compatible signal (1.1 MHz maximum repetition rate, 200 ns minimum pulse width) or contact closure. External reference provides four modes of operation.

Int Ref: Normal waveform function generator operation when in internal reference and the Ext Ref BNC is either left unconnected or connected to + 5 Vdc or a TTL high.

Ext Ref: External Reference operation by applying frequency to the Ref In BNC with external reference selected. Frequency input controls frequency of the selected waveform at the output. The output frequency will be 1/1000 the reference frequency. Maximum output frequency is 1.100 kHz. When external reference is selected, the display is disabled and blanked.

Manual Hold: At any point on the output waveform by use of the Ref button. Reference mode must be "Int Ref" as above. When Ref button is pressed, the output is stopped. When pressed again, the waveform will start again exactly where it stopped.

Electrical Hold: At any point on the output waveform:

When in "Int Ref" operation and 1.100 kHz or below, hold the waveform by applying 0 Vdc or a TTL low to the Ext Ref BNC or through remote contact closure shorting out the BNC.

When in "Ext Ref" operation, hold the waveform by removing the external signals at Ext Ref BNC or bringing it to 0 Vdc.

1.2.2 Frequency Precision

Frequency Display Accuracy

± 1 count of 1100 counts, which is 0.09% of range. Stabilizer maintains same reading indefinitely.

Time Symmetry

Square waveform variation from 1100 to 100 counts on display less than:

± 0.1% to 1.100 kHz (across bottom five specified ranges),
± 1% to 110.00 kHz,
± 5% to 11.00 MHz.

1.2.3 Amplitude Precision

Sine Variation with Frequency

Less than:
± 0.2 dB on all ranges up through the 10.0 to 110.0 kHz range,
± 1.5 dB to 11.00 MHz.
Referenced to 1 kHz.

1.2.4 Waveform Characteristics

Sine Distortion

Less than 0.5% THD up through the 1.00 to 11.00 kHz range and less than 1% THD up through the 10 to 110.0 kHz range. All harmonics 40 dB down from the fundamental across the 100 to 1100 kHz range and 28 dB across the 1.00 to 11.00 MHz range.

Triangle Linearity

Greater than 99% to 110 kHz.

Square Wave Rise and Fall Times

Less than 22 ns at Function Out with 10 Vp-p output into 50Ω.

Square Wave Total Aberrations

Each peak less than 5% of p-p amplitude

1.2.5 General

Output Protection

Function outputs are protected against a short circuit to any voltage between ± 10V dc and also have internal fused protection (both output and common conductors) against accidental application of up to 250 Vac or 350V dc.

Stability

Amplitude, Frequency (Non-Stabilized) and DC Offset: After 30 minute warm-up;

±0.10% of range for 10 minutes,
±0.50% of range for 24 hours.

Frequency (Stabilized): ±0.10% of range for ≥10 minutes, 0 to 50°C.

Environmental

Temperature Range: 25°C ± 10°C for spec operation, operates 0°C to 50°C, −20°C to +75°C for storage.

Warm-up Time: 20 minutes for specified operation.

Altitude: Sea level to 10,000 ft for operation. Sea level to 40,000 ft for storage.

Relative Humidity: 95% at 25°C and at sea level (noncondensing).

Dimensions

21.1 cm (8.3 in.) wide, 8.6 cm (3.4 in.) high, 30.5 cm (12 in.) deep.

Weight

3.4 kg (7 1/2 lb) net, 4.5 kg (10 lb) shipping.

Power

90 to 128, 180 to 256V, 48 to 66 Hz, less than 35 VA.

NOTE

All specifications apply for display between 1100 and 100 frequency counts; amplitude at 10 Vp-p into 50Ω.

SECTION 2
INITIAL PREPARATION

2.1 UNPACKING INSPECTION

After carefully unpacking the instrument, visually inspect all external parts for possible damage. If damage is discovered, file a claim with the carrier who transported the instrument. The shipping container and packing material should be saved in case reshipment is required.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

WARNING

To preclude injury or death due to shock, the third wire earth ground must be continuous to the facility power outlet. Before connecting to the facility power outlet, examine extension cords, autotransformers, etc., between the instrument and the facility power outlet for a continuous earth ground path. The earth ground can be identified at the plug on the instrument power cord; of the three terminals, the earth ground terminal is the nonmatching shape, usually cylindrical.

CAUTION

To prevent damage to the instrument, check for proper match of line and instrument voltage and proper fuse type and rating.

Unless otherwise specified at the time of purchase, this instrument was shipped from the factory with the power transformer connected for operation on a 115 Vac line supply and with a 3/8 amp fuse. If the unit is shipped for 115 Vac operation, there will be no markings or tags on the unit. If the unit is shipped for 220 Vac operation, there will be a 220 Vac tag on the rear panel of the unit.

2.2.2 Verifying the Line Voltage

CAUTION

All calibration pots are located inside the bottom cover on the circuit board. Be careful not to bump any pots, as this may require a recalibration of the instrument. Moving R103, located near the front panel, can keep the generator from operating; if adjustment is needed, refer to table 5-1 steps 1 through 10.

To verify the line voltage (or change the fuse), the operator must first remove the top and bottom covers. Remove the top and bottom using the following steps and figure 2-1.

1. Remove two (2) screws holding top and bottom covers to rear panel.
2. Slide both covers (together as a unit) to the rear and remove from the chassis assembly.

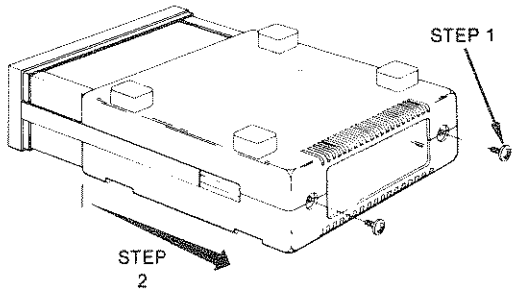


Figure 2-1. Top and Bottom Cover Removal

After the covers have been removed, the line voltage can be checked by viewing the voltage label through the inspection hole as shown in figure 2-2.

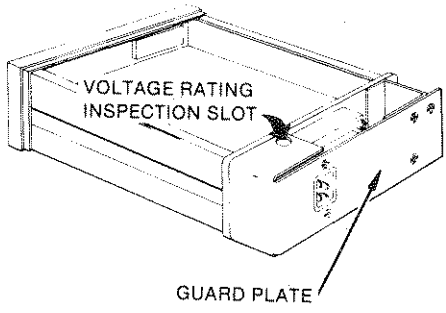


Figure 2-2. Line Voltage Inspection Hole

2.2.3 Fuse and Voltage Selection

If the line voltage is not correct, perform the following steps and refer to figure 2-3 for steps 1 and 2, and figure 2-4 for steps 3 thru 5 to change the line voltage and fuse.

1. Remove the five screws attaching the guard plate.
2. Hold the ac power receptacle assembly against the rear panel while removing the guard plate.

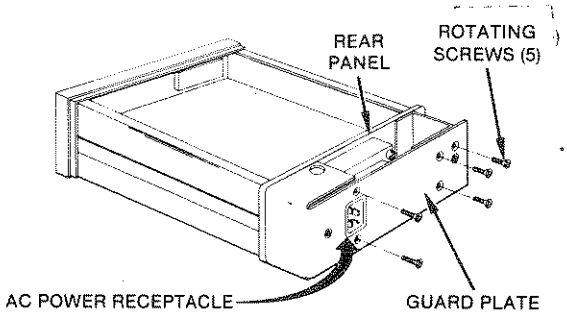


Figure 2-3. Guard Plate Removal

3. Hold the ac power receptacle firmly against the rear panel and remove the voltage selector connector from the ac primary board. Rotate the connector until the correct voltage selector indicator is on top.

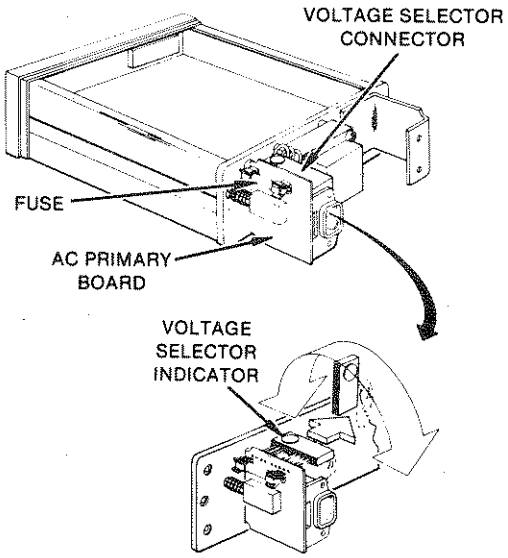


Figure 2-4. Fuse and Voltage Selection

4. Reinstall the voltage selector connector.
5. Remove the fuse and install new fuse as called out in table 2-1.

Table 2-1. Voltage/Fuse Selection

Connector Position	Voltage Range	Fuse
115V	90 to 128 Vac	3/8 amp
220V	180 to 256 Vac	3/16 amp

WARNING

Because lethal voltages are exposed, do not apply ac power to the unit until the guard plate is attached to the unit.

2.2.4 Reassembly

Refer to figure 2-5 for steps 1 thru 5 and figure 2-6 for steps 6 thru 8.

1. Ensure the power rod goes through the slot in the front panel and the ac primary board seats into the slot in the rear panel.
2. Align the guard plate to the ac power receptacle and check the routing of all wires to prevent pinching wires between the transformer and guard plate.
3. Verify that the power rod extends through the front panel slot, the circuit board seats correctly in the rear panel slot.
4. Verify the guard plate, ac power receptacle and rear panel standoffs are properly aligned and then secure with two screws.
5. Fasten the guard plate to the unit with the three remaining screws.

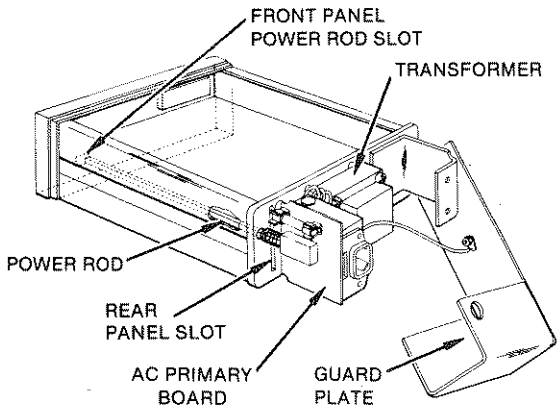


Figure 2-5. Rear Chassis Assembly

CAUTION

When sliding on the bottom cover, avoid pinching any coaxial cables located near the front panel.

6. Turn the instrument upside down, position the bottom cover over the guard shield, and then slide the bottom cover forward approximately two inches while engaging the cover and slides (see figure 2-6, detail A and detail B). Don't slide the cover on yet.
7. Turn the instrument right side up. Install the top cover using the same procedure as in step 6. Don't slide the cover on yet.
8 Align the rear of both the top and bottom cover with each other so that the cover interlocks are properly mated. Once mated, hold the covers firmly together and slide the chassis assembly into the mated top and bottom covers.
9. Secure covers to the chassis assembly using two screws as shown in figure 2-1.

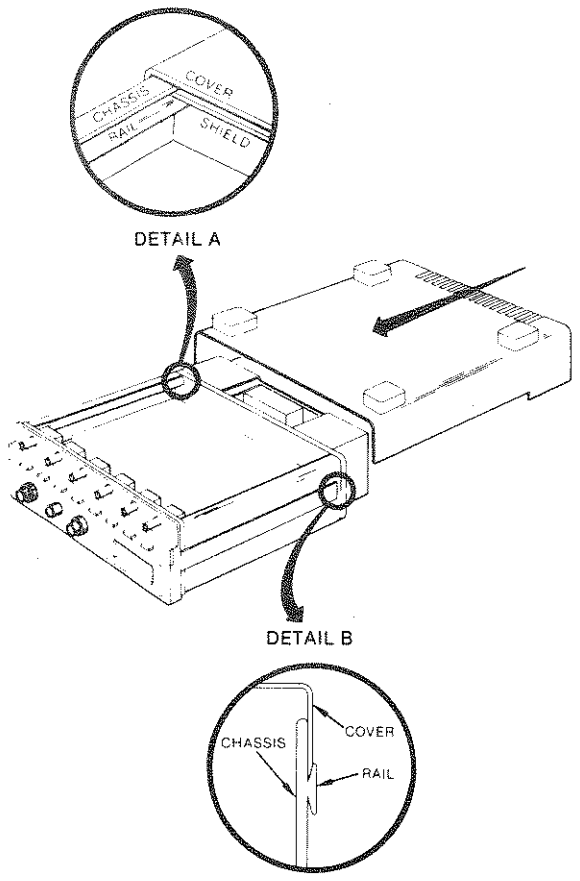


Figure 2-6. Top and Bottom Cover Installation

2.2.5 Signal Connections

Use RG58U 50Ω or equivalent 50Ω coaxial cables equipped with BNC connectors to distribute signals.

NOTE

Signal ground may be floated up to ±42V with respect to chassis ground. Be aware that all signal grounds are common and must all be floated together.

2.3 INITIAL CHECKOUT PROCEDURE

The initial checkout procedure in table 2-2 allows the operator to learn the basic operation and capabilities of the Model 21 in an easy and orderly fashion. In addition, it can be used as a receiving inspection or post-repair checkout. While this procedure verifies functional operation of this instrument, it does not verify the calibration. **The frequencies shown are typical values and should only be used as a guide.** Required tools and test equipment are shown below.

Instrument	Comments
Oscilloscope	Dual channel, 100 MHz bandwidth
Voltage Source	+5Vdc
50Ω Feedthrough	0.5% accuracy, 2W
External Generator	200 Hz to 1.1 MHz TTL output
BNC Tee	1 male, 2 female connector
BNC Coax Cable	RG58U, 3 ft. length (3 each)

2.3.1 Using the Procedure

The checkout procedure (table 2-2) can be used several different ways. It can be started at step 1 and followed straight through to the final step. Or, it can be entered at the highlighted steps, which start specific groups of checks. If the table is being followed in sequence from the previous step, perform the instructions as written. But, if starting from a high lighted step, the Model 21 must be reset to the power on settings (see below). To do this, turn the Power Off, then On.

Power On status:

Frequency Range: 0.001 to 1.100 kHz
Mode: Continuous
Function: Sine
Haver: Off
Reference: Int.
Stabilizer: Off

2.3.2 Front Panel Switches

The Func, Mode, and Freq Range switches are bidirectional. To use these switches, the operator must press the left or right side of the switch's front surface, as

indicated by the arrows on the panel. Pressing the center of any bidirectional switch does not ensure correct operation. All other switches can be pressed anywhere.

When a switch is pressed, either the frequency or an annunciator on the display will change, as shown in table 2-2.

Table 2-2. Initial Checkout Procedure

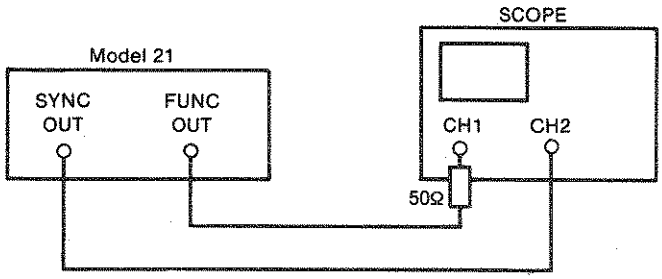
NOTE

1. *Before beginning this procedure, review paragraph 2.3.*
2. *Frequencies shown are typical and should only be used as a guide.*
3. *If starting at a highlighted step, first press Power Off, then On.*

Initial Settings

Control	Setting
Frequency	
Coarse	cw
Fine	cw
Amplitude	cw
D.C. Offset	off

Test Setup 1



Scope	Setting
Time base	0.2 ms/div
CH1 Vert	2V/div
CH2 Vert	2V/div
Trigger	CH2
Display	CH1

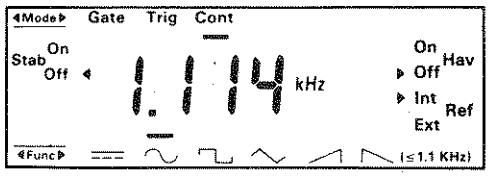
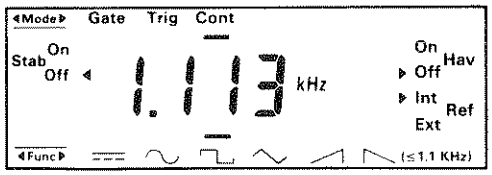
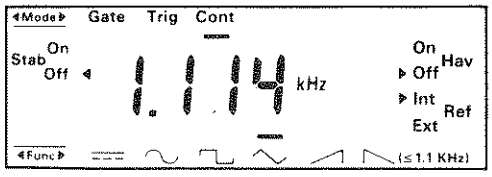
Step	Control	Operation	Display	Observation/Comments
Function Check				
1	Set to Initial Settings Power On			Connect as shown in test setup 1. 1.1 kHz, 10Vp-p sine wave.
2(a)	Func	Press Once		10Vp-p square wave
2(b)		Press Once		10Vp-p triangle

Table 2-2. Initial Checkout Procedure (Continued)

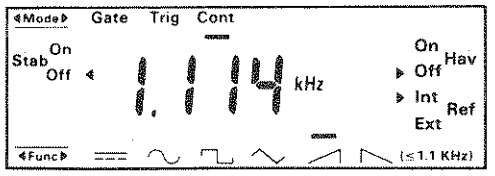
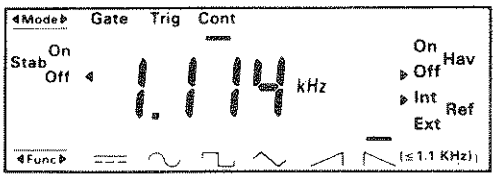
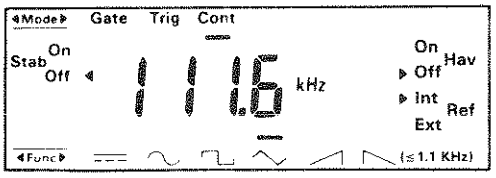
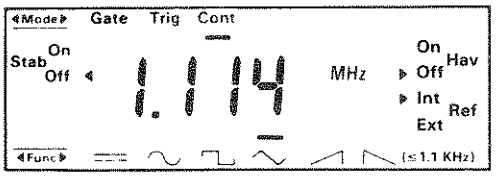
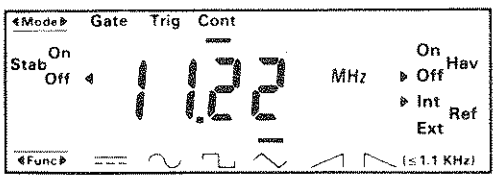
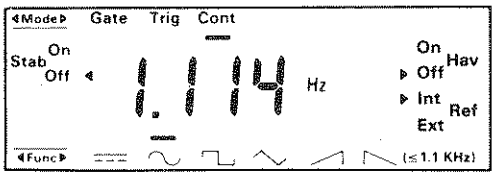
Step	Control	Operation	Display	Observation/Comments
2(c)	Func	Press Once		10Vp-p ramp down.
2(d)		Press Once		10Vp-p ramp down.
Frequency Range Check (11k to 11 MHz)				
3(a)	Freq Range	Press Once		11 kHz, 10Vp-p triangle. Ramp defaults to triangle above the 1.1 kHz range.
3(b)		Press Once		110 kHz.
3(c)		Press Once		1.1 MHz.
3(d)		Press Once		11 MHz.
Frequency Range Check (110 Hz to 110 mHz)				
4	Set to Initial Settings			Connect as shown in test setup 1. 1.1 kHz, 10Vp-p sine wave.
	Power	Press to Off then to On.		

Table 2-2. Initial Checkout Procedure (Continued)

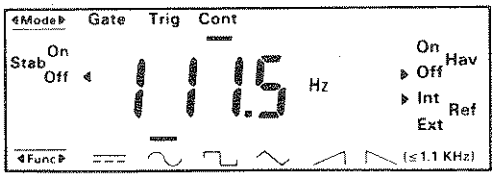
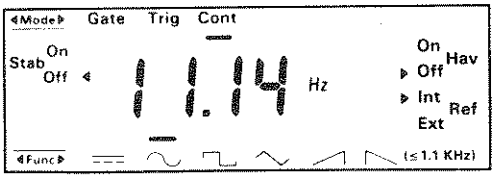
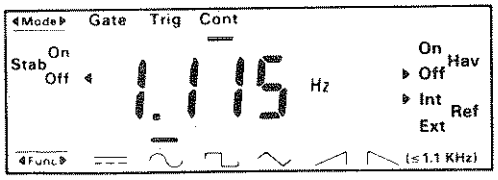
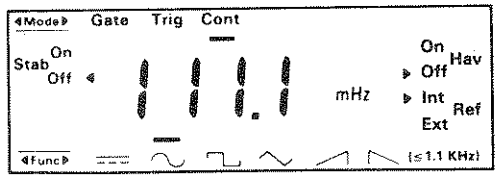
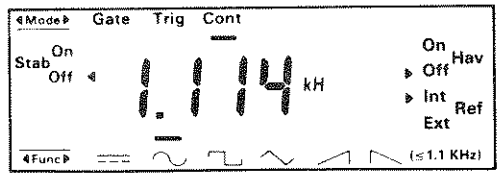
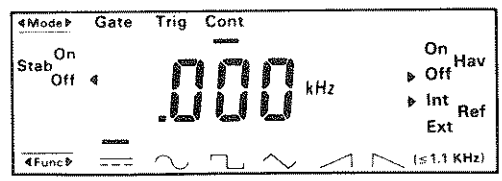
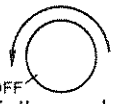
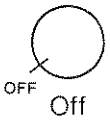
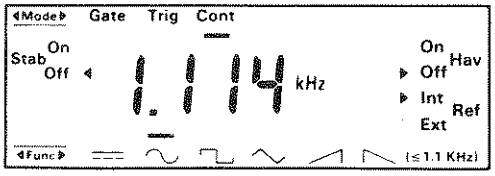
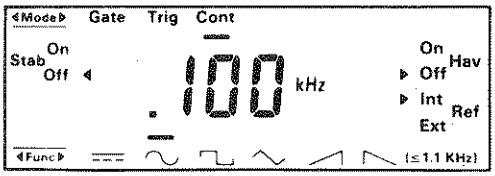
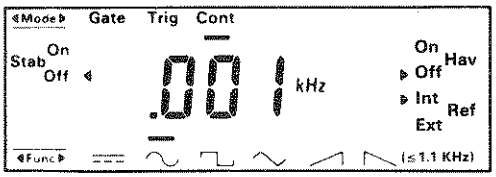
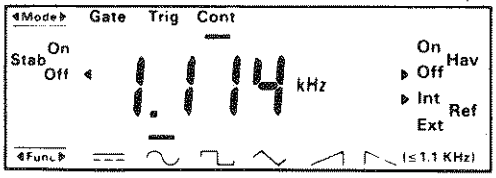
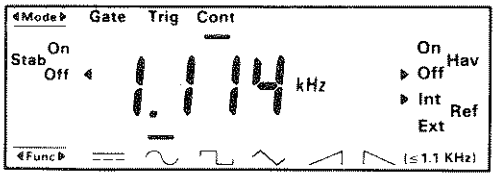
Step	Control	Operation	Display	Observation/Comments
5(a)	Freq Range	 Press Once		110 Hz.
5(b)		 Press Once		11 Hz.
5(c)		 Press Once		1.1 Hz.
5(d)		 Press Once		110 mHz.
DC Offset Check				
6	Set to Initial Settings			Connect as shown in test setup 1. 1.1 kHz, 10Vp-p sine wave.
	Power	Press to Off, then to On.		
7	Func	 Press Once		0 Vdc.
8(a)	D.C. Offset	 Full cw		Greater than +5 Vdc.
8(b)		 Full ccw, but not off		Greater than −5 Vdc.

Table 2-2. Initial Checkout Procedure (Continued)

Step	Control	Operation	Display	Observation/Comments
8(c)		 Off		0 Vdc
Coarse and Fine Frequency Check				
9	Set to Initial Settings			Connect as shown in test Setup 1. 1.1 kHz, 10 Vp-p sine wave.
	Func	 Press Once		
10	Frequency Coarse	 Full ccw		Approximately 11:1 frequency change. Verify all display segements function.
11	Frequency Fine	 Full ccw		Approximately 100.1 frequency change.
12	Frequency Coarse and Fine	 Both full cw		Total frequency change of 1100:1.
Amplitude Check				
13	Set to Initial Settings			Connect as shown in test setup 1. 1.1 kHz, 10Vp-p sine wave; output level decreases to 1 Vp-p as control is rotated.
	Amplitude	 Rotate ccw		

Test Setup 2

Scope	Setting
Time base	0.2 ms/div
CH1 Vert	0.2V/div
CH2 Vert	2V/div
Trigger	CH2
Display	CH1

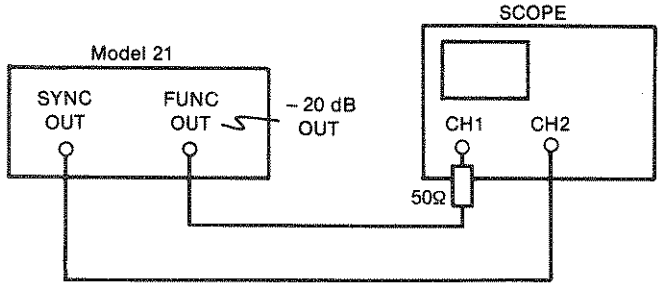
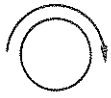
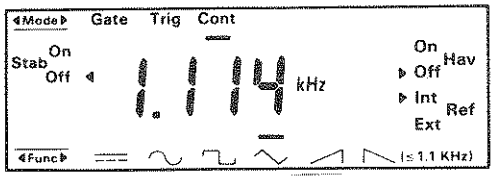
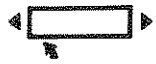
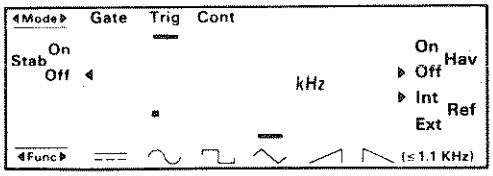
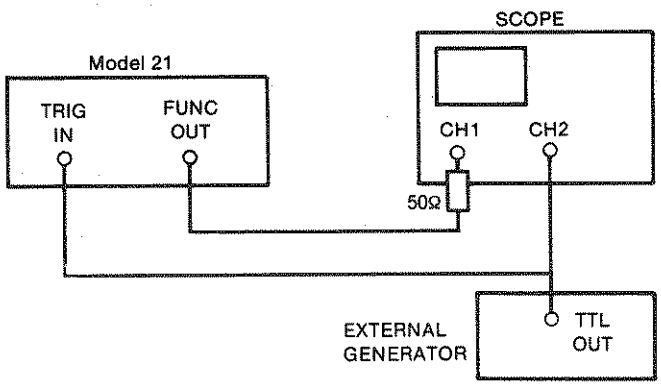


Table 2-2. Initial Checkout Procedure (Continued)

Step	Control	Operation	Display	Observation/Comments
13(b)		 Rotate cw		Connect as shown in test setup 2. 1.1 kHz, 1 Vp-p triangle.
Sync Out Check				
14				Display CH2; 1.1 kHz TTL square wave.
Trigger and Gated Check				
15	Set to Initial Settings			Connect as shown in test setup 1. 1.1 kHz, 10 Vp-p triangle.
	Func	 Press Twice		
16(a)	Mode	 Press Once		Approximately 0 Vdc level.

Test Setup 3



Settings	Scope
Time base	1 ms/div
CH1 Vert	2 V/div
CH2 Vert	2 V/div
Trigger	CH2
Display	CH1 and CH2

External Generator Setting
200 Hz TTL

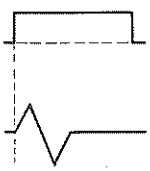
16(b)		Connect as shown in test setup 3.		CH2: Trigger Input CH1: Triggered Triangle 

Table 2-2. Initial Checkout Procedure (Continued)

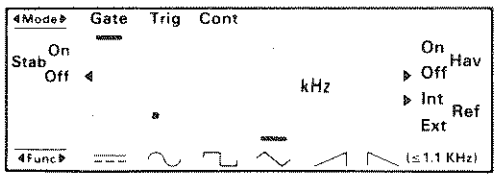
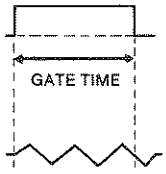
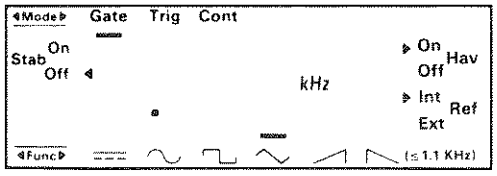
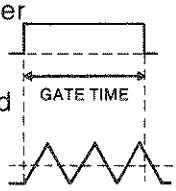
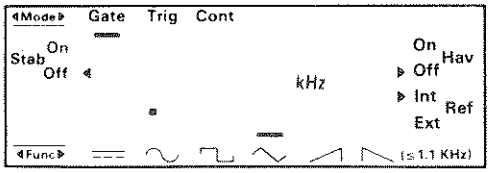
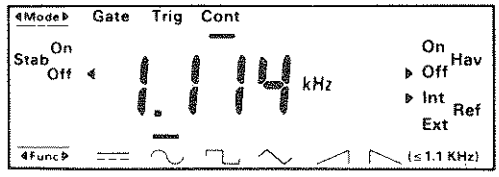
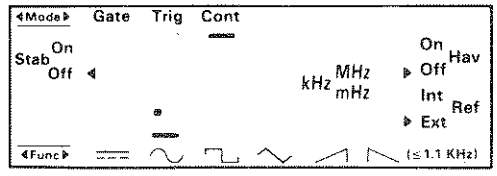
Step	Control	Operation	Display	Observation/Comments
16(c)	Mode	Press Once		CH1: Trigger Input CH2: Gated Triangle 
Haver Waveforms Check				
17(a)	Haver	Press Once		CH2: Trigger Input CH1: Gated Haver Triangle 
17(b)		Press Once		Disconnect external generator. Display and Trigger on CH1. Quiescent at negative peak of triangle.
Manual Trigger Check				
18	Trigger	Press and Hold		Continuous triangle while trigger button is pressed.
External Reference Check				
19	Set to Initial Settings			Connect as shown in test setup 1. 1.1 kHz, 10 Vp-p sine wave.
	Power	Press to Off, then to On.		
20(a)	Ref	Press Once		Quiescent at a dc level

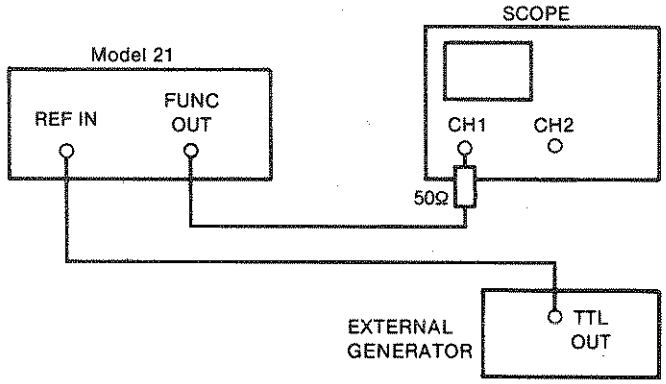
Table 2-2. Initial Checkout Procedure (Continued)

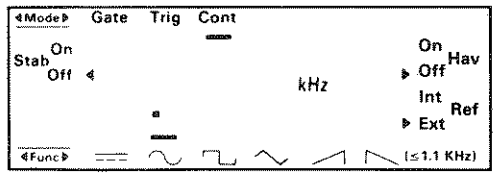
Step	Control	Operation	Display	Observation/Comments

Test Setup 4

Scope	Setting
Time base	0.1 ms/div
CH1 Vert	2V/div
Trigger	CH1
Display	CH1

External Generator Setting
1 MHz TTL



20(b)		Connect as shown in test setup 4.		1 kHz sine wave. Output frequency tracks the external generator as the frequency is lowered.
20(c)				Disconnect external generator. Quiescent at a dc level.

Stabilizer Check

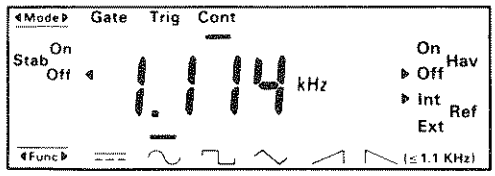
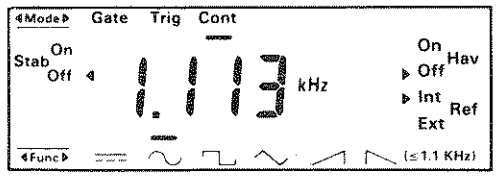
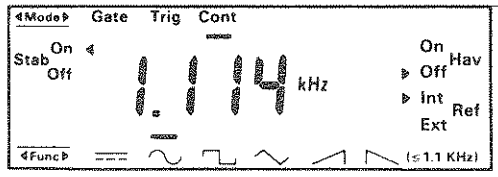
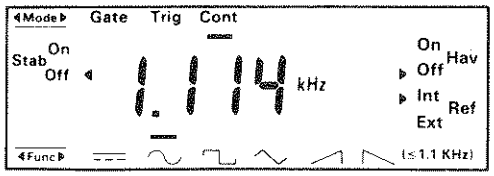
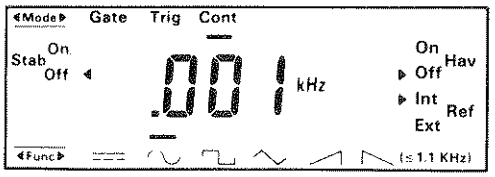
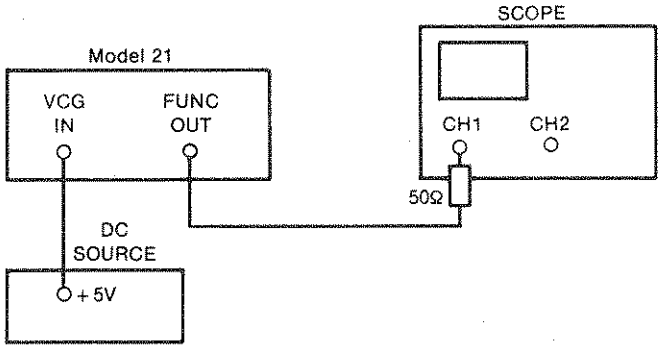
21	Set to Initial Settings Ref	 Press Once		Connect as shown in test setup 1. 1.1 kHz, 10 Vp-p sine wave.
22	Frequency Fine	See Comments		Rotate knob until the least significant digit fluctuates between two digits.
23	Stab	 Press Once		The least significant digit remains stabilized.

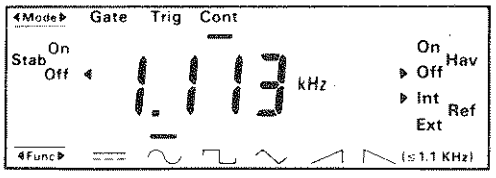
Table 2-2. Initial Checkout Procedure (Continued)

Step	Control	Operation	Display	Observation/Comments
VCG Check				
24	Set to Initial Settings			1.1 kHz, 10 Vp-p sine wave.
	Stab	 Press Once		
25	Frequency Coarse and Fine	 Both Full CCW		Low frequency sine wave

Test Setup 5

Scope	**Setting**
Time base	0.2 ms/div
CH1 Vert	2V/div
Display	CH1



26	VCG In	+ 5 Vdc		Connect as shown in test setup 5. 1.1 kHz, 10 Vp-p sine wave.

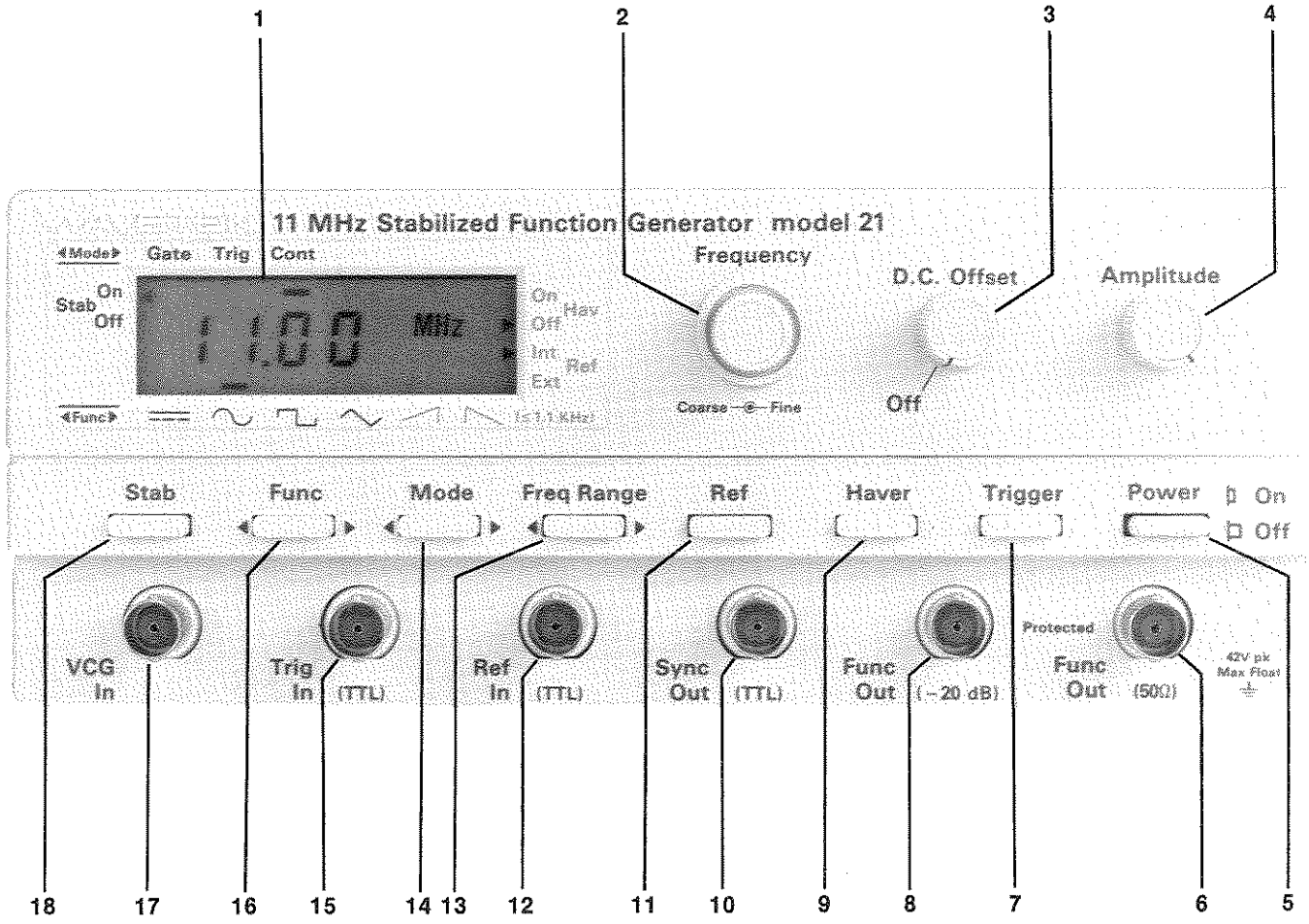


Figure 3-1. Controls and Connectors

SECTION 3
OPERATION

3.1 INTRODUCTION

This section describes the operation of the Model 21. The first part describes the controls and connectors of the instrument. The following parts describe how to use the various functions and modes of the Model 21.

3.2 CONTROLS AND CONNECTORS

The front panel controls and connectors are shown in figure 3-1 and keyed (bold numbers) to the following descriptions.

1 **Display** A 3½ digit (1100 count) LCD frequency display which incorporates annunciators that indicate mode, function (waveform), stabilizer on/off, haverwave on/off, and internal/external reference.

2 **Frequency Controls** Consist of two controls: fine and coarse. The Coarse frequency control, the outer knob of the concentric pair, allows coarse frequency adjustment (approximately 1000 counts) within the selected frequency range.

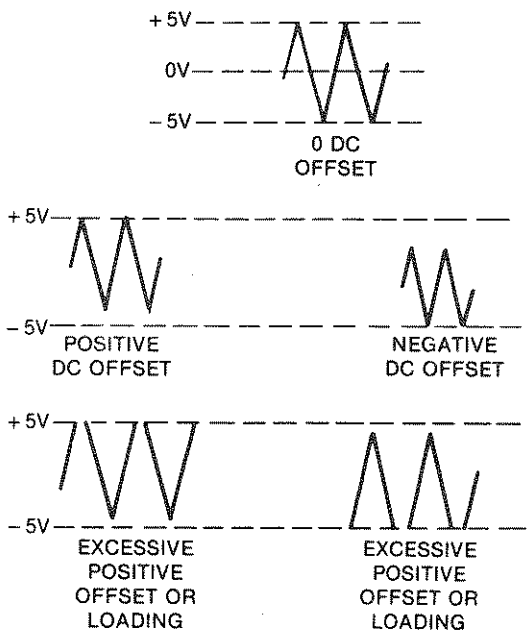
The fine frequency control, the inner knob of the concentric pair, allows fine frequency adjustment (approximately 100 counts) within the selected frequency range. Together the fine and coarse controls provide a range of 1100:1.

3 **D.C. Offset Control** This knob controls the dc voltage and offset of waveforms. A clockwise rotation vertically offsets the waveform up from the normal position (figure 3-2). A counterclockwise rotation vertically offsets the waveform down from the normal position (figure 3-2). A full counterclockwise rotation to Off ensures zero offset.

4 **Amplitude Control** This knob controls waveform amplitudes. Rotate the control full clockwise for maximum amplitude (see table 3-1). A counterclockwise rotation decreases the amplitude by 20 dB.

5 **Power Switch** The power switch turns the instrument On or Off. At power-up the instrument initializes in the following conditions:

Stab: Off
Func: Sine
Mode: Cont
Freq Range: 0.001 to 1.100 kHz
Ref: Int
Hav: Off



Function Out (50Ω) terminated with 50Ω

Figure 3-2. DC OFFSET Control

Table 3-1 Maximum Voltage at Function Out 0 dB

Function	Open Circuit	50Ω Termination
∿∿⊓ /|\/|	20 Vp-p	10 Vp-p
DC	±10V	±5V

6 **Function Output Connector** This BNC connector is the main output for the selected function. The Amplitude knob **4** controls the amplitude from 1 to 10 Vp-p into a 50Ω load (20 Vp-p into open circuit). Source impedance is 50Ω.

7 **Trigger Button** In triggered mode, the trigger button, when pressed, manually initiates a single cycle of waveform. In the gated mode, it gates the output until the button is released; the last gated cycle will always be completed. The quiescent output depends on the waveform selection and dc offset (see figure 3-3).

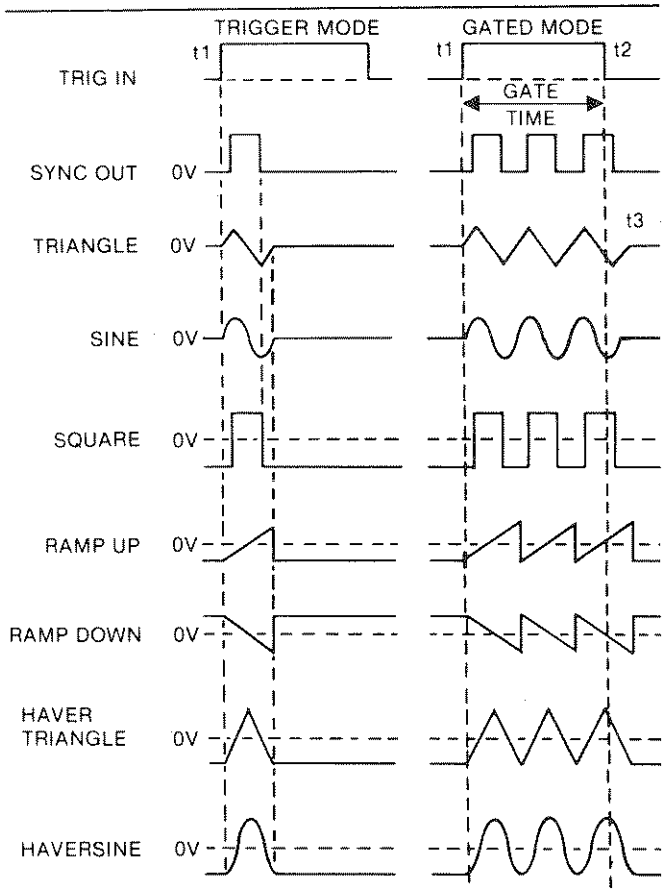


Figure 3-3. Waveforms

8 **Function Output (−20dB)** This BNC connector is the same as the Func Out **6** except the output is 1/10th (−20 dB) of the amplitude, 0.1 to 1 Vp-p. Both the waveform and offset are attenuated at Func Out (−20 dB). Source impedance is 50Ω.

9 **Haver Switch** This switch selects either the normal 0° (Haver Off) or −90° (Haver On) start/stop phase of triggered sine and triangle (figure 3-3). An annunicator on the LCD display **1** indicates the haver status. Haver wave may be selected in the trigger or gates modes using sine, triangle, and square functions on or below the 0.001 to 1.100 kHz frequency range.

10 **Sync Output** This output is a TTL square wave at the frequency of the generator. This output can be used as a synchronizing reference for the Function Outputs **6** and **8**. Phase of the waveforms relative to the sync output is shown in figure 3-3.

11 **Reference Switch** This switch serves two functions: a reference selector or manual hold control.

As a reference selector, the switch selects the reference for the waveform synthesizer, either internal or external. The annunciator on the LCD dipslay **1** indicates the reference status.

As a manual hold control with the internal reference selected and no input or TTL high at Ext Ref BNC **12**, pressing this button stops the waveform. Press the Ref button again to start the waveform.

12 **External Reference Connector** On frequency ranges below 1.100 kHz, the external reference connector serves two functions: first as an external reference input for the waveform synthesizer and second as an electrical hold for the waveform. The input functions when used with the Ref switch **11** are as follows:

External Reference Mode allows the use of an external reference signal for the synthesizer, producing a 1000 step synthesized waveform at 1.100 kHz and below. The input frequency must be 1000 times the desired output frequency; for example, 100 kHz input produces a 100 Hz output. Maximum input frequency is a 1.1 MHz TTL signal.

Manual Hold with the internal reference selected and no input or a TTL high at the Ext Ref BNC, pressing the Ref button **11** stops the waveform. Press the Ref button to again start the waveform.

Electrical Hold can be used for both internal and external reference modes. In internal reference mode, a 0Vdc, TTL low, or contact closure to ground will stop the waveform; +5V, TTL high, or an open will start the waveform from where it stopped. In external reference, removing the reference signal or supplying 0Vdc stops the waveform; applying the reference signal starts the waveform from where it stopped.

13 **Frequency Range Switch** This switch, when pushed on the left or right, steps through the nine frequency ranges as shown below.

Specified Range	Lowest Obtainable Frequency
11.00 to 1.00 MHz	0.01 MHz
1.100 to 0.100 MHz	0.001 MHz
110.0 to 10.0 kHz	0.1 kHz
11.00 to 1.00 kHz	0.01 kHz
1.100 to 0.100 kHz	0.001 kHz
110.0 to 10.0 Hz	0.1 Hz
11.00 to 1.00 Hz	0.01 Hz
1.100 to 0.100 Hz	0.001 Hz
110.0 to 10.0 mHz	0.1 mHz

The Frequency knobs **2** adjust the frequency within a range. The frequency and range is displayed on the LCD display **1**. Each range has an 1100:1 breadth.

14 **Mode Switch** This switch, when pushed on the left or right, steps through the three operating modes of the instrument.

Continuous Generator runs continuously at the selected frequency.

Triggered Generator is quiescent (quiescent level depends on waveform and offset selected, see figure 3-3) until triggered, when one complete cycle of waveform is generated.

Gated As for triggered except the waveform is continuous for the duration of the gate signal. When the signal stops, the last waveform cycle started is completed.

An annunciator on the display indicates the selected mode.

15 **Trigger In Connector** This connector accepts a positive-going TTL level input (t_1) to trigger and gate the generator, as shown in figure 3-3. A negative-going edge (t_2) ends the gated operation. When triggered, the generator produces one complete cycle for each trigger input. When gated, the generator produces continuous cycles until the gate signal (t_2) is removed; the last cycle started is always completed (t_3).

16 **Function Switch** This switch, when pushed on the left or right, steps through the six functions of the Model 21: sine ∿, triangle ∿, square ⊓, ramp up ⟋, ramp down ⟍, and dc. An annunciator on the LCD display **1** indicates the selected function. Ramps are only available on and below the 1.100 kHz range.

17 **VCG In Connector** This connector accepts 0 to ± 5V ac or dc input signals, which, when summed with a level proportional to the frequency knobs setting, controls the output frequency within the selected range. Positive input levels increase the frequency, while negative inputs decrease the frequency. Frequency excursions of 1100:1 are possible by placing the Frequency knobs to full clockwise (0 to −5V) or counterclockwise (0 to +5V). Input impedance is 5kΩ and it has a slew rate of 0.1V/μs. If frequency stabilization is selected, the VCG In connector is internally disconnected.

18 **Stabilizer Switch** This switch references the generator to an internal standard which maintains the frequency within ± 1 (least significant) digit. An annunciator on the LCD display **1** indicates the status of the stabilizer. The stabilizer works only in the continuous mode and with an internal reference.

3.3 OPERATION

Perform the initial checkout procedure in Section 2 for a feel of the instrument. Any questions concerning individual controls and connectors may be answered in paragraph 3.2. Bold numbers are keyed to figure 3-1. Outputs are shown in figure 3-3.

3.3.1 Signal Termination

Proper signal termination, or loading, of the generator connectors is necessary for its specified operation. For example, figure 3-4 shows proper termination of the Func Out (50Ω) connector. Placing the 50Ω terminator, or 50Ω resistance, in parallel with a higher impedance, matches the receiving instrument input impedance to the coax characteristic and generator output impedance, thereby minimizing signal reflection or power loss on the line due to impedance mismatch.

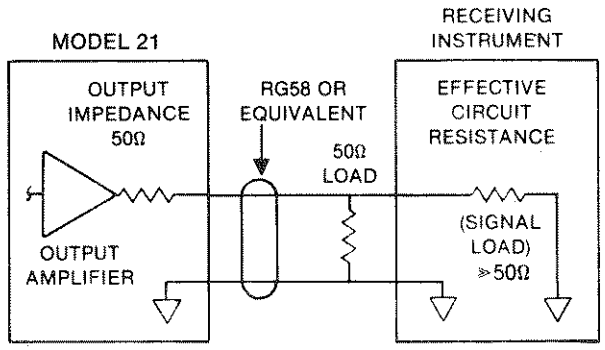


Figure 3-4. Signal Termination

The input and output impedances of the generator connectors are listed below:

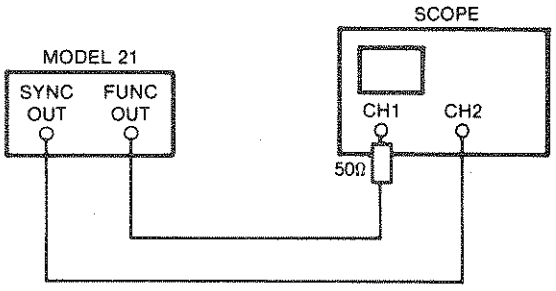
Connectors	Impedance
Func Out (50Ω) **6**	50Ω
Func Out (– 20 dB) **8**	50Ω
Sync Out **10**	TTL
Swp Out **12**	600Ω
Trig In **15**	TTL
VCG In **17**	5kΩ

3.3.2 Continuous Operation

The basic generator supplies a continuous function (waveform) at a fixed frequency set by the operator.

Control	Setting
Freq Range **13**	Set to the desired frequency range.
Frequency Coarse and Fine **2**	Set to the desired frequency within a range.
Mode **14**	Select continuous.
D.C. Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (– 20 dB).
Func **16**	Set to desired function.
Func Out (50Ω) **6** or Func Out (– 20 dB) **8**	Connect to circuit under test (refer to paragraph 3.3.1).

To demonstrate continuous operation connect the instruments as shown below, then set the controls as listed below.



Model 21 Settings	Scope Settings
Power: On	Time base: 0.2 ms/div.
Amplitude: cw	CH1 Vert: 2V/div
D.C. Offset: Off	CH2 Vert: 2V/div.
Frequency knobs: cw	Trigger: CH2.
	Display: CH1.

Observation: The scope displays a 1.1 kHz, 10 Vp-p sine wave.

3.3.3 Voltage Controlled Generator (VCG) Operation

VCG is an external electronic means of controlling the frequency of the generator by using signal levels of up to 5V peak. This allows the generator to be swept (up or down in frequency) or frequency modulated.

Control	Setting
Freq Range **13**	Set to the desired frequency range. Frequency can only be changed within a range.
Frequency Coarse and Fine **2**	For positive dc inputs at VCG In, set the Frequency knobs to the lower frequency limit. For negative dc inputs at the VCG In, set the Frequency knobs to a higher frequency limit. For modulation with an ac input at VCG In, set the Frequency knobs at the desired center frequency
VCG In **17**	As required.
Mode **14**	Select continuous.
D.C. Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-3).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (– 20 dB).
Func **16**	Set to desired function.
Func Out (50Ω) **6** or Func Out (– 20 dB) **8**	Connect to circuit under test (refer to paragraph 3.3.1).

NOTE

Excessive VCG input voltage may cause nonlinear operation when the generator attempts to exceed the range limits.

The generator can be swept up to 1100:1 with a 5V input signal to the VCG In connector. With the frequency set to 1100, excursions between – 5 and 0V at VCG In provide a 1100:1 decreasing frequency. With the frequency set to 0000, excursions between 0V and + 5V at the VCG

In provide a 1100:1 increase frequency within the frequency range.

The VCG nomograph, figure 3-5 , gives examples of how an input voltage affects the output frequency. Example 1 shows that with 0V VCG input, the Frequency knobs determine the output frequency. Example 2 shows that a positive VCG input increases the output frequencies. Example 3 shows that a negative VCG input decreases the output frequency. In the nomograph decimal points are not shown. The output frequency must be multiplied by the range. For example, in example number 2 if the frequency range is set to the .001 to 1.100 kHz range, the display will read 0.550 kHz and when the VCG voltage is applied the display will read 1.1 kHz.

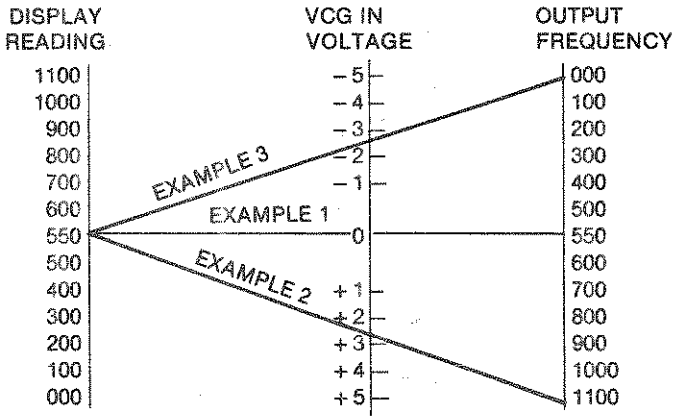
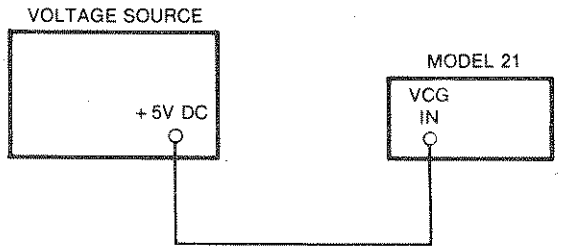


Figure 3-5. VCG Nomograph

To demonstrate VCG operation, connect the instruments as shown below, then set the controls as listed below.



Model 21 Settings	Voltage Source Settings
Power: On	Output level: +5Vdc.
Frequency knobs: ccw	

Observation: The display reads approximately 1.1 kHz.

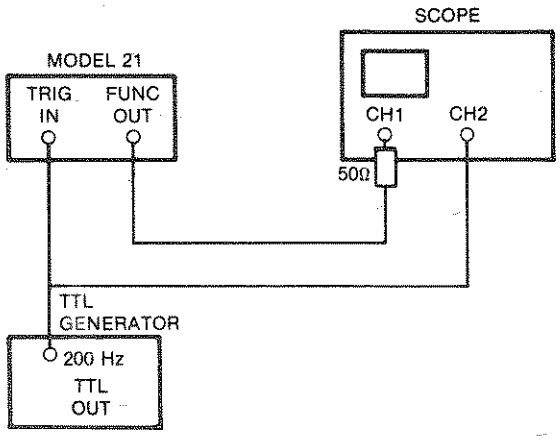
3.3.4 Triggered Operation

A triggered generator produces a single waveform each time a trigger signal is received. The Model 21 can be triggered by manual control or with a TTL signal.

Control	Setting
Freq Range **13**	Set to the desired frequency range.
Frequency Coarse and Fine **2**	Set to the desired frequency within a range.
D.C. Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (−20 dB).
Func **16**	Set to desired function.
Mode **14**	Select Trigger.
Func Out (50Ω) **6** or Func Out (−20 dB) **8**	Connect to circuit under test (refer to paragraph 3.3.1).
Trig In **15**	Connect to TTL signal source at desired trigger repetition frequency (less than Model 21 frequency).
Trigger **7**	Press to trigger.

The triggered waveform starts from a quiescent point (Sine and triangle: 0Vdc; square, ramp up, haver sine, and haver triangle: lower level; ramp down: upper level. All waveforms may be d.c offset). The Model 21 triggers on the rising (⌐) edge of the trigger signal.

To demonstrate trigger operation, connect the instruments as shown below, then set the controls as listed below.



Model 21 Settings	Scope Settings	TTL Generator
Power: On	Time base: 1ms/div.	Frequency: 200Hz.
Frequency knobs: cw	CH1 Vert: 2V/div.	Output level: TTL.
Amplitude: cw	CH2 Vert: 2V/div.	
D.C. Offset: Off	Trigger: CH2	
Mode: Trigger	Display: CH1 and 2.	

Observation: Scope Channel 1 displays a single 1.1 kHz, 10Vp-p sine wave coincident with the rising edge of the trigger input signal (CH2).

3.3.5 Gated Operation

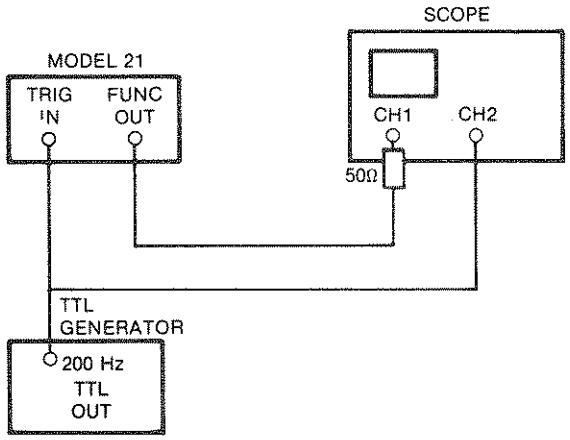
A gated generator produces a continuous output waveform for the duration of the trigger signal. The Model 21 can be gated by manual control (Trig Switch) or with an external TTL signal (Trig In).

Control	Setting
Freq Range **13**	Set to the desired frequency range.
Frequency Coarse and Fine **2**	Set to the desired frequency within a range.
D.C. Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (−20 dB).
Mode **14**	Select Gate.
Func **16**	Set to desired function.
Func Out (50Ω) **6** or Func Out (−20 dB) **8**	Connect to circuit under test (refer to paragraph 3.3.1).
Trig In **15**	Connect to TTL signal source at desired trigger repetition frequency (less than the generator waveform frequency).
Trig **7**	Press in to start gate; release to stop gate.

The gated waveform starts from a quiescent point (Sine and triangle: 0Vdc; square, ramp up, haver sine, and haver triangle: lower level; ramp down: upper level. All waveforms may be dc offset).

The instrument gates from the rising edge (⌐‾) to the falling edge (‾¬) of the Trig In signal. The last cycle started will be completed.

To demonstrate gate operation, connect the instrument as shown below, then set the controls as listed below.



Model 21 Settings	Scope Settings	TTL Generator
Power: On	Time base: 1ms/div.	Frequency: 200 Hz.
Amplitude: cw	CH1 Vert: 2V/div.	Output
D.C. Offset: Off	CH2 Vert: 2V/div.	Level: TTL
Frequency knobs: cw	Trigger: CH2.	
Mode: Gate	Display: CH1 and 2	

Observation: Scope CH1 displays gated sine waves starting at the rising edge of the trigger input (CH2) and ending after the falling edge of the trigger input.

3.3.6 Stabilizer Operation

The stabilizer, when turned on, locks the frequency to the display frequency reading. Stabilizer circuit maintains the generator frequency at this setting. The stabilizer works on all frequency ranges. Thus, the frequency range can be changed without unlocking the stabilizer.

Control	Setting
Freq Range **13**	Set to the desired frequency range.
Frequency Coarse and Fine **2**	Set to the desired frequency within a range.
Mode **14**	Select continuous.

D.C. Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (– 20 dB).
Func **16**	Set to desired function.
Func Out (50Ω) **6** or Func Out (– 20 dB) **8**	Connect to circuit under test (refer to paragraph 3.3.1).
Stab **18**	Select On.

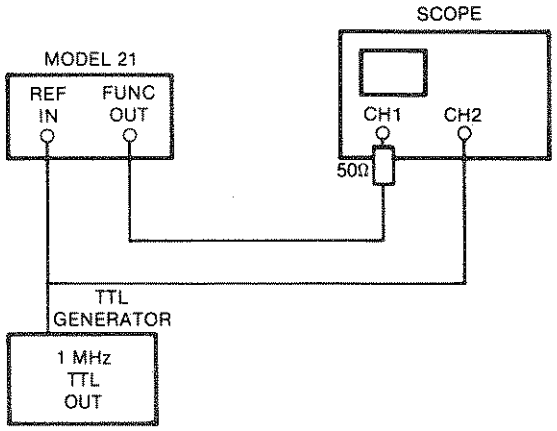
No demonstration of frequency stabilization is given.

3.3.7 External Reference Operation

When external reference is selected with an external reference signal input, the external reference signal controls the instruments frequency. The instrument frequency will be 1/1000 of the reference frequency. Maximum reference frequency is 1.1 MHz TTL signal. This produces a maximum 1.1 kHz output. There is no minimum frequency. Thus, the output frequency can be well below the minimum frequency of the Model 21.

Control	Setting
Mode **14**	Select continuous.
DC Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (– 20 dB).
Func **16**	Set to desired function.
Func Out (50Ω) **6** or Func Out (– 20 dB) **8**	Connect to circuit under test (refer to paragraph 3.3.1).
Ref **11**	Select Ext Ref.
Ref In **12**	Connect to external reference source. 1.1 MHz (maximum) TTL signal.

To demonstrate external reference operation, connect the instruments as shown, then set the controls as listed below.



Model 21 Settings	Scope Settings	TTL Generator
Power: On	Time base: 0.1ms/div.	Frequency: 1MHz.
Frequency knobs: cw	CH1 Vert: 2V/div.	Output level: TTL.
Amplitude: cw	Trigger: CH1	
D.C. Offset: Off	Display: CH1	
Ref: Ext		

Observation: The scope displays a 1kHz, 10Vp-p sine wave. This is 1/1000 the Ref In frequency.

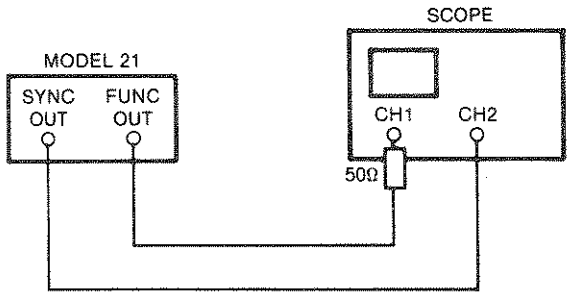
3.3.8 Manual Hold Operation

For manual hold, the Model 21 operates exactly the same as continuous except when the Ref switch **11** is pressed, the waveform immediately stops at a dc level. Pressing the Ref switch again starts the waveform.

Control	Setting
Freq Range **13**	Set to the desired frequency range.
Frequency Coarse and Fine **2**	Set to the desired frequency within a range, 1.1 kHz or below.
Mode **14**	Select Continuous.
D.C. Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (– 20 dB).
Func **16**	Set to desired function.

Func Out (50Ω) **6** or Func Out (– 20 dB) **8**	Connect to circuit under test (refer to paragraph 3.3.1).
Ref In **12**	Open circuit, + 5Vdc, or TTL high.
Ref **11**	Select external reference to hold and internal reference to restart.

To demonstrate manual hold operation, connect the instruments as shown below, then set the controls.



Model 21 Settings	**Scope Settings**
Power: On	Time base: 0.2V/div.
Frequency knobs: cw	CH1 Vert: 2V/div.
Amplitude: cw	CH2 Vert: 2V/div.
D.C. Offset: Off	Trigger: CH2.
Ref: As directed	Display: CH1.

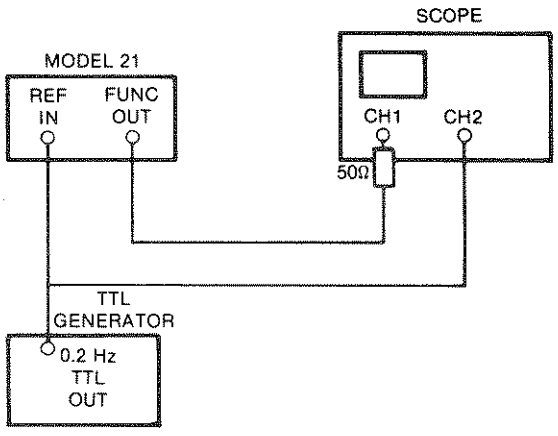
Observation: The scope displays a continuous 1.1 kHz, 10Vp-p sine wave. When the Ref switch **11** is pressed once, the waveform immediately stops at some dc level. press Ref again to resume the waveform.

3.3.9 Electrical Hold Operation

For electrical hold, the Model 21 operates exactly the same as continuous, except the output can be stopped and held at any point.

Control	**Setting**
Freq Range **13**	Set to the desired frequency range. Must be 1.1 kHz or below.
Frequency Coarse and Fine **2**	Set to the desired frequency within a range.
Mode **14**	Select continuous.
DC Offset **3**	Set as desired. Limit offset to prevent clipping (see figure 3-2).
Amplitude **4**	Set to desired output level at Func Out (50Ω) or Func Out (– 20 dB).
Func **16**	Set to desired function.
Func Out (50Ω) **6** or Func Out (– 20 dB) **8**	Connect to circuit under test (refer to paragraph 3.3.1).
Ref In **12**	For Int Ref operation (1.1 kHz range and below) a contact closure, TTL low, or 0Vdc holds the waveform. An open, TTL high, or + 5Vdc releases the waveform. For Ext Ref opeation, (1.1 kHz range and below) removing the reference signal or applying 0Vdc holds the waveform. Connecting the reference signal releases the waveform.
Ref **11**	Set to the desired reference source.

To demonstrate external reference operation, connect the instruments as shown, then set the controls as listed below.



Model 21 Settings	**Scope Settings**	**TTL Generator**
Power: On	Time base: 0.1ms/div.	Frequency: 0.2Hz.
Frequency knobs: cw	CH1 Vert: 2V/div.	Output level: TTL.
Amplitude: cw	Trigger: CH1	
D.C. Offset: Off	Display: CH1	

Observation: The Model 21 produces continuous 1.1 kHz, 10Vp-p sine waves when the Ref In signal is high. When the Ref In signal goes low, the output waveform is held at dc level.

SECTION 4
CIRCUIT DESCRIPTION

4.1 INTRODUCTION

The Model 21, an 11 MHz stabilized function generator, operates as an analog waveform generator at frequencies above 1.100 kHz and a digital waveform synthesizer at frequencies below 1.100 kHz. In addition, the frequency, regardless of range, can be stabilized to the display frequency. Refer to figure 4-1.

The function generator loop, controlled by Frequency Coarse and Fine verniers, VCG In, Trig In and the stabilizer, is the heart of the generator. On the four frequency ranges above 11.00 kHz, the function generator loop produces triangle and square waves that are routed directly to the function selector located in the output block; a sine converter, also in the output block, modifies the triangle into a sine wave. The waveform synthesizer produces all the waveforms on the five lower frequency ranges (110.0 mHz, 1.100 Hz, 11.00 Hz, 110.0 Hz, and 1.100 kHz). The waveform can be clocked either internally from the function generator loop through the stabilizer (MFSQ) or externally from an external signal (Ref In). Each clock pulse (MFSQ or Ref In) steps the synthesizer through its 1000 output levels, thus the clock signal is 1000 times the output frequency of the syn-

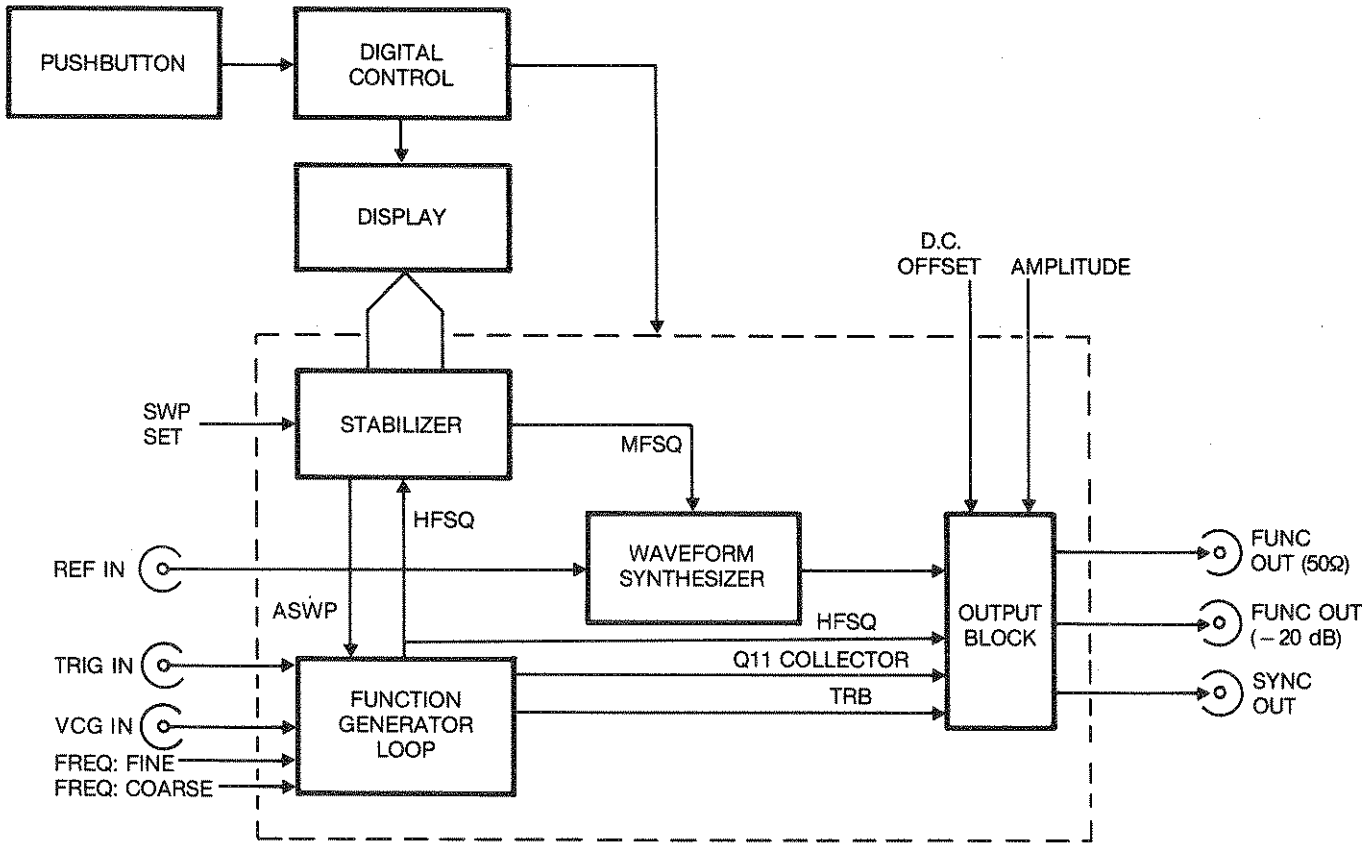


Figure 4-1. Model 21 Block Diagram

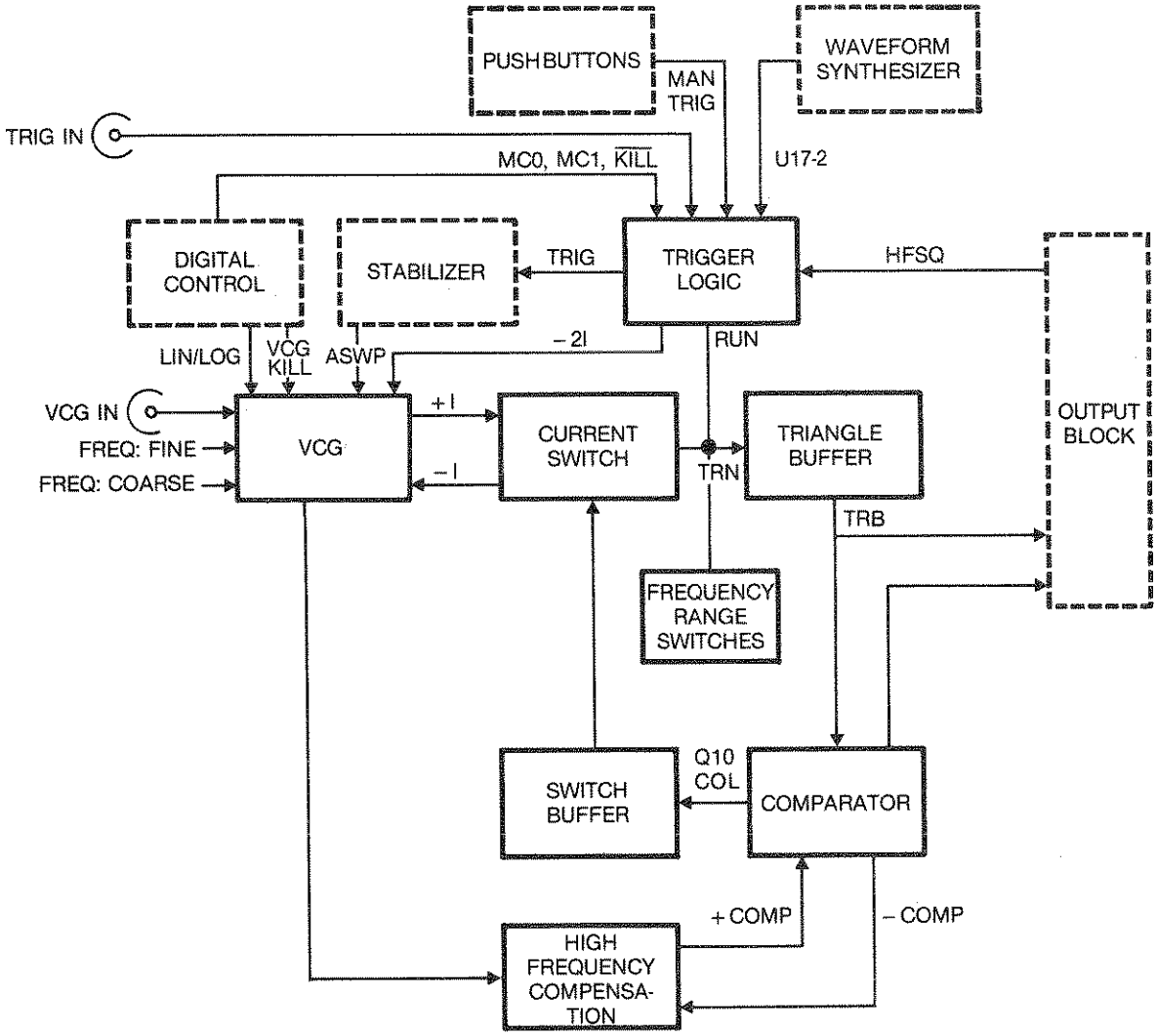


Figure 4-2. Function Generator Loop

thesizer. The synthesizer output, like the higher frequencies, is routed through the function selector. For all ranges, the output block, controlled by the digital control, Amplitude and DC Offset controls, selects and controls the output signal at the Func Out (50Ω), Func Out (– 20dB), and Sync Out connectors. When in Stab mode, the stabilizer monitors the frequency output, the same as the frequency shown on the display, from the function generator loop and provides a voltage feedback (ASWP) to the function generator loop, thus keeping the frequency within one least significant count regardless of the frequency range.

The digital control sets the circuits shown in the dotted outline to a default state when the unit is initially turned on. When a pushbutton is pressed, the pushbutton control causes the digital control to change parameters in the appropriate circuit. The digital control along with the stabilizer controls the front panel display.

4.2 DETAILED CIRCUIT DESCRIPTION

4.2.1 Function Generator Loop

Figure 4-2 shows an expanded diagram of the function generator loop that consists of the VCG (voltage controlled generator), current switch, frequency range switches, triangle buffer, comparator, switch buffer, high frequency compensation, and trigger logic circuits.

The VCG produces two currents (+ I and – I), alternately switched in and out by the current switch and controlled by the output of the switch buffer which charge (+ I) or

discharge (– I) one of four range capacitors in the frequency range switches to produce a linear triangle. The specific frequency is determined by the magnitude of the + I and – I currents. The triangle is amplified by the triangle buffer which drives the comparator that detects the triangle peaks and causes the comparator to switch output states; the threshold level of the comparator is controlled by the high frequency compensation circuit. The output of the comparator controls the switch buffer output state which, in turn, controls the current switch. The function generator loop only produces the top four frequency ranges, the five lower ranges are produced by using the function generator loop to clock the waveform synthesizer. The trigger logic circuit enables or disables the function generator loop depending on the selected mode.

4.2.1.1 VCG

The VCG (ref: schematic 0103-00-1116 sheet 1) consists of the VCG amplifier, current sources, current sink, and trigger control current sink. The VCG amplifier (U1 pin 1) converts voltages from the VCG In (except in Stab mode), FRFINE (frequency fine), FRCOARSE (frequency coarse), into currents that controls the current source and sinks (U28) which set the desired frequency within the selected range. A gain adjustment (R1) controls the top-of-range frequency, while R13 sets the 1100:1 (bottom-of-range) frequency. R11 controls the offset of the amplifier and zener diode CR1 limits the voltage swing at U1 pin 1 to within 30% over the maximum allowable swing. CR2 and CR3 prevent excessive voltages at VCG In from damaging the VCG amplifier.

Current Source and Current Sink: The current source and current sink, part of the VCG circuit, regulate the current leaving the current source, (+ I) and the current entering the current sink, (– I). The negative signal from the VCG amplifier (U1 pin 1) is converted into a current leaving summing node at U1 pin 9 through R1 and R12. U1 pin 8 controls current sunk by Q1 which, in turn, controls current sourced by Q2 and the two transistors in the upper half of U28.

Operational amplifier (U1 pin 8) holds pin 9 at ground potential. When pin 9 tries to go negative, pin 8 goes positive, which causes Q1 to sink current through R18. This lowers the voltage at the base of Q2 and the two transistors in U28 which sources sufficient current through Q2's collector to hold U1 pin 9 at 0V; increased current now flows from the current source (U28 pin 12). CR4 limits the voltage swing at U1 pin 8 to within 30% over the maximum allowable swing.

An increase in current through R42 pin 16 appears like a positive input to the operational amplifier (U1 pin 5) driving the output at pin 7 positive. This raises the voltage at U28 pin 1 that causes pin 3 to sink more current until virtually all the current through R42 pin 16 passes through U28 pin 3, maintaining a virtual ground at U1 pin 5. Increased current now flows into the current sink (– I) through U28 pin 6 which tracks the current source. The emitter resistors for Q4 and U28 pins 2 and 4 are all 1kΩ, therefore the collector currents at U28 pin 3, – I (pin 6), and Q4 will be equal.

Trigger Control Current Sink: The trigger control current sink clamps the triangle node (TRN) at ground potential during the "off" state in the triggered and gated modes.

When the generator is gated "off", RUN goes low, reverse biasing CR7. As the triangle node rises toward the zero crossing point, a greater proportion of the – 2I current emitter resistor at U28 is 500Ω, flows through U3 pin 9. Equilibrium is reached when the trigger holding current is equal to the positive current (+ I) being supplied to the generator loop, preventing the triangle node voltage from rising any further. The matched diodes in U3 have equal currents through them [(– I) + (– I) = (– 2I)] and the anode at pin 4 is grounded, hence the voltage drops across the two diodes are equal and the triangle node is held at ground potential. This stops the triangle waveform on the rising slope and ensures that at least one complete cycle will be generated every time the generator is triggered. Also, refer to paragraph 4.2.1.8 Trigger Logic.

4.2.1.2 Current Switch

The current switch (ref: schematic 0103-00-1116 sheet 2) consists of the diode switches (CR10, 11, 12, 13) currrent source buffer (Q7) and current sink buffer (Q17). Controlled by the square buffer, it alternately allows the charging (+ I), and discharging (– I) of the selected frequency range capacitor (see paragraph 4.2.1.3) to produce a triangle waveform.

The current switch sources current buffered by Q7 (+ I), or sinks current buffered by Q17 (– I) at the switch output (junction or CR10 and CR12). The instantaneous polarity of the Switch Buffer output control line (junction or R59 and R60) determines the direction of the sinked or sourced current flow.

With the control line at + 2V, CR11 and CR12 are reverse biased and – I current through CR10 linearly charges the selected timing capacitor. At the same time, current flows from the control line through CR13 into the current sink. With the control line at – 2V, CR10 and CR13 are reverse biased. The timing capacitor linearly discharges through CR12 to the current sink and current is sourced through CR11 into the control line.

4.2.1.3 Frequency Range Switches

The frequency range switches (ref: schematic 0103-00-1116 sheet 2) consist of the four basic range capacitors and their controls. Each range capacitor or set of capacitors covers 10% to 100% of full scale. A logic level signal from the frequency range control circuit switches in the range capacitor. For example, when $\overline{FR6}$ goes low, it turns on Q22 which sources about 30 mA through R108 and diodes CR25 and CR26. With CR26 forward biased, the diodes impedance to ground is less than 2Ω and the range capacitor set (C40, C41 and C42) is effectively connected to ground. When this range is not selected, $\overline{FR6}$ is high, Q22 is turned off, and R109 pulls the anode of CR25 to −15V. The voltage divider, R106 and R107, brings the anode of CR26 to −7.5V through the 10 MΩ resistor R105, reverse-biasing CR26. This provides a very high impedance, disconnecting the range capacitor. Frequency range control lines ($\overline{FR4}$ and $\overline{FR5}$) operate the same way by connecting matched capacitors of 0.0047 μF (C43) and 0.047 μF (C45) to the TRN line.

Capacitance for the highest frequency range (100 pF) consists of all the stray capacitance at the triangle node added to C39 and C38 (the 11 MHz adjustment capacitor). Frequency range control line ($\overline{FR6}$) connects an additional 400 pF (C41, C42) and the 1.1 MHz adjustment (C40) to TRN.

4.2.1.4 Triangle Buffer

The triangle buffer (ref: schematic 0103-00-1116 sheet 2), a high speed FET input voltage follower with a low impedance output and unity gain, buffers the current switch and frequency range capacitor from relatively high current circuits in the output block and the comparator.

The triangle buffer consists of Q14, acting as a high input impedance source follower, and Q15, acting as a low output impedance emitter follower. The difference between the input and output voltage of the circuit is controlled by adjusting the current through Q14, such that, the gate-source voltage is equal and opposite to the base-emitter drop of Q15, this causes the two voltages to cancel each other. The baseline adjustment, R103 sets the current through Q14.

4.2.1.5 Comparator

The comparator (ref: schematic 0103-00-1116 sheet 2) detects the peak of the triangle and produces two square wave outputs. One square wave output from the comparator (Q10 collector) drives the switch buffer, while a second square wave of opposite polarity (Q11 collector) drives the output block. The comparator's threshold voltage is set by the +COMP and −COMP from the high frequency compensation circuit.

As the triangle voltage at the base of Q19 reaches the positive threshold voltage (+1V), set by U3 pin 2, Q19 turns on as Q18 turns off. When Q18 and Q19 switch, they also cause the second differential pair, Q10 and Q11, to switch. As Q10 switches "off", current through R63 decreases and the collector of Q10 goes low, (about −1.6V). The current drain through R90 determines the collector voltage of Q10. CR17 and CR18 increase the transistor switching speed of Q18 and Q19 by limiting the signal swing at their collectors to about 0.7V. Resistors R64 and R71 increase the switching speed of Q10 and Q11 by providing a small current which keeps them from turning entirely off, and diodes CR16 and CR19 are switched on and off to further guarantee that Q10 and Q11 do not switch off.

Diode bridge (U3 pins 5, 6, 8) operate similar to the current switch. The switch buffer output (U3 pin 6) state determines the polarity of the comparator threshold at pin 2. The comparator threshold voltage at pin 2 is limited to ±1V by the voltage drop across the 332Ω resistor (R92) since the +COMP and −COMP currents supply no more than 3 mA. The high frequency compensation circuit reduces the +COMP and -COMP currents on the highest frequency range which lowers the comparator threshold voltage at the base of Q18 to compensate for switching delays (see paragraph 4.2.1.7).

Output transistors Q10 and Q11 have different values of collector and emitter resistors to match the input requirements of the buffer that each drives.

4.2.1.6 Switch Buffer

The switch buffer (ref: schematic 0103-00-1116 sheet 2) shifts the level of the comparator's square wave to provide a voltage excursion (±2.2V) capable of driving the current switch. The switch buffer is a complementary emitter follower biased on by the voltage drops across CR14 and CR15 and controlled by the comparator output at the collector of Q10. The ±2.2V square wave output controls the current switch in the generator loop and the polarity of the comparator threshold voltage.

4.2.1.7 High Frequency Compensation

High frequency compensation (ref: schematic 0103-00-1116 sheet 2) circuit sets the threshold voltage of the comparator. On the lower frequency ranges (110.0 mHz through 1.100 MHz), the value of the +COMP and −COMP currents set up the comparator threshold voltage at the base of Q18; each current has a fixed value of 3mA through the resistor R92. On the 1.00 to 11.00 MHz range, the threshold voltage is lowered to compensate for switching delays in the function

generator loop; this maintains the triangle peaks at the same levels as on lower ranges.

On the lower frequency ranges with HF COMP disconnected, R80 and R81 holds U27 pins 2 and 3 and the emitter of Q5 at 0.0V. This puts 15V across series resistors R83 and R85 and −10V at the base of Q16. The same current that flows through R85 also flows through R52. This puts +10V at the base of Q6. The emitter of Q6 is +10.7V which causes 3mA to flow from the collector of Q6 through U3 and R92 to ground during half of the cycle setting up a threshold voltage at the base of Q18. On the opposite half of the cycle, the base of Q18 switches to −1V because the same amount of current (3mA) flows from ground through R92 and U3 to the collector of Q16.

In the 11.00 MHz frequency range, HF COMP (U2 pin 10 of the VCG) is connected to U27 pin 3. At top of the range, 2.5mA is sinked from ground through R80 and R81 to the collector of Q4 in the VCG lowering the voltage at U27 pin 3 to about −5V. This decreases the voltage at the emitter of Q5, as well as the current through R83, R85, and R52 which forces the bases of Q6 and Q16 closer to their respective power supply voltages. The current through R92, the collectors of Q6 and Q16, and the threshold voltage at the base of Q18 are all decreased. This new lower threshold voltage causes the triangle to switch earlier than normal. If the generator is not at full scale, a voltage indirectly proportional to the frequency is set at the base of Q18.

4.2.1.8 Trigger Logic

The trigger logic circuit (ref: schematic 0103-00-1116 sheet 3) allows the generator loop to be externally triggered or gated. When in trigger or gated modes (determined by MC0 and MC1), the trigger logic circuit prevents the generator from running by sinking away the current from the triangle node (TRN) that would normally charge the timing capacitor. Pressing the Trigger button or connecting a signal to the Trig In (TTL) BNC releases TRN which allows the generator to run until HFSQ completes one complete cycle. In addition, the synthesizer output at U22 pin 6 must be high to stop the generator when the frequency range is 1.1 kHz or lower. $\overline{\text{KILL}}$ inhibits the generator when in DC function.

The following paragraphs describe the relationship in various conditions relative to the trigger logic.

Continuous Mode: In Continuous Mode, U12 pin 4 (MC0) is low which holds U12 pin 6 low and sets U23 pin 5 high. $\overline{\text{KILL}}$ (U22 pin 13) will be high for all functions except DC and U22 pin 11 will be low. This sets U23 pin 9 high causing the generator to free-run.

Trig Mode: In Trig Mode, U12 pin 4 (MC0) is held high and U15 pin 4 (MC1) is held low which forces U15 pin 6 and U12 pin 6 high. If the Trigger pushbutton on the front panel is not pressed, U15 pin 10 remains high and U15 pin 10 remains high and U15 pin 8 is in phase with the Trig In signal at U21 pin 13.

With no signal present at Trig In, U23 pin 3 is low. HFSQ is low, U22 pin 8 is high, and U23 pin 5 is low. If $\overline{\text{KILL}}$ (U22 pin 13) is high, U22 pin 11 will be high. U20 pin 10 (LF) is low for frequency ranges 11.00kHz and above which forces U20 pin 8 high. Also, since U22 pin 2 is high, U23 pin 12 is low. Pin 9 will be low disabling the generator.

U15 pin 8 will go high when the Trigger switch on the front panel is pressed (U15 pin 10 goes low) or when an external trigger signal is received (U21 pin 13 goes high). Because the D input at pin 2 is connected to +5V the Q output (U23 pin 5) is high. With $\overline{\text{KILL}}$ (U22 pin 13) high, U22 pin 11 will go low which sets U23 pin 9 (RUN) high and causes the generator to run. At the positive transition of HFSQ (U22 pin 9), U23 pin 11 goes low. On the next negative transition of HFSQ, U23 pin 11 goes high, which clocks the low at pin 12 to pin 9 (RUN) and stops the triangle on its rising edge. Only one cycle of generator output is enabled for each trigger pulse applied.

Gate Mode: In Gate Mode, MC1 (U15 pin 4), MC0 (U12 pin 4), U15 pin 6, U12 pin 6, and U15 pin 10 are high while U23 pin 3 is low. If $\overline{\text{KILL}}$ (U22 pin 13) is high, U22 pin 11 will be high. When LF (U20 pin 10) is low, frequency ranges 11.00 kHz and above, U20 is forced high; because in gate mode $\overline{\text{SWP RUN}}$ is high, U22 pin 3 will be low which disables the generator.

When Trigger on the front panel is pressed (U15 pin 10 goes low) or a voltage at Trig In causes U21 pin 13 to go high, U15 pin 8 also goes high clocking the Q output (U23 pin 5) high. With $\overline{\text{KILL}}$ (U22 pin 13) high, U22 pin 11 will go low which sets U23 pin 9 (RUN) high and causes the generator to run. For the duration of the time the trigger signal at Trig In remains high or the Trigger button is pressed, U15 pin 6 and U12 pin 6 will remain low. This sets U23 pin 5 high, forces U23 pin 10 (S) low, sets RUN (U23 pin 9) high, and enables the generator to free-run.

When U23 pin 3 goes low, U15 pin 6 and U12 pin 6 go high. On the next negative transition of HFSQ, U22 pin 8 goes high which clocks the low at pin 12 to the output at pin 9 (RUN) and stops the triangle oscillation when it reaches 0V.

Low Frequency: When the Frequency range is 1.1 kHz or lower, the trigger logic works much the same as previously described, except U23 pin 12 must be low to stop the generator. This occurs at either the zero crossing of the rising edge of the triangle (Haver Off), or at the negative peak of the triangle (Haver On). If Haver is Off, U13 pin 6 (waveform synthesizer) functions as a zero crossing detector that controls the trigger logic. If Haver is on, U16 (waveform synthesizer) acts as a negative

peak detector. U22 pin 6 goes low in either condition. With U22 pin 6 high, the next positive transition at U17 pin 3 forces $\overline{Q}$ (U17 pin 6) low. For the five lowest frequency ranges, LF (U20 pin 10) is high, this makes pin 8 high and causes U22 pin 3 to go low.

Haver Off: When Haver is Off, HAV (U19 pin 11) is low, which disables U16 and maintains U22 pin 4 high. The zero crossing detector (U13 pin 9) controls the trigger logic; see Low Frequency above.

Haver On: When Haver is on, U19 pin 11 (HAV) is high which disables the zero crossing detector (U13 pin 9). Thus, with HAV high, U16 pin 6 detects the negative peak and controls the trigger logic.

DC Function: If Func is set to DC, U22 pin 13 ($\overline{KILL}$) will be low. This clears U23 and pin 9 (RUN) is forced low, which disables the generator.

4.2.2 Waveform Synthesizer

The waveform synthesizer produces the digitally synthesized waveforms used on the five lower frequency ranges (1.100 kHz and below). It consists of seven circuits: ÷1/÷100 counter, reference selector, ÷1000 up/down counter, waveform EPROM, data selector, latch, and DAC, as shown in figure 4-3 and schematic 0103-00-1116 sheet 3.

The reference selector specifies which reference, external or internal, clocks the 9-bit up/down counter.

External refererence enters through the Ref In BNC. Its frequency must be 1000 times the desired output frequency. Diodes CR40 and CR41 and two inverters (U21) act to prevent damage to the remaining circuitry caused by excessive voltage swings at the Ref In BNC.

The internal reference originates from the function generator loop at HFSQ. This signal must pass through the ÷1/÷100 divider (U7B, U8B; ref: schematic 0103-00-1115 sheet 3) where the frequency is either divided by 1 or 100, depending upon the selected frequency range, see table 4-1.

Table 4-1. Internal Reference Selection

Frequency Range	Generator Loop Frequency (HFSQ)	÷1/÷100	Medium Frequency Square Wave (MFSQ)
.100 to 1.100 kHz	.100 to 1.100 MHz	÷1	1.100 to 1.100 MHz
10.0 to 110.0 kHz	10.0 to 110.0 kHz	÷1	10.0 to 110.0 kHz
1.00 to 11.00 kHz	1.00 to 11.00 kHz	÷1	1.00 to 11.00 kHz
.100 to 1.100 Hz	10.0 to 110.0 kHz	÷100	.100 to 1.100 kHz
10.0 to 110.0 mHz	10.0 to 11.00 kHz	÷100	10.0 to 110.0 Hz

This new signal (MFSQ) is 1000 times the output frequency. The control line $\overline{EFC}$ (U15 pin 11) controls the reference selector (ref: schematic 0103-00-1116 sheet 3).

For external reference, $\overline{EFC}$ is held low, which inhibits MFSQ and enables U15 pin 12. The refernce clock, U15 pin 11, is inverted relative to the Ref In signal.

When $\overline{EFC}$ goes high and the Ref In is held high or floats, the internal reference clocks the counter. If Ref In is forced low (external or internal reference), the reference clock (U15 pin 11) is immediately forced high, which stops the clock and holds the synthesizer waveform at a dc level.

The 9-bit up/down counter (U6, U10, U11, and U14) counts from 0 to 499, then reverses and counts from 499 to 0. The counter steering circuit (U11, U16, and U18) watches for the top and bottom counts, then reverses the direction of the counter. When the counter increments, U17 pin 12 is low and pin 8 is high. At the top count, U18 pin 1 toggles high, disabling the counter for one cycle. Also at the top count, U17 pin 12 goes high and on the next clock pulse from U15 pin 11, U17 pin 8 (the counter up/down control line) goes low, causing the counter to begin to decrement, returning U18 pin 1 to its original low state. At the bottom count, U18 pin 1 again goes high, disabling the counter for one cycle. U17 pin 12 goes low, and on the next clock pulse from U15 pin 11, U17 pin 8 goes high, causing the counter to begin to increment. U18 pin 1 again returns low.

The counter output drives the inputs of EPROM (U9) which contains the data needed to produce the sine, triangle, ramp up, and ramp down waveforms. The status of lines FS0 and FS1 determine the waveform by selecting which block of data as accessed; see table 4-2. For sine and triangle waves, the EPROM produces one half cycle, negative to positive peak, on the up count (0 to 499), then uses the same data in reverse, positive to negative peak, on the down count (499 to 0). The data from the EPROM (U9) is latched through U8 to DAC U7.

Table 4-2. EPROM Control Lines

FS0	FS1	Function
0	0	DC
0	0	Sine wave
0	1	Triangle
1	0	Ramp up
1	1	Ramp down

The DAC converts the data from the EPROM into a current, SYNTH SIG, for the function selector.

The synthesizer can also produce ramp up and ramp down waveforms. These ramps are stored in the EPROM (U9), as are the sine and triangle waveforms. To produce the ramps, the line FS0 goes high. The line FS1 selects either the ramp up (FS1 low) or ramp down (FS1 high). In generating the ramps, the up/down counter functions the same as it does for triangles and sine waves; counting 0 to 499 and 499 to 0, except that the least significant bit to the EPROM is controlled by the data selector (U11, U12). The U/D line (U17 pin 9) is the complement of the line that causes the counter to count up or down. When counting up, U/D is low, which holds the least significant bit low. This allows only even addresses to be accessed. When counting down, U/D is high, the least significant bit is held high, and only odd addresses are accessed.

4.2.3 Stabilizer

The stabilizer serves two functions. First, it measures the generator's frequency and drives the frequency display. Second, it compares the displayed frequency,

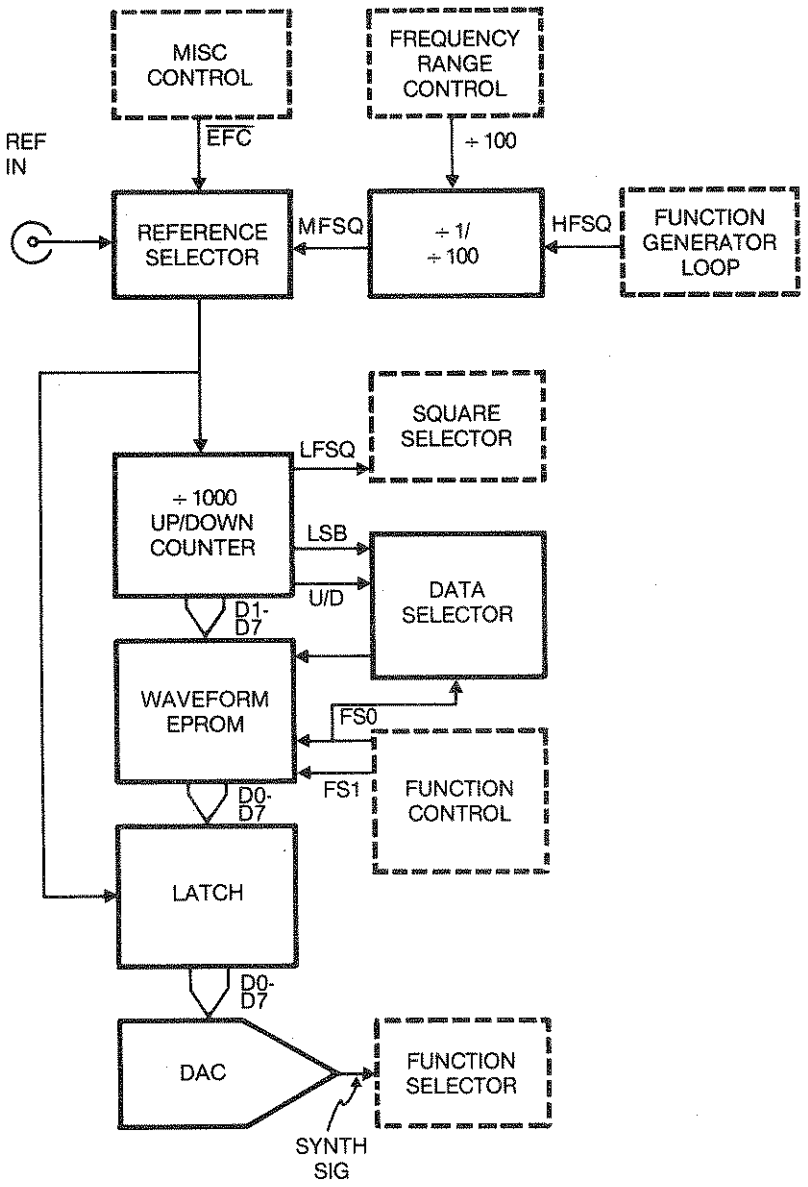


Figure 4-3. Waveform Synthesizer

two latches (U1B, U3B) and two comparators (U2B, U4B) controls the frequency correction or sweep block.

Latches: The latch (U1B, U3B) receives its data directly from the frequency counter. The MEMCLK, when it goes high for 20 μs, clocks the frequency data to the output registers of the latches. Outputs from the latch drive both the display drivers and Q inputs of the frequency comparators (U2B, U4B). The MEMCLK occurs approximately every 100 ms, see figure 4-5 for timing relationships.

When the stabilizer is enabled, the MEMCLK line remains low. This holds the frequency data (displayed frequency) stored in the latches.

Frequency Comparator: The frequency comparator consists of two individual comparators (U2B, U4B) which are daisy chained together via gate U6C. It monitors data from the frequency counter and compares it against the outputs from the latches. This produces two levels which control the up/down counter in the frequency correction or sweep circuit.

When the stabilizer is off, the P and Q lines are always the same (P = Q). When the stabilizer is on, the P data can change while the Q data remains unchanged. The comparator detects the change and switches its two output lines (U4B pins 1 and 19) as shown in table 4-4.

Table 4-4. Comparator — U/D Counter Relationship

Condition	U4B Pin 19	U4B Pin 1	Correction U/D Counter
P = Q*	Low	High	Counter Disabled
P<Q	High	High	Counts Up
P>Q	High	Low	Counts Down

NOTE

P = Frequency data from the frequency counter.
Q = Frequency data from the latches.
*Also Stabilizer off condition.

4.2.3.5 Frequency Correction or Sweep.

When the stabilizer is on, the frequency correction circuit (ref: schematic 0103-00-1115 sheet 3), controlled by the frequency comparator, makes frequency corrections to the function generator loop. This block consists of the 8-bit up/down counter (U9F, U8F) and the DAC (U8G) along with its summing amplifier (U9G).

8-Bit Up/Down Counter: The 8-bit up/down counter (U9F, U8F), controlled by two lines from the frequency comparator, uses its output to increment or decrement the DAC. Table 4-4 illustrates how the comparator controls the up/down counter. The FRCHG pulse clocks the counter every 100 ms; see figure 4-5. The line SWPT from the mode control logic maintains the data inputs to the counter at a TTL low. When the stabilizer is turned on, the STAB line from the misc control logic goes high to enable the counter. For stabilizer off, the STAB line goes low and on the next FRCHG clock transition the outputs all go to a TTL low except the most significant bit which is held high. The 8 data lines from the counter directly drive the inputs of the frequency correction DAC.

Digital to Analog Converter and Summing Amplifier: The digital to analog converter (U8G), DAC, converts the 8 bits of digital data from the 8 bit up/down counter into a proportional analog current. The amplifier (U9G) sums the DACs current to produce a voltage which, when the stabilizer is on, drives the ASWP input of the function generator loop. A resistor (R29) sets the DAC's fixed reference DAC range is ±2% of the set frequency..

4.2.4 Output Block

The output block, shown in figure 4-6, consists of the square buffer, square selector, square shaper, sine converter, function select, preamplifier, output amplifier, and attenuator. It also has output protection circuits for both Func Out BNCs. The output block selects the appropriate waveform and connects it to the Func Out BNCs.

4.2.4.1 Square Buffer

The square buffer (ref: schematic 0103-00-1116 sheet 2) amplifies the square wave from the function generator loop (Q11 collector). The output (HFSQ) drives the trigger logic, frequency counter, and square selector. The square buffer is similar to the switch buffer (ref: paragraph 4.2.1.6) except for output phasing and output level. Square buffer output is 0 to + 5V. A highly differentiated portion of HFSQ is coupled through C24, C25 and C31 to the triangle node. This signal counteracts switching transients which are coupled through the current switch diode bridge.

4.2.4.2 Square Selector

The square selector (ref: schematic 0103-00-1116 sheet 3) picks either HFSQ from the square buffer or the low frequency square wave from the synthesizer. Outputs from the square selector drive the square shaper and Sync Out connector.

Above the 1.1 kHz frequency range, LF (U20 pin 13) is low, which enables U20 pin 4; the output (U21 pin 6) is the complement of HFSQ. This signal goes to U16 pin 2) and through two overvoltage protection inverters (U21) to the Sync Out connector.

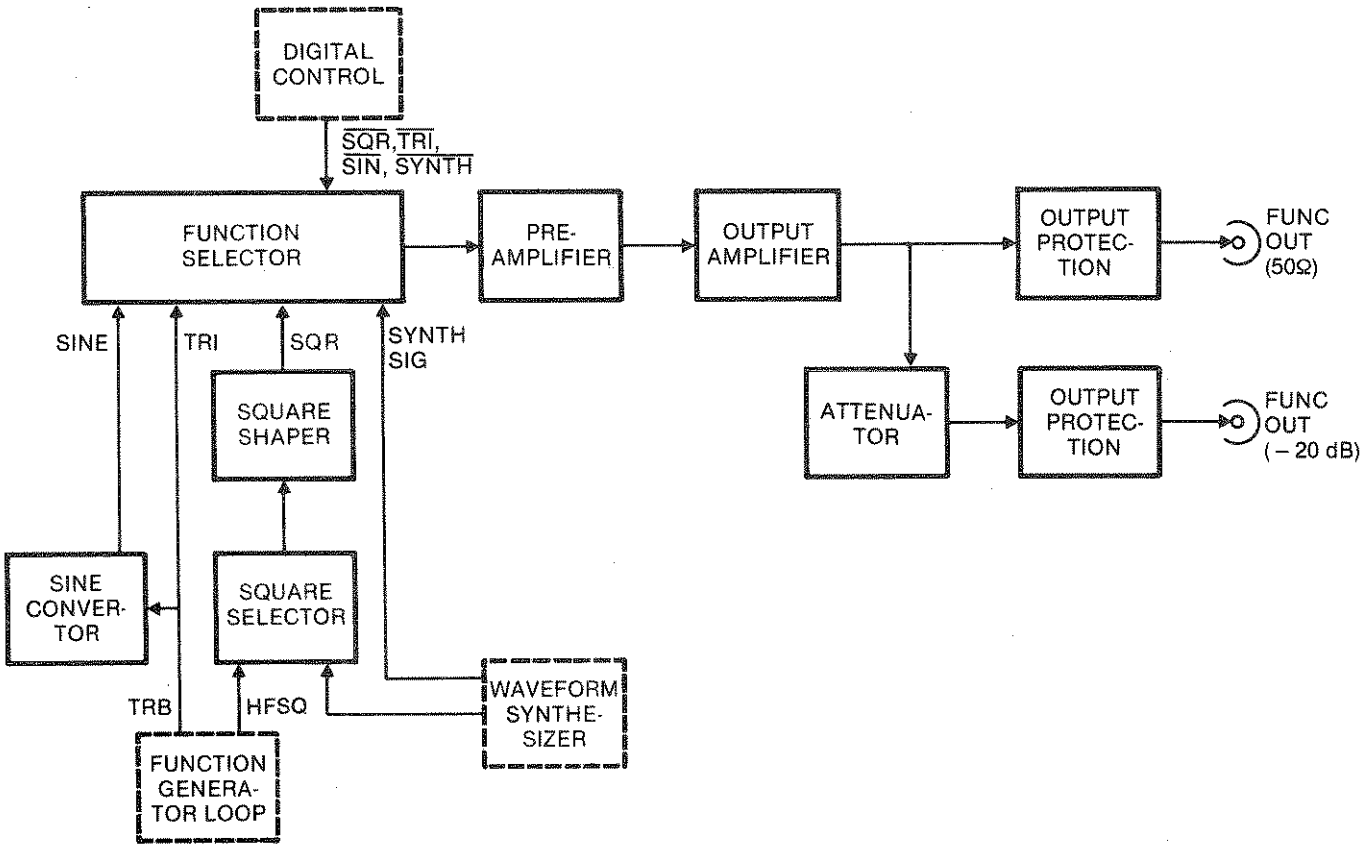


Figure 4-6. Output Block Diagram

For frequency ranges 1.1 kHz and below LF (U19 pin 9) is high, this enables U20 pin 3 and routes the square wave from the waveform synthesizer to U16 pin 2.

If Func is set to square wave, SQR at U19 pin 5 will be low, which puts U16 pin 1 high. The signal at U16 pin 2 will pass in phase to the square shaper via TTL SQ. For all functions other than square wave, SQR will be high disabling TTL SQ (U16 pin 12).

4.2.4.3 Square Shaper

The square shaper (ref: schematic 0103-00-1116 sheet 3) takes the TTL signal (TTL SQ) from the square selector and converts it to a clean, fast square wave current (± 1mA) that drives the preamplifier providing square wave is selected. The square wave is created by alternately sourcing and sinking current through the diode switch (CR36 through 39).

The voltage divider (R141, CR33, CR34, CR35, R144) converts TTL SQR to a bipolar signal, which switches the diodes in the square shaper. When TTL SQ is high, the voltage at the cathode of CR36 is approximately + 1.5V. CR38 sinks current from the TTL SQ signal while CR37 sources 1mA from the + 15V supply through U5 pin 6 to the preamplifier. When TTL SQ toggles low, the voltage at the cathode of CR36 is approximately – 1.5V. CR36 sources current to the TTL SQ signal and CR39 sinks 1mA from the preamplifier through U5 pin 6 to the – 15V supply. The current source and sink for upper and lower levels of square waves are independently adjustable by R142 and R147 respectively. Resistor R146 sets high frequency square wave peaking.

4.2.4.4 Sine Converter

The sine converter (ref: schematic 0103-00-1116 sheet 3) transforms the triangle into a sine wave for the function select. The sine converter uses the logarithmic response characteristics of the six matched diodes (U4) to approximate a sine wave current output. Buffered triangle output (TRB) enters the converter at U4 pins 2, 3, and 9. SIN DIST A trim pot (R121) adjusts the converter input for diode forward voltage variation. Two other adjustments, SIN DIST B and SIN DIST C (R132 and R137), balance the positive and negative peaks respectively. The current output is switched through FET switch

(U5) when $\overline{SIN}$ is low. TRI LEVEL trim pot (R126) adjusts the triangle form current that enters FET switch (U5) which is enabled by a low at $\overline{TRI}$.

4.2.4.5 Function Select

The function select circuit (ref: schematic 0103-00-1116 sheet 3) connects either the synthesizer output signal (SYNTH SIG), the square wave (TTL SQ), the sine converter output, or the buffered triangle (TRB) to the input of the preamplifier. Signal switching is handled by 4 section CMOS analog switch (U5). The synthesizer signal SYNTH SIG (U5 pin 14) is prevented from entering the preamplifier input (pin 15) until $\overline{SYNTH}$ goes low, which shorts pins 14 and 15 together. Switch bounce is prevented by C57 and C58 which eliminate ringing on the control line. Except for signal names and component numbers, the remaining 3 sections are identical and need no further discussion.

Both the triangle and sine FET switches (U5) are provided with increased isolation when they are not selected by shorting their inputs to ground through Q27 or Q28. For example, when $\overline{TRI}$ is high (not selected), Q26 is turned off, the collector of Q26 goes low, forward biasing Q27. This effectively shorts the emitter of Q27 together at ground.

4.2.4.6 Preamplifier

The preamplifier (ref: schematic 0103-00-1116 sheet 4) inverts and amplifies the signal current from the function selector to a sufficient voltage level for the output amplifier. The gain of the preamplifier is controlled by R184, which sets the sine wave amplitude. Zener diodes CR44 and CR45 convert the ±15V power supply voltages to ±9.4V.

4.2.4.7 Output Amplifier

The output amplifier (ref: schematic 0103-00-1116 sheet 4) provides the final gain and output drive capabilities of the instrument and is composed of an inverted summing amplifier (with a gain of about 10) for high-frequency signals, and a differential amplifier for dc and low-frequency signals. The differential amplifier also allows the dc offset of the Func Outputs.

AC Signal Path: High-frequency signals couple into the symmetrical emitter followers Q29 and Q32 through capacitors C91 and C92 respectively. These emitter followers drive the symmetrical inverter stage consisting of Q30 and Q33. Diodes CR46 and CR47, along with the 10Ω resistor R175, increase the switching speed of the output stage transistors Q31 and Q34 by maintaining a bias current which keeps them always partially on. The output signal (+ and − 20V, maximum) feeds back through resistors R176 and R177 to the input. Two 100Ω resistors (R196 and R197) set the output impedance for the Func Out (50Ω) connector.

DC Signal Path: The dc and low-frequency path in the output amplifier is through the transistor array (U26) connected as a differential amplifier. The output of the differential input stage (U26 pin 3), is inverted at U26 pin 9, and varies the current through transistor Q30. The signal at the collector of Q30 changes until the fed back signal through R176 and R177 balances with the input, either signals through R166 or offset through R167 and R168. The PNP transistors (U26) balance the current through the differential input pair and provide a high impedance load for the first stage output. Capacitor C85 limits the speed of this section at high frequencies.

Offset Circuit: When the D.C. Offset switch is turned on, the voltage on the wiper of R3 is converted to current through R167 and R168. This current is proportional to the voltage and polarity at the wiper of R3 and enters the summing node to provide dc control of the input current, and therefore the output voltage offset.

4.2.4.8 Attenuator

The attenuator (ref: schematic 0103-00-1116 sheet 4), consists of a 498Ω resistors (R198 and R199) and a 54.9Ω resistor (R200), provides 20dB of attenuation at 50Ω output impedance to the Func Out (−20dB) connector.

4.2.4.9 Output Protection

The output protection circuits (ref: schematic 0103-00-1116 sheet 4) guard the output amplifier from excessive external voltages that could be accidentally connected to either of the Func Out BNCs that could damage the instrument.

There are two safeguards to protect the output amplifier.

1. Two in-line fast-blow fuses for each Func Out connector.
2. Four voltage-limiting, high current diodes (CR50 through CR53) that provide additional protection at the Func Out (50Ω) connector.

4.2.5 Pushbutton Interface

When a front panel pushbutton is pressed, one of the inputs to the pushbutton interface (ref: figure 4-7 and schematics 0103-00-1115 sheet 1 and 0103-00-1117) is connected to either +5V or ground reversing the logic level of the appropriate pushbutton interface output. The MAN TRIG line from the pushbutton interface goes to the trigger logic, while the remaining lines go to the digital control block. Each switch drives a Schmitt trigger gate. RC circuits prevent multiple pulsing at the input of each gate. Outputs drive the appropriate control circuit within the unit.

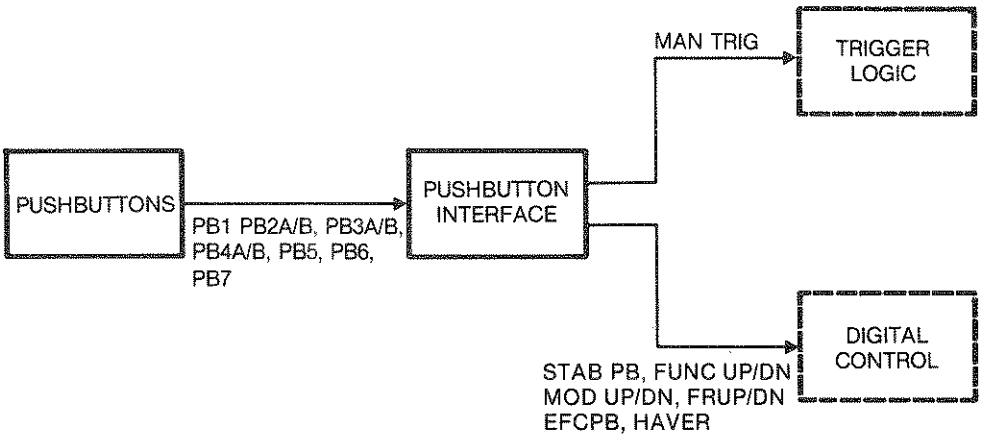


Figure 4-7. Pushbutton Interface

4.2.6 Digital Control

The digital control block (figure 4-8) consists of the power on reset, mode control, misc. control, frequency range control and function control circuits.

4.2.6.1 Power-On Reset

The power-on reset circuit (ref: schematic 0103-00-1115 sheet 3) sets all other digital control block circuits to an initial state. On initial power up, C57 holds U3G pin 13

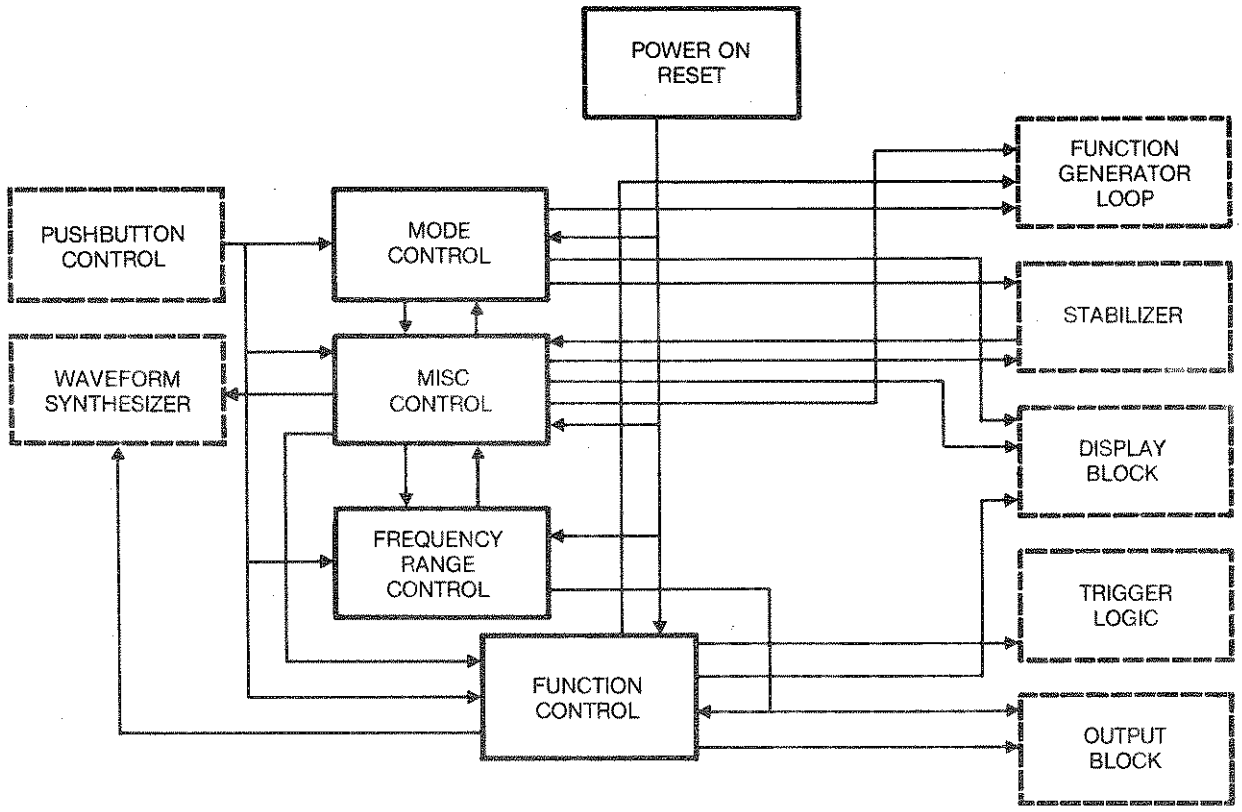


Figure 4-8. Digital Control

low, MR (U3G pin 12) goes high, and $\overline{MR}$ (U3G pin 4) goes low; MR and $\overline{MR}$ reset the various digital control circuits. After about ½ second, C57 charges to approximately 2.5V, pin 12 (MR) toggles low, and pin 4 ($\overline{MR}$) toggles high. These levels now remain constant for the remainder of the time the unit is on.

4.2.6.2 Mode Control

As the Mode pushbutton control lines (ref: figure 4-9) are pulsed, the mode control circuit steps through a sequence of modes either up (MOD UP) or down (MOD DN). This selects one of the output mode lines low. These mode lines, in conjunction with additional logic gates, control the trigger logic, stabilizer, display block, and misc control. External frequency control ($\overline{EFC}$) combines with $\overline{CONT}$ and $\overline{STOP}$ to produce BL.

The mode control circuit (ref: schematic 0103-00-1115 sheet 2) contains the up/down counter (U4G), which has separate "count up" and "count down" inputs, and receives pulsed signals from U5G originating from the MOD UP and MOD DN pushbutton buffers. The output of this counter drives decoder U4F, which selects one of the available modes. The two NAND gates (U5G) serve to prevent any fruther up or down count beyond the capability of the unit. At one extreme (Cont Mode), U5G pin 8 is low, causing pin 10 to remain high at all times, disabling pin 9. In the other extreme, (Gate Mode), U5G pins 11, 12, and 13 perform the same function. The lines $\overline{SWPT}$ and $\overline{SWP}$ always reamins low, while the line $\overline{SWP}$ always remains high. MC0 and MC1 control the trigger logic. $\overline{CONT}$ controls the misc. control. $\overline{GATE}$; $\overline{TRIG}$, and $\overline{CONT}$ enable the appropriate segment on the front panel display. In Trig or Gate Modes, BL disables all number segments of the display.

4.2.6.3 Misc Control

The misc control circuit (ref: figure 4-10 and schematic 0103-00-1115 sheet 2) performs various functions within the instrument. Its circuits selects the internal or external references, enables or disables the haverwaves, and turns on or off the stabilizer.

Internal/External Reference: The reference counter (U8C) receives a pulse from the pushbutton interface circuit (U3G pins 10 and 11) each time the Ref pushbutton is pressed. This causes the counter output (U8C pin 3) to change states. The output (EFC) turns on and off the Ext Ref annunicator. The inverter (U8D) inverts the EFC input to produce $\overline{EFC}$ which blanks the display (BL), selects the reference source, turns on and off the Int Ref annunciator, and selects the synthesized waveform.

Haverwave: The haver wave counter (U7A) receives a pulse from the pushbutton interface (U3G pin 6) each time the Haver pushbutton is pressed. This causes the counter output (U7A pin 3) to change states. To enable the haver wave, both the counter output and the line LF must be high which causes lines THAV and CHAV to be high. THAV controls the trigger logic circuit and CHAV enables the Hav annunciators. LF is high when external reference is selected or the synthesized frequency ranges are selected or both.

Stabilizer: The stab flip-flop (U6F) receives a pulse (STABPB) from the Pushbutton Interface. Since both J/K inputs to U6F (pins 10 and 11) are always high, the two flip-flop outputs (pins 14 and 15) change state each time the flip-flop receives a STABPB pulse. When the stabilizer is off, STAB is high. U4E inverts $\overline{STAB}$ to produce STAB which, when low, MEMCLK is pulsed with each transition of U7E pin 13. When the stabilizer is on, $\overline{STAB}$ is low, making STAB high, which in turn holds MEMCLK low at all times. With $\overline{STAB}$ low, VCG KILL is high, disconnecting the VCG In BNC from the input of the VCG circuit. The stabilizer is disabled by U6G pin 1 if UNSTAB (U6G pin 3) goes low, caused by the freq going out of range, or if the unit is in any mode other than Cont.

4.2.6.4 Frequency Range Control

The frequency range control circuit (ref: figure 4-11 and schematic 0103-00-1115 sheet 2) steps through a sequence of frequency ranges. As the Freq Range pushbutton is pressed, the pushbutton interface detects whether the frequency range should increase (FRUP) or decrease (FRDN). The circuit's output lines control the stabilizer, display block, output block, function control, and misc control. External frequency control ($\overline{EFC}$) combines with other control lines to produce LF.

Up/down counter (U6E), which has separate "count up" and "count down" inputs, receives pulsed signals from U5F originating from the freq range (FRUP and FRDN) pushbutton buffers. The output of this counter drives decoder (U6D), which selects one of its output lines to be low. $\overline{FR7}$, which controls the HF COMP on the analog board and goes to the frequency counter, is driven directly by one of these lines. From the remaining output lines are decoded the appropriate frequency range control lines (FR4, FR5, and FR6), which are inverted by the frequency counter circuit before going to the analog portion of the generator. The 9 output frequency ranges of the generator originate from these 4 control lines (FR4, FR5, FR6, and $\overline{FR7}$), the low frequency synthesizer, and the ÷ 100 control line. In the 5 lowest ranges, LF is high which, unless square function is selected, enables $\overline{SYNTH}$ (through the function control). This connects the output of the LF waveform synthesizer to the input of the preamplifier. The output frequency of the synthesizer is 1/1000th of the range selected. For example, if FR5

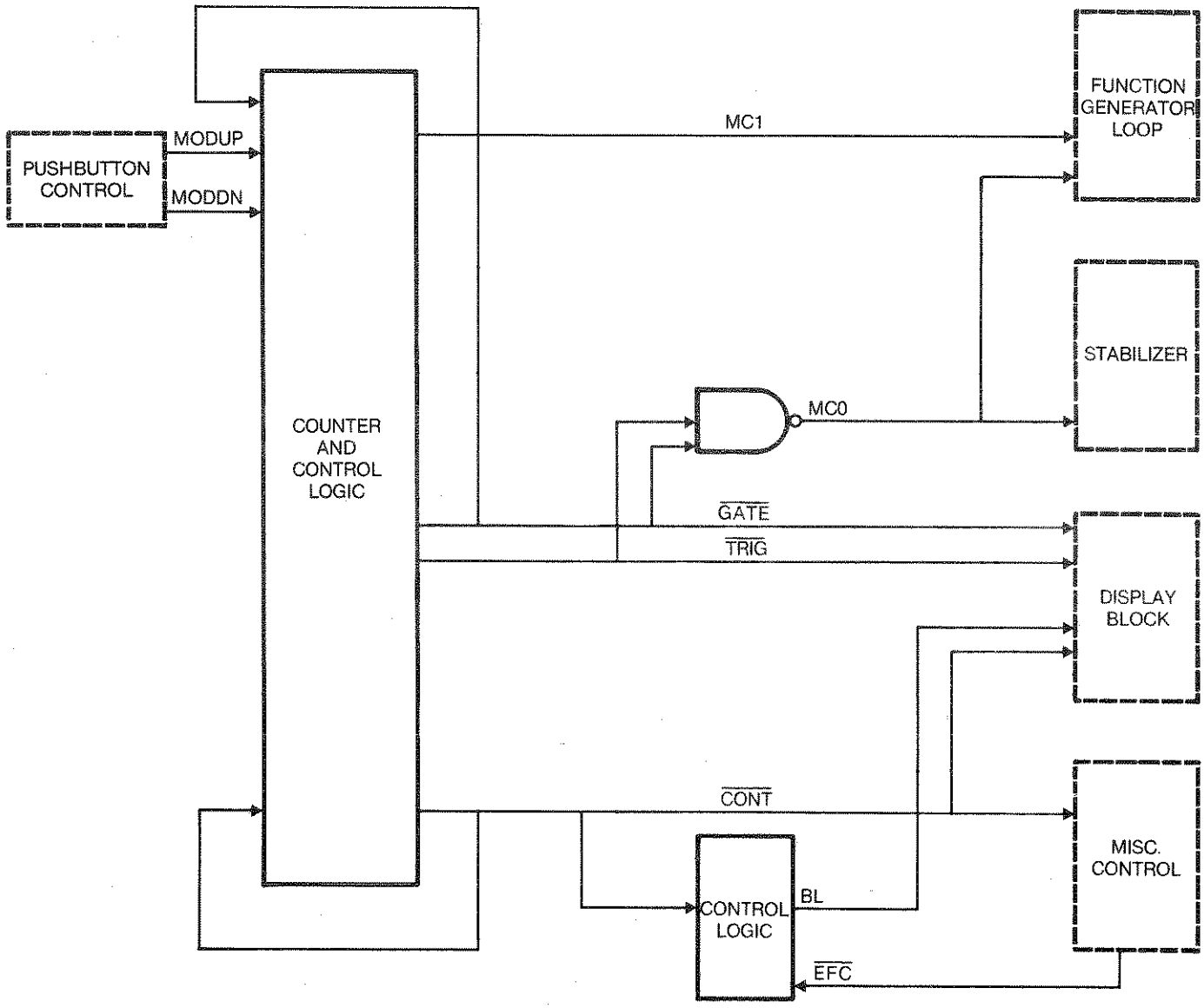


Figure 4-9. Mode Control

(110kHz range) is selected, the output frequency range of the synthesizer (and therefore the Func Out connectors), would be 110Hz. In addition, in the 3 lowest ranges, $\overline{\div 100}$ is low, further dividing this signal by 100. Using the same example, the synthesizer output frequency range would now be 110 mHz. Two NAND gates (U5F), serve to prevent any up or down count beyond the capability of the unit. At one extreme (110mHz frequency range), U5F pin 1 is low, causing pin 3 to remain high at all times, disabling pin 2. In the other extreme, (11.00 MHz), U5F pins 8, 9, and 10 perform this function.

On the display, DmHz controls the "mHz" emblem, DHz controls "Hz", DK controls "K", and DMHz controls "MHz". The decimal points are controlled by DDP1, DDP2, and $\overline{\text{DDP3}}$.

4.2.6.5 Function Control

The function control (ref: figure 4-12 and schematic 0103-00-1115 sheet 2), steps through a sequence of functions. As the Func pushbutton is pressed, the Pushbutton Interface detects whether the function should increase (FUNCUP) or decrease (FUNCDN). The

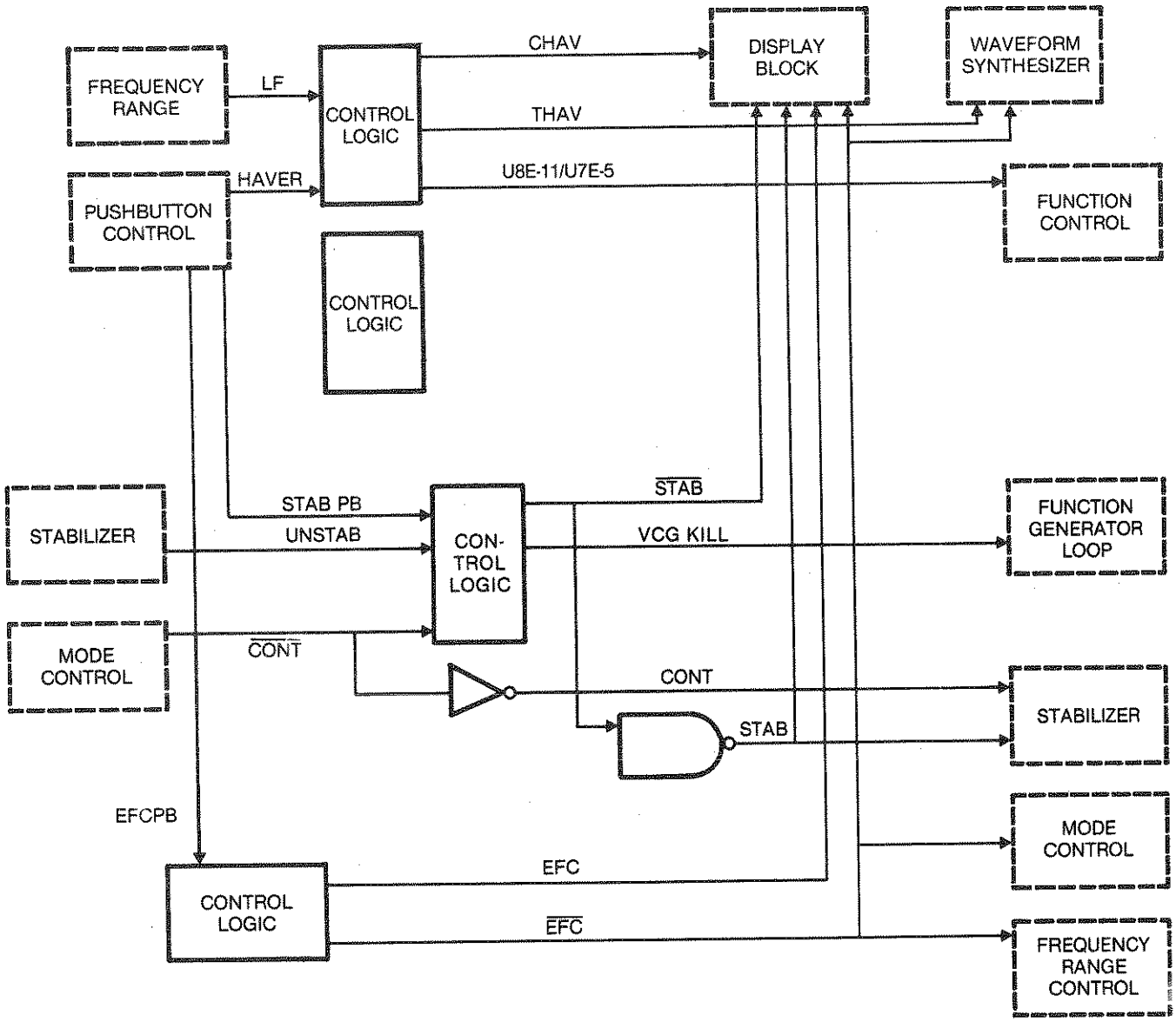


Figure 4-10. Misc Control

circuits output lines control the waveform synthesizer, display block, output block, and trigger logic.

Up/down counter U5D, which has separate "count up" and "count down" inputs, receives pulsed signal from U5F originating from the FUNC UP and FUNC DN pushbutton buffers. The output of this counter drives decoder U4D, which selects one of the available functions. The two NAND gates (U5F) serve to prevent any further up or down count beyond the capability of the unit. At one extreme (DC), U5F pin 13 is low, which causes pin 11 to remain high at all times and disables pin 12. In the other extreme, (negative going ramp), U5F pins 4, 5, and 6 perform the same function. In the nonsynthesized frequency ranges, output lines $\overline{TRI}$, $\overline{SIN}$, and $\overline{SQR}$ select the waveform to be sent to the preamplifier. When LF (from the frequency range control circuit) is high and the unit is in sine, triangle, or either ramp function, $\overline{SYNTH}$ is low which connects the output of the LF waveform synthesizer to the input of the preamplifier. FS0 and FS1 select the waveform at the LF waveform synthesizer output. When the unit is in square function, $\overline{SQR}$ is low, which connects the output of the Square Shaper to the input of the preamplifier. $\overline{\wedge}$, $\overline{\sqcup}$, $\overline{\sim}$, $\overline{\diagdown}$, $\overline{\diagup}$ enable the appropriate segment on the front panel display.

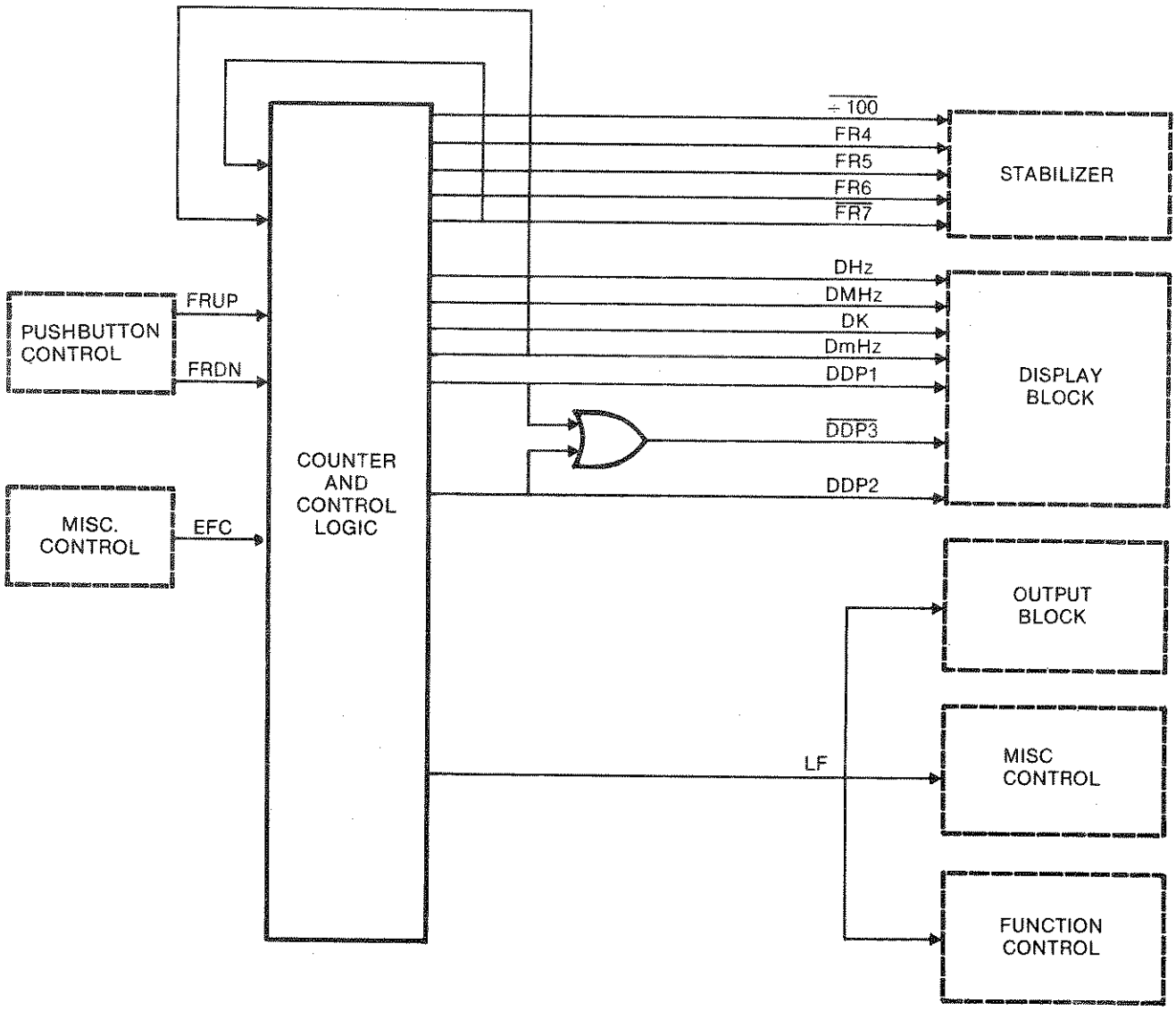


Figure 4-11. Frequency Range Control

4.2.7 Display Block

The display block (ref: figure 4-13 and schematics 0103-00-1115 sheet 1 and 0103-00-1117) consists of the display drivers and the display. Two 30 Hz signals, (BP and its complement $\overline{BP}$) originating from U5C, synchronize the LCD and the segment drivers. To enable a segment of the display, 5Vrms is needed between BP and the control line for that segment. Therefore, BP and the segment control line must be out of phase from each other.

The following example explains all exclusive-or gates which drive the bars, arrows, and decimal points on the display. When the unit is in Cont Mode, U3F pin 9 ($\overline{CONT}$) is low. The $\overline{BP}$ signal at pin 8 is in phase with the signal at pin 10 (Z3) and is therefore out of phase with BP. This results in a rms voltage of 5V between BP and Z3, enabling the segment. When the unit is not in Cont Mode, a high at pin 9 causes the output at pin 10 to be in phase with BP, resulting in an rms voltage of 0V, disabling the segment. Data for these gates originate from the various digital control circuits in the unit.

Lines D2A through D4D, which originate from the frequency comparator, determine which number segments are enabled. Each output line (2A through 4G) drives a

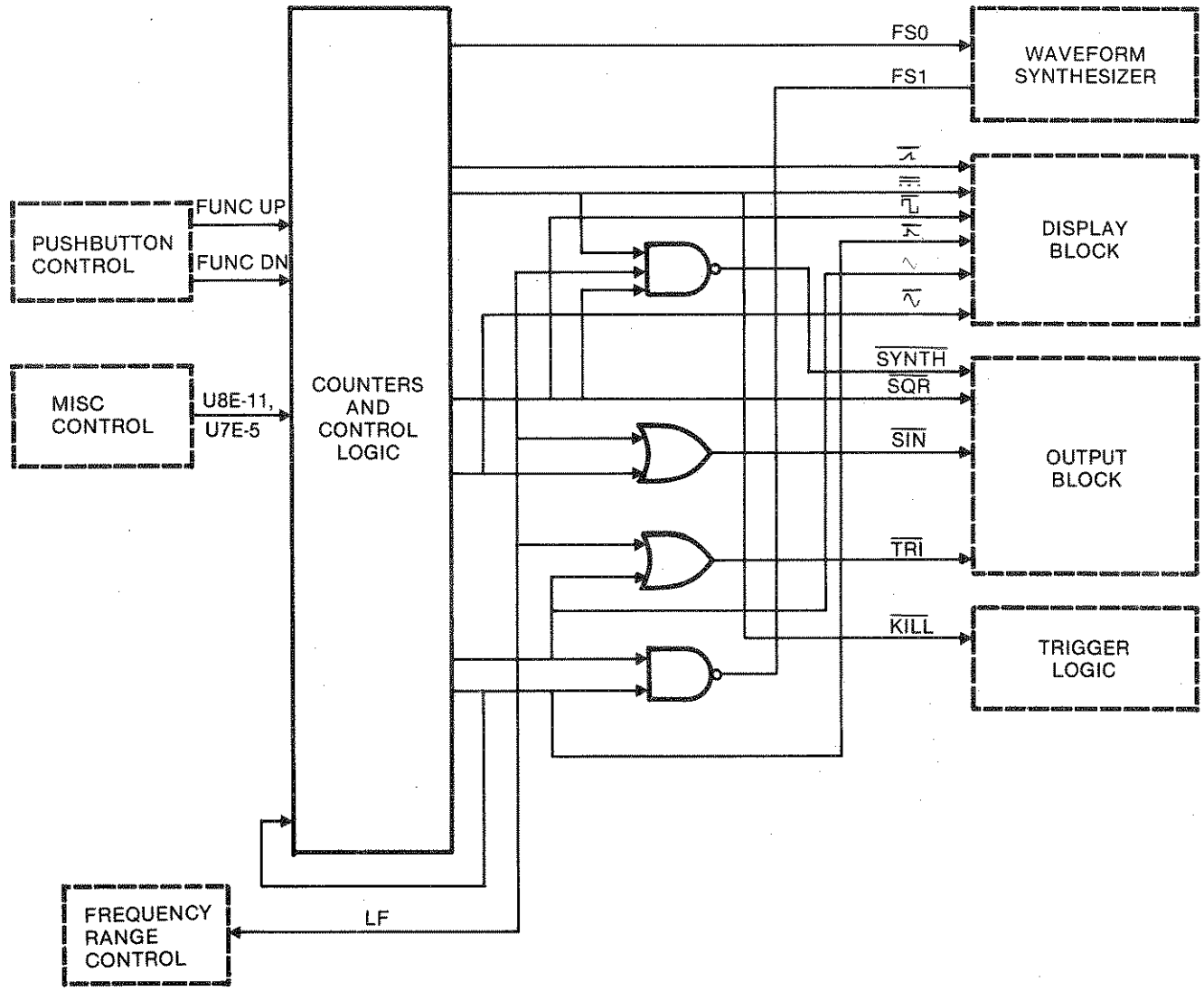


Figure 4-12. Function Control

number segment except in Trig or Gate Modes when they are disabled by BL.

4.2.8 Power Supply

Three power supply voltages, +15V, −15V, and +5V are generated on the power supply circuit board (ref: schematic 0103-00-1113).

4.2.8.1 +5V Supply

In the +5V supply, ac from the transformer T1 (located on the rear panel), is rectified by CR2 and filtered by C9, C10, and C11 to provide unregulated dc for regulator VR2. This three-terminal regulator normally operates with a 1.25V difference between its input and output terminals. C12 provides additional filtering at the output of the regulator.

4.2.8.2 ±15V Power Supplies

The ±15V Power Supplies provide power to the analog sections of the instrument. R2, which is in series with the output of the +15V regulator, causes current limiting to take place at a lower value than the internal limiting provided by the regulator. As the current through R2 reaches its limiting value, the voltage drop across R2 reaches 0.4V. Any further current through R2 causes the regulator to lower the output voltage until the current falls back to the limiting value.

The −15V supply operates similarly to the +15V supply, however the polarities are reversed.

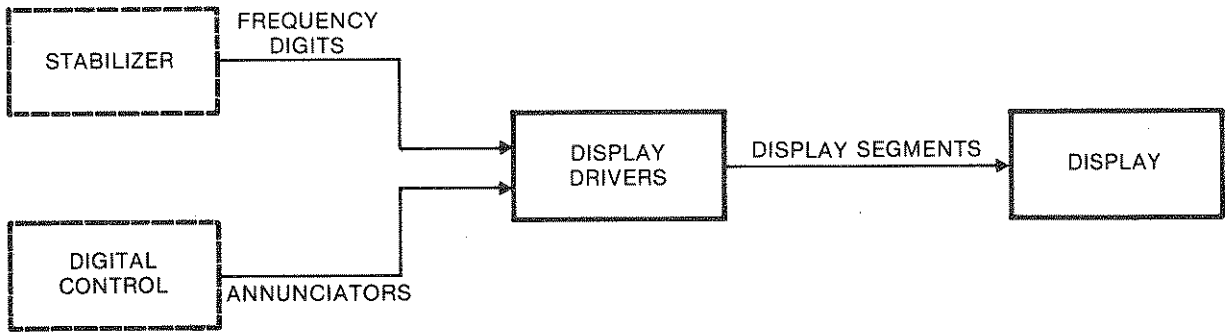


Figure 4-13. Display Block

SECTION 5
CALIBRATION

5.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize turnaround time.

5.2 REQUIRED TEST EQUIPMENT

Voltmeter . . . . . Millivolt dc measurement (0.1% accuracy), true rms
Oscilloscope, Dual Channel . . . ≥100 MHz bandwidth
Counter . . . . . ≥20 MHz (0.01% accuracy)
50Ω Feedthru . . . . . ±0.5% accuracy, 2W
Distortion Analyzer . . . . . To 200 kHz
RG58U Coax Cable . . . 3 ft length BNC male contacts
Spectrum Analyzer . . . . . To 60 MHz

5.3 CALIBRATION

NOTE

Before removing the cover, disconnect the instrument from the ac power source. Refer to Section 2 for cover removal, except leave top cover on and remove only bottom cover for calibration. Invert the instrument so generator board adjustments are on top and place the bottom cover on top of the unit to maintain the operating temperture during calibration.

After referring to the following preliminary data, perform calibration, as necessary, per table 5-1. If performing partial calibration, check previous settings and adjustments for applicability. Figure 5-1 shows waveform generator board calibration points.

NOTE

The completion of these calibration procedures returns the instrument to correct calibration. All limits and tolerances given in these procedures are calibration guides and should not be interpreted as instrument specifications. Instrument specifications are given in Section 1 of this manual.

1. All measurements made at the FUNC OUT connector must be terminated into a 50Ω (±0.5%) load.

WARNING

With the covers removed, dangerous voltage points may be exposed. Contact with any of these points could cause serious injury or death.

2. Start the calibration by removing the bottom cover, connecting the unit to an ac source, and setting these front panel switches as follows:

Frequency
  Fine . . . . . CW
  Coarse . . . . . CW
Amplitude . . . . . CW
D.C. Offset . . . . . Off

3. Allow the unit to warm up at least 30 minutes for final calibration. Keep the instrument covers on to maintain heat. Lift bottom cover only to make adjustments or measurements.

Table 5-1. Calibration Procedure

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
1	Power Supply Regulators	DC Voltmeter	J10 Pin 2	Paragraph 5.3 step 2			Black (−) lead ground
2			J10 Pin 5			−15V ± 350 mV	Red (+) lead dc volts
3			J10 Pin 6			+5V ± 250 mV	
4			J10 Pin 7			+15V ± 350 mV	
5	Triangle Amplifier Balance		J10 Pin 3		R103	0V ± 100 mV	Rough adjustment only
6					R86	0V ± 20 mV	
7	Function Out	Scope	Func Out (50Ω)			10Vp-p sine wave (Approximately 2 cycles)	Terminate with 50Ω Scope Settings: 2V/div. 0.2ms/div.
8				Step Func button to right		Functions match display (correct amplitude and frequency)	
9	Output Amplifier Balance			Func: ⎓ (dc)	R157	0V ± 10 mV	Display shows 00.0 kHz Scope setting: 10 mV/div. (or maximum scope sensitivity if more than 10 mV)
10	Trigger Baseline			Freq range: step to right twice to 110.0 kHz range Func: ∿ Mode: Trig	R103	0Vdc ± 50 mV	Scope setting: 0.1V/div. Verify baseline 0VDC ± 100 mV over full range of Coarse Frequency knob (Frequency Fine knob full cw)
11	VCG Zero	DC Voltmeter	VCG In BNC	MODE: CONT Func: ⊓⊔ Frequency knobs: both fully ccw	R11	0V ± 0.5 mV	Use coax cable with no termination
12	1100:1 Frequency	Scope	Func Out (50Ω)		R13	First transition occurs at center vertical grid line, for 50 Hz.	Use coax cable with 50Ω termination Scope settings: 2V/div. 2ms/div. Trigger slope: − (Neg) Horizontal position: Trace begins at extreme left vertical grid line
13	1100:1 Symmetry				R38	Second transition occurs at extreme right vertical grid (within 2% (1 minor division)	Repeat steps 12 and 13 if necessary. Alternate method: magnify X10 and alternate trigger slope between + and −, set R38 for <2 divisions assymetry.
14	High Symmetry			Frequency knobs: fully cw Freq Range: 11.00 kHz	R20	<0.1% (½ minor div.) symmetry	Scope setting: 2V/div. 10μs/div. X10 Magnification, alternate trigger slopes while adjusting R20 for minimum assymetry.

Table 5-1. Calibration Procedure (Continued)

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
15		Scope	Func Out (50Ω)	Coarse Frequency: 5kHz	Verify only	<0.5% asymmetry (Verify <2½ minor divisions)	Scope setting: 20μs/div. Magnification: Off
16	Sine Distortion	Distortion Analyzer		Frequency knobs: fully cw Func: ∿	R121, R132, R137, R86	Minimum distortion (typically 0.2 to 0.3%)	Adjust R86 slightly if necessary.
17	Full Scale Frequency	Counter		Func: ⊓	R1	11.15 kHz on display	Display reads same as counter ± 0.01 kHz
18		Display		Switch between Range: 11 kHz and 110 kHz Freq Ranges		11 kHz Freq Range: 11.05 kHz to 11.25 kHz. 110 kHz Freq Range: 110.5 kHz to 112.5 kHz.	Set for best frequency balance between freq ranges. C44 (.001 μF nominal value) trims 11.00 kHz range.
19	11:1 Frequency			Freq Range: 110 kHz Frequency Coarse knob: fully ccw	Verify only	10 kHz ± 2 kHz on display	
20	High Frequency Calibration			Frequency knobs: fully cw Freq Range: 1.100 MHz	C40	1.115 MHz ± .005 MHz on display	C41 may be trimmed to obtain equal adjustment above and below 1.110 MHz
21				Frequency Coarse knob: fully ccw		Note display reading	
22				Freq Range: 11.00 MHz Frequency Coarse knob: fully ccw	C38	Set for 10 times reading noted in previous step	C39 may be trimmed to obtain equal adjustment above and below goal frequency
23				Frequency knobs: fully cw	R80	11.15 MHz ± .05 MHz	
24	Amplitude	True rms Voltmeter		Func: ∿ Freq Range: 11.00 kHz Freq Coarse Knob: fully ccw	R184	3.55 Vac ± 0.015 Vac (3.535 Vac to 3.565 Vac)	
25				Func: ∿	R126	2.90 Vac ± 0.015 Vac (2.885 Vac to 2.915 Vac)	
26				Frequency knobs: fully cw Freq Range: 1.100 kHz	R151		

Table 5-1. Calibration Procedure (Continued)

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
27	Amplitude	DC Voltmeter	Func Out (50Ω)	Freq Range: 110.0 mHz Function: ⊓⊔	R142	+5.025 Vdc ± 0.025 Vdc +5.00 Vdc to 5.05 Vdc on positive peak	Turn frequency coarse knob fully ccw to hold each peak while adjusting, then return cw
28					R147	−5.025 Vdc ± 0.025 Vdc −5.00 Vdc to −5.05 Vdc on negative peak	
29	Waveform Quality and Frequency Response	Scope		Frequency knobs: fully cw Freq Range: 1.100 MHz Amplitude: 8Vp-p	R146	Minimum aberations <4% (320 mV)	Scope settings: 2V/div. 0.1 μs/div. (Observe peak-to-peak aberations at 0.5V/DIV by adjusting vertical position)
30				Amplitude: fully cw		Rise/Fall <22 ns	Scope settings: X10 Magnification
31				Func: ∿ Frequency knobs: fully cw Freq Range: 11.00 MHz	Verify only	Amplitude between 8.6V and 10V inclusive	Scope settings: Magnification Off
32		Spectrum Analyzer		Freq Range: 1.100 MHz		Harmonics less than −40 dBc from 1.1 MHz to 0.1 MHz	Rotate coarse freq control through its range and return fully cw
33				Freq Range: 11 MHz		Harmonics less than −28 dBc from 11 MHz to 1 MHz	
34	D.C. Offset	Scope or DC Voltmeter		Function: ⎓ (dc) D.C. Offset: fully cw		Minimum +5VDC	Calibration complete, start of functional check out.
35				D.C. Offset: ccw (not in detent)		−5VDC or more negative	
36	−20 dB Output	Scope		D.C. Offset: Off Func: ⊓⊔ Frequency knobs: fully cw Freq Range: 11.00 kHz		Approximately 10Vp-p square wave	Scope settings: 2V/div. 20μs/div.
37			Func Out (−20 dB)			Approximately 1Vp-p square wave. Note value.	Scope settings: .2V/div.
38			Func Out (50Ω)	Amplitude: fully ccw		Verify Vp-p less than value noted in step 37	

Table 5-1. Calibration Procedure (Continued)

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
39	Sync Out	Scope	Sync Out	Amplitude: fully cw	Verify only	Normal TTL level square wave	Remove 50Ω termination Scope setting: 2V/div.
40	Trigger, Gate and Haver			Mode: Trig		Display shows Trig (numbers blanked)	Approximately 0Vdc
41			Func Out (50Ω)	Func: ∿		Verify triggered sine wave	Connect 1kHz TTL signal from external source to channel 2 and Trig In (TTL) BNC. Scope settings: .2ms/div. Trigger to channel 2 Monitor channel 1
42				Mode: Gate		Display shows Gate Verify gated sine wave	
43				Freq Range: 1.100 kHz Haver: On		Gated Haversine	Change external signal at Trig In (TTL) BNC to 100 Hz Scope settings: 2ms/div.
44	Manual Trigger			Haver: Off		Sine wave when Trigger button pressed	Disconnect external signal source, scope channel 2 and Trig In (TTL) Trigger to channel 1
45	VCG In			Mode: Cont Freq Range: 110.0 kHz Frequency knobs: fully ccw Func: ⊓		Display shows 110 kHz ± 5 kHz	Connect +5VDC to VCG In BNC. Verify STAB is off.
46						Verify one cycle >5 divisions	Remove voltage from VCG In BNC Scope setting: 2ms/div.
47	External Reference			Frequency knobs: fully cw Freq Range: 1.100 kHz Func: ∿ Ref: Int		Waveform changes to DC at various voltage levels as Ref In (TTL) BNC intermittently shorted to ground	Scope setting: .2ms/div.
48				Ref: Ext		Slightly over 2 cycles displayed on scope. Instrument display blanked	Connect 1.1 MHz TTL signal to Ref In (TTL) BNC

Table 5-1. Calibration Procedure (Continued)

Step	Check	Tester	Test Point	Control Setting	Adjust	Result	Remarks
49	Stab	Scope	Func Out (50Ω)	Stab: Off Ref: Int Frequency Fine: initially centered Frequency Coarse: adjust for 500Hz Func: ⊓⊔ Stab: On	Verify only	Quickly turn Frequency Fine knob as indicated and verify the following: 1) Rotate fine control cw to move transition from center to 3 cm 2) Transition travels approximately 2 centimeters toward center of scope display 3) Transition jumps back to 3 centimeters left of center grid line 4) Stab now Off	Disconnect Ref In BNC Scope settings: X10 Magnification: On Adjust horizontal position for square wave transition at center vertical grid line Stab automatically disengages when it reaches its electrical limit.
50				Use Frequency Fine knob to return square wave transition to center vertical grid line Stab: On		Same as step 49 in opposite direction	Repeat as in step 49 except turn Frequency Fine knob ccw to initially move transition 3 centimeters right
51	Frequency Ranges			Frequency knobs: fully cw		Display reads between 1.105 kHz and 1.125 kHz.	Scope settings: 50μs/div. X10 Magnification: Off Set horizontal variable for 1 cycle on screen
52				Freq Range: 110.0 Hz		Display reads between 110.5 Hz and 112.5 Hz. Scope screen shows 1 cycle.	Scope setting: 0.5ms/div.
53				Freq Range: 11.00 Hz		Display reads between 11.05 Hz and 11.25 Hz. Scope screen shows 1 cycle.	Scope setting: 5ms/div. Trigger mode: Normal
54				Freq Range: 1.100 Hz		Display reads between 1.105 Hz and 1.125 Hz. Scope screen shows 1 cycle.	Scope setting: 50ms/div.
55				Freq Range: 110.0 mHz		Display reads between 110.5 mHz and 112.5 Hz. Scope screen shows 1 cycle.	Scope setting: 0.5 sec/div.

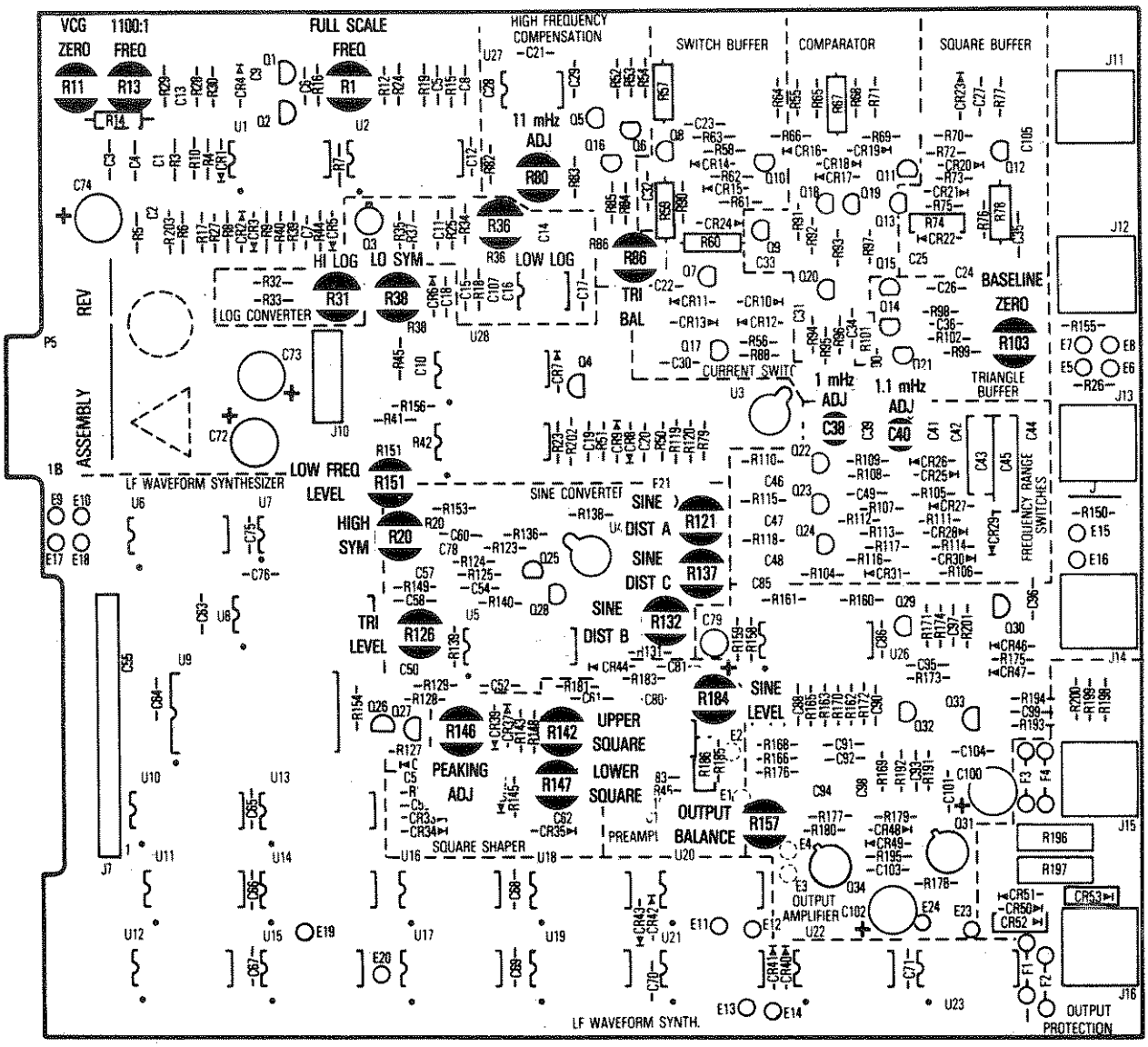


Figure 5-1. Calibration Points