INSTRUCTION MANUAL

Model 275

12 MHz Programmable Arbitrary Function Generator

WAVETEK®

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SAFETY FIRST

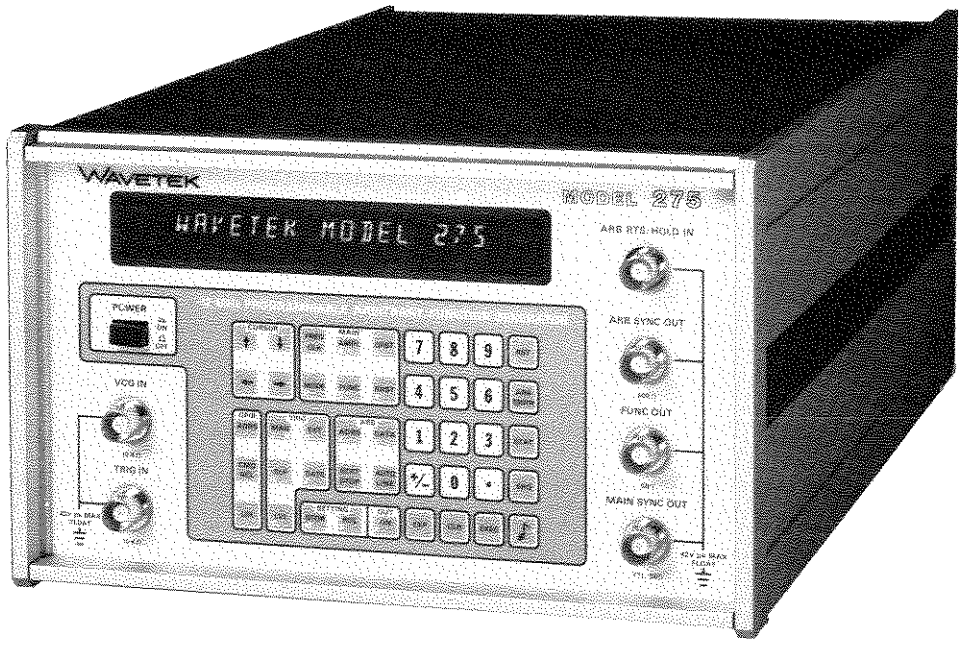
Protect yourself. Follow these precautions:

- Don't touch the outputs of the instrument or any exposed test wiring carrying the output signals. This instrument can generate hazardous voltages and currents.
- Don't bypass the power cord's ground lead with two-wire extension cords or plug adaptors.
- Don't disconnect the green and yellow safety-earth-ground wire that connects the ground lug of the power receptacle to the chassis ground terminal (marked with ⏚ or ⚠).
- Don't hold your eyes extremely close to an rf output for a long time. The normally nonhazardous low-power rf energy generated by the instrument could possibly cause eye injury.
- Don't plug in the power cord until directed to by the installation instructions.
- Don't repair the instrument unless you are a qualified electronics technician and know how to work with hazardous voltages.
- Pay attention to the **WARNING** statements. They point out situations that can cause injury or death.
- Pay attention to the CAUTION statements. They point out situations that can cause equipment damage.

WARNING

This instrument normally contains a lithium battery. Where lithium is prohibited, such as aboard U.S. Navy ships, verify that the lithium battery has been removed.

Do not recharge, short circuit, disassemble, or apply heat to the lithium battery. Violating this rule could release potentially harmful lithium. Observe polarity when you replace the battery.



Model 275, Programmable Arbitrary/Function Generator

SECTION 1
GENERAL DESCRIPTION

1.1 MODEL 275

The Wavetek 275 Programmable Arbitrary/Function Generator produces sine, triangle and square waveforms as well as user-defined arbitrary waveshapes. Any of the waveforms can be generated in the continuous, triggered, gated or burst modes. External width and dc functions are also provided.

Data entry is from the front panel or GPIB (IEEE 488-1978). Numeric input is entered in free format: fixed, floating, or exponential notation. Parameters may be entered in any order. Internally, all entries are interactively checked for errors and displayed on the front panel, or they may be accessed through the GPIB.

Arbitrary waveform amplitude resolution is 12 bits. Horizontal resolution is 2048 points (standard), expandable to 8192 points (optional). Arbitrary waveform clock period is programmable within the range of 267 ns to 267 s per point with 0.2% accuracy. Non-arbitrary waveform frequency range is 0.01 Hz to 12 MHz.

Output level is specified from 10 mV to 10 Vp-p into a 50Ω termination and 20 mV to 20 Vp-p into an open circuit with 3 digits of resolution. Offset can be programmed to vary the waveform base line up to ±10V, or in the dc function, to vary the dc output.

All inputs and outputs are protected against short circuits and excessive voltages between ±15V. The function output is further protected against voltage inputs up to 140 Vac or ±200 Vdc. Activation of the protection circuits will cause a front panel error message and may cause a GPIB service request.

Up to 75 sets of complete front panel settings can be stored in memory. The memory has a non-rechargeable lithium battery back up for a minimum of 6 months (typically 1 to 2 years). A "low battery" warning will be indicated on the display when the battery voltage drops to 80% of its normal voltage.

WARNING

This equipment uses a BR-1/2A, 3V lithium battery, that contains less than 0.3 grams of lithium. To prevent the release of a potentially harmful substance, DO NOT RECHARGE, SHORT CIRCUIT, DISASSEMBLE, OR APPLY HEAT TO THE BATTERY. In addition, observe correct polarity when replacing.

1.2 ACCESSORIES

Rack mounts for a single instrument, rack mounts for two series 270 instruments side-by-side and instrument slides are available accessories. Refer to paragraph 1.3.13 for details.

1.3 SPECIFICATIONS

1.3.1 Main Generator Waveforms (Functions)

Programmable sine ∿ , triangle △ , square ⊓ , square complement, dc, external width, arbitrary and filtered arbitrary.

Sine Distortion (THD at 5 Vp-p):
<0.5% 10 mHz to 99.9 kHz.
No harmonics above
−40 dBc 100 kHz to 999 kHz
−30 dBc 1 MHz to 12 MHz.

Time Symmetry:
±1% ±8 ns.

Square Transition Time:
<15 ns.

Square Overshoot:
<4% at full amplitude.

Triangle Linearity: 99% to 100 kHz.

1.3.2 Operational Modes (For All Functions Including ARB)

Continuous:
Output continuous at programmed frequency or clock rate.

Triggered:
Output quiescent until triggered by external signal, internal trigger, GPIB trigger or manual trigger, then generates one cycle at programmed frequency or clock rate.

Gated:
Similar to triggered mode, except that output is continuous for the duration of the gate signal. The last cycle started is completed.

Burst:
Similar to triggered mode, except that the number of cycles produced is programmable.
Count Range: 1 to 1,048,200.
Burst Rate: 12 MHz maximum.

1.3.3 Operational Modes (ARB Only)

Triggered ARB with Ramp-to-Start:
One cycle of ARB waveform is initiated on the trigger input. External RTS signal (at ARB RTS/HOLD IN) causes ARB output to slowly ramp to data value at start address of the ARB waveform. If RTS signal is not received before stop address is reached, RTS is initiated at stop address.

Triggered ARB with Reset:
Same as Triggered ARB with Ramp-to-Start except the Reset signal (or stop address) causes immediate reset to start address.

Triggered ARB with Hold and Triggered Ramp-to-Start:
One cycle of the ARB waveform is initiated on trigger input. Leading edge of Hold signal causes ARB to hold. Second leading edge (Reset signal) causes immediate reset to start. If stop address is reached before Hold signal then stop address causes hold.

Triggered ARB with Hold and Triggered Reset:
One cycle of ARB waveform is initiated on trigger input. Leading edge of Hold signal causes ARB to hold. Second leading edge (Reset signal) causes immediate reset to start. If stop address is reached before Hold signal, then stop address causes hold.

Single Step:
Same as Continuous mode except when Arbitrary function is selected ARB clock rate is replaced by trigger input so that ARB clock can be supplied externally or with function generator.

Examine:
When Arbitrary function is selected the output will be voltage (data value) present at address specified on address program. This allows ARB waveform to be examined one point at a time by specifying address of desired point.

Triggered ARB with Hold on Breakpoint:
ARB waveform is initiated upon trigger input and held at programmed breakpoints. Start and stop addresses are ignored in this mode.

1.3.4 Frequency

Range:
10 mHz to 12 MHz for sine, triangle, square, square complement, >15 MHz for external width. ARB frequency range dependent upon clock rate and block size. Clock rate 267 ns to 267 s.

Block Size:
2 points to 2048 points (option to 8192 points).

Resolution:
3 digits.

Accuracy:
±2% for non-ARB modes, ±0.2% for ARB modes.

Repeatability (24 hr):
±1% for non-ARB modes, 0.01% for ARB modes.

Jitter:
≤0.1% of period ±100 ps

Control:
Frequency may be controlled by programmed value or external VCG input.

Value:
Frequency value is keyboard or GPIB programmable with automatic range selection.

VCG (Voltage Controlled Generator):
Ac or dc input controls frequency. 0 to ±12V into 10 kΩ for up to 1200:1 frequency change in each of 9 frequency ranges (range must be programmed). Slew rate is limited to 1V/μs.

1.3.5 Amplitude

Range:
0.01 to 10 Vp-p into 50Ω (0.02 to 20 Vp-p into open circuit) from main output. Absolute peak amplitude plus offset may not exceed 5V into 50Ω (10V into open circuit).

Resolution:
3 digits or 10 mV when absolute peak amplitude plus offset >0.5V; 3 digits or 1 mV when absolute peak amplitude plus offset ≤0.5V.

Accuracy:
±2% of programmed value and:
±5 mV for 0.1 to 1V (peak amplitude + offset <0.5V),
±20 mV for 1.01 to 10V,
±50 mV for all other.

Repeatability (24 hr):
±1% ±10 mV.

Flatness (at 5 Vp-p):
0.1 dB to 100 kHz, 1.5 dB to 12 MHz.

1.3.6 Offset

Range:
DC or offset programmable from −5V to +5V into 50Ω (-10V to +10V into open circuit). Absolute peak amplitude plus offset may not exceed 5V into 50Ω (10V into open circuit).

Resolution:
3 digits or 10 mV when absolute peak amplitude plus offset >0.5V, 3 digits or 1 mV when absolute peak amplitude plus offset ≤0.5V.

Accuracy:
±40 mV in dc function.

Repeatability (24 hr):
±20 mV.

1.3.7 Outputs

Function Output: Source of primary waveforms. Programs control provides:
Output on, 50Ω source impedance;
Output off, high Z (>500kΩ);
Output off, low Z (terminated in approximately 50Ω).

Protection:
Output protected to 140 Vac or 200 Vdc without internal damage.

Main Sync Output:
Sync signal is at programmed frequency and TTL level.
Level:
≤0.4V to ≥2.4V into 50Ω,
≤0.8V to ≥4.8V into open circuit.

Source Impedance:
50Ω.

Timing:
Concurrent with function output in square; lags sine and triangle by 90°.

Over/Undershoot:
<10% into 50Ω.

Protection:
Output protected from short circuit to any voltage between ±15 Vdc.

Arb Sync Output:
5 Vp-p into 600Ω, programmable phase control. RCL 4000 initiates positive ARB sync; RCL 4001 initiates negative ARB sync.

Source Impedance:
600Ω.

Protection:
Output protected from short circuit to any voltage between ±15V.

1.3.8 Inputs

External Trigger:
Trigger of input circuit is programmable for a + or − signal slope and required threshold level.
Level: −10 to +10V.
Resolution: 20 mV.
Accuracy: ±500 mV (for signals with less than 10 V/µs slew rate).
Input Impedance: 10 kΩ.
Maximum Trigger Rate: 12 MHz (15 MHz for External Width function).
Minimum Trigger Width: 20 ns.
Minimum Amplitude: 500 mVp-p to 1 MHz, 1 Vp-p to 15 MHz.
Protection: Input protected to ±50V.

VCG in:
Voltage control of generator frequency. See Frequency.
Range: 0.01 to ±12V.
Impedance: 10kΩ.
Protection: Input protected to ±50V.

ARB RTS/HOLD Input:
Trig input and RTS/Hold Input are logically internally common. Having two inputs provides processing for independently generated trigger and RTS/hold signal. (NOTE: Inputs are buffered prior to being logically "OR"ed together.)
Protection: Input protected from short circuit to any voltage between ±15V.

1.3.9 Internal Trigger

Non-ARB Functions
Range: 3.75 mHz to 3.75 MHz.
Resolution: 4 digits.
Accuracy: 0.2%.

ARB Functions
Range: 10 mHz to 3.75 MHz.
Resolution: 3 digits.
Accuracy: 2%.

1.3.10 ARB Characteristics

Horizontal Resolution:
2048 points standard; 8192 points optional.

Vertical Resolution:
12 bits (-2048 to +2047).

Auto-Line:
Allows a straight line to be drawn between the last two data points specified.

Programmable Filter on ARB Waveform:
Non-Filtered Arb waveform: Settling time 1.5 μs.
Filtered Arb waveform: Settling time 1 ms.

Programmable Ramp-to-Start Rate:
Fast: approximately 5 ms/bit;
Slow: approximately 20 ms/bit.

Programmable 3 digit ARB Clock:
Period ranges from 267 s to 267 ns with 0.2% accuracy.

1.3.11 GPIB Programming

IEEE 488-1978 compatible. Nonisolated. Double buffered.
Address: 0-30, keyboard or internal switch selectable. Internal switch can lock out keyboard selection. Power-up address is internal setting.

Subsets: SH1, AH1, T6, TE0, L4, SR1, RL1, PP0, DC1, C0, E2.

Interface Timing:

Frequency	16 ms
Amplitude	13 ms
Offset	14 ms
Mode	6 ms
Function	5 ms
INT/EXT	5 ms
Execute	20 ms to 4 sec
Store	11 ms
Output	10 ms
Slope	5 ms
Burst Count	10 ms
Rate	35 ms
Recall	185 ms
Reset	185 ms
Start	20 ms
Stop	20 ms
GET Mode	5 ms to 4 sec
ADRS	10 ms
DATA	15 ms
AUTO LINE	20 ms to 2 sec

1.3.12 General

Stored Settings:
Non-volatile memory for 75 stored settings.

Environmental:
Temperature Range: 25°C ±10°C for specified operation; operates 0°C to 50°C; −50°C to +75°C for storage.
Altitude: Sea level to 10,000 ft for operation. Sea level to 40,000 ft for storage.
Relative Humidity: 95% at 20°C at sea level (non-condensing).
Warm-up Time: 20 minutes for specified operation.

Dimensions:
21.7 cm (8.54 in) wide (half-rack); 13.3 cm (5.25 in) high; 39.4 cm (15.5 in) deep.

Weight:
5.9 kg (13 lb) net, 7.2 kg (16 lb) shipping.

Power:
90 to 105, 108 to 126, 198 to 231, or 216 to 252 volts rms; 48 to 66 Hz, 1 phase; <40 watts.

1.3.13 Options

002: Rear Panel Connectors
Front panel BNC connectors relocated to rear panel.

004: Extended Block Size
Extends arbitrary waveform memory block size to 8192 points.

1.3.14 Accessories

Style 12: Single Rack Adapter Kit
Allows right or left mounting in a standard 19 inch rack. 5 1/4 inches high.

Style 13: Dual Rack Adapter Kit
Allows any 270 series instrument to be mounted side-by-side in a standard 19 inch rack. 5 1/4 inches high.

Rack Slides

SECTION 2
INSTALLATION AND INTERFACE

2.1 MECHANICAL INSTALLATION

After unpacking the instrument, visually inspect all external parts for possible damage to connectors, surface areas, etc. If damage is discovered, file a claim with the carrier who transported the unit. The shipping container and packing material should be saved in case reshipment is required.

The generator can be used as a bench instrument or rack mounted. The 275 can be converted to rack mounts in the field by using the following kits.

Rack Mount Kit	Part Number	Reference Drawing
Single Instrument (left or right mounting)	1101-00-1043	0102-00-1043
Dual Instruments	1101-00-1041	0102-00-1041
Rack Slides	1101-00-1042	0102-00-1042

NOTE

The rack slides can only be used with dual rack mounted instruments.

Whether used on a bench or in a rack, ensure that there is no impedance to air flow at any surface of the instrument. Before rack mounting, it may be desirable to perform the initial checkout (paragraph 3.1) to verify operation of all functions.

2.2 ELECTRICAL INSTALLATION

2.2.1 Power Connection

NOTE

Unless otherwise specified at the time of purchase, this instrument was shipped from the factory with the power transformer connected for operation on a 120 Vac line supply and with a ½ amp fuse.

Conversion to other input voltages requires a change in rear panel fuse holder voltage card position and fuse (figure 2-1) according to the following procedure.

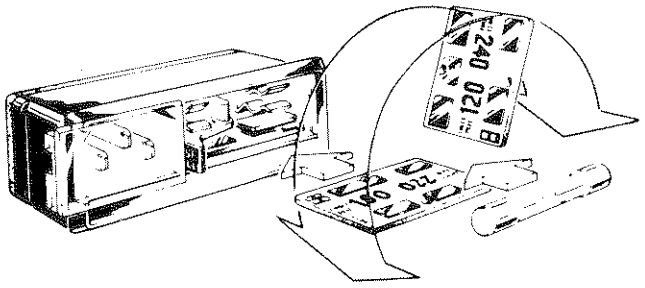


Figure 2-1. Voltage Selector and Fuse

1. Disconnect the power cord at the instrument, open fuse holder cover door and rotate fuse-pull to left to remove the fuse.

2. Remove the small printed circuit board and select operating voltage by orienting the printed circuit board to position the desired voltage to the top left side. Push the board firmly into its module slot.

Card Position	Input Vac	Fuse
100	90 to 105	3/4 amp
120	108 to 126	3/4 amp
220	198 to 231	3/8 amp
240	216 to 252	3/8 amp

3. Rotate the fuse-pull back into the normal position and insert the correct fuse into the fuse holder. Close the cover door.

4. Connect the ac line cord to the mating connector at the rear of the unit and the power source.

2.2.2 Signal Connections

NOTE

Use RG58U 50Ω or equivalent 50Ω coaxial cables equipped with BNC connectors to distribute signals.

Instrument BNC connectors are:

TRIG IN. Acceptable trigger level and slope are programmable; −10 kΩ impedance.

MAIN SYNC OUT. 0V to >2.4V into50Ω impedance; >4.8V open circuit.

FUNC OUT. Up to 10 Vp-p into 50Ω impedance; up to 20 Vp-p into >50 kΩ impedance.

VCG IN. 0.01 to 12V; 10 kΩ impedance.

ARB SYNC OUT. 0V to 10V pulse into 600Ω impedance.

ARB RTS/HOLD IN. TTL input, 1 kΩ impedance. Used in Arb function only. RTS/HOLD and TRIG IN are internally OR'd in RTS modes.

Signal ground may be floated up to ±42 volts with respect to chassis ground. Be aware that all signal grounds are common and must all be floated together.

2.2.3 GPIB Connections

The GPIB I/O rear panel pin connections and signal names are given in table 2-1. The panel connector is an Amphenol 57-10240 or equivalent and connects to a GPIB bus cable connector (available from Wavetek in 1 and 2 meter lengths).

2.2.4 GPIB Address

For instruments on the General Purpose Interface Bus (GPIB), ensure that the instrument GPIB address is correct. The GPIB address can be changed by the internal switch (for access, remove the bottom cover, see figure 2-2) or the front panel GPIB ADRS key (e.g., ADRS 4 EXEC). The switch sections are labeled from 1 through 5 and their OFF position noted (OFF = Binary "0" in table 2-2). To verify the address, press ADR on the front panel. The device number (decimal) will be displayed. Upon power-up, the address is always that of the internal switch.

Table 2-1. GPIB Data In/Out

Pin	Signal
1	DIO1
2	DIO2
3	DIO3
4	DIO4
5	EOI
6	DAV
7	NRFD
8	NDAC
9	IFC
10	SRQ
11	ATN
12	Chassis Ground
13	DIO5
14	DIO6
15	DIO7
16	DIO8
17	REN
18	Signal Gnd
19	
20	
21	
22	
23	
24	

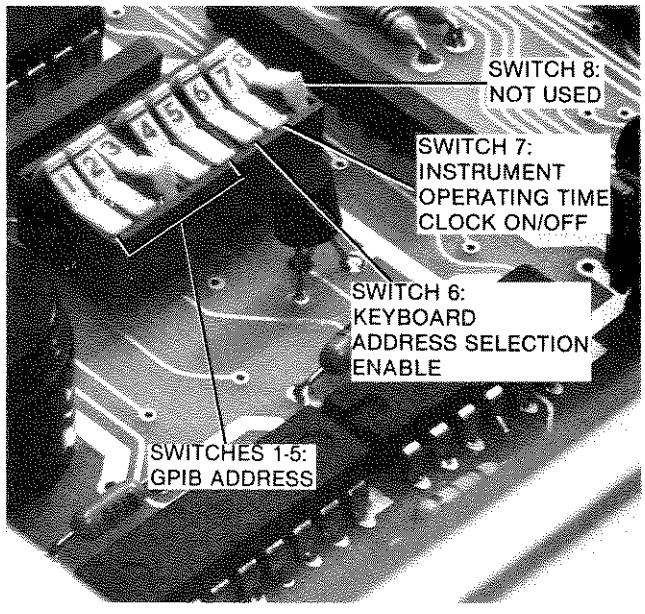


Figure 2.2 GPIB Address Selector Switch

Table 2-2. GPIB Address Codes

	ASCII		Switch Position					Hexa-decimal	
Device	Listen	Talk	1	2	3	4	5	Listen	Talk
0	(space)	@	0	0	0	0	0	20	40
1	!	A	1	0	0	0	0	21	41
2	"	B	0	1	0	0	0	22	42
3	#	C	1	1	0	0	0	23	43
4	$	D	0	0	1	0	0	24	44
5	%	E	1	0	1	0	0	25	45
6	&	F	0	1	1	0	0	26	46
7	'	G	1	1	1	0	0	27	47
8	(	H	0	0	0	1	0	28	48
9	)	I	1	0	0	1	0	29	49
10	*	J	0	1	0	1	0	2A	4A
11	+	K	1	1	0	1	0	2B	4B
12	,	L	0	0	1	1	0	2C	4C
13	—	M	1	0	1	1	0	2D	4D
14	.	N	0	1	1	1	0	2E	4E
15	/	O	1	1	1	1	0	2F	4F
16	0	P	0	0	0	0	1	30	50
17	1	Q	1	0	0	0	1	31	51
18	2	R	0	1	0	0	1	32	52
19	3	S	1	1	0	0	1	33	53
20	4	T	0	0	1	0	1	34	54
21	5	U	1	0	1	0	1	35	55
22	6	V	0	1	1	0	1	36	56
23	7	W	1	1	1	0	1	37	57
24	8	X	0	0	0	1	1	38	58
25	9	Y	1	0	0	1	1	39	59
26	:	Z	0	1	0	1	1	3A	5A
27	;	[	1	1	0	1	1	3B	5B
28	<	\	0	0	1	1	1	3C	5C
29	=	]	1	0	1	1	1	3D	5D
30	>	^	0	1	1	1	1	3E	5E

NOTE

Address 31 is not allowed.

2.2.5 Initial Checkout and Operation Verification

Make the equipment setup as shown in figure 2-3 and perform the steps in table 2-3 to verify Wavetek 275 operation. If further explanations are required, refer to figure 3-1 and table 3-1.

Figure 2-3. Test Setup

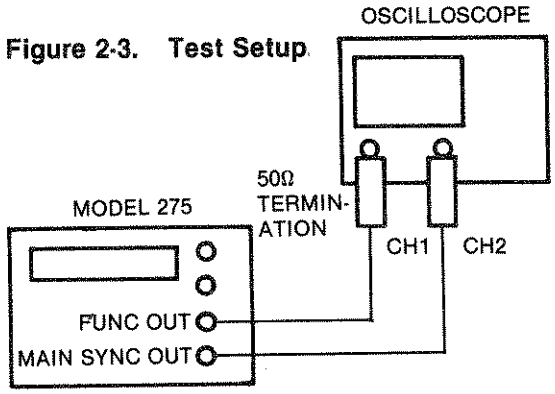


Table 2-3. Initial Checkout

Step	Test	Tester & Setup	Program	Desired Results
1	Wake-up State		Power: ON	Display: All segments, decimal points and commas light up for 1 second.
2	Wake-up Status		Press STAT key.	Display (changes automatically): FREQ 1 KHz AMPLITUDE 5V OFFSET 0V MODE CONTINUOUS (0) FUNC SINE (0) BURST COUNT 2 CLK 1 μs (488 HZ) (122 Hz with option 004, extended block size. START ADRS 0000 STOP ADRS 2047 (8191 with option 004, extended block size. OUTPUT OFF (0) EXTERNAL TRIGGER (0) TRIG RATE 200 HZ TRIG SLOPE POS (0) TRIG LEVEL 1.5V
3	Status Search		STAT	Status display sequence stops.
4			↑	Status progresses forward.
5			↓	Status progresses backward.
6			STAT	Status display automatic sequence continues.
7	Beeper Test.		Press FREQ key a few times.	Beeper sounds every time key is pressed.
8			Press ♪, then FREQ key a few times.	Beeper is silent.
9			♪	Beeper enabled
10	Command Recall.		Press each of the 6 keys in the MAIN generator section 4 times then CMD RCL.	Strings of characters shown on display. Characters are the ones shown on lower left of each key
11			Press → then ←.	Moves characters right then left 4 at a time.

Table 2-3. Initial Checkout

Step	Test	Tester & Setup	Program	Desired Results
12	GPIB Address and Status.		ADRS 1 EXEC then 30 EXEC.	Display: GPIB ADRS 1 then GPIB ADRS 30.
13	Quality Assurance Procedure.	Connect Wavetek 275 and oscilloscope as shown in figure 2-3. Scope setting: CH1 2V/div; horizontal 0.2 ms/div; CH2 2V/div; trigger on CH2.	Press: RCL 2000 EXEC.	Display: (0) BEGIN QA PROC. Scope: CH1, 5 Vp-p 1 kHz sine wave. CH2, 2.5 Vp-p 1 kHz square wave
14	Frequency: Exercises Each Frequency Bit and the Sine Wave Function.		Press: CURSOR ↑ once.	Display: (1) FREQUENCY. Scope: CH1, 5 Vp-p sine wave continuously sweeping from 1 kHz to 10 kHz. CH2, 2.5 Vp-p square wave synchronous with CH1.
15	Amplitude: Exercises Each Amplitude Bit and the Triangle Wave Function.		Press: CURSOR ↑ once.	Display: (2) AMPLITUDE. Scope: CH1, 1 kHz triangle wave, amplitude continuously increases from 1V to 10 Vp-p. CH2, 2.5 Vp-p square wave synchronous with CH1.
16	Offset: Exercises Each DC Offset Bit and Square Function.		Press: CURSOR ↑ once.	Display: (3) OFFSET. Scope: CH1, 1 Vp-p square wave. DC offset continuously increases from −4V to +4V. CH2, 2.5 Vp-p square wave synchronous with CH1.
17	Trigger Circuit.	Trigger Scope on CH1.	Press: CURSOR ↑ once.	Display: (4) TRIGGER. Scope: CH1, 500 Hz 5 Vp-p square wave. CH2, 2.5 Vp-p 100 μs pulse, delayed 50 μs relative to positive edge of CH1 waveform.
18	Gate Circuit.		Press: CURSOR ↑ once.	Display: (5) GATE. Scope: CH1, 500 Hz 5 Vp-p square wave. CH2, 2.5 Vp-p pulse burst, six 100 μs pulses.
19	Burst Circuit.		Press: CURSOR ↑ once.	Display: (6) BURST. Scope: CH1, 5 Vp-p pulse, fixed repetition rate of 2 ms, variable width 1.6 ms to 250 μs. CH2, pulse train of 100 μs wide pulses, 2.5 Vp-p. Number of pulses per train steps from 9 to 2.
20			Press: CURSOR ↑ once.	Display: (7) END QA PROC. Scope: CH1, 5 Vp-p pulse, 250 μs wide, repetition rate 2 ms. CH2, burst of two 100 μs pulses, burst repetition rate 2 ms.

SECTION 3
OPERATION

3.1 INTRODUCTION TO OPERATION

The Wavetek 275 may be operated either locally, from the front panel keyboard, or remotely, via the GPIB (General Purpose Interface Bus). This manual presents local operation first, then additional information required for remote operation. Users who plan to control the instrument remotely should read *both* sections.

3.2 FRONT PANEL CONTROLS AND CONNECTORS

The front panel contains the power switch, keyboard, display and (unless option 002, rear panel connectors, has been specified) the BNC signal connection jacks. Figure 3-1 shows the location of all front panel controls and connectors. Table 3-1, which is keyed to the numeric identifiers in Figure 3-1, briefly lists the purpose of each control or connector for quick reference. Further information on the controls is contained in section 3.5, LOCAL OPERATION.

3.3 POWER-UP

When ac power is applied to the instrument, the microprocessor performs internal checks and initializes the internal circuitry. During the first second, the microprocessor performs a display test by lighting all display segments. The display then indicates

```
BUSY, PLEASE WAIT
```

during the remainder of the initialization. When the initialization is complete,

```
WAVETEK MODEL 275
```

is displayed. During power-up, all parameters are set to default values.

Table 3-1. Controls and Connectors

Key Ref No.	Control or Connector	Description
1	CURSOR	← and → position the cursor to any numerical digit (indicated by the flashing digit on the display). ↑ and ↓ increment or decrement codes, storage addresses or the flashing digit (features carry action) of a parameter value. ← and → are also used to move a displayed program string (CMD RCL) to the left or right in increments of 4 characters. Because ↑ and ↓ employ an automatic execute, the instrument output is instantly changed with cursor action.
2	DISPLAY	Twenty character readout (both manually and remotely accessible). Advises operator of parameters and values, errors, warnings and GPIB activity. Also displays programming strings.

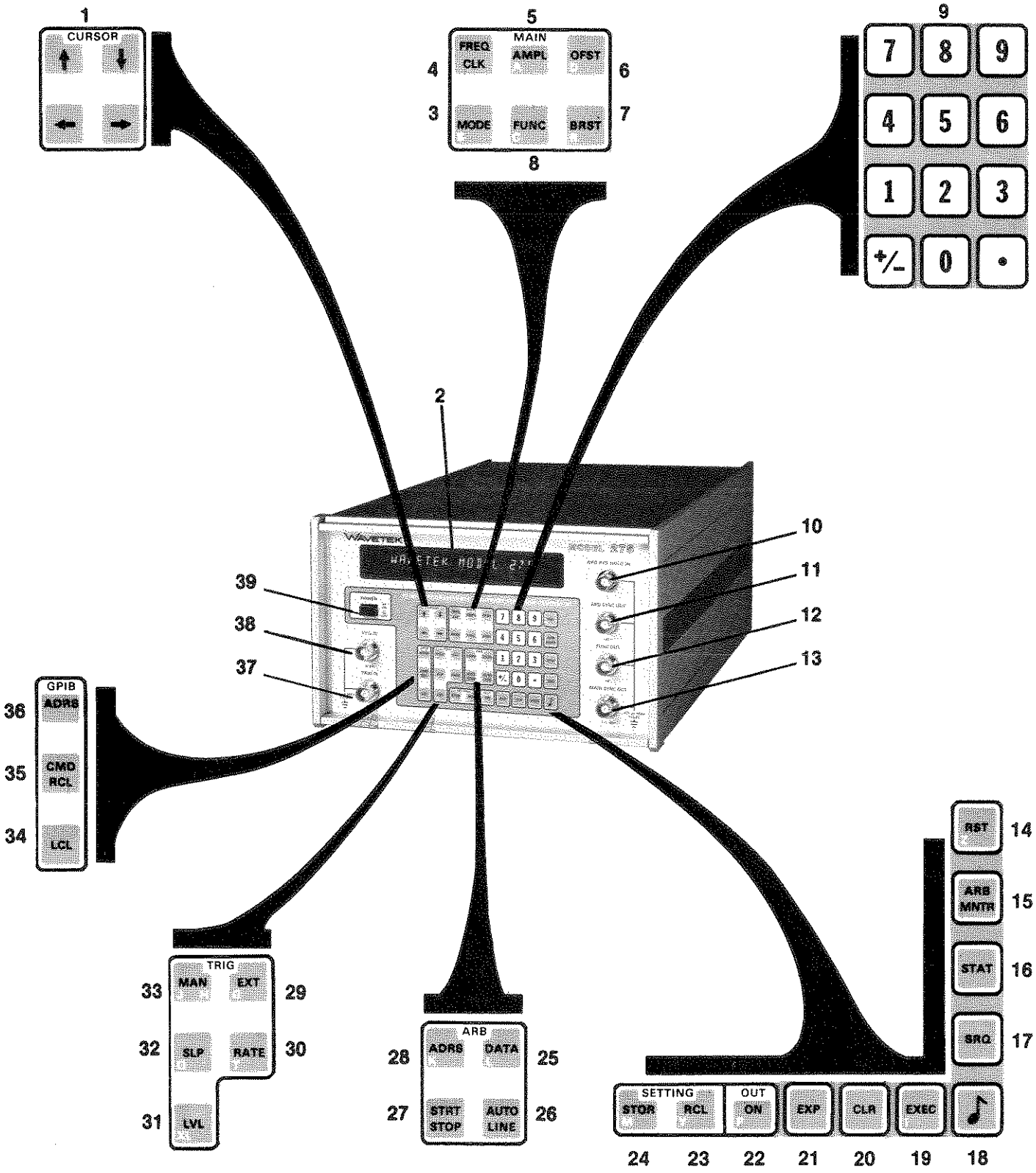


Figure 3-1. Controls and Connectors

Table 3-1. Controls and Connectors (Continued)

Key Ref No.	Control or Connector	Description
3	MODE (B)	Displays main generator and Arb generator modes and enables change. There are eleven modes.

MODE	CODE
Continuous	0
Trigger	1
Gate	2
Burst	3
Triggered Arb with Ramp-to-Start	4
Triggered Arb with Hold and Triggered Ramp-to-Start	5
Triggered Arb with Reset	6
Triggered Arb with Hold and Triggered Reset	7
Single Step	8
Examine	9
Triggered Arb with Hold on Breakpoint	10

Key Ref No.	Control or Connector	Description
4	FREQ/CLK	Displays main generator frequency and Arb clock time. Main generator frequency is 10 mHz to 12 MHz with 3 digit resolution. Arb generator range dependent upon clock rate and block size. Clock rate 267 ns to 267 s. Block size 2 points to 2048 points (option to 8192 points).
5	AMPL(A)	Displays output amplitude programming and enables change. Amplitude maximum is 10.0 Vp-p into 50Ω.
6	OFST(D)	Displays dc offset programming and enables change. DC offset used with amplitude adjusts the output waveform offset bias. Maximum offset is ±5V into 50Ω.
7	BRST(R)	Displays burst count and enables change. Burst count can be from 1 to 1,048,200. This is the number of waveform cycles in the burst each time it is triggered.
8	FUNC (C)	Displays function (waveform) programming and enables change. Function may be one of eight output waveforms.

FUNCTION	CODE
Sine	0
Triangle	1
Square	2
Square Complement	3
DC	4
External Width	5
Arbitrary	6
Filtered Arbitrary	7

Key Ref No.	Control or Connector	Description
9	NUMERICAL KEYBOARD	Used with other keys to enter data or retrieve information. Free format data entry allows fixed point, floating point and scientific (exponential) notation. Microprocessor will round off as required.

Table 3-1. Controls and Connectors (Continued)

Key Ref No.	Control or Connector	Description
10	ARB RTS/HOLD IN	TTL input provides processing for independently generated trigger and generated trigger and Ramp-to-Start signals. Used in Arb function only to trigger Arb waveform, initiate hold, ramp-to-start or reset. Trig input and RTS/hold input are internally ORed in RTS modes, and both may be used to initiate any of the events for the Arb waveform.
11	ARB SYNC OUT	Provides a 0V to 10V pulse (open circuit), 0V to 5V pulse (600Ω). Pulse width is five Arb clock cycles with leading edge of pulse occurring at currently programmed address followed by an execute. Pulse polarity is selectable. RCL 4000 EXEC selects positive pulse. RCL 4001 EXEC selects negative pulse.
12	FUNC OUT	The main output of selected waveforms. Function output is off at power-up and reset. Output control key 22 sets FUNC OUT at on or off with 50Ω impedance.
13	MAIN SYNC OUT	The sync signal has the same frequency as FUNC out signal when a non-arbitrary function is selected and is 0V to >2.4V (TTL level) into a 50Ω load (>4.8V open circuit).
14	RST (Z)	Returns the instrument waveform parameters to their power-on condition. Stored settings are not affected.
15	ARB MNTR	Displays the current Arb generator address, data, and output voltage. Provides a real time monitor of slowly changing Arb waveforms. This feature does not interfere with the Arb waveform output.
16	STAT	Gives the current waveform generator status by displaying each parameter and value momentarily. Pressing the key a second time holds the display.
17	SRQ	To use the SRQ key, the instrument must be in the local mode and the SRQ mode bit 128 must be selected. Under these conditions pressing the SRQ key asserts the SRQ line of the GPIB.
18	♪	Turns audible tone on or off. If there is no tone when key is pressed, pressing restores the tone.
19	EXEC (I)	Causes all the entered instructions to be error checked and transferred to waveform circuits. No parameter entries will change the output until execute (EXEC key, CURSOR ↑, CURSOR ↓, GPIB I, GPIB GET, GPIB Z or RESET) is received. This permits a complete test setup to occur at one time with no in-between parameter change aberrations. Execute is not required to cause data to be entered into Arb memory.
20	CLR	Corrects front panel and scratch-pad numerical entries. (An asterisk on the display indicates that the value displayed has not been executed and resides in scratch-pad memory only.)

Table 3-1. Controls and Connectors (Continued)

Key Ref No.	Control or Connector	Description
21	EXP (E)	Designates the next numerical and +/− entries pertaining to the power of the X10 multiplier.
22	OUT ON (P)	Displays output and load status and enables change. Output status programming codes are:

OUTPUT	CODE
Output Off (0) (>100kΩ)	0
Output On (1) (50Ω)	1
Output Off, Lo Z (2) (≅50Ω)	2

23	RCL (Y)	Displays the status of setting recall (none recalled, recall setting No. _____, or No. _____ last recalled) and enables the change of address of settings to be recalled. Stored settings can be recalled to scratch-pad memory only and do not affect the instrument output operation if recall is alpha terminated but not executed. Recall settings and selections are:

SETTINGS	RCL
Recall last power off condition	0
Recall user-stored settings	1-75
Internal calibration procedure	1000-1031
Internal QA test/demo procedure	2000-2007
Keyboard lockout off	3000
Keyboard lockout on	3001
Arb Sync output positive	4000
Arb Sync output negative	4001
Slow Ramp-to-Start	5000
Fast Ramp-to-Start	5001
Clear break points	6000

24	STOR (M)	Displays address of last storage location used and enables storage location address change. The settings stored are those currently in scratch-pad memory; the instrument output operation is not disturbed by storage action. A minus (−) address entry erases the stored settings at that address from memory. There are 75 non-volatile stored settings.
25	DATA (L)	Displays the Arb memory data value for the currently displayed address. Ranges from −2048 to +2047. Value −2048 corresponds to the negative peak amplitude. Value +2047 corresponds to the positive peak amplitude. Entry of valid data causes the address to be incremented by one. An execute is not required to cause data to be entered into memory.
26	AUTO LINE (XK)	Automatically causes a straight line to be written into Arb memory between the last two data points. Auto line will over-write any previously stored data between the two data points.
27	STRT STOP	Displays the start-stop memory locations for the desired block of Arb memory. If a START is > STOP the specified block will wrap around the end of Arb memory.

Table 3-1. Controls and Connectors (Continued)

Key Ref No.	Control or Connector	Description
28	(ARB) ADRS (K)	Displays the Arb memory address point. Ranges from 0000 to 2047 for standard units. Range expanded to 8191 with memory option. When programming an Arb address for the purpose of entering data an execute is not required. If address is being specified for the purpose of moving ARB sync location, an execute is required.
29	EXT (G)	Displays the trigger source and enables change. There are two trigger sources.

SOURCE	CODE
External (BNC, Man, GPIB)	0
Internal	1

30	RATE (T)
	Displays the internal trigger rate and enables change. RATE range is 10 mHz to 3.75 MHz with 2% accuracy for Arb functions, 3.75 mHz to 3.75 MHz with 0.2% accuracy for non-Arb functions.
31	LVL (XL)
	Displays programmed trigger level and enables change. Trigger level is the voltage at which the trigger circuit is sensitive to the TRIG IN BNC input signals. Trigger level may be set in the ±10 Vdc range with 20 mV resolution.
32	SLP (Q)
	Displays selects slope and enables change. Selects generator triggering on the rising or falling edge of the TRIG IN BNC signal.

TRIGGER	CODE
Positive slope	0
Negative slope	1

33	MAN TRIG (J) (H)
	Triggers output when in any of the modes requiring trigger. The two ASCII codes (J and H) are for gating; J gates on and H gates off. EXT key 29 must be 0 (External Source).
34	LCL
	Takes the instrument out of remote control without affecting the rest of the bus with the following exception: A GPIB LLO command will override the key logic and inhibit its operation.
35	CMD RCL
	Displays the last 40 parameters, values and actions (all in ASCII code) sent to the instrument from the keyboard and the GPIB. The display shows only 20 characters at a time, and the CURSOR ← and → must be used to see the entire 40 character string.
36	(GPIB) ADRS
	Displays the GPIB decimal address and enables change, with the following exception: The GPIB address cannot be changed by front panel control if the internal disable switch has been set.
37	TRIG IN
	A sufficient external signal level transition triggers or gates the generator when generator mode requires a trigger or gate signal. The required level is determined by key 31 and the required transition by key 32.

Table 3-1. Controls and Connectors (Continued)

Key Ref No.	Control or Connector	Description
38	VCG IN	The VCG input accepts ac or dc voltages used to externally control the frequency of the main generator. A positive voltage applied to the VCG IN connector will increase the generator frequency; a negative voltage will decrease the frequency. 0.01V to 12V gives approximately 1200:1 frequency change. Input impedance is 10 kΩ.
39	POWER ON/OFF	Turns generator on or off.

3.4 LOCAL OPERATION

Local operation is accomplished from the front panel keyboard. The front panel keys fall into three general categories:

1. Action keys, which cause an immediate action when pressed.
2. Parameter keys, which display the current value of a parameter (such as frequency), but do not cause any action until a new value is entered.
3. Numeric keys, which are used for entry of numeric data. These keys are [0] through [9], [+/-], [.] and [EXP].

Many of the keys are labelled with an alphabetic character in addition to the name of the key function. These alphabetic characters are for reference in remotely controlling the instrument, and for reading back previous commands from the display with the [CMD RCL] key. Four of the keys have alphabetic characters associated with the key, but the letters are not marked on the keys. These keys are: [EXP], [FREQ CLK], [AUTO LINE] and [STRT STOP]. Appendix B, Programming Command Summary, lists the ASCII character associated with each key, and also lists ASCII commands for which there is no equivalent keyboard key. Remote operation will be covered in section 3.5 of the manual.

3.4.1 Action Keys

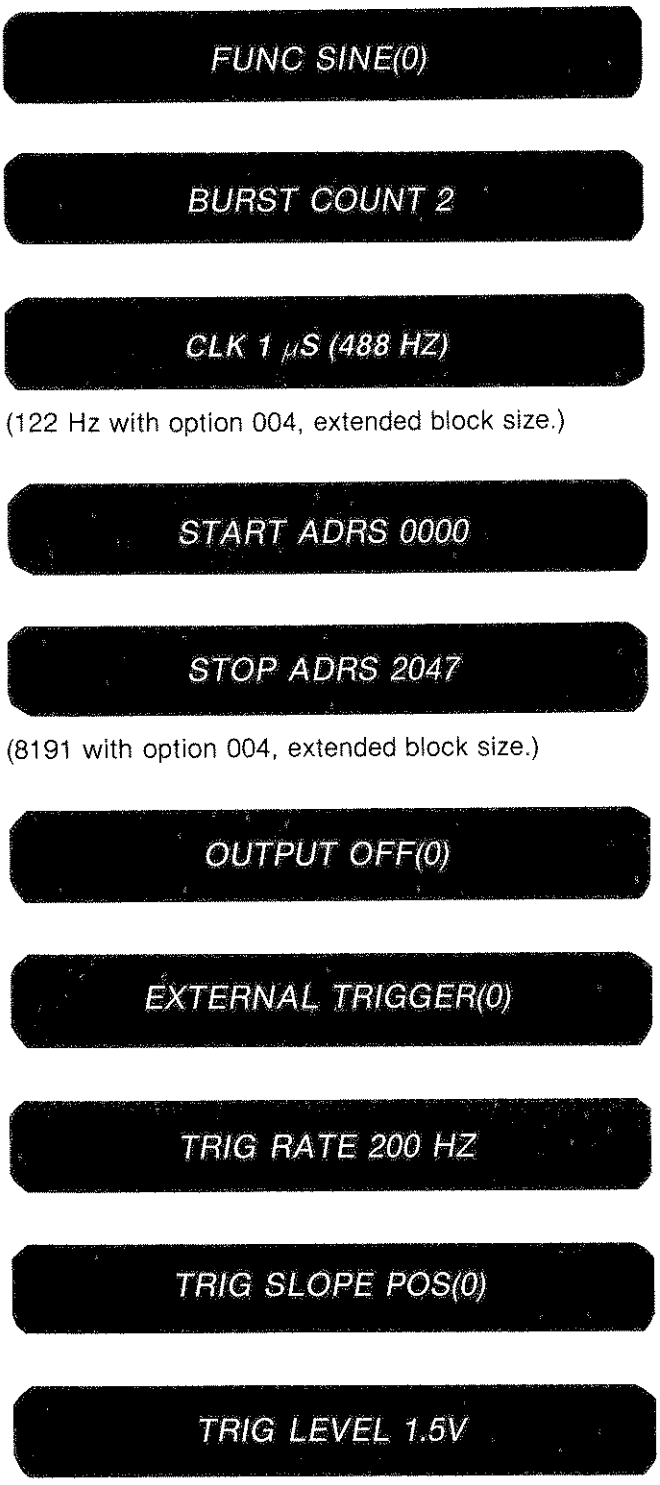
The keys that cause an immediate action when pressed and do not require entry of a numerical parameter value are the CURSOR keys, RESET, ARB MONITOR, STATUS, SRQ, Tone, EXECUTE, CLEAR, LOCAL and COMMAND RECALL.

3.4.1.1 Tone Key

An audible tone indicates that a key is pressed. Pressing [♪] will inhibit or enable the key tone. If there is no tone when keys are pressed, pressing [♪] restores the tone.

3.4.1.2 Status Key

Pressing [STAT] (the status key) will cause the display to sequentially indicate the current instrument parameters. At power on or reset, the following parameters will be displayed:



(122 Hz with option 004, extended block size.)

(8191 with option 004, extended block size.)

By pressing [STAT], the display will stop on the existing readout, and the status display may be incremented forward or backwards with the [↑] or [↓] CURSOR keys. Holding down the [↑] or [↓] key will cause the display to continuously increment or decrement.

NOTE: the [STAT] key displays only the actual operating parameters of the instrument, not parameters that may be temporarily stored in scratch-pad memory and not yet executed.

3.4.1.3 Cursor Keys

The cursor keys [↑], [↓], [←] and [→] are used to modify a parameter value and cause immediate execution of the new value. The [↑] and [↓] keys are used to increment or decrement a parameter value. Holding the key down continuously causes the value to continuously increment or decrement.

The [←] and [→] keys are used to select which digit of a multiple digit parameter will be incremented or decremented. The selected digit will flash alternately bright and dim on the display. Some parameters, such as the arbitrary waveform START and STOP addresses, can only be incremented or decremented in steps of 1, and the [←] and [→] keys will have no effect when this parameter is selected. Also, these keys will have no effect on a parameter that contains primarily single-digit values, such as mode or function.

3.4.1.4 Reset Key

The [RST Z] (Reset) key returns the instrument waveform parameters to their power-on default values. This key does not affect stored settings, arbitrary waveform memory, or COMMAND RECALL memory.

3.4.1.5 Execute Key

The [EXEC] (Execute) key transfers all data from the scratch-pad memory to the waveform circuit memory. (A leading asterisk (*) on the display indicates that the parameter value has not been executed.)

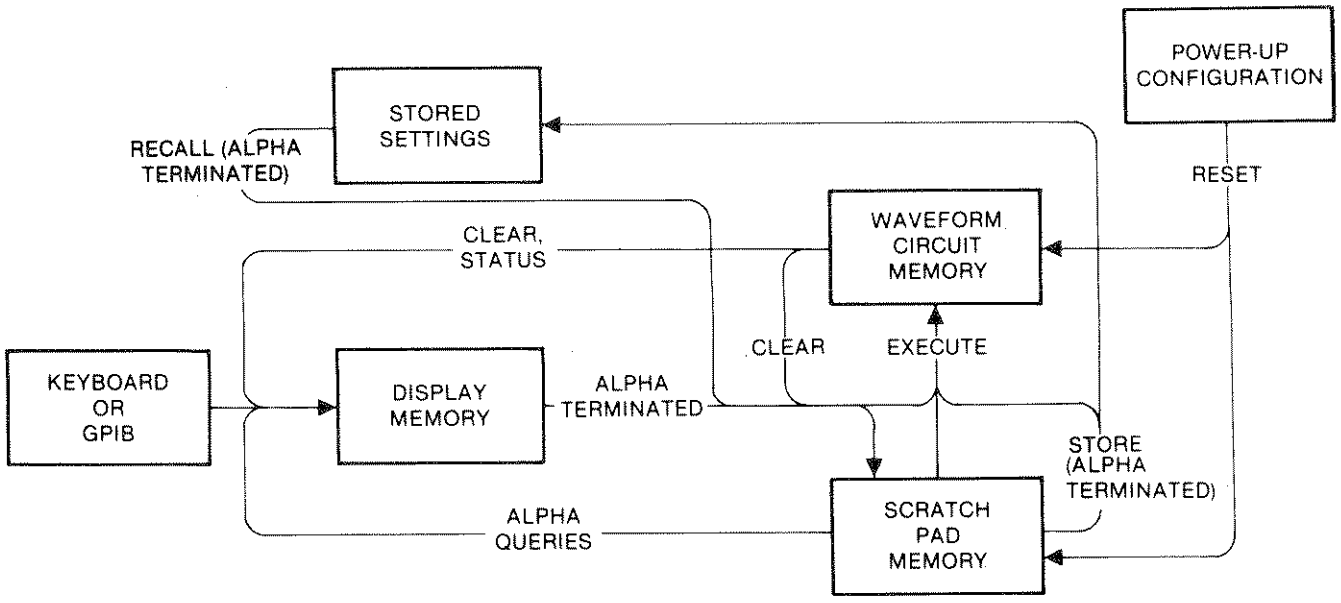


Figure 3-2. Memory Structure

Example: Press [AMPL A] [9] [.] [9] [9] . A dash at the end of the string of characters means that the string of characters has not been terminated (nor executed). The display will show

AMPLITUDE 9.99_

Press [AMPL A] . again. The display will be

*AMPLITUDE 9.99V

Press [EXEC] . The display will change to

AMPLITUDE 9.99V

3.4.1.6 Clear Entry Key

The [CLR] (Clear) key erases a parameter value which has been entered but not executed. The [CLR] key removes the numeric digits entered after the last parameter key. (Clearable entries are always prefixed by an asterisk or suffixed by a dash.) The display reverts to that caused by the previous accepted value of the parameter being programmed.

3.4.1.7 Local Key

The [LCL] (Local) key removes the instrument from the bus command and places it under front panel control. This key can be locked out from the GPIB controller with the LLO command if so desired.

3.4.1.8 SRQ Key

The [SRQ] key asserts the SRQ line of the GPIB if the key has been enabled by the GPIB controller. Further information will be found in the REMOTE OPERATION section of the manual (section 3.5).

3.4.1.9 Command Recall Key

Pressing the [CMD RCL] (Command Recall) key displays the last 20 commands from the keyboard or GPIB in the form of ASCII characters. Keyboard commands not

associated with an ASCII character (such as the cursor keys) are not shown. The display shows *all* commands associated with an ASCII character, even if the command is erroneous or has been superseded by a later command.

Example: Press [MODE B] [0] [FUNC C] [1] [AMPL A] [2] [OFST D] [3] [FREQ CLK] [1] [0] [0] [EXEC I].

Press [FUNC C] [0] [FREQ CLK] [1] [EXP] [3] [EXEC I].

Press [CMD RCL]. The display will show:

```
B0C1A2D3F100IC0F1E3I
```

The letters B, C, A, D, F, E and I are the ASCII codes for mode, function, amplitude, offset, frequency, exponent, and execute respectively. Note that the display contains two commands for function and frequency, but that only the last command for each parameter is the actual instrument setting. The ASCII codes for most parameters are shown on the keys. Two exceptions in the above example are frequency and exponent.

Now press [FREQ CLK] [1] [EXP] [9] [EXEC I]. The display will indicate

```
FREQ ERROR
```

Press [CMD RCL]. The last 5 characters on the display will be "F1E9I", even though the frequency command was outside the frequency range of the instrument.

Using the cursor [←] and [→] keys shifts the display 4 characters to the left or right to allow the eventual display of up to 40 characters.

NOTE

If the [CMD RCL] key is pressed immediately after turning on the instrument, the display will be blank because no characters have been programmed.

3.4.1.10 Arb Monitor Key

The [ARB MNTR] key allows monitoring of the address, data value and actual output voltage of a slowly changing arbitrary waveform. The Arb address is indicated by the letter "X", the Arb data value by the letter "Y", and the output voltage by the letter "V". A typical display might show, for example:

```
X0019 Y+1900 V+1.002
```

3.4.2 Parameter Keys

The parameter keys allow display of a current parameter value, modification of the current value with the cursor keys, or entry of a new value using the numeric keys. The parameter keys are functionally grouped as controls for main waveform, trigger, stored settings, output, GPIB and arbitrary waveform data entry.

3.4.2.1 Main Waveform Controls

The MAIN block of controls contains the parameter keys for frequency and clock period, amplitude, offset, mode, function and burst count.

3.4.2.1.1 Frequency/Clock Key

The [FREQ CLK] key selects frequency in cycles per second if a non-arbitrary waveform has been selected with the [FUNC C] key. If an arbitrary waveform has been selected, the [FREQ CLK] key selects clock period in seconds per arbitrary waveform address location.

3.4.2.1.2 Amplitude Key

The [AMPL A] key selects output waveform amplitude in volts peak-to-peak into a 50Ω load. For an arbitrary waveform, this value represents the peak-to-peak amplitude using the full data range (−2048 to +2047) of the arbitrary waveform memory. The waveform will be symmetrical about the selected offset voltage. (For an arbitrary waveform, a data value of zero corresponds to an output equal to the selected offset voltage.) Amplitude range (with no offset) is 10 mV to 10V peak-to-peak into a 50Ω load. Open-circuit amplitude will be approximately twice as high.

3.4.2.1.3 Offset Key

The [OFST D] key selects output waveform offset in volts.

Offset is the voltage (into a 50Ω load) midway between the waveform amplitude peaks. For example, to obtain a square wave having voltage levels of 0V and +5V, program an amplitude voltage of 5V and an offset voltage of 2.5V. For an arbitrary waveform, the offset voltage is the output voltage for a data value of zero. To avoid output clipping, offset voltage plus peak amplitude (p-p amplitude/2) must not exceed 5V. To avoid loss of amplitude resolution, amplitudes less than 100 mV require an offset voltage of less than 500 mV.

3.4.2.1.4 Burst Key

The [BRST F] key selects the number of waveform cycles that are generated when the generator is triggered in the BURST mode. The burst count can be set from 1 to 1,048,200 cycles.

3.4.2.1.5 Function Key

The [FUNC C] key selects the type of waveform at the FUNC OUT connector.

[FUNC C] [0] selects a sine wave.

[FUNC C] [1] selects a triangle wave.

[FUNC C] [2] selects a square wave of the same polarity as the MAIN SYNC OUT signal.

[FUNC C] [3] selects a square wave of opposite polarity of the MAIN SYNC OUT signal.

[FUNC C] [4] selects the DC function. The FUNC OUT voltage is a DC level at the programmed OFFSET voltage. The AMPLITUDE and MODE settings have no effect on the output.

[FUNC C] [5] selects the EXTERNAL WIDTH function. The FUNC OUT voltage is controlled by the AMPLITUDE, OFFSET and TRIGGER controls. For example, selecting amplitude 5V and offset 0V results in a FUNC OUT voltage of- 2.5V when the generator is not triggered and +2.5V when triggered. Selecting amplitude 5V and offset 2.5V will result in an output voltage of 0V not triggered and 5V when triggered. The internal or external trigger gates the voltage to the high state for the duration of the trigger signal. With one exception, the output will be gated by the selected trigger source regardless of the MODE programmed. The exception is the BURST (3) mode. In the BURST mode, a trigger pulse of any duration will cause the output to be gated to the high state for the duration of the burst count, which is determined by generator frequency and number of burst cycles programmed.

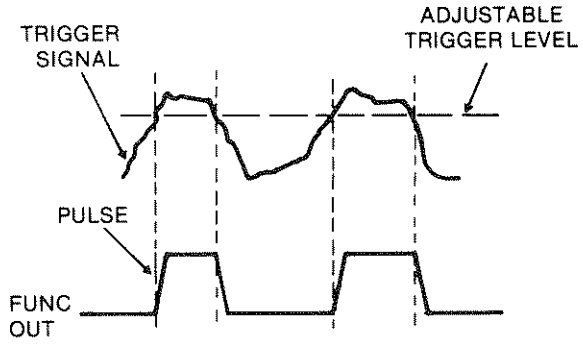


Figure 3-3. External Width

[FUNC C] [6] selects the arbitrary waveform. This waveform must have been previously stored by the user in the arbitrary waveform memory.

[FUNC C] [7] selects the arbitrary waveform filtered by an R-C low-pass filter having a time constant of 250 microseconds.

3.4.2.1.6 Mode Key

The [MODE B] key determines the conditions under which the selected function will be present at the FUNC OUT connector. Modes 4 through 10 are applicable only to the arbitrary waveform functions.

[MODE B] [0] selects a continuous waveform.

[MODE B] [1] selects a triggered waveform. One cycle of the selected function will be generated each time the generator is internally or externally triggered.

MODE B 2 selects a gated waveform. The selected function will be present at the FUNC OUT connector for the duration of the internal or external trigger signal. The last cycle started is completed.

MODE B 3 selects a the BURST mode. When the generator is internally or externally triggered, it will produce the number of waveform cycles previously programmed with the BRST B key.

MODE B 4 selects the Triggered Arb with Ramp-to-Start mode. When the generator is externally or manually triggered, one cycle of the arbitrary waveform is produced. At the end of the waveform block, the generator output voltage is gradually returned to the waveform starting voltage at the selected (FAST or SLOW) RTS rate. The Ramp-to-Start operation may be initiated before the end of the waveform block by externally or manually triggering the generator. During the Ramp-to-Start operation, the display reads.

RTS IN PROGRESS

At the conclusion of the Ramp-to-Start operation,

RTS COMPLETED

is displayed. Internal trigger cannot be used in this mode. The front panel lockout is turned on during the RTS operation.

MODE B 5 selects Triggered Arb with Hold and Triggered Ramp-to-Start. Manually or externally triggering the generator produces one cycle of the arbitrary waveform. At the end of the arbitrary waveform block, the output voltage holds constant at the final value. A second trigger pulse initiates the Ramp-to-Start operation. A trigger pulse received before the end of the waveform block places the waveform on "hold"; the next trigger pulse initiates Ramp-to-Start. Internal trigger can not be used in this mode. The front panel lockout is turned on during the RTS operation.

MODE B 6 selects Triggered Arb with Reset. Internally, externally or manually triggering the generator produces one cycle of the arbitrary waveform. At the end of the waveform block, the output returns to the waveform starting value. For an arbitrary waveform, this mode is almost identical to the TRIGGERED (1) mode, with the exception that in mode 6 a second trigger pulse can cause reset before the end of the waveform.

MODE B 7 selects Triggered Arb with Hold and Triggered Reset. Internally, externally or manually triggering the generator produces one cycle of the arbitrary waveform. At the end of the waveform block, the output voltage remains unchanged until another trigger pulse is received. When this occurs, the output voltage is reset to the waveform starting value. The waveform can be placed on "hold" before it reaches the end of the waveform block by a second trigger pulse. The next trigger pulse resets the waveform back to the starting value.

MODE B 8 selects the Single Step mode. The arbitrary waveform is advanced one address with each internal, external or manual trigger pulse. The waveform may be reset to address 0000 by momentarily switching to the EXAMINE (9) mode and then back to the Single Step (8) mode, or by selecting and executing *any* address.

MODE B 9 is the Examine mode. This mode permits any point on the arbitrary waveform to be monitored as a dc level at the FUNC OUT connector, and also allows the data value and voltage at the selected address to be displayed using the ARB MNTR key. To monitor any point on the arbitrary waveform, select and execute the desired address.

Example: To examine the waveform at address 19, press ADRS K 1 9 EXEC I The voltage at that point on the arbitrary waveform may now be observed at the FUNC OUT connector. If desired, press the ARB MNTR

key. A typical display might show

Of course, the data (Y) value will depend on the value previously programmed for that point on the waveform. The voltage (V) value will depend on both the programmed data value and the programmed amplitude setting.

Note that this mode requires an EXECUTE command after the address value, and that this command will change the ARB SYNC setting. After using the EXAMINE mode, the ARB SYNC must be reset to 0000 (or other desired address) by selecting and executing the address of the desired sync point.

[MODE B] [1] [0] selects the Triggered Arb with Hold on Breakpoint mode. In this mode, the programmed START and STOP addresses are ignored. Once the generator is internally, externally or manually triggered, it will continuously scan the *entire* range of arbitrary waveform memory, stopping only at the next programmed breakpoint. Breakpoints are individually set or cleared by using the [ADRS K] and [DATA L] keys. To set or clear an individual breakpoint, press the [ADRS K] key and enter the breakpoint address. Then press the [DATA L] key. The display will contain the address and the breakpoint status as either "BKPT CLR(0)" or "BKPT SET (1)". To clear the breakpoint, press [0]; to set the breakpoint press [1]. Then terminate the entry by pressing either the [ADRS K] or [DATA L] key. (An EXECUTE command is *not* required for setting or clearing an *individual* breakpoint.)

To clear *all* breakpoints, press [RCL Y] [6] [0] [0] [0] [EXEC I]. The display will read

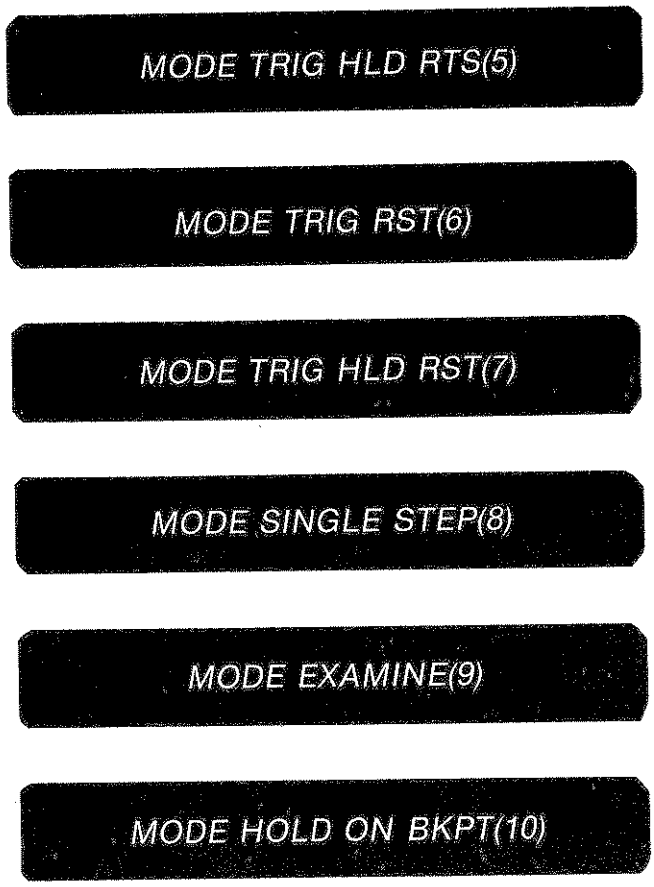
for several seconds, then

(An EXECUTE command *is* required for clearing *all* breakpoints.)

All breakpoints may be cleared by using the RCL 6000 command while the Wavetek 275 is set to any mode or function. However, clearing or setting *individual* breakpoints requires that the instrument be set to mode 10. In any other mode, the [DATA L] key enters arbitrary waveform data, not breakpoint status.

Because the Wavetek 275 ignores START and STOP addresses in mode 10 and scans the entire arbitrary waveform memory block, utilizing less than the full waveform block will require the user to reset the instrument to the programmed START address by momentarily switching to the EXAMINE (9) mode. This may be done either manually, using the front panel controls, or by remote computer control. If desired, a new START address may be programmed while the instrument is temporarily in the EXAMINE (9) mode.

The front panel displays for the various modes are:



In the front panel MODE displays, the abbreviation RTS stands for Ramp-To-Start, while RST means ReSeT. Ramp-to-Start is a *gradual* return of the waveform output voltage to the starting value, while RESET is a very *rapid* return.

3.4.2.2 Trigger Controls

The TRIG block of controls contains the parameter keys for internal/external trigger selection, internal trigger rate, external trigger slope, external trigger level (threshold), and manual trigger. The trigger keys affect the instrument output only in the TRIGGERED, GATED and BURST modes, or if the EXTERNAL WIDTH function has been selected.

3.4.2.2.1 Internal/External Key

The Internal/External trigger select key has only two parameter codes associated with it. [EXT G] [0] selects external trigger; [EXT G] [1] selects internal trigger.

3.4.2.2.2 Rate Key

The [RATE T] key selects the internal trigger rate in cycles per second (Hz). It has no effect when external trigger is selected.

3.4.2.2.3 Level Key

The [LVL XL] key selects the threshold level (in volts) for the external trigger signal applied to the TRIG IN connector. It has no effect when internal trigger is selected.

3.4.2.2.4 Slope Key

The [SLP Q] key selects the external trigger slope. A parameter code of 0 selects positive trigger slope; a code of 1 selects negative trigger slope. Positive trigger slope causes the instrument to be triggered (in the triggered modes) as the external TRIG IN signal crosses the trigger threshold level in a positive-going direction, or to remain gated ON (in the gated modes) as long as the TRIG IN signal is more positive than the programmed threshold level. Negative trigger slope causes the instrument to be triggered as the TRIG IN signal crosses the trigger threshold level in a negative-going direction, or to remain gated ON as long as the TRIG IN signal is more negative than the programmed threshold level. The [SLP Q] key has no effect when internal trigger is selected.

3.4.2.2.5 Manual Key

The [MAN J H] key manually triggers or gates the instrument when the key is pressed if external trigger has been selected.

3.4.2.3 Arbitrary Waveform Controls

The ARB control block contains the keys for arbitrary waveform address and data, START and STOP addresses, and the AUTO LINE feature.

3.4.2.3.1 Address Key

The [ADRS K] key is used to enter the arbitrary waveform address for the purpose of entering the arbitrary

waveform data, reading arbitrary waveform data, setting the breakpoints or setting the ARB SYNC address. In most modes, pressing the [ADRS K] key causes the display to show both the address (X value) and data (Y value) stored at that address. (In mode 10 the display shows address and breakpoint status.) The address value is displayed at full brightness; the data value (or breakpoint status) at reduced brightness. This indicates that any new value will be entered as an address value, not a data value (or breakpoint status). Address entries do not need an EXECUTE command, except for the purpose of setting the ARB SYNC address.

3.4.2.3.2 Data Key

The [DATA L] key is used to enter the arbitrary waveform data value (or breakpoint status) after the address has been selected. Pressing the [DATA L] key causes the display to show both the address and data value (or breakpoint status), but the data value (or breakpoint status) is at full brightness to indicate that any new value will be entered as a data value (or breakpoint status), not an address value. Data or breakpoint entries do not require an EXECUTE command.

3.4.2.3.3 Auto-Line Key

The [AUTO LINE] key causes a straight line to be written into arbitrary waveform memory between the last two data points entered.

3.4.2.3.4 Start/Stop Key

The [STRT STOP] key causes alternate displays of the START and STOP addresses and enables entry of new values. These addresses define the end-points of the portion of arbitrary waveform memory that is to be "played back" (except in mode 10, where they are ignored). Entry of START and STOP addresses requires an EXECUTE command.

3.4.2.4 Stored Setting Controls

The SETTING block of controls contains two keys; [STOR M] and [RCL Y]. These keys are used to store instrument settings in non-volatile memory, and to recall user-stored and factory-programmed settings.

3.4.2.4.1 Store Key

The [STOR M] key causes the display to show the location of the settings most recently stored or deleted, and enables entry of a storage location for the current instrument settings. The settings stored are those in scratch-pad memory (whether they have been executed or not). Locations available for user-stored settings are 1 through 75. Entering a negative value (−1 through −75) deletes the settings at the specified storage location. An EXECUTE command is not required for storing a setting. The Wavetek 275 automatically stores the current instrument settings in location 0 when power is turned off.

3.4.2.4.2 Recall Key

The [RCL Y] key causes the display to show the location of the most recently recalled settings (if any), or the message resulting from previous recall of a factory-stored setting. Attempting to recall a message from a non-existent location will result in display of the error message

A display of

indicates that the settings in that location have been deleted. An EXECUTE command is not required to recall settings to scratch-pad memory, but *is* required to transfer the settings from scratch-pad memory to waveform memory. Recall settings and selections are:

SETTINGS	RCL
Recall last power off condition	0
Recall user-stored settings	1-75
Internal calibration procedure	1000-1031
Internal QA test/demo procedure	2000-2007
Keyboard lockout off	3000
Keyboard lockout on	3001
Arb Sync output positive	4000
Arb Sync output negative	4001
Slow Ramp-to-Start	5000
Fast Ramp-to-Start	5001
Clear break points	6000

3.4.2.4.3 Output Control

The OUT block of controls contains only one key, labelled [OUT ON P]. Entering a code of 0 turns the output off and leaves the output connector in a high-impedance state. A code of 1 turns the output on. A code of 2 turns the output off, but leaves the output connector terminated in approximately 50Ω.

3.4.2.4.4 GPIB Controls

The only parameter key in the GPIB block of controls is the [ADRS] key. (The [CMD RCL] and [LCL] keys were previously defined as action keys; that is, keys that do not require a numerical parameter entry.) Pressing the [ADRS] key causes the GPIB address of the instrument to be displayed. (The GPIB address should not be confused with the arbitrary waveform address.) At power-up, the GPIB address is always that of the internal switches. A new value of GPIB address may be entered from the keyboard if the internal disable switch has not been set. An EXECUTE command is not required. Pressing the [ADRS] key causes the [CMD RCL] key to display the characters "XA" , but this code *cannot* be used to *remotely* change the GPIB address.

3.4.3 Numeric Keys

The numeric keys [0] through [9] , [+/-] , [.] and [EXP] are used to enter new parameter values. Data entry is free format (i.e., fixed point, floating point, or exponential (scientific) notation).

Fixed Point	Decimal point remains at far right.
Floating Point	You program the decimal point. It floats to the left in its designated position as you enter more numerals.
Exponential Notation	A value, then [EXP] followed by the exponent of a times ten multiplier. When the value (mantissa) is limited to one digit before the decimal point, exponential notation is called scientific notation.

Table 3-2 gives some examples of the many ways the value 100 can be programmed.

Table 3-2. Examples of Value Programming

Local (Keyboard)	Remote (ASCII)	Standard Notation
100	100	100
0100	0100	100 (leading zeroes are ignored)
1 EXP 2	1E2	1×10^2
.01 EXP 4	.01E4	$.01 \times 10^4$
.01 EXP 304	.01E304	$.01 \times 10^4$ (last two exponent digits only are used)
1000 EXP ±1	1000E-1	1000×10^{-1}
1 EXP ±2±	1E-2-	1×10^2 (two minus signs cancel)
1 EXP .2	1E.2	1×10^2 (decimal points in exponent are ignored)

The digits entered before the [EXP] key is pressed are the mantissa; the digits entered after [EXP] (only two are allowed) are the exponent. The result is the mantissa times 10 to the exponent power. For example, [9] [.] [9] [9] [EXP] [2] is equal to $9.99 \times 10^2 = 999$.

Only one decimal point and one [EXP] are allowed per number; additional ones are ignored. The sign toggle character [+/-] may appear any number of times. It causes the sign of the mantissa (if [EXP] has not been pressed) or the exponent (if [EXP] has been pressed) to

be reversed (if negative, then positive, and vice versa) each time it appears. If an undesired value is entered prior to execution (the [EXEC] key), the [CLR] key can be used to erase it.

3.4.3.1 Parameter Termination and Execution

Because the number input format is so general, the microprocessor must be told when the last numeric character has been entered so it can evaluate the number. Numeric entry can be terminated by pressing any parameter key and some other command keys. In general, any key associated with an alphabetic character (except [EXP] and [RST Z]) will terminate an entry.

When a numeric parameter entry is terminated, the new value is rounded off and tested to see if it is a legal value for the parameter being changed. If it is legal, the new value is entered into the instrument's scratch-pad memory. (See figure 3-2, Memory Structure.) Parameters are not transferred from scratch-pad memory to waveform circuit memory until the [EXP] key (or the cursor [↑] or [↓] keys) are pressed. An asterisk (*) in the display indicates that the parameter has been terminated but not yet executed, and may be erased before execution by using the [CLR] key. A few parameters that do not directly affect waveform circuit memory (such as GPIB [ADRS K] and SETTING [STOR M]) require only termination and not execution. These exceptions will be discussed separately.

3.4.3.2 Errors

Attempting to enter a value outside the legal limits of the parameter being programmed will result in an immediate error message when numeric entry is terminated. The instrument will disregard the new value and retain the previously programmed value in scratch-pad memory.

Example: Press [AMPL A] [1] [1] [AMPL A]. The display will indicate

An error message is also displayed if a non-existent or deleted stored setting is recalled.

Interparameter inconsistencies (such as amplitude and offset that are individually within limits but add up to a peak output of greater than 5V peak into 50Ω) are not tested until the [EXEC], [↑] or [↓] keys are pressed. The resulting error is displayed, and transfers of values are made to waveform circuits regardless of the error indicated.

Example: Press [AMPL A] [8] [OFST D] [4] [EXEC]. The display will indicate

3.4.4 Parameter Entry

Most parameters (commands that require a numeric entry) are entered first into scratch-pad memory, then transferred to waveform circuit memory when the [EXEC] key is pressed. (See figure 3-2, Memory Structure.) This allows the instrument user to change all output waveform parameters simultaneously. A few parameters (such as GPIB [ADRS K] and [STOR M]) do not require an [EXEC] command.

There are three basic methods of entering parameters:

1. Select the desired parameter, enter the desired numerical value or code, and execute the command. This causes an immediate parameter change.

   Example: [AMPL A] [1] [0] [EXP] [+/-] [3] [EXEC]

   causes an immediate amplitude change to 10 mV.

2. Select the desired parameter, enter the desired numerical value or code, select the next parameter, enter the desired numerical value or

code for this parameter, etc. After all parameter values have been entered, press [EXEC] to change all parameters simultaneously.

Example: [FUNC C] [2] [FUNC C] [FREQ CLK] [5] [EXP] [3] [MODE E] [0] [AMPL A] [1] [OUT ON P] [1] [EXEC] results in a continuous 5 kHz square wave with peak-to-peak amplitude of 1V and turns on the generator output. Note that in this particular example, the function was selected before the frequency, and the [FUNC C] key was pressed again to terminate the function entry before the [FREQ CLK] key was pressed.

This is necessary only if the instrument had previously been set to an arbitrary waveform function. The waveform memory contains two separate locations for non-arbitrary waveform frequency and arbitrary waveform clock period. The [FREQ CLK] key selects frequency if a non-arbitrary function has been selected, or selects clock period for an arbitrary waveform. This restriction does not apply to remote operation, as separate ASCII control characters are provided for frequency and clock.

3. Select the desired parameter, then increment or decrement the present value with the [↑] or [↓] cursor controls. (This is particularly useful for the MODE or FUNCTION parameters if you haven't yet learned their numerical codes, as the display will indicate both the parameter name and numerical code.

   Helpful Hint: When changing the MODE or FUNCTION, the error message

```
MODE/FUNC CONFLICT
```

   will be displayed if an arbitrary waveform mode and non-arbitrary waveform function are selected. This condition may be avoided if the MODE is left set at CONTINUOUS (0) while the FUNCTION is being changed.

   For parameters that will accept more than one digit of numerical value, first select the digit to be incremented or decremented with the [←] and [→] cursor controls. The display will indicate the digit selected by alternately flashing this digit bright and dim. The [←] and [→] cursor keys have no effect on parameters which accept primarily a single digit, such as MODE or FUNCTION

   Note that use of the [↑] or [↓] cursor controls will cause an automatic EXECUTE and therefore an immediate change in the waveform parameter. If this is undesirable, the generator output may be temporarily turned off during parameter changes. (Press [OUT ON P] [0] [EXEC] or [OUT ON P] [↓].)

   To continuously increment or decrement a parameter value, hold down the [↑] or [↓] cursor key.

   The cursor controls will have no effect if the displayed parameter value is followed by a cursor in the form of a horizontal underline.

   Example:

```
FREQ 1_
```

   This indicates that entry of the value has already been started using the numeric keys, and that the instrument is expecting another numeric key, another parameter key, or the [CLR] or [EXEC] key.

To display the value of a parameter without changing it, press the parameter key but do not press any numeric keys or the [↑] or [↓] cursor keys. If the first character of the display is an asterisk, it indicates that the parameter has been entered only into scratch-pad memory, and not yet into waveform memory. An undesired entry in scratch-pad memory

can be cleared with the CLR key.

Example: Press AMPL A 5 EXEC I . The display will show

AMPLITUDE 5V

Press AMPL A 1 AMPL A . The display will now show

*AMPLITUDE 1V

3.4.5 Arbitrary Waveform Controls

Arbitrary waveforms are stored as data values in a random-access memory (RAM). The RAM address corresponds to the waveform position on the X-axis of a graph or oscilloscope; the RAM data at this address corresponds to the Y-axis value. There are basically two methods of entering waveform data into the ARB RAM:

1. Waveforms composed of straight line segments may be entered using the AUTO LINE key.

2. More complex waveforms may be entered one data point at a time.

3.4.5.1 Waveform Entry with AUTO LINE Key

The first step in entering a waveform with the AUTO LINE key is to draw or graph the desired waveform, and determine the X and Y coordinates of the ends of each straight line segment. In this example, we will enter the letter "W" for display on an oscilloscope. We will arbitrarily choose to use the full standard horizontal range of 2048 points (addresses 0000 to 2047) and the full vertical range of 4096 points (data values of −2048 to +2047). A drawing of the desired waveform, including the line segment end-points, is shown in figure 3-4.

Horizontal Scale = 10 Oscilloscope Divisions = 2048 Address Points
Vertical Scale = ±2½ Oscilloscope Divisions = Data Values −2048 to +2047.

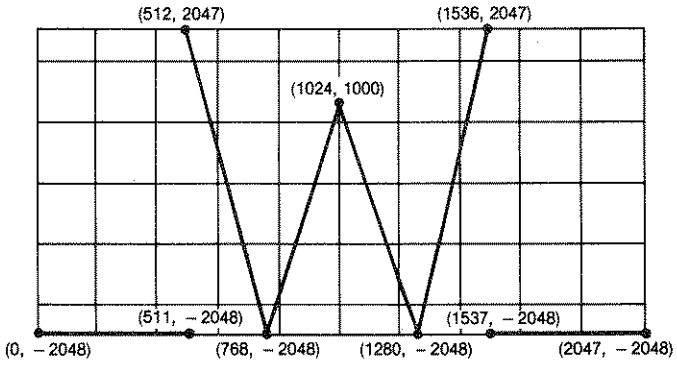
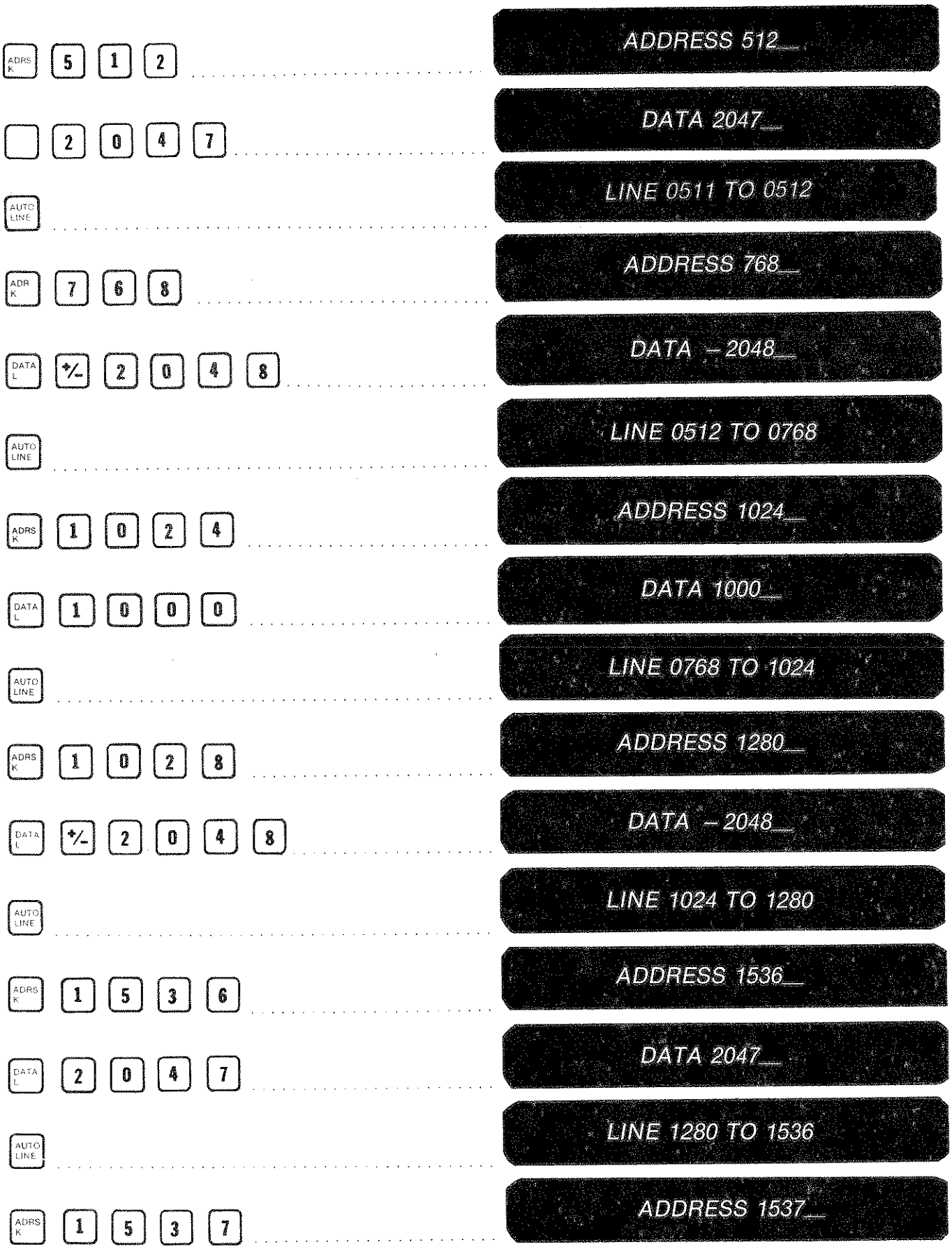


Figure 3-4. Sample Graph of Arbitrary Waveform

Keystrokes and resulting displays for entry of this waveform are shown below:

KEYSTROKES	RESULTING DISPLAY
ADRS K 0	ADDRESS 0_
DATA L +/− 2 0 4 8	DATA −2048_
ADRS K 5 1 1	ADDRESS 511_
DATA L +/− 2 0 4 8	DATA −2048_
AUTO LINE	LINE 0000 TO 0511


ADRS K 5 1 2
ADDRESS 512__
2 0 4 7
DATA 2047__
AUTO LINE
LINE 0511 TO 0512
ADR K 7 6 8
ADDRESS 768__
DATA L +/- 2 0 4 8
DATA −2048__
AUTO LINE
LINE 0512 TO 0768
ADRS K 1 0 2 4
ADDRESS 1024__
DATA L 1 0 0 0
DATA 1000__
AUTO LINE
LINE 0768 TO 1024
ADRS K 1 0 2 8
ADDRESS 1280__
DATA L +/- 2 0 4 8
DATA −2048__
AUTO LINE
LINE 1024 TO 1280
ADRS K 1 5 3 6
ADDRESS 1536__
DATA L 2 0 4 7
DATA 2047__
AUTO LINE
LINE 1280 TO 1536
ADRS K 1 5 3 7
ADDRESS 1537__

DATA L, +/-, 2, 0, 4, 8	DATA −2048_
AUTO LINE	LINE 1536 TO 1537
ADRS K, 2, 0, 4, 7	ADDRESS 2047_
DATA L, +/-, 2, 0, 4, 8	DATA 2048
AUTO LINE	LINE 1537 TO 2047
ADRS K, 0, EXEC I	X(0000) Y(−2048)
RCL V, 4, 0, 0, 0, EXEC I	ARB SYNC POSITIVE

The last two steps of the above sequence were not part of waveform entry, but were used to set the ARB SYNC at address 0 and to select positive ARB SYNC.

To set the start and stop addresses of the arbitrary waveform, press the STRT STOP key once or twice until the display contains the words STRT ADRS. Then press 0. The display will indicate

START ADRS 0_

Now press STRT STOP, 2, 0, 4, 7, EXEC I

The display will show

STOP ADRS 2047

To display the waveform on an oscilloscope, let's first arbitrarily choose an output level of 5V peak-to-peak and a waveform frequency of 100 Hz. The arbitrary waveform generator clock period for a 100 Hz waveform containing 2048 steps is calculated in the following manner:

100 cycles per second is equal to 0.01 seconds per cycle. 0.01 seconds per cycle divided by 2048 steps per cycle equals 4.88 microseconds per step.

To obtain the continuous arbitrary waveform at the desired amplitude and frequency, press the following keys: MODE B, 0, FUNC C, 6, AMPL A, 5, FREQ CLK, 4, ., 8, 8, EXP, +/-, 6, OUT ON P, 1, EXEC I

The waveform may now be observed by connecting the oscilloscope to the FUNC OUT connector and externally triggering the scope from ARB SYNC OUT.

3.4.5.2 Point-by-Point Waveform Entry

Waveforms not made up of straight line segments may be entered into arbitrary waveform memory one data point at a time. Extremely complex waveforms are most easily entered by remote computer control. In the following example, we will enter a simple 20 step staircase waveform from the keyboard. We will arbitrarily choose to place the waveform in ARB RAM addresses 0000 to 0019, use data values of 0000 to 1900 in increments of 100, and display the waveform at a 100 Hz rate (1 mS per division on an oscilloscope screen 10 divisions wide.)

In this example, we will choose to set the ARB RAM start and stop addresses before entering the waveform data into memory.

Press the STRT STOP key. If the display contains the words STOP ADRS, push the STRT STOP key again, and the display will indicate the current setting for the start address. If

the current value displayed is not

START ADRS 0000

press the [0] and [EXEC] keys. Press the [STRT STOP] key again. If the display does not show

STOP ADRS 0019

press the keys [1] [9] [EXEC]. The display will now show

STOP ADRS 0019

To enter the waveform into memory, press the following keys:

[ADRS] [0] [DATA] [0]
[DATA] [1] [0] [0]
[DATA] [2] [0] [0]
[DATA] [3] [0] [0]
[DATA] [4] [0] [0]
[DATA] [5] [0] [0]
[DATA] [6] [0] [0]
[DATA] [7] [0] [0]
[DATA] [8] [0] [0]
[DATA] [9] [0] [0]
[DATA] [1] [0] [0] [0]
[DATA] [1] [1] [0] [0]
[DATA] [1] [2] [0] [0]
[DATA] [1] [3] [0] [0]
[DATA] [1] [4] [0] [0]
[DATA] [1] [5] [0] [0]
[DATA] [1] [6] [0] [0]
[DATA] [1] [7] [0] [0]
[DATA] [1] [8] [0] [0]
[DATA] [1] [9] [0] [0]

Press [DATA] again. The display will indicate an address (X value) of 0020 and the data (Y value) previously stored at this address. Note that terminating the data entry with the [DATA] key automatically incremented the address, making it unnecessary to specify an address (other than the starting address) during point-by-point entry of waveform data. However, the last data entry has left the address set at 0020, which is outside the 0000 to 0019 range of the start and stop addresses that we previously entered. If the instrument were left in this condition, the next operation of the [EXEC] key or the [↑] or [↓] cursor keys would cause the ARB SYNC to be set to address 0020, which is outside our specified waveform block, and *the ARB SYNC pulse would never occur!* To prevent this, we will set the ARB SYNC to address 0000 by pressing [ADRS] [0] [EXEC]. We will also select positive ARB SYNC by pressing [RCL] [4] [0] [0] [0] [EXEC].

The instrument will verify this setting by displaying

ARB SYNC POSITIVE

To set the waveform block frequency to 100 Hz, calculate the required clock period in the following manner:

100 cycles per second is equal to 0.01 seconds per cycle. 0.01 seconds per cycle divided by 20 steps per cycle is equal to 500 μs per step.

To enter a 500 μs clock period press [FREQ CLK] [5] [0] [0] [EXP] [+/-] [6] [EXEC].

Note that the waveform amplitude shown on the oscilloscope is less than the Wavetek 275 displays when the [AMPL] key is pressed. This is because the

Wavetek 275 display shows the peak-to-peak amplitude for the full 4096 point range of the ARB RAM, but our demonstration waveform range is only 1900 points. For this waveform, the Wavetek 275 amplitude should be set to (4096/1900) X the desired waveform amplitude. To get an actual amplitude of 1Vp-p for our demonstration waveform, set the instrument amplitude to 2.16V.

3.4.5.3 Multiple Arbitrary Waveforms

The number of arbitrary waveforms that may be stored in arbitrary waveform memory is limited only by the complexity (number of data points) of each waveform and the number of total waveform storage locations (2048 standard, 8192 optional). Each waveform may be "played back" separately by entering and executing the ARB SYNC, START and STOP addresses of the portion of the arbitrary waveform memory that contains the desired waveform. These addresses (and other waveform parameters) may then be stored in a separate stored setting memory, making it possible to recall a different arbitrary waveform with a maximum of four keystrokes. The START and STOP addresses are entered with the [STRT STOP] key; the ARB SYNC address is entered with the [ADRS K] key.

NOTE

Failure to set the ARB SYNC address within the range of the START and STOP addresses will result in the ARB SYNC pulse never occurring.

3.4.5.4 Checking and Monitoring Arbitrary Waveform

There are four methods which can be used to check or monitor the arbitrary waveform. These are:

1. Use the [ADRS K] and numeric keys to enter and terminate an address, then read the address and data values from the display. This method works in any mode except mode 10, where the display will indicate breakpoint status instead of data value. The generator may be set for a non-arbitrary waveform, or an arbitrary waveform that is running (is being clocked.)

   Example: For our 20 step staircase demonstration waveform, press [ADRS K] [1] [8] [ADRS K] . The display will show

   X(0018) Y(1800)

   Press [1] [9] [ADRS K] . The display will show

   X(0019) Y(1900)

2. Select the ARBITRARY (6) function and EXAMINE (9) mode. Select *and execute* the desired address, then press the [ARB MNTR] key and read the address, data value and actual voltage at this point on the waveform on the display. The waveform voltage may also be monitored at the FUNC OUT connector with a dc voltmeter or oscilloscope terminated in 50Ω.

   Example: For our 20 step staircase demonstration waveform, press [FUNC C] [6] [MODE B] [9] [ADRS K] [1] [8] [EXEC I] [ARB MNTR] . The display will indicate

   X0018 Y + 1800 V + 0.949

   Press [ADRS K] [↑] [ARB MNTR]. The display will show

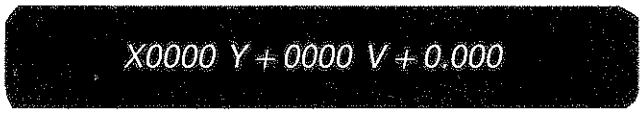
   X0019 Y + 1900 V + 1.002

3. Select the ARBITRARY (6) function and SINGLE STEP (8) mode. Select and terminate *any* address to return to the starting address. Select and execute either external trigger, or internal trigger and trigger rate. Press the [ARB MNTR] key and read the address, data value and actual voltage at each point on the waveform. Voltage may also be monitored at the FUNC OUT connector with a dc voltmeter or oscilloscope terminated in 50Ω. If external trigger has been selected, the manual trigger key must be pressed each time it is desired to advance the waveform to the next step. (Or the instrument may be triggered from an external signal at the TRIG IN connector.) When the waveform reaches the previously programmed STOP address, the next internal or external trigger

pulse will return the waveform to the START address.

Examples: For our 20 step staircase demonstration waveform:

a. Press [FUNC C] [6] [MODE B] [8] [ADRS K] [0] [EXT G] [0] [EXEC I] [ARB MNTR]. Repeatedly pressing the [MAN J H] key will cause the display to advance from



to

b. Press [FUNC C] [6] [MODE B] [8] [ADRS K] [0] [ARB MNTR] [EXT G] [1] [RATE T] [1] [EXEC I]. The display will automatically advance at one second per step from

to

The display may be returned to the starting address at any time by pressing [ADRS K] [0] [ADRS K] [ARB MNTR].

4. Select and execute ARBITRARY (6) function, any desired mode, and a slow clock speed (such as one second.) Press the [ARB MNTR] key and observe the arbitrary waveform address, data value and actual output voltage on the display. (In the triggered and gated modes it will be necessary to trigger the generator.) Note that during Ramp-to-Start (RTS) operations, the displayed address will remain at the programmed stop address while the amplitude data and voltage both return to the value programmed for the start address.

NOTE

After checking or monitoring the arbitrary waveform, don't forget to reset the ARB SYNC to the desired location by selecting and executing the desired address.

3.4.6 Stored Settings

User instrument settings may be stored in up to 75 internal memory locations, and later accessed either randomly or sequentially. In addition, the internal memory also contains an internal QA Test/Demonstration procedure and instrument settings used during the internal stored calibration procedure. Current instrument settings are automatically stored in location zero for retention when power is turned off. Seven memory locations contain commands that the user recalls to control front panel lockout, arbitrary waveform sync polarity, arbitrary waveform Ramp-to-Start rate, and to clear all arbitrary waveform breakpoints.

3.4.6.1 Storage of Setting

To store an instrument setting, enter the desired parameters into scratch-pad memory. It is not necessary to transfer the parameters to waveform memory by pressing the [EXEC I] key. Press the [STOR M] key, enter the number of the desired storage location (1 to 75), and press the [STOR M] key again.

Example: To store settings in memory location 75, press [STOR M] [7] [5] [STOR M]. The display will indicate

3.4.6.2 Deletion of Stored Setting

To delete a stored setting, press the [STOR M] key, the [+/-] key, and the number of the storage location to be deleted. Then press the [STOR M] key again.

Example: To delete stored setting 75, press [STOR M] [+/-] [7] [5] [STOR M]. The display will indicate

No. 75 LAST DELETED

3.4.6.3 Recall of Stored Setting

To recall a stored setting, press the [RCL Y] key and the number of the setting to be recalled. Press the [RCL Y] key again to transfer the setting to scratch-pad memory, or press the [EXEC I] key to transfer the setting to waveform memory.

Examples:

To recall stored setting 3 to scratch-pad memory, press [RCL Y] [3] [RCL Y].

To recall stored setting 3 to waveform memory, press [RCL Y] [3] [EXEC I].

In either case, the display will indicate

No. 3 LAST RECALLED

Attempting to recall a deleted setting will result in a display of

CANNOT RECALL

3.4.6.4 Modification of Stored Setting

To modify a stored setting, recall the setting to scratch-pad memory, enter new value(s) for the parameter(s) to be changed, then store the setting back in the previous location.

Example: To change the amplitude parameter in stored setting #3 to 5V, press [RCL Y] [3] [AMPL A] [5] [STOR M] [3] [STOR M].

3.4.6.5 Recall of Consecutive Stored Settings

To recall consecutive stored settings, recall and execute the first stored setting. Then use the cursor [↑] key to recall the next higher-numbered stored setting, or the [↓] key to recall the next lower-numbered stored setting. Using the cursor keys causes an automatic EXECUTE, and also causes deleted settings to be skipped.

Example:

KEYSTROKES DISPLAY AFTER KEYSTROKES

[RCL Y] [1] [0] [EXEC I]

No. 10 LAST RECALLED

[↑]

No. 11 LAST RECALLED

[↓]

No. 12 LAST RECALLED

3.4.6.6 Recall of Last Power Off Condition

To recall the last power-off condition of the instrument, press [RCL Y] [0] [EXEC I]. Note that this command must be used *immediately* after power-on, *before* any other command is executed. Memory #0 is constantly updated with instrument status at each press of the [EXEC I] key, and will no longer contain the previous power-off parameters after any other command is executed.

3.4.6.7 Stored Performance Verification

An internally stored program exercises the instrument circuits to enable a quick verification of operation. An oscilloscope must be used to observe this procedure. Connect as shown in figure 3-5 and set up the scope as follows:

1. Trigger on sync output (CH2).
2. Set time/Div to 0.2 mS.
3. Set CH1 to 5V/Div.
4. Set CH2 to 2V/Div.

Press [RCL Y] [2] [0] [0] [0] [EXEC I] to start the

Recommended Oscilloscope Settings:

1. Trigger on sync output (CH2).
2. .2 ms. Time/Div.
3. CH1 : 5V/Div
   CH2 : 2V/Div

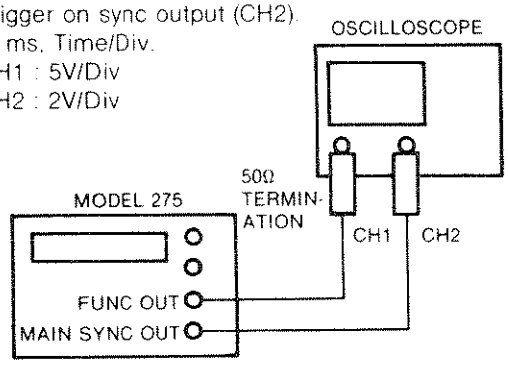


Figure 3-5. Test Connections for Stored Performance Verification

Quality Assurance procedure. The display will indicate

```
(0) BEGIN QA PROC
```

The oscilloscope displays a function output sine wave and a sync output square wave.

Press [↑] to select these steps:

1. A rapid stepping of frequencies.
2. A rapid stepping of amplitude.
3. A square wave that steps from a negative to positive offset and repeats.

For the remaining steps trigger the scope on the CH1 FUNC OUT signal.

4. A trigger circuit test.
5. A gate circuit test.
6. A burst circuit test.

3.4.6.8 Calibration Procedure

The calibration procedure is called by pressing [RCL Y] [1] [0] [0] [0] [RCL Y]. The front panel display will read "(0) CAL 275 VX.Y)" where X.Y identifies the software version. Each press of [↑] steps to the next calibration prompt. Press [↑] and observe the display:

```
(1) +15V SUPP, R39
```

This display tells the technician to adjust the +15V power supply with potentiometer R39. By pressing [↑], all calibration prompts can be displayed and required internal control setups will be made automatically. Test points and test equipment setup are included in section 5 of the manual.

3.4.6.9 Front Panel Lockout

To lock out the front panel controls that directly affect the output waveform, press [RCL Y] [3] [0] [0] [1] [RCL Y]. The display will indicate

```
LOCKOUT ON
```

With the lockout on, pressing the [EXEC], [RST Z], [ADRS K], [DATA L] or [AUTO LINE] keys will result in a front panel display of

```
PANEL LOCKOUT ON
```

Pressing other keys that normally affect the output waveform will result in placing the new parameter into only scratch-pad memory. The display will show an asterisk (*) in front of the parameter value.

To turn off the front panel lockout, press [RCL Y] [3] [0] [0] [0] [RCL Y]. The display will show

```
PANEL LOCKOUT OFF
```

NOTE

This command is not the same as the local lockout (LLO) command that can be programmed remotely.

3.4.6.10 Arbitrary Waveform Sync Polarity

To select positive arb sync polarity, press [RCL Y] [4]

[0] [0] [0] [EXEC]. The display will indicate

ARB SYNC POSITIVE

To select negative arb sync polarity, press [RCL Y] [4] [0] [0] [1] [EXEC] The display will show

ARB SYNC NEGATIVE

Note that this command requires the [EXEC] key to be pressed.

3.4.6.11 Ramp-to-Start Rate

To select slow ramp-to-start rate, press [RCL Y] [5] [0] [0] [0] [EXEC]. The display will show

RTS RATE SLOW

For fast ramp-to-start rate, press [RCL Y] [5] [0] [0] [1] [EXEC]. The display will indicate

RTS RATE FAST

This command requires the [EXEC] key to be pressed.

Fast RTS rate requires about 20 seconds to ramp the arbitrary waveform over the full arbitrary waveform data range of −2048 to +2047. Slow RTS rate requires about a minute and 20 seconds. RTS time depends only on the selected rate and the difference between the arbitrary waveform data values at the START and STOP addresses. It is independent of AMPLITUDE and CLOCK settings.

3.4.6.12 Breakpoint Clear

To clear all arbitrary waveform breakpoints, press [RCL Y] [6] [0] [0] [0] [EXEC]. The display will show

CLEAR BREAK POINT

This command also requires the [EXEC] key to be pressed.

3.4.7 VCG Operation

The frequency of the main (non-arbitrary) waveform generator may be controlled by an ac or dc signal applied to the VCG IN BNC connector. A positive control voltage will increase the generator frequency; a negative voltage will decrease frequency. Frequency may be changed by the VCG control voltage only within a frequency range. Table 3-3, Internally Selected Frequency Ranges, shows the frequency ranges and corresponding VCG ranges. Figure 3-6, VCG (FM) Nomograph, illustrates the VCG voltage required to change the programmed frequency to the desired output frequency. (Frequencies in this figure are shown as significant digits, without the range multiplier.) Frequency range must be selected before applying the VCG signal.

For example, Table 3-3 shows that if the frequency is programmed to 500 Hz, the Wavetek 275 selects the 10^2 range. As shown in the example of Figure 3-6, a programmed frequency of 500 Hz and a +5V VCG input will produce an actual output frequency of 1 kHz.

Another example is a 1200:1 frequency sweep from 1 kHz to 1.2 MHz using 0.01 to 12.0 volt VCG signal.

Table 3-3. Internally Selected Frequency Ranges

Range Name	Programmed Frequency Range	VCG Range
10^6	1.00 MHz-12.0 MHz	10.0 kHz-12.0 MHz
10^5	100 kHz-999 kHz	1.00 kHz-1.20 Mhz
10^4	10.0 kHz-99.9 kHz	100 Hz-120 kHz
10^3	1.00 kHz-9.99 kHz	10.0 Hz-12.0 kHz
10^2	100 Hz-999 Hz	1.00 Hz-1.20 kHz
10^1	10.0 Hz-99.9 Hz	100 mHz-120 Hz
10^0	1.00 Hz-9.99 Hz	10 mHz-12.0 Hz
10^{-1}	100 mHz-999 mHz	1.00 mHz-1.20 Hz
10^{-2}	10.0 mHz-99.9 mHz	100 μHz-120 mHz

Table 3-3 shows that the frequency range is 10^5. To get in that range, program any value within the 10^5 range. Next, program [FREQ CLK] [0] [EXEC] . The display will show

FREQ 0 HZ (VCG)

(This will leave the generator set to the desired range, but remove the internally generated frequency control voltage.) A 0.01 volt VCG voltage will cause the output frequency to be 1 kHz, and a 0.01V to 12V VCG input will cause a 1 kHz to 1.2 MHz frequency sweep.

The VCG input has no effect on an arbitrary waveform.

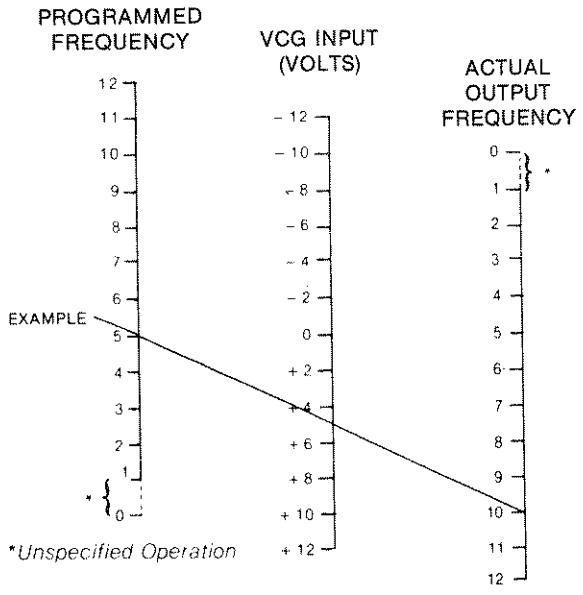


Figure 3-6. VCG (FM) Nomograph

3.5 REMOTE OPERATION

The Wavetek 275 may be remotely controlled via the General Purpose Interface Bus (GPIB). To remotely control the instrument:

1. Connect the instrument to the GPIB system with the standard GPIB connector. (See section 2.2.3 of the manual.)
2. Set the instrument GPIB address to a unique device identification number (between 0 and 30) either with the internal switches or with the front panel GPIB ADRS key. (See section 2.2.4 of the manual.)
3. Remotely program the desired instrument GET, SRQ and Talk responses by sending the XG, XQ and XT codes along with the proper numerical value for each parameter. (The exact method of sending the characters will depend on the type of controller being used.)
4. Send the desired ASCII control codes over the GPIB to the instrument.

3.5.1 ASCII Control Codes

The remote control ASCII characters for the Wavetek 275 are listed in Appendix B, Programming Command Summary. Please note that:

1. Not all front panel keys have a directly equivalent remote control command. These keys are:

   ARB MNTR
   The cursor keys ↑, ↓, ←, →
   CLR
   ♪
   STAT
   SRQ
   GPIB ADRS
   CMD RCL
   LCL

2. Not all remote control commands have a directly equivalent front panel key. These commands are:

   Percent Frequency (XF)
   GET mode (XG)
   SRQ Mode (XQ)
   Talk Mode (XT)
   Recall Next Lesser Numbered Program (XU)
   Terminator (XV)
   Recall Next Greater Numbered Program (XW)

3. In most cases, the front panel keys that have an equivalent remote control command are marked with the corresponding ASCII control codes. The exceptions are:

   EXP
   FREQ CLK
   STRT STOP
   AUTO LINE

4. Some of the remote control commands consist of two letters, and start with the letter "X". This letter "X" is merely a prefix that is used in order to allow the number of remote control codes to exceed the number of letters in the alphabet. These two-letter codes must be sent without any

space, punctuation or other character between the letters.

5. A few front panel keys perform two functions, but have separate remote control codes for the two functions. These keys are:

   FREQ CLK
   MAN trigger
   STRT STOP

3.5.2 Setting Instrument GET, SRQ and Talk Modes

3.5.2.1 Setting the Talk Mode

The Talk mode determines what the instrument will say when it is addressed as a talker on the GPIB. The talk mode is remotely programmed with the XT command. Valid parameter values are XT0 through XT11. Only one talk response may be programmed at any one time.

XT0 Programming error list (only errors from GPIB input). XT0 is the power-up talk mode. A typical error string is E 1F 2AD 3Y. Some error string characteristics are:

a. All error strings begin with E.

b. Most recent error is at the end of string.

c. Errors are separated by blanks.

d. Class 1 errors: A 1 followed by programming character that caused the error.

e. Class 2 errors: A 2 followed by the two conflicting program characters.

f. Class 3 errors: A 3 followed by M (store) or Y (recall).

g. Error strings can be up to 80 characters including E and blanks.

h. After transfer, the instrument clears the error string.

XT1 Poll Byte Response. The byte that would be sent if a serial poll were to be performed. The controller, upon reading this byte, clears the poll byte and resets the SRQ line if asserted.

XT2 The most recently selected parameter and its value. Example: FREQ 1E3. (The "most recently selected parameter" is the parameter at the end of the command string.) If no parameter is selected; e.g., power-on state, reset, or execute command, then the instrument returns NO PARAMETER SELECTED. Note that the NO PARAMETER SELECTED message will be returned if the last command in the string is an EXECUTE command (I).

XT3 The entire instrument setup after last execute. Example: F1EA1D0C0P0Q0XL1.5.

XT4 The instrument setup when execute is received; same format as XT3.

XT5 Instrument Identification: WAVETEK MODEL 275 V(X.Y). X.Y identifies the software version number.

XT6 The time since the instrument was powered on. Example: TIME: 1.3. Unit of measure is hours with 0.1 hour (6 minute) resolution.

XT7 The accumulated operating time. Example: TOTAL TIME: 306.2. NOTE: Toggling switch 7 (figure 2-2) clears the instrument operating-time clock. With SW7 on, the clock runs during power on. With SW7 off, the clock clears to zero.

XT8 The number of stored settings installed. For the standard Wavetek 275: STORED SETTINGS 75.

XT9 Readback of ARB generator status: Returns the instantaneous value of the ARB output in the form "X D.DDED Y D.DDED V D.DDED".

XT10 Returns the data at the current address then increments the address. Used to load a waveform from a Wavetek 275 to a controller. Returns " – 9999" when front panel lockout is activated.

XT11 Returns the data value at the beginning of the Ramp-to-Start (RTS) operation.

XT12 For factory use only.

3.5.2.2 Setting the SRQ Mode

The SRQ mode determines the conditions under which the instrument will send a service request message (SRQ) to the controller. Unlike the Talk mode, which allows only one response at a time to be programmed, the SRQ mode may be programmed for any desired combination of conditions.

XQ followed by a value (0 through 255) selects the conditions under which the Wavetek 275 asserts the SRQ line and rsv (request for service) bit. The equivalent binary value is a "mask" for the serial poll response byte (shown in table 3-4). The binary mask selects certain conditions that will be recognized as conditions that assert the SRQ line and rsv bit. All other conditions are ignored (masked).

Table 3-4 shows the serial poll response byte. Each of the 8 bits represents a condition that, if selected by

the SRQ mode, will assert the GPIB's SRQ line and the serial poll byte's rsv bit. Each bit may be selected individually or in various combinations. The rsv bit (bit decimal value 64) will have no effect if selected.

For example, XQ1 dictates that the SRQ line and the serial poll byte's rsv bit are asserted when there is a program error; such as a frequency beyond the instrument's limits. The serial poll response byte will be 0100 0001.

In another example, XQ131 dictates that the SRQ line and the rsv bit are asserted when a program error has occurred, the output protection is enabled, or the SRQ key is pressed. The serial poll response byte will be 1100 0011.

To select the SRQ mode:

1. Determine the conditions under which you want the instrument to sent an SRQ message to the controller.
2. Look up (in table 3-4) the decimal value of the serial poll response bit that corresponds to each desired condition.
3. Add the decimal values of the selected bits.
4. Program the instrument with the XQ code and this decimal value.

3.5.2.3 Setting the GET Mode

XG followed by its code selects what actions occur when a Group Execute Trigger (GET) command is sent to the Wavetek 275. This code may only be 0.

With "XG" set to "0" and upon receipt of the GET, the programmed waveform values are transferred to the waveform generator circuits, and then the microprocessor sends a trigger pulse if the mode is not continuous. This is the same sequence of events that would occur if an execute, then a trigger action (IJH) were programmed, except that no error checking is done. GET mode 0 is the power-up condition.

3.5.3 Setting the End of String (Terminator) Character.

XV followed by its argument designates a new End Of String (EOS) or terminator character. The argument is the decimal value of the ASCII character that is to be the new terminator (the EOS character recognized by the Wavetek 275). Any ASCII character except NUL is accepted.

The terminator character has two uses. During output, it is appended to the end of every response to a

Table 3-4. Serial Poll Response Byte

Bit Binary Position	Bit Decimal Value	Bit Name	Bit Description
1000 0000	128 (MSB)	SRQ Key	Indicates that front panel SRQ key has been pressed.
0100 0000	64	rsv	Request for Service.
0010 0000	32	RTS Complete	Indicates that Ramp-to-Start operation has been completed.
0001 0000	16	Execute Complete	Indicates that execute command has been completed.
0000 1000	8	Low Battery	Indicates a low battery level for memory back-up battery.
0000 0100	4	Fuse Blown	Indicates output connector fuse has blown.
0000 0010	2	Output Protection	Indicates output protection is tripped.
0000 0001	1 (LSB)	Program Error	Indicates a program error.

talk request on the GPIB. During input, it signals the end of a group of programming characters. Since it is always recognized, even in a quoted string, it can be used to ensure that the instrument is in a known state, so that following programming characters will be interpreted correctly.

At power-on time, the EOS character is the line feed control character, ASCII character LF (decimal value 10). When the Wavetek 275 issues a talk message, the EOS character is the last byte sent. In addition, the End Or Identify (EOI) line is pulsed low (END message) during the EOS character transmission. If the GPIB controller does not look for the END message (EOI line low), and it does not recognize the Line Feed (LF) as a string terminator, a new EOS character will be needed. For example, to change the EOS character from an LF to a Carriage Return (CR), program XV13. (Numerical values of ASCII characters are listed in Appendix A.)

3.5.4 Remote Control of Instrument Display

The single quote character (') is used to program a string of characters to be displayed on the front panel display. Program a single quote, the characters to be displayed, followed by either another single quote or by the terminator character. When the second quote or the terminator is programmed, the first 20 characters programmed after the first quote are displayed on the front panel. If fewer than 20 characters are programmed, then blanks are added to fill the display.

3.5.5 Differences Between Controllers

GPIB control commands are *not* part of the standardized BASIC computer language, and will vary from one make of controller to the next. For example, the Wavetek 6000 Instrumentation Computer uses a WRITE statement to send information to the instrument, while another make uses an OUTPUT command. Obviously, you will have to consult your controller manual for the proper controller commands. The GPIB commands and sample programs in this manual were written using a Wavetek 6000 Instrumentation Computer, with the Wavetek 275 GPIB address set to 09.

3.5.6 Sending Instrument Commands

To send GPIB commands to the Wavetek 275 it is not necessary to individually control the GPIB lines or send bus management commands such as "attention" or "unlisten". The controller handles this chore automatically. For example, to set the instrument output amplitude to 5V, the command is WRITE @709:"A5I". This command sends the ASCII characters "A5I" via interface 7 to instrument 09. Alphabetic characters must be sent enclosed in quotation marks or as an alphanumeric variable. Numeric characters may also be sent as a numeric value or a numeric variable. For example, if the numeric variable X contains the value 5 and alphanumeric variable Y$ contains the ASCII characters A5I, then the following commands are all equivalent:

```
WRITE @709:"A5I"
WRITE @709:"A",5,"I"
WRITE @709:"A",X,"I"
WRITE @709:Y$
```

3.5.7 Reading Instrument Responses

Except for asserting the SRQ line, the instrument will not transmit data on the bus until it is commanded to do so by the controller. The two ways that the controller requests information are with a talk command or a serial poll. (The Wavetek 275 does not use the parallel poll.)

3.5.7.1 Talk Command

The controller we are using in these examples uses a READ statement to command the instrument to talk. The instrument response is read into an alphanumeric variable, then the variable is displayed on the controller screen. *What* the instrument will say when it is addressed to talk depends on the talk message (XT) code previously programmed. The commands used are:

```
READ @709:READBACK$
WRITE @0:READBACK$
```

3.5.7.2 Serial Poll

A serial poll is usually performed after one of the instruments on the bus asserts the SRQ line. It is done to determine *which* instrument originated the SRQ, and *what* the the problem (or condition) is. The serial poll response byte is read into a numeric variable. The numeric value of the variable may be printed or displayed, or the bits in the variable can be individually checked and a predetermined action taken. The conditions that will cause the SRQ line to be asserted depend on the previously programmed value of the SRQ (XQ) code.

Example 1:

```
STATUS @709:DEVICE_STATUS
WRITE @0:"DEVICE STATUS = ";DEVICE_STATUS
```

Example 2:

```
STATUS @709:STATUS_BYTE
IF BIT(0,STATUS_BYTE) THEN WRITE @0:"PRO-
  GRAM ERROR"
IF BIT(1,STATUS_BYTE) THEN WRITE @0:"OUT-
  PUT PROTECTION"
IF BIT(2,STATUS_BYTE) THEN WRITE @0:"FUSE
  BLOWN"
IF BIT(3,STATUS_BYTE) THEN WRITE @0:"LOW
  BATTERY"
IF BIT(4,STATUS_BYTE) THEN WRITE @0:"
  EXECUTE COMPLETED"
IF BIT(5,STATUS_BYTE) THEN WRITE @0:"RAMP-
  TO-START COMPLETED"
IF BIT(7,STATUS_BYTE) THEN WRITE @0:"FRONT
  PANEL SRQ KEY PRESSED"
```

Note that in the above example that we did not check the condition of bit 6 in the serial poll response byte. This is the "request for service" bit, and will automatically be 1 if any of the other bits are 1. However, in a large system with many instruments on the bus, it may be desirable to first check bit 6 to determine which instrument(s) are requesting service, then check the remaining bits to determine what services the instrument is requesting.

3.5.8 SRQ Interrupts

The method of handling SRQ interrupts is highly dependent on the type of controller. For the controller used for the sample demonstration programs in this manual, SRQ interrupts are handled by interrogating the GPIB registers and storing the value in a numeric variable. Bit 10 in this numeric variable, which corresponds to the status of the SRQ line, is then checked to see if the bit value is 1. If so, a serial poll is then performed to determine which instrument(s) requested service.

The following example is from the sample demonstration programs in this manual:

Example:

```
• • •
170 GO SUB CHECK_FOR_SRQ
• • •
260 CHECK_FOR_SRQ:ASK @7:GPIB_REGISTERS
• • •
270 IF BIT(10,GPIB_REGISTERS) THEN GO SUB
SERIAL_POLL.
• • •
```

Statement 170 sends the program to the subroutine labelled CHECK_FOR_SRQ.

Statement 260 copies the contents of the GPIB registers into numeric variable GPIB_REGISTERS.

Statement 270 checks bit 10 in the numeric variable GPIB_REGISTERS, and if it is equal to 1 sends the program to the subroutine labelled SERIAL_POLL.

Once again, the reader is reminded that the sample programs and statements in this manual were written using one particular make of controller, and that it will be necessary for the user to check the programming manual for his controller.

3.5.9 Sample Demonstration Programs

Because each test system is unique and controller programming commands are not standardized, it is impossible to provide actual application programs in this manual. The following sample demonstration programs were written for a Wavetek 6000 Instrumentation Computer controlling a single instrument (the Wavetek 275), and demonstrate instrument control, readback from instrument, SRQ interrupts and the serial poll, and loading of computer-generated arbitrary waveforms. The programs also demonstrate some of the Wavetek extensions of the BASIC computer language: Program labels, DO loops, and unlimited length variable names. In all programs, the Wavetek 275 GPIB address is set to 9. The programs are presented as tables containing both the actual program statements and explanatory comments.

Table 3-5 contains a simple program to send control commands to the Wavetek 275 and read back the instrument response. It does not monitor the SRQ line nor perform a serial poll.

Table 3-5. Sample Demonstration Program 275-1

Program Statements	Explanation
100 ! PROGRAM 275-1	Comment statement containing program identification.
110 DIM CONTROL$*80	Set length of alphanumeric control variable for maximum expected number of control characters.
120 DIM READBACK$*80	Set length of alphanumeric readback variable for maximum expected number of readback characters.
130 CLEAR	Clear controller screen.
140 DO	Start of endless loop. (No UNTIL or WHILE condition is specified.)
150 WRITE @0:"ENTER ASCII CONTROL CODES."	Prompt user for control codes.
160 INPUT CONTROL$	Stop program while user types instrument control codes into controller, then place control codes into alphanumeric variable CONTROL$.
170 WRITE @709:CONTROL$	Send control codes in alphanumeric variable CONTROL$ via interface 7 (GPIB) to instrument with GPIB address 9 (Wavetek 275).
180 READ @709:READBACK$	Command instrument on interface 7 address 9 to talk. Place received data in alphanumeric variable READBACK$.
190 WRITE @0:READBACK$	Display contents of alphanumeric variable READBACK$ on controller screen.
200 LOOP	End of loop. Return to DO statement to prompt user for next instrument control codes.
210 END	End of program.

Table 3-6 contains a slightly more elaborate program to send control commands to the Wavetek 275 and read back the instrument response. It does not monitor the SRQ line, but does perform a serial poll and display the results as a numerical value.

Table 3-6. Sample Demonstration Program 275-2

Program Statements	Explanation
100 ! PROGRAM 275-2	Comment statement containing program identification.
110 DIM CONTROL$*80	Set length of alphanumeric control variable for maximum expected number of control characters.
120 DIM READBACK$*80	Set length of alphanumeric readback variable for maximum expected number of readback characters.
130 CLEAR	Clear controller screen.
140 DO	Start of endless loop. (No UNTIL or WHILE condition is specified.)
150 WRITE @0:"ENTER ASCII CONTROL CODES."	Prompt user for control codes.
160 INPUT CONTROL$	Stop program while user types instrument control codes into controller, then place control codes into alphanumeric variable CONTROL$.
170 WRITE @709:CONTROL$	Send control codes in alphanumeric variable CONTROL$ via interface 7 (GPIB) to instrument with GPIB address 9 (Wavetek 275).
180 READ @709:READBACK$	Command instrument on interface 7 address 9 to talk. Place received data in alphanumeric variable READBACK$.
190 WRITE @0:READBACK$	Display contents of alphanumeric variable READBACK$ on controller screen.
200 STATUS @709:DEVICE_STATUS	Read the status byte of device 09 (Wavetek 275) on port 7 (GPIB). Place results in numeric variable DEVICE_STATUS.
210 WRITE @0:"DEVICE STATUS = "; DEVICE_STATUS	Display value of numeric variable DEVICE_STATUS on controller screen.
220 LOOP	End of loop. Return to DO statement to prompt user for next instrument control codes.
230 END	End of program.

Table 3-7 contains a program to send control commands to the Wavetek 275, read back the instrument response, monitor the SRQ line, perform a serial poll and display the results as a message on the controller screen. Because the program stops at the INPUT statement, it does *not* monitor for a *delayed* SRQ, such as "RAMP-TO-START COMPLETED".

Table 3-7. Sample Demonstration Program 275-3

Program Statements	Explanation
100 ! PROGRAM 275-3	Comment statement containing program identification.
110 DIM CONTROL$*80	Set length of alphanumeric control variable for maximum expected number of control characters.
120 DIM READBACK$*80	Set length of alphanumeric readback variable for maximum expected number of readback characters.
130 CLEAR	Clear controller screen.
140 DO	Start of endless loop (no UNTIL or WHILE condition is specified).
150 WRITE @0:"ENTER ASCII CONTROL CODES."	Prompt user for control codes.
160 INPUT CONTROL$	Stop program while user types instrument control codes into controller, then place control codes into alphanumeric variable CONTROL$.
170 WRITE @709:CONTROL$	Send control codes in alphanumeric variable CONTROL$ via interface 7 (GPIB) to instrument with GPIB address 9 (Wavetek 275).
180 READ @709:READBACK$	Command instrument on interface 7 address 9 to talk. Place received data in alphanumeric variable READBACK$.
190 WRITE @0:READBACK$	Display contents of alphanumeric variable READBACK$ on controller screen.
200 ASK @7:GPIB__REGISTERS	Retrieve the contents of both the bus register and status register from the I/O card of GPIB port 7. Place the results in numeric variable GPIB__REGISTERS.
210 IF BIT(10,GPIB__REGISTERS) THEN GO SUB SERIAL__POLL	Check the value of bit 10 (SRQ line) in numeric variable GPIB__REGISTERS. If the bit value is 1 then perform the subroutine labeled SERIAL__POLL.
220 LOOP	End of loop. Return to DO statement to prompt user for next instrument control codes.
230 SERIAL__POLL: STATUS @709:STATUS__BYTE	Program label indicating start of serial poll subroutine. Perform serial poll of instrument on interface 7 (GPIB) address 9. Place results in numeric variable STATUS__BYTE.

Table 3-7. Sample Demonstration Program 275-3 (Continued)

Program Statements	Explanation
240 IF BIT(0,STATUS_BYTE) THEN WRITE @0:"PROGRAM ERROR"	If bit 0 of numeric variable STATUS_BYTE is equal to 1 then display "PROGRAM ERROR" message on controller screen.
250 IF BIT(1,STATUS_BYTE) THEN WRITE @0:"OUTPUT PROTECTION	If bit 1 of numeric variable STATUS_BYTE is equal to 1 then display "OUTUT PROTECTION" message on controller screen.
260 IF BIT(2,STATUS_BYTE) THEN WRITE @0:"FUSE BLOWN"	If bit 2 of numeric variable STATUS_BYTEis equal to 1 then display "FUSE BLOWN" message on controller screen.
270 IF BIT(3,STATUS_BYTE) THEN WRITE @0:"LOW BATTERY"	If bit 3 of numeric variable STATUS_BYTE is equal to 1 then display "LOW BATTERY" message on controller screen.
280 IF BIT(4,STATUS_BYTE) ' THEN WRITE @0:"EXECUTE COMPLETED"	If bit 4 of numeric variable STATUS_BYTE is equal to 1 then display "EXECUTE COMPLETED" message on controller screen.
290 IF BIT(5,STATUS_BYTE) THEN WRITE @0:"RAMP-TO-START COMPLETED"	If bit 5 of numeric variable STATUS_BYTE is equal to 1 then display "RAMP-TO-START COMPLETED" message on controller screen.
300 IF BIT(7,STATUS_BYTE) THEN WRITE @0:"FRONT PANEL SRQ KEY PRESSED"	If bit 7 of numeric variable STATUS_BYTE is equal to 1 then display "FRONT PANEL SRQ KEY PRESSED" message on controller screen.
310 RETURN	End of serial poll subroutine.
320 END	End of program.

Table 3-8 contains a program to send control commands to the Wavetek 275, read back the instrument response, monitor the SRQ line, perform a serial poll and display the results as a message on the controller screen. This program continuously monitors for a delayed SRQ, such as "RAMP-TO-START COMPLETED".

Table 3-8. Sample Demonstration Program 275-4

Program Statements	Explanation
100 ! PROGRAM 275-4	Comment statement containing program identification.
110 DIM CONTROL$*80	Set length of alphanumeric control variable for maximum expected number of control characters.
120 DIM READBACK$*80	Set length of alphanumeric readback variable for maximum expected number of readback characters.
130 CLEAR	Clear controller screen.

Table 3-8. Sample Demonstration Program 275-4 (Continued)

Program Statements	Explanation
140 WRITE @0:"ENTER ASCII CONTROL CODES."	Prompt user for control codes.
150 INPUT CONTROL$	Stop program while user types instrument control codes into controller, then place control codes into alphanumeric variable CONTROL$.
160 WRITE @709:CONTROL$	Send control codes in alphanumeric variable CONTROL$ via interface 7 (GPIB) to instrument with GPIB address 9 (Wavetek 275).
170 GO SUB CHECK_FOR_SRQ	Perform subroutine labelled CHECK _FOR_SRQ to check for an interrupt.
180 READ @709:READBACK$	Command instrument on interface 7 address 9 to talk. Place received data in alphanumeric variable READBACK$.
190 WRITE @0:READBACK$	Display contents of alphanumeric variable READBACK$ on controller screen.
200 WRITE @0	Display blank line on controller screen.
210 WRITE @0:"PRESS 'STOP' AND 'RUN' KEYS TO ENTER NEW COMMAND."	Display message to prompt operator to stop then restart program to enter new command.
220 WRITE @0	Display blank line on controller screen.
230 DO	Start of endless loop (no UNTIL or WHILE condition is specified) to check for SRQ interrupt.
240 GO SUB CHECK_FOR_SRQ	Perform subroutine labelled CHECK _FOR_SRQ to check for an interrupt.
250 LOOP	End of loop to continuously check for SRQ interrupt.
260 CHECK_FOR_SRQ: ASK @7:GPIB_REGISTERS	Label for subroutine to check SRQ line. Retrieve the contents of both the bus register and status register from the I/O card of GPIB port 7. Place the results in numeric variable GPIB_REGISTERS.
270 IF BIT(10,GPIB_REGISTERS) THEN GO SUB SERIAL_POLL	Check the value of bit 10 (SRQ line) in numeric variable GPIB_REGISTERS. If the bit value is 1 then perform the subroutine labelled SERIAL_POLL.
280 RETURN	End of subroutine to check for SRQ interrupt.
290 SERIAL_POLL:STATUS @709:STATUS_BYTE	Program label indicating start of serial poll subroutine. Perform serial poll of instrument on interface 7 (GPIB) address 9. Place results in numeric variable STATUS_BYTE.

Table 3-8. Sample Demonstration Program 275-4 (Continued)

Program Statements	Explanation
300 IF BIT(0,STATUS_BYTE) THEN WRITE @0:"PROGRAM ERROR"	If bit 0 of numeric variable STATUS_BYTE is equal to 1 then display "PROGRAM ERROR" message on controller screen.
310 IF BIT(1,STATUS_BYTE) THEN WRITE @0:"OUTPUT PROTECTION"	If bit 1 of numeric variable STATUS_BYTE is equal to 1 then display "OUTPUT PROTECTION" message on controller screen.
320 IF BIT(2,STATUS_BYTE) THEN WRITE @0:"FUSE BLOWN"	If bit 2 of numeric variable STATUS_BYTE is equal to 1 then display "FUSE BLOWN" message on controller screen.
330 IF BIT(3,STATUS_BYTE) THEN WRITE @0:"LOW BATTERY"	If bit 3 of numeric variable STATUS_BYTE is equal to 1 then display "LOW BATTERY" message on controller screen.
340 IF BIT(4,STATUS_BYTE) WRITE @0:"EXECUTE COMPLETED"	If bit 4 of numeric variable STATUS_BYTE is equal to 1 then display "EXECUTE COMPLETED" message on controller screen.
350 IF BIT(5,STATUS_BYTE) WRITE @0:"RAMP-TO-START COMPLETED"	If bit 5 of numeric variable STATUS_BYTE is equal to 1 then display "RAMP-TO-START COMPLETED" message on controller screen.
360 IF BIT(7,STATUS_BYTE) THEN WRITE @0:"FRONT PANEL SRQ KEY PRESSED"	If bit 7 of numeric variable STATUS_BYTE is equal to 1 then display "FRONT PANEL SRQ KEY PRESSED" message on controller screen.
370 RETURN	End of serial poll subroutine.
380 END	End of program.

Table 3-9 contains a program that remotely loads the stairstep demonstration waveform that was entered manually in the previous section of the manual. Note that when we previously manually loaded the waveform we allowed the Wavetek 275 to automatically increment the arbitrary waveform address, but that in this program, for the purpose of demonstration, we chose to specify each address.

Table 3-9. Sample Demonstration Program "STAIRS"

Program Statements	Explanation
100 ! PROGRAM "STAIRS"	Comment line containing program identification.
110 CLEAR	Clear controller screen.
120 WRITE @0:"LOADING" WAVEFORM"	Display "LOADING WAVEFORM" on controller screen.

Table 3-9. Sample Demonstration Program "STAIRS" (Continued)

Program Statements	Explanation
130 WRITE @709:"S500E-6 A2.16D0B0C6XB0XH19P1 Y4000K0I'LOADING WAVEFORM' "	Send the following commands to device 09 (Wavetek 275) on interface 7 (GPIB) so that the waveform may be observed as it is loaded: Set clock period to 500 μS. Set amplitude to 2.16V p-p. Set offset to 0V. Set mode to 0 (continuous). Sec function to 6 (arbitrary). Set start address to 0. Set stop address to 19. Set output to 1 (on). Recall stored setting 4000 to set positive arb sync polarity. Set Arb sync address to 0. Execute all previous commands. Display "LOADING WAVEFORM" on instrument front panel display.
140 FOR X=0 TO 19	Start of loop; increment arbitrary waveform address from 0 to 19 by 1.
150 LET Y=100*X	Calculate Arb data at each address.
160 WRITE @709:"K",X,"L",Y	Send address command, address value, data command and data value via interface 7 (GPIB) to instrument with GPIB address 09 (Wavetek 275.)
170 NEXT X	End of loop.
180 WRITE @709:"K0M1I 'WAVEFORM LOADED' "	Reset Arb Sync to address 0 and store all instrument settings in location 1. Display "WAVEFORM LOADED" on instrument front panel display.
190 CLEAR	Clear controller screen.
200 BEEP 2000,100	Generate audible beep from controller.
210 WRITE @0:"WAVEFORM LOADED."	Display "WAVEFORM LOADED" on controller screen.
220 STOP	Stop running program.
230 END	End of program.

Table 3-10 contains a program that remotely loads the "W" demonstration waveform that was entered manually in the previous section of the manual.

Table 3-10.Sample Demonstration Program "W"

Program Statements	Explanation
100 ! PROGRAM "W"	Comment line containing program identification.
110 CLEAR	Clear controller screen.
120 WRITE @0:"LOADING WAVEFORM"	Display "LOADING WAVEFORM" on controller screen.
130 WRITE @709:"B0C6A5 S4.88E-6P1Y4000XB20 XH2047K20I'LOADING WAVEFORM' "	Send the following commands to device 09 (Wavetek 275) on interface 7 (GPIB) so that the waveform may be observed as it is loaded: Set mode to 0 (continuous). Sec function to 6 (arbitrary). Set amplitude to 5V p-p. Set clock period to 4.88 μS. Set output to 1 (on). Recall stored setting 4000 to set positive arb sync polarity. Set start address to 20. Set stop address to 2047. Set arb sync address to 20. Execute all previous commands. Display "LOADING WAVEFORM" on instrument front panel display.
140 WRITE @709:"K20L-2048"	Set Arb address to 20, Arb data to −2048.
150 WRITE @709:"K511 L-2048XK"	Set address to 511, data to −2048, draw straight line between last two data points (20 and 511).
160 WRITE @709:"K512L2047XK"	Address 512, data 2047, auto-line.
170 WRITE @709:"K768 L-2048XK"	Address 768, data −2048, auto-line.
180 WRITE @709: "K1024L1000XK"	Address 1024, data 1000, auto-line.
190 WRITE @709:"K1280 L-2048XK"	Address 1280, data −2048, auto-line.
200 WRITE @709: @709:"K1536L2047XK"	Address 1536, data 2047, auto-line.
210 WRITE @709:"K1537 L-2048XK"	Address 1537, data −2048, auto-line.

Table 3-10. Sample Demonstration Program "W" (Continued)

Program Statements	Explanation
220 WRITE @709:"K2047 L-2048XK"	Address 2047, data −2048, auto-line.
230 WRITE @709:"K20M2I 'WAVEFORM LOADED' "	Reset Arb Sync to address 20 and store all instrument settings in location 2. Display "WAVEFORM LOADED" on instrument front panel display.
240 CLEAR	Clear controller screen.
250 BEEP 2000,100	Generate audible beep from controller.
260 WRITE @0:"WAVEFORM LOADED."	Display "WAVEFORM LOADED" on controller screen.
270 STOP	Stop running program.
280 END	End of program.

Table 3-11 contains a program that remotely loads a damped sine waveform. The program contains the minimum number of statements required for loading the waveform, but does not set the instrument to display the waveform as it is being loaded.

Table 3-11. Sample Demonstration Program "DSIN1"

Program Statements	Explanation
100 PROGRAM "DSIN1"	Comment statement containing program identification.
110 OPTION ANGLE DEGREES	Sets controller for trigonometric functions expressed in degrees (instead of radians).
120 WRITE @709:"K",0	Set arbitrary waveform address to zero.
130 FOR I = 0 TO 2047	Start of loop that increments arbitrary waveform address from 0 to 2047 by 1. Note that this address is not sent to the instrument; the instrument is allowed to increment this address automatically.
140 LET L = 2048*EXP(-I/512))* SIN(2*I)	Calculate damped sine data (amplitude) value from address value.
150 WRITE @709:"L",L	Send data command and data value via interface 7 (GPIB) to instrument address 9 (Wavetek 275.)
160 NEXT I	End of loop.
170 STOP	Stop running program.
180 END	End of program.

Table 3-12 contains a more elaborate program that remotely loads the same damped sine waveform. This program sets up the instrument to display the waveform as it is being loaded, stores the instrument settings, calculates the data values, loads the waveform, displays the waveform loading status on both the controller screen and the instrument display, and displays the time required to load the waveform. (Actual loading time was :56.)

Table 3-12. Sample Demonstration Program "DSIN2"

Program Statements	Explanation
100 PROGRAM "DSIN2"	Comment statement containing program identification.
110 CLEAR	Clear the controller screen.
120 WRITE @0:"LOADING WAVEFORM"	Display "LOADING WAVEFORM" on controller screen.
130 LET T1 = TIME	Read controller timer and place resulting starting time in numeric variable T1.
140 OPTION ANGLE DEGREES	Sets controller for trigonometric functions expressed in degrees (instead of radians).
150 WRITE @709: "K0L0K2047L0XK S4.883E-6A5D0B0C6P1Y4000I 'LOADING WAVEFORM' "	Sends the following commands via interface 7 (GPIB) to instrument address 9 (Wavetek 275). Clear arbitrary waveform memory by drawing straight line at data value 0 between addresses 0 and 2047. Set clock period to 4.883 μS. Set amplitude to 5V p-p. Set offset to 0V. Set set mode to 0 (continuous). Set function to 6 (continuous). Set instrument output to ON (1). Recall setting 4000 to set Arb Sync positive. Execute all previous commands. Display "LOADING WAVEFORM" on instrument front panel display.
160 WRITE @709: "XB0XH2047K0I"	Set START address to zero. Set STOP address to 2047. Set arbitrary waveform address to zero. Execute all previous commands.
170 FOR I = 0 TO 2047	Start of loop that increments arbitrary waveform address from 0 to 2047 by 1. Note that this address is not sent to the instrument; the instrument is allowed to increment this address automatically.
180 LET L = 2048*EXP(−I/512)) *SIN(2*I)	Calculate damped sine data (amplitude) value from address value.
190 WRITE @709:"L",L	Send data command and data value via interface 7 (GPIB) to instrument address 9 (Wavetek 275.)

Table 3-12. Sample Demonstration Program "DSIN2" (Continued)

Program Statements	Explanation
200 NEXT I	End of loop.
210 WRITE @709:"K0M5I 'WAVEFORM LOADED' "	Send the following commands via interface 7 (GPIB) to instrument (GPIB) to instrument address 9 (Wavetek 275): Set Arb Sync address to zero. Store instrument settings in location 5. Execute all previous commands.
220 LET T2 = TIME	Read controller timer and place resulting ending time in numeric variable T2.
230 LET T = T2-T1	Subtract starting time from ending time and place resulting elapsed time (total seconds) in numeric variable T.
240 LET M = INT(T/60)	Calculate elapsed minutes.
250 LET S = T-60*M	Calculate elapsed seconds.
260 BEEP 2000,100	Generate audible beep from controller.
270 CLEAR	Clear controller screen.
280 WRITE @0:"WAVEFORM LOADED."	Display "WAVEFORM LOADED." on controller screen.
290 WRITE @0 USING 300: "LOADING TIME ",M,":",S	Display elapsed time in minutes and seconds using the format in line 300.
300 FORMAT:C,F2,C,FZ2	Format statement for elapsed time display in line 290.
310 STOP	Stop running program.
320 END	End of program.

3.6 THE GENERAL PURPOSE INTERFACE BUS

This section of the manual is provided for readers who wish further background information on the GPIB.

The GPIB interface in the Wavetek 275 is an implementation of the IEEE 488-1978 standard as a computer-to-peripheral and a peripheral-to-peripheral interface. This implementation includes all electrical, mechanical, timing and protocol considerations. It supports the following interface functions:

SH1 Complete source handshake.
AH1 Complete acceptor handshake.
T6 Basic Talker.
TE0 No extender talker.
L4 Basic listener.
SR1 Complete service service request (software select).
RL1 Remote/local and local lockout.
PP0 No parallel poll capability.
DC1 Complete device clear/selective device clear.
DT1 Complete device trigger capability.
E2 Tri-state drivers.

The talk capability allows a device to send data (such as error message readings) out over the bus. The listen capability allows a device to receive data (such as device programming information) from the bus.

3.6.1 GPIB Structure

The General Purpose Interface Bus consists of 16 negative-true signal lines as shown in figure 3-7.

These 16 lines include 8 bi-directional data lines, 3 handshake lines and 5 control lines. All devices on the bus interface to these lines with passive pull-up and active pull-down. Thus, any device may "assert" a line by pulling it down to the logic low, or "true" state. If no device is asserting the line, it is pulled up to the logic high, or "false" state. (Only the controller is allowed to assert certain lines.)

As shown in figure 3-7, devices connected to the bus may be a LISTENER (only), TALKER (only), LISTENER/TALKER or CONTROLLER. More than one controller may be connected to the bus, but only one controller may be hard-wired as SYSTEM CONTROLLER, and only one controller at a time may assume the role of ACTIVE CONTROLLER.

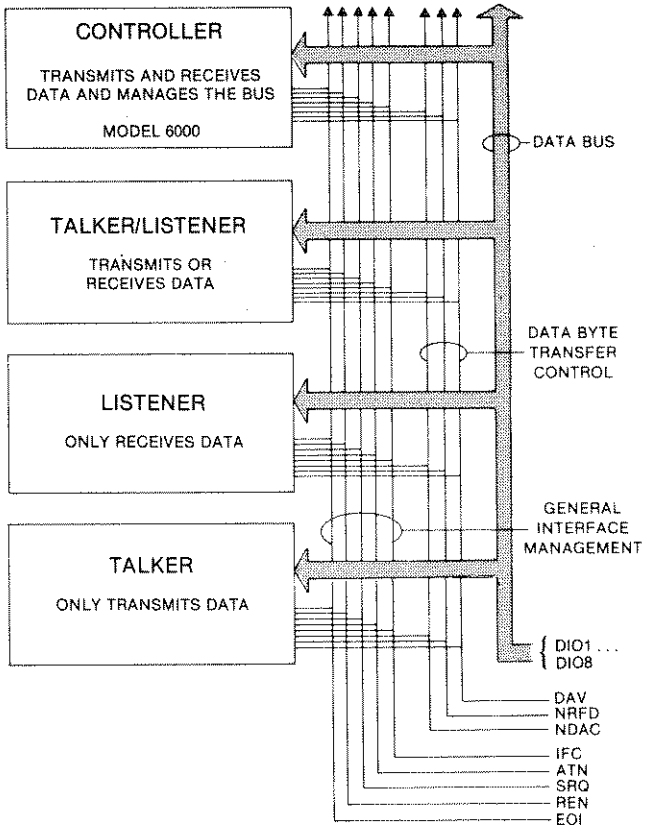


Figure 3-7. GPIB Structure

3.6.2 GPIB Lines

The mnemonics used to identify the GPIB lines are:

DIO1-DIO8	Data In/Out Lines
ATN	Attention
REN	Remote Enable
DAV	Data Available
NRFD	Not Ready For Data
NDAC	Not Data Accepted
EOI	End Or Identify
SRQ	Service Request
IFC	Interface Clear

The functions of the GPIB lines are:

DIO1-DIO8 These eight lines (Data In/Out) are used to send commands from the controller and to transfer data back and forth between instruments and the controller.

ATN The Attention line is operated only by the active controller. It specifies whether the information on lines DIO1-DIO8 is data (ATN false) or a command (ATN true). Whenever ATN is set true, no activity is allowed on the bus except for controller-originated messages.

REN The Remote Enable line controls whether devices on the GPIB are in local or remote modes. In the local mode, devices respond to front panel commands and do not respond to GPIB originated commands. In remote mode, the situation is reversed; GPIB originated commands are obeyed, while front panel commands are ignored. The Wavetek 275 enters the remote state when it receives its listen address and REN is enabled. The Wavetek 275 then stays in the remote mode until the REN line is put in the local state, a Go To Local (GTL) command is received or the LCL front panel key is pressed.

DAV, NRFD, NDAC These are the "handshake" lines (Data Valid, Not Ready For Data and Not Data Accepted) which regulate the transmission of information over the lines DIO1-DIO8. For each command or data byte transferred, a complete handshake cycle occurs. This handshake is designed to hold up the bus until the slowest device has accepted the information. A description of the handshake cycle is given in the next paragraph, after the definition of the GPIB lines.

EOI — When ATN is false, EOI (End Or Identify) indicates that the data on lines DIO1-DIO8 is the last byte of a data message. When the Wavetek 275 receives a data byte with EOI true, it automatically supplies a terminator character following the data byte. When the Wavetek 275 transmits the last byte of a message (which is always a terminator character) it also sets EOI true.

SRQ — The Service Request line is used by the Wavetek 275 and other devices on the bus to signal the controller that they request attention. Since the SRQ line is common to all devices, additional tests must be made to determine which devices are signaling. The controller performs a Serial Poll to accomplish this.

IFC — The Interface Clear line is asserted by the system controller to reset the interface logic in all devices connected to the bus to a known initial state.

3.6.3 Handshake Sequence

The three handshake lines, Data Valid (DAV), Not Ready for Data (NRFD) and Not Data Accepted (NDAC) are used in a typical data exchange as follows:

All devices currently designated as active listeners would indicate (via the NRFD line) when they are ready for data. A device not ready would pull this line low (ground), while a device that is ready would let the line float high. Since a low overrides a passive high, this line will stay low until all active listeners are ready for data. When the talker senses this, it places the next data byte on the data lines and then pulls DAV low. This tells the listeners that the information on the data lines is valid and that they may read it. Each listener (at its own speed) then takes the data and lets the NDAC line go high. Again, only when all listeners have let NDAC go high will the talker sense that all listeners have read the data. It can then remove DAV (let it go high) and start the entire sequence over again for the next byte of data.

3.6.4 GPIB Commands

Commands sent over lines DIO1-DIO8 with ATN true are divided into five classes:

1. Listen Addresses
2. Talk Addresses
3. Secondary Addresses
4. Universal Commands

   DCL Device Clear
   SPE Serial Poll Enable
   SPD Serial Poll Disable
   LLO Local Lockout

5. Addressed Commands

   GTL Go To Local
   SDC Selective Device Clear
   GET Group Execute Trigger

These commands and command groups are shown with their binary codes in Appendix A.

3.6.4.1 Listen Addresses

Listen addresses are used to command a device to read any data bytes transmitted over lines DIO1-DIO8. There are 31 different available addresses (hexadecimal codes 20 through 3E, ASCII codes SP through >). A 32nd address, called unlisten (hexadecimal 3F, ASCII ?) is used to command all devices to not read data bytes. The Wavetek 275 listen address is selected by internal switches (figure 2-2) or by front panel keyboard; e.g., ADRS 1 EXEC for address number one. Either method of selection specifies the lower 5 bits of the address (ref: table 2-2). Pressing the front panel ADRS key displays the GPIB address as a decimal device number. At power-on, the address is always that set by internal switches. Another internal switch (figure 2-2) can lock out address selection by front panel keyboard if desired. Each time ADRS is pressed, XA will appear in the CMD RCL string. The address can not be reprogrammed from the GPIB.

3.6.4.2 Talk Addresses

Talk addresses are used to command a device to transmit data over lines DIO1-DIO8. There are 31 different available addresses (hexadecimal codes 40 through 5E, ASCII codes @ through ^). A 32nd address, called untalk (hexadecimal 5F, ASCII _) is used to command all devices to cease talking. The lower 5 bits of the Wavetek 275 talk address are selected by the same switches used to select the listen address. Thus, if the Wavetek 275 listen address is hexadecimal 21 (ASCII !), the talk address is hexadecimal 41 (ASCII A). Pressing the front panel ADRS key displays the GPIB address as a decimal device number.

NOTE: As shown in section 3.5 of the manual, use this decimal device number for programming both talk

and listen commands. Separate talk and listen addresses are not used in program commands.

3.6.4.3 Secondary Addresses

Secondary address are used following a talk or listen address to provide the ability to address more than the 31 devices provided for by simple talk or listen addresses. Secondary addresses are ignored by the Wavetek 275.

3.6.4.4 Universal Commands

Universal commands are used to command a device to perform designated actions. Universal commands are recognized at all times. Universal commands performed by the Wavetek 275 are:

1. Device Clear (DCL) — Resets the Wavetek 275 to the initial power-on settings. DCL affects all devices on the bus.
2. Serial Poll Enable (SPE) — Causes the instrument to engage in a serial poll by responding with the serial poll status byte when addressed as a talker. Data line DIO7 will be on, if service is being requested on the SRQ line. When the status byte is read, it is reset to an ASCII blank, and the SRQ line is released (of course, it may still be held down by other devices). The status byte is also available by reading the Wavetek 275 talk message number 1. When this message is read, the status byte is reset and the SRQ released as for the serial poll.
3. Serial Poll Disable (SPD) — Discontinues serial poll. Returns instrument to normal talk modes.
4. Local Lockout (LLO) — Causes the Wavetek 275 to enter a state where the front panel LCL key is inoperative. In this state, the keyboard is disabled and the instrument will only accept parameter changes through the GPIB. To enable keyboard control, the GPIB controller must place the REN line in the local state.

3.6.4.5 Addressed Commands

Addressed commands are used to command a device to perform designated actions. Addressed commands are recognized only when the instrument is addressed as a *listener*. Addressed commands performed by the Wavetek 275 are:

1. Go To Local (GTL) — commands the Wavetek 275 to go to the local mode.
2. Selective Device Clear (SDC) — Resets the Wavetek 275 to initial power-on conditions. SDC affects only the selected unit.
3. Group Execute Trigger (GET) — Causes the actions specified by the GET mode (XG) code. If the Wavetek 275 microprocessor is idle (i.e., not processing a previously sent programming string), a GET command will be completed within 2.5 ms of receipt. Otherwise, it will not be done until current programming is processed.

3.6.5 Using the GPIB

This GPIB section of this manual has deliberately been placed after the REMOTE OPERATION section, because in actual practice the GPIB is much easier to use than its description would indicate. Some points to remember when programming a GPIB controller:

1. It is not necessary to use separate listen or talk addresses, or to worry about the ASCII or hexadecimal equivalent of the address. Simply program the decimal device number, which is same number previously programmed into the Wavetek 275 with the internal address switches or the front panel GPIB ADRS key.
2. When using the standard WRITE command, it is not necessary to program the state of the ATN line, etc. The controller performs these "handshake" functions automatically. (Some controllers have an alternate command, such as COMMAND @, that will allow the advanced programmer access to individual commands such as "attention" and "unlisten".)
3. The GPIB mnemonics (DCL, GET, etc.) are *not* necessarily the actual commands used by the controller. For example, on the controller used to write the sample programs in this manual, the command with the GPIB mnemonic GET translates to an actual controller command of TRG @.
4. Controller GPIB commands are not part of the standardized BASIC computer language, and the commands will vary from one make of controller to the next. Refer to the GPIB programming manual for your make of controller.

SECTION 4
CIRCUIT DESCRIPTION

4.1 GENERAL DESCRIPTION

The Wavetek 275 Arbitrary/Function Generator consists of four major sections (figure 4-1): the microprocessor control section located on the microprocessor/power supply board, the operator interface located on the display board, the function generator section located on the function generator board, and the frequency synthesizer, arbitrary waveform generator, burst counter and data registers located on the auxiliary board. Each of these major blocks is described briefly in this general description and then in more detail in following paragraphs.

4.1.1 Microprocessor Control

The microprocessor (figure 4-2) is the clearinghouse for all control operations. Through its software program in Read Only Memory (ROM), the microprocessor accepts commands from the front panel keyboard or the IEEE-488 General Purpose Interface Bus (GPIB), then sends operating parameters to the function generator circuits and auxiliary circuits, stores these parameters in Random Access Memory (RAM), and controls the front panel display.

The microprocessor section contains the analog interface circuitry which decodes and holds status information for the function generator board. A sample-and-hold circuit provides four analog voltages to control the function generator. Power supplies in this section power all the circuits of the instrument.

4.1.2 Operator Interface

The operator interface located on the display board

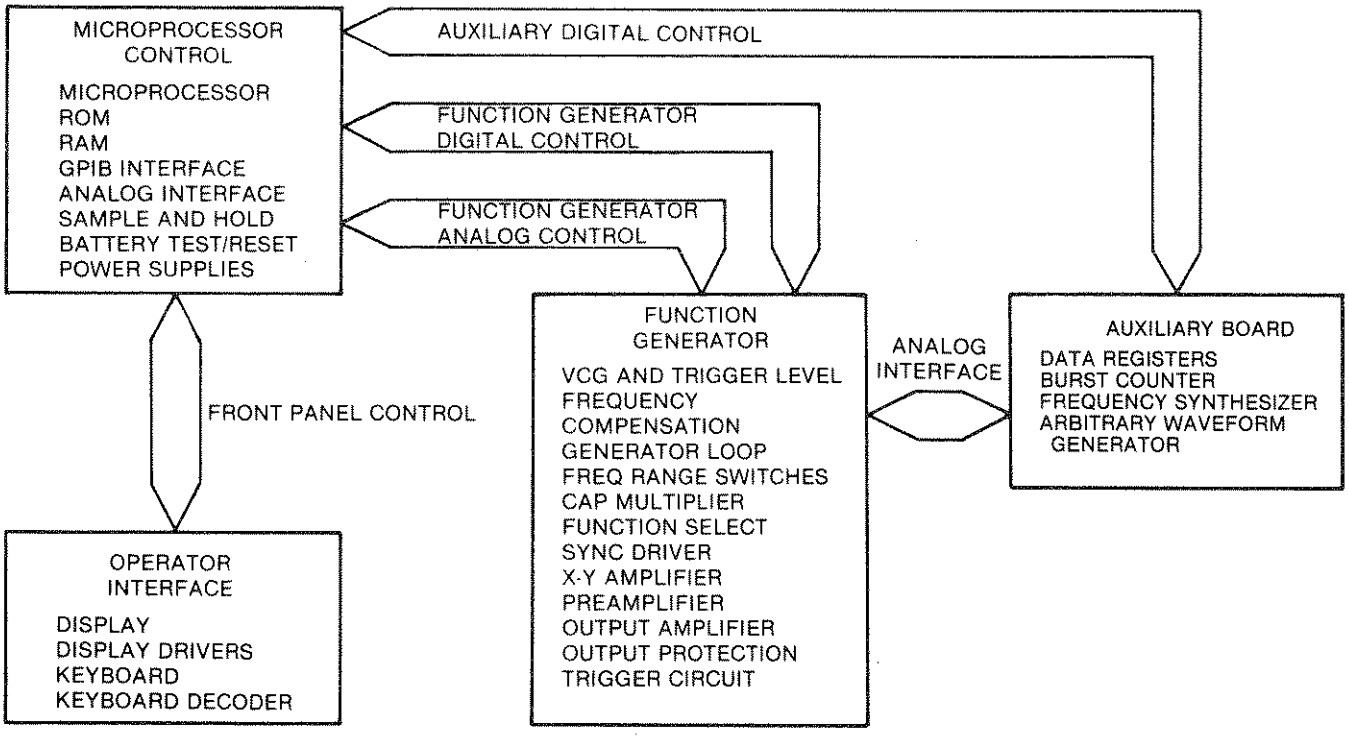


Figure 4-1. Major Blocks

(figure 4-2), includes the front panel keyboard, the fluorescent display, decoders and drivers. The microprocessor recognizes entries from the keyboard and performs the appropriate instruction. Display drivers transfer display information from the microprocessor to the 20 character, vacuum-fluorescent alphanumeric display.

4.1.3 Function Generator

The basic generator loop, figure 4-2, contains a hysterisis switch which creates a triangle waveform by alternately switching equal positive and negative constant currents into a capacitor. The switching points are determined by comparing the triangle peak voltages against two reference levels. A complement of the switching waveform controls the trigger timing in the mode logic, drives the square shaper, and is buffered to provide the instrument's synchronization output (SYNC OUT). Decade values of capacitors determine the basic ranges for frequencies from 100 Hertz up. Below 100 Hertz, a capacitance multiplier scales down the triangle current to provide the four lowest decades of frequency in the instrument.

Within any selected frequency range, a Voltage Controlled Generator (VCG) circuit varies the triangle current proportionally to the frequency control voltage (FRQ) from the microprocessor section. This circuit also controls high frequency compensation by proportionately decreasing the reference levels to compensate for time delays.

The function select circuit chooses a buffered triangle wave, a square wave derived from the hysterisis switch, or a sine wave derived by a sine converter from the triangle wave. (The arbitrary waveform, when selected, is applied directly to the input of the X-Y multiplier, and the function select circuit turns off the square, sine and triangle waveforms.) An X-Y multiplier circuit takes the current output from the function switch and, with its associated preamplifier, varies the waveform amplitude in proportion to the amplitude control voltage (AMP) from the microprocessor.

The output amplifier provides the final gain and output drive capabilities for the waveform, and sums offset from the amplifier into the signal as required. When the output signal peaks are programmed to be less than 1.0 volt, output voltage is attenuated by the decade output attenuator.

If excessive voltage is sensed on the output, the output protection circuit opens all the attenuator relays to protect the instrument. A voltage high enough to arc across the relays will blow a fast-acting fuse to further protect the instrument from major damage.

A trigger input circuit allows the generator to be triggered or gated externally. An internal control voltage (TRL) controlled by the microprocessor determines the level at which an external signal (at TRIG IN) triggers or gates the generator. The external trigger signal can also be gated directly into the square shaper to provide an external width function. Circuitry for internal trigger control is contained on the auxiliary board.

4.1.4 Auxiliary Board

The auxiliary board contains the frequency synthesizer, arbitrary waveform generator, and burst counter circuits.

The frequency synthesizer generates the frequencies used to clock the arbitrary waveform generator when an arbitrary waveform function is selected, or to internally trigger the instrument when internal trigger and a non-arbitrary function are selected.

The arbitrary waveform generator creates a user-defined waveform from data stored in an internal RAM.

The burst counter enables the generator output for a predetermined number of output cycles when the burst mode is selected and the circuit is triggered.

The auxiliary board also contains data registers to latch data from the buffered data bus to control other circuits on the board.

4.2 MICROPROCESSOR CONTROL CIRCUIT DESCRIPTION

The microprocessor control section and its associated circuits (figure 4-3) are located on the Microprocessor/Power Supply circuit board accessible beneath the bottom cover of the instrument. Descriptions in this section include the microprocessor/memory circuits, GPIB interface, battery test and reset circuitry, analog interface, sample and hold circuitry and instrument software.

The following descriptions refer to figure 4-3 and the microprocessor/power supply schematics in the back of this manual.

4.2.1 Microprocessor/Memory

The microprocessor/memory section includes the microprocessor itself, an address latch to demultiplex the lower order address bits, an address decoder to select appropriate memory locations or addressable registers, read only memory (ROM), random access memory (RAM), a data latch to hold data for transfer to analog and display registers, the beeper circuit, and the GPIB address switch and register.

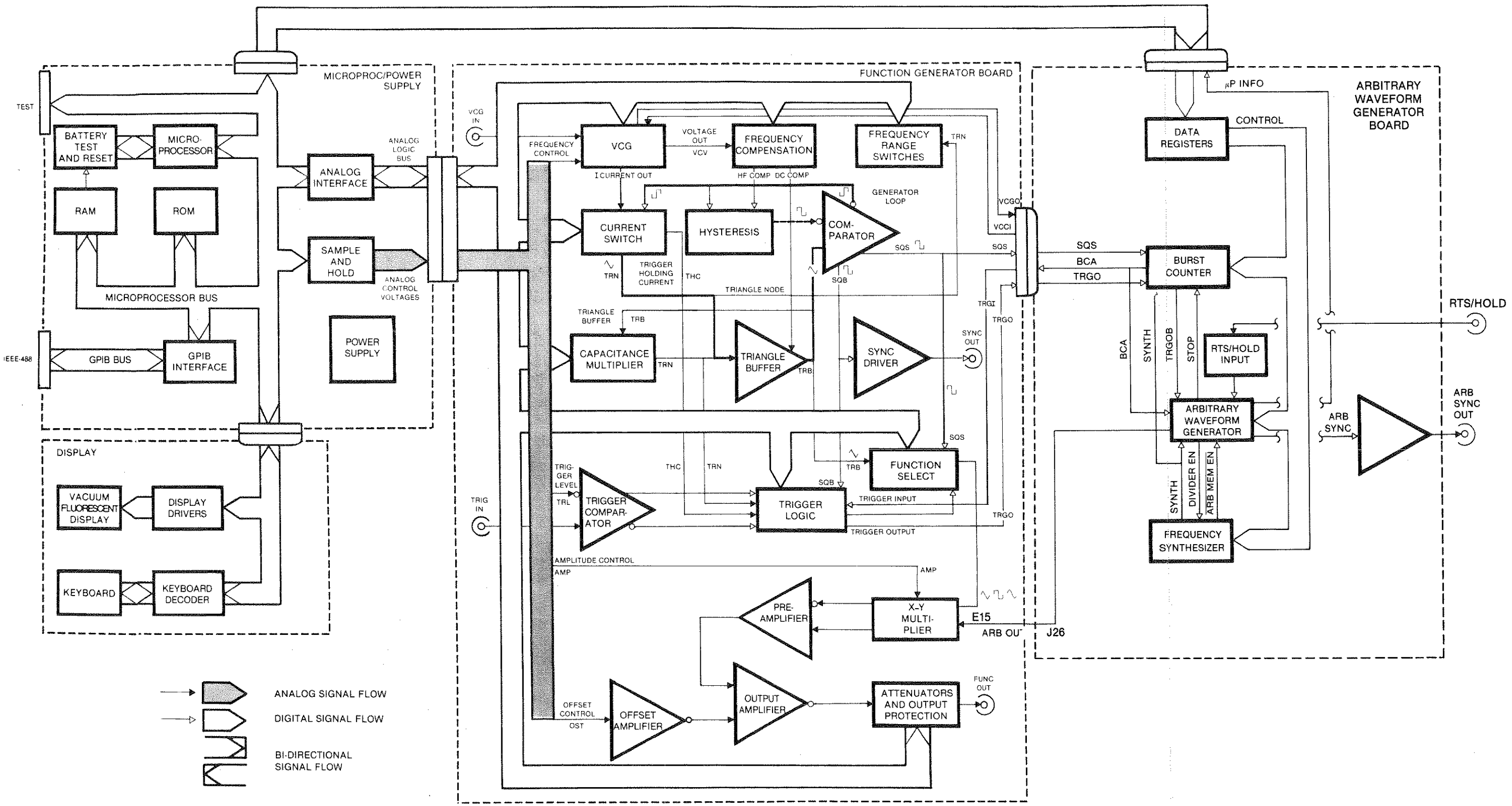


Figure 4-2. Functional Block Diagram

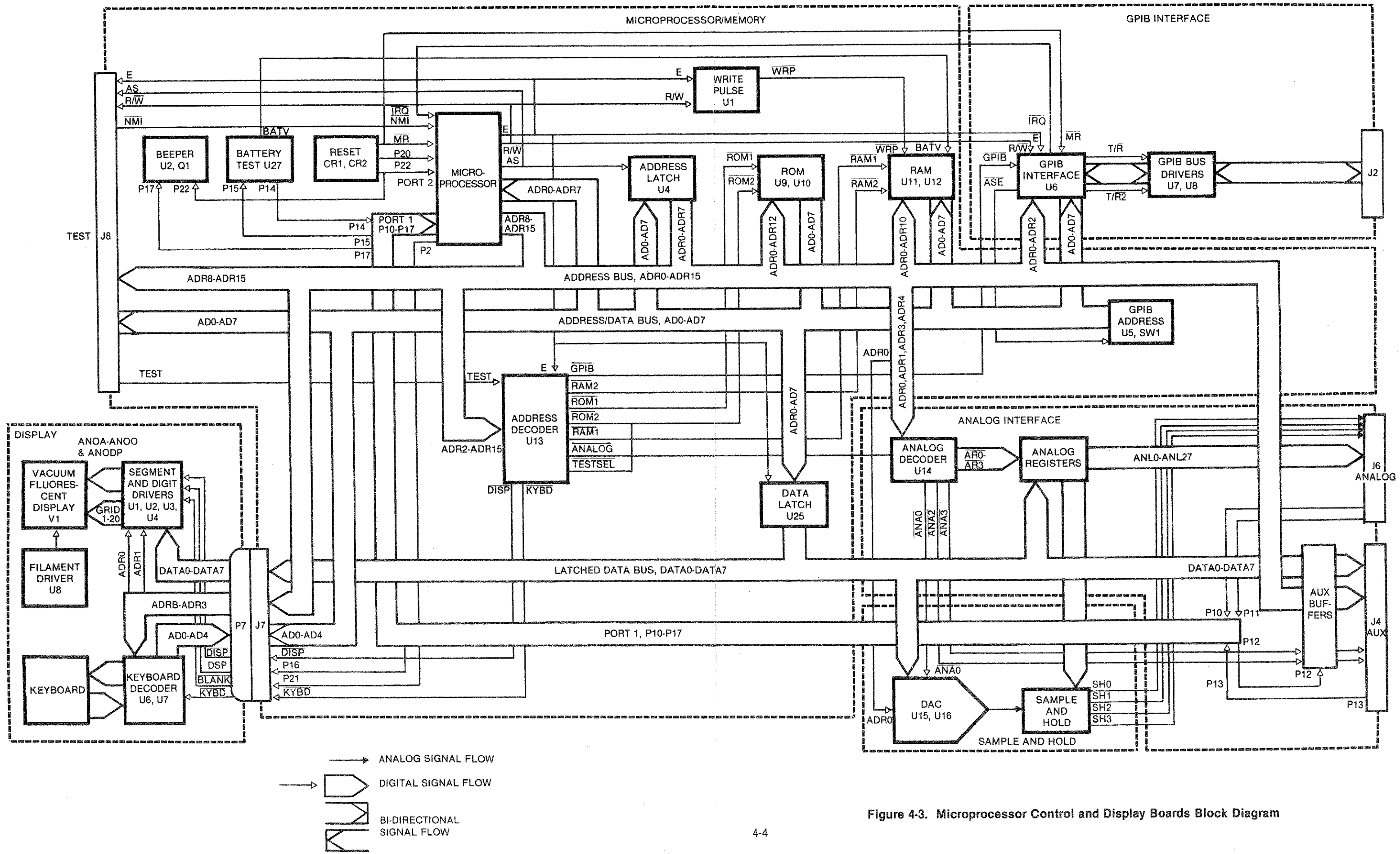


Figure 4-3. Microprocessor Control and Display Boards Block Diagram

4.2.1.1 Microprocessor

The 6803 microprocessor, U3, is in its expanded-multiplexed mode (mode 2), as determined by mode control programming diodes, CR1 and CR2. This mode allows the microprocessor to address external memory by using port 3 (P30-P37) as the multiplexed low-order address/data bus, port 4 (P40-P47) as the high-order address bus, with pins 39 and 38 as the address strobe and read/write line (R/$\overline{W}$) respectively. Ports 1 (P10-P17) and 2 (P20-P24) are always I/O ports.

A clock-generating circuit within the microprocessor uses an external 4 MHz crystal, Y1, between the XTAL 1 and XTAL 2 pins to develop its internal phase clocks and the 1 MHz system enable clock (E). Figure 4-4 shows the approximate timing for major signals and busses in the microprocessor/memory system. Actual system timing varies somewhat from instrument to instrument, so signal spacing may be different within the 1 μs period of the system clock.

The microprocessor responds to three interrupt inputs: master reset ($\overline{RESET}$), which initializes the microprocessor; the external interrupt request line ($\overline{IRQ}$),which the GPIB interface uses to signal the processor; and the non-maskable interrupt ($\overline{NMI}$), which is not used in the instrument, but is available on the test connector.

4.2.1.2 Address Latch

An octal latch, U4, demultiplexes the address/data bus from the microprocessor to hold the low-order addresses (ADR0-ADR7) during the part of the E clock cycle that data occurs on the multiplexed bus. Latching occurs on the negative transition of the AS signal (U3, pin 39). See timing diagram, figure 4-4.

4.2.1.3 Data Latch

Octal latch, U25, demultiplexes data from the address/data bus much the same way as the address latch (U4), except that the falling edge of the E clock, rather than AS, is used to latch the data.

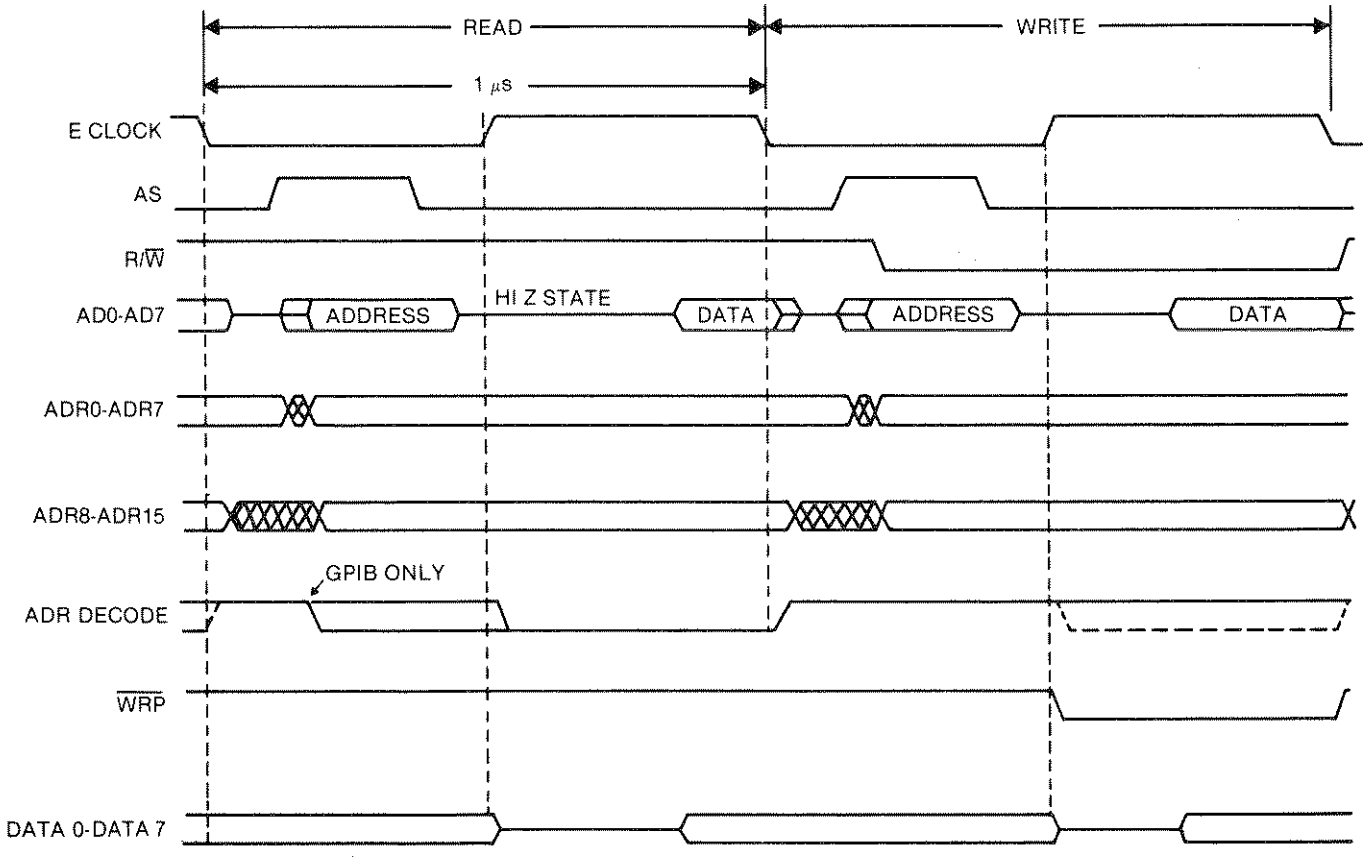


Figure 4-4. Microprocessor Timing Diagram

4.2.1.4 Address Decoder

A field programmable gate array, U13, decodes the upper 14 bits of the 16 address lines to select one of eight possible addressable devices or circuits. These are the keyboard decoder ($\overline{KYBD}$), display drivers ($\overline{DISP}$), IEEE-488 interface ($\overline{GPIB}$), RAM location 1 ($\overline{RAM1}$), RAM location 2 ($\overline{RAM2}$), ROM location 1 ($\overline{ROM1}$), ROM location 2 ($\overline{ROM2}$), and the analog interface registers ($\overline{ANALOG}$). In addition, a ninth output decodes the reset and interrupt vector addresses into ROM2 for normal operation, but allows a test input to direct these vectors into external memory. A memory map, table 4-1, shows the position in memory for each of the above blocks.

4.2.1.5 ROM

Two read-only-memories, U9 (ROM1) and U10 (ROM2), contain the program for the microprocessor. Their respective locations in memory are adjacent as shown in the memory map, table 4-1. $\overline{ROM1}$ and $\overline{ROM2}$ from the address decoder enable the appropriate IC on the rising edge of E clock. A brief description of microprocessor operation will be covered in the software section.

4.2.1.6 RAM

The microprocessor uses two random access memories, U11 and U12, as a scratch pad memory and as memory for stored settings. The $\overline{RAM1}$ or $\overline{RAM2}$ line from the address decoder enables the selected RAM on the rising edge of the E clock. During a write cycle, the write pulse circuit ANDs the read/$\overline{write}$ line from the processor (R/$\overline{W}$) with the E clock to generate a write pulse ($\overline{WRP}$) after all address lines have become stable. A lithium battery (BT1) maintains a sufficient voltage level to prevent the loss of information stored in both RAMs when external power is removed. Schottky diode CR5 conducts when the + 5V supply falls below the battery's voltage (approximately 3V). Diode CR4 prevents the battery from discharging through the rest of the circuit. The battery voltage is also supplied to the auxiliary board to prevent the loss of arbitrary waveforms stored in RAM during power-off.

4.2.1.7 Beeper

The microprocessor generates a 62.5 kHz signal continuously at port 22 (P22) after start-up procedure is complete. To generate an audible beep, the processor sends a positive pulse from port 17 (P17) to the reset line of a 12-bit ripple counter, U2. The counter reset condition enables the 62.5 kHz signal from port 22 to the clock input of the counter. The fifth stage output of the counter drives a transistor switch which in turn drives the beeper at approximately 2 kHz. When the eleventh and twelfth states of the counter both go positive, U1-3 inhibits the 62.5 kHz signal from the processor and stops the beeper. This gives a beep about 50 ms long.

Table 4-1. Memory Map

Addressable Devices	Address (Hexadecimal)
Internal Register	$0000 – $001F
Analog	$0020 – $003F
DISP, GPIB (See Note 1)	$0040 – $005F
KYBD & Not Used (See Note 2)	$0060 – $007F
Internal RAM	$0080 – $009F
Not Used	$0100 – $9FFF
ROM 1	$A000 – $BFFF
ROM 2	$C000 – $DFFF
RAM 1	$E000 – $E7FF
RAM 2	$E800 – $EFFF
Not Used	$F000 – $FFEF
Vector (ROM 2) (See Note 3)	$FFF0 – $FFFF

Notes

1. DISP $40 – $43, GPIB $58 – $5F
2. KYBD $60 – $6F, Not Used $70 – $7F
3. Alternate addresses for last 16 locations in ROM 2.

4.2.1.8 GPIB Address

An 8 section DIP switch (SW1), selects the GPIB address for the instrument. Since IEEE-488 specifications allow only 31 possible addresses for GPIB instruments (binary 0-30), only the first five switches S1-S5 (GA0-GA4), are used to select the actual address. S6 (FPADEN) enables or disables the front panel address entry capability. A momentary closure of S7 resets the elapsed operating time counter in the microprocessor. S8 is not used.

An inverting tri-state buffer, U5, gates the address switch information onto the multiplexed address/data bus when enabled by the address switch enable line (ASE) from the IEEE-488 interface device.

4.2.2 GPIB Interface

The GPIB Interface section of the microprocessor board interfaces with the instrument's microprocessor and handles all the handshake protocol and data transfer over the IEEE-488 General Purpose Interface Bus (GPIB).

Most of the IEEE-488 instrument bus protocol functions are handled by the General Purpose Interface Adapter (GPIA), a single IC, U6. Data and control portions of the bus require high current driving capability and specific line termination which the Bus Drivers, U7 and U8, provide. These two sections of the bus have different requirements depending on whether the instrument is acting as a talker or a listener: the data transceiver, U7A or U7B, always acts as a transmitter during talk modes and a receiver during listen modes, but the control transceiver requires that some lines transmit while others receive in both of these modes. These different requirements are met in the "A" transceivers by using different parts for each function (the 75160A for data and the 75161A for control) or in the "B" transceivers by using an extra control line (pin 11 on the 3447.) The instrument is able to use either type of bus transceiver scheme.

The IEEE-488 Interface IC, U6, does all the handshaking requirements of the 1978 IEEE-488 standard. When the controller on the bus sends either the instrument's talk or listen address or a serial poll, U6 signals the instrument's microprocessor by asserting the interrupt request line, $\overline{IRQ}$ (a low on U6, pin 40). The processor can then interrogate any of the eight registers internal to U6. Data from the IEE-488 bus (listen mode) is accessed by reading from the data registers in U6; data output (talk mode) is written to the same register. The address strobe enable line ($\overline{ASE}$) from the interface IC, U6, controls the select line to U5 that enables the GPIB address switch, SW1.

The microprocessor can read this switch by a read of the address register in U6, which causes U6 to set $\overline{ASE}$ low during the E-clock (data) portion of the microprocessor clock cycle. This address is not necessarily the address used by the interface IC (U6); that address is stored in U6 by writing into the internal address register. The actual address of the instrument can be changed by front panel control, but will return to the address specified by the GPIB address switch during a microprocessor reset cycle (power-up).

During the microprocessor reset cycle (power up), $\overline{MR}$ to U6 pin 19 ($\overline{RESET}$) inhibits all the outputs to the bus drivers and the drivers themselves to prevent false information from being transmitted over the bus. In addition, to prevent a false service request message state (SRQ asserted), port 20 from the microprocessor scans the SRQ line at U6, pin 23 to keep a program monitor of the status of the SRQ flag out of U6. A false state could otherwise occur if a very fast controller addressed the instrument in quick succession before the instrument's microprocessor had time to reset SRQ.

For a complete definition of the GPIB lines, refer to paragraph 3.6 in the OPERATION section of the manual.

4.2.3 Battery Test and Reset

One-half of dual operational amplifier U27 acts as a voltage comparator to detect low voltage on the battery, BT1. When the microprocessor goes through its power up procedure and every six minutes thereafter, the processor strobes port 15 (P15) to a low state to simulate the battery's normal load when power is shut off, then checks the output of the comparator at port 14 (P14). If the battery voltage drops below +2.4V, the comparator goes high and the processor sets an internal flag. At power up, this flag causes an immediate display warning for low battery; after power up, a reset command, storing a stored setting or recalling a stored setting causes the warning display or an SRQ, depending on whether the command originates from the keyboard or the GPIB bus.

The second half of U27, acting as a comparator, serves as a microprocessor reset circuit. During power up, diode CR19 is reverse biased, allowing the positive input to U27 (pin 5) to rise to the voltage determined by R59 and R60 (approximately +4.7V). With CR18 forward biased, the negative input to the comparator (U27, pin 6) rises more slowly, at the time constant determined by R57 and C72 (about 100 ms.) Since it takes about two time constants for the

negative input to charge as high as the positive input, about 200 ms elapse before transistor Q2 is turned off and the $\overline{\text{RESET}}$ line to the microprocessor is allowed to rise. When power to the instrument is shut off and the +5V line begins to drop, diode CR18 is reverse biased and the negative input to the comparator falls at the same rate as the +5V line. Diode CR19 is forward biased, so the voltage at the positive input falls more slowly. When the +5V line falls slightly below +4.75V, the comparator turns on Q2 and keeps the microprocessor reset as the power continues to fall.

4.2.4 Analog Interface

The analog interface consists of an analog decoder that decodes addresses in the analog section of memory, analog registers that hold digital information for the function generator board, and auxiliary buffers that route data to the auxiliary board.

4.2.4.1 Analog Decoder

When the microprocessor selects the analog section of memory ($\overline{\text{ANALOG}}$ goes low), a 2 to 4 line decoder (U14A) decodes the 32 bytes of memory from ADR3 and ADR4 into four, 8-byte blocks ($\overline{\text{ANA0}}$-$\overline{\text{ANA3}}$). $\overline{\text{ANA0}}$ selects the digital-to-analog converter, U15. $\overline{\text{ANA1}}$ is decoded further from ADR0 and ADR1 by U14B to select the analog registers ($\overline{\text{AR0}}$-$\overline{\text{AR3}}$). $\overline{\text{ANA2}}$ and $\overline{\text{ANA3}}$ select registers on the auxiliary board.

4.2.4.2 Analog Registers

The analog registers hold the analog control logic for the function generator board, ANL0-ANL27, and the four sample-and-hold select lines. Latched data (DATA0-DATA7) is strobed into registers U21 through U24 by the falling edge of the analog register control lines, $\overline{\text{AR0}}$ through $\overline{\text{AR3}}$ respectively. ANL0 through ANL27 appear at the analog connector, J6.

4.2.4.3 Auxiliary Buffers

The tri-state auxiliary buffers, U28 and U29, prevent the latched data lines from injecting noise through the auxiliary connector (J4) to the auxiliary board by inhibiting the buffers except when the auxiliary board registers are being addressed. One-half of U28 (input pins 2,4,6,8) is continuously enabled, but the signals at its inputs do not change until the microprocessor selects the auxiliary registers. At this time, the buffered port 12 (P12) enables the buffered data (BDATA0-BDATA7) and buffered address (BADR0-BADR2) lines.

4.2.5 Sample and Hold

The sample-and-hold section consists of the DAC (digital-to-analog converter), U15, the −10.24V reference for the DAC, and four sample-and-hold circuits that demultiplex the DAC output to provide four separate analog control voltages for the function generator board.

4.2.5.1 DAC

The 10-bit digital-to-analog converter, U15, contains its own internal registers for latching data and interfaces directly to the latched data bus (DATA0-DATA7). When the microprocessor transfers data into the DAC with ADR0 high (approximately every millisecond), the negative transition of ANA0 latches the most significant 8 bits from the data lines into the DAC's internal register. A second transition of $\overline{\text{ANA0}}$ with ADR0 low latches the least significant bits. The current output of the DAC (U15 pin 12) is converted to a voltage output by operational amplifier U16A at pin 1 using a feedback internal to the DAC at U15 pin 14.

4.2.5.2 −10.24V Reference

Since the DAC circuit provides an inverted programmable portion of the reference voltage, the reference must be negative to get a positive output. This adjustable negative voltage is generated by operational amplifier U16B in an inverting configuration with a gain of less than −1 and using the highly regulated +15V power supply as its input. R16 adjusts the voltage for precisely −10.24V corresponding to a 10 mV step for each binary step of the DAC.

4.2.5.3 Sample and Hold

The microprocessor sequences the DAC through four discrete voltages at about 1 ms each (4 ms for a complete cycle). The four sample-and-hold circuits latch each of these analog voltages in turn to provide the four separate analog control voltages to the function generator board, SH0 through SH3, appearing at J6. In the following paragraph, component designations refer to the first sample and hold section that generates SH0 (corresponding to frequency control, FRQ, on the function generator board). The other sample and hold circuits act similarly.

Within a few microseconds after the appropriate voltage appears at the output of the DAC circuit, the sample-and-hold control line from U24 pin 12 turns on the analog switch U17A and the DAC output charges the holding capacitor C28. Since the analog switch, U17A, transmits a small charge from its logic input (pin 1) to the analog output (pin 3), an inverter, U18F, generates an opposing signal and the capacitor, C27, injects the opposite charge to cancel the effect.

Because these charges do not exactly coincide in time, the result is a high-frequency bipolar spike that must be eliminated. A two-stage filter consisting of R18, C29, R19 and C30 accomplishes this. The holding capacitor C28 continues to charge until the next sequence is due. The control signal from U24 pin 12 turns analog switch U17A off before loading the following circuit's DAC information at U17D. The analog switch's high output impedance in the "off" state and the high input impedance of the buffer at U19B maintain the voltage on the output of the circuit with negligible discharge until the next cycle selects this sample-and-hold circuit again.

4.2.6 Power Supply

Four power supply voltages, +15V, −15V, +5V and +45V (figure 4-5) are generated on the microprocessor/power supply circuit board. The pass elements for each of the supplies are three-terminal regulators (VR1, VR2, VR3 and VR4) which normally operate with a 1.25V difference between their output and reference terminals. The +5V and +45V supplies use very little additional circuitry. In these simpler supplies, the reference voltages are provided by a resistor divider.

4.2.6.1 +5V Supply

In the +5V supply (Microprocessor/Power Supply Schematic, sheet 3), ac from the transformer, T1 (located on the rear panel), is rectified by CR13 and filtered by C56 and C57 to provide unregulated dc for the regulator, VR3. Resistive divider R49 and R50 sets the voltage at the reference input, pin 3, to provide an output of +5V ±5% at E2, while C58 and C59 provide additional filtering at the output of the regulator. R53 loads the supply to guarantee operation of the regulator if the +5V test jumper is removed. CR14 prevents C59 from discharging back through the regulator when power to the instrument is turned off.

4.2.6.2 +45V Supply

The +45V supply operates much the same as the +5V supply except that the unregulated dc at VR4 pin 1 and the regulated output voltage (at pin 2) are much higher. The divider, R52 and R51, sets the output slightly below +45V so the 5% tolerance of the regulator cannot give an output greater than +45V.

4.2.6.3 ±15V Supplies

The + and −15V supplies that power the analog sections of the instrument require greater accuracy and

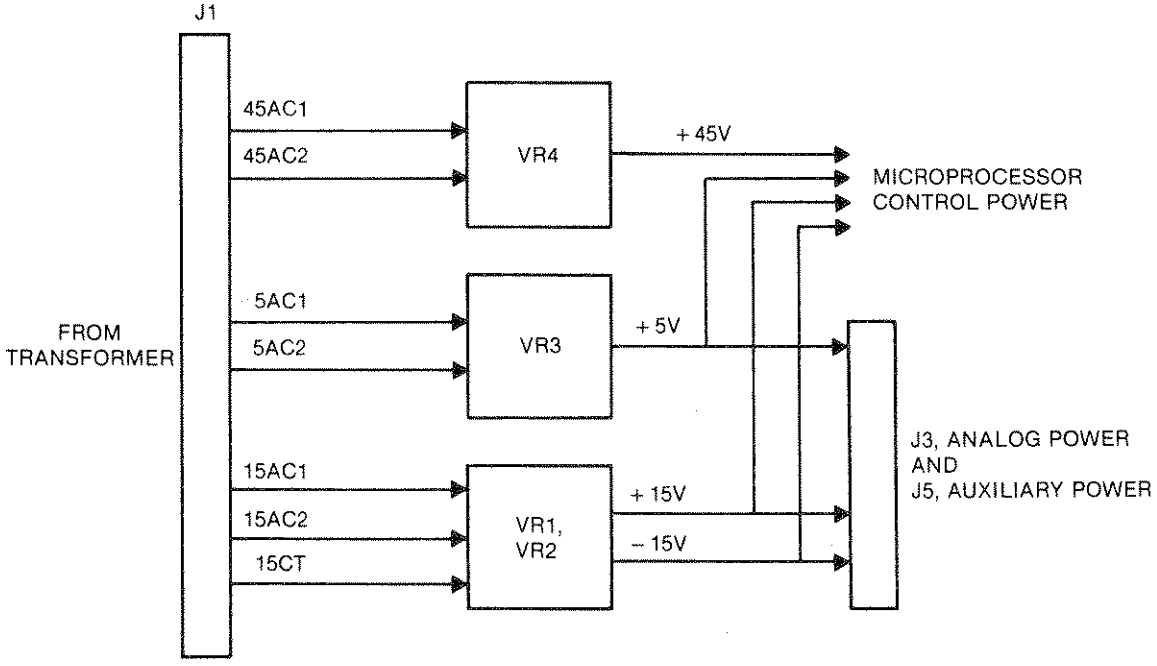


Figure 4-5. Power Supply

stability than the basic regulator provides, so some additional circuitry is necessary. In the +15V supply, the operational amplifier, one-half of U26, compares a portion of the output voltage with a stable zener reference diode, CR10. The op-amp's inverted output drives the reference input of the regulator to compensate for any error in the output. Since the op-amp output cannot operate within 1.25V of its positive supply voltage, a divider, consisting of R35 and R36, allows the output to operate near ground potential. R33, which is in series with the output of the regulator, causes current regulation to take place at a lower value than the internal limiting that the regulator provides. As the current through R33 reaches its limiting value, the voltage drop across R33 reaches 1.25V, the normal voltage difference between the regulator output and reference pins. Any further current through R33 now creates a greater than 1.25V drop that the regulator senses at VR1 pin 3 as an overvoltage and responds by decreasing its output voltage until the current falls back to the limiting value. Diode CR9, in series with the op-amp output (U26 pin 1) prevents the op-amp from sourcing any extra current through R35 that would change the output current limit. A small current through R34 keeps the op-amp in its operating range up to the current limit. C69 and C70 speed up the external regulation to match the internal regulator. R39 allows the output to be adjusted to precisely +15V.

The −15V supply operates similarly to the +15V supply, but the polarities are reversed and the op-amp tracks the +15V supply rather than using another zener as a reference. R47 adjusts the −15V supply.

4.2.7 Microprocessor Software

Although a detailed description of software is beyond the scope of this manual, some discussion of the microprocessor operation is helpful in understanding how the instrument functions.

Figure 4-6 shows the three main program loops for microprocessor operation: a fast background loop, a slow background loop, and the parser-procedure loop. The background loops only check registers for interrupt flags set by external or timer interrupts. The parser selects and calls procedures when the program enters it, and returns control to the fast background loop when a procedure is finished.

4.2.7.1 Fast Background

The fast background loop inspects the three internal registers (GPIB, keyboard and timer) for interrupt flags (non-zero states) and then returns to its beginning. If no interrupt flags are set, the entire loop takes only about 50 to 60 μs. If a flag is set, the loop time increases by the length of the interrupt procedure. If either of the first two register flags (GPIB or keyboard) are set, the background program calls the parser. When the parser completes an operation, it returns the program to the beginning of the fast background loop. If the timer register flag is set, the program enters the slow background loop.

4.2.7.2 Slow Background

The timer flag in the fast background loop looks for an overflow in the 2^{16} bit (which occurs about every 66 ms) of the timer counter (part of the microprocessor IC). The slow background loop then examines a series of other registers: GPIB address change, output protection flag, elapsed time (with its associated battery test timer), a status display timer, and an auxiliary board status flag.

Address Change. The GPIB address change actually compares two sets of two registers: it compares the stored keyboard-entry address, (if enabled) with the register in the GPIB interface and if they are different, enters the new value in the interface; it also compares the previously stored value of the internal address switch with the current setting of the switch, and if they are different, enters the new switch setting in the switch storage location, the GPIB interface, and the front panel register. In addition, if the keyboard entry is disabled, it inhibits the first comparison. The elapsed time counter is reset at this time if the reset section of the switch, SW1 (ETR) changes.

Output Protection Flag. The output protection flag initiates a short routine, when set, that displays the front panel output protection error message, sets SRQ in the GPIB interface, initiates an extended warning beep by repeating 32 beep activations spaced by a timer, and opens up all the output relays on the function generator board.

Elapsed Time Flag. The elapsed time flag is set at 6 minute intervals by the timer. It updates the elapsed time counter (adds 0.1 hr) and initiates the battery test timer. The battery test routine loads the battery for about 120 ms then checks the battery test circuit for low battery voltage. If the battery is low, the routine sets a flag that causes a store, recall, or reset command to display a low battery warning, give a double beep and set SRQ.

Status Display Timer. The status display timer works only when the instrument is set to display status. At intervals of about 1.17s, the timer flag is set and the next background pass causes the equivalent of a cursor command to the instrument, advancing the status display.

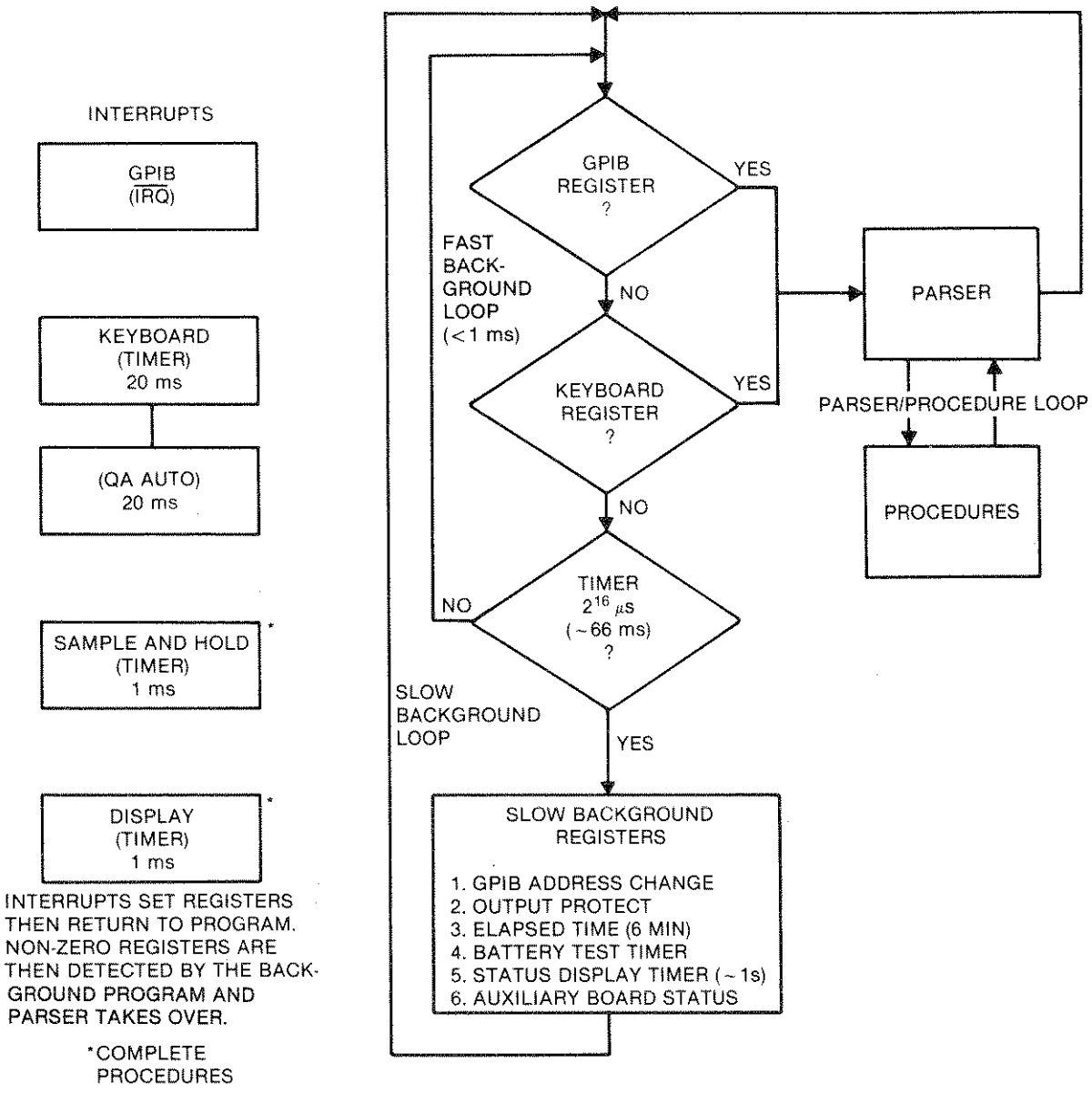


Figure 4-6. Program Loops

Auxiliary Board Status. In the Wavetek 275, the auxiliary board status line is used to read back serial data or monitor one of the three status lines. The data source is selected by U25 on the auxiliary board in response to commands from the microprocessor via the buffered data bus.

4.2.7.3 Parser/Procedure

The parser handles all programming chores except short housekeeping routines. When the parser is called, it examines a series of registers and decides which routines are required, then calls the required procedure which, when complete, returns control to the parser. When the parser has scanned all the condition registers, it returns control to the fast background. Even if their functions appear simple, the parser and the procedures with their interpretive functions make up the bulk of the program.

4.2.7.4 Interrupts

There are only two ways the processor program can be interrupted: through $\overline{IRQ}$ (generated by the GPIB

interface) or through an internal timer (used for all other interrupt requirements).

GPIB Interrupts. GPIB interrupts are initiated by the GPIB responding to GPIB bus commands. When the interrupt occurs, a byte is read from the GPIB interface and stored in a register. The program then returns to its pre-interrupt position. It is the fast background program that actually inspects the register and passes control to the parser, which in turn decides what routines are called to process the information.

Timer Interrupts. Certain subroutines are run during initial power-up and periodically during the time the instrument is on. These subroutines are initiated when the number in the clock register (within the microprocessor) matches the preset number in any of the interrupt registers (within the microprocessor). Upon completion of the subroutine, the preset number corresponding to the elapsed time required between successive interrupts for the function is again added to that interrupt register. The clock timer continues to increment its own register, and when the number in this register again matches the interrupt register, the subroutine is initiated. These interrupt registers work independently of each other and may set another register (as in the keyboard interrupt) or they may initiate an entire subroutine.

4.3 OPERATOR INTERFACE CIRCUIT DESCRIPTION

The operator interface section is located on the display circuit board, which is mounted behind the front panel. Included are the display circuits (consisting of the segment drivers, digit drivers, the filament driver, and the display), and the keyboard circuits (consisting of the keyboard decoder and the keyboard).

Refer to the display schematic in the back of this manual for circuits described in the following paragraphs.

4.3.1 Display

The display circuit consists of vacuum fluorescent display, V1, filament driver, U8, segment drivers, U1 and U2, and digit drivers, U3 and U4. The display is strobed on, one digit at a time, by the microprocessor.

The microprocessor controls the display multiplexing. A 1 ms timer interrupt initiates a display scan routine that advances one digit at a time on the display and enters the appropriate decoded drive information. After the twentieth digit (20 ms), the microprocessor resets an internal counter, and the digit scan repeats.

Figure 4-7 shows the digit timing sequence for the display. The interrupt timer in the processor sets $\overline{\text{BLANK}}$ (Port 21) low. Inverted by U5E, this signal disables all display drivers (which blanks the display) and advances the shift register in the digit drivers, U3 and U4. After about 200 μs, $\overline{\text{BLANK}}$ returns to its high state and the appropriate digit is enabled (GRID1-GRID20). When the processor's scan counter reaches 20, it sets the digit scan position line.

During the time $\overline{\text{BLANK}}$ is low, the processor recalls the digit information already decoded for the 16 segment display and stores this data in latches within segment drivers U1 and U2. The display segment timing is shown in figure 4-8. About 120 μs after the falling edge of the $\overline{\text{BLANK}}$, the processor loads the two-byte segment data into the segment driver registers. $\overline{\text{DISP}}$ from the address decoder strobes the buffered data (DATA0-DATA7) into U1 (lower order byte) or U2 (upper order byte) determined by ADR0 and ADR1. The rising edge of $\overline{\text{BLANK}}$ then enables the output lines (ANOA-ANOO and ANODP) to drive the segment anodes of the display.

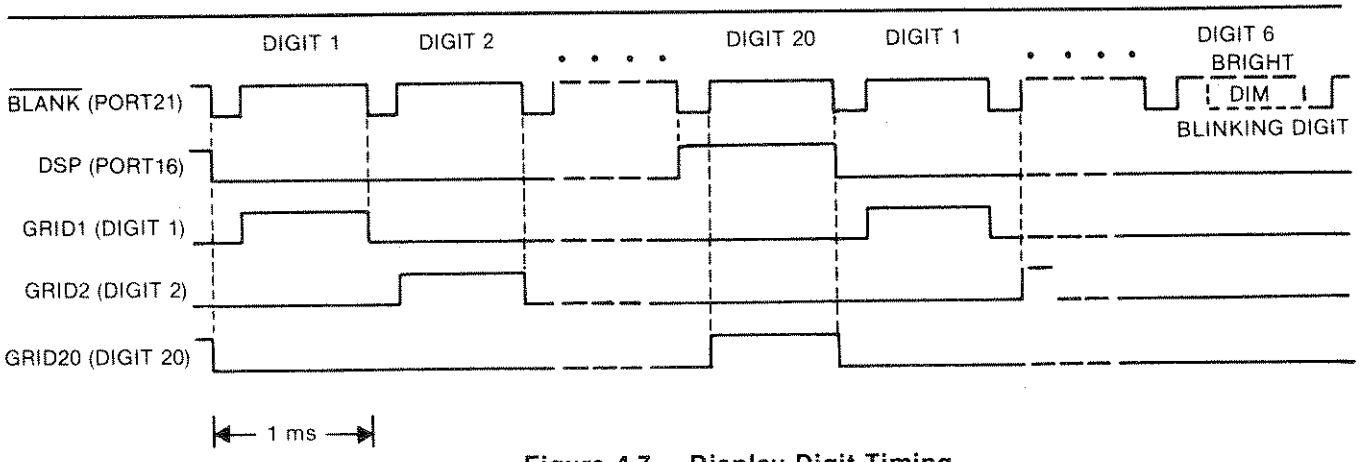


Figure 4-7. Display Digit Timing

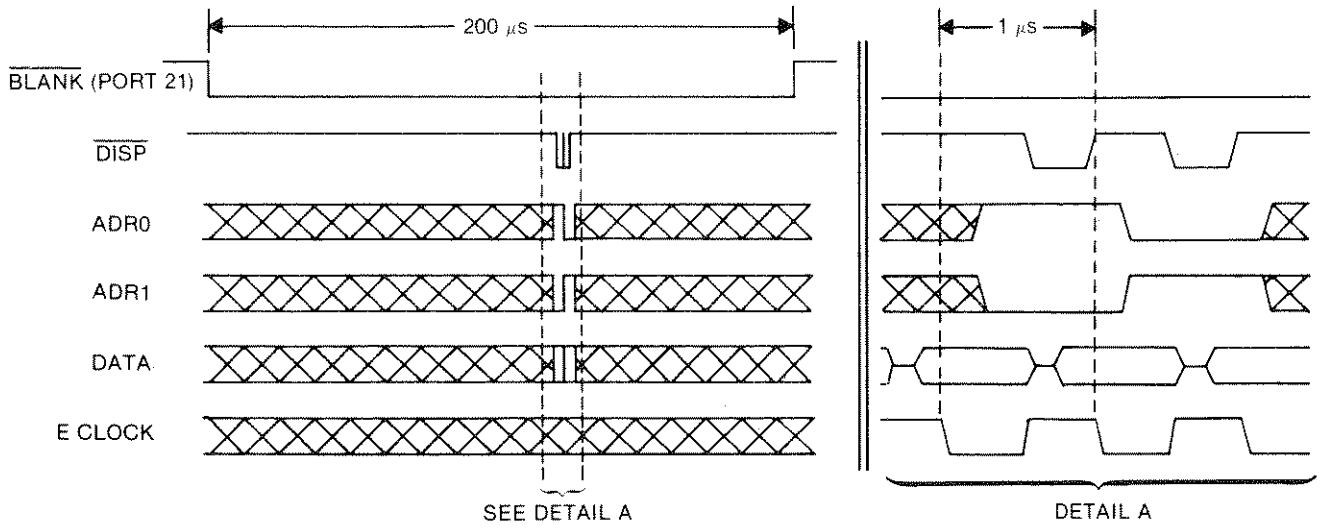


Figure 4-8. Display Segment Timing

In the vacuum fluorescent display, all segment lines are common and individual grids enable each digit. Display filament power is provided by the driver circuit which is an IC timer, U8, configured as a 50 kHz oscillator with a 40% duty cycle. Since the output at U8 pin 3 swings from 0 to +15V, the average dc level is about +6V. This allows the grid lines to pull 6V negative with respect to the filament, which also serves as the cathode. Capacitor C14 acts as an ac ground to maintain a constant dc level across the entire length of the filament.

4.3.2 Keyboard

The keyboard section of the operator interface consists of the keyboard itself, (a 45 switch array mounted just behind the front panel overlay), and the keyboard decoder, U6 and U7, mounted on the display board.

The keyboard is an X-Y matrix of switches. Scanning pulses are applied to the columns of the matrix by U7, and key closures are detected at the matrix rows by U6.

Every 20 ms, the processor scans the keyboard decoder as a series of memory locations. A 4-to-10 line decoder, U7, decodes the four low-order latched address bits (ADR0-ADR3) to the 9-line side of the 9 by 5 switch array. If the operator presses a key on the front panel, the closed contact allows the appropriate decoded address line from the inverting output of the 4-to-10 line decoder (U7) to pull down 1 of 5 pull-up resistors in R3. During the data valid part of the E-clock cycle of the processor, $\overline{\text{KYBD}}$ from the address decoder enables the tri-state buffer, U6, and the processor reads a low at 1 of 5 bits on the address/data bus. The processor can then call the appropriate routine for the key pressed. If the keyboard scan finds no key pressed, the processor returns to its normal routines.

4.4 FUNCTION GENERATOR CIRCUIT DESCRIPTION

The function generator circuit board is accessible beneath the top cover of the instrument below the swing-up auxiliary board. This section includes the VCG and trigger level circuits, the basic generator loop, frequency range switches, capacitance multiplier, frequency compensation circuits, sync output driver, trigger circuit with mode logic, function select circuit including the sine converter and square logic, X-Y multiplier, preamplifier, offset amplifier, output amplifier and output protection circuits.

Refer to the function generator schematic in the back of this manual for circuits described in the following paragraphs.

4.4.1 VCG and Trigger Level

The VCG circuit converts a 0 to +10V control voltage from either the microprocessor board or the external VCG input to positive and negative currents that control the frequency of the generator loop. The input stage acts as a summing amplifier. The control voltage from the processor board, FRQ (normally between +1 and +10V), develops a current through R4 and R5 into the summing node, pin 2 of U2A. R4 and R5, with C1, also act as a filter for the FRQ line to reduce the microprocessor switching noise. The first

stage has a gain of approximately −0.4, so its output at U2A pin 1 ranges typically 0.4V to −4.0V. When the external VCG input is used, FRQ is normally set to 0V by programming FREQ 0, EXEC from the front panel, and the voltage from the external VCG input across R6 now determines the first stage output. CR1 and CR2 prevent excessive voltage at VCG IN from damaging the VCG amplifier. For frequencies between 10 MHz and 12 MHz, an overrange control, $\overline{OVR}$, adds a fixed 0.2 mA through R1 and R2 to increase the maximum voltage out of the first stage (or current out of the entire VCG circuit). The 10 kHz to 99.9 kHz range control, $\overline{FR5}$, increases the current from FRQ by paralleling R3 across the series combination of R4 and R5. This increase compensates for the larger relative capacitance on this range due to the minimum triangle node capacitance (C43 and C44) added to the smallest fixed range capacitor (C50). A gain adjustment (R8) in the first stage is used to control the top-of-range frequency. R11 controls the first stage offset to zero the low end of the external VCG input.

With the VCG jumper in its normal operating position (E9 to E10), the first stage output becomes the VCV (Voltage Control Voltage) output to the variable current sources and the high-frequency compensation circuit. The E10 to E11 connection, which allows the auxiliary board to modify the frequency control voltage, is not used in the Wavetek 275. A simplified schematic of the VCG amplifier is shown in figure 4-9.

The current sources operate on the following principles:

1. The collector current of a transistor depends on its base current and its current gain, and is relatively independent of collector load resistance.
2. The base drive of a transistor can be adjusted to provide a known reference current in a known resistance in its collector circuit.
3. This same base drive, applied to a second matched transistor, will cause the second transistor to have the same collector current as the first transistor.

The negative current source is shown in the figure 4-10 simplified schematic diagram. The Voltage Control Voltage (VCV) is inverted by operational amplifier U2C, and drives transistor U3A to whatever value collector current is required to cause the U3A collector voltage to be equal to VCV. (At this point, both inputs of operational amplifier U2C are at the same voltage, and equilibrium is established.) Since the upper end of collector resistor R22D is held at ground potential (as will be explained later) and the voltage at the lower end is equal to VCV, the current through the resistor ($-I_{ref}$) is proportional to VCV. The same base drive is applied to U3B to generate the negative current source (−I), and is also applied to transistors U3C and Q1 to generate the Trigger Holding Current (THC).

The positive current source (shown in simplified schematic figure 4-11) operates in a similar manner, and tracks the negative current source. Operational amplifier U2D drives transistor U3E to whatever value collector current is required to maintain a "virtual ground" at the junction of R22C and R22D. Since these two resistors are in series, their currents are equal ($+I_{ref} = -I_{ref}$). The U3E base drive is then applied to matched transistor U3D to generate the positive current source (+I) for the generator loop.

The current source circuit also generates a Trigger Holding Current (THC) which is used to clamp the

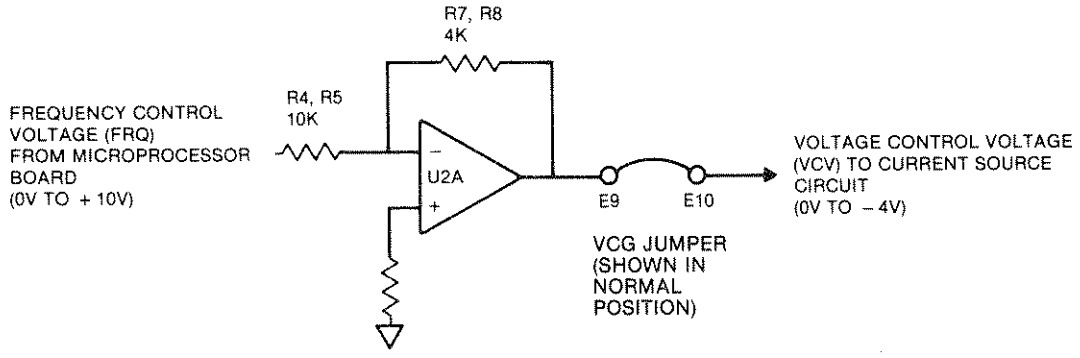


Figure 4-9. Simplified Schematic Diagram, VCG Amplifier

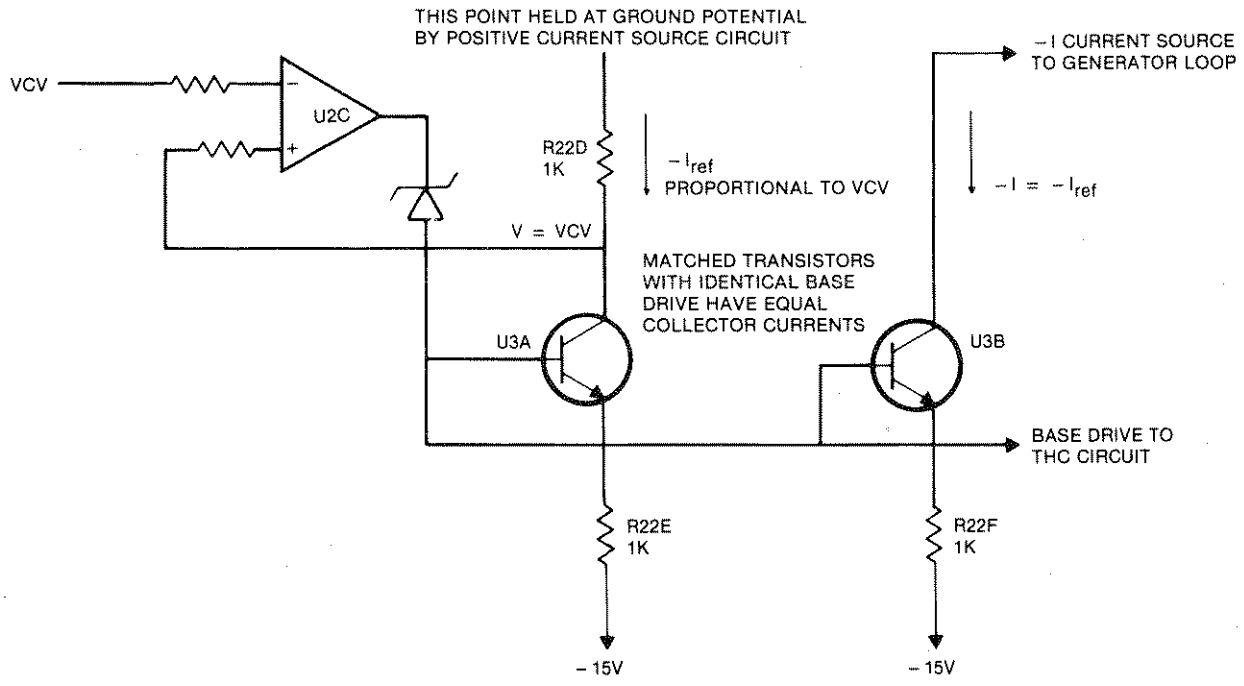


Figure 4-10. Simplified Schematic Diagram, Negative Current Source

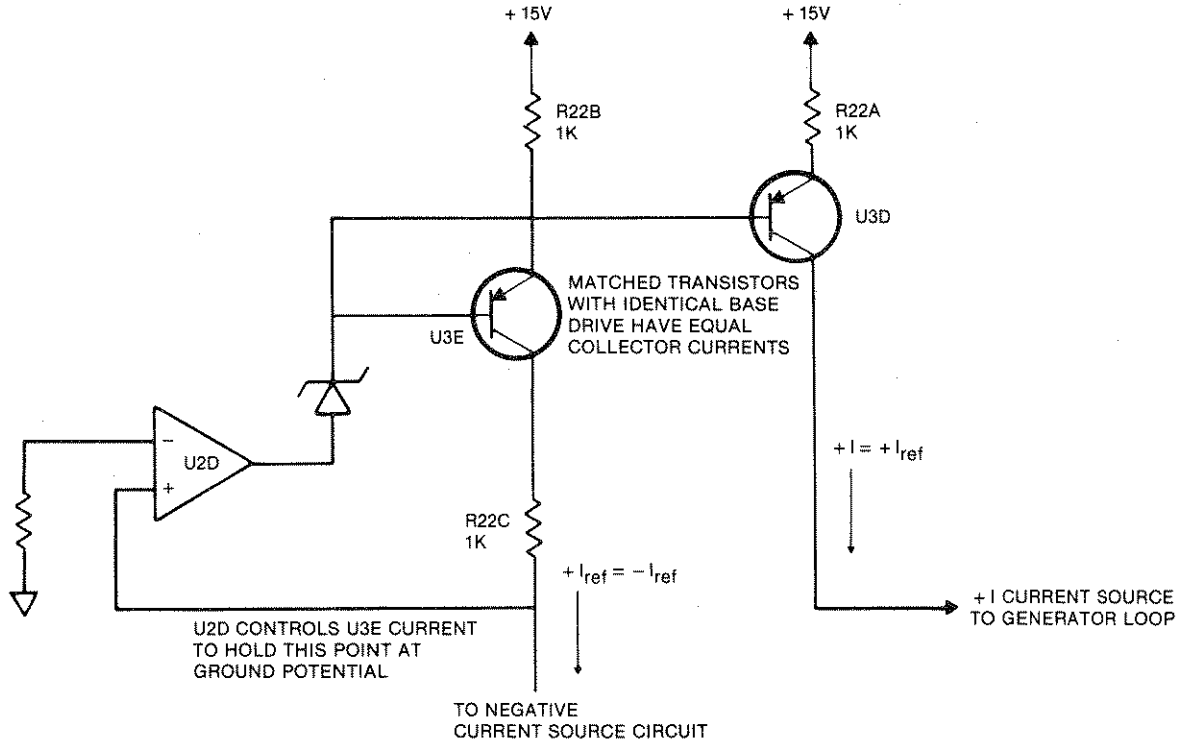


Figure 4-11. Simplified Schematic Diagram, Positive Current Source

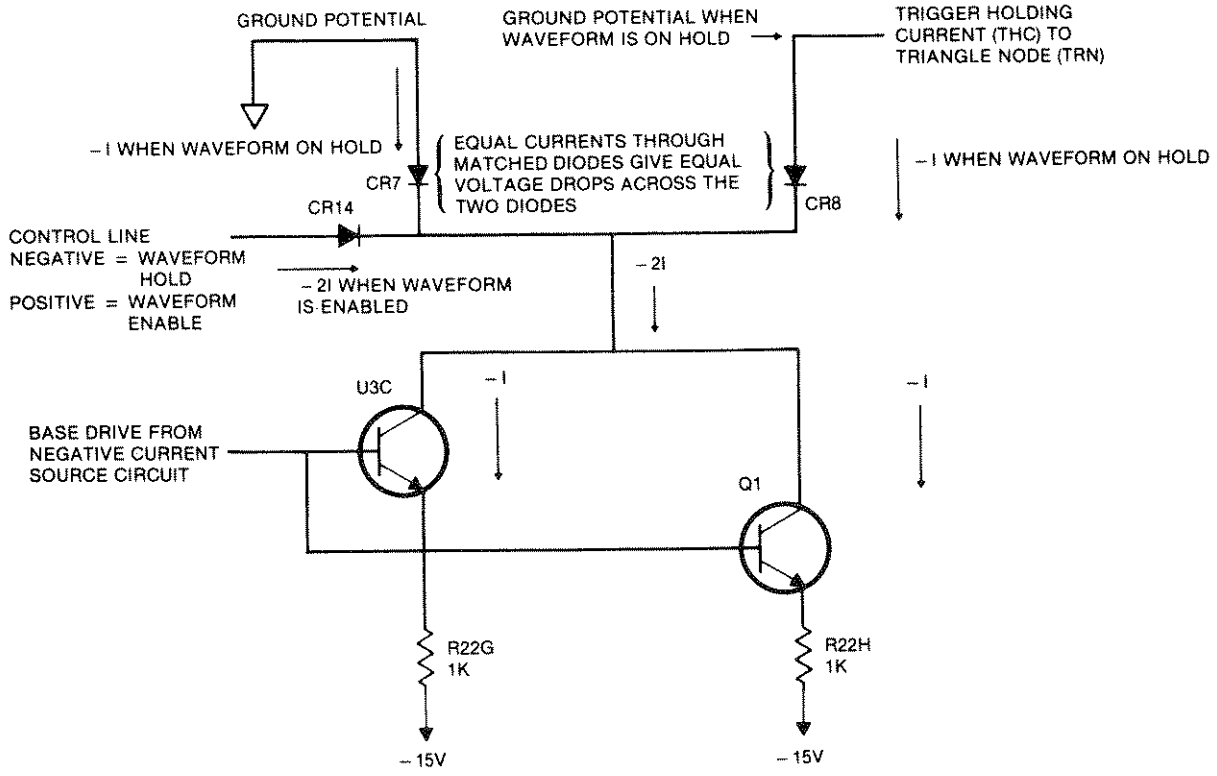


Figure 4-12. Simplified Schematic Diagram, THC Circuit

triangle node at ground potential during the "off" state in the gated and triggered modes. The circuit is shown in simplified schematic diagram figure 4-12.

The same transistor base drive that creates the negative current source (−I) is also applied to transistors U3C and Q1, driving each transistor to a collector current equal to −I. The two collectors are connected in parallel to provide a current equal to twice the −I current source. This −2I current is supplied by CR14 in the trigger circuit while the generator is gated "on".

When the generator is gated "off", a negative voltage is applied to the CR14 anode. This transition always occurs at the negative peak of the triangle waveform, and the −2I current is momentarily supplied by CR7. As the triangle node rises toward ground potential, a greater proportion of the −2I current flows through CR8. Equilibrium is reached when the trigger holding current is equal to the positive current (+I) being supplied to the generator loop, and the triangle node voltage cannot rise any further. Since the matched diodes CR7 and CR8 have equal currents through them and the anode of CR7 is grounded, the voltage drops across the two diodes will also be equal and the triangle node will be held at ground potential. This stops the waveform smoothly at the leading edge and ensures that at least one complete cycle will be generated every time the generator is triggered.

R23 adjusts the positive current source to precisely match the negative current and therefore maintain waveform symmetry. R12, which adjusts the low end frequency, sets the offset of the positive current amplifier, U2D, to match the offset of the negative current amplifier, U2C. R15 adds or subtracts current through the reference string to balance symmetry at low currents. The 8.2V zener diodes, CR4 and CR6, allow U3 pins 14 and 1 to approach the positive and negative supply rails respectively. Diodes CR3 and CR5 prevent latch-up.

The trigger level amplifier consists of an operational amplifier (U2B) in an inverting configuration that translates the trigger level control voltage from the microprocessor board (TRL, 0 to +10V) to the level used at the trigger comparator (TLO, +10 to −10V).

4.4.2 Generator Loop

The Generator Loop, shown in simplified schematic figure 4-13, produces simultaneous square and triangular waveforms. The triangular waveform is generated by alternately charging and discharging a timing capacitor from adjustable constant-current sources. The value of the selected timing capacitor

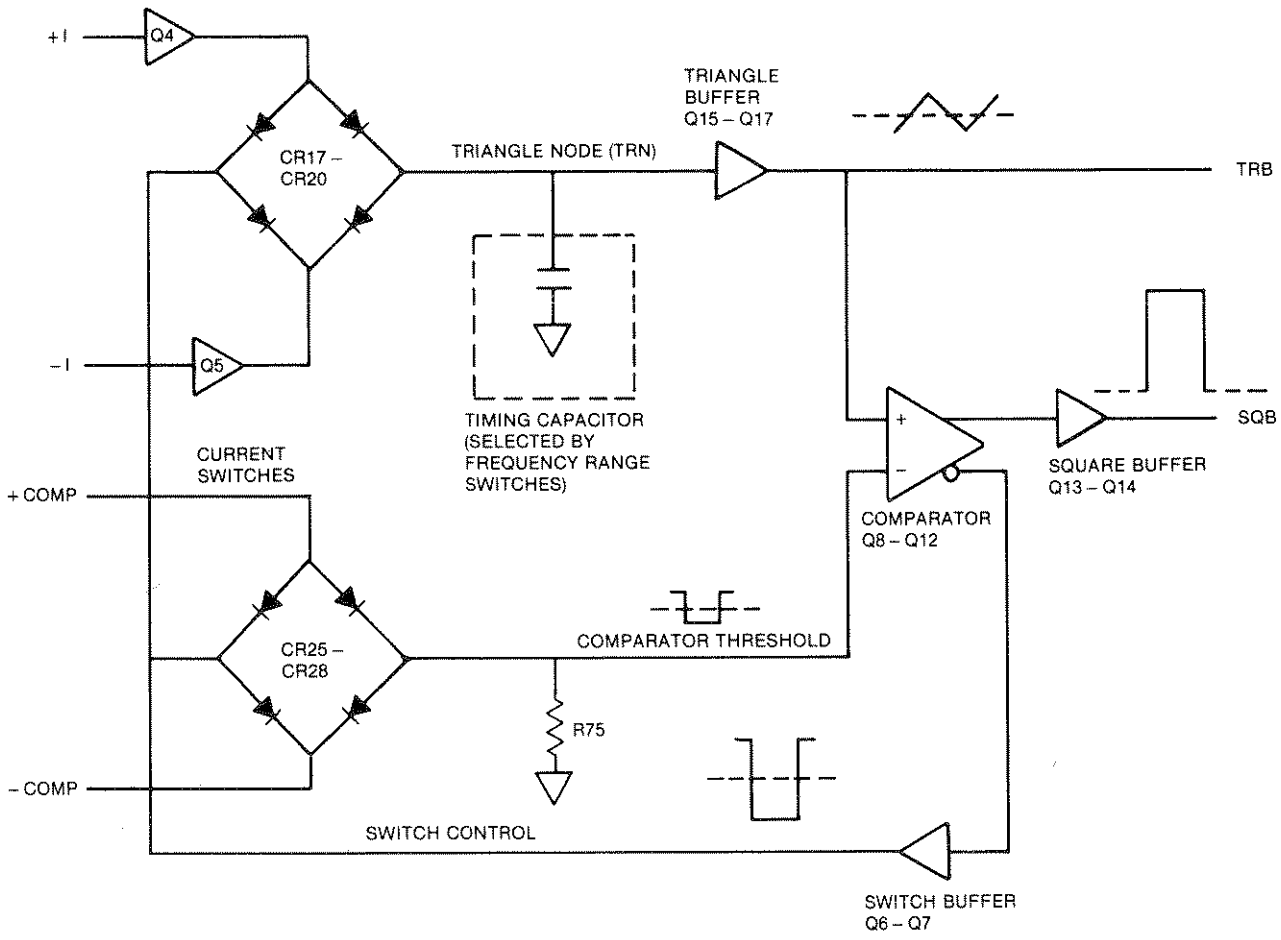


Figure 4-13. Simplified Schematic Diagram, Generator Loop

determines the frequency range of the loop. Within any range, frequency is determined by the magnitude of the +I and –I currents from the VCG circuit. Charging the capacitor from a current source gives a linear voltage change with respect to time, instead of the exponential curve that would result if a resistor were used.

The comparator monitors the amplitude of the triangle wave, and when it reaches the comparator threshold, the comparator changes states. The state of the comparator output determines the polarity of the comparator threshold and the direction of the capacitor charge/discharge current. The comparator output is also used to generate the square wave output.

Magnitude of the comparator threshold is determined by the value of the +COMP and –COMP currents from the high frequency compensation circuit. The positive or negative current selected by current switch CR25-CR28 flows through R75, and the voltage drop across R75 becomes the comparator threshold voltage. The high frequency compensation circuit reduces the +COMP and –COMP currents on the three highest frequency ranges to reduce the comparator threshold voltage to compensate for switching delays.

Operation of the diode current switch is illustrated in simplified schematic diagram figure 4-14. In this simplified schematic, voltage drops across the forward-biased diodes are assumed to be 0.6 volts, and the voltages shown are not intended to represent exact circuit voltages. Although this diagram shows the CR17-CR20 current switch, the same principles of operation also apply to the CR25-CR28 circuit.

The current switch has three inputs and one output. The inputs are the positive and negative currents (buffered by Q4 and Q5) and the control voltage; the output is the switched current. The magnitude of the control voltage must be greater than the voltage at the output that is caused by the switched current flowing

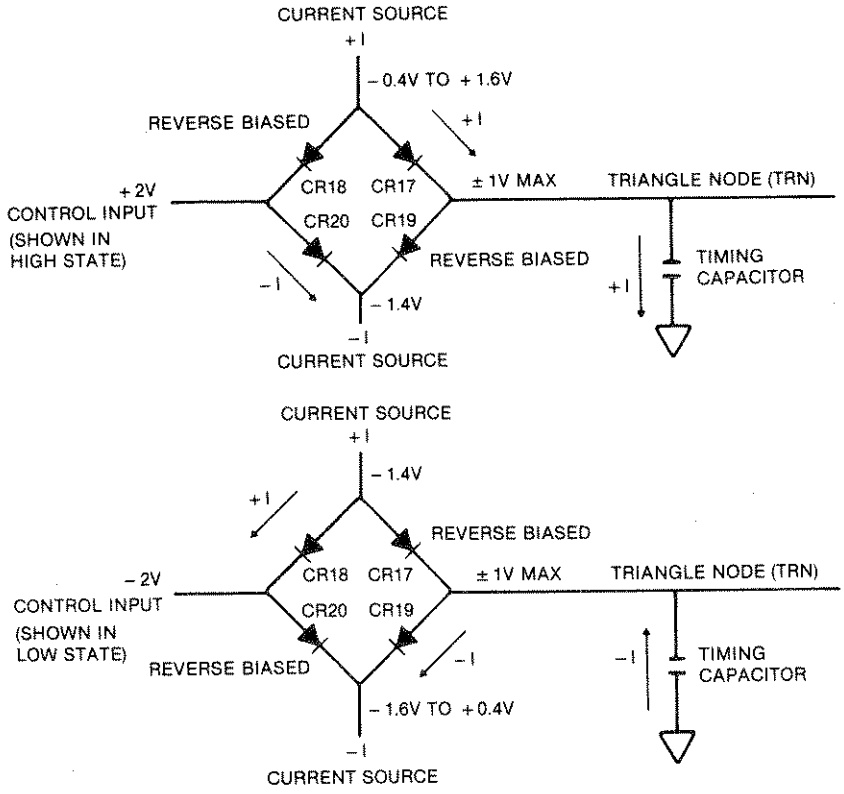


Figure 4-14. Simplified Schematic Diagram, Current Switch

through the external load. In this example, voltage at the triangle node (TRN) will not exceed ±1V before the comparator changes states and causes the voltage to move in the opposite direction.

With the control input at +2V, CR18 and CR19 are reverse biased. Current flows from the +I source through CR17 into the timing capacitor, and from the control line through CR20 into the negative current source. With the control line input at −2V, CR17 and CR20 are reverse biased. Current flow is from the +I source through CR18 into the control line, and from the timing capacitor through CR19 to the −I source.

The CR25-CR28 current switch operates in a similar manner. Voltage at the output of this switch is limited to ±1V by the 3 mA maximum value of the current and the 332Ω resistance of R75.

For the remainder of the circuit description of the Generator Loop, refer to the complete schematic diagram.

The comparator is made up of current source Q10, differential pair Q9 and Q11, and a second differential pair, Q8 and Q12. As the rising ramp of the triangle wave at the base of Q11 reaches the positive reference level (+1V) at the base of Q9, Q11 of the differential pair turns on as Q9 turns off. CR29 and CR30 increase the transistor switching speed by limiting the signal swing at the collectors of Q9 and Q11 to about 0.7V. As Q9 and Q11 switch, they also cause the second differential pair, Q8 and Q12, to switch. Resistors R72 and R84 increase the switching speed of Q8 and Q12 respectively by providing a small current which keeps them from turning entirely off. As Q8 switches to its relatively "off" state, current through R73 decreases and the collector of Q8 falls to its low state, about −1.6V, determined by the current drain through R71. The collector of Q8 drives the switch buffer; the square buffer is driven by Q12 in the opposite side of the comparator. These two stages have different values of collector and emitter resistors to match the output requirements of the associated buffers.

The switch buffer (Q6-Q7) is a push-pull emitter follower biased on by the voltage drops across CR22 and CR23. The output is a ±2.2V square wave that drives the two current switches in the generator loop.

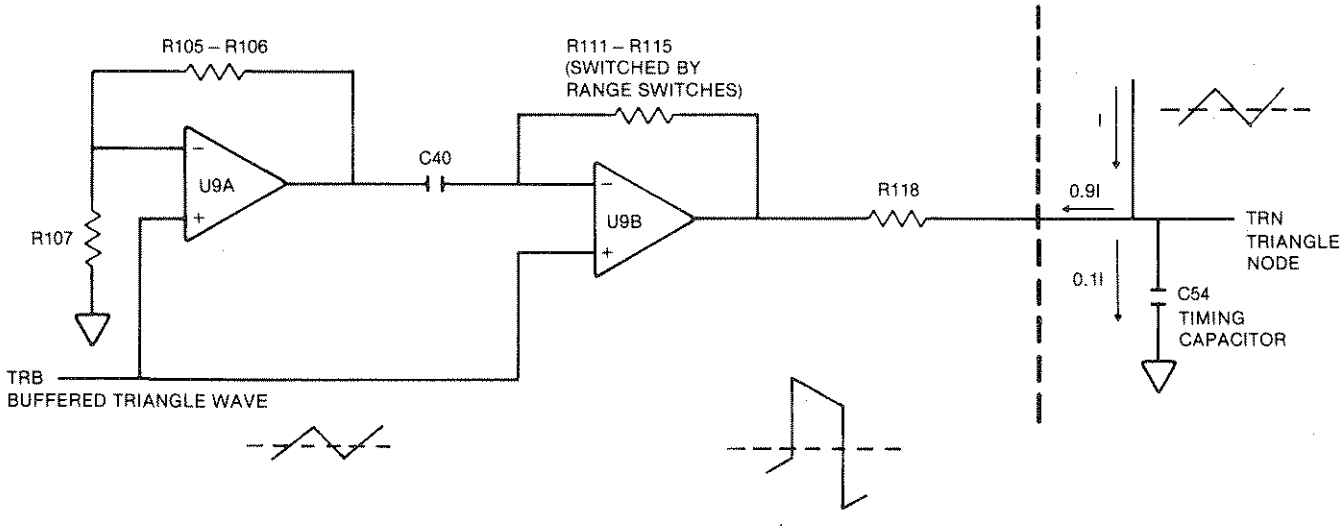
The square buffer (Q13-Q14) is similar to the switch buffer circuit, except that resistor values are tailored for a 0 to +5V output. This signal, SQB, is used to drive the sync driver and trigger circuits. The SQB signal is attenuated by R100 and R101 to provide the SQS signal used by the square logic and the auxiliary board. A highly differentiated portion of the SQB transient is coupled through C35, C36 and C27 to the triangle node to counteract switching transients which are coupled through the current switch diode bridge.

The alternating linear ramp (triangle wave) at the triangle node is buffered by the triangle buffer, a high speed FET input voltage follower. This circuit consists of Q15, acting as a source follower, and Q16, acting as an emitter follower. The voltage difference between the input and output of the circuit is controlled by maintaining the current through Q15 so that the gate-source voltage is equal and opposite to the base-emitter drop of Q16 and the two voltages cancel each other. The current through Q15 is initially set by adjusting R99, the NODE DC adjustment, after which the dc amplifier in the frequency compensation circuit maintains this adjustment through the constant current source, Q17, to compensate for temperature changes in Q15.

4.4.3 Frequency Range Switches

The selected range capacitor determines the frequency range from 100 Hz to 12 MHz. Each range normally covers 10% to 99.9% of full scale. Capacitance for the highest frequency range consists of all the stray capacitance on the triangle node added to C43 (the 1 MHz adjustment capacitor) and C44, which brings the total to 100 pF. The next range switches in an additional 900 pF, made up of C46, C47 and the 100 kHz adjustment C45. The next three ranges switch in successive matched capacitors of 0.01μF (C50), 0.1μF (C52) and 1.0μF (C54).

Each range capacitor is switched in by a logic level signal from the microprocessor board. For example, when $\overline{FR6}$ (Frequency Range from 0.1 MHz to 1 MHz) goes low, it turns on Q18, which sources about 30 mA through R124 and diodes CR36 and CR37. When CR37 is forward biased with this amount of current, its impedance to ground is less than 2Ω, and the range capacitor made up of C45, C46 and C47 is effectively connected to ground. When this range is not selected, $\overline{FR6}$ is high, turning off Q18 and allowing R125 to pull the anode of CR36 to −15V. The voltage divider, R121 and R122, pulls the anode of CR37 to −7.5V through the 10 MΩ resistor R123. Reverse-biased CR37 now provides an essentially infinite impedance,



NOTES:

1. Direction of currents shown is for capacitor charging in positive direction.
2. Ratio of capacitor current to total current depends on frequency range selected.

Figure 4-15. Simplified Schematic Diagram, Capacitance Multiplier

effectively disconnecting the range capacitor. The other range switches operate in exactly the same way.

4.4.4 Capacitance Multiplier

The capacitance multiplier extends the low end frequency range by drawing off (through R118) most of the charging current to and from the largest range capacitor, C54. The circuit is shown in simplified form in figure 4-15. The U9B output waveform is a triangle wave superimposed on a square wave. The square wave component determines the polarity of the voltage across R118, and therefore the direction of current flow through this resistor. The triangle component maintains the magnitude of the R118 voltage and current constant to maintain linearity of the triangle node waveform.

The square wave component is generated by differentiating the triangle wave. The triangle wave is amplified by U9A, then differentiated by C40 and U9B. U9B also sums the triangle wave at its non-inverting input with the square wave. The resulting output is applied to the triangle node through R118.

The capacitance multiplier is switched in at frequencies below 100 Hz by a logic low on the $\overline{\text{CPM}}$ control line. The proportion of capacitor charging current is determined by the range resistors. $\overline{\text{FR2}}$ selects R111 (plus the 99.9 Hz adjust, R112) and decreases the capacitor charging current to 10% of its normal value. Each successive decade of added resistance decreases the capacitor current to 10% of its previous range. R105 adjusts the overall calibration of the capacitance multiplier by adjusting the gain of the first amplifier, and R117 adjusts the capacitance multiplier symmetry by adjusting the offset of the second amplifier.

4.4.5 Frequency Compensation

The Frequency Compensation circuit contains the high frequency compensation, which reduces the Generator Loop comparator threshold on the three highest frequency ranges to compensate for comparator switching delays, and the dc amplifier circuit, which dynamically controls the dc offset in the triangle buffer.

The high frequency compensation circuit is shown in simplified schematic diagram figure 4-16. This circuit generates the two adjustable constant currents (+COMP and −COMP) that alternately flow through R75 in the comparator circuit in the Generator Loop to develop the comparator threshold voltages. On the lower frequency ranges, these currents each have a fixed value of 3 mA. On the three highest ranges, the currents are reduced in proportion to both the range selected and the programmed frequency within the range.

On the lower frequency ranges, the range switches are all open, and voltage divider R53, R50, R52 develops a voltage of +7.5V at the junction of R53 and R50. This voltage is applied to the non-inverting input of operational amplifier U7B, which drives the source of Q2 (and the inverting input of U7B) to the same voltage. The resulting +7.5V at the junction of R56 and R54 causes a current of 3.75 mA in R56 and 0.75 mA in R54. The difference of these two currents is the 3 mA +COMP current.

U7A and Q3 track the positive current source to generate a negative current (−COMP) of equal magnitude. U7A monitors the voltage at the midpoint of R54 and R57, which are connected in series between the source of Q2 and the source of Q3. As U7A acts to keep its two inputs at equal voltages (and the midpoint of the resistors at ground potential) it drives the Q3 source to a voltage equal in magnitude and opposite in polarity to the voltage at the Q2 source. The Q3 source voltage determines the currents in R57 and the series combination of R59 and R60. The difference of these two currents is the 3 mA −COMP current.

Operational amplifier U7C converts the negative Voltage Control Voltage (VCV) to a voltage that is positive in proportion (within any frequency range) to the programmed frequency. Although the range of this voltage is 0V to +6V, it will normally be above +0.6V except at the bottom end of the lowest frequency range. On the top three frequency ranges, one of the solid-state range switches is closed by a logic low on its control line, connecting this voltage through one of the range resistors (R42, R43 or R47) to the R53, R50, R52 voltage divider. This raises the voltage at the junction of R53 and R50, causing the absolute values of the Q2 and Q3 source voltages to increase and the source currents to decrease. The result is a decrease in the +COMP and −COMP currents proportional to both frequency range and programmed frequency within the range.

R44 causes a small voltage change in the output currents proportional to VCV to compensate for a small non-linearity in frequency tracking. R60 balances the triangle waveform, while R45 and R46 allow adjustment of frequency on the top two frequency ranges. Zener diodes CR15 and CR16 (not shown on the simplified schematic) act as level shifters to allow the operational amplifier outputs to operate near ground

NOTES:

1. Value of voltage or current shown is for VCV input of zero volts.
2. Absolute value of voltage increases in proportion to programmed frequency.
3. Absolute value of current decreases as programmed frequency is increased.
4. Amount of voltage or current change with frequency depends on setting of range switch. (No change if switches are all "open".)
5. Operational amplifier produces whatever output is required to maintain its two inputs at equal voltages.

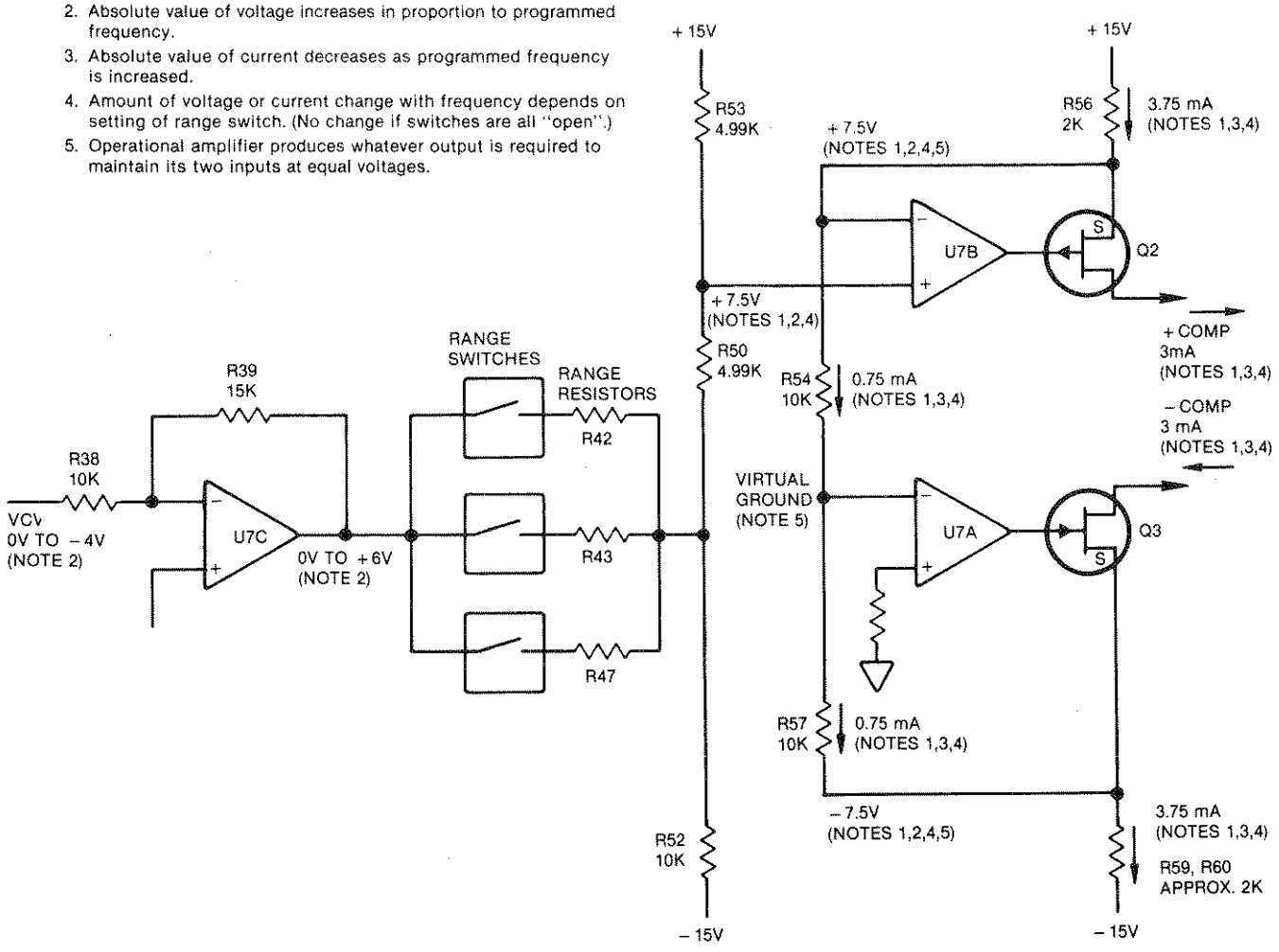


Figure 4-16. Simplified Schematic Diagram, High Frequency Compensation

potential while the gates of Q2 and Q3 operate closer to the supply voltages.

The dc amplifier keeps the output of the triangle buffer at the same dc level as the input by varying the current through the constant current source, Q17, and therefore through the input FET, Q15. It does this by comparing highly filtered signals at the operational amplifier inputs, U7D pins 12 and 13, and varying the current through R104 to compensate for errors. Below 100 Hz, $\overline{\text{DCA}}$ switches out filter capacitors C17 and C58; this allows U7D pin 14 direct control of the current through R104, thus giving greater accuracy.

4.4.6 Sync Driver

The Sync Driver is a double emitter follower that buffers the generator loop's square output, SQB, to provide a synchronizing signal for the instrument.

Transistors Q26 and Q27 are biased on by the voltage drop across CR52 and CR53. R171 and R175 provide about 4 mA through the diodes, and resistors R173, R181 and R183 balance the current so the transistors also have about 4 mA through them. The small emitter resistors also prevent thermal runaway. Collector resistors protect the transistors from overvoltage at

the output connector, and capacitors C70 and C71 prevent large signal swings at high frequencies that would reduce the gain of the transistors and add noise to the circuit.

4.4.7 Trigger Circuit

The trigger circuit allows the instrument user to trigger or gate the generator from an external signal of widely varying characteristics with a fixed and stable delay between the trigger source and the resultant generator output.

Trigger comparator U4 compares the level of the trigger input with the reference level (TLO) programmed in the generator. The comparator output goes to a logic low at U4 pin 9 if the trigger input becomes greater than the reference level and positive trigger slope (+TR) has been selected, or it goes to a logic low at U4 pin 11 if the trigger input becomes less than the reference level and negative trigger slope (−TR) has been programmed. A logic low transition at either comparator output will cause a logic high at the pin 8 output of NAND gate U5C; this positive-going transition clocks the remainder of the trigger logic.

In the Wavetek 275 the output of the trigger comparator at U5C is always routed through the auxiliary board, and the TRIG JUMPER is connected from E13 to E14. This jumper must never be connected from E12 to E13, as this will place the output of NAND gate U5C on the function generator board in parallel with the output of U6B on the auxiliary board.

Refer to Figure 4-17, Simplified Schematic Diagram, Trigger Circuit Mode Logic, for the following discussion. The trigger circuit is enabled by a logic high on the MC0 line. Selection of triggered or gated mode is performed by logic line MC1; the line is low for triggered mode or high for gated mode.

In the triggered mode, only one cycle of generator output is enabled for each trigger pulse applied. A logic low on mode control line MC1 disables NAND gate U5D. The high level on the output of U5D disables the direct $\overline{SET}$ input of flip-flop U6B and enables NAND gate U5B. A positive logic transition at trigger jumper terminal E13 clocks flip-flop U6B to the "set" condition, causing the $\overline{Q}$ output to go low. This low is applied to the direct $\overline{CLEAR}$ input of U6A, giving a logic low at the U6A Q output. The low at U6A-Q causes a high at the output of NAND gate U5A, reverse biasing diode CR8 and allowing the generator loop to oscillate. The first positive transition of SQB, 90° later on the triangle waveform, is inverted by NAND gate U5B and applied to the $\overline{CLEAR}$ input of U6B to clear the $\overline{Q}$ output high, thereby removing the low from the $\overline{CLEAR}$ input of U6A. The next negative transition of SQB is inverted by U5B, and clocks U6A to the "set" condition. The high at U6A-Q causes the output of gate U5A to go low, forward biasing diode CR8 and stopping the triangle oscillation on its rising edge.

In the gated mode, the generator output is continuously enabled for the entire duration of the applied trigger signal. A logic high on mode control line MC1 enables NAND gate U5D, causing the U5D output to be low whenever the E13 trigger level is high. Operation in the gated mode is the same as in the triggered

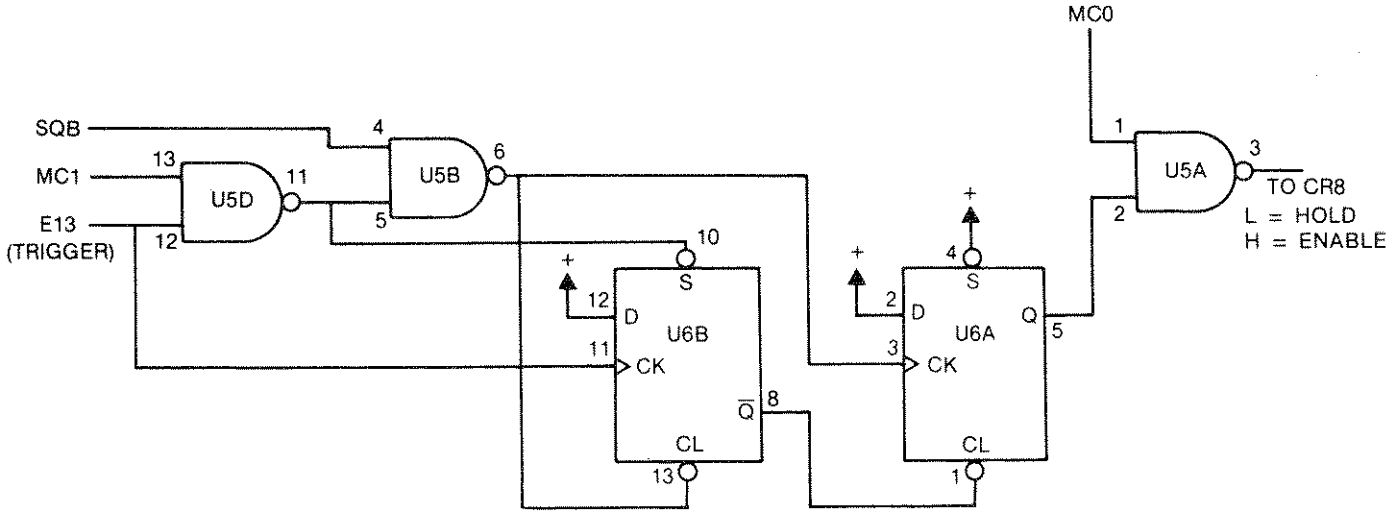


Figure 4-17. Simplified Trigger Circuit Mode Logic Schematic Diagram

mode except that during the time that the E13 trigger level is high, the resulting low at the U5D output will:

1. Hold flip-flop U6B in the "set" condition via the direct $\overline{SET}$ input.
2. Disable NAND gate U5B, preventing the SQB signal from clearing U6B and clocking U6A until after the trigger signal is removed.

Resistors R29, R303, R34, R31 and R32 divide the reference (TLO) and input (TRIG IN) voltages by a factor of 4 to bring them within range of the U4 comparator. Diodes CR9, CR10 and CR11 protect the U4 comparator from excessive voltage at the trigger input. Resistors R33 and R35 provide a small amount of hysterisis at the U4 comparator input to prevent false triggering on noise.

4.4.8 Function Select

The function select circuit connects the sine, triangle or square (all disconnected in dc or the arbitrary waveform functions) to the current input of the X-Y multiplier.

The sine wave input is created from the triangle buffer output, TRB, by the sine converter which uses the logarithmic response characteristics of semiconductors diodes to approximate a sine wave current output. The SIN DIST A adjustment, R142, adjusts the converter input for diode forward voltage variation. The six diodes in U11 give a three stage sine approximation using very closely matched characteristics of the diodes. Two adjustments, SIN DIST B and SIN DIST C (R154 and R157), balance between stages for positive and negative peaks respectively. The current output is switched through FET switch U12A when $\overline{SIN}$ is selected.

The triangle level control (R148), provides an adjustable current to FET switch, U12C controlled by $\overline{TRI}$. Both the triangle and sine FET switches provide increased isolation by shorting the FET switch input (with Q25 and Q22 respectively) when the switch is off.

The square logic selects which rectangular waveform is fed to the square shaper. A logic high on the $\overline{SQR}$ control line selects the uninverted SQS square wave, while a high on the SQR line selects the SQS signal after it has been inverted by U13C. A logic high on the external width control line (EXW) selects the output of the trigger circuit, TRGI.

The pulse input, PLSI, and associated control lines PLS and $\overline{PLS}$ are not used in the Wavetek 275.

The square shaper converts the TTL level signal at U13A pin 3 to ±1 mA. It shifts the TTL signal and uses it to switch current sources through a diode switch (CR48 through CR51) and into the FET switch U12D (controlled by $\overline{RCT}$). The current sources for upper and lower levels of square waves are independently adjustable by R164 and R168 respectively.

4.4.9 X-Y Multiplier and Offset

4.4.9.1 X-Y Multiplier

The X-Y multiplier is a precision voltage-controlled amplifier that drives the preamplifier with a signal level directly proportional to the amplitude control voltage (AMP) from the microprocessor board.

As shown in the figure 4-18 block diagram, the X-Y multiplier consists of five major circuit groups: Logarithmic signal compressor, variable gain signal amplifier, logarithmic dc reference, variable gain reference amplifier, and dc amplifiers. The input signal (XYI or EXT IN) is logarithmically compressed in U18A, then amplified by variable gain signal amplifier U19A. Because the control voltage vs. gain characteristic of the variable gain amplifier is not linear, the remainder of the circuit is required to convert the input amplitude control voltage (AMP) to a modified gain control voltage.

U18B generates a dc reference voltage proportional to the logarithm of the difference of two currents. This reference voltage is amplified by variable gain reference amplifier U19B and fixed gain dc amplifiers U17A and U17D, then compared to the amplitude control voltage (AMP) by U17B. U17B provides the modified gain control voltage to both variable gain amplifiers, and adjusts the gain of the reference amplifier upwards or downwards as required until the amplified reference voltage is equal to the input amplitude control voltage (AMP). The same modified gain control voltage that controls the gain of the variable gain reference amplifier is also applied to the variable gain signal amplifier.

The logarithmic signal compressor (U18A) consists of a differential transistor pair connected as diodes. One side of the differential pair is connected to ground, the other side to the XYI signal input and also, via R300, to the external input, EXT IN. Each side of the differential pair is biased to about 3 mA (the optimum diode current for logarithmic compression) by the current source transistor within the IC. The input signal current (±1 mA) on the XYI line causes a small ac voltage across the diode that varies approximately as the logarithm of the total current. This voltage also drives one base of the output differential pair (U19 pin 2), while the other base is approximately at ground

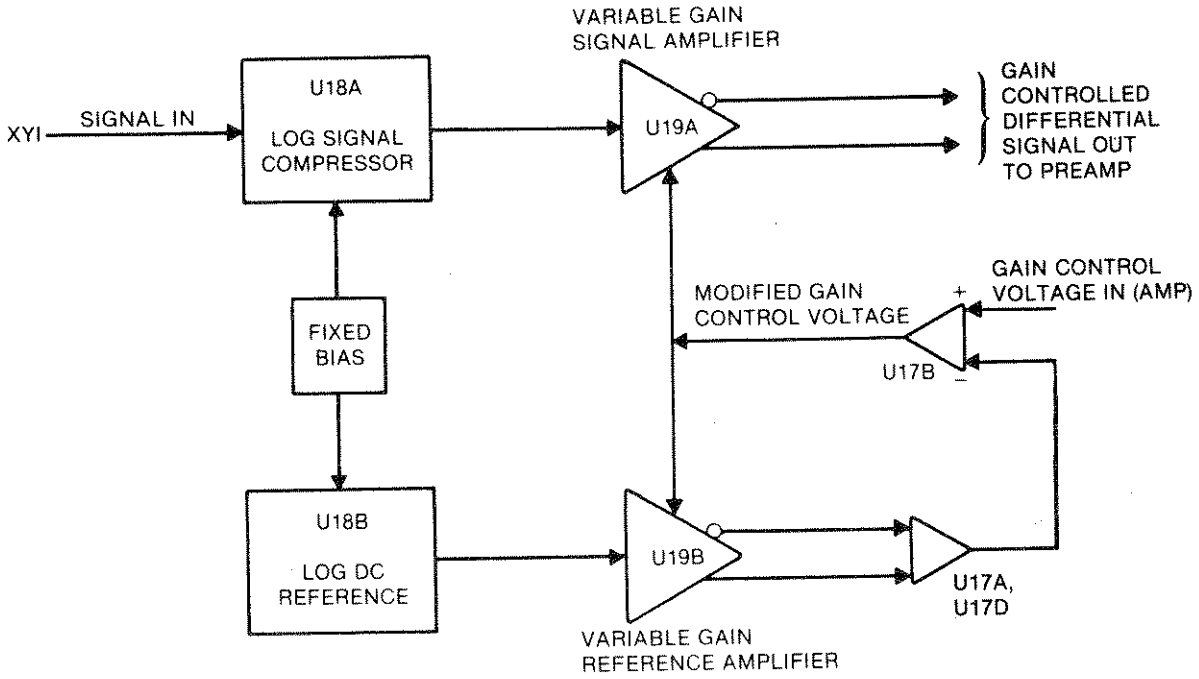


Figure 4-18. X-Y Multiplier Block Diagram

potential, adjusted by the multiplier distortion adjustment, R255. The current source transistor in the output stage (U19 pin 3) is driven by the modified gain control voltage. Maximum output from the stage occurs with a maximum total bias current of 6 mA; less bias current produces less output.

The logarithmic dc reference (U18B) is configured much the same as the logarithmic signal compressor described above. Total bias current through the differential pair is fixed at 6 mA, but is unevenly split, with 4 mA through one side and 2 mA through the other side (limited by R242 and R243). This corresponds to the current ratio in the signal compressor during peaks of the signal, when the instantaneous peak signal current of 1 mA adds to the 3 mA dc current in one half of the differential pair and subtracts from the 3 mA dc current in the other half. The dc reference voltage is taken from U18 base and collector terminals 8 and 9.

A simplified schematic diagram of the variable gain reference amplifier and associated dc amplifiers is shown in figure 4-19. The input amplitude control voltage (AMP) drives U17B (pin 5), which in turn drives the base (pin 11) of the current source transistor in U19B. The base of one side of the differential pair (U19 pin 9) is connected to ground through a resistor; the base of the other side of the pair (U19 pin 6) is connected to the log dc reference voltage. These base voltages will maintain the currents in the differential pair in the ratio 1:2 regardless of total current flow determined by the current source transistor. The collectors of the differential pair are connected to the inverting inputs of operational amplifiers U17D and U17A (pins 13 and 2). These inverting inputs are "virtual grounds"; because the non-inverting inputs of these amplifiers are grounded, each amplifier will provide whatever output level is required to keep its two inputs at the same voltage level. The value of resistors R256 through R258 were chosen so that with 6 mA through the current source transistor in U19B:

1. 2 mA flows through R256 from U17D pin 17 to U19B pin 7.
2. 2 mA flows through R257 from U17D pin 14 to U19B pin 8.
3. An additional 2 mA flows from U17A pin 1 through R258 to U19B pin 8.
4. The voltage at the output of U17A (pin 1) is 10 Vdc, which exactly equals the 10 Vdc external AMP input, maintaining the inputs of U17B (pins 5 and 6) at equal voltages.

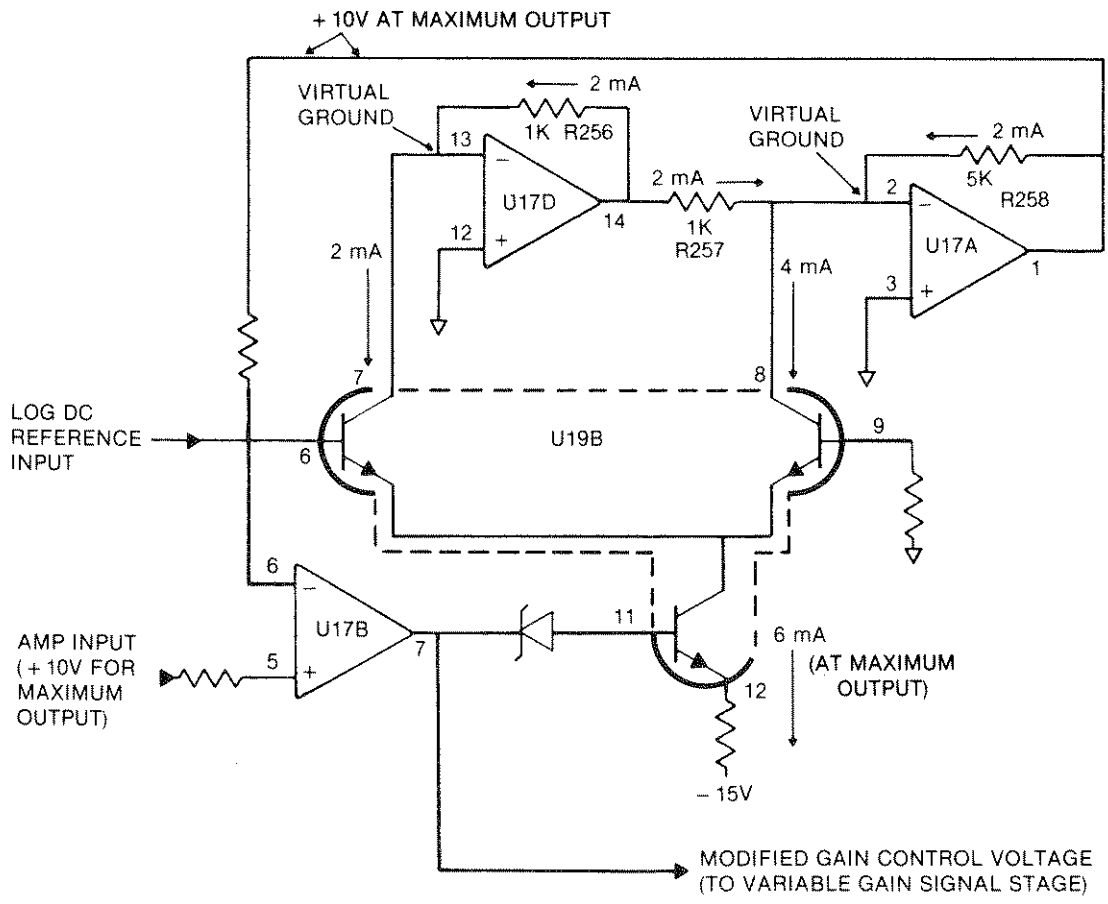


Figure 4-19. Variable Gain Reference Amplifier

With input amplitude control voltage (AMP) less than 10V, all voltages and currents in the circuit are proportionately less.

The output of the circuit is the modified gain control voltage at the output of U17B (pin 7). This voltage is used to control the variable gain signal amplifier.

Fixed bias for both sections of U18 is provided by R248, CR59 and CR60. CR61 performs a level shifting function, allowing the base terminals of U19 (pins 3 and 11) to operate near the negative supply voltage while the output of U17 (pin 7) operates closer to ground potential.

The X-Y multiplier circuit contains four calibration adjustments: R241, R242, R251 and R255. Adjustment procedure for these controls is given in the CALIBRATION section of the manual.

4.4.9.2 Offset Circuit

The offset circuit is a level translator that converts the 0 to + 10V input from the microprocessor board (OST) into a + 5 to – 5 Vdc signal that sums into the output amplifier. Any offset caused by the operational amplifier at U17C pin 8 is corrected by the offset zero adjustment, R237. The output of the amplifier is then adjusted for dc offset by the offset adjust, R208.

4.4.10 Preamplifier

The preamplifier takes the differential current output of the X-Y multiplier from U19 pins 1 and 14 and converts it to a single-ended voltage output at the anode of CR54. The voltage at the inputs of the differential stage (U15 pins 3 and 16) must be maintained at about + 0.7 volts to bias the input transistors whose emitters are at ground. The emitter of the transistor at U15 pin 8 provides the current to maintain this voltage. The current can be as high as 6 mA or as low as 0.06 mA, depending on the current required by the output stage of the X-Y multiplier. Added to this current is the bias current for the preamplifier itself, about 1 mA each through the feedback resistor strings consisting of the 750Ω, 0.1% resistors R189

and R192, and R194 and R198. The full-scale current output of the X-Y multiplier is ±1 mA in each leg of the output differential stage, and this current is translated into a ±0.75 Vac signal at U15-8 and a ±1.5 Vac signal of the opposite phase at the CR54 anode. PNP transistors Q28 and Q29 act as constant current sources for the input stage collectors (U15-2 and U15-1 respectively) and they also act as an ac bootstrap through coupling capacitors C76 and C79. The emitter follower stages, U15-8 and U15-11, isolate the collectors of the input stages to provide a low impedance output.

4.4.11 Output Amplifier

The output amplifier is an inverting and summing amplifier with a gain of about −6.67 for the ac signal from the preamplifier. The amplifier operates differently for high-frequency signals than for low-frequency signals; high-frequency signals couple into the symmetric emitter followers Q30 and Q31 through capacitors C90 and C91 respectively. The emitter followers then drive the symmetrical inverter stage consisting of Q32 and Q33. Diodes CR55 and CR56, with the 10Ω resistor, R219, provide a bias current through the output stage of Q34, Q35, Q36 and Q37 to increase output speed by keeping the transistors always on. The 10Ω emitter resistors, R227, R228, R231 and R232, balance the current through the parallel output stage transistors to improve their power handling capability. The output signal (+ and − 10V, maximum) is fed back through resistors R223 and R217 in series to the input. The trim capacitors, C97 (output amplifier peaking) and C122 (output amplifier roll-off), adjust the amplifier high speed characteristics by rolling off or peaking the feedback signal respectively.

The low-frequency (and dc) path in the output amplifier is through the transistor array, U16, connected as an operational amplifier. The positive output of the differential input stage (U16-3) is inverted at U16-9. This signal decreases the current through transistor Q32 and the signal at its collector falls until the fed back signal balances the input, either ac (through R207) or offset (through R208 and R209). The PNP transistors in U16 balance the current through the differential input pair and provide a high impedance load for the first stage output. Capacitor C86 decreases the speed of the low-frequency section at high frequencies.

4.4.12 Output Protection and Attenuator

There are three output amplifier protection safeguards to protect this circuit against major damage under the severest accidental misuse, including accidental connection of line power to the FUNC OUT connector. These safeguards are:

1. An overvoltage sensing circuit that detects voltages that exceed the ±15V limits at the FUNC OUT connector. When an overload is detected, the circuit opens all relays in the output attenuator circuits and disconnects the amplifier from FUNC OUT.
2. An in-line fuse to protect the amplifier in case the voltage is great enough to arc across the relay contacts. Should the fuse blow, a sensing circuit alerts the microprocessor.
3. Two voltage-limiting, high current diodes (CR57 and CR58) at the amplifier output that prevent an externally applied voltage from pulling the amplifier output line beyond the range of the ±15V supplies.

4.4.12.1 Overvoltage Sense Circuit

The overvoltage sense circuit compares the voltage at FUNC OUT (through isolating 1 MΩ resistors R298 and R299) with the ±15V power supplies at U20 pin 4 and U20 pin 6 respectively. If the voltage at FUNC OUT goes higher than +15V or lower than −15V, the appropriate comparator output (U20 pin 2 or U20 pin 1 respectively) goes negative. Since the outputs are wire-ORed, when either output becomes negative it drives the comparator output at U20 pin 14 positive. This turns off Q38 and opens all relays to disconnect the amplifier from the output. The positive level at U20 pin 14 also signals the microprocessor (via the OAP line) that the output protection circuit has been activated. The microprocessor immediately signals the operator through the front panel display, the beeper and the GPIB. Removal of the external overvoltage immediately returns the output to its previous state and normal operation is resumed. The response of the relays is usually fast enough to prevent any damage whatsoever to the output amplifier with overvoltages up to 200 Vdc or 140 Vac.

4.4.12.2 Fuse Protection

Voltages greater than ±200V may cause the relay contacts to arc and conduct. If such a condition occurs, a fast-acting fuse, F1, will generally blow soon enough to prevent, or at least minimize, damage to the instrument. A fuse sense circuit detects when the fuse is blown by pulling the output side of the fuse toward +15V through 1 MΩ resistor, R288. If the fuse is open during power-up or reset (K1 off), the sense point rises higher than the amplifier output would normally let it go and the comparator output at U20-13 goes high if that voltage rises above +13.6V. The

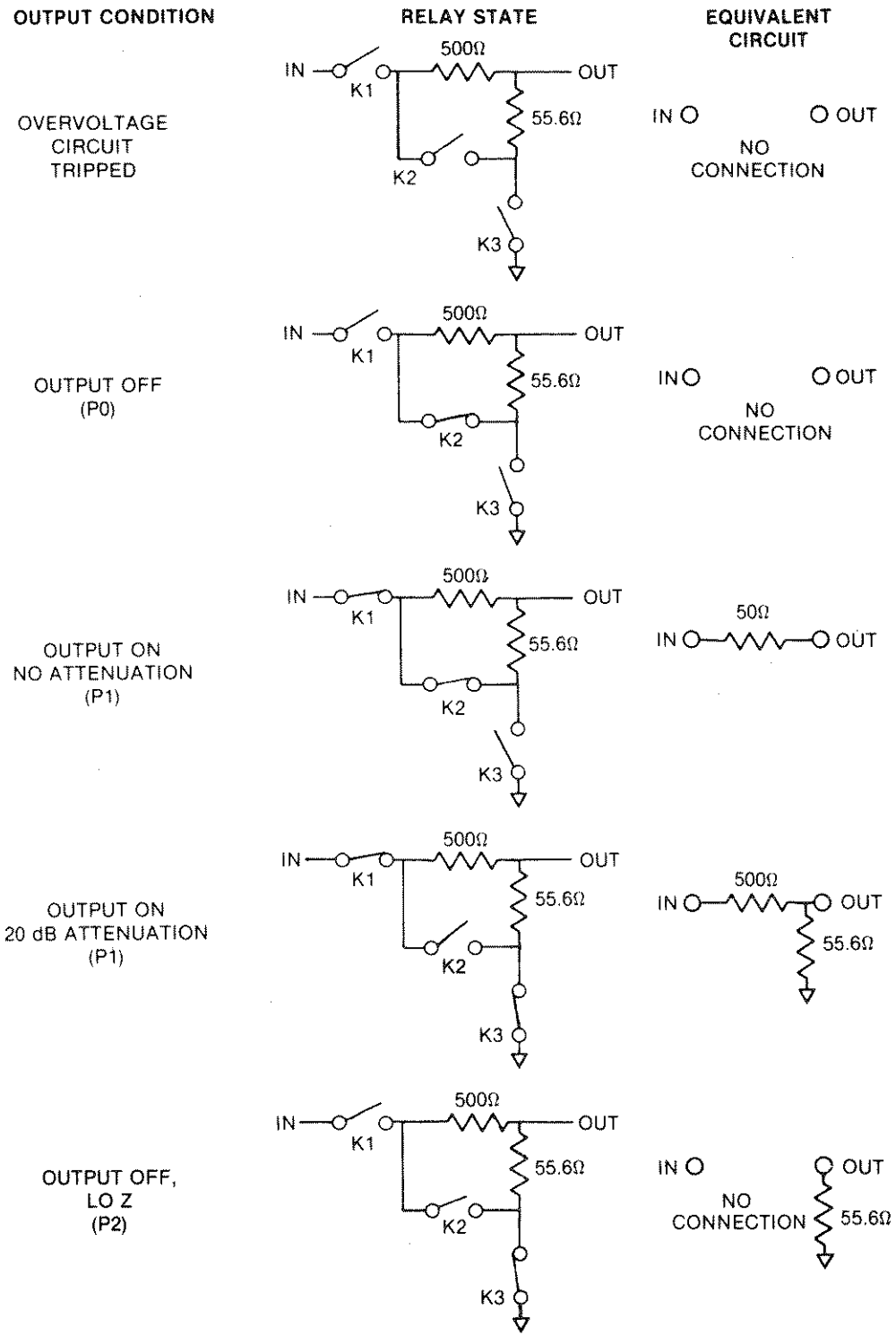


Figure 4-20. Output Attenuator Relay States

microprocessor samples the logic levels at the fuse-blown indicator line (FUB) and signals the operator through the front panel display and the GPIB bus.

4.4.12.3 Output Attenuator

All three output relays (K1, K2 and K3) are independently driven by Q39, Q40 and Q41 and controlled by logic lines OA0 and OA2 from the microprocessor. OA0 determines whether or not the output amplifier is connected, while OA2 switches the attenuator in or out. K2 and K3 both operate from the OA2 line, and operate opposite of each other (when one is on, the other is always off).

There are five possible combinations of operating states for the three relays. They are:

1. Overvoltage circuit tripped (Q38 turned off).
2. OUTPUT OFF (0) mode.
3. OUTPUT ON (1) mode, no attenuation. Output voltages (amplitude + offset) programmed for greater than 1.00V.
4. OUTPUT ON (1) mode, 20 dB attenuation. Output voltages (amplitude + offset) programmed for 1.00V or less.
5. OUTPUT OFF, LO Z (2) mode. Output terminated in approximately 50 ohms.

Relay states for these five conditions are shown in simplified schematic diagram Figure 4-20. In this figure, R289-R292 and R295 are shown as a single 50Ω resistor; R293, R294, R296 and R297 are shown as a single 55.6Ω resistor.

4.5 AUXILIARY BOARD CIRCUIT DESCRIPTION

The auxiliary board contains four major functional circuit groups. These are:

1. The arbitrary waveform generator, which generates a user-defined waveform from data stored in an internal RAM.
2. The burst counter, which enables the generator output for a predetermined number of output cycles when the burst mode is selected and the circuit is triggered.
3. The frequency synthesizer, which generates frequencies used to clock the arbitrary waveform generator when an arbitrary waveform function is selected, or to internally trigger the instrument when internal trigger and a non-arbitrary function are selected.
4. The data registers, which store data from the 8-bit data bus to drive 79 of the internal data and control lines.

4.5.1 Data Registers

The data register circuit consists of address decoders U18 and U19, and data registers U3-U5, U14-U17, U31-U32 and U34. The address decoders are enabled, one at a time, by a logic low on either the $\overline{ANA2}$ or $\overline{ANA3}$ line (J16 pins 12 and 13.) The selected decoder provides a logic low on one of its eight output lines; the output line selected is determined by the binary value of the three input address lines. For example, an address of "000" selects output 0, while an address of "111" selects output 7. Four of the 16 outputs are used directly as control or clock lines; two of the outputs are not used, and the remaining ten outputs are used to latch data into the data registers.

The ten data registers are octal type "D" flip-flops that latch data from the buffered data bus (J16 pins 1 through 8) onto the register output pins, where it is continuously available to the remainder of the circuits on the board. Each register is clocked by the microprocessor and address decoder at a time when the data on the buffered data bus is valid for that particular register. Clocking occurs on the rising edge of the clock pulse, at the end of the momentary low on the clock line.

4.5.2 Burst Counter

The burst counter enables the function generator or arbitrary waveform generator for a predetermined number of cycles when the burst mode is selected and the circuit is internally or externally triggered. The four circuit groups within the burst counter are the trigger select logic, the burst clock select gates, the burst logic and the preset counter. Figure 4-21 shows a simplified functional block diagram of the burst counter circuit.

The trigger select logic determines whether the burst logic will be triggered externally from the output of the trigger comparator on the function generator board via the TRGO line, or internally from either the output of the frequency synthesizer (via the SYNTH line) or the square wave output of the function generator (via the SQS line). The selected trigger source (TRGOB) is also supplied to the arbitrary waveform generator for use in some of the non-burst modes.

The burst clock select gates allow the burst counter to count either the SQS square wave output of the function generator or the STOP signal from the arbitrary waveform generator. This STOP signal occurs at the end of every arbitrary waveform cycle.

The preset counter counts the number of waveform cycles that occur during the burst. When the predetermined number of cycles have been counted, the

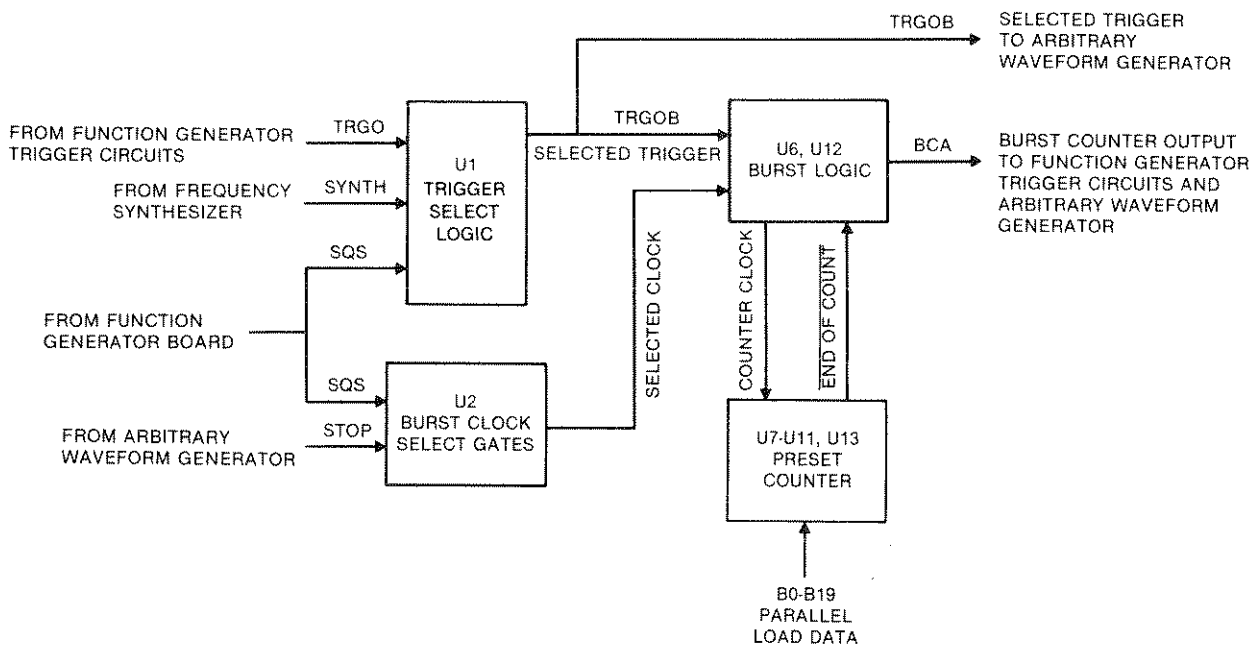


Figure 4-21. Simplified Functional Block Diagram, Burst Counter Circuit

counter circuit signals the burst logic via a logic low on the "$\overline{\text{end-of-count}}$" line.

The burst logic, when triggered in the burst mode, gates the selected burst clock source through to the counter circuit and latches the burst counter output line (BCA) high for the duration of the count. If burst mode is not selected, the burst logic gates the selected trigger input (TRGOB) directly through to the output line (BCA). The BCA line is routed to the arbitrary waveform generator, and also to the remainder of the trigger logic on the function generator board via the TRGI line (J15 pin 7.)

The trigger select logic uses an 8-input multiplexer, U1, to select one of three trigger sources. U1 selects the input that corresponds to the binary value on its three address lines. Only four of the eight inputs are used, and the most significant bit address line (pin 9) is permanently grounded. An address of "000" selects the function generator SQS waveform at pin 4. A value of "001" selects the frequency synthesizer output at pin 3. A value of "010" or "011" selects the external trigger signal TRGO at either pin 2 or pin 1, which are wired in parallel. The output from pin 5 is applied to the burst logic.

The burst clock select gates (U2A through U2D) select either the SQS output of the function generator or the STOP pulses from the arbitrary waveform generator for application to the burst logic and counter clock. A logic high on the BURST CLK SEL line enables NAND gate U2B, and is inverted by U2D to disable U2A. A logic low on the control line disables U2B and enables U2A. U2C combines the output of the selected gate with the constant logic high from the disabled gate, and re-inverts the selected signal to the original polarity. R1 and C4 filter undesired switching spikes from the STOP line to prevent false clocking.

The preset counter is composed of presettable 4-bit binary counters U7 through U11, and terminal count detector NAND gate U13. When the preset counter receives clock pulses from the burst logic, it preloads data from the data registers then counts pulses from the burst clock select gates, counting upwards from the preloaded value. When the final count value is reached, the circuit commands the burst logic to return the BCA output line low.

Although U7 through U11 are capable of counting to 1,048,575 ($2^{20}-1$), the maximum count is limited to 1,048,200 by terminal count detector U13. The binary equivalent of 1,048,200 is $2^3 + 2^7 + 2^9 + \ldots + 2^{19}$, and only those counter output lines are monitored by U13. (Note that some of the counter outputs are not used.) The binary number that will be loaded from the data registers into the preset counter is this maximum count minus the desired count plus one. (The burst

logic will always allow one extra cycle after the preset counter reaches maximum count.)

At maximum count, all of the U13 inputs are high, and the output is low. This logic low is applied to the counter $\overline{\text{LOAD}}$ inputs, and also to the burst logic. The allowable combinations of burst counter trigger and clock are as follows:

1. For a non-arbitrary waveform with internal trigger, the burst counter is triggered by the synthesizer and counts the function generator output (SQS).
2. For an arbitrary waveform with internal trigger, the burst counter is triggered by the function generator (SQS) output and counts arbitrary waveform cycles via the STOP line. (In the arbitrary waveform modes the synthesizer is used to clock the arbitrary waveform generator and is not available for internal triggering.)
3. For a non-arbitrary waveform with external trigger, the burst counter is triggered by the trigger comparator output line (TRGO) and counts the SQS function generator output.
4. For an arbitrary waveform with external trigger, the burst counter is triggered by the TRGO line and counts arbitrary waveform generator STOP pulses.

The microprocessor will not select illogical combinations of trigger and clock, such as SQS trigger and SQS clock, or SYNTH trigger and STOP pulse clock.

The burst logic consists of NAND gates U6A through U6D, and type "D" flip-flops U12A and U12B. This circuit is activated by a trigger pulse (TRGOB) from the trigger select logic, and provides a logic high on the Burst Counter Active (BCA) line. In the burst mode, the BCA line is held high for the duration of the burst. When the burst mode is not selected, the BCA output pulse is a copy of the input pulse at TRGOB. The BCA output is applied to both the function generator (via the TRGI line at J16 pin 7) and the arbitrary waveform generator.

In the burst mode, the BURST line is at a logic high, and the $\overline{\text{BURST}}$ line is at a logic low. The logic low on the $\overline{\text{BURST}}$ line disables NAND gate U6D and enables NAND gate U6B via the constant high at the U6D output. The logic low on the $\overline{\text{BURST}}$ line is also applied to the data input of flip-flop U12A.

Initially, the counter is in the maximum-count condition, and the output of the terminal count detector is at a logic low. This logic low is applied to the $\overline{\text{LOAD}}$ inputs of counter stages U7 through U11 to enable loading of the preset data at the next clock pulse. The same logic low disables NAND gate U6A to prevent the selected clock signal (SQS or STOP) from clocking the counter, and enables NAND gate U6C (via the logic high on the U6A output) to allow the load pulse from U12A to clock the preset data into the counter stages.

A positive logic transition at the TRGOB trigger input clocks the U12A Q output low. The negative-going transition at the U12A Q output is inverted by U6C and applied to the counter clock inputs to load the preset data. As soon as the counter is loaded with preset data, it is no longer at the maximum count condition and the U13 output goes high, disabling the counter LOAD inputs and enabling NAND gate U6A. However, at this point, the SQS square wave input cannot yet reach the counter clock inputs because NAND gate U6C is disabled by a logic low from U12A.

After a time delay determined by R4 and C12, the logic low at the U12A Q output is applied to the U12B $\overline{\text{SET}}$ input to set the U12B $\overline{\text{Q}}$ output low. This low is inverted by U6B and provides a logic high on the BCA output line. The logic low at the U12B $\overline{\text{Q}}$ output is also applied back to the direct $\overline{\text{SET}}$ input of U12A to set the U12A Q output high. The logic high from the U12A Q output enables NAND gate U6C to pass the selected clock pulses (SQS or STOP) to the counter.

When the counter reaches maximum count, the output of the terminal count detector U13 goes low, disabling NAND gate U6A and preventing clock pulses from reaching the counter. U13 also supplies a logic low to the data input of flip-flop U12B. The next positive transition of the selected clock will clock the U12B Q output high, causing U6B to return the BCA output line to a logic low state.

When the burst mode is not selected, the BURST line is at a logic low state and the $\overline{\text{BURST}}$ line is at a logic high. The logic low on the BURST line holds the $\overline{\text{CLEAR}}$ input of flip-flop U12B low, maintaining a logic high from the U12B $\overline{\text{Q}}$ output to enable NAND gate U6B. The logic high on the $\overline{\text{BURST}}$ line enables NAND gate U6D. Any trigger signal applied to the TRGOB line will be gated through U6D and U6B to the BCA output.

Resistors R2 and R3, marked "TRIM" on the schematic, are external pull-up resistors to increase speed and reduce power consumption of the preset counter. These resistors are not required for type 74LS counters, but space has been provided for them on the board for future use with type 74HC devices. These resistors, when used, have a typical value of 10kΩ.

4.5.3 Frequency Synthesizer

The frequency synthesizer generates the 3.75 mHz to 3.75 MHz signal used to clock the arbitrary waveform generator in the arbitrary waveform modes or to internally trigger the function generator circuit in the non-arbitrary modes. The frequency synthesizer contains two major circuit groups; the Phase Locked Loop (PLL) composed of U35, U37 and U38, and programmable binary divider U36. (Operation of the U34 data register was previously discussed in section 4.5.1.) The PLL circuit operates over the frequency range of 7.5 MHz to 15 MHz in 1 kHz increments. The 7.5 MHz to 15 MHz signal is then divided by the selected ratio (between 2^2 and 2^{31}) in U36 to yield the desired output frequency within the range of 3.75 mHz to 3.75 MHz. (Note that the circuit is actually capable of operating down to 3.5 mHz, but that the microprocessor will not accept entries for frequencies below 3.75 mHz.)

The following circuit groups are part of the PLL circuit: The PLL IC, loop filter, level translator and voltage-controlled oscillator (VCO). Operation of the entire loop will be discussed after these individual circuits are described.

Figure 4-22 is a simplified functional block diagram of the synthesizer circuit which shows the internal functions of the U35 PLL IC. U35 contains the reference oscillator, reference divider (÷ R), variable divider (÷ N), phase detector and internal registers and latches. The reference oscillator uses an external crystal (Y1) to generate a 6.144 MHz reference frequency. The reference divider is hard-wired (at pins 1, 2 and 18) for a division ratio of 6144. The 6.144 MHz reference frequency is divided by 6144, and the resulting 1 kHz reference is applied to one input of the internal phase detector. The variable divider (÷ N) is programmed by serial data at the pin 11 data input. This data is clocked

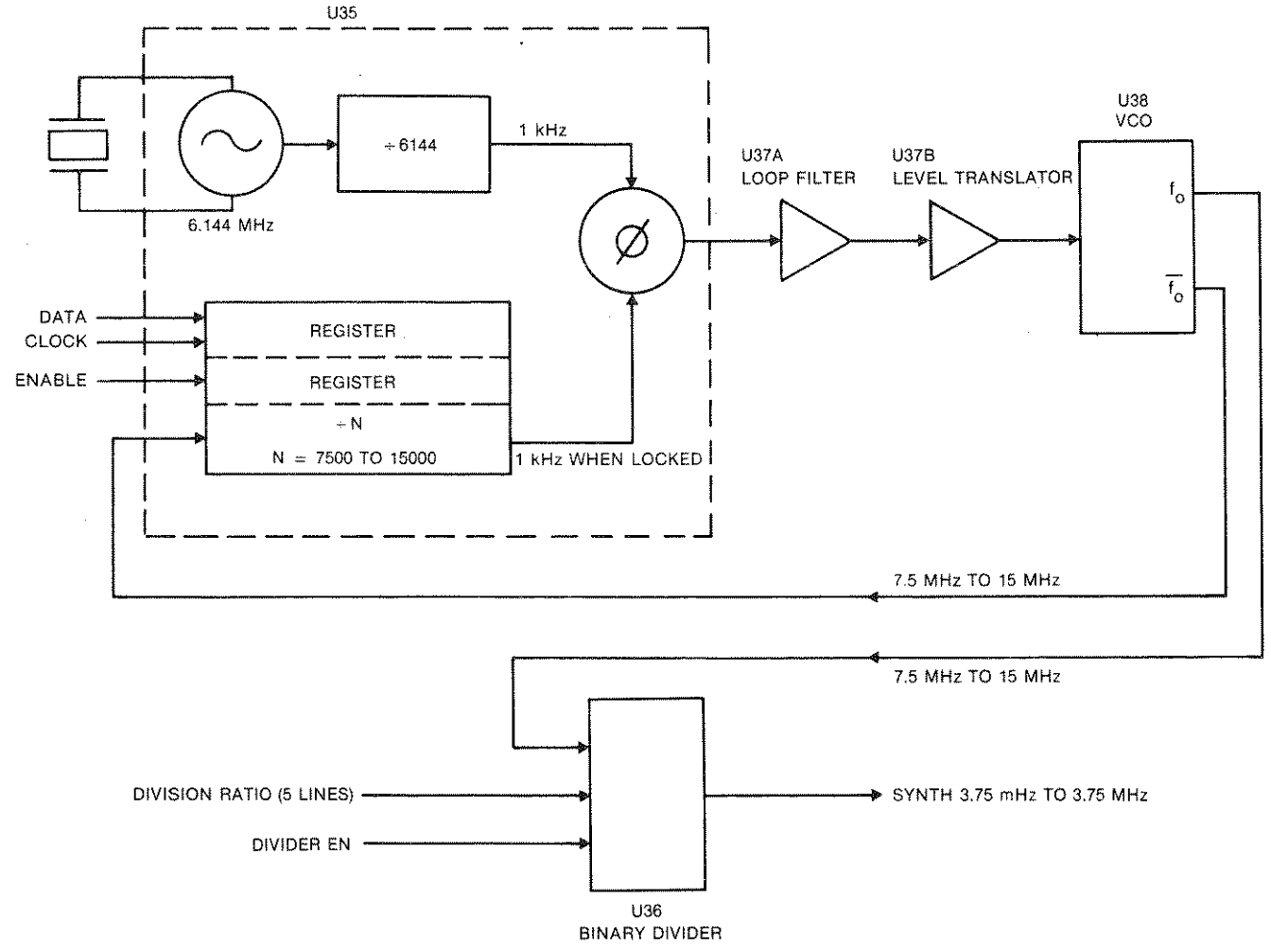


Figure 4-22. Simplified Functional Block Diagram, Synthesizer Circuit

into a 16-bit internal shift register by low-to-high transitions on the pin 10 clock line. The first two bits control internal switches, one of which controls the $\overline{\text{ARB MEM EN}}$ line. The remaining 14 bits are a binary representation of the ÷N division ratio, and are loaded most significant bit first. When the serial load is complete, a logic high on the pin 12 enable line latches the data in the shift register into the programmable ÷N counter. The IC is capable of a ÷N range of 3 to 16,838, but the range used in the Wavetek 275 is from 7500 to 15,000. The output of the ÷N counter is applied to the other input of the internal phase detector, and is also at 1 kHz when the loop is locked.

The internal phase detector is a digital tri-state device. It produces negative-going pulses when the variable frequency is greater than the reference frequency or is leading it in phase. Positive-going pulses are produced when the variable frequency is less than the reference frequency or is lagging in phase. The output is in a high-impedance state when the two signals are of equal frequency and phase.

Loop filter U37A converts the positive-going and negative-going pulses from the U35 phase detector to a steady dc frequency control voltage. The time constant of the filter is determined by C34 and the series value of R18 and R21. The time constant of the loop is therefore approximately 23.3 milliseconds. The damping of the loop is determined by R21. C33 is a high frequency bypass used to reduce noise in the filter. Voltage divider R19/R20 sets the voltage on U37A input pins 2 and 3 to 2.5 Vdc. The output of the loop filter U37A varies from approximately +8.0 Vdc to −4.0 Vdc.

Level translator U37B inverts the polarity of the U37A loop filter output and translates the voltage to the level required by the U38 voltage-controlled oscillator (VCO). The voltage at U37B input pins 5 and 6 is set to 2.1 Vdc by R23 and R24. Under normal operation the output at U37B pin 7 varies between +1.2 Vdc and +3.2 Vdc.

U38 is a TTL voltage-controlled oscillator (VCO). The output frequency is established by the value of C36 in combination with the voltage-sensitive inputs used for frequency control and frequency range. Output frequency increases with an increase in frequency control voltage and decreases with an increase in range control voltage. The output of the level translator (U37B) is applied to the frequency control input (pin 13) and a fixed voltage of approximately 1.7 Vdc from voltage divider R46/R47 is applied to the range control input (pin 2). R46 is a test-select part with a nominal value of 5kΩ.

The VCO provides two outputs; pin 6 provides the input to the variable divider (÷N) circuit in the U35 PLL IC, while pin 8 drives programmable divider U36. The VCO can be turned off by a logic high on the VCO OFF line (pin 8). R48 is a temperature compensation resistor provided on the board to permit a type 74LS628 IC to be substituted for the type 74LS624.

The PLL circuit as a whole operates in the following manner:

1. The VCO output is divided by the selected ratio (N) in the variable (÷N) divider. The divider output is applied to one input of the phase detector.
2. The phase detector compares the frequency and phase of the variable divider output to a fixed 1 kHz reference frequency from the reference (÷R) divider.
3. The phase detector, loop filter and level translator generate a dc VCO control voltage that changes as required to drive the VCO frequency to exactly N times the 1 kHz reference. When this occurs, the outputs of the reference (÷R) and variable (÷N) dividers are at the same frequency and in phase, and the loop is locked.
4. The loop will remain locked at this frequency until the variable division ratio N is changed.

In the Wavetek 275, the value of N is between 7500 and 15,000, giving a VCO output frequency range of 7.5 MHz to 15 MHz. The VCO output frequency is applied to programmable binary divider U36.

U36 is a programmable binary divider capable of dividing by a selected ratio within the range 2^2 to 2^{31}. The desired 2^n ratio is selected by applying the binary value of "n" to the "E" through "A" input control lines. "A" is the least significant bit, while "E" is the most significant bit. For example, for a division ratio of 2^2, input lines "E" through "A" would be programmed with the binary value "00010". A binary input of "11111" would select a ratio of 2^{31}. Programming a value less than 2 would inhibit the output and is never done.

A low on the DIVIDER EN line initializes the divider by clearing all of the internal flip-flops. The momentary low on this line is originated by the state machine circuit in the triggered arbitrary waveform modes to provide a stable and predictable timing relationship between the trigger pulse and resulting output waveform.

4.5.4 Arbitrary Waveform Generator

The arbitrary waveform generator creates the user-defined waveform from data stored in the internal

memory. In this discussion, the following circuit groups are considered to be part of the arbitrary waveform generator:

1. The PHASE ACCUMULATOR, which generates the address for the ARB RAM circuit.
2. The ARB RAM circuit, which stores digital data representing the point-by-point amplitude value of the arbitrary waveform.
3. The ARB OUT circuit, which converts the digital amplitude data to an analog waveform.
4. The STATE MACHINE, which controls the actions of the arbitrary waveform generator.
5. Other miscellaneous circuits, such as the microprocessor readback data selector and the ARB SYNC OUT amplifier.

A simplified functional block diagram of the arbitrary waveform generator is shown in figure 4-23. Waveform data from the microprocessor (via the data registers) is loaded into ARB RAM, and the desired RAM starting address is loaded into the counters in

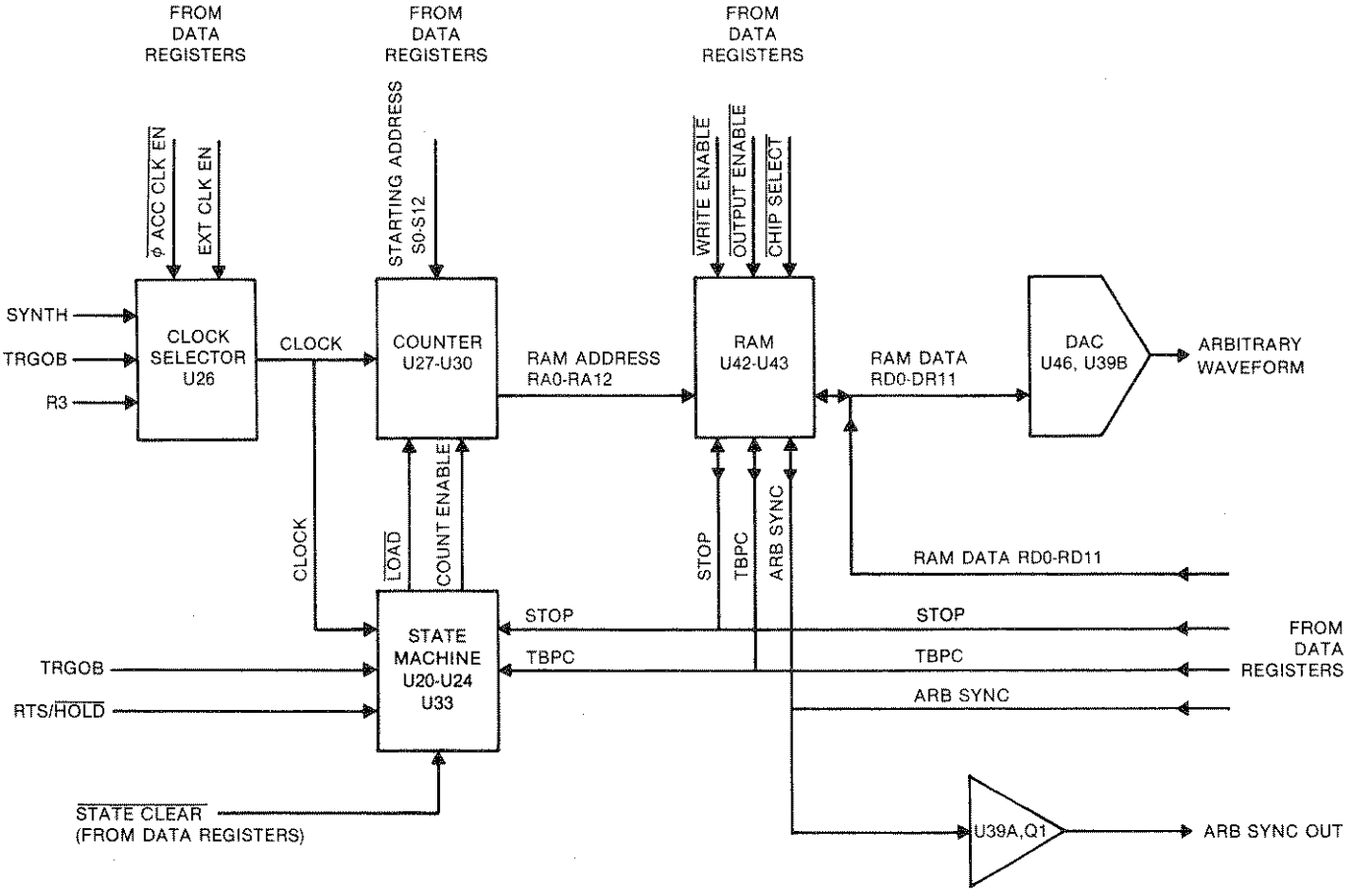


Figure 4-23. Simplified Functional Block Diagram, Arbitrary Waveform Generator

the PHASE ACCUMULATOR circuit. The counter, sequenced by the selected clock source, counts upwards from the starting address to increment the RAM address. At each RAM address, the previously stored data at that location is read out to the ARB OUT circuit. (The RAM also stores some control signals.) The RAM data is converted to an analog waveform by the ARB OUT circuit. The STATE MACHINE controls the actions of the arbitrary waveform generator, primarily the counter $\overline{\text{LOAD}}$ and COUNT ENABLE lines. Miscellaneous circuits select data to be read back to the microprocessor via the auxiliary board status flag line (J6 pin 20) and provide ARB SYNC OUT signal for the front panel connector.

4.5.4.1 Phase Accumulator

The phase accumulator circuit contains a clock selector circuit and a presettable binary counter. The counter is loaded with the desired ARB RAM starting address, then is sequenced by the selected clock source to increment the address. Both the clock selector circuit and the presettable counter are quite similar to the trigger selector and presettable counter in the burst counter circuit.

The clock select logic uses an 8-input multiplexer, U26, to select one of three clock sources. U26 selects the input that corresponds to the binary value on its three address lines. Only four of the eight inputs are used, and the most significant bit address line (pin 9) is permanently grounded. A binary address value of "000" selects the synthesizer output at pin 4. A value of "001" selects the TRGOB output of the burst counter trigger select logic. A value of "010" or "011" selects the R3 output of address decoder U18 at either pin 2 or pin 1, which are wired in parallel. The output from pin 5 is applied to the phase accumulator counter, the state machine counter and the state machine trigger circuit.

The R3 output of the address decoder is selected for clocking preload data into the counter, either for use as a starting point in the count cycle or for loading the ARB RAM address through the counter to the RAM for loading RAM data. The TRGOB output of the burst counter trigger select logic is selected for clocking the counter in the "single step" mode. The SYNTH output is selected for most other arbitrary waveform modes.

Preset data is loaded into the counter circuit (U27 through U30) on the positive edge of the clock pulse when the $\overline{\text{LOAD}}$ line (pin 9) is low. The counter is incremented by a positive-going transition on the clock line when the ENABLE inputs (pins 7 and 10) of the first counter stage (U27) are high. Both these inputs are originated by the STATE MACHINE circuit. The pin 10 ENABLE input of the remaining counter stages are connected to the CARRY output (pin 15) of the *preceeding* counter stage. The pin 7 ENABLE input of U28 through U30 are all connected to the carry output of the *first* counter stage.

4.5.4.2 ARB RAM Circuit

The ARB RAM circuit contains the Random Access Memories (U42 and U43), which store data values representing the point-by-point amplitude of the arbitrary waveform, and the parallel-to-serial shift registers (U40, U41, U44 and U45) which read the address and data values back to the microprocessor in serial form.

The RAMs can be either the standard 2048 word components (type 6116) or optional 8192 word components (type 6264). The 6264 is a 28 pin part; the 6116 has 24 pins. The circuit board contains a 28 pin socket, and the schematic shows the socket pin numbers. When the 24 pin part is used, it is inserted in the socket so that pin 1 of the RAM mates with pin 3 of the socket and pin 24 of the RAM mates with socket pin 26. Figure 4-24 shows the ARB RAM Pin Connections.

Note that when the smaller part is inserted in the larger socket in the manner just described, most of the pin functions line up properly. The exceptions are:

1. RAM address RA11 (pin 23 on the socket) is connected to the $\overline{\text{WRITE ENABLE}}$ line of the chip (pin 21.) The E5/E6/E7 jumper on the circuit board allows this socket pin to be connected to either the RA11 RAM address line or the R15 control line from the address decoder. The E5 to E6 connection of the jumper selects R15; the E6 to E7 connection selects the RA11 address line. THIS JUMPER MUST BE MOVED IF THE OPTIONAL LARGER RAM IS INSTALLED!
2. The second chip select line (CS2) on the socket (pin 26) is connected to the pin 24 supply voltage terminal (V_{cc}) of the chip. This doesn't matter in this circuit, because this pin is connected to V_{cc} on the circuit board.
3. Pin 28 on the socket (V_{cc}) is not connected. However, as previously mentioned, the chip receives V_{cc} from the CS2 socket pin (pin 26). Note that the smaller chip requires only *one* CHIP SELECT input.
4. Pin 27 on the socket ($\overline{\text{WRITE ENABLE}}$) is not connected. As previously mentioned, this control line (R15) is supplied to the smaller chip via the E5 to E6 jumper.

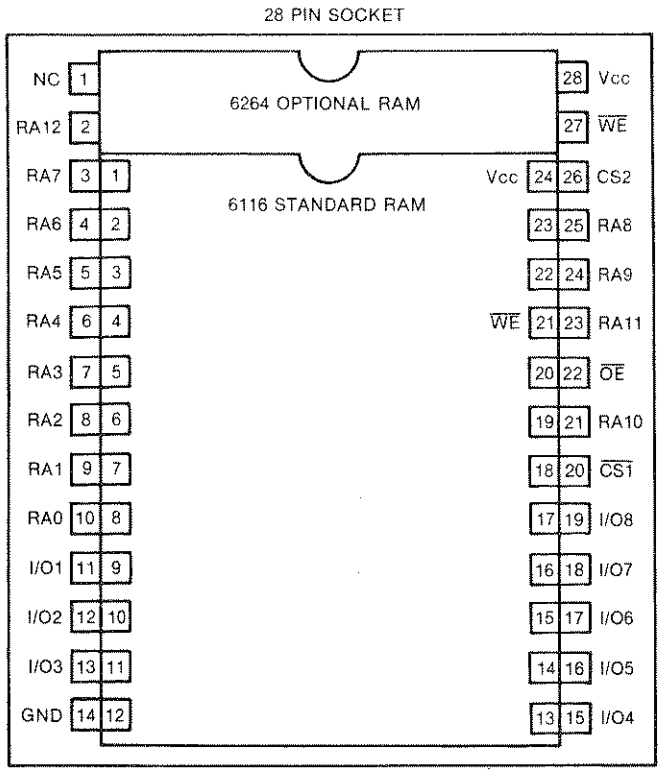


Figure 4-24. ARB RAM Pin Connections

5. RAM address line RA12 at socket pin 2 is not connected. The smaller RAM does not use address lines RA11 and RA12.

The remainder of the RAM circuit description will refer to the *socket* pin numbers marked on the schematic. Refer to figure 4-24, ARB RAM Pin Connections, as required for the pin numbers of the smaller standard 2048 word RAM.

Each RAM has one input for power, three control inputs, 11 or 13 address inputs (depending on RAM size), and eight data ports. Corresponding inputs of the two RAMs are wired in parallel, while the data ports remain separate.

V_{cc} power is applied to pins 28 and 26. The power is applied through a separate line from the microprocessor board, and has battery back-up for retaining the memory contents when the instrument is turned off.

The $\overline{\text{ARB MEM EN}}$ line controls the $\overline{\text{CHIP SELECT}}$ input of the two RAMs. This line is pulled low by the open-drain switch in the PLL IC (U35) to enable the RAM. When the instrument is turned off, the line is pulled high through R33 by the battery back-up voltage on the V_{cc} line.

The $\overline{\text{RAM EN}}$ line from the data registers is connected to the RAM $\overline{\text{OUTPUT ENABLE}}$ inputs. A logic low on this line allows the RAM to place data on the data I/O lines. A logic high disables the RAM output to prevent conflicting data when the RAM is being written to, or when the microprocessor is directly controlling these lines (via the data registers) during ramp-to-start operations. Whenever the RAM outputs are enabled, data registers U31 and U32 are disabled (their outputs are in a high-impedance state) by a logic high on the $\overline{\text{LATCH EN}}$ line.

The $\overline{\text{RAM WRITE ENABLE}}$ is controlled by the R15 line from the address decoder (U18 and U19). A momentary logic low on this line causes the data applied to the I/O ports to be written into the RAM at the location selected by the address lines.

The RAM address lines select a location for storage or retrieval of digital data. The location corresponds to the binary value of the logic levels on the address lines. RA0 is the least significant bit, while RA12 or RA10 (depending on RAM size) is the most significant bit. During arbitrary waveform generation, the address is incremented by the counter in the phase accumulator circuit at a rate determined by the selected clock source. During the data loading operation, each address is placed on the microprocessor data bus, latched into data registers U14 and U15, then clocked into the counter from the parallel load inputs by a clock pulse on the R3 line from address decoder U18. During this loading operation, the phase accumulator counter does *not* count.

The RAM data ports are bi-directional. The RAM places data on the lines when the $\overline{\text{RAM EN}}$ line is low. To read data into the RAM, the RAM output is disabled by a high on the $\overline{\text{RAM EN}}$ line, data registers U31 and U32 are enabled by a logic low on the $\overline{\text{LATCH EN}}$ line, and data from the registers is written into the selected RAM location by a momentary low on the R15 ($\overline{\text{WRITE ENABLE}}$) line. U42 contains waveform data bits RD0 through RD7, while U43 stores waveform data bits RD8 through RD11 and the control bits STOP, $\overline{\text{STOP}}$, ARB SYNC and TBPC. RAM data bits RD0 through RD11 are a binary representation of arbitrary waveform amplitude. RD0 is the Least Significant Bit (LSB); RD11 is the Most Significant Bit (MSB). These data lines control the Digital-to-Analog Converter (DAC) in the ARB OUT section. The $\overline{\text{STOP}}$ and STOP bits are low and high respectively at the last five addresses in the selected waveform block. The Trigger Break Point Control (TBPC) is high at addresses where a breakpoint has been programmed. The ARB

SYNC bit, which drives the front panel ARB SYNC OUT connector via the ARB SYNC OUT amplifier, is programmed by the operator at the last address executed. The STOP, $\overline{\text{STOP}}$ and TBPC bits control the state machine circuit.

Shift registers U40, U41, U44 and U45 read the RAM address and data values back to the microprocessor in serial form. The registers are loaded with address and data information by a logic low on the $\overline{\text{PARALLEL LOAD}}$ input (pin 1), which is controlled by the R8 line from the address decoder. Each positive-going transition of the CLOCK input (pin 2, connected to the R7 line) shifts one bit of data out of the Q7 output (pin 9) into the serial data input of the next register (pin 10). The output of the last register (U45) is connected to one of the inputs of the microprocessor readback data selector (U25).

4.5.4.3 ARB OUT Circuit

The ARB OUT circuit generates an arbitrary waveform voltage having an amplitude proportional to the binary value of the data on the RAM data lines RD0 through RD11. The three circuit groups within the ARB OUT circuit are the Digital-to-Analog Converter (DAC) U46, current-to-voltage converter U39B, and the slew rate switches (U47).

Digital-to-Analog Converter (DAC) U46 produces an output current that is proportional to both the analog reference input current and the binary value of the digital input. The reference input current is applied to pin 14, which is held at "virtual ground" by the internal reference amplifier. The reference current is equal to the reference voltage (+15V in this circuit) divided by the reference resistance (the series value of R34 and R35). The digital input is applied on data lines RD0 through RD11. RD0 is the least significant bit; RD11 is the most significant bit. Output current flows from pin 18 to the negative supply.

Maximum full-scale output current (with all the digital inputs turned "on") is:

$$I_{fs} = 4 \times (V_{ref}/R_{ref}) \times (4095/4096)$$

The non-inverting input of the reference amplifier (pin 15) is grounded through resistor R36. R36 is matched in value to R35 to minimize temperature drift.

Trimmer R34 allows a slight adjustment of the reference current to calibrate the positive peak of the arbitrary waveform.

Figure 4-25 shows a simplified schematic diagram of the current-to-voltage converter. U39B is an inverting amplifier with its inverting input at "virtual ground". The non-inverting input (pin 5) is grounded through a resistor, and the operational amplifier will produce whatever output voltage is required to maintain its inverting input (pin 6) at the same voltage. The DAC output current (shown as I_1 in this figure) flows from the virtual ground through the DAC to the negative supply. This current is proportional to the binary value of the DAC digital input. A fixed current (I_2 in this figure) flows from the +15V supply through R37 and R38 to the virtual ground. The third current to or from this point (shown as I_3) is the current through feedback resistor R39.

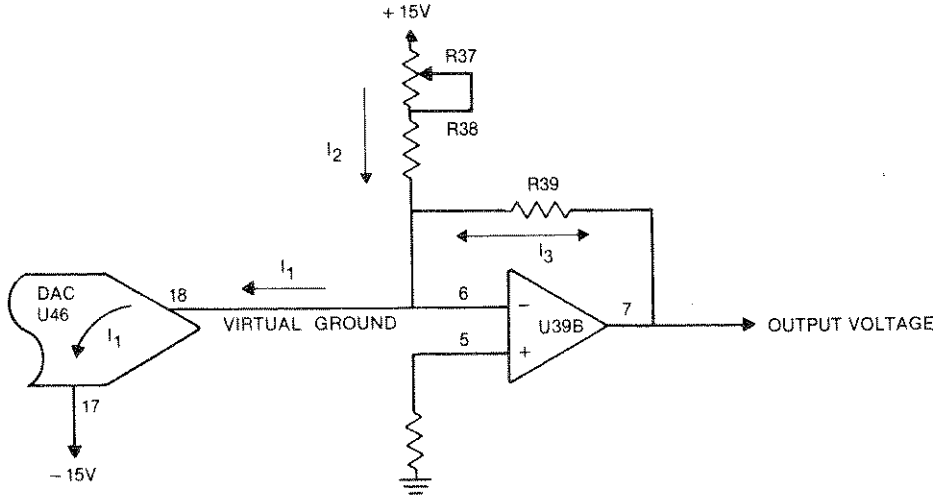


Figure 4-25. Simplified Schematic Diagram, Current-to-Voltage Converter

To keep its inverting input at "virtual ground", U39B must adjust its output voltage to a value that will make the sum of the currents flowing toward the virtual ground equal to the sum of the currents leaving the point. At low values of DAC current I_2 is greater than I_1, the current through R39 flows away from the virtual ground, and the amplifier output is negative. At high values of DAC current I_1 is greater than I_2, R39 current flows toward virtual ground, and amplifier output is positive. When I_1 is equal to I_2, I_3 is zero and the amplifier output voltage is zero.

Trimmer R37 allows a slight adjustment of the I_2 current to calibrate the negative peak of the arbitrary waveform.

U47A through U47B are FET switches that control the amount of filtering (and therefore the slew rate) of the arbitrary waveform. A logic low on the $\overline{\text{FSLEW}}$ control line turns on U47A and U47B, placing 100 pF capacitor C55 on the output line. A logic low on the $\overline{\text{SSLEW}}$ line turns on U47D and U47C, selecting a larger value capacitor (C56, 0.1 μF) to give more filtering and slower slew. When an arbitrary waveform function is not selected, all the switches are turned off.

4.5.4.4 State Machine Circuit

The state machine circuit controls the actions of the arbitrary waveform generator in the various arbitrary waveform modes, primarily by controlling the phase accumulator $\overline{\text{LOAD}}$ and COUNT ENABLE lines. The two major circuit groups within the state machine circuit are the state machine sequence control circuit and the state machine trigger circuit.

4.5.4.4.1 State Machine Trigger Circuit

The state machine trigger circuit generates the two signals that may be selected to enable the state machine sequencer. These signals are LATCHED TRIGGER and RTS (Ramp-to-Start). LATCHED TRIGGER is initiated by either the selected trigger source (TRGOB) of the RTS/HOLD input, and is high for one interval between phase accumulator clock pulses. A logic high on the RTS line is caused by a high on either the LATCHED TRIGGER line or the STOP bit in the ARB RAM. Note that these are logically OR functions, even though they are implemented with NAND gates.

The RTS/HOLD INPUT circuit protects NAND gate U20A from excessive voltages that may to applied to the RTS/HOLD input. Diodes CR1 and CR2 prevent the gate input from being pulled more than one diode drop above +5V or below ground. R8 holds this point at a logic low (one diode drop below ground) in the absence of an externally applied signal. R7 limits the diode and gate currents that may be caused by the external voltage. R7 is bypassed by a small value capacitor (C17) to improve frequency response at waveform edges.

U20A through U20C perform a logical OR operation to combine the trigger selector output (TRGOB) with the RTS/HOLD input. Each signal is applied through a NAND gate used as an inverter (U20A and U20B) and a small value coupling capacitor (C47 and C58) to the input of NAND gate U20C (also used as an inverter.) The input of U20C is held at a dc level of +2.5V by voltage divider R44 and R45. This voltage is a TTL logic high, just above the threshold point. A low-to-high logic transition on either the TRGOB line or the RTS/HOLD input causes a brief negative-going pulse at the U20C input. U20C inverts this pulse to drive the clock input of the trigger latch circuit.

NAND gate U20D performs a logical OR function to combine the LATCHED TRIGGER condition with the STOP condition to generate the RTS signal. To perform the logical OR operation with the NAND gate, the two gate input signals are applied as inverted complements $\overline{\text{LATCHED TRIGGER}}$ (from the trigger latch) and $\overline{\text{STOP}}$ (from the ARB RAM). These complementary signals are low when true, and a low on either input line will produce a logic high on the NAND gate RTS output line.

Flip-flops U21A and U21B hold the LATCHED TRIGGER line high for the interval between the next two clock pulses following the trigger pulse. This trigger latch circuit is enabled by a high on the $\overline{\text{TRIG INHIBIT}}$ line. The next trigger pulse at the U21A clock input latches the high from the $\overline{\text{TRIG INHIBIT}}$ line through to the U21A Q output, where it is applied to the U21B data input. The next clock pulse from the phase accumulator clock selector latches the high at the U21B data input through to the U21B Q output, where it is applied to the state counter circuit. The logic low at the U21B complementary $\overline{Q}$ output is applied back to the U21A direct $\overline{\text{RESET}}$ input, which resets the U21A Q output low and holds it low, overriding the U21A data and clock inputs. The U21A Q output going low applies a logic low on the U21B data input. The next U21B clock pulse latches the logic low at the U21B data input through to the U21B Q output, and the LATCHED TRIGGER line returns low. At the same time, the U21B $\overline{Q}$ output goes high, releasing the $\overline{\text{RESET}}$ input of U21A and allowing the next trigger pulse to clock U21A. Note that U21A will not change state when it is clocked if the $\overline{\text{TRIG INHIBIT}}$ is low.

The complementary $\overline{Q}$ output of U21B also is used as one of the inputs to U20D to generate the RTS signal. The complementary $\overline{Q}$ output of U21A drives the divider enable gate circuit to reset (clear) the binary divider in the synthesizer circuit.

The U21A $\overline{Q}$ output is capacitively coupled to one input of NAND gate U33D. This input (pin 12) is held just above the TTL logic high threshold by voltage divider R12/R13. The high-to-low transition of the U21A $\overline{Q}$ output causes a momentary logic low at this point, which causes a positive pulse at the U33D output if the SYNTH SYNC EN input is high. This positive pulse is gated through U33B if the SYNTH EN line is high, and inverted to cause a negative-going pulse on the DIVIDER EN line. This momentary low clears all the internal flip-flops in the synthesizer binary divider (U36), providing a stable delay between the trigger pulse and the leading edge of the synthesizer output waveform. The synthesizer divider is continuously enabled by a logic low on the SYNTH EN line in the continuous arbitrary waveform modes and in non-arbitrary modes that use the synthesizer output as an internal trigger. A logic high on the SYNTH EN line and a logic low on the SYNTH SYNC EN line disable the divider to reduce noise in the continuous or externally triggered non-arbitrary modes.

4.5.4.4.2 State Machine Sequence Control Circuit

The state machine sequence control circuit contains Read Only Memory (ROM) U24, which contains the stored control commands; state counter U23, which controls the least two significant ROM address lines; multiplexer U22, which selects the ENABLE source for the state counter; and the branch enable gates, U33A and U33C, which connect the burst counter output (BCA) to one of the state counter preload inputs in the gated and burst modes.

ROM U24 is controlled by five address lines. The three most significant bits of the address are controlled by mode select lines M_0 through M_2. The least two significant bits are controlled by the least significant bits of the state counter (U23). The address lines select a storage location within the ROM. At each storage location are eight data bits which are placed on the ROM output lines. These lines are:

Pin 1, the ENABLE line to the phase accumulator counter.

Pin 2, the $\overline{\text{LOAD}}$ line to the phase accumulator counter.

Pin 3, the $\overline{\text{TRIG INHIBIT}}$ line to the state machine trigger circuit.

Pin 4, the $\overline{\text{LOAD}}$ control to the state machine counter.

Pins 5 through 7, which control the state machine multiplexer, U22.

Pin 9, the HOLD readback line to the microprocessor via U25.

State counter U23 is a 4-bit binary presettable counter. The least significant preset input is controlled by the branch enable gates. All other preset inputs are grounded. The counter is clocked by the output of the phase accumulator clock selector U26, and enabled by the output of multiplexer U22. The counter $\overline{\text{LOAD}}$ line is controlled by one of the U24 ROM outputs. When the line is low, the counter is prevented from counting, and will latch the preset data through to the outputs on the leading edge of the next clock pulse. The least two significant output bits control the two least significant bits of ROM U24; the other two counter outputs are not used. The counter may be cleared by a low on the STATE CLEAR line.

Multiplixer U22 selects one of 8 inputs to apply to the state counter ENABLE line. The input selected is determined by the binary value of the bits on the three control lines. Pin 9 is the most significant bit; pin 11 is the least significant bit. Two of the eight inputs are not identified by name on the schematic diagram, yet we will be referring to them frequently in the following text and state diagrams. These are the Q output of U21B (pin 9), which we will call LATCHED TRIGGER, and the output (pin 11) of NAND gate U20D, which we will refer to as RTS. Table 4-2 lists the binary value of the control line bits, the name of the input selected, and the conditions which will enable the state counter to count.

Operation of the state counter is explained by the state diagram in figures 4-26 through 4-33. In each diagram, the circle represents the circuit states that may occur in the selected mode of operation. Each state is numbered starting at zero, and the number of permissible states for each mode will be between one and four, depending on the mode selected. The state numbers on any state diagram are not related to the state numbers on a diagram for a different mode. For example, state zero in the continuous mode is *not* the same as state zero in the triggered mode.

The paths between states are represented by arrows, and the arrow is labelled with the event that causes the transition. It should be remembered that except for $\overline{\text{STATE CLEAR}}$, each transition *requires a clock pulse* in addition to the specified event.

For each state, the figure also shows the binary value

Table 4-2. Selectable State Counter Enable Inputs

Binary Value of U22 Control Inputs	U22 Input Selected	Conditions Under Which State Counter U23 Is Enabled to Count
0	RTS	When triggered or when at end of arbitrary waveform.
1	STOP	When at end of arbitrary waveform.
2	TBPC	When at programmed waveform breakpoint.
3	+5V	Always.
4	Latched Trigger	When triggered.
5	Ground	Never.
6	Ground	Never.
7	Ground	Never.

of the ROM input, the binary value of the ROM output, and the action that each ROM output bit will cause. The three most significant bits of the ROM input are supplied by the mode control lines; the last two bits from the state counter. The ROM output bits are factory programmed at each address location to cause the desired control actions in that state. An "X" in the binary ROM output number indicates a "don't care" condition; in that state the bit will have no effect and it doesn't matter whether it is a "1" or a "0". All binary numbers are listed most significant bit (MSB) first.

The state diagrams are arranged in ascending order of ROM address. The first state diagram will be discussed in great detail; explanation of the remaining state diagrams will be more concise.

In the Continuous (0) or Single-Step (8) modes, a "000" on the mode control lines and "00" from the state counter gives a ROM input address of "00000". The information programmed in the ROM at this location is a binary "X0011011".

The first bit of the ROM output data is the HOLD readback line to the microprocessor. The value of this bit is not significant in the continuous or single-step modes, as the microprocessor looks at the HOLD line only in the RTS modes.

The next three bits select the logic line that enables the state machine counter. "001" selects the STOP bit from the ARB RAM.

The fifth bit controls the state counter $\overline{\text{LOAD}}$ line. A "1" on this line prevents the counter from loading.

Bit 6 is the $\overline{\text{TRIG INHIBIT}}$ line. A logic "0" inhibits the trigger circuit in modes and states where the trigger circuit is not required. This prevents an externally applied signal from accidentally resetting the binary divider in the synthesizer circuit via the DIVIDER EN line.

The seventh bit places a "1" on the phase accumulator counter $\overline{\text{LOAD}}$ line to prevent the next clock pulse from loading the counter.

The last bit of the ROM output places a "1" on the phase accumulator counter ENABLE line, to enable the counter to increment when clocked.

Thus, in state 0 of the continuous and single step modes, clock pulses from the phase accumulator clock selector (U26) increment the phase accumulator counter, but the state counter is inhibited from counting by the logic "0" from the STOP output of the ARB RAM.

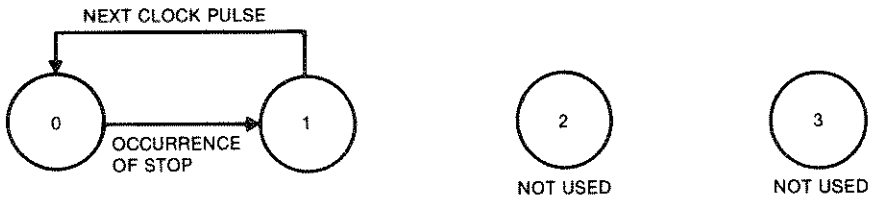
The phase accumulator counter increments the ARB RAM address to create the programmed waveform. At the end of the arbitrary waveform, the STOP bit (which is programmed into the ARB RAM by the front panel START/STOP key or the equivalent remote control command) is high, enabling the state counter. The next clock pulse advances the state counter to state 1, which results in a ROM input address of "00001". The ROM data at this location is "XXXX000X".

The first ROM output bit (HOLD line) is still irrelevant for the same reason as in state 0. The next three bits, which select the source of the state counter ENABLE signal are not significant because bit 5, a "0", instructs the state counter to $\overline{\text{LOAD}}$, which will inhibit counting. The trigger is still inhibited by a "0" on the $\overline{\text{TRIG INHIBIT}}$ line, for the same reason as in the last state. Bit 7 places a "0" on the phase accumulator $\overline{\text{LOAD}}$ line. The last bit, which controls the phase accumulator ENABLE line, has no effect, as the low on the $\overline{\text{LOAD}}$ line automatically inhibits counting.

The preload data present at the input of the state counter is "0000". As previously mentioned, the three most significant bits are hard-wired to ground. The

remaining bit is high only in the burst or gated modes when the burst counter output line (BCA) is high. The next clock pulse will load this data ("0000") into the state counter and will also load preset data S0-S12 into the phase accumulator counter. The state counter has now returned to state 0.

In the gated and burst modes, the BRANCH EN line is high, enabling the branch enable gates. If the output line of the burst counter circuit (BCA) is high, a logic "0001" will be loaded into the state counter, returning the circuit to state 1. If the BCA line is low, the counter preload data is "0000", and the state machine returns



ROM Input	00000	00001		
ROM Output	X0011011	XXXX000X		
HOLD Readback	X = "Don't Care"	X = Don't Care"		
State Counter Enable Source	001 = STOP	XXX = Don't Care"		
State Counter $\overline{\text{LOAD}}$	1 = Don't Load	0 = Load		
$\overline{\text{TRIG INHIBIT}}$	0 = Inhibit	0 = Inhibit		
Phase Acc. $\overline{\text{LOAD}}$	1 = Don't Load	0 = Load		
Phase Acc. COUNT	1 = Count	X = "Don't Care"		

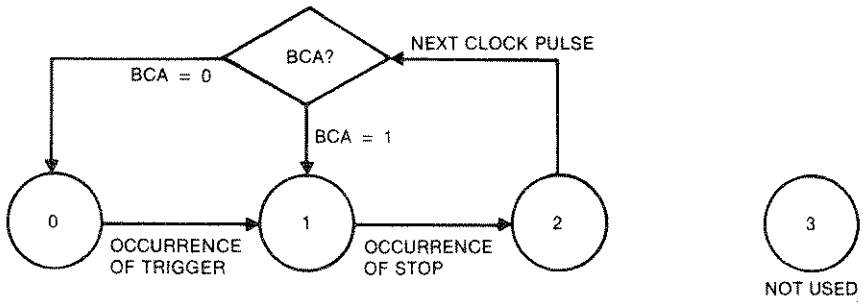
Figure 4-26. State Diagram for CONTINUOUS (0) and SINGLE STEP (8) Modes.

In state 0 of the Triggered (1), Gated (2) and Burst (3) modes the trigger circuit is enabled and the phase accumulator counter $\overline{\text{LOAD}}$ line is low. The state counter is disabled until it receives a logic high from the LATCHED TRIGGER line. When this line goes high, the state counter is enabled and the next clock pulse will advance the counter to state 1. This clock pulse will also load the starting address of the arbitrary waveform into the phase accumulator counter.

In state 1 the trigger circuit is inhibited and the phase accumulator is enabled. The phase accumulator counter increments the ARB RAM address until the STOP bit from the ARB RAM goes high. When this occurs, the state counter is enabled and advances to state 2 at the next clock pulse.

In state 2, the $\overline{\text{LOAD}}$ inputs of both the phase accumulator counter and the state counter are enabled, and the next clock pulse will reload the state counter. to state 0. The same clock pulse that clocks the state counter out of state 2 will also reload the phase accumulator counter with the starting address of the arbitrary waveform. If the state machine returns to state 1, the programmed arbitrary waveform is repeated. If the state counter returns to state 0, it waits for another trigger pulse.

In the Triggered Arb with Hold on Break Point (10) mode, the state machine prevents the phase accumulator from counting until the state counter is enabled by a logic high on the LATCHED TRIGGER line. As soon as the state counter is enabled, the next clock pulse advances it to state 1 and the phase accumulator counter is allowed to increment the ARB RAM address. The occurrence of a logic high on the Trigger Break Point Control (TBPC) line from the ARB RAM allows the state counter to be clocked to state 2, which again inhibits the phase accumulator counter and enables the state counter $\overline{\text{LOAD}}$ line. The next



ROM Input	00100	00101	00110	
ROM Output	X100110X	X0011011	XXXX010X	
HOLD Readback	X = "Don't Care"	X = Don't Care"	X = "Don't Care"	
State Counter Enable Source	100 = LATCHED TRIGGER	001 = STOP	XXX = "Don't Care"	
State Counter $\overline{\text{LOAD}}$	1 = Don't Load	1 = Don't Load	0 = Load	
$\overline{\text{TRIG INHIBIT}}$	1 = No Inhibit	0 = Inhibit	1 = No Inhibit	
Phase Acc. $\overline{\text{LOAD}}$	0 = Load	1 = Don't Load	0 = Load	
Phase Acc. COUNT	X = "Don't Care"	1 = Count	X = "Don't Care"	

Figure 4-27. State Diagram for TRIGGERED (1), GATED (2) and BURST (3) Modes.

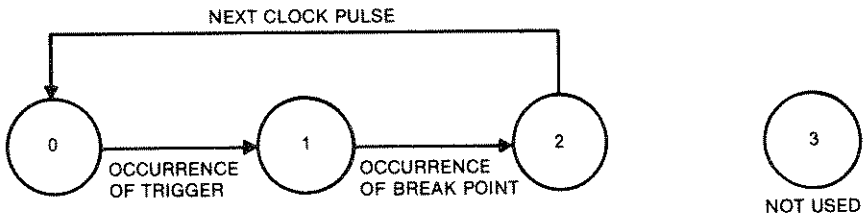
clock pulse reloads the state counter with zeros, which returns it to state 0 to await another trigger pulse.

NOTE

The start and stop addresses are not used by the sequence control circuit in this mode. Each time the Wavetek 275 is triggered the output waveform will run until a break point occurs. The ARB memory sequences through its full memory range and then "wraps around" to the beginning to continue. Branching from one break point to another can be accomplished by changing from mode 10 (Triggered Arb with Hold on Break Point) to mode 9 (Examine) and immediately back to mode 10. This forces the ARB to the current start address, and it will continue from that point on the next trigger. If desired, a new start address can be programmed while the instrument is temporarily set to mode 9.

In the Triggered Arb with Ramp-to-Start (4) mode, the state machine waits in state 0 until the state counter is enabled by a high on the LATCHED TRIGGER line. The next clock pulse then loads the phase accumulator counter and advances the state counter to state 1. In state 1, the phase accumulator counter is allowed to increment until the state counter is enabled by a high on the RTS line. The RTS signal is a logical OR combination of the external signal at the RTS/HOLD front panel connector OR the TRGOB output of the U1 trigger selector in the burst counter circuit (latched by U21) OR the STOP signal from the ARB RAM. Whichever signal occurs first will enable the state counter to be clocked to state 2, removing the enable to the phase accumulator counter. In state 2 the state counter and the phase accumulator counter are both inhibited from either counting or loading, and the microprocessor is alerted by a logic "1" on the HOLD line. The microprocessor then takes direct control of RAM data lines RD0 through RD11 to ramp the arbitrary waveform back to the starting amplitude. At the end of the ramp-to-start operation, the microprocessor clears the state counter to state 0 via the $\overline{\text{STATE CLEAR}}$ line.

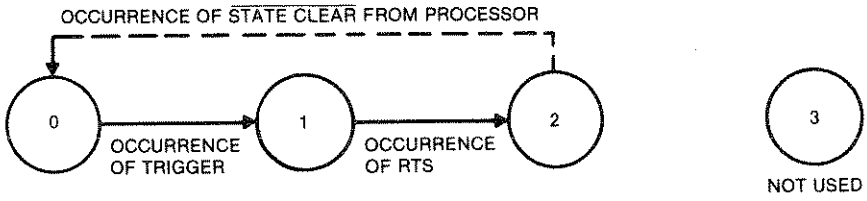
The Triggered Arb with Hold and Triggered Ramp-to-Start (5) mode is similar to the Triggered Arb with Ramp-to-Start (4) mode, with the addition of a



NOTE: ARB memory sequences through full memory range, stopping only at programmed break points, then "wraps around" to the beginning to continue.

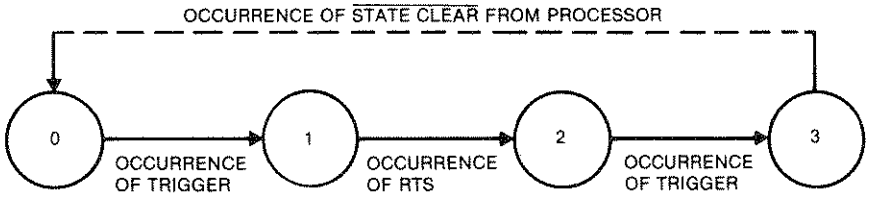
ROM Input	01000	01001	01010	
ROM Output	X1001110	X0101011	XXXX0010	
HOLD Readback	X = "Don't Care"	X = Don't Care"	X = "Don't Care"	
State Counter Enable Source	100 = LATCHED TRIGGER	010 = TBPC	XXX = "Don't Care"	
State Counter $\overline{\text{LOAD}}$	1 = Don't Load	1 = Don't Load	0 = Load	
$\overline{\text{TRIG INHIBIT}}$	1 = No Inhibit	0 = Inhibit	0 = Inhibit	
Phase Acc. $\overline{\text{LOAD}}$	1 = Don't Load	1 = Don't Load	1 = Don't Load	
Phase Acc. COUNT	0 = Don't Count	1 = Count	0 = Don't Count	

Figure 4-28. State Diagram for TRIGGERED ARB WITH HOLD ON BREAK POINT (10) Mode.



ROM Input	01100	01101	01110	
ROM Output	0100110X	00001111	11111010	
HOLD Readback	0 = Not On Hold	0 = Not On Hold	1 = On Hold	
State Counter Enable Source	100 = LATCHED TRIGGER	000 = RTS	111 = Ground (Don't Ground)	
State Counter $\overline{\text{LOAD}}$	1 = Don't Load	1 = Don't Load	1 = Don't Load	
$\overline{\text{TRIG INHIBIT}}$	1 = No Inhibit	1 = No Inhibit	0 = Inhibit	
Phase Acc. $\overline{\text{LOAD}}$	0 = Load	1 = Don't Load	1 = Don't Load	
Phase Acc. COUNT	X = "Don't Care"	1 = Count	0 = Don't Count	

Figure 4-29. State Diagram for TRIGGERED ARB WITH RAMP-TO-START (4) Mode.



ROM Input	10000	10001	10010	10011
ROM Output	0100110X	00001111	01001110	11111010
HOLD Readback	0 = Not On Hold	0 = Not On Hold	0 = Not On Hold	1 = On Hold
State Counter Enable Source	100 = LATCHED TRIGGER	000 = RTS	100 = LATCHED TRIGGER	111 = Ground (Don't Count)
State Counter $\overline{\text{LOAD}}$	1 = Don't Load	1 = Don't Load	1 = Don't Load	1 = Don't Load
$\overline{\text{TRIG INHIBIT}}$	1 = No Inhibit	1 = No Inhibit	1 = No Inhibit	0 = Inhibit
Phase Acc. $\overline{\text{LOAD}}$	0 = Load	1 = Don't Load	1 = Don't Load	1 = Don't Load
Phase Acc. COUNT	X = "Don't Care"	1 = Count	0 = Don't Count	0 = Don't Count

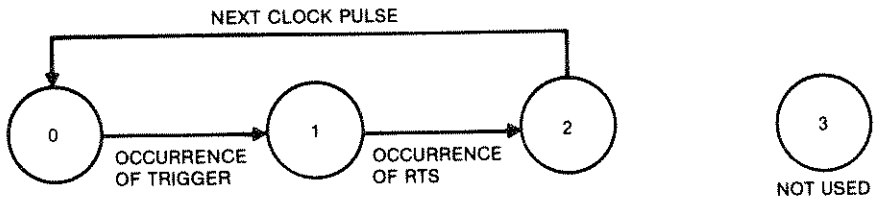
Figure 4-30. State Diagram for TRIGGERED ARB WITH HOLD AND TRIGGERED RAMP-TO-START (5) Mode.

"holding" state that requires an additional trigger pulse to initiate the ramp-to-start operation. In state 2 the phase accumulator counter is inhibited from either counting or loading, and the LATCHED TRIGGER line is selected for enabling the state counter. When the LATCHED TRIGGER line goes high, the next clock pulse advances the state counter to state 3, and the microprocessor is signalled to begin the ramp-to-start operation via a "1" on the HOLD readback line.

In state 0 of the Triggered Arb with Reset (6) mode, the state machine holds the phase accumulator counter $\overline{\text{LOAD}}$ line low, and the state counter is disabled by a low on the LATCHED TRIGGER line. As soon as the LATCHED TRIGGER line goes high, the next clock pulse will load the starting address of the arbitrary waveform into the phase accumulator counter and advance the state counter to state 1. In state 1, the state counter is disabled by a low on the RTS line, but the phase accumulator counter is enabled, and increments the ARB RAM address. A logic high on the RTS line (caused by an RTS/$\overline{\text{HOLD}}$ input from the front panel connector, a trigger pulse, or a high on the STOP bit from the ARB RAM) again enables the state counter, and it advances to state 2 on the next clock pulse. In state 2 the phase accumulator counter is inhibited and the state counter $\overline{\text{LOAD}}$ line is enabled, and the next clock pulse reloads the state counter with zeros to return it to state 0.

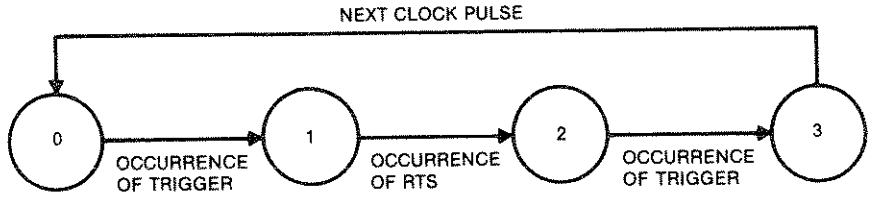
The Triggered Arb and Hold with Triggered Reset (7) mode is similar to the Triggered Arb with Hold and Triggered Ramp-to-Start (5) mode, except that in the last state (state 3), the $\overline{\text{LOAD}}$ line to the state counter is low, and the next clock pulse will reload the counter.

In state 0, the phase accumulator $\overline{\text{LOAD}}$ line is low, which inhibits counting. The state counter waits for a high on the LATCHED TRIGGER line, then advances to state 1 on the next clock pulse. (This clock pulse also reloads the phase accumulator counter.) In state 1 the phase accumulator counter is enabled, and the state counter waits for a STOP or LATCHED TRIGGER signal via the RTS line. A high on the RTS line allows the state counter to be clocked to state 2. In state 2, the phase accumulator counter is inhibited and the state counter waits for a high on the LATCHED TRIGGER line. A trigger pulse enables the state counter to advance to state 3 on the next clock pulse. In state 3 the $\overline{\text{LOAD}}$ line to the state counter is held low, and the next clock pulse reloads the counter, returning the state machine to state 0.



ROM Input	10100	10101	10110	
ROM Output	X100110X	X0001111	XXXX0110	
HOLD Readback	X = "Don't Care"	X = "Don't Care"	X = "Don't Care"	
State Counter Enable Source	100 = LATCHED TRIGGER	000 = RTS	XXX = "Don't Care"	
State Counter $\overline{\text{LOAD}}$	1 = Don't Load	1 = Don't Load	0 = Load	
$\overline{\text{TRIG INHIBIT}}$	1 = No Inhibit	1 = No Inhibit	1 = No Inhibit	
Phase Acc. $\overline{\text{LOAD}}$	0 = Load	1 = Don't Load	1 = Don't Load	
Phase Acc. COUNT	X = "Don't Care"	1 = Count	0 = Don't Count	

Figure 4-31. State Diagram for TRIGGERED ARB WITH RESET (6) Mode.



ROM Input	11000	11001	11010	11011
ROM Output	X100110X	X0001111	X1001110	XXXX0010
HOLD Readback	X = "Don't Care"	X = "Don't Care"	X = "Don't Care"	X = "Don't Care"
State Counter Enable Source	100 = LATCHED TRIGGER	000 = RTS	100 = LATCHED TRIGGER	XXX = "Don't Care"
State Counter $\overline{\text{LOAD}}$	1 = Don't Load	1 = Don't Load	1 = Don't Load	0 = Load
$\overline{\text{TRIG INHIBIT}}$	1 = No Inhibit	1 = No Inhibit	1 = No Inhibit	0 = Inhibit
Phase Acc. $\overline{\text{LOAD}}$	0 = Load	1 = Don't Load	1 = Don't Load	1 = Don't Load
Phase Acc. COUNT	X = "Don't Care"	1 = Count	0 = Don't Count	0 = Don't Count

Figure 4-32. State Diagram for TRIGGERED ARB WITH TRIGGERED RESET (7) Mode.

ROM Input	11100			
ROM Output	XXXX000X			
HOLD Readback	X = "Don't Care"			
State Counter Enable Source	XXX = "Don't Care"			
State Counter $\overline{\text{LOAD}}$	0 = Load			
$\overline{\text{TRIG INHIBIT}}$	0 = Inhibit			
Phase Acc. $\overline{\text{LOAD}}$	0 = Load			
Phase Acc. COUNT	X = "Don't Care"			

Figure 4-33. State Diagram for EXAMINE (9) Mode.

The Examine (9) mode uses only one state, state 0. In this mode, logic lows on the $\overline{\text{LOAD}}$ inputs inhibit both the state counter and phase accumulator counter, and the selected ARB RAM address is clocked through the phase accumulator counter to the ARB RAM. The microprocessor then reads back the ARB RAM address and data in serial form through the microprocessor readback data selector, U25.

4.5.4.5 Other Arbitrary Waveform Generator Circuits

The remaining circuits within the arbitrary waveform generator are the ARB SYNC OUT circuit and the microprocessor readback data selector.

4.5.4.5.1 Microprocessor Readback Data Selector

The microprocessor readback data selector, U25, is an 8-input multiplexer that selects one of four data inputs for application to the μP INFO line. The input selected is determined by the binary value on control lines DS2-DS0. Table 4-3 lists the control inputs for each data source, and also gives an explanation of the source.

4.5.4.5.2 ARB SYNC OUT Circuit

The ARB SYNC OUT circuit amplifies the ARB SYNC bit from the ARB RAM for application to the front panel ARB SYNC OUT connector. The circuit is a non-inverting operational amplifier (U39A) and emitter-follower (Q1). Circuit gain is set to 2 by resistors R30 and R28. Resistor R32 sets the output impedance at the connector to 600Ω.

Before suspecting this circuit of malfunction, verify that an ARB SYNC pulse has been programmed somewhere between the arbitrary waveform START and STOP points. If the ARB SYNC pulse is inadvertently programmed after the STOP point, the ARB SYNC OUT pulse will never occur.

4.5.5 Power Distribution

The +15V, −15V and +5V dc power for most of the circuits enters the board at the J17 AUXILIARY POWER CONNECTOR. Each line is filtered by ferrite

Table 4-3. Microprocessor Readback Data Selector Control Inputs

DS2-DS0 Binary Value	Selected Data Source	Explanation
000	HOLD	From state machine ROM; in ramp-to-start modes logic high signals microprocessor to begin ramp-to-start operation. Not significant in other modes.
001	DATA SERIAL OUT	Serial readback of ARB RAM data and address from shift registers in ARB RAM circuit.
010	N/C	No connection.
011	BCA	Logic high in BURST mode indicates that burst counter is active. In non-burst modes, the signal is a copy of the TRGOB output of the trigger select logic (U1).
100	JUMP	Connected to E6 of the jumper terminals in the ARB RAM circuit; informs the microprocessor whether the standard or optional larger RAM is installed.
101	N/C	No connection.
110	N/C	No connection.
111	N/C	No connection.

bead inductors FB1-FB3 and capacitors C1-C3. Additional filtering is provided by small value bypass capacitors at various locations on the board.

The +5V power for the ARB RAM is supplied by a separate line from pin ± 19 of the J16 DIGITAL INTERFACE CONNECTOR. This line is automatically switched over to the backup battery on the microprocessor board when the instrument is turned off.

SECTION 5
CALIBRATION

5.1 FACTORY REPAIR

Wavetek maintains a Customer Service department. If an instrument is returned to Wavetek for repair or calibration, a detailed description of the specific problem should be attached to minimize turn around time.

5.2 CALIBRATION

Table 5-1 lists the equipment required to perform the calibration procedures in table 5-2.

The setup for each calibration step and a displayed operator cue are contained within the firmware.

Table 5-1. Calibration Test Equipment

Instrument	Suggested Model	Comment
Digital Voltmeter	Fluke 8050A	DC accuracy: 0.01% AC accuracy (true rms): 0.2%
Distortion Analyzer		Frequency range: 5 Hz to 100 kHz Distortion measurement: 0.1 to 100%
Frequency Counter		Frequency range: 0.5 Hz to 13 MHz Frequency accuracy: ±1 ppm
Oscilloscope Main frame Plug-in Vertical Amplifier Dual Time Base Sampler	 Tektronix 7904 Tektronix 7A26 Tektronix 7B53A Tektronix 7S14	 Bandwidth: dc to 500 MHz Bandwidth: dc to 200 MHz Sensitivity: 5 mV to 5V/div Input impedance: 1 MΩ Time/div: 5 ns to 5 s Bandwidth: dc to 1 GHz
Terminations	Tektronix 011-0129-00 Tektronix 011-0049-01	50Ω ± 0.1%, 2W 50Ω ± 2.0%, 2W
Attenuator	Tektronix 011-0059-02	10X, 50Ω, 2W
Coax Cable	Tektronix 012-0057-01	50Ω, 3 ft length

Amplitude and Offset calibration requires a 50 ± 0.05Ω termination. If a precision termination is not available, a correction factor (K) can be derived, which can be used to calculate a normalized calibration value.

K is derived as follows:

$$K = \frac{R + 50}{2R}$$, where R is the value of the terminator used.

To calculate a normalized calibration value, divide the value from Desired Results by K. Or, multiply the measurement by K, which should equal the value from Desired Results.

Calibration steps and cues can be accessed by pressing RCL 1001 EXEC, RCL 1002 EXEC, etc. for each step of the calibration procedure in table 5-2. Calibration points are shown in figures 5-1 through 5-3.

Periodic calibration is needed because of component aging, which depends on instrument on-time and environment. Use six months as an initial calibration period. If possible keep records of the parameter values and modify the time between calibration if the records indicate.

NOTE

The completion of the calibration procedure returns the instrument to correct alignment.

CALIBRATION LIMITS AND TOLERANCES ARE NOT INSTRUMENT SPECIFICATIONS

Instrument specifications are given in Section 1 of this manual.

Before beginning the calibration procedure, verify the correct placement of the following jumpers located on the function generator board (ref: figure 5-2):

VCG Jumper	E9 to E10
Trig In Jumper	E13 to E14

To gain access to the Microprocessor/Power Supply board (steps 1 to 3), remove the bottom cover (2 screws).

To gain access to the Function Generator (steps 4 to 28) and Arbitrary Waveform Generator boards (steps 29 and 30), remove the top cover (2 screws), next remove the two screws on the right of the Arbitrary Waveform Generator board, and lift the Arbitrary Waveform Generator board up to access Function Generator board adjustments(the Arbitrary Waveform Generator board pivots on the left side).

NOTE

1. *EXEC (Execute), required to implement parameter value change, has been omitted from the calibration procedure.*
2. *Each step (RCL 1001, 1002 etc) also can be incremented and executed by using the cursor control (ref: paragraph 3.4.1.3).*
3. *When using the Function Output BNC, it must be terminated with a 50Ω termination.*

Table 5-2. Calibration Procedure

NOTE: Open column indicates previous entry remains applicable

Step	Check	Tester	Cal Point	Program	Adjust	Desired Results	Remarks
			NOTE: Steps 1 through 3 are power supply adjustments (see figure 5-1).				
1	+15V SUPP, R39	DVM (dc mode)	J3-1, TP2 (GND)	RCL 1001	R39	+15 ± .002 Vdc	
2	−15V SUPP, R47		J3-5, TP2 (GND)	RCL 1002	R47	−15 ± .002 Vdc	
3	−10.24V REF, R16		TP1, TP2 (GND)	RCL 1003	R16	−10.24 ± .002 Vdc	
			NOTE: Steps 4 through 28 are function generator adjustments (see figure 5-2)				
4	NODE BAL, R99	DVM (dc mode)	J23-9, TP1 (GND)	RCL 1004	R99	0 ± 1.0 Vdc	
5	TRI BALANCE, R60		J23-7, TP1 (GND)	RCL 1005	R60	0 ± .002 Vdc	
6	VCG ZERO, R11		VCG IN BNC (Front Panel)	RCL 1006	R11	0 ± .001 Vdc	
7	HI SYMM, R23	Oscilloscope	FUNC OUT (terminate with 50Ω)	RCL 1007	R23	50% Duty Cycle ±0.5 μs	
8	LO SYMM, R15			RCL 1008	R15	50% Duty Cycle ±0.5 μs	
9	LO FREQ, R12	Frequency Counter		RCL 1009	R12	10 ± .1 Hz	
10	HI FREQ, R8			RCL 1010	R8	999 ±1.0 Hz	Steps 9 and 10 interact; repeat if necessary.

Table 5-2. Calibration Procedure (Continued)

Step	Check	Tester	Cal Point	Program	Adjust	Desired Results	Remarks
11	1 MHz, C43	Frequency Counter	FUNC OUT (terminate with 50Ω)	RCL 1011	C43	1 ± .001 MHz	After making the initial adjustments in steps 11 and 12, record the frequency in each step. Place the arbitrary waveform generator board in the operating position. Record the new frequency for each step. Note the difference in frequency. Lift up the arbitrary waveform generator board. Increase the frequency by the frequency difference. Repeat steps 11 and 12 if necessary.
12	9.99 MHz, R45			RCL 1012	R45	9.99 ± .01 MHz	
13	100 kHz, C45			RCL 1013	C45	100 ± .1 kHz	
14	999 kHz, R46			RCL 1014	R46	999 ± 1 kHz	Steps 13 and 14 interact; repeat if necessary.
15	10 Hz SYM, R117	Oscilloscope		RCL 1015	R117	Symmetry 50% ± .1%	
16	0.999 Hz, R105	Frequency Counter		RCL 1016	R105	.999 ± .001 Hz	
17	99.9 Hz, R112			RCL 1017	R112	99.9 ± .1 Hz	
18	SINE DIST	Distortion Analyzer		RCL 1018	R142 R154 R157 R255	< .3%	Adjust for minimum distortion.
19	MULT BAL, R241	Oscilloscope		RCL 1019	R241	≤ .070 Vp-p	Adjust for minimum amplitude variation. Steps 18 and 19 interact; repeat if necessary.
20	OFFSET 0, R237	DVM (dc mode)	FUNC OUT (terminate with .1% 50Ω load)	RCL 1020	R237	0 ± .005 Vdc	
21	OFFSET +5, R208			RCL 1021	R208	5 ± .005 Vdc	
22	HI AMPL, R242	DVM (ac mode)		RCL 1022	R242	3.536 ± .01 Vac	
23	LO AMPL, R251			RCL 1023	R251	.357 ± .002 Vac	
24	TRI AMPL, R148			RCL 1024	R148	2.887 ± .003 Vac	
25	SQR LOWER, R168	DVM (dc mode)		RCL 1025	R168	−5 ± .005 Vdc	
26	SQR UPPER, R164			RCL 1026	R164	5 ± .005 Vdc	
27	ATTEN ADJ, R295			RCL 1027	R295	.500 ± .001 Vdc	
28	WAVEFORM C97, C122, R96	Oscilloscope with Sampler Plug in	FUNC OUT (terminate with X10, 50Ω attenuator)	RCL 1028	C97 C122 R96	Aberrations ≤3.3% ± 40 mV Rise/Fall < 14.5 ns	
	NOTE: Steps 29 and 30 are arbitrary waveform generator adjustments (See figure 5-3).						
29	ARB − PEAK Adjustment	DVM (dc mode)	FUNC OUT (terminate with 50Ω)	RCL 1029	R37	−5.000 Vdc ±.005 Vdc	
30	ARB + PEAK Adjustment			RCL 1030	R34	+5.000 Vdc ±.005 Vdc	

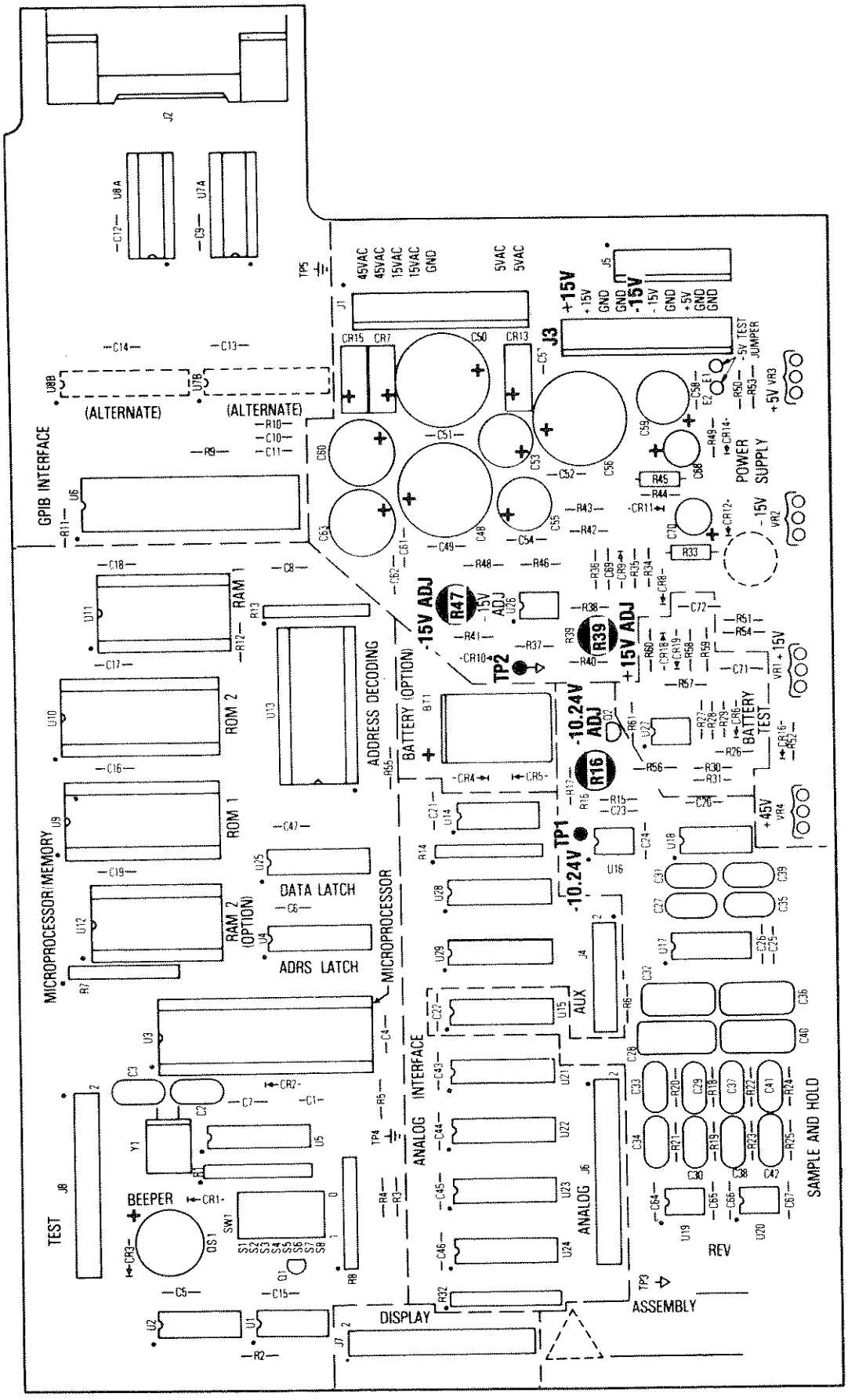


Figure 5-1. Microprocessor/Power Supply Calibration Point Locations

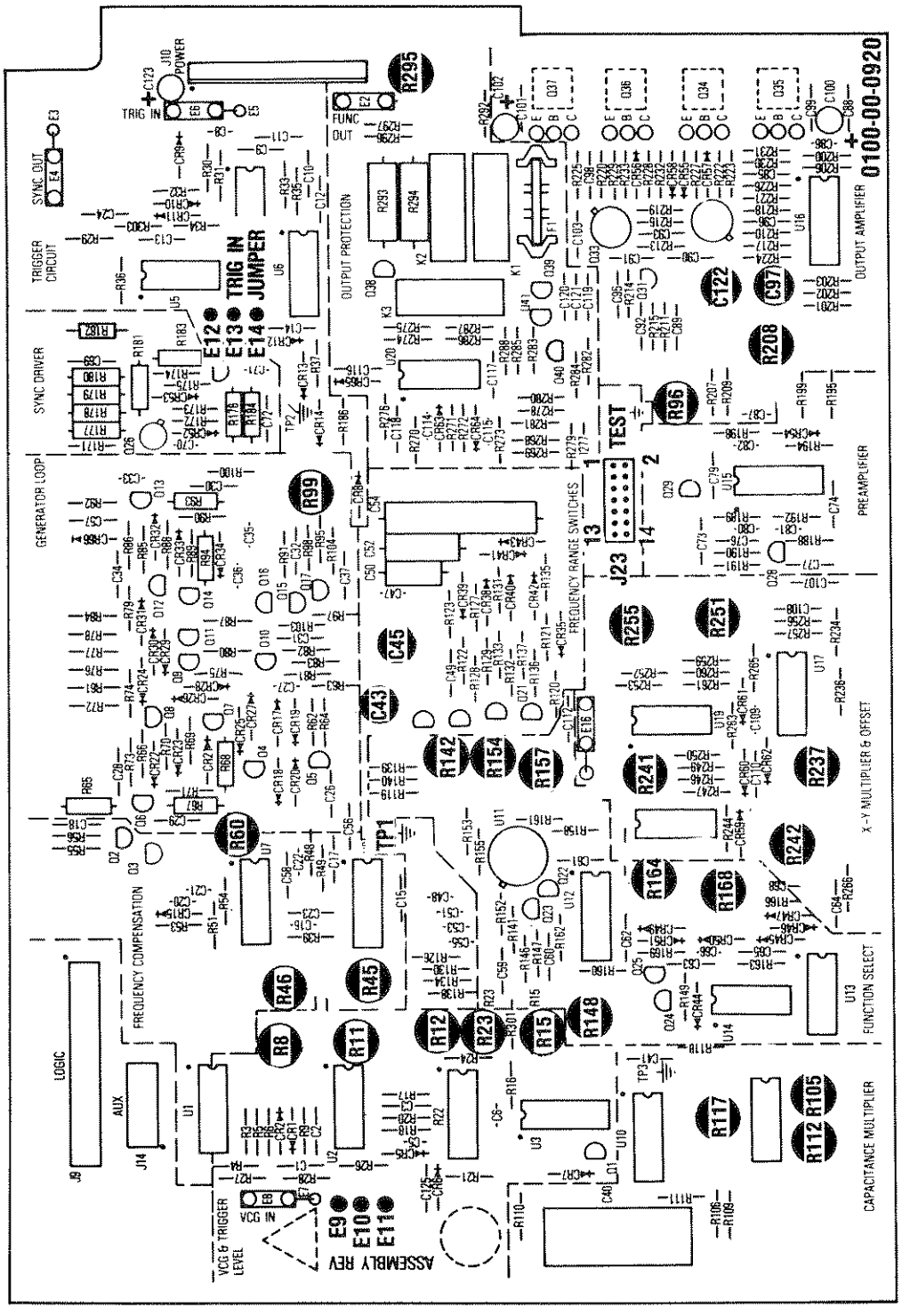


Figure 5-2. Function Generator Calibration Point Location

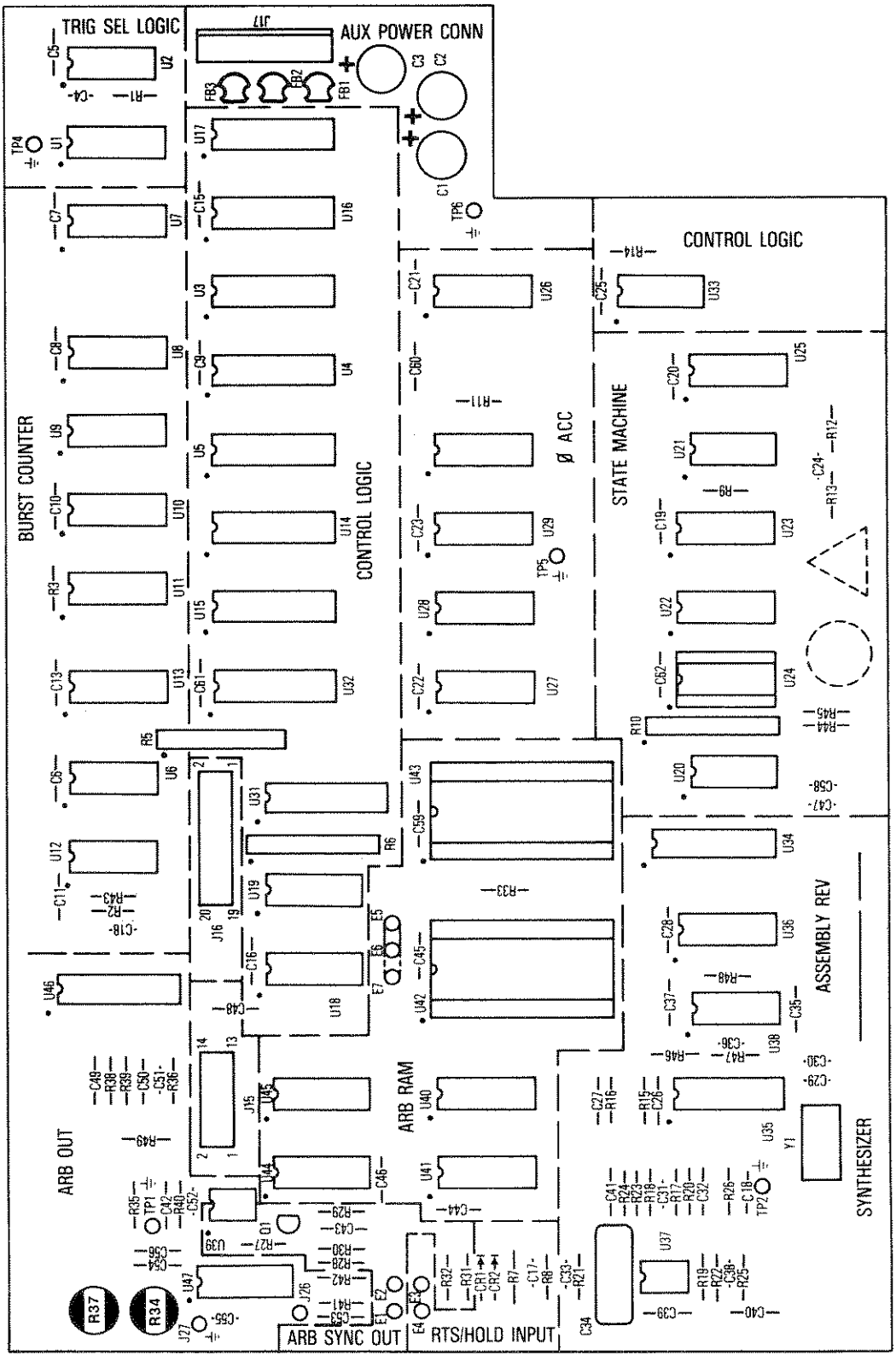


Figure 5-3. Arbitrary Waveform Generator Board Calibration Point Locations

SECTION 6
TROUBLESHOOTING

6.1 FACTORY REPAIR

Wavetek maintains a factory repair department for those customers not possessing the necessary personnel or test equipment to maintain the instrument. If an instrument is returned to the factory for calibration or repair, a detailed description of the specific problem should be attached to minimize turnaround time.

6.2 BEFORE YOU START

Since no troubleshooting guide can possibly cover all the potential problems, the aim of this guide is to give a methodology which, if applied consistantly, will lead to the problem area. Therefore, it is necessary to familiarize yourself with the instrument by reviewing the functional description and the detailed circuit description in conjunction with the schematic. Successful troubleshooting depends upon understanding the circuit operation within each functional block as well as the block relationships.

6.3 TROUBLESHOOTING

Table 6-1 gives an index of common symptoms. For each symptom a troubleshooting step is referenced that will aid in the solution of the problem. Individual component troubleshooting is given in paragraph 6.4 recommended test equipment is given in paragraph 5.2 and circuit schematics are in the back of this manual.

In all problems:

1. Double check for proper parameter settings.
2. Verify power supplies are in specification.
3. Calibrate or rule out calibration as a problem.
4. Inspect components, wiring and circuit boards for heat damage.
5. Recalibrate as necessary after circuit repair.

Find the instrument symptom in table 6-1 and proceed as directed to the proper troubleshooting step. After verifying the referenced step is okay, proceed to the following step unless directed otherwise.

Table 6-3 provides voltages and waveforms for circuits on the Function Generator Board. These

Table 6-1. Symptoms

Symptom	Table 6-2 Step
Display does not light	1.1-1.3
Display is not "WAVETEK 275" at power up	2
"BATTERY LOW" displayed	3
Keyboard has no effect	4
Cannot recall stored settings	5
Won't work on GPIB	6
Keyboard will not work with unit on GPIB	7
No output or incorrect output at FUNC OUT (output on)	8
No output or incorrect frequency	8.1
High frequency incorrect, sine distortion excessive at low frequencies, or no output	8.2
Sine distortion excessive, no output, or no sync output	8.3
No output or frequency incorrect below 100 Hz	8.4
Excessive sine distortion, amplitude errors, or no output	8.5
Offset errors or no output	8.6
Output offset or no output	8.7
No triangle out	9
No square out	10
Trigger or gated mode error	11
No burst or incorrect burst count	12
Internal trigger does not function or is inaccurate	13
No arbitrary function output	14
Monitor key inoperative	15
No ARB SYNC output	16
RTS/HOLD input inoperative	17

measurements were made with the default instrument parameters automatically selected at power-on or after pressing the RESET key, except that the output is turned on (OUT 1).

Tables 6-4 through 6-8 are truth tables of the logic states for the lines controlling frequency ranges, output relays, waveform functions, trigger modes and trigger slope.

6.4 TROUBLESHOOTING INDIVIDUAL COMPONENTS

6.4.1 Transistor

1. A transistor is defective if more than one volt is measured across its base-emitter junction in the forward direction.
2. A transistor when used as a switch may have a few volts reverse bias voltage across base emitter junction.
3. If the collector and emitter voltages are the same, but the base emitter voltage is less than 500mV forward voltage (or reversed bias), the transitor is defective.
4. A transistor, when used as a linear amplifier, is defective if its base current is larger than 10% of its emitter current (calculate currents from voltage across the base and emitter series resistors).
5. In a transistor differential pair (common emitter stages), either their base voltages are the same in normal operating condition, or the one with less forward voltage across its base emitter junction should be off (no collector current); otherwise, one of the transistors is defective.

6.4.2 Diode

A diode (except a zener) is defective if there is greater than one volt (typically 0.7 volt) forward voltage across it.

6.4.3 Operational Amplifier

1. The "+" and "−" inputs of an operational amplifier will generally have less than 15 mV voltage difference when operating under normal conditions except when used as a comparator.
2. When the output of the amplifier is connected to the "−" input (voltage follower connection), the output should be the same voltage as the "+" input voltage; otherwise, the operational amplifier is defective.
3. If the output voltage stays at maximum positive, the "+" input voltage should be more positive than "−" input voltage, or vice versa; otherwise, the operational amplifier is defective.

6.4.4 FET Transistor

1. No gate current should be drawn by the gate of a FET transistor. If so, the transistor is defective.
2. The gate-to-source voltage for a junction FET (JFET) is always reverse biased under a normal operating condition; e.g., the source voltage is more positive than the gate voltage for a N-Channel JFET such as 2N5485, and the source voltage is more negative than gate voltage for a P-Channel JFET such as 2N5462. Otherwise, the FET is defective.

6.4.5 Capacitor

1. Shorted capacitors have zero volts across their terminals.
2. Opened capacitor can be located (but not always) by using a good capacitor connected in parallel with the capacitor under test and observing the resulting effect.

6.4.6 Digital TTL IC's (e.g. 7400 Series)

1. The device is operating correctly if the output high state is $> +2.4$V and low state is $< +0.5$V.
2. The input must show the same two levels as in step 1. If the levels are between $+0.8$V and $+2.0$V, the connection to the driving circuit output is open.

Table 6-2. Troubleshooting

Step	Symptom	Check	Circuit Description Paragraph	Major Components	Schematic (No./Sheet/ Location)	Remarks
1.1	Display does not Light	AC Power	—	—	—	
		a. Power Source	—	—	—	
		b. Power Cord	—	—	—	
		c. Power Fuse	—	—	Rear panel	
		d. Power Selection	—	—	Rear panel	
		e. Power Switch	—	—	Inside rear panel	

Table 6-2. Troubleshooting (Continued)

Step	Symptom	Check	Circuit Description Paragraph	Major Components	Schematic (No./Sheet/ Location)	Remarks
1.2		DC Power				
		a. +45V supply	4.2.6.2	VR4, CR15-16, C60,63	1094/3/A4-7	
		b. +5V supply	4.2.6.1	VR3, CR13-14, C56,59	1094/3/B4-7	
		c. ±15V supply	4.2.6.3	VR1-2, CR7-12, U26, C48,50,53,55	1094/3/D3-7	
1.3		Display				
		a. Supply Voltages	4.3.1	J11	0921/1/C7	
		b. Filament Driver		U8, CR3-4, C14-15	0921/1/C3	
		c. Segment and Digit Drivers		U1-5, CR1-2	0921/1/C4-7	
		d. Fluorescent Display		V1	0921/1/C1-2	
2	Does not display "WAVETEK 275" at power-up	Microprocessor section				
		a. Reset Circuit	4.2.3	U3,27, CR1-2, 18-19	1094/1/C7, 2/A3	If okay return to step 1
		b. E-clock	4.2.1.1	U3, 6, 13, 25	1094/1/D6	
		c. Address Strobe (AS)	4.2.1.1	U3, 4	1094/1/D6	
		d. Address/Data Bus (AD)	4.2.1.1	U3,4-6,9-12	1094/1/C6	
		e. Address Bus (ADR)	4.2.1.2	U3-4,6,9-15,28	1094/1/C6	
		f. Microprocessor Software	4.2.7	U9-10	—	
3	"BATTERY LOW" displayed	Battery Backup	4.2.3			
		a. Battery below 2.4V		BT1, CR4, 5	1094/1/A3	If okay return to step 2
		b. Battery Test Circuit		U27, CR6	1094/2/A3	
4	Keyboard has no effect	Keyboard				
		a. ↵ key	4.3.2	Keyboard	Front panel	If okay return to step 2
		b. LCL key	4.3.2	Keyboard	Front panel	
		c. Keyboard	4.3.2	Keyboard	0921/1/B4	
		d. Keyboard decoder	4.3.2	U6,7	0921/1/A3-6	
5	Cannot recall stored settings	Stored Settings	4.2.3			
		a. Battery backup		BT1, U12	1094/1/A3-4	If okay return to step 2
		b. Reset		U27, CR18, 19	1094/2/A3	
6	Won't work on GPIB	GPIB				
		a. Address switch	4.2.1.8	SW1, U5	1094/1/C5	If okay return to step 2
		b. Remote indicator	4.2.2	U6-8	1094/1/C3	
		c. Command recall	4.2.2	U6-8	1094/1/C3	
7	Keyboard will not work with unit on GPIB	Local Lockput				
		a. Verify remote indicator (R) not displayed		LCL key	Front panel	If okay return to step 6
		b. Verify local lockout not set		GTL command	GPIB	
8	No or incorrect output at FUNC OUT (output on)	Test Connector: See Remarks				RESET instrument, with output
		on. If bad refer to:				
		a. J23 pin 11 VCGTST = 0.0 ± 0.1 Vdc			1101/3/B1	step 8.1
		b. J23 pin 9 DCCOMP = 0.0 ± 5.0 Vdc			1101/3/B1	step 8.2
		c. J23 pin 7 TRITST = 0.0 ± 0.1 Vdc			1101/3/B1	step 8.3
		d. J23 pin 13 AMPLDC = 5.0 ± 0.2 Vdc			1101/3/B1	step 8.5
		e. J23 pin 1 PATEST = 0.0 ± 0.1 Vdc			1101/3/B1	step 8.6 If okay go to step 8.7

Table 6-2. Troubleshooting (Continued)

Step	Symptom	Check	Circuit Description Paragraph	Major Components	Schematic (No./Sheet/ Location)	Remarks
8.1	No output or incorrect frequency	VCG				
		a. SH0 (FRQ input)	4.2.5.3	U15-19, C28	1094/2/C2	
		b. VCG Amp & Compensation	4.4.1	U1-2, CR1-2	1101/1/C4	
		c. Curent Sources	4.4.1	U2-3, Q1, CR4-6	1101/1/C4	
8.2	High frequency incorrect, sine distortion excessive at low frequencies or no output.	Frequency Compensation				
		a. DC Amplifier	4.4.5	U7-8, C17,58	1101/2/C6	
		b. High Frequency Comp	4.4.5	U1, U7-8, Q2-3, CR15-16	1101/2/C6	
8.3	Sine distortion excessive, no output, or no sync output	Main Generator				
		a. Current Switch	4.4.2	Q4-5, CR17-20	1101/2/D4	
		b. Switch Buffer	4.4.2	Q6-7, CR21-23	1101/2/C4	
		c. Comparator	4.4.2	Q8-12, CR24-31	1101/2/C3	
		d. Square Buffer	4.4.2	Q13-14, CR32-34	1101/2/C2	
		e. Triangle Buffer	4.4.2	Q15-17, CR66	1101/2/C1	
		f. Frequency Range Switches	4.4.3	Q18-21, CR35-43, C43-47, 50, 52, 54	1101/2/B2-4	
		g. Sync Driver	4.4.6	Q26-27j CR52-53	1101/3/C3-D3	
8.4	No output, or frequency incorrect below 100 Hz	Capacitance Multiplier	4.4.4	U8-11, C40	1101/2/A6-7	
8.5	Excessive sine distortion and amplitude errors, or not output	Amplitude Control				
		a. SH1 (AMP)	4.2.5.3	U15-19, C32	1094/2/C2	
		b. Sine Converter	4.4.8	U11-12, Q22-23, R145	1101/3/C4-6	
		c. XY Multiplier	4.4.9	U17-19, CR59-62	1101/4/A5-8	
8.6	Offset Errors or no output	Preamplifier	4.4.10	U15, Q28-29, CR54	1101/4/C5-7	
8.7	Output offset or no output	Output				
		a. SH2 (OST)	4.2.5.3	U15-18,20, C36	1094/2/C2	
		b. Offset	4.4.9	U17	1101/4/B5	
		c. Output Amplifier	4.4.11	U16, Q30-37, CR55-58	1101/4/C1-5	
		d. Fuse and Fuse Sense	4.4.12.2	U20, F1	1101/4/B1-2	
		e. Overvoltage Sense	4.4.12.1	U20, CR63-65	1101/4/B4	
		f. Output Attenuator	4.4.12.3	Q38-41, K1-3	1101/4/B1-2	
9	No triangle out	Triangle Level	4.4.8	U12, Q24-25	1101/3/B5-6	If okay return to step 8.3
10	No square out	Square				
		a. Square Logic	4.4.8	U13-14	1101/3/B5-6	If okay return to step 8.3d
		b. Square Shaper	4.4.8	U12, CR45-51	1101/3/A3-4	
11	Trigger or gated mode error	Trigger Circuit				
		a. SH3 (TRL)	4.2.5.3	U15-18,20, C40	1094/2/B2-3	If okay return to step 8.1c
		b. Trigger Level Amplifier	4.4.1	U2	1101/1/B6	
		c. Trigger Comparator	4.4.7	U4, CR9-11	1101/1/B5	
		d. Mode Logic	4.4.7	U5-6, CR7-8,12-14	1101/1/B4	

Table 6-2. Troubleshooting (Continued)

Step	Symptom	Check	Circuit Description Paragraph	Major Components	Schematic (No./Sheet/ Location)	Remarks
12	No burst or incorrect burst count	Burst Counter				
		a. Auxiliary Buffers	4.2.4.3	U28-39	1094/2/B6-7	
		b. Auxiliary Connectors		cables	connectors	
		c. TRIG IN Jumpers	4.4.7	E13-E14	1101/1/A4	
		d. Program Decode	4.5.1	U18, U19	1079/2/C7	
		e. Program Registers	4.5.1	U3-U5	1079/1/B5	
		f. Burst Mode Logic	4.5.2	U12, U6	1079/1/B2	
		g. Preset Counter	4.5.2	U7-U11	1079/1/A4	
		h. Burst Clock Select	4.5.2	U2	1079/1/D6	
		i. Burst Trigger Select	4.5.2	U1	1079/1/C7	
13	Internal Trigger does not function or is inaccurate	Internal Synthesizer				
		a. VCO (synthesizer) Output	4.5.3	U38	1079/3/C3	
		b. PLL Chip	4.5.3	U35	1079/3/D5	
		c. Loop Filter	4.5.3	U37A	1070/3/D4	
		d. Level Translator	4.5.3	U37B	1079/3/D3	
		e. Binary Divider	4.5.3	U36	1079/3/C5	
		f. SYNTH Data Latch	4.5.1	U34	1079/3/D5	
		Trigger Select Logic				
		a. TRIG Select Switch	4.5.2	U1	1079/1/C7	
		b. Logic Register	4.5.1	U5	1079/1/A5	
		c. Logic Register	4.5.1	U16	1079/2/C5	
14	No Arbitrary Function Output	Internal Synthesizer	4.5.3	U34-U38	1079/3/C4	Check internal trigger operation.
		Sequence Control Logic	4.5.4.4	U21-U25	1079/2/B4	
		Mode Control Register	4.5.1	U16	1079/2/C5	
		ϕ Accumulator	4.5.4.1	U26-U30	1079/2/D2	
		ARB RAM	4.5.4.2	U42, U43	1079/3/B7	
		ARB DAC	4.5.4.3	U46, U39	1079/3/B3	
		ARB Function Selector Switch	4.5.4.3	U47	1079/3/B2	
15	Monitor Key Inoperative	μPROC Data Selector	4.5.4.5.1	U25, U17	1079/2/B3	
		Data Serial Registers	4.5.4.2	U40, U41, U44, U45	1079/3/B7	
		Data Strobes	4.5.1	U18, U19	1079/2/C7	
16	No ARB SYNC Output	ARB Address Programming	—	—	—	ARB address must be programmed between the start and stop addresses.
		ARB SYNC OUT Buffer	4.5.4.5.2	U39A, Q1	1079/3/D2	
		ARB RAM	4.5.4.2	U43	1079/3/A7	

Table 6-2. Troubleshooting (Continued)

Step	Symptom	Check	Circuit Description Paragraph	Major Components	Schematic (No./Sheet/ Location)	Remarks
17	RTS/HOLD Input Inoperative	Mode Programming	—	—	—	Must be in an RTS mode for the RTS/HOLD input to function.
		RTS Input Buffer	4.5.4.4.1	U20A, C	1079/2/B6	
		External Input Sequence Latch	4.5.4.4.1	U21A, B	1079/2/B5	
		State Machine	4.5.4.4.2	U22-24	1079/2/A4	

Table 6-3. Function Generator Board Voltages (Reset Condition)

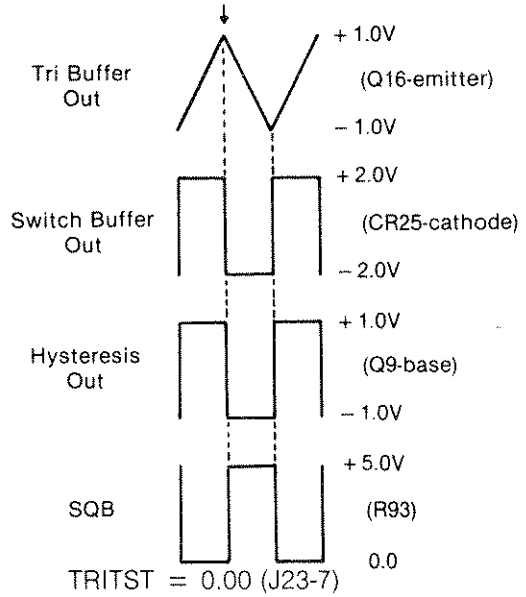
Circuit	Control Voltages	Circuit Voltages
VCG and trigger level	$\overline{OVR}$ = TTL high (J9-19) $\overline{FR5}$ = TTL high (J9-10) FRQ = 1.00V (J9-1) TRL = +4.25V (J9-4)	TLO = +1.5V (U2-7) THC = +1.2V (U3-9) VCV = −0.4V (E10) VCGTST = 0.00 Vdc (J23-11)
Frequency compensation	$\overline{FR7}$ = TTL high (J9-12) $\overline{FR6}$ = TTL high (J9-11) $\overline{FR5}$ = TTL high (J9-10) $\overline{DCA}$ = TTL low (J9-18)	DC COMP = 0 ± 5V (U7-14)
Generator loop		 TRITST = 0.00 (J23-7) DC COMP = 0 ± 5V (J23-9)

Table 6-3. Function Generator Board Voltages (Reset Condition) (Continued)

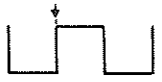
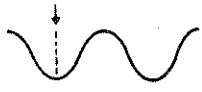
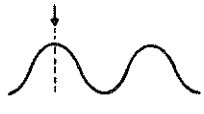
Circuit	Control Voltages	Circuit Voltages
Frequency range	$\overline{FR3}$ = TTL high (J9-8) $\overline{FR4}$ = TTL low (J9-9) $\overline{FR5}$ = TTL high (J9-10) $\overline{FR6}$ = TTL high (J9-11)	
Capacitance multiplier	$\overline{FR0}$ = TTL high (U10-9) $\overline{FR1}$ = TTL high (U10-8) $\overline{FR2}$ = TTL low (U10-1) $\overline{CPM}$ = TTL high (U10-16)	TRB  + 1.0V – 1.0V
Trigger circuit	+ TR = TTL high (J9-22) – TR = TTL low (J9-21) MC0 = TTL low (J9-16) MC1 = TTL low (J9-17)	TLO = + 1.5V (R29) THC = + 1.2V (CR14-cathode) SQB =  + 5.0V 0.0V (U5-4)
Function select	SQR = TTL low (U14-1) $\overline{SQR}$ = TTL low (U14-10) PLS = TTL low (U14-2) $\overline{PLS}$ = TTL low (U14-5) EXW = TTL low (U13-12) $\overline{SIN}$ = TTL low (R141) $\overline{TRI}$ = TTL high (R149) $\overline{RCT}$ = TTL high (R170)	TRB  + 1.0V (R139/140) – 1.0V
X-Y multiplier and offset		OST = + 5.00V (R235) Amp out = 0.0 Vdc (U17-8) AMP = + 5.00V (R266) AMPLDC = + 5.00V (J23-13)
Preamplifier		Preamp out  + 0.75 CR54-anode) – 0.75 PATEST = 0.0 Vdc (J23-1)
Output amplifier		Off amp out = 0.0 Vdc (R207) Preamp out  + 0.75 (R209) – 0.75 PATEST = 0.0 Vdc (J23-1) Out amp out  + 5.0V (R231/232) – 5.0V

Table 6-3. Function Generator Board Voltages (Reset Condition) (Continued)

Circuit	Control Voltages	Circuit Voltages
Output protection	FUB = TTL low (J9-34) OAP = TTL low (J9-33) OA0 = TTL low (J9-13) OA2 = TTL low (J9-15)	Fuse sense input  +5.0V (F1) −5.0V

Table 6-4. Frequency Truth Table

Frequency Range	FR0	FR1	FR2	FR3	FR4	FR5	FR6	FR7	CPM	OVR	DCA
10.0 – 99.9 mHz	1	1	1	0	1	1	1	1	0	1	1
100 – 999 mHz	0	1	1	0	1	1	1	1	0	1	1
1.00 – 9.99 Hz	1	0	1	0	1	1	1	1	0	1	1
10.0 – 99.9 Hz	1	1	0	1	1	1	1	1	0	1	1
100 – 999 Hz	1	1	0	0	1	1	1	1	1	1	0
1.00 – 9.99 kHz	1	1	0	1	0	1	1	1	1	1	0
10.0 – 99.9 kHz	1	1	0	1	1	0	1	1	1	1	0
100 – 999 kHz	1	1	0	1	1	1	0	1	1	1	0
1.00 – 9.99 MHz	1	1	0	1	1	1	1	0	1	1	0
10.0 – 12.0 MHz	1	1	0	1	1	1	1	0	1	0	0

Table 6-5. Output Relay Truth Table

Condition	OA0	OA2	OA1
Ampl + |Ofst| > 1.00V, Output On	1	0	1
Ampl + |Ofst| ≤ 1.00V, Output On	1	1	0
Output Off, Hi Z (~539 kΩ)	0	0	1
Output Off, Lo Z (~55.6Ω)	0	1	0

Table 6-6. Function Truth Table

Function	$\overline{SIN}$	$\overline{TRI}$	$\overline{RCT}$	SQR	$\overline{SQR}$	PLS	$\overline{PLS}$	EXW	
Sine	0	1	1	0	0	0	0	0	∿
Triangle	1	0	1	0	0	0	0	0	∿
Square	1	1	0	1	0	0	0	0	⊓
Sqr Comp	1	1	0	0	1	0	0	0	⊔
DC	1	1	1	0	0	0	0	0	⎓
Ext Width	1	1	0	0	0	0	0	1	

Table 6-7. Mode Truth Table

Mode	MC0	MC1	
Cont	0	0	
Trig	1	0	
Gate	1	1	(Includes Burst Mode)

Table 6-8. Trigger Truth Table

Trigger	+TR	−TR	
+ (Rising)	1	0	⊣‾
− (Falling)	0	1	‾⊢
Man Trig	1	1	

SECTION 7
PARTS AND SCHEMATICS

7.1 DRAWINGS

The following assembly drawings, parts lists and schematics are in the arrangement shown below.

7.2 ERRATA

Under Wavetek's product improvement program, the latest electronic designs and circuits are incorporated into each Wavetek instrument as quickly as development and testing permit. Because of the time needed to compose and print instruction manuals, it is not always possible to include the most recent changes in the initial printing. Whenever this occurs, errata pages are prepared to summarize the changes made and are inserted inside the shipping carton with this manual. If no such pages exist, the manual is correct as printed.

7.3 ORDERING PARTS

When ordering spare parts, please specify part number, circuit reference, board, serial number of unit, and, if applicable, the function performed.

NOTE

An assembly drawing number is not necessarily the assembly part number. However, the assembly parts list number is the assembly part number.

Instrument Schematic	0004-00-0203
Instrument Parts List	1000-00-0203
Chassis Assembly	0102-00-1659
Chassis Parts Lists	1101-00-1659
Front Panel Assembly	0102-00-1003
Front Panel Parts List	1101-00-1103
Display Schematic	0103-00-0921
Display Assembly	1100-00-0921
Display Parts List	1100-00-0921
Function Generator Schematic	0103-00-1101
Function Generator Assembly	1100-00-1101
Function Generator Parts List	1100-00-1101
Microprocessor/Power Supply Schematic	0103-00-2202
Microprocessor/Power Supply Assembly	1100-00-2202
Microprocessor/Power Supply Parts List	1100-00-2202
Prom Package	1109-00-0024
Arb Gen Board Schematic	0103-00-1079
Arb Gen Board Assembly	1100-00-1079
Arb Gen Board Parts List	1100-00-1079

REV	ECN	BY	DATE	APP

A5 REAR PANEL ASSY

J18 AC POWER RECP
100 - 120 V - 1/2 A SB
220 - 242 1/4 A SB
F1

J2 IEEE - 488
1 D101
2 D102
3 D103
4 D104
5 EOI
6 DAV
7 RFD
8 DAC
9 IFC
10 SRQ
11 ATN
12
13 D105
14 D106
15 D107
16 D108
17 REN
18 GND
19 GND
20 GND
21 GND
22 GND
23 GND
24 GND

T1 1204-00-0049
W1
P1
J1
45 VAC
45 VAC
15 VAC
15 VAC
GND
5 VAC
5 VAC

TEST CONNECTOR
J8
E
ADR 15
GND
ADR 14
A5
ADR 13
GND
ADR 12
NMI
ADR 11
GND
ADR 10
GND
ADR 9
GND
ADR 8
GND
AD7
GND
AD6
GND
AD5
TEST
AD4
GND
AD3
+5V
AD2
N.C.
AD1
N.C.
AD0
GND
R/W

A6
μ PROC/POWER SUPPLY BOARD

A2 FRONT PANEL ASSY

J7 P7
W4
+45V
GND
+5V
+5V
+5V
+5V
+5V
KYBD
PORT
PORT 16
DISP
GND
AD4
AD3
AD2
AD1
AD0
ADR 3
ADR 2
ADR 1
ADR 0
GND
DATA 7
DATA 6
DATA 5
DATA 4
DATA 3
DATA 2
DATA 1
DATA 0
GND
GND
GND
+15V

J11

A3 DISPLAY BOARD 1100 - 00 - 0921

A4 CABLE INTERFACE BOARD

J3 P3 J6 P6 J4 P4 J5 P5
W13
W14
+15V
+15V
GND
GND
-15V
-15V
+5
GND
GND
SH0
SH1
SH2
SH3
ANL 0
ANL 1
ANL 2
ANL 3
ANL 4
ANL 5
ANL 6
ANL 7
ANL 8
ANL 9
ANL 10
ANL 11
ANL 12
ANL 13
ANL 14
ANL 15
ANL 16
ANL 17
ANL 18
ANL 19
ANL 20
ANL 21
ANL 22
ANL 23
ANL 24
ANL 25
ANL 26
ANL 27
PORT 10
PORT 11
W2
W3
FRQ
AMP
OST
TRI
FR 0
FR 1
FR 2
FR 3
FR 4
FR 5
FR 6
FR 7
CA 0
CA 1
CA 2
MC 0
MC 1
OCA
OVS
CAM
-TR
+TR
EXW
SQR
SIN
TRI
RET
PLS
PLS
OAP
PUB

A7 FUNCTION GENERATOR BOARD

P10 J10 P9 J9
W20 ARB OUT
E15 E16

A8 OUTPUT FUSE BOARD

J16 P16 J17 P17
W15
GND
VCG1
GND
VCG0
GND
GND
TRIG
GND
TRIG0
GND
PLS1
GND
SQS
GND

A10 AUXILLARY FUNCTION BOARD

J26 J27 P26 P27 J15 P15 J14 P14

E1
E2
E3
E4

FUNC OUT { E1 E2
SYNC OUT { E3 E4
TRIG IN { E5 E6
VCG IN { E7 E8

W5
W6
W7
W8

P13 J13 P12 J12
W16
W17
W18
W19
W9
W10
W11
W12

J24 ARB SYNC OUT
J25 ARB RTS /HOLD IN
J19 FUNC OUT
J20 MAIN SYNC OUT
J21 TRIG IN
J22 VCG IN

TEST CONNECTOR
J23
PA TEST
+5 VT
-15 VT
GND
+5 VT
GND
TRI TST
GND
DC COMP
GND
VCG TST
GND
AMP LDC
GND

A1 CHASSIS ASSY

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN FN AQUINO
DATE
PROJENGR RBA
RELEASE APPROV RBA
TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE: SCHEMATIC INSTRUMENT

MODEL NO. 275
DWG NO. 0004-00-0203
REV
CODE IDENT 23338
SHEET 1 OF 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	SCHEMATIC, INSTRUMENT	0004-00-0203	WVTK	0004-00-0203	1
NONE	FINAL CAL PROCEDURE	0006-00-0203	WVTK	0006-00-0203	1
NONE	SPECIFICATIONS	0007-00-0203	WVTK	0007-00-0203	1
NONE	PCA, DISPLAY	270-0921	WVTK	1100-00-0921	1
NONE	PCA, CABLE INTERFACE	270-1006	WVTK	1100-00-1006	1
NONE	PCA, ARB GEN BOARD	275-1079	WVTK	1100-00-1079	1
NONE	PCA, FUNCTION GEN BD	275-1101	WVTK	1100-00-1101	1
NONE	ASSY MICRO-PROC/GPIB BOARD	1100-00-2202	WVTK	1100-00-2202	1
NONE	ASSY, FRONT PANEL-275	275-1103	WVTK	1101-00-1103	1
NONE	ASSY, REAR PANEL	275-1170	WVTK	1101-00-1170	1
NONE	CHASSIS ASSY 275	275-1659	WVTK	1101-00-1659	1
NONE	PROM PACKAGE	275-0024	WVTK	1109-00-0024	1
NONE	CHASSIS CABLE KIT	275-1099	WVTK	1207-00-1099	1
NONE	NUT, SPEED, SELF RETAIN	C7494-632-4	TINN	2800-09-0003	2
NONE	101-6F INSERT	101-6F	WVTK	3300-00-0013	1
NONE	CARTON 22X15 1/4X10	101-6A	WVTK	3300-01-0010	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	MODEL 275 12MHZ PROG ARB/FUNC GEN	1000-00-0203	E
		PAGE 1	

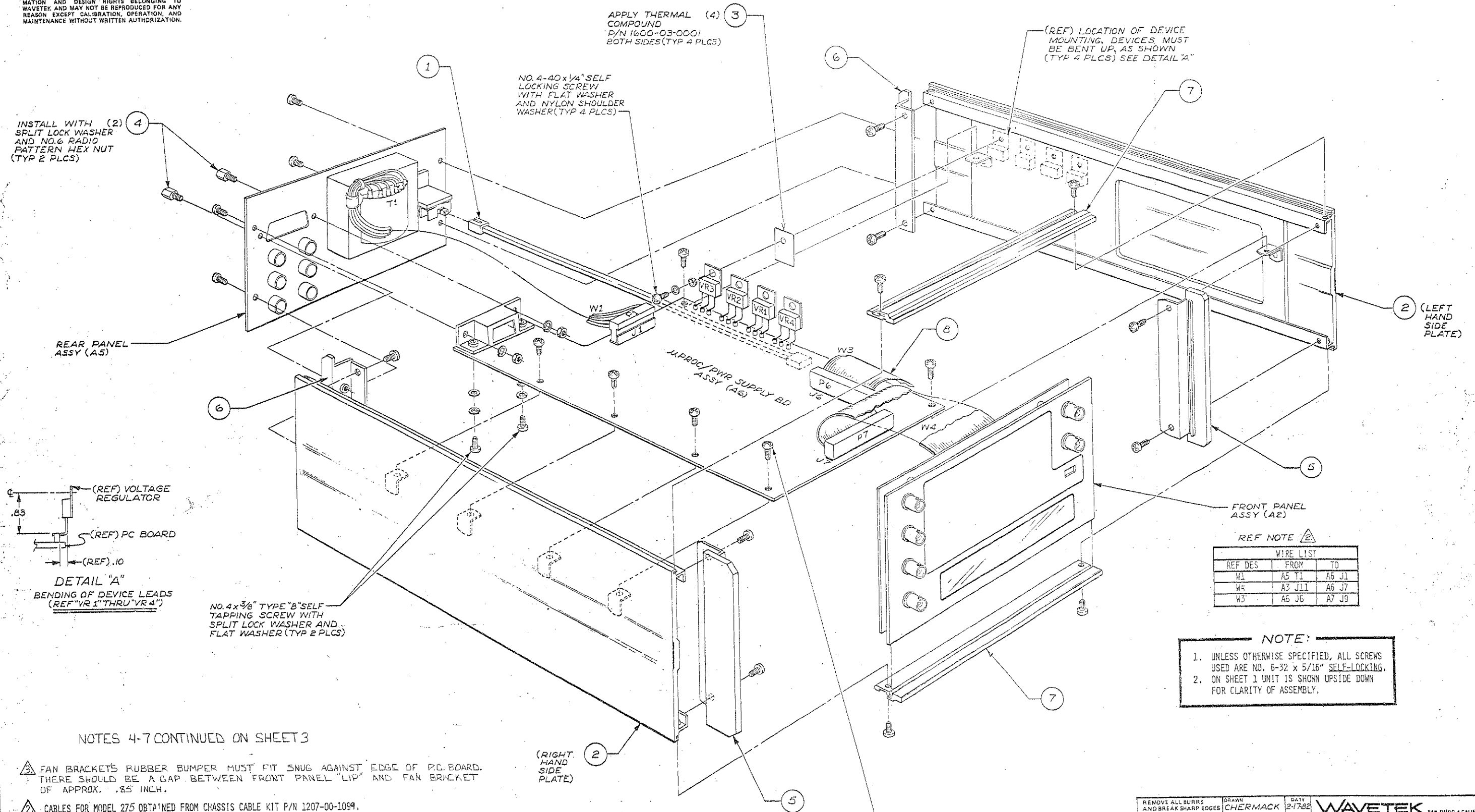
REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	1/4, 200#, SINGLE, RSC PWR CORD	17251	BELDN	6001-80-0005	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	MODEL 275 12MHZ PROG ARB/FUNC GEN	1000-00-0203	E
		PAGE 2	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE				DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES		WAVETEK Wavetek Inc.			
x/x ± 1/64	xxx ± .005	.xx ± .01	∠ ± 1°	DRAWN	DATE	TITLE: PARTS LIST GENERATOR MODEL 275			
MATERIAL:				CHKD					
				ENG APPR.					
FINISH:				MFG APPR.		SIZE D	MODEL NO 275	DRAWING NO 1000-00-0203	REV E
				ISSUED		SCALE:	CODE IDENT 23338	SHEET 1 OF 1	

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE

REV	ECN	BY	DATE	APP
A	ECO # 34-010	MS	2-8-84	DMB



WIRE LIST		
REF DES	FROM	TO
W1	A5 T1	A6 J1
W4	A3 J11	A6 J7
W3	A6 J6	A7 J9

NOTE:

1. UNLESS OTHERWISE SPECIFIED, ALL SCREWS USED ARE NO. 6-32 x 5/16" SELF-LOCKING.
2. ON SHEET 1 UNIT IS SHOWN UPSIDE DOWN FOR CLARITY OF ASSEMBLY.

NOTES 4-7 CONTINUED ON SHEET 3

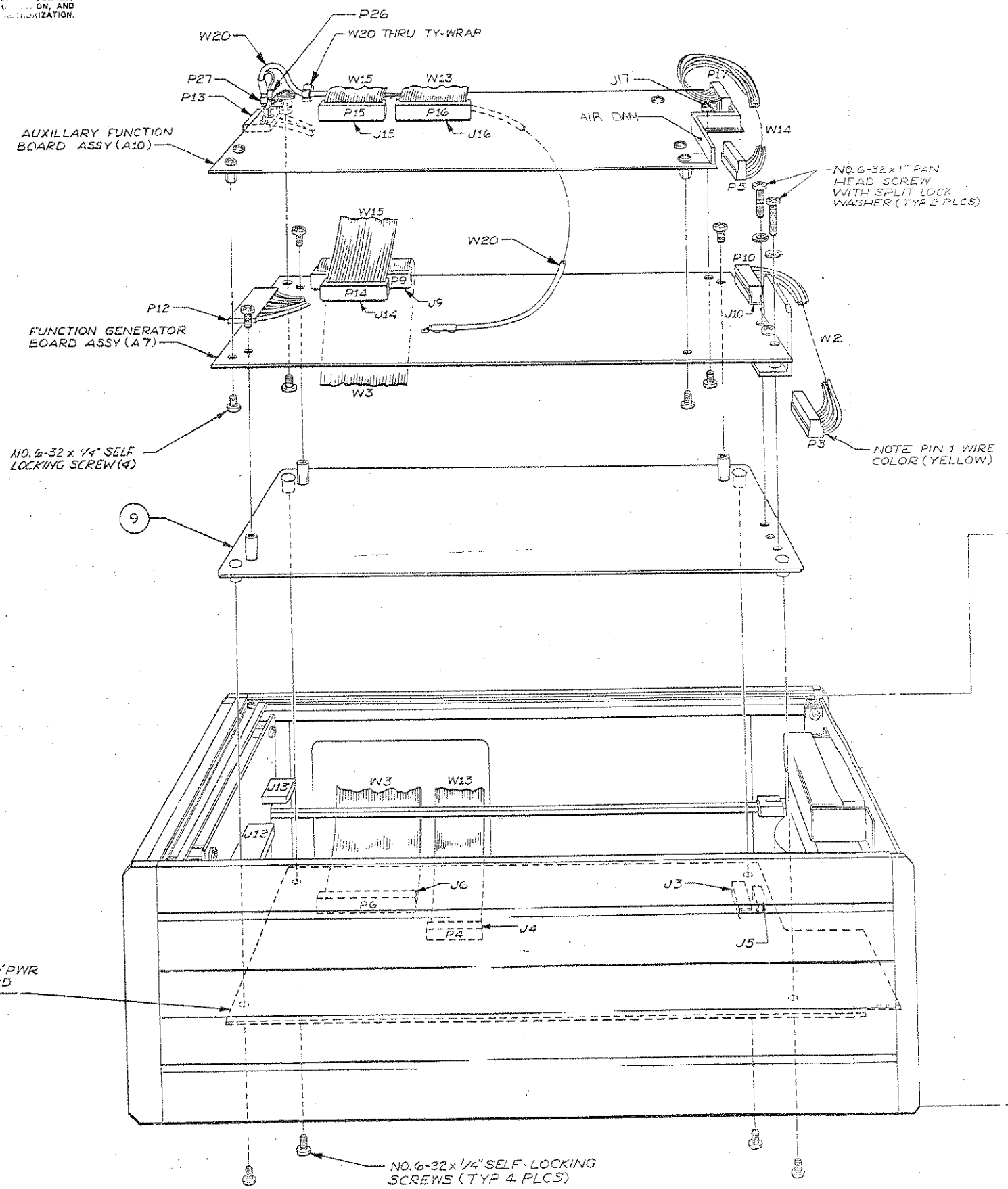
3. FAN BRACKETS RUBBER BUMPER MUST FIT SNUG AGAINST EDGE OF P.C. BOARD. THERE SHOULD BE A GAP BETWEEN FRONT PANEL "LIP" AND FAN BRACKET OF APPROX. .85 INCH.

2. CABLES FOR MODEL 275 OBTAINED FROM CHASSIS CABLE KIT P/N 1207-00-1099.

1. FOR UNIT INTERCONNECTION SEE INSTRUMENT SCHEMATIC # 0004-00-0180.

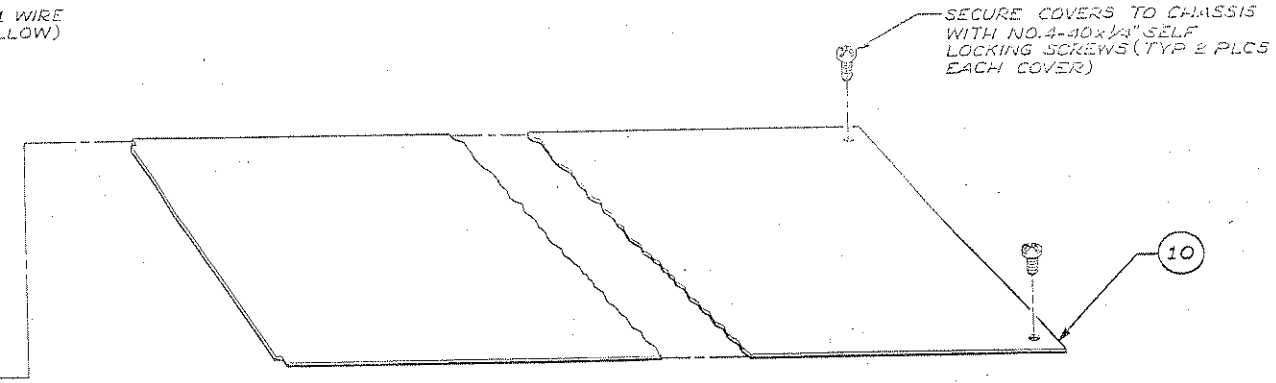
NOTE: UNLESS OTHERWISE SPECIFIED

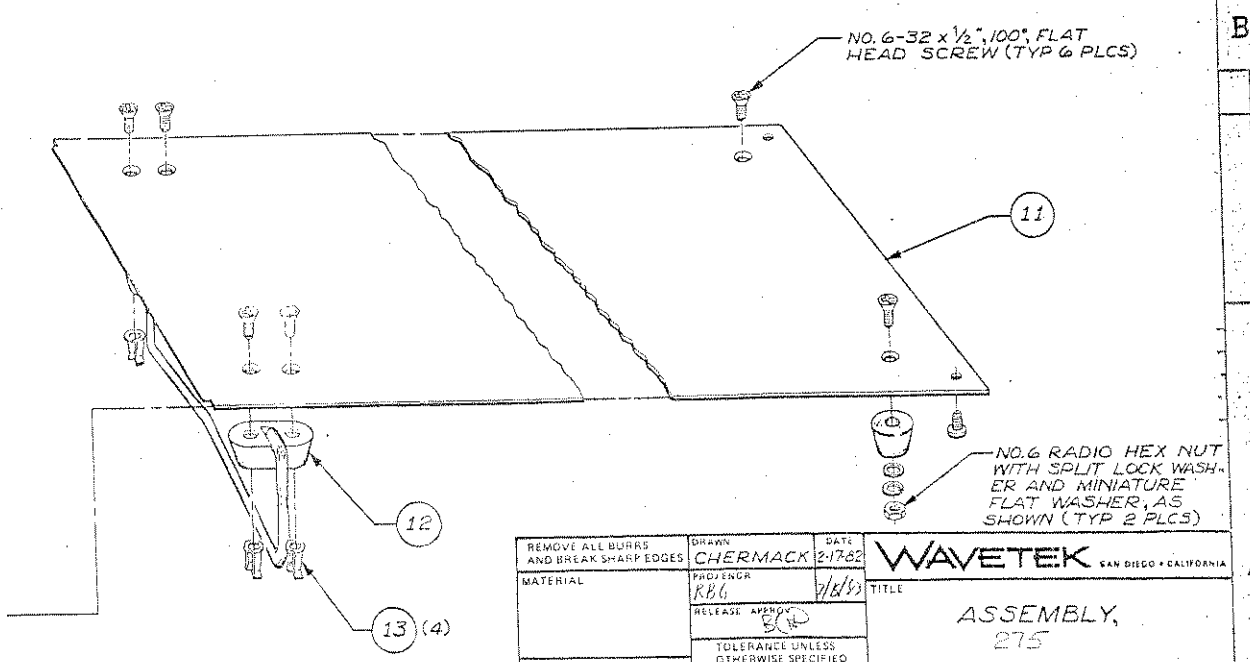
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 2-1782	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR K86	7/15/83	TITLE ASSEMBLY, 275
FINISH WAVETEK PROCESS	RELEASE APPROV BJ		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG	MODEL NO 275	DWG NO 0102-00-1659 REV A
	SCALE NONE	CODE IDENT 23338	SHEET 1 OF 4



REF NOTE (2)

WIRE LIST		
REF DES	FROM	TO
W2	A6 J3	A7 J10
W3	A6 J6	A7 J9
W5,W6,W7,W8	A7	A4 J12
W16,W17	A10	A4 J13
W14	A10 J5	A6 J17
W13	A6 J4	A10 J16
W15	A7 J14	A10 J15
W20	A7 E15	A10 J26
	A7 E16	A10 J27



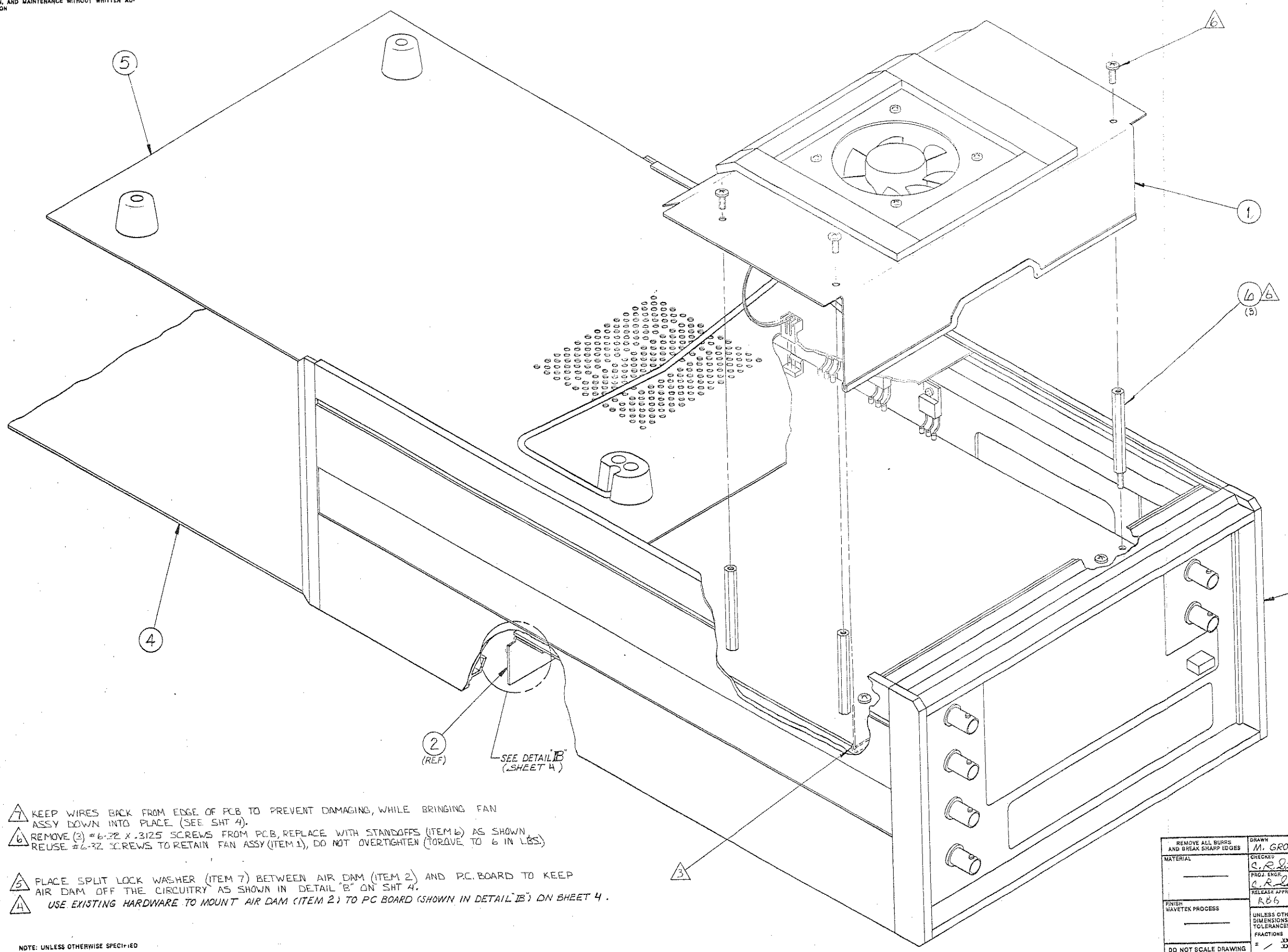


NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 2-17-82	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR KBG	7/8/83	TITLE ASSEMBLY, 275
FINISH WAVETEK PROCESS	RELEASE AGENCY		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ± .010 ANGLES ±1° XX ± .030		
	DO NOT SCALE DWG	MODEL NO 275	DWG NO. 0102-00-1659 REV A
	SCALE NONE	CODE IDENT 23338	SHEET 2 OF 4

REV	ECN	BY	DATE	APP

REV	ECO	BY	DATE	APP



7 KEEP WIRES BACK FROM EDGE OF PCB TO PREVENT DAMAGING, WHILE BRINGING FAN ASSY DOWN INTO PLACE. (SEE SHT 4).

6 REMOVE (3) #6-32 X .3125 SCREWS FROM PCB, REPLACE WITH STANDOFFS (ITEM 6) AS SHOWN. REUSE #6-32 SCREWS TO RETAIN FAN ASSY (ITEM 1), DO NOT OVERTIGHTEN (TORQUE TO 6 IN LBS.)

5 PLACE SPLIT LOCK WASHER (ITEM 7) BETWEEN AIR DAM (ITEM 2) AND P.C. BOARD TO KEEP AIR DAM OFF THE CIRCUITRY AS SHOWN IN DETAIL "B" ON SHT 4.

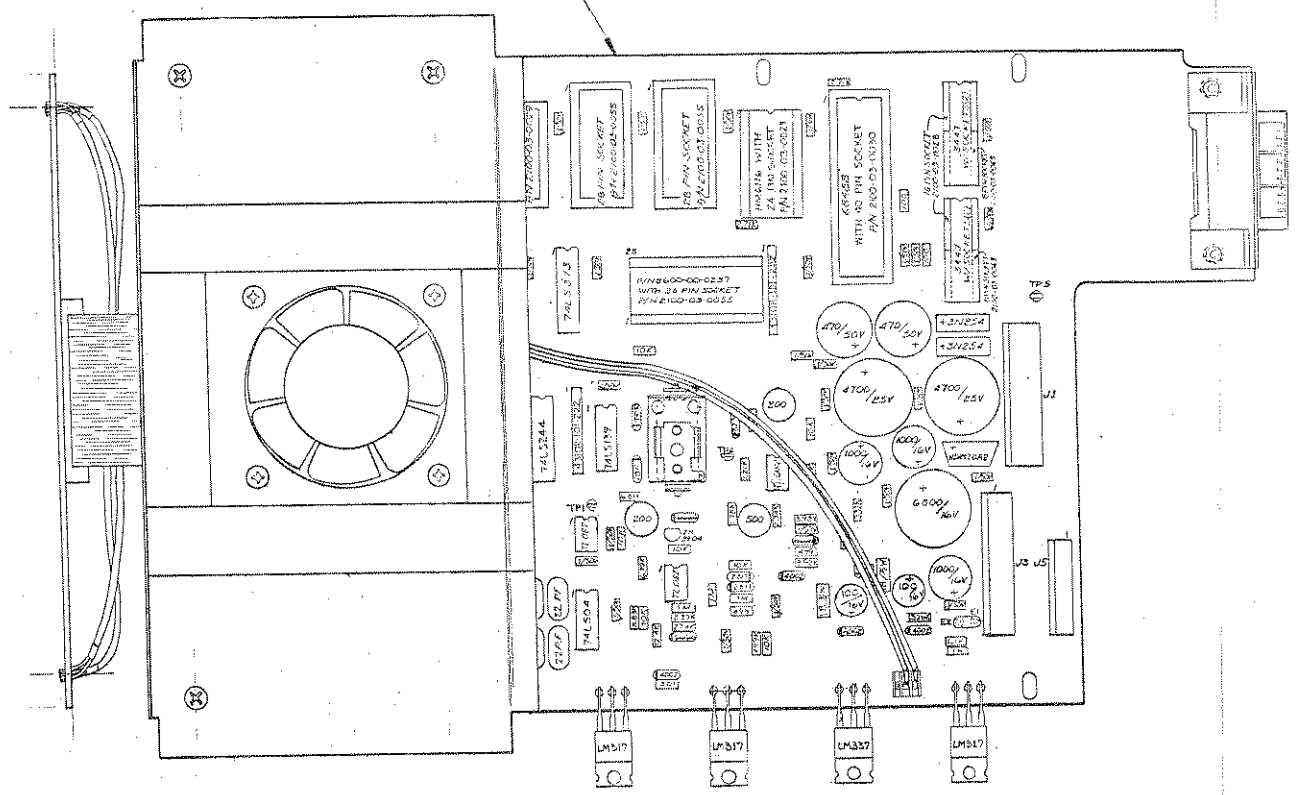
4 USE EXISTING HARDWARE TO MOUNT AIR DAM (ITEM 2) TO PC BOARD (SHOWN IN DETAIL "B") ON SHEET 4.

NOTE: UNLESS OTHERWISE SPECIFIED

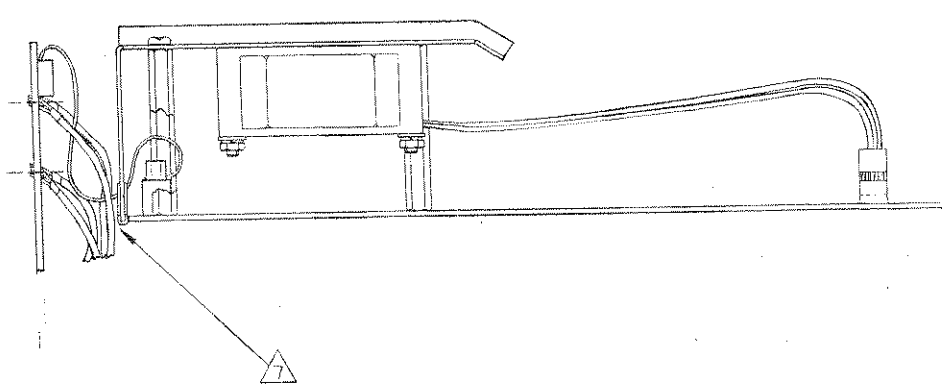
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN M. GROVES	DATE 2-8-08	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL —	CHECKED C.R.L.	2/8/08	TITLE ASSEMBLY-275
	PROJ. ENGR. C.R.L.	2/8/08	
	RELEASE APPROV. R.B.G.	7/3/08	
FINISH WAVETEK PROCESS —	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES XX ± .03 XXX ± .010 ± /		SIZE D · FSCM NO. 23338 · DWG. NO. 0102-00-1659 · REV A
DO NOT SCALE DRAWING			SCALE FULL · MODEL 275 · SHEET 3 OF 4

SEE SHEET 1

(PCA, MICRO PROCESSOR/POWER SUPPLY BOARD, P/N 0101-00-2202)

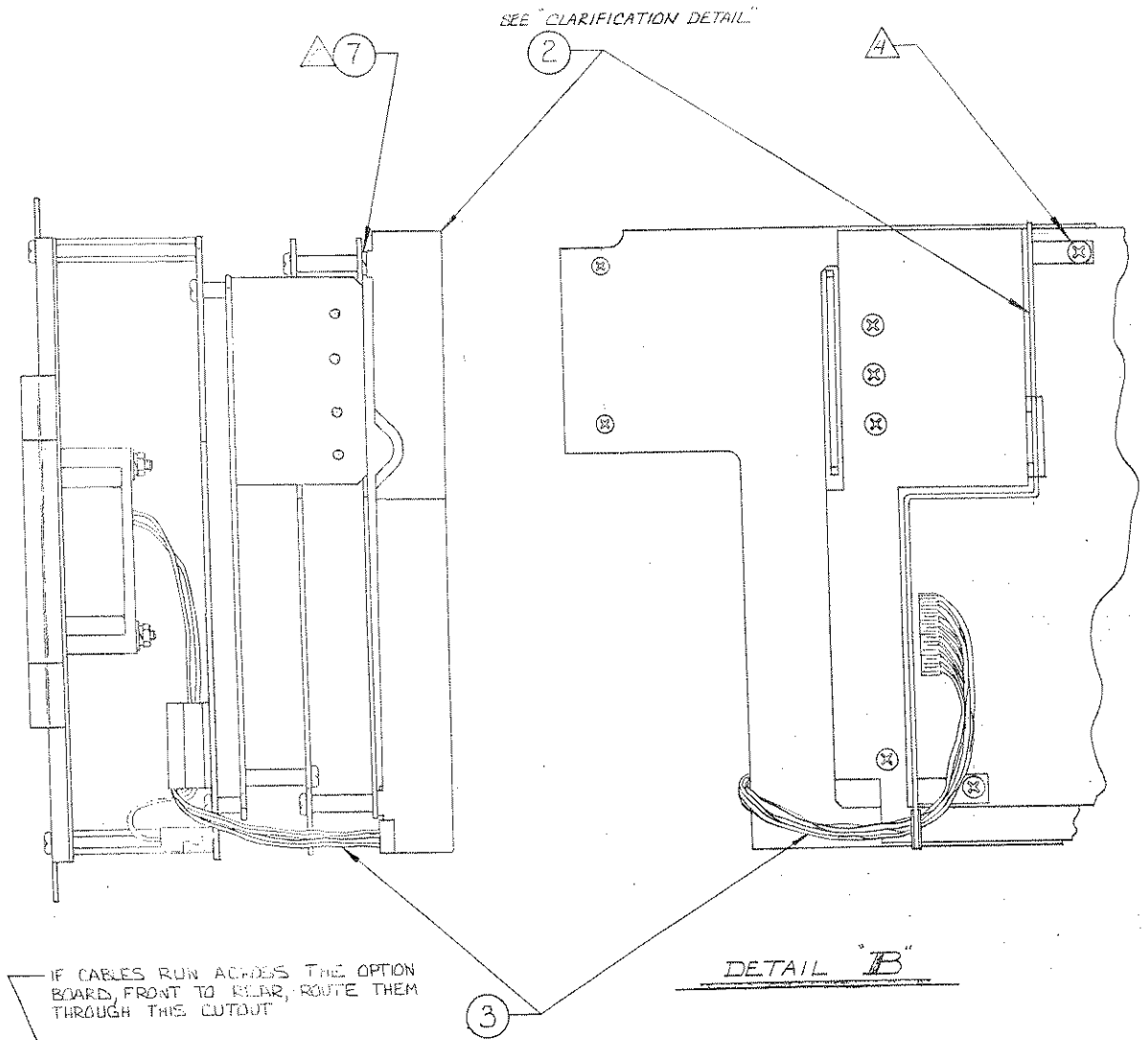


DETAIL "A"

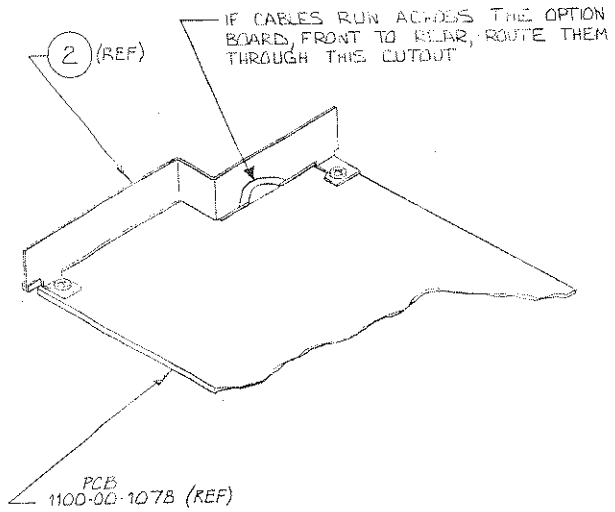


NOTE: UNLESS OTHERWISE SPECIFIED

SEE "CLARIFICATION DETAIL"



DETAIL "B"



CLARIFICATION DETAIL
SCALE : NONE

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN M. GROVES	DATE 2-8-88	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	CHECKED		TITLE ASSEMBLY-275
	PROJ. ENGR.		
FINISH WAVETEK PROCESS	RELEASE APPROV.		
DO NOT SCALE DRAWING	UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES .XX ± .XXX ±		SIZE D | FSCM NO. 23338 | DWG. NO. 0102-00-1659 | REV A SCALE FULL | WEIGHT 275 | SHEET 4 OF 4

REV	ECO	BY	DATE	APP.

ZONE	LTR	ECO NO	CHANGED BY	APPR'D. BY		DATE

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, CHASSIS-275	0102-00-1659	WVTK	0102-00-1659	1
NONE	PCA, ARB GEN BOARD	275-1079	WVTK	1100-00-1079	1
NONE	PCA, FUNCTION GEN BD	275-1101	WVTK	1100-00-1101	1
NONE	ASSY MICRO-PROC/GPIB BOARD	1100-00-2202	WVTK	1100-00-2202	1
NONE	ASSY, FRONT PANEL-275	275-1103	WVTK	1101-00-1103	1
NONE	ASSY, REAR PANEL	275-1170	WVTK	1101-00-1170	1
NONE	PROM PACKAGE	275-0024	WVTK	1109-00-0024	1
NONE	ASSY, CHASSIS SUB 275-1659	275-2552	WVTK	1206-00-2552	1
NONE	ASSY, FAN	1206-00-3088	WVTK	1206-00-3088	1
NONE	ASSY, AIR DAM 275	1206-00-3115	WVTK	1206-00-3115	1
NONE	CHASSIS CABLE KIT	275-1099	WVTK	1207-00-1099	1
NONE	COVER, TOP-270	1400-02-4332	WVTK	1400-02-4332	1
NONE	COVER, BOTTOM-270	1400-02-4342	WVTK	1400-02-4342	1
	STANDOFF MALE/FEM, 1.687H, .250 HEX 6-32 THD,	1473-M03-F07-632	UNICP	2800-02-0039	3
NONE	WASHER	B51547F015	MOT	2800-11-0015	4

WAVETEK PARTS LIST	TITLE: CHASSIS ASSY 275	ASSEMBLY NO.: 1101-00-1659	REV: C
		PAGE 1	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE				DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	
X/x ± 1/64	.xxx ± .005	.xx ± .01	± 1°	DRAWN	DATE
MATERIAL:				CHKD	
FINISH:				ENG APPR.	
				MFG APPR.	
				ISSUED	

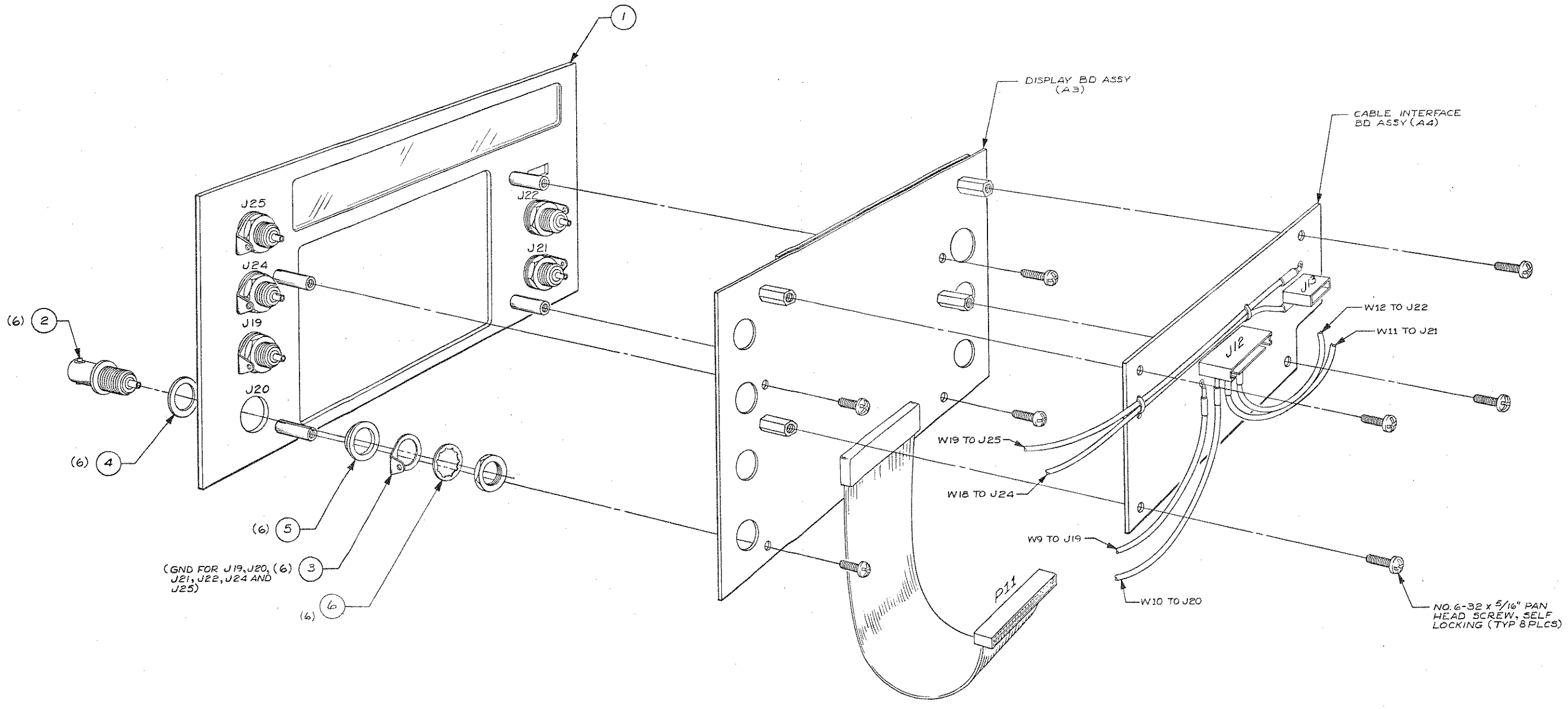
WAVETEK
Wavetek Inc.

TITLE: PARTS LIST
ASSY, CHASSIS

SIZE	MODEL NO.	DRAWING NO.	REV
D	275	1101-00-1659	C

SCALE: | CODE IDENT 23338 | SHEET 1 OF 1

REV	ECN	BY	DATE	APP
/	3612 CLASS III	SC	1-1483	BS
B	#7841	M.O. 3-5-87	3/9/87	SS



WIRE LIST		
REF. DES.	FROM	TO
W9	A4 E1	J19
	A4 E2	J19
W10	A4 E3	J20
	A4 E4	J20
W11	A4 E5	J21
	A4 E6	J21
W12	A4 E7	J22
	A4 E8	J22
W19	A4 E9	J25
	A4 E10	J25
W18	A4 E11	J24
	A4 E12	J24

NOTE. UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S. CHERMACK	DATE 1-26-82	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR P.N.Z.	2/15/87	TITLE ASSEMBLY, FRONT PANEL (A2)
FINISH WAVETEK PROCESS	RELEASE APPROV P.N.Z.		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG	MODEL NO 273, 275, 278	DWG NO 0102-00-1003 REV B
	SCALE NONE	CODE IDENT 23338	SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

8 7 6 5 4 3 2 1

ZONE	LTR	ECO NO	CHANGED BY	APPR'D BY	DATE

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, FRONT PANEL	0102-00-1003	WVTK	0102-00-1003	1
NONE	ASSY, PANEL	275-1104	WVTK	1206-00-1104	1
2	CONN BNC	KC-7946	KING	2100-01-0002	6
3	SOLDER LUG	1497	SMITH	2100-04-0012	6
6	WASHER, 1/2 IN IT	1/2 IN IT WASHER	CMRCL	2800-24-0008	12
5	WASHER, SHOULDER	2668	SMITH	2800-27-0004	12
4	WASHER NYLON FLAT	2264-N-385	AMTOM	2800-28-0005	6

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	ASSY, FRONT PANEL-275	1101-00-1103	C

PAGE 1

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE				DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	
x/x ± 1/64	.xxx ± .005	.xx ± .01	± 1°	DRAWN	DATE
MATERIAL:				CHKD	
FINISH:				ENG APPR.	
				MFG APPR.	
				ISSUED	

WAVETEK
Wavetek Inc.

TITLE
PARTS LIST
ASSY, FRONT PANEL

SIZE	MODEL NO	DRAWING NO.	REV
D	275	1101-00-1103	C

SCALE: | CODE IDENT 23338 | SHEET 1 OF 1

R.S.Knapp

REV	ECN	BY	DATE	APP
A	# 3904	SC	8-10-83	
/	4154 CLASS III	SC	2-6-84	

SEGMENT DRIVERS

U1 UCN4815A: DATA Ø–DATA 7, ADR Ø, CE, OE, STROBE → ANO O, ANO DP, ANO F, ANO E, ANO D, ANO C, ANO B, ANO A

U2 UCN4815A: DATA Ø–DATA 7, ADR 1, CE, OE, STROBE → ANO N, ANO M, ANO L, ANO K, ANO J, ANO I, ANO H, ANO G

C1, C2 .1/50V; +5V, +45V

U5A LS04: DISP → BLANK

R1 1K

DIGIT DRIVERS

U4 UCN 4810A: DSP, DI, CLK, DO, OE → GRID 1 – GRID 10

U3 UCN 4810A: DI, CLK, OE → GRID 11 – GRID 20

CR1, CR2 FD6666; R2 1K; C3, C4, C6, C7 .1/50V

FILAMENT DRIVER

R6 10; R4 63.4K; R5 95.3K; CR3; CR4 FD6666(2); U8 NE555; C15 100/16V; C11 .1/50V; C12 910pf; C13 .1/50V; C14 100/16V; +15V

VACUUM FLOURESCENT DISPLAY

V1 FG206A2: GRID 1 – GRID 20; FILA, FILA; P0, PDP, PF, PE, PD, PC, PB, PA, PN, PM, PL, PK, PJ, PI, PH, PG → ANO O, ANO DP, ANO F, ANO E, ANO D, ANO C, ANO B, ANO A, ANO N, ANO M, ANO L, ANO K, ANO J, ANO I, ANO H, ANO G

J11 DISPLAY

1	+45V	20	ADØ
2	GND	21	ADR1
3		22	GND
4		23	DATA 7
5		24	DATA 6
6		25	DATA 5
7	+5V	26	DATA 4
8	KYBD	27	DATA 3
9	BLANK	28	DATA 2
10	DSP	29	DATA 1
11	DISP	30	DATA Ø
12	GND	31	GND
13	AD4	32	GND
14	AD3	33	GND
15	AD2	34	+15 V
16	AD1		
17	ADØ		
18	ADR3		
19	ADR2		

C16, C17 .1/50V; TO GND ON INTERFACE BD (A4); C9 100/16V

U5B LS04

KEYBOARD

U6 74LS240: AD Ø–AD 4 → KYBD; R3 10K SIP; C8 .1/50V

U7 74LS145: ADR Ø–ADR 3; C10 .1/50V

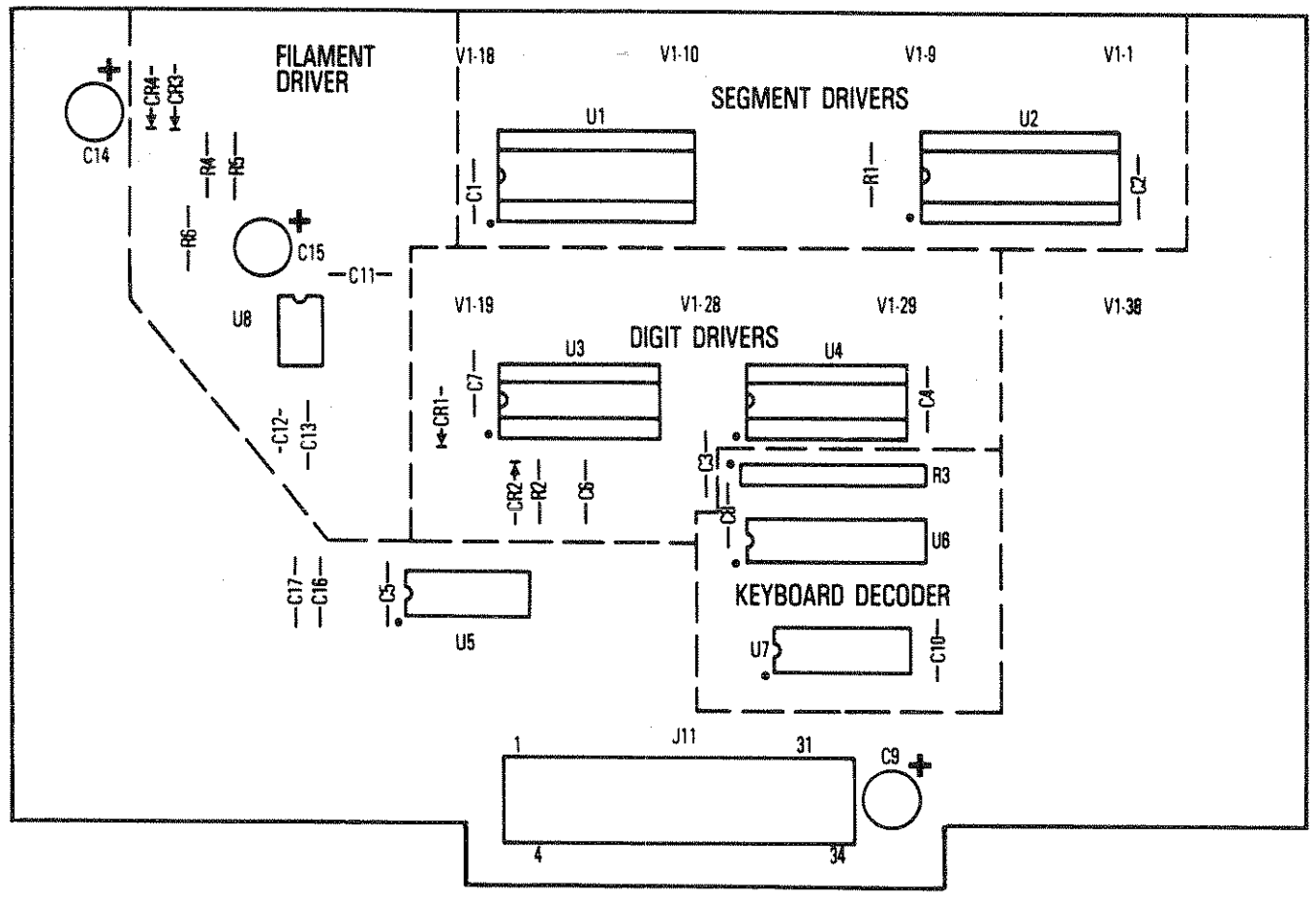
KEYBOARD DECODER

4. ALL CAPACITORS ARE SHOWN IN MICRO-FARADS.
3. ALL RESISTORS ARE SHOWN IN OHMS.
2. ALL DIODES ARE FD6666.
1. REFERENCE DESIGNATORS SHOWN ARE PARTIAL, PREFIX WITH ASSEMBLY REF DES (A3).

NOTE UNLESS OTHERWISE SPECIFIED

BISHOP GRAPHICS/ACCUPRESS REVISED NO. A4884

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S.CHERMACK	DATE 8-17-81	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR R.B.L.	7/15/83	TITLE: SCHEMATIC, DISPLAY BOARD (A3)
FINISH WAVETEK PROCESS	RELEASE APPROV P.W.		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1° XX ± .030		
	DO NOT SCALE DWG	MODEL NO. 270 SERIES	DWG NO. 0103-00-0921 REV A
	SCALE	CODE IDENT 23338	SHEET 1 OF 1



MADE FROM 0100-00-0921-3D

WAVETEK SAN DIEGO, CALIFORNIA

TITLE

DISPLAY

MODEL NO	ASSY NO	REV
275	1100-00-0921	
CODE IDENT 23338	SHEET 4 OF 4	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, DISPLAY	0101-00-0921	WVTK	0101-00-0921	1
NONE	SCHEMATIC, DISPLAY	0103-00-0921	WVTK	0103-00-0921	1
NONE	SPK ASSY, KEYBOARD	178/270-0939	WVTK	1206-00-0939	1
C1 C10 C11 C13 C16 C17 C2 C3 C4 C5 C6 C7 C8	CAP, CER, MON, .1MF, 50V, AXIAL	CAC03Z5U104Z050A	CORNG	1500-01-0405	13
C12	CAP, MICA, 910PF, 100V, 1 %, RADIAL	DM15-911F	ARCO	1500-19-1101	1
C14 C15 C9	CAP, ELECT, 100MF, 35V RADIAL LEAD, SP .20	ULB1V101M	NICH	1500-31-0102	3
NONE	DISPLAY BOARD	270-0921	WVTK	1700-00-0921	1
NONE	SKT, IC, 22 PIN	DILB22P-108T	BURND	2100-03-0035	2
NONE	SOCKET, 18 PIN	DILB18P-108T	BURND	2100-03-0050	2
V1	DISPLAY, FLOUR.	FG206A2	ITRON	2400-03-0009	1
NONE	STANDOFF, SWAGE .500 H, .250 HEX6-32, .062 MAT'L	1531B-1/2-11	USECO	2800-02-0003	4
R1 R2	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	2
R6	RES, MF, 1/8W, 1%, 10	RN55D10R0F	MEPCO	4701-03-1009	1
R4	RES, MF, 1/8W, 1%, 63.4K	RN55D-6342F	TRW	4701-03-6342	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, DISPLAY	1100-00-0921	A
		PAGE 1	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R5	RES, MF, 1/8W, 1%, 95.3K	RN55D-9532F	TRW	4701-03-9532	1
R3	RES NETWORK 10K 2% 10PIN SIP BUSS	4310R-101-103	BOURN	4770-00-0008	1
CR1 CR2 CR3 CR4	DIODE 1N4148 COMPUTER, G/P, 75V, 200M A, SWITCHING	1N4148	FAIR	4807-02-6666	4
W4	ASSY, RIBBON CABLE	922522-34-02-4.5	A/P	6002-00-0009	1
U8	TIMING CIRCUIT, SILICON MONOLITHIC	LM555CN	NSC	7000-05-5500	1
U3 U4	DRIVER, 10 BIT SI, BIMOS	TL4810AN	TI	8000-48-1000	2
U1 U2	DRIVER, LTCH/SORC, BIMOS	UCN5815A	SPRAG	8000-48-1500	2
U5	INVERTER, HEX, TTL	74LS04	TI	8000-74-0410	1
U7	CDDR/DRV, BCD-DEC, TTL	74LS145	SIG	8007-41-4510	1
U6	BUF, OCT 3ST OUT, TTL	M74LS240P	MITSU	8007-42-4010	1

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	PCA, DISPLAY	1100-00-0921	A
		PAGE 2	

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PCA, DISPLAY
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1 .XX ±.030		
	DO NOT SCALE DWG	MODEL NO 275	DWG NO 1100-00-0921 REV A
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

NOTE UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP

VCG & TRIGGER LEVEL

REV	ECN	BY	DATE	APP
A	# 3904	SC	7-29-83	QA
B	ECN 4336	RO	9-7-84	
C	7093	RO	2-14-85	KJ
D	ECO 8251	SC	5-20-87	
E	ECO 9631		6/4/88	DMD

VCG COMPENSATION
VCG AMPLIFIER
CURRENT SOURCES
+5V
+15 VR
DG211 U1D
R1 150K
R2 150K
OVR
DG211 U1C
R3 1M
FR5
FRQ
R4 4.99K
R5 4.99K
C1 .1
R7 3.57K
FREQ HI
R8 1K CW
C2 .1
TL084 U2A
R6 10K
VCG IN
GND
C3 .1
CR1 IN4148
CR2 IN4148
R10 1M
R11 100K CW
R9 2.49K
VCG ZERO
VCGO
VCGI
FREQ LO
R12 100K CW
R13 499K
C4 100PF
R14 1K
TL084 U2D
CR3 IN4148
R17 1K
LO SYM
R15 100K CW
R16 1M
R19 4.99K
C124 .1
CR4 IN959B
R22 1K DIP
HI SYM
R23 100 CW
R24 23.7K
U3B CA3096A
R22 1K DIP
C6 220 PF
+I
VCV
VCGTST
R301 10K
VCG JUMPER
R18 1K
C5 100PF
TL084 U2C
R20 1K
CR5 IN4148
CR6 IN959B
C125 .1
R21 4.99K
-I
CR7 FD777 ⚠6
THC
U3A
SS
Q1 2N3903
R22 1K DIP
-15 VR
+5V
+15V
TRIGGER LEVEL AMPLIFIER
-15VR
R25 30.1K
R26 20K
R27 4.99K
R28 4.99K
TRL
C7 .1
TL084 U2B
TLO
R29 4.99K
C24 .1
R303 2.49K
C9 .1
C10 .1
R304 20K
C126 1.5PF
R33 100K
CR9 IN4148
-TR
C8 10 PF
R30 3.32K
R31 7.5K
TRIG IN
GND
U4 NE529
R32 2.49K
CR10 IN4148
CR11 751A
R35 100K
+TR
R34 2.49K
R305 20K
C127 1.5 PF
C11 .1
C12 .1
SQB
U5B 74F00
U5D 74F00
MC1
U5C 74F00
TRIG JUMPER
TRGO
TRGL
74F74
MCØ
U5A 74F00
C13 .1
C14 .1
R36 2.49K
CR8 FD777 ⚠6
TRN
CR12 IN4148
CR13 IN4148
CR14 IN4148
R37 8.25K
-15V
TP1 TP2 TP3 TP4

LAST USED	NOT USED
R303	R143, R144
C126	
CR68	
U20	
Q41	
K3	
E16	
TP1	

9. * NOMINAL VALUE CALLED OUT ON PARTS LIST.
⚠8 MATCH SET RESISTORS (3) P/N 4789-00-0043 (REF R113, R114, R115)
⚠7 MATCHED SET CAPACITORS (3) P/N 1509-80-0008 (REF C50, C52, C54)
⚠6 MATCHED PAIR FD777 DIODES P/N 4898-00-0004 (REF CR8, CR7)
⚠5 MATCHED SET .1% RESISTORS (4) P/N 4701-02-7500 (REF R194, R198, R189, R192).
4. ALL CAPACITORS ARE IN MICRO-FARADS.
3. ALL DIODES ARE FD6666
2. ALL RESISTORS ARE IN OHMS.
1. REFERENCE DESIGNATORS SHOWN ARE PARTIAL, PREFIX WITH ASSEMBLY REF DES (A7)
NOTE: UNLESS OTHERWISE SPECIFIED

TRIGGER COMPARATOR & SLOPE LOGIC
MODE LOGIC

TRIGGER CIRCUIT

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S. THOMPSON	DATE 11-23-83	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR	7-15-85	TITLE SCHEMATIC FUNCTION GENERATOR BOARD (A7)
FINISH WAVETEK PROCESS	RELEASE APPROV		TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030
	DO NOT SCALE DWG		MODEL NO. 275
	SCALE		DWG NO. 0103-00-1101 REV E
			CODE IDENT 23338 SHEET 1 OF 4

BISHOP GRAPHICS/ACCUPRESS RECORDER NO. A-5894

FREQUENCY COMPENSATION

HIGH FREQUENCY COMPENSATION

GENERATOR LOOP

CURRENT SWITCH · SWITCH BUFFER · COMPARATOR · SQUARE BUFFER · TRIANGLE BUFFER

TRIANGLE BUFFER OUTPUT

DC COMPENSATION

TRIANGLE NODE

DC AMPLIFIER

CAPACITANCE MULTIPLIER

FREQUENCY RANGE SWITCHES

△6 SEE PAGE 1

△7 SEE PAGE 1

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S.THOMPSON	DATE 11-23-81	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR	7-15-82	TITLE SCHEMATIC FUNCTION GENERATOR BOARD (A7)
FINISH WAVETEK PROCESS	RELEASE APPROV	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.030 ANGLES ±1°	
	DO NOT SCALE DWG		MODEL NO. 275 · DWG NO. 0103-00-1101 · REV E
	SCALE		CODE IDENT 23338 · SHEET 2 OF 4

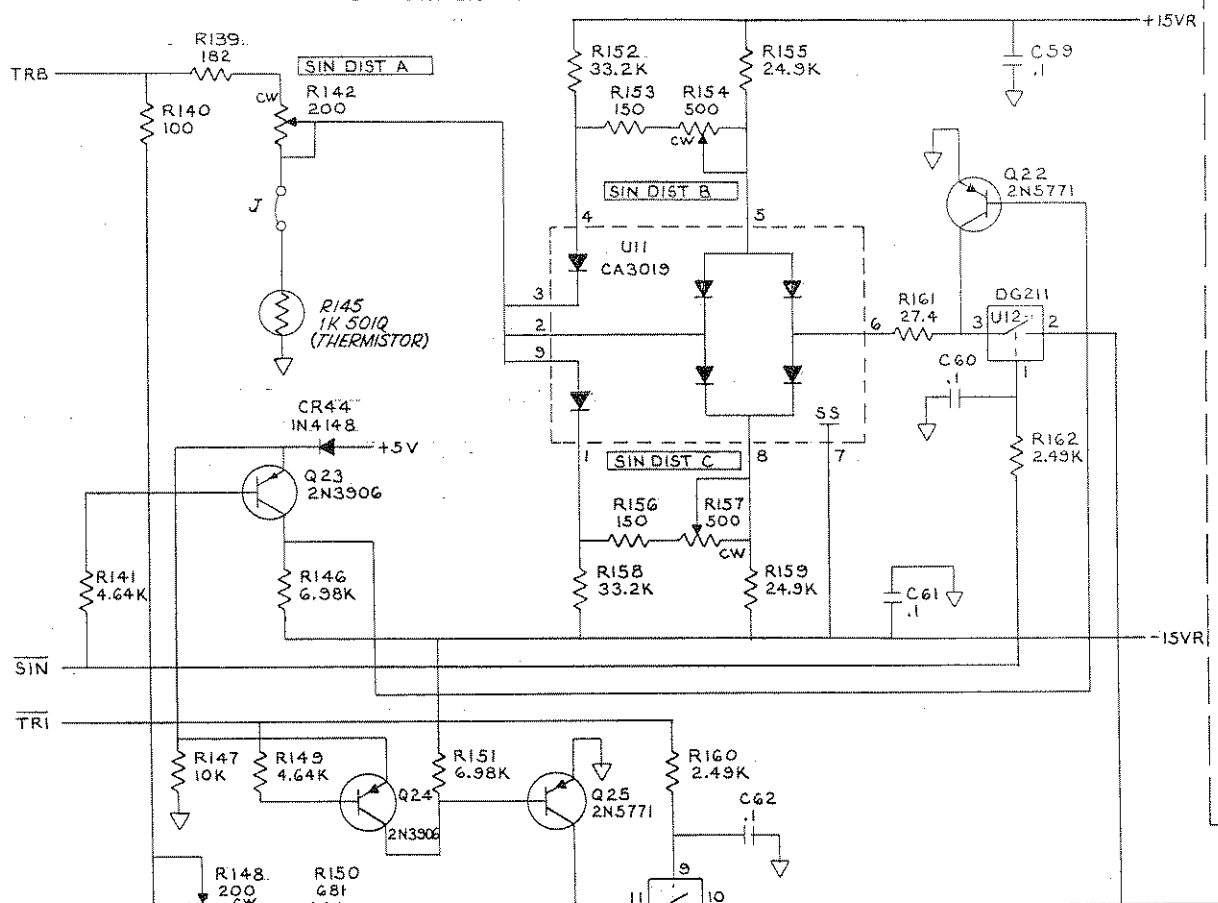
BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-4994

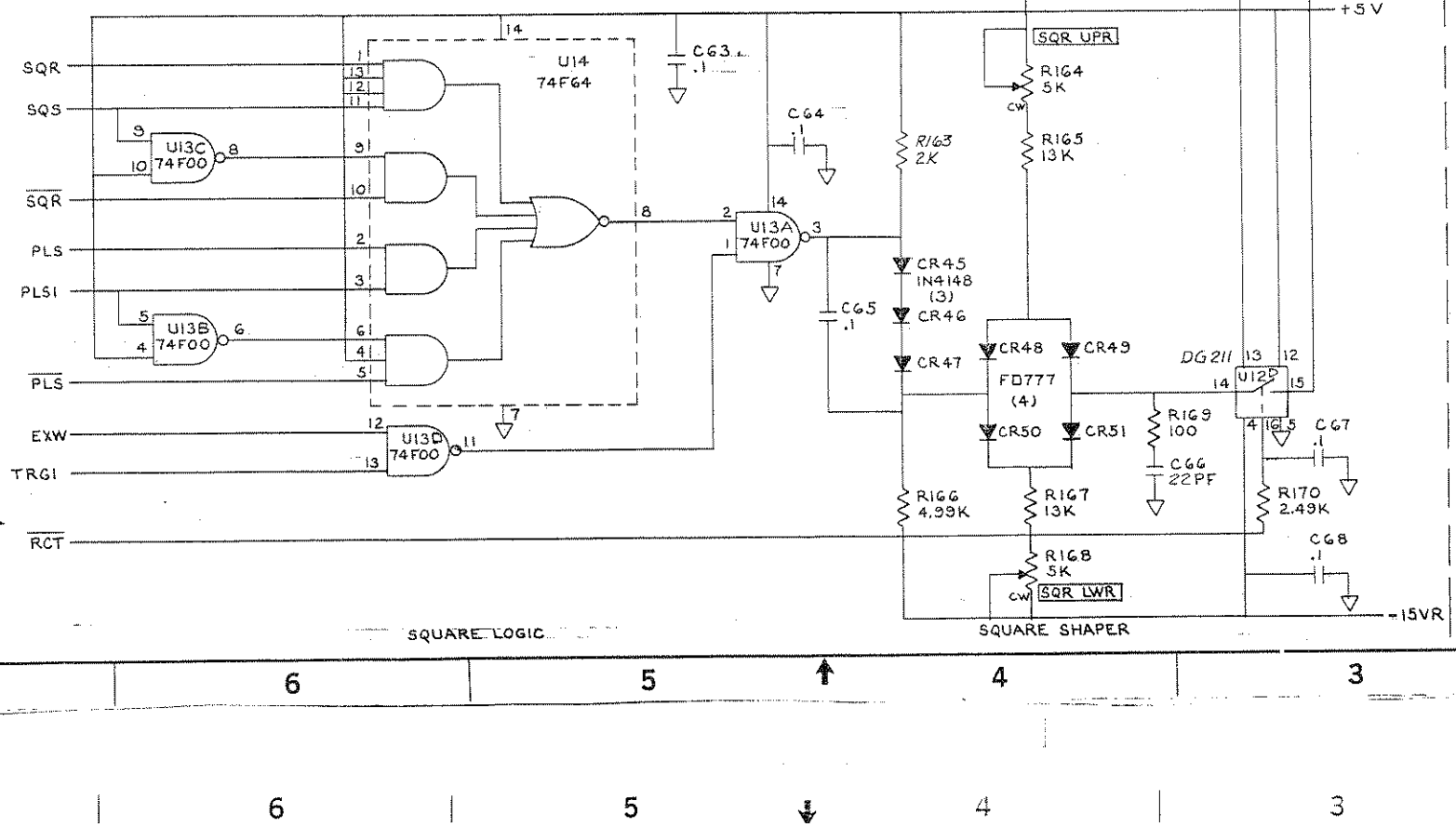
REV	ECN	BY	DATE	APP'D

REV	ECN	BY	DATE	APP

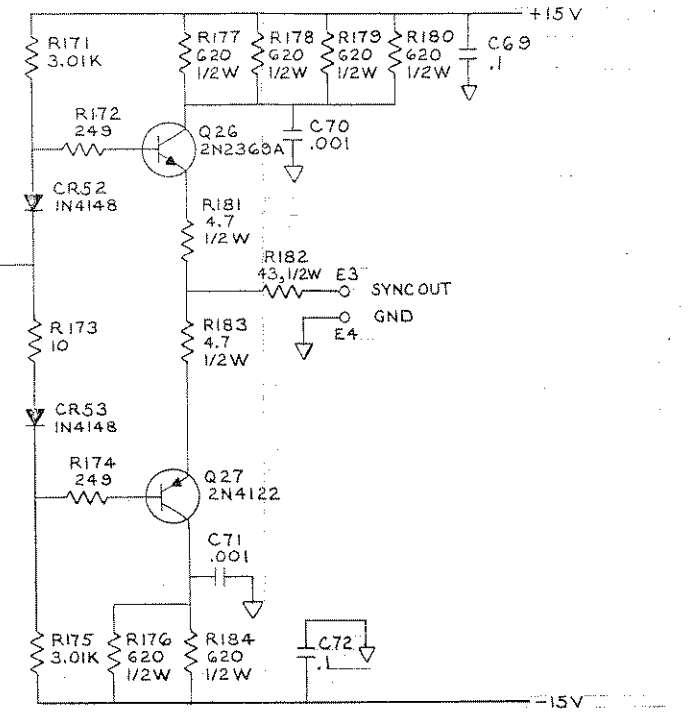
FUNCTION SELECT

SINE CONVERTER





SYNC DRIVER



J9
LOGIC

FRQ	1	FRQ
AMP	2	AMP
OST	3	OST
TRL	4	TRL
ANLØ	5	$\overline{FRØ}$
ANL1	6	$\overline{FR1}$
ANL2	7	$\overline{FR2}$
ANL3	8	$\overline{FR3}$
ANL4	9	$\overline{FR4}$
ANL5	10	$\overline{FR5}$
ANL6	11	$\overline{FR6}$
ANL7	12	$\overline{FR7}$
ANL8	13	OAØ
ANL9	14	
ANL10	15	OA2
ANL11	16	MCØ
ANL12	17	MC1
ANL13	18	$\overline{DCA}$
ANL14	19	$\overline{OVR}$
ANL15	20	$\overline{CPM}$
ANL16	21	-TR
ANL17	22	+TR
ANL18	23	EXW
ANL19	24	$\overline{SQR}$
ANL20	25	SQR
ANL21	26	$\overline{SIN}$
ANL22	27	$\overline{TRI}$
ANL23	28	$\overline{RCT}$
ANL24	29	$\overline{PLS}$
ANL25	30	PLS
ANL26	31	
ANL27	32	
PORTIØ	33	OAP
PORTI1	34	FUB

J14
AUX

GND	1	
VCG1	2	VCG1
GND	3	
VCGO	4	VCGO
GND	5	
GND	6	
TRG1	7	TRG1
GND	8	
TRGO	9	TRGO
GND	10	
PLSI	11	PLSI
GND	12	
SQS	13	SQS
GND	14	

J23
TEST

PATEST	1	PATEST
+15V	2	+15VT
-15V	3	-15VT
+5V	4	GND
	5	+5VT
	6	GND
TRITST	7	TRITST
	8	GND
DCCOMP	9	DCCOMP
	10	GND
VCGTST	11	VCGTST
	12	GND
AMPLDC	13	AMPLDC
	14	GND

R185 R186 R187 100(3)

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S.THOMPSON	DATE 11-23-81	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE SCHEMATIC FUNCTION GENERATOR BOARD (A7)
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG	MODEL NO. 275	DWG NO. 0103-00-1101 REV. E
	SCALE	CODE IDENT 23338	SHEET 3 OF 4

PREAMPLIFIER

OUTPUT AMPLIFIER

XY MULTIPLIER

OUTPUT ATTENUATOR

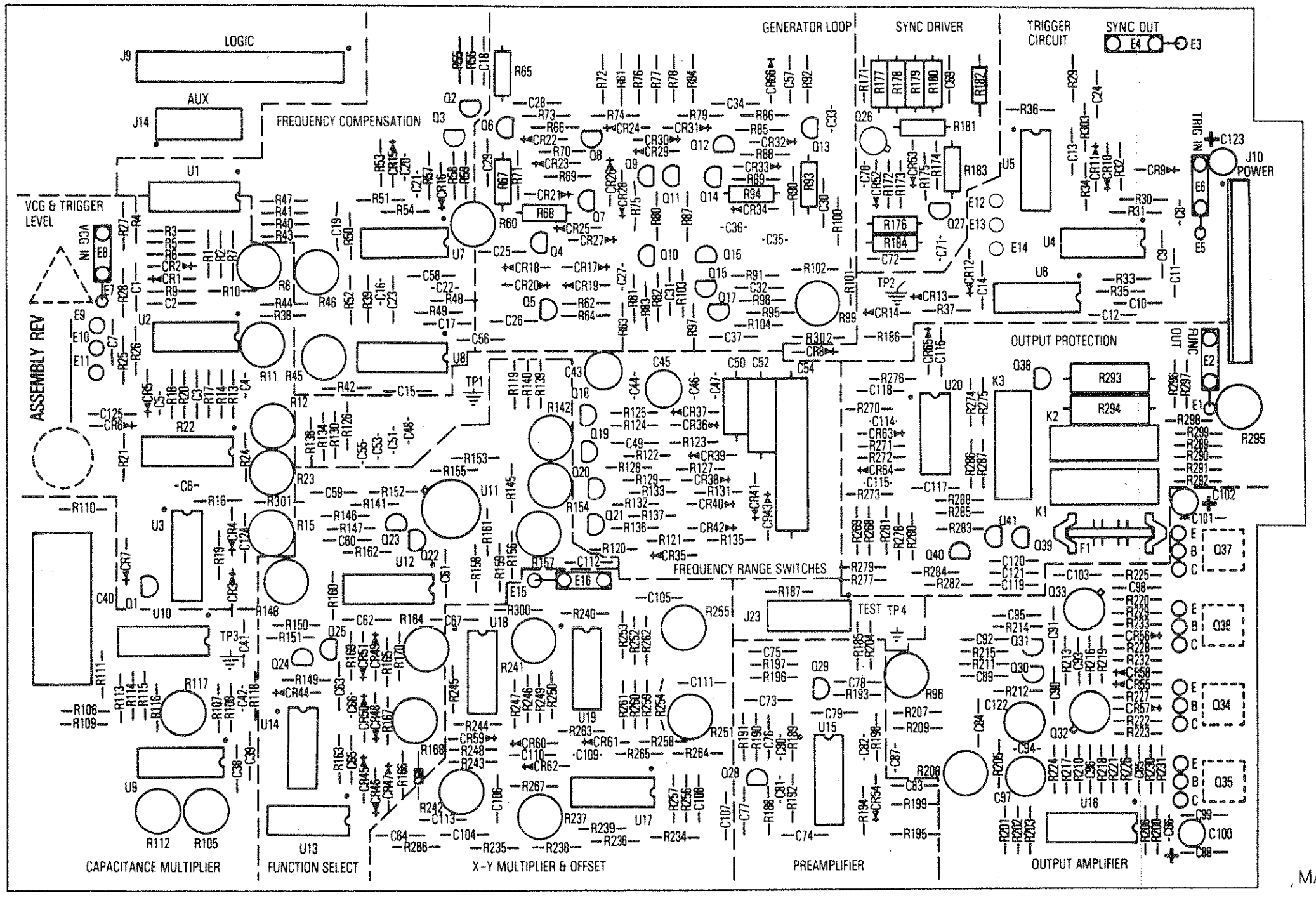
OUTPUT PROTECTION

XY MULTIPLIER & OFFSET

5. SEE PAGE 1 NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S.THOMPSON	DATE 11-23-81	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJENGR PGA	7/5/83	TITLE SCHEMATIC FUNCTION GENERATOR BOARD (A7)
FINISH WAVETEK PROCESS	RELEASE APPROV PGA		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX : 010 ANGLES : 1° XX : 030		MODEL NO. 275
	DO NOT SCALE DWG		DWG NO. 0103-00-1101 REV
	SCALE		CODE IDENT 23338 SHEET 4 OF 4

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-2894



MADE FROM 0100-00-0920-3F

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROTENCR		TITLE: FUNCTION GENERATOR ASSEMBLY
	RELEASE APPROV		
FINISH: WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG		MODEL NO: 275 / DWG NO: 1100-00-1101 / REV
	SCALE		CODE IDENT: 23338 / SHEET 1 OF 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, FUNCTION GENERATOR	0101-00-1101	WVTK	0101-00-1101	1
NONE	SCHEMATIC, FUNCTION GENERATOR	0103-00-1101	WVTK	0103-00-1101	1
F1	PCA, OUTPUT FUSE BD	1200-00-0977	WVTK	1200-00-0977	1
NONE	ASSY, XSISTOR MNTG ANGLE	270-1009	WVTK	1206-00-1009	1
C22 C27 C35 C36	CAP, CER, 5PF, 1KV	DD-050	CRL	1500-00-5011	4
C114 C115 C16 C20 C21 C8 C94	CAP, CER, 10PF, 1KV	DD-100	CRL	1500-01-0011	7
C4 C5	CAP, CER, 100PF, 1KV	DD-101	CRL	1500-01-0111	2
C33 C48 C51 C53 C55 C70 C71 C87	CAP, CER, .01MFD, 1KV	DD-102	CRL	1500-01-0211	8
C42	CAP CER MON .01MF 50V, AXIAL	CAC02Z5U103Z100A	CORNG	1500-01-0310	1
C1 C10 C101 C103 C104 C105 C106 C107 C108 C11 C110 C111 C112 C113 C116 C117 C118 C119 C12 C120 C121 C124 C125 C13 C14 C15 C17 C18 C19 C2 C23 C24 C25 C26 C28 C29 C3 C30 C31 C32 C34 C37 C38 C39 C41 C49 C56 C57 C58 C59 C60 C61 C62 C63 C64	CAP, CER, MON, .1MF, 50V, AXIAL	CAC03Z5U104Z050A	CORNG	1500-01-0405	82

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GEN BD | ASSEMBLY NO. 1100-00-1101 | REV F | PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C65 C67 C68 C69 C7 C72 C73 C74 C75 C76 C77 C78 C79 C83 C84 C85 C88 C89 C9 C90 C91 C92 C93 C95 C96 C98 C99					
C86	CAP, CER, 150PF, 1KV	DD-151	CRL	1500-01-5111	1
C126 C127 C82	CAP, CER, 1.5PF, 1KV	NCD1.5PF1KVK750-CR	NIC	1500-01-5507	3
C109 C66	CAP, CER, 22PF, 1KV	DD-220	CRL	1500-02-2011	2
C6	CAP, CER, 220PF, 1KV	DD-221	CRL	1500-02-2111	1
C80 C81	CAP CER MON 2.7PF 50V	IMCAC2R7D	ARCO	1500-02-7505	2
C44T	CAP, CER, 33PF, 1KV	DD-330	CRL	1500-03-3011	1
C46	CAP, MICA, 56PF, 500V	DM15-560J	ARCO	1500-15-6000	1
C47	CAP, MICA, 820PF, 300V	DM15-821F	ARCO	1500-18-2101	1
C40	CAP, MYLR, 2MF, 200V	2MFW205K	AMRAD	1500-42-0504	1
C122 C43	CAP, VAR, 3.5-13PF, 250V	7S-TRIK0-02 3.5/13PF	TRIKO	1500-51-3000	2
C45 C97	CAP, VAR, 7-35PF 250V	7S-TRIK0-02 7/35 PF	TRIKO	1500-53-5000	2
C100 C102 C123	CAP, TANT, 22MF, 15V	196D226X9015KA1	SPRAG	1500-72-2601	3
C50 C52 C54	CAP SET, POLYC MIXED MATCHED SET	180-501	WVTK	1509-80-0008	1

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GEN BD | ASSEMBLY NO. 1100-00-1101 | REV F | PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	FUNCTION GENERATOR	270-0920	WVTK	1700-00-0920	1
J10	CONN, HEADER	09-60-1101	MOLEX	2100-02-0088	1
J14	CONN, HOUSING, 14 PIN WITH POLARIZING TABS	2100-02-0136	WVTK	2100-02-0136	1
J9	CONN, HOUSING, 34 PIN WITH POLARIZING TABS	2100-02-0138	WVTK	2100-02-0138	1
NONE	TERM	2000B1	USECO	2100-05-0009	12
TP1 TP2 TP3 TP4	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	4
J23	CONN, HEADER, 14 PIN 2X7	CA-D14RSP100-230-090	CA	2100-05-0053	1
NONE	SPACER, HINGED .750H, .250D&-32 THD	LT3021	LYNTR	2800-03-0009	2
NONE	SPACER .750H, .250 HEX&-32 THRU	2323	SMITH	2800-03-0010	2
NONE	SPACER, SWAGE .562H, .250 DIA	BR6310B-0.562-31	LYNTR	2800-04-0017	3
NONE	HEAT SINK	207	WAKE	2800-11-0001	2
NONE	TRANSIPAD	10160	METRS	2800-11-0004	2
NONE	JUMPER	451-2871-01-03-10	CAMBN	3000-00-0034	2
E10 E11 E12 E13 E14 E9	PINS, JUMPER	450-3704-01-03	CAMBN	3000-00-0035	6

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GEN BD | ASSEMBLY NO. 1100-00-1101 | REV F | PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	DIGI-CLIP	MC-20	CMPCP	3000-00-0093	4
NONE	DIGI-GUIDE	MC-10-1/2	CMPCP	3000-00-0094	2
K1 K2 K3	RELAY, REED, FORM-A	1503-10-2	WABSH	4500-00-0007	3
R295	POT, TRIM, 20	91AR20	BECK	4600-02-0000	1
R11 R117 R12 R15 R251	POT, TOP TRIM, 20T, 100K	68WR100K	BECK	4609-90-0001	5
R99	POT, TOP TRIM, 20T, 10K	68WR10K	BECK	4609-90-0002	1
R105 R255 R46	POT, TOP TRIM, 20T, 20K	68WR20K	BECK	4609-90-0003	3
R237 R242 R45	POT, TOP TRIM, 20T, 2K	68WR2K	BECK	4609-90-0004	3
R241 R8	POT, TOP TRIM, 20T, 1K	68WR1K	BECK	4609-90-0005	2
R164 R168	POT, TOP TRIM, 20T, 5K	68WR5K	BECK	4609-90-0013	2
R206 R23	POT, TOP TRIM, 20T, 100	68WR100	BECK	4609-90-0019	2
R112 R142 R148 R96	POT, TOP TRIM, 20T, 200	68WR200	BECK	4609-90-0020	4
R154 R157 R60	POT, 20T, TOP TRIM, 500 OHM	68WR500	BECK	4609-90-0023	3
R182	RES, C, 1/2W, 5%, 43	RCR20G430JS	AB	4700-25-0430	1
R181 R183 R65 R67 R68 R93 R94	RES, C, 1/2W, 5%, 4.7	RC-1/2-4R7J	STKPL	4700-25-0479	7

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GEN BD | ASSEMBLY NO. 1100-00-1101 | REV F | PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R176 R177 R178 R179 R180 R184	RES, C, 1/2W, 5%, 620	RC-1/2-621J	STKPL	4700-25-6200	6
R189 R192 R194 R198	RES, MF, 1/8W, .1%, 750	RN55E-7500B	MEPCO	4701-02-7500	4
R109 R119 R140 R149 R185 R186 R187 R211 R213 R220 R222 R244 R247 R250 R261 R66 R69 R80 R85 R89	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	20
R103 R14 R17 R18 R191 R197 R20 R201 R202 R256 R257 R42 R82 R98	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	14
R102 R104 R107 R108 R116 R147 R188 R193 R204 R234 R264 R265 R301 R302 R38 R40 R52 R54 R57 R6 R95	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	21
R285 R287 R33 R35	RES, MF, 1/8W, 1%, 100K	RN55D-1003F	TRW	4701-03-1003	4
R10 R16 R270 R273 R276 R286 R288 R298 R299 R3	RES, MF, 1/8W, 1%, 1M	RN55D-1004F	TRW	4701-03-1004	10
R110 R173 R219 R226 R227 R228 R229 R230 R231 R232 R233 R296 R70 R88 R97	RES, MF, 1/8W, 1%, 10	RN55D10R0F	MEPCO	4701-03-1009	15
R245 R246 R248 R81	RES, MF, 1/8W, 1%, 1.1K	RN55D-1101F	TRW	4701-03-1101	4
R118 R249 R262	RES, MF, 1/8W, 1%, 1.21K	RN55D-1211F	TRW	4701-03-1211	3
R297	RES, MF, 1/8W, 1%, 12.4	RN55D-12R4F	TRW	4701-03-1249	1

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GEN BD | ASSEMBLY NO. 1100-00-1101 | REV F | PAGE 5

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R165 R167	RES, MF, 1/8W, 1%, 13K	RN55D-1302F	TRW	4701-03-1302	2
R153 R156 R200 R207 R210 R92	RES, MF, 1/8W, 1%, 150	RN55D-1500F	TRW	4701-03-1500	6
R278 R39	RES, MF, 1/8W, 1%, 15K	RN55D-1502F	TRW	4701-03-1502	2
R1 R2	RES, MF, 1/8W, 1%, 150K	RN55D-1503F	TRW	4701-03-1503	2
R62	RES, MF, 1/8W, 1%, 15.8K	RN55D-1582F	TRW	4701-03-1582	1
R238	RES, MF, 1/8W, 1%, 1.62K	RN55D-1621F	TRW	4701-03-1621	1
R59 R84	RES, MF, 1/8W, 1%, 1.78K	RN55D-1781F	TRW	4701-03-1781	2
R139	RES, MF, 1/8W, 1%, 182	RN55D-1820F	TRW	4701-03-1820	1
R289 R290 R291 R292	RES, MF, 1/8W, 1%, 1.96K	RN55D-1961F	TRW	4701-03-1961	4
R163 R212 R214 R263 R56 R76 R78	RES, MF, 1/8W, 1%, 2K	RN55D-2001F	TRW	4701-03-2001	7
R125 R129 R133 R137 R26 R304 R305 R43	RES, MF, 1/8W, 1%, 20K	RN55D-2002F	TRW	4701-03-2002	8
R221 R225	RES, MF, 1/8W, 1%, 21.5	RN55D-21R5F	TRW	4701-03-2159	2
R100 R101 R203	RES, MF, 1/8W, 1%, 221	RN55D-2210F	TRW	4701-03-2210	3
R126 R130 R134 R138 R280	RES, MF, 1/8W, 1%, 2.21K	RN55D-2211F	TRW	4701-03-2211	5
R24	RES, MF, 1/8W, 1%, 23.7K	RN55D-2372F	TRW	4701-03-2372	1

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GEN BD | ASSEMBLY NO. 1100-00-1101 | REV F | PAGE 6

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES | MATERIAL | FINISH WAVETEK PROCESS | DRAWN | DATE | PROJ ENGR | RELEASE APPROV | TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030 | DO NOT SCALE DWG | SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE: PARTS LIST PCA, FUNCTION GEN BD

MODEL NO. 275 | DWG NO. 1100-00-1101 | REV F | CODE IDENT 23338 | SHEET 1 OF 2

REV	ECN	BY	DATE	APP

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R44	RES, MF, 1/8W, 1%, 243K	RN55D-2433F	TRW	4701-03-2433	1
R172 R174	RES, MF, 1/8W, 1%, 249	RN55D-2490F	TRW	4701-03-2490	2
R160 R162 R170 R195 R266 R300 R303 R32 R34 R36 R71 R83 R9	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	13
R155 R159 R213	RES, MF, 1/8W, 1%, 24.9K	RN55D-2492F	TRW	4701-03-2492	3
R239 R252	RES, MF, 1/8W, 1%, 27.4K	RN55D-2742F	TRW	4701-03-2742	2
R161 R253 R259	RES, MF, 1/8W, 1%, 27.4	RN55D-27R4F	TRW	4701-03-2749	3
R171 R175 R282 R284	RES, MF, 1/8W, 1%, 3.01K	RN55D-3011F	TRW	4701-03-3011	4
R25	RES, MF, 1/8W, 1%, 30.1K	RN55D-3012F	TRW	4701-03-3012	1
R41	RES, MF, 1/8W, 1%, 301K	RN55D-3013F	TRW	4701-03-3013	1
R73 R75 R87	RES, MF, 1/8W, 1%, 332	RN55D-3320F	TRW	4701-03-3320	3
R206 R30	RES, MF, 1/8W, 1%, 3.32K	RN55D-3321F	TRW	4701-03-3321	2
R152 R158	RES, MF, 1/8W, 1%, 33.2K	RN55D-3322F	TRW	4701-03-3322	2
R63 R74 R79	RES, MF, 1/8W, 1%, 33.2	RN55D-33R2F	TRW	4701-03-3329	3
R7	RES, MF, 1/8W, 1%, 3.57K	RN55D-3571F	TRW	4701-03-3571	1
R86	RES, MF, 1/8W, 1%, 392	RN55D-3920F	TRW	4701-03-3920	1

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GEN BD | ASSEMBLY NO. 1100-00-1101 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R205	RES, MF, 1/8W, 1%, 42.2	RN55D-42R2F	TRW	4701-03-4229	1
R209	RES, MF, 1/8W, 1%, 464	RN55D-4640F	TRW	4701-03-4640	1
R120 R141 R149	RES, MF, 1/8W, 1%, 4.64K	RN55D-4641F	TRW	4701-03-4641	3
R240	RES, MF, 1/8W, 1%, 4.75K	RN55D-4751F	TRW	4701-03-4751	1
R77	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	1
R166 R19 R21 R216 R235 R236 R256 R260 R27 R277 R279 R28 R281 R283 R29 R4 R5 R50 R51 R53 R55 R58 R91	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	23
R106	RES, MF, 1/8W, 1%, 49.9K	RN55D-4992F	TRW	4701-03-4992	1
R13 R254 R268 R269 R47	RES, MF, 1/8W, 1%, 499K	RN55D-4993F	TRW	4701-03-4993	5
R218	RES, MF, 1/8W, 1%, 51.1	RN55D-51R1F	TRW	4701-03-5119	1
R190 R196 R90T	RES, MF, 1/8W, 1%, 5.76K	RN55D-5761F	TRW	4701-03-5761	3
R72	RES, MF, 1/8W, 1%, 6.19K	RN55D-6191F	TRW	4701-03-6191	1
R150	RES, MF, 1/8W, 1%, 681	RN55D-6810F	TRW	4701-03-6810	1
R146 R151 R61 R64	RES, MF, 1/8W, 1%, 6.98K	RN55D-6981F	TRW	4701-03-6981	4
R199 R224	RES, MF, 1/8W, 1%, 750	RN55D-7500F	TRW	4701-03-7500	2
R121 R122 R243 R267 R31	RES, MF, 1/8W, 1%, 7.5K	RN55D-7501F	TRW	4701-03-7501	5

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GEN BD | ASSEMBLY NO. 1100-00-1101 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R271 R272 R274 R275	RES, MF, 1/8W, 1%, 78.7K	RN55D-7872F	TRW	4701-03-7872	4
R111	RES, MF, 1/8W, 1%, 825	RN55D-8250F	TRW	4701-03-8250	1
R37	RES, MF, 1/8W, 1%, 8.25K	RN55D-8251F	TRW	4701-03-8251	1
R217	RES, MF, 1/8W, 1%, 909	RN55D-9090F	TRW	4701-03-9090	1
R124 R128 R132 R136 R223	RES, MF, 1/8W, 1%, 90.9	RN55D-90R9F	TRW	4701-03-9099	5
R293 R294	RES, MF, 1W, 1%, 100	RN70D-1000F	TRW	4701-33-1000	2
R22	RES NETWORK 1K 2W 16PIN DIP	4116R-001-102	BOURN	4770-00-0019	1
R113 R114 R115	RES, MF, MIXED SET	4789-00-0043	WVTK	4789-00-0043	1
R123 R127 R131 R135 R48 R49	RES, MF, 1/4W, 1%, 10M	CC1005F	AB	4799-00-0056	6
CR11 CR15 CR16 CR54 CR61	DIODE, ZENER, 5.1V, 5% TOL, 500MW, G/B, IN751A	1N751A	FAIR	4801-01-0751	5
CR60	DIODE, ZENER, 6.2V, IN823	1N823A	MOT	4801-01-0823	1
CR4 CR6 CR66	DIODE, ZENER 500MW SILICON PLANAR	1N959	SIEM	4801-01-0959	3
CR21 CR34	DIODE, ZENER 10V, GLASS SILICON, 1W	1N4740A	MOT	4801-01-4740	2
CR36 CR37 CR38 CR39 CR40	DIODE, HIGH	1N5282	FAIR	4801-01-5282	10

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GEN BD | ASSEMBLY NO. 1100-00-1101 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
CR41 CR42 CR43 CR57 CR58	CONDUCTANCE, ULTRA FAST				
CR17 CR18 CR19 CR20 CR29 CR30 CR48 CR49 CR50 CR51	DIODE, ULTRA FAST	FD777	FAIR	4807-02-0777	10
CR1 CR10 CR12 CR13 CR14 CR22 CR23 CR25 CR26 CR27 CR28 CR3 CR32 CR33 CR35 CR44 CR45 CR46 CR47 CR5 CR52 CR53 CR55 CR56 CR59 CR62 CR63 CR64 CR65 CR9	DIODE 1N4148 COMPUTER, O/P, 75V, 200MA, SWITCHING	1N4148	FAIR	4807-02-6666	31
CR24 CR31	DIODE 5082-2811 SCHOTTKY, 15V, 20MA	5082-2811	HP	4809-02-2811	2
CR7 CR8	DIODE, M/PR, FD-777 QTY: 2: 4807-02-0777	164-501-93	WVTK	4898-00-0004	1
G33 G34 G35	TRANS 2N2219A NPN GENERAL PURPOSE TO-5	2N2219A	NSC	4901-02-2191	3
G26	TRANS, SILICON PLANAR, EPITAXIAL NPN	2N2369A	MOT	4901-02-3691	1
G32 G36 G37	TRANS 2N2905A PNP GENERAL PURPOSE TO-5	2N2905A	NSC	4901-02-9051	3
G10 G11 G13 G16 G30 G6 G9	TRANS, NPN, TO-92	2N3563	FAIR	4901-03-5630	7
G38	TRANS, GENERAL PURPOSE, PNP, TO-92	2N3638A	CARTR	4901-03-6381	1

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GEN BD | ASSEMBLY NO. 1100-00-1101 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
G1	TRANS, GENERAL PURPOSE, NPN, TO-92	2N3903	NSC	4901-03-9030	1
G17 G39 G40 G41	TRANS 2N3904 NPN GENERAL PURPOSE TO-92	2N3904	FAIR	4901-03-9040	4
G18 G19 G20 G21 G23 G24	TRANS 2N3906 PNP GENERAL PURPOSE TO-92	2N3906	FAIR	4901-03-9060	6
G27	TRANS, GENERAL PURPOSE, PNP, TO-92	2N4122	NSC	4901-04-1220	1
G2 G4	TRANS, P-CHANNEL JFETS	2N5462	MOT	4901-05-4620	2
G15 G3 G5	TRANS, N-CHANNEL JFETS	2N5485	MOT	4901-05-4850	3
G12 G14 G22 G25 G28 G29 G31 G7 G8	TRANS 2N5771 PNP SWITCH TO-92	2N5771	NSC	4901-05-7710	9
R145	THERMISTER	1K-501-K	MCI	5300-00-0011	1
U9	OP AMP, DUAL JFET INPUT	TL083CN	TI	7000-00-8300	1
U17 U2 U7	OP AMP, QUAD BIMOS MOS/FET INPUT	TL084CN	TI	7000-00-8400	3
U20	COMPARATORS, QUAD VOLTAGE	MLM339P	MOT	7000-03-3900	1
U4	IC	NE529N	SIG	7000-05-2900	1

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GEN BD | ASSEMBLY NO. 1100-00-1101 | REV F

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U11	DIODE, ULTRA FAST, LOW CAPACITANCE	CA-3019	RCA	7000-30-1900	1
U18 U19	TRANS ARRAY, DIFFERENTIAL AMP, DUAL IN	CA-3054	RCA	7000-30-5400	2
U15	TRANS ARRAY, GENERAL PURPOSE, NPN	CA3083	FAIR	7000-30-8300	1
U16 U3	TRANS ARRAY, NPN/PNP	CA-3096AE	RCA	7000-30-9600	2
U1 U10 U12 U8	SW, QUAD ANALOG, CMOS	DG211CJ	SILCON	8000-02-1100	4
U13 U5	GATE, NAND, QUAD 2INP, TTL	74F00PC	FAIR	8000-74-0002	2
U14	4-2-3-2 INP ADI, TTL	74F64PC	FAIR	8000-74-6402	1
U6	FLIP-FLOP DUAL, D-POS EDGE TRIG, TTL	74F74PC	FAIR	8000-74-7402	1

WAVETEK PARTS LIST | TITLE: PCA, FUNCTION GEN BD | ASSEMBLY NO. 1100-00-1101 | REV F

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES | MATERIAL | FINISH WAVETEK PROCESS | DRAWN | DATE | PROJ ENGR | RELEASE APPROV | TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030 | DO NOT SCALE DWG | SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE: PARTS LIST PCA, FUNCTION GEN BD

MODEL NO. 275 | DWG NO. 1100-00-1101 | REV F | CODE IDENT 23338 | SHEET 2 OF 2

MICROPROCESSOR/MEMORY

GPIB INTERFACE

A	ECN 4777	RO	5-84	/6
B	ECO # 89-010	NS	1-24-89	DMB

TEST J8

MICROPROCESSOR

ADDRESS LATCH

GPIB ADDRESS

DATA LATCH

ROM

RAM

WRITE PULSE

IEEE-488 INTERFACE

ALTERNATE BUS DRIVERS

IEEE488 BUS DRIVERS

ADDRESS DECODER

P/N 8600-00-0237

RAM PWR (2A2)

1. REFERENCE DESIGNATORS SHOWN ARE PARTIAL, PREFIX WITH ASSEMBLY REF DES (A6).
2. ALL DIODES ARE FD6666.
3. ALL RESISTORS ARE SHOWN IN OHMS.
4. ALL CAPACITORS ARE SHOWN IN MICRO-FARADS.
5. LAST REFERENCE DESIGNATORS USED ARE: R61, C72, CR19, VR4, SW1, U29, Q2, BT1
6. PROM'S PROGRAMMED PER MODEL, SEE PARTS LIST.

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S.CHERMACK	DATE 1-8-83	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR R.B.C.	7/8/87	TITLE: SCHEMATIC MICRO PROC/POWER SUPPLY BOARD (A6)
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.030 ANGLES ±1°		
	DO NOT SCALE DWG		MODEL NO. 270 SERIES; DWG NO. 0103-00-2202; REV B
	SCALE		CODE IDENT 23338; SHEET 1 OF 3

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

SAMPLE AND HOLD

DAC

-10.24V REF
R17 6.81K
-10.24V
TP1
+15V
R15 10K
R16 200
U16B
TL082
-10.24 REF ADJ
C22 .1/50V +15V
C23 .1/50V +15V
U16A
TL082
C24 .1/50V -15V
ADRØ
U15 DAC 1006
DATAØ
DATA 1
DATA 2
DATA 3
DATA 4
DATA 5
DATA 6
DATA 7

ANALOG DECODER

+5V
R14 2.2K SIP
U14A 1/2 LS139
ADR 3
ADR 4
ANALOG
ANAØ
ANA1
ANA2
ANA3
C21 .1/50V +5V
U14B 1/2 LS139
ADRØ
ADR 1
ARØ
AR1
AR2
AR3

SAMPLE AND HOLD

C25 .1/50V +15V +5V
C20 .1/50V +5V
1/4 DG211 U17A
C26 .1/50V -15V
C27 22 pF
U18F LS04
R18 301K
R19 301K
TL082
C64 .1/50V +15V
U19B
C65 .1/50V -15V
C28 1 mf POLYE
C29 910 pF SM
C30 910 pF SM
1/4 DG211 U17D
C31 22 pF
U18A LS04
R20 301K
R21 301K
U19A
TL082
C32 .1 POLYE
C33 910 pF SM
C34 910 pF SM
1/4 DG211 U17B
C35 22 pF
U18C LS04
R22 301K
R23 301K
TL082
C66 .1/50V +15V
U20A
C67 .1/50V -15V
C36 .1 POLYE
C37 910 pF SM
C38 910 pF SM
1/4 DG211 U17C
C39 22 pF
U18D LS04
R24 301K
R25 301K
U20B
TL082
C40 .1 POLYE
C41 910 pF SM
C42 910 pF SM

BATTERY TEST AND RESET

+5V
C71 .1/50V
R59 4.99
R57 1M
CR18
2811(2)
CR19
R58 1M
+15V
TL082
U27B
C72 .1/50V
R61 10K
R60 10K
MR
Q2 2N3904
CR17
CR6
PORT 15
+5V
+15V
R29 27.4K
TL082
BATV
U27A
R26 12.4K
R28 2.37K
R27 1M
-15V
R30 10K
R31 3.83K
PORT 14
R56 6.19K

DISPLAY

J7
1 +45V
2
3
4
5
6
7 +5V
8 KYBD
9 PORT 21
10 PORT 16
11 DISP
12
13 AD4
14 AD3
15 AD2
16 AD1
17 ADØ
18 ADR 3
19 ADR 2
20 ADR 1
21 ADRØ
22
23 DATA 7
24 DATA 6
25 DATA 5
26 DATA 4
27 DATA 3
28 DATA 2
29 DATA 1
30 DATA Ø
31
32
33
34 +15V.

NOTE: UNLESS OTHERWISE SPECIFIED

AUX BUFFERS

+5V
U29 LS244
DATA Ø
DATA 1
DATA 2
DATA 3
DATA 4
DATA 5
DATA 6
DATA 7
B DATA Ø
B DATA 1
B DATA 2
B DATA 3
B DATA 4
B DATA 5
B DATA 6
B DATA 7
U28 LS244
PORT 12
N.C.
ADR Ø
ADR 1
ADR 2
B ADRØ
B ADR 1
B ADR 2

ANALOG REGISTERS

+5V
ARØ
U21 C374
C43 .1/50V
ANLØ
ANL 1
ANL 2
ANL 3
ANL 4
ANL 5
ANL 6
ANL 7
AR1
U22 C374
C44 .1/50V
ANL 8
ANL 9
ANL 10
ANL 11
ANL 12
ANL 13
ANL 14
ANL 15
AR2
U23 C374
C45 .1/50V
ANL 16
ANL 17
ANL 18
ANL 19
ANL 20
ANL 21
ANL 22
ANL 23
AR3
U24 C374
C46 .1/50V
ANL 24
ANL 25
ANL 26
ANL 27

ANALOG

J6
SHØ → 1
SH1 → 2
SH2 → 3
SH3 → 4
ANLØ → 5
ANL 1 → 6
ANL 2 → 7
ANL 3 → 8
ANL 4 → 9
ANL 5 → 10
ANL 6 → 11
ANL 7 → 12
ANL 8 → 13
ANL 9 → 14
ANL 10 → 15
ANL 11 → 16
ANL 12 → 17
ANL 13 → 18
ANL 14 → 19
ANL 15 → 20
ANL 16 → 21
ANL 17 → 22
ANL 18 → 23
ANL 19 → 24
ANL 20 → 25
ANL 21 → 26
ANL 22 → 27
ANL 23 → 28
ANL 24 → 29
ANL 25 → 30
ANL 26 → 31
ANL 27 → 32
PORT 10 → 33
PORT 11 → 34

AUX

J4
B DATA Ø → 1
B DATA 1 → 2
B DATA 2 → 3
B DATA 3 → 4
B DATA 4 → 5
B DATA 5 → 6
B DATA 6 → 7
B DATA 7 → 8
B ADR Ø → 9
B ADR 1 → 10
B ADR 2 → 11
ANA 2 → 12
ANA 3 → 13
14
15
16
17
18
19
RAM PWR (1A5)
PORT 13 → 20

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN S.CHERMACK DATE 1-8-83
PROJ ENGR R.B.4 7/16/83
RELEASE APPROV
TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.020
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO • CALIFORNIA

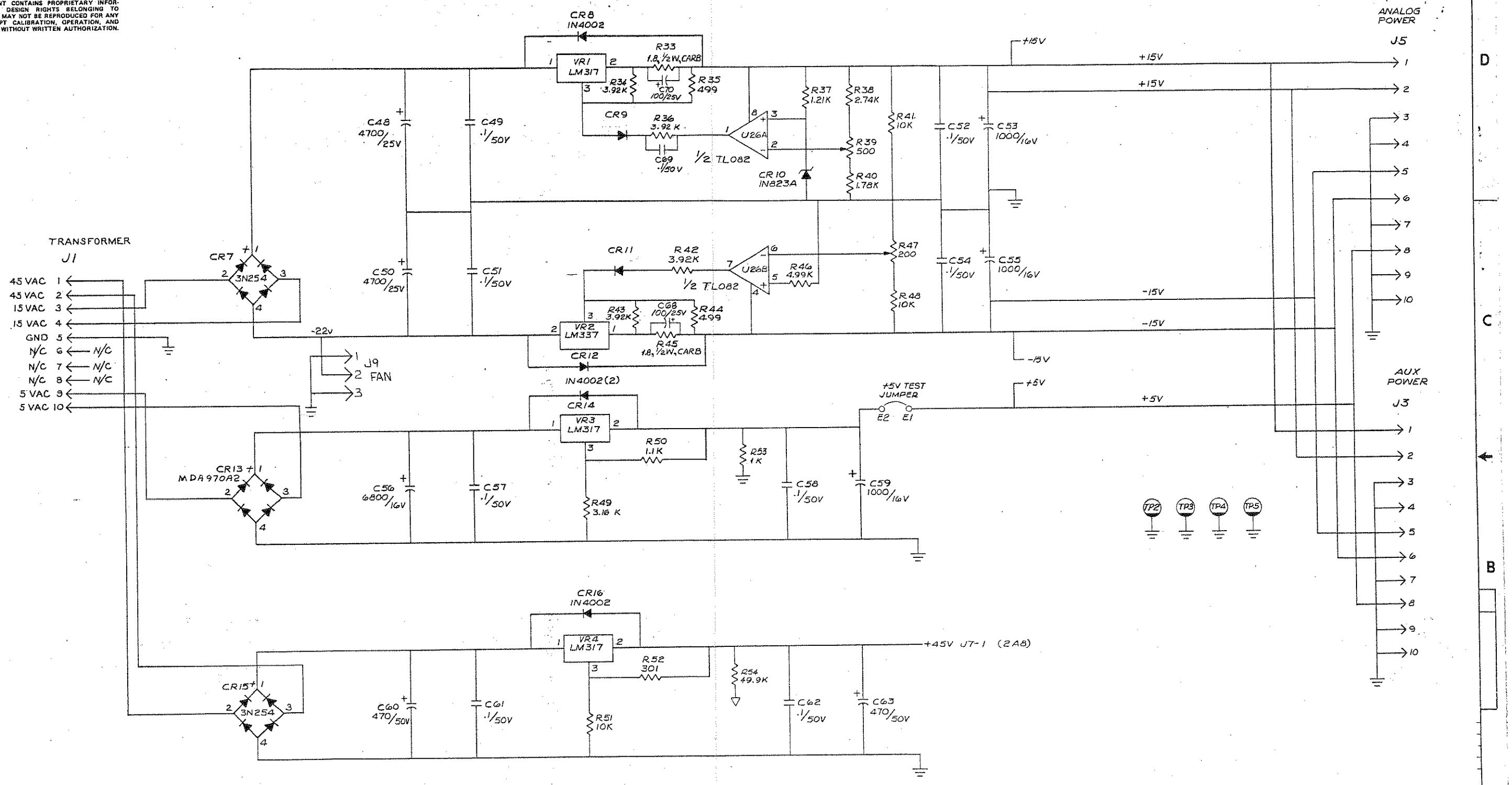
TITLE
SCHEMATIC MICRO PROC/POWER SUPPLY BOARD (A6)

MODEL NO.	DWG NO.	REV
270 SERIES	0103-00-2202	AB
CODE IDENT 23338	SHEET 2 OF 3	

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3994

ANALOG INTERFACE

POWER SUPPLY

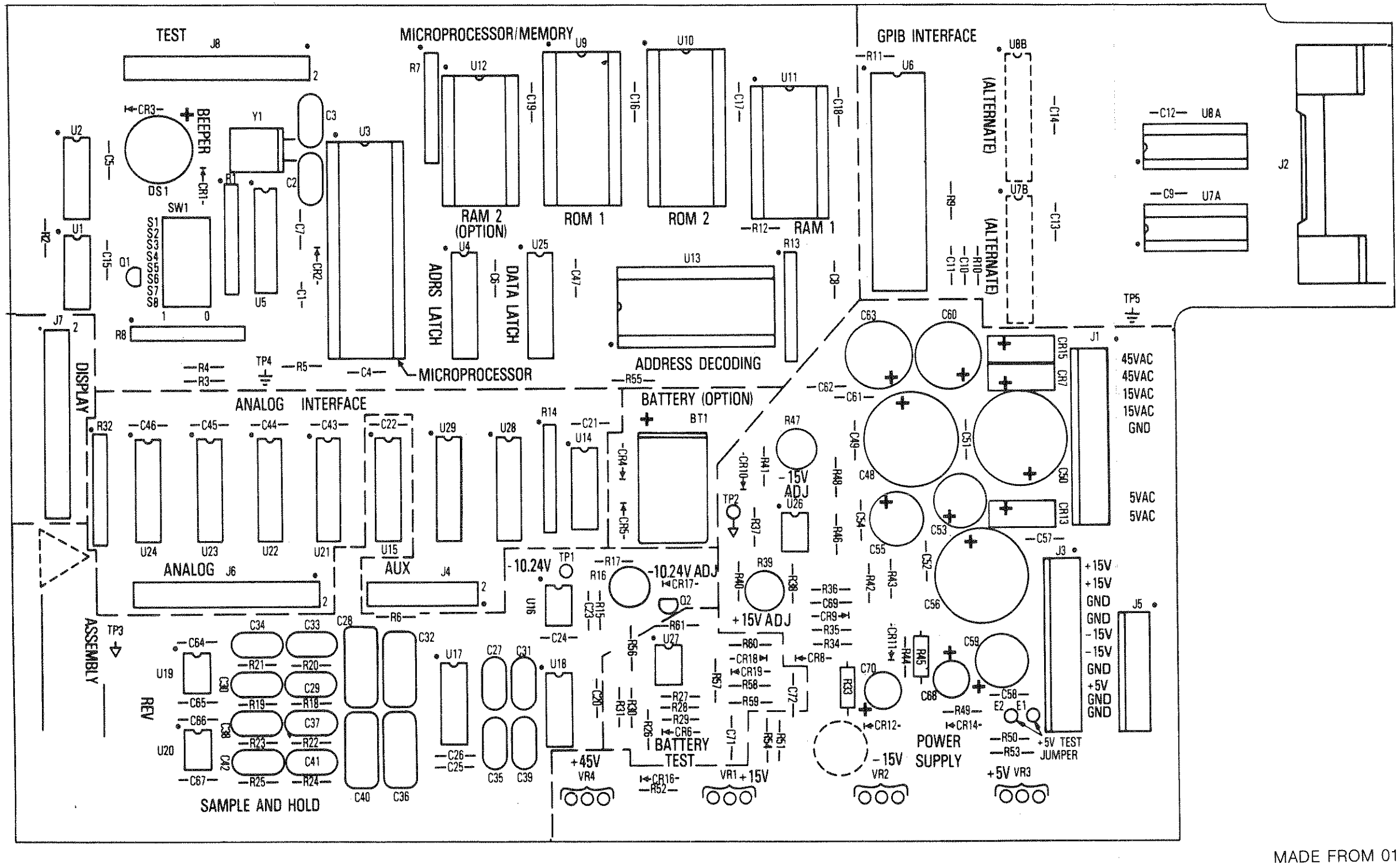


NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S.CHERMACK	DATE 4-8-83	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR R.B.L	7/15/83	TITLE: SCHEMATIC MICRO PROC/POWER SUPPLY BOARD (A6)
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 XX ±.030 ANGLES ±1°		
	DO NOT SCALE DWG		MODEL NO. 270 SERIES · DWG NO. 0103-00-2202 · REV B
	SCALE		CODE IDENT 23338 · SHEET 3 OF 3

REV	ECN	BY	DATE	APP

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3994



MADE FROM 0100-00-2202-3A

WAVETEK SAN DIEGO, CALIFORNIA

TITLE: MICRO PROC/POWER SUPPLY

MODEL NO.	ASSY NO.	REV
275	1100-00-2202	
CODE IDENT 23338	SHEET 1 OF 1	

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, MICRO-PROC/GPIB BOARD	0101-00-2202	WVTK	0101-00-2202	1
NONE	SCHEMATIC MICRO-PROC/GPIB BOARD	0103-00-2202	WVTK	0103-00-2202	1
C1	CAP, CER, .001MF, 1KV	DD-102 LONG LEAD	CRL	1500-01-0201	1
C10 C11 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C4 C43 C44 C45 C46 C47 C49 C5 C51 C52 C54 C57 C58 C6 C61 C62 C64 C65 C66 C67 C69 C7 C71 C72 C8	CAP, CER, MON, .1MF, 50V, AXIAL	CAC03Z5U104Z050A	CORNG	1500-01-0405	41
C27 C31 C35 C39	CAP, CER, 22PF, 1KV	DD-220	CRL	1500-02-2011	4
C2 C3	CAP, MICA, 27PF, 500V	DM15-270J	ARCO	1500-12-7000	2
C29 C30 C33 C34 C37 C38 C41 C42	CAP, 910PF, 100V, 5%	DM15-911J	ARCO	1500-19-1100	8
C68 C70	CAP, ELECT, 100MF, 35V RADIAL LEAD, SP .20	ULB1V101M	NICH	1500-31-0102	2
C53 C55 C59	CAP, ELECT, 1000MF/16V RADIAL LEAD, SP .20	NRE102M16V10X20	NIC	1500-31-0211	3
C60 C63	CAP, ELECT, 470MF/50V RADIAL LEAD, SP .30	CRE SERIES 470/50	CAPAR	1500-34-7103	2
C48 C50	CAP, ELECT, 4700MF/25V RADIAL LEAD, SP .50	NRE 4700/25	NIC	1500-34-7202	2

WAVETEK PARTS LIST | TITLE: ASSY MICRO-PROC/GPIB BOARD | ASSEMBLY NO. 1100-00-2202 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
C56	CAP, ELECT, 6800MF, 16V RADIAL LEAD, SP .50	NRE 6800/16	NIC	1500-36-8201	1
C32 C36 C40	CAP, MYLAR, .1MF, 100V	225P10491WD3	SPRAG	1500-41-0444	3
C28	CAP, MYLAR, 1MF, 100V, RADIAL	PMT2R1.0K100	ITT	1500-41-0524	1
NONE	DRILL DRWG, MICRO-PROC/GPIB BOARD	270-2202	WVTK	1700-00-2202	1
J1 J3	CONN, HEADER	09-60-1101	MOLEX	2100-02-0088	2
J5	CONN, HEADER, 10 PIN	1-640456-0	AMP	2100-02-0133	1
J4	CONN, HOUSING, 20 PIN WITH POLARIZING TABS	2100-02-0137	WVTK	2100-02-0137	1
J6 J7	CONN, HOUSING, 34 PIN WITH POLARIZING TABS	2100-02-0138	WVTK	2100-02-0138	2
NONE	SKT, IC, 16PIN	DILB16P-108T	BURND	2100-03-0028	2
NONE	SKT, IC, 24PIN	DILB-24P-108	BURND	2100-03-0029	2
U6A	SKT, IC, 40PIN	DILB40P-108T	BURND	2100-03-0030	1
NONE	SKT, IC, 28PIN	DILB28P-108T	BURND	2100-03-0055	3
NONE	SOCKET, 8 PIN	DILB08P-108T	BURND	2100-03-0063	2
NONE	TERM	2000B1	USECO	2100-05-0009	12

WAVETEK PARTS LIST | TITLE: ASSY MICRO-PROC/GPIB BOARD | ASSEMBLY NO. 1100-00-2202 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
TP1 TP2 TP3 TP4 TP5	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	5
J8	CONN, HEADER, 34 PIN	929836-01-17	AP	2100-05-0041	1
J2	CONNECTOR, MOD FROM: 2100-02-0126	2100-99-0062	WVTK	2100-99-0062	1
Y1	CRYSTAL, 4MHZ	180-502	MTRON	2300-99-0004	1
	RIVET 1/8X3/16L	1125-0406	AVDEL	2800-12-0011	1
NONE	JUMPER	461-2871-01-03-10	CAMBN	3000-00-0034	1
E1 E2	PINS, JUMPER	450-3704-01-03	CAMBN	3000-00-0035	2
DS1	BEEPER	QM8-06	STMIC	3000-00-0085	1
NONE	BATTERY HOLDER	3000-00-0090	WVTK	3000-00-0090	1
BT1	BATTERY, LITHIUM, 3V	BR-1/2A	PANAS	4000-02-0007	1
R16 R47	POT, TRIM, 200	91AR200	BECK	4600-02-0101	2
R39	POT, TRIM, 500	91AR500	BECK	4600-05-0104	1
R33 R45	RES, C, 1/2W, 5%, 1.8	RC-1/2-1R8J	STKPL	4700-25-0189	2
R10 R9	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	2
R53	RES, MF, 1/8W, 1%, 1K	RN55D-1001F	TRW	4701-03-1001	1
R15 R30 R41 R48 R51 R55 R60	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	8

WAVETEK PARTS LIST | TITLE: ASSY MICRO-PROC/GPIB BOARD | ASSEMBLY NO. 1100-00-2202 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R61 R27 R3 R4 R5 R57 R58 R6	RES, MF, 1/8W, 1%, 1M	RN55D-1004F	TRW	4701-03-1004	7
R50	RES, MF, 1/8W, 1%, 1.1K	RN55D-1101F	TRW	4701-03-1101	1
R37	RES, MF, 1/8W, 1%, 1.21K	RN55D-1211F	TRW	4701-03-1211	1
R26	RES, MF, 1/8W, 1%, 12.4K	RN55D-1242F	TRW	4701-03-1242	1
R40	RES, MF, 1/8W, 1%, 1.78K	RN55D-1781F	TRW	4701-03-1781	1
R11 R12	RES, MF, 1/8W, 1%, 2.21K	RN55D-2211F	TRW	4701-03-2211	2
R28	RES, MF, 1/8W, 1%, 2.37K	RN55D-2371F	TRW	4701-03-2371	1
R2	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	1
R38	RES, MF, 1/8W, 1%, 2.74K	RN55D-2741F	TRW	4701-03-2741	1
R29	RES, MF, 1/8W, 1%, 27.4K	RN55D-2742F	TRW	4701-03-2742	1
R52	RES, MF, 1/8W, 1%, 301	RN55D-3010F	TRW	4701-03-3010	1
R18 R19 R20 R21 R22 R23 R24 R25	RES, MF, 1/8W, 1%, 301K	RN55D-3013F	TRW	4701-03-3013	8
R49	RES, MF, 1/8W, 1%, 3.16K	RN55D-3161F	TRW	4701-03-3161	1
R31	RES, MF, 1/8W, 1%, 3.83K	RN55D-3831F	TRW	4701-03-3831	1
R34 R36 R42 R43	RES, MF, 1/8W, 1%, 3.92K	RN55D-3921F	TRW	4701-03-3921	4

WAVETEK PARTS LIST | TITLE: ASSY MICRO-PROC/GPIB BOARD | ASSEMBLY NO. 1100-00-2202 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R35 R44 R59	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	3
R46	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	1
R54	RES, MF, 1/8W, 1%, 49.9K	RN55D-4992F	TRW	4701-03-4992	1
R56	RES, MF, 1/8W, 1%, 6.19K	RN55D-6191F	TRW	4701-03-6191	1
R17	RES, MF, 1/8W, 1%, 6.81K	RN55D-6811F	TRW	4701-03-6811	1
R1 R8	RES NETWORK 10K 2% 10PIN SIP BUSS	4310R-101-103	BOURN	4770-00-0008	2
R13 R14 R32 R7	RES NETWORK 2.2K 2% 10PIN SIP BUSS	4310R-101-222	BOURN	4770-00-0011	4
CR10	DIODE, ZENER, 6.2V, 1N823	1N823A	MOT	4801-01-0823	1
CR12 CR14 CR16 CR8	DIODE, 1N4002 GEN PURPOSE RECT. 100V, 1A	1N4002	FAIR	4801-02-0001	4
CR15 CR7	DIODE, RECTIFIER, BRIDGE	3N254	MOT	4801-02-0254	2
CR4	DIODE, RECT, SCH BARRIER	MBR 120	MOT	4806-02-0120	1
CR11 CR17 CR3 CR6 CR9	DIODE 1N4148 COMPUTER, Q/P, 75V, 200MA, SWITCHING	1N4148	FAIR	4807-02-6666	5
CR1 CR18 CR19 CR2 CR5	DIODE 5082-2811	5082-2811	HP	4809-02-2811	5

WAVETEK PARTS LIST | TITLE: ASSY MICRO-PROC/GPIB BOARD | ASSEMBLY NO. 1100-00-2202 | REV C

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
CR13	SCHOTTKY, 15V, 20MA BRIDGE ASSY, 4 AMP	RS602	DIODE	4899-00-0037	1
Q1 Q2	TRANS 2N3904 NPN GENERAL PURPOSE TO-92	2N3904	FAIR	4901-03-9040	2
SW1	SWITCH PC	2400080	EECO	5199-00-0004	1
VR1 VR3 VR4	VOLT REGULATOR, 3 TERMINAL ADJUSTABLE POS	LM317T	NSC	7000-03-1700	3
VR2	VOLT REGULATOR	LM337T	NSC	7000-03-3700	1
U16 U19 U20 U26 U27	OP AMP INPUT	TL082CP	TI	7000-08-2000	5
U15	DAC	DAC1006LCN	NAT	7000-10-0600	1
U17	SW, QUAD ANALOG, CMOS	D9211CJ	SLCON	8000-02-1100	1
U7B U8B	BUS XCVR, BIDIR, D, TTL	MC3447P3	MOT	8000-34-4700	2
U11 U12	RAM 2K X 8, CMOS STATIC	CXK5816PN-12L	SONY	8000-61-1600	2
U3	MICROPROCESSOR, 8BIT	MC6803L	MOT	8000-68-0300	1
U1	GATE, NAND, QUAD 2-INP, TTL	SN74LS00N	TI	8000-74-0010	1
U18	INVERTER, HEX, TTL	74LS04	TI	8000-74-0410	1

WAVETEK PARTS LIST | TITLE: ASSY MICRO-PROC/GPIB BOARD | ASSEMBLY NO. 1100-00-2202 | REV C

ZONE	LTR	ECO NO.	CHANGED BY	APPR'D BY	DATE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE

x/x	.xxx	xx	∠
± 1/64	± .005	± .01	± 1°

MATERIAL:

FINISH:

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

	DRAWN	DATE
	CHKD	
	ENG APPR.	
	MFG APPR.	
	ISSUED	

WAVETEK
Wavetek Inc.

TITLE: PARTS LIST
PCA, MICRO-PROC
POWER SUPPLY

SIZE	MODEL NO.	DRAWING NO.	REV
D	275	1100-00-2202	C

SCALE: | CODE IDENT 23338 | SHEET 1 OF 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U2	COUNTER, 12 BIT NIN, CMOS	14040	RCA	8001-40-4000	1
U6	ADPT, GPIB INTERFACE	MC68488P	MOT	8006-84-8800	1
U14	DECODER, DUAL 2-4, TTL	74LS139	SIG	8007-41-3910	1
U5	BUF, OCT 3ST OUT, TTL	M74LS240P	MITSU	8007-42-4010	1
U28 U29	BUF, OCT 3ST OUT, TTL	SN74LS244N	TI	8007-42-4410	2
U25 U4	LATCH, OCTAL TRANSPAR W/3 STATE	74LS373	MOT	8007-43-7310	2
U21 U22 U23 U24	FLIP-FLOP, OCT D, CMOS	MM74C374N	NSC	8007-43-7430	4

WAVETEK PARTS LIST	TITLE: ASSY MICRO-PROC/GPIB BOARD	ASSEMBLY NO. 1100-00-2202	REV C

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE	DO NOT SCALE DWG REMOVE ALL BURRS BREAK SHARP EDGES	WAVETEK Wavetek Inc.
x/x ± 1/64 | .xxx ± .005 | .xx ± .01 | ± 1°	DRAWN / DATE	TITLE: PARTS LIST PCA, MICRO-PROC POWER SUPPLY
MATERIAL:	CHKD	
FINISH:	ENG APPR.	
	MFG APPR.	
	ISSUED	SIZE D | MODEL NO. 275 | DRAWING NO. 1100-00-2202 | REV C
		SCALE: | CODE IDENT 23338 | SHEET 2 OF 2

R.S.Knapp

ZONE	LTR	ECO NO	CHANGED BY	APPR'D. BY	DATE

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	PROM INSTALLATION DRAWING(MICRO-PROC/	0101-00-1025	WVTK	0101-00-1025	1
A6U13	IC, PROGRAMMED REF: 8008-21-0200	8600-00-0237	WVTK	8600-00-0237	1
U9	EPROM, PROGRAMMED SET V2.5 REF: 8000-27-6400	8600-00-0427	WVTK	8600-00-0427	1
U10	EPROM, PROGRAMMED SET V2.5 REF: 8000-27-6400	8600-00-0428	WVTK	8600-00-0428	1

WAVETEK PARTS LIST	TITLE: PROM PACKAGE	ASSEMBLY NO. 1109-00-0024	REV E
		PAGE 1	

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST PROM PACKAGE
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		MODEL NO. 275 / DWG NO. 1109-00-0024 / REV E
	DO NOT SCALE DWG		CODE IDENT 23338 / SHEET 1 OF 1
	SCALE		

REV	ECN	BY	DATE	APP

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-1894

REV	ECN	BY	DATE	APP
A	# 3904	SC	7-29-83	
/	4154 CLASS III	SC	2-7-84	
B	ECN 4169	RO	3-89	

TRIG SEL LOGIC

BURST CLK SEL (A5)

74F00

R1 499 STOP(3A6)

U2D U2A U2B U2C

C4 220pF

C5 .1/50V +5V

ANALOG INTERFACE CONNECTOR

J15

-1 N/C
-2 N/C
-3
-4 N/C
-5
-6
-7 BCA(B1)
-8 TRGO
-9
-10
-11 N/C
-12 SQS
-13
-14

SYNTH TRIG SEL (A5)
INT/EXT (2C4)
SYNTH (3C4)

U1 74LS151

TRGOB (2B7, 2D2)

+5V

AUXILIARY POWER CONNECTOR

J17

-1 N/C FB1 +15V
-2
-3 FB2 -15V
-4
-5
-6 N/C FB3 +5V
-7
-8
-9
-10

C1 100/25V
C2 100/25V
C3 100/25V

TP1 TP2 TP4 TP5 TP6

DATA REGISTERS

R13 (2B7)

U3 74C374

R12 (2B7)

C9 .1/50V +5V

U4 74C374

R11 (2B7)

U5 74C374

(2D3)
B DATA Ø
B DATA 1
B DATA 2
B DATA 3
B DATA 4
B DATA 5
B DATA 6
B DATA 7

SYNTH TRIG SEL (C7)
S SLEW (3A3)
BURST CLK SEL (D6)
F SLEW (3B5)

1/4 74F00 U6A U6C

R3 TRIM

R2 TRIM

C6 .1/50V

C7 .1/50V

C8 .1/50V

U7 74LS161

U8 74LS161

U9 74LS161

U10 74LS161

U11 74LS161

B1 B2 B3 B4 B5 B6 B7 B8 B9 B10 B11 B12 B13 B14 B15 B16 B17 B18 B19

C10 .1/50V

BURST COUNTER

C11 .1/50V

U12B 1/2 74F74

U12A 1/2 74F74

BURST (2C4)

R4 392

C12 100pF

1/4 74F00 U6D

U6B

BCA (C8, 2B4, 2A6)

C13 .1/50V

U13 74S133

NOTE: UNLESS OTHERWISE SPECIFIED

6. PROM'S PROGRAMMED PER MODEL, SEE PARTS LIST.
5. LAST REFERENCE DESIGNATORS USED ARE: R49, C62, CR2, U47, Q1, Y1
4. ALL CAPACITORS ARE SHOWN IN MICRO-FARADS.
3. ALL RESISTORS ARE SHOWN IN OHMS.
2. ALL DIODES ARE FD6666.
1. REFERENCE DESIGNATORS SHOWN ARE PARTIAL PREFIX WITH ASSEMBLY REF DES (A10).

REMOVE ALL BURRS AND BREAK SHARP EDGES
MATERIAL
FINISH WAVETEK PROCESS
DRAWN CHERMACK DATE 1-19-83
PROJENGR RBZ 1/25/83
RELEASE APPROV RBZ
TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030
DO NOT SCALE DWG
SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE
SCHEMATIC, ARBITRARY WAVEFORM GENERATOR BOARD (A10)

MODEL NO. 275
DWG NO. 0103-00-1079
REV B
CODE IDENT 23338
SHEET 1 OF 3

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894

DATA REGISTERS

J16 DIGITAL INTERFACE CONNECTOR

R5 10K SIP

U14 74C374 — S8 (B2), S9 (B2), S10 (B2), S11 (B2), S12 (B2), VCO OFF (3C3), SYNTH SYNC EN (3C6), SYNTH EN (3C5), RØ (C7)

U15 74C374 — SØ (C2), S1 (C2), S2 (C2), S3 (C2), S4 (C2), S5 (C2), S6 (C2), S7 (C2), R1 (C7)

U16 74C374 — MØ (A4), M1 (A4), M2 (A4), INT/EXT (1C7), BRANCH EN (A6), BURST (1C2), BURST (1C2), EXT CLK EN (D2), R2 (C7)

U17 74C374 — LATCH EN (3C7, 3D6), DSØ (C3), DS1 (C3), DS2 (C3), N/C, Ø ACC CLK EN (D2), RAM EN (3A7, 3B7), STATE CLK (A4), R10 (B7)

B DATA Ø, B DATA 1, B DATA 2, B DATA 3, B DATA 4, B DATA 5, B DATA 6, B DATA 7 (1A6, 1D8)

Ø ACCUMULATOR

Ø ACC CLK EN (C3), EXT CLK EN (C4), SYNTH (3C4), TRGOB (1C6), R3 (C7), R11 10K, CLK (C5)

U26 74LS151

U27 74HC161 — RAØ (3B7, 3A7), RA1 (3B7, 3A7), RA2 (3B7, 3A7), RA3 (3B7, 3A7)

U28 74HC161 — RA4 (3B7, 3A7), RA5 (3B7, 3A7), RA6 (3B7, 3A7), RA7 (3B7, 3A7)

U29 74HC161 — RA8 (3B7, 3A7), RA9 (3B7, 3A7), RA10 (3B7, 3A7), RA11 (3B7, 3A7)

U30 74HC161 — RA12 (3B7, 3A7), N/C, N/C, N/C, N/C

C21, C22, C23, C60 .1/50V

U18 74HC138 — BADRØ, BADR1, BADR2, ANA2, ANA3; RØ (C7), R1 (C6), R2 (C5), R3 (D2), R4 (3C8), R5 (3C6), R6 (3C5), R7 (3B6)

U19 74HC138 — R6 10K SIP; R8 (3B6), N/C, R10 (C4), R11 (1D5), R12 (1B5), R13 (1A5), N/C, R15 (3B7, 3A7, 3B8)

μP INFO

C59 .1/50V RAM POWER (3B7)

RTS/HOLD INPUT

RTS/HOLD INPUT, E1, E2, R7 1.21K, C17 150pF, CR1 FD6666, CR2 FD6666, R8 49.9K, -15V

U20A, U20B, U20C, U20D LS132; C47 100pF, C58 100pF, R44 2K, R45 2K

TRGOB (1C6), STOP (3A6), RTS

STATE MACHINE

CLK (D2)

U21A, U21B 1/2 74LS74 — TRIG INHIBIT (A3)

LATCHED TRIGGER

U22 74LS151 — STOP (3A6), TBPC (3A6), Mø (C5), M1 (C5), M2 (C5), R9 10K, C19 .1/50V

U23 74HC161 — HOLD (C4), TRIG INHIBIT (B6), STATE CLR (C3)

U25 74LS151 — DS2 (C3), DS1 (C3), DSØ (C3), HOLD (A3), DATA SERIAL OUT (3A6), N/C, BCA (1B1), JUMP (3A8), μP INFO (B6), C20 .1/50

SYNTH SYNC EN (C7), C24 100pF, R12 2K, R13 2K, SYNTH EN (C7), U33D, U33B, DIVIDER EN (3C5)

U33A, U33C LS132 — BCA (1B1), BRANCH EN (C4), R14 10K

R10 10K SIP; C62 .1/50V; Mø (C5), M1 (C5), M2 (C5), HOLD (C4), TRIG INHIBIT (B6)

U24 1/N8600-00-0248

NOTE: UNLESS OTHERWISE SPECIFIED

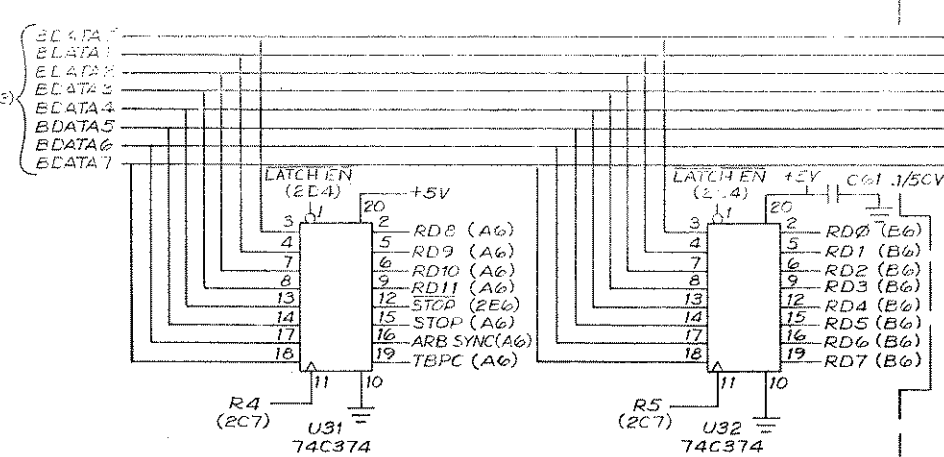
BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3994

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 1-7-82	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: SCHEMATIC, ARBITRARY WAVEFORM GENERATOR BOARD (A10)
FINISH WAVETEK PROCESS	RELEASE APPROV		TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030
	DO NOT SCALE DWG		MODEL NO 275
	SCALE		DWG NO 0103-00-1079 REV B
	CODE IDENT 23338		SHEET 2 OF 3

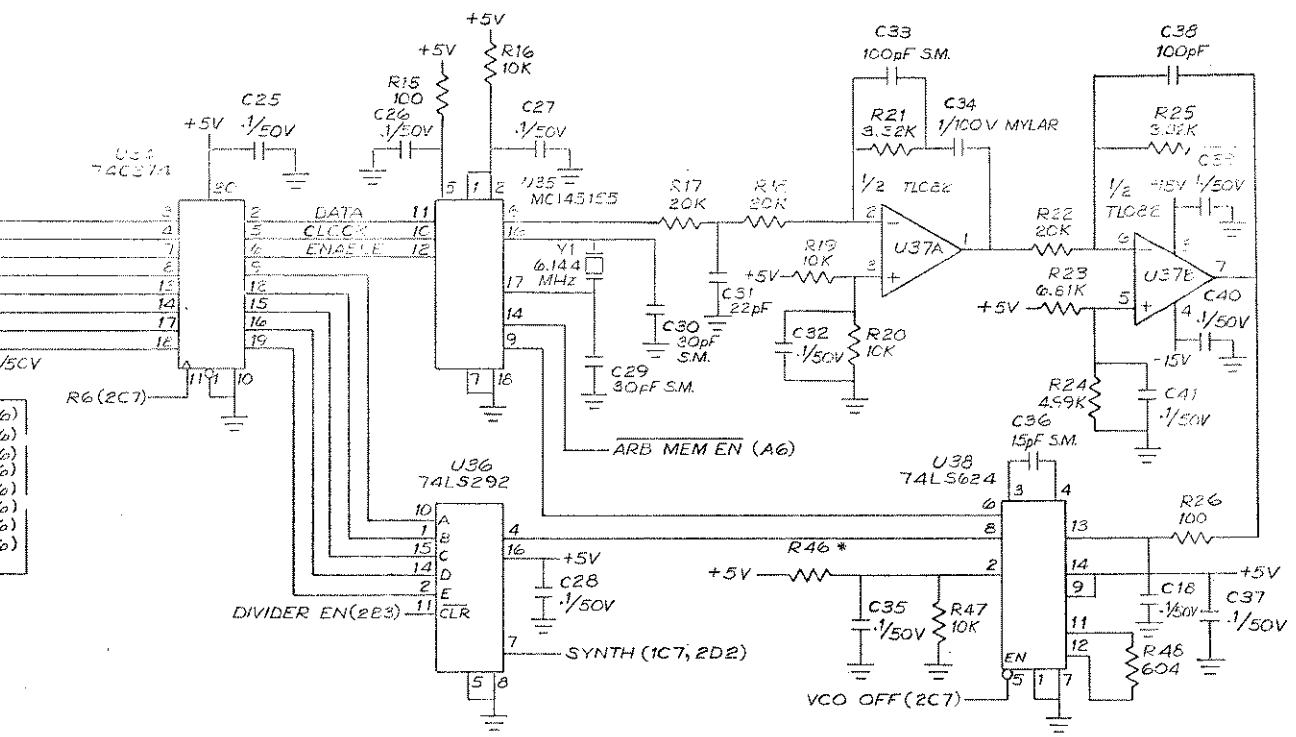
REV	ECN	BY	DATE	APP

REV	ECN	BY	DATE	APP

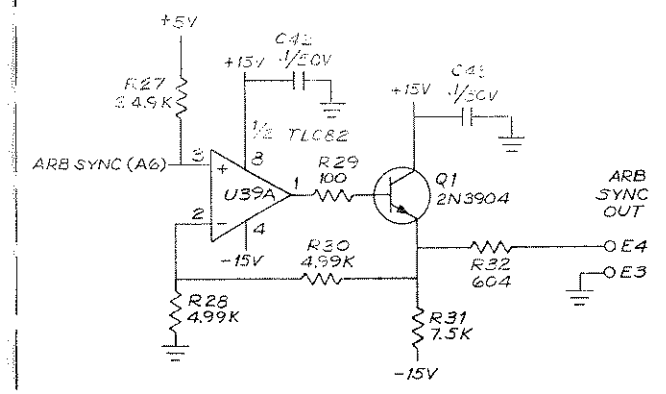
DATA REGISTERS



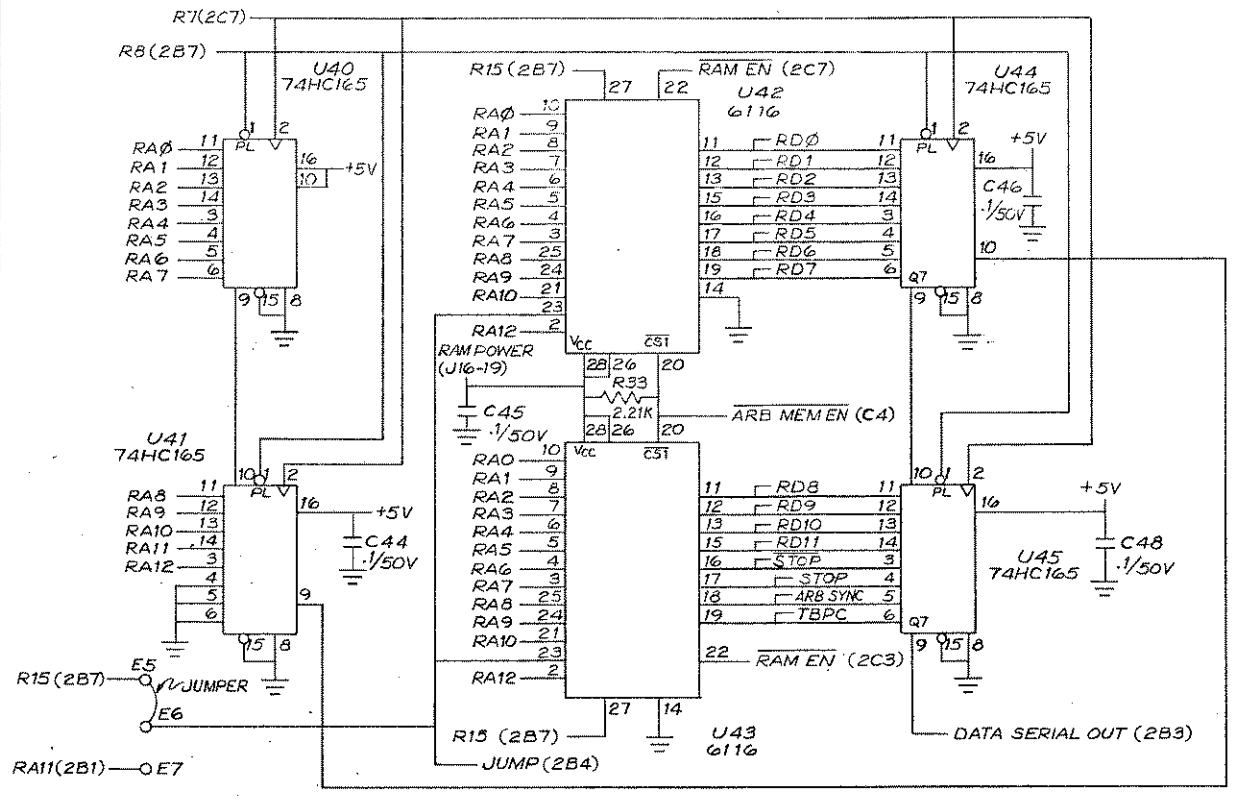
SYNTHESIZER



ARB SYNC OUT

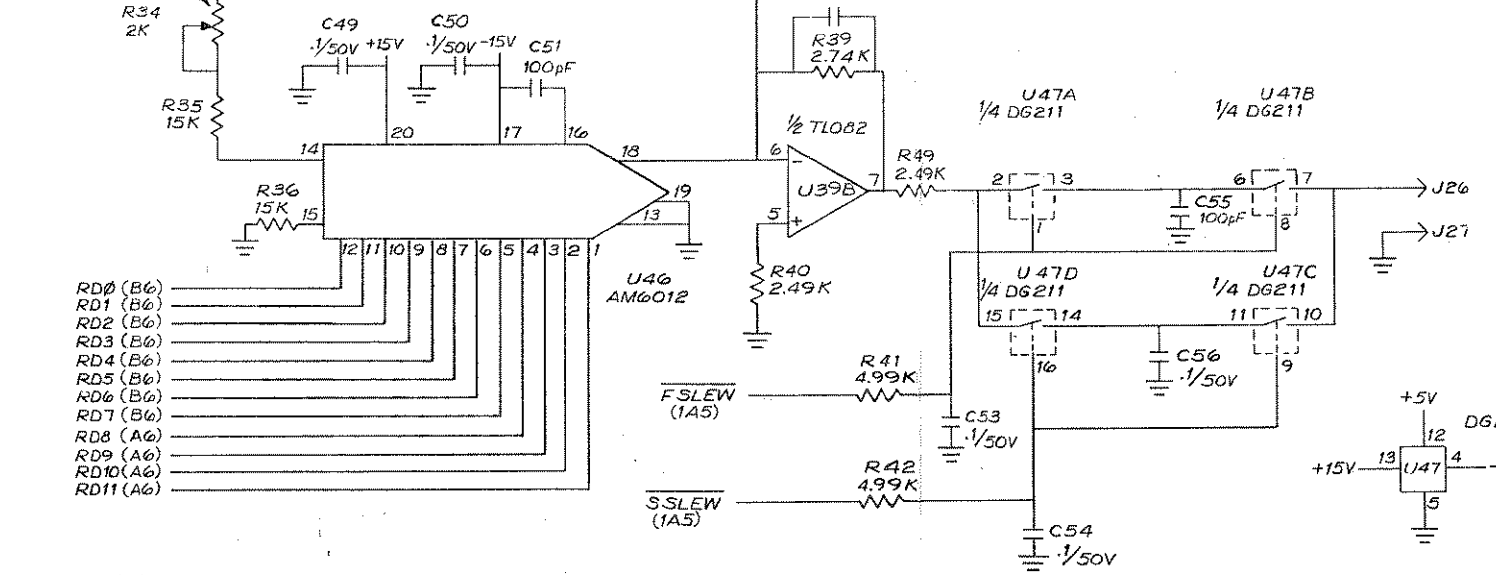


ARB RAM



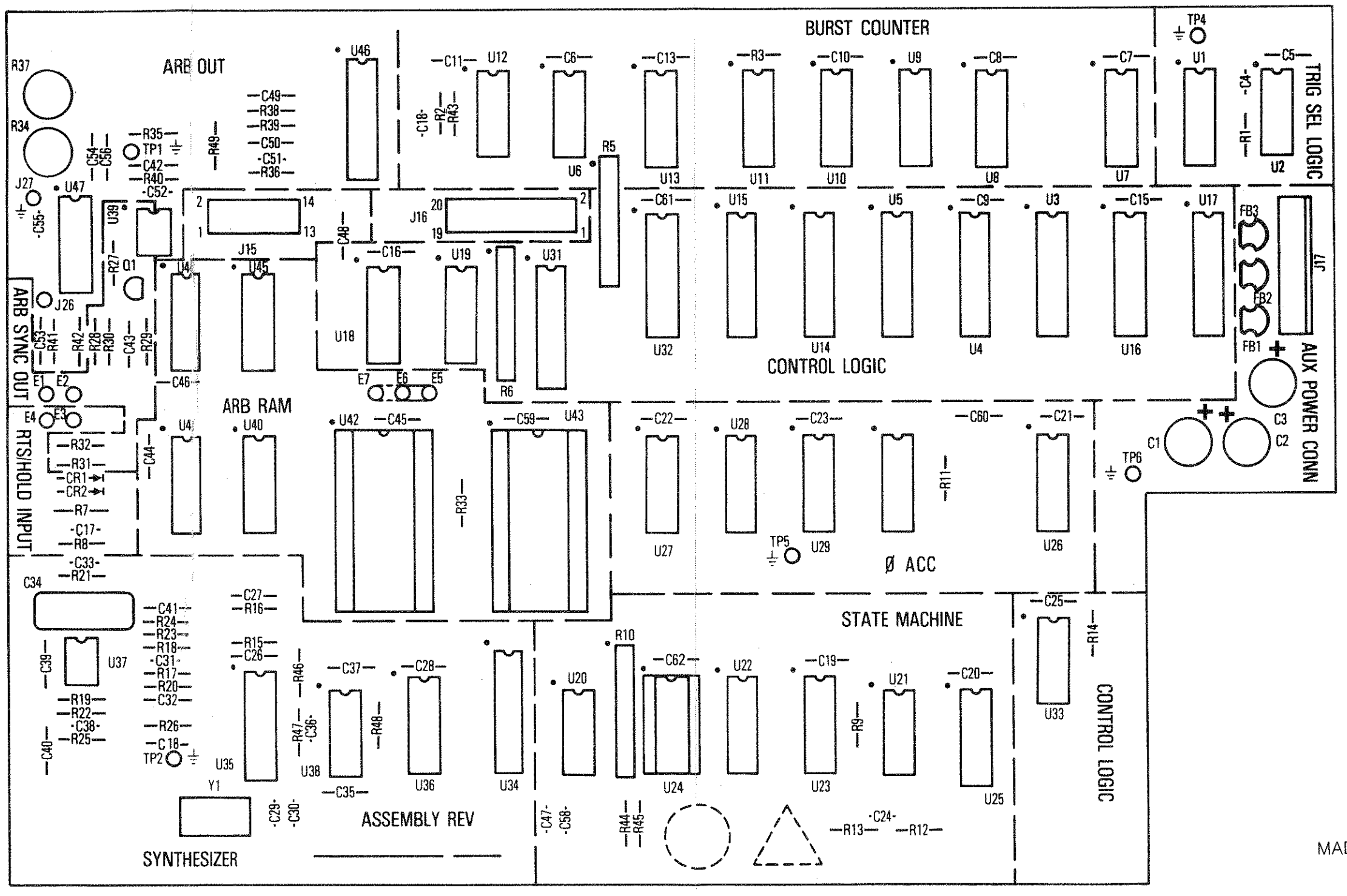
NOTE: UNLESS OTHERWISE SPECIFIED

ARB OUT



REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 1-683	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL	PROJ ENGR RBJ	7/15/83	TITLE: SCHEMATIC, ARBITRARY WAVEFORM GENERATOR BOARD(A10)	
FINISH WAVETEK PROCESS	RELEASE APPROV RBJ			
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± 010 ANGLES ± 1° XX ± 030			
	DO NOT SCALE DWG SCALE		MODEL NO. 275	DWG NO. 0103-00-1079 REV B
			CODE IDENT 23338	SHEET 3 OF 3

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894



MADE FROM 0100-00-1079-3E

WAVETEK SAN DIEGO, CALIFORNIA

TITLE
ARB GEN BOARD ASSEMBLY

MODEL NO	ASSY. NO.	REV
275	1100-00-1079	

CODE IDENT 23338 SHEET 1 OF 1

ZONE	LTR	ECO NO	CHANGED BY	APPR'D. BY	DATE

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, ARB GEN BOARD	0101-00-1079	WVTK	0101-00-1079	1
NONE	SCHEMATIC, ARB GEN BOARD	0103-00-1079	WVTK	0103-00-1079	1
NONE	ASSY, AUX BOARD SHIELD	275-1102	WVTK	1206-00-1102	1
C12 C24 C38 C47 C51 C55 C58	CAP, CER, 100PF, 1KV	DD-101	CRL	1500-01-0111	7
C10 C11 C13 C15 C16 C18 C19 C20 C21 C22 C23 C25 C26 C27 C28 C32 C35 C37 C39 C40 C41 C42 C43 C44 C45 C46 C48 C49 C5 C50 C53 C54 C56 C59 C6 C60 C61 C62 C7 C8 C9	CAP, CER, MON, .1MF, 50V, AXIAL	CAC03Z5U104Z050A	CORNG	1500-01-0405	41
C17	CAP, CER, 150PF, 1KV	DD-151	CRL	1500-01-5111	1
C31	CAP, CER, 22PF, 1KV	DD-220	CRL	1500-02-2011	1
C4	CAP, CER, 220PF, 1KV	DD-221	CRL	1500-02-2111	1
C52	CAP, CER, 33PF, 1KV	DD-330	CRL	1500-03-3011	1
C33	CAP, MICA, 100PF, 500V	DM15-101J	ARCO	1500-11-0100	1
C36	CAP, MICA, 15PF, 500V	DM15-150J	ARCO	1500-11-5000	1
C29 C30	CAP, MICA, 30PF, 500V, RADIAL	DM15-300J	ARCO	1500-13-0000	2
C1 C2 C3	CAP, ELECT, 100MF, 35V	ULS1V101M	NICH	1500-31-0102	3

WAVETEK PARTS LIST | TITLE: PCA, ARB GEN BOARD | ASSEMBLY NO. 1100-00-1079 | REV B | PAGE 1

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
	RADIAL LEAD, SP .20				
C34	CAP, MYLAR, 1MF, 100V, RADIAL	PMT2R1.0K100	ITT	1500-41-0524	1
NONE	ARB GEN BOARD	275-1079	WVTK	1700-00-1079	1
J17	CONN, HEADER, 10 PIN	1-640456-0	AMP	2100-02-0133	1
J15	CONN, HOUSING, 14 PIN WITH POLARIZING TABS	2100-02-0136	WVTK	2100-02-0136	1
J16	CONN, HOUSING, 20 PIN WITH POLARIZING TABS	2100-02-0137	WVTK	2100-02-0137	1
NONE	SKT, IC, 16PIN	DILB16P-108T	BURND	2100-03-0028	1
NONE	SKT, IC, 28PIN	DILB28P-108T	BURND	2100-03-0055	2
NONE	PIN, MALE	60809-2	AMP	2100-05-0020	4
NONE	BUSS BAR STANDOFF	2110-001	ARTWR	2100-05-0024	5
Y1	CRYSTAL, 6.144 MHZ	MP-1	MTRON	2300-00-0014	1
NONE	TIE MOUNT	TM-256C	PANDT	2800-00-0005	1
NONE	TY-WRAP	TY-523M	TB	2800-00-0006	2
NONE	MNTG CLIP, CABLE TIE	SNF-2	WKESR	2800-00-0031	1
NONE	JUMPER	461-2871-01-03-10	CAMBN	3000-00-0034	1

WAVETEK PARTS LIST | TITLE: PCA, ARB GEN BOARD | ASSEMBLY NO. 1100-00-1079 | REV B | PAGE 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
E5 E6 E7	PINS, JUMPER	450-3704-01-03	CAMBN	3000-00-0035	3
FB1 FB2 FB3	BALUN CORE	2873000902	FARIT	3100-00-0002	3
R37	POT, TRIM, 1K	91AR1K	BECK	4600-01-0209	1
R34	POT, TRIM, 2K	91AR2K	BECK	4600-02-0201	1
R15 R26 R29	RES, MF, 1/8W, 1%, 100	RN55D-1000F	TRW	4701-03-1000	3
R11 R14 R16 R19 R20 R47 R9	RES, MF, 1/8W, 1%, 10K	RN55D-1002F	TRW	4701-03-1002	7
R35 R36	RES, MF, 1/8W, 1%, 15K	RN55D-1502F	TRW	4701-03-1502	2
R12 R13 R44 R45	RES, MF, 1/8W, 1%, 2K	RN55D-2001F	TRW	4701-03-2001	4
R17 R18 R22	RES, MF, 1/8W, 1%, 20K	RN55D-2002F	TRW	4701-03-2002	3
R33	RES, MF, 1/8W, 1%, 2.21K	RN55D-2211F	TRW	4701-03-2211	1
R40 R49	RES, MF, 1/8W, 1%, 2.49K	RN55D-2491F	TRW	4701-03-2491	2
R27	RES, MF, 1/8W, 1%, 24.9K	RN55D-2492F	TRW	4701-03-2492	1
R39	RES, MF, 1/8W, 1%, 2.74K	RN55D-2741F	TRW	4701-03-2741	1
R21 R25	RES, MF, 1/8W, 1%, 3.32K	RN55D-3321F	TRW	4701-03-3321	2
R4	RES, MF, 1/8W, 1%, 392	RN55D-3920F	TRW	4701-03-3920	1
R1	RES, MF, 1/8, 1%, 499	RN55D-4990F	TRW	4701-03-4990	1
R24 R28 R30 R41 R42 R46	RES, MF, 1/8W, 1%, 4.99K	RN55D-4991F	TRW	4701-03-4991	6

WAVETEK PARTS LIST | TITLE: PCA, ARB GEN BOARD | ASSEMBLY NO. 1100-00-1079 | REV B | PAGE 3

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
R8	RES, MF, 1/8W, 1%, 49.9K	RN55D-4992F	TRW	4701-03-4992	1
R32 R48	RES, MF, 1/8W, 1%, 604	RN55D-6040F	TRW	4701-03-6040	2
R23	RES, MF, 1/8W, 1%, 6.81K	RN55D-6811F	TRW	4701-03-6811	1
R31 R38	RES, MF, 1/8W, 1%, 7.5K	RN55D-7501F	TRW	4701-03-7501	2
R7	RES, MF, 1/4W, 1%, 1.21K	RN60D-1211F	TRW	4701-13-1211	1
R10 R5 R6	RES NETWORK 10K 2% 10PIN SIP BUSS	4310R-101-103	BOURN	4770-00-0008	3
CR1 CR2	DIODE 1N4148 COMPUTER, G/P, 75V, 200MA, SWITCHING	1N4148	FAIR	4807-02-6666	2
Q1	TRANS 2N3904 NPN GENERAL PURPOSE TO-92	2N3904	FAIR	4901-03-9040	1
W15	RIBBON CABLE (3 INCH)	6002-00-0018	WVTK	6002-00-0018	1
W13	RIBBON CABLE (7 INCH)	6002-00-0019	WVTK	6002-00-0019	1
U37 U39	OP AMP INPUT	TL082CP	TI	7000-08-2000	2
U46	DAC 12 BIT	AM6012PC	AMD	7000-60-1200	1
U47	SW, QUAD ANALOG, CMOS	DG211CJ	SLCON	8000-02-1100	1
U42 U43	RAM 2K X 8, CMOS STATIC	CXK5816PN-12L	SONY	8000-61-1600	2

WAVETEK PARTS LIST | TITLE: PCA, ARB GEN BOARD | ASSEMBLY NO. 1100-00-1079 | REV B | PAGE 4

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U2 U6	GATE, NAND, QUAD 2INP, TTL	74F00PC	FAIR	8000-74-0002	2
U12	FLIP-FLOP DUAL, D-POS EDGE TRIG, TTL	74F74PC	FAIR	8000-74-7402	1
U21	FLIP-FLOP DUAL, D-POS EDGE TRIG, TTL	74LS74	TI	8000-74-7410	1
U20 U33	GATE, NAND, QUAD S/TRIG, TTL	74LS132	TI	8007-41-3210	2
U13	GATE NAND 13-INPUT POSITIVE	74S133	TI	8007-41-3301	1
U18 U19	DECODER, 3-8 LINE, CMOS	MC74HC138N	MOT	8007-41-3840	2
U1 U22 U25 U26	MUX, DATA, 1 OF 8, TTL	74LS151	TI	8007-41-5110	4
U10 U11 U7 U8 U9	COUNTER, SYNC 4B, TTL	74LS161	SIG	8007-41-6110	5
U23 U27 U28 U29 U30	COUNTER, PROG 4B BIN, CMOS	MC74HC161N	MOT	8007-41-6140	5
U40 U41 U44 U45	SHIFT REG, 8B PIS, CMOS	74HC165	MOT	8007-41-6540	4
U36	PROG DIV/TIMER, TTL	74LS292	TI	8007-42-9210	1
U14 U15 U16 U17 U3 U31 U32 U34 U4 U5	FLIP-FLOP, OCT D, CMOS	MM74C374N	NSC	8007-43-7430	10

WAVETEK PARTS LIST | TITLE: PCA, ARB GEN BOARD | ASSEMBLY NO. 1100-00-1079 | REV B | PAGE 5

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
U38	VCO, TTL	74LS624	TI	8007-46-2410	1
U35	SYNTH, PLL FREQ, CMOS	MC145155	MOT	8100-00-0007	1
U24	IC, PROGRAMMED REF: 8007-41-8801	8600-00-0248	WVTK	8600-00-0248	1

WAVETEK PARTS LIST | TITLE: PCA, ARB GEN BOARD | ASSEMBLY NO. 1100-00-1079 | REV B | PAGE 6

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES AND TOLERANCES ARE
x/x ± 1/64 | .xxx ± .005 | .XX ± .01 | ∠ ± 1°
MATERIAL:
FINISH:

DO NOT SCALE DWG
REMOVE ALL BURRS
BREAK SHARP EDGES

	DATE
DRAWN	
CHKD	
ENG APPR.	
MFG APPR.	
ISSUED	

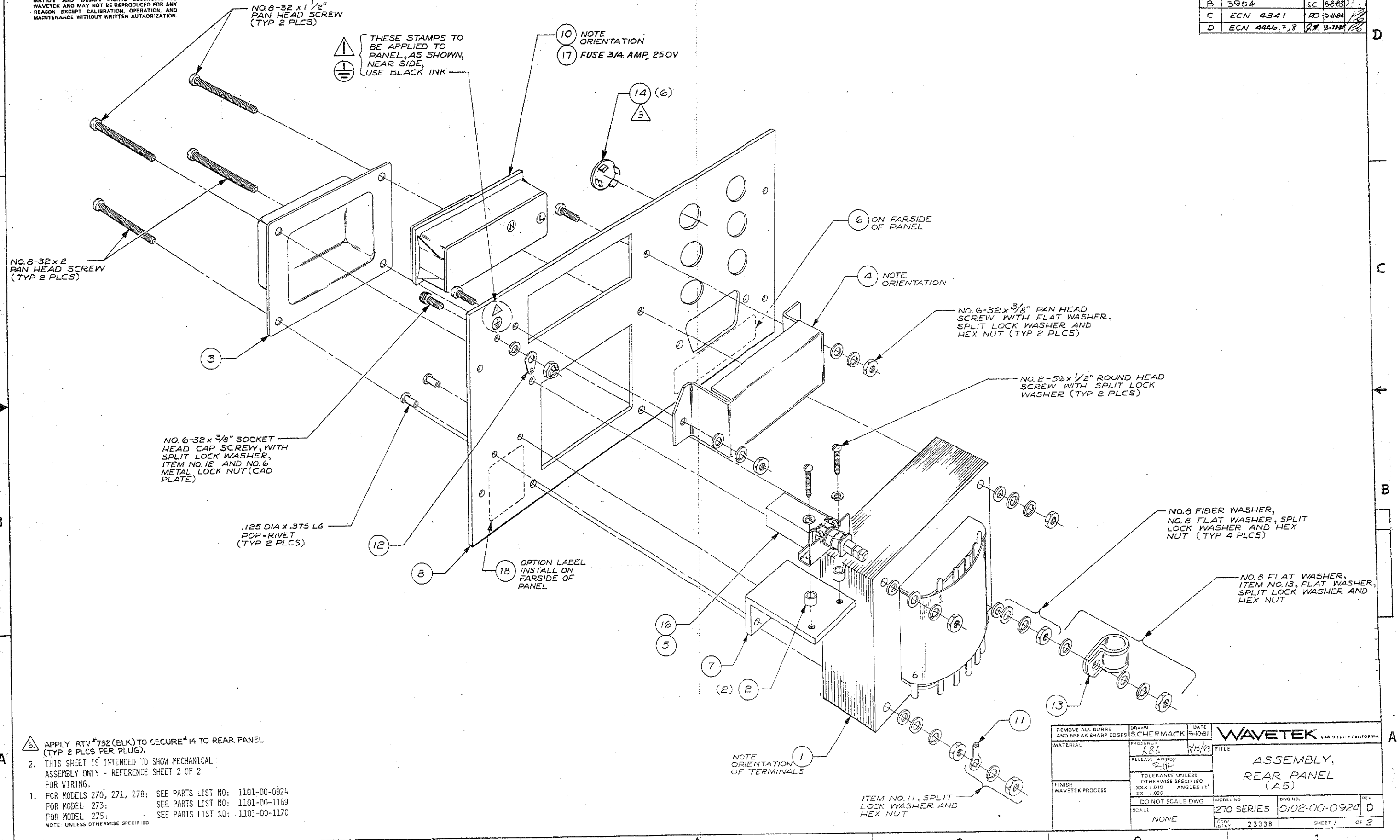
WAVETEK
Wavetek inc.

TITLE: PARTS LIST
PCA, ARB GEN BOARD

SIZE D | MODEL NO. 275 | DRAWING NO. 1100-00-1079 | REV B
SCALE: | CODE IDENT 23338 | SHEET 1 OF 1

R.B.Knapp

REV	ECN	BY	DATE	APP
/	3756 (CL II)	fra	5/11/83	
/	3770 (CL II)	fra	5/19/83	
A	3874	SGC	7-7-83	
B	3904	SC	8-8-83	
C	ECN 4341	RO	9-11-84	
D	ECN 4446, 7, 8	[illegible]	3-28-85	



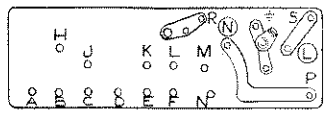
3. APPLY RTV*732 (BLK) TO SECURE*14 TO REAR PANEL (TYP 2 PLCS PER PLUG).
2. THIS SHEET IS INTENDED TO SHOW MECHANICAL ASSEMBLY ONLY - REFERENCE SHEET 2 OF 2 FOR WIRING.
1. FOR MODELS 270, 271, 278: SEE PARTS LIST NO: 1101-00-0924
   FOR MODEL 273: SEE PARTS LIST NO: 1101-00-1169
   FOR MODEL 275: SEE PARTS LIST NO: 1101-00-1170

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN S.CHERMACK	DATE 9-10-81	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR RBG	9/15/83	TITLE ASSEMBLY, REAR PANEL (A5)
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG	MODEL NO 270 SERIES	DWG NO. 0102-00-0924 REV D
	SCALE NONE	CODE IDENT 23338	SHEET 1 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A3104

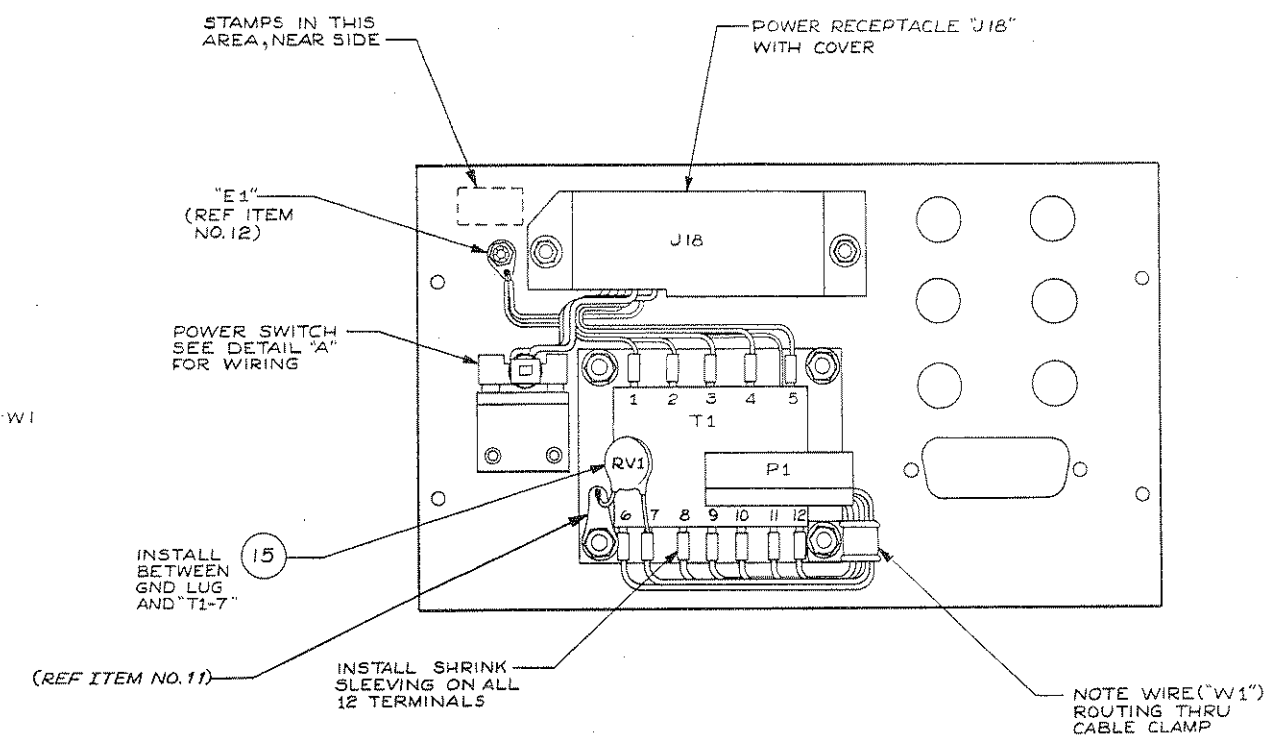
REV	ECN	BY	DATE	APP

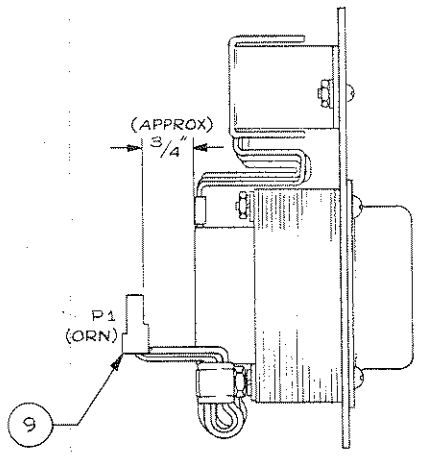


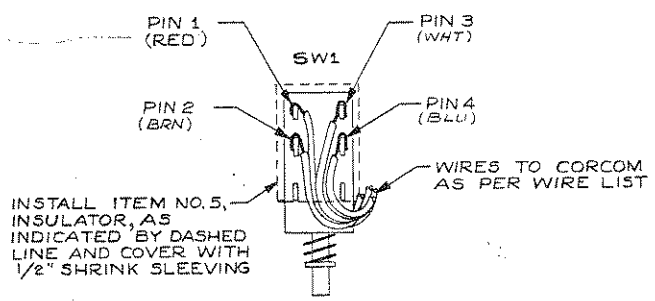
POWER RECEPTACLE PIN MARKING

WIRE LIST				
			DESTINATION	
AWG	COLOR	LENGTH	FROM	TO
18	BLU	4	P1-1	T1-11
18	BLU	4	P1-2	T1-12
18	GRN	5 1/2	P1-3	T1-6
18	GRN	5 1/4	P1-4	T1-8
18	WHT	5 1/2	P1-5	T1-7
			P1-6	
			P1-7	
			P1-8	
18	RED	5 1/2	P1-9	T1-9
18	RED	5 1/4	P1-10	T1-10
22	BLK		J18-C	T1-1
22	ORN		J18-A	T1-2
22	WHT/BLK		J18-E	T1-3
22	GRY		J18-D	T1-4
22	WHT/GRY		J18-F	T1-5
22	GRN/YEL		A5-E1	T1(SHIELD)
22	BUS		J18-B	J18-H
22	BRN		J18-R	SW1-2
22	RED		J18-S	SW1-1
22	BLU		J18-L	SW1-4
22	WHT		J18-P	SW1-3
22	GRN/YEL		J18-⏚	A5-E1

W1

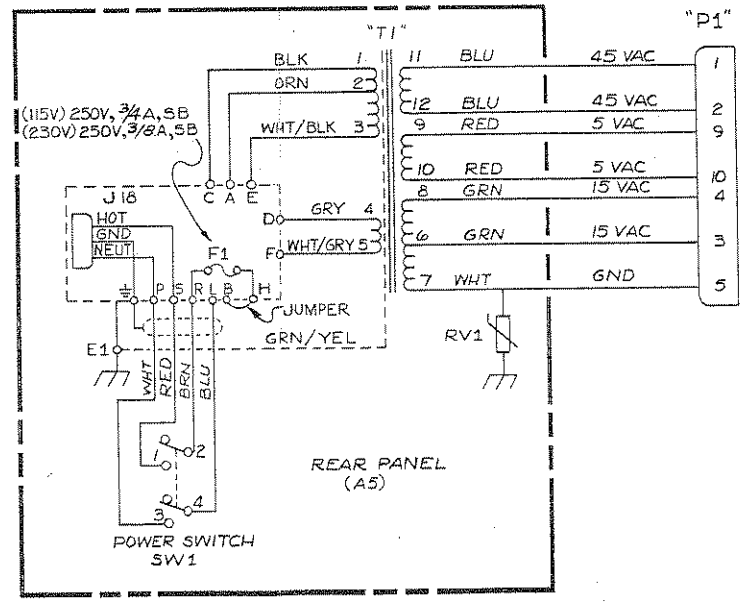






DETAIL "A"

POWER SWITCH WIRING AND INSULATOR ASSY



NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 11-5-81	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR A136	7/16/82	TITLE ASSEMBLY, REAR PANEL (A5)
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		MODEL NO. 270 SERIES
	DO NOT SCALE DWG		DWG NO. 0102-00-0924 REV D
	SCALE		CODE IDENT 23338 SHEET 2 OF 2

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, REAR PANEL	0102-00-0924	WVTK	0102-00-0924	1
1	TRANSFORMER	270-0049	WVTK	1204-00-0049	1
2	SPACER	8480	WVTK	1400-00-0653	2
3	END BELL	157-500-EB	WVTK	1400-00-3224	1
4	SHIELD, PWR	801-6210	WVTK	1400-00-6210	1
5	INSULATOR, PWR SWITCH REF: 1600-99-0001	801-8370	WVTK	1400-00-8370	1
6	I.D. LABEL	801-9090	WVTK	1400-00-9090	1
7	BRACKET, SWITCH MNTG	189-3263	WVTK	1400-01-3263	1
18	LABEL, OPTION	270-4960	WVTK	1400-01-4960	1
8	REAR PANEL FROM: 1400-01-3882	275-6879	WVTK	1400-01-6879	1
9	CONNECTOR, HOUSING 18 AWG	1-640431-0	AMP	2100-02-0115	1
10	RECEPTACLE	6VJ1	CORCM	2100-03-0026	1
11	TERM, LOCK LUG	1414-8	SMITH	2100-04-0010	1
12	SOLDER LUG	11A144	ZIER	2100-04-0025	1
17	FUSE, 3/4A, 250V, 5-8	313-750	LITFU	2400-05-0011	1

WAVETEK PARTS LIST | TITLE: ASSY, REAR PANEL | ASSEMBLY NO. 1101-00-1170 | REV B

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
13	CLAMP, CABLE	9927	SMITH	2800-00-0022	1
14	PLUG BUTTON MATTE FINISH	62PP050BM14 BLK	MICRO	2800-35-0005	6
15	VARISTOR	4899-00-0045	WVTK	4799-00-0048	1
16	SWITCH ASSY PB	5103-00-0020	WVTK	5102-00-0005	1

WAVETEK PARTS LIST | TITLE: ASSY, REAR PANEL | ASSEMBLY NO. 1101-00-1170 | REV B

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN	DATE	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR		TITLE: PARTS LIST ASSY, REAR PANEL
	RELEASE APPROV		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° XX ±.030		MODEL NO. 275 / DWG NO. 1101-00-1170 / REV B
	DO NOT SCALE DWG		CODE IDENT 23338 / SHEET 1 OF 1
	SCALE		

NOTE: UNLESS OTHERWISE SPECIFIED

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, RACK ADAPTER KIT, SINGLE	0102-00-1043	WVTK	0102-00-1043	1
NONE	EAR, RACK ADAPT	270-5512	WVTK	1400-01-5512	1
NONE	EAR, RACK ADAPT	270-5522	WVTK	1400-01-5522	2
NONE	ANGLE BRACKET, RACK ADAPT, SINGLE	270-5533	WVTK	1400-01-5533	2
NONE	EAR, RACK ADAPT	270-5542	WVTK	1400-01-5542	1
NONE	SCREW, PAN, CAD I, CROSS RECESS, 10-32 X 5/8	10-32 X 5/8 PAN	CMRCL	2800-38-0110	4
NONE	SCREW, PAN, CAD I, CROSS RECESS, 8-32 X 3/8	8-32 X 3/8 PAN	CMRCL	2800-38-8106	4
NONE	LOCKWASHER, SPLIT, PLATED, #10	#10 REG	CMRCL	2800-42-0000	4
NONE	LOCKWASHER, #8 SPLIT RING BIN 540	#8SRLW	CMRCL	2800-42-8000	4

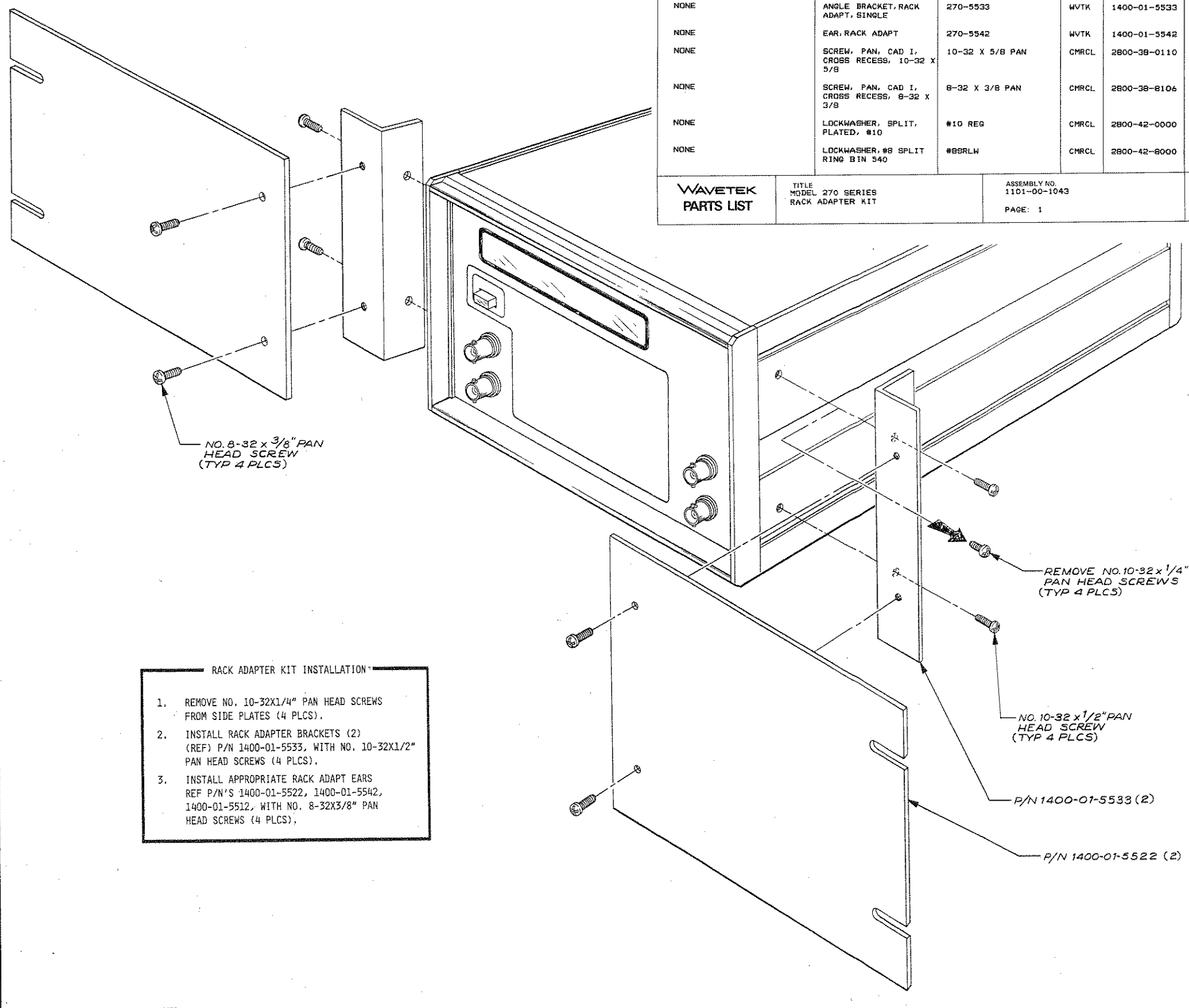
WAVETEK PARTS LIST

TITLE
MODEL 270 SERIES
RACK ADAPTER KIT

ASSEMBLY NO.
1101-00-1043

PAGE: 1

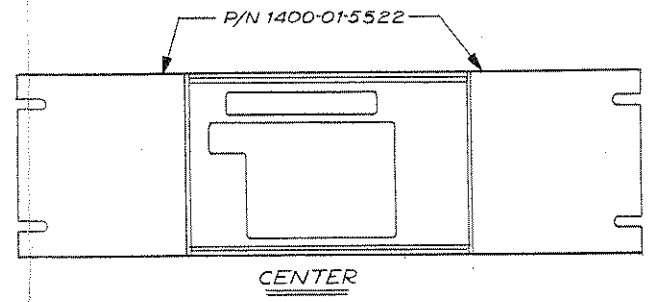
REV A

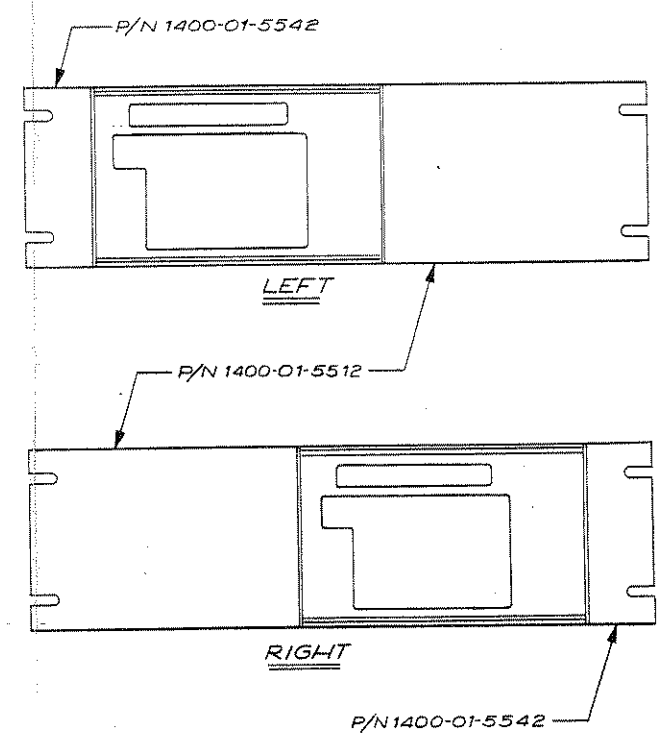


RACK ADAPTER KIT INSTALLATION

1. REMOVE NO. 10-32X1/4" PAN HEAD SCREWS FROM SIDE PLATES (4 PLCS).
2. INSTALL RACK ADAPTER BRACKETS (2) (REF) P/N 1400-01-5533, WITH NO. 10-32X1/2" PAN HEAD SCREWS (4 PLCS).
3. INSTALL APPROPRIATE RACK ADAPT EARS REF P/N'S 1400-01-5522, 1400-01-5542, 1400-01-5512, WITH NO. 8-32X3/8" PAN HEAD SCREWS (4 PLCS).

NOTE: UNLESS OTHERWISE SPECIFIED

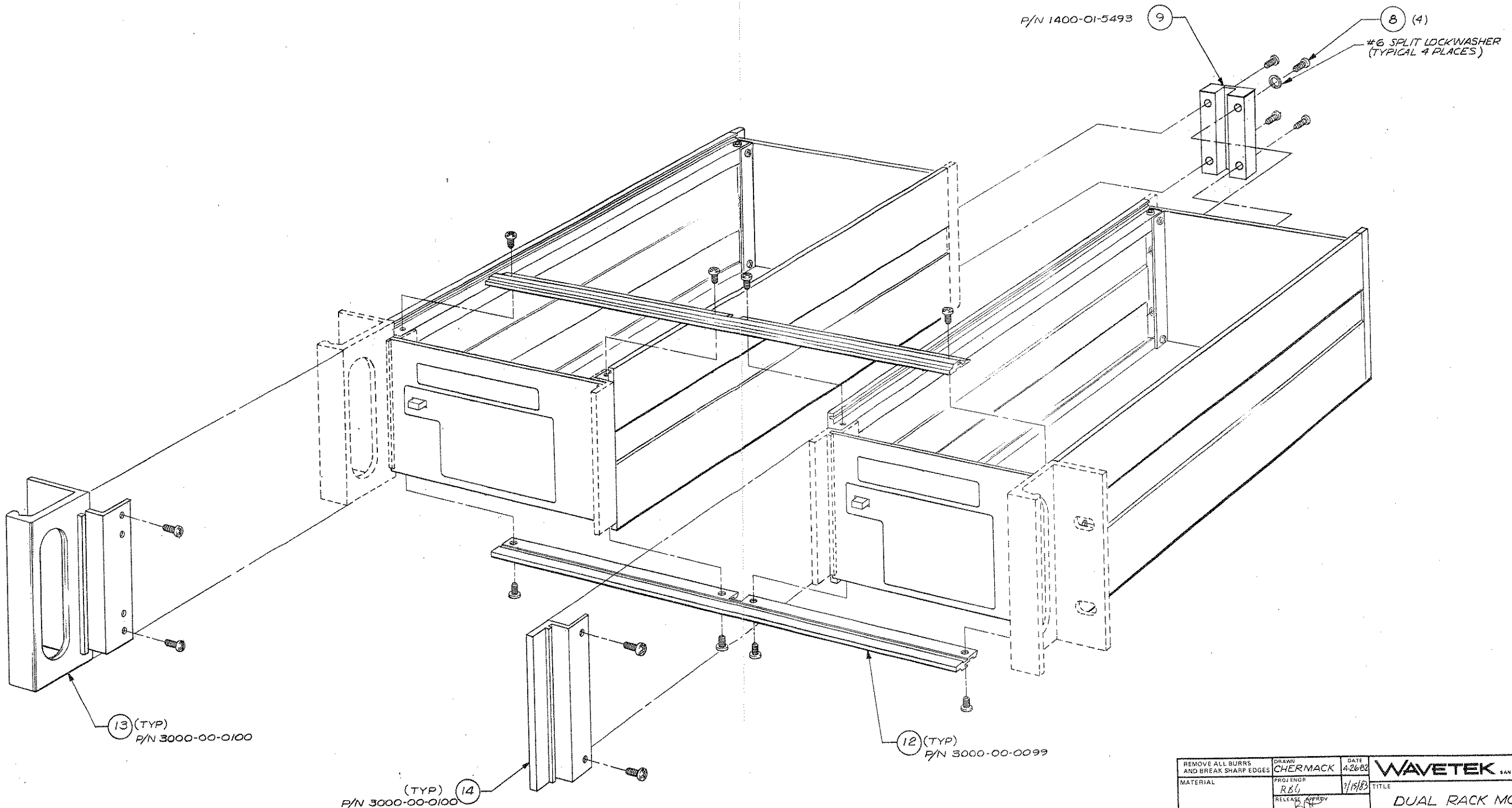




REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 91382	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR RBG	7/15/82	TITLE ASSEMBLY, RACK ADAPTER KIT
	RELEASE APPROV BAP		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG	MODEL NO 270 SERIES	DWG NO. 0102-00-1043 REV A
	SCALE NONE	CODE IDENT 23338	SHEET 1 OF 1

REV	ECN	BY	DATE	APP
A	# 3932	SC	91482	

A	ECN 4090	RO	3/84	



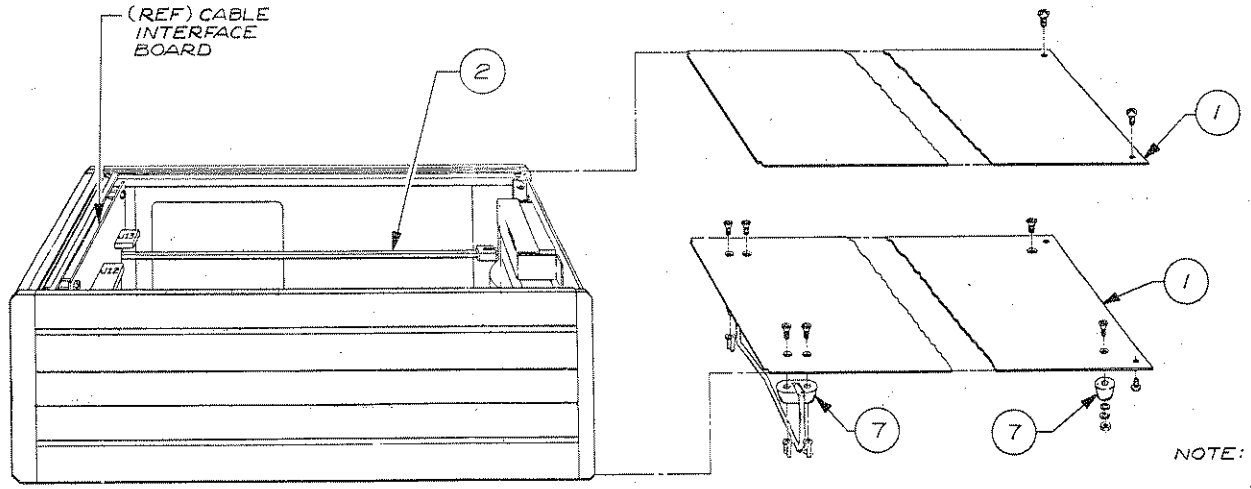
VIEW "A"

NOTE: UNLESS OTHERWISE SPECIFIED

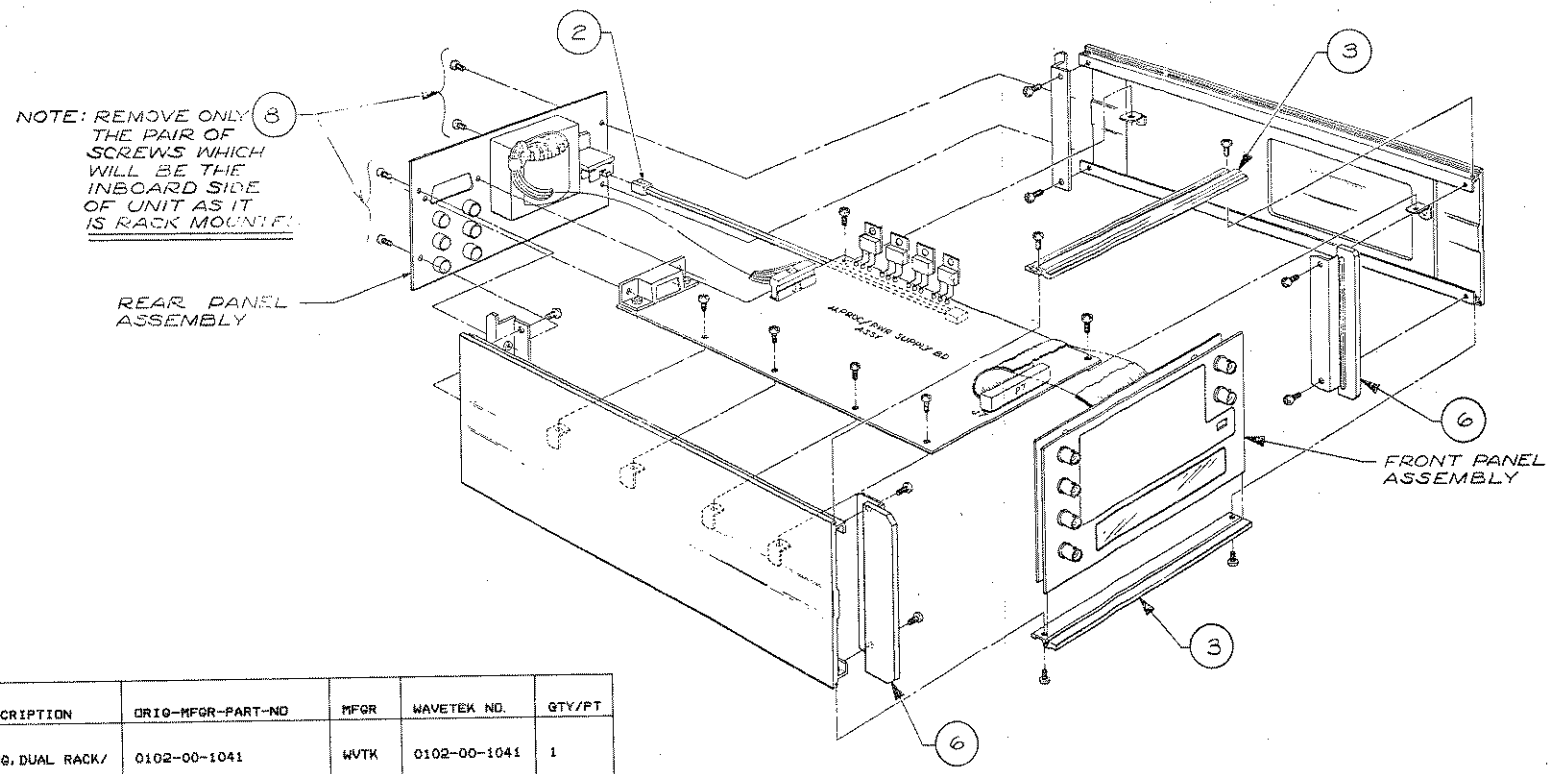
REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 4.26.82	WAVETEK SAN DIEGO • CALIFORNIA
MATERIAL	PROJ ENGR RBG	7/15/83	TITLE: DUAL RACK MOUNT, 270 SERIES
FINISH WAVETEK PROCESS	RELEASE APPROV		
	TOLERANCE UNLESS OTHERWISE SPECIFIED .XXX ±.010 ANGLES ±1° .XX ±.030		
	DO NOT SCALE DWG		MODEL NO. 270 SERIES / DWG NO. 0102-00-1041 / REV A
	SCALE NONE		CODE IDENT 23338 / SHEET 1 OF 2

REV	ECN	BY	DATE	APP

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3994



VIEW "B"



SEQUENCE OF CHANGES FOR DUAL RACK-MOUNTING (USE ORIGINAL SCREWS EXCEPT ITEM 9.)

1. REMOVE TOP AND BOTTOM COVERS (REF ITEMS #1)
2. REMOVE POWER ROD ASSEMBLY (REF ITEM #2) THRU FRONT PANEL ASSEMBLY.
3. REMOVE BOTH TOP AND BOTTOM FRONT HORIZONTAL TRIM PIECES (REF ITEMS #3) TO BE REPLACED BY NEW TRIM (REF ITEMS #12).
4. DISCONNECT PLUGS, "P12" (AND "P13" IF APPLICABLE) FROM CABLE INTERFACE BD., ALSO DISCONNECT "P7" FROM MICROPROC/POWER SUPPLY BOARD.
5. REMOVE FRONT PANEL ASSEMBLY.
6. REMOVE FRONT VERTICAL TRIM PIECES (REF ITEMS #6) AND REPLACE WITH APPROPRIATE REPLACEMENTS (REF ITEM #'S 13 AND 14).
7. REMOVE FEET AND BAIL ASSEMBLY (REF ITEMS #7) FROM BOTTOM COVER, AND REASSEMBLE BY REVERSING STEPS 1 THROUGH 6.
8. REMOVE APPROPRIATE (INBOARD ONLY) REAR PANEL MOUNTING SCREWS (REF ITEMS #8).
9. INSTALL NEW VERTICAL BRACKET (REF ITEM #9) TO REAR PANELS OF UNITS ON INBOARD MOUNTING HOLES, USING SUPPLIED 6-32 x 3/4 SCREWS AND #6 LOCKWASHER.

VIEWS ARE SHOWN TO ILLUSTRATE MECHANICAL BUILD UP OF UNIT PERTAINING TO ITEMS WHICH MUST BE REMOVED AND REPLACED BY NEW ITEMS TO MAKE A DUAL RACK MOUNT SET UP.

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, DUAL RACK/ ADAPTER	0102-00-1041	WVTK	0102-00-1041	1
NONE	JOINER, REAR PANEL	270-5493	WVTK	1400-01-5493	1
NONE	SCREW, 6-32X3/4 PHP, Z	6-32 X 3/4 PAN	CMRCL	2800-38-6112	4
NONE	#6 LOCKWASHER, PLATED	#6SRLW	CMRCL	2800-42-6000	4
NONE	EXTRUSION, TOP/ BOTTOM	MP-40951-0	BUKEY	3000-00-0099	2
NONE	HANDLE, DUAL RACK MOUNT	MP40110-2	BUKEY	3000-00-0100	2
NONE	EXTRUSION, FRONT SIDE	MP-40952-01	BUKEY	3000-00-0101	2

WAVETEK PARTS LIST	TITLE	ASSEMBLY NO.	REV
	R/M STYLE 13, DUAL R/A KIT, 270 SERIES	1101-00-1041	A
		PAGE 1	

VIEW "C"

VIEW "C" IS SHOWN WITH UNIT UPSIDE DOWN.

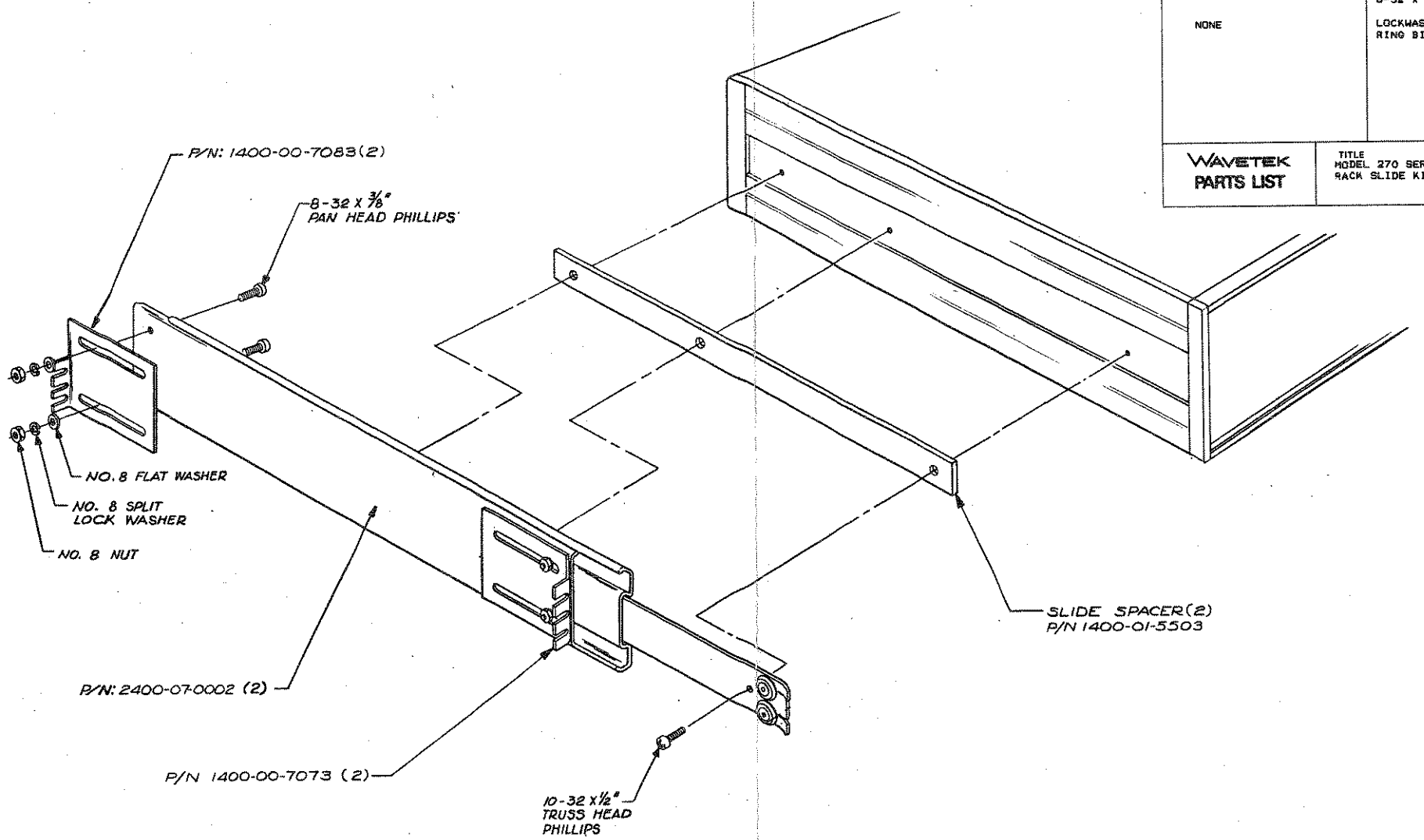
NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 4-26-82	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJ ENGR RBG	7/15/83	TITLE: DUAL RACK MOUNT 270 SERIES
	RELEASE APPROV BCH		
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1° XX ±.030		
	DO NOT SCALE DWG	MODEL NO 270 SERIES	DWG NO 0102-00-1041 REV A
	SCALE NONE	CODE IDENT 23338	SHEET 2 OF 2

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3854

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, RACK SLIDES	0102-00-1042	WVTK	0102-00-1042	1
NONE	EAR, RACK SLIDE	1400-00-7073	WVTK	1400-00-7073	2
NONE	EAR, RACK SLIDE	1400-00-7083	WVTK	1400-00-7083	2
NONE	SPACER, SLIDE	1400-01-5503	WVTK	1400-01-5503	2
NONE	SLIDES REF: 2400-99-0002	1108D-20-1	NL	2400-07-0002	2
NONE	NUT, HEX, CAD I, 8-32	8-32 HEX NUT	CMRCL	2800-14-8100	8
NONE	SCREW, TRUSS HD, CROSS RECESS, 10-32X 3/8	10-32 X 3/8	CMRCL	2800-20-0106	6
NONE	WASHER, FLAT, #8	#8 FW	CMRCL	2800-26-8000	8
NONE	SCREW, PAN, CAD I, CROSS RECESS, 8-32 X 3/8	8-32 X 3/8 PAN	CMRCL	2800-38-8106	8
NONE	LOCKWASHER, #8 SPLIT RING BIN 540	#8SRLW	CMRCL	2800-42-8000	8

WAVETEK PARTS LIST	TITLE MODEL 270 SERIES RACK SLIDE KIT	ASSEMBLY NO. 1101-00-1042 PAGE: 1	REV A

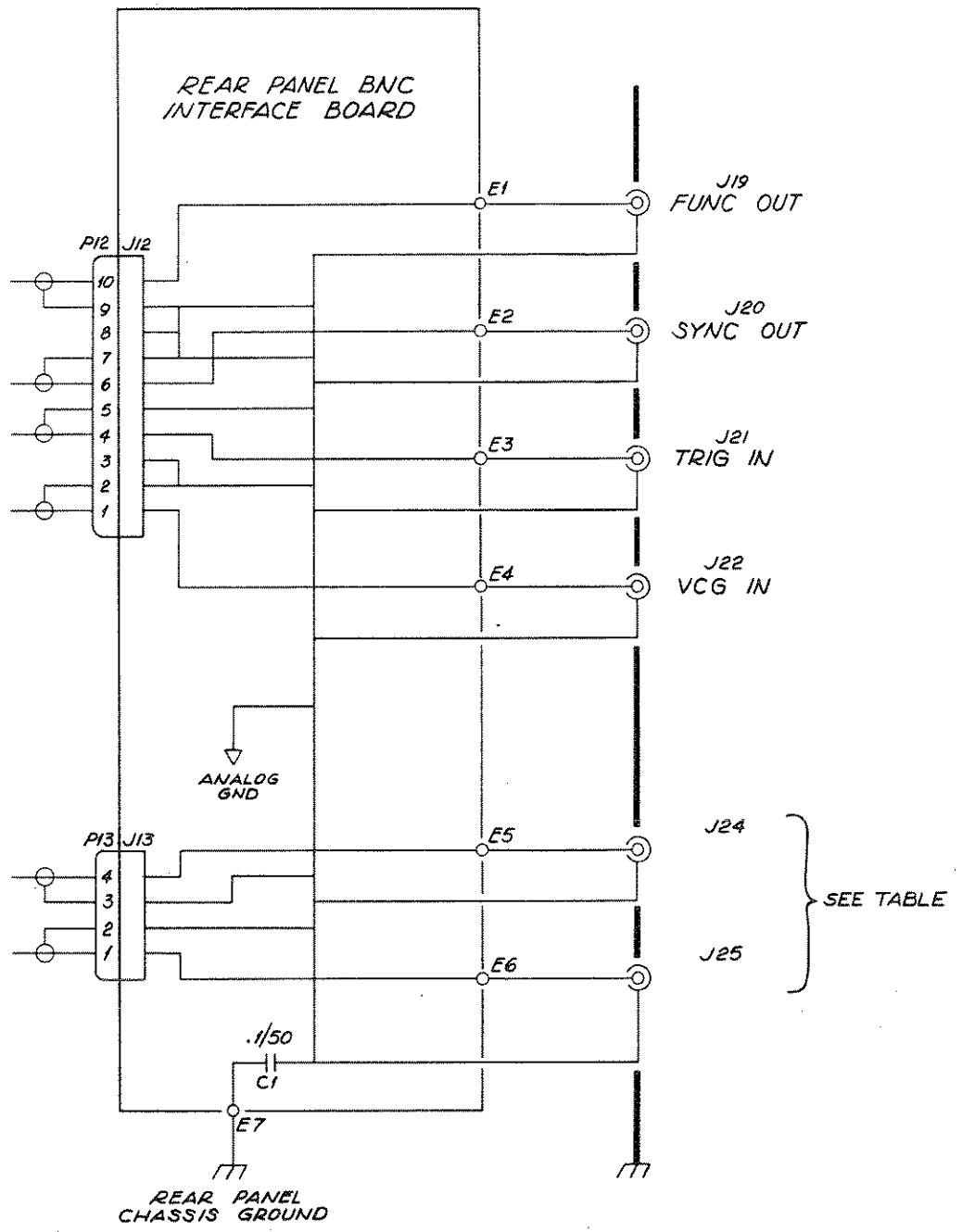


TYP BOTH SIDES

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN CHERMACK	DATE 9.30.82	WAVETEK SAN DIEGO, CALIFORNIA
MATERIAL	PROJENGR KBL	9/15/83	TITLE ASSEMBLY, RACK SLIDE
	RELEASE	APPROV	
FINISH WAVETEK PROCESS	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ± .010 ANGLES ± 1 XX ± .020		
	DO NOT SCALE DWG	MODEL NO 270 SERIES	DWG NO 0102-00-1042 REV
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A-3894



TABLE

MODEL	CONNECTOR	LABEL
270	J24	N/A
	J25	N/A
271	J24	N/A
	J25	N/A
273	J24	MARKER OUT
	J25	HORZ/GCV OUT
275	J24	ARB RTS/HOLD IN
	J25	ARB SYNC OUT
278	J24	REF IN
	J25	REF OUT

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	ASSY DRWG, REAR PANEL BNC BOARD	0101-00-1010	WVTK	0101-00-1010	1
NONE	SCHEMATIC, REAR PANEL BNC BOARD	0103-00-1010	WVTK	0103-00-1010	1
C1	CAP, CER, MON, .1MF, 50V	CAC03Z5U104Z050A	CORNG	1500-01-0405	1
10	REAR PANEL BNC BD	1700-00-1010	WVTK	1700-00-1010	1
6	CONNECTOR, HEADER (10 PIN)	102202-7	AMP	2100-02-0132	1
2	TERM, LOCK LUG	1414-8	SMITH	2100-04-0010	1

WAVETEK PARTS LIST	TITLE PCA, REAR PANEL BNC	ASSEMBLY NO. 1100-00-1010 PAGE: 1	REV

NOTE UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES	DRAWN FN AQUINO 6/2/82	WAVETEK SAN DIEGO • CALIFORNIA	
MATERIAL	PROJ ENGR RBS 7/15/82	TITLE OPTION 002 REAR PANEL BNC'S	
FINISH WAVETEK PROCESS	RELEASE APPROV [illegible]		
	TOLERANCE UNLESS OTHERWISE SPECIFIED XXX ±.010 ANGLES ±1 XX ±.030		
	DO NOT SCALE DWG	MODEL NO 270 SERIES	DWG NO 0103-00-1010 REV A
	SCALE	CODE IDENT 23338	SHEET 1 OF 1

BISHOP GRAPHICS/ACCUPRESS REORDER NO. A 3954

REV	ECN	BY	DATE	APP

REFERENCE DESIGNATORS	PART DESCRIPTION	ORIG-MFGR-PART-NO	MFGR	WAVETEK NO.	QTY/PT
NONE	INSTALLATION DRAWING MODEL 275-004 OPTION	0002-00-0208	WVTK	0002-00-0208	1
NONE	RAM, 8KX8 STATIC	HM6264LP-15	HTACH	8000-62-6400	2

WAVETEK PARTS LIST

TITLE: OPTION 004 ARB EXTENDED MEMORY FOR MODEL 275

ASSEMBLY NO.: 1000-00-0208

REV:

PAGE 1

NOTE: UNLESS OTHERWISE SPECIFIED

REMOVE ALL BURRS AND BREAK SHARP EDGES

MATERIAL

FINISH: WAVETEK PROCESS

DRAWN | DATE

PROJENGR

RELEASE APPROV

TOLERANCE UNLESS OTHERWISE SPECIFIED: .XXX ±.010 ANGLES ±1° .XX ±.030

DO NOT SCALE DWG

SCALE

WAVETEK SAN DIEGO • CALIFORNIA

TITLE: PARTS LIST MODEL 275-004 OPTION ARB EXTENDED MEMORY

MODEL NO.: 275

DWG NO.: 1100-00-0208

REV:

CODE IDENT: 23338

SHEET 1 OF 1

REV	ECN	BY	DATE	APP

APPENDIX A
AMERICAN STANDARD CODE FOR INFORMATION INTERCHANGE (ASCII)

b7 b6 b5 / BITS / b4 b3 b2 b1 / column / row	0_0	MSG[1]	0_1	MSG	$0_1{}_0$	MSG	$0_1{}_1$	MSG	$1_0{}_0$	MSG	$1_0{}_1$	MSG	$1_1{}_0$	MSG	$1_1{}_1$	MSG
	0		1		2		3		4		5		6		7	
0 0 0 0 / 0	NUL		DLE		SP		0		@		P		\		p	
0 0 0 1 / 1	SOH	GTL	DC1	LLO	!		1		A		Q		a		q	
0 0 1 0 / 2	STX		DC2		"		2		B		R		b		r	
0 0 1 1 / 3	ETX		DC3		#		3		C		S		c		s	
0 1 0 0 / 4	EOT	SDC	DC4	DCL	$		4		D		T		d		t	
0 1 0 1 / 5	ENQ	PPC[3]	NAK	PPU	%		5		E		U		e		u	
0 1 1 0 / 6	ACK		SYN		&		6		F		V		f		v	
0 1 1 1 / 7	BEL		ETB		'		7		G		W		g		w	
1 0 0 0 / 8	BS	GET	CAN	SPE	(		8		H		X		h		x	
1 0 0 1 / 9	HT	TCT	EM	SPD	)		9		I		Y		i		y	
1 0 1 0 / 10	LF		SUB		*		:		J		Z		j		z	
1 0 1 1 / 11	VT		ESC		+		;		K		[		k		{	
1 1 0 0 / 12	FF		FS		,		<		L		\		l		|	
1 1 0 1 / 13	CR		GS		-		=		M		]		m		}	
1 1 1 0 / 14	SO		RS		.		>		N		^		n		~	
1 1 1 1 / 15	SI		US		/		?	UNL	O		_	UNT	o		DEL	

MLA ASSIGNED TO DEVICE

MTA ASSIGNED TO DEVICE

MEANING DEFINED BY PCG CODE

MEANING DEFINED BY PCG CODE

ADDRESSED COMMAND GROUP (ACG)

UNIVERSAL COMMAND GROUP (UCG)

[4] LISTEN ADDRESS GROUP (LAG)

TALK ADDRESS GROUP (TAG)

PRIMARY COMMAND GROUP (PCG)

SECONDARY COMMAND GROUP (SCG)

[1]MSG = INTERFACE MESSAGE
[2]b1 = DIO1 . . . b7 = DIO7
[3]REQUIRES SECONDARY COMMAND
[4]DENSE SUBSET (COLUMN 2 THROUGH 5)

DC4	=	DCL	Device clear
DC1	=	LLO	Local lockout
NAK	=	PPU	Parallel poll unconfigure
EM	=	SPD	Serial poll disable
CAN	=	SPE	Serial poll enable

} Universal Command Group

SOH	=	GTL	Go to local
EOT	=	SDC	Selected device clear
ENQ	=	PPC	Parallel poll configure
BS	=	GET	Group execute trigger
HT	=	TCT	Take control

} Addressed Command Group

APPENDIX B
PROGRAMMING COMMAND SUMMARY
(Excluding GPIB Command Groups Given in Appendix A).

Control and Data Names	Model 275 Key	ASCII Character (GPIB)
Change Sign	+/−	−
Decimal Point	•	•
0, 1, 2, . . . 9	0, 1, 2, . . . 9	0, 1, 2, . . . 9
Amplitude	AMPL	A
Mode	MODE	B
Function	FUNC	C
Offset	OFST	D
Exponent	EXP	E
Frequency	FREQ CLK	F
External/Internal Trigger	EXT	G
Manual Trigger Released (Gate Off)	MAN (Released)	H
Execute	EXEC	I
Manual Trigger Pushed	MAN (Pressed)	J
Arb Address	ADB ADRS	K
Arb Data	ARB DATA	L
Store Setting	STOR	M
Output On/Off	ON	P
Trigger Slope	SLP	Q
Burst	BRST	R
Arb Clock Period	FREQ CLK	S
Internal Trigger Rate	RATE	T
Recall Setting	RCL	Y
Reset	RST	Z
Start Address	STRT STOP	XB
Percent Frequency	_____	XF
Get Mode	_____	XG
Stop Address	STRT STOP	XH
Auto-line	AUTO LINE	XK
Trigger Level	LVL	XL
SRQ Mode	_____	XQ
Talk Mode	_____	XT
Recall Next Lesser Numbered Program	_____	XU
Terminator	_____	XV
Recall Next Greater Number Program	_____	XW
Arb Monitor	ARB MNTR	_____
Cursor	↑, ↓, ←, →	_____
Clear Entry	CLR	_____
Beep On/Off	♪	_____
Status Display	STAT	_____
Service Request	SRQ	_____
GPIB Address	GPIB ADRS	_____
Command Recall	CMD RCL	_____
Return to Local	LCL	_____

APPENDIX B (Cont)

Function (C) Code

0 Sine
1 Triangle
2 Square
3 Square Complement
4 DC
5 External Width
6 Arbitrary
7 Filtered Arbitrary

Main Generator Mode (B) Code

0 Continuous
1 Triggered
2 Gated
3 Burst
4 Triggered Arb with Ramp-to-Start
5 Triggers Arb and Hold with Triggered Ramp-to-Start
6 Triggered Arb with Reset
7 Triggered Arb and Hold with Triggered Reset
8 Single Step
9 Examine
10 Triggered Arb with Hold on Break Point

Output On/Off (P) Code

0 Output Off, HI Z
1 Output On
2 Output Off, LO Z

Trigger Slope (Q) Code

0 Positive Edge
1 Negative Edge

GET Mode (XG) Codes

NOTE: This parameter selects which kind of action the 275 will take when it receives a GET command.

0 Execute and Trigger Upon Receipt of GET Command (No Error Checking).

SRQ (XQ) Code

NOTE: This parameter selects the conditions under which the SRQ line is asserted. Value can be 0 through 255. The equivalent binary value masks or unmasks the serial poll response byte bits as shown in table B-1. Example: Binary1 = Selected, Binary 0 = Not Selected.

XQ1 is the SRQ power-up mode. (The rsv bit is always asserted selected or not.)

Table B-1
Serial Poll Response Byte

Bit Weight	**128 (MSB)**	**64**	**32**	**16**	**8**	**4**	**2**	**1 (LSB)**
Bit Meaning	SRQ Key (Front Panel)	rsv	Ramp to Start Com-pleted	Execute Com-pleted	Low Battery	Fuse Blown	Output Protection	Program Error
Example*	1	0	0	0	0	0	0	1

Select Program Error and SRQ key (XQ129**)*

Talk Message (XT) Code

NOTE: This parameter selects the kind of message the 275 will send when it is addressed as a talker on the GPIB.

0 Programming Error list (only errors from GPIB input). 0 is the power-up talk mode. A typical error string is E 1F 2AD 3Y. Some error string characterics are:

a. All error strings begin with E.

b. Most recent error is at the end of string.

c. Errors are separated by blanks.

d. Class 1 Errors: A 1 followed by programming character that caused the error.

e. Class 2 Error: A 2 followed by the two conflicting program characters.

f. Class 3 Error: A 3 followed by M (Store) or Y (Recall).

g. Error strings can be up to 80 characters including E and blanks.

h. After transfer, the instrument clears the error string.

1 Poll Byte Response: The byte that would be sent if a serial poll were performed. The controller, upon reading this byte, clears the poll byte and resets the SRQ line if asserted.

2 The most recently selected parameter and its value. Example: FREQ 1E3. (The "most recently selected parameter" is the parameter at the end of the command string.) If no parameter is selected; e.g., power-on state, reset, or execute command then the instrument returns: NO PARAMETER SELECTED. Note that the NO PARAMETER SELECTED message will be returned if the last command in the string is an EXECUTE command (I).

3 The entire instrument setup after last execute. Example: F1EA1D0C0P0Q0XL1.5.

4 The instrument setup when executed is received; same format as XT3.

5 Instrument Identification: WAVETEK MODEL 275 V(X.Y). X.Y identifies the software version number.

6 The time since the instrument was powered on. Example Time: 1.3. Unit of measure is hours with 0.1 hour resolution (6 minutes).

7 The accumulated operating time. Example: TOTAL TIME: 306.2.

NOTE:

Toggling switch 7 (figure 2-2) clears the instrument-operating-time clock. With SW7 on, the clock runs during power on. With SW7 off, the clock clears to zero.

8 The number of stored settings installed. For the 275: STORED SETTINGS 75.

9 Readback of ARB generator status: Returns the instantaneous value of the ARB output in the form "X D.DDED Y D.DDED V D.DDED".

10 Returns the data at the current address then increments the address. Used to load a waveform from a Wavetek 275 to a controller. Returns " – 9999" when front panel lockout is activated.

11 Returns the data value at the beginning of the Ramp-to-Start (RTS) operation.

12 For factory use only.

APPENDIX C
DISPLAYS

Key Pressed	Display - ACTUAL (Explanation)
ADRS	ADDRESS VALUE (X)
ADRS	GPIB ADRS (Decimal address)
AMPL	AMPLITUDE (Value) (mV or V)
ARB MNTR	Value (X)(Y) (Volts)
♪ (beep)	(Audible beep)
BRST	BURST COUNT (Value)
CLR	(Clears any unexecuted numerical entry of the last parameter entered)
CMD RCL	(A string of letters and numbers up to 40 characters long displayed 20 characters at a time and shifted by the cursor ←, →)
CURSOR ←, →	(If a value is being displayed, the selected digit blinks. If there is no value being displayed, there is no effect. If it was a command recall, ← shifts the display four characters to the left. If it was a command recall, → shifts the display four characters to the right.
CURSOR ↑	(If the display is a value, code or storage location number, it increments.)
CURSOR ↑	(If the display is a value, code or a storage location number, it decrements.)
DATA	DATA Value (Y)
EXEC	EXECUTE (If no type 2 errors)
EXP	(If previous display was a value or a code, it is suffixed with an E.)
EXT	EXTERNAL TRIGGER (0) or INTERNAL TRIGGER (1)
FREQ/CLK	FREQ (Value) (mHz, Hz, kHz or MHz), CLK (Value) ns, μs, ms, sec)
FUNC (MAIN)	FUNC (Function) (Code)
LCL	LOCAL
LVL	TRIG LEVEL (Value) (mV or V)

Under remote operation, certain characters may appear in the extreme right side of the display. Those characters are:

R — Remote
L — Addressed to Listen
T — Addressed to Talk
Q — Request for service because of selected SRQ code.

APPENDIX C (Continued)
DISPLAYS

Key Pressed	Display - ACTUAL (Explanation)
MAN TRIG	(When pressed: No display if in continous mode, TRIGGER if in any triggered or burst mode, GATE if in gated mode. When released no effect in any triggered or burst mode; GATE OFF if in a gated mode.)
MODE	MODE (Mode) (Code)
ON	OUTPUT (OFF; ON (1); or OFF, LO Z(2))
OFST	OFFSET (+ or −) (Value) (mV, V)
RATE	TRIG RATE (Value) (mHz,Hz, KHz, or MHz)
RCL	No. (Value) LAST RECALLED
RST	RESET or UNIT REMOTE (if in remote)
SLP	TRIG SLOPE (POS (0) or NEG (1))
STOR	No. (Value) LAST STORED
STAT	(Display changes automatically) FREQ (Value) (mHz, Hz, kHz or MHz) AMP (Value) (mV or V) OFFSET (Value) (mV or V) MODE (Mode) (Code) FUNC (Function) (Code) BURST (Value) CLOCK (Value) (nsec, μsec, msec, or sec) START ADDRESS (Value) STOP ADDRESS (Value) OUTPUT (OFF (0); ON (1); or OFF, LO Z(2)) EXTERNAL (0), INTERNAL (1) TRIG RATE (mHz, Hz, KHz, or MHz) TRIG SLOPE (POS or NEG) (Code) TRIG LEVEL (+ or −) (Value) (mV or V)
(Number key)	(Number corresponding to the selected key.)

APPENDIX D MODE, WAVEFORM AND TIMING REFERENCE SHEET

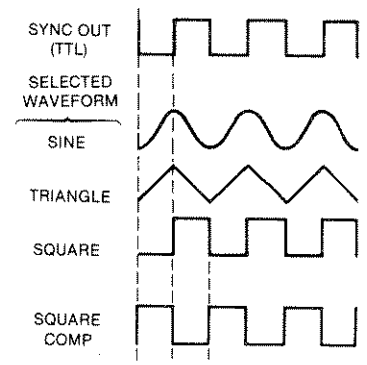
Functions

Code	Function
0	Sine
1	Triangle
2	Square
3	Square Complement
4	DC
5	External Width
6	Arbitrary
7	Filtered Arbitrary

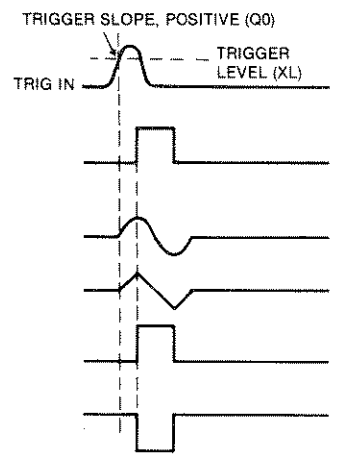
Operational Modes (Function/ARB)

Code	Mode
0	Continuous
1	Triggered
2	Gated
3	Burst
4	Triggered Arb with Ramp-to-Start
5	Triggered Arb with Hold and Triggered Ramp-to-Start
6	Triggered Arb with Reset
7	Triggered Arb with Hold and Triggered Reset
8	Single Step
9	Examine
10	Triggered Arb with Hold on Breakpoint

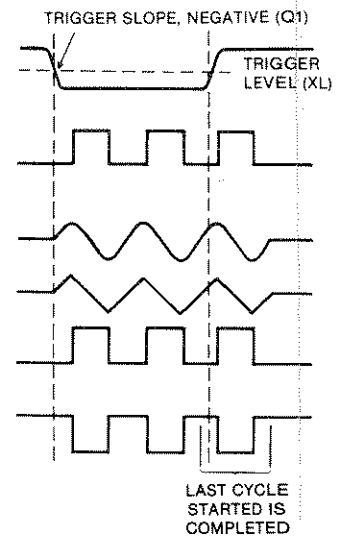
Mode 0 Continuous



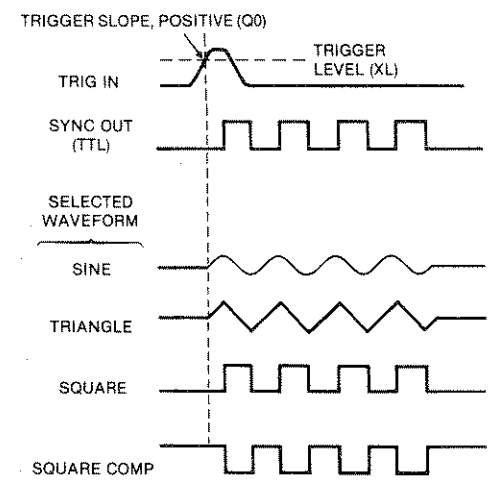
Mode 1 Triggered



Mode 2 Gated



Mode 3 Burst



NOTE: NUMBER OF CYCLES IS PROGRAMMED (1 THROUGH 1,048,200)

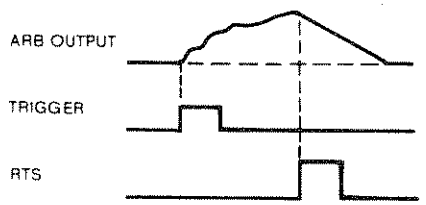
Recall Setting Menu

Recall (RCL)	Setting
RCL 0	RCL Last Power Off Condition
RCL 1-75	RCL Standard Stored Settings
RCL 1000-1031	Internal Calibration Procedure
RCL 2000-2007	Internal QA Test/ Demonstration Procedure
RCL 3000	Panel Lockout Off
RCL 3001	Panel Lockout On
RCL 4000	Arb Sync Positive
RCL 4001	Arb Sync Negative
RCL 5000	Ramp-to-Start Slow
RCL 5001	Ramp-to-Start Fast
RCL 6000	Clear All Breakpoints

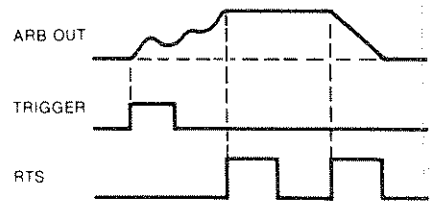
ARB Monitor

Continuously samples address and data of Arb generator for display on front panel. Also available from GPIB.

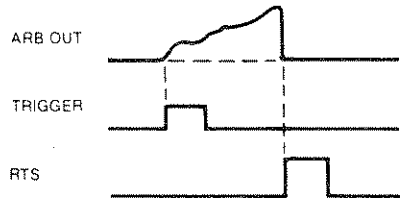
Mode 4 Trig Arb Ramp-to-Start



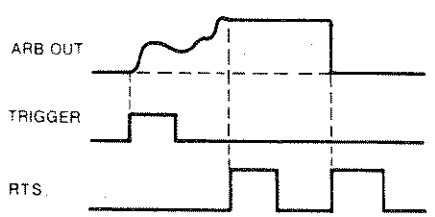
Mode 5 Trig Arb Hold and RTS



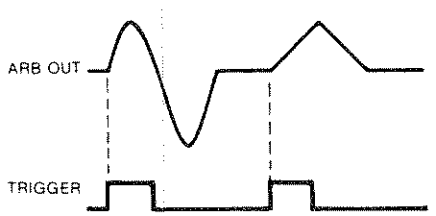
Mode 6 Trig Arb With Reset



Mode 7 Trig Arb Hold and Reset



Mode 10 Trig Arb Hold On Breakpoint



APPENDIX E
Glossary of Mnemonics

Microprocessor/Power Supply Board

AD0 to AD7	Bidirectional, multiplexed, 8 bit address/data bus from/to microprocessor
ADR0 to ADR15	16 bit address bus from microprocessor-lower 8 bits are latched from AD0 to AD7
$\overline{\text{ANA0}}$ to $\overline{\text{ANA3}}$	4 line address decoding for analog con trol lines to function generator and synthesizer board
$\overline{\text{ANALOG}}$	Decode line for analog section of memory
ANL0 to ANL27	28 analog logic signals to function generator board
$\overline{\text{AR0}}$ to $\overline{\text{AR3}}$	4 line address decoding to analog registers for function generator board control lines
AS	Address strobe from microprocessor
ATN	IEEE-488 "attention"
BADR0 to BADR2	3 buffered address lines to synthesizer board
BATV	Battery voltage
BDATA0 to BDATA7	8 bit, buffered, latched data bus to synthesizer board
D101 to D108	8 bit, IEEE-488 data bus
DAC	IEEE-488 "data accepted"
DATA0 to DATA7	8 bit, latched data bus for control lines to the display, sample and hold, and analog interface
DAV	IEEE-488 "data valid"
$\overline{\text{DISP}}$	Decode line for display section of memory
E	Enable line from microprocessor
EOI	IEEE-488 "end or identify"
FPADEN	Front panel GPIB address entry switch
GA0 to GA4	GPIB address switches corresponding to 2^0 through 2^4 respectively. (1 through 16) adding to 31 maximum
$\overline{\text{GPIB}}$	Decode line to select the IEEE-488 interface (general purpose interface bus)
IFC	IEEE-488 "interface clear"
$\overline{\text{KYBD}}$	Decode line to select keyboard
$\overline{\text{MR}}$	Master reset to initialize microprocessor
$\overline{\text{NMI}}$	Non-maskable interrupt line to microprocessor
PORT 10 to PORT 17	8 line I/O port 1 to/from microprocessor
PORT 20 to PORT 24	5 line I/O port 2 to/from microprocessor
$\overline{\text{RAM1}}$ & $\overline{\text{RAM2}}$	Address decode lines for random access memory IC's 1 and 2
REN	IEEE-488 "remote enable"
RFD	IEEE-488 "ready for data"
$\overline{\text{ROM1}}$ to $\overline{\text{ROM2}}$	Address decode lines for read-only memory IC's 1 and 2
R/$\overline{\text{W}}$	Read/write line from microprocessor
SH0 to SH3	4 sample-and-hold analog signals to function generator board

APPENDIX E (Cont)

SRQ	IEEE-488 "service request"
TEST	Control line to allow operation with external test program—not normally used
$\overline{WRP}$	Write pulse to RAM

Display Board (Excluding Mnemonics Common to Microprocessor/Power Supply Board)

ANOA to ANOO & ANODP	Vacuum florescent display anodes corresponding to 14 segments, comma, and and decimal point, respectively
$\overline{BLANK}$	Blanking control for display and scan clock
DSP	Display synchronizing pulse for shift register scan
GRID 1 to GRID 20	Display grids controlling each digit

Function Generator Board

AMP	Analog control voltage for amplitude (SH1)
AMPLDC	XY multiplier feedback of amplitude control dc test line
$\overline{CPM}$	Capacitance multiplier select line (ANL15)
$\overline{DCA}$	DC amplifier select line (ANL13)
DCCOMP	DC compensation and low frequency linearity correction for triangle buffer test line
EXW	External width select line (ANL18)
$\overline{FR0}$ to $\overline{FR7}$	Frequency range select lines to range capacitors, capacitance multiplier, and frequency compensation (ANL0 to ANL7)
FRQ	Analog control voltage for frequency (SH0)
FUB	Signal to microprocessor that output fuse is blown (PORT11)
MC0 & MC1	2 mode control lines (ANL11 and ANL12)
OA0 & OA2	2 output attenuator control lines (ANL8 and ANL10)
OAP	signal to microprocessor that the output amplifier protection circuit is operating (PORT 10)
OST	Analog control voltage for offset (SH2)
$\overline{OVR}$	Frequency overrange select line (ANL14)
PATEST	Preamplifier output test line
PLS	Pulse input select line (ANL25)
$\overline{PLS}$	Pulse complement select line (ANL24)
PLSI	Pulse input from auxiliary board
$\overline{RCT}$	Rectangular waveform select line—square or pulse (ANL23)
$\overline{SIN}$	Sine wave select line (ANL21)
SQB	Output from square buffer
SQR	Square wave select line (ANL20)
$\overline{SQR}$	Square complement select line (ANL19)
SQS	Square buffer to square logic signal
THC	Trigger holding current
TRB	Triangle buffer output
TRGI	Trigger input from arb gen board
TRGO	Trigger output to arb gen board
$\overline{TRI}$	Triangle wave select line (ANL22)
TRITST	Triangle buffer output test line

APPENDIX E (Cont)

TRL	Analog control voltage for trigger level (SH3)
TRN	Triangle generation current node
VCGI	Not used in Wavetek 275
VCGO	Not used in Wavetek 275
VCGTST	Voltage control generation circuit test line
VCV	Voltage control generation circuit voltage ouput
XYI	X-Y multiplier input
+I	Tracking current (I) source from VCG
−I	Tracking current (I) sink to VCG
+TR	Rising edge trigger select line (ANL 17)
−TR	Falling edge trigger select line (ANL 16)

Arbitrary Waveform Generator Board

$\overline{\text{ARB MEM EN}}$	CHIP SELECT line to ARB RAMs U42 and U43. Logic low enables RAMs.
ARB SYNC	Data line from ARB RAM circuit. Line is at logic high at last executed ARB RAM address.
B0-B19	Preset data lines for burst counter.
BCA	Output from burst counter circuit. Line is at logic high while burst counter is active (counting).
BRANCH EN	Control line to state machine sequence control circuit. Line is at logic high in gated and burst modes.
BURST	Burst counter control line; logic high enables burst counter.
$\overline{\text{BURST}}$	Logic complement of BURST line; is at logic low in burst mode.
BURST CLK SEL	Control line to select burst counter clock source; logic high selects SQS output of function generator board, while logic low selects STOP signal from ARB RAM circuit.
CLK	Output of phase accumulator clock selector U26.
D0-D7	Buffered data bus from microprocessor board via J16 DIGITAL INTERFACE CONNECTOR.
DATA SERIAL OUT	Data line from ARB RAM circuit shift registers to microprocessor readback data selector circuit.
DIVIDER EN	Control line to U36 programmable divider. Logic high enables divider; logic low initializes divider by clearing all internal flip-flops.
DS0-DS2	Data select lines to U25 microprocessor readback data selector.
EXT CLK EN	One of two control lines to phase accumulator clock selector U26. When the $\overline{\phi}$ $\overline{\text{ACC CLK EN}}$ line is low: a logic low on the EXT CLK EN line selects the SYNTH signal as the phase accumulator clock source, while a logic high selects the TRGOB signal.
$\overline{\text{FSLEW}}$	One of two slew rate control lines to ARB OUT circuit. Logic low on this line selects fast arbitrary waveform slew rate.
HOLD	Control line from state machine ROM to microprocessor readback data selector U25. The logic level on this line is significant only in the RTS modes; a logic high signals the microprocessor to begin the Ramp-to-Start operation.

APPENDIX E (Cont)

$\overline{\text{INT}}$/EXT — One of the control inputs to the U1 trigger select logic. A logic high on this line selects the TRGO output of the trigger comparator on the function generator board, while a logic low on this line allows the SYNTH TRIG SEL line to select either the synthesizer or function generator as the trigger source.

JUMP — Data line from ARB RAM jumper terminal E6 to microprocessor readback data selector U25. From the data on this line, the microprocessor can determine the position of the ARB RAM jumper, and therefore the size of the ARB RAMs installed.

$\overline{\text{LATCH EN}}$ — Active low enable line to data registers U31 and U32.

M0-M2 — Mode control lines to state machine ROM.

R0-R8 — Data register strobe lines. Low-to-high transition latches data at input of register through to register output.

R10-R13 — Data register strobe lines. Low-to-high transition latches data at input of register through to register output.

R15 — Data register strobe line. Low-to-high transition latches data at input of register through to register output.

RA0-RA12 — ARB RAM address lines from phase accumulator counter.

$\overline{\text{RAM EN}}$ — ARB RAM control line from data registers; logic low on line enables ARB RAM output.

RAM PWR — Power for ARB RAMs U42 and U43. Power is automatically supplied from backup battery on microprocessor board when instrument is turned off.

RD0-RD11 — Data lines from ARB RAM circuit.

S0-S12 — Lines from data registers to phase accumulator counter preset inputs.

SQS — Logic level square wave output of function generator board; used as input to burst counter and one of the inputs to the trigger select logic.

$\overline{\text{SSLEW}}$ — One of two slew rate control lines to ARB OUT circuit. Logic low on this line selects slow arbitrary waveform slew rate.

$\overline{\text{STATE CLR}}$ — Control line from data latch to U23 state counter. A logic low on this line clears the state counter.

STOP — Logic line from ARB RAM circuit; is at logic high at programmed stop address.

$\overline{\text{STOP}}$ — Complement of STOP line; is at logic low at programmed stop address.

SYNTH — Output of U36 in frequency synthesizer; can be selected as trigger source for burst counter or clock source for phase accumulator.

SYNTH EN — Control line to NAND gate U33B in state machine circuit. A logic low on this line forces the DIVIDER EN line to an unconditional logic high. A logic high on the SYNTH EN line allows the state machine trigger circuit to pulse the DIVIDER EN line low if the SYNTH SYNC EN line is also at a logic high.

SYNTH SYNC EN — Contol line to NAND gate U33D in state machine circuit. A logic high on this line allows the state machine trigger circuit to pulse the DIVIDER EN line low if the SYNTH EN line is also at a logic high.

SYNTH TRIG SEL — One of the control inputs to the trigger select logic. If internal trigger is selected, logic low on this line selects SQS output of function generator board while logic high selects SYNTH output of frequency synthesizer.

TBPC — Trigger Break Point Control. Data line from ARB RAM circuit; is at logic high at programmed breakpoints.

APPENDIX E (Cont)

TRGO — Trigger output from function generator board to U1 trigger select logic.

TRGOB — Buffered trigger output from U1 trigger select logic.

$\overline{\text{TRIG INHIBIT}}$ — Logic line from state machine sequence control circuit ROM U24 to U21A in state machine trigger circuit. A logic low on this line inhibits the state machine trigger circuit.

VCO OFF — Control line to VCO in synthesizer circuit. Logic high turns VCO off.

$\overline{\phi \text{ ACC CLK EN}}$ — One of two control lines to phase accumulator clock selector U26. A logic high on this line selects the R3 input from address decoder U18. A logic low enables the EXT CLK EN line to select either the SYNTH or TRGOB signal as the phase accumulator clock source.

μP INFO — Data line from U25 microprocessor readback data selector to microprocessor board via J16 digital interface connector.

APPENDIX F
WAVEFORM MEASUREMENTS

Frequency Jitter Measurement

Frequency jitter is defined as the cycle to cycle variation in period. Using a scope (with time base multiplier) display a square wave such that one cycle covers more than half the display (see figure F-1). Trigger the scope internally on the leading edge of signal. Using the time base multiplier expand the leading edge of the cycle after trigger by a factor of 100. Jitter is the peak to peak horizontal excursion of the displayed edge (see figure F-2). % jitter is given by:

$$\% \text{ Jitter} = (\text{Jitter/Period}) \times 100$$

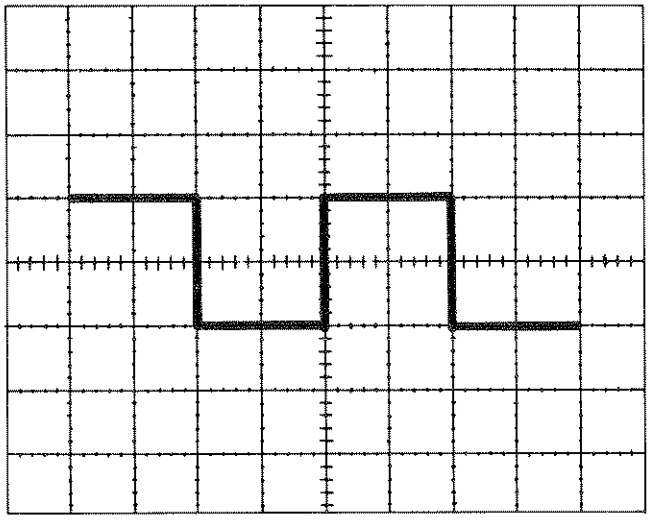


Figure F-1.

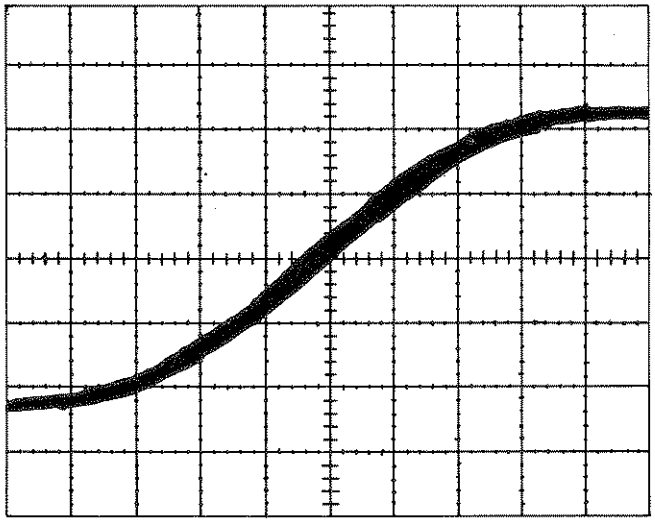


Figure F-2.

This test method is accurate for jitter caused by random or non-coherent noise sources. Coherent (harmonically related) cycle-to-cycle jitter requires unique verification.

Amplitude Measurements

There are several factors to be considered when making amplitude measurements. The type of DVM, the frequency range over which the meter is accurate, and the accuracy of the 50Ω load used for termination are the most important.

1. There are three basic types of DVM's: Averaging, true rms, and averaging scaled. The readings obtained can vary by more than 10% depending on DVM type and the waveform. The correct readings (related to volts peak to peak) are given below for each type of meter and each waveform.

   Average Reading:

Function	Reading
Sine	Vp-p/π
Triangle	Vp-p/4
Square	Vp-p/2

   True RMS:

Function	Reading
Sine	Vp-p/$2\sqrt{2}$
Triangle	Vp-p/$2\sqrt{3}$
Square	Vp-p/2

   Averaging Scaled: This type of meter measures internally like an average reading meter, but the displayed reading is scaled (multiplied by a constant) to read like a true rms meter. This scaling technique only works on sine waveforms; however, it gives less obvious results for other waveforms. The correct readings are given below:

Function	Reading
Sine	Vp-p/$2\sqrt{2}$
Triangle	(Vp-p × 1.1107)/4
Square	(Vp-p × 1.1107)/2
	or
Triangle	(Vp-p/4) × 1.1107
Square	(Vp-p/2) × 1.1107

2. Most ac volt meters have a relatively limited range of frequencies over which the meter is most accurate. For most meters this range is

about 500 Hz-5 kHz. In order to make accurate measurements the basic accuracy of the meter in its specified frequency operating range should be less than 0.2%.

3. The 50Ω load used to terminate the signal being measured can also introduce significant errors into the amplitude accuracy measurement. In general the measurement will be in error by 1/2% for every 1% error in the load. Standard loads available from Tektronix are ±2% accuracy. Therefore up to 1% error in amplitude measurement can result when using these loads. It is recommended to use a 0.1% accurate termination or to compensate the readings obtained based on the actual load value. The method for doing this is given below.
   a. Let R be the value of the termination.
   b. Let K be the correction factor applied to the DVM reading:

      Then: (correct reading) = (DVM reading) × K

      where $K = \frac{R+50}{2R}$

   Using this method the load tolerance can be ±5%.

Symmetry Measurements

1. Symmetry defined as a percentage is the ratio of positive half cycle time to the period (see figure F-3):

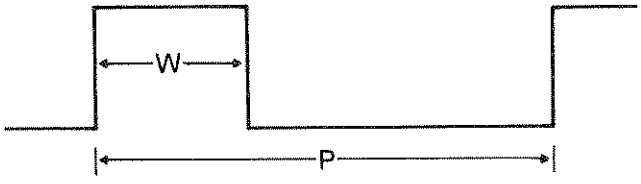


Figure F-3.

Where: % symmetry = (W/P) × 100

2. Symmetry error is, therefore, the difference from 50% symmetry:

   % Symmetry Error = [(½P—W)/P] × 100

3. When using a scope and alternately triggering on + and − slope of signal the symmetry error measured is twice the actual error. Therefore, when using this method the measured error must be divided by 2. Also, this method is only accurate at frequencies where the rise and fall time is not a significant part of the period. The period should be about 1000 times greater than the rise/fall time. This is about 10 μs or 100 kHz.
4. To measure symmetry at 12 MHz a different technique must be used. Connect signal (terminated into 50Ω) to a sampler set at 10 ns/div. Upper and lower levels should be exactly centered about horizontal centerline on scope display (see figure F-4). Rising edges of first and second cycle should be exactly equidistant from vertical center line. The distance of the falling edge from the vertical center line at the point falling edge crosses horizontal center line is the symmetry error.

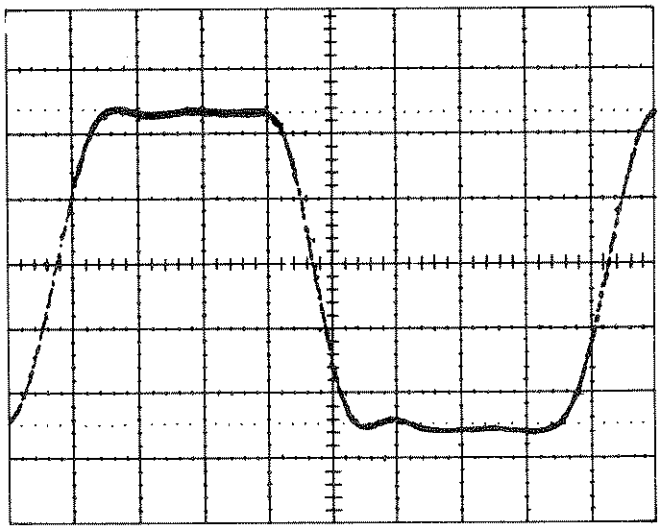


Figure F-4.

Waveform Quality Measurement

Waveform quality measurements should always be made using a sampling oscilloscope with precision 50Ω termination and cabling. Standard RG58 coax cable is not good enough for waveform quality measurements. Percent aberration is the ratio of absolute peak-to-peak variation from the 0% (negative level) or 100% (positive level) point on the square waveform to the absolute peak-to-peak amplitude of the square wave. See figures F-5, F-6 and formula shown below. In order to get an accurate display the top (or bottom) of the waveform should be expanded both vertically and horizontally to fill the scope display. The pictures below were made on a 5 Vp-p square waveform at 3 MHz and the scope horizontal and vertical were set to 20 ns/div and 100 mV/div respectively. Also, best

results are obtained when using the low noise (averaging) setting on the sampling scope.

$$\% \text{ ABERRATION} = \frac{|PK - PK\ VAR|}{|PK - PK\ SQWA|} \times 100$$

SQWA = SQUARE WAVE AMPLITUDE

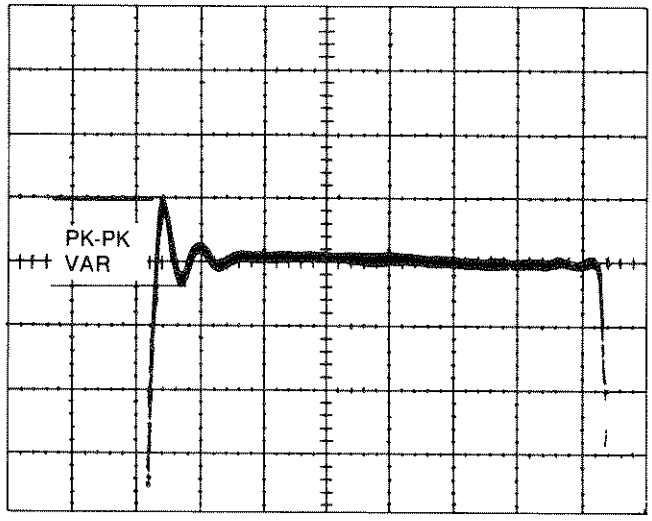


Figure F-5.

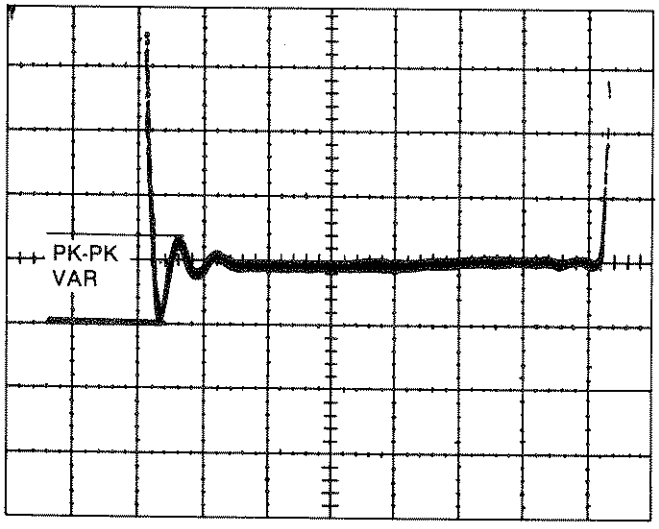


Figure F-6.

Width Measurement

Width is measured from the 50% point of the leading edge of the pulse to the 50% point of the trailing edge (see figure F-7). The pulse at the function out must be loaded into 50Ω.

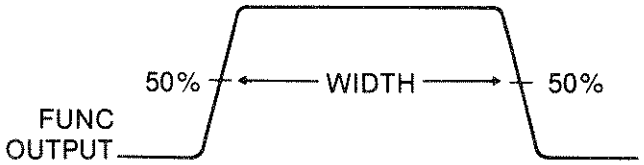


Figure F-7.

Width Duty Cycle Definition

Defined as a percentage, width duty cycle is the ratio of width to the minimum period that does not cause pulse dropout:

$$\% \text{ DUTY CYCLE} = (\text{WIDTH/MIN PERIOD}) \times 100$$

For example, if width were set to 100 ns and the minimum period that could be programmed before pulse dropout occurred was 163 ns then the duty cycle would be:

$$\% \text{ DUTY CYCLE} = (100E\text{-}9/163E\text{-}9) \times 100$$
$$\% \text{ DUTY CYCLE} = 61.3\%$$

Width Jitter Measurement

Width jitter is defined as the pulse to pulse variation in pulse width. Using a scope (with time base multiplier) display one pulse on scope display so the pulse covers at least half of display (see figure F-8). Scope must be triggered internally on leading edge of pulse (not sync out). Using the time base multiplier expand the trailing edge of pulse by a factor of 100. Jitter is measured as the peak to peak horizontal excursion of the trailing edge (see figure F-9). % Jitter is:

$$\% \text{ Jitter} = (\text{Jitter/Width}) \times 100$$

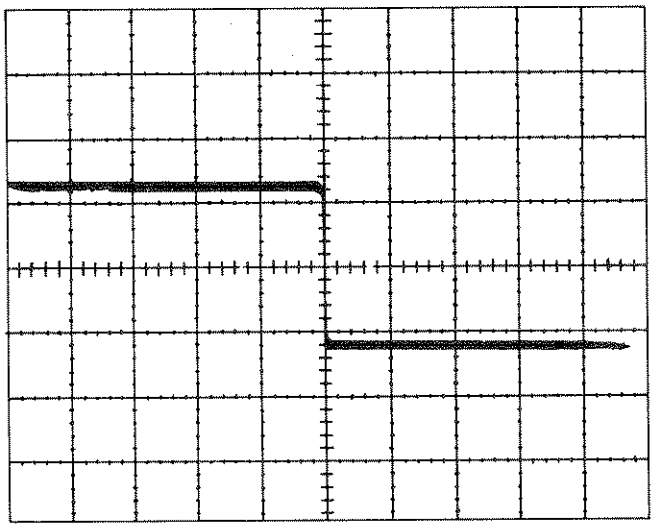


Figure F-8.

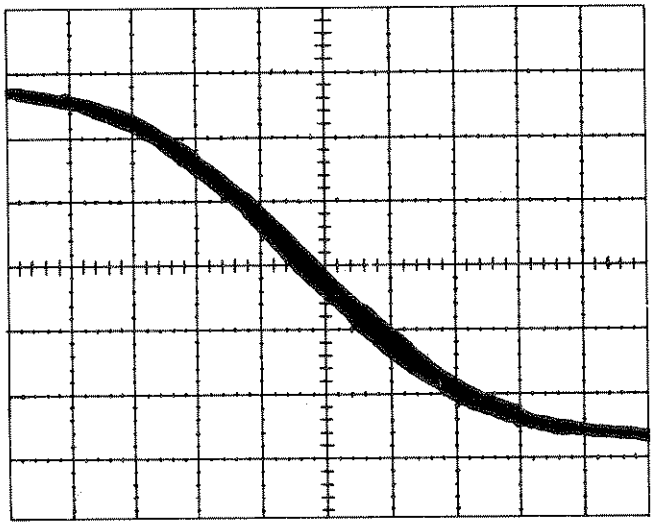


Figure F-9.