IEE 6703

ANALOG INTEGRATED CIRCUITS (I)

Lecture Note

CHUNG-YU WU

Integrated Circuits and Systems Laboratory
Department of Electronics Engineering
National Chiao Tung University
September 2000

IEEE 6703 ANALOG INTEGRATED CIRCUITS (I)

CHUNG-YU WU
FALL, 2000

Course Contents:

1. Analog MOSFET Device Physics and SPICE Models
2. CMOS Process Technology and Layout Rules
3. Current Sources and Simple Voltage Sources
4. Amplifiers, Level Shifting Circuits, and Output Stages
5. Noise Analysis of Analog Amplifiers
6. Midband Analysis of Operational Amplifiers (OP AMPs)
7. Frequency Response of Analog ICs
8. Design Procedures of CMOS OP AMPs
9. Special-Purpose CMOS OP AMPs
10. Passive Components and MOS Switches
11. Bandgap References
12. Sample and Hold Circuits

Text Book:

Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, 2000

References:

1. David Johns and Ken Martin, Analog Integrated Circuit Design, John Wiley & Sons, 1997
2.Roubik Gregorian, Introduction to CMOS OP AMPs and Comparators, John Wiley & Sons, 1999

3. Roubik Gregorian and Gabor C. Temes, Analog MOS Integrated Circuits for Signal Processing, John Wiley & Sons, 1987
4. Technical Papers

Final Scores:

Will be determined by (1) Homework 20%
(2) Mid-Term Test 30%
(3) Final Exam 30%
(4) Chip Design Project 20% (This Semester)
20% (Next Semester)

Chip Design Schedule:

Presimulation Deadline: ：Dec. 4, 2000
Layout Deadline ：Dec. 25, 2000
Post-Simulation Deadline：Jan. 8, 2001
Tapeout :

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Chapter 1 Device Physics and SPICE Models of Analog MOSFETs

§1-1 Device Physics and Operational Principle

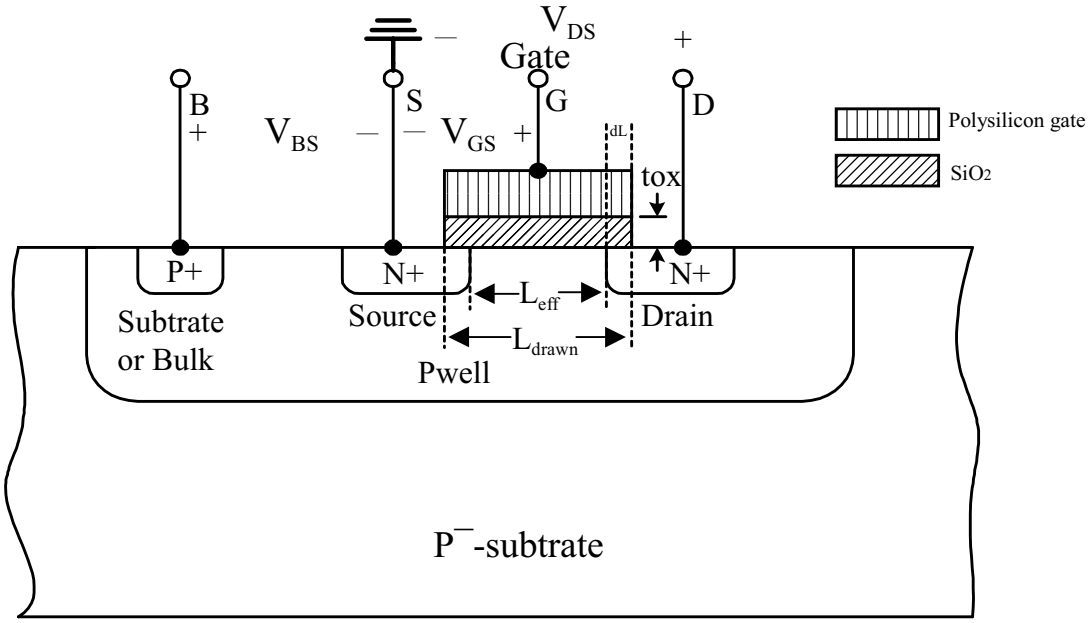


Fig.1 Cross-sectional view of a n-channel MOSFET.

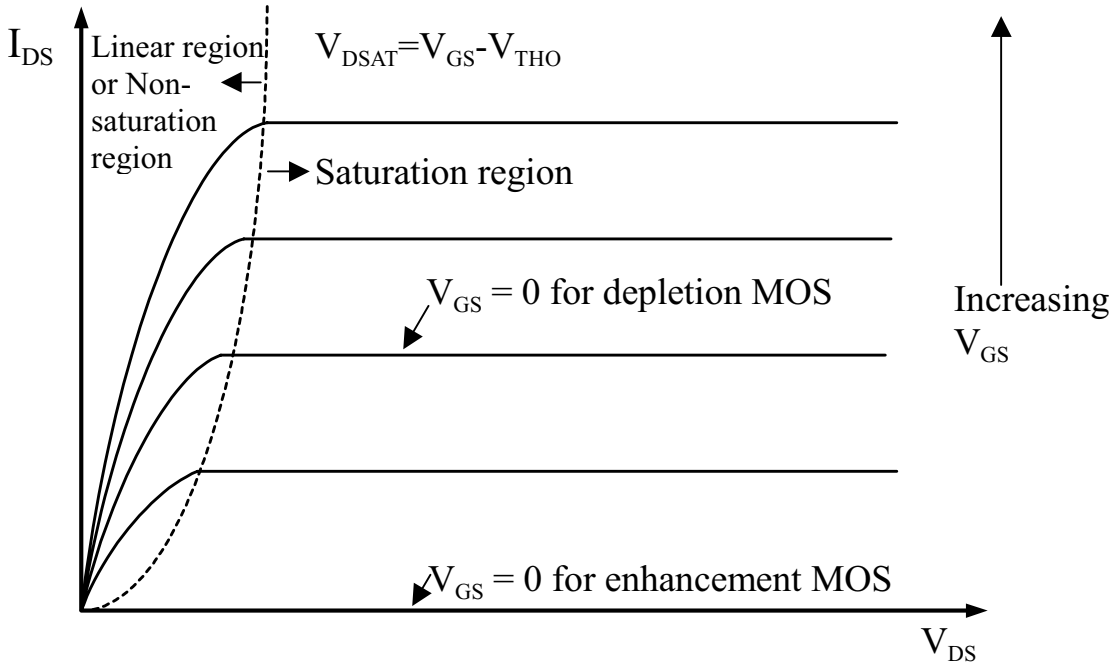
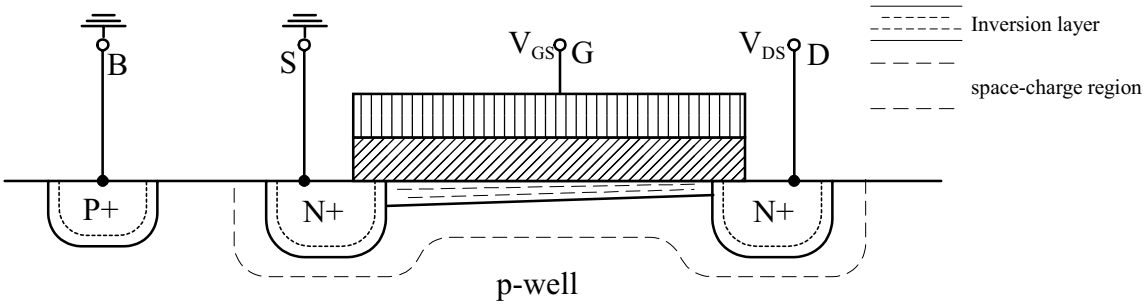


Fig.2 I_{DS}-V_{DS} characteristics of long-channel NMOSFET.

Linear Region (Non-saturation Region)：



$V_{GS} > V_{THO}$ (threshold voltage)

⇒ electron inversion layer (~200Å) is formed

⇒ For small V_{DS}, it likes an uniform resistor with length L_{eff}, width W_{eff}, and thickness 200 Å

⇒ Linear I_{DS}-V_{DS} curve

I_{DS} = (velocity along channel length) • (charges per unit channel length)

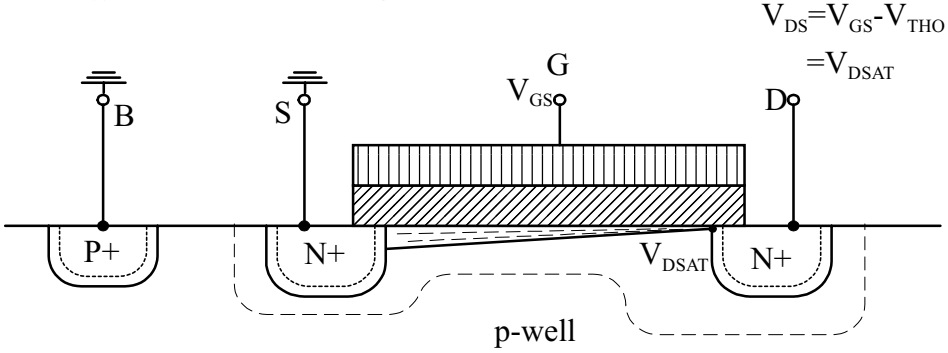
$$= (\mu \frac{V_{DS}}{L_{eff}})[C_{OX} W_{eff} (V_{GS} - V_{THO})] = \mu C_{OX} \frac{W_{eff}}{L_{eff}} (V_{GS} - V_{THO}) V_{DS}$$

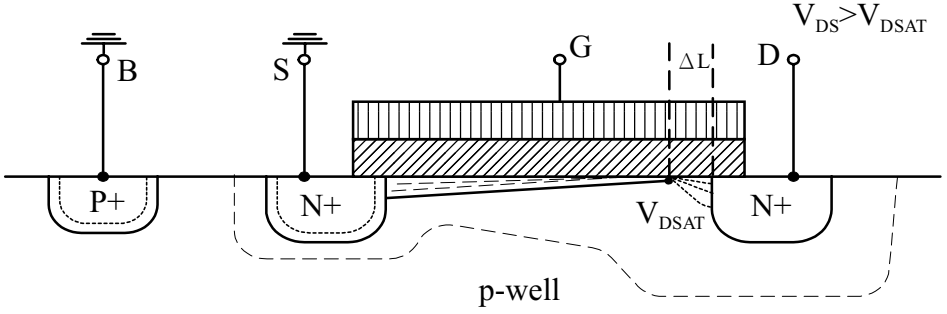
⇒ For slightly larger V_{DS},

$$I_{DS} = (\mu \frac{V_{DS}}{L_{eff}}) \left[C_{OX} W_{eff} (V_{GS} - V_{THO} - \frac{1}{2} V_{DS}) \right] = \mu C_{OX} \frac{W_{eff}}{L_{eff}} \left[(V_{GS} - V_{THO}) V_{DS} - \frac{1}{2} V_{DS}^{\ 2} \right]$$

Saturation Region：

1.Pinched-off saturation in long-channel devices





At $V_{DS} = V_{DSAT} = V_{GS}-V_{THO}$，the channel is pinched off ($V_{GD} = V_{THO}$).

$$I_{DS} = \frac{uC_{ox}}{2}\frac{W_{eff}}{L_{eff}}(V_{GS} - V_{THO})^2$$

When $V_{DS} > V_{DSAT}$，the pinched-off point of V_{DSAT} along the channel is moved toward the source with a distance ΔL from the drain.

$\Rightarrow$ Within ΔL，the electrons can be very quickly swept toward the drain region. Thus the current is not dependent upon the physical behavior of electrons within ΔL.

$$\Rightarrow \quad I_{DS} = \frac{\mu C_{ox}}{2}\frac{W_{eff}}{L_{eff} - \Delta L}(V_{GS} - V_{THO})^2$$

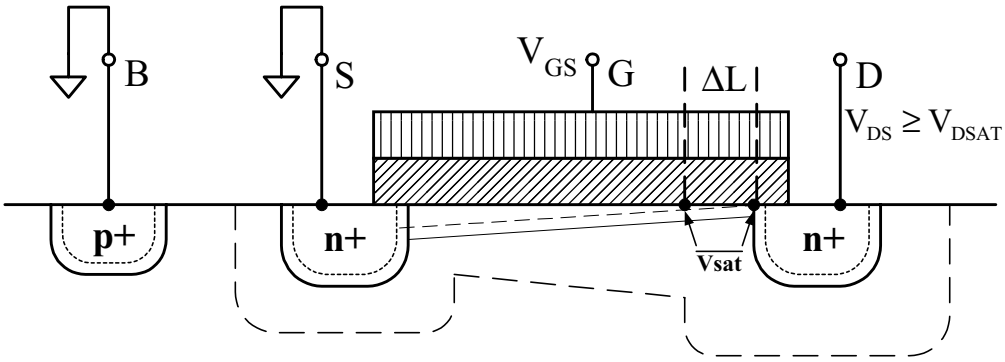
$$\cong \frac{\mu C_{ox}}{2}\frac{W_{eff}}{L_{eff}}(V_{GS} - V_{THO})^2$$

for $\Delta L << L$ (long-channel device)

$\Rightarrow$ constant current characteristics.

2. Velocity saturation in short-channel devices

In short-channel devices $L_{drawn} < 4\mu m$，velocity saturation occurs before pinched-off.



$$\bar{v}_{SAT} = \mu\frac{V_{DSAT}}{L_{eff}}$$

$$I_{DSAT} = \mu\frac{V_{DSAT}}{L_{eff}}[C_{ox}W_{eff}(V_{GS} - V_{THO} - \frac{1}{2}V_{DSAT})]$$

When $V_{DS} > V_{DSAT}$, the charges per unit channel length are increased by a factor of $\frac{L_{eff}}{L_{eff} - \Delta L}$ effectively.

$$I_{DS} = I_{DSAT} \frac{L_{eff}}{L_{eff} - \Delta L}, \quad V_{DS} \uparrow \Rightarrow \Delta L \uparrow \Rightarrow I_{DS} \uparrow$$

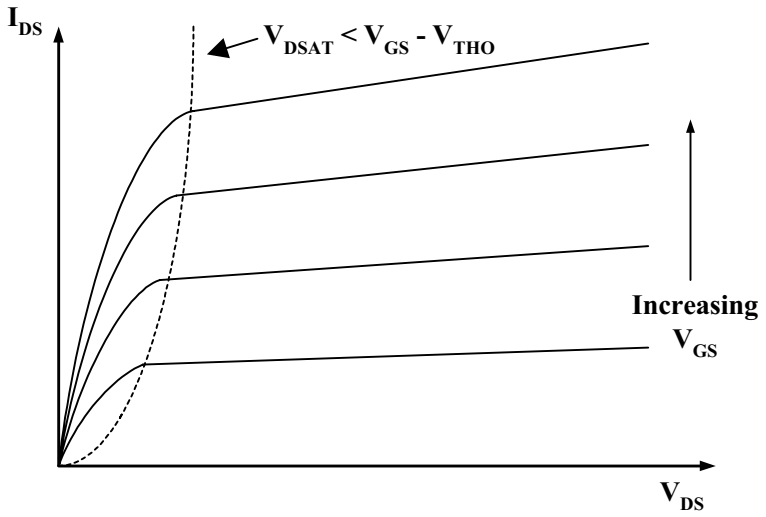
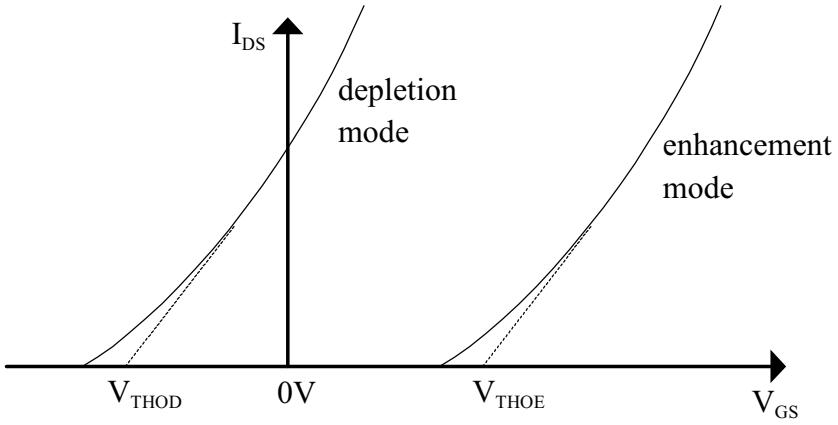


Fig. 3 I_{DS}-V_{DS} characteristics of short-channel NMOSFET

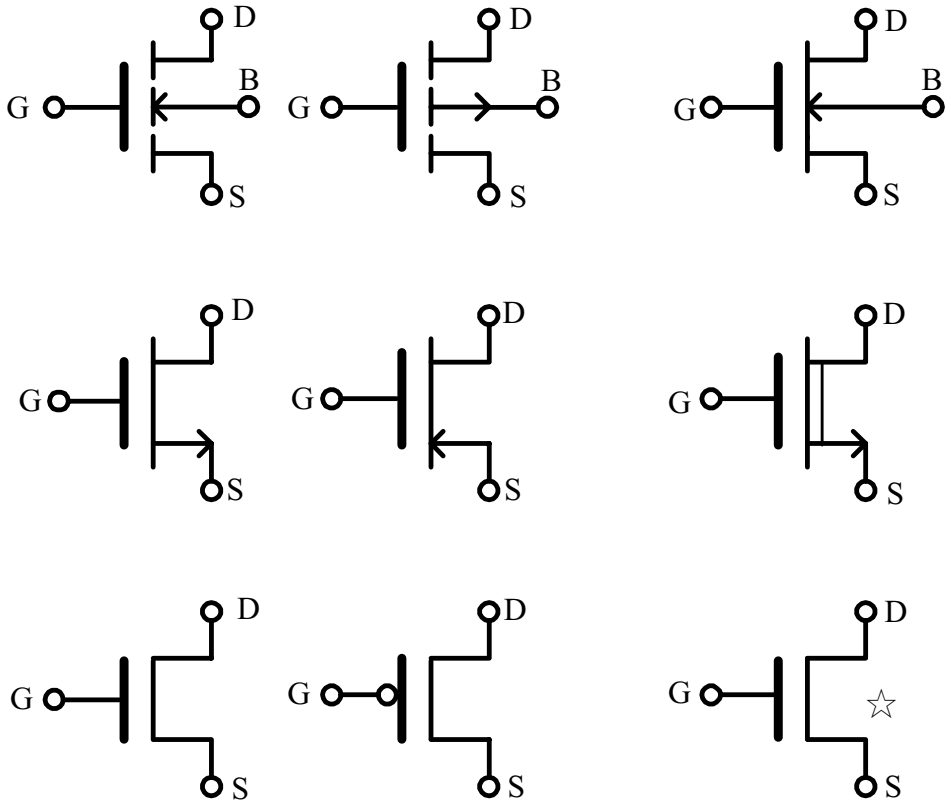
I_{DS}-V_{GS} characteristics：



Device symbols：

Enhancement-Mode MOSFET　　Depletion-Mode

n-channel　　p-channel　　n-channel



§1-1.1 Threshold Voltage V_{TH}

$$V_{TH}=\phi_{MS}-\frac{Q_{SS}}{C_{OX}}+\phi_S+\frac{Q_B}{C_{OX}}=V_{FB}+\phi_S+\frac{Q_B}{C_{OX}} \qquad V_{FB}\equiv\phi_{MS}-\frac{Q_{SS}}{C_{OX}} \qquad V_{TH}\overset{+NMOS}{:-PMOS}$$

ϕ_{MS} : gate material to silicon potential barrier

Q_{SS} : surface charge density (C/cm^2)

ϕ_S : surface potential under strong inversion

$$\phi_S=2\frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) \text{ or } 2\frac{kT}{q}\ln\left(\frac{n_i}{N_D}\right) \qquad \phi_S\overset{+NMOS}{:-PMOS}$$

Q_B : bulk charge density (C/m^2)　　$Q_B\overset{+NMOS}{:-PMOS}$

C_{OX} : channel oxide capacitance per unit area

$$C_{OX}=\frac{\varepsilon_{sio_2}}{T_{ox}} \qquad C_{OX}\cong 0.037 fF/\mu m^2 \text{ for } T_{OX}=100\,Å$$

Gate Material	Φ_{MS}(V)		$\frac{Q_{SS}}{C_{OX}}\left[\begin{matrix}N_D/N_A=5\times10^{14}\,cm^{-3}\\ t_{ox}=100\,\mathring{A}\end{matrix}\right]$	V_{FB}(V)	
	PMOS	NMOS	(V)	PMOS	NMOS
metal	−0.3	−0.85	−0.03	−0.33	−0.88
n^+_polysilicon	−0.25	−0.80	−0.023	−0.273	−0.823
p^+_polysilicon	+0.80	+0.30	−0.023	+0.777	+0.277

$Q_B=\sqrt{2\in_{si} qN_A\Phi_S}$ for $V_{BS}=0$，i.e. zero substrate bias
(N_D)

$Q_B=\sqrt{2\in_{si} qN_A(\Phi_S-V_{BS})}$ V_{BS}: ＋ forward bias
(N_D)

− reverse bias

$V_{TH}=V_{THO}+GAMMA\sqrt{\Phi_S}\left[\sqrt{1-V_{BS}/\Phi_S}-1\right]$ V_{THO}: zero-bias threshold voltage

$=V_{THO}+GAMMA\left[\sqrt{\Phi_S-V_{BS}}-\sqrt{\Phi_S}\right]$ $\in_{si}$:permitivity of Si

V_{TH} and V_{THO}: ＋(−) for enhancement NMOS (PMOS)

$GAMMA=\frac{1}{Cox}\sqrt{2\in_{si} qN_A}$ GAMMA：body effect factor

Body Effect，Substrate Bias Effect

：$|V_{BS}|\uparrow$ forward bias $\Rightarrow V_{TH}\downarrow$

$|V_{BS}|\uparrow$ reverse bias $\Rightarrow V_{TH}\uparrow$

$GAMMA\cong 0.1$ to 1.0 $GAMMA\ \alpha\sqrt{N_A}$

To obtain a large enough V_{THO} and a small GAMMA
$\Rightarrow$implantation for threshold voltage adjustment on a small N_A (N_D) sub.
enhancement implant & depletion implant.

§1-1.2 Level 49 BSIM3 Version3 SPICE MOS Model-Threshold Voltage

Ref：1.Star-Hspice Manual, Release 1998.2

2.BSIM3v3.2.2 Manual, http://www-device.eecs.berkeley.edu/~bsim3/get.html

Threshold Voltage Equation

$$V_{th} = V_{th0ox} + K_{1ox}\cdot\sqrt{\Phi_s - V_{bseff}} - K_{2ox}V_{bseff}$$
$$+ K_{1ox}\left(\sqrt{1+\frac{Nlx}{L_{eff}}}-1\right)\sqrt{\Phi_s} + \left(K_3 + K_{3b}V_{bseff}\right)\frac{Tox}{W_{eff}' + W_0}\Phi_s$$
$$- D_{VTOw}\left(exp\left(-D_{VT1w}\frac{W_{eff}'L_{eff}}{2l_{tw}}\right)+2exp\left(-D_{VT1w}\frac{W_{eff}'L_{eff}}{l_{tw}}\right)\right)\left(V_{bi}-\Phi_s\right)$$
$$- D_{VTO}\left(exp\left(-D_{VT1}\frac{L_{eff}}{2l_t}\right)+2exp\left(-D_{VT1}\frac{L_{eff}}{l_t}\right)\right)\left(V_{bi}-\Phi_s\right)$$
$$-\left(exp\left(-D_{sub}\frac{L_{eff}}{2l_{to}}\right)+2exp\left(-D_{sub}\frac{L_{eff}}{l_{to}}\right)\right)\left(E_{tao}+E_{tab}V_{bseff}\right)V_{ds}$$

$$V_{th0ox} = V_{th0} - K_1\cdot\sqrt{\Phi_s}$$

$$K_{1ox} = K_1\cdot\frac{T_{ox}}{T_{oxm}}$$

$$K_{2ox} = K_2\cdot\frac{T_{ox}}{T_{oxm}}$$

$$l_{t0} = \sqrt{\varepsilon_{si}X_{dep0}/C_{ox}}$$

$$l_t = \sqrt{\varepsilon_{si}X_{dep}/C_{ox}}\left(1+D_{VT2}V_{bseff}\right)$$

$$l_{tw} = \sqrt{\varepsilon_{si}X_{dep}/C_{ox}}\left(1+D_{VT2w}V_{bseff}\right)$$

$$X_{dep} = \sqrt{\frac{2\varepsilon_{si}\left(\Phi_s - V_{bseff}\right)}{qN_{ch}}}$$

$$X_{dep0} = \sqrt{\frac{2\varepsilon_{si}\Phi_s}{qN_{ch}}}$$

$$V_{bseff} = V_{bc} + 0.5\left[V_{bs} - V_{bc} - \delta_1 + \sqrt{\left(V_{bs}-V_{bc}-\delta_1\right)^2 - 4\delta_1 V_{bc}}\right]\quad \delta_1=0.001\text{V}$$

$$V_{bc} = 0.9\left(\Phi_s - \frac{K_1^2}{4K_2^2}\right)$$

$$V_{bi} = v_t\ln\left(\frac{N_{ch}N_{DS}}{n_i^{\,2}}\right)$$

N_{DS}=1e20/cm^3

where Toxm is the gate oxide thickness at which parameters are extrated with a default value of Tox.

Threshold Voltage Model Parameters：

Name	Units	Default	Comments
TOX	m	150e-10	Gate oxide thichness
VTHO	V	0.7	Threshold voltage of long channel device at V_{bs}=0 and small V_{ds}(typically 0.7 for n-channel, -0.7 for p-channel)
NSUB	cm^{-3}	6.0e16	Substrate doping concentration
NCH	cm^{-3}	1.7e17	Peak doping concentration near interface
NLX	m	1.74e17	Lateral nonuniform doping along channel
K1	V$^{1/2}$	0.50	First-order body effect coefficient
K2	-	-0.0186	Second-order body effect coefficient
K3	-	80.0	Narrow width effect coefficient
K3B	1/V	0	Body width coefficient of narrow width effect
W0	M	2.5e-6	Narrow width effect coefficient
DVT0W	1/m	0	Narrow width coefficient 0, for Vth, at small L
DVT1W	1/m	5.3e6	Narrow width coefficient 1, for Vth, at small L
DVT2W	1/V	-0.032	Narrow width coefficient 2, for Vth, at small L
DVT0	-	2.2	Short channel effect coefficient 0, for Vth
DVT1	-	0.53	Short channel effect coefficient 1, for Vth
DVT2	1/V	-0.032	Short channel effect coefficient 2, for Vth
ETA0	-	0.08	Subthreshold region DIBL (Drain Induced Barrier Lowering)coefficient
ETAB	1/V	-0.07	Subthreshold region DIBL coefficient
DSUB	-	DROUT	DIBL coefficient exponent in subthreshold region
VBM	V	-3.0	Maximum substrate bias, for Vth calculation

Other related model parameters: 13 parameter of L_{eff} , W_{eff} , and W_{eff}'

Effects on Threshold Voltage

1 Short-Channel effect

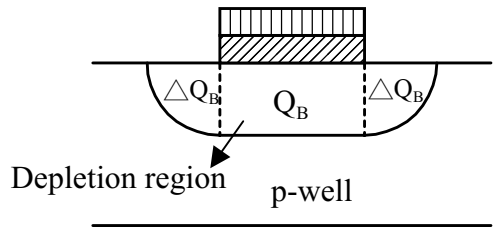
L_{drawn} ↓ =>V_{th} ↓ ∵effective Q_B ↓ shared by source-drain junction depletion changes

HSPICE Model Parameters:DVT0,DVT1,DVT2

2 Narrow-Channel effect

W_{drawn} ↓ =>V_{th} ↑

∵effective Q_B ↑ by △Q_B caused by the fringing electric field

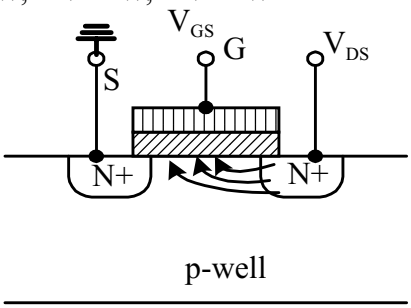


HSPICE Model Parameters:K3, K3B, W0, DVT0W, DVT1W, DVT2W

3 DIBL (Drain-Induced Barrier Lowering) effect

$V_{DS}\uparrow$ =>electrons in the channel can be induced by the positive voltage at the drain as that at the gate

=> $V_{th}\downarrow$



HSPICE Model Parameters: ETA0, ETAB, DSUB

4 Body effect

HSPICE Model Parameters: NLX, K1, K2, VBM

§ 1-1.3 First-Order MOS I_{DS}-V_{DS} Equations

Linear , non-saturation , or triode region ($V_{DS} < V_{DSAT}$, $V_{GS} > V_{TH}$)

$$I_{DS} = \frac{\mu_n C_{ox}}{2}\frac{W_{eff}}{L_{eff}}\left[2V_{DS}(V_{GS}-V_{TH})-V_{DS}^{\ 2}\right]$$

μ_n : electron surface mobility

$$L_{eff} = L_{drawn} - 2dL$$

$$W_{eff} = W_{drawn} - 2dW$$

$$V_{TH} = V_{THO} - \gamma\left(\sqrt{\Phi_S - V_{BS}} - \sqrt{\Phi_S}\right)$$

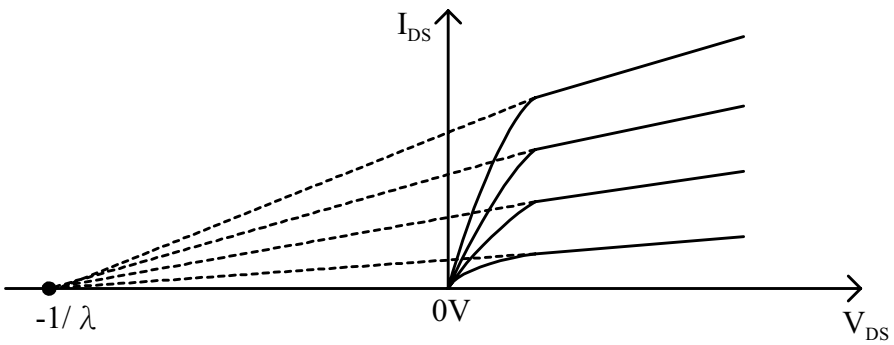
Saturation region ($V_{DS} > V_{DSAT}$, $V_{GS} > V_{TH}$)

$$I_{DS} = \frac{\mu_n C_{ox}}{2}\frac{W_{eff}}{L_{eff}}(V_{GS}-V_{TH})^2(1+\lambda V_{DS})$$

λ : effective Early-Effect factor

$$\frac{1}{10}V^{-1} \text{or} \frac{1}{100}V^{-1}$$

$$\lambda \approx \sqrt{\frac{2\varepsilon_{si}}{qN_{SUB}}}\frac{1}{2L\sqrt{V_{DS}-V_{DSAT}}}$$



Saturation region or weak inversion region： ($V_{TH} - V_{off} < V_{GS} < V_{TH}$)

$$I_{DS} \cong I_{so} \exp(V_{GS} / n\nu_t)[1 - \exp(-V_{DS} / \nu_t)]$$

$$I_{so} = \mu_0 \frac{W_{eff}}{L_{eff}} \sqrt{\frac{q\varepsilon_{si} N_{ch}}{2\Phi_S}} \nu_t^2$$

$$n \cong 1 + \frac{C_d}{C_{ox}} = 1 + \frac{1}{C_{ox}} \sqrt{\frac{qN_{sub}\varepsilon_{si}}{2(\Phi_S - V_{BS})}}$$

1-1.4 Level 49 BSIM3 Version 3 SPICE MOS Model – I_{DS}-V_{DS} Equation

1. Effective (V_{GS}-V_{TH})=V_{GST}

$$V_{gsteff} = \frac{2nv_t ln\left[1 + exp\left(\frac{V_{gs} - V_{th}}{2nv_t}\right)\right]}{1 + 2nC_{ox}\sqrt{\frac{2\Phi_s}{q\varepsilon_{si} N_{ch}}} exp\left(-\frac{V_{gs} - V_{th} - 2V_{off}}{2nv_t}\right)}$$

$$n = 1 + N_{factor}\frac{C_d}{C_{ox}} + \frac{\left(C_{cds} + C_{dscd}V_{ds} + C_{dscb}V_{bseff}\right)\left[exp\left(-D_{VT1}\frac{L_{eff}}{2l_t}\right) + 2exp\left(-D_{VT1}\frac{L_{eff}}{l_t}\right)\right]}{C_{ox}} + \frac{C_{it}}{C_{ox}}$$

$$C_d = \frac{\varepsilon_{si}}{X_{dep}}$$

Effective $(V_{GS} - V_{TH})$ Model Parameters

Name	**Units**	**Default**	**Comments**
VOFF	V	-0.08	Offset voltage in subthreshold region
NFACTOR	-	1.0	Subthreshold region swing
CIT	F/m^2	0.0	Interface state capacitance
CDSC	F/m^2	2.4e-4	Drain/source and channel coupling capacitance
CDSCD	F/Vm^2	0	Drain bias sensitivity of CDSC
CDSCB	F/Vm^2	0	Body coefficient for CDSC

Other related model parameters：20 parameters of V_{th} , and 13 parameters of L_{eff} , W_{eff} , and W_{eff}'

2. Mobility

For mobMod=1 (Default)

$$\mu_{eff} = \frac{\mu_o}{1 + \left(U_a + U_c V_{bseff}\right)\left(\frac{V_{gsteff} + 2V_{th}}{Tox}\right) + U_b\left(\frac{V_{gsteff} + 2V_{th}}{Tox}\right)^2}$$

Mobility Model Parameters

Name	Units	Default	Comments
U0	$cm^2/V/sec$	670 nmos 250nmos	Low field mobility at T=*TREF=TNOM*
UA	m/V	2.25e-9	First-order mobility degradation coefficient
UB	m^2/V^2	5.87e-19	Second-order mobility degradation coefficient
UC	1/V	-4.65e-11 or –0.0465	Body bias sensitivity coefficient of mobility -4.65e-11 for MOBMOD=1,2 or, -0.0465 for MOBMOD=3

Other related model parameters：20 parameters of V_{th} , 6 parameters of V_{gsteff} , and 13 parameters of L_{eff} , W_{eff} , and W_{eff}'

3.Drain Saturation Voltage

For $R_{ds} > 0$ or $\lambda \neq 1$;

$$V_{dsat} = \frac{-b - \sqrt{b^2 - 4ac}}{2a}$$

$$a = A_{bulk}{}^2 W_{eff} v_{sat} C_{ox} R_{DS} + \left(\frac{1}{\lambda} - 1\right) A_{bulk}$$

$$b = -\left[\left(V_{gsteff} + 2v_t\right)\left(\frac{2}{\lambda} - 1\right) + A_{bulk} E_{sat} L_{eff} + 3A_{bulk}\left(V_{gsteff} + 2v_t\right) W_{eff} v_{sat} C_{ox} R_{DS}\right]$$

$$c = \left(V_{gsteff} + 2v_t\right) E_{sat} L_{eff} + 2\left(V_{gsteff} + 2v_t\right)^2 W_{eff} v_{sat} C_{ox} R_{DS}$$

$$\lambda = A_1 V_{gsteff} + A_2$$

For $R_{DS} = 0$ and $\lambda = 1$

$$V_{dsat} = \frac{E_{sat} L_{eff}\left(V_{gsteff} + 2v_t\right)}{A_{bulk} E_{sat} L_{eff} + \left(V_{gsteff} + 2v_t\right)}$$

$$A_{bulk} = \left[1 + \frac{K_{lox}}{2\sqrt{\Phi_s - V_{bseff}}}\left[\frac{A_0 L_{eff}}{L_{eff} + 2\sqrt{X_J X_{dep}}}\left[1 - A_{gs} V_{gsteff}\left[\frac{L_{eff}}{L_{eff} + 2\sqrt{X_J X_{dep}}}\right]^2\right] + \frac{B_0}{W_{eff}'}\right]\right] \cdot \frac{1}{1 + KetaV_{bseff}}$$

$$E_{sat} = \frac{2V_{sat}}{\mu_{eff}}$$

Drain Saturation Voltage Model Parameters

Name	Units	Default	Comments
A0	-	1.0	Bulk charge effect coefficient for channel length
AGS	1/V	0.0	Gate bias coefficient of Abulk
B0	m	0.0	Bulk charge effect coefficient for channel
B1	m	0.0	Bulk charge effect width offset
KETA	1/V	-0.047	Body-bias coefficient of bulk charge effect
VSAT	msec	8e4	Saturation velocity of carrier at T=*TREF=TNOM*
A1	1/V	0	First nonsaturation factor
A2	-	1.0	Second nonsaturation factor
XJ	m	0.15e-6	Junction depth

Other related model parameters：20 V_{th} , 6V_{gsteff} , 13 L_{eff} , W_{eff} , and W_{eff}' , and 4R_{DS}

4.Effective V_{DS}

$$V_{dseff} = V_{dsat} - \frac{1}{2}\left(V_{dsat} - V_{ds} - \delta + \sqrt{(V_{dsat} - V_{ds} - \delta)^2 + 4\delta V_{dsat}} \right)$$

Effective V_{DS} Model Parameter

Name	Units	Default	Comments
DELTA	V	0.01	Effective Vds parameter

Other related model parameters：9V_{sat} , 20 V_{th} , 6V_{gsteff} , 13 L_{eff} , W_{eff} , and W_{eff}' , and 4R_{DS}

5.Drain Current Expression

$$I_{ds} = \frac{I_{dso(V_{dseff})}}{1 + \dfrac{R_{ds} I_{dso(V_{dseff})}}{V_{dseff}}} \left(1 + \frac{V_{ds} - V_{dseff}}{V_A} \right) \left(1 + \frac{V_{ds} - V_{dseff}}{V_{ASCBE}} \right)$$

$$I_{dso} = \frac{W_{eff} \mu_{eff} C_{ox} V_{gsteff} \left(1 - A_{bulk} \dfrac{V_{dseff}}{2(V_{gsteff} + 2v_t)} \right) V_{dseff}}{L_{eff} \left[1 + V_{dseff} / (E_{sat} L_{eff}) \right]}$$

$$V_A = V_{Asat} + \left(1 + \frac{P_{vag} V_{gsteff}}{E_{sat} L_{eff}} \right) \left(\frac{1}{V_{ACLM}} + \frac{1}{V_{ADIBLC}} \right)^{-1}$$

$$V_{ACLM} = \frac{A_{bulk} E_{sat} L_{eff} + V_{gsteff}}{P_{CLM} A_{bulk} E_{sat} litl} (V_{ds} - V_{dseff})$$

$$V_{ADIBLC} = \frac{(V_{gsteff} + 2v_t)}{\theta_{rout} (1 + P_{DIBLCB} V_{bseff})} \left(1 - \frac{A_{bulk} V_{dsat}}{A_{bulk} V_{dsat} + V_{gsteff} + 2v_t} \right)$$

$$\theta_{rout} = P_{DIBLC1} \left[\exp\left(-D_{ROUT} \frac{L_{eff}}{2 l_{t0}} \right) + 2 \exp\left(-D_{ROUT} \frac{L_{eff}}{l_{t0}} \right) \right] + P_{DIBLC2}$$

$$\frac{1}{V_{ASCBE}} = \frac{P_{scbe2}}{L_{eff}} \exp\left(\frac{-P_{scbe1} litl}{V_{ds} - V_{dseff}} \right)$$

$$V_{Asat} = \frac{E_{sat}L_{eff} + V_{dsat} + 2R_{DS}\nu_{sat}C_{ox}W_{eff}V_{gsteff}\left[1 - \frac{A_{bulk}V_{dsat}}{2\left(V_{gsteff} + 2\nu_t\right)}\right]}{2/\lambda - 1 + R_{DS}\nu_{sat}C_{ox}W_{eff}A_{bulk}}$$

$$litl = \sqrt{\frac{\varepsilon_{si}T_{ox}X_j}{\varepsilon_{ox}}}$$

Name	Units	Default	Comments
PCLM	-	1.3	Coefficient of channel length modulation values≦0 will result in an error message and program exit
PDIBLC1	-	0.39	DIBL (Drain Induced Barrier Lowering) Effect cofficient 1
PDIBLC2	-	0.0086	DIBL effect coefficient 2
PDIBLCB	1/V	0	Body effect coefficient of DIBL effect coefficients
DROUT	-	0.56	Length dependence coefficient of the DIBL Correction parameter in Rout
PVAG	-	0	Gate dependence of Early voltage

Other related model parameters：1V_{dseff}, 9V_{sat}, 20 V_{th}, 6V_{gsteff}, 13 L_{eff}, W_{eff}, and W_{eff}', and 4R_{DS}

6.Substrate Current

$$I_{sub} = \alpha_0(V_{ds} - V_{dseff})\exp\left(-\frac{\beta_0}{V_{ds} - V_{dseff}}\right)\frac{I_{ds0}}{1 + \frac{R_{ds}I_{ds0}}{V_{dseff}}}\left(1 + \frac{V_{ds} - V_{dseff}}{V_A}\right)$$

Substrate Current Model Parameters

Name	Units	Default	Comments
ALPHA0	m/V	0	The first parameter of impact ionization current
BETA0	V	30	The second parameter of impact ionization current

Other related model parameters：1V_{dseff}, 9V_{sat}, 20 V_{th}, 6V_{gsteff}, 13 L_{eff}, W_{eff}, and W_{eff}', and 4R_{DS}

7.Subthreshold Drain Current

$$I_{ds} = I_{so}(1 - \exp(-\frac{V_{ds}}{\nu_t}))\exp(\frac{V_{gsteff} + |V_{off}|}{n\nu_t})$$

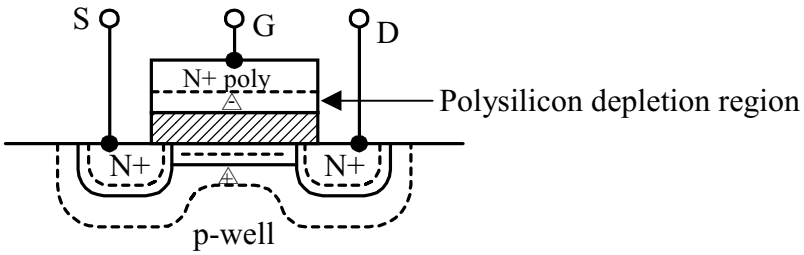
$$I_{so} = \mu_0\frac{W_{eff}}{L_{eff}}\sqrt{\frac{q\varepsilon_{si}N_{ch}}{2\Phi_s}}\,\nu_t^{\,2}$$

where V_{off} is the offset voltage which is an important parameters determining the drain current at V_{gs}=0.

Related model parameters

VOFF, NFACTOR, CIT, CDSC, CDSCB, CDSCD, ETAO, ETAB, DSUB.

8. Polysilicon Depletion Effect



$$V_{poly}=\frac{1}{2}X_{poly}E_{poly}=\frac{qN_{gate}X^2_{poly}}{2\varepsilon_{si}}$$

$$\varepsilon_{ox}E_{ox}=\varepsilon_{si}E_{poly}=\sqrt{2q\varepsilon_{si}N_{gate}V_{poly}}$$

$$V_{gs}-V_{FB}-\Phi_s=V_{poly}+V_{ox}$$

$$a(V_{gs}-V_{FB}-\Phi_s-V_{poly})^2-V_{poly}=0$$

$$a=\frac{\varepsilon_{ox}^2}{2q\varepsilon_{si}N_{gate}T_{ox}^2}$$

$$V_{gs\_eff}=V_{FB}+\Phi_s+\frac{2q\varepsilon_{si}N_{gate}T_{ox}^2}{\varepsilon_{ox}^2}\left(\sqrt{1+\frac{2\varepsilon_{ox}^2(V_{gs}-V_{FB}-\Phi_s)}{q\varepsilon_{si}N_{gate}T_{ox}^2}}-1\right)$$

Polysilicon Depletion Effect Model Parameters

Name	Units	Default	Comments
NGATE	cm^{-3}	infinite	Poly gate doping concentration

9. Effective Channel Length and Width

$$L_{eff}=L_{drawn}-2dL$$

$$W_{eff}=W_{drawn}-2dw$$

$$W'_{eff}=W_{draw}-2dW'$$

$$dW=dW'+dW_gV_{gsteff}+dW_b\left(\sqrt{\Phi_S-V_{bseff}}-\sqrt{\Phi_S}\right)$$

$$dW'=W_{int}+\frac{W_l}{L^{Wln}}+\frac{W_w}{W^{Lwn}}+\frac{W_{wl}}{L^{Wln}W^{Lwn}}$$

$$L_{eff}=L_{drawn}-2dL$$

$$dL=L_{int}+\frac{L_l}{L^{Lln}}+\frac{L_w}{W^{Lwn}}+\frac{L_{wl}}{L^{Lln}W^{Lwn}}$$

Effective Channel Length and Width Model Parameters

Name	Units	Default	Comments
WINT	m	0.0	Width offset fitting parameter from I-V without bias
WLN	-	1.0	Power of length dependence of width offset
WW	m^{WWN}	0.0	Coefficient of width dependence fo width

			offset
WWN	-	1.0	Power of width dependence of width offset
WWL	m^{WWN} $*m^{WWN}$	0.0	Coefficient of length and width cross term for width offset
DWG	m/V	0.0	Coefficient of Weff's gate dependence
DWB	$M/V^{1/2}$	0.0	Coefficient of Weff's substrate body bias dependence
LINT	m	0.0	Length offset fitting parameter from I-V Without bias
LL	m^{LLN}	0.0	Coefficient of length dependence for length offset
LLN	-	1.0	Power of length dependence of length offset
LW	m^{LWN}	0.0	coefficient of width dependence for length offset
LWN	-	1.0	Power of width dependence of length offset
LWL	m^{LWN} $*m^{LLN}$	0.0	Coefficient of length and width cross term for length offset

Other related model parameters：$6V_{gsteff}$ and $20V_{th}$

10.Source/Drain Resistance

$$R_{dr} = \frac{R_{dsw}\left(1 + P_{rwg}V_{gsteff} + P_{rwb}\left(\sqrt{\Phi_s - V_{bseff}} - \sqrt{\Phi_s}\right)\right)}{\left(10^6 W_{eff}'\right)^{W_r}}$$

Source/Drain Resistance Model Parameters

Name	**Units**	**Default**	**Comments**
RDSW	ohm・μm	0.0	Parasitic source drain resistance per unit width
PRWG	1/V	0	Gate bias effect coefficient of RDSW
PRWB	$1/V^{1/2}$	0	Body effect coefficient of RDSW
WR	-	1.0	Width offset from Weff for Rds calculation

11.Temperature Effects

$$V_{th(T)} = V_{th(Tnorm)} + (K_{T1} + K_{1U}/L_{eff} + K_{T2}V_{bseff})(T/T_{norm} - 1)$$

$$\mu_{a(T)} = \mu_{a(Tnorm)}\left(\frac{T}{T_{norm}}\right)^{\mu_{te}}$$

$$v_{sat(T)} = v_{sat(Tnorm)} - A_T(T/T_{norm} - 1)$$

$$R_{dsw(T)} = R_{dsw(T_{norm})} + P_{T}\left(\frac{T}{T_{norm}} - 1\right)$$

$$U_{a(T)} = U_{a(Tnorm)} + U_{a1}(T/T_{norm} - 1)$$

$$U_{b(T)} = U_{b(Tnorm)} + U_{b1}(T/T_{norm} - 1)$$

$$U_{c(T)} = U_{c(Tnorm)} + U_{c1}(T/T_{norm} - 1)$$

Temperature Effects Model Parameters

Name	Units	Default	Comments
KT1	V	0.0	Temperature coefficient for Vth
KT1L	m-V	0.0	Temperature coef. for channel length dependence of Vth
KT2	-	0.022	Body bias coefficient of Vth temperature effect
UTE	-	-1.5	Mobility temperature exponent
UA1	m/V	4.31e-9	Temperature coefficient for UA
UB1	$(m/V)^2$	-7.61e-18	Temperature coefficient for UB
UC1	m/V^2	-5.69e-11	Temperature coefficient for UC
AT	m/sec	3.3e4	Temperature coefficient for saturation velocity
PRT	ohm-um	0	Temperature coefficient for RDSW

1-1.5 Level 49 BSIM3 Version 3 SPICE MOS Model-MOS Diode Equations

1. I-V model of S/B diode

ijth $\neq 0$

If $V_{bs} < V_{jsm}$

$$I_{bs} = I_{sbs}\left[\exp\left(\frac{V_{bs}}{Nv_t}\right)-1\right]+G_{min}V_{bs}$$

otherwise

$$I_{bs} = ijth + \frac{ijth + I_{sbs}}{NV_t}\left(V_{bs} - V_{jsm}\right)+G_{min}V_{bs}$$

$$V_{jsm} = NV_t \ln\left(\frac{ijth}{I_{sbs}}+1\right)$$

$$I_{sbs} = A_{S_{eff}}J_S + P_{S_{eff}}J_{SW}$$

$$A_{S_{eff}} = 2\cdot HDIF\cdot SCALM\cdot WMLT\cdot W_{eff}$$ (As is not specified)

$$A_{S_{eff}} = M\cdot A_S\cdot WMLT^2\cdot SCALE^2$$ (As is specified)

$$P_{S_{eff}} = 4\cdot HDIF\cdot SCALM\cdot WMLT$$ (Ps is not specified)

$$P_{S_{eff}} = M\cdot Ps\cdot SCALE\cdot WMLT$$

$A_{S_{eff}}$ ：effective source junction area

$P_{S_{eff}}$ ：effective source junction perimeter

SCALE（SCALM）：scaling for element (model) statement parameters

Temperature effect

$$J_S(T) = J_S(T_{nom}) \exp\left[\frac{\frac{E_{go}}{v_{t0}} - \frac{E_g}{v_t} + XTI \cdot \ln\left(\frac{T}{T_{nom}}\right)}{N}\right]$$

$$J_{SW}(T) = J_{SW}(T_{nom}) \exp\left[\frac{\frac{E_{go}}{v_{t0}} - \frac{E_g}{v_t} + XTI \cdot \ln\left(\frac{T}{T_{nom}}\right)}{N}\right]$$

$$E_{go} = 1.16 - \frac{7.02 \times 10^{-4} T_{nom}{}^2}{T_{nom} + 1108}$$

$$E_g = 1.16 - \frac{7.02 \times 10^{-4} T^2}{T + 1108}$$

2. I-V model of D/B diode

$V_{bs} \rightarrow V_{bd}$

$V_{jsm} \rightarrow V_{jdm}$

$I_{sbs} \rightarrow I_{sbd}$

$A_{seff} \rightarrow A_{deff}$

$P_{seff} \rightarrow P_{deff}$

MOS Diode I-V model parameters

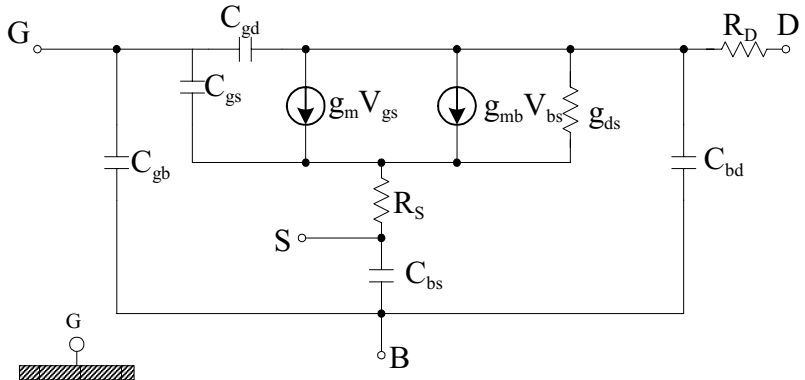
Name	**Units**	**Default**	**Comments**
JS	A/m^2	0.0	Bulk junction saturation current (Default deviates from BSIM3v3=$1.0e^{-4}$)
JSW	A/m	0.0	Sidewall bulk junction saturation current
NJ	-	1	Emission coefficient (not used with ACM=3)
XTI	-	3.0	Junction current temperature exponent

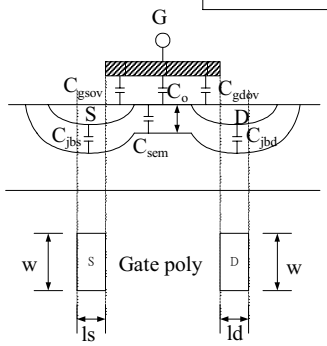
MOS Geometry Model Parameters

Name	**Unit**	**Default**	**Description**
HDIF	m	0	Length of heavily doped diffusion, from contact to lightly doped region(ACM=2,3 only)

LD	m		Lateral diffusion into channel from source and drain diffusion. If LD and XJ are unspecified, LD default=0.0. When LD is unspecified, but XJ is specified, LD is calculated from XJ. LD default=0.75 · XJ. For Level 4 only, lateral diffusion is derived form LD · XJ. LDscaled=LD · SCALM
LDIF	m	0	Length of lightly doped diffusion adjacent to gate(ACM=1,2) LDIFscaled=LDIF · SCALM
WMLT		1	Width diffusion layer shrink reduction factor

§ 1-2 Small-Signal Model of MOSFETs





$A_S = W \cdot ls$ bottom plate source junction area

$A_D = W \cdot ld$ bottom plate drain junction area

$P_S = 2(W+ls)$ perimeter of source juncion

$P_D = 2(W+ld)$ perimeter of drain junction

$$C_{gsov}(C_{gdov})\left[\cong C_o L_D\right] = CGSO(CGDO)$$

$$C_{jbs} = C_j A_s \frac{1}{\left(1-\frac{V_{BS}}{P_B}\right)^{MJ}} + C_{jsw} P_s \frac{1}{\left(1-\frac{V_{BS}}{P_B}\right)^{MJSW}}$$

for C_{jbd}, $V_{BS} \to V_{BD}$
$A_S \to A_D$
$P_S \to P_D$

V_{BS}: $+$ forward bias; $-$ reverse bias

$$C_{sem} = \varepsilon_{si}/x_d = \varepsilon_{si}\Big/\sqrt{2\varepsilon_{si}(\varphi_s - V_{BS})/qN_A}$$
(N_D)

$$g_m \equiv \frac{\partial I_{DS}}{\partial V_{GS}} = 2\sqrt{I_{DS}\frac{\mu_n C_o}{2}\frac{W}{L}} \quad (\text{sat. region})$$

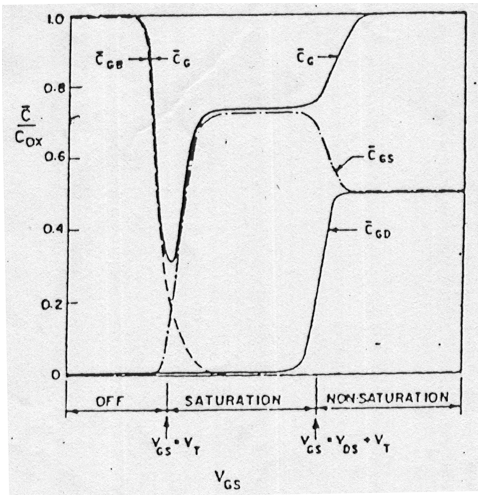
$$g_{mb} \equiv \frac{\partial I_{DS}}{\partial V_{BS}} \cong \frac{GAMMA\ g_m}{2\sqrt{\Phi_s - V_{BS}}} = g_m \eta \quad (\text{sat. region})$$

where $\eta = \dfrac{GAMMA}{2\sqrt{\Phi_s - V_{BS}}}$

$$\frac{1}{r_{ds}} = g_{ds} = \frac{\partial I_{DS}}{\partial V_{DS}} \cong \lambda I_D \quad (\text{sat.}) \qquad R_D, R_S: \text{drain/source resistance}$$

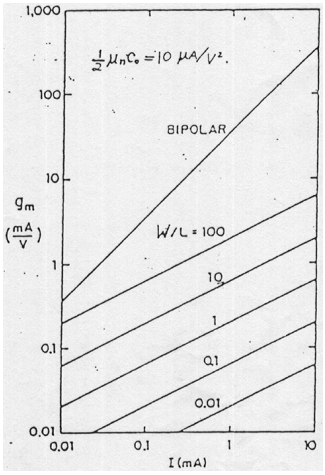
	OFF	LINEAR	SATURATION
C_{gs}	$C_{gsov}W$	$WC_{gsov} + \frac{1}{2}C_oWL$	$WC_{gsov} + \frac{2}{3}C_oWL$
C_{gd}	$C_{gdov}W$	$WC_{gdov} + \frac{1}{2}C_oWL$	WC_{gdov}
C_{gb}	$0.9C_oWL$	0	$0.1C_oWL$
C_{bs}	C_{jbs}	$C_{jbs} + \frac{1}{2}C_{sem}WL$	$C_{jbs} + \frac{2}{3}C_{sem}WL$
C_{bd}	C_{jbd}	$C_{jbd} + \frac{1}{2}C_{sem}WL$	C_{jbd}

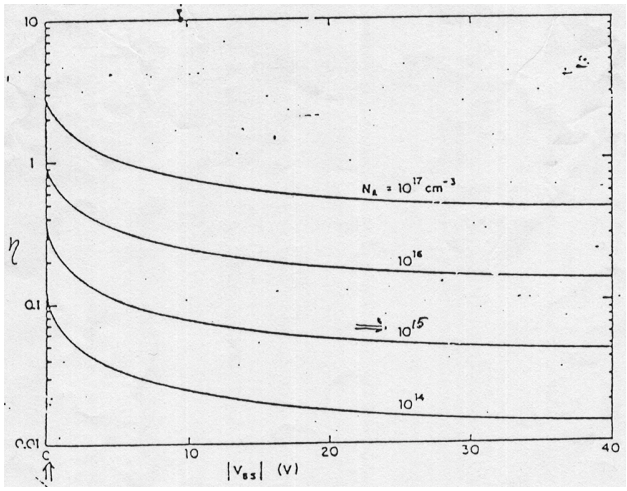
Exact calculation of C_{gs}, C_{gd} and C_{gb} :



Typical device
Transconductance (gm)
versus drain current (I_D)

gm for BJT > gm for MOS





Parameter $\eta \equiv \frac{\text{GAMMA}}{2\sqrt{\Phi_s - V_{BS}}}$ versus $|V_{BS}|$

✧ In this figure, $|V_{BS}| = 0\ V$ does not mean short-circuited substrate and source!

Junction Capacitance Model Parameters

Name	Units	Default	Comments
ACM	-	0	Area calculation method selector (Start-Hspice specific)
CJ	F/m^2	$5.79e^{-4}$	zero-bias bulk junction capacitance (Default deviates from BSIM3v3 = $5.0e^{-4}$)
CJSW	F/m	0.0	zero-bias sidewall bulk junction capacitance (Default deviates from BSIM3v3 = $5.0e^{-10}$)

CJSWG	F/m	CJSW	zero-bias gate-edge sidewall bulk junction capacitance (not used with ACM=0-3)
PB	V	1.0	bulk junction contact potential
PBSW	V	1.0	sidewall bulk junction contact potential
MJ	-	0.5	bulk junction grading coefficient
MJSW	-	0.33	sidewall bulk junction grading coefficient
PHP	V	PB	bulk sidewall junction contact potential

Note that ACM=2 (UMC 0.5μm CMOS) invokes the standard Start-Hspice junction model in pg. 15-40 to 15-51, Start-Hspice Manual, Release 1998.2.

For junction parasitic resistance, ACM=2 also uses the equations in pg. 15-40 to 15-51, Start-Hspice Manual, Release 1998.2.

Junction Resistance Model Parameters

Name	Units	Default	Description
RD	ohm/sq	0.0	drain ohmic resistance. This parameter is usually lightly doped regions' sheet resistance for ACM 1.
RDC	ohm	0.0	additional drain resistance due to contact resistance
RS	ohm/sq	0.0	source ohmic resistance. This parameter is usually lightly doped regions' sheet resistance for ACM 1.
RSC	ohm	0.0	additional source resistance due to contact resistance
RSH	ohm/sq	0.0	drain and source diffusion sheet resistance

AC and capacitance model parameter

Name	Units	Default	Comments
CAPMOD	-	0	Selects from BSIM3 versions 3.0 3.1 3.11(version=3.11 is the HSPICE97.4 equivalent to BSIM3v3 version3.1)
XPART	-	1	Charge portioning rate flag(default deviates from BSIM3V3=0)
CGSO	F/m	P1(see Note1)	Non-LDD region source-gate overlap capacitance per unit channel length

CGDO	F/m	P2(see Note2)	Non-LDD region source-gate overlap capacitance per unit channel length
CGBO	F/m	0	Gate-bulk overlap capacitance per unit channel length
CGS1	F/m	0.0	Lightly doped source-gate overlap region capacitance
CGD1	F/m	0.0	Lightly doped source-gate overlap region capacitance
CKAPPA	F/m	0.6	Coefficient for lightly doped region overlap capacitance fringing field capacitance
CF	F/m	(see note3)	Fringing field capacitance
CLC	M	0.1e-6	Constant term for the short channel model
CLE	-	0.6	Exponential term for the short channel model
DLC	M	LINT	Length offset fitting parameter from CV
DWC	M	WINT	Width offset fitting parameter from CV

The capacitance model equation can be seen from BSIM 3v3.2.2 manual in appendix B.note that capmod=2 and XPART=0 (0/100 charge partition)

§ 1-3 Other HSPICE Model parameter

Model Flags

Name	**Units**	**Default**	**Comment**
VERSION	-	3.11	Selects from BSIM3 version 3.0,3.1,3.11(version=3.11 is the HSPICE97.4 equivalent to BSIM3v3 version3.1)
BINFLAG	-	0	Uses wref,lref when set>0.9
NOIMOD	-	1	Berkeley noise modelflag
NLEV	-	0(off)	Star-Hspice noise model flag (non-zero overrides NOIMOD)(star-HSPICE specific)
NQSMOD	-	0(off)	NQS Model is not supported in Level49
SFVTFLAG	-	1(on)	Spline function for Vth(star-Hspice specific)
VFBFLAG	-	0(off)	UFB selector for CAPMOD=0(star-HSPICE specific)

Bin Description Parameter

Name	**Units**	**Default**	**Comment**
LMIN	M	0.0	minimum channel length
LMAX	M	1.0	Maximum channel length
WMIN	M	0.0	minimum channel width
WMAX	M	1.0	Maximum channel width
BINUNIT	-	0	Flicker noise parameter

Process Parameter 5

Noise Parameter 7

NQS Parameter 1

Chapter 2 CMOS Process Technology and Layout Rule

§ 2 – 1 Typical Submicron CMOS Process Flow

0.5μm SPDM twin-well polycide-gate CMOS technology

Major Process Steps:

1. Lightly-doped (15-20 Ω-cm , P) p-type substrate , <100>
2. N-well region definition (NW , Mask # 1)
3. N-well implantation (phosphorus) Fig. 3-1

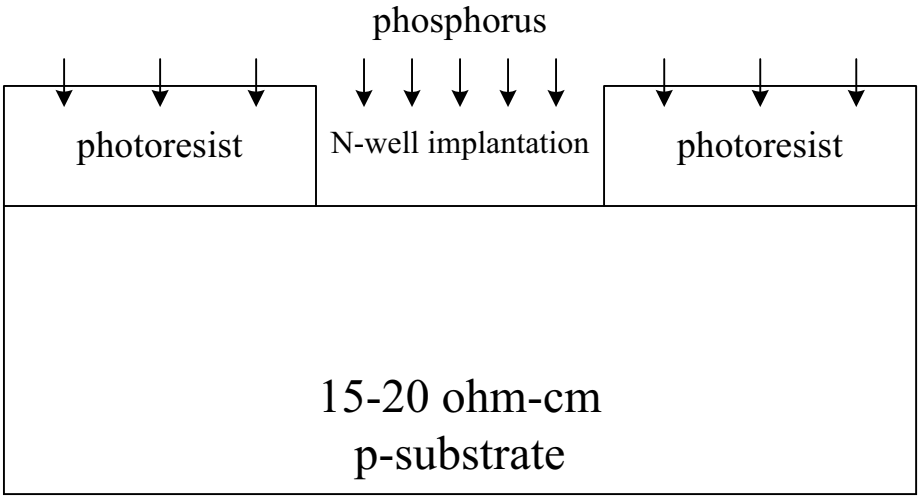


Fig. 3-1

4. P-well region definition (PW , Mask # 2)
5. P-well implantation (Boron) Fig. 3-2

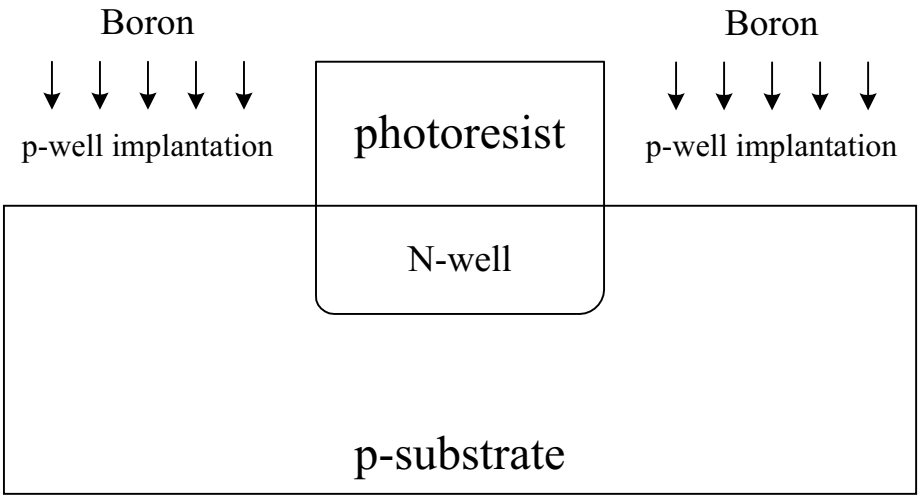


Fig. 3-2

6. Well drive-in with 350 Å oxide growth , 1100°C
7. Oxide strip.
8. Pad oxide growth (200 Å) ±25 Å , 920 °C
9. Si_3N_4 deposition (1500 Å) ±200 Å , 780 °C
10. Field oxide definition (SN , Mask #3)
11. Si_3N_4 and pad oxide etch
12. Field oxidation (500 Å) , 980 °C
13. P-field implantation definition (PF , Mask #4)
14. P-field implantation (Boron) Fig. 3-3

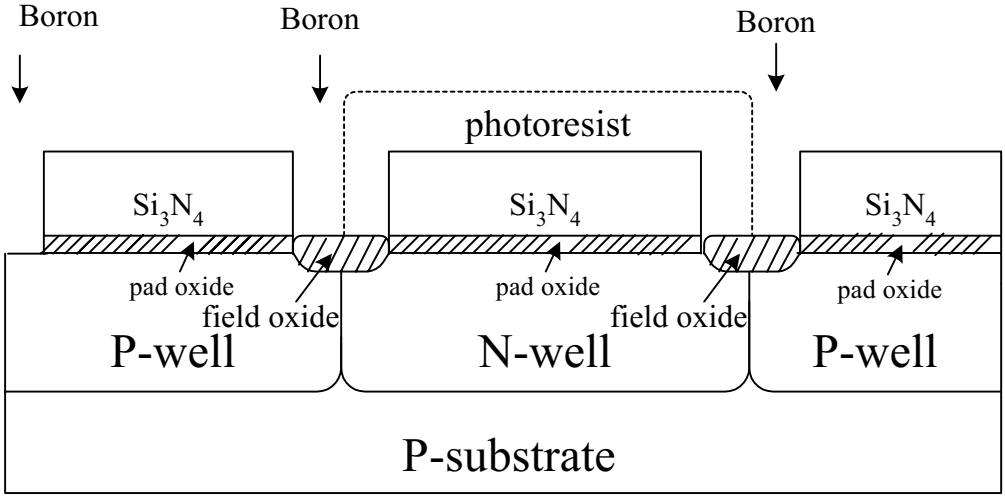


Fig. 3-3

15. Photoresist strip
16. Si_3N_4 and pad oxide removal

17. Pregate oxide growth (250 Å) and etch away
18. Pregate oxide growth (110 Å)
19. Threshold adjustment implantation (Boron) Fig. 3-4

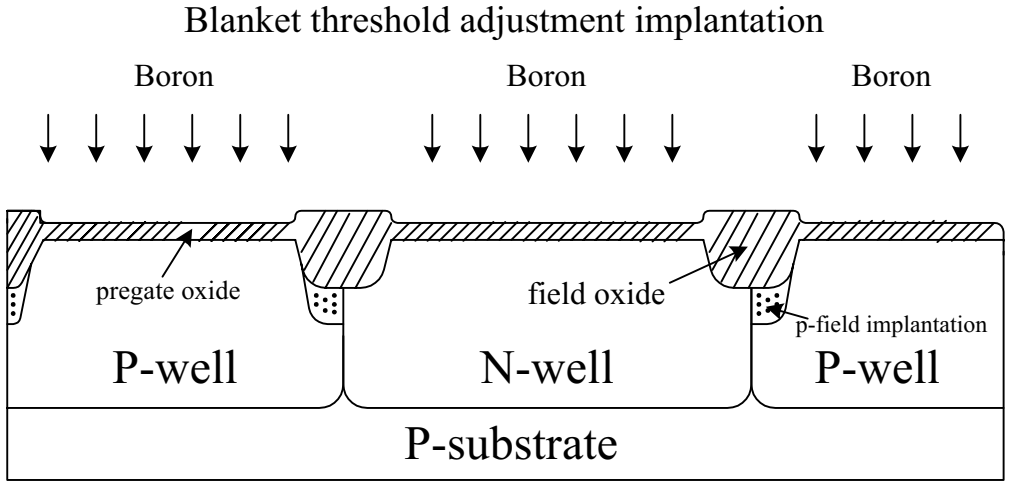


Fig. 3-4

20. Pregate oxide etching
21. Gate oxide growth (85 Å)
22. Polysilicon deposition (1500 Å)
23. Polysilicon doped with phosphorus (43 Ω/□)
24. WSi_2 deposition (1250 Å)
25. Polysilicon definition (PO , Mask #5)
26. Polysilicon etch Fig. 3-5

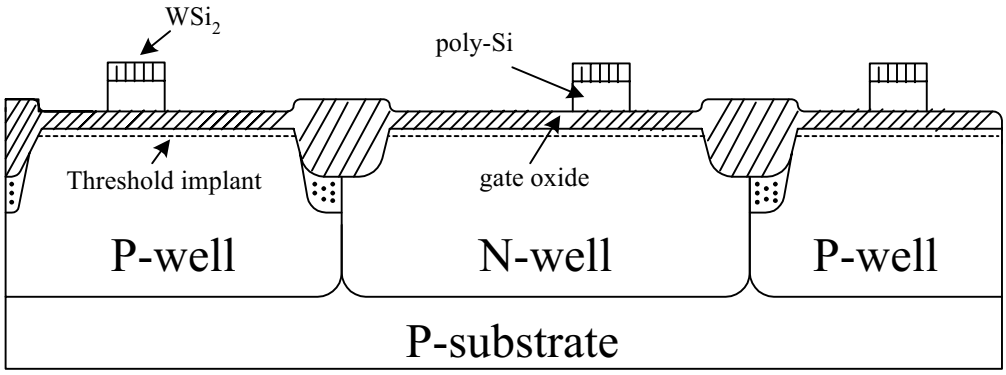


Fig. 3-5

27. NLDD implant definition (NM , Mask #6)
28. NLDD implantation (phosphorus and Asenic shallow implant)
29. WSi_2 anneal (180 Å)

30. PLDD implant definition (PM , Mask #7)
31. PLDD implantation (BF_2 shallow implant) Fig. 3-6

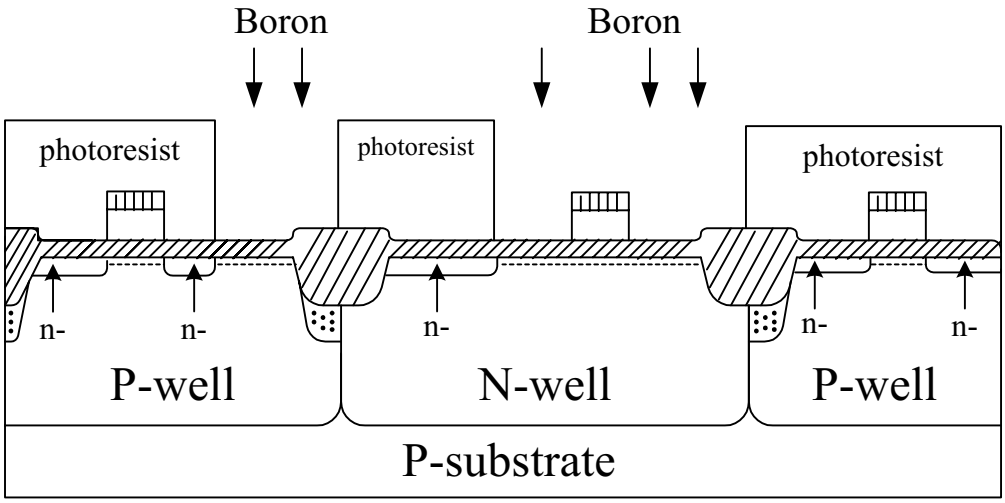


Fig. 3-6

32. Conformal sidewall spacer oxide deposition (2000 Å) , 700 °C
33. Anisotropic sidewall oxide etchback to form spacers
34. N^+ source/drain implant definition (NP , Mask #8)
35. N^+ source/drain implantation (As) Fig. 3-7

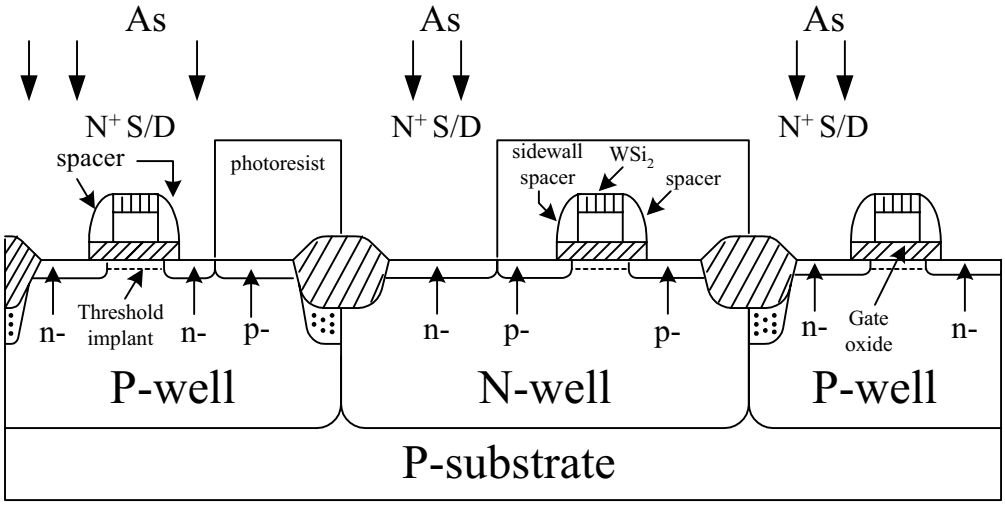


Fig. 3-7

36. P^+ source/drain implant definition (PP , Mask #9)
37. P^+ source/drain implantation (BF_2)
38. Low Temperature Oxide (LTO) – Boron – Phosphate Silicon Glass (BPSG) deposition (9000 Å doped , 2000 Å undoped)
39. Flow , 850 °C

40. Contact definition (CO , Mask #10)
41. Contact etching
42. Annealing Fig. 3-8

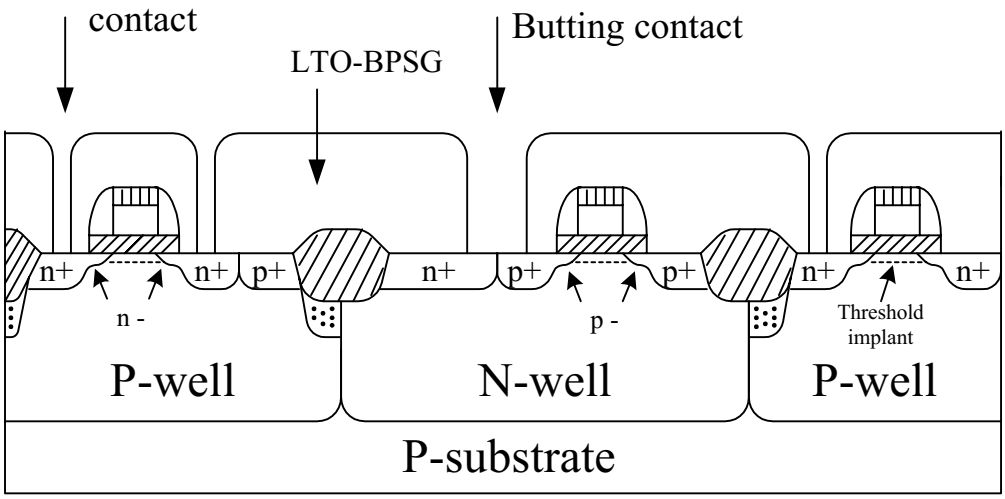


Fig. 3-8

43. Plug barrier deposition (Ti 400 Å / TiN 1000 Å)
44. Barrier annealing
45. W Plug deposition 6000 Å
46. Metal 1 sputtering (AlCu 4000 Å / TiN 1400 Å)
47. Metal 1 definition (M1 , Mask #11)
48. Metal 1 etching
49. Via oxide deposition (2000 Å + 5000 Å + 2000 Å)
50. Via hole definition (VI , Mask #12)
51. Via hole etching
52. Plug barrier2 TiN(1000 Å)
53. Plug deposition2 W(6000 Å)
54. Metal 2 sputtering [AlCu (18000 Å) / TiN (250 Å)]
55. Metal 2 definition (M2 , Mask #13)
56. Metal 1 etching Fig. 3-9

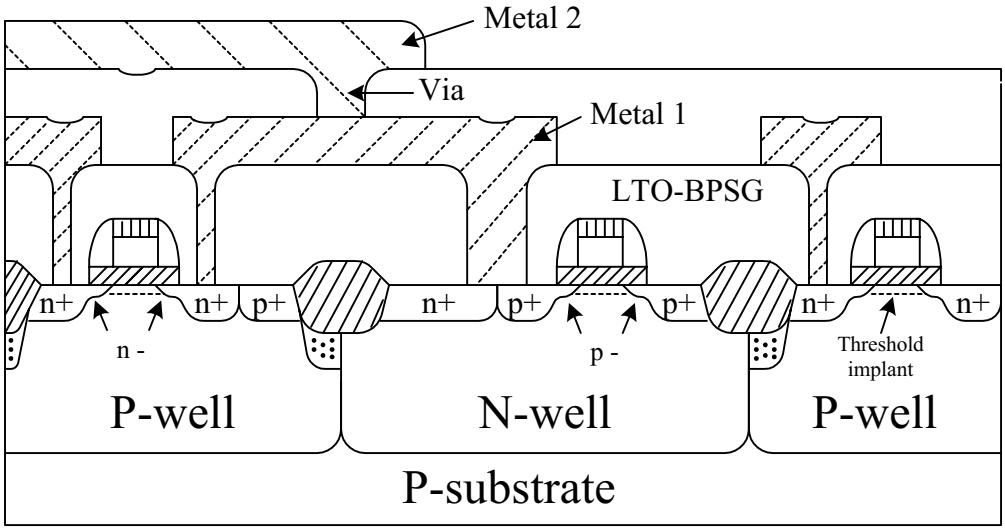


Fig. 3-9

57. Passivation oxide deposition (2000 Å)
58. Passivation Si_3N_4 deposition (7000 Å)
59. Pad definition (CB , Mask #14)
60. Alloy

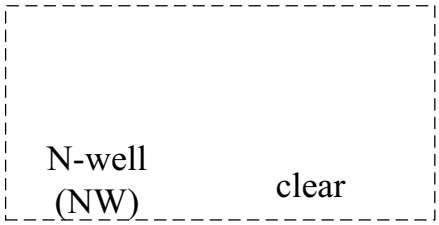
Total photolithography steps : 14

§ 2 – 2 Typical CMOS layout example

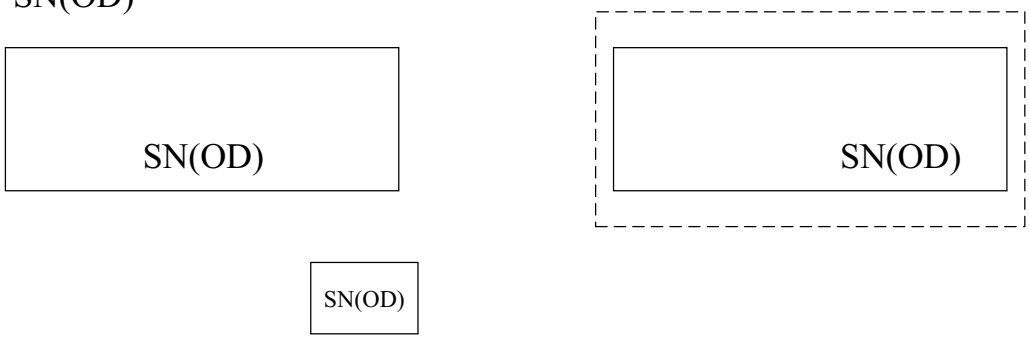
(1) Well Masking _ _ _ _ _ _ _
NW,PW

dark

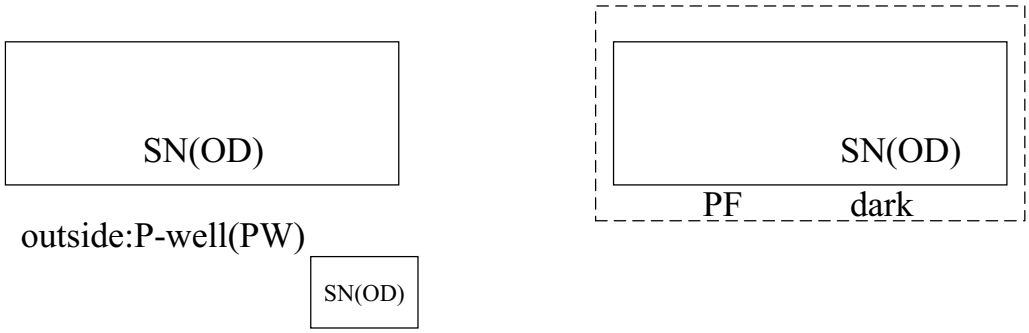
outside: P-well (PW)



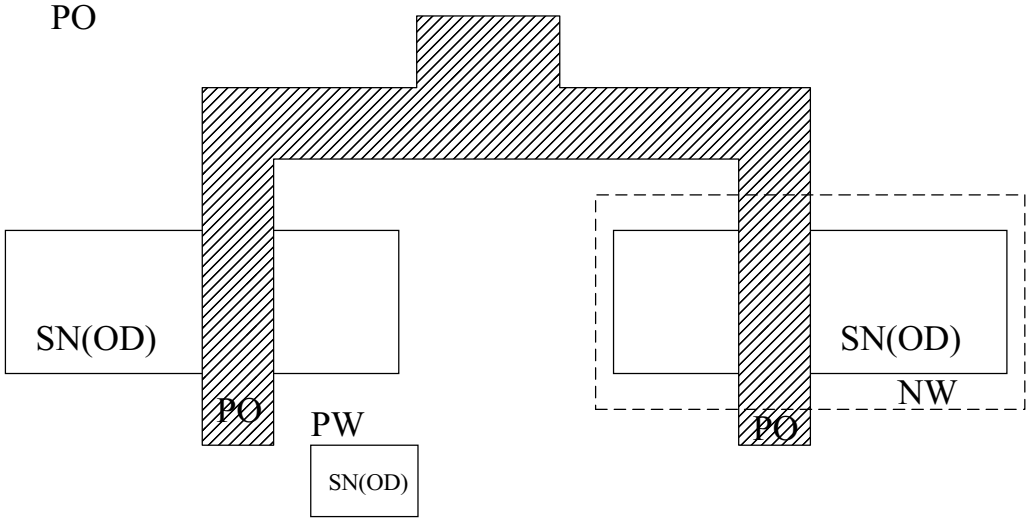
(2) Field-Oxide (Thin-Oxide) Masking ————
SN(OD)



(1A) P-Field Masking (PF)



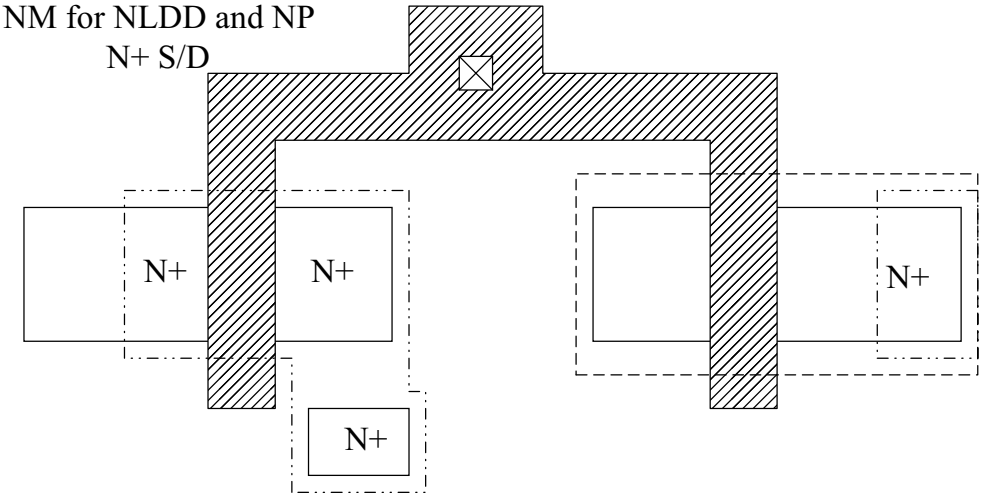
(3) Poly Masking
PO



(4) N+ Masking

NM for NLDD and NP

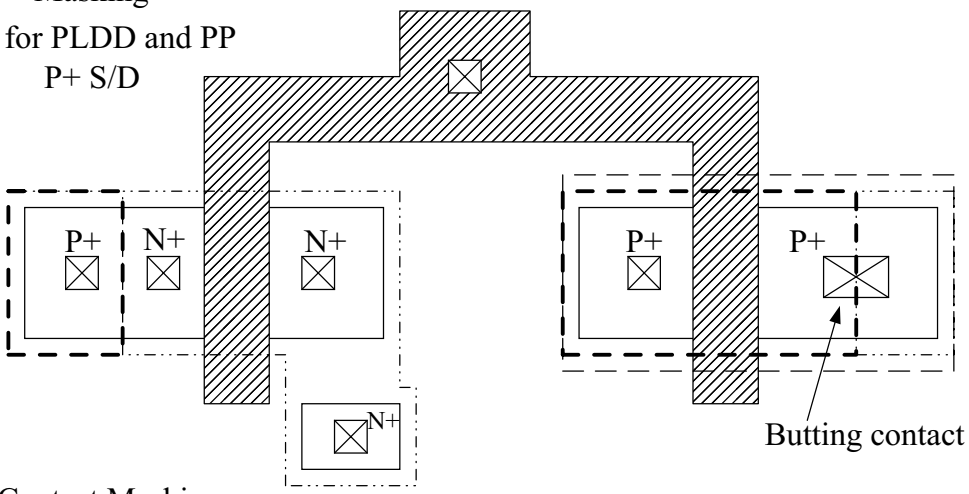
N+ S/D



(5) P+ Masking

PM for PLDD and PP

P+ S/D



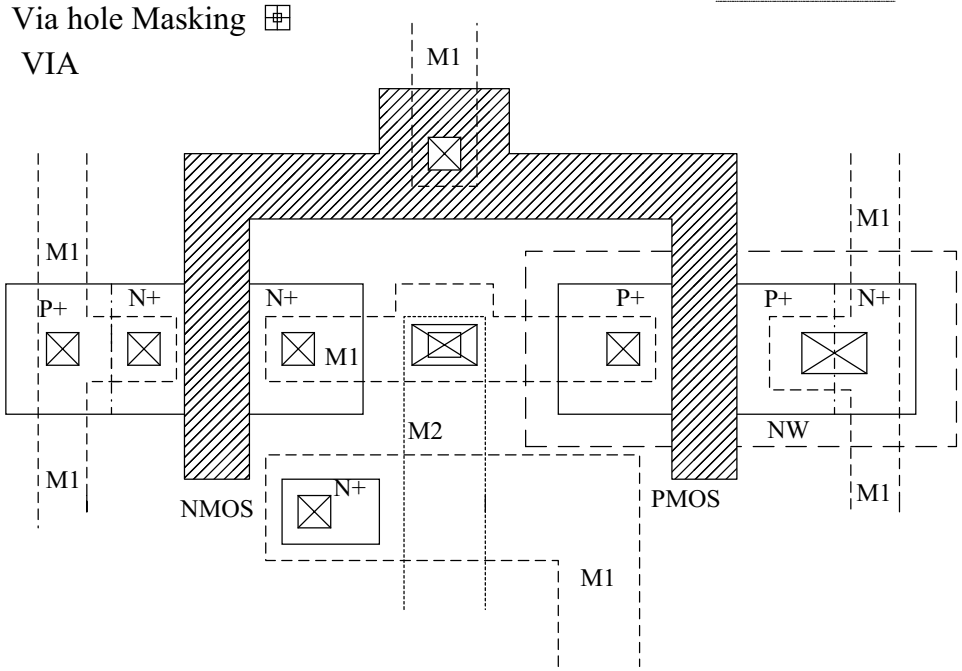
(6) Contact Masking

CO ⊠ shown in the above figure

(7) Metal 1 Masking ---------- M1

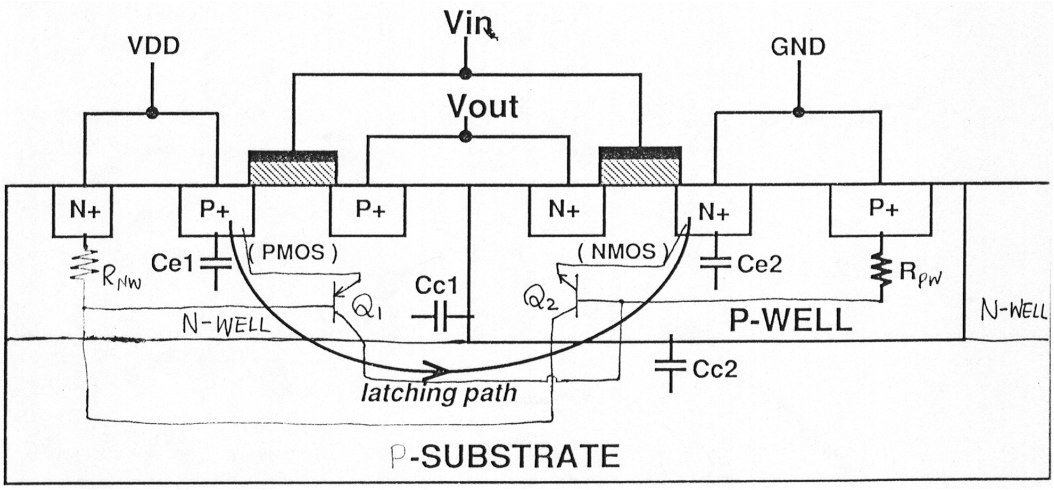
(8) Via hole Masking ⊞ VIA

(9) Metal 2 Masking M2

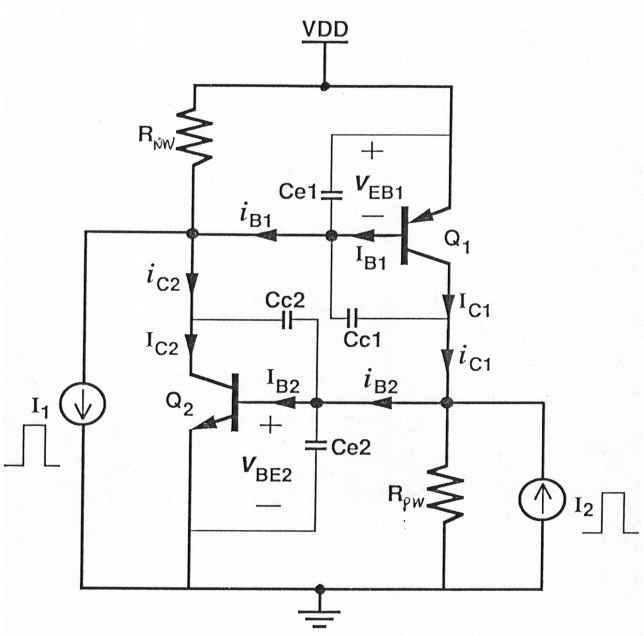


§ 2-3 Layout Rules for Latchup

Parasitic p-n-p-n (SCR) structure in bulk CMOS：



Lumped equivalent circuit of the parasitic p-n-p-n (SCR) structure：



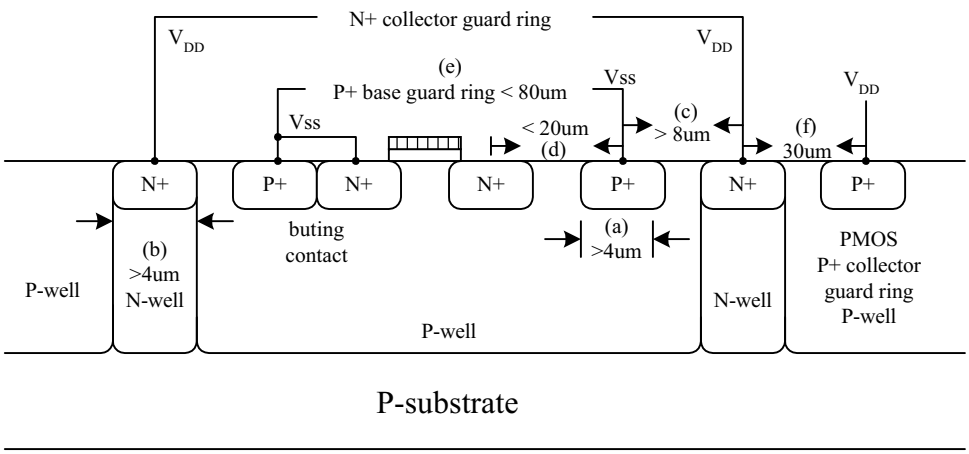
§ 2-3.1 Layout rule of MOS transistors for I/O parts or large driver (Based on 0.8μm layout rule)

1. NMOS transistor：

(1) A P+ base guard ring should surround the NMOS. The P+ base guard ring must be connected to Vss by an unbroken metal line.

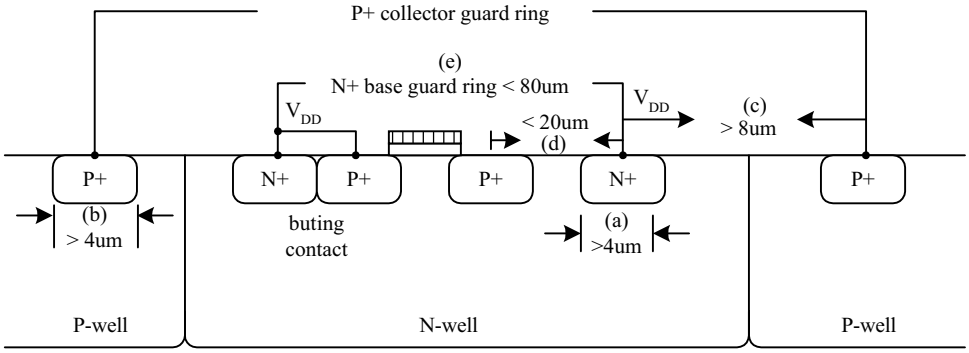
(2) Maximum distance between surrounded P+ base guard ring is 80μm (e)

(3) Minimum width of the P+ base guard ring is 4μm (a)



(4) Maximum distance between N+ source/drain areas and the nearest p-well contact inside the P+ base guard ring must be less than 20μm (d). A butting contact is preferred if the process is allowed.
(5) N+ collector guard ring coupled with N-well should be placed outside the p-well region. The N+ guard ring must be connected to V_{SS} by an unbroken metal line.
(6) The minimum width of the N+ collector guard ring is 4μm(b).
(7) The minimum space between the P+ base guard ring and the N+ collector guard ring is 8μm(c).
(8) Minimum space between NMOS N+ collector guard ring and PMOS P+ collector guard ring is 30μm(f).

2. PMOS transistor:



(1) A N^+ base guard ring should surround the PMOS. The N^+ base guard ring must be connected to VDD by an unbroken metal line.
(2) Maximum distance between the surrounded N^+ base guard ring is 80μm.(e)
(3) Minimum width of the N^+ base guard ring is 4μm (a)
(4) Maximum distance between P^+ source/drain areas and the nearest N-well contact inside the N^+ base guard ring must be less than 20μm(d). A butting contact is preferred if the process is allowed.
(5) P^+ collector guard ring should be placed outside the N-well region. The P^+ collector guard ring should be connected to Vss by an unbroken metal line.

(6) Minimum width of the P^+ collector guard ring is 4μm.
(7) Minimum space between N^+ base guard ring and P^+ collector guard ring is 8μm (c).

§ 2-3.2 Layout rule of internal circuits

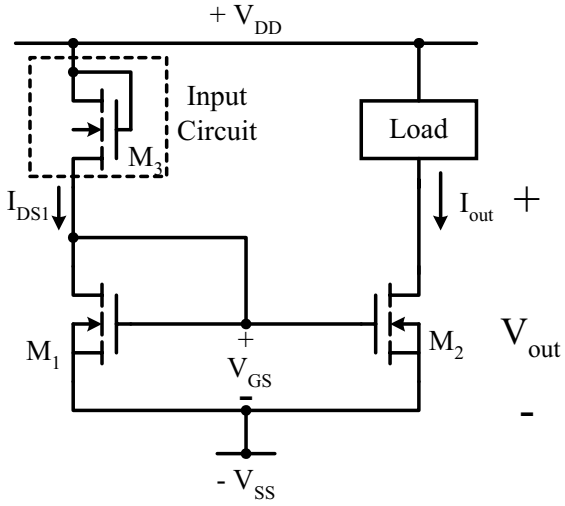
(1) The internal circuit must be separated from I/O transistors with at least a double ring structure (with one N^+ connected to VDD and one P^+ connected to Vss).
(2) It is also recommended that large drivers are surrounded with a double guard ring structure.
(3) In an N-well (P-well), N-well (P-well) contacts should be used as many as possible. The maximum distance between a $P^+(N^+)$ source/drain area and the nearest N-well (P-well) contact is 40μm.

Chapter 3 Current Sources and Simple Voltage Sources

§ 3-1 MOS Simple Current Sources

§ 3-1.1 NMOS Current Sources

1. MOS Widlar current mirror



(M_3) M_1: $V_{GS} = V_{DS} \Rightarrow V_{DS} > V_{GS} - V_{TH}$ Both are sat.

M_2: must be kept in the sat. region

i.e. $V_{out} > V_{GS} - V_{TH}$ or V_{DSAT}

$$I_{out} = I_{DS2} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_2 (V_{GS2} - V_{TH2})^2 (1 + \lambda_2 V_{out})$$

$$I_{DS1} = I_{DS3} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TH1})^2 (1 + \lambda_1 V_{GS1})$$

$$= \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_3 (V_{GS3} - V_{TH3})^2 (1 + \lambda_3 V_{GS3})$$

M_1 is identical to $M_2 \Rightarrow$ $V_{TH1} = V_{TH2} = V_{TH}$

$\lambda_1 = \lambda_2 = \lambda$

$\mu_n C_{ox}$ are the same

$$\frac{I_{out}}{I_{REF}} = \frac{(W/L)_1}{(W/L)_2}\frac{1 + \lambda V_{out}}{1 + \lambda V_{DS}}$$

$I_{DS1} = I_{DS3} = I_{REF}$ is called the reference current .

It can be generated by M_3 or other input circuits.

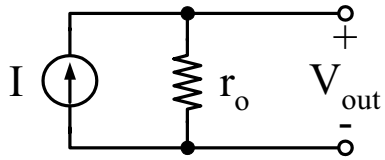
* If $\lambda \to 0 \Rightarrow \quad \frac{I_{out}}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}$

The output current I_{out} depends only on the geometric ratio. $\Rightarrow I_{out}$ can be a constant current if I_{REF} is a stable current.

I_{out} is nearly independent of V_{out} if M_2 is sat.

* $r_o = r_{ds2} = (\lambda I_{out})^{-1}$ $\qquad L_2 \uparrow \Rightarrow r_o \uparrow$

Remember:



Ideal current source:

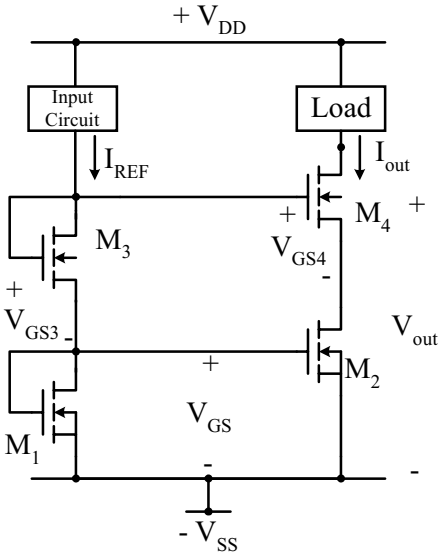
(1) I = constant , indep. of the loading and V_{out}

(2) $r_o = \infty$.

* To guarantee matched device characteristics, $L_1 = L_2$ is preferred and long channel devices are used. W_1 and W_2 should be kept large enough to avoid narrow channel effect.

* Can be used in the subthreshold poeration.

2. Cascode MOS Widlar current mirror



* M_4 and M_2 must be in the saturation region.
* M_1/M_2 (M_3/M_4) should have matched device characteristics.
* M_4 and M_2 must be in the sat. region
  $\Rightarrow$ Large V_{out} is required
  $\Rightarrow$ The voltage swing of the load is limited especially for low
  V_{DD}.

* $r_o = r_{ds2} + r_{ds4} + r_{ds2} r_{ds4} (1+\eta_4) g_{m4} \approx g_{m4} r_{ds2} r_{ds4}$
  High output resistance (by a factor of $g_{m4} r_{ds4}$)
  $\Rightarrow$ Long channel is used for M_4 to obtain a large r_{ds4}

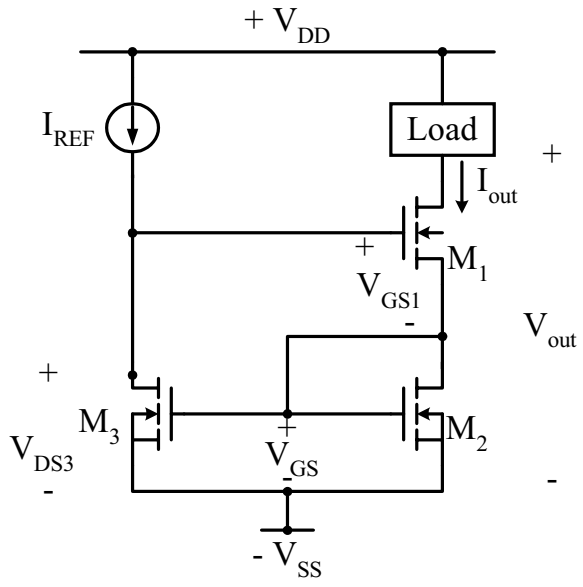
* $\frac{I_{out}}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1} \frac{1+\lambda V_{DS2}}{1+\lambda V_{GS}}$
  The output current is still determined by the bottom mirror.

* To guarantee $V_{GS} = V_{DS2}$ and matched device characteristics, $(W/L)_2/(W/L)_1 = (W/L)_4/(W/L)_3$ is used and $L_1=L_2=L_3=L_4$ is preferred. Thus $V_{GS3}=V_{GS4}$ and $V_{GS}=V_{DS2}$.

* Note that M_3 and M_4 have body effect
  $\Rightarrow V_{GS3}/V_{GS4} \uparrow$ and required $Vout \uparrow$
  $\Rightarrow (W/L)_3 > (W/L)_1$
  $(W/L)_4 > (W/L)_2$ is adopted for compensation.

* The resistance seen from the input circuit is much smaller than $r_0 \Rightarrow$ Inbalance r_o.

* Can be used in the subthreshold operation.



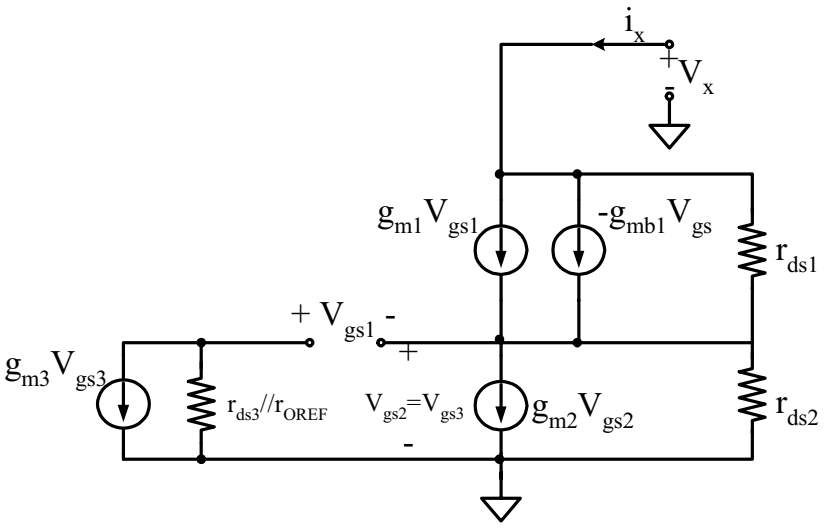
3.MOS Wilson current source

$$\frac{I_{out}}{I_{REF}} = \frac{(W/L)_2}{(W/L)_3}\frac{1+\lambda V_{DS2}}{1+\lambda V_{DS3}}$$
$$V_{DS2} = V_{GS}$$
$$V_{DS3} = V_{GS} + V_{GS1}$$
$$V_{DS2} \neq V_{DS3}$$

* Inherent inbalance

$\Rightarrow \frac{I_{out}}{I_{REF}}$ depends on V_{GS} and V_{GS1}

$\Rightarrow$ High precision ratio is not obtainable.



$$r_o \cong r_{ds1} + r_{ds1}\left[\frac{g_{m1}g_{m3}(r_{ds3} // r_{OREF}) + g_{m1}}{g_{m2} + \frac{1}{r_{ds2}} + g_{mb1}}\right] + \frac{1}{g_{m2} + \frac{1}{r_{ds2}} + g_{mb1}}$$

If $r_{ds2} >> \frac{1}{g_{m2}}$

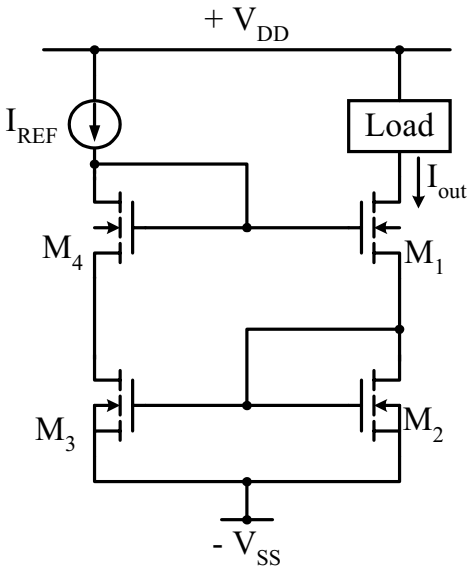
$$\Rightarrow r_o = \frac{1}{(g_{m2} + \eta_1 g_{m1})} + r_{ds1}\left\{1 + (\frac{g_{m1}}{g_{m2} + \eta_1 g_{m1}})[1 + g_{m3}(r_{ds3} // r_{OREF})]\right\}$$
$$\cong g_{m3}(r_{ds3} // r_{OREF})(\frac{g_{m1}}{g_{m2} + \eta_1 g_{m1}})r_{ds1}$$

Assume $g_{m1} = g_{m2} = g_{m3} = g_m$ and $\eta_1 \to 0$

$$r_o \cong \frac{1}{g_m} + r_{ds1}[2 + g_m(r_{ds3} // r_{OREF})]$$
$$\cong r_{ds1}[g_m(r_{ds3} // r_{OREF})]$$

* The output resistance is nearly the same as that of the cascoded current mirror.
* Only 3 MOS's are used.
* Can be operated in the subthreshold region.

4. Improved Wilson current source



$$\frac{I_{out}}{I_{REF}} = \frac{(W/L)_2}{(W/L)_3}\frac{1+\lambda V_{GS2}}{1+\lambda V_{DS3}}$$

$$V_{DS3} = V_{GS2} + V_{GS1} - V_{GS4}$$

Set $V_{GS1} = V_{GS4}$ $\left[i.e. \quad (W/L)_1 / (W/L)_4 = (W/L)_2 / (W/L)_3\right]$

$\Rightarrow V_{DS3} = V_{GS2}$

$\frac{I_{out}}{I_{REF}} = \frac{(W/L)_2}{(W/L)_3}$ precise ratio.

* Inherent balance like the cascode current source.

* High output resistance.

* 4 MOS's are needed.

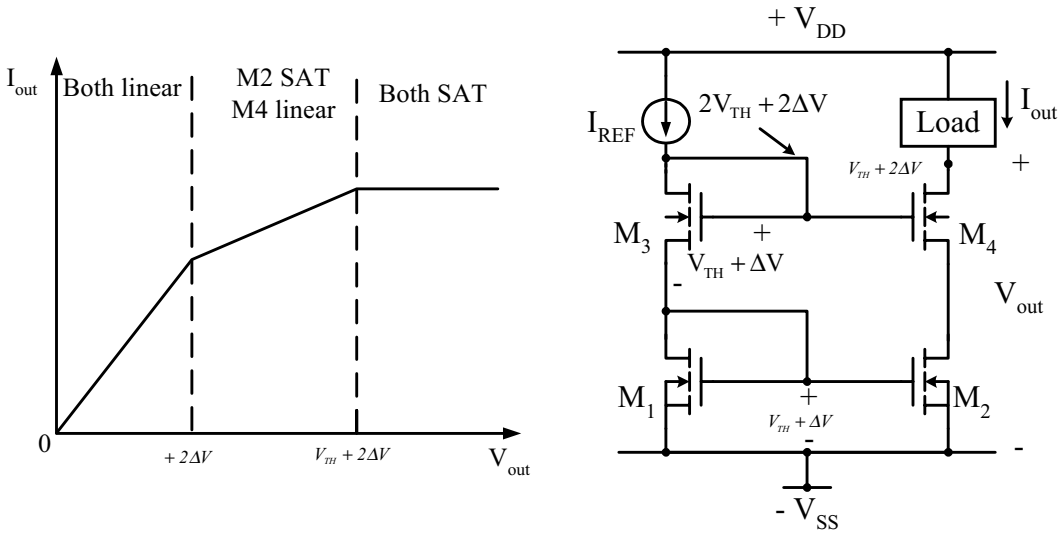
* $(W/L)_1 / (W/L)_4 = (W/L)_2 / (W/L)_3 \Rightarrow V_{DS3} = V_{GS2} = V_{GS3}$

and M3 sat.

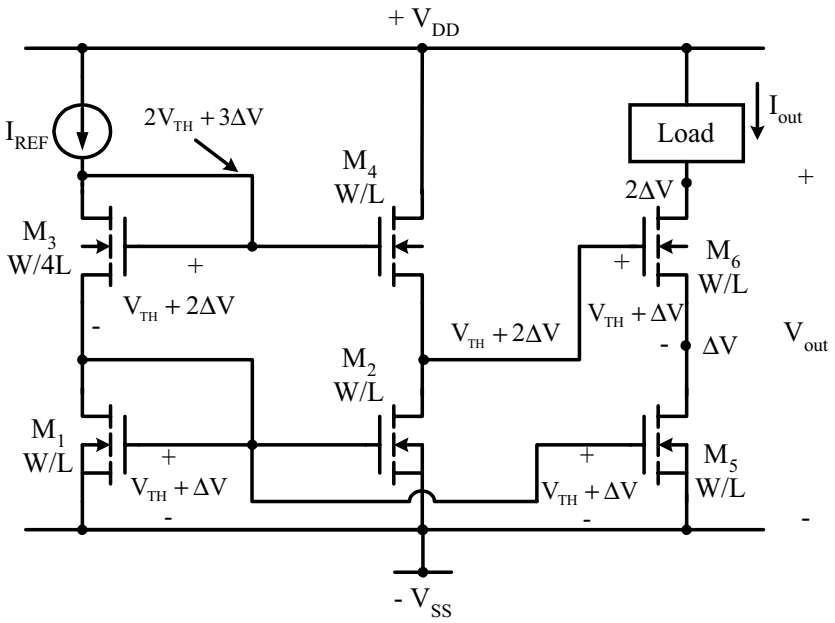
* Better r_o balance between load and I_{REF} nodes.
* Can be used in the subthreshold operation.

5. High-swing cascode current source

A. Conventional type :



B. With source-follower level shifter :



$$I_{DS1} = I_{DS3} = \frac{W}{L}\frac{\mu_n C_{ox}}{2}(V_{TH} + \Delta V - V_{TH})^2$$

$$= \frac{1}{4}\frac{W}{L}\frac{\mu_n C_{ox}}{2}(V_{GS3} - V_{TH})^2$$

$$\Rightarrow V_{GS3} = V_{TH} + 2\Delta V$$

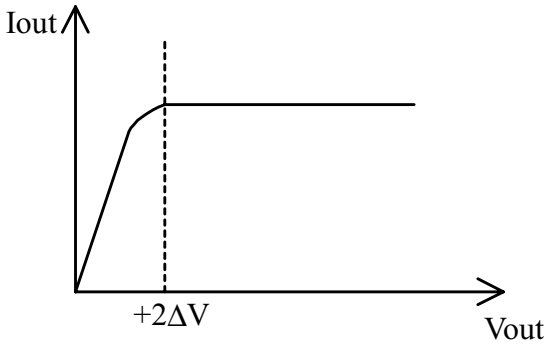
*High r_o.

*High output swing.

*Two extra MOS's.

*$V_{DS1}=V_{TH}+\Delta V \neq V_{DS5}=\Delta V$

Inbalance current ratio.



C. With constant V_B bias circuit

M_3 in saturation:

$$V_B - V_{TH3} \le V_{GS1}(=Vx)$$

M_1 in saturation:

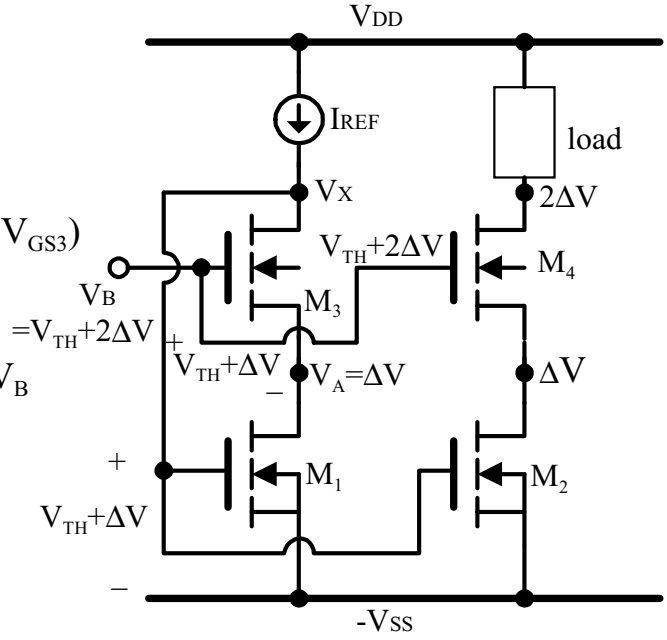
$$V_{GS1} - V_{TH1} \le V_A(=V_B - V_{GS3})$$

$$\Rightarrow \quad V_{GS3} + (V_{GS1} - V_{TH1}) \le V_B$$

$$\le V_{GS1} + V_{TH3}$$

$$\Rightarrow \quad V_{GS3} - V_{TH3} \le V_{TH1}$$

or $\Delta V \le V_{TH}$



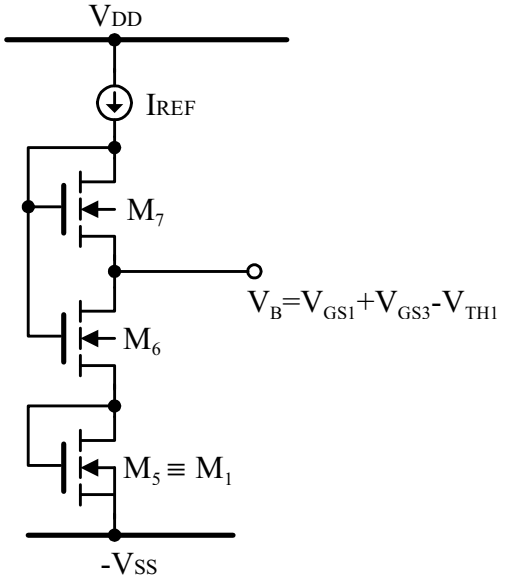
If $V_B=V_{GS3}+(V_{GS1}-V_{TH1})=V_{TH}+2\Delta V$

$\Rightarrow$ * The swing of load can be $V_{DD}-2\Delta V$.

* M_1 and M_2 have the same V_{DS} to obtain a precise current ratio.

The generation of V_B :

$M_5 \equiv M_1 \Rightarrow V_{GS5}= V_{GS1}$
$\Rightarrow (W/L)_6 < (W/L)_3$
$\Rightarrow V_{GS6} > V_{GS3}$
$(W/L)_7$ is large
$V_{GS7} \cong V_{TH7} > V_{TH1}$
Choose $(W/L)_6$ so that
$V_{GS6} - V_{GS7}= V_{GS3} - V_{TH1}$



§ 3-1.2 General Advantages of MOS Current Sources

1. Effective current gain $\beta \rightarrow \infty$

   ⇒ No dc loading of slave stages on the master stage

   (Unlike the BJT multi-stage current mirrors)

2. Current ratio ≅ MOS channel geometric ratio

3. High packing density

4. I_{out} can be as small as several nA.

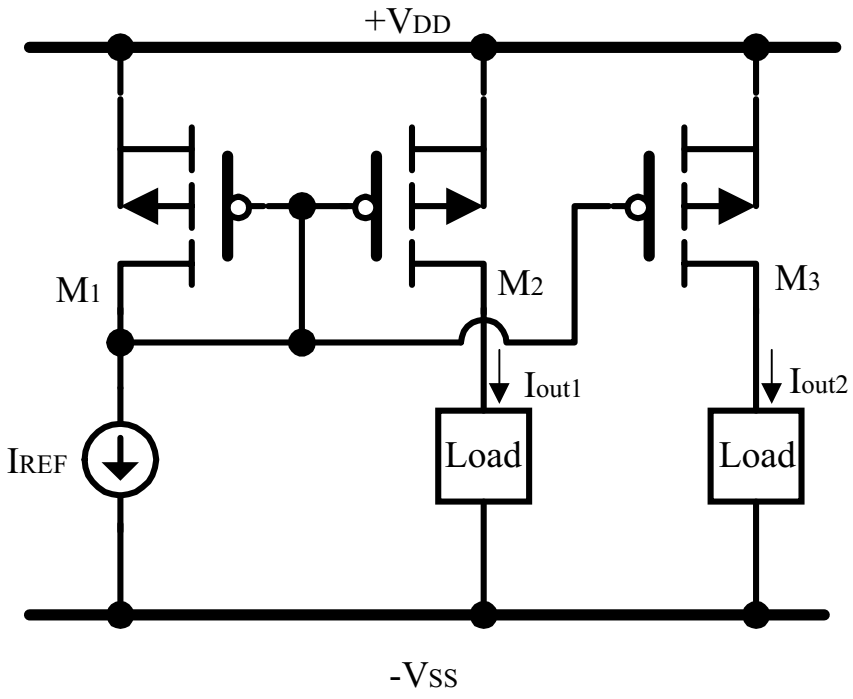
   Generally, if Iout < ~nA, leakage current dominates the output current

   ⇒ The ratio is not constant anymore.

§ 3-1.3 PMOS/CMOS Current Sources

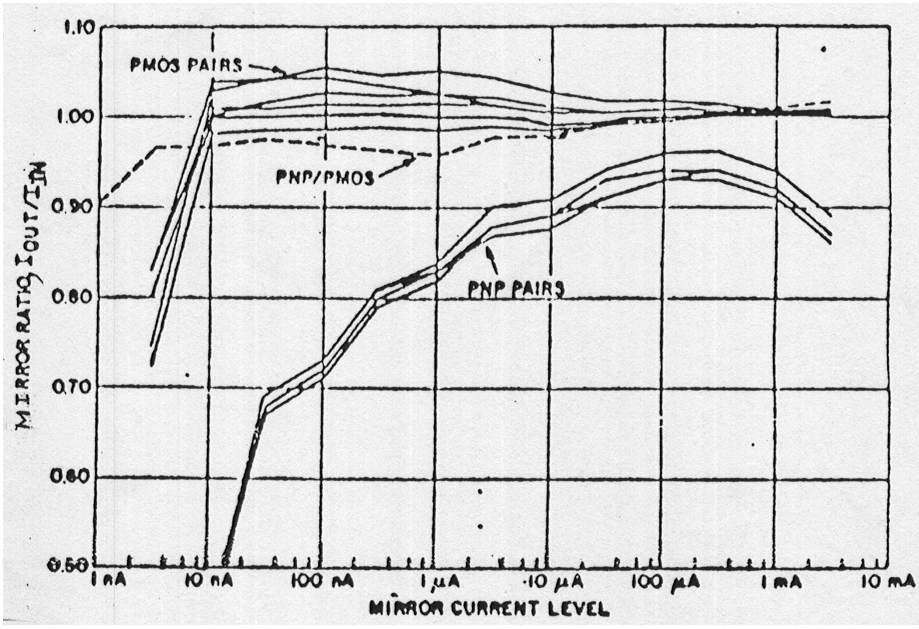
All NMOS current sources can be converted into PMOS current sources. They can be used in CMOS technology.

Example: Multi-stage PMOS Widlar current source



* Iout $>$ 10μA $\Rightarrow$ $V_{GS} > V_T$ and $I_D \propto (V_{GS} - V_T)^2$, square law

$\Rightarrow$ good ratio constancy.



§ 3-2 Supply – Independent Current Sources

§ 3-2.1 CMOS Peaking Current Source

CASE I：Subthreshold operation

In M1 and M3,

$I_{DO1}=I_{DO3}$ ，$V_{DS} >> v_t$

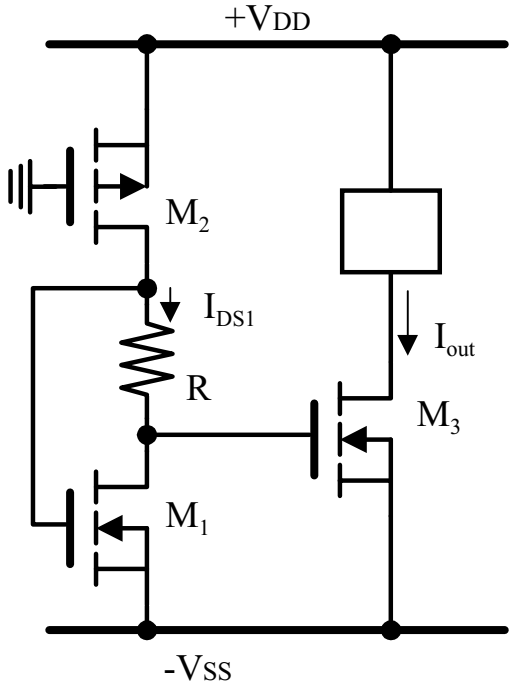
$V_{GS1}=I_{DS1}R+V_{GS3}$

$$I_{DS1}=\left(\frac{W}{L}\right)_1 I_{D0}e^{V_{GS1}/nv_t}$$

$$=\left(\frac{W}{L}\right)_1 I_{D0}e^{(I_{DS1}R+V_{GS3})/nv_t}$$

where $I_{D0}=I_{S0}/(W/L)$

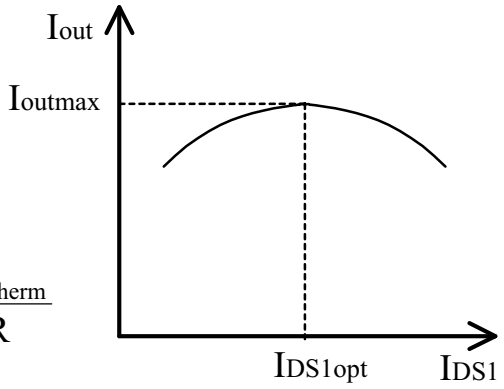
$$I_{out}=I_{D3}=\left(\frac{W}{L}\right)_3 I_{D0}e^{V_{GS3}/nv_t}$$



$$\frac{I_{out}}{I_{DS1}} = \frac{(W/L)_3}{(W/L)_1} e^{-I_{DS1}R/nv_t}$$

$$I_{out} = I_{DS1}\frac{(W/L)_3}{(W/L)_1}\exp\left(-\frac{RI_{DS1}}{nv_t}\right)$$

$$\frac{\partial I_{out}}{\partial I_{D1}} = 0,\ \frac{\partial^2 I_{out}}{\partial I_{D1}^{\ 2}} < 0 \Rightarrow I_{D1opt} = \frac{nV_{therm}}{R}$$



$$\Rightarrow I_{out\,max} = \frac{(W/L)_3}{(W/L)_1}\frac{nv_t}{eR} = \frac{(W/L)_3}{(W/L)_1}\frac{I_{DS1opt}}{e}$$

* Power supply independent current with output current proportional to v_t
* Choose $I_{REF}=I_{DS1}=I_{DS1opt}$, I_{outmax} can be controlled by R or $(W/L)_3/(W/L)_1$
* R can be implemented by the n+ source/drain diffusion.
  It can also be made by adjustable resistors.
* If $I_{REF}=I_{DS1opt}$ has some inevitable variations, the resultant variations on I_{outmax} is reduced because $\partial I_{out}/\partial I_{DS1}$ arround I_{DS1opt} is very small.
* Two-stage peaking current sources can be used to further reduce the variations of I_{outmax}. I_{out} can be used to generate I_{DS1opt}
* Process variation and temperature coefficient (positive) on R should be considered.

CASE II: Saturation operation

$$I_{DS1} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TH})^2$$

$$= \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_1 (V_{GS3} + I_{DS1}R - V_{TH})^2$$

$$I_{out} = I_{DS3} = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_3 (V_{GS3} - V_{TH})^2$$

$$I_{out} = \frac{(W/L)_3}{(W/L)_1}\frac{(V_{GS3} - V_{TH})^2 I_{DS1}}{(V_{GS3} - V_{TH} + I_{DS1}R)^2}$$

$$\frac{\partial I_{out}}{\partial I_{DS1}} = 0, \frac{\partial^2 I_{out}}{\partial I_{DS1}^{\ 2}} < 0 \Rightarrow I_{DS1opt} = \frac{V_{GS3} - V_{TH}}{R}$$

$$\Rightarrow I_{out\,max} = \frac{(W/L)_3}{(W/L)_1}\frac{V_{G3} - V_{TH}}{4R} = \frac{(W/L)_3}{(W/L)_1}\frac{1}{4} I_{DS1opt}$$

* $I_{out\,max}$ is power supply independent, but not proportional to v_t.

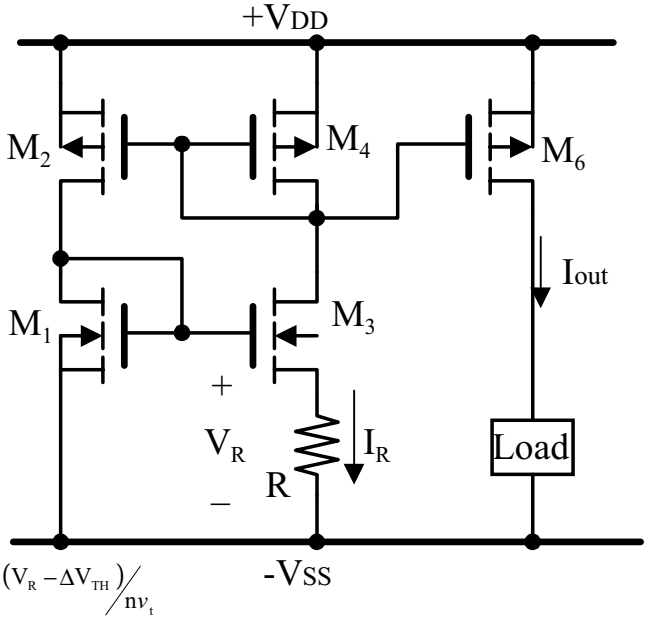
* Other features are the same as those in the subthreshold operations.

§ 3-2.2 CMOS v_t Standard Current Source

M1, M2, M3 and M4 are operated in the subthreshold region.

CASE I:

M1 and M3 are in the same p-well



$$V_{GS3} = V_{GS1} - V_R + \Delta V_{TH}$$

$$V_{DS1} >> v_t, V_{DS3} >> v_t$$

$$I_{DS1} = \left(\frac{W}{L}\right)_1 I_{DON} e^{V_{GS1}/nv_t}$$

$$= I_{DS2} = \left(\frac{W}{L}\right)_2 I_{DOP} e^{V_{GS2}/nv_t}$$

$$I_{DS4} = \left(\frac{W}{L}\right)_4 I_{DOP} e^{V_{GS2}/nv_t}$$

$$= I_{DS3} = \left(\frac{W}{L}\right)_3 I_{DON} e^{V_{GS1}/nv_t} e^{-(V_R - \Delta V_{TH})/nv_t}$$

$$\Rightarrow e^{V_{GS2}/nv_t} = \frac{\left(W/L\right)_1}{\left(W/L\right)_2} e^{V_{GS1}/nv_t}$$

$$\left(\frac{W}{L}\right)_4 \frac{\left(W/L\right)_1}{\left(W/L\right)_2} e^{V_{GS1}/nv_t} = \left(\frac{W}{L}\right)_3 e^{V_{GS1}/nv_t} e^{-(V_R - \Delta V_{TH})/nv_t}$$

$$\Rightarrow V_R = nv_t \ln\left[\frac{\left(\frac{W}{L}\right)_3\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1\left(\frac{W}{L}\right)_4}\right] + \Delta V_{TH}$$

where $\Delta V_{TH} = \text{GAMMA}\left(\sqrt{\phi_S + V_R} - \sqrt{\phi_S}\right)$

CASE II:

M3 is in a separated well(special process)with V_{BS}=0, $V_{GS3} = V_{GS1} - V_R$

$$\Rightarrow V_R = nV_t \ln\left[\frac{\left(W/L\right)_3\left(W/L\right)_2}{\left(W/L\right)_1\left(W/L\right)_4}\right]$$

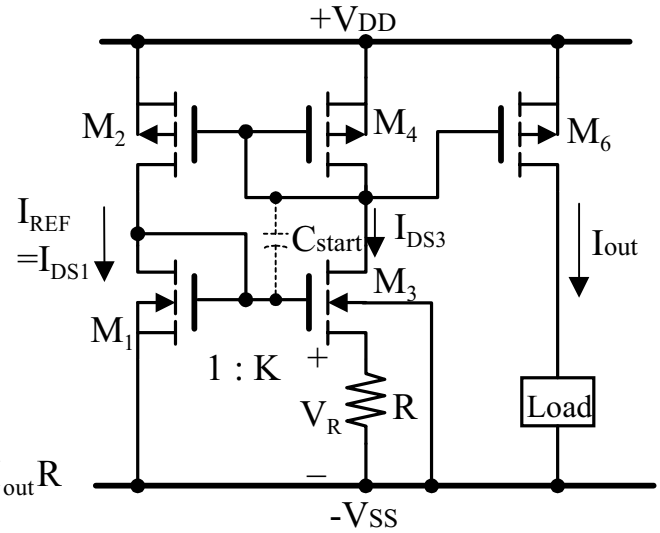
$$I_R = V_R/R$$

$I_{out}=[(W/L)_6/(W/L)_4]I_R$

* The output current is power-supply independent.
* Since I_R is small enough, the start-up circuit is not necessary.
* R may be implemented by n^+ diffusion or adjustable resistors.
* Process variations on R should be considered.
* The temperature coefficient of R is usually positive. Thus I_R is not linearly proportional to temperature exactly.

§ 3-2.3 Constant – g_m Current Source

All MOS devices are operated in the saturation region



$V_{GS1}=V_{GS3}+I_{D3}R$

$I_{REF}=I_{DS1}=I_{out}$

$I_{DS3}=KI_{DS1}$

$$\sqrt{\frac{2I_{out}}{\mu_n C_{ox} K(W/L)_1}} + V_{TH1}$$

$$= \sqrt{\frac{2I_{out}}{\mu_n C_{ox} K(W/L)_1}} + V_{TH3} + I_{out}R$$

$$I_{out} = \frac{2}{\mu_n C_{ox}(W/L)_1}\frac{1}{R^2}\left(1-\frac{1}{\sqrt{K}}\right)^2 - \left(\frac{2\Delta V_{TH}}{R} + \frac{\Delta V_{TH}^{\ 2}}{I_{out}R^2}\right)$$

$$\cong \frac{2}{\mu_n C_{ox}(W/L)_1}\frac{1}{R^2}\left(1-\frac{1}{\sqrt{K}}\right)^2 \qquad \text{If } \Delta V_{TH} \text{ is small}$$

$$g_{mload} = \sqrt{2\mu_n C_{ox}(W/L)_{load} I_{D1}}$$

$$= \sqrt{\frac{(W/L)_{load}}{(W/L)_1}}\frac{2}{R}\left(1-\frac{1}{\sqrt{K}}\right)$$

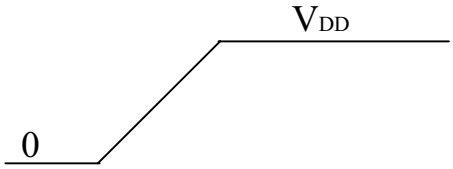
* The g_{mload} of the load NMOS device is independent of power supply voltages and depends upon R and channel geometric ratio.
* Both temperature coefficient and process variations of R still affect g_m.
* R can be tuned to compensate its process variation.
* R can be realized by switched-capacitor resistors for better accuracy and tunability. However, clocks and capacitors are required.
* ΔV_{TH} due to the body effect of M_3 causes error in I_{out}.
* R can be moved to the source of M_4 to avoid the body effect.

∵PMOS in 0.5μm CMOS process can have separate n-wells.

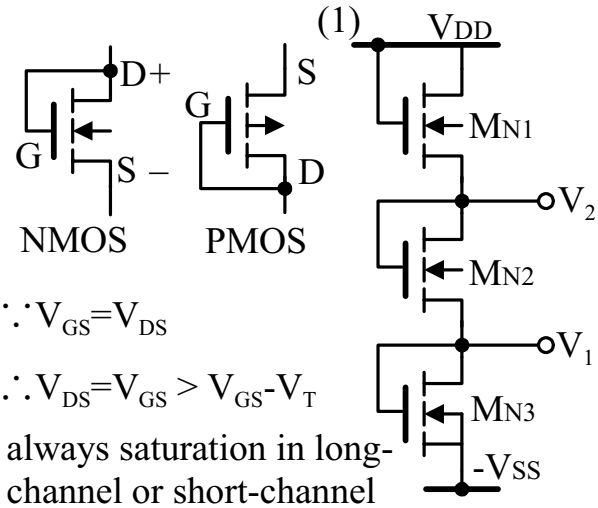
** Requires start-up circuit to stabilize the circuit as V_{DD}/V_{SS} is powered up. Adding C_{start} is a simple way to perform start-up.

* Requires careful HSPICE simulation and analysis for the start-up circuit.

Transient analysis using the ramp V_{DD} waveform.



§3-3 Simple MOS Voltage Sources (For capacitive loads only)



∵$V_{GS}=V_{DS}$

∴$V_{DS}=V_{GS} > V_{GS}-V_T$

always saturation in long-channel or short-channel devices

(2) PMOS version

* For 0.5μm CMOS technology all subtrates are the same p-type semiconductor connected to ground or $-V_{SS}$.

⇒ Body effect in M_{N1} and M_{N2}

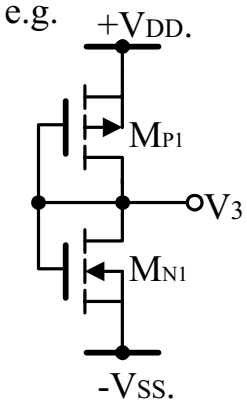
* For PMOS version, separate n-wells can be used.

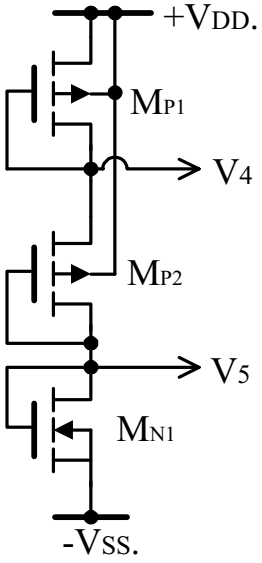
⇒ No body effect, but larger chip area.

* $V_{DD}+V_{SS} > V_{THMN1}+V_{THMN3}+V_{THMN2}$
* $I_{VDD}=I_{VSS} \propto V_{DD}+V_{SS}$
* M_{N1}, M_{N2}, and M_{N3} may have different channel dimensions.
* Output resistance $\propto 1/g_m$

(3) NMOS-PMOS combinations

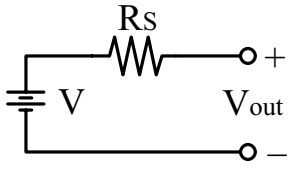
e.g.





Ideal Voltage Source : (1) Rs = 0

(2) Vout =V = constant
independent of
current loading.

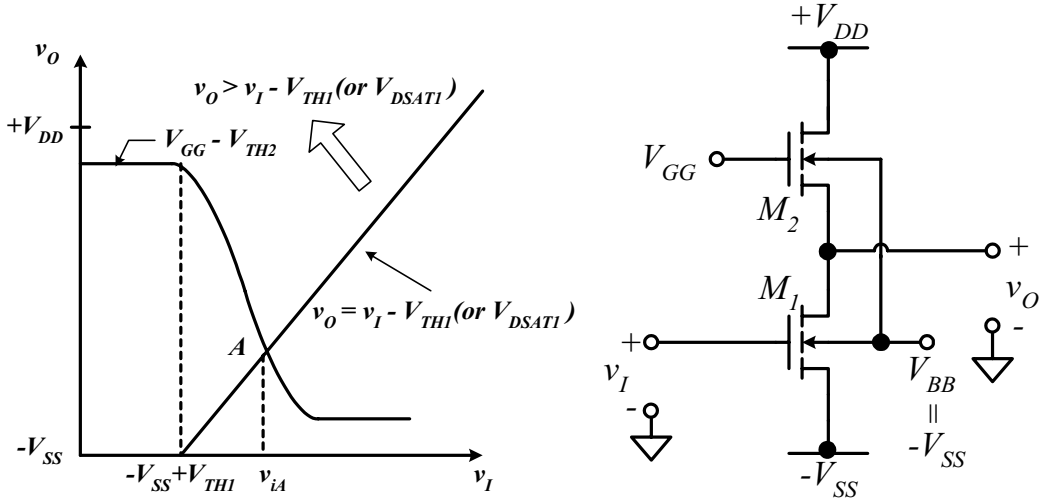


Chapter 4 CMOS Amplifiers, Level Shifting Circuits, and Output stages

4-1 Active-Load MOS Amplifiers

4-1.1 NMOS Amplifiers

1. Simple NMOS common-source amplifier



* M_1 and M_2 must be always biased in the saturation region.

* M_1 sat $\Rightarrow \; v_O \geq V_{DSAT1} \leq v_I - V_{TH1}$

  M_2 sat $\Rightarrow \; V_{DD} - v_O \geq V_{DSAT2} \leq V_{GG} - V_{TH2} - v_O$

* $V_{GG} < V_{DD} + V_{TH2} \Rightarrow V_{GG} < V_{DD}$

Transfer characteristic:

Assume $\lambda \to 0$, $GAMMA \to 0$, and the same $\mu_n C_{ox}$

$$\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_1 (v_I + V_{SS} - V_{TH2})^m = \frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)_2 (V_{GG} - v_O - V_{TH2})^m, 1 \leq m \leq 2$$

$$\Rightarrow v_O = V_{GG} - \left(\frac{(W/L)_1}{(W/L)_2}\right)^{\frac{1}{m}} (v_I + V_{SS} - V_{TH1}) - V_{TH2}$$

$V_{ODC} \propto V_{IDC}$

At point A , $v_{IA} = v_{OA} + V_{TH1}$

$$\Rightarrow v_{OA} = \frac{\left(V_{GG} - V_{TH2} - \left(\frac{(W/L)_1}{(W/L)_2} \right)^{\frac{1}{m}} V_{SS} \right)}{1 + \left(\frac{(W/L)_1}{(W/L)_2} \right)^{\frac{1}{m}}}$$

The range of v_O in which both MOS are in the saturation region is

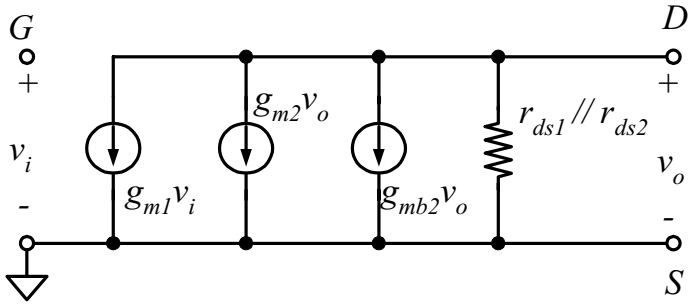
$$V_{GG} - V_{TH2} > v_O \geq \frac{\left(V_{GG} - V_{TH2} - \left(\frac{(W/L)_1}{(W/L)_2} \right)^{\frac{1}{m}} V_{SS} \right)}{1 + \left(\frac{(W/L)_1}{(W/L)_2} \right)^{\frac{1}{m}}} \text{ or } V_{DSAT1}$$

$$A_v \equiv \frac{\partial v_O}{\partial v_I} = -\left(\frac{(W/L)_1}{(W/L)_2} \right)^{\frac{1}{m}} \quad , \quad (W/L)_2 < 1 \text{ for high } A_v$$

The range for v_I is

$$-V_{SS} + V_{TH1} \leq v_I \leq \frac{\left(V_{GG} - V_{TH2} - \left(\frac{(W/L)_1}{(W/L)_2} \right)^{\frac{1}{m}} V_{SS} \right)}{1 + \left(\frac{(W/L)_1}{(W/L)_2} \right)^{\frac{1}{m}}} + V_{TH1} \text{ (or } v_{IA})$$

Small-signal model:



$$A_v \equiv \frac{v_o}{v_I} = -\frac{g_{m1}}{g_{m2} + g_{mb2} + \frac{1}{r_{ds1} || r_{ds2}}} \approx -\frac{g_{m1}}{g_{m2} + g_{mb2}}$$

if $(g_{m2} + g_{mb2}) >> \frac{1}{r_{ds1} || r_{ds2}}$

$$A_v = -\frac{g_{m1}}{g_{m2}} \cdot \frac{1}{1 + \eta_2} = -\alpha_2 \frac{g_{m1}}{g_{m2}}$$

where $\eta_2 = \dfrac{GAMMA_2}{2\sqrt{V_{BB} + v_O + \phi_S}}$ $\qquad \alpha_2 \equiv \dfrac{1}{1+\eta_2}$

$g_m = 2\sqrt{\dfrac{\mu_n C_{ox}}{2}\left(\dfrac{W}{L}\right)\cdot I_{DS}}$ or $m\left(\dfrac{\mu_n C_{ox}}{2}\cdot\dfrac{W}{L}\cdot {I_{DS}}^{m-1}\right)^{\frac{1}{m}}$

$\Rightarrow A_v = -\alpha_2\sqrt{(W/L)_1 \big/ (W/L)_2}$ or $-\alpha_2[(W/L)_1 \big/ (W/L)_2]^{\frac{1}{m}}, \quad 1 < m < 2$

If $\eta_2 << 0$, $\alpha_2 = 1$. ($GAMMA_2 \downarrow$, $V_{BB} + v_O \uparrow \Rightarrow \eta_2 \downarrow$)

$\Rightarrow A_v = -\sqrt{(W/L)_1 \big/ (W/L)_2}$ or $\left[-(W/L)_1 \big/ (W/L)_2\right]^{\frac{1}{m}}$

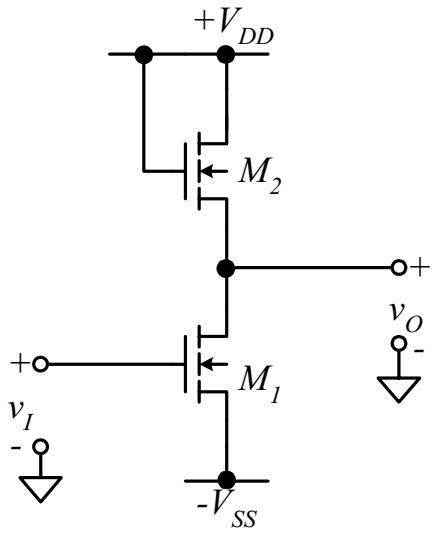
* The voltage gain is determined by the geometeric ratio.

  Example: $(W/L)_1 = 10 \quad (W/L)_2 = 0.1 \quad \alpha_2 = 1$

  $\Rightarrow A_v = -\sqrt{100} = -10$

* The body effect of M_2 degrades the voltage gain.
* The dc output voltage is dependent on the input dc bias voltage or equivalently the dc operating current.

2. NMOS inverter without V_{GG}



Amplifier range:

$$V_{DD} - V_{TH2} > v_O \geq \frac{\left(V_{DD} - V_{TH2} - \left(\dfrac{(W/L)_1}{(W/L)_2}\right)^{\frac{1}{m}} V_{SS}\right)}{1 + \left(\dfrac{(W/L)_1}{(W/L)_2}\right)^{\frac{1}{m}}} \quad \text{or } V_{DSAT1}$$

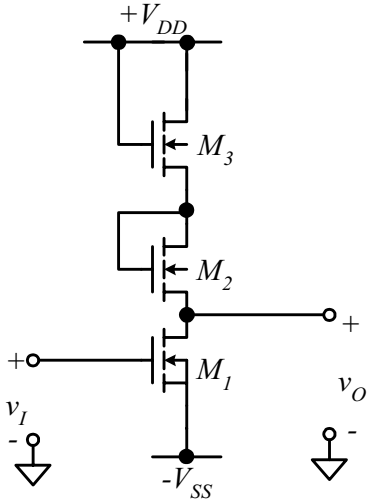
$$-V_{SS}+V_{TH1}\le v_I\le \frac{\left(V_{DD}-V_{TH2}-\left(\frac{(W/L)_1}{(W/L)_2}\right)^{\frac{1}{m}}V_{SS}\right)}{1+\left(\frac{(W/L)_1}{(W/L)_2}\right)^{\frac{1}{m}}}+V_{TH1}$$ or v_{IA}

$$V_{ODC}=V_{DD}-\left(\frac{(W/L)_1}{(W/L)_2}\right)^{\frac{1}{m}}(V_{IDC}+V_{SS}-V_{TH1})-V_{TH2}$$

* No extra power supply V_{GG} is required.

* $A_v=-\alpha_2\left(\frac{(W/L)_1}{(W/L)_2}\right)^{\frac{1}{m}}\Rightarrow (W/L)_2<1$ for high A_v

3. Split-Load inverter



Single M_2 $\Rightarrow (W/L)_2<<1$ very long channel device

$$C_{gs2}=\frac{2}{3}C_{ox}(L\cdot W)_2=\frac{2}{3}C_{ox}\frac{W^2}{(W/L)_2}$$

$$(W/L)_2<<1\Rightarrow C_{gs2}\uparrow$$

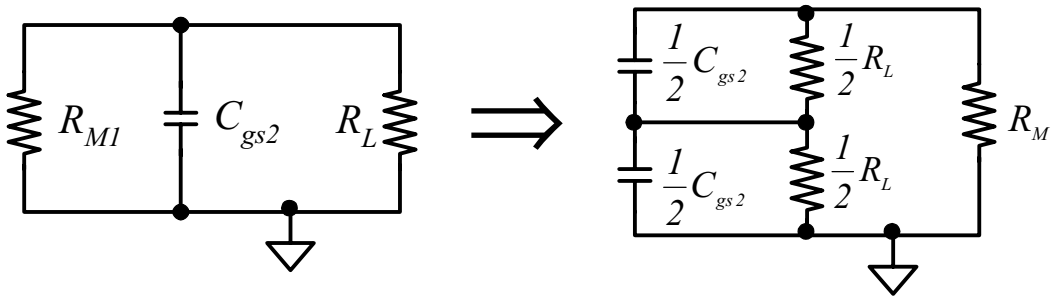
$$f_{-3dB}\approx\frac{1}{2\pi\frac{1}{g_{m2}}C_{gs2}}=\frac{3I_{DS}{}^2}{2\pi\frac{\mu_nC_{ox}}{2}W^2C_{ox}(V_{GS2}-V_{TH2})^3}$$

$$I_{DS}\uparrow\Rightarrow f_{-3dB}\uparrow\ ;\ C_{gs2}\uparrow\Rightarrow f_{-3dB}\downarrow$$

$\Rightarrow$ Split load

(1) RC time constant $\downarrow$ $\quad f_{-3dB} \uparrow$

(2) Gain is nearly unchanged



$$C_{gs2}(R_L \,//\, R_{M1}) \cong R_L C_{gs2}$$

$$\frac{1}{2}C_{gs2}[\frac{1}{2}R_L \,//(\frac{1}{2}R_L + R_{M1})] + \frac{1}{2}C_{gs2}[\frac{1}{2}R_L \,//(\frac{1}{2}R_L + R_{M1})] \cong \frac{1}{2}R_L C_{gs2}$$

4. NMOS Cascode amplifier

If $I_{DS1} = I_{DS2}$

$$A_{v1} \equiv \frac{v_{D1}}{v_I} = -\alpha_2 \frac{g_{m1}}{g_{m2}} = -\alpha_2 \left[\frac{(W/L)_1}{(W/L)_2}\right]^{1/m}$$

If $I_{DS1} = I_{DS3}$

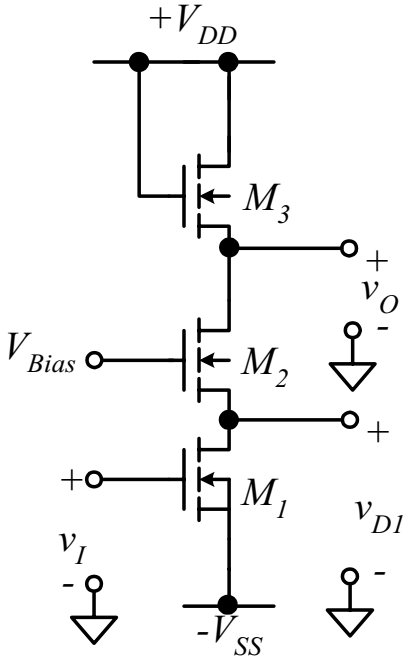
$$A_v \equiv \frac{v_O}{v_I} = -\alpha_3 \frac{g_{m1}}{g_{m3}} = -\alpha_3 \left[\frac{(W/L)_1}{(W/L)_3}\right]^{1/m}$$

$$C_{in} = C_{gs1} + C_{gd1}\left(1 + \frac{g_{m1}}{g_{m2}}\right)$$

If $g_{m1} = g_{m2}$

$\Rightarrow C_{in} = C_{gs1} + 2C_{gd1}$

$C_{in} \propto g_{m1}/g_{m2}$



* Design considerations:

(1) $\left(W/L\right)_1 = \left(W/L\right)_2 \Rightarrow g_{m1} = g_{m2}$ (Neglecting the body effect of M_2)

Keep C_{in} Small , Miller Effect $\downarrow$

(2) $\left(W/L\right)_3 << \left(W/L\right)_1 \Rightarrow g_{m3} << g_{m1}$, Voltage gain $A_v \uparrow$

(3) $V_{DS2}(V_{DS1})$ must be large enough to keep $M_2(M_1)$ sat.

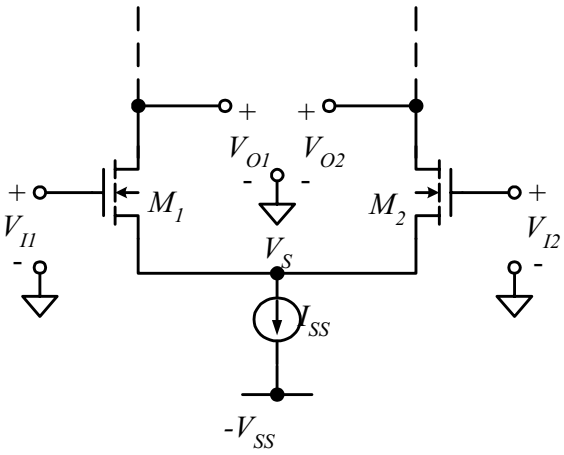
* $g_{m1} < g_{m2} \Rightarrow A_{v1} < 1 \Rightarrow$ Smaller Miller effect

But $\left(W/L\right)_1 < \left(W/L\right)_2$ is not recommended.

$\because$ V_{DS1} will become smaller $\Rightarrow M_1$ may not be in the sat. region.

* $\left(W/L\right)_2 > \left(W/L\right)_1$ slightly to compensate the body effect of M_2 .

5. MOS source-couple pair



$$I_{DS1} = \left(\frac{\mu_n C_{ox}}{2}\right)_1 \left(\frac{W}{L}\right)_1 (V_{GS1} - V_{TH1})^2$$

$$I_{DS2} = \left(\frac{\mu_n C_{ox}}{2}\right)_2 \left(\frac{W}{L}\right)_2 (V_{GS2} - V_{TH2})^2$$

$$I_{DS1} + I_{DS2} = I_{SS}$$

$$V_{GS1} = V_{I1} - V_S$$

$$V_{GS2} = V_{I2} - V_S$$

Assume identical devices

i.e. $V_{TH1} = V_{TH2}, \left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$ and $\left(\frac{\mu_n C_{ox}}{2}\right)_1 = \left(\frac{\mu_n C_{ox}}{2}\right)_2 = \frac{\mu_n C_{ox}}{2}$

$$\Rightarrow \Delta I_{DS} \equiv I_{Ds1} - I_{DS2} = \frac{\mu_n C_{OX}}{2}\frac{W}{L}(\Delta V_I)\sqrt{\frac{2I_{SS}}{\frac{\mu_n C_{OX}}{2}\frac{W}{L}} - (\Delta V_I)^2}$$

where $\Delta V_I \equiv V_{I1} - V_{I2}$ (input differential voltage)

If $\Delta V_I \le \sqrt{\frac{I_{SS}}{\frac{\mu_n C_{OX}}{2}\frac{W}{L}}}$

$\Rightarrow \Delta I_D \propto \Delta V_I$, linear range

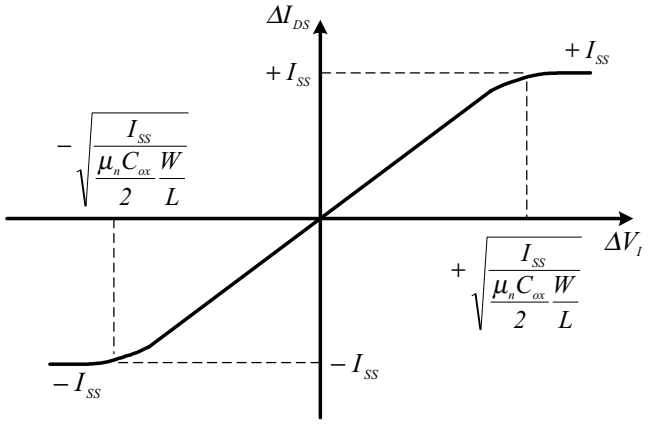
$\Rightarrow$ between $+\frac{I_{SS}}{2}$ and $-\frac{I_{SS}}{2}$.

Linear range $\propto \sqrt{I_{SS}}, \frac{L}{W}$

Typically, $\Delta V_I \approx \pm 300mv$ to

$\pm V$ in the linear range,

Larger than that of the emitter-couple pair.



$$G_m \equiv \left.\frac{\partial \Delta I_{DS}}{\partial \Delta V_I}\right|_{\Delta V_I=0} = \left(\frac{\mu_n C_{OX}}{2}\frac{W}{L}\right)\sqrt{\frac{2I_{SS}}{\frac{\mu_n C_{OX}}{2}\frac{W}{L}} - (\Delta V_I)^2} - \frac{\mu_n C_{OX}}{2}\left(\frac{W}{L}\right)\Delta V_I$$

$$\left.\frac{\Delta V_I}{\sqrt{\frac{2I_{SS}}{\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)} - (\Delta V_I)^2}}\right|_{\Delta V_I=0}$$

$$= 2\sqrt{\frac{I_{SS}}{2}\frac{\mu_n C_{ox}}{2}\left(\frac{W}{L}\right)} = g_{m1} \text{ or } g_{m2}$$

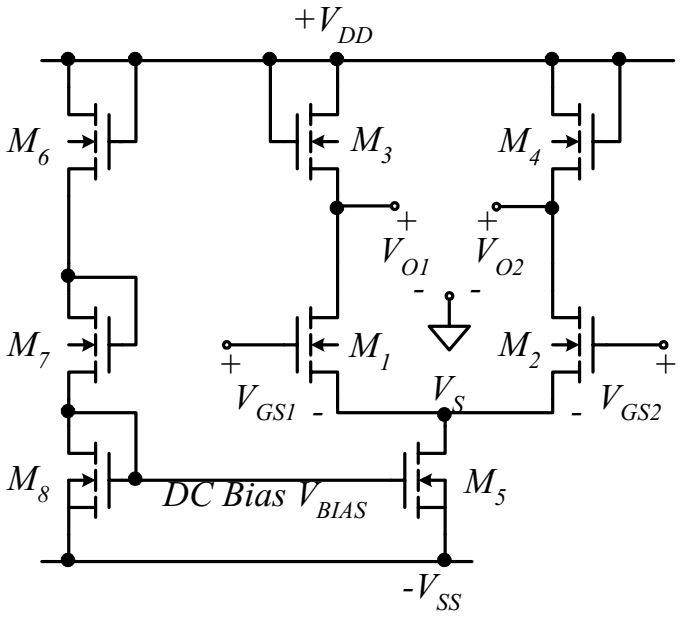
$$= \sqrt{I_{SS}(\mu_n C_{ox})\left(\frac{W}{L}\right)}$$

* Gm is the differential output transconductance

Gm at $\Delta V_I=0$ is the maximum.

* If operated in the subthreshold region, Gm max = g_{m1} or $g_{m2}=\frac{I_{DS}}{nv_t}$

6. NMOS differential stage



DC considerations :

(1) Transfer characteristic :

$(W/L)_1=(W/L)_2$ $(W/L)_3=(W/L)_4$

Source-coupled pair M_1 and M_2

$$\Rightarrow \Delta I_{DS} \equiv I_{DS1} - I_{DS2} = (\frac{\mu_n C_{ox}}{2}\frac{W}{L})_1(\Delta V_I)\sqrt{\frac{2I_{SS}}{(\frac{\mu_n C_{ox}}{2}\frac{W}{L})_1} - (\Delta V_I)^2}$$

where $\Delta V_I \equiv V_{I1} - V_{I2}$

$$I_{DS3} = I_{DS1} = \frac{\mu_n C_{ox}}{2}(\frac{W}{L})_3(V_{DD} - V_{O1} - V_{TH3})^2$$

$$I_{DS4} = I_{DS2} = \frac{\mu_n C_{ox}}{2}(\frac{W}{L})_3(V_{DD} - V_{O2} - V_{TH4})^2$$

$$V_{O1} = V_{DD} - V_{TH3} - \sqrt{\frac{I_{DS1}}{\frac{\mu_n C_{ox}}{2}(\frac{W}{L})_3}} \qquad V_{O2} = V_{DD} - V_{TH4} - \sqrt{\frac{I_{DS2}}{\frac{\mu_n C_{ox}}{2}(\frac{W}{L})_3}}$$

$$\Delta V_O \equiv V_{O1} - V_{O2} = V_{TH4} + \sqrt{\frac{I_{DS2}}{\frac{\mu_n C_{ox}}{2}(\frac{W}{L})_3}} - V_{TH3} - \sqrt{\frac{I_{DS1}}{\frac{\mu_n C_{ox}}{2}(\frac{W}{L})_3}}$$

$$= (V_{TH4} - V_{TH3}) + \frac{1}{\sqrt{\frac{\mu_n C_{ox}}{2}(\frac{W}{L})_3}}(\sqrt{\frac{I_{SS}}{2} - \frac{\Delta I_{DS}}{2}} - \sqrt{\frac{I_{SS}}{2} + \frac{\Delta I_{DS}}{2}})$$

$$= f(I_{SS}, \Delta V_I)$$

$\Rightarrow \Delta V_O$ *vs* ΔV_I is the voltage transfer characteristic.

(2) Input voltage limits :

Positive maximum common-mode voltage V_{ICM}^+

$$V_{ICM}^+ = V_{O1} + V_{TH1} = V_{DD} - V_{TH3} - \sqrt{\frac{I_{SS}/2}{(\mu_n C_{ox}/2)(W/L)_3}} + V_{TH1}$$

(long-channel device)

V_{ICM}^+ such that V_{O1}-V_S=V_{DSAT1} (short-channel device)
(M1 and M2 sat.)

Negative maximum common-mode voltage V_{ICM}^-

M5 must be sat.

$$V_{ICM}^{-} = V_{BIAS} + V_{TH5} + \sqrt{\frac{I_{SS}/2}{(\mu_n C_{ox}/2)(W/L)_1}} + V_{TH1}$$

(long-channel device)

V_{ICM}^{-} such that $V_S+V_{SS}=V_{DSAT5}$ (short-channel device)

Positive maximum differential voltage V_{ID}^{+}

$$V_{ID}^{+} = V_{DD} - V_{TH3} + \sqrt{\frac{I_{SS}}{(\mu_n C_{ox}/2)(W/L)_3}} + V_{TH1}$$ (long-channel device)

V_{ID}^{+} such that $V_{O1}-V_S=V_{DSAT1}$ (short –channel device)

(Keep M1 or M2 sat.)

Negative maximum differential voltage V_{ID}^{-}

$V_{ID}=-V_{ID}^{+}$

(3) Input offset voltage

$$V_{OS} \equiv V_{GS1} - V_{GS2}\Big|_{V = V_2}$$

$$= \sqrt{\frac{I_{DS1}}{(\mu_n C_{ox}/2)_1(W/L)_1}} + V_{TH1} - \sqrt{\frac{I_{DS2}}{(\mu_n C_{ox}/2)_2(W/L)_2}} - V_{TH2}$$

$$V_{O1} = V_{O2} = V_O = V_{DD} - V_{TH3} - \sqrt{\frac{I_{DS1}}{(\mu_n C_{ox}/2)_3(W/L)_3}}$$

$$= V_{DD} - V_{TH4} - \sqrt{\frac{I_{DS1}}{(\mu_n C_{ox}/2)_4(W/L)_4}}$$

$$\Rightarrow \sqrt{I_{DS1}} = \sqrt{(\mu_n C_{ox}/2)_3(W/L)_3}(V_{DD} - V_{TH3} - V_O)$$

$$\sqrt{I_{DS2}} = \sqrt{(\mu_n C_{ox}/2)_4(W/L)_4}(V_{DD} - V_{TH4} - V_O)$$

$$\Rightarrow V_{OS}=\sqrt{\frac{\left(\frac{\mu_n C_{OX}}{2}\right)_3\left(\frac{W}{L}\right)_3}{\left(\frac{\mu_n C_{OX}}{2}\right)_1\left(\frac{W}{L}\right)_1}}(V_{DD}-V_O-V_{TH3})$$

$$-\sqrt{\frac{\left(\frac{\mu_n C_{OX}}{2}\right)_4\left(\frac{W}{L}\right)_4}{\left(\frac{\mu_n C_{OX}}{2}\right)_2\left(\frac{W}{L}\right)_2}}(V_{DD}-V_O-V_{TH4})+(V_{TH1}-V_{TH2})$$

Define $\Delta X_2 = X - X_2 \qquad X_2 = -X + X_2)$

$$\Rightarrow X_1 = X_{12}+\frac{\Delta X_{12}}{2} \qquad X_2 = X_{12}-\frac{\Delta X_{12}}{2}$$

$$\Rightarrow V_{OS}=\sqrt{\frac{\left(\frac{\mu_n C_{OX}}{2}\right)_{34}\left(\frac{W}{L}\right)_{34}}{\left(\frac{\mu_n C_{OX}}{2}\right)_{12}\left(\frac{W}{L}\right)_{12}}}(V_{DD}-V_O-V_{TH34})[\frac{\Delta\left(\frac{\mu_n C_{OX}}{2}\right)_{34}}{2\left(\frac{\mu_n C_{OX}}{2}\right)_{34}}+\frac{\Delta\left(\frac{W}{L}\right)_{34}}{2\left(\frac{W}{L}\right)_{34}}$$

$$-\frac{\Delta\left(\frac{\mu_n C_{OX}}{2}\right)_{12}}{2\left(\frac{\mu_n C_{OX}}{2}\right)_{12}}-\frac{\Delta\left(\frac{W}{L}\right)_{12}}{2\left(\frac{W}{L}\right)_{12}}-\frac{\Delta V_{TH34}}{V_{DD}-V_O-V_{TH34}}]+\Delta V_{TH12}$$

$$=\sqrt{\frac{I_{DS34}}{(\frac{\mu_n C_{ox}}{2})_{12}(\frac{W}{L})_{12}}}\left[\frac{\Delta(\frac{\mu_n C_{ox}}{2})_{34}}{2(\frac{\mu_n C_{ox}}{2})_{34}}-\frac{\Delta L_{34}}{2L_{34}}+\frac{\Delta W_{34}}{2W_{34}}-\frac{\Delta(\frac{\mu_n C_{ox}}{2})_{12}}{2(\frac{\mu_n C_{ox}}{2})_{12}}-\frac{\Delta W_{12}}{2W_{12}}+\frac{\Delta L_{12}}{2L_{12}}\right]$$

$$-\sqrt{\frac{\left(\frac{\mu_n C_{OX}}{2}\right)_{34}\left(\frac{W}{L}\right)_{34}}{\left(\frac{\mu_n C_{OX}}{2}\right)_{12}\left(\frac{W}{L}\right)_{12}}}\Delta V_{TH34}+\Delta V_{TH12}$$

$$\cong\sqrt{\frac{I_{DS34}}{(\frac{\mu_n C_{ox}}{2})_{12}(\frac{W}{L})_{12}}}\left[\frac{\Delta W_{34}}{2W_{34}}+\frac{\Delta L_{12}}{2L_{12}}\right]+\Delta V_{TH12}-\sqrt{\frac{(\frac{\mu_n C_{ox}}{2})_{34}(\frac{W}{L})_{34}}{(\frac{\mu_n C_{ox}}{2})_{12}(\frac{W}{L})_{12}}}\Delta V_{TH34}$$

$$=\Delta V_{TH12}+(V_{GS12}-V_{TH12})\left[\frac{\Delta W_{34}}{2W_{34}}+\frac{\Delta L_{12}}{2L_{12}}\right]-\sqrt{\frac{(\frac{W}{L})_{34}}{(\frac{W}{L})_{12}}}\Delta V_{TH34}$$

* If ΔV_{TH} is large and the differential gain is high,

$V_{OS} \cong \Delta V_{TH12}$

* If $\frac{\Delta W}{2W}$ and $\frac{\Delta L}{2L}$ is large , keep $V_{GS12} - V_{TH12}$ small.

$$\Rightarrow V_{OS} \cong (V_{GS} - V_{TH12})(\frac{\Delta W_{34}}{2W_{34}} + \frac{\Delta L_{12}}{2L_{12}})$$

$V_{OS} \propto$ input overdrive voltage

* If operated in the subthreshold region,

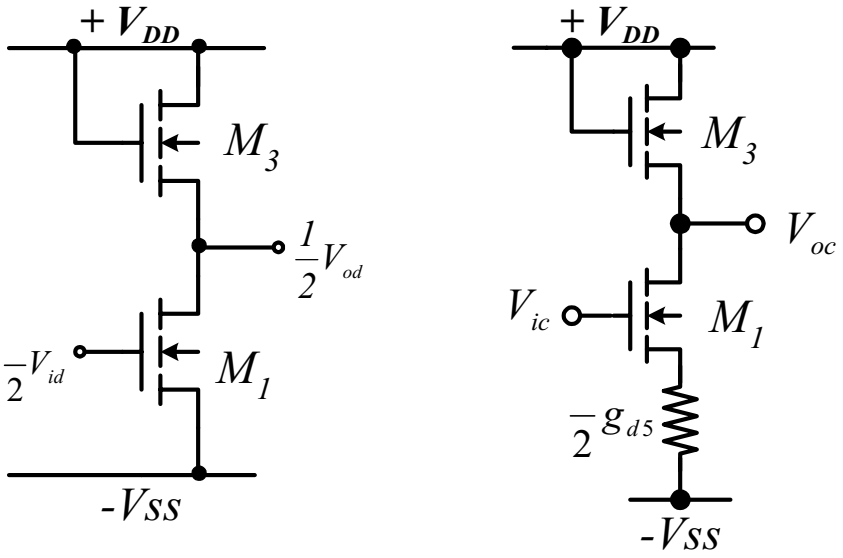
$$I_{DS} \propto exp(\frac{V_{GS}}{nv_t})$$

V_{OS} is smaller than that operated in the saturation region.

This case is similar to the BJT case. $\because V_{OS} \propto \Delta I_{DS}$)

(3) AC Gain

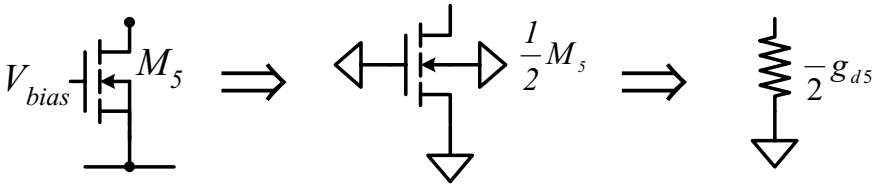
Differential signal *Common-mode signal*



Half-Circuit concept:

$$A_{dm} \equiv \frac{v_{od}}{v_{id}} = -\alpha_3 \frac{g_{m1}}{g_{m3}}$$

Common-mode half-circuit:



$$A_{cm} \equiv \frac{v_{oc}}{v_{ic}} = -\alpha_1\alpha_3 \frac{g_{d5}}{2g_{m3}}$$

$$CMRR \equiv \frac{A_{dm}}{A_{cm}} = \frac{2g_{m1}}{g_d\ \alpha_1}$$

* $L_5 \uparrow \Rightarrow g_{d5} \downarrow \Rightarrow CMRR \uparrow$

* When cascoded current source is used for Iss, $_{d5} \downarrow \Rightarrow CMRR \uparrow$

But $Vs \uparrow \Rightarrow$ common-mode range $\downarrow$

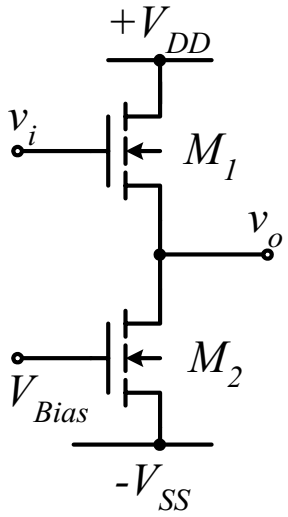
7. NMOS source follower

The voltage gain (midband) is

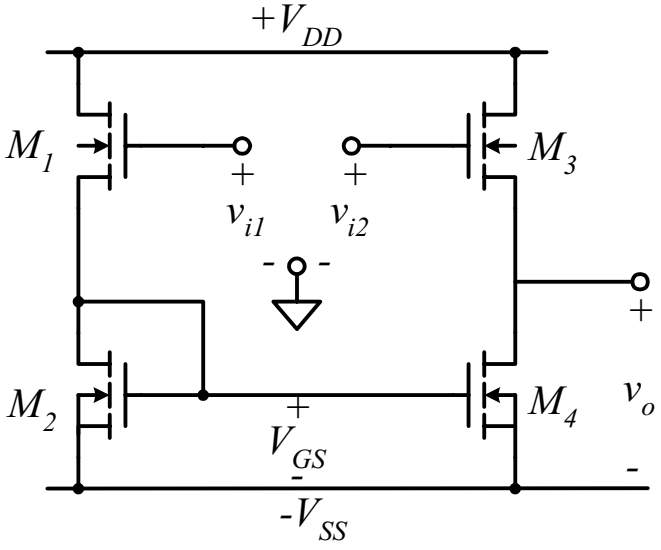
$$A_v = \frac{g_{m1}}{\frac{g_{m1}}{\alpha_1} + \frac{1}{r_{ds1}} + \frac{1}{r_{ds2}}} < 1$$

If $r_{ds1}\ , r_{ds1} >> \frac{\alpha_1}{g_{m1}}$

$\Rightarrow A_v \cong \alpha_1 < 1$, smaller than that of the emitter follower.



8. NMOS differential-input to single-ended converter



$$A_v = \frac{N+1}{2} = \frac{\alpha_3}{1+\frac{\alpha_3}{g_{m3}}(\frac{1}{r_{ds3}}+\frac{1}{r_{ds4}})} (= \frac{v_o}{(v_{i1}-v_{i2})})$$

where $N = \dfrac{g_{m1}g_{m4}}{g_{m3}(\frac{g_{m1}}{\alpha_1}+g_{m2}+\frac{1}{r_{ds1}}+\frac{1}{r_{ds2}})}$

If $M_2 \equiv M_4$, $M_3 \equiv M_1$, $\dfrac{1}{r_{ds}} << g_m$

$\Rightarrow$ $g_{m2} = g_{m4}$, $g_{m3} = g_{m1}$

$$N \cong \frac{g_{m4}}{g_{m4}+g_{m3}/\alpha_3}$$

$$A_v \cong \alpha_3 \frac{2g_{m4}+g_{m3}/\alpha_3}{2g_{m4}+2g_{m3}/\alpha_3} < 1$$

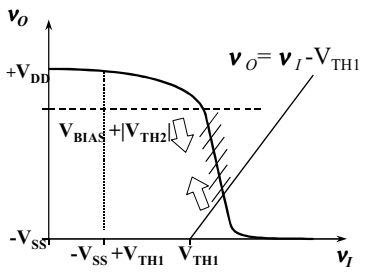
$$CMRR = \frac{1+N}{2(1-N)} = \frac{1}{2}+\frac{g_{m4}}{g_{m3}/\alpha_3}$$

To obtain a large CMRR , $g_{m4} >> g_{m3}/\alpha_3$

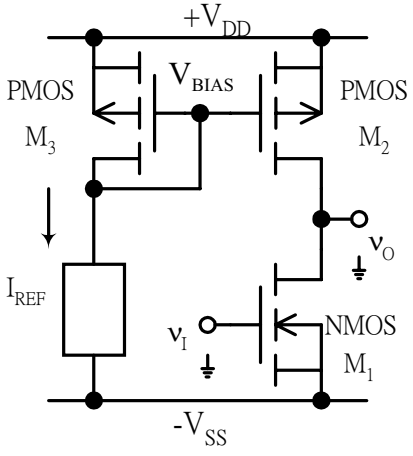
$$\Rightarrow A_v \cong \alpha_3 < 1$$

§ 4-1.2 CMOS Amplifier

1. Simple common-source amplifier



M_2 : PMOS current source



$$M_1 \text{ and } M_2 \text{ sat.} \Rightarrow V_{BIAS}+|V_{TH2}| > v_o > v_I - V_{TH1} \text{ or } V_{DD}-|V_{DSAT2}| \geq V_o \geq V_{DSAT1}-V_{SS}$$

$A_v = -g_{m1}(r_{ds1} // r_{ds2})$

$g_{m1} = \sqrt{2I_{DS1}\mu_n C_{ox}\left(\frac{W}{L}\right)_1}$, $r_{ds1} = \frac{1}{\lambda_1 I_{S1}}$ $r_2 = \frac{1}{\lambda_2 I_{S2}}$

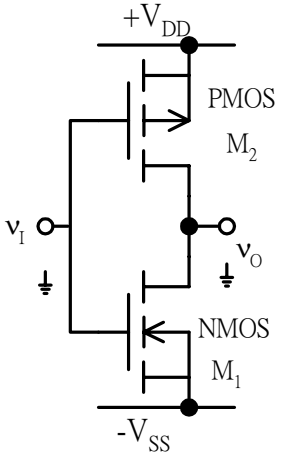
$\Rightarrow A = \frac{1}{\sqrt{I_{S1}}}\left(\frac{1}{\lambda_1 + \lambda_2}\right)\sqrt{2\mu C\left(\frac{W}{L}\right)_1}$

$|A_v| \propto \frac{1}{\sqrt{I_{DS1}}}$ (long-channel devices)

$|A_v| \propto (I_{DS1})^{-\frac{1}{m}}$ (short-channel devices)

Output resistance r_o $r_o = r_{ds1} // r_{ds2}$

2. Complementary CMOS common-source amplifier



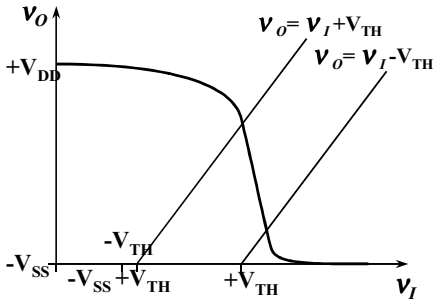
Assume $V_{TH1} = |V_{TH2}| = V_{TH}$

If $v_I - V_{TH} < v_o < v_I + V_{TH}$ or $V_{DD} - |V_{DSAT2}| \geq v_o \geq V_{DSAT1} - V_{SS}$

$\Rightarrow M_1$ and M_2 are saturated

$A_v = -(g_{m1} + g_{m2})(r_{ds1} // r_{ds2})$

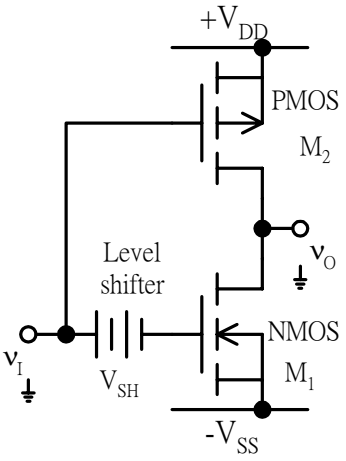
$r_o = r_{ds1} // r_{ds2}$



*Higher gain than the circuit in 1.

*Narrow operating range.

3. Complementary inverter with level shifter.



M_2 sat. $\Rightarrow V_{DD} - v_I - V_{TH} < V_{DD} - v_o$

M_1 sat. $\Rightarrow v_I - V_{SH} + V_{ss} - V_{TH} < v_o + V_{SS}$

$\Rightarrow v_I - V_{TH} - V_{SH} < v_o < v_I + V_{TH}$

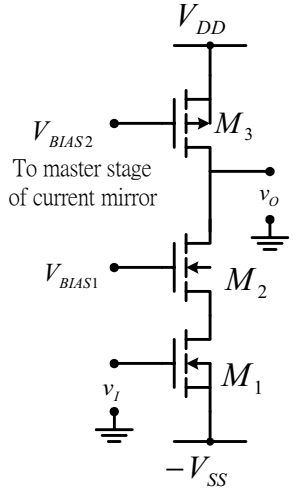
* $r_o = r_{ds1} // r_{ds2}$

* The range of v_o is increased by V_{SH}.

* In the short-channel case, $V_{GS1} \downarrow$ *by* V_{SH},

$V_{DSAT1} \downarrow \Rightarrow$ The range is also increased.

4. Cascode amplifier with PMOS current-source load



$$A_v = -g_{m1}[r_{ds3} \| (\frac{1}{\alpha_2} g_{m2} r_{ds1} r_{ds2})]$$

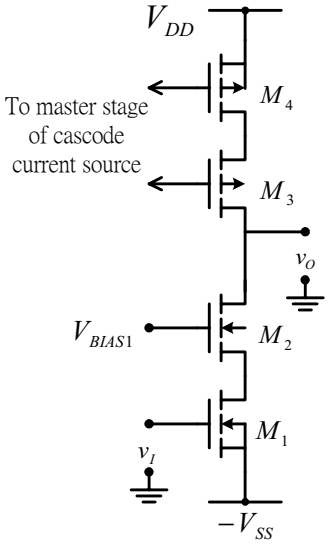
$$\cong -g_{m1} r_{ds3}$$

$$r_o = r_{ds3} \| (\frac{1}{\alpha_2} g_{m2} r_{ds1} r_{ds2})$$

$$\cong r_{ds3}$$

* PMOS devices can be used as cascode amplifier whereas NMOS device as current source.

5. Cascode amplifier with PMOS cascode current-source load



$$A_v = -g_{m1}[(\frac{1}{\alpha_3} g_{m3} r_{ds4} r_{ds3}) \| (\frac{1}{\alpha_2} g_{m2} r_{ds1} r_{ds2})]$$

$$\cong -\frac{1}{2\alpha} g_{m1} g_m r_{ds}^2$$

if $\alpha_3 = \alpha_2 = \alpha$

$g_{m3} = g_{m2} = g_m$

$r_{ds4} = r_{ds3} = r_{ds2} = r_{ds1} = r_{ds}$

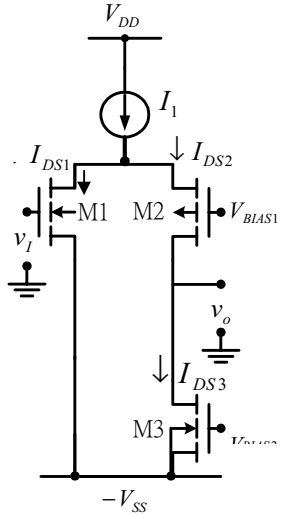
$$r_o \cong \frac{1}{2\alpha} g_m r_{ds}^2$$

* Larger r_o and A_v

* Limited output voltage swing

➔High-swing cascode current source is preferred

6. Folded cascode amplifier



M1: CS amplifier

M2: CG amplifier

Optimal operating point:

$$I_{DS1} = I_{DS2} = \frac{I_1}{2} = I_{DS3}$$

$g_{m1} = g_{m2}$

(to avoid large Miller capacitance at input)

$$A_v = -g_{m1}\{r_{ds3} \| [g_{m2}(r_{ds1} \| r_{dsI1}) r_{ds2}]\}$$

$$\cong -g_{m1} r_{ds3}$$

$r_o = r_{ds3} \| [g_{m2}(r_{ds1} \| r_{dsI1})r_{ds2}]$

* Nearly the same A_v and r_o can be achieved as the cascode amplifier
* Less devices in cascode at the input CS amplifier

➔M1 can be easily operated in the saturation region

7. Improved cascode amplifier with current injection circuitry

conventional cascode amplifier

$$A_v \cong -g_{m1}r_{ds3} \propto \frac{1}{\sqrt{I_{DS}}}$$

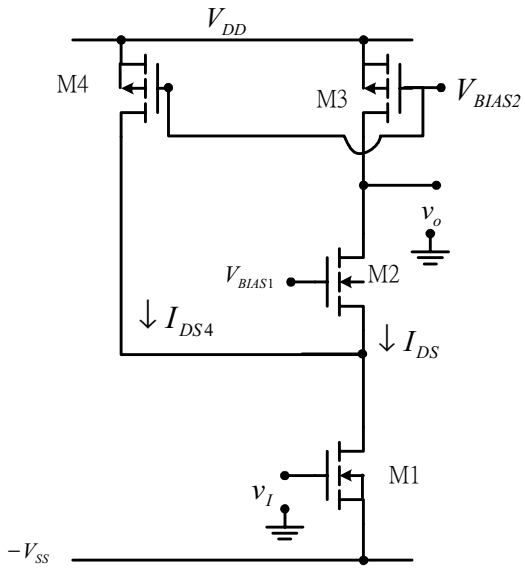
$I_{DS} \downarrow \Rightarrow A_v \uparrow$ until subthreshold

M3: current source as load

M4: current-injection current source

$$A_v \cong -g_{m1}r_{ds3} \propto \frac{\sqrt{I_{DS4}}}{\sqrt{I_{DS}}}$$

To increase A_v ➔ $I_{DS4} \uparrow$ and $I_{DS} \downarrow$



* Higher voltage gain and the same r_o
* Extra device M4 and extra power dissipation
* Firstly, design the circuit of M1, M2, and M3. Then add M4. Readjust the channel dimensions to keep the dc bias so that all devices are in saturation.

8. Differential amplifier with PMOS load

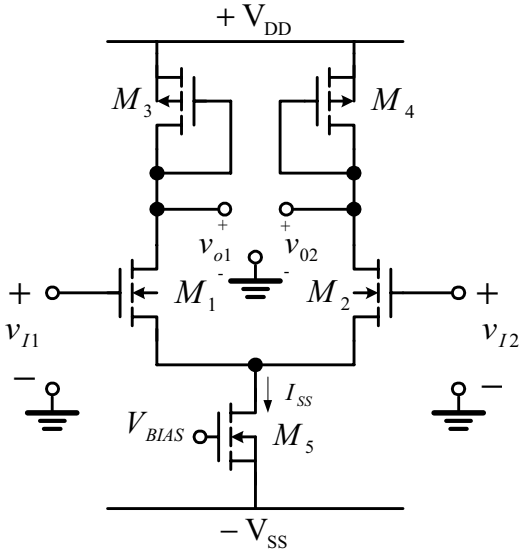
Half-circuit method can be used

$$v_{id} \equiv v_{I1} - v_{I2}\ ,\quad v_{ic} \equiv \frac{v_{I1} + v_{I2}}{2}$$

$$v_{od} \equiv v_{O1} - v_{O2}\ ,\quad v_{oc} \equiv \frac{v_{O1} + v_{O2}}{2}$$

$$A_{dm} \equiv \frac{v_{od}}{v_{id}} \cong -g_{m1}\frac{1}{g_{m3}}$$

$$A_{cm} \equiv \frac{v_{oc}}{v_{ic}} \cong -\alpha_1 \frac{g_{d5}}{2g_{m3}}$$



$$CMRR \equiv \left|\frac{A_{dm}}{A_{cm}}\right| \cong \frac{2g_{m1}}{g_{d5}\cdot\alpha_1}$$

$$r_{od} \cong \frac{1}{gm3}$$

$$r_{oc} \cong \frac{1}{gm3}$$

*Matched devices for M_1/M_2 and M_3/M_4

* $A_{cm} < 1$ can be achieved

9. Different amplifier with PMOS current-source load

M_3, M_4 :Two slave stages of the current mirror

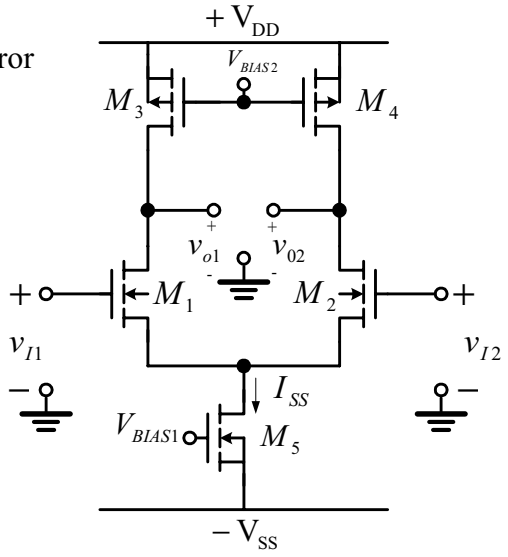
=> current-source load

$$A_{dm} \cong -g_{m1}\left(r_{ds1} \parallel r_{ds3}\right)$$

$$A_{cm} \cong -\frac{\alpha_1}{2r_{ds5}}\left(r_{ds3} \parallel g_{m1}r_{ds5}r_{ds1}\right)$$

$$CMRR \cong -\frac{2g_{m1}\left(r_{ds1} \parallel r_{ds3}\right)r_{ds5}}{\alpha_1 r_{ds3}}$$

* $g_{m1} \uparrow$, $r_{ds5} \uparrow$ => CMRR $\uparrow$



* $A_{cm} < 1$ is preferred => $r_{ds5} > r_{ds3}$

* I_{SS} can be realized by cascode or high-swing cascode current source to increase

$$r_{ds5}\left(=\frac{1}{g_{d5}}\right)$$

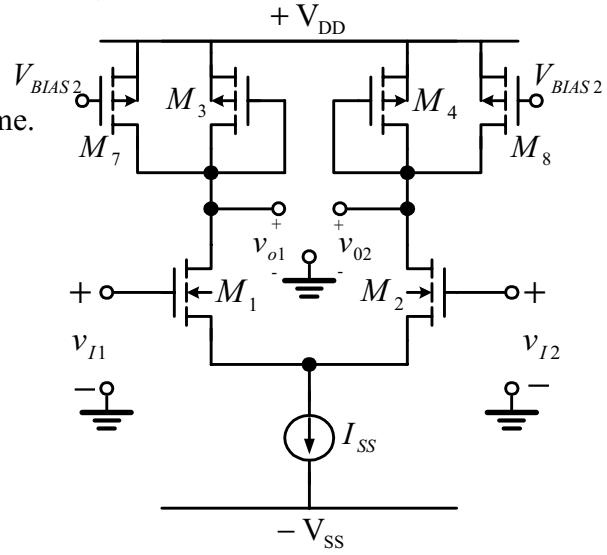
10. Differential amplifier with PMOS current injection circuit

If I_{SS} remains unchanged, gm1=gm2 the same.

But gm3=gm4 is reduced by $\frac{1}{\sqrt{2}}$ if

$I_{DS3} = I_{DS4}$ is reduced by half.

$\Rightarrow A_{dm} \uparrow$ by $\sqrt{2}$



$r_{ds7} = r_{ds8} >> \frac{1}{gm3} = \frac{1}{gm4}$

CMRR is the same.

* If M_3 and M_4 are current-source loads , could A_{dm} be increased? Why?

11. Differnetial cascode amplifier

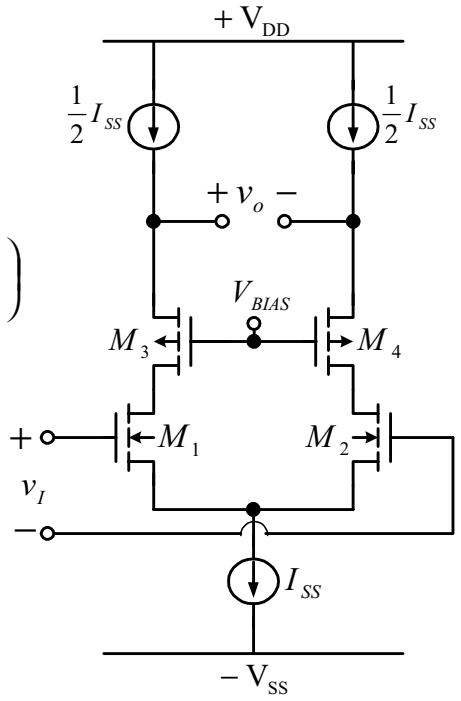
$v_O \equiv v_{O1} - v_{O2}$

$v_I \equiv v_{I1} - v_{I2}$

*Higher A_{dm}

*4 MOS devices stacked $\left(M_1, M_3, I_{SS}, \frac{1}{2} I_{SS}\right)$

$\Rightarrow V_{DD} + V_{SS}$ might not be enough to maintain all the devices in saturation when low supply voltage is used.



12. Differential Folded cascode amplifier

*To retain the characteristics of cascode amplifier, the optimal design is

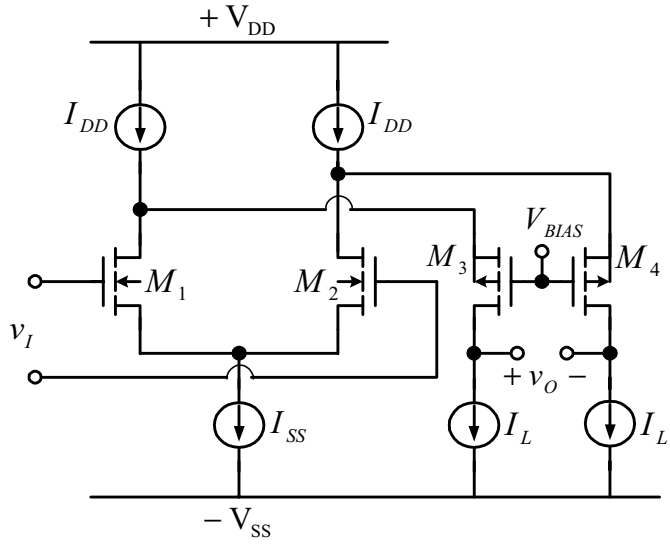
$I_{DD} = I_{SS}$

$I_L = \frac{1}{2} I_{SS}$

* Only 3 MOS devices stacked

=>low voltage operation is possible

* $V_{ICM} \uparrow$ why?



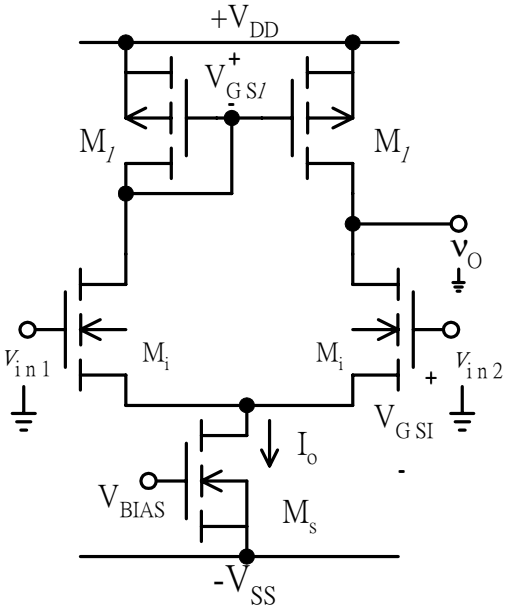
13. CMOS differential-input to single-ended-output converter.

Version I : NMOS input

DC operating point :

It is better to keep $V_{ODC} \cong V_{DD} - V_{GSI}$

for better current-mirror balance.



Common-mode range :

$$V_{ICM}+ = V_{DD} + V_{THN} - V_{GSI}$$

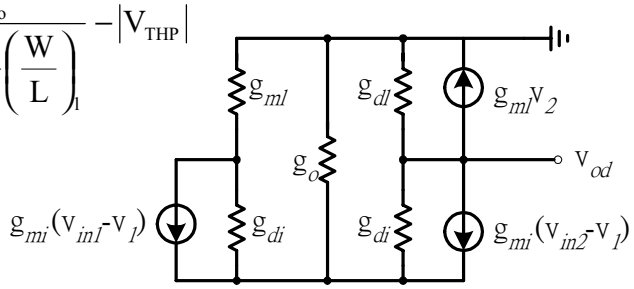
$$= V_{DD} + V_{THN} - \sqrt{\frac{I_o/2}{\frac{\mu_p C_{oxp}}{2}\left(\frac{W}{L}\right)_l}} - |V_{THP}|$$

$$V_{ICM}- = V_{GSI} + V_{BIAS} - V_{THN}$$

$$= \sqrt{\frac{I_o/2}{\frac{\mu_p C_{oxn}}{2}\left(\frac{W}{L}\right)_i}} + V_{BIAS}$$

Differential-mode range :

$$V_{Id}^{+} = -V_{Id}^{-} = V_{DD} + V_{THN} - \sqrt{\frac{I_o}{\frac{\mu_p C_{oxp}}{2}\left(\frac{W}{L}\right)_l}} - |V_{THP}|$$



$$v_{in1} = \frac{v_{id}}{2} + v_{ic}$$

$$v_{in2} = \frac{-v_{id}}{2} + v_{ic}$$

$\Rightarrow$ Exact A_{cm} and A_{dm} can be solved.

$$A_{dm} \approx \frac{g_{mi}}{g_{dl} + g_{di}} \qquad A_{cm} \approx -\frac{g_o g_{di}}{2g_{ml}(g_{dl} + g_{di})}$$

$$\text{CMRR} \equiv \left|\frac{A_{dm}}{A_{cm}}\right| \approx 2\frac{g_{mi} g_{ml}}{g_o g_{di}} \qquad \text{output resistance } r_o \approx \frac{1}{g_{dl} + g_{di}}$$

* Longer channel in Ms leads to smaller g_o and higher CMRR.

* $A_{dm} \propto \frac{1}{\sqrt{I_o}}$ or $(I_o)^{-1/m}$ => higher bias current, lower gain.

* In the weak inversion region, $g_{mi} \propto$ Io => $A_{dm} \approx$ constant.

* Cascode current source can be used for Io to increase CMRR,but Vicm $\downarrow$

* This circuit is not a pure symmetric differential circuit. But it can be approximated by a differential circuit and half -circuit analysis method can be used.

* Signal paths:

v_{in1} :

$v_{in1} \rightarrow v_{gsl}$: $A_v' = -g_{mi}\dfrac{1}{g_{ml}}$

$v_{gsl} \rightarrow v_o$: $A_v'' = -g_{ml}(r_{dsl} // r_{dsi})$

⇨ $A_v\big|_{v_1} = A_v' A_v'' = g_{mi}(r_{dsl} // r_{dsi}) = A_{dm}$

How about $v_{in1} \rightarrow v_1 \rightarrow v_o$?

v_{in2} :

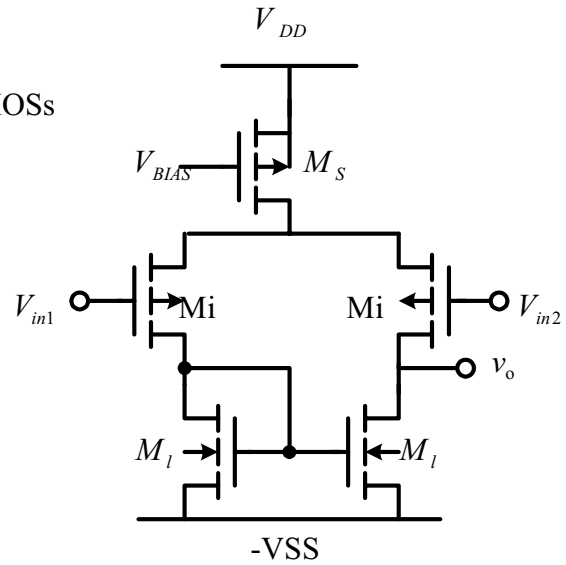
$v_{in2} \rightarrow v_o$: $A_v\big|_{vin2} = -g_{mi}(r_{dsl} // r_{dsi}) = |A_{dm}|$

How about $v_{in2} \rightarrow v_1 \rightarrow v_{gsl} \rightarrow v_o$?

The voltage gain of the four signal paths have nearly the same amplitudes. But different signal paths affect the high frequency response.

Version II: PMOS input

* Lower noise(1/f noise) due to input PMOSs
* Lower output dc voltage



14. The available amplifier circuits in CMOS trechnology

1). NMOS amplifier in 4-1.1
2). PMOS amplifier with the same configurations as in 4-1.1
3). CMOS amplifiers (NMOS version) in 4-1.2
4). PMOS version with the same configurations as in 4-1.2

Comparisons:

1) NMOS(PMOS) amplifiers versus CMOS amplifiers

	single-type MOS amplifier	CMOS amplifier
Voltage gain	Low	High
Output resistance	Low	High
Immunity to process variations	High	Low
Power dissipation	High	Low

2) NMOS amplifier (CMOS amplifier with NMOS version) versus PMOS amplifier (CMOS amplifier with PMOS version)

1.Better frequency response

2.Smaller chip area

3) Differential amplifier versus single-ended-output amplifier

1.Excellent common-mode signal rejection capability

Common-mode signals: external noise, dc voltage due to variations, power-supply noise, substrate noise.

2.Good for weak signal amplification in noisy environment.

3.Wide applications especially in high-frequency ICs.

4.More component used ➔ Higher power dissipation and larger chip area.

5.Matched devices are required ➔ Special care is need in layout and process.

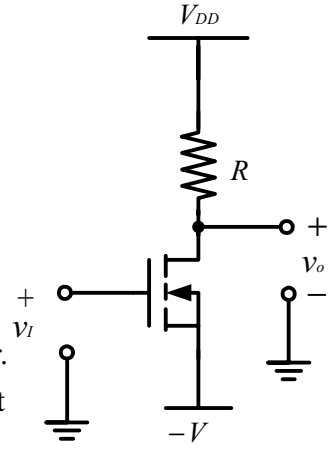
6.I/O testing requires special I/O external circuits or equipment.

§4.2 Passive-Load MOS Amplifiers

§4-2.1 Resistive-load MOS amplifiers

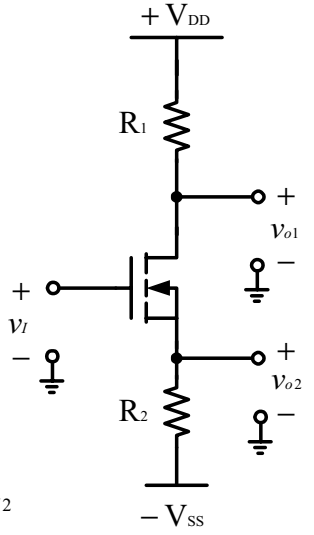
1. Resistive-Load MOS amplifier

$Av = -g_{m1}R$, $r_o \approx R$



* Low voltage gain and low r_o
* If R ↑, M1 might be in the linear region.
* Only used for low-gain high-frequency amplifier.
  ∵ Parasitic capacitance of R is smaller than that of the current-source active load.
* Process variations of R might be ±20%.

2. Resistive-load MOS phase splitter



$$A_{V1} \equiv \frac{V_{O1}}{V_i} \cong -\alpha_1 \frac{R_1}{R_2}$$

$$A_{V2} \equiv \frac{V_{O2}}{V_i} \cong \frac{\alpha_1 g_{m1} R_2}{g_{m1} R_2 + \alpha_1}$$

$$r_{o1} \cong R_1$$

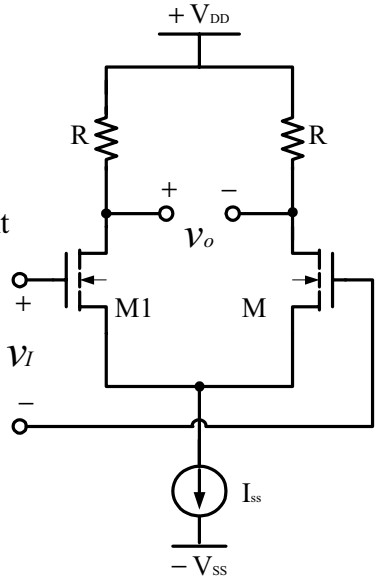
$$r_{o2} \cong R_2 \left\| \frac{1}{g_m} \right.$$

* R1 and R2 can be chosen so that $A_{V1} = A_{V2}$

➔ Phase splitter

* Process variation effect of R1 and R2 on A_{V1} and A_{V2} is reduced.

3. Resistive-load differential amplifier



* Suitable for low-gain low-r_o high-frequency amplifiers.

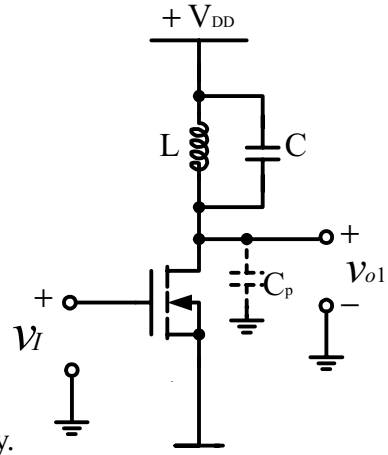
* I_{SS} can be generated by the constant-gm current source with R_{cogm}

➔ I_{SS} or $g_{m1}, g_{m2} \propto \frac{1}{R_{cogm}}$

➔ $A_{dm} = -g_{m1} R \propto \frac{R}{R_{cogm}}$

➔ Process variation of R and temperature coefficient of R can be compensated.

§ 4-2.2 Inductive load MOS amplifier



1. LC-tank MOS amplifier

* If L is implemented by on-chip inductor, only ~GHz RF operation is allowed.

* L combined with the parasitic capacitance Cp and the capacitor C to form a LC tank.

➔ Narrow-band amplifier or tuned amplifier.

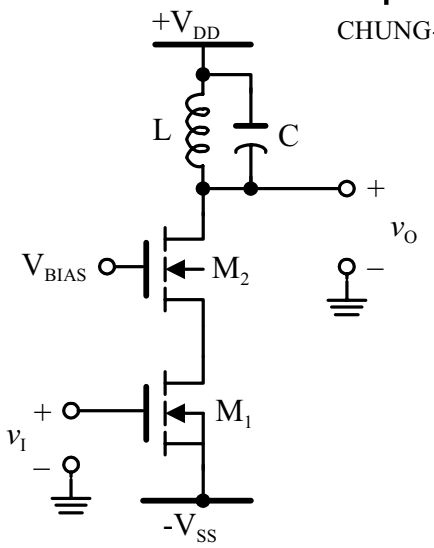
➔Bandpass amplifier with frequency selectivity.

2. LC-tank MOS cascode amplifier

*The output LC-tank impedance has a much smaller effect on the input impedance at high frequency due to the isolation effect of M2.

* $V_{ODC} = V_{DD}$

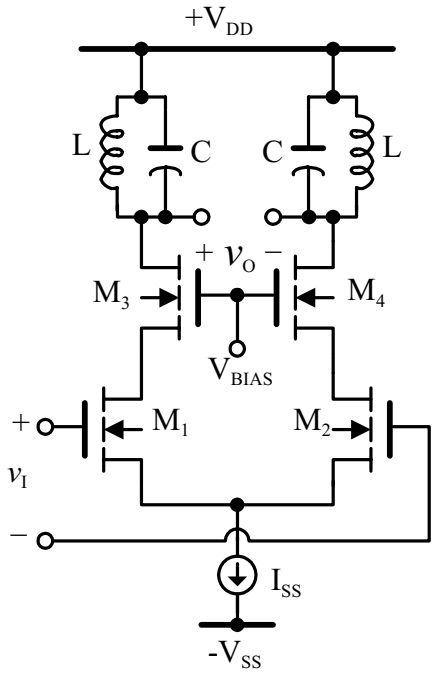
$v_O > V_{DD}$



3. MOS differential cascodee amplifier with series LC-tank

* $V_{O1DC} = V_{O2DC} = V_{DD}$

*Two LC-tanks are required.



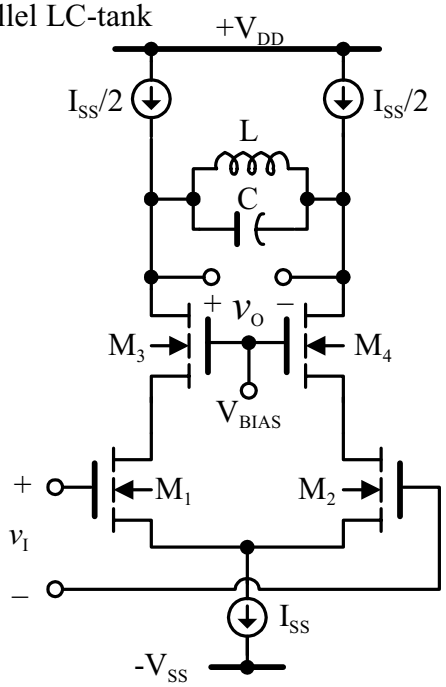
4. MOS differential cascode amplifier with parallel LC-tank

* Only one LC-tank is used

=>chip area↓

* $V_{O1DC} = V_{O2DC} < V_{DD}$

*Bandpass amplifier with the maximum differential gain the same as that of the cascode amplifier.

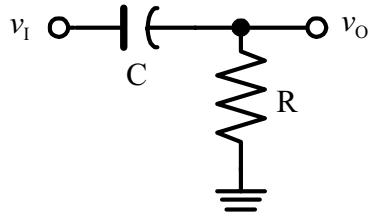


§ 4-3 Level shifting circuits

Purpose: to provide a dc voltage difference between input and output signals so that the dc level of the output signal is acceptable for the next amplifier stage.

∵ At low frequency operation below several tens MHz, dc blocking capacitors are not effective in blocking the dc voltage and passing the ac signal.

DC blocking capacitor:



ac gain: $\left|\frac{Vo}{Vi}\right| = \left|\frac{R}{R - j\frac{1}{wc}}\right| = \frac{R}{\sqrt{R^2 + \left(\frac{1}{wc}\right)^2}} \cong \frac{1}{1 + \frac{1}{2}\frac{\left(\frac{1}{wc}\right)}{R^2}}$

At 10MHz, $w \cong 6.3\times10^7$ rad/sec

CASE1: If C=10PF, $\frac{1}{wc} = \frac{1}{6.3}\times10^4\,\Omega \cong 1.6k\Omega$

To obtain 1% signal attenuation, we have

$$\left|\frac{v_o}{v_i}\right| = 0.99 \quad => \frac{1}{2}\frac{\left(\frac{1}{wc}\right)^2}{R^2} \cong 0.1$$

$$=>R=\left(\frac{1}{wc}\right)\frac{1}{\sqrt{0.02}} \cong 11.2k\Omega$$

The values of R and C are too large and area-consuming.

CASE 2: At 1GHz, $w=6.3\times10^9$ rad/sec

If C=1PF, $\frac{1}{wc} = \frac{100}{6.3} \cong 160\Omega$

The required R for 1% attenuation is

$$R=7(\frac{1}{wc})=1.12k\Omega$$

The values of R and C are reasonable.

1. Simple level shifting circuit

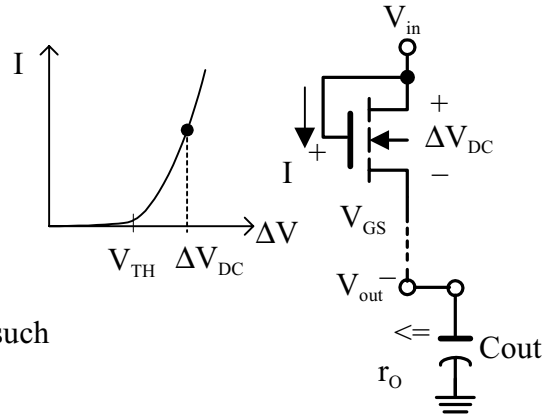
$\triangle V_{DC}=V_{GS}$

* W/L $<<1$ to obtain a large $\triangle V_{DC}$
* Output resistance looking into Vout is very large

$r_O \cong \frac{1}{g_m}$ $\because W/L<<1,\ g_m \downarrow \Rightarrow r_O \uparrow$

* Frequency response could be degraded by such a large r_O.

$\because$ r_OCout $\uparrow$



2. High-Z level shifting circuit

$\triangle V_{DC}(NMOS)=+V_{GS}$

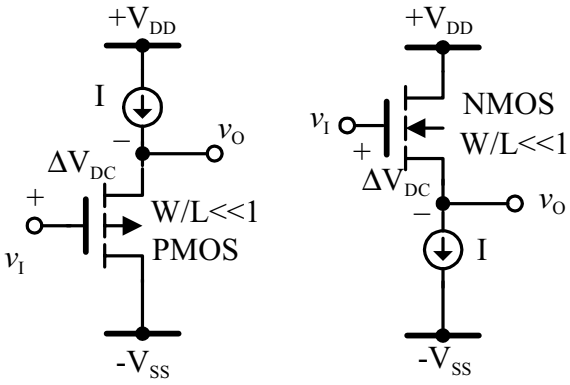
$\triangle V_{DC}(PMOS)=-V_{GS}$

* $r_O \cong \frac{1}{g_m}$

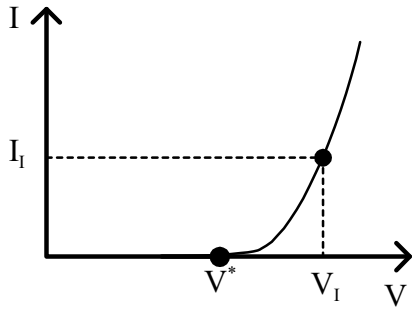
$\because W/L<<1$

$\Rightarrow r_O \uparrow (\triangle V_{DC} \uparrow)$

Frequency response could be degraded.

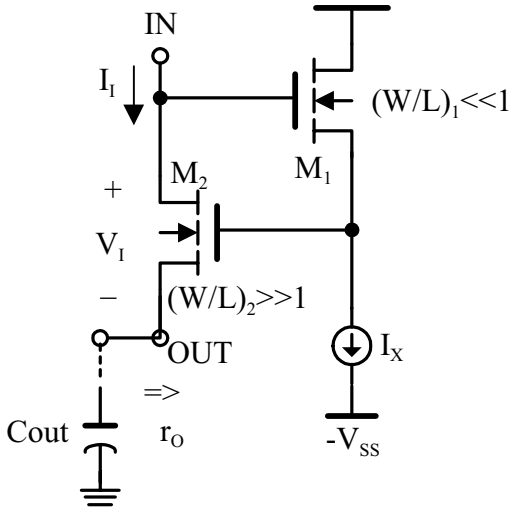


3. Low-Z level shifting circuit



$V^*=V_{TH2}+V_{GS1}$

$=V_{TH2}+V_{TH1}+\sqrt{\frac{Ix}{\left(\frac{\mu C_{ox}}{2}\right)_1 (W/L)_1}}$



$$V_I = V^* + \sqrt{\frac{I_I}{\left(\frac{\mu C_{ox}}{2}\right)_2 (W/L)_2}}$$

$\because (W/L)_1 << 1$ and $(W/L)_2 >> 1$ =>large enough V^*

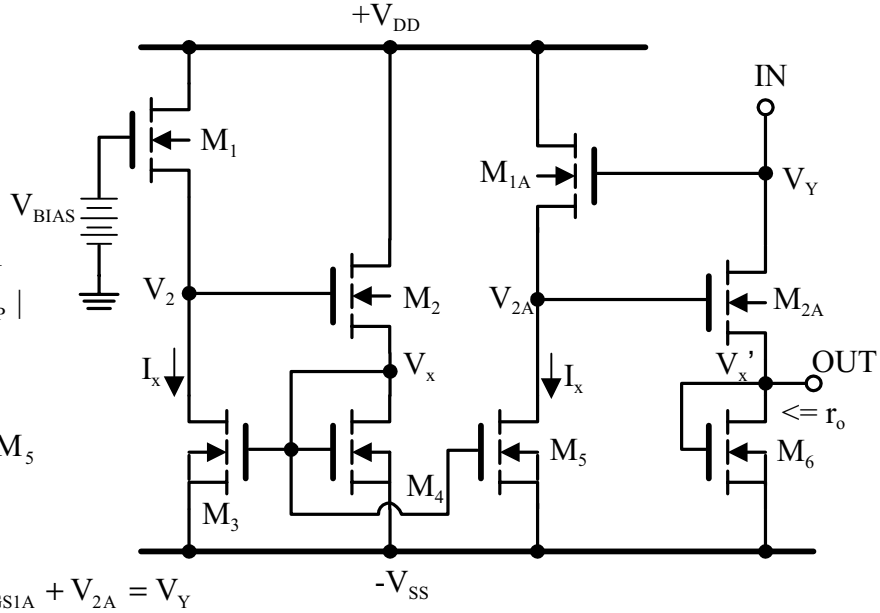
$V_I \cong V^*$ independent of I_I

* V_I (dc voltage shift) can be stabilized by choosing a large $(W/L)_2$ and a stable I_x.

* $r_0 \cong \frac{1}{g_{m2}}$ is not large since $(W/L)_2 >> 1$.

=> Better frequency response.

4. Replica bias circuit



$(W/L)_6, (W/L)_4 >> 1$

$\Rightarrow V_{GS4} \cong V_{GS6} \cong V_{THN}$

$\Rightarrow V_X \cong V_X'$

$(W/L)_2, (W/L)_{2A} >> 1$

$\Rightarrow V_{GS2} \cong V_{GS2A} \cong |V_{THP}|$

$\Rightarrow V_2 \cong V_{2A}$

$M_1 \cong M_{1A}$ and $M_3 \cong M_5$

$I_{DS3} = I_{DS5} = I_X$

$V_{GS1} = V_{GS1A}$

$V_{BIAS} = V_{GS1} + V_2 = V_{GS1A} + V_{2A} = V_Y$

* Provide a fixed bias voltage $V_Y = V_{BIAS}$ at the input node to stablize the preceding stage.

* Provide a DC voltage shift of $V_Y - V_X'$

* The output resistance looking into the OUT node is very small

$(r_o \cong \frac{1}{g_{m2A}} \| \frac{1}{g_{m6}}, (W/L)_{2A}, (W/L)_6 >> 1 \Rightarrow r_o \downarrow)$

* The matching between $M_1(M_3)$ and $M_{1A}(M_5)$ is very important to stablize V_Y.

§ 4-4 MOS Output stages

§ 4-4.1 Requirements

(1) Suitable power and voltage swing to drive an adequate external load equally in both positive and negative directions.

(2) Acceptably low levels of signal distortion.

(3) Minimum output impedance.

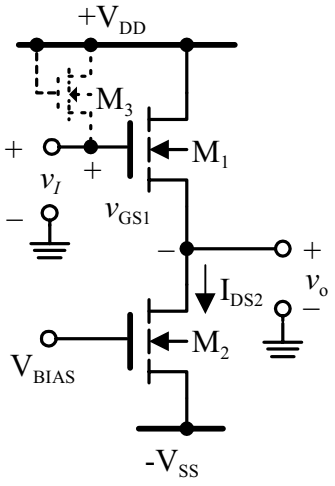
(4) Low quiescent power dissipation and maximum efficiency.

(5) High frequency response.

(6) Buffering the previous gain stage from C_L or R_L

§ 4-4.2 NMOS (PMOS) Output Stages

1.Source followers (Enhancement device)



* Voltage swing:

$$v^{+}_{o\max} = v_I - v_{GS1}$$

$$= V_{DD} - V_{TH3} - v_{GS1} \text{ (or } V_{TH1}\text{)}$$

(not full level to V_{DD})

$$v^{-}_{o\max} = V_{BIAS} - V_{TH2} \text{ (M_2 sat)}$$

$$= -V_{SS} \text{ (M_1 off)}$$

* $r_0 \cong \dfrac{1}{g_{m1}}$

Small r_0 Need large $(W/L)_1$ and I_{DS1}

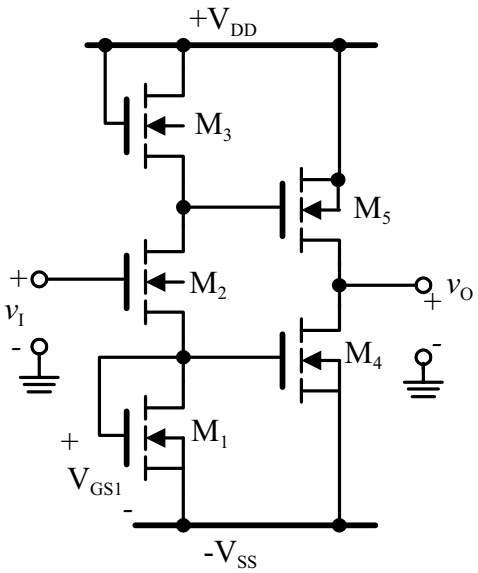
* The rise time is decreased by the larger $(W/L)_1$

But the fall time is fixed by I_{DS2}

=>Unsymmetric driving capability.

* Provide a dc voltage shift and a voltage gain smaller than 1

2. Phase-splitting output driver



* voltage swing: (low)

$$v_{o\max}{}^{+} = V_{DD} - V_{TH3} - V_{TH5}$$

(M2 and M4 are off)

$$v_{o\max}{}^{-} = -V_{SS} - V_{GS1} + V_{TH4} \text{ (M4 sat.)}$$

$$= -V_{ss} + V_{DS4} > -V_{SS}$$

(maximum)

* Fall time is not limited by the current source.

* $r_o \approx \left(1/g_{m5}\right) \| \left(r_{ds4}\right) \approx 1/g_{m5}$

3. NMOS output stage with feedback

M3, M4 : output common-source amplifier.

M1, M2 : First common-source amplifier

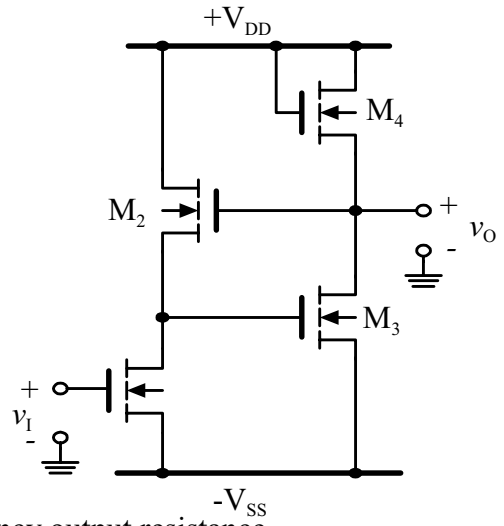
M2 : series-shunt negative feedback

Series-shunt negative feedback

=> voltage gain ↓

frequency bandwidth ↑

output resistance ↓



$$r_o = \frac{\alpha_4 / g_{m4}}{1 + \left(\alpha_2 \alpha_4 g_{m3} / g_{m4} \right)}$$ midfrequency output resistance

$$A_v = \frac{g_{m1}}{g_{m2}} \frac{\alpha_2 \alpha_4 g_{m3} / g_{m4}}{1 + \left(\alpha_2 \alpha_4 g_{m3} / g_{m4} \right)}$$ midfrequency voltage gain

If $\alpha \to 1$ $$A_V \equiv \sqrt{\frac{(W/L)_1}{(W/L)_2}} \frac{\sqrt{(W/L)_3 / (W/L)_4}}{1 + \sqrt{(W/L)_3 / (W/L)_4}}$$

* Larger $g_{m3} / g_{m4} \Rightarrow r_0 \downarrow,\ A_o \uparrow$

* The W/L ratio of M1,M2,M3 and M4 can be suitably designed to satisfy the specifications on (1) voltage gain ; (2) output swing ; (3) power dissipation ; (4) chip area ; (5) fast transient ; (6) good frequency response.
((5) and (6) involve non-linear analysis)

§ 4-4.3 CMOS Output Stages

1.Simple source follower.(NMOS and PMOS)
Too larger r_o

2.Class AB puah-pull CMOS output buffer

*Capable of low standby power.

e.g. $I_{bias} \cong$ nA

$I_{out} \cong <$ 1mA

* $V_{ODC} = \frac{V_{DD} + V_{SS}}{2}$ is desired

*Small output voltage swing.

If R_L exists at the output node, the voltage swing is further degraded.

3.Emitter-follower output stage.

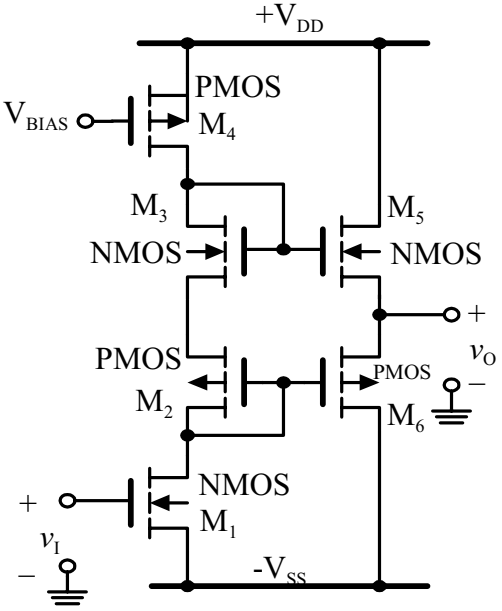
* $r_o \downarrow$

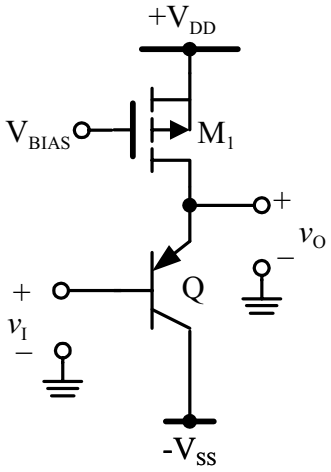
* Q_1 : free BJT in CMOS n-well technology.
Voltage swing:

$v_{O\max}^{-} = v_I + |V_{BE}|$

$= V_{SS} + |V_{BE}|$ (if $v_{I\max}^{-} = -V_{SS}$)

$v_{O\max}^{+} = +V_{DD}$ (If Q_1 is off)





* The collector series resistance r_C of Q_1 may degrade the output swing and saturate the transistor.

Chapter 5 Midband Analysis of CMOS Operational Amplifiers (OP AMPs)

§5-1 General Considerations

§5-1.1 General Procedures to analyze an OP AMP IC

1. Identify all the biasing circuits (current & voltage).
2. Identify all the protection circuits and then take them away.
3. Calculate all the operating currents and voltages.
4. Trace the signal path and identify the amplifier, buffer, level shifter, and output driver configurations.
5. Calculate the midfrequency gain.
6. Identify the compensation circuits.
7. Calculate the high-frequency response.
8. Perform the SPICE simulations to obtain the performance parameters.

§5-1.2 Some important OP AMP Specifications

1. Open-loop differential gain $A_d(\omega)$.
2. Open-loop common-mode gain $A_c(\omega)$.
3. Common-mode rejection ratio (CMRR)

$$CMRR(\omega) \equiv \left|\frac{A_d(\omega)}{A_c(\omega)}\right| = \left[\left.\frac{\partial V_{io}}{\partial V_{ic}}\right|_{V_o=0}\right]^{-1}$$

where V_{io} is the input offset voltage

V_{ic} is the input common-mode voltage

4. Output swing.

5. Unity-gain frequency f_u.

6. Upper 3-dB frequency $f_{3\text{-}dB}$.

7. Power-supply rejection ratio (PSRR).

$$PSRR^{+}(\omega) \equiv \left| \frac{A_d(\omega)}{\frac{\partial V_o}{\partial V_{DD}}(\omega)} \right| = \left[\frac{\partial V_{io}}{\partial V_{DD}}(\omega)\Big|_{V_o=0} \right]^{-1}$$

$$PSRR^{-}(\omega) \equiv \left| \frac{A_d(\omega)}{\frac{\partial V_o}{\partial V_{SS}}(\omega)} \right| = \left[\frac{\partial V_{io}}{\partial V_{SS}}(\omega)\Big|_{V_o=0} \right]^{-1}$$

8. Slew rate and settling time

Slew rate: Maximun $\frac{d}{dt}v_o$ in an unity-gain close-loop OP Amp with a fixed step input under maximum load.

Settling time: The time required for the OP AMP in an unity-gain closed loop to reach ~% of its final value with a fixed step input under maximum load.

9. Linearity and harmonic distortion

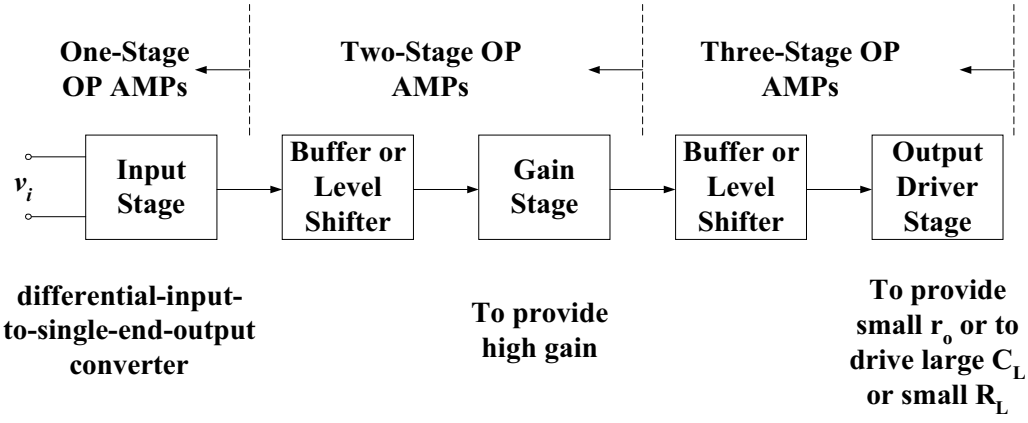
Usually dominated by the output stage.

Closed-loop characteristics.

10. Equivalent input noise and input offset

Usually dominated by the input stage.

§5-1.3 General Block Diagram of an OP AMP



§5-2 One-Stage (Single-Stage) CMOS OP AMPs

§5-2.1 Single-ended-output OP AMPs

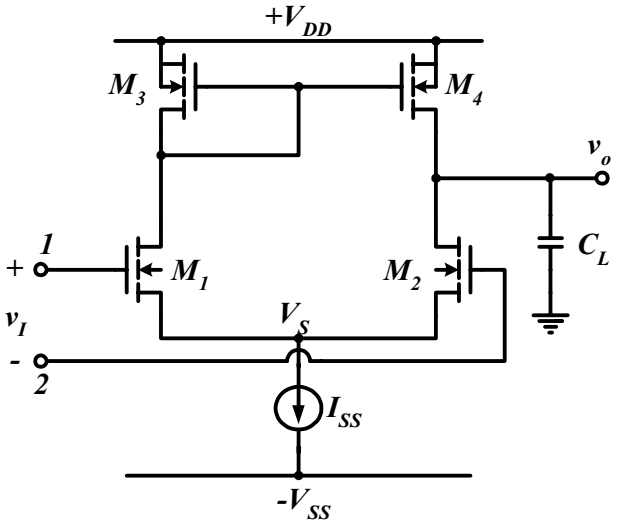
1. Simple OP AMP

* Inverting input: 2

Noninverting input: 1

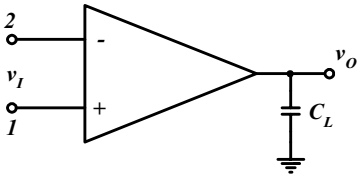
* Open-loop voltage gain

$$\equiv \frac{v_o}{v_i} = A_d = -g_{mN}(r_{dsP} // r_{dsN})$$



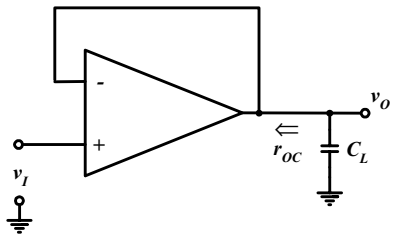
* Open-loop output resistance

$$r_o = r_{dsP} // r_{dsN}$$



Close-loop output resistance

$$r_{oc} \cong \frac{r_{dsP} // r_{dsN}}{1 + g_{mN}(r_{dsP} // r_{dsN})} \cong \frac{1}{g_{mN}}$$



The closed-loop output resistance is independent of the open-loop output resistance.

* The dominate pole is located at the output with the RC time constant r_oC_L.

* $A_d \sim 100$, Power dissipation ~ μW, $f_u \sim$ MHz.

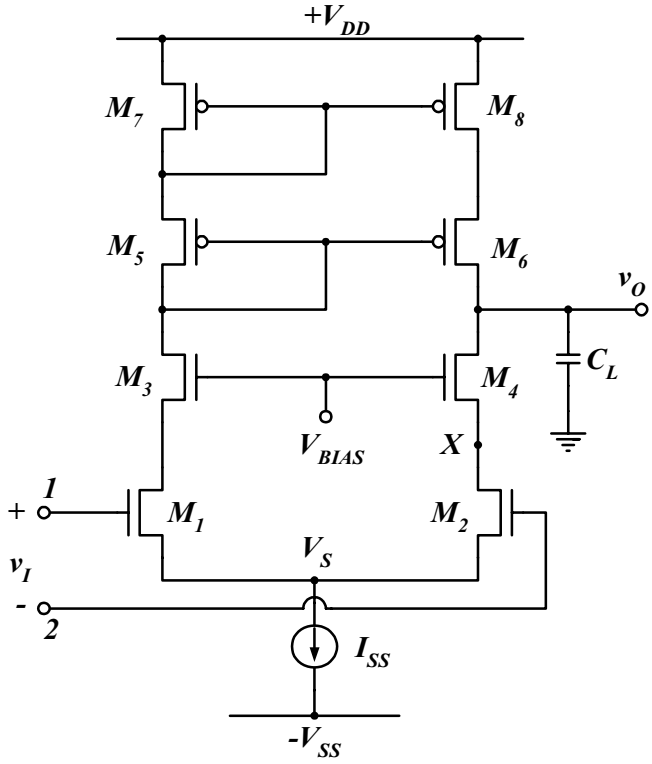
Suitable for small-load internal-use applications.

* Cannot drive heavy load.
* Output swing: $V_{DD} - |V_{DSATP}| \rightarrow -V_{SS} + V_S + V_{DSATN}$

2. Telescopic cascode OP AMP with cascode-current-source load

* Open-loop voltage gain

$$A_d = -g_{mN}(g_{mN} r^2_{dsN} \,//\, g_{mP} r^2_{dsP})$$



* Open-loop

$$r_o = g_{mN} r^2_{dsN} \,//\, g_{mP} r^2_{dsP}$$

Close-loop

$$r_{oc} \cong \frac{1}{g_{mN}}$$

* In the unity-gain feedback, the node 2 is connected to the output node.

$\Rightarrow M_2$ and M_4 sat.

$\Rightarrow V_{o\,min} = V_{BIAS} - V_{TH4}$,

$$V_{o\,max} = V_x + V_{TH2} = V_{BIAS} - V_{GS4} + V_{TH2}$$

$\Rightarrow$ Output swing $= V_{TH2} - (V_{GS4} - V_{TH4}) \le V_{TH2}$

Too small output swing

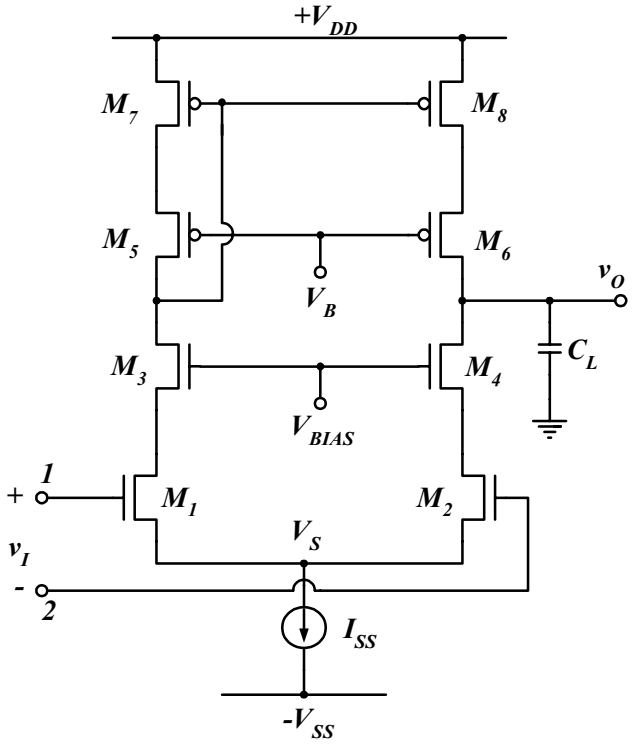
Not suitable for unity gain buffer.

* Limit output swing:

$$V_{DD} - |V_{DSAT8}| - |V_{DSAT6}| \rightarrow -V_{SS} + V_S + V_{DSAT2} + V_{DSAT4}$$

3. Telescopic cascode OP AMP with high-swing cascode-current-source load

* Higher output swing
* Not suitable for unity-gain buffer



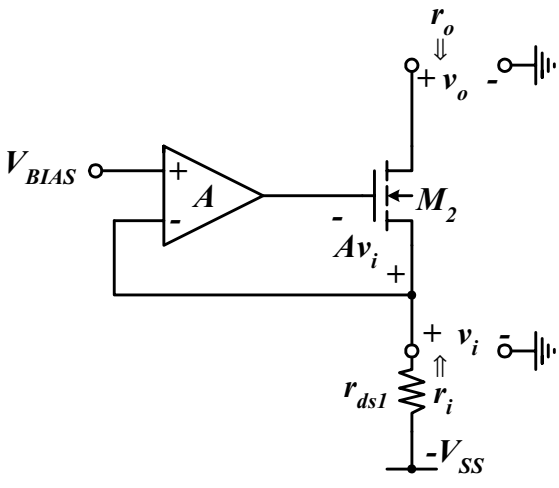
4. Telescopic cascode OP AMP with gain-boosting (or enhanced-output -impedance) circuit

1) Basic concept

* $v_i \rightarrow Av_i \rightarrow i_o = Ag_m v_i$

$$\frac{i_o}{v_i} = Ag_m$$

The transconductance is boosted by A times, $A \sim 100$.



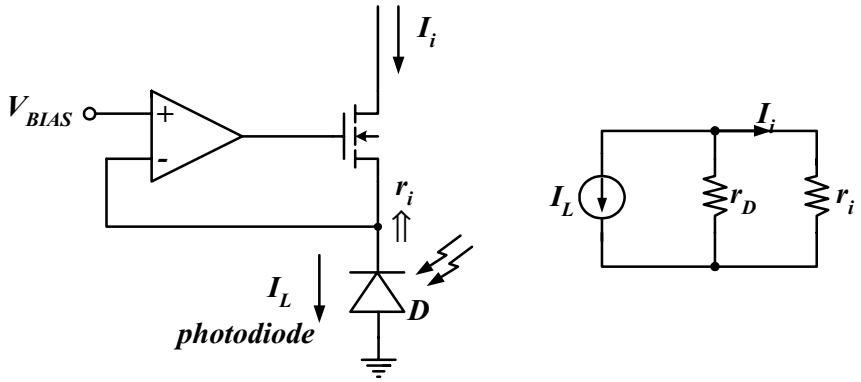
* $r_i \cong \frac{1}{g_m}\frac{1}{A} \sim 100\Omega - 10\Omega$

The input resistance is lowered by A times.

Suitable for current input because of small r_i.

$\Rightarrow$ High injection efficiency

Example:



If the output resistance of D is not large, e.g. r_D=10KΩ,

We need $r_i \le 100\Omega$ to obtain $I_i = I_L \dfrac{10K\Omega}{10K\Omega + r_i} \cong 99\ \%$ of I_L

⇒ 99 % injection efficiency and stable photodiode reverse bias V_{BIAS}

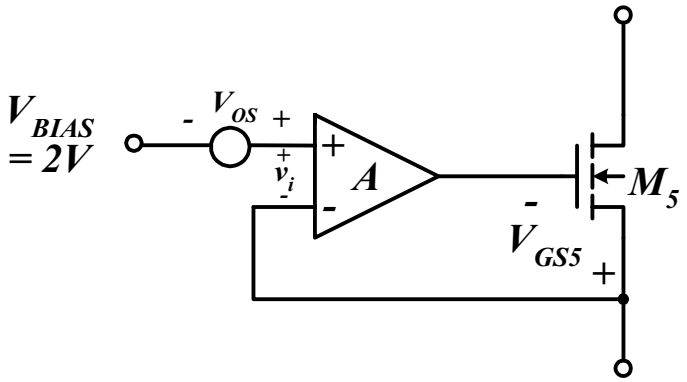
* $r_o \cong (G_{m2} r_{ds1}) r_{ds2} = A g_{m2} r_{ds1} r_{ds2}$

The output resistance is boosted by A times as compared to the cascode structure without A.

No extra cascode device is required

⇒ The swing is not further degraded.

* Offset voltage problem



A = 100, V_{OS} = 0V, V_{GS5} = 1.4V > V_{TH5} = 1.1V,

⇒ v_i = 14mV and M_5 is turned on to provide negative feedback.

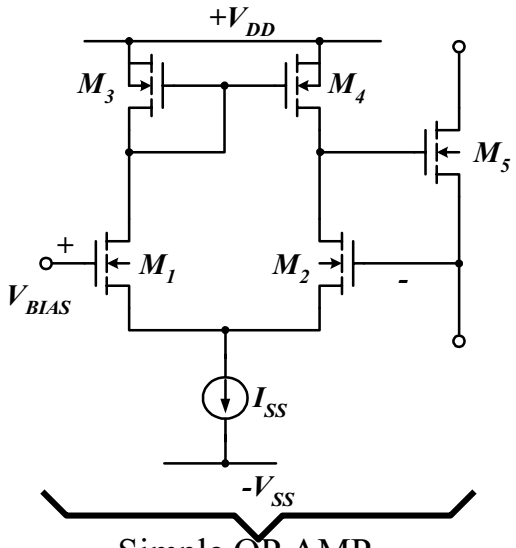
But if V_{OS} = -5mV

$\Rightarrow V_{GS5}$ = 0.9V smaller than V_{TH5}

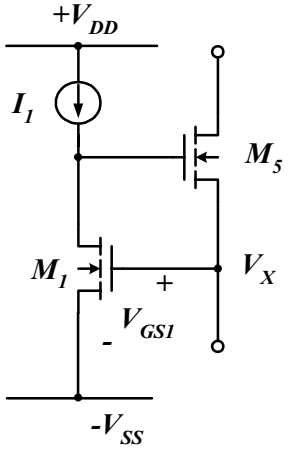
$\Rightarrow M_5$ is off and the circuit fails.

So suitable systematic offset should be introduced to make sure that $V_{OS} > 0$

* Realization



Simple OP AMP

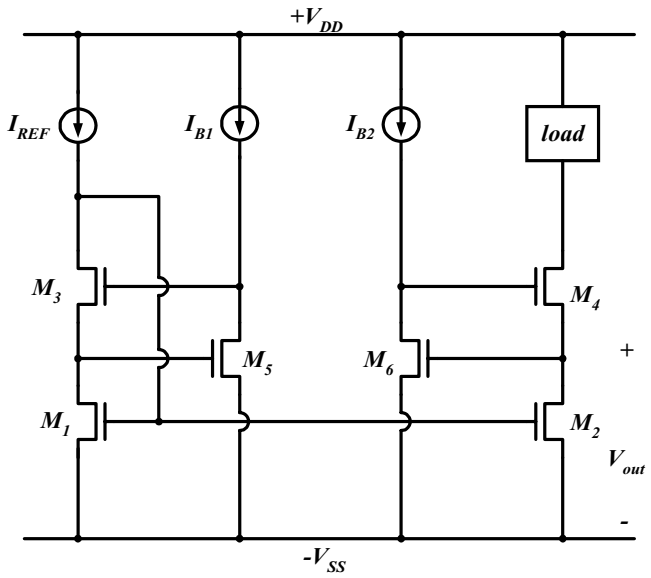


$V_x = V_{GS1} - V_{SS}$ fixed

$A = -g_{m1}(r_{ds1} // r_{o1})$

2) Current mirror with enhanced-output-impedance circuit

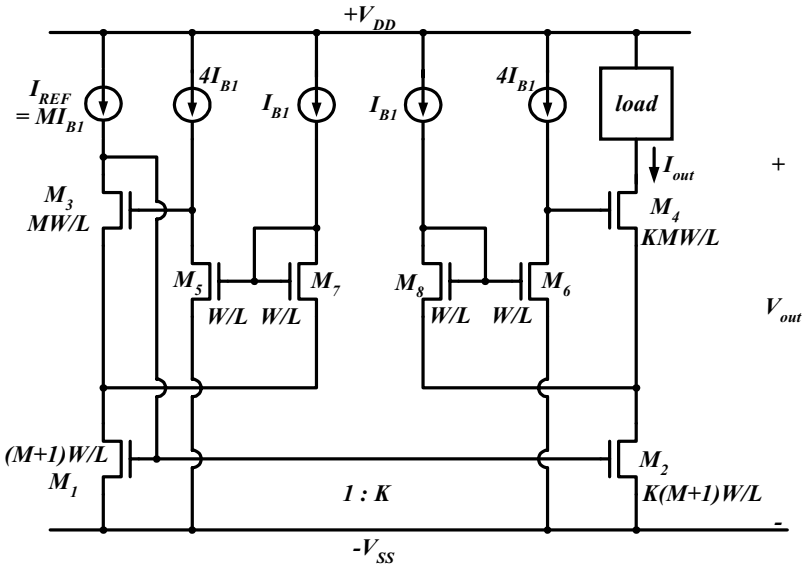
A: The Sackinger implementation



* Low swing
* $r_o = (g_{m4} r_{ds2} r_{ds1})[g_{m6}(r_{ds6} // r_{OB2})]$
* Minimum required V_{out}

  $V_{out} = V_{GS6} + V_{GS4} - V_{TH4}$
* $V_{GS6} = V_{GS5} \Rightarrow V_{DS1} = V_{DS2}$ precise current ratio

B: High-swing implementation



* Add extra devices M_7 and M_8 to decrease V_{DS1} and V_{DS2}.
* $V_{DS1} = V_{GS5} - V_{GS7}$

  $V_{DS2} = V_{GS6} - V_{GS8}$
* High swing

  Min $V_{out} = V_{GS6} - V_{GS8} + V_{GS4} - V_{TH4}$
* $I_{out} = KI_{REF}$

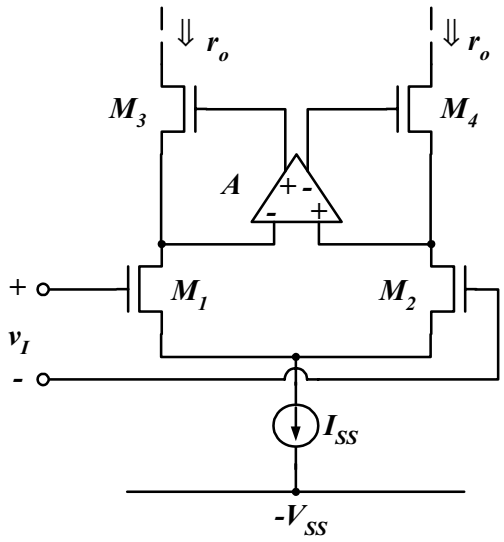
  $V_{DS1} = V_{DS2} \Rightarrow$ precise ratio

3) OP AMPs

A: Using the gain-boosting circuit in cascode amplifier

* $g_{m3} = g_{m4}$ is increased by A times.
* The effective resistance seen by M_1 and M_2 is lowered by A times

  $\Rightarrow$ The gain is lowered by A



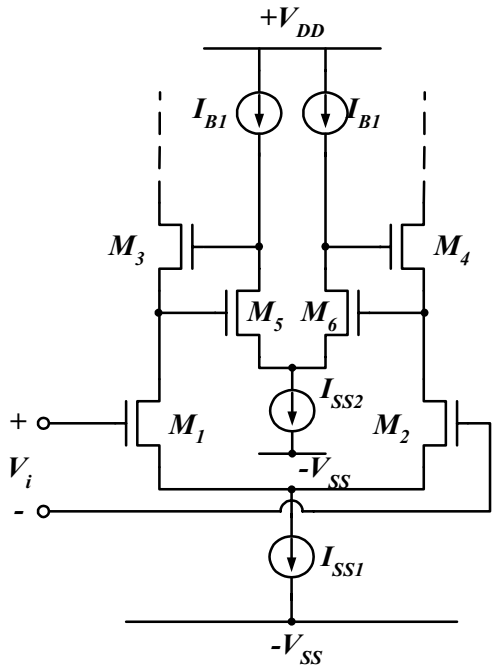
times.

⇒ Has much less Miller capacitance at the input while keeping M_1 and M_2 saturated.

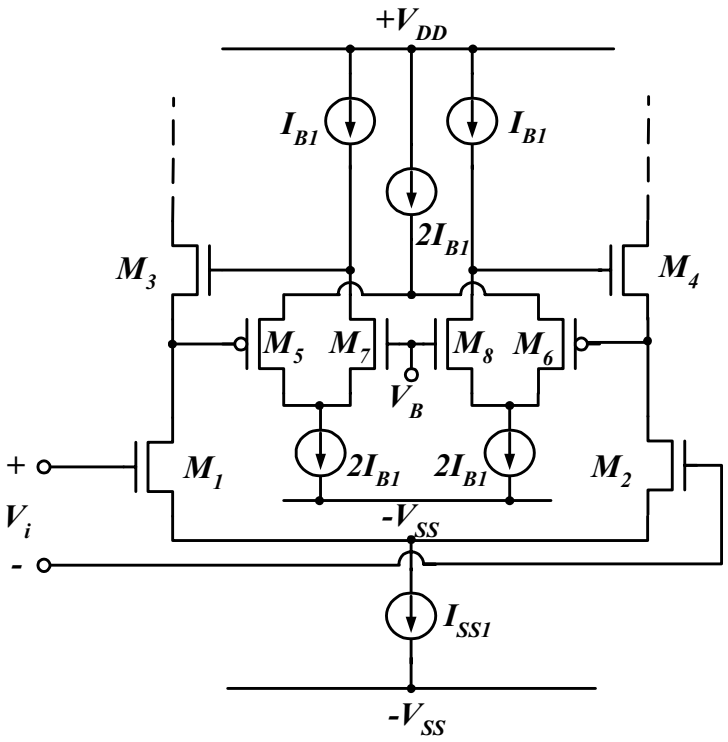
* r_o seen by M_3 and M_4 is increased by A times ⇒ Gain boosting

* Realization

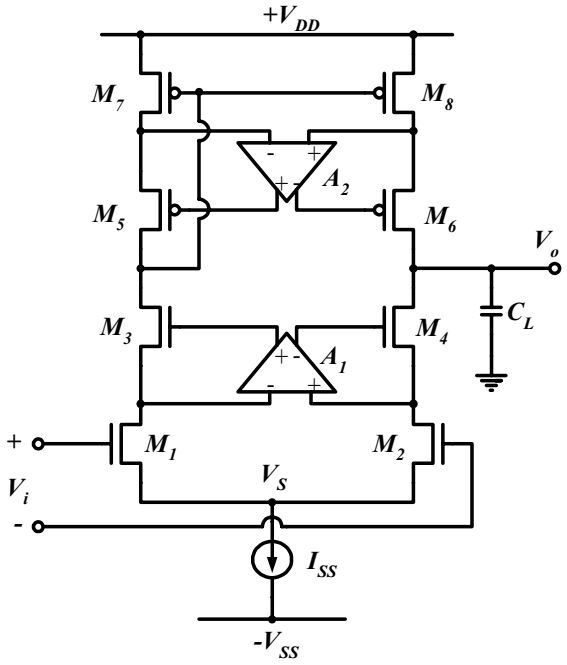
Why I_{SS2} ?



The amplifier A is realized by fully differential folded cascode amplifier

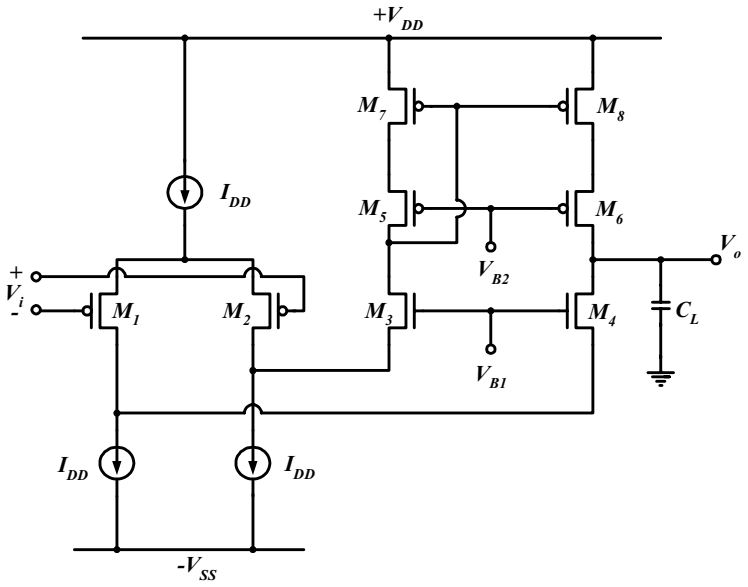


B: Using the gain-boosting circuits in both cascode amplifier and current-mirror load



5. Folded cascode OP AMP

1) PMOS input



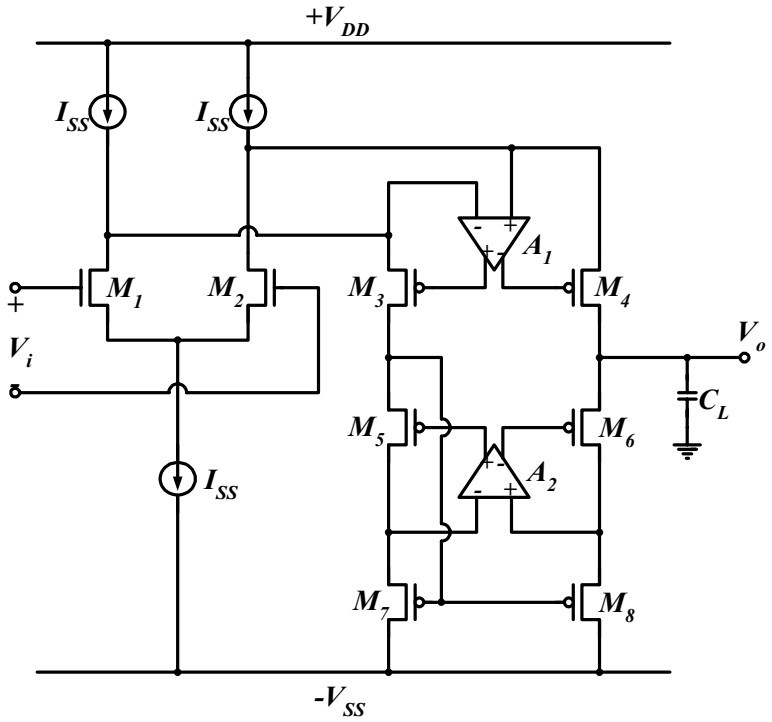
* Higher power dissipation than the telescopic cascode OP AMP.

* Higher input equivalent noise and input offset voltage

∵ More devices are involved.

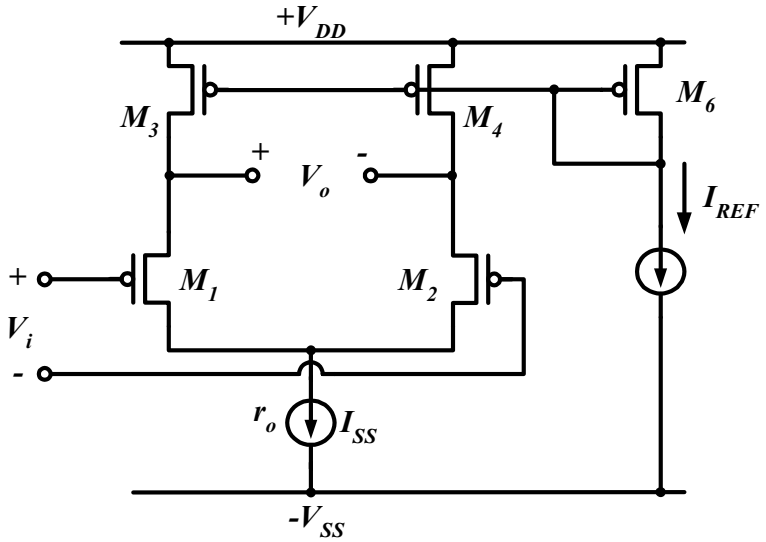
* Higher V_{ICM} range and higher output swing.
* Lower voltage gain as compared with the PMOS-input telescopic cascode OP AMP. Why ?
* Lower r_o

2) With the gain-boosting circuit



§5-2.2 Fully differential OP AMPs

1. Simple OP AMPs

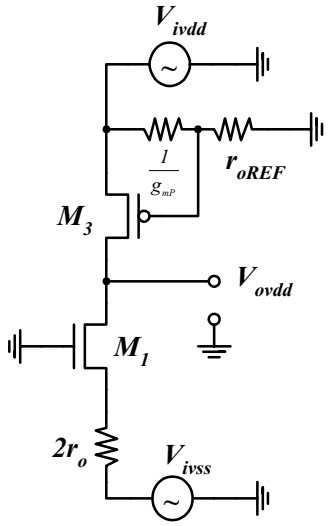


* $A_{dm} \cong -g_{mN}(r_{dsN} \,//\, r_{dsP})$

$$A_{cm\cong} = -\frac{\alpha_1 r_{dsP}}{2r_o}$$

$$CMRR = \frac{\alpha_1 g_{mN}(r_{dsN} \,//\, r_{dsP}) r_{dsP}}{2r_o}$$

* Power supply noise gain



$$A_{cvddm} \cong +g_{mP}[r_{dsP} \,//\, (g_{mN} 2r_o) r_{dsN}][\frac{1}{g_{mP} r_{oREF} + 1}] \cong \frac{r_{dsP}}{r_{oREF}} \cong 1$$

$$A_{cvssm} \cong +(\frac{\frac{1}{g_{mN}}}{2r_o + \frac{1}{g_{mN}}})[g_{mN}(r_{dsN} \,//\, r_{dsP})] = \frac{r_{dsN} \,//\, r_{dsP}}{2r_o + \frac{1}{g_{mN}}}$$

$$PSRR+ \equiv \frac{|A_{dm}|}{|A_{cvddm}|} = \frac{g_{mN}(r_{dsN} \,//\, r_{dsP})}{g_{mP} r_{dsP}}$$

$$g_{mP} > g_{mN} \quad \text{for large } PSRR+$$

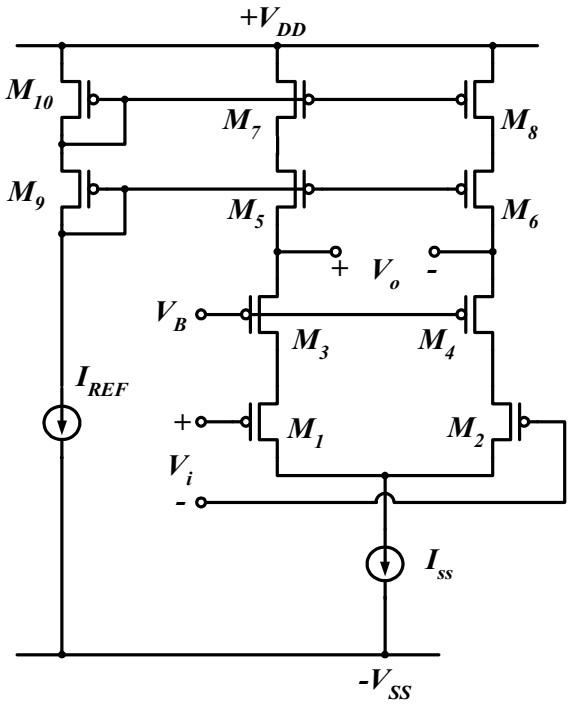
$$PSRR- \equiv \frac{|A_{dm}|}{|A_{cvssm}|} = \frac{g_{mN}(r_{dsN} \,//\, r_{dsP})(2r_o + \frac{1}{g_{mN}})}{(r_{dsN} \,//\, r_{dsP})} \cong 2 g_{mN} r_o$$

$$PSRR- > PSRR+$$

$PSRR+$ for V_{DD} is not high enough.

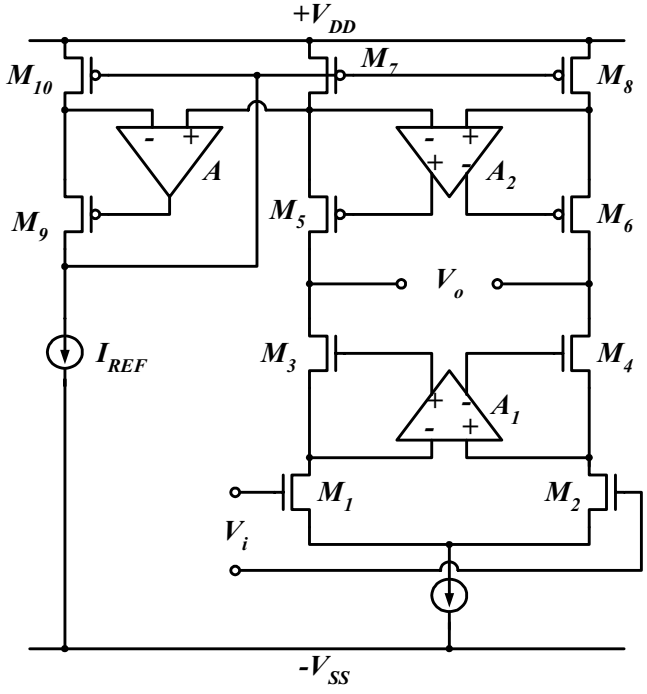
* Commond-Mode Feedback (*CMFB*) is required to decrease A_{cm} and increase *CMRR*. With *CMFB* circuit, *PSRR* ↑.

2. Telescopic cascode OP AMPs with cascode or high-swing cascode current-source load

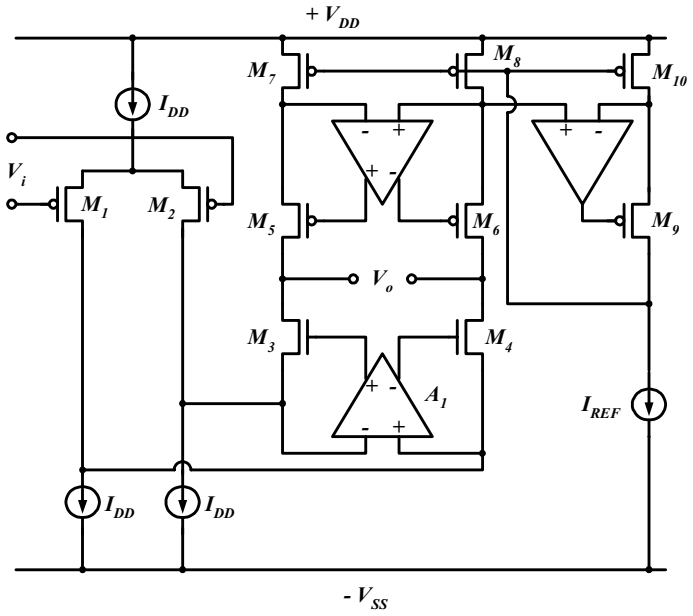


	cascode	high-swing cascode
Output swing	Low	High
PSRR+	?	?
PSRR-	High	High

3. Telescopic cascode OP AMPs with gain-boosting cascode amplifier or current-source load
   * To obtain maximum swings at the output, A_2 must employ an NMOS-input differential pair (high output dc voltage) whereas A_1 an PMOS-input one (Low output dc voltage)
   * Very high voltage gain



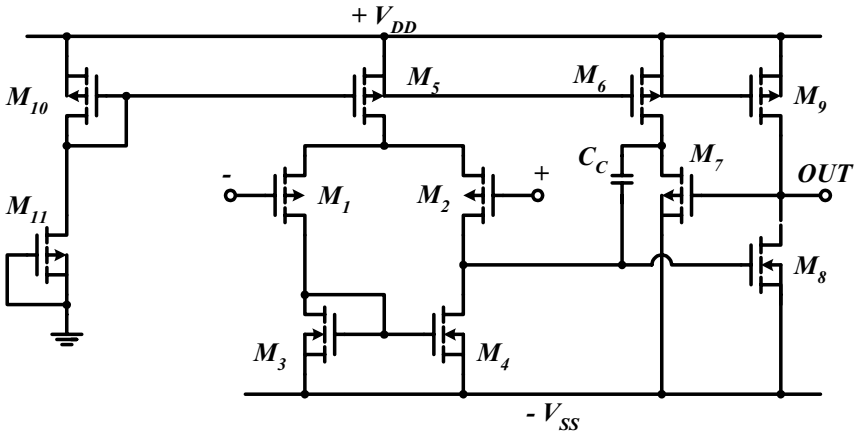
4. Folded cascode OP AMPs with cascode, high-swing cascode, or gain-boosting current-source load



§5-3 General-Purpose Two-Stage CMOS OP AMPs

§5-3.1 Single-ended-output OP AMPs

1. PMOS-input design I



M_{10}, M_1 : Master stage of PMOS current mirror.

M_5, M_6, M_9 : Slave stages

M_1, M_2, M_3, M_4, M_5: Differential-input-to-single-ended - output converter (input stage)

M_8, M_9 : CS amplifier with current-source load (gain stage)

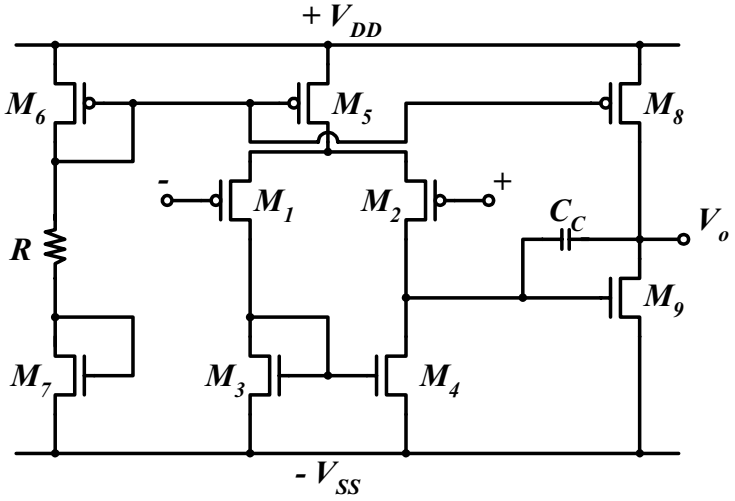
M_6, M_7, C_C : Compensation circuit with source follower.

OP AMP Characteristics :

Open-loop dc gain: 60 ~ 66 dB

CMRR : 60 dB

2. PMOS-input design II



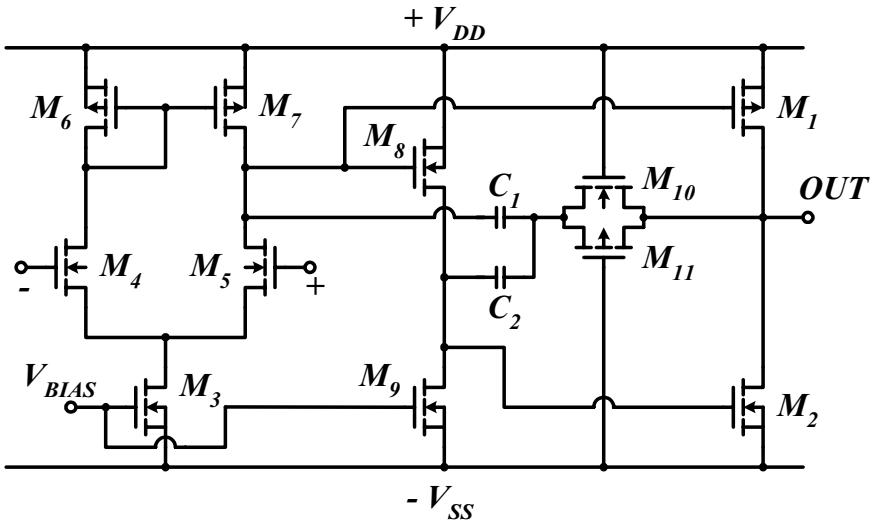
C_C : Compensation capacitor

R : n+ diffusion resistor

* First commercial CMOS OP AMP

* Designed by Motorola in 12-bit ADC.

3. NMOS-input design with level-shifted CMOS amplifier



C_2 : for PSRR (V_{DD}) consideration.

C_1 : normal compensation capacitor

Reference : IEEE JSSC, vol. sc-14, pp. 961-969, Dec. 1979

* Designed by AMI in PCM voice CODEC.

OP AMP characteristics:

Open-loop gain : 90 dB

CMRR : 73 dB

PSRR+ : 68 dB

PSRR- : 70 dB

Input offset : 10 mV (standard deviation)

0.4 mV (mean)

4. Typical characteristics of CMOS 2-stage OP AMPs

Reference : IEEE JSSC, vol. sc-17, pp. 969-982, Dec. 1982

Open-loop dc gain (C_L only) : $10^3 \sim 10^4$ (60 dB ~ 80 dB)

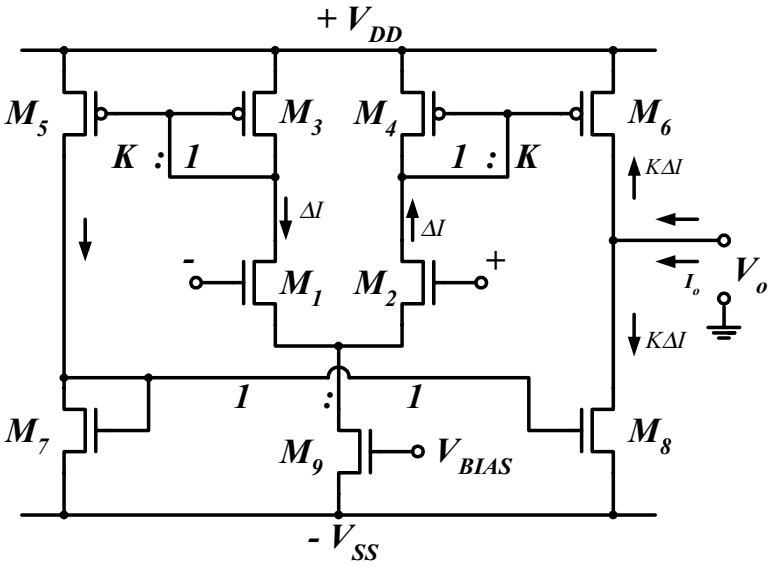
PSRR : 60 dB ~ 70 dB

Input offset : 2 mV (standard deviation)

Input common-mode range : within 1V of supply voltage.

5. Output Transconductance Amplifier (OTA) or current-mirror OP AMP

Reference : IEEE JSSC, vol. sc-19, pp. 349-359, June 1984



M_3, M_5 / M_4, M_6 : PMOS current mirrors

M_7, M_8 : NMOS current mirror

$M_1 \sim M_4$, M_9 : Input stage

$M_5 \sim M_8$: Gain stage

ΔV_{in} (input differential voltage) $\Rightarrow \Delta I \Rightarrow K\Delta I \Rightarrow \Delta I_{out} = 2K\Delta I = I_o$

$$G_m \equiv \frac{\Delta I_{out}}{\Delta V_{in}} = g_m K \qquad A_v = G_m(r_{ds6} \,//\, r_{ds8})$$

Characteristics :

Open-loop gain : 58 dB

Total dc current；4μA

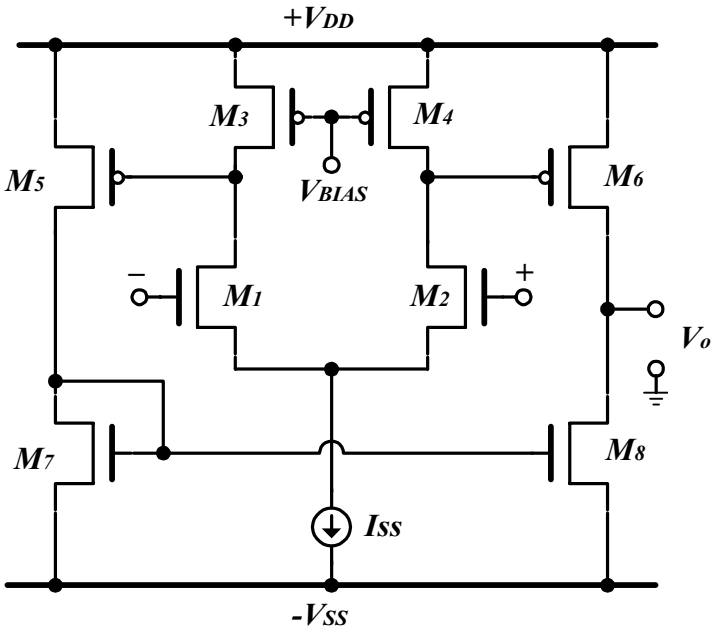
Output load capacitance；~10pF

* DC power dissipation can be decreased.

Micropower ICs for low-power applications.

* Frequency response, slew rate, and output load C_L are limited.

6. Modified OTA



* Higher G_m and higher open-loop voltage gain.

  $Gm \cong 2g_{m12}(r_{ds34} \,||\, r_{ds12})\, g_{m56}$

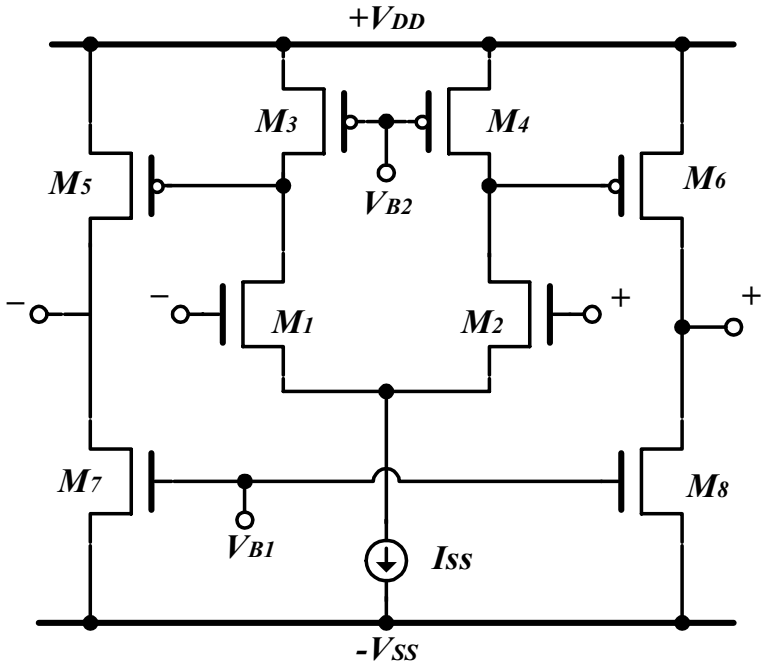
* Frequency compensation is required.
* Designed by Toshiba in C^2MOS ADC.

  Reference ; IEEE JSSC, vol.sc-13, pp.779-785, Dec. 1978

* M_5 (M_7) is matched to M_6 (M_8) => The effect of V_{TH} variations on M_6 and M_8 can be reduced.

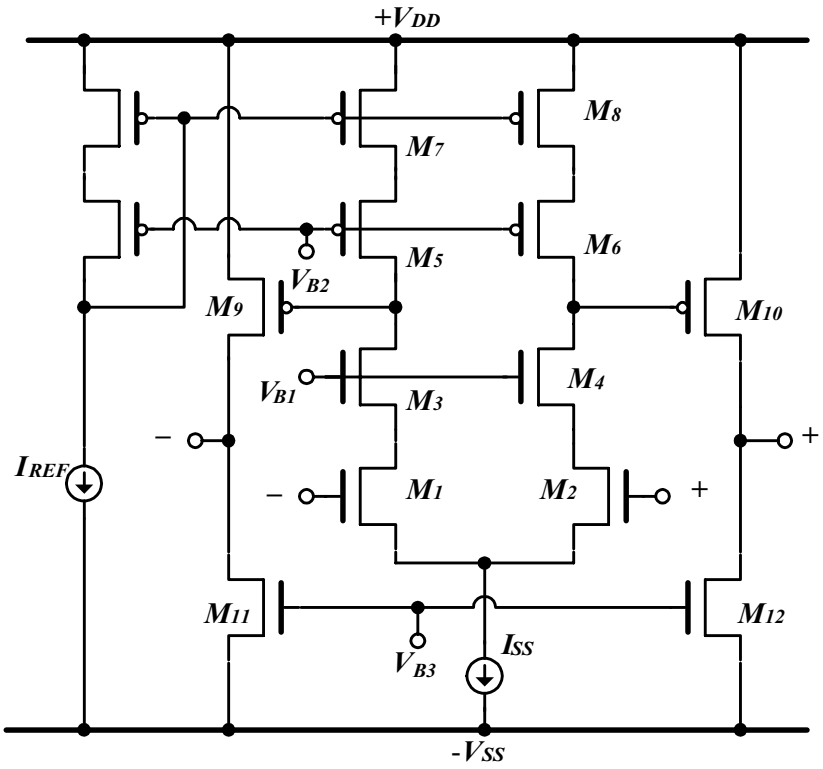
§ 5-3.2 Fully differential OP AMPs

1. Simple OP AMP



* Open-loop gain $A_v \cong g_{m12}(r_{ds12} \,||\, r_{ds34})\, g_{m56}(r_{ds56} \,||\, r_{ds78})$
* Frequency compensation is required.
* CMFB is required.

2. High-gain OP AMP



* Higher gain because of high-swing cascode current-source load.
* If high-swing cascode current source is not used, the design of M_9 and M_{10} is difficult.

  $\because \; V_{GS910} = V_{DS78} + V_{DS56}$

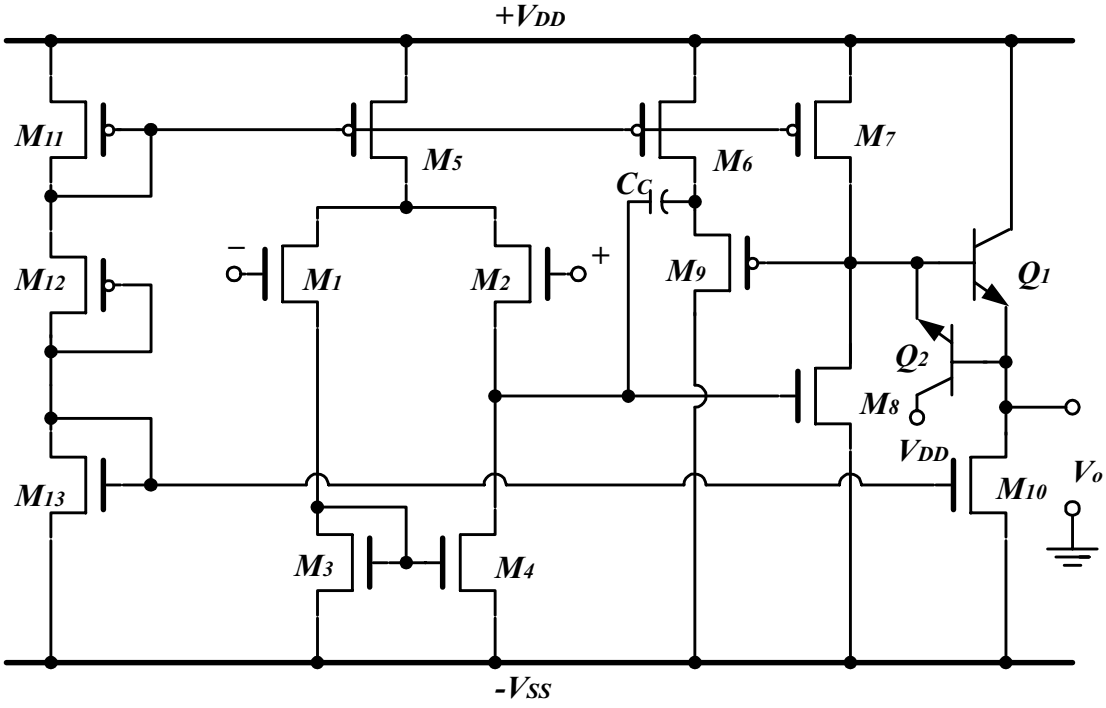
3. General comparion

	Gain	Output Swing	Power Dissipation	Speed	Noise
Telescopic	Medium	Medium	Low	Highest	Low
Folded Cascode	Medium	Medium	Medium	High	Medium
Two-stage	High	Highest	Medium	Low	Lowest
Gain-boosted	High	Medium	High	Medium	Medium

§ 5-4 General-Purpose Three-Stage CMOS OP AMPs

1. Using the emitter follower as output stage

I ;



M_6, M_9, C_C ; Frequency compensation circuit

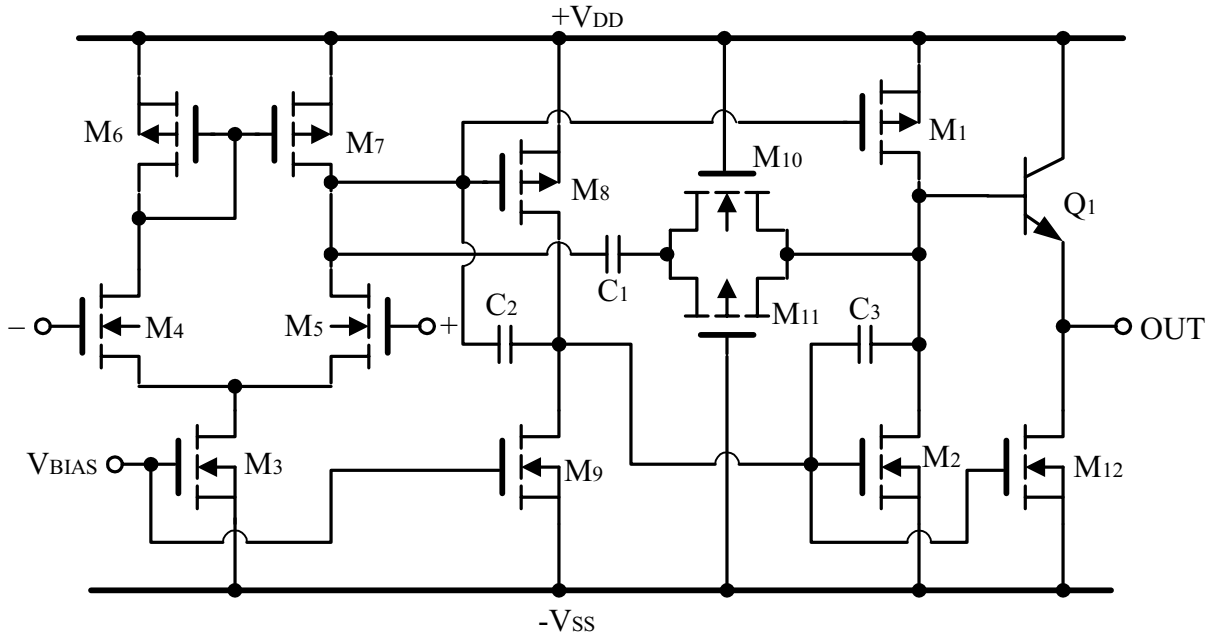
Q_2 ; Protection circuit for Q_1 to avoid the reverse breakdown of B-E junction diode of Q_1.

Q_1, M_{10} ; Emitter follower as output stage.

* Designed by Westinghouse for analog signal processing.

* Open-loop gain = 60db, power dissipation = 16mW.

II.



M10, M11, C1：Frequency compensation circuit.
C2, C3　　：Improving frequency response of Av and PSRR.

§5-5 Common-Mode Feedback (CMFB) Circuits

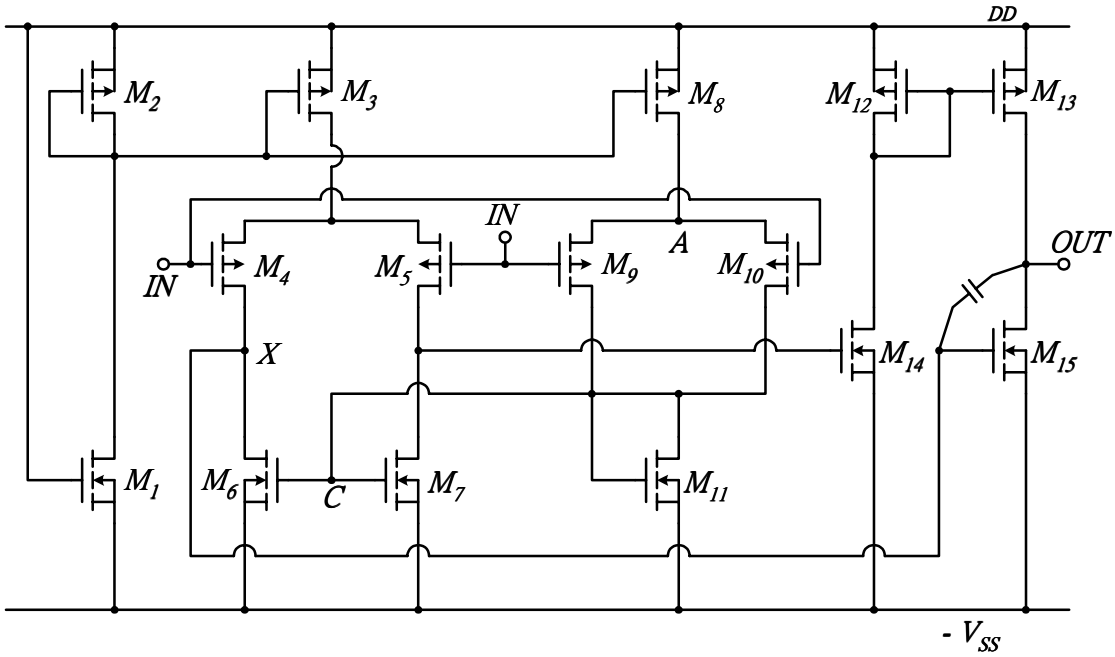
Purposes：1.To provide a stable common-mode level to the nodes.
2.To decrease the common-mode gain.

Design Considerations：

1.To create a negative feedback path only for common-mode signals. For differential signals, CMFB has no effect on circuit performance.
2.To keep power dissipation and chip area of CMFB circuit as low as possible.
3.CMFB is not required in single-ended-output OP AMPs. But it can be used to boost CMRR.
4.CMFB is required in differential-output OP AMPs.

§5-1.1 CMFB circuits for single-ended-output CMOS OP AMPs

1. Reference : IEEE JSSC, vol. sc-13, pp. 779-785, Dec. 1978



M_8, M_9, M_{10}, M_{11} : CMFB circuit

$$M_9 \equiv M_{10} \equiv M_4 \equiv M_5$$

* IN+, IN- ↑ ⇒ X, Y ↑ ⇒ common-mode voltage ↑

IN+, IN- ↑ ⇒ B ↑ ⇒ C ↑ ⇒ X, Y ↓ ⇒ compensation

* For differential signals, A and B are ac grounded

⇒ CMFB circuit has no effect on differential signals.

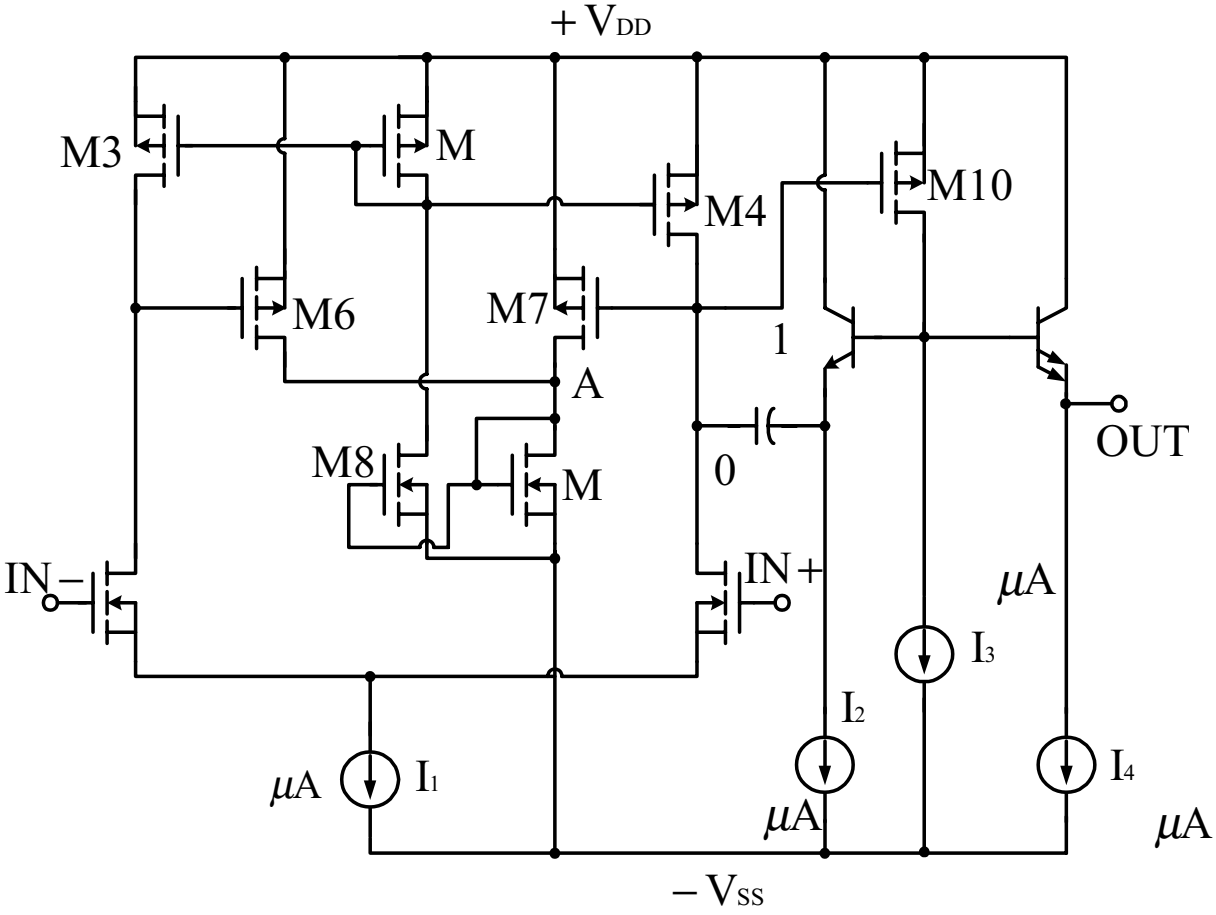
* What is the purpose of M_8 ?

* Designed by Toshiba in C^2MOS ADC

* OP AMP characteristics :

Supply voltage : 5V
Supply current : 150μA
Input common-mode range : +1V ~ +4.5V
Input offset voltage : ± 1mV
CMRR : 75dB
Open-loop gain : 90dB
Output swing : 0 ~ 5V

2.Reference: IEEE JSSC , vol. sc-14, pp. 38-46 , Feb. 1979



Q_1, I_2, C_c : Frequency compensation circuit
M_6, M_7, M_9, M_8, M_5 : CMFB circuit.

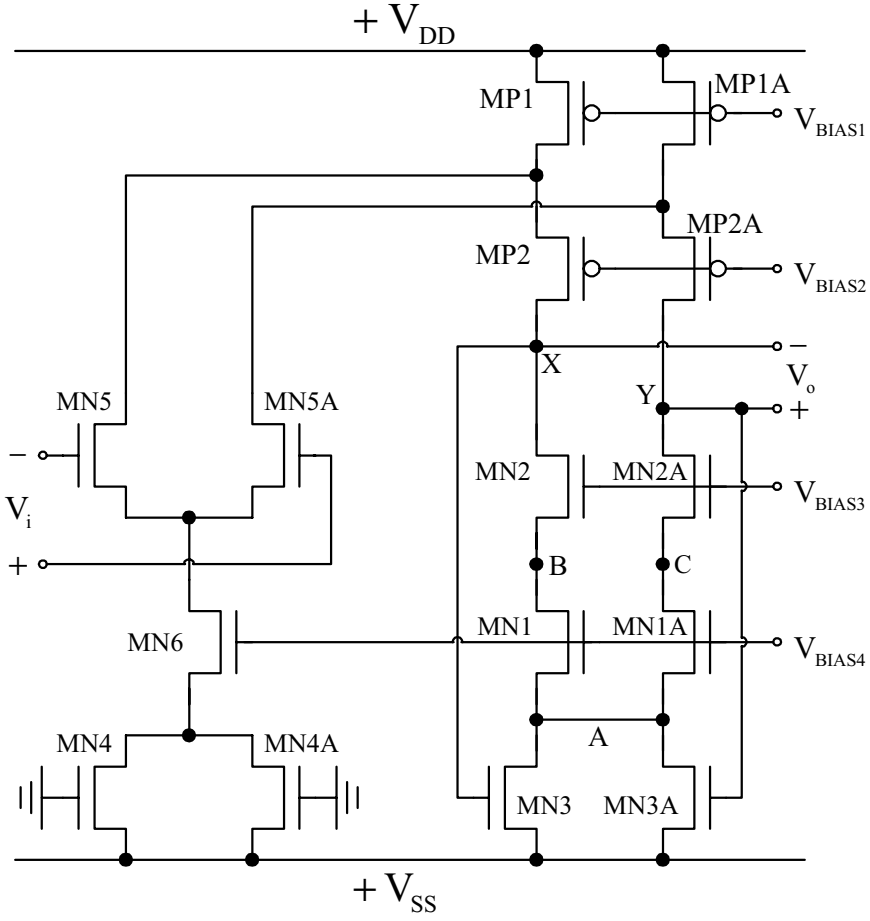
* IN+ , IN- ↑ ➔ X, Y ↓ ➔ common – mode voltage ↓

  ➔ A ↑ ➔ B ↓ ➔ X, Y ↑ ➔compensation.

* For differential signals, A is ac grounded.
  ➔No effect on differential signals.
* Keep $I_{DS6}=I_{DS7}=25$ $_{DS9}=I_{DS8}=I_{DS5}=50$
  and $I_{DS3}=I_{DS4}=25$
* Designed by MOSTEK in PCM Codec.

5-5.2 CMFB circuit for differential-output CMOS OP MP

1. Reference；IEEE JSSC , vol.sc-18 , pp.652-664 , Dec.1983



MN3 , MN3A : CMFB circuit

*Common-mode signals at $X,Y \uparrow \Rightarrow A \downarrow \Rightarrow B,C \downarrow \Rightarrow X,Y \downarrow$

*For differential signals , A is ac grounded.

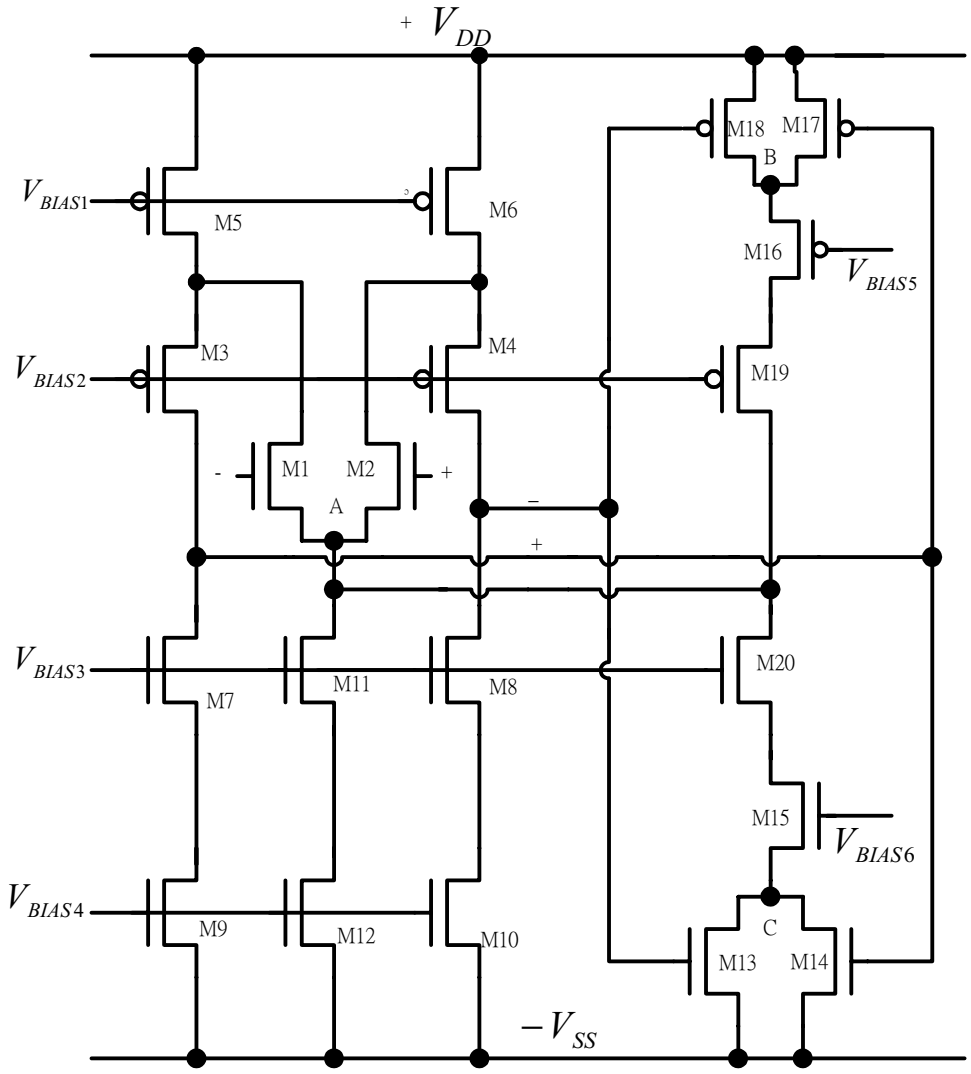
*Why MN4 and MN4A?

*Output swing is decreased by MN3 and MN3A.
To reduce the effect , MN3 and MN3A can be operated in the linear region.

*Output CM level is still a function of device parameters.

*Under differential signals , due to I_{DS} nonlinearity , A is not exactly ac ground $\Rightarrow$ differential characteristics are changed.

2.Reference: IEEE JSSC ,vol.SC-19, pp.912-918, Dec.1984



M13~M20: CMFB circuit

Cascoded common-mode amplifier

*For differential signals,nodes A,B,and C are ac grounded.

3. Resistive CMFB circuit

*For differential signals,

A is ac grounded.

$A_{dm} = g_{m12}(r_{ds12} // r_{ds34} // R_F)$

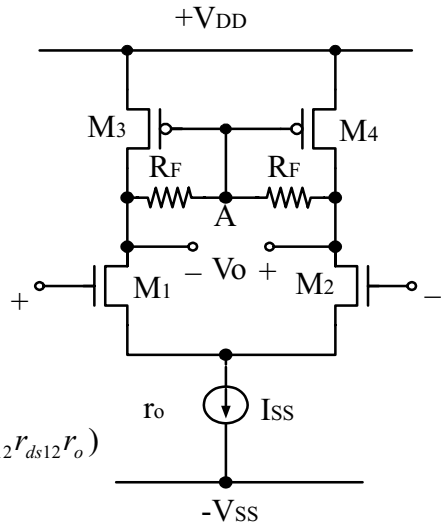
A_{dm} is decreased by R_F

*For CM signals,

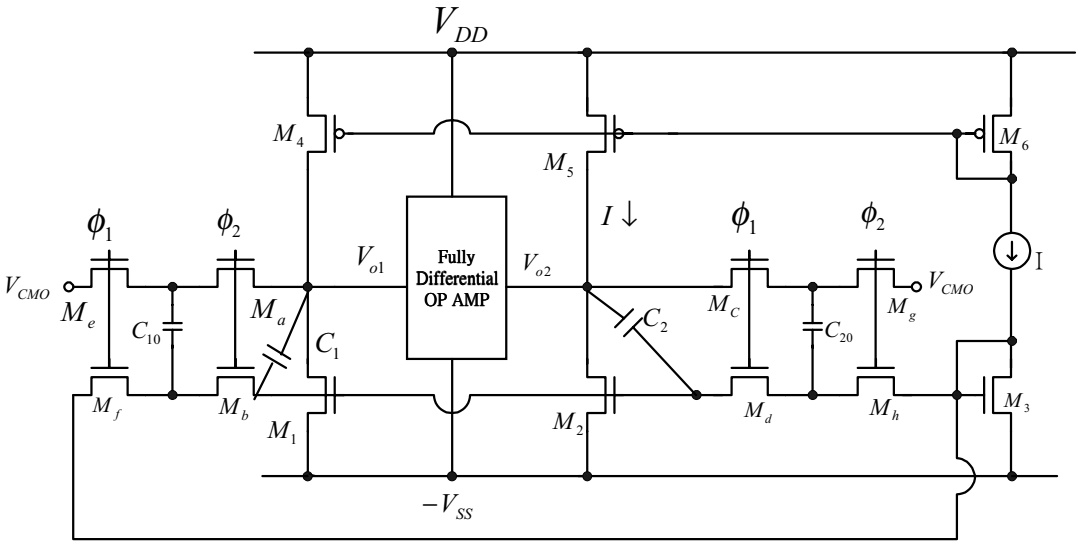
$$A_{cm} \approx -\alpha_{12}\frac{1}{2g_{m34}r_o}$$

smaller than $-\frac{\alpha_{12}}{2r_o}(r_{ds34} // g_{m12}r_{ds12}r_o)$

⇨ CMRR ↑



4. Dynamic CMFB (DCMFB) circuit



Reference: IEEE JSSC, vol. SC-20, pp.1122-1132, Dec.1985

V_{CMO}, ϕ_1, ϕ_2, $M_a \sim M_h$: CMFB circuit

$M_1 \sim M_6$: current sources associated with CMFB circuit

* DCMFB versus static CMFB

1.Less power dissipation.

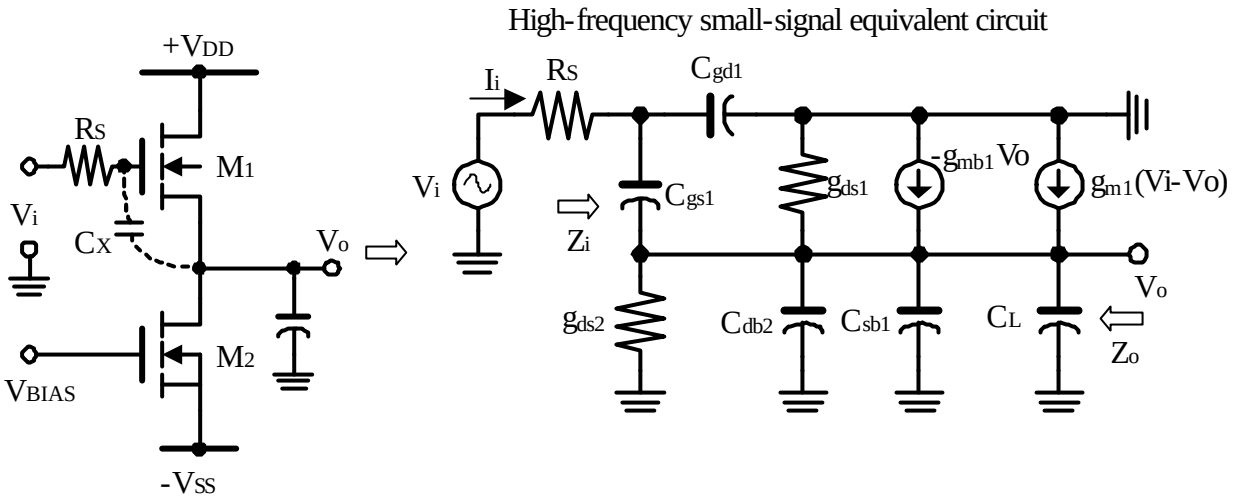
2.Has no effect on output swing, noise, and speed of the OP AMP.

3.ϕ_1, ϕ_2 nonoverlapping clocks are required.

Chapter 6 Frequency Response of MOS Amplifiers

§6-1 Single-Stage Amplifier

§6-1.1 Source follower



$$A_V(s) \equiv \frac{Vo(s)}{Vi(s)} = \frac{sC_{gs1} + g_{m1}}{Rs(C_{gs1}C_{Leq} + C_{gs1}C_{gd1} + C_{gd1}C_{Leq})s^2 + (\frac{g_{m1}}{\alpha_1}RsC_{gd1} + C_{Leq} + C_{gs1})s + g_{m1}/\alpha_1 + G_{Leq}}$$

where $G_{Leq}=g_{ds1}+g_{ds2}$, $C_{Leq}=C_L+C_{sb1}+C_{db2}$

* Left-Half-Plane (LHP) pole: $fp = \frac{G_{Leq} + g_{m1}/\alpha_1}{2\pi(C_{gs1} + C_{Leq})}$

$$\text{LHP zero: } fz = \frac{g_{m1}}{2\pi C_{gs1}}$$

In general, $fp < fz$ $\because C_{Leq} > C_{gs1}$

* If $\frac{C_{Leq}}{C_{gs1}} = (\frac{1}{\alpha_1} - 1) + \frac{G_{Leq}}{g_{m1}}$, we have

fp = fz and $Av(s) \cong \frac{C_{gs1}}{C_{gs1} + C_{Leq}} \cong 1$ indep. of s.

=>Better high frequency response.

How to achieve this?

Adding an extra capacitor Cx such that

$$Cx+C_{gs1}=C_{Leq}\left[\frac{1}{(\frac{1}{\alpha_1}-1)+\frac{G_{Leq}}{g_{m1}}}\right]$$

$$Zi(s)\equiv\frac{Vi(s)}{Ii(s)}=\left[\frac{1}{C_{gs1}s}+\frac{C_{gs1}s+g_{m1}}{C_{gs1}s(G_{Leq}+g_{mb1}+sC_{Leq})}\right]\Big\|(C_{gd1}s)$$

* If $g_{mb1}+G_{Leq}<< C_{Leq}S$ and C_{gd1} is neglected,

$$Zi(s)\cong\frac{1}{C_{gs1}S}+\frac{1}{C_{Leq}S}+\frac{g_{m1}}{C_{gs1}C_{Leq}S^2}$$

The input impedance consists of the series connected

C_{gs1}, C_{Leq}, and the negative resistance

$$-\frac{g_{m1}}{C_{gs1}C_{Leq}\omega^2}$$

Thus oscillation is possible.

* If $g_{mb1}+G_{Leq}$ is neglected, the equivalent input capacitances

$$Cin=Cgd1\Big\|Cin'$$

$$Cin'\cong C_{Leq}\left(\frac{1}{\frac{C_{Leq}}{C_{gs1}}+1+\frac{g_{m1}}{C_{gs1}s}}\right)$$

For large g_{m1}, $C_{in}'<<C_{Leq}$

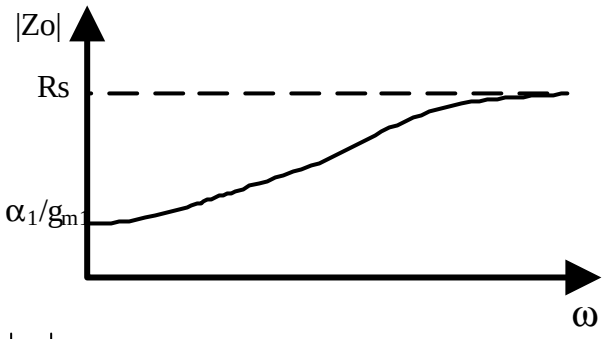
The large load capacitance C_L is well blocked or buffered from the preceding stage.

$$Zo(s)\equiv\frac{Vo(s)}{Io(s)}\Big|_{Vi=0}=\frac{1}{G_{Leq}+g_{mb1}+sC_{Leq}+(sC_{gs1}+g_{m1})\frac{R_sC_{gd1}s+1}{R_s(C_{gd1}s+C_{gs1}s)+1}}$$

* If s = 0, $Zo = Ro = \frac{1}{g_{m1}+g_{mb1}}$

If $s\rightarrow\infty$, Zo'(without C_{Leq})$\cong$ Rs for $Rs<\frac{1}{G_{Leq}+g_{m1}}$ and $C_{gs1}>>C_{gd1}$

Since usually $Rs>\frac{1}{g_{m1}+g_{mb1}}$, we have



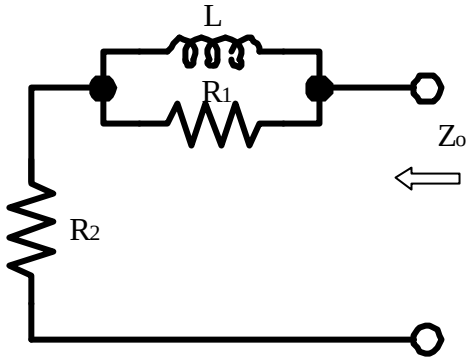
=> |Zo| α ω => Inductive load

$$Zo(s) \cong \frac{R_s C_{gs1} s + 1}{g_{m1}/\alpha_1 + C_{gs1} s}$$

$$R_1 = R_s - \frac{\alpha_1}{g_{m1}}$$

$$R_2 = \frac{\alpha_1}{g_{m1}}$$

$$L = \frac{C_{gs1}\alpha_1}{g_{m1}}\left(R_s - \frac{\alpha_1}{g_{m1}}\right)$$



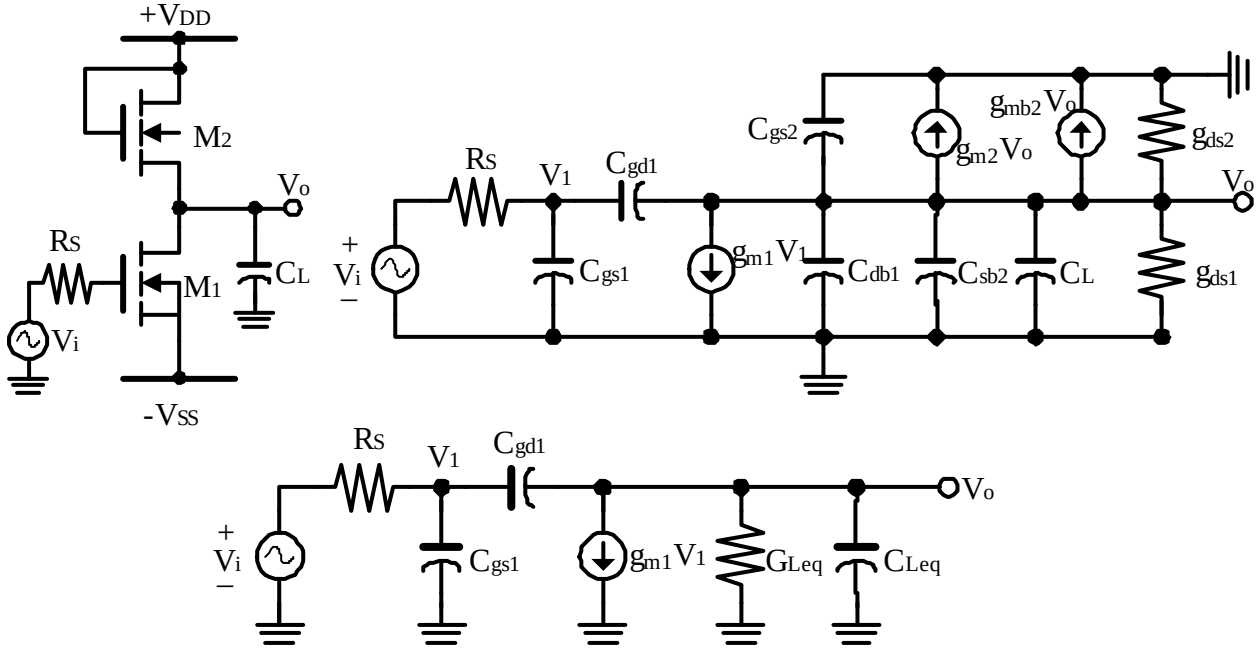
L and C_L causes output signal ringing.

* Two source followers in cascade might cause oscillation because

First SF ： L in Zo 1

Second SF ：-R and Cin Z_{i2}

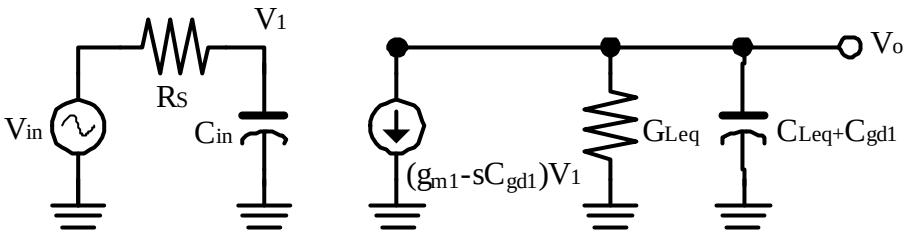
§6-1.2 Enhancement－load NMOS common-source gain stage



$G_{Leq}=g_{ds1}+g_{ds2}+g_{m2}+g_{mb2}$

$C_{Leq}=C_{db1}+C_{gs2}+C_{sb2}+C_L$

Applying the Miller's theorem, we have



$C_{in}=C_{gs1}+C_{gd1}(1+g_{m1}/G_{Leq})$

$$=>Av(s)\cong\frac{G_s(sC_{gd1}-g_{m1})}{(sC_{in}+G_s)\left[s(C_{Leq}+C_{gd1})+C_{Leq}\right]}$$

* Right-Half-Plane Zero：$Sz = g_{m1}/C_{gd1}$
* Left-Half-Plane Poles ：$S_{p1}=-G_s/C_{in}$ (input pole)

$S_{p2}=-G_{Leq}/(C_{Leq}+C_{gd1})$ (output pole).

If C_{gd1} and C_{Leq} are small $=>S_{p1}$ is the dominant pole.

* If C_L is large, the dominate pole is $S_{p2}\cong(g_{m2}+g_{mb2})/C_L$
* The input impedance can be approximated by

$$Zin\cong\frac{1}{\left[C_{gs1}+(1+g_{m1}\frac{1}{G_{Leq}})C_{gd1}\right]s}$$ near the upper 3dB frequency.

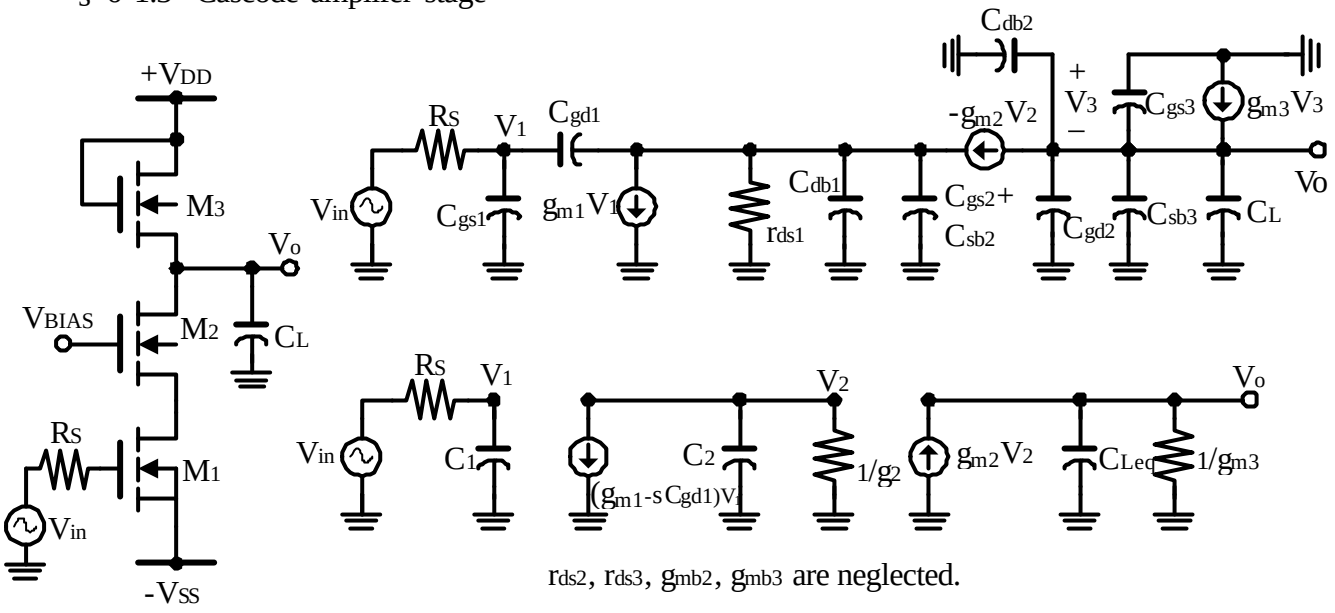
* The exact Zin is

$$Zin\cong C_{gs1}s\left\|\left[\frac{1+\frac{1}{G_{Leq}}(C_{gd1}+C_{Leq})s}{C_{gd1s}(1+g_m\frac{1}{G_{Leq}}+\frac{1}{G_{Leq}}C_{Leq}s)}\right]\right.$$

If $\left|\frac{1}{G_{Leq}}(C_{gd1}+C_{Leq})s\right|$ <<1 and $\left|\frac{1}{G_{Leq}}C_{gds1}s\right|<<(1+gm\frac{1}{G_{Leq}})$,

Zin can be approximated by the previous formula.

§ 6-1.3 Cascode amplifer stage



r_{ds2}, r_{ds3}, g_{mb2}, g_{mb3} are neglected.

$$g_2 = g_{m2} + \frac{1}{r_{ds1}}$$

$$C_2 = C_{gs1} + (1 + \frac{g_{m1}}{g_{m2}})C_{gd1}$$

$$C_2 = C_{gd1} + C_{db1} + C_{gs2} + C_{sb2}$$

$$C_{Leq} = C_L + C_{gd2} + C_{db2} + C_{sb3} + C_{gs3}$$

$$A_v(s) = \frac{-G_s g_{m2}(sC_{gd1} - g_{m1})}{(sC_1 + G_s)(sC_2 + g_2)(sC_{Leq} + g_{m3})}$$

RHP Zero: $S_z = \frac{g_{m1}}{C_{gd1}}$

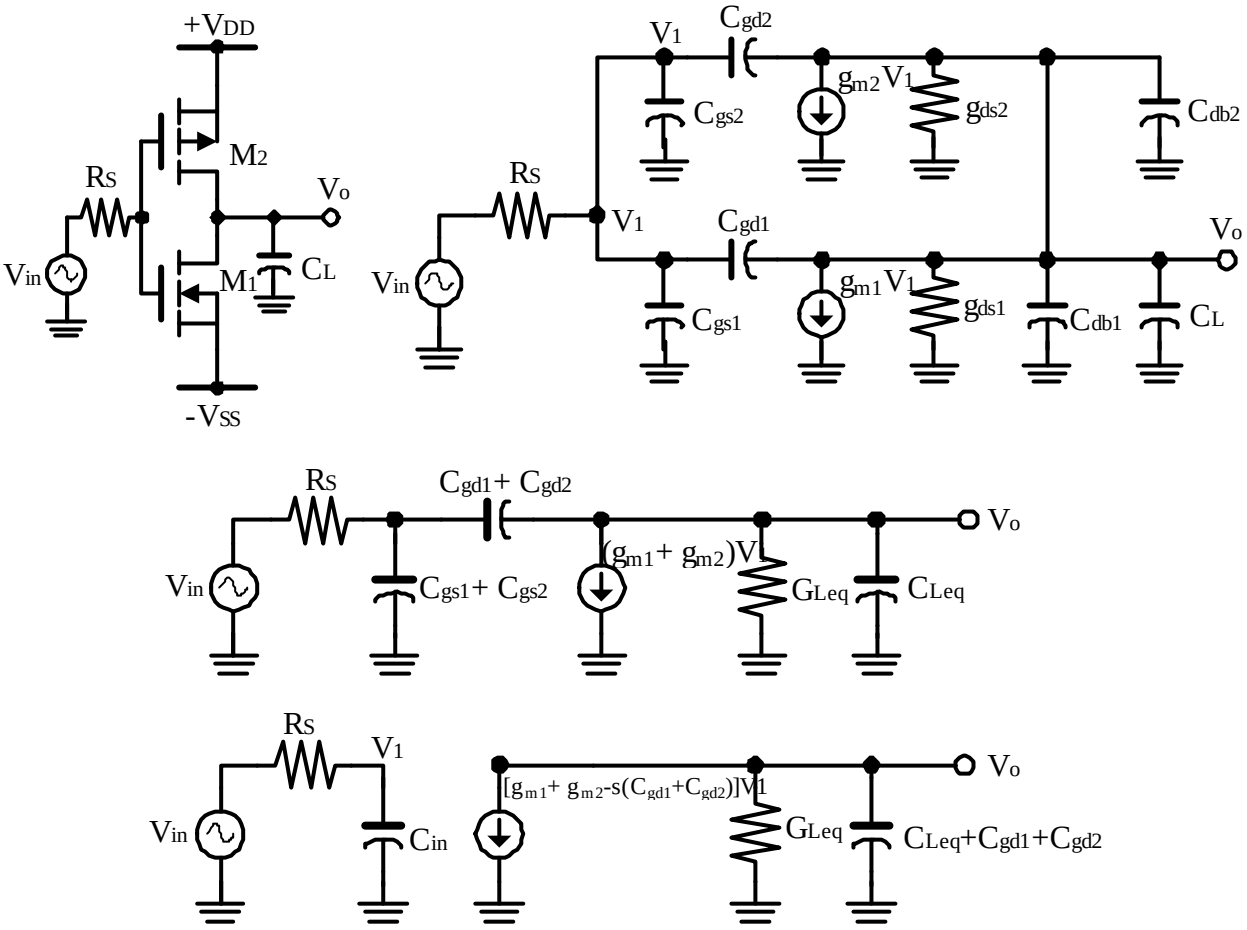
LHP Pole : $S_{p1} = -\frac{G_s}{C_1}$; $S_{p2} = -\frac{g_2}{C_2}$; $S_{p3} = \frac{-g_{m3}}{C_{Leq}}$

S_{p1} usually is the dominant pole.

$$\Rightarrow f_{3dB} \cong \frac{|S_{p1}|}{2\pi} = \frac{G_s}{2\pi C_1}$$

* Typically, $g_{m1} = g_{m2}$, then $C_1 = C_{gs1} + 2C_{gd1}$

§ 6-1.4 CMOS gain stage



$$G_{Leq} = g_{ds1} + g_{ds2} \qquad C_{Leq} = C_{db1} + C_{db2} + C_L$$

$$C_{in} = C_{gs1} + C_{gs2} + (1 + \frac{g_{m1} + g_{m2}}{G_{Leq}})(C_{gd1} + C_{gd2})$$

$$A_v(s) \cong \frac{G_s[s(C_{gd1} + C_{gd2}) - (g_{m2} + g_{m2})]}{[s(C_{gd1} + C_{gd2} + C_{Leq}) + G_{Leq}](sC_{in} + G_s)}$$

RHP Zero: $S_z = \dfrac{g_{m1} + g_{m2}}{C_{gd1} + C_{gd2}}$

LHP Poleo: $S_{p1} = -\dfrac{G_s}{C_{in}}$

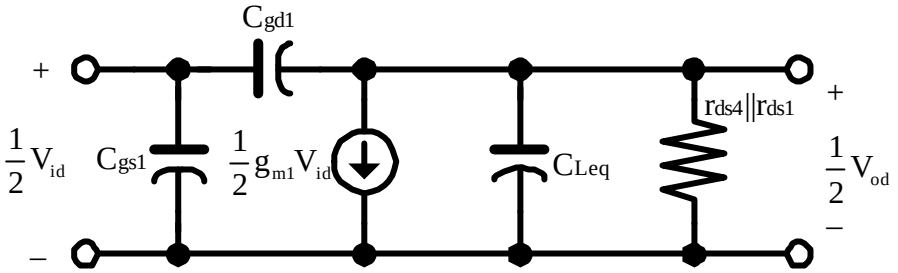
$$S_{p2} = -\frac{G_{Leq}}{C_{gd1} + C_{gd2} + C_{Leq}}$$

If R_s is large enough (R_s is the output resistance of the preceding stage),
$|S_{p1}| << |S_{p2}|$

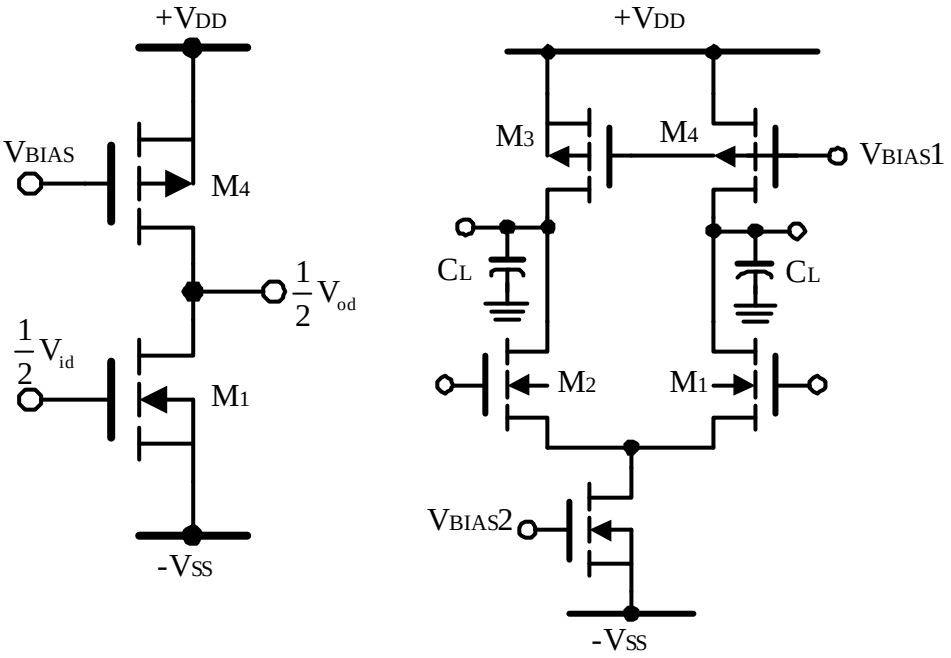
S_{p1} is the dominant pole.

§ 6-1.5 CMOS differential amplifier

1.Differential-mode half circuit



$$C_{Leq} \equiv C_L + C_{db4} + C_{db1}$$

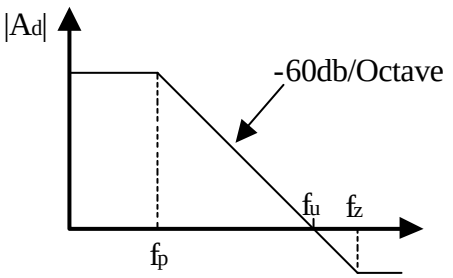


$$A_d = \frac{V_{od}}{V_{id}} = H(s) = -\frac{g_{m1}}{g_{ds4}+g_{ds1}}\left[\frac{1-s\frac{C_{gd1}}{g_{m1}}}{1+(\frac{C_{Leq}+C_{gd1}}{g_{ds4}+g_{ds1}})s}\right]$$

RHP Zero: $f_z = \frac{g_{m1}}{2\pi C_{gd1}}$ $\quad f_z > f_p$

LHP Pole: $f_p = \frac{g_{ds4}+g_{ds1}}{2\pi(C_{db4}+C_{db1}+C_L+C_{gd1})}$

$f_u \quad A_0 f_p = \frac{g_{m1}}{2\pi(C_{db4}+C_{db1}+C_L+C_{gd1})}$



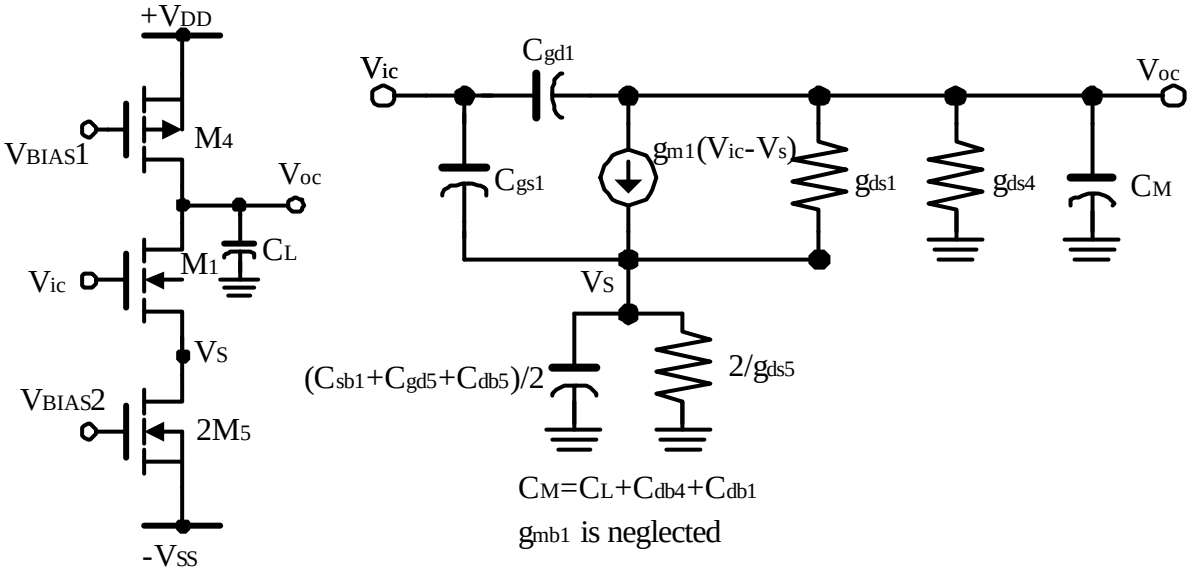
2.Common-mode half circuit:

$$(g_{ds4}+sC_M)V_{oc} + g_{ds1}(V_{oc}-V_s) + g_{m1}(V_{ic}-V_s) + C_{gd1}s(V_{oc}-V_{ic}) = 0$$

$$g_{ds1}(V_s - V_{oc}) + V_s(\frac{1}{2r_{ds5}} + \frac{C_{gd5} + C_{db5} + C_{sb1}}{2}s) - g_{m1}(V_{ic} - V_s) - C_{gs1}s(V_{ic} - V_s) = 0$$

$$V_s[\frac{1}{2r_{ds5}} + \frac{1}{2}(C_{gd5} + C_{db5} + C_{sb1})s + C_{gs1}s] = -[g_{ds4} + sC_M + sC_{gd1}]V_{oc} + (C_{gs1}s + C_{gd1}s)V_{ic}$$

$$V_s = -\frac{[g_{ds4} + sC_M + sC_{gd1}]V_{oc} - (C_{gs1}s + C_{gd1}s)V_{ic}}{\left[\frac{1}{2r_{ds5}} + \frac{C_{gd5} + C_{db5} + C_{sb1}}{2}s + C_{gs1}s\right]}$$



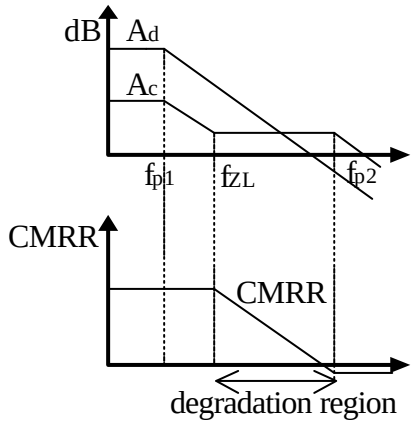
$C_M = C_L + C_{db4} + C_{db1}$

g_{mb1} is neglected

$$\Rightarrow A_c(s) = \frac{V_{oc}}{V_{ic}} = -\frac{-C_{gd1}(\frac{C_{gd5} + C_{db5} + C_{sb1}}{2} + C_{gs1})s^2 + [(\frac{C_{gd5} + C_{db5} + C_{sb1}}{2} + C_{gs1})g_{m1}}{(\frac{C_{gd5} + C_{db5} + C_{sb1}}{2} + C_{gs1})(C_M + C_{gd1})s^2 + [(\frac{C_{gd5} + C_{db5} + C_{sb1}}{2} + C_{gs1})}$$

$$\frac{-\frac{1}{2r_{ds5}}C_{gd1} - (g_{ds1} + g_{m1})(C_{gs1} + C_{gd1})]s + \frac{1}{2r_{ds5}}g_{m1}}{(g_{ds4} + g_{ds1}) + \frac{C_M + C_{gd1}}{2r_{ds5}} + (C_M + C_{gd1})(g_{ds1} + g_{m1})]s + \frac{g_{ds4} + g_{ds1}}{2r_{ds5}} + (g_{ds1} + g_{m1})g_{ds4}}$$

Solve the pole-zero position : $\Rightarrow$ 1 RHP zero, 1 LHP zero,2 LHP poles



f_{ZR} f_{ZL} f_{p1} f_{p2}

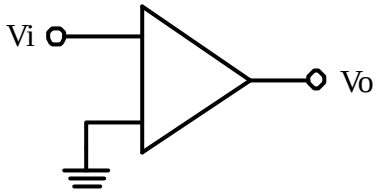
$f_{ZR} >> f_{ZL}$

f_{p1}: C_M f_{p2}: $(C_{gd5}+C_{db5}+C_{sb1})/2$

$f_{p1} < f_{p2}$

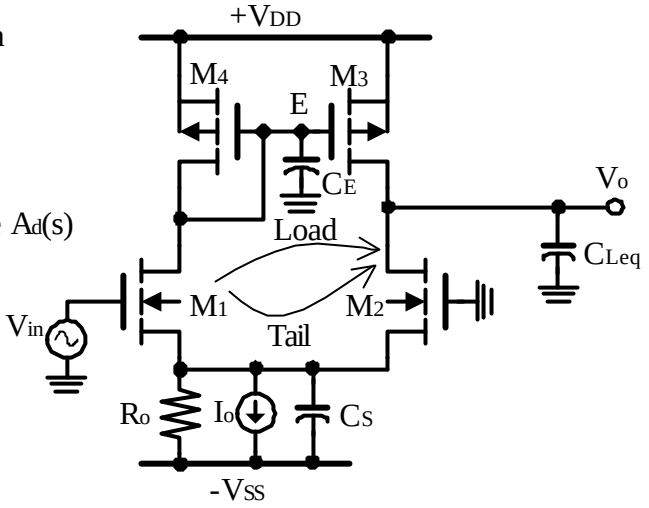
Load pole tail pole

§ 6-1.6 CMOS differential-input-to-single-ended output converter



$$V_i = V_{id} + V_{ic} \quad V_o = V_{od} + V_{oc}$$

* The hail-circuit method cannot be used in the high frequency analysis.
* Two unequal signal paths to the output
  - $\Rightarrow$ Load path and tail path
  - $\Rightarrow$ Both C_s and C_E appears in the $A_d(s)$ expression.
* There are two dominate poleo in A_d.



Output pole $W_{p1} \cong \dfrac{g_{ds1} + g_{ds4}}{C_{Leq}}$

Mirror pole $W_{p2} \cong \dfrac{g_{m34}}{C_E}$

Tail path: $A_1(s) = \dfrac{A_0}{1 + \dfrac{s}{W_{p1}}}$

Load path: $A_2(s) = \dfrac{A_0}{(1 + \dfrac{s}{W_{p1}})(1 + \dfrac{s}{W_{p2}})}$

$$A_d(s) = A_1(s)A_s(s) = \frac{A_0(2 + \dfrac{s}{W_{p2}})}{(1 + \dfrac{s}{W_{p1}})(1 + \dfrac{s}{W_{p2}})}$$

LHP zero: $W_{z1} \cong \dfrac{2g_{m34}}{C_E} = 2W_{p2}$

* Approximate analysis:

The dominant pole of $A_d(s)$ is $S_{p1} = -\dfrac{g_{ds1} + g_{ds4}}{C_{Leq}}$ (output pole)

$$A_d(s) \cong \frac{g_{m1}}{sC_{Leq} + (g_{ds1} + g_{ds4})}$$

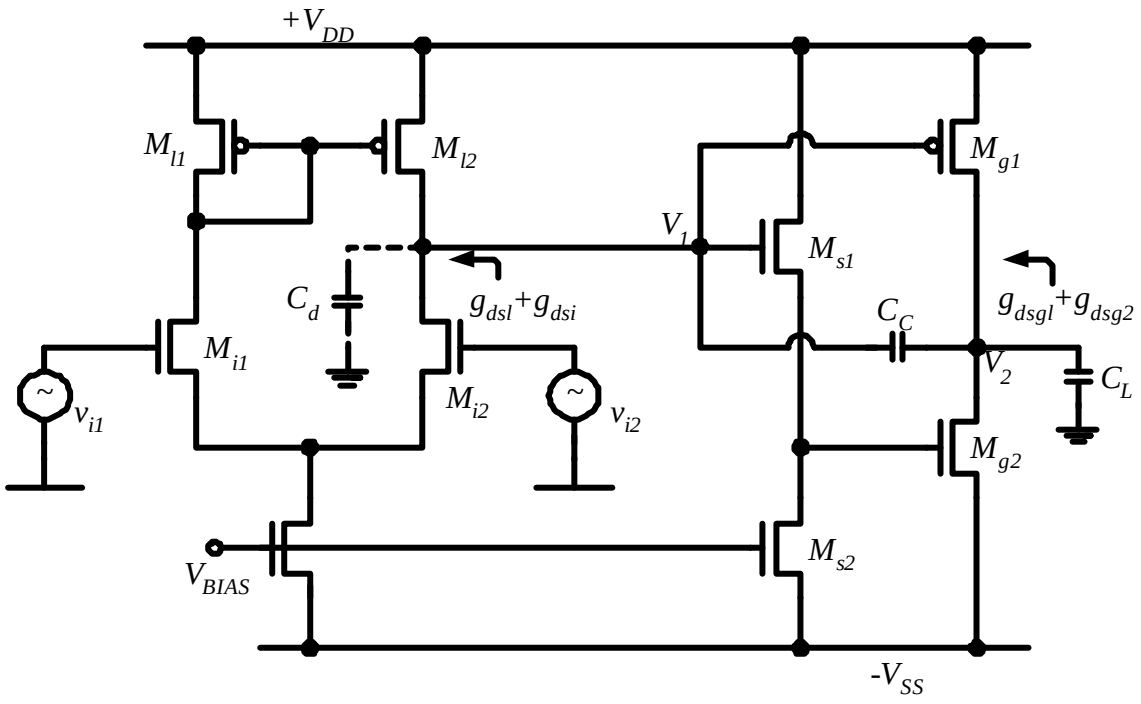
The $A_c(s)$ can be written as $A_c(s) \cong -\frac{g_{ds1}}{2g_{m4}} \frac{(\frac{1}{R_0}) + sC_s}{sC_{Leq} + (g_{ds1} + g_{ds4})}$

The dominant pole of $A_c(s)$ is $S_{p1} = -\frac{g_{ds1} + g_{ds4}}{C_{Leq}}$

But the left-half-plane zero is $S_{zL} = -\frac{1}{R_0}(\frac{1}{C_s})$

The CMRR$(\equiv \frac{A_d}{A_c})$ is degradated by 20dB/decade at high frequency.

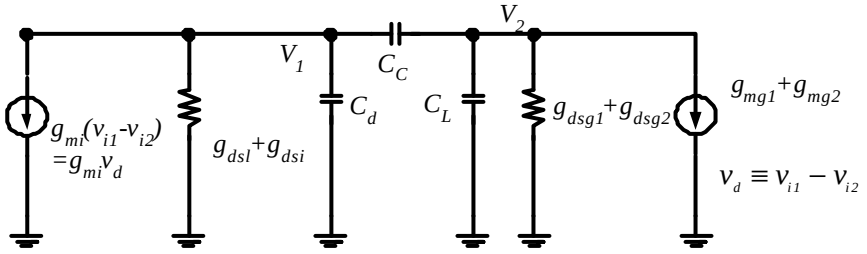
§6-2 Frequency Compensations



Without C_C

$$S_{P1} = -\frac{1}{C_d}(g_{dsl} + g_{dsi}) \ , \quad S_{P2} = -\frac{1}{C_L}(g_{dsg1} + g_{dsg2})$$

equivalent circuit



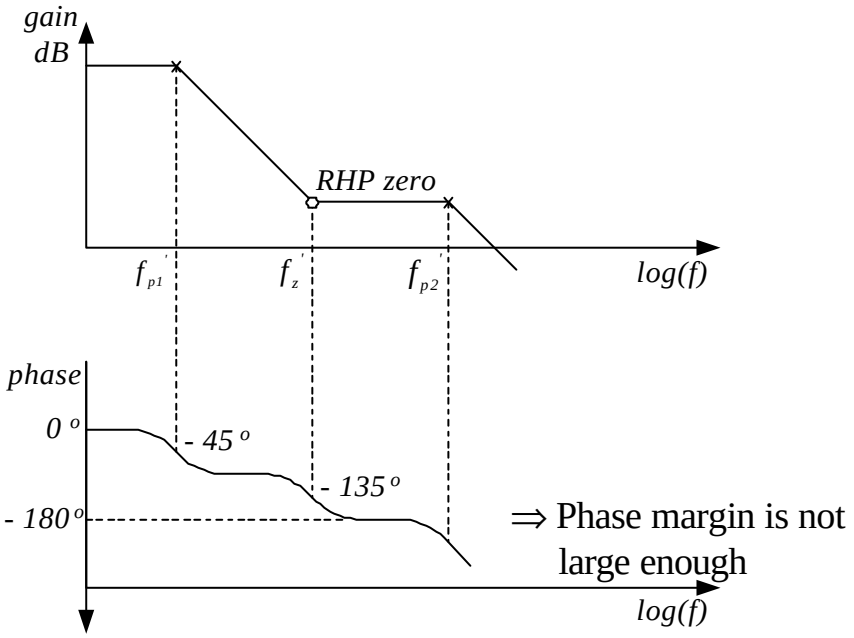
$$H(s)=\frac{v_2}{v_{i1}-v_{i2}}$$

$$=\frac{+g_{mi}(g_{mg1}+g_{mg2})R_dR_o(1-\dfrac{sC_C}{g_{mg1}+g_{mg2}})}{1+s[(C_L+C_C)R_O+(C_C+C_d)R_d+C_C(g_{mg1}+g_{mg2})R_OR_d]+(C_CC_L+C_CC_d+C_dC_L)R_OR_ds^2}$$

where $R_o \equiv -\dfrac{1}{g_{dsg1}+g_{dsg2}}$ $\qquad$ $R_d \equiv -\dfrac{1}{g_{dsl}+g_{dsi}}$

$$\Rightarrow \quad S_{p1}' \approx -\frac{1}{(g_{mg1}+g_{mg2})R_OR_dC_C} \qquad S_{p2}' \approx -\frac{C_C(g_{mg1}+g_{mg2})}{C_OC_L+C_dC_L+C_dC_C}$$

$$S_z' \approx \frac{g_{mg1}+g_{mg2}}{C_C} \quad \rightarrow \text{RHP Zero}$$



$\Rightarrow$ Phase margin is not large enough

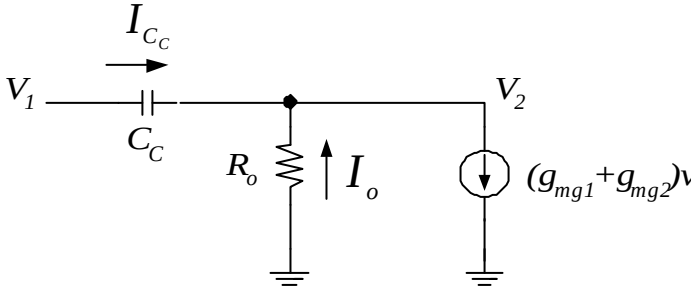
* Feedforward effect on C_C

How to solve this problem ?

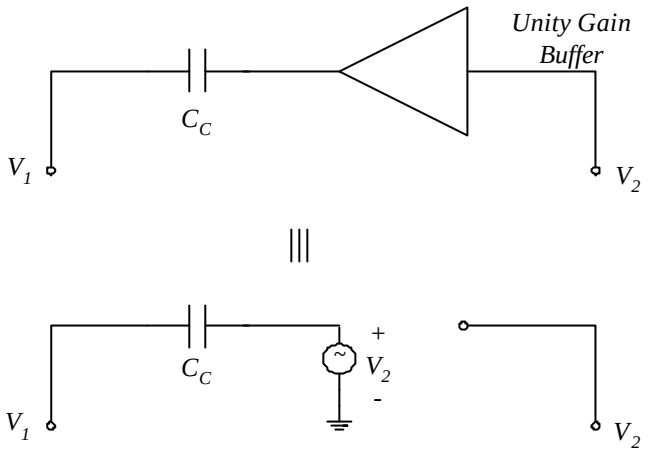
If $I_{C_C}=(g_{mg1}+g_{mg2})V_d$,

$I_o=0$ and $V_2=0$

$\Rightarrow$ A zero is formed.



§6-2.1 Using a unity-gain buffer in the feedback path



* Isolate node 1 from node 2 to prevent feedforward.
* Keep the Miller effect unchanged.
* Source follower can act as a unity gain buffer.

$$g_{mi}V_d + \frac{V_1}{R_d} + C_d sV_1 + (V_1 - V_2)C_c s = 0 \qquad \text{--------- (1)}$$

$$(g_{mg1} + g_{mg2})V_1 + \frac{1}{R_o}V_2 + C_L sV_2 = 0 \qquad \text{--------- (2)}$$

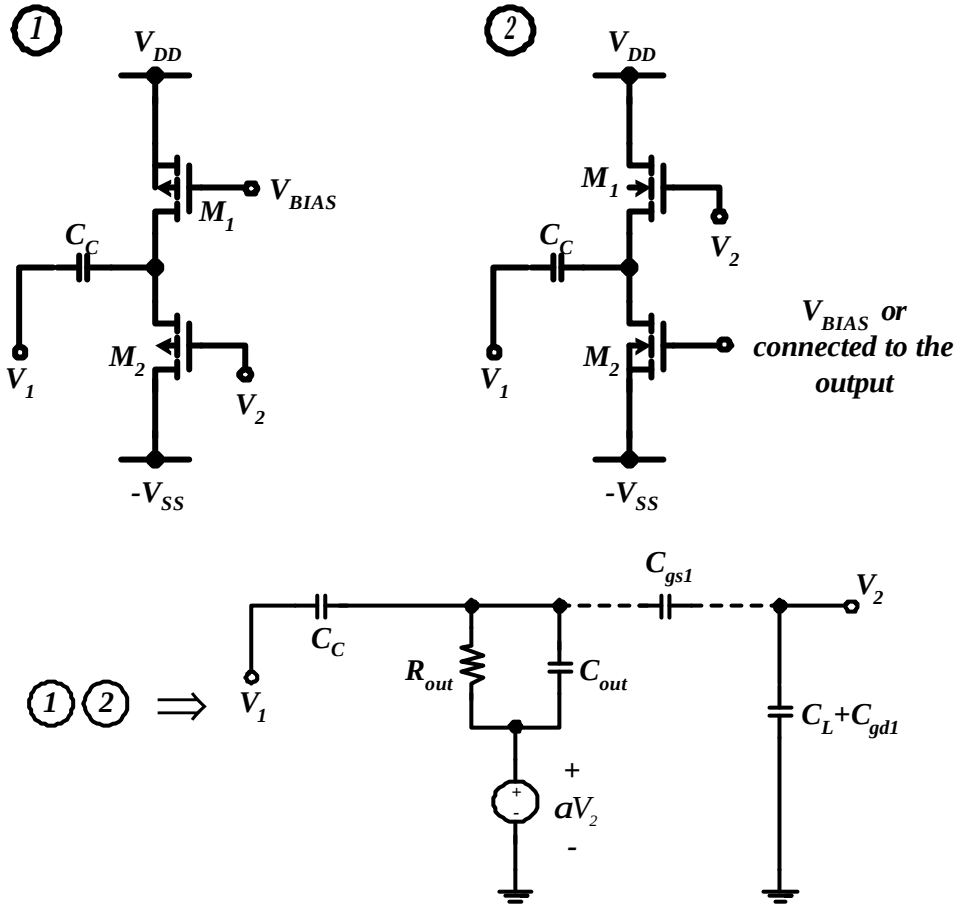
$$H(s) = \frac{V_2}{V_d}$$

$$= \frac{g_{mi}(g_{mg1} + g_{mg2})}{1 + s\left[R_o C_c + R_d(C_d + C_c) + C_c(g_{mg1} + g_{mg2})R_o R_d\right] + (C_c C_L + C_d C_L)R_o R_d s}$$

$$S_{p1}' \approx -\frac{1}{(g_{mg1} + g_{mg2})R_o R_d C_c} \quad \text{(unchanged)}$$

$$S_{p2}' \approx -\frac{C_c(g_{mg1} + g_{mg2})}{C_c C_L + C_d C_L} \qquad \text{RHP Zero has be eliminated.}$$

Actual Circuits :



* C_{gs1} may introduce a RHP zero. But usually this RHP zero is large.

∵ C_{gs1} is very small.

* $R_{out} \approx (\frac{1}{g_{m1}} \| \frac{1}{g_{m2}})$

$$g_{mi}V_d + \frac{V_1}{R_d} + C_d s V_1 + (V_1 - aV_2)(\frac{1}{C_c s} + \frac{1}{\frac{1}{R_{out}} + C_{out}s})^{-1} = 0$$

If $\frac{1}{R_{out}} \geq C_{out}s$

$$\Rightarrow \left(\frac{1}{C_c s} + \frac{1}{\frac{1}{R_{out}} + C_{out}s} \right)^{-1} \approx \frac{C_c s}{C_c R_{out} s + 1}$$

The numerator of $H(s)=\frac{V_2(s)}{V_d(s)}$ is $g_{mi}(g_{mg1}+g_{mg2})(C_cR_{out}s+1)$

$\Rightarrow$ LHP Zero : $-\frac{1}{C_cR_{out}}$

If R_{out} is large , LHP Zero may form a pole-zero doublet with S_{p1}' or S_{p2}'

$\Rightarrow$ very slow slew rate !!

If R_{out} is small , too large g_{m1} or g_{m2} is required.

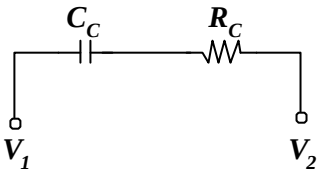
$\Rightarrow$ (large area ,large power)

$\Rightarrow$ large C_{out}. Freq. Resp. $\downarrow$

* Somehow difficult to design.

* Also the power dissipation of the buffer is large. (additional power dissipation)

§6-2.2 Adding Rc in series with Cc.



$H(s)=\frac{v_2}{v_d}$ can be solved.

Low frequency gain : $A_{dm}=g_{mi}(g_{mg1}+g_{mg2})R_oR_d$

LHP Poles : $S_{P1}\cong\frac{-1}{(g_{mg1}+g_{mg2})R_oR_dC_c}$ (unchanged)

$$S_{P2}\cong-\frac{(g_{mg1}+g_{mg2})C_c}{C_dC_L+C_cC_L+C_dC_c}$$ (unchanged)

$$S_{P3}\cong-\frac{C_dC_c+C_dC_L+C_cC_L}{R_CC_dC_LC_c}$$

$$\begin{pmatrix}LHP\\RHP\end{pmatrix}Zero: S_Z=-\frac{g_{mg1}+g_{mg2}}{C_c[R_c(g_{mg1}+g_{mg2})-1]}$$

1. If $R_C = \dfrac{1}{g_{mg1} + g_{mg2}}$ or $R_C = \dfrac{1}{g_{m2}}$ g_{m2} : second-stage transconductance

$S_Z \to \pm\infty$ No effect on the frequency response of the OP.

S_{P1} dominant pole $\Rightarrow$ $A_d(s) \cong \dfrac{A_{dm}}{\dfrac{s}{S_{P1}} + 1} = \dfrac{A_{do} S_{P1}}{s + S_{P1}}$

For $w >> S_{P1}$ $A_d(jw) = \dfrac{A_{dm} S_{P1}}{jw}, |A_d(jw)| = \dfrac{A_{dm} S_{P1}}{w}$

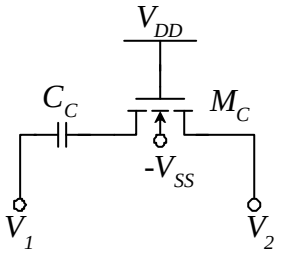
At w_u , $|A_d(jw_u)| = 1$ $\Rightarrow$ $w_u = A_{dm} S_{P1} = \dfrac{g_{mi}}{C_c}$

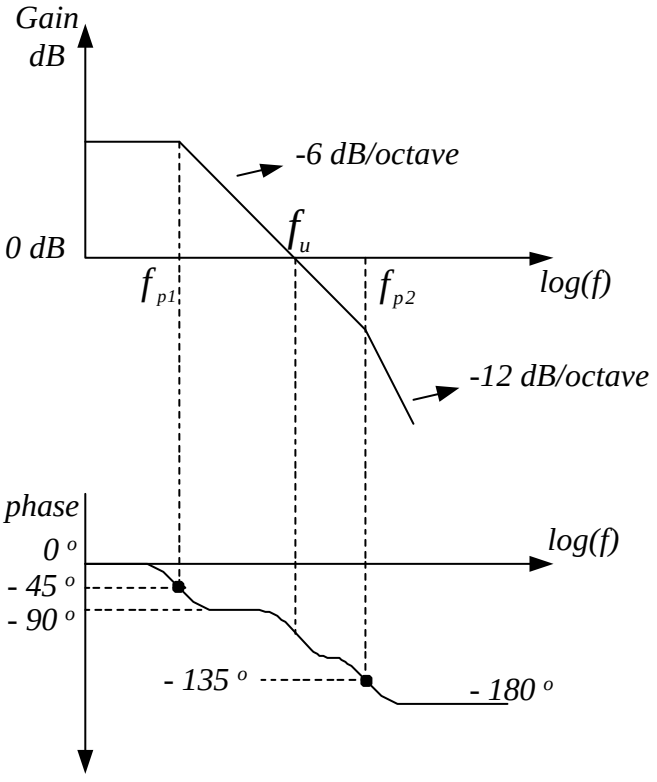
Large $C_L \Rightarrow S_{P2} \approx -\dfrac{g_{mg1} + g_{mg2}}{C_L}$

For phase margin $45^0 \sim 60^0$ $\Rightarrow$ $\dfrac{S_{P2}}{w_u} \cong 2 \sim 4, \dfrac{C_c}{C_L} \dfrac{g_{mg1} + g_{mg2}}{g_{mi}} = 2 \sim 4$

If $\dfrac{g_{mi}}{g_{mg1} + g_{mg2}} \cong 2 \sim 4$, $C_L \cong C_c$ stable

1) NMOS Realization :

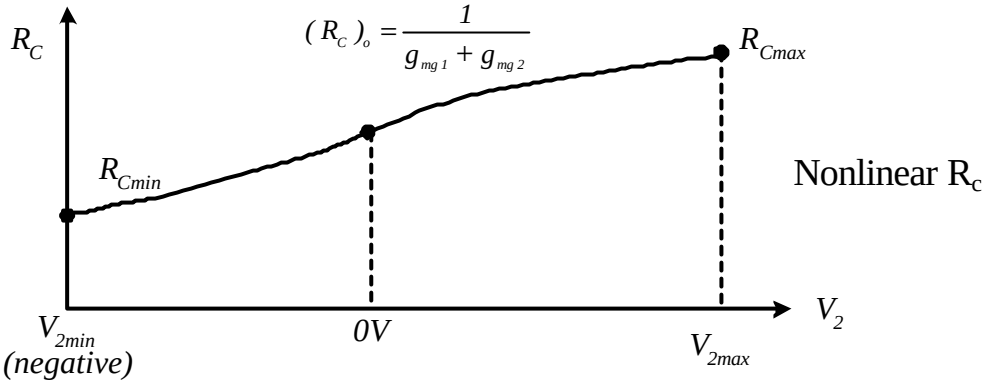




$$I_{DS} = \frac{m_n C_{ox}}{2}\frac{W}{L}\left[2(V_{DD} - V_2 - V_{TH})V_{DS} - V_{DS}^{\ 2}\right] ,$$

$$R_C = \left(\frac{\partial I_{DS}}{\partial V_{DS}}\right)^{-1}\Bigg|_{V_{DS}=0} = \frac{1}{\frac{m_n C_{ox}}{2}\frac{W}{L}\left[2(V_{DD} - V_2 - V_{TH})\right]}$$

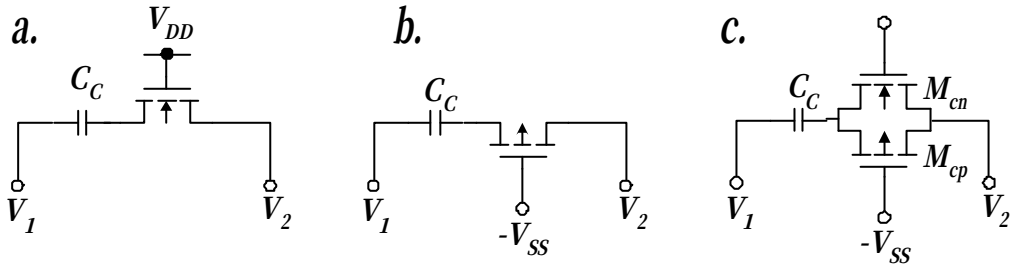
$V_2 \uparrow$ $V_{TH} \uparrow$ body effect



Design R_c : (1) Design R_c, s.t. $(R_c)_{V_2=0V} = \frac{1}{g_{m2}}\left(\frac{1}{g_{mg1} + g_{mg2}}\right)$

(2) At $R_c = R_{cmax}$ or R_{cmin} ,
S_z must be large enough ! Otherwise, frequency performance will be degradated.

1) CMOS Realizations :



Consider the case in *c.*:

$$I_{DSn} = \frac{m_n C_{ox}}{2}\frac{W_n}{L_n}\left[2(V_{DD} - V_2 - V_{THn})V_{DS} - V_{DS}^{\ 2}\right]$$

$$R_{cn} = \frac{1}{\frac{m_n C_{ox}}{2}\frac{W_n}{L_n}\left[2(V_{DD} - V_2 - V_{THn})\right]}$$

$$I_{DSp} = \frac{m_p C_{ox}}{2}\frac{W_p}{L_p}[2(V_2 + V_{SS} - V_{THp})V_{DS} - V_{DS}^{\ 2}]$$

$$R_{cp} = \frac{1}{\frac{m_p C_{ox}}{2}\frac{W_p}{L_p}[2(V_2 + V_{SS} - V_{THp})]}$$

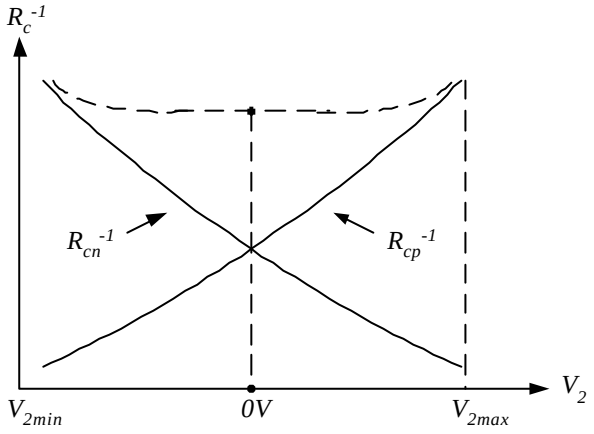
$$R_c^{-1} = (R_{cn} // R_{cp})^{-1} = R_{cn}^{-1} + R_{cp}^{-1}$$

$$= \frac{m_n C_{ox}}{2}\frac{W_n}{L_n}[2(V_{DD} - V_2 - V_{THn})] + \frac{m_p C_{ox}}{2}\frac{W_p}{L_p}[2(V_2 + V_{SS} - V_{THp})]$$

If $\frac{m_n C_{ox}}{2}\frac{W_n}{L_n} = \frac{m_p C_{ox}}{2}\frac{W_p}{L_p} = b$

$$R_c^{-1} = b[2V_{DD} - 2V_{THn} + 2V_{SS} - 2V_{THp}]$$ nearly indep. Of V_2

$$R_c^{-1}\Big|_{V_2=0V} = g_{mg1} + g_{mg2}$$



2. If $R_c = \frac{1 + (C_d + C_L)/C_C}{g_{mg1} + g_{mg2}}$

$S_z = S_{p2}$ and pole-zero cancellation occurs.

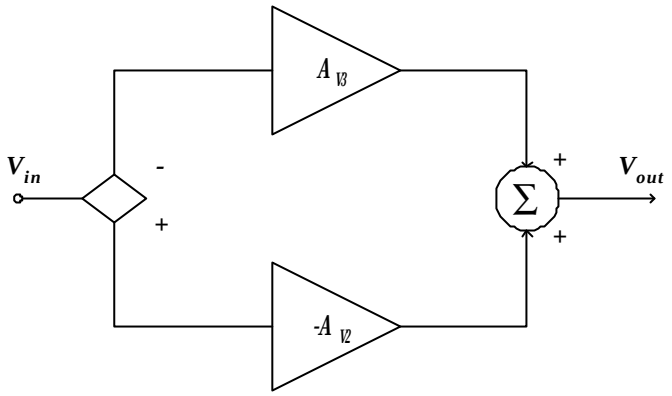
$\Rightarrow S_{p3} >> S_{p1} \Rightarrow A_{dm}S_{p1} < S_{p3} \Rightarrow$ stable

However, if the cancellation is not complete

$\Rightarrow$ pole-zero doublet occurs ! $\Rightarrow$ slow slew rate.

§6-2.2 Feedforward compensation

A_{v3} is the gain of the source follower



$$A_{v3}=\frac{A_{v3}(0)(1+\frac{s}{z_3})}{(1+\frac{s}{P_3})}$$

1 LHP zero
1 LHP pole

$$A_{v2}=\frac{A_{v2}(0)(1-\frac{s}{z_1})(1+\frac{s}{z_2})}{(1+\frac{s}{P_1})(1+\frac{s}{P_2})}$$

2 LHP poles
1 RHP zero (C_C)
1 LHP zero

z_3 & z_2 are generated from the C_{gs} of the source follower.

$$\frac{V_{out}}{V_{in}}=A_{VTOT}(s)=A_{V2}(s)+A_{V3}(s)$$

$$=[A_{V2}(0)+A_{V3}(0)]\frac{(1+\frac{s}{z_1'})(1+\frac{s}{z_2'})(1+\frac{s}{z_3'})}{(1+\frac{s}{p_1})(1+\frac{s}{p_2})(1+\frac{s}{p_3})}$$

p_1' : dominant pole

z_1', z_2', z_3' : LHP Zeros

Design consideration : Any zeros below the unity-gain frequency must be placed as close as possible to their matching poles. This prevents the formation of any doublet !

$z_1' = p_2$ by adding CB1 and CB2(3.8pF) to control $C_{gs9}+C_{gs11}$

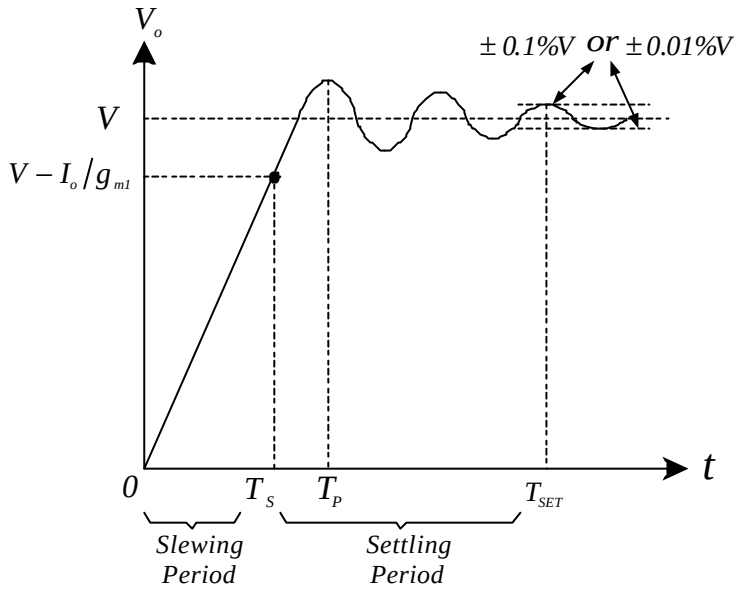
Ref:IEEE JSSC , col SC-14, no.6 pp.1070-1077 , DEC.1979

Feedfoward +Miller(direct)

Ref:IEEE JSSC , col SC-15, no.6 pp.921-928 , DEC.1980

Feedfoward +Unity gain buffer + Miller

§ 6-3 Settling Behavior



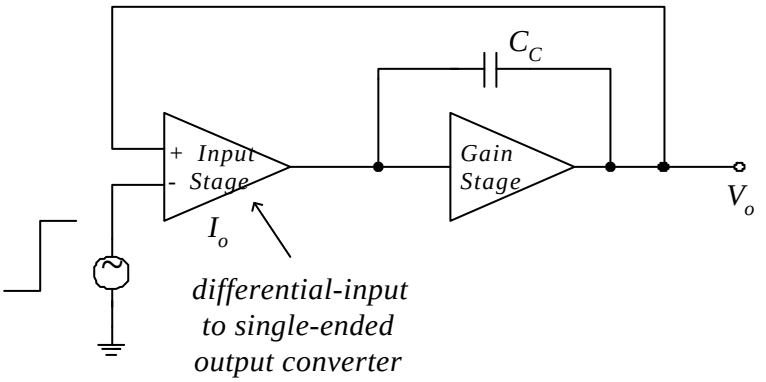
Slewing Period (*Ts*): V_o from 0V to $V\text{-}I_o/g_{m1}$ under voltage follower connection and worse case loading.(nonlinear operation)

Settling Period ($T_{SET}\text{-}T_s$):

V_o from ($V\text{-}I_o/g_{m1}$) to $\pm 0.1\%$ V or $\pm 0.01\%$ V (quasi-linear operation)

Settling Time (T_{SET}): T_s +($T_{SET}\text{-}T_s$) = slewing period + settling period.

§ 6-3.1 Single-pole case



Slew rate:

$$SR \equiv \frac{dVo}{dt}\Big|_{max} = \frac{I_o}{C_c}$$

$$w_u = \frac{g_{mi}}{C_c} \leftarrow \text{single-pole case}$$

$$SR = \frac{I_o w_u}{g_{mi}} = w_u \sqrt{\frac{I_o}{2\frac{uC_{ox}}{2}(\frac{W}{L})_i}}$$

§ 6-3.1 Two-pole case

Ref；IEEE JSSC vol.SC-17, no.1 pp.74-80, Feb. 1982

$$Ts = -\frac{1}{w_1} ln[1 - \frac{g_{m1}}{I_o a_o}(V - \frac{I_o}{g_{m1}})$$ Fig.2

approximation： $e^{-w_1 T_S} \cong 1 - w_1 T_S$ => eq.(19) conventional expression

After Ts： $V_o = V - I_o/g_{m1}$ Input voltage = $V-(V-I_o/g_{m1}) = I_o/g_{m1}$

=> enter the linear (or quasi-linear) region

Feedback Function for unity-gain voltage-follower connection

=> $A(s) = \frac{a(s)}{1 + a(s)}$ eq.(20)-(23)

two poles： $S = -xw_n \pm \sqrt{x^2 - 1} w_n$ eq.(24) $\boxed{\xi = \frac{\omega_1 + \omega_2}{2\omega_n}}$

(double negative real poles) damping ratio

x = 1 critically damped

x < 1 underdamped x > 1 overdamped

(complex conjugate poles) (real and negative pole)

$$x = \frac{w_1 + w_2}{2w_n} \cong \frac{\sqrt{w_2}}{2\sqrt{a_o w_1}} = \frac{\sqrt{w_2}}{2\sqrt{w_u}} = \frac{\sqrt{g_{m2}/c_2}}{2\sqrt{g_{m1}/c_c}}$$ (C_C, C_2 >> C_1)

$x \gtrless 1 \quad \Rightarrow C_C \gtrless 4(\frac{g_{m1}}{g_{m2}})C_2 \quad (C_C, C_2 >> C_1)$

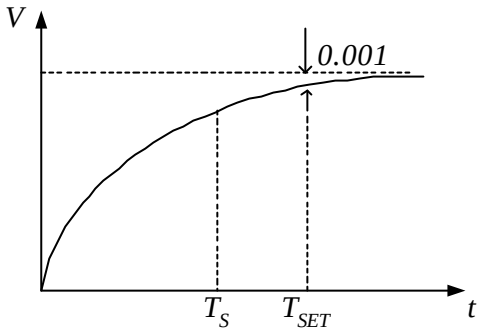
$\Rightarrow \quad w_2 \gtrless 4w_u \Leftrightarrow \frac{w_2}{w_u} = 2 \sim 4$ $\quad \omega_2 < 4\omega_u$ underdamped; $\omega_2 > 4\omega_u$ overdamped

(1) Underdamped: T_S eq. (14) or (19) max.overshoot: eq.(36)

T_P eq. (35), (33) settling time: eq.(40),(39)

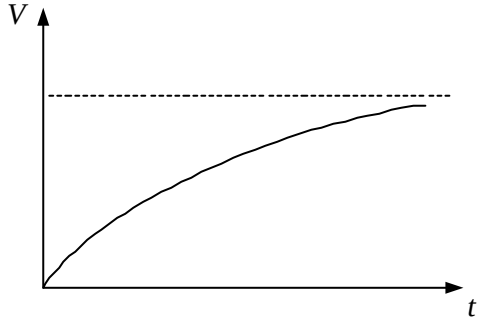
(2) Critically Damped $V_o(t)$: eq.(41)

T_{SET} : eq.(43)



(3) Overdamped T_{SET}: eq.(47)

Simulation & Calculation : Fig.7, Fig.8



Further references:

(1) IEEE JSSC, vol. SC-18, pp.389-394, Aug. 1983

(2) IEEE JSSC, vol. SC-21, pp.478-483, June. 1986

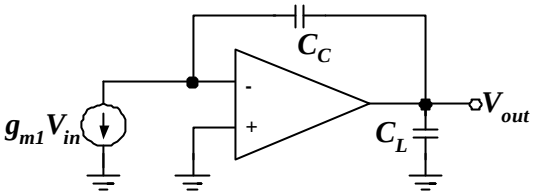
§ 6-4 Slew rate of CMOS OP AMPs

§ 6-4.1 Two-stage OP AMPs

Two poles: $S_{p1}, S_{p2}, |S_{p1}| << |S_{p2}|$

If $|S_{p1}| << w_u << |S_{p2}|, V_{out}(s) = g_{mi} V_{in}(s) / sCc$

$$\frac{V_{out}(jw)}{V_{in}(jw)} = \frac{g_m}{jwCc}$$



At $w = w_u$, $\frac{V_{out}}{V_{in}} = 1$

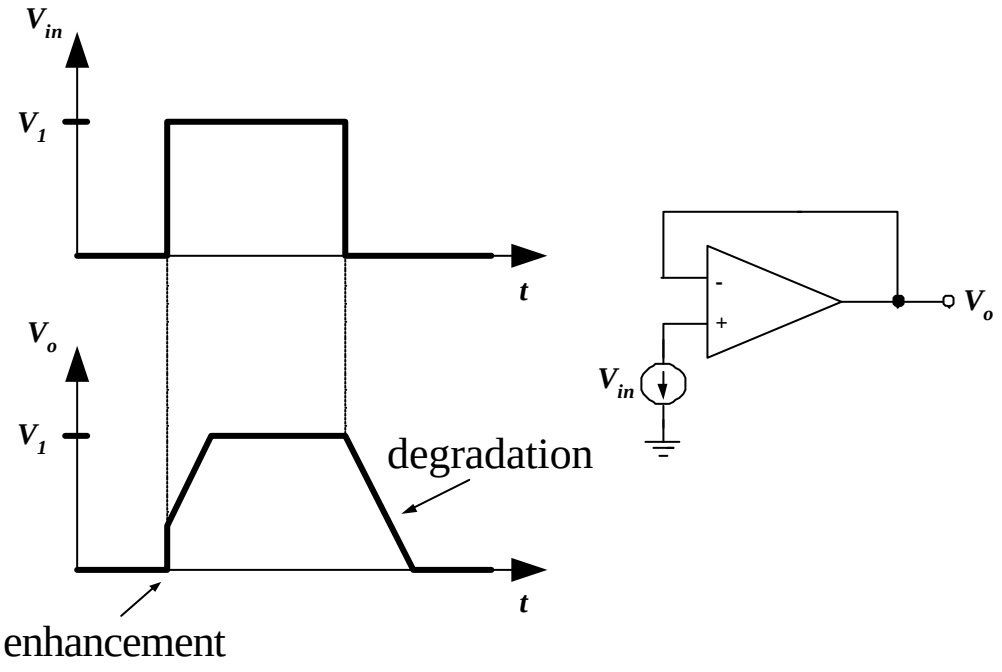
$$\Rightarrow w_u = \frac{g_{mi}}{C_C} \quad or \quad C_C = g_{mi} / w_u$$

The slew rate $SR = \frac{dV_{out}}{dt}\Big|_{max} = I_o / C_C = \frac{I_C w_u}{g_{mi}} = w_u \sqrt{\frac{I_o}{2uC_{ox}(W/L)i}}$

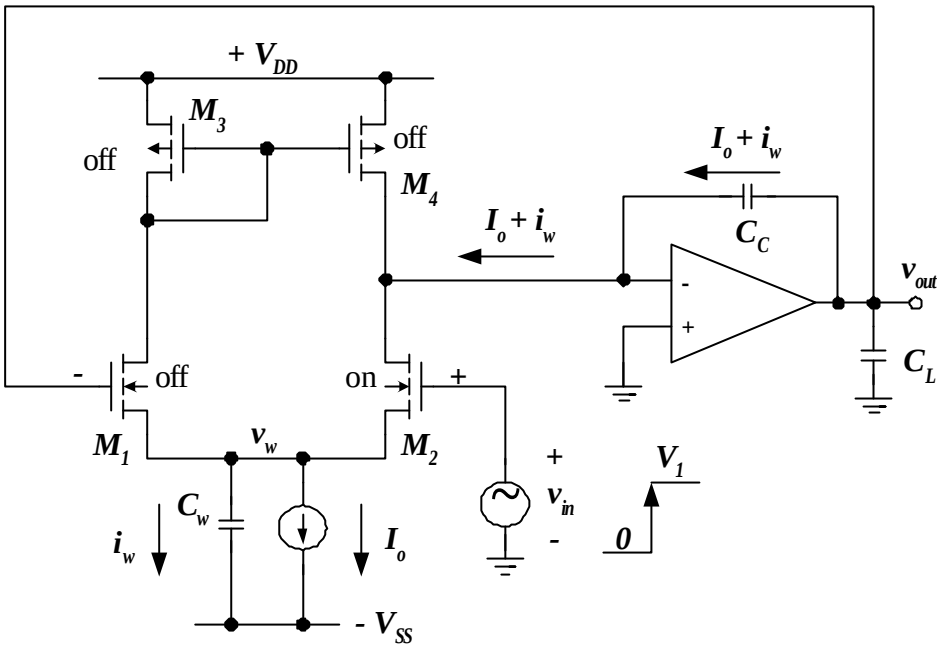
$$w_u \uparrow, I_o \uparrow, (W/L)_i \downarrow \Rightarrow \text{SR} \uparrow$$

* $I_o / C_L \geq I_o / C_C$ or $C_L \frac{dV_{out}}{dt} \leq C_C \frac{dV_{out}}{dt} (= I_o)$

Slew rate enhancement and degradation



(1) Positive step

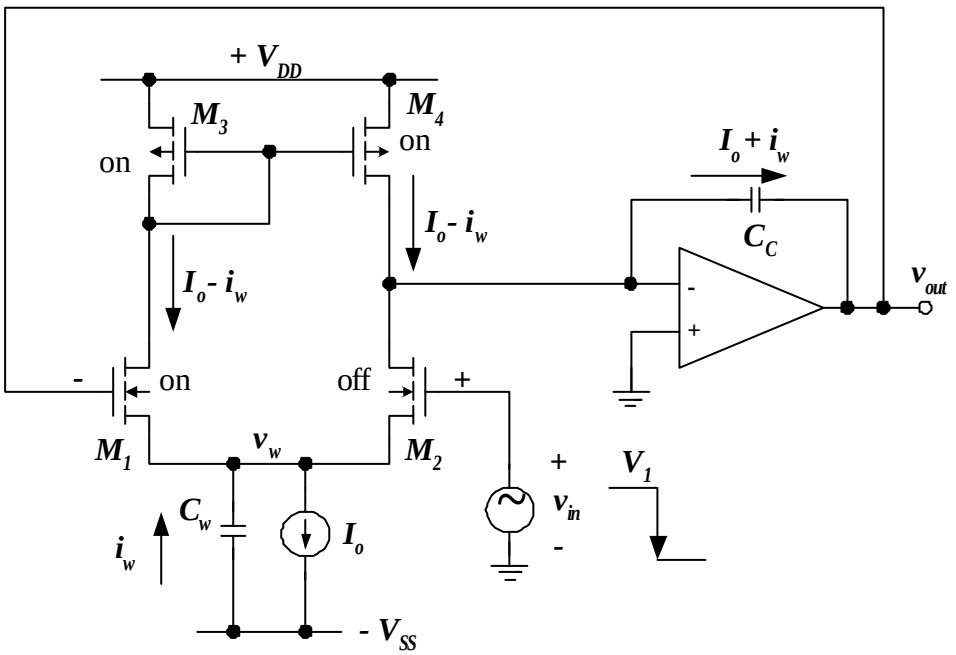


$$i_w(t) = C_w \frac{dv_w(t)}{dt} \cong C_w \frac{dv_{in}(t)}{dt}$$

$$v_{out}(t) = \frac{1}{C_C}\int_0^t (I_o + i_w)dt = \frac{I_o}{C_C}t + \frac{C_w}{C_C}\int_0^t \frac{dv_{in}}{dt}dt$$

$$= \frac{I_o}{C_C}t + \frac{C_w}{C_C}V_1 u(t)$$

(2) Negative step



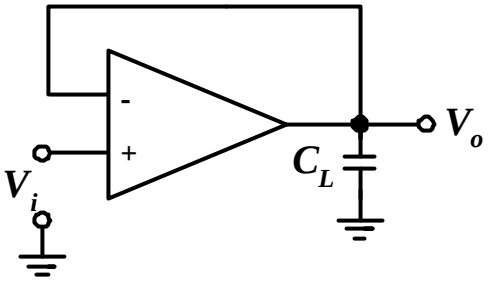
$$v_{out} \cong v_w$$

$$\frac{d}{dt}v_{out} = -\frac{I_o - i_w}{C_C} = \frac{dv_w}{dt} = -\frac{i_w}{C_w} \quad \Rightarrow i_w = \frac{I_o C_w}{(C_C + C_w)}$$

$$\frac{dv_{out}}{dt} = -\frac{I_o}{C_C + C_w}$$ slew degradation

§ 6-4.2 Single-stage OP AMPs

$$SR = \frac{I_o}{C_L}$$

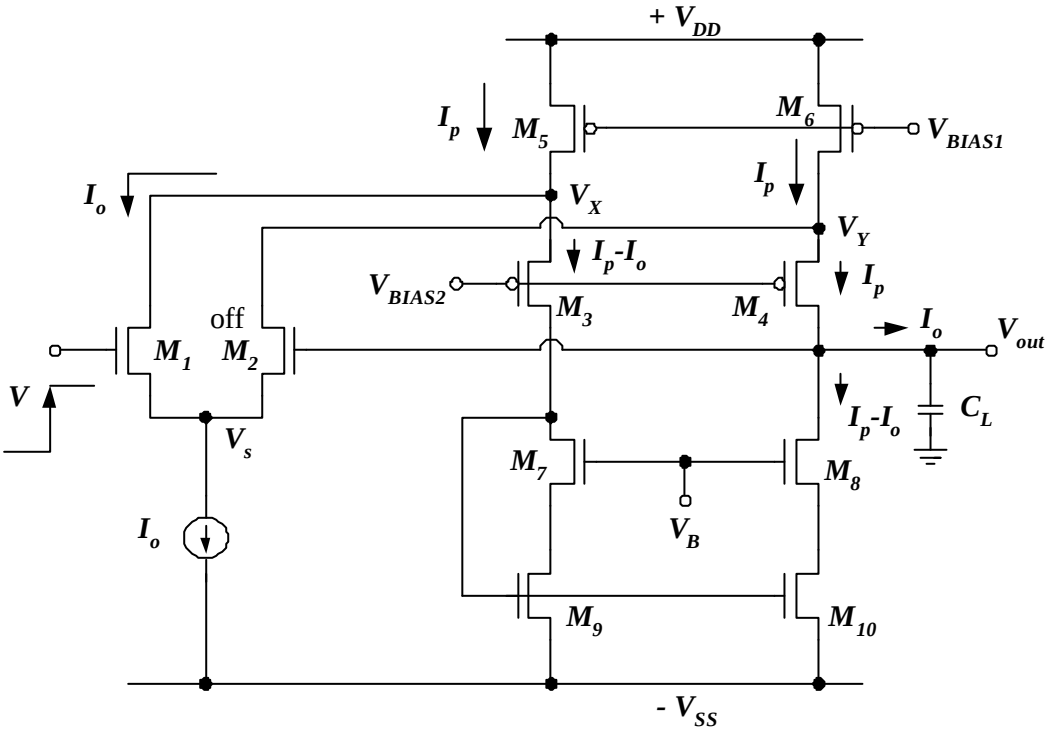


Different phase margins

$\Rightarrow$ different settling behavior.

I_o : First-stage bias current

SR of the folded cascode OP AMPs



$$SR = \frac{I_o}{C_L}$$

* If I_p=I_o, we can keep M_5, M_1 and I_o current source in saturation.

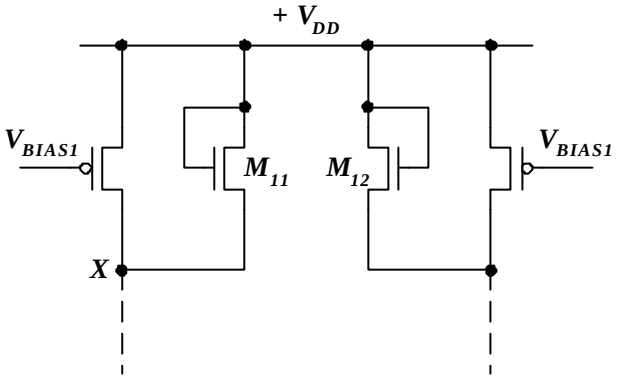
The change of V_x is not significant because the gain of the common-source amplifier M_1 is nearly equal to –1. When M_2 is turned on, the recovery time of V_x is very short.

* If $I_p < I_o$, the current source I_o is forced to linear region and $V_s\downarrow$ $V_x\downarrow$. The decrease of V_x is large. Thus the recovery time of V_x when M_2 is turned on is very long, $\Rightarrow$ The settling is slow down.

How to solve this problem?

(1) Keep $I_p = I_o$ as the optimal design.

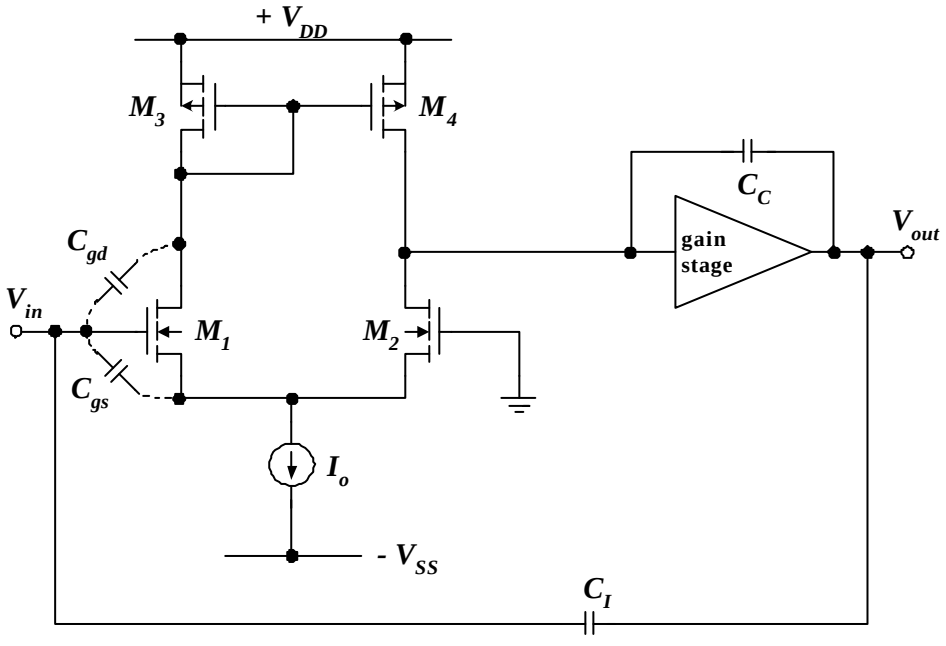
(2) Add clamping devices between V_{DD} and $V_x(V_Y)$



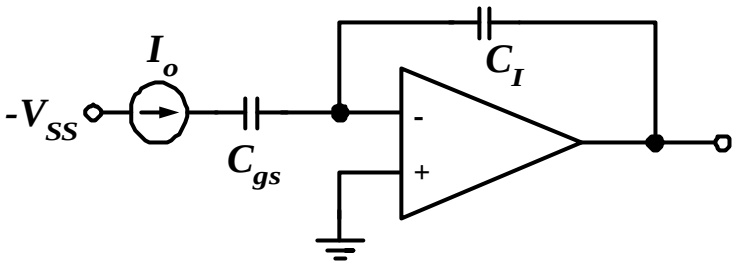
In normal operation, M_{11} and M_{12} are turned off by setting V_{DD}-$V_x < V_{TH11}, V_{TH12}$.

§ 6-5 Power supply rejection ratio (*PSRR*)

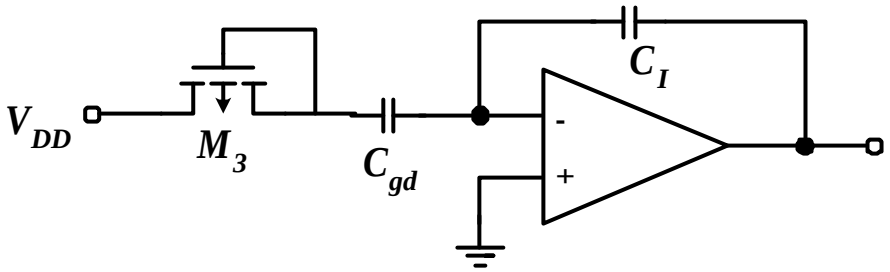
§ 6-5.1 Low frequency analysis for integrators



$$\frac{\partial V_{out}}{\partial V_{SS}} \cong \frac{C_{gs}}{C_I}\left[\frac{\partial I_o}{\partial V_{SS}}\frac{1}{2g_{m1}} + \frac{\partial V_{GS1}}{\partial V_{SS}}\right] + \frac{C_{gd}}{C_I}\frac{1}{2g_{m3}}\frac{\partial I_o}{\partial V_{SS}}$$



$$\frac{\partial V_{out}}{\partial V_{DD}} \cong -\frac{C_{gd}}{C_I}\left[1 - \frac{\partial I_o}{\partial V_{DD}}\frac{1}{2g_{m3}}\right] + \frac{C_{gs}}{C_I}\frac{1}{2g_{m1}}\frac{\partial I_o}{\partial V_{DD}}$$



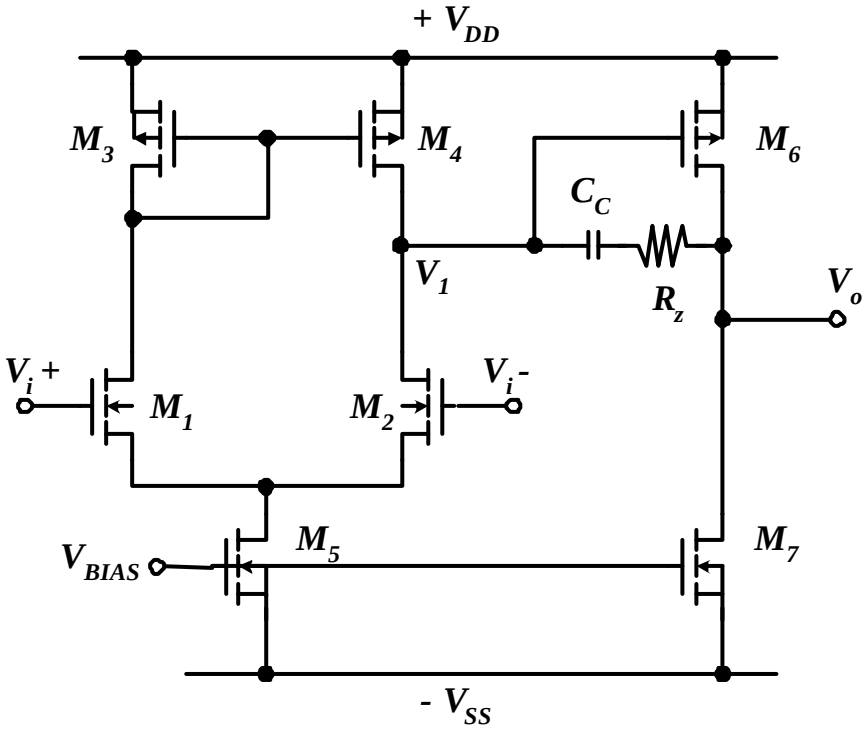
Ref. : IEEE , JSSC , vol.SC-15 , pp.929-938 , Dec. 1980.

* C_{gs}/C_I and C_{gd}/C_I have a strong effect on $PSRR^+$ and $PSRR^-$.

* Small $C_I \Rightarrow$ chip area $\downarrow$ but $PSRR \downarrow$.

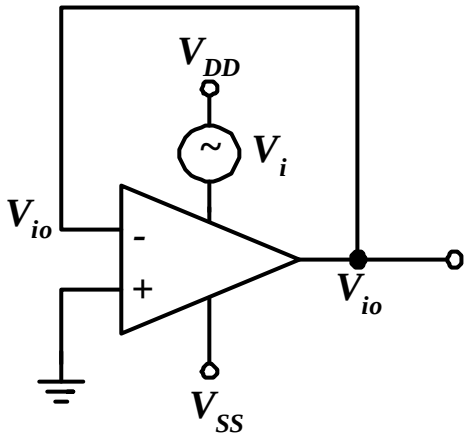
§ 6-5.2 High frequency analysis for OP AMP's

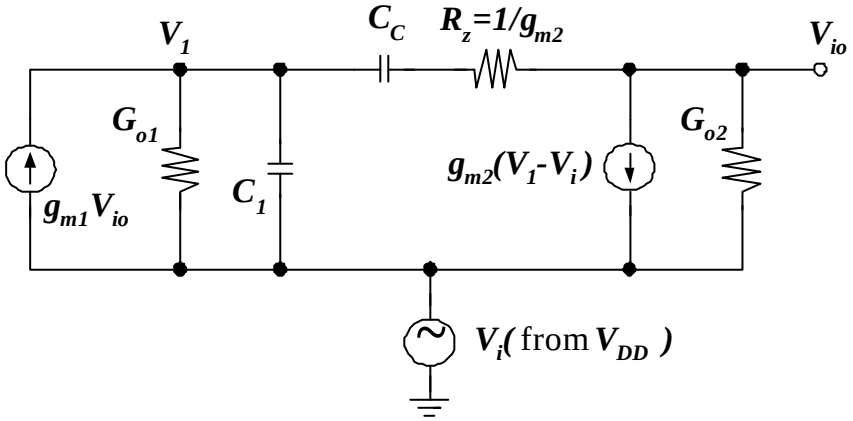
Ref. : IEEE JSSC , vol. sc-19 , pp. 919-925 , Dec. 1984.



$$* \quad PSRR^{+} \equiv \frac{\left|\frac{\partial V_o}{\partial V_i}\right|}{\left|\frac{\partial V_o}{\partial V_{DD}}\right|} = \frac{\left|\frac{\partial V_o}{\partial V_i}\right|_{V_o=0}}{\left|\frac{\partial V_o}{\partial V_{DD}}\right|_{V_o=0}} = \left[\left.\frac{\partial V_{io}}{\partial V_{DD}}\right|_{V_o=0}\right]^{-1}$$

How to calculate $\frac{\partial V_{io}}{\partial V_{DD}}$?





$$PSRR^{+}(s) \cong \frac{s + G_{o1}G_{o2}/(g_{m2}C_c)}{s + g_{m1}/C_c}$$

where $G_{o1}=g_{o4}$ (g_{o2} is connected to the drain of M_5 which is open-circuited, i.e. $r_{ds5} \to \infty$)

$G_{o2}=g_{o6}$ $(r_{ds7} \to \infty)$

$G_{o1}G_{o2}/(g_{m2}C_c) < g_{m1}/C_c$

$\Rightarrow$ Low-frequency LHP zero degrades the *PSRR* .

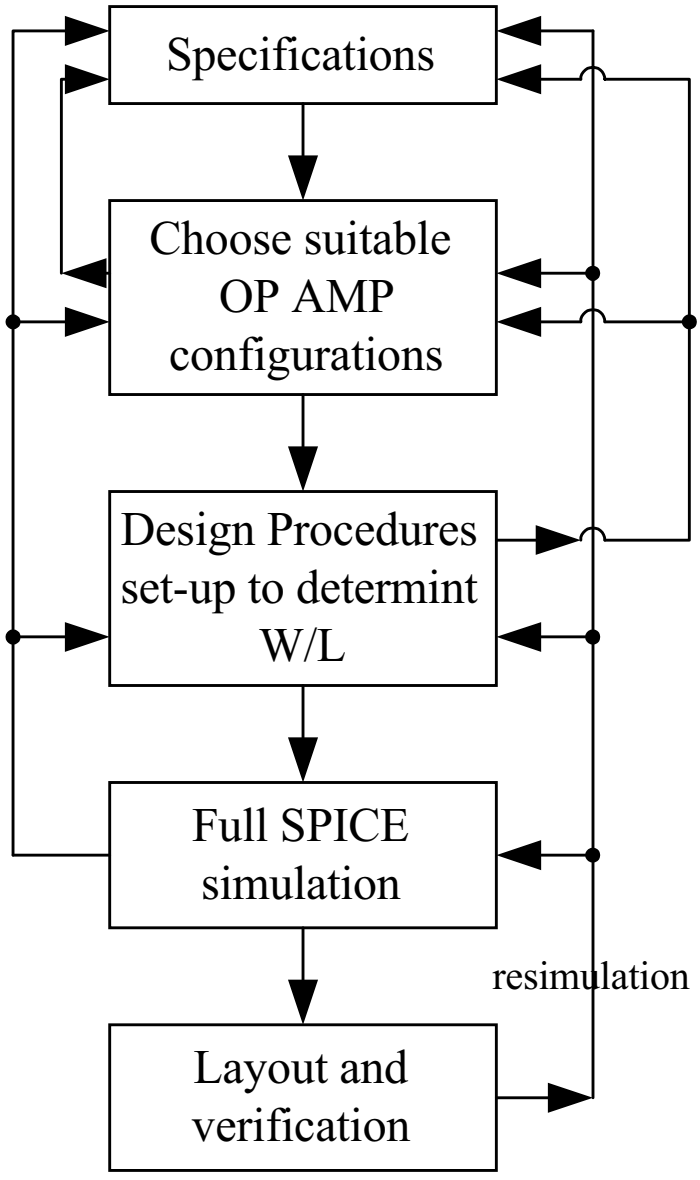
* To improve *PSRR*, C_c must be decoupled from the gate of M_6 to eliminate the LHP zero .

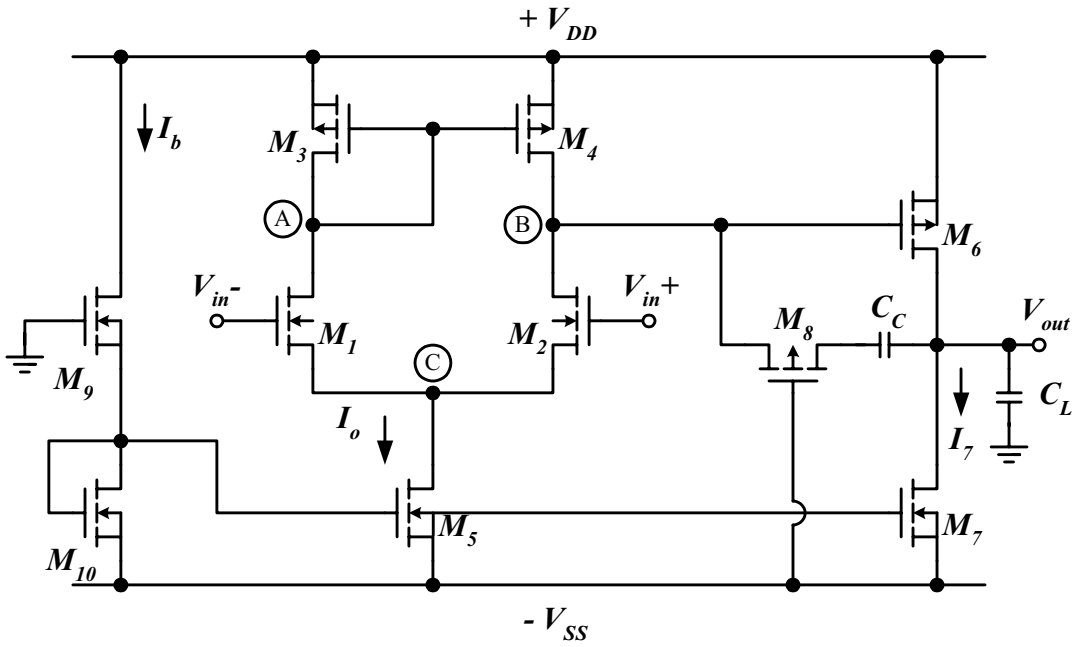
Chapter 7 Design Procedure of CMOS OP AMPs and Pratical Design Considerations on Noise and Offset

§ 7-1 Typical design procedure of two-stage CMOS OP AMPs

Synthesis or Design：Determine the circuit configuration and its MOS device dimensions from the specfications.

Flow Diagram：





Specfications

Low frequency gain	≧ 70dB	Phase margin	> 60°
Unity-gain frequency	≧ 2MHz	C_L	10pF
Slew rate	≧ 4V/μs	V_{DD}=V_{SS}	5V
CMRR	≧ 80dB		

Device parameters

$\mu C_{ox}/2$	$30\mu A/V^2$	$12\mu A/V^2$
	(NMOS)	(PMOS)
V_{TO}	1.2V	-1V

Procedures：

1. Choose a suitable C_c

   Example：choose C_c=C_L=10pF

2. According to the phase margin in the specifications, determine the second pole position.

Example：choose f_T= 2MHz

$$|S_{p2}| \cong +\frac{g_{m6}}{C_L} = 3\omega_u \cong 3g_{mi}/C_c$$

$$|S_{P2}| = 3\omega_u \Rightarrow \text{ Phase margin} > 60^o$$

3. Determine the transconductances of the first stage and the second stage.

   Example : $g_{m6} = 3g_{mi} = 3\omega_u C_L = 3\times 2\pi \times 2\times 10^6 \times 10^{-11}$

   $\Rightarrow g_{m6} = 377\mu$ mho

   $g_{mi} = 125.7\mu$ mho

4. From the slew rate specification, determine the bias currents in the first and the second stages.

   Example : $S = \frac{I_o}{C_C} \geq 4V/\mu s$

   Choose $S = 4V/\mu s, \Rightarrow I_o = 40\mu A$

   The negative-going slew rate is also limited by the Q_7 current source. To reduce or eliminate its effect, S_{ro} is set to 4S.

   $$S_{ro} = 2.5S = 10V/\mu s = \frac{I_7}{C_L}$$

   $$\Rightarrow I_7 = C_L S_{ro} = 100\mu A$$

5. Use the design rule for reducing the systematic offset voltage to design the transconductance of the load MOSFET's.

   Example : $\frac{(W/L)_3}{(W/L)_6} = \frac{(W/L)_4}{(W/L)_6} = \frac{I_o/2}{I_7} = \frac{1}{5}$

   $$g_{ml} = g_{m3} = g_{m4} = \sqrt{\frac{(W/L)_3 \cdot I_o/2}{(W/L)_6 \cdot I_7}}\, g_{m6}$$

   $$= \frac{I_o/2}{I_7} g_{m6} = \frac{1}{5} g_{m6} \cong 75.4\mu \text{ mho}$$

6. Calculate A_{dm} and *CMRR* to verify the design.

Example : $A_{dm} = \frac{g_{mi}g_{m6}}{(g_{dl}+g_{di})(g_{d6}+g_{d7})} \cong \frac{g_{mi}g_{m6}}{(\lambda I_o)(2\lambda I_7)}$

$\cong 6582 > 76dB \quad (\lambda = 0.03V^{-1} \text{ for } L \cong 10\mu m)$

$$CMRR = 2\frac{g_{mi}g_{ml}}{g_{d5}g_{di}} \approx \frac{2g_{mi}g_{ml}}{(\lambda I_o)(\lambda I_o/2)} \approx 26327 \approx 88dB$$

$g_{mi} = C_cW_u$, $I_o = C_cS$, $g_{m6}=3W_uC_L$, $I_7=S_{ro}C_L$

$g_{ml}=I_og_{m6}/2I_7=3C_cSW_u/2S_{ro}$

$$\Rightarrow \quad A_{dm} \approx \frac{3\omega_u^{\ 2}}{2\lambda^2 S_{ro}S} \quad ; \quad CMRR \approx \frac{6\omega_u^{\ 2}}{\lambda^2 S_{ro}S} \approx 4A_{dm}$$

If A_{dm} and *CMRR* could not satisfy the specifications, ω_o , S, and g_{mi} or g_{m6} can be readjusted .

7. Determine the nulling resistor R_c provoded by M_8.

Example: If $S_z \rightarrow S_{p2}$

$$R_c = \frac{1+(C_d+C_L)/C_c}{g_{m6}} \approx \frac{2}{g_{m6}} \approx 5.3K\Omega$$

If $S_z \rightarrow \infty$

$$R_c = \frac{1}{g_{m6}} = 2.65K\Omega$$

$$R_c = \frac{1}{\frac{\mu_p C_{ox}}{2}\frac{W_8}{L_8}\left[2\left(V_{SS}+V_B-|V_{TH8}|\right)\right]}$$

8. Dimension M_5 and M_7.

W/L can't be too small $\Rightarrow$ too large V_{GS}.

Can't be too large $\Rightarrow$ C_w too large $\Rightarrow$ *CMRR* $\downarrow$

$C_L \uparrow \Rightarrow$ phase margin $\downarrow$

Example: $\left(\frac{W}{L}\right)_5 = \frac{I_o}{\frac{\mu_n C_{ox}}{2}(V_{GS5} - V_{TH5})^2} \approx 5.33$ ($\frac{\mu_n C_{ox}}{2} \approx 30 \mu A/V^2$

$V_{GS5} - V_{TH5} \approx 0.5V$)

$$\left(\frac{W}{L}\right)_7 = \frac{I_7}{\frac{\mu_n C_{ox}}{2}(V_{GS7} - V_{TH7})^2} \approx 13.33$$

Choose $L_5=L_7=10\mu m \Rightarrow W_5=54\mu m$, $W_7=133\mu m$

9. Dimension M_1-M_4 and M_6

Example: $g_m \approx 2\sqrt{\frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right) I_D}$ 0

$$\left(W/L\right)_1 = \left(W/L\right)_2 \approx \frac{8m_i^2}{4\frac{\mu_n C_{ox}}{2} I_o/2} \approx 6.58$$

$$(W/L)_3 = (W/L)_4 \approx \frac{g_{ml}^2}{4\frac{\mu_p C_{ox}}{2}\frac{I_o}{2}} \approx 5.92$$

$$(W/L)_6 = 5(W/L)_3 \approx 29.6$$

Choose $L=10\ \mu m$

$\Rightarrow\ W_1 = W_2 = 66\mu m$ ，$W_3 = W_4 = 60\mu m$ ，$W_6 = 300\mu m$

10. Estimate the dc bias voltage.

Example：$|V_{GS3}| = |V_{THP3}| + \sqrt{\frac{I_o/2}{\frac{\mu_p C_{ox}}{2}(W/L)_3}} = 1 + \sqrt{\frac{20}{12\times 6}} \approx 1.527$

$$\Rightarrow V_A = V_B = V_{DD} - |V_{GS3}| = 3.473V$$

$$\frac{I_O}{2} = \frac{\mu_n C_{ox}}{2}(W/L)_1(-V_C - V_{THn})^2$$

$$\Rightarrow V_C = -1.518V$$

11. Dimension M_8

Example： $2\frac{\mu_p C_{ox}}{2}(W/L)_8(5+3.473-1)=\frac{1}{R_C}$

$\Rightarrow (W/L)_8 \approx 1.052$

choose $W_8 = L_8 = 10\mu m$.

12. Determine V_{BIAS} and dimension M_9 and M_{10}

Example： $V_{GS} = V_{THn} + 0.5V = 1.7V$

$V_{BIAS} = -V_{SS} + V_{GSS} = -3.3V$

Choose $I_b = 20\mu A$

$\Rightarrow V_{GS9} = 0 - V_{BIAS} = 3.3V \Rightarrow V_{BIAS} = -3.3V$

$V_{GS10} = V_{BIAS} + V_{SS} = -1.7V$

$$(W/L)_9 = \frac{I_b}{\frac{\mu_n C_{ox}}{2}(V_{GS9} - V_{THn})^2} \approx 0.1512$$

$$(W/L)_{10} = \frac{I_b}{\frac{\mu_n C_{ox}}{2}(V_{GS10} - V_{THn})^2} \approx 0.2667$$

Choose $W_9 = 10\mu m$, $L_9 = 66\mu m$ and

$W_{10} = 27\mu m$, $L_{10} = 10\mu m$.

13. Use SPICE to simulate the overall OP AMP and make the necessary adjustment.

Reference : Reference Book No. 3, (Gregorian and Temes) pp. 222-241.

§7-2 Practical Design Consideration on Noise

§7-2.1 Noise of MOS devices

1) shot noise

* Due to the fluctuation in the number of carriers crossing a given surface in the conductor in any time interval.
* If the carrier density is low and the external electric field is high so that the interaction among the carriers are negligible, we have

$$\overline{i_{ns}^2} = 2qI(BW)$$

where i_{ns} is the random variation of the current.
I is the average current.
BW is the bandwidth in which the noise is measured.

* When an MOSFET is operated in the saturation region, inversion carrier density is high. => $\overline{i_{ns}^2}$ is much smaller than that predicted by the formula.

Shot noise is not important.

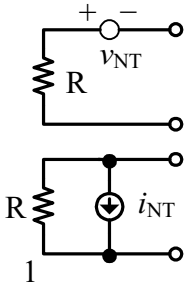
* In the subthreshold region, shot noise is higher.

2) Thermal noise

* Generated by the random thermal motion of the carriers in a resistor.
* The mean square of the noise voltage v_{nT} and the noise current i_{nT} are

$$\overline{v_{nT}^2} = 4KTR(BW)$$

$$\overline{i_{nT}^2} = 4KTG(BW)$$

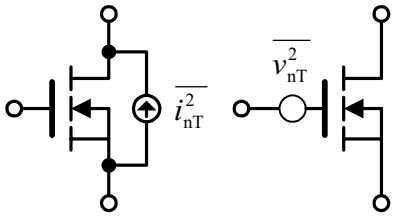


* In MOSFETs, R is the incremental channel resistance.

If the MOSFET is in the saturation region, $R = \frac{3}{2g_m} = \frac{1}{\frac{2}{3}g_m}$

$$\overline{v_{nT}^2} = \overline{(i_{nT}/g_m)^2} = \frac{8}{3}\frac{KT}{g_m}BW$$

* The spectral density $\overline{v_{nT}^2}/BW$ is independent of frequency $\Rightarrow$ White noise.
* Circuit models:



$\overline{v_{nT}^2}$:gate-referred noise voltage source.

* $\sqrt{\frac{\overline{v_{nT}^2}}{BW}} = \frac{nV}{\sqrt{H_z}}$

* When the MOSFET is turned off (R=∞, G=0), $\overline{i_{nT}^2}$ is very small.

  ⇒ Noiseless open circuit.

3) Flicker $(1/f)$ noise

* Generated by the trapping and releasing electrons from the channel caused by the interfacial states.
* Slow process ⇒ important at low frequencies

  ⇒ $1/f$ noise. Below ~ KH_z

* $\overline{v_{nf}^2} = \frac{K}{C_{ox}WL}\frac{BW}{f}$ $\qquad \overline{i_{nf}^2} = g_m{}^2\overline{v_{nf}^2}$

* (WL) ↑ , C_{ox} ↑ , Temperature ↓ , density of surface state ↓ ⇒ $\overline{v_{nf}^2}$ ↓

4) Combined noise

$$i_n = \sqrt{\overline{i_{nT}^2} + \overline{i_{nf}^2}} = \sqrt{(4KTG + Kg_m^2/(C_{ox}WLf)]BW}$$

∵independent noise sources.

$$v_n = \frac{i_n}{g_m}$$

§7-2.2 Noise Performance of NMOS Amplifiers

1) Enhancement-load amplifier

$$A_{V1} = -\alpha_2\sqrt{\frac{W_1L_2}{W_2L_1}} \quad \text{for} \quad e_{n1}$$

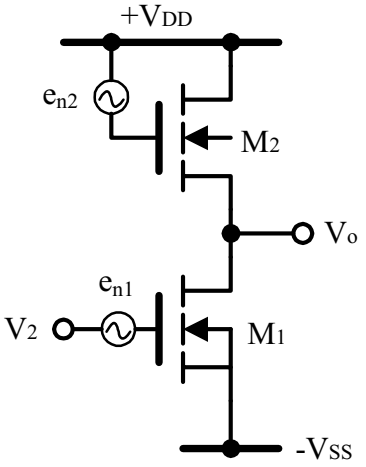
$$A_{V2} = \alpha_2 \quad \text{for} \quad e_{n2}$$

The equivalent input noise voltage

$$e_n(IN) = \frac{1}{A_{V1}}\sqrt{(A_{V1}e_{n1})^2 + (A_{V2}e_{n2})^2}$$

$$= e_{n1}\sqrt{1 + (\frac{A_{V2}e_{n2}}{A_{V1}e_{n1}})^2}$$

$$= \sqrt{\frac{a_n}{W_1L_1}(1 + \frac{L_1}{L_2})^2}$$



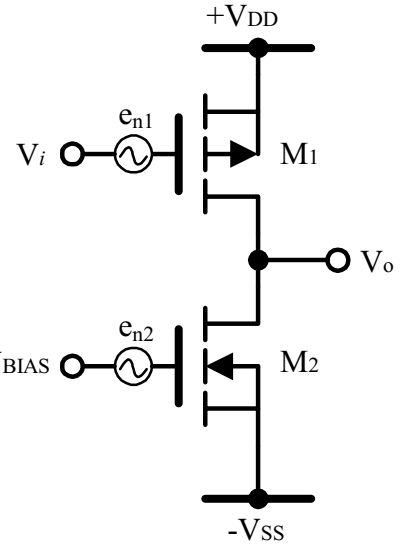
e_n : 1/f noise

$$e_n = \sqrt{\frac{a_n}{WL}}$$

* $W_1 \uparrow$, $L_2 \uparrow$ $\Rightarrow$ smaller $e_n(IN)$
* There exits an optimal $L_1 = L_2$ * Independent of W_2

§7-2.3 Noise Performance of CMOS Amplifiers

1) CMOS amplifier



$$A_{V1} = -g_{m1}(r_{ds1} \| r_{ds2})$$

$$A_{V2} = -g_{m2}(r_{ds1} \| r_{ds2})$$

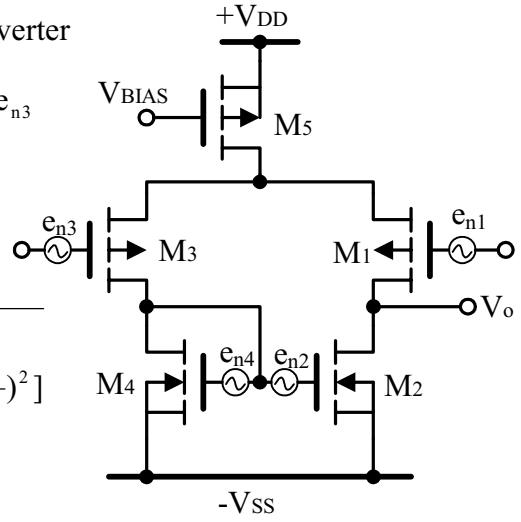
$$g_{m1} = 2\sqrt{(\frac{\mu_n C_{ox}}{2})_1 \frac{W_1}{L_1} I_D}$$

$$g_{m1} = 2\sqrt{(\frac{\mu_n C_{ox}}{2})_2 \frac{W_2}{L_2} I_D}$$

$$e_n(IN) = \sqrt{\frac{a_{n1}}{W_1 L_1}[1 + \frac{(\frac{\mu_p C_{ox}}{2})_2 a_{n2}}{(\frac{\mu_n C_{ox}}{2})_1 a_{n1}} (\frac{L_1}{L_2})^2]}$$

Design considerations for low noise can be found.

2) CMOS differential-input to single-ended converter



$$A_{V1} = \frac{1}{2}(g_{m1} + g_{m2})(r_{ds1} \| r_{ds2}) \quad \text{for } e_{n1},\ e_{n3}$$

$$A_{V2} = g_{m2}(r_{ds1} \| r_{ds2})$$

If $g_{m1} = g_{m3}$ and $g_{m2} = g_{m4}$

$$\Rightarrow e_n(IN) = \sqrt{2\frac{a_{n1}}{W_1 L_1}[1 + \frac{(\frac{\mu_n C_{ox}}{2})_2 a_{n2}}{(\frac{\mu_p C_{ox}}{2})_1 a_{n1}} (\frac{L_1}{L_2})^2]}$$

* $W_1 \uparrow$, $L_2 \uparrow$, $e_n(IN) \downarrow$

* Optimal $L_1 = \sqrt{\frac{(\frac{\mu_p C_{ox}}{2})_1 a_{n1}}{(\frac{\mu_n C_{ox}}{2})_2 a_{n2}}} L_2$

* The noise from M_2 and M_4 loads is very important!

Example : PMOS : $(\frac{\mu C_{ox}}{2})_p = 3\mu A / V^2$

$$a_{np} = 48 \times 10^3 (\mu V \cdot \mu m)^2 \quad \text{for } 20Hz \sim 20KHz$$

NMOS : $(\frac{\mu C_{ox}}{2})_N = 7\mu A / V^2$

$$a_{nn} = 380 \times 10^3 (\mu V \cdot \mu m)^2 \quad \text{for} \quad 20Hz \sim 20KHz$$

* NMOS is much more noisy than PMOS due to much larger $1/f$ noise

Why? 1.higher surface-state density

2.nonuniform trap center distribution (more centers near conduction band)

3.Efficient election trapping and releasing.

Bias current $I_D = 5\mu A$, Gain : $\approx 44dB$

Design Ⅰ: M_1, M_3 : $500\mu m / 5\mu m$ PMOS

M_2, M_4 : $100\mu m / 4\mu m$ NMOS

$\Rightarrow e_n(IN) = 38\mu V \quad 20Hz \sim 20KHz$

(33.9)

Design Ⅰ: M_1, M_3 : $500\mu m / 5\mu m$ PMOS

M_2, M_4 : $50\mu m / 44\mu m$ NMOS

$\Rightarrow e_n(IN) = 7.5\mu V \quad 20Hz \sim 20KHz$

(6.9)

3) CMOS inverter amplifier

$$A_V \equiv \frac{V_o}{V_i} = (g_{m1} + g_{m2})(r_{ds1} \| r_{ds2})$$

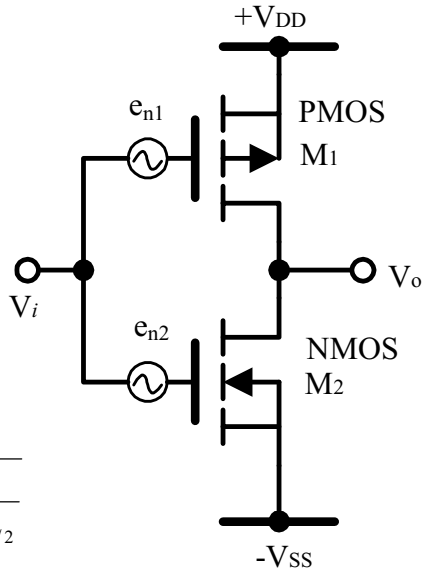
$$A_{V1} = -g_{m1}(r_{ds1} \| r_{ds2}) \quad \text{for} \quad e_{n1}$$

$$A_{V2} = -g_{m2}(r_{ds1} \| r_{ds2}) \quad \text{for} \quad e_{n2}$$

$$e_n(IN) = \frac{\sqrt{(g_{m1}e_{n1})^2 + (g_{m2}e_{n2})^2}}{g_{m1} + g_{m2}}$$

If $g_{m1} = g_{m2}$

$$\Rightarrow e_n(IN) = \frac{1}{2}\sqrt{e_{n1}^{\ 2} + e_{n2}^{\ 2}} = \frac{1}{2}\sqrt{\frac{a_{n1}}{W_1 L_1} + \frac{a_{n2}}{W_2 L_2}}$$



* Larger size WL $\Rightarrow$ smaller noise

If $g_{m1} \neq g_{m2}$

$$\Rightarrow e_n(IN) = \sqrt{\frac{a_{n1}}{W_1 L_1}\left(1+\frac{\left(\frac{\mu_n C_{ox}}{2}\right)_2}{\left(\frac{\mu_p C_{ox}}{2}\right)_1}\frac{a_{n2}}{a_{n1}}\frac{L_2^{\,2}}{L_1^{\,2}}\right)} \Big/ \left(1+\sqrt{\frac{\left(\frac{\mu_n C_{ox}}{2}\right)_2}{\left(\frac{\mu_p C_{ox}}{2}\right)_1}\frac{W_2}{W_1}\frac{L_1}{L_2}}\right)$$

* Increase the channel length of the transistor having the highest a_n parameter.

Example : Bias current 100μA

Design Ⅰ : $M_1 : {}^{1000\mu m}/_{5\mu m}$, $M2 : {}^{400\mu m}/_{4\mu m}$

$\Rightarrow e_n(IN) = 8.1\mu V(7.97\mu V)$ 20Hz ~ 20KHz

Design Ⅱ : $M_1 : {}^{1000\mu m}/_{5\mu m}$, $M2 : {}^{200\mu m}/_{8\mu m}$

$\Rightarrow e_n(IN) = 5.9\mu V(5.65\mu V)$ 20Hz ~ 20KHz

Design Ⅲ : $M_1 : {}^{500\mu m}/_{10\mu m}$, $M2 : {}^{400\mu m}/_{4\mu m}$

$\Rightarrow e_n(IN) = 10.5\mu V(10.36\mu V)$

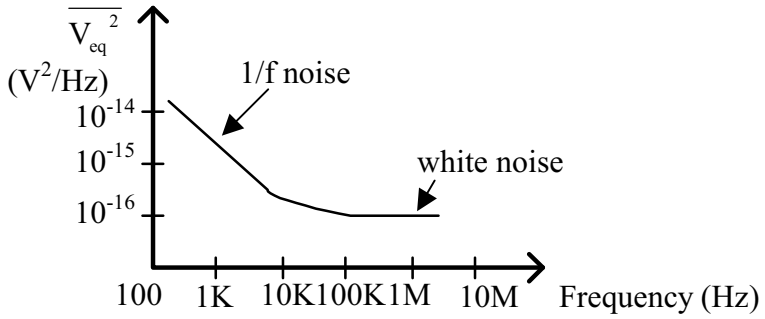
* Best noise figure $\Rightarrow$ highest ${}^{W}/_{L}$ in PMOS

lowest ${}^{W}/_{L}$ in NMOS

Note : WL for PMOS (NMOS) are the same.

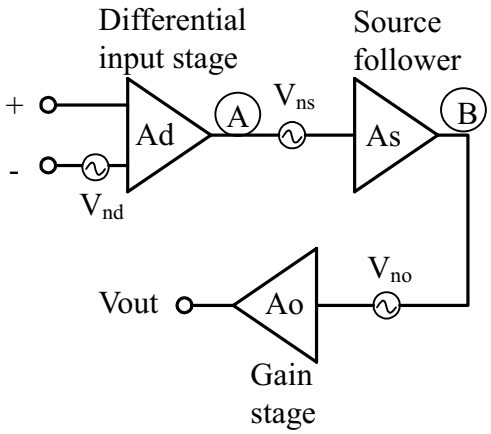
Reference : J.-C. Bertails, JSSC, vol.SC-14, pp.773-776, Aug.1979.

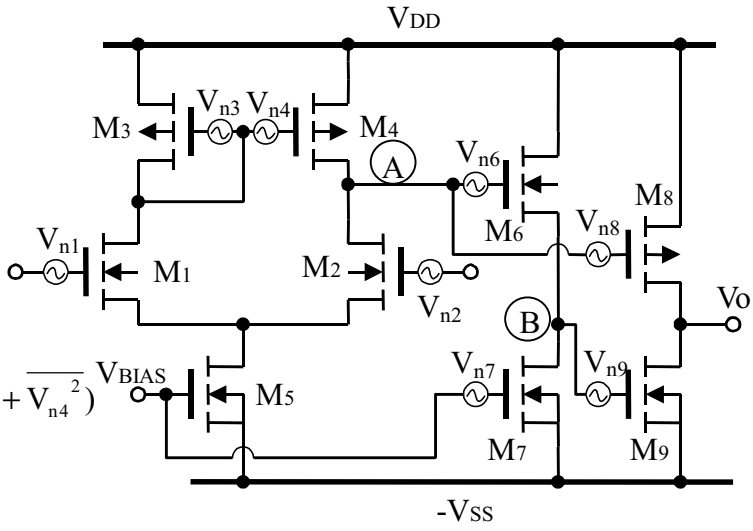
Noise spectrum of a typical MOSFET :



§7-2.4 Noise performance of CMOS OP AMPs

1.Midband Analysis





$$\overline{V_{nd}^2} = \overline{V_{n1}^2} + \overline{V_{n2}^2} + \left(\frac{g_{m4}}{g_{m1}}\right)\left(\overline{V_{n3}^2} + \overline{V_{n4}^2}\right)$$

$$\overline{V_{ns}^2} = \overline{V_{n6}^2} + (g_{m7}/g_{m6})^2\,\overline{V_{n7}^2}$$

$$\overline{V_n^2} \approx \overline{V_{nd}^2} + \overline{V_{ns}^2}\Big/A_d^2 = \overline{V_{n1}^2} + \overline{V_{n2}^2} + \left(g_{m4}\Big/g_{m1}\right)^2\left(\overline{V_{n3}^2} + \overline{V_{n4}^2}\right) + \left[\overline{V_{n6}^2} + \left(g_{m7}\Big/g_{m6}\right)^2\overline{V_{n7}^2}\right]\Big/A_d^2$$

* At low frequency (<1KHz) , $1/f$ noise dominates and $|A_d(w)| >> 1$

$\Rightarrow \overline{V_{ns}^2}$ has a negligible effect on the OP noise.

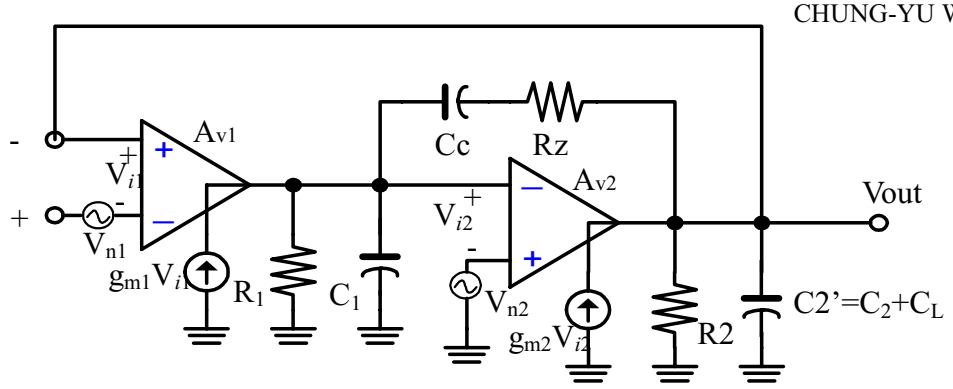
The input stage dominates the overall noise contribution.

* At high frequency where $|A_d(w)| \approx g_{m7}/g_{m6} >> 1$, ($\because M_6$, M_7 is a level shifter, g_{m6} is small to obtain a large $V_{Gs6} \Rightarrow g_{m7}/g_{m6} >> 1$), the effect of V_{n7} is comparable to that of V_{n1} and V_{n2}. Thus M_7 must be a low-noise device (like PMOS).

The effect of V_{no} is negligible on the total equivalent input noise voltage since the gain of the gain stage is very high.

§7-2.5 High frequency analysis (for white noise)

For CMOS 2-stage OP AMP (without level shifter), the small-signal equivalent circuit is



(under unity-gain feedback)

$$\frac{V_{out}}{V_{in1}}=\frac{A_V[1-sC_c(\frac{1}{g_{m2}}-R_z)]}{1+A_V+as+bs^2+cs^3}$$

$$\frac{V_{out}}{V_{in2}}=A_{V2}\frac{\{1+s[C_c(R_1+R_z)+C_1R_1]+s^2C_1C_cR_1R_z\}}{(1+A_V)+as+bs^2cs^3}$$

when $A_V=A_{V1}+A_{V2}$

$$a=C_c[A_V(\frac{1}{g_{m1}}-\frac{1}{g_{m2}}+R_z)+R_1+R_2+R_z]+C_1R_1+C_2'R_2$$

$$b=R_1R_2(C_1C_2'+C_1C_c+C_2'C_c)+R_zC_c(C_1R_1+C_2'R_2)$$

$$c=C_1C_2'C_cR_1R_2R_z$$

Usually, $|A_V|>>1$, $R_z<<R_1$, $R_z<<R_2$, $C_1<<C_c$, $C_1<<C_L$, and $C_2<<C_L$

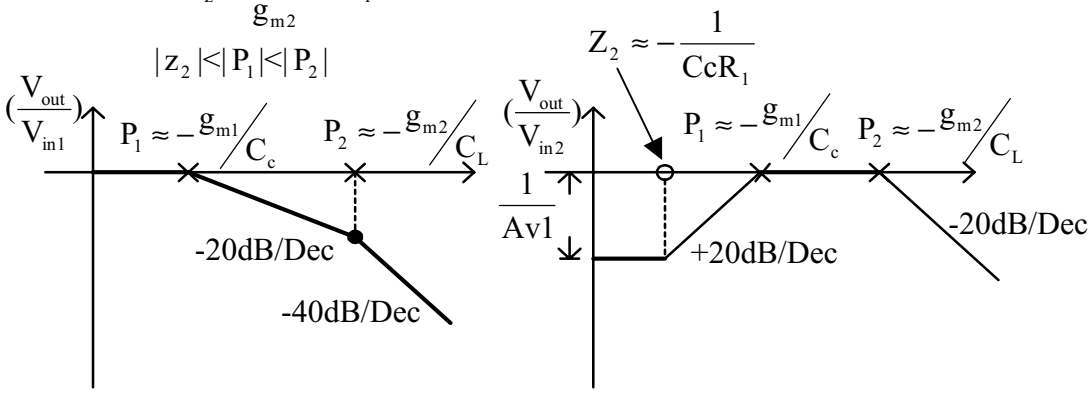
$\Rightarrow$ LHP Poleo : $P_1\approx-g_{m1}/C_c$; $P_2\approx-g_{m2}/C_L$, $P_3\approx-1/C_1R_z$

RHP zero $(\frac{V_{out1}}{V_{in1}})$: $z_1=[C_c(\frac{1}{g_{m2}}-R_z)]^{-1}$;

LHP zeros : $-\frac{1}{C_cR_1}=z_2$, $z_3\approx-\frac{1}{C_1R_z}$ $(z_3\rightarrow\infty)$

If $R_z=\frac{1}{g_{m2}}\Rightarrow z_1=\infty$

$|z_2|<|P_1|<|P_2|$



The equivalent noise bandwidths are

$$BW_1 = {g_{m1}}/{4C_c} \quad (= {|P_1|}/{4})$$

$$BW_2 = {g_{m2}}/{4C_L} - {g_{m1}}/{4C_c} \quad (= {|P_2|}/{4} - {|P_1|}/{4})$$

$$\approx {g_{m2}}/{4C_L} \quad (Cc >> C_L)$$

$$\overline{V_{ntot}}^2 = \sum 4KT\gamma_i \frac{1}{g_{mi}}(BW_i)A_i, \ \gamma_i = \text{constant}(\approx \frac{3}{2})$$

(Consider only thermal noise)

$$= \frac{A_V}{1+A_V} 4KT\gamma_1 \frac{1}{g_{m1}}({g_{m1}}/{4C_c}) + \frac{A_{V2}'}{1+A_V'} 4KT\gamma_2 \frac{1}{g_{m2}}({g_{m2}}/{4C_L})$$

$$= \frac{A_V}{1+A_V}\gamma_1 \frac{KT}{C_c} + \frac{A_{V2}'}{1+A_V'}\gamma_2 \frac{KT}{C_L}$$

where A_{V2}' and A_V' are average gains between P_1 and P_2.

* The total white noise of the OP AMP is inversely proportional to C_c and C_L.
* Due to the foldover effect in SCF, white noise (thermal noise) becomes important.
* 1) Clock feedthrough noise; 2) noises coupled from the power supplies, clock, and ground lines, and from the substrate; 3) white noise and flicker noise generated in the switches and OP AMPs are three major noise sources in the switched-capacitor circuits.

§7-2.6 Dynamic range of OP AMPs

$V_{in,max}$: the maximum input voltage which an OP AMP can handle without generating an excess amount of nonlinear distortion.

$V_{in,min}$: the minimum input signal voltage which still does not drown in noise and distortion.

$$\text{Dynamic range} \equiv 20\log_{10}({V_{in,max}}/{V_{in,min}})$$

For an open-loop OP AMP,

$$V_{in,max} \approx V_{cc} / A_d$$

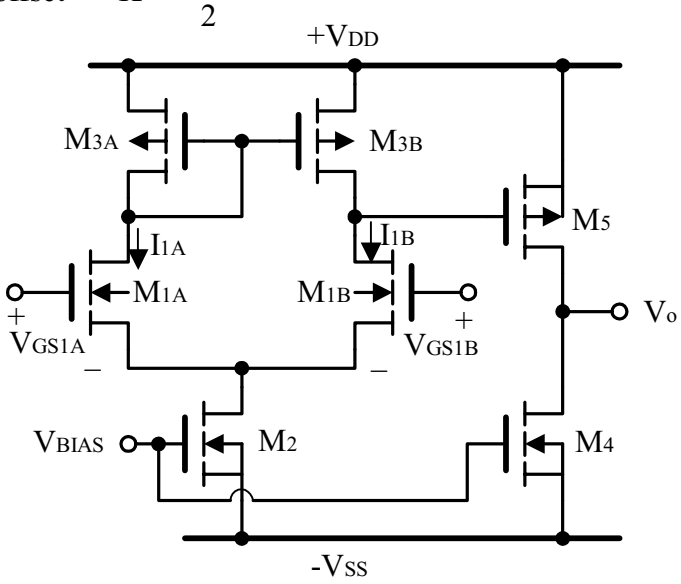
$$V_{in,min} \approx \sqrt{\overline{V_n^2}}$$

$$\Rightarrow \text{ Dynamic range } \approx 30-40\text{dB}.$$

§7-3 Practical Design Consideration on Offset

§7-3.1 Input offset voltage of a CMOS OP AMP

1). Random offset $\quad K \equiv \dfrac{C_{ox}\mu}{2}$



$V_o=V_{DD}-V_{GS3}$

$V_{GS3A}=V_{GS3B}-V_{GS3}$

$$V_{OS} \equiv V_{GSIA} - V_{GSIB} = \left[\frac{2}{K_{N1A}}\left(\frac{L}{W}\right)_{1A} I_{1A}\right]^{\frac{1}{2}} - \left[\frac{2}{K_{N1B}}\left(\frac{L}{W}\right)_{1B} I_{1B}\right]^{\frac{1}{2}} + V_{TH1A} - V_{TH1B}$$

$$= \Delta V_{TH1} + \left(\frac{2}{K_N} I_1\right)^{\frac{1}{2}} \left[\left(\frac{L_1 + \frac{\Delta L_1}{2}}{W_1 + \frac{\Delta W_1}{2}}\right)^{\frac{1}{2}} - \left[\frac{L_1 - \frac{\Delta L_1}{2}}{W_1 - \frac{\Delta W_1}{2}}\right]^{\frac{1}{2}}\right] + \cdots\cdots$$

$$\cong \Delta V_{TH1} + \left(\frac{2}{K_N} I_1 \frac{L_1}{W_1}\right)^{\frac{1}{2}} \left[\left(1 + \frac{1}{2}\frac{\Delta L}{2L_1}\right)\left(1 - \frac{1}{2}\frac{\Delta W}{2W_1}\right) - \left(1 - \frac{1}{2}\frac{\Delta L}{2L_1}\right)\left(1 + \frac{1}{2}\frac{\Delta W}{2W_1}\right)\right] + \cdots$$

$$\cong \Delta V_{TH1} + \left(\frac{2}{K_N} I_1 \frac{L_1}{W_1}\right)^{\frac{1}{2}} \left(\frac{\Delta L}{2L_1} - \frac{\Delta W}{2W_1}\right) - \left(\frac{2}{K_N} I_1 \frac{L_1}{W_1}\right)^{\frac{1}{2}} \left(\frac{\Delta K_N}{2K_N}\right) + \left(\frac{2}{K_N} I_1 \frac{L_1}{W_1}\right)^{\frac{1}{2}} \left(\frac{\Delta I}{2I_1}\right)$$

$$A \equiv \frac{A_1 + A_2}{2} \qquad \Delta A \equiv A_1 - A_2$$

$$\Delta I = I_{1A} - I_{1B} = \frac{K_{P3A}}{2}\left(\frac{W}{L}\right)_{3A}(V_{GS3} - V_{TH3A})^2 - \frac{K_{P3B}}{2}\left(\frac{W}{L}\right)_{3B}(V_{GS3} - V_{TH3B})^2$$

$$= \frac{K_P}{2}\frac{W_3}{L_3}(V_{GS3} - V_{TH3})^2\left(\frac{\Delta K_P}{K_P} + \frac{\Delta W_3}{W_3} - \frac{\Delta L_3}{L_3} - \frac{2\Delta V_{TH3}}{V_{GS3} - V_{TH3}}\right)$$

$$= I_1\left(\frac{\Delta K_P}{K_P} + \frac{\Delta W_3}{W_3} - \frac{\Delta L_3}{L_3} - \frac{2\Delta V_{TH3}}{V_{GS3} - V_{TH3}}\right)$$

$$\Rightarrow V_{OS} = \Delta V_{TH1} + \left(\frac{2}{K_N} I_1 \frac{L_1}{W_1}\right)^{\frac{1}{2}}\left[\frac{\Delta L_1}{2L_1} - \frac{\Delta W_1}{2W_1} - \frac{\Delta K_N}{2K_N} + \frac{\Delta K_P}{2K_P} + \frac{\Delta W_3}{2W_3} - \frac{\Delta L_3}{2L_3} - \frac{\Delta V_{TH3}}{V_{GS3} - V_{TH3}}\right]$$

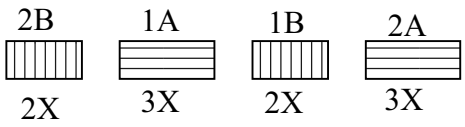
$$\cong \Delta V_{TH1} + (V_{GS1} - V_{TH1})\left(\frac{\Delta W_3}{2W_3} + \frac{\Delta L_1}{2L_1}\right) - \left(\frac{K_P}{K_N}\frac{W_3}{W_1}\right)^{\frac{1}{2}}\Delta V_{TH3} \quad (\text{If } \frac{\Delta L_3}{2L_3}, \frac{\Delta W_1}{2W_1} \to 0)$$

2).Systematic offset. $V_{OS} = \frac{V_{Odc}}{A_O}$ where $V_{Odc} \neq 0$ and A_O is the dc gain of the OP AMP.

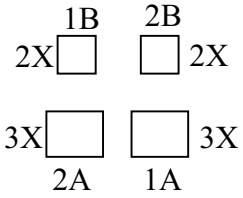
7-3.2 Low offset design techniques for CMOS OP AMPs

1. Layout techniques to reduce the random offset.

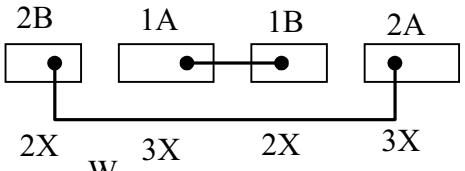
   a).linear varation of devices across a row of transistor or a matrix of transistors.

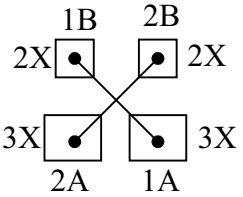


or



   b).cross-coupled connection





$I_{DS} \propto V_{gs}^{\ 2} \cdot \frac{W}{L}$ $L_{2B} = KL_{1B}, L_{2A} = KL_{1A}$, $\frac{L_{1B}}{L_{2A}} = \frac{L_{2B}}{L_{1A}} = N$, W's are the same

Cross-coupled: $I_{DS1A} + I_{DS1B} = I_{DS2A} + I_{DS2B}$

$$\frac{V_{GS1}^{\ 2}}{L_{1A}} + \frac{V_{GS1}^{\ 2}}{L_{1B}} = \frac{V_{GS2}^{\ 2}}{L_{2A}} + \frac{V_{GS2}^{\ 2}}{L_{2B}} \Rightarrow \frac{V_{GS1}}{V_{GS2}} \cong \sqrt{\frac{1+KN}{K+N}}$$

If K=1 => precision channel length control $\Rightarrow \frac{V_{GS1}}{V_{GS2}} \cong 1 \Rightarrow$ Ordered dimension error $\cong 0 \Rightarrow V_{OS} \cong 0$

If K=1.1, N=1.1 ➔ $\frac{V_{GS1}}{V_{GS2}} = 1.0023$

But for single-pair design (1B, 2B, or 1A, 2A)

$\frac{V_{GS1}}{V_{GS2}} = \sqrt{K} = \sqrt{1.1} = 1.049$ larger V_{GS} error ➔ larger V_{OS}

Ref: RCA Review, vol. 39, pp.250-277, June 1978.

c) Common-centroid structures to reduce ΔV_{TH}

Ref: IEEE JSSC, vol. SC-13, pp.791-798, Dec. 1978
IEEE JSSC, vol. SC-16, pp.661-668, Dec. 1981

2.General optimum matching rules to reduce the random offset

1. Same structure
2. Same temperature
3. Same shape, same size
4. Minimum distance
5. common-centroid geometries
6. Same orientation
7. Same surroundings
8. Non minimum size

Ref.: IEEE JSSC, vol. SC-20, pp.657-665, June 1985

3.Low $V_{GS} - V_{TH1}$ to reduce the dimensional random offset

4.Dimension design to eliminate the systematic offset

$\frac{(W/L)_{3A}}{(W/L)_5} = \frac{(W/L)_{3B}}{(W/L)_5} = \frac{1}{2}\frac{(W/L)_2}{(W/L)_4}$ ➔ $V_{odc} = 0$ ➔ systematic offset ≈ 0

To avoid the process-induced variations in channel lengths, we usually choose $L_5 = L_{3A} = L_{3B}$. But this design will enhance the noise contribution from the PMOS M_{3A}, M_{3B} (NMOS M_{3A}, M_{3B} for PMOS-input structure).

➔ A compromise is required.

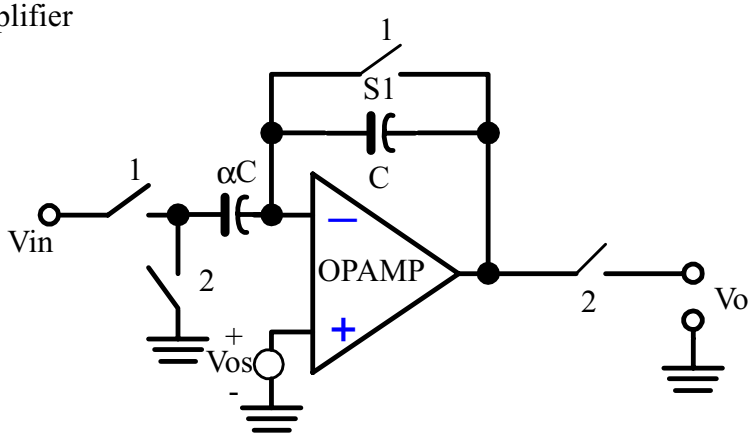
5.Sample-data techniques to eliminate the offset voltage.

Ref.: IEEE JSSC, p.499, Aug. 1978
IEEE JSSC, vol. SC-10, pp.371-379, Dec. 1975
IEEE JSSC, vol. SC-20, pp.805-807, June. 1985
IEEE JSSC, vol. SC-17, pp.1008-1013, Dec. 1986
IEEE JSSC, vol. SC-16, pp.745-748, Dec. 1981
IEEE JSSC, pp.837-844, Aug. 1985

Applications: Zero-offset OP AMPs, High-precision comparators, Instrumentation amplifiers, High-precision amplifiers, Switched-capacitor amplifier, Switched-capacitor network.

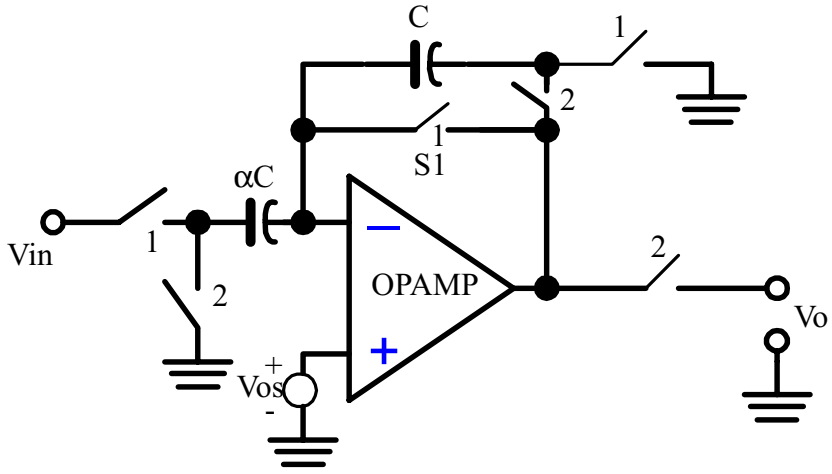
1) Offset cancellation in OP-AMP-based switched-capacitor(SC) amplifier

(1) SC amplifier

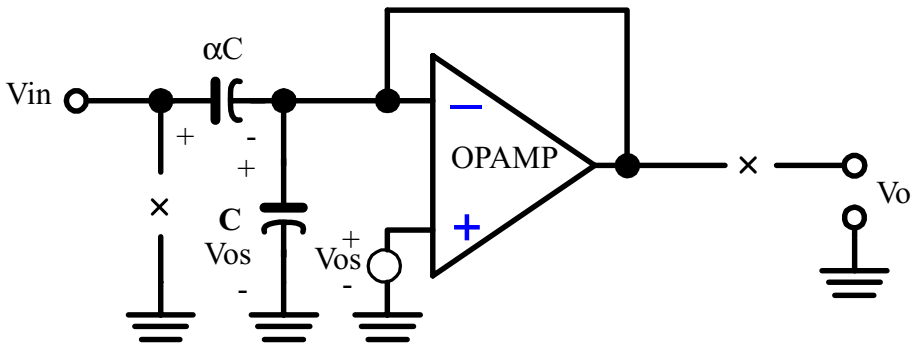


$$\frac{Vin\alpha C}{C}+V_{OS}=V_O \qquad \Rightarrow \frac{V_O}{V_{in}}=\alpha+\frac{V_{OS}}{V_{in}}$$

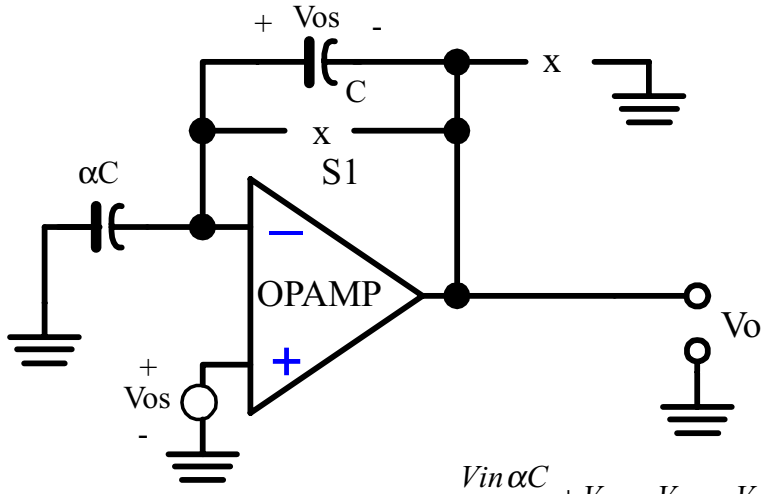
(2) Modified SC Amplifier



Step 1: Switch 1 ON, Switch 2 OFF:



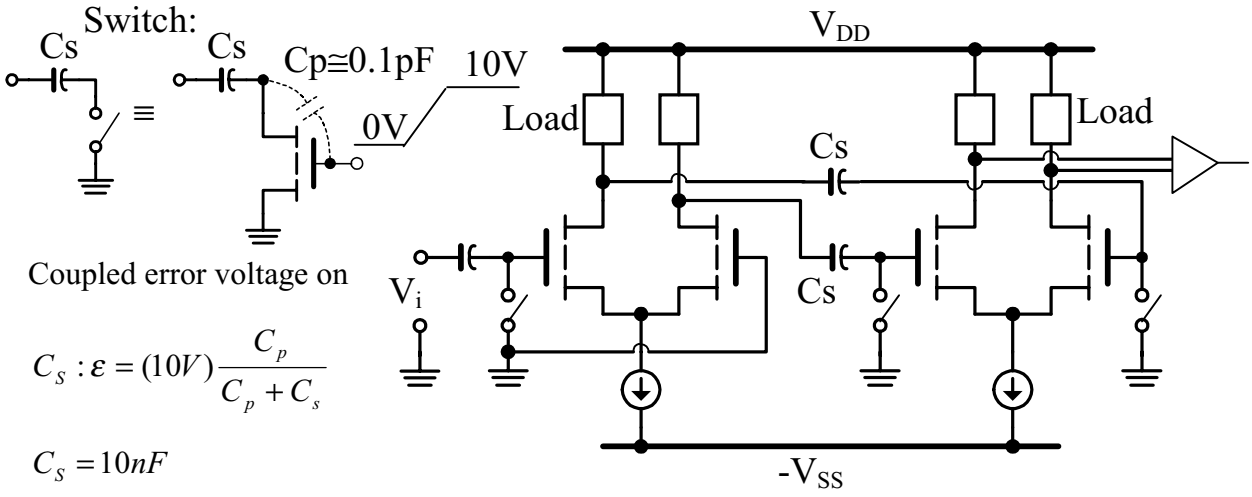
Step 2: Switch 2 ON, Switch 1 OFF:



$$\frac{Vin\,\alpha C}{C} + V_{OS} - V_{OS} = V_O$$

*The charge injection error of the switched S1 cannot be eliminated.

2) Offset cancellation in precision amplifier



Coupled error voltage on

$$C_S : \varepsilon = (10V)\frac{C_p}{C_p + C_s}$$

$$C_S = 10nF$$

$$\Rightarrow \varepsilon = 10V\,\frac{0.1pF}{0.1pF + 10000\,pF}$$

$$= 100\mu V$$

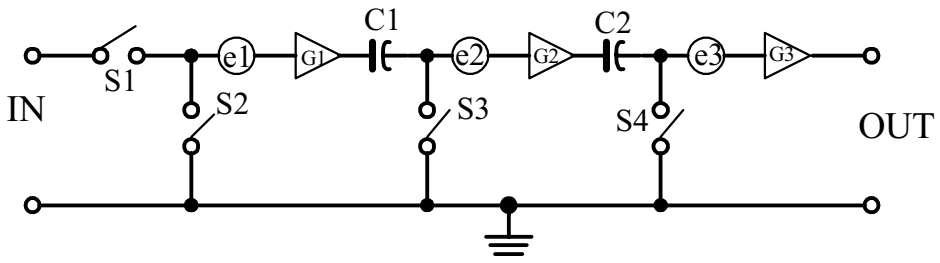
$$C_S \uparrow \varepsilon \downarrow$$

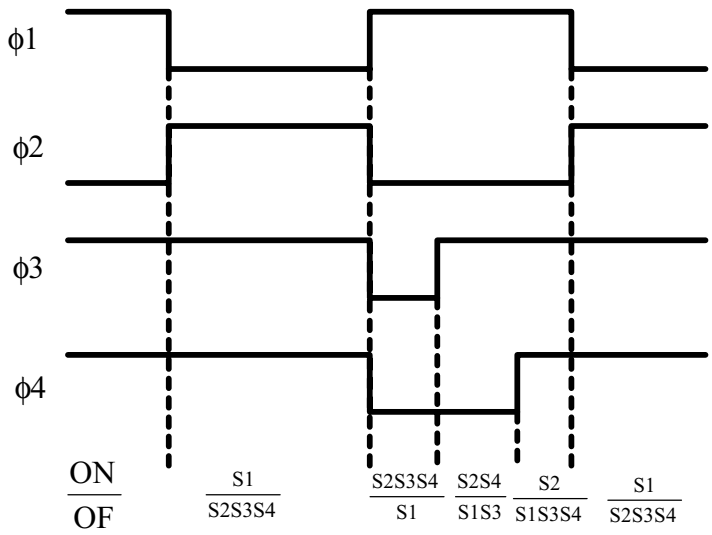
or using the differential outputs rather than the single output to eliminate the common mode voltage ε

* amplifier with offset voltage memorization
* residual voltage successive memorization (RSM) amplifier
* auto-zero design
* chopper-stablized design

※ capable of reducing the offset voltage by 1~4 order of magnitude

RSM amplifier(P-MOSFETs)





$V_{off} = (e_n + \varepsilon_n) / G_1 G_2 ... G_{n-1}$

e_n : input offset voltage

ε_n : parasitic clock error pulse of the nth stage

Chapter 8 Advanced Design Techniques and Recent Design Examples of CMOS OP AMPs

§8-1 Advanced Design Techniques of CMOS OP AMPs

§8-1.1 Improved PSRR and frequency compensation

P.6-26

$$\frac{\partial V_{out}}{\partial V_{ss}} \approx \frac{C_{gs}}{C_I}\left[\frac{\partial I_o}{\partial V_{ss}}\frac{1}{2g_{m1}}+\frac{\partial V_{GS1}}{V_{ss}}\right]+\frac{C_{gd}}{C_I}\frac{1}{2g_{m3}}\frac{\partial I_o}{\partial V_{ss}}$$

$$\frac{\partial V_{out}}{\partial V_{DD}} \approx \frac{C_{gd}}{C_I}\left[1-\frac{\partial I_o}{\partial V_{DD}}\frac{1}{2g_{m3}}\right]+\frac{C_{gs}}{C_I}\frac{1}{2g_{m1}}\frac{\partial I_o}{\partial V_{DD}}$$

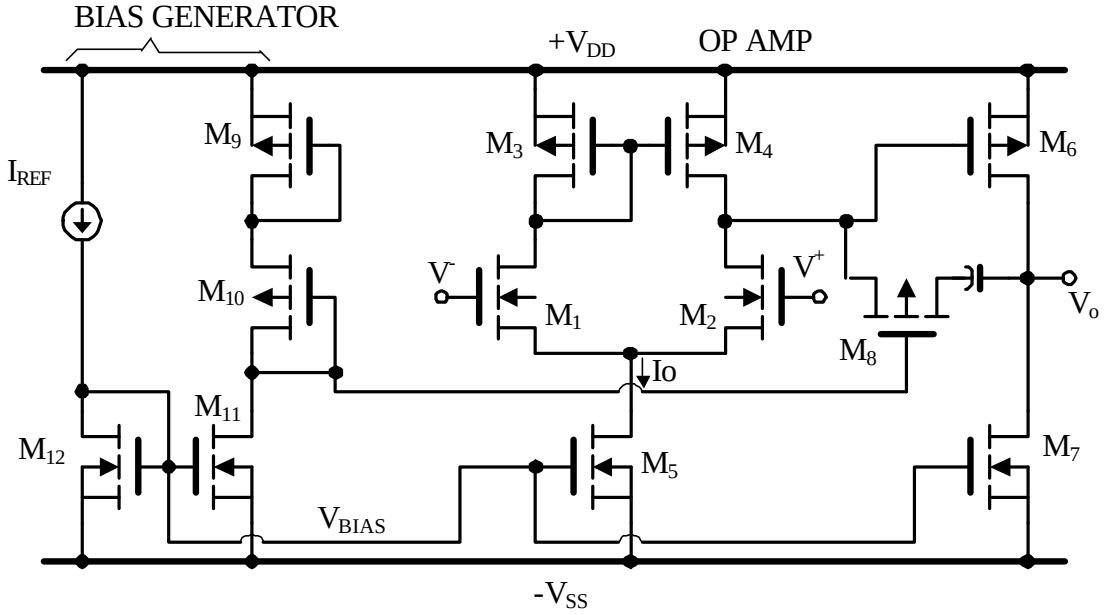
Where I_o represents the input stage bias current.

If I_o is independent of V_{ss} and V_{DD}

and the input devices have no body effect.

==> $\frac{\partial V_{out}}{\partial V_{ss}} \to 0$ $\frac{\partial V_{out}}{\partial V_{DD}} \to -\frac{C_{gd}}{C_I}$

Ref.: IEEE JSSC, vol. SC-15, pp.929-938, Dec. 1980



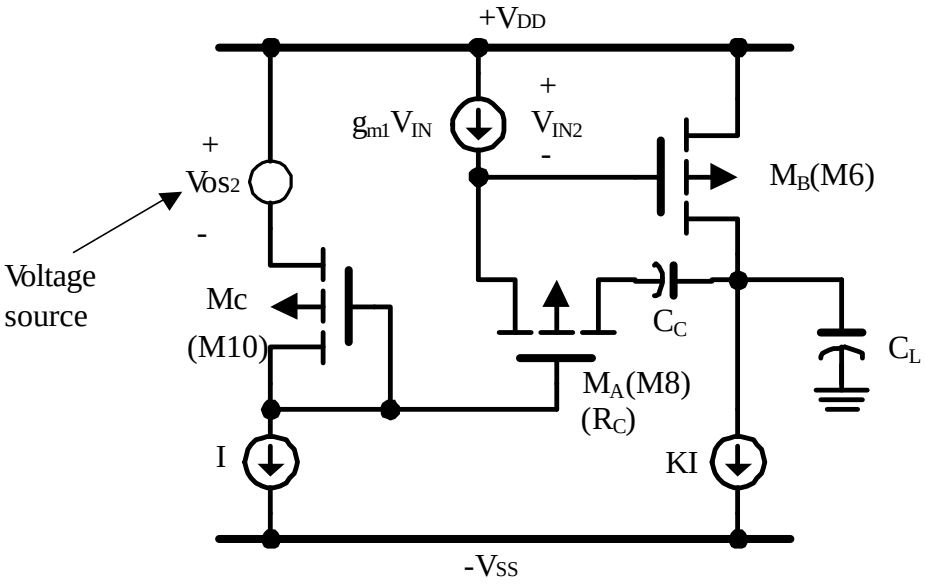
* I_{REF} is generated by using the power supply independent current source.

* V_{BIAS} is nearly independent of V_{DD} and V_{ss}.

*It is better to use separate p-wells for M_1 and M_2 to avoid the body effect.

*Tracking RC compensation

Conceptual circuits :



In the quiescent case ,$Vin_2=V_{OS2}$

$$\text{If } (W/L)_A \approx [(W/L)_B \bullet (W/L)_C \bullet K]^{1/2} \frac{Cc}{Cc+C_L}$$

$$\Rightarrow R_{dsA} \approx \frac{Cc+C_L}{g_{m2}Cc} \approx Rc$$

The requires Rc is $Rc = 1/g_{m2}[1+(C_d+C_L)/Cc] \approx 1/g_{m2}[(Cc+C_L)/C_C]$

Thus LHP zero=LHP pole P2

and P3 becomes the second pole.

The stability considerations,

$$P_3 \geq A_{do}P_1$$

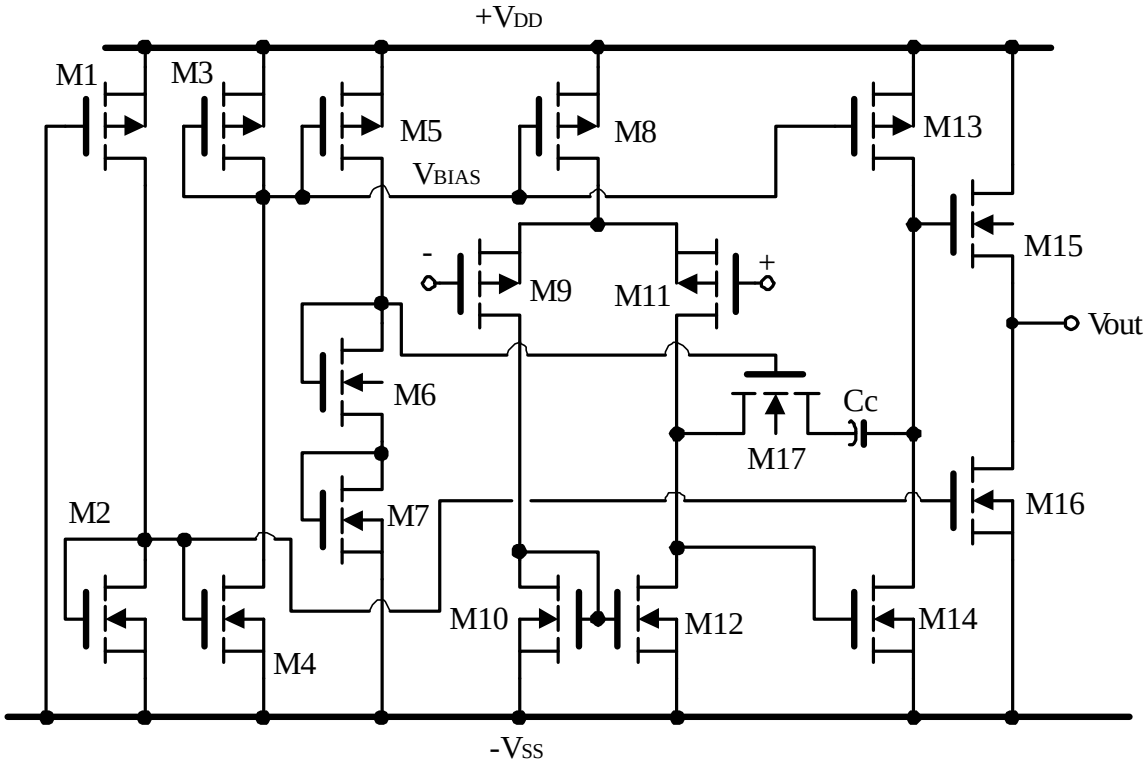
or $$Cc \geq \sqrt{\frac{g_{m1}}{g_{m2}}c_1c_L}$$

allows a smaller gm2 and larger C_L

* $R_{dsA} \approx Rc$ indep of temperature, process , and supply variations.

=>Tracking design to make sure that z=P_2

=>No pole-zero doublet problem!

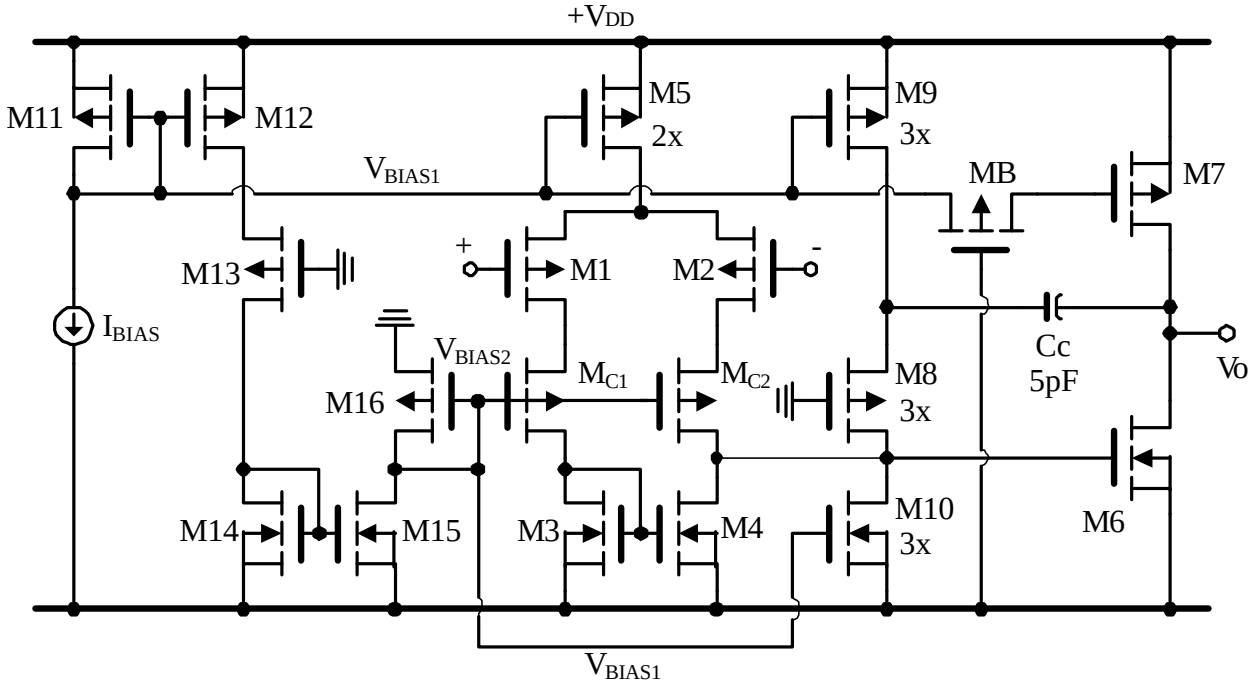


* M17,Cc : Tracking RC compensation.
* M9,M11:Sharing the separate n-well.
* V_{BIAS} is not strictly independent of V_{DD} and V_{SS}.

§8-1.2 Improved frequency compensation technique.

Ref.: IEEE JSSC ,vol.sc-18, pp 629-633, Dec.1983

Grounded gate cascode compensation

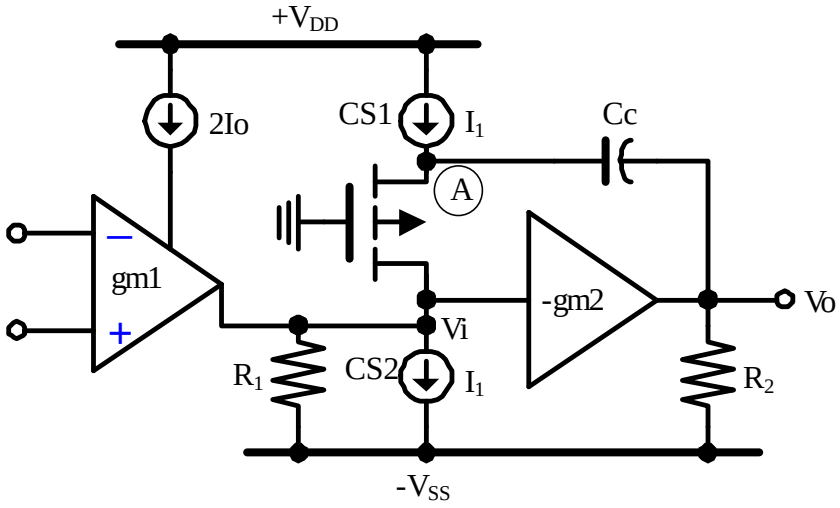


MB,Cgs_7:low pass filter for high frequency noises.

M8,M9,M10:new compensation circuit.

M11~M16:Bias generator.

Conceptual circuits:



Net current in C_C $(C_c \frac{d}{dt} V_o)$ enters the second stage.

The input voltage Vi can' t reach the node Ⓐ

➔ * Better PSRR (∵ no low-freq. zero) , especially PSRR

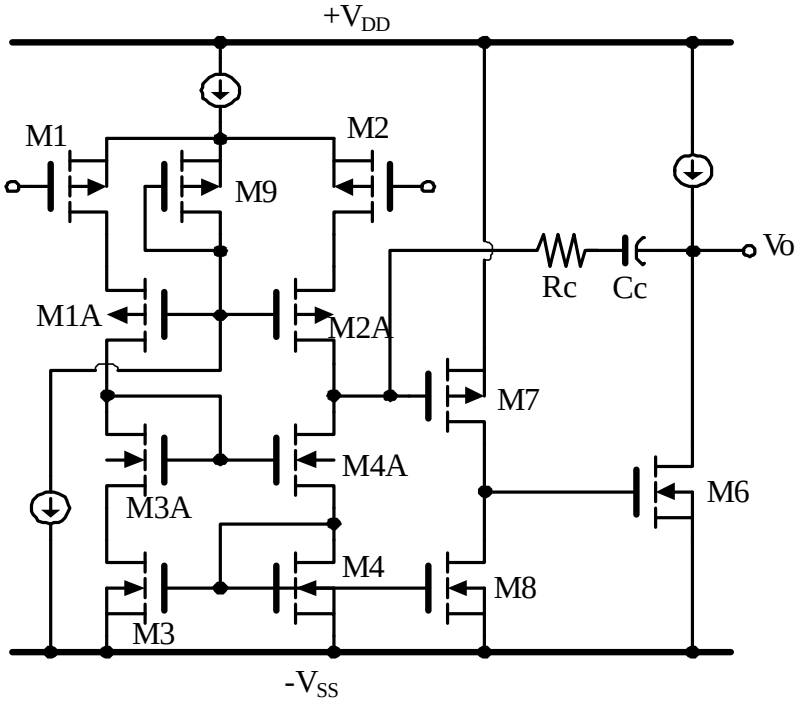
* Allow larger capacitive loads.

* Slight increase in complexity , random offset and noise.

§ 8-1.3 Improved cascode structure

1. To improve gain:

Ref: IEEE JSSC , vol. SC-17, pp. 969-982, Dec. 1982 ☆☆

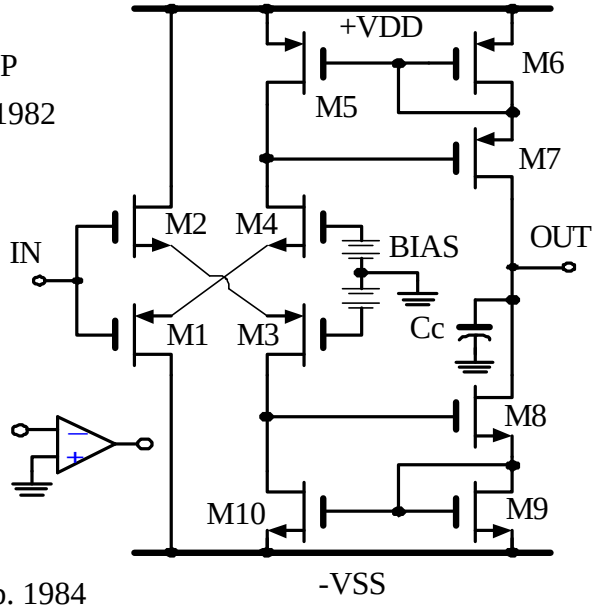


* Substantial reduction in input-stage common-mode range.
* Improved wilson current source is used as the load to improve the balance of the first stage.

2. Single-stage push-pull class AB CMOS OP AMP

Ref: IEEE JSSC , vol.sc-17, pp.969-982, Dec. 1982

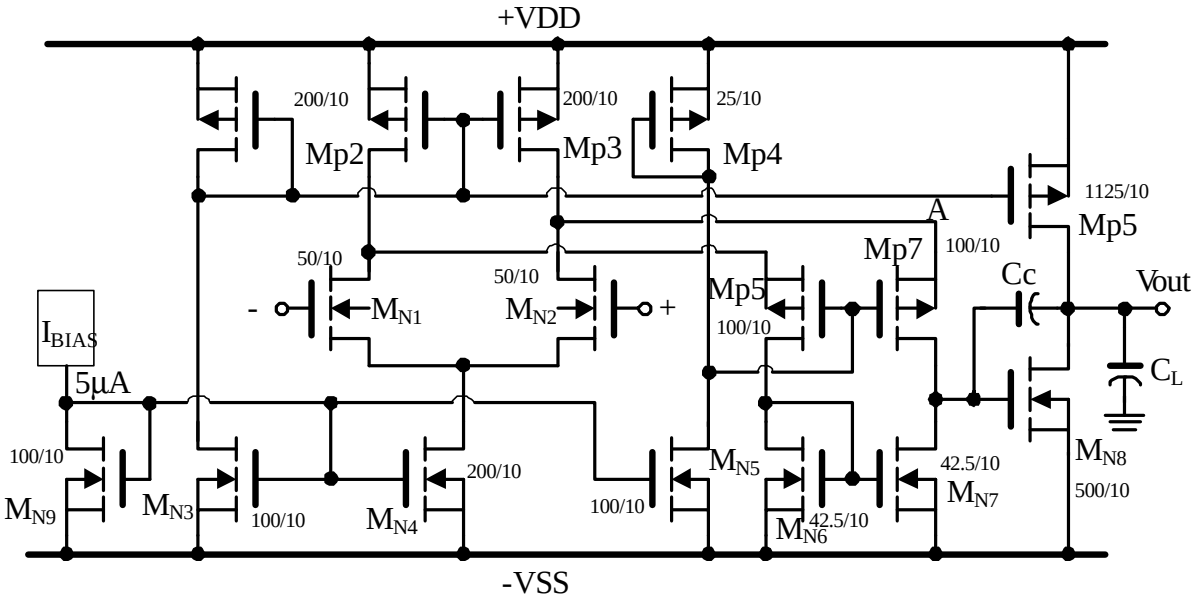
* Inverting mode only. (+ grounded)
* Capable of high current driving and high voltage gain.
* Not a differential-amplifier-based OP AMP.



3. Cascoded CMOS OP AMP with high ac PSRR

Ref: (1) IEEE JSSC , vol. SC-19, pp.55-61, Feb. 1984
(2) IEEE JSSC , vol SC-19, pp. 919-925, Dec. 1984

1) Original version

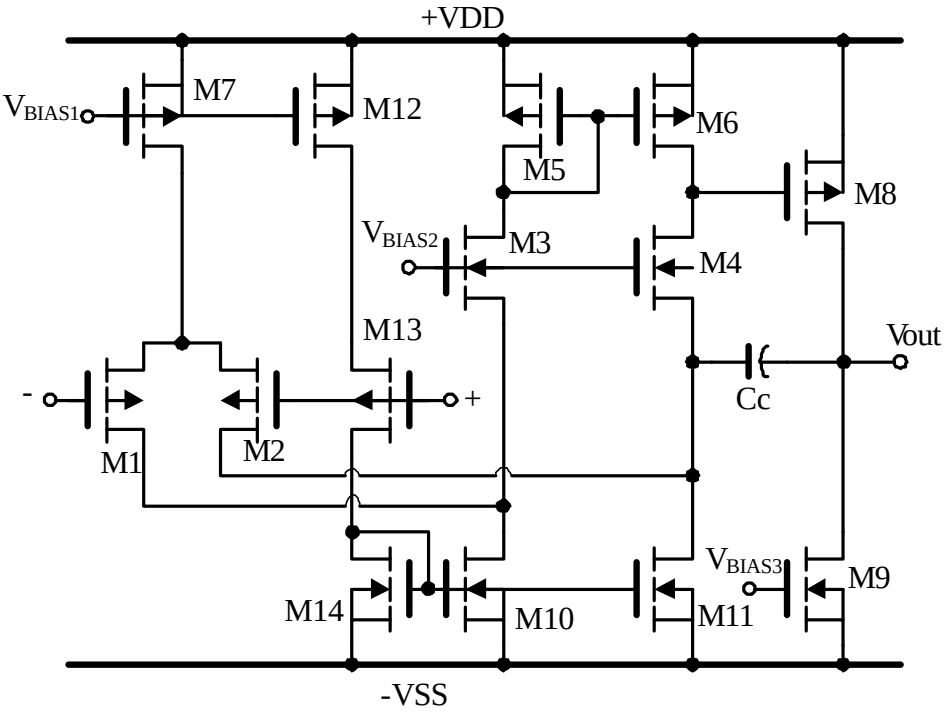


Chrarcteristics:

V_{DD}=V_{SS}=2.5V	
Input offset voltage	5mV
Supply current	100ì A
Output voltage range	-V_{SS}~V_{DD}
Input common mode range	-V_{SS}+1.47V ~ V_{DD}
CMRR @ 1KHz	99dB
Unity-gain frequency	1.0MHz
Slew rate	1.8 V/ì sec

* Better input common-mode range.
* Vic↓ ➔ V_{DSN4}↓ ➔ I_{DSN4}↓ ➔ V_A↑ ➔ M_{N8} is turned on ➔ V_{out}→-V_{SS} voltage spike at V_{out}.
* The possible spike in the settling period.

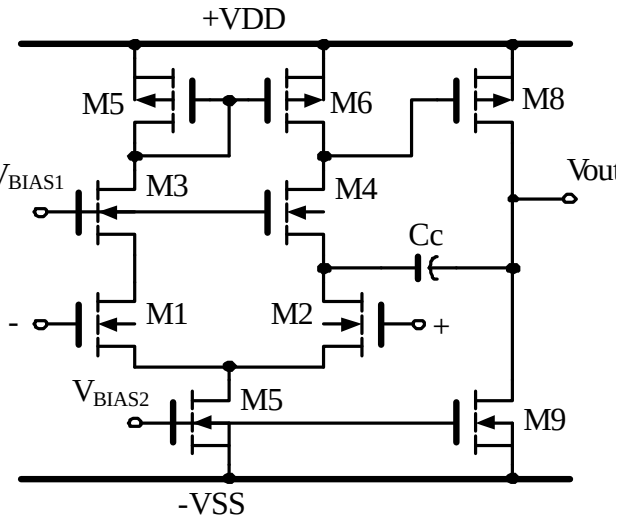
2) Improved version



* M_{12}, M_{13} and M_{14} : Let the drain bias currents of M_{10} and M_{11} follow the change of I_{D7} under positive input common mode voltage.
  ⇒ No voltage spike at V_{out}
  Also serves as CMFB
* Better PSRR and input common-mode range.
* C_c is decoupled from the gate of the driver M_8.

4.Simple cascoded CMOS OP AMP

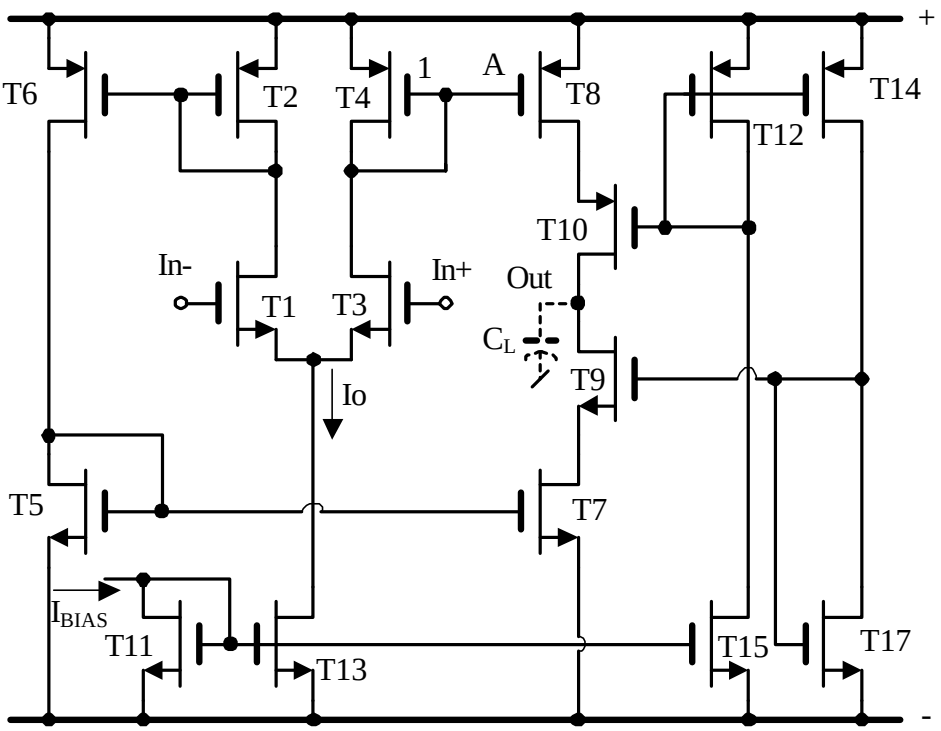
Ref.:IEEE JSSC , vol.SC-19 , pp.919~925 , Dec. 1984



* Good PSRR
* Reduced input common range.
  ⇒ restrict its applications to those which use a virtual ground.

5.Single-stage cascode OTA

Ref.: IEEE JSSC , vol. SC-20 , pp.657~665 , June 1985 ☆☆



T_9, T_{10} : Cascode structure

* Output conductance ↓ without any noise penalty and with only a very small reduction of phase margin.

  ⇒ Gain↑ no any compensation is necessary.

* Maximum output swing↓

§ 8-2 Advanced Design Techniques on High-frequency Non-differential-type CMOS OP AMPs

1. Single-ended push-pull CMOS OP AMP

*Current-gain-based design

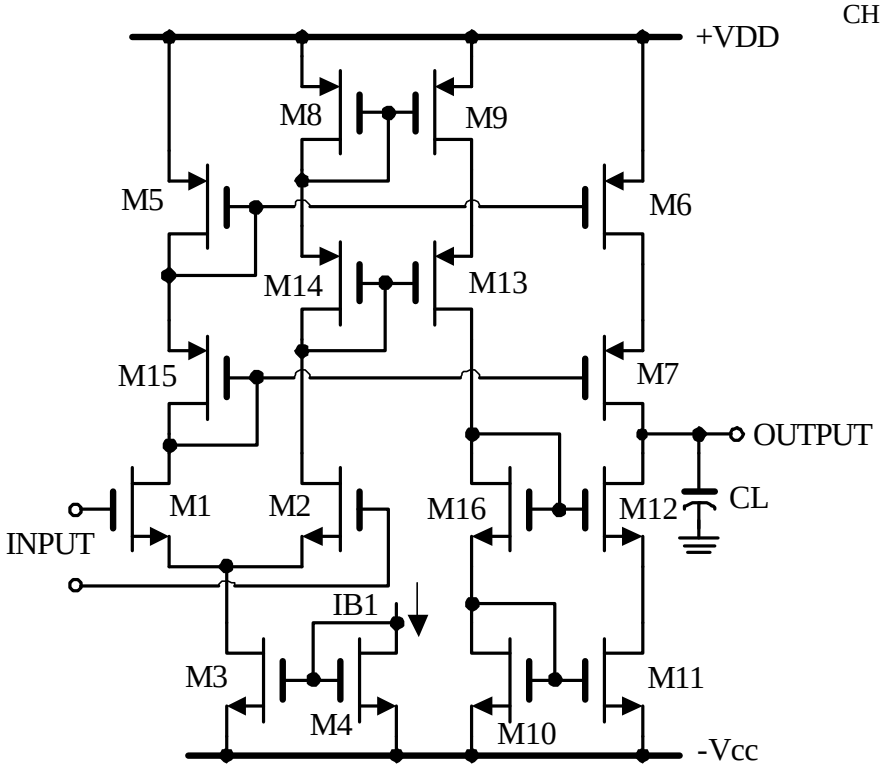


TABLE I

Parameter	Measured Value
DC-Open Circuit Gain	69dB
Unity0Gain Bandwidth	70MHz
Phase Margin	40^o
Slew Rate	$200V / m\text{sec}$
PSRR (DC^+)	68dB
PSRR (DC^-)	66dB
Input Offset Voltage	10mV
CMRR (DC)	62dB
Output Voltage Swing	$1.5V_P$
Output Resistance	$3M\Omega$
Input Referred Noise (@1KHz)	$0.54mV/\sqrt{Hz}$
DC-Power Dissipation	1.1mWatt

$V_{DD} = +3V$; $V_{CC} = -3V$; $I_{B1} = 50mA$; CL=1pF

TABLE II

Bias Current	Unity-Gain Bandwidth	DC-Open Circuit Voltage Gain	DC-Power Dissipation
$25mA$	50MHz	70dB	0.55mW
$50mA$	70MHz	69dB	1.1mW
$100mA$	100MHz	66dB	2.2mW

$V_{DD} = +3V$; $V_{CC} = -3V$; CL=1pF

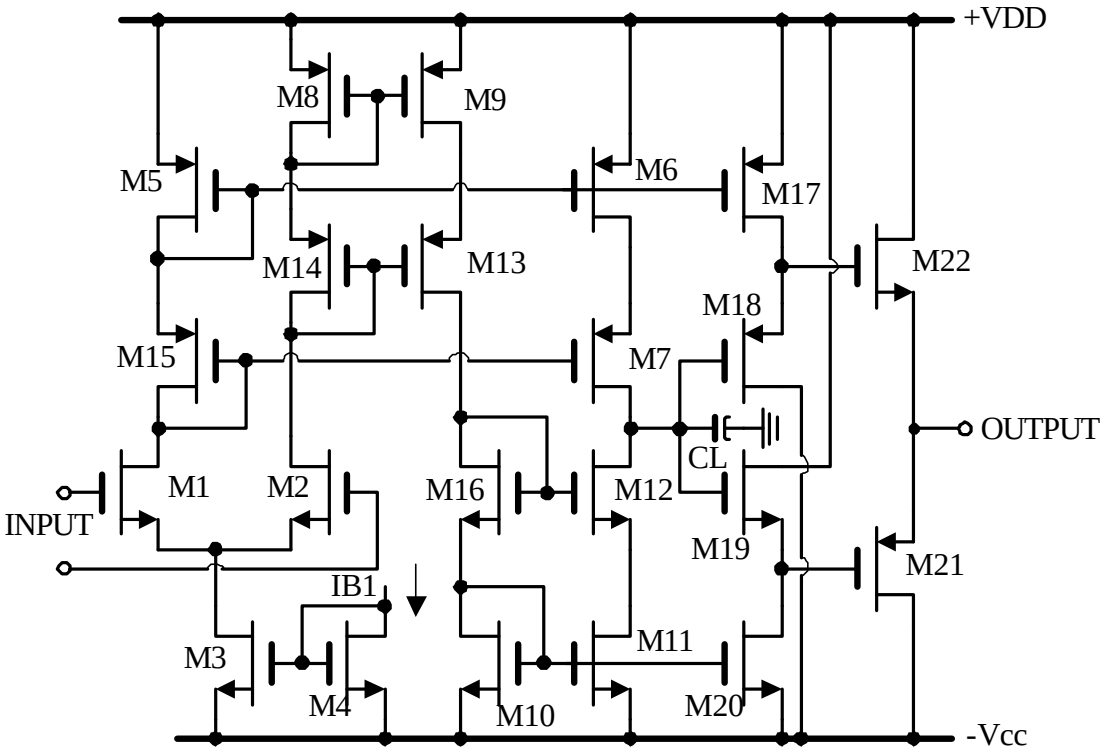
2.Low output resistance CMOS OP AMP

*C_L is a compensation capacitor

*For low-resistance load

*Smaller maximum output voltage swing.

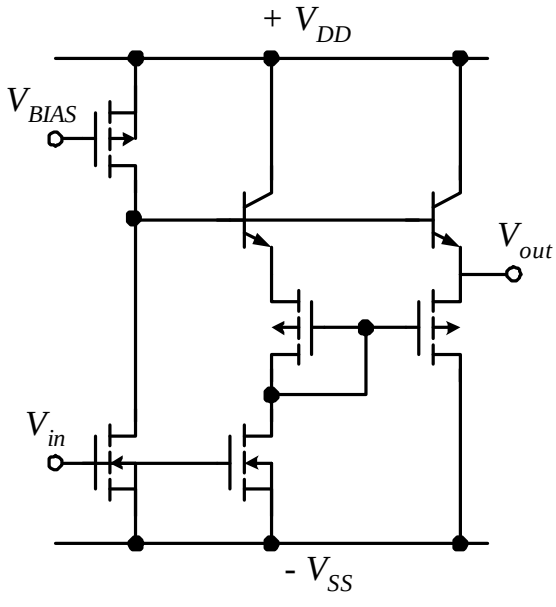
* $I_{B1} = 50mA, C_L = 1pF$, $f_u = 60MHz$



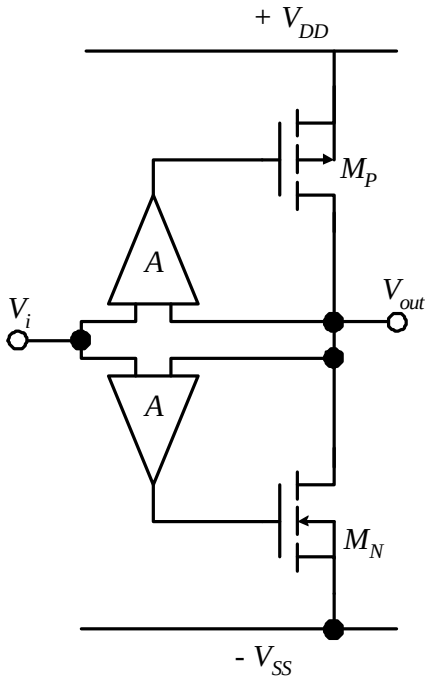
§ 8-3 Advanced Design Techniques on High-drive MOS Power or Buffer OP AMPs

§ 8-3.1 Efficient Output Stages.

A. CMOS output stage using a biplar emitter follower and a low-threshold PMOS source follower.

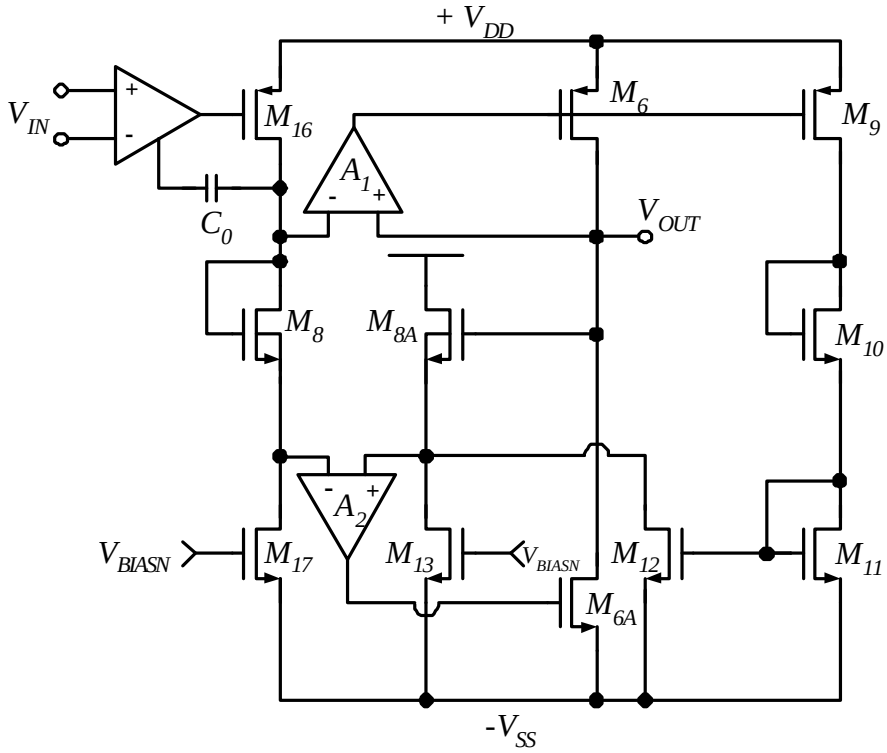


B. Complementary class B output stage using compound devices with common-source output MOS.

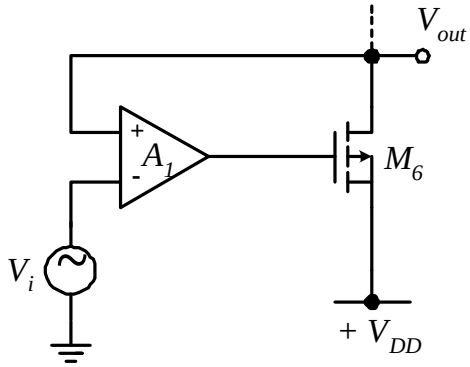


§ 8-3.2 High-drive power or buffer CMOS OP AMPs

1. Large swing CMOS power amplifier (National Semiconductor)



* Noninverting unity gain amplifier



$V_{in} \cong V_{out}$

M_6 provides the negative feedback

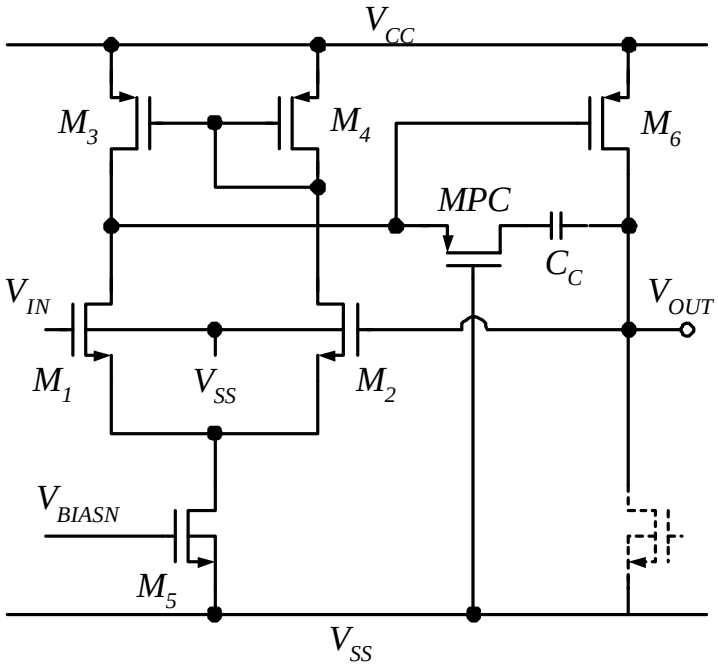
* A_1, M_6 and A_2, M_{6A} form a class AB push-pull output stage.

* Full swing from $+V_{DD}$ to $-V_{SS}$

* $M_9, M_{10}, M_{11},$ and M_{12} form a current feedback to stablize the bias current of M_6 and M_{6A}.

Offset in A_1 ,e.g. $V_{inA1}^- \uparrow \Rightarrow V_{outA1} \downarrow \Rightarrow I_{DM6} \uparrow$ and $I_{DM9} \uparrow \Rightarrow I_{DM11} \uparrow$ and $I_{DM12} \uparrow \Rightarrow V_{GSM8A} \uparrow$ and $V_{inA2}^+ \downarrow \Rightarrow V_{out} \uparrow$, i.e. $V_{inA1}^+ \uparrow \Rightarrow V_{out} \downarrow \Rightarrow V_{inA1}^- \downarrow$ (virtual short between + and -) $\Rightarrow V_{inA2}^- \downarrow$ througt $M_8 \Rightarrow$ All the bias voltage and current are restored to the normal values and the offset is absorbed by M_{8A}.

Since the current feedback is not unity gain ,some current variation in transistors M_6 and M_{6A} still exists.



Large positive common mode range allows M_6 to source large amount of current to the load. (because $V_{in} \cong V_{out}$)

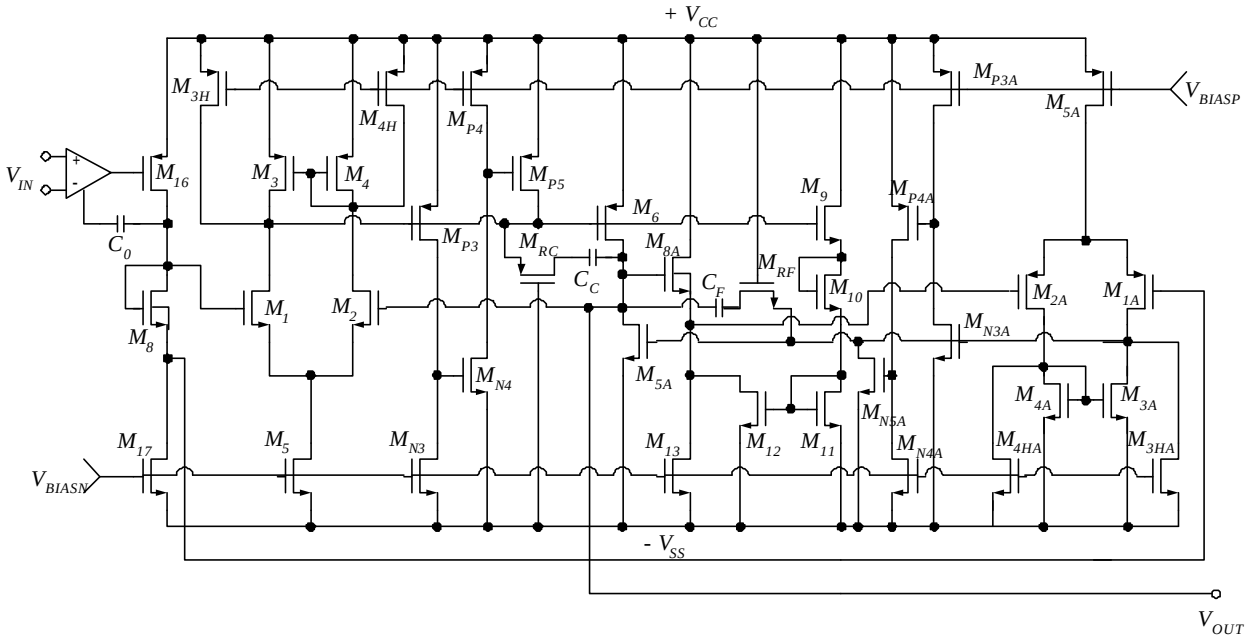
The maximum V_{GS6} which M_1 and M_2 still in the saturation region is

$$V_{GS6\,max} = -(V_{DD} - (V_{IN} - V_{GS1} + V_{DSAT1})) = -(V_{CC} - V_{IN} + V_{TH1})$$

$$\Rightarrow V_{TH1} \uparrow \Rightarrow V_{GS6\,max} \uparrow \Rightarrow I_{DM6} \uparrow$$

(1). Threshold implant to increase V_{THO1}

(2). Negative substrate bias $-V_{SS}$ to increase V_{TH1}



* The input stage is not shown in the diagram.

* M_{16}, M_8, M_{17} form the second stage with C_D the Miller compensation capacitor.

* If $V_{out} \to -V_{SS}, V_{DSM5} \to 0$ and $I_{DSM5} \to 0$.

$\Rightarrow M_1, M_2, M_3$ and M_4 are off

$\Rightarrow M_{3H}$ and M_{4H} are still on to keep $V_{GS6} \cong 0V$.

Otherwise, M_6 will be turned on.

Similarly, M_{3HA} and M_{4HA} turn off M_{6A} in the positive voltage swing

* $M_{P3}, M_{N3}, M_{N4}, M_{P4}$ and M_{P5} are output short-circuit protection circuitry.

Normally, M_{P5} is off.

When $I_{DM6} \cong 60mA$, $I_{DMP3} \uparrow \Rightarrow I_{DMN4} \uparrow \Rightarrow V_{GSMP5} \uparrow$.

$\Rightarrow I_{DM6}$ is limited to approximately 60 mA.

Table I

POWER AMPLIFIER PREFORMANCE

Parameter	Simulation	Measured Results
Power dissipation($\pm 5V$)	7.0mW	5.0mW
A_{vol}	82dB	83dB
F_u	500KHz	420KHz
V_{offset}	0.4mV	1mV
PSRR+(dc)	85dB	86dB
(1KHz)	81dB	80dB
PSRR-(dc)	104dB	106dB
(1KHz)	98dB	98dB
THD V_{IN}=3.3V_p R_L=300Ω	0.03%	0.13%(1KHz)
C_L=1000 pF	0.08%	0.32%(4KHz)
V_{IN}=4.0V_p R_L=15 kΩ	0.05%	0.13%(1KHz)
C_L=200 pF	0.16%	0.20%(4KHz)
$T_{settling}$ (0.1%)	3.0us	<5.0us
Slew rate	0.8V/us	0.6V/us
1/f noise at 1KHz	N/A	130nV/Hz
Broad-band noise	N/A	49nV/Hz
Die area		1500$mils^2$

TABLE II

COMPONENT SIZES (μm, pF)

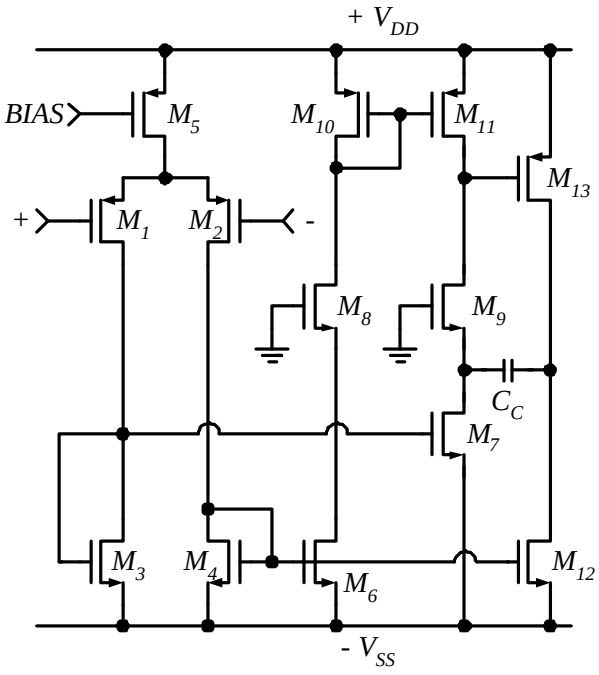
MI6	184/9	M8A	481/6
MI7	66/12	M13	66/12
M8	184/6	M9	27/6
M1,M2	36/10	M10	6/22
M3,M4	194/6	M11	14/6
M3H,M4H	16/12	M12	140/6
M5	145/12	MP3	8/6
M6	2647/6	MN3	244/6
MRC	48/10	MP4	43/12
CC	11.0	MN4	12/6
M1A,M2A	88/12	MP5	6/6
M3A,M4A	196/6	MN3A	6/6
M3HA,M4HA	10/12	MP3A	337/6
M5A	229/12	MN4A	24/12
M6A	2420/6	MP4A	20/12
MRF	25/12	MN5A	6/6
CF	10.0		

Maximum loads : 300Ω and 1000pF to ground.

Ref.:IEEE JSSC , vol.SC-18 , pp.624-629 , Dec.1983

2. High-performance CMOS power amplifier (Siemens AG)

(1). New input stage : 3 gain stages.



* Cc is connected to the source of M_9 to improve PSRR

* Three poles and one zero :

$$Z = \frac{-2g_{m6}g_{m8}g_{m13}}{C_c g_{m6} g_{m13} + C_1 g_{m8} g_{m12}} \qquad \text{LHP.}$$

$$P_1 \cong \frac{-g_{ds10}g_o}{g_{m13}C_c}$$

$$P_2, P_3 \cong \frac{-g_{m8}(C_c + C_O)}{2C_O C_c} \pm j\left[\frac{g_{m8}g_{m13}}{C_O C_1} - \left(\frac{g_{m8}(C_O + C_C)}{2C_O C_c}\right)^2\right]^{1/2}$$

where $g_o \equiv g_{ds12} + g_{ds13}$

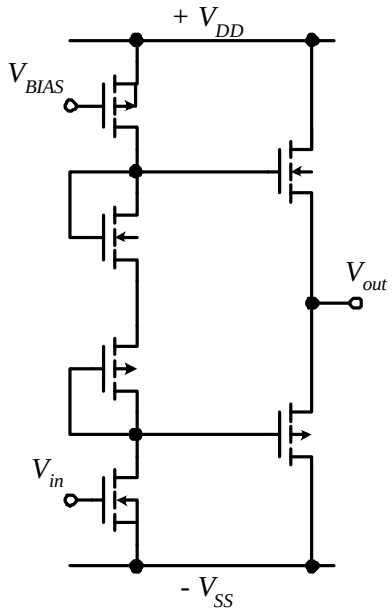
$$C_O = C_L + C_{db12} + C_{db13}$$

$$C_1 = C_{gs13} + C_{db11} + C_{db9} + C_{gd9}$$

Design guidelines for stability :

g_{m8} large , $g_{m13} >> g_{m6}$

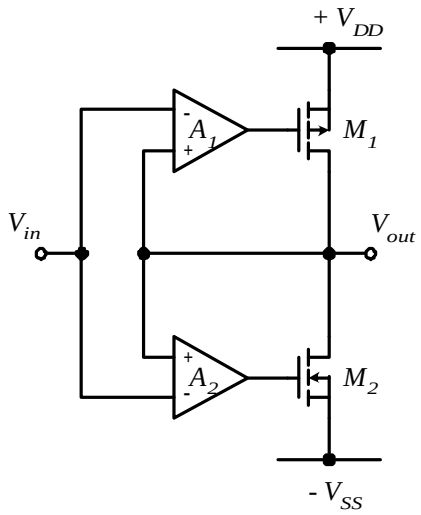
(2). Output stage



Class AB source follower

* One pole and one zero at high frequencies.

* Not full swing

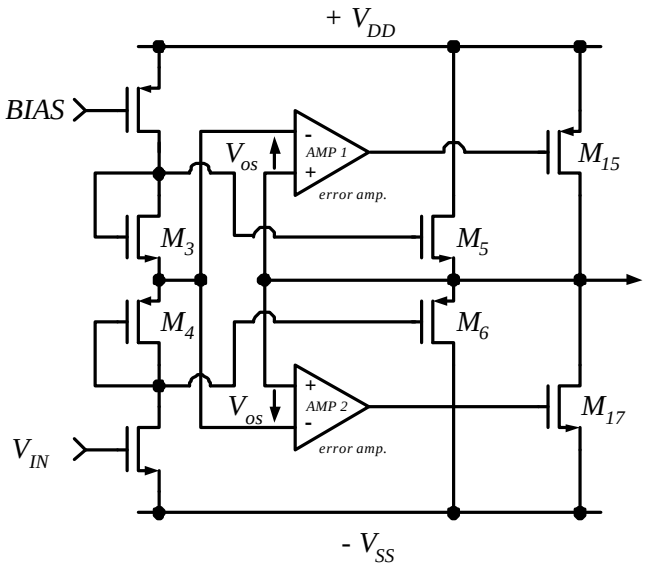


Pseudo source follower

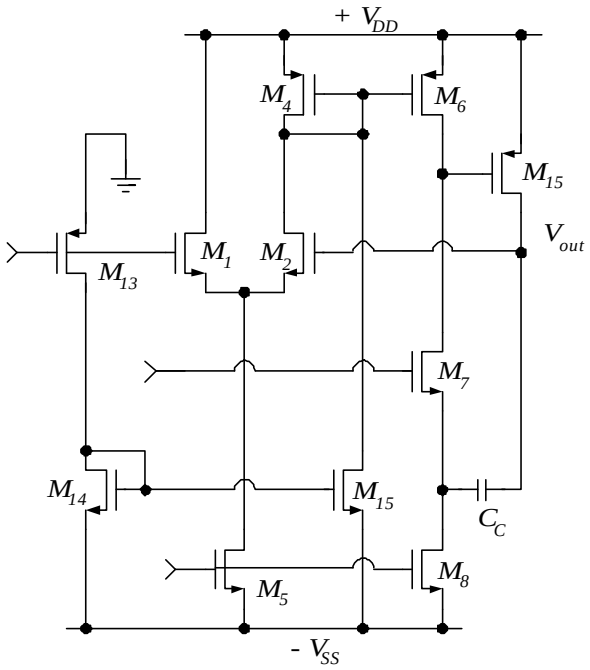
* The quiescent current in M_1 and M_2 will vary widely with variations in Vos1 and Vos2.
* Suitable common-mode range of the two amplifiers A_1 and A_2 are required.
* Large phase shift at high frequencies due to A_1 and A_2 $\Rightarrow$ stability problem.

Combined output stage:

* M_1 and M_2 are turned off in the quiescent state by building a small offset voltage into A_1 and $A_2 \Rightarrow M_3$-M_6 control the output quiescent currents.
* M_2 (M_1) sinks (sources) approximately 95% of the required currents.
* M_1 and M_2 provide a high-frequency feed-forward path.



Still has a smaller swing limited by M_5, M_6 .



* M_{13}, M_{14} and M_{15} form a circuit to turn off M_{15} when $V_{out} < V_{TP13}$ (negative)
* C_c : compensation.
* Three poles and one zeros.

$$Z_1 \approx -\frac{g_{m7} + g_{mbs7}}{C_c + C_{gs7}}$$

$$P_1 \approx \frac{-g_L}{C_L + C_C \dfrac{g_{m15}}{g_{ds6}}}$$

$$P_2, P_3 \approx -\frac{g_{m7}(C_c + C_L)}{2C_cC_L} \pm j\left[\frac{g_{m7}g_{ds6}(C_L + C_c\dfrac{g_{m15}}{g_{ds6}})}{C_cC_LC_1} - \left(\frac{g_{m7}(C_c + C_L)}{2C_cC_L}\right)^2\right]^{\frac{1}{2}}$$ where

$$C_1 = C_{gs9} + C_{db6} + C_{db7} + C_{gd7}$$

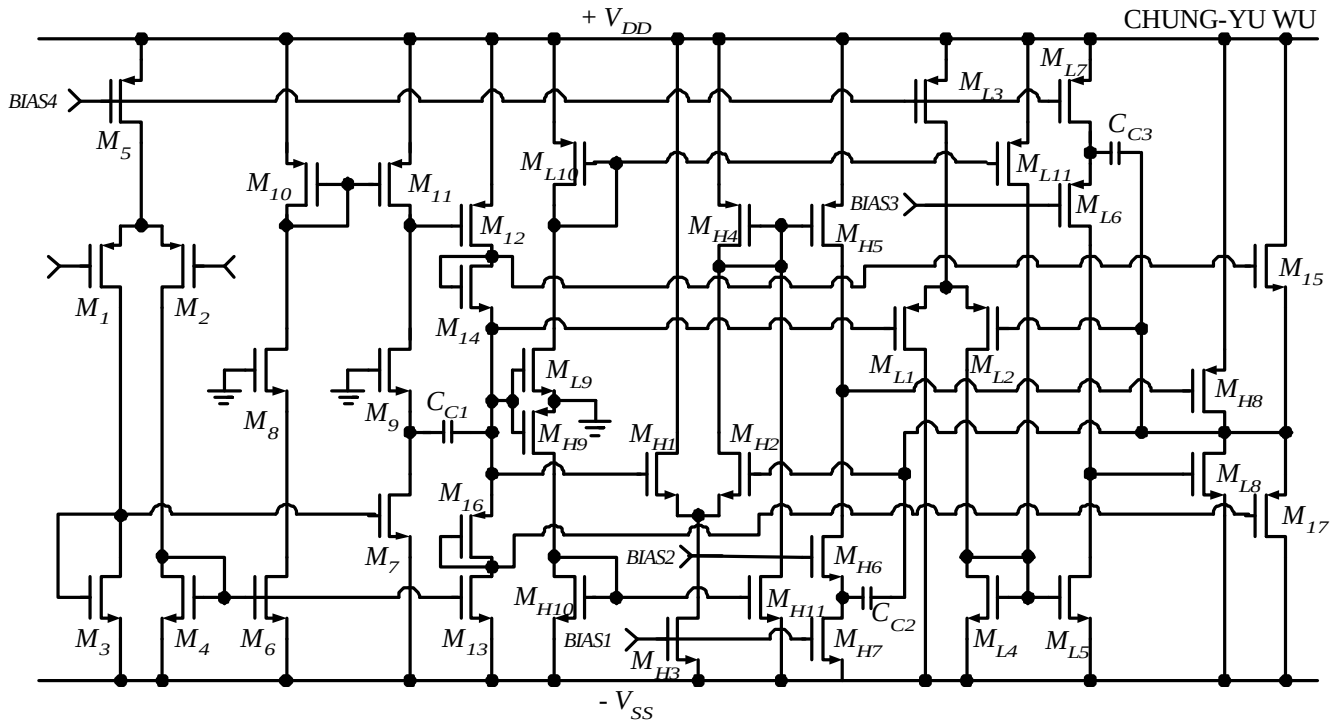


TABLE I Component Sizes

M1	400/15	MH1	48/10	ML1	48/6
M2	400/15	MH2	50/10	ML2	50/6
M3	150/10	MH3	500/15	ML3	300/15
M4	150/10	MH4	300/6	ML4	150/5
M5	100/15	MH5	300/6	ML5	100/5
M6	150/10	MH6	200/5	ML6	300/6
M7	150/10	MH7	250/15	ML7	100/15
M8	300/5	MH8	700/6	ML8	400/5
M9	300/5	MH9	15/6	ML9	5/5
M10	300/10	MH10	10/15	ML10	5/15
M11	300/10	MH11	20/15	ML11	15/15
M12	1200/10	Cc1	20pf		
M13	600/10	Cc2	4pf		
M14	200/5	Cc3	4pf		
M15	200/5				
M16	600/6				
M17	600/6				

TABLE II

POWER AMPLIFIER PERFORMANCE SUMMARY

(First Revision)

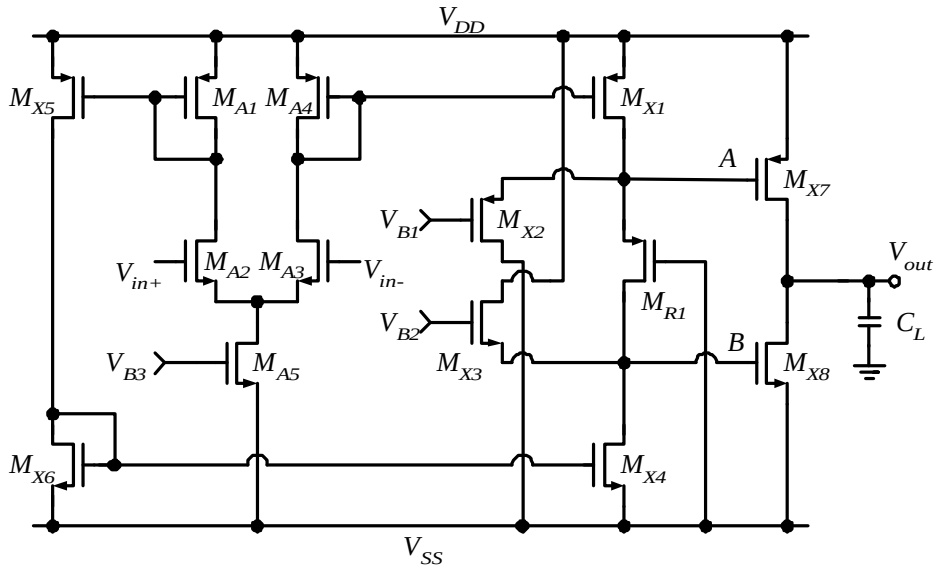
parameter	**Measured Results**
Supplies	±5V
Open-Loop Gain	93dB
Bandwidth	1.2MHz
Power Dissipation $\bar{x}$	12.7 mW
ó	1.76mW
Output Swing (R_L=200Ù)	±3.1V
PSRR+ at DC	93dB
1 kHz	91dB
10 kHz	76dB
100 kHz	60dB
PSRR- at DC	102dB
1 kHz	89dB
10 kHz	75dB
100 kHz	53dB
Slew Rate	1.5V/î s
Input Common Mode Range	+3.3V
	-5.5V
Die Area (5î m CMOS)	1000 $mils^2$
Harmonic Distortion (3 kHz) V_{in}=3 V_p R_L=200Ù	
HD2	-73dB
HD3	-78dB

Maximum Loads : 1000pF and 200Ùto ground.

Ref.: IEEE JSSC , vol. sc-20, pp.1200-1205, Dec. 1985.

3. Efficient Unity-gain CMOS buffer for driving large C_L.

High-drive OTA buffer



Bias stage

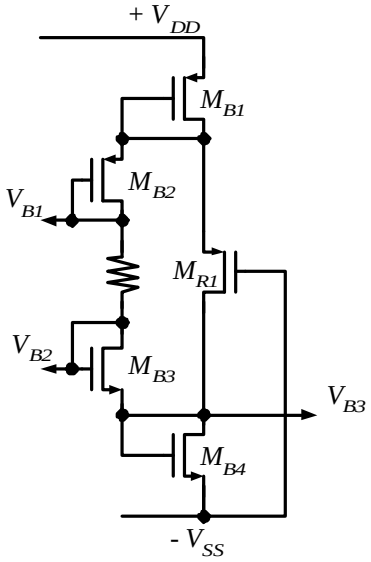


TABLE I

TRANSISTORS' DIMENSIONS

TRANSISTOR	W (μm)	L (μm)
MX1, MX5	225	3
MX2	75	3
MX3	30	3
MX4, MX6	90	3
MR1	6	21
MA1, MA4	45	3
MA2, MA3	450	3
MA5	36	3
MX7	600	3
MX8	240	3

* M_{R1} has a low W/L and is operated in the linear region

$\Rightarrow$ like a linear resistor.

* M_{X2} and M_{X3}

Quiescent operation:

✧ M_{X2} and M_{X3} are on.

$\Rightarrow$ Keep V_{GSMX7} and V_{GSMX8} low to reduce dc power.

$\Rightarrow$ Provide a low-impedance level at node A and B.

The low-order poles created by the Miller cap. of M_{X7} and M_{X8} can be avoid

* If $V_{in} << 0$

  M_{X3}-M_{X6} are turned off and M_{X1} and M_{X2} are on

  $\Rightarrow$ Node A has a high voltage $\Rightarrow$ M_{X7} off.

  $V_B = V_A$ because of $M_{R1} \Rightarrow M_{X8}$ on.

* In the bias circuit, $M_{R2} \leftrightarrow M_{R1}$, $M_{B1} \leftrightarrow M_{X1}$, $M_{B2} \leftrightarrow M_{X2}$, $M_{B3} \leftrightarrow M_{X3}$, $M_{B4} \leftrightarrow M_{X4}$.

  In the quiescent case, $V_{GSMX1} \approx V_{GSMX7}$ and $V_{GSMX4} \approx V_{GSMX8}$

  $\Rightarrow$ The current in M_{B1} and M_{B4} controls that in M_{X1} and M_{X4} and M_{X7} and M_{X8}.

* R_{BIAS} controls the current through M_{B2} and M_{B3}.

  $\Rightarrow$ i.e. the current through M_{X2} and M_{X3}.

Characteristics:

3 μm CMOS area: 100mils^2.

$C_L \geq 100$pF and $R_L \geq 10$ kΩ : stable.

C_L=5000pF $\Rightarrow$ f ≈ 100kHz.

TABLE II
BUFFER' S PERFORMANCE

PARAMETER	MEASURED VALUE	SPICE
Supply Voltage	± 2.5 V	± 2.5 V
Supply Current	285 μA	270 μA
Voffset	< 10 mV	5 mV
Voltage Gain	+ 1.00 V/V	+ 1.00 V/V
F_{3dB} (C_L=100pF)	6 MHz	8 MHz
Gain Peaking	0.4 dB	0
R_{oCL}	330 Ω	270 Ω
CMRR	80 dB	84 dB
Input CM Range	± 1.8 V	± 1.7 V
SR (CL=5nF)	± 0.9 V/μs	± 1.0 V/μs
$T_{settling}$ (to 1%)	3.9 μs	4 μs

Input Noise Density F = 1 kHz	270 $V/\sqrt{H_Z}$	NA
F = 50 kHz	70 $V/\sqrt{H_Z}$	NA

Ref.: IEEE JSSC, vol. sc-21, pp.464-469, June 1986.

§ 8-4 Advanced Design Techniques on Fully differential type CMOS OP AMPs

1. Low-noise chopper-stabilized OP AMP

Techniques for the reduction of 1/f noise:

1) Use large device geometries.

Possibly too large chip area.

2) Use buried channel devices

Not a standard technology.

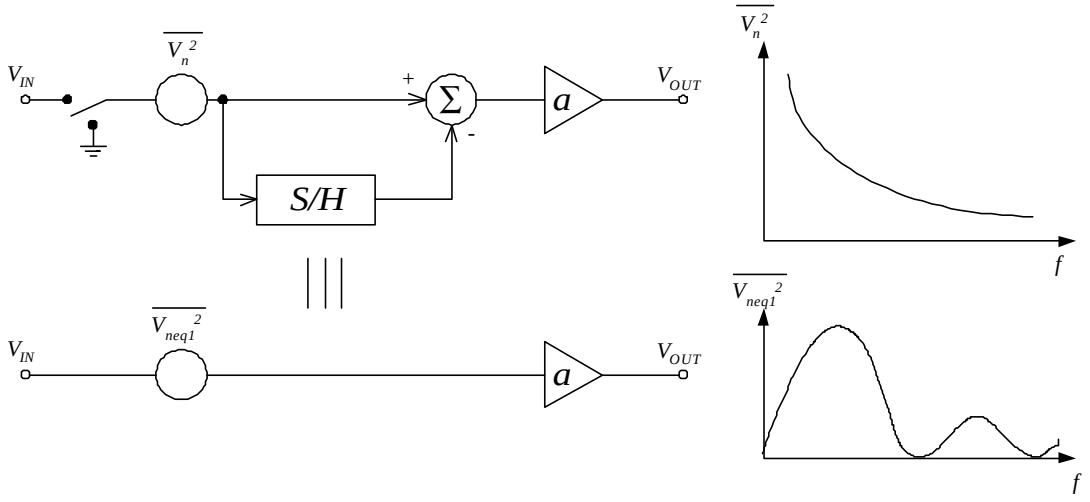
3) Transform the noise to a higher frequency range

So that it does not contarninate the signal.

a. The correlated double sampling (CDS) method

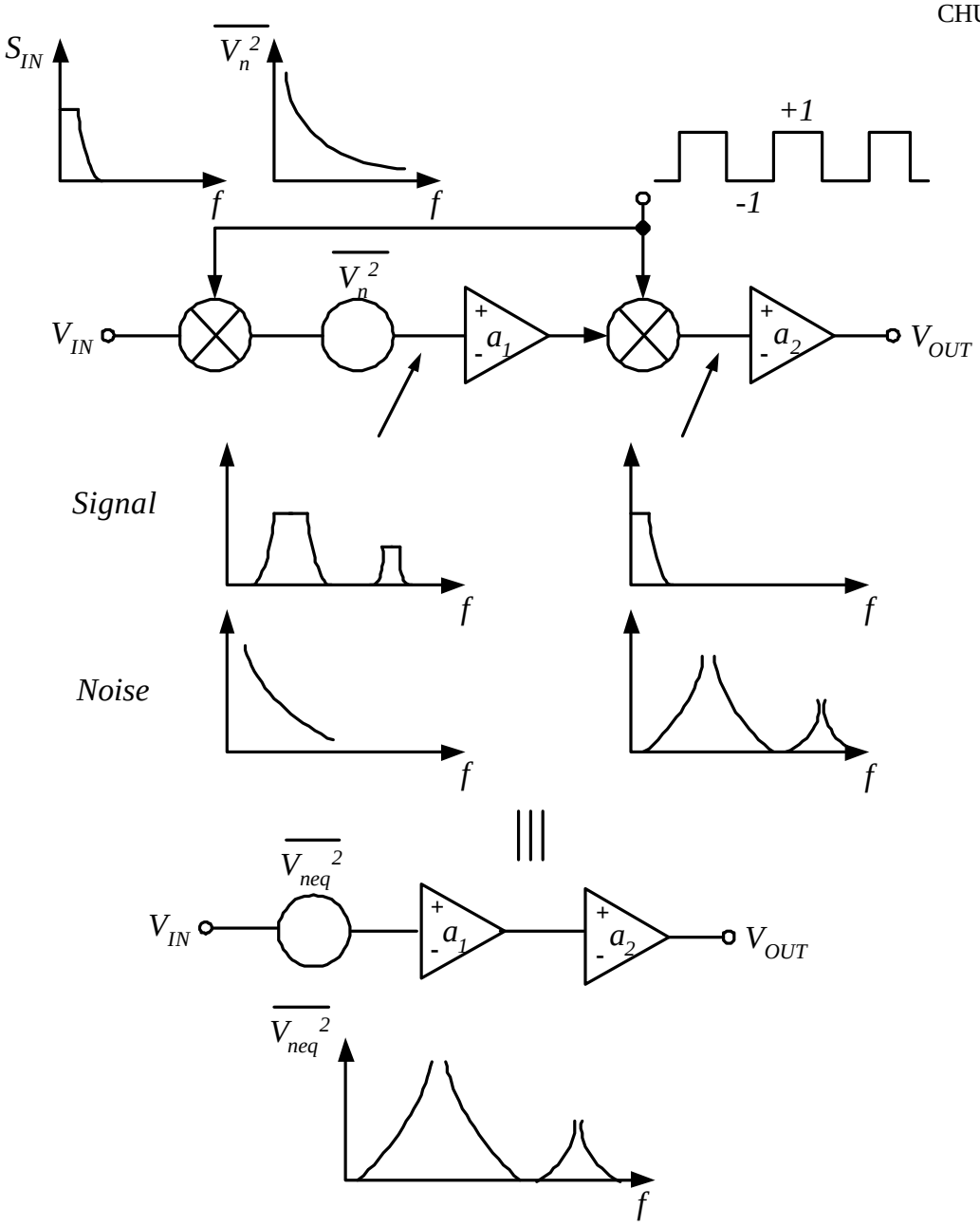
b. The chopper stabilization method

a. CDS method



⇒ Noise reduction

b. Chopper stabilization method



* If the chopper frequency is much higher than the signal bandwidth, the 1/f noise in the signal band will be greatly reduced.

Example: Fully differential class AB chopper stabilized OP AMP with DCMFB circuit.

Major advantage of fully differential OP AMPs:

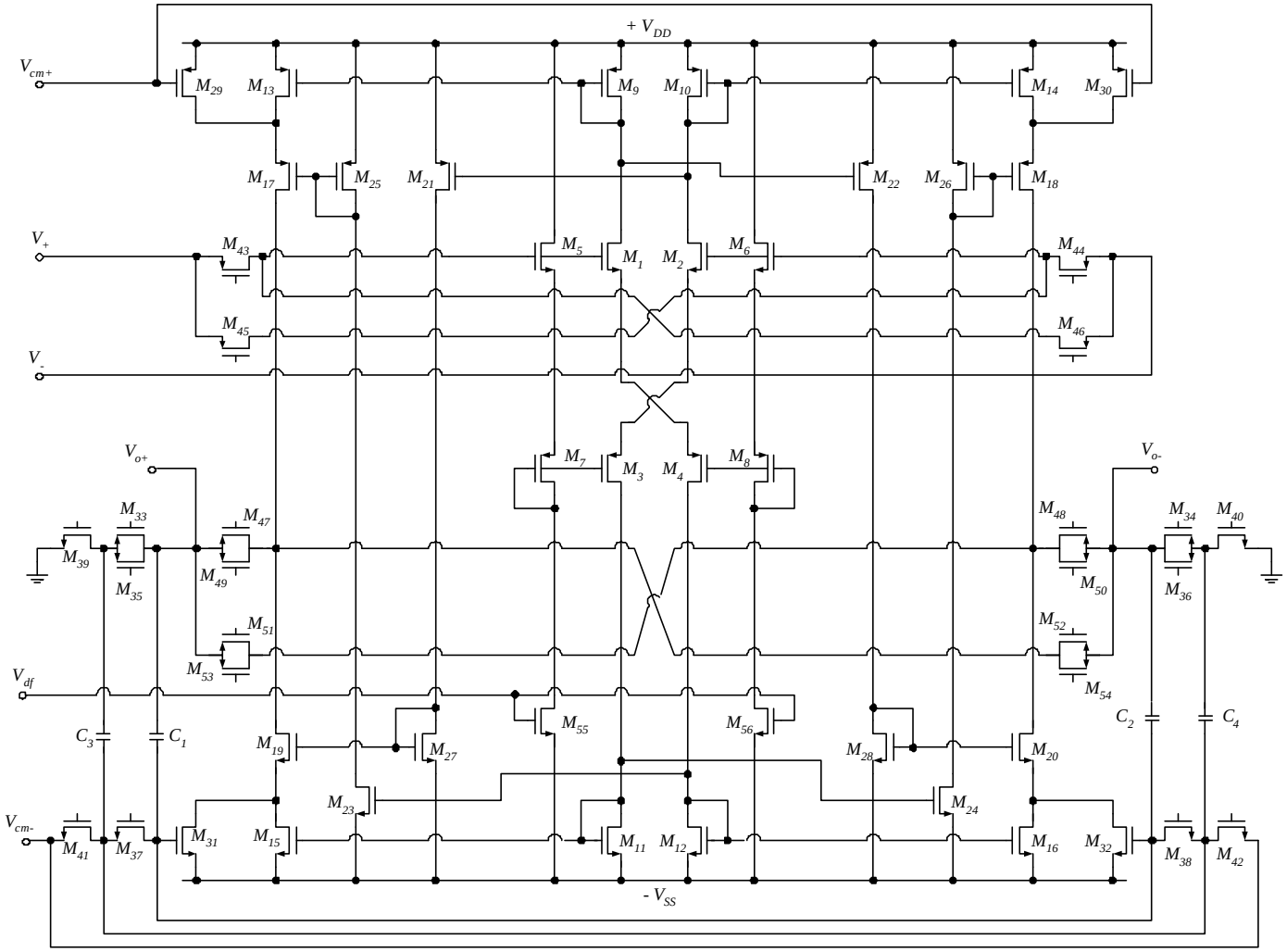
1. Improvement of PSRR
2. Improvement of dynamic range
3. double the output swing
4. Reduction on the sensitivity to clock and supply noise.

Disadvantage:

1. Larger area, mainly due to interconnection

2. Additional design complexity

3. Increase power dissipation.



M43-M46, M47-M54: the input chopper and the output chopper.

M29-M42, C1-C4 : DCMFB circuit

Device	W(um)	L(um)	Device	W(um)	L(um)
M1	25	3	M19	7	3.5
M2	25	3	M20	7	3.5
M3	25	3	M21	17.5	3.5
M4	25	3	M22	17.5	3.5
M5	25	3	M23	7	3.5
M6	25	3	M24	7	3.5

M7	25	3	M25	3.5	3.5
M8	25	3	M26	3.5	3.5

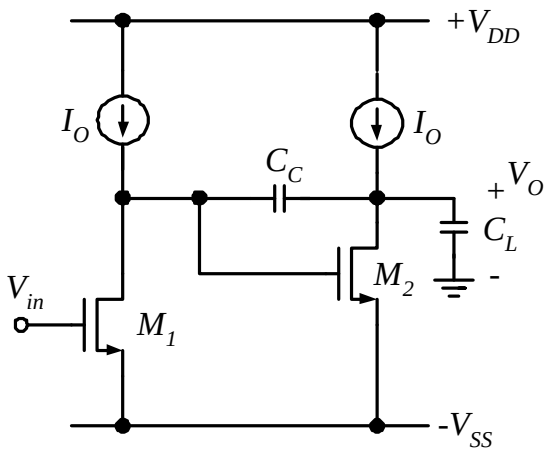
M9	10	3.5	M27	3	7
M10	10	3.5	M28	3	7
M11	4	3.5	M29	12	3.5
M12	4	3.5	M30	12	3.5
M13	17.5	3.5	M31	16	3.5
M14	17.5	3.5	M32	18	3.5
M15	7	3.5	M33-M34	7	3
M16	7	3.5	M55	7	3
M17	17.5	3.5	M56	7	3
M18	17.5	3.5			

Ref: IEEE JSSC vol.sc-21, pp.57-64 Feb.1986

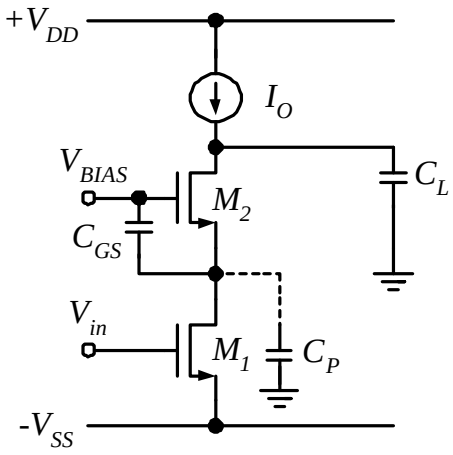
2. Fully differential folded cascode amplifier(National Semiconductor)

For internal OP AMPs, high output impedance is O.K.

$\Rightarrow$ simple 2-stage or single-stage OP AMP.



TWO-STAGE



SINGLE-STAGE

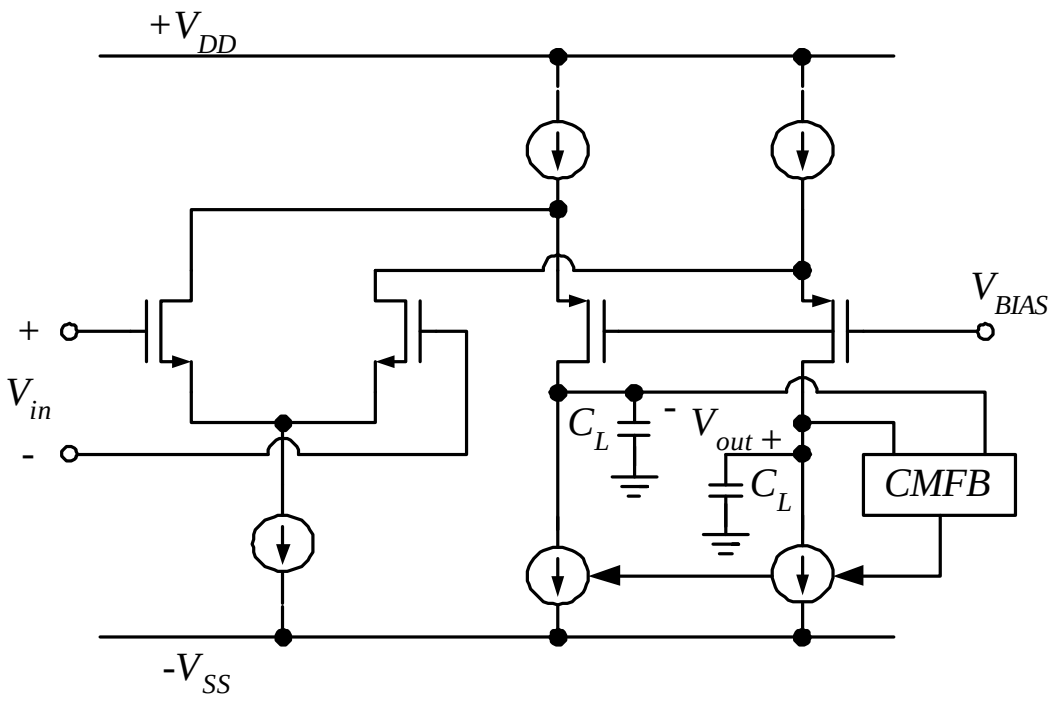
CASCODE

DOMINANT AND NONDOMINANT POLE LOCATIONS
FOR THE TWO-AND SINGLE-STAGE AMPLIFIERS

	Dominant pole location	Nondominant pole location
Two-stage amplifier	$\frac{1}{r_o C_c g_m r_o}$	$\frac{g_m}{C_L}$
One-stage amplifier	$\frac{1}{r_o C_L g_m r_o}$	$\frac{g_m}{C_p}$

In general, the higher the 2nd pole frequency, the faster the settling response.

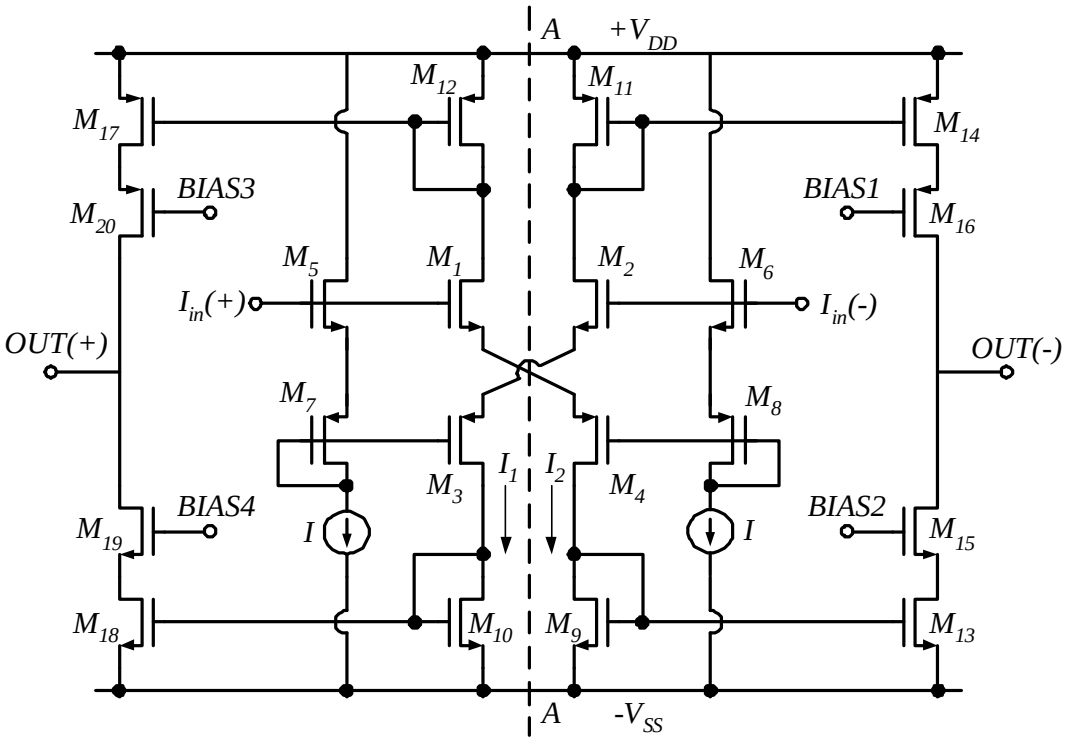
$\Rightarrow$ Single-stage cascode amp. has a faster settling behavior.

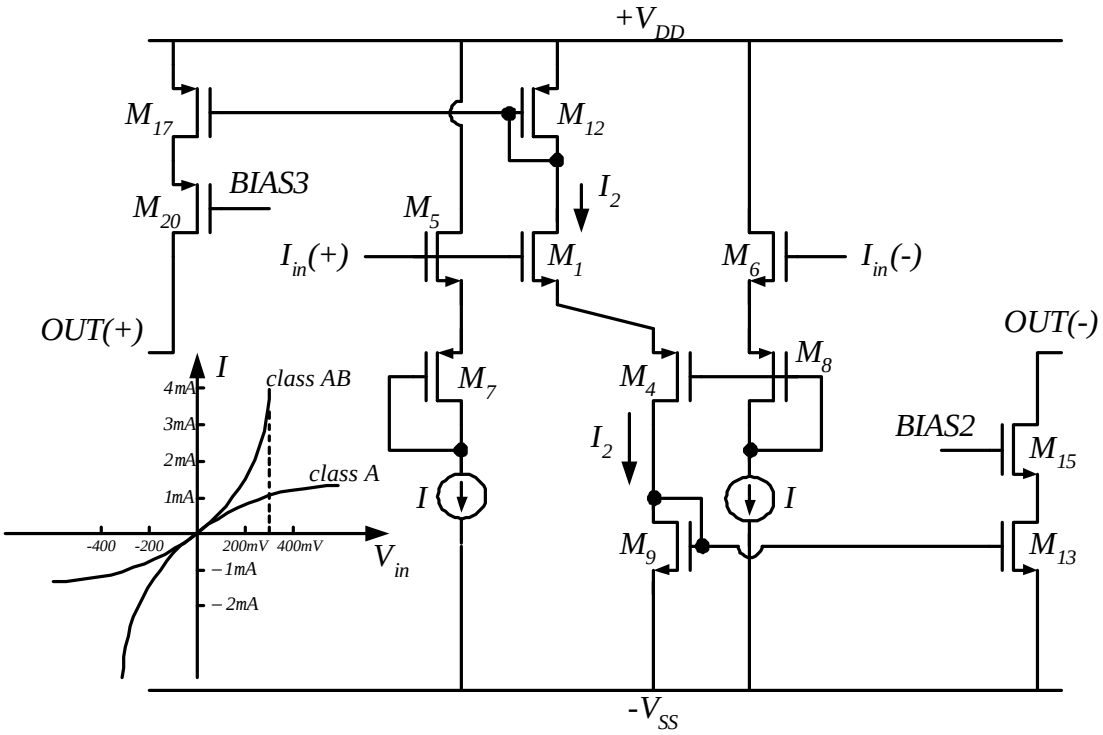


CMFB: Common-mode feedback circuitry

3. High-performance micropower fully differential OP AMP.

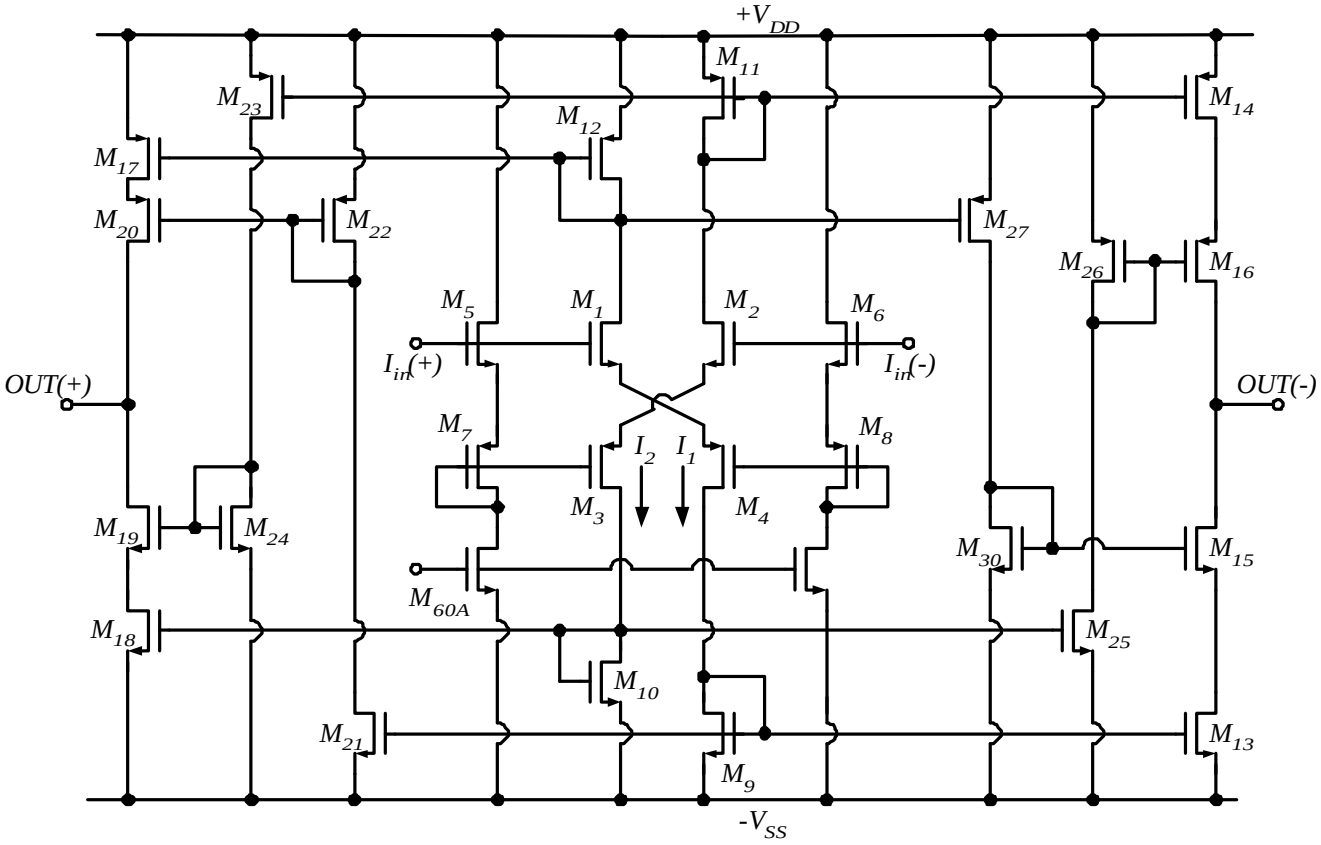
Simplified schematic of the class AB amplifier:



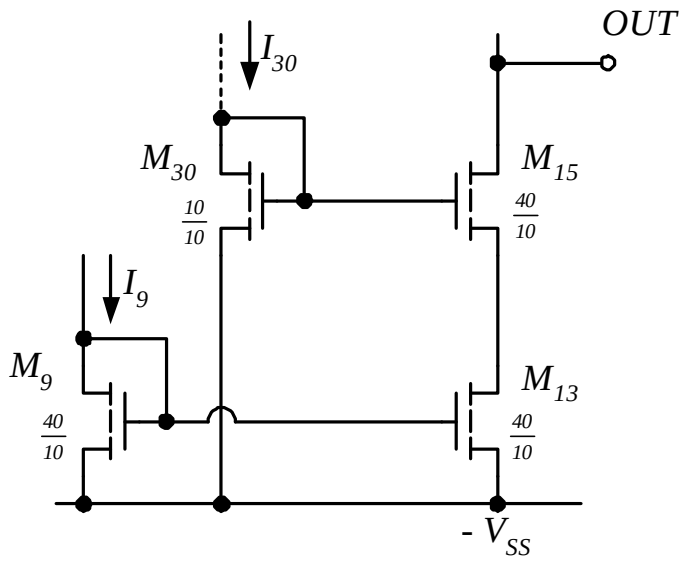


Active portion of the amplifier for a positive input signal.

Detailed schematic of the entire amplifier without CMFB:



* NMOS dynamically biased current mirror:



If $I_9 = I_{30}$, $V_{GS9} = V_{GS13} = V_{GS15}$

$$V_{DS13} = V_{GS30} - V_{GS9}$$

Set $V_{DG13} = -V_{TH} \Rightarrow V_{GS30} = 2V_{GS9} - V_{TH}$

Design $(\frac{W}{L})_{30}$, such that $V_{GS30} = 2V_{GS9} - V_{TH}$

$\Rightarrow$ M_{13} is always sat. at the edge of the linear region.

$\Rightarrow$ Output swing$\uparrow$

* Dynamic CMFB is used.

AMPLIFIER DEVICE SIZES

DEVICE	Z(μ m)	L(μ m)
M1	180	6
M2	180	6
M3	140	6
M4	140	6
M5	150	6
M6	150	6
M7	200	6
M8	200	6
M9	22	10
M10	22	10

M11	29	7
M12	29	7
M13	22	10
M14	29	7
M15	22	6
M16	29	6
M17	29	7
M18	22	10
M19	22	6
M20	29	6
M21	20	9
M22	6	12
M23	28	6
M24	6	14
M25	20	9
M26	6	12
M27	28	6
M30	6	14

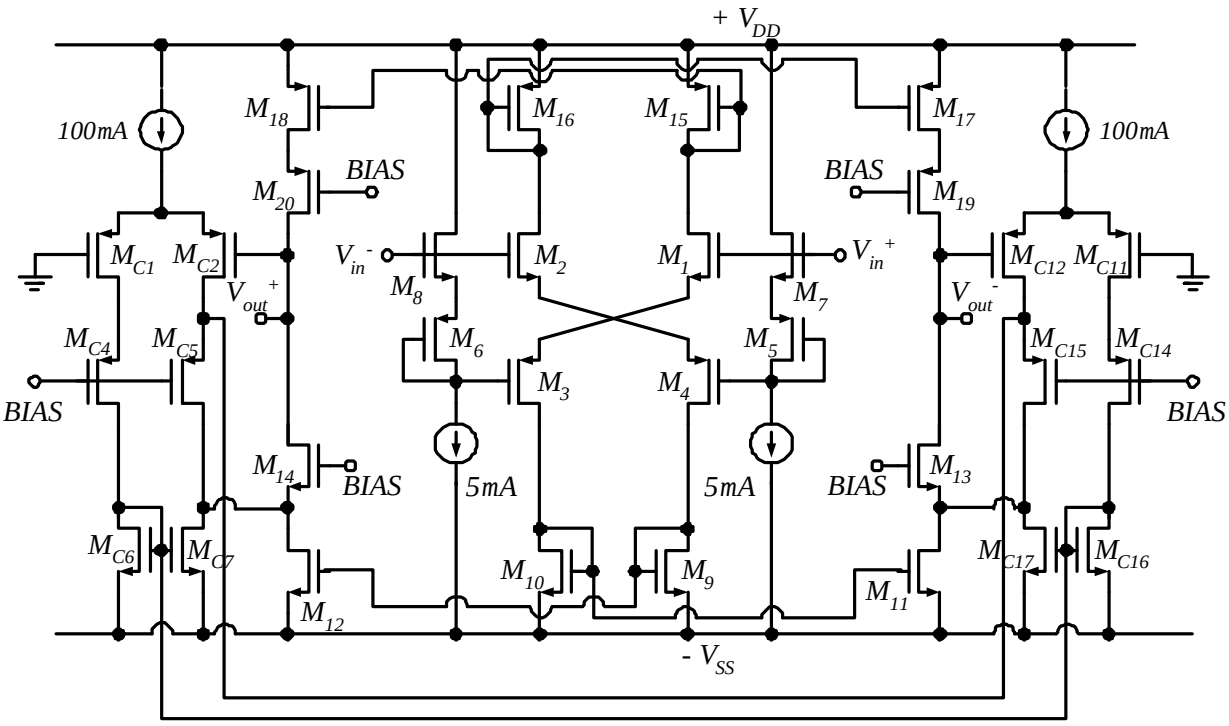
AMPLIFIER SPECIFICATIONS

CORE AMPLIFIER SPECIFICATIONS (0-5 Volts Supply) 100 μW Quiescent Power Dissipation	
DIFFERENTIAL GAIN	>10.000★
UNITY GAIN FREQUENCY	2 MHz★
NOISE	140 nV/$\sqrt{Hz}$ 1KHz 50 nV/$\sqrt{Hz}$ white
OUTPUT SWING	0.5 Volts from Supply★
AREA	300 $mils^2$

★inferred from filter measurement

Ref: IEEE JSSC, vol. SC-20, pp.1122-1132, Dec. 1985

4. Fully differential class AB OP AMP with CMFB circuit



Characteristics:

Technology	: 5um, P-well CMOS, double-poly cap.		
Open loop gian	: 1180	unity-gain freq	: 10Mhez
CMRR	: 61db	power consumption	: 2.3mw
Area	: 290 mils^2	power supply	: ± 5*V*

Ref: IEEE JSSC ,vol.sc-20 , pp.1103-1112 , Ddec,1985

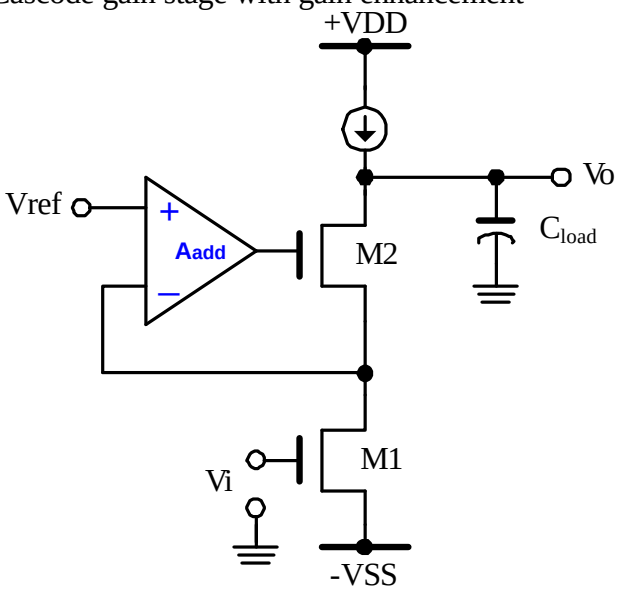
§ 8-5 Recent Design Examples of CMOS OP AMPs

§ 8-5.1 Fast-settling CMOS OP AMP for SC Circuit with 90-dB DC Gain

Reference : IEEE JSSC, vol.25, no.6, pp.1379-1384, Dec 1990.

1.Gain boosting

1) Cascode gain stage with gain enhancement

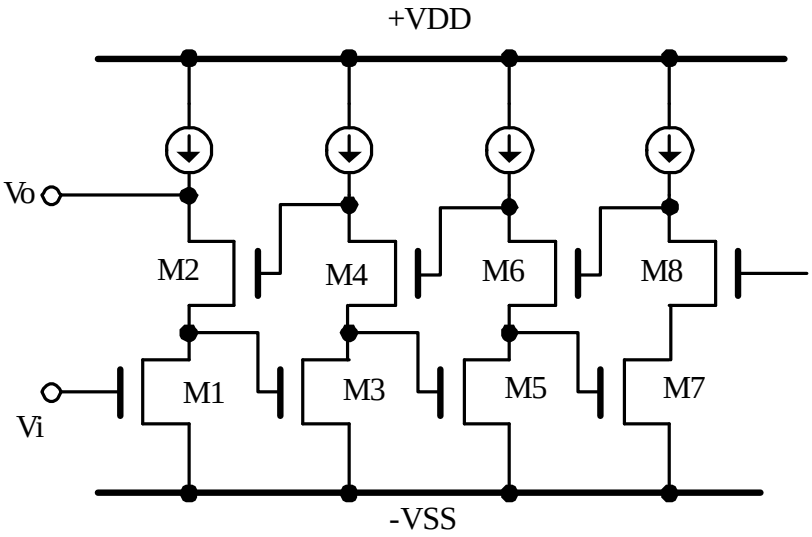


$$R_{out} = [g_{m2} r_{o2} (A_{add} + 1) + 1] r_{o1} + r_{o2}$$

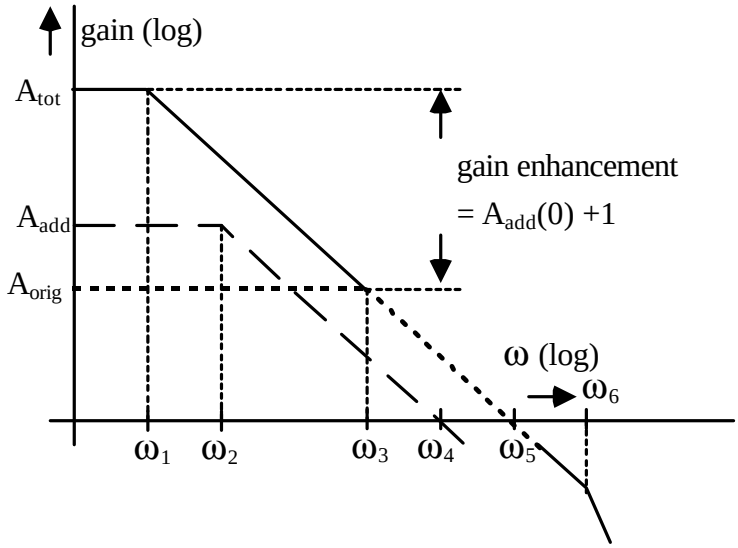
$$A_{tot} = g_{m1} r_{o1} [g_{m2} r_{o2} (A_{add} + 1) + 1]$$

$$A_{orig} = g_{m1} g_{m2} r_{o1} r_{o2}$$

2) Repetitive implementation of gain enhancement



2.High-frequency behavior



w_3 : Upper 3-dB frequency of A_{orig}

w_5 : Unity-gain frequency of A_{tot}

w_2 : Upper 3-dB frequency of A_{add}

w_4 : Unity-gain frequency of A_{add}

w_1 : Upper 3-dB frequency of A_{tot}

w_5 : Unity-gain frequency of A_{orig}

We want $\omega_5\big|_{Aorig} = \omega_5\big|_{Atot}$

$\omega_2 > \omega_1$ => The bandwidth is determined by ω_1, i.e. R_{out} and C_{load}.

=> $\omega_4 > \omega_3$

But $\omega_4 < \omega_5$ for easy design of A_{add}.

A_{add} and M2 forms a close loop with the dominant pole of ω_2 and the second pole at the source of M2, i.e. ω_6

The stability consideration requires $\omega_4 < \omega_6$

=>The safe range of ω_4 is

$$\omega_3 < \omega_4 < \omega_6$$

* The repetitive usage of the gain-enhancement techniques yields a decoupling of the op-amp gain and unity-gain frequency fu. That is:gain↑ without fu↓.

3.Settling behavior

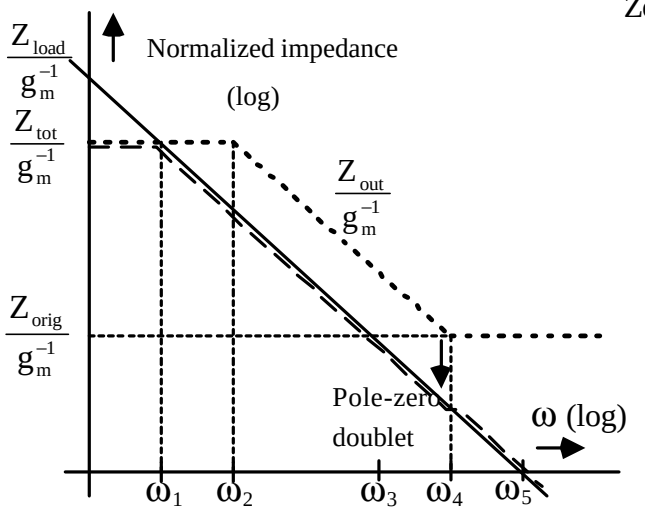
1. Total output impedance Ztot

Ztot= $Z_{load} // Z_{out}$

Z_{load}: impedance of C_{load}

Zout: output impedance of the amplifier

Zout ≅ Zorig (Add+1)



ω_2 : Upper-3dB freq. Of A_{add}

➔the same for Z_{out}

ω_4 : Unity-gain freq. Of A_{add}

For $\omega > \omega_4$, $A_{add} < 1$➔ $Z_{out} \rightarrow Z_{orig}$

➔A zero is formed at ω_4 for Z_{out}

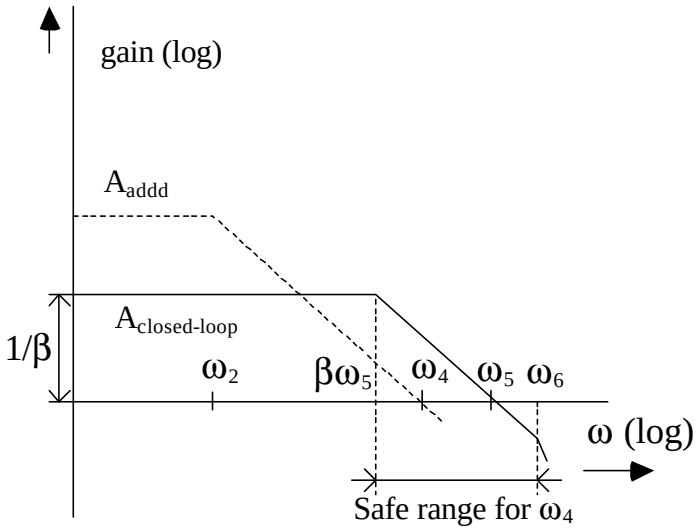
$Z_{total} = Z_{load} \parallel Z_{out}$ ➔A pole-zero doublet is formed around ω_4

➔The same doublet of A_{total}

3. Design technique for fast settling

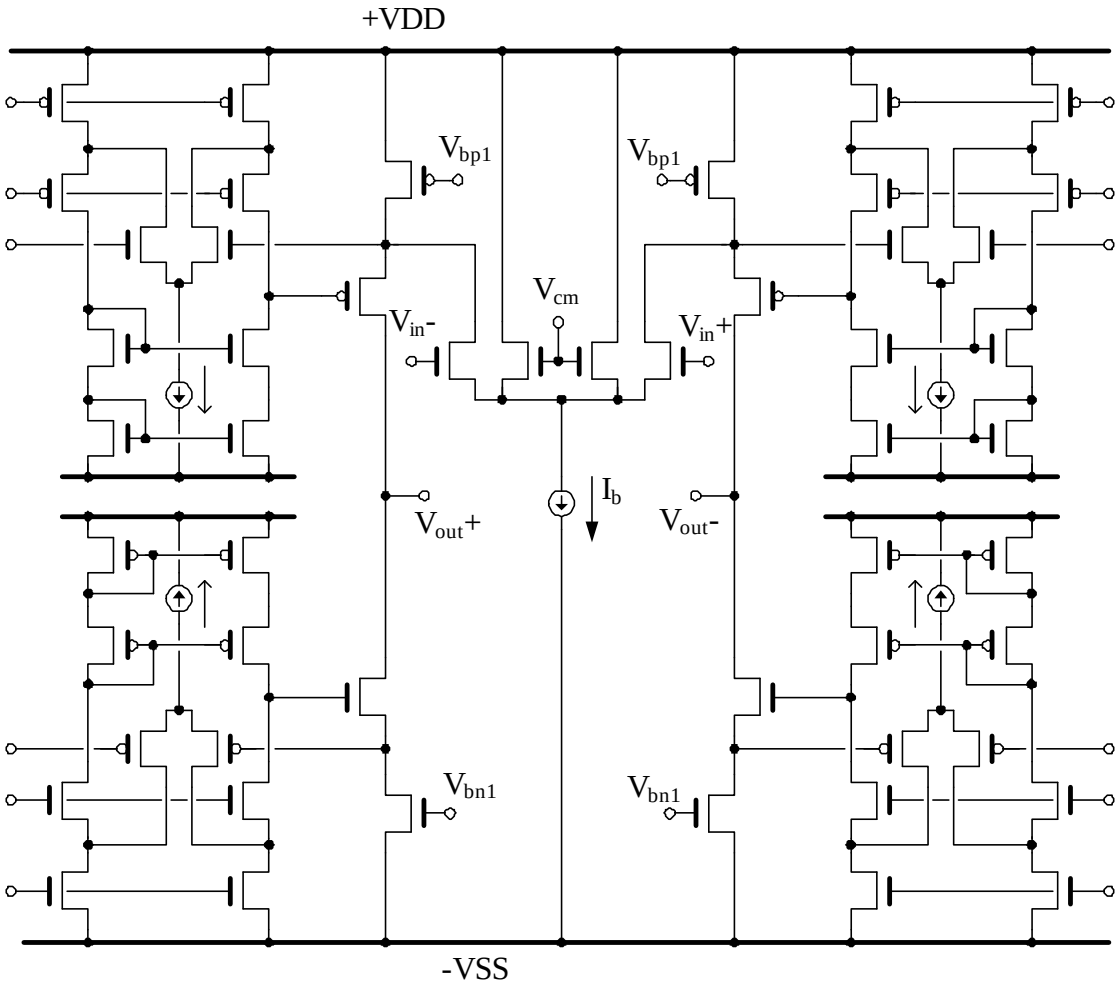
The time constant of the doublet, $\frac{1}{\omega_{PZ}}$, must be smaller than the main close-loop time constant, $\frac{1}{\beta\omega_{unity}}$. where β is the feedback factor.

The safe range for the ω_4.



$$\beta\omega_5 < \underset{\text{doublet}}{\omega_4} < \omega_6$$

4. CMOS OP AMP circuit



MAIN CHARACTERISTICS OF THE OP AMP

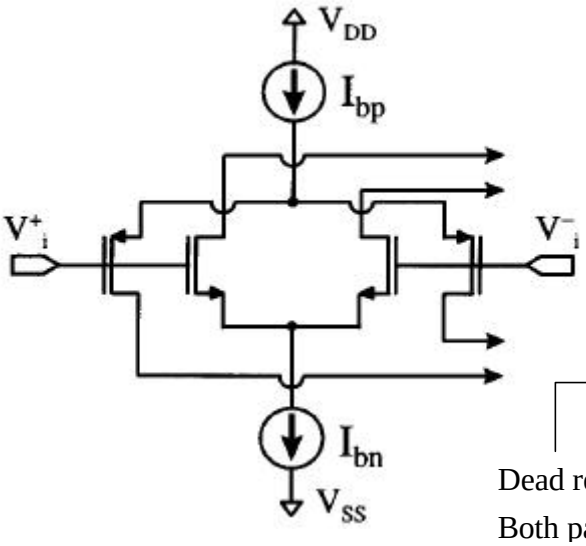
Gain enh.	on	Off
DC-gain	90dB	46dB
Unity-gain freq.	116MHz	120MHz
Load cap.	16pF	16pF
Phase margin	64deg.	63deg
Power cons.	52mW	45mW
Output-swing	4.2V	4.2V
Supply voltage	5.0V	5.0V
Settling time 0.1% , $\Delta V_o = 1V$	61.5ns	-

§ 8-5.2 1V Rail-to-Rail CMOS OP AMPs

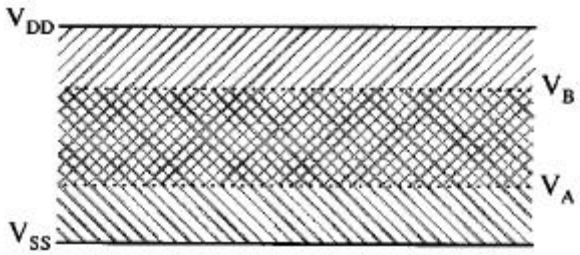
Ref.: IEEE JSSC vol.35, no.1, pp.33-44 Jan. 2000

1. Typical input stage for rail-to-rail amplifiers

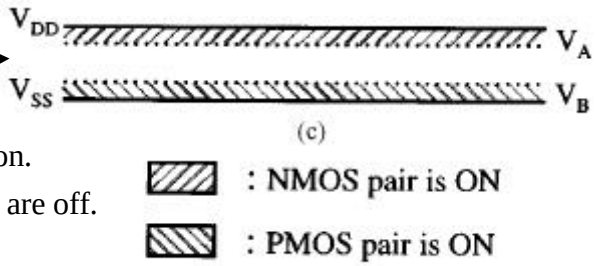
* Parallel-connected complementary differential pairs.



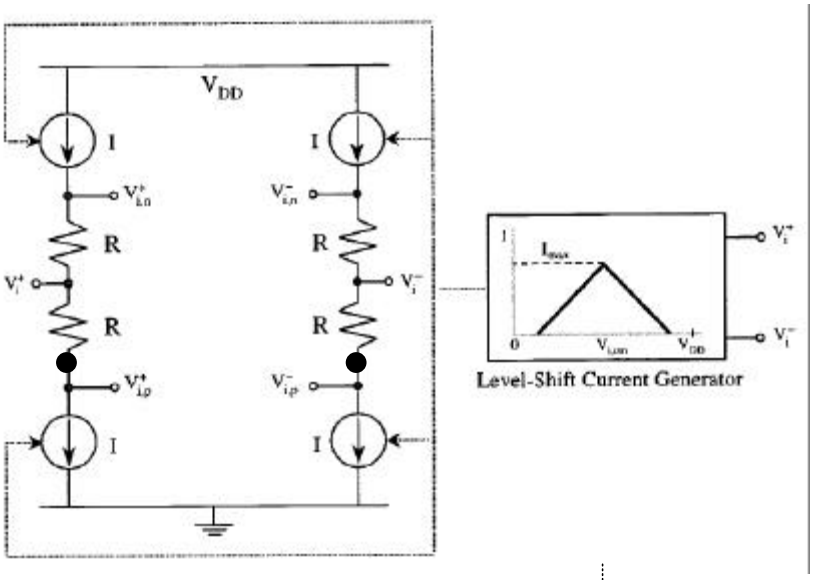
* Operating zones for low VDD/VSS



* Operating zones for extremely low VDD/VSS



2. Dynamic level-shifting current generator



Vi,n,cm=Vi,cm+IR

Vi,p,cm=Vi,cmi-IR

* The input resistance over the entire voltage range is infinite and no loading effect or input current over the previous stage.

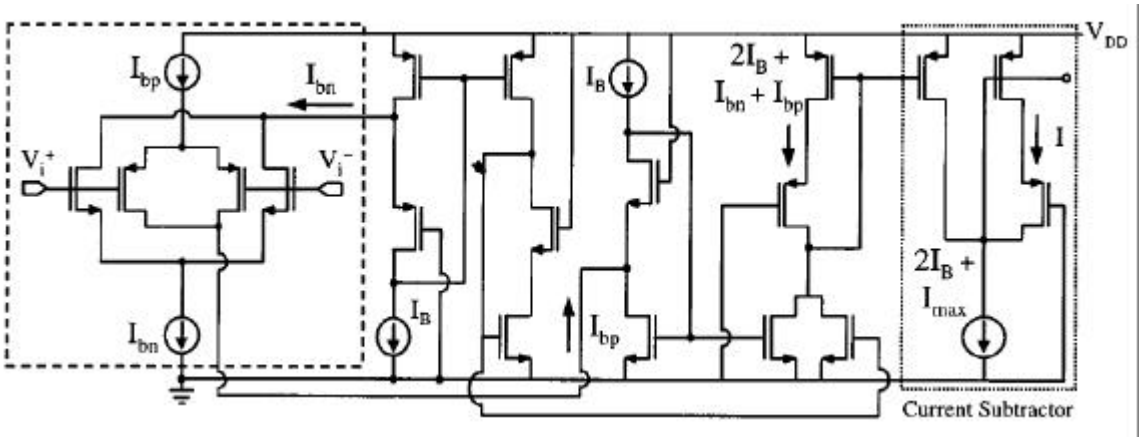
Usually mismatches cause negligible input current.

* The symmetrical topology ensures very high CMRR

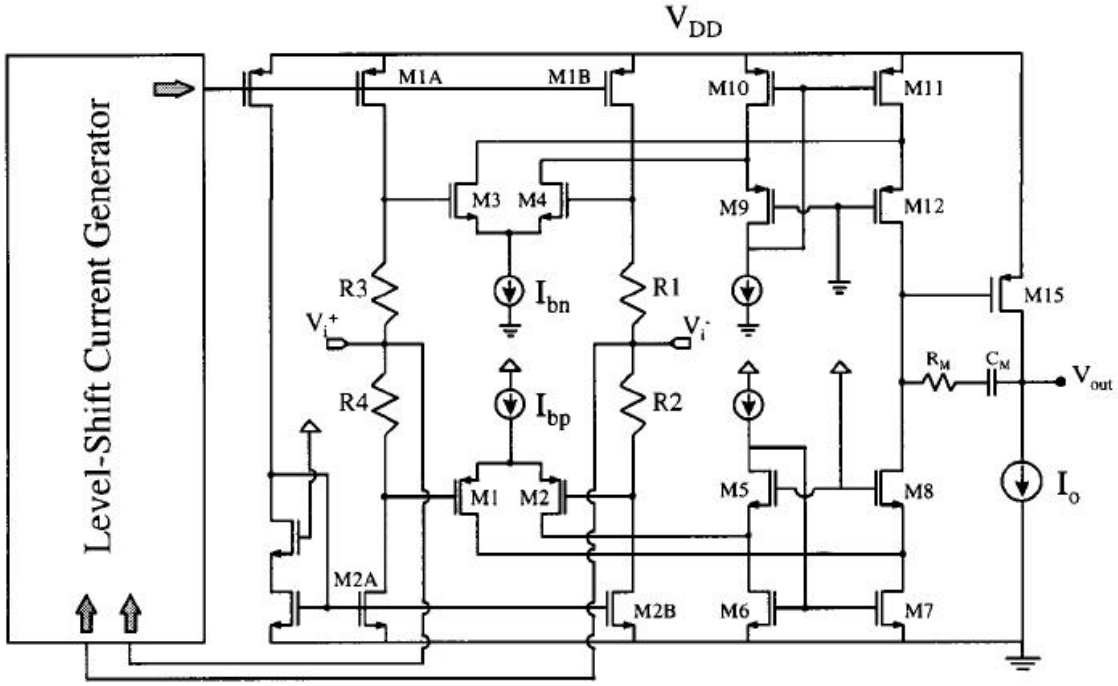
$$CMRR = \frac{1}{RG_m}\left(\frac{\Delta R}{R} + \frac{\Delta G_m}{G_m}\right)^{-1}$$

where $G_m = \Delta I / \Delta V_{i,cm}$

Circuit implementation



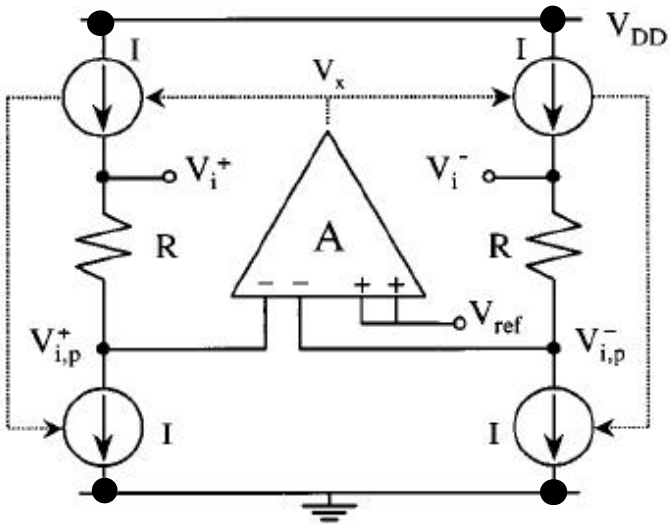
3. Rail-to-rail very LV CMOS OP AMP with input dynamic level-shifting circuit



MAIN TRANSISTOR ASPECT RATIOS (IN μm) AND ELEMENT VALUES OF THE AMPLIFIER BASED ON COMPLEMENTARY PAIRS

M1A,M1B	400/5	M15	700/2
M2A,M2B	200/5	R1-R4	30 *K*Ω
M1,M2	400/2	R_M	5 *K*Ω
M3,M4	200/2	C_M	10pF
M5-M8	400/5	$I_{bn} = I_{bp}$	10μA
M9-M12	500/5	I_o	40μA

4. Input CM adapter



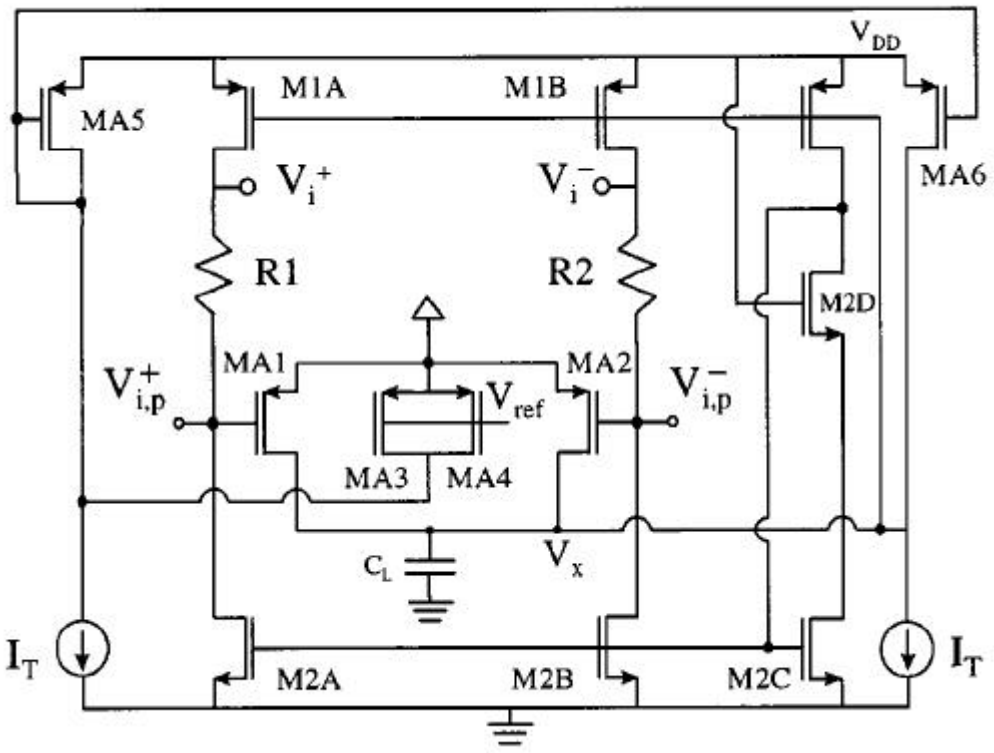
$$Vx = A[2V_{ref} - (V_{i,p}^{+} + V_{i,p}^{-})]$$
$$= 2A(V_{ref} - V_{i,p,cm})$$

$$I = G_m V_x$$
$$\Rightarrow V_{i,p,cm} \cong V_{ref} + \frac{V_{i,cm}}{2RG_mA}$$

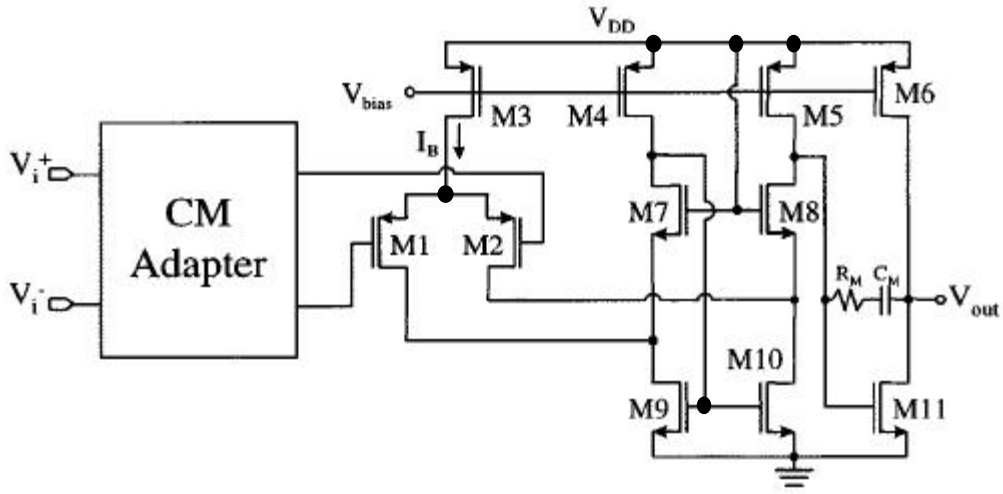
$$V_{i,p,dm} = V_{i,dm}$$

*$V_{i,cm}$ is degraded by A and $V_{i,p,cm} \cong V_{ref}$

Circuit implementation:



5. Very LV CMOS OP AMP with a single differential pair and the input CM adapter.



Main transistor ratios(in μm) and element values of the amplifier based on a single input pair

M1A M1B	1000/6	M6	1600/2
M2A M2B	600/4	M7-M10	300/4
MA1-MA4	50/2	M11	700/2
MA5-MA6	300/4	R1-R2	15KΩ
M2D	150/2	R_M	5KΩ
M1,M2	200/2	C_M	5pF
M3-M5	400/2	Is=Ir/2	10μA

6.Measured results

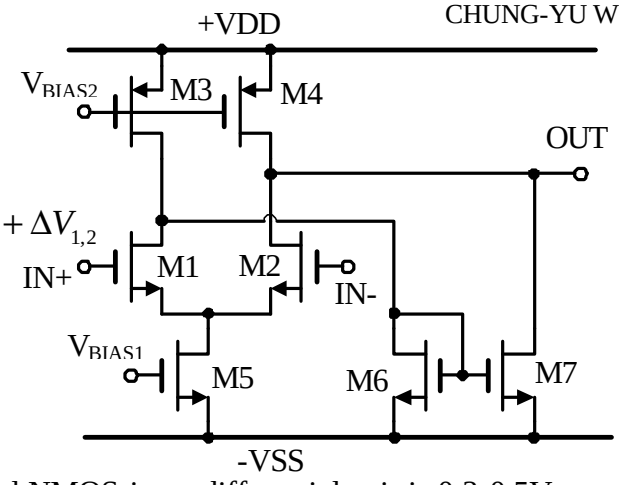
Experimental performance of amplifiers(Vsupply=1V,technology:1.2μm CMOS, C_L=15pF)

Parameter	Dynamic-shifting amp	CM adapater amp
Active die area	0.81mm^2	0.26 mm^2
Ido(supply current)	410uA	208uA
DC gain	87dB	70.5dB
unity-gain frequency	1.9Mhz	2.1Mhz
Phase margin	61°	73°
SR+ SR-	0.8V/us 1V/us	0.9V/us 1.7V/us
THD(0.5Vpp@1kHz) THD(0.5Vpp@40kHz	-54dB -32dB	-77dB -57dB
Vni(@1KHz) Vni(@10KHz) Vni(@1MHz)	267nV/$\sqrt{Hz}$ 91nV/$\sqrt{Hz}$ 74nV/$\sqrt{Hz}$	359nV/$\sqrt{Hz}$ 171nV/$\sqrt{Hz}$ 82nV/$\sqrt{Hz}$
CMRR	62dB	58dB
PSRR+ PSRR-	-54.4dB -52.1dB	-56.7dB -51.5dB

§8-5.3 1.5V High Drive Capability CMOS OP AMP

Ref.: IEEE JSSC vol.34, no.2, pp. 248-252, Feb. 1999

1. Folded-mirror differential input stage



$$V_{CM} \le V_{GS\,6,7} + V_{THn} = 2V_{THn} + \Delta V_{6,7}$$

$$V_{CM} \ge V_{DSsat\,5} + V_{GS\,1,2} = 2V_{THn} + \Delta V_5 + \Delta V_{1,2}$$

$$CMR = V_{THn} - \Delta V_5$$

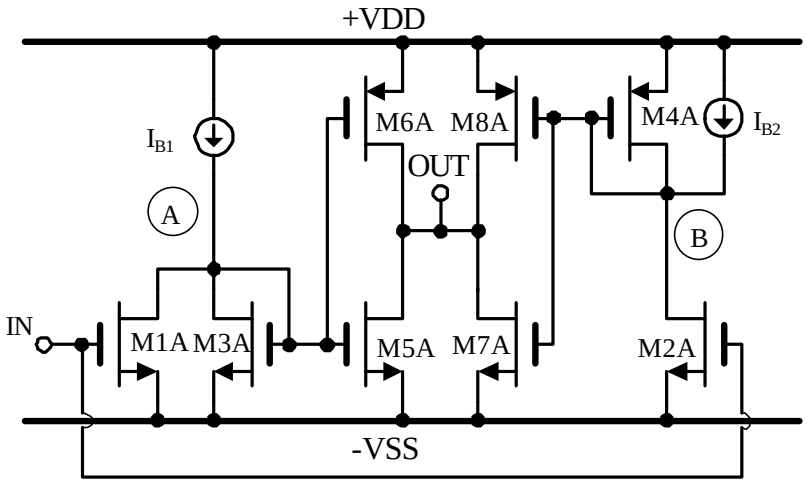
ΔV : overdrive voltage.

CMR is independent of supply voltage.

For V_{DD}=1.5V , CMR=0.6 ~ 0.7V

CMR of the conventional NMOS-input differential pair is 0.3-0.5V

2. Output Stage



Input section : M1A-M4A , I_{B1} , I_{B2}

Output section: M5A-M6A and M7A-M8A

M5A, M8A sat

M6A, M7A off.

For low input levels , M6A and M7A off ➔ Class A operation.

For large positive input signals,

$I_{D1A}=I_{B1}$ ➔ M3A and M5A OFF

➔ $V_A \rightarrow -V_{SS}$

➔ M_{6A} is turned on to supply most of the output current.

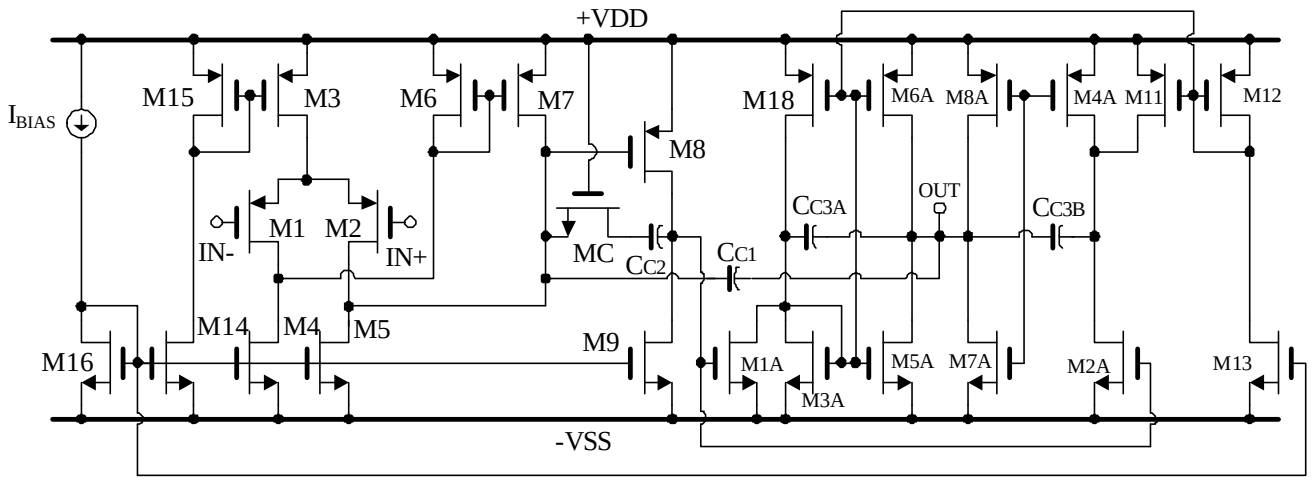
But M7A remains cutoff.

The current of M8A is increased.

For large negative input signals, M_{7A} supplies most of the output current.

$(W/L)_{5A,8A} << (W/L)_{6A,7A}$ for low dc power dissipation and high drive.

3. Overall LV CMOS OP AMP.



Dominant pole : $Wp1 \approx \frac{1}{r_{o5,7}\{(g_{m8}r_{o8,9})2[g_{m5A,8A}(r_{o5A} \| r_{o8A})]\}Cc}$

Gain-bandwidth product: $W_{GBW} \approx \frac{g_{m1,2}}{C_{c1}}$

Hybrid nested Miller compensation: C_{C1}, C_{C2}, $C_{C3A,B}$

The inner amplifier M_8,M_9,M_{1A}~M_{8A} contributes the nondominant poles.

* The two-stage OP AMP M_1~M_9 has a gain-bandwidth product of $\frac{g_{m1,2}}{C_{c2}}$

and the gain of $\frac{g_{m1,2}}{sC_{c2}}$ at high frequency. The gain of M_1-M_7 at high frequency is

$\frac{g_{m1,2}}{sC_{c1}}$. Thus the gain of the gain stage M8 and M9 is approximately equal to $\frac{C_{C1}}{C_{C2}}$.

* The open-loop gain of the inner amplifier is

$$A_{in} \cong -\left(\frac{C_{C1}}{C_{C2}}\right)\left(\frac{g_{m1A,2A}}{g_{m3A,4A}}\right)2g_{m5A,8A}\left(r_{o5A} \| r_{o8A}\right)$$

Dominant pole : $w_{P1in} \cong \frac{g_{m3A,4A}}{g_{m5A,8A}(r_{o5A} \| r_{o8A})C_{C3A,B}}$

Second pole : $w_{P2in} \cong \frac{2g_{m5A,8A}}{C_L}$

Gain-bandwidth product : $\omega_{GBWin} \cong 2\frac{C_{C1}}{C_{C2}}\frac{g_{m1A,2A}}{C_{C3A,B}}$
or the second pole of the
whole amplifier

Design consideration :

To obtain a maximally flat Butterworth response without gain peaking, we have the unity-gain frequency equal to one half of the second-pole frequency.

$$\omega_{GBWin} = \omega_{uin} = \frac{1}{2}\omega_{P2in}$$

$$\omega_{GBW} = \omega_{u} = \frac{1}{2}\omega_{uin} = \frac{1}{2}\omega_{GBWin}$$

Reference : IEEE JSSC, vol.27, pp.1709-1716, Dec. 1992.

Setting $2C_{C3A,B} = C_{C2}$, we have

$$C_{C1} = 2\frac{g_{m1,2}}{g_{m5A,8A}}C_L$$

$$C_{C2} = 2C_{C3A,B} = \sqrt{2g_{m1,2}g_{m1A,2A}} \cdot \frac{C_L}{g_{m5A,8A}}$$

Component values :

M1,M2,M3,M9,M1A,M2A,M10	60/2
M4,M5,M11,M12,M13	20/2
M6,M7	15/2
M8	90/2
M3A	5/1.2
M4A	15/1.2
M5A	30/1.2
M7A	120/1.2
M6A	360/1.2
M8A	90/1.2
M14,M16	10/1.2
M15,MC	30/2
C_{C1}	4pF
C_{C2}	6pF
C_{C3A},C_{C3B}	2pF
I_{BIAS}	5uA
V_{TH}	0.8V

Experimental results:

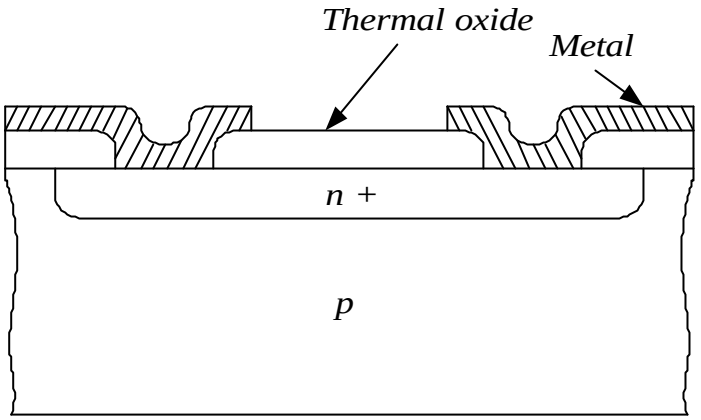
MEASURED MAIN PERFORMANCE

Open-Loop Gain	68dB
GBW	1MHz
Phase Margin	65^o
Gain Margin	16dB
Settling Time(0.1%), $\Delta V = 200mV$	400ns
Slew Rate	1 V/ μs
THD@1kHz $V_{out} = 0.5V$ RL=500Ω Closed-Loop Gain=20dB	-57dB
PSRR+@1kHz	75dB
PSRR- @1kHz	75dB
CMRR @1kHz	95dB
Offset	< 8mv
Power Dissipation	280 μW
Die Size	$0.08\,mm^2$
Technology	1.2 μm CMOS
Loading	50pF ‖ 500Ω

Chapter 9 Passive Components and Switches

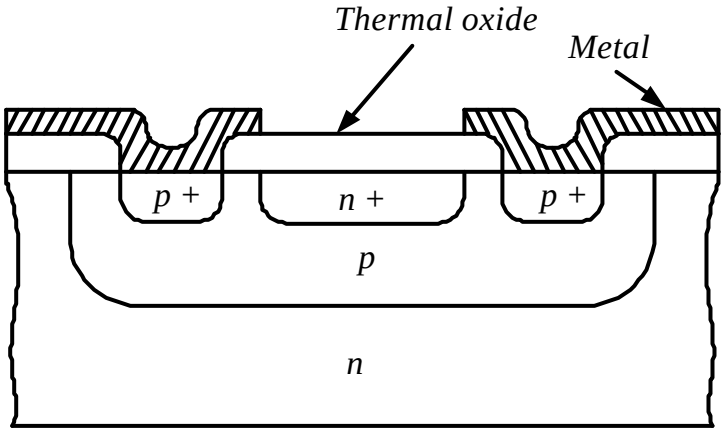
§ 9-1 Resistors

1. Source/Drain diffused resistor



* Compatible with NMOS and CMOS. metal-gate and Si-gate techniologies.
* $R_{\square}$ = *20 ~ 100W* /□ (*100KW* max)
* Temperature Coefficient of Resistance (TCR) = 500~1500 ppm/^{o}C.
  Voltage Coefficient of Resistance (VCR)=100~500ppm/^{o}C
  Tolerance= ± 20% (Absolute)
* High parasitic capacitance (n^{+}-p junction cap.)
  Piezoresistance error. (Because of shallow junction)

2. P-well (N-well) diffused resistor (Well or tub resistor)

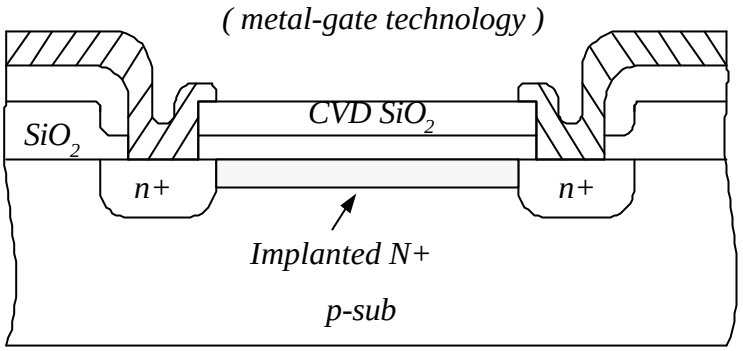


* Compatible with CMOS metal-gate or Si-gate technology.
* $R_{\square}$= *1KW ~ 5KW* /□
  Large VCR

Tolarance= ± 40% (absolute)

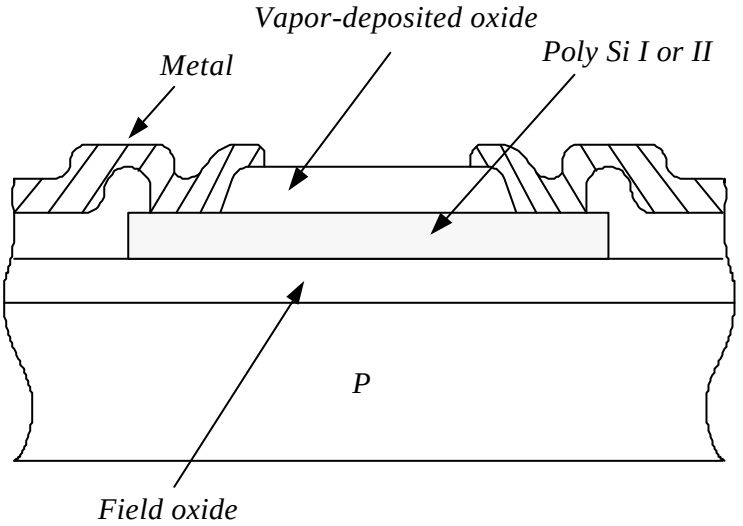
* Large depth and lateral spreading ⇒ narrow resistors are impossible.

3. Implanted resistor



* Compatible with NMOS and CMOS, metal-gate and Si-gate technologies.
* Need an additional masking step.
* $R_{\square} > 500\Omega \sim 1000\Omega / \square$; can be accurately controlled.
* Higher VCR ; smaller tolerance.
* Difficult to eliminate the piezoresistance effect.
* The resistor implant can be combined with the depletion implant.

4. Poly-Si resistor



* Realizable by NMOS and CMOS Si-gate technologies.
* $R_{\square} = 30\Omega \sim 200\Omega / \square$ (doped with the source/drain diffusion)
* TCR ≅ 500~1500 ppm/^{o}C ; Tolerance= ± 40%

* Can be trimmed by laser or poly fuse.
* Fully isolated with smaller parasitic capacitance.

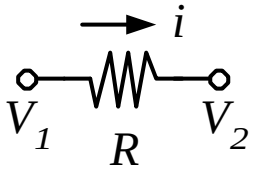
✧ Version I :Poly-I resistor

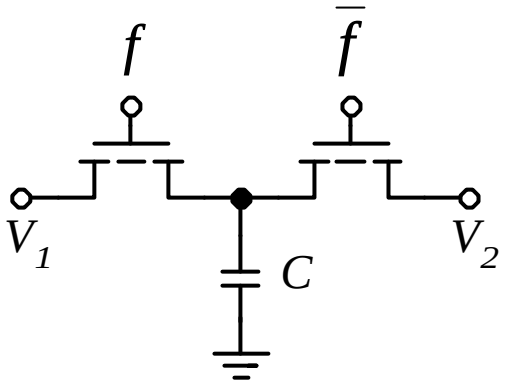
✧ Version II:Poly-II resistor

✧✧ Version III :Poly-I and Poly-II distributed RC structure (please see the structure shown in poly to poly capacitor)

5. Switched-capacitor simulated resistor

* Realizable by NMOS and CMOS , metal-gate and Sigate technologies.
* High frequency operation?





$i = \frac{V_1 - V_2}{R}$

f_C is the clock frequency of f or $\bar{f}$

$i = \frac{C(V_1 - V_2)}{T}$, $R = \frac{T}{C} = \frac{1}{f_C \cdot C}$

6. Thin-film resistor

* Realizable by NMOS and CMOS, metal-gate and Si-gate technologies.
* Need additional process steps.
* Si-Chromium resistor or Mo resistor.
* Laser trimming is possible.
* Non-conventional material may be involved.

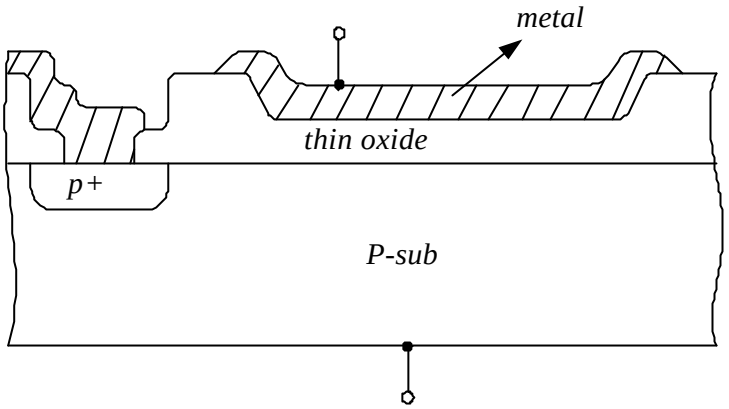
§ 9-2 Capacitors

1. PN junction capacitor

* Well known and understood.
* Nonlinear capacitance with a large VCR.

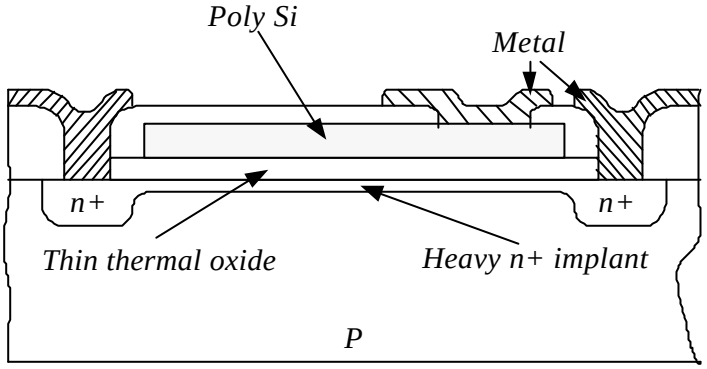
* Compatible with all MOS technologies.

2. MOS capacitor



* Realizable only by NMOS and CMOS metal-gate technology.
* TC=25 ppm/^{o}C
  Tolerance=±15%
  VC=25ppm/V
* Voltage-dependent capacitance
  accumulation depletion
  Co $(Co^{-1}\ Cd^{-1})^{-1}$

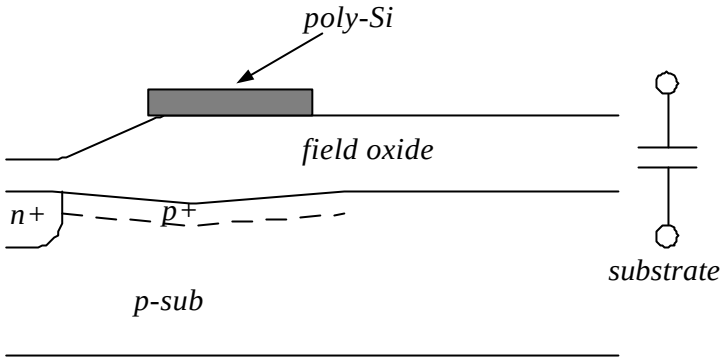
3. Poly (or metal) to bulk silicon capacitor



* Realizable by NMOS and CMOS poly-Si-gate (metal-gate) technologies.
* Need an extra mask to define the heavy n^{+} implant as the bottom plate.
* Can be trimmed by laser on poly-fuse.
  (Poly-fuse : blown with 10-20mA)
* Bottom plate pn junction parasitic capacitance ($\approx 15\% - 30\%$)
* VC of the capacitor$\approx$ -10ppm/V

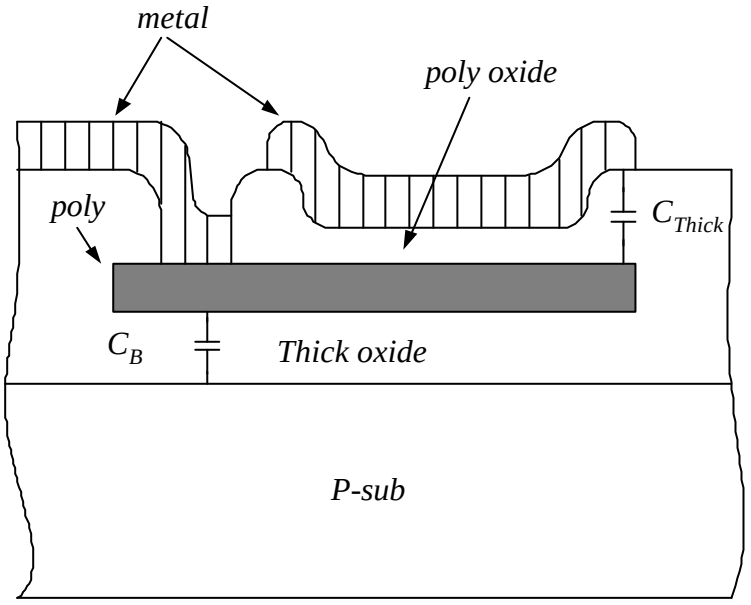
* TC ≈ 20-50 ppm/^{o}C
* Tolerance ≈ ±15%

4. Poly to field implant region capacitor



* Realizable only by NMOS and CMOS Si-gate technologies with the field implant.
* Smaller oxide capacitance per unit area
  ∵ Thick field oxide
* The capacitor's bottom plate must be always connected to the substrate.
* Low quality dielectric oxide.

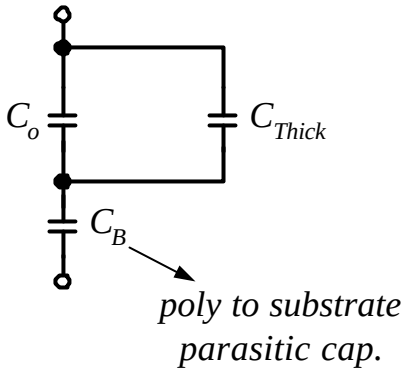
5. Metal to poly capacitor



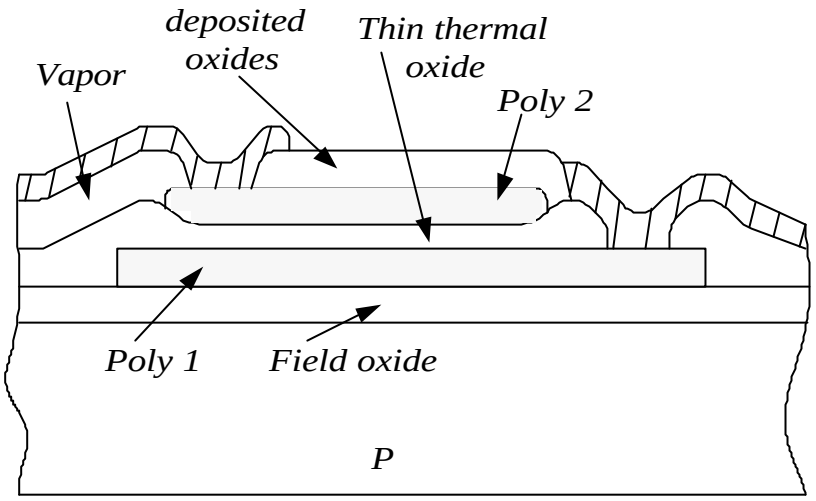
* Realizable by NMOS and CMOS Si-gate technologies.
* Interdielectric is poly-oxide.
* Extra mask to define the ploy-oxide pattern.
* Poly fuse trimming is possible.
* CVD oxide is not good as capacitor dielectric

∵ hysteresis in Q-V due to dielectric changing and relaxation.

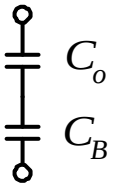
* For reliability consideration, the top metal layer must be larger than the poly oxide layer.
  ⇒ C_{Thick} exists
  ⇒ parasitic capacitance
* VC=100ppm/v, TC=100ppm/^{o}C



6. poly to poly capacitor



* Realizable by NMOS and CMOS double-poly technologies.
* VC=100ppm/v
  TC=100ppm/^{o}C
* Double-poly
  ⇒ EPROM or E^2PROM are available
  ⇒ may be applied in trimming
* The poly2 area may be smaller than the poly-oxide area
  ⇒ small C_{Thick}



General Reference: D. J. Allstot and W. C Black, Jr., IEEE Proc. vol-71, pp967-986, 1983.

§ 9-3 Tolerance Considerations.

Resistors : Absolute tolerance ≈ ±20% ~ ±40%
Matching or ratio tolerance ≈ ±0.1% ~ ±10%
Capacitors: Absolute tolerance ≈ ±15%

Matching or ratio tolerance $\approx \pm 0.01\% \sim \pm 1\%$

Resistors :

$$R = Rs\frac{L}{W} \quad , \quad \frac{DR}{R} = \frac{DL}{L} - \frac{DRs}{Rs} \approx \frac{DL}{L} - \frac{DW}{W}$$

If L is large $\Rightarrow \frac{DL}{L} \approx 0 \Rightarrow \frac{DR}{R} \approx \frac{DW}{W}$

$$R = \frac{\overline{r}}{Xt}\frac{L}{W} \quad , \quad s_R = \left[\left(\frac{d\overline{r}}{\overline{r}}\right)^2 + \left(\frac{dL}{L}\right)^2 + \left(\frac{dW}{W}\right)^2 + \left(\frac{dXt}{Xt}\right)^2\right]^{1/2}$$

$$= \frac{dW}{W} \qquad for \quad long \quad resistor$$

* Long resistor pattern is recommended in precise resistors.

Capacitors:

$$C = \frac{e_{sio2}}{t_{ox}}WL \qquad \frac{DC}{C} = \underbrace{\frac{DW}{W} + \frac{DL}{L}} + \underbrace{\frac{De_{si02}}{e_{sio2}} - \frac{Dt_{ox}}{t_{ox}}}$$

edge effect Oxide effect

CASE I : Absolute tolerance

$\frac{DC}{C} = \frac{DW}{W} + \frac{DL}{L}$ (if W and L are small or De_{sio2} and *Dtox* are neglible)

If ΔW and ΔL are independent with $s_{Dl} = s_{Dw} = s_l$

$s_{\frac{DC}{C}} = s_l\sqrt{\frac{1}{W^2} + \frac{1}{L^2}}$ (random variation)

Assume L=W=d , $s_{\frac{DC}{C}} = \frac{\sqrt{2}\sqrt{l}}{d}$ is minimum

$\Rightarrow \; s_{\frac{DC}{C}}\Big|_{square(L=W)} < s_{\frac{DC}{C}}\Big|_{non-square(W\neq L)}$

For the same WL ,minimum perimeter leads to minimum telerance.

Circular shape?

CASEII : Ratio or Matching tolerance under geometry random variation

$$a \equiv \frac{C_1}{C_2} = \frac{W_1 L_1}{W_2 L_2} \quad , \quad \frac{da}{a} = \frac{dC_1}{C_1} - \frac{dC_2}{C_2}$$

$$s_{\frac{da}{a}} = \sqrt{s_{\frac{dc_1}{c_1}}^{\,2} + s_{\frac{dc_2}{c_2}}^{\,2}} = s_l \sqrt{\frac{1}{L_1^{\,2}} + \frac{1}{W_1^{\,2}} + \frac{1}{L_2^{\,2}} + \frac{1}{W_2^{\,2}}}$$

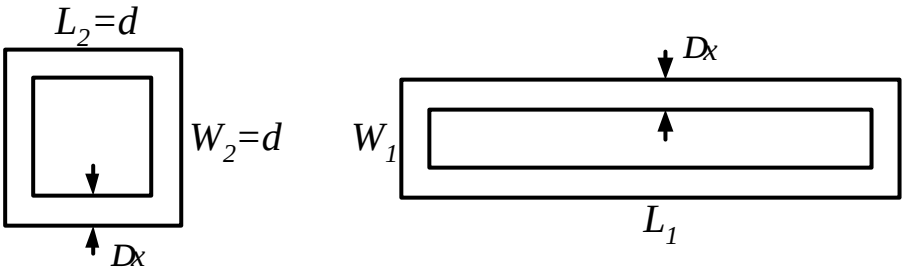
For W_2=L_2=d, $s_{\frac{da}{a}} = \frac{s_l}{d}\sqrt{2 + \frac{L_1^{\,2} + W_1^{\,2}}{(ad)^2}}$

$$\Rightarrow \left. s_{\frac{da}{a}} \right|_{min} = 2\frac{s_l}{d} \quad \text{if} \quad L_1 = W_1 = \sqrt{a}\,d \qquad (1)$$

square versus square

CASE III : Ratio tolerance under the uniform undercut effect

Uniform undercut is not a random variation.



$$a \equiv \frac{C_1}{C_2} = \frac{W_1 L_1}{d^2}$$

$$a_{actual} = \frac{W_1 L_1 - P_1 Dx + 4Dx^2}{d^2 - P_2 Dx + 4Dx^2} \cong \frac{W_1 L_1 - P_1 Dx}{d^2 - P_2 Dx}$$

$$\frac{Da}{a} \cong \frac{Dx}{d^2}\left(P_2 - \frac{P_1}{a}\right)$$

IF $P_2 = \frac{P_1}{a} \Rightarrow Da \cong 0$ i.e. $4d = \frac{2(W_1 + L_1)}{a}$

So $\left.\begin{array}{l} W_1 L_1 = ad^2 \\ 2(W_1 + L_1) = 4da \end{array}\right\}$

$$\Rightarrow W_1 = d\left(a - \sqrt{a^2 - a}\right) \quad ; \quad L_1 = d\left(a + \sqrt{a^2 - a}\right) \qquad (2)$$

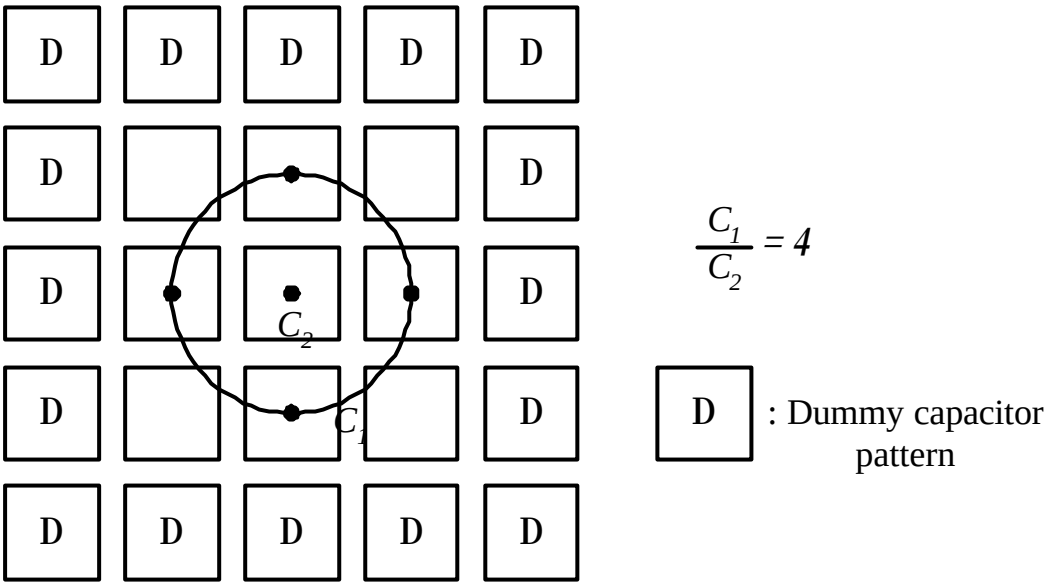
$$s_{\frac{da}{a}} = \frac{s_l}{d}\sqrt{6 - \frac{2}{a}} \overset{a>>1}{\cong} \frac{s_l}{d}\sqrt{6}$$

If $a = 1$, both conditions(1) and (2) can be satisfied

$\Rightarrow$ Ratio tolerance $\downarrow$

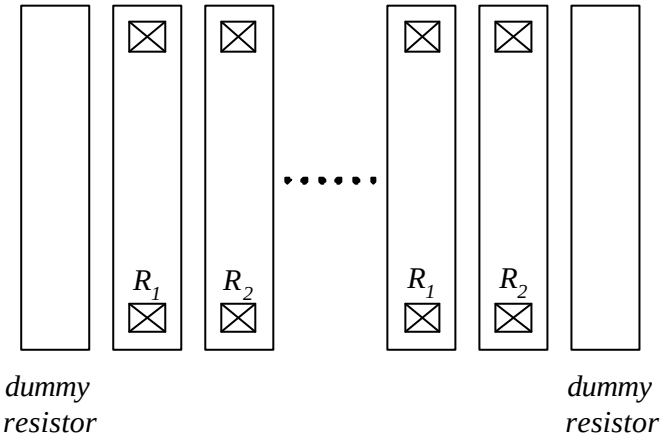
CASE IV : Ratio tolerance under edge and oxide effects

Take $a = 1 \Rightarrow$ unit capacitor array



* Centralized structure to avoid the oxide effect.
* Dummy capacitor may be omitted to save area.
* Ratio tolerance can be ±0.06 %

Similarly, for resistors, we have

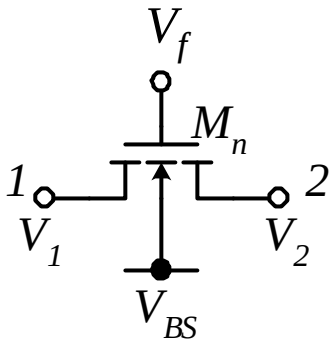


* Ratio tolerance can be ±0.25 %

§ 9-4 The MOS Switch

1. The NMOS switch

1) If $V_\phi \geq V_1 + V_{THN}$, M_N on $\Rightarrow V_2 = V_1$ full transimission



Example:

V_1= 0V, V_ϕ= 3V $\Rightarrow$ V_2= 0

V_1= 5V, V_ϕ= 8V, V_{TN} =1.5V $\Rightarrow$ V_2= 5V

2) If $V_1 + V_{THN} > V_f > V_{THN}$, M_N on

$V_2 = V_f - V_{THN}$

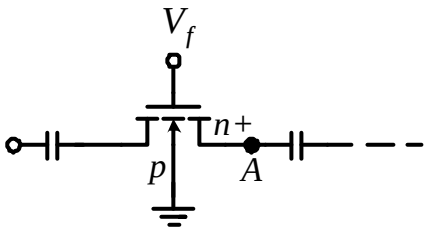
Example: $V_\phi = 5V$, $V_1 = 5V$, $V_{THN} = 1.5V$ (under substrate bias), $V_{BS} = 0V$

$\Rightarrow V_2 = 3.5V$

3) If $V_f < V_{THN}$, M_N off

Node 1 or 2 may be floating

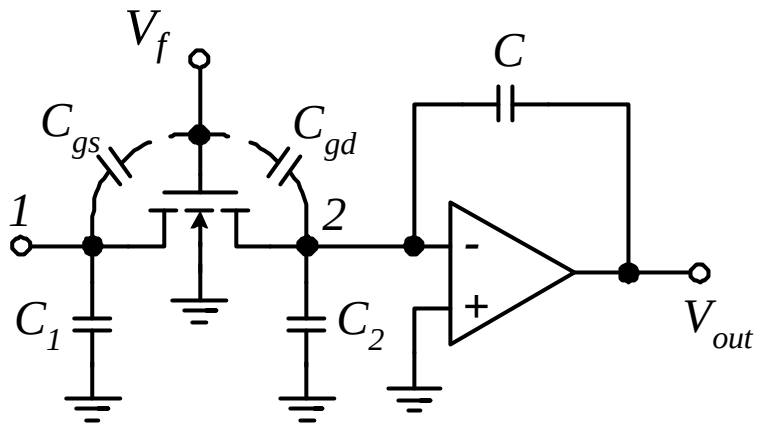
$\Rightarrow$ V_1 or V_2 will be gradually charged or discharged by the leakage current in MOS or PN junctions.



If $V_f = 0V$ for a very long time, $V_A \to 0V$ by the n^+p junction leakage current $\Rightarrow$ Not allowable in circuit design

* When the switch is turned on or off, the charging or discharging current is nonlinear $\Rightarrow$ Nonlinear resistor

Capacitance feedthrough effect:



$V_f : V_{DD} \rightarrow 0$

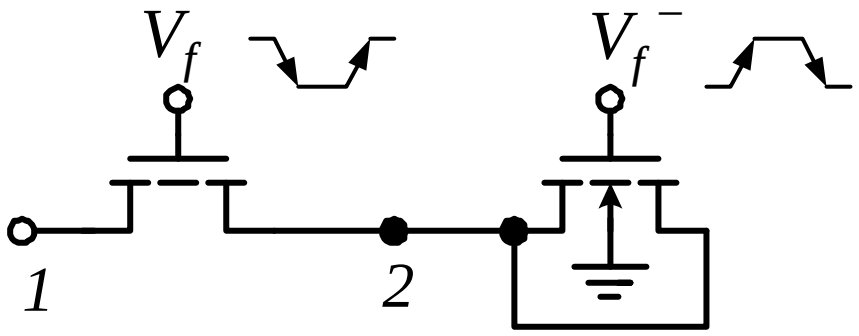
$$V_{1f} \approx V_{1i} - V_{DD}\frac{C_{gs}}{C_{gs}+C_1}$$

$$V_{2f} \approx V_{2i} - V_{DD}\frac{C_{gd}}{C_{gd}+C_1}$$

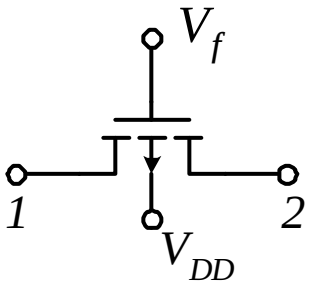
error voltage

Example: $C_{gd} \approx 0.02PF, C_2 = 2PF, V_{DD} = 10V$, error voltage $\approx 0.1V$

Compensation circuit:



2. The PMOS switch



* Can pass high voltage without offset.

Example: $V_\phi = 0V$, $V_{DD} = 5V = V_1$

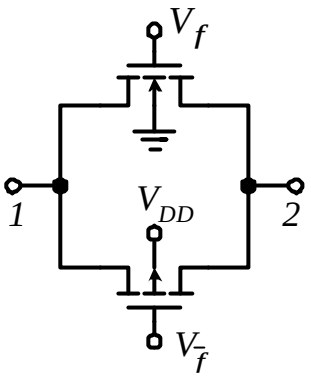
$\Rightarrow V_2 = 5V \quad \because 1 = source$ and $|V_{GS}| = 5V$

* Can' t pass low voltage completely.

  Example: $V_\phi = 0V$, $V_{2i} = 5V$, $V_1 = 0V$, $|V_{TP}| = 1.5V$

  $\Rightarrow V_{2f} \approx 1.5V \neq 0V$

3. The CMOS switch



* Full transmission
* The clock feedthrough effect can be greatly compensated, if the delay between V_f and $V_{\bar{f}}$ is zero.
* Nonlinear C_{gs} and C_{gd} and the delay between V_f and $V_{\bar{f}}$ make the compensation of the feedthrough effect quite complicated.
* If $V_1 = 5V = V_f, V_{\bar{f}} = 0V, V_{DD} = 5V, V_{TN} = |V_{TP}| = 1.5V$

  $V_2 = 0V \rightarrow V_2 = 5V - 1.5V = 3.5V$: NMOS and PMOS

  $V_2 = 3.5V \rightarrow V_2 = 5V$: Only PMOS

  If V_1=0V, V_{2i}=5V

  $V_2 = 5V \rightarrow V_2 = 1.5V$: NMOS and PMOS

  $V_2 = 1.5V \rightarrow V_2 = 0V$: Only NMOS

Chapter 10 CMOS Bandgap References

§10-1 Basic Principles of Bandgap References (BGR)

$V_{BE(on)} = mV_{therm}\ln(I_1 / I_S)$

$I_S = qAn_i{}^2\overline{D_n}/Q_B$ $\quad I_S$: Reverse saturation current of a BJT

$= Bn_i{}^2\overline{D}$ $\quad A$: Area of a BJT

$= B'n_i{}^2T\overline{m}$ $\quad Q_B$: Base minority carrier charges

where B and B' are constants, indep. of T. $\quad \overline{D}$: Average diffusivity of carriers

$\overline{m} = CT^{-n}$ $\quad$ C:Constant, indep. of T.

n:Temp. exponent.

$n_i{}^2 = ET^3\exp(-V_{GO}/V_{therm})$ $\quad E$: Constant, indep. of T.

V_{GO} : Energy gap.

$\Rightarrow V_{BE(on)} = mV_{therm}\ln[I_1T^{-g}F\exp(V_{GO}/V_{therm})]$

F : Constant , indep. of T.

$g = 4 - n$

$I_1 = GT^a$ where I_1 is the collector current and G is a temp.-indep. constant.

$\Rightarrow V_{BE(on)} = V_{GO} - V_{therm}[(g-a)\ln T - \ln(FG)]$

In general, the output voltage V_{out} is a sum of $V_{BE(on)}$, and KV_{therm} with a weighting factor K such that V_{out} is nearly indep. of T.

$$V_{BE(on)} + KV_{therm} = V_{out} = V_{GO} - mV_{therm}(g-a)\ln T + mV_{therm}[K + \ln(FG)] \text{ .....(1)}$$

$$\left.\frac{dV_{out}}{dT}\right|_{T=T_O} = 0 = \frac{mV_{thermo}}{T_O}[K + \ln(FG)] - \frac{mV_{thermo}}{T_O}(g-a)\ln T_O - \frac{mV_{thermo}}{T_O}(g-a) + \frac{d}{dT}V_{GO}$$

$$\Rightarrow K + \ln(FG) = (g-a)\ln T_O + (g-a) - \left(\frac{d}{dT}V_{GO}\right)\cdot\frac{T_O}{mV_{thermo}} \text{ ....(2)}$$

Substituting (2) into (1) , we have

$$V_{out} = V_{GO} + mV_{therm}(g-a)(1+\ln\frac{T_O}{T}) - T\frac{d}{dT}V_{GO}$$

$$V_{GO} = 1.16 - \frac{7.02\times10^{-4}\cdot T^2}{T+1108}$$

$$\left.\frac{d}{dT}V_{GO}\right|_{T=T_O} = -\frac{14.04\times10^{-4}T_O(T_O+1108) - 7.02\times10^{-4}\cdot T_O{}^2}{(T_O+1108)^2}$$

$$= -\frac{14.04\times10^{-4}\cdot T_O}{T_O+1108} + \frac{7.02\times10^{-4}\cdot T_O{}^2}{(T_O+1108)^2}$$

$$\Rightarrow V_{out} = mV_{therm}(g-a)(1+\ln\frac{T_O}{T}) + 1.16 - \frac{7.02\times10^{-4}\cdot T^2}{T+1108} - \frac{14.04\times10^{-4}\cdot T_O T}{T_O+1108} + \frac{7.02\times10^{-4}\cdot T_O^2\cdot T}{(T_O+1108)^2}$$

If $g = 3.2, m = 1, a = 1, T_O = 25^O C$

$$\Rightarrow V_{out}(T)\big|_{T=25^O C} = 1.16 + 2.2(0.0259) - \frac{21.06\times10^{-4}(298)^2}{298+1108} + \frac{7.02\times10^{-4}(298)^2}{(298+1108)^2}$$

$$= 1.093V$$

§10-2 Bipolar Bandgap Reference

Widlar bandgap reference

*Feedback element Q_4 is used to force Q_3 on.

*Q_4 also serves as a start-up circuit.

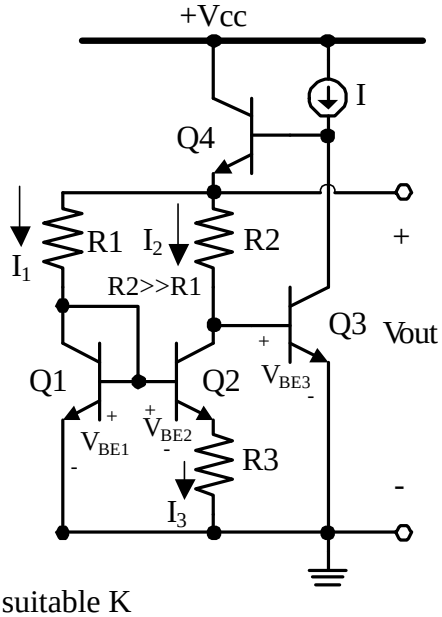
*$V_{out} = I_2R_2 + V_{BE3}$

$I_2 = I_3$ if $I_{B2} = I_{B3}$

$$I_3 = \frac{V_{BE1} - V_{BE2}}{R_3} = \frac{1}{R_3}mV_{therm}\left[\ln(\frac{I_1}{I_2}) + \ln(\frac{I_{S2}}{I_{S1}})\right]$$

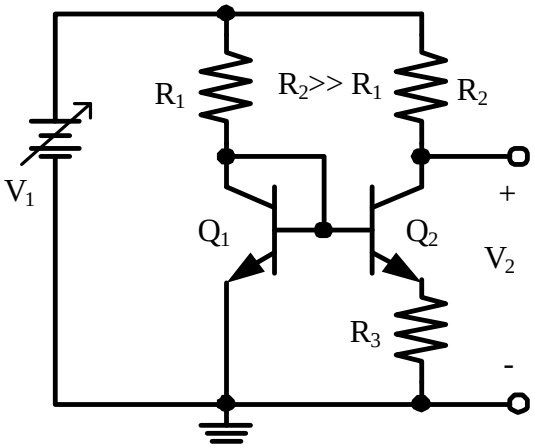
$$V_{out} = V_{BE3} + \left\{\frac{R_2}{R_3}m\left[\ln\left(\frac{R_2}{R_1}\right) + \ln\left(\frac{I_{S2}}{I_{S1}}\right)\right]\right\}\cdot V_{therm}$$

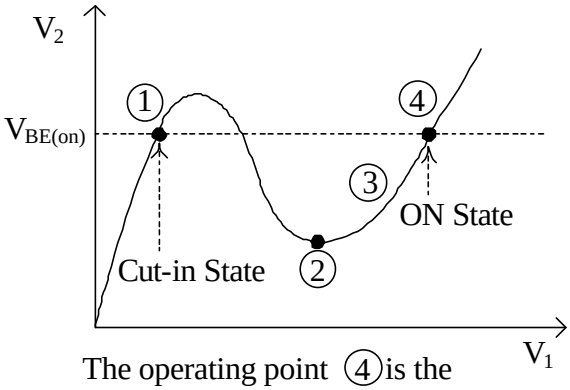
$I_1/I_2 = R_2/R_1$ If $V_{BE1} = V_{BE3}$



Adjust R_2/R_3 , R_2/R_1 and I_{S2}/I_{S1} to give a suitable K

And Keep $I \cong I_2$ to obtain $I_{B2} \cong I_{B3}$ and $\frac{I_{S3}}{I_{S1}} = \frac{I_3}{I_1}$ to obtain $V_{BE1} = V_{BE3}$.





The operating point ④ is the desired operating point

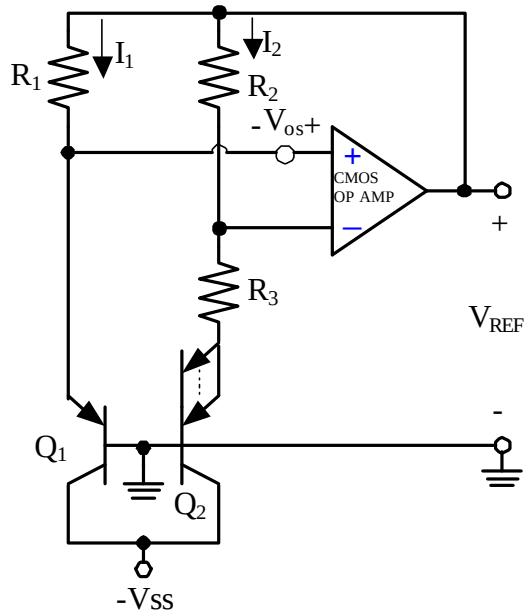
=>Need a start-up circuit.

§10-3 CMOS Real Bandgap Reference (BGR)

§10-3.1 CMOS BGR via BJTs and Resistors

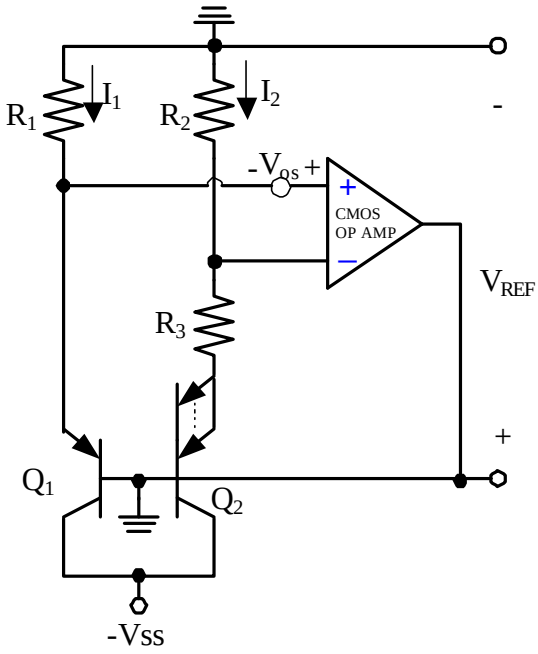
Version 1:

N-well CMOS, positive V_{REF}



Version 2:

N-well CMOS, Negative V_{REF}



Q_1,Q_2:Substrage-well-source/drain parasitic vertical BJTs

$$V_{BE} = mV_{therm} \ln \frac{I_E}{I_S}$$

$$V_{REF} = \pm\{V_{BE1} + \frac{R_2}{R_3} V_{therm} (\ln \frac{R_2}{R_1} + \ln \frac{I_{s2}}{I_{s1}}) + V_{OS}[\frac{R_3 + R_2}{R_3}]\}$$

Typical design values:

I_1=80 μ A I_2=8 μ A

$$R_2 \approx \frac{0.6V}{8\mu A} = 75K\Omega,\ R_1 = \frac{R_2}{10} = 7.5K\Omega,\ R_3 = \frac{60mV}{8\mu A} = 7.5K\Omega$$

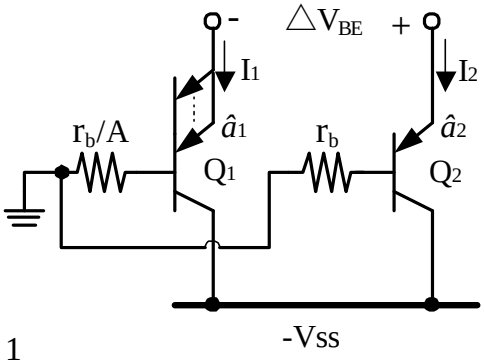
Large resistance➔use well resistors

R1,R2,R3: n+/p+ diffusion resistors

n+ - poly resistors

well resistors

Both transistors are in the active region



Error analysis:

1. Error due to base resistances

$$V_{BE1} = V_{therm} \ln \frac{I_1}{I_S} + V_{therm} \ln \frac{1}{1+\frac{1}{\beta_1}} + \frac{r_b I_1}{A\beta_1}$$

$$\Delta V_{BE} = V_{therm} \ln A + V_{therm} \ln \frac{I_2}{I_1} + V_{therm} \ln \frac{1+\frac{1}{\beta_1}}{1+\frac{1}{\beta_2}} + r_b\left(\frac{I_2}{\beta_2} - \frac{I_1}{A\beta_1}\right)$$

If $\hat{a}_1$, $\hat{a}_2$ are not large enough or r_b is too large,

➔ ΔV_{BE} due to r_b and β is large.

$$V_{REF} = \pm\{V_{BE1} + V_{OS}\left(\frac{R_3+R_2}{R_3}\right) + \frac{R_2}{R_3} V_{therm}\left(\ln\frac{R_2}{R_1} + \ln\frac{I_{s2}}{I_{s1}} + \ln\frac{1+\frac{1}{\beta_1}}{1+\frac{1}{\beta_2}}\right) + \frac{R_2}{R_3} r_b\left(\frac{I_2}{\beta_2} - \frac{I_1}{A\beta_1}\right)\}$$

2.Error due to input offset voltage V_{os}

V_{os}=10mV, $V_{OS}(1+\frac{R_2}{R_3}) \approx 10V_{OS} = 100mV$

TC error due to

$$V_{OS} : \frac{1}{V_{REF}} \frac{d}{dT} V_{REF} = \frac{(1+\frac{R_2}{R_1})V_{OS}}{V_{REF} T_0} = \frac{10 \times 10mV}{1.26V \times 300^o K} = 264\, ppm/^o C$$

3.Error due to Bias current variation

$$V_{BE1} = V_{therm} \ln \frac{I_1}{I_{S1}} = V_{Threm} \ln \frac{V_{therm} \ln A}{R\ I_{S1}}$$ (R_3=R_1)

$$= V_{therm} \ln \frac{V_{therm} \ln A}{R_1(T_O) I_{S1}} + V_{therm} \ln \frac{R_1(T_O)}{R_1(T)} \qquad I_1 = I_2$$

If R_1 is indep. of T $\Rightarrow V_{BE} = V_{therm} \ln \frac{V_{therm} \ln A}{R_1(T_O) I_{S1}}$

If R_1 depends on T $\Rightarrow V_{BE} = V_{therm} \ln \frac{V_{therm} \ln A}{R_1(T_O) I_{S1}} + V_{therm} \ln \frac{R_1(T_O)}{R_1(T)}$

$$V_{BE} = V_{BE}\big|_{ideal} - V_{therm} \cdot \left(\frac{1}{R} \frac{dR}{dT}\bigg|_{T_O} \right)(T - T_O) - V_{therm} \left(\frac{1}{2R} \frac{d^2R}{dT^2}\bigg|_{T_O} \right)(T - T_O)^2$$

$PTAT^2$ $PTAT$ $PTAT^3$ $PTAT$

$$+ V_{therm} \left(\frac{1}{2R^2} \frac{dR}{dT}\bigg|_{T_O} \right)(T - T_O)^2 - .....$$

$PTAT^3$ $PTAT$

If R is only linearly dependent on T, we still have $PTAT^2$ term
The $PTAT^2$ term can be cancelled via curvature compensations.

4.TC Error due to Base Resistance

$$\Delta V_{BE} = r_b \frac{I_2}{\beta_2}$$

$$\text{TC error} = (1 + \frac{R_2}{R_1}) \frac{r_b I_2}{V_{ref} \beta_2} \left(\frac{1}{r_b} \frac{dr_b}{dT} + \frac{1}{I_2} \frac{dI_2}{dT} - \frac{1}{\beta_2} \frac{d\beta_2}{dT} \right)$$

Example : $r_b = 2K\Omega$, TC of $r_b = 1000 ppm/^O C$, $I_2 = 30mA$, $\beta = 150$,

TC of $\beta = 7000 ppm/^O C$

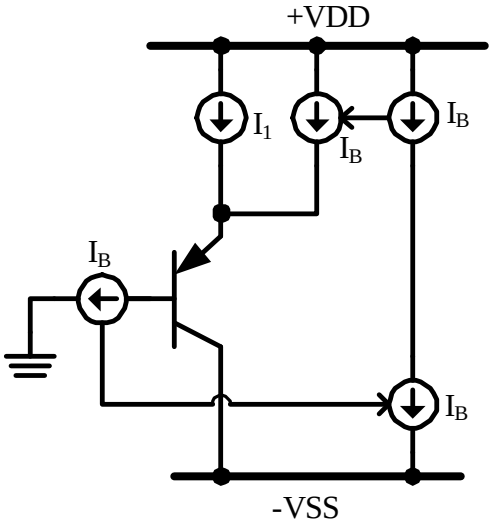
$\Rightarrow$ TC = –8.6 $ppm/^O C$

5.Error due to base current

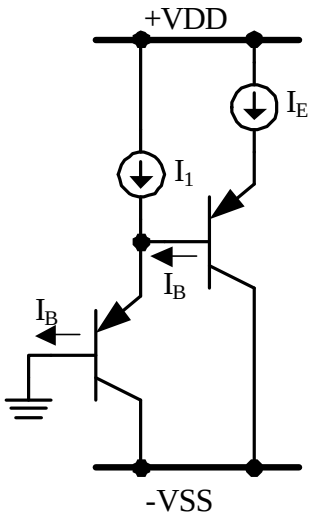
Base current cancellation technique

*To compensate for the different between the collector, emitter, or base current

Version 1:



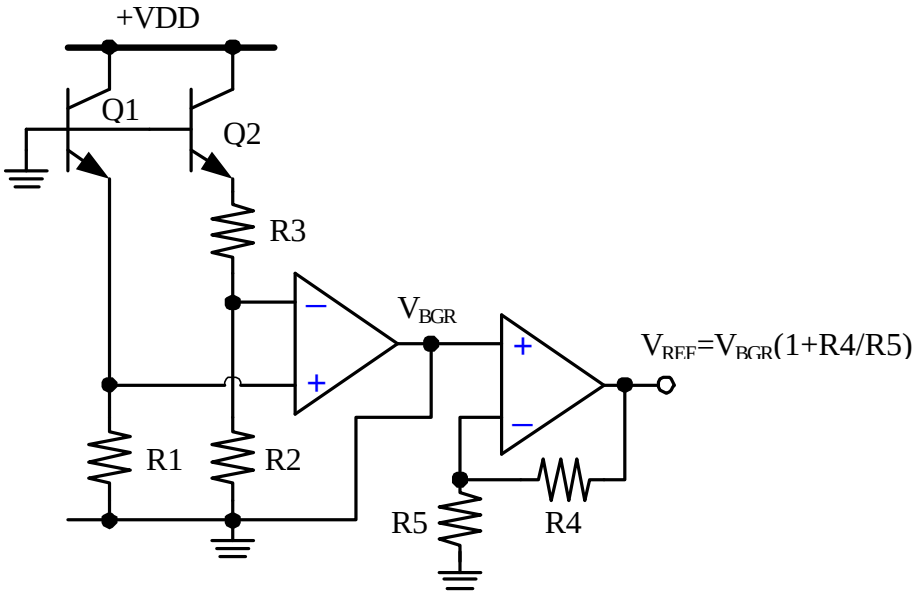
Version2:



Ref:1.IEEE J .Solid-State Circuits, vol.SC-18, pp634-640, DEC. 1983

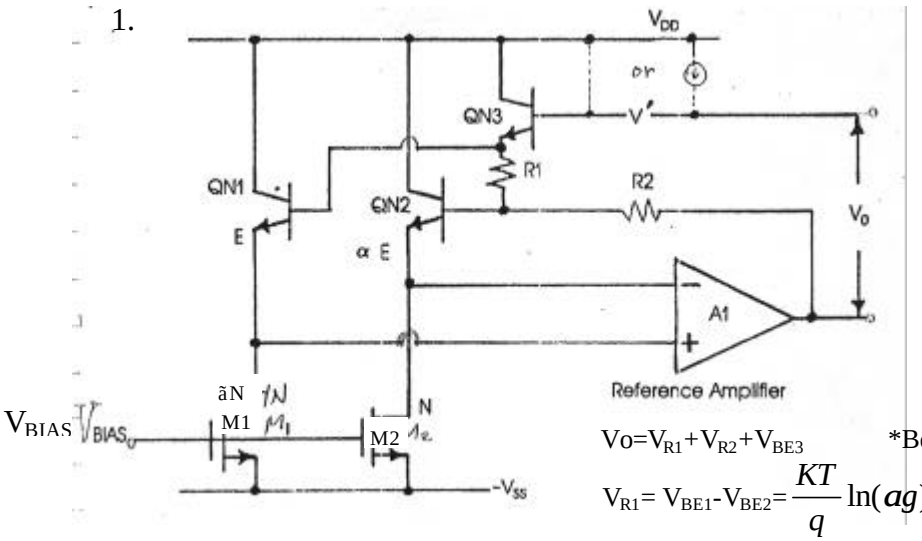
2. IEEE J .Solid-State Circuits, vol.SC-19, pp1014-1021, DEC. 1984

The circuit to obtain V_{REF} from a BGR



§ 10-3.2 Improved structure

1.

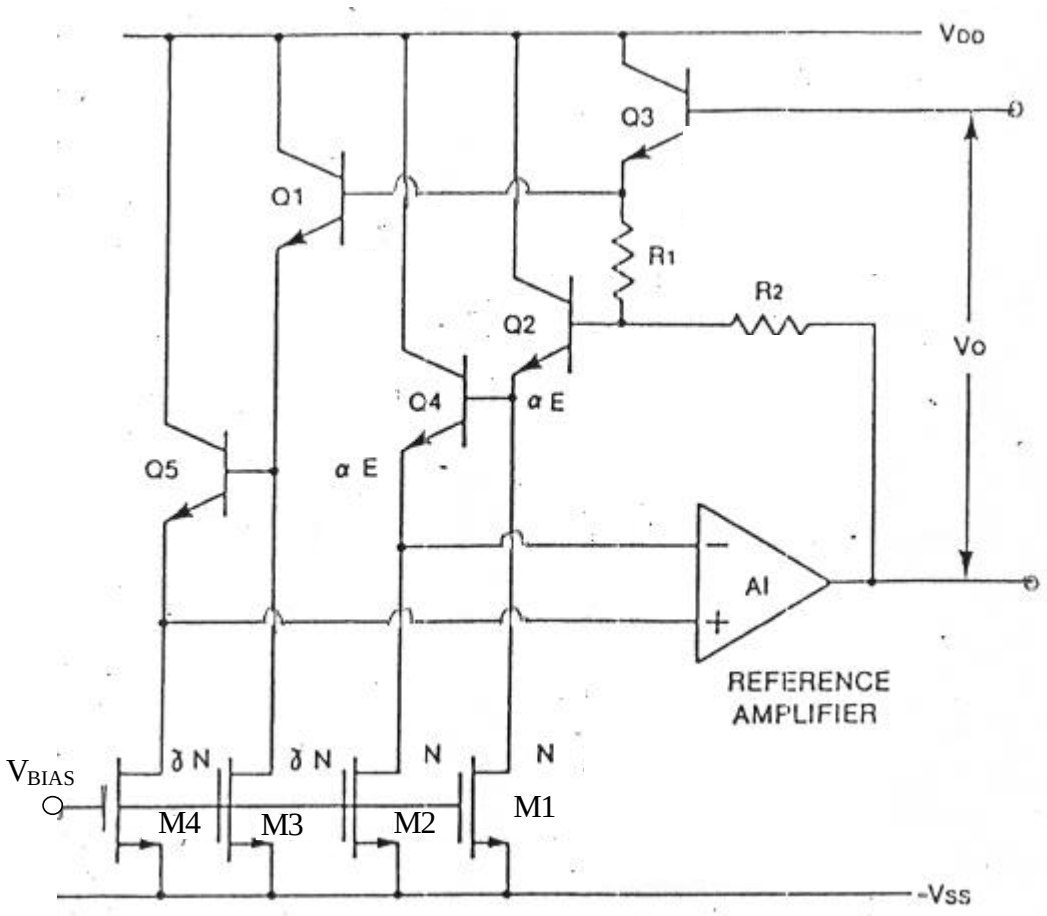


Vo=V_{R1}+V_{R2}+V_{BE3} *Better matching

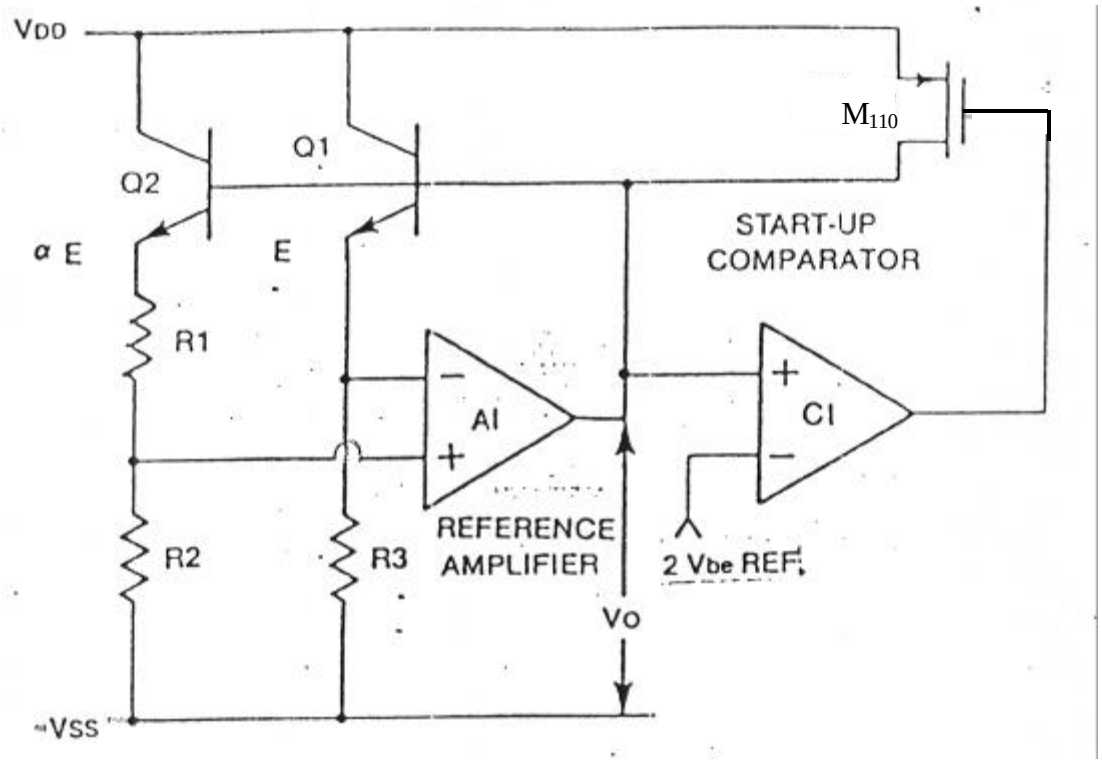
V_{R1}= V_{BE1}-V_{BE2}= $\frac{KT}{q}\ln(ag)$

Vo=VBE3+ $\frac{KT}{q}[\ln(ag)]$(1+R/R) =>Bandgap Reference

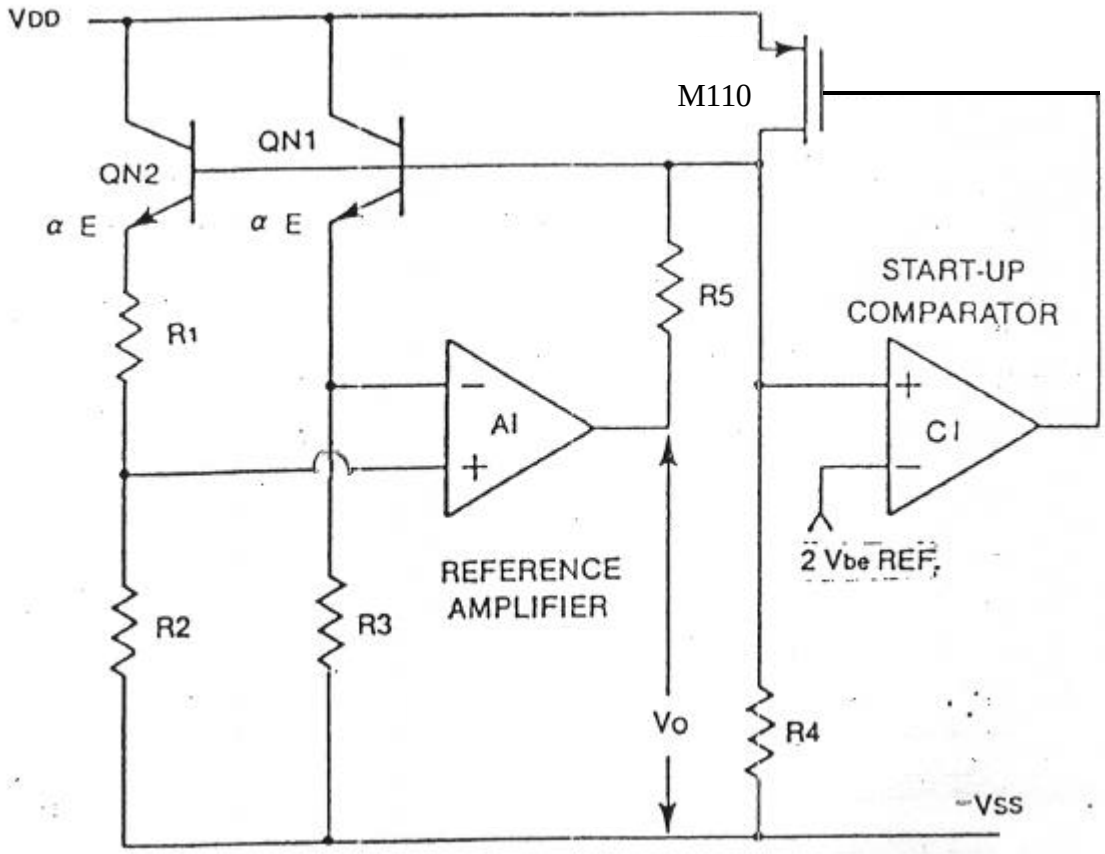
2.

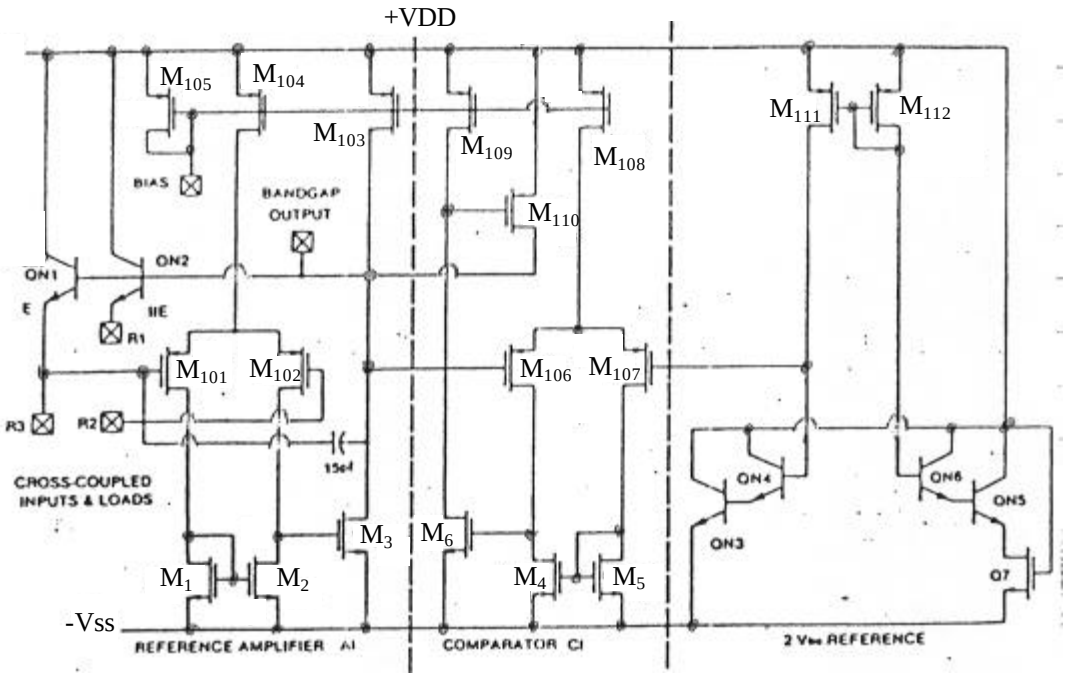

VDD
Q3
Q1
R1
R2
Q2
Vo
Q4
α E
Q5
α E
AI
REFERENCE
AMPLIFIER
VBIAS
∂ N
∂ N
N
N
M4
M3
M2
M1
-Vss

3.

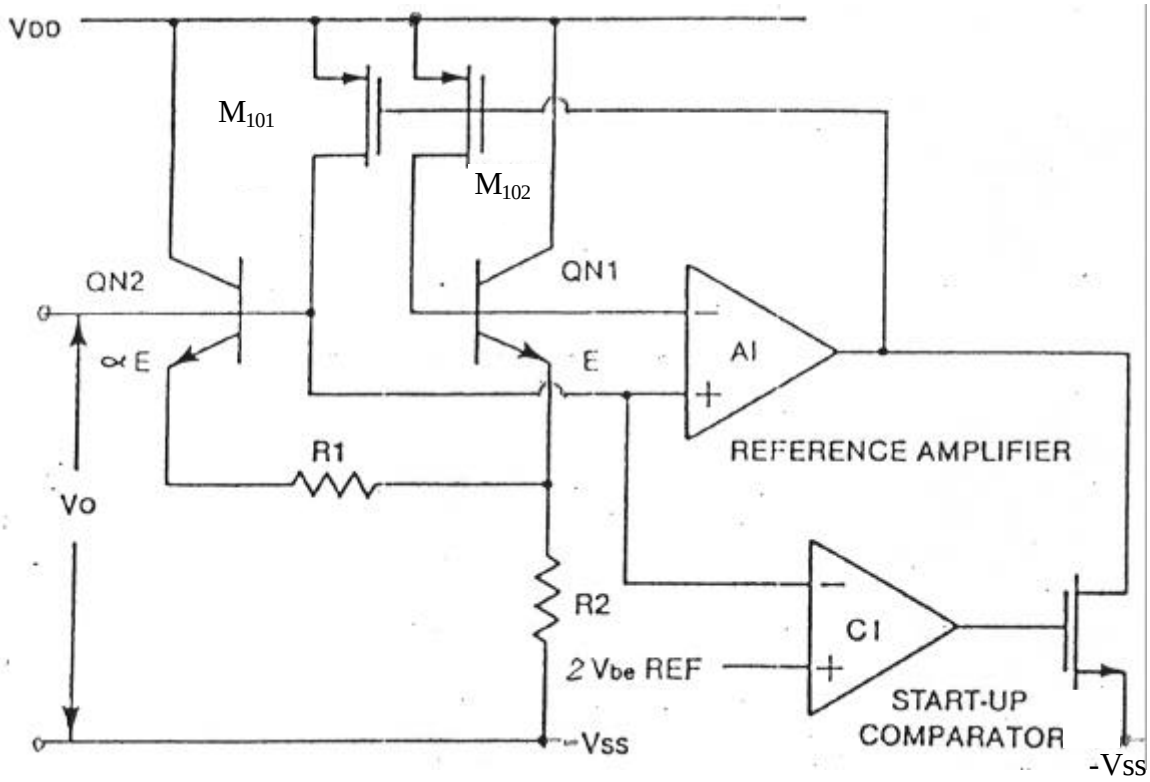

VDD
M110
Q1
Q2
START-UP
COMPARATOR
α E
E
R1
AI
CI
REFERENCE
AMPLIFIER
2 Vbe REF.
R2
R3
Vo
-VSS

4.


VDD
M110
QN1
QN2
α E
α E
R1
R5
START-UP
COMPARATOR
A1
C1
REFERENCE
AMPLIFIER
2 Vbe REF
R2
R3
Vo
R4
-Vss


+VDD
M105
M104
M103
M109
M108
M111
M112
BIAS
BANDGAP
OUTPUT
M110
QN1
QN2
E
IIE
R1
M101
M102
M106
M107
R3
R2
CROSS-COUPLED
INPUTS & LOADS
QN4
QN6
QN5
QN3
Q7
M3
M6
M1
M2
M4
M5
-Vss
REFERENCE AMPLIFIER A1
COMPARATOR C1
2 Vbe REFERENCE

5.Low Power Supply Circuit:



*Low driving capability

Power supply limits:

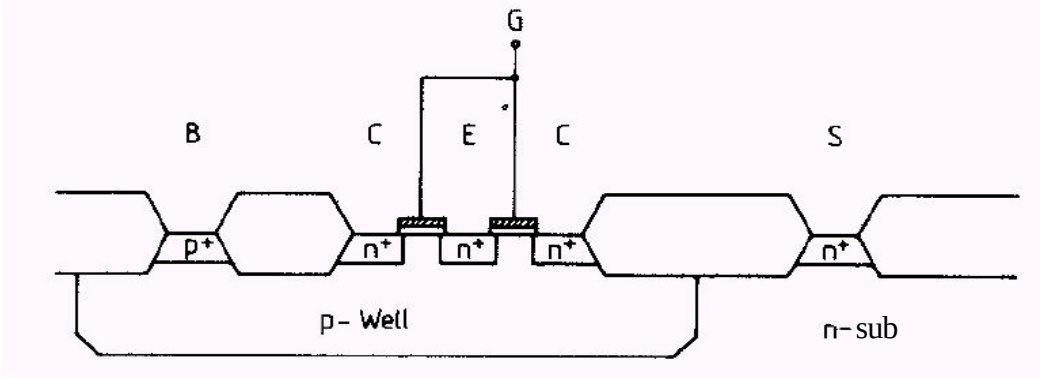
	Low Possible	Voltage T=25°C
Bandgap reference Topology	PMOS Inputs	NMOS Inputs
	$V_{TP} \leq 1.0V$	$V_{TN} \leq 1.0V$
1	1.5v	2.2v
2	1.95v	2.95v
3	1.90v	-
5	2.5v	1.5v

§ 10-3.3 CMOS BGR via lateral Transistor

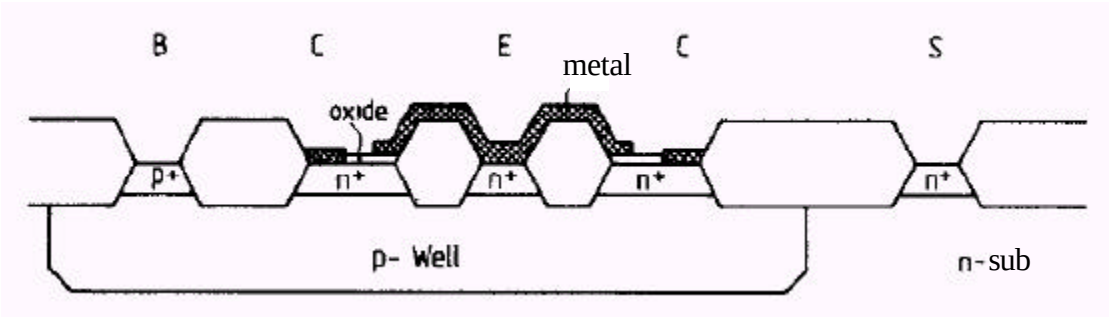
Ref:IEEE J .Solid-State Circuits, vol. SC-20, pp.1151-1157, DEC. 1985

Structure of a lateral BJT in CMOS:

A.

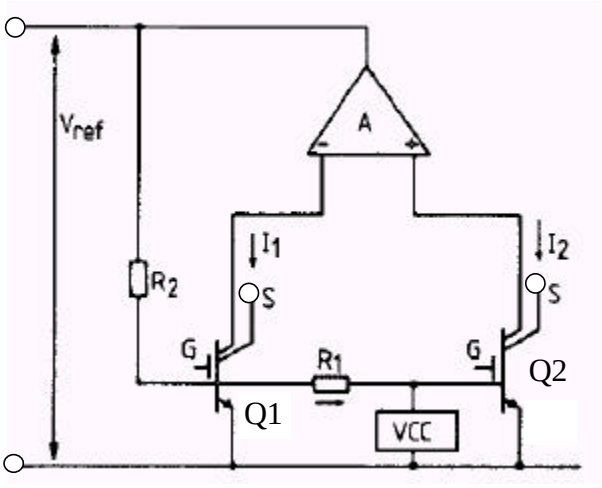


B.

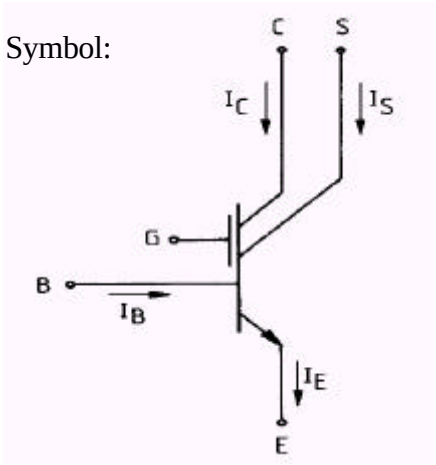


Voltage reference via LBJT:

Conceptual circuit：



Symbol:



A:Current comparator

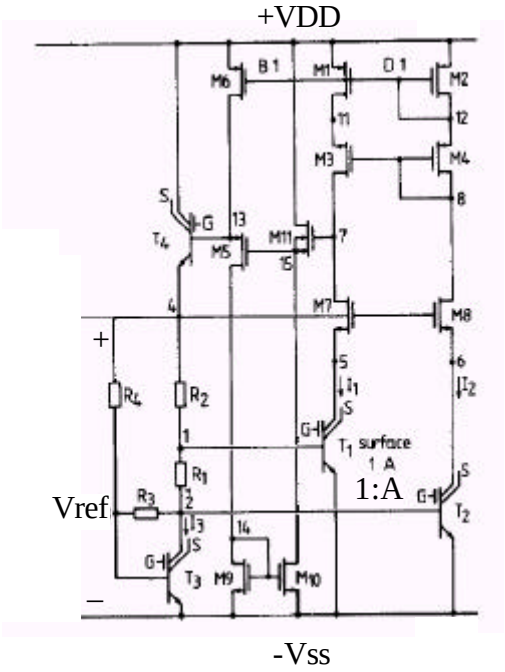
VCC:Voltage-controlled current source

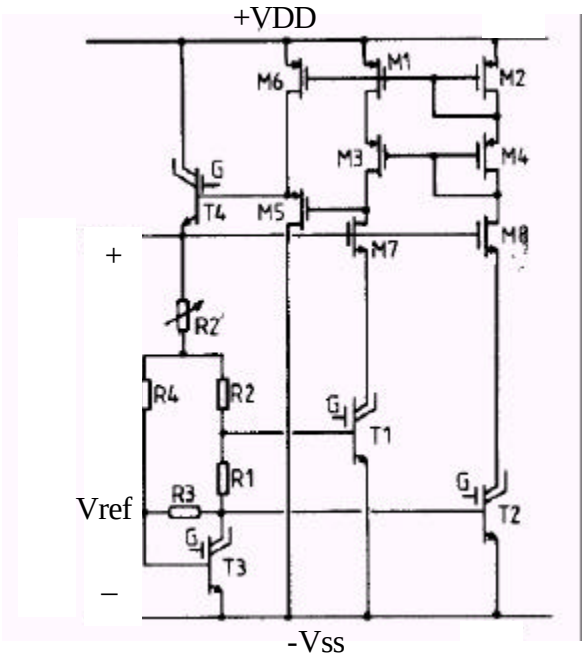
G:A negative voltage is applied to cause accumulation.

Advantages:(1)The offset of the amplifier A has a negligible effect on V_{REF}

(2)Simple structure.

Purpose of VCC : To provide a current path for $I_{R1} >> I_{B1}, I_{B2}$





* High supply voltage.
* Two source follwers+one emitter follower in(A) current amp.=>higher current gain

* Low supply voltage
* Low current gain in A
* R2 is trimmable

R4,R3,T3:VCC

R3: To keep T3 from quasi-saturation

R4:To sense the output voltage and transform it into the collector current of T3.

* All resistor are polyresistors
* Low output impedance.

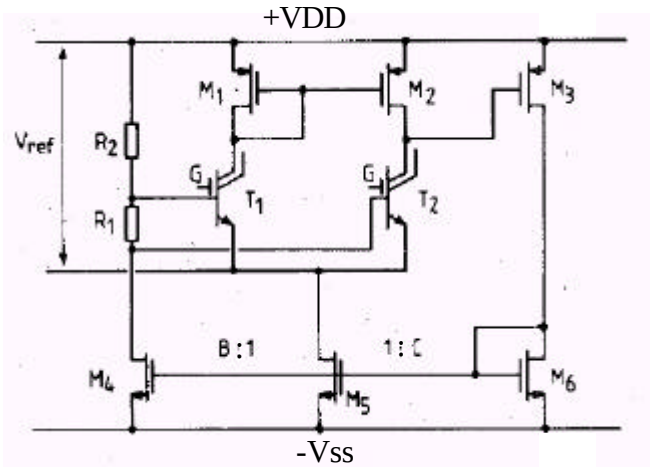
Measured results:

V_{REF} mean :1.2285V ;	standard deviation :150ì V
Minimal supply voltage	2.2V
Supply current	79ì A
Noise spectra	$316nV/\sqrt{Hz}(white)$; $560nV/\sqrt{Hz}(\frac{1}{f},1KHz)$
PSRR(100Hz)	60dB
Load regulation (ÄVout/Iout)	3.6ì V/ì A
Chip area	0.42 mm^2

High PSRR BGR:

* R_1,R_2 may be p-well resistors and PSRR still high.

Experimental results:



V_{REF}	1.2281V (mean)
	350ì V (ó)
Minimal Supply	1.7V
Supply Current	20ì A
Noise Spectra	$500nV/\sqrt{Hz}(white)$
	$1mV/\sqrt{Hz}(\frac{1}{f},1KHz)$
PSRR(100Hz)	77dB
Load Regulation ($ÄV_{out}/I_{out}$)	4.1mv/ì A
Chip area	0.18 mm^2

Curvature-Compensated BGR:

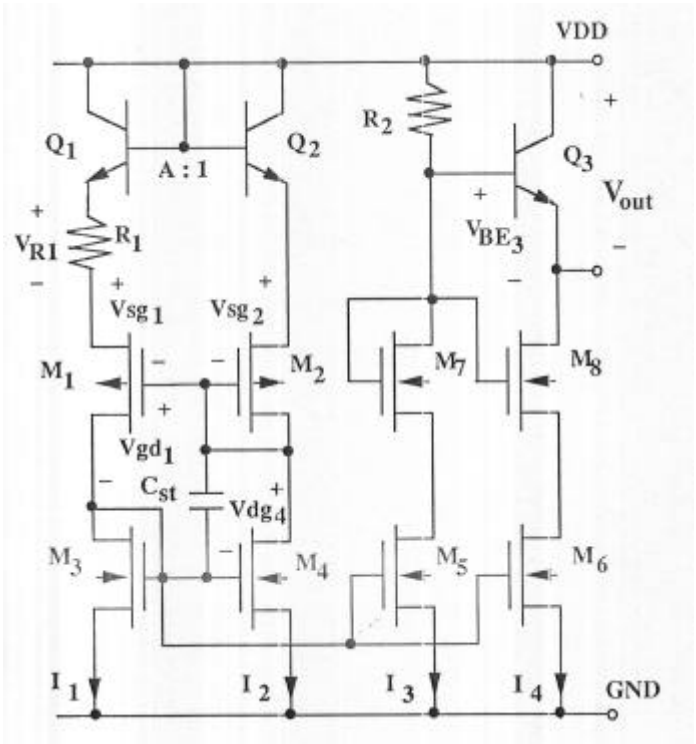
Ref: IEEE J. Solid-State Circuits, vol. sc-20, pp.1283-1285, Dec. 1985

§10-4 High-Precision Curvature-Compensated CMOS Bandgap Voltage References (BVR)

Ref: Int. J. of Analog ICs and Signal Processing, Kluwer, pp. 207-215, 1992

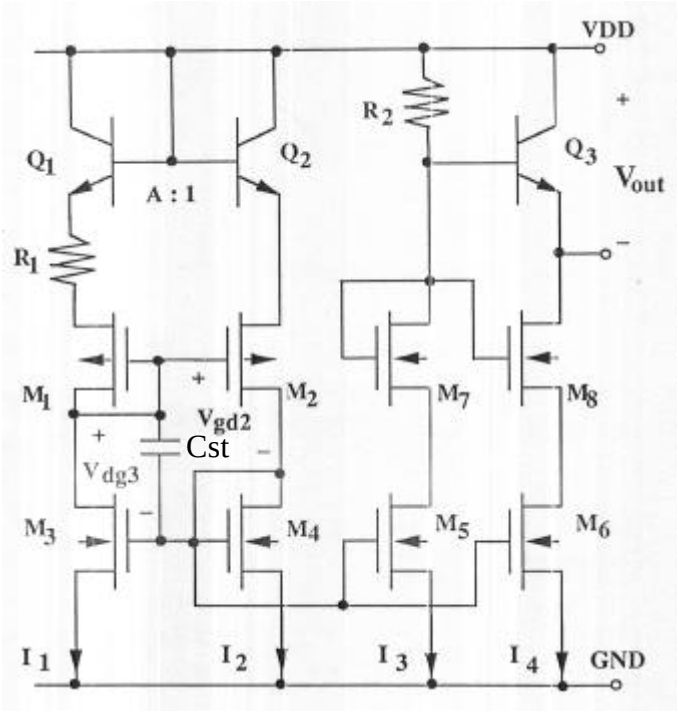
1. Type A structure

The circuit stricture of the proposed BVR (Type A)

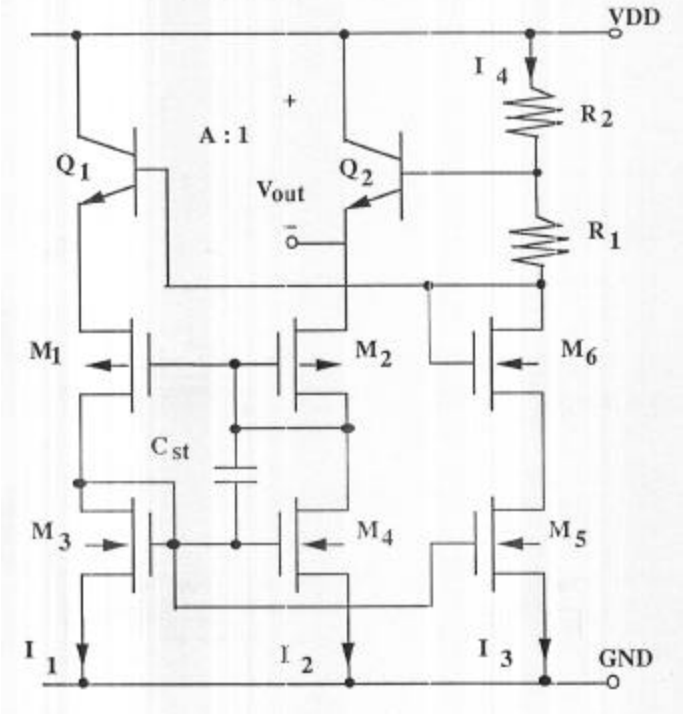


$$V_{out} = V_{BE3} + I_3 R_2 = V_{BE3} + r_3 \frac{R_2}{R_1}\left(\frac{kT}{q}\ln A^* + \Delta V_{sg}\right)$$

2. Type $\bar{A}$ structure

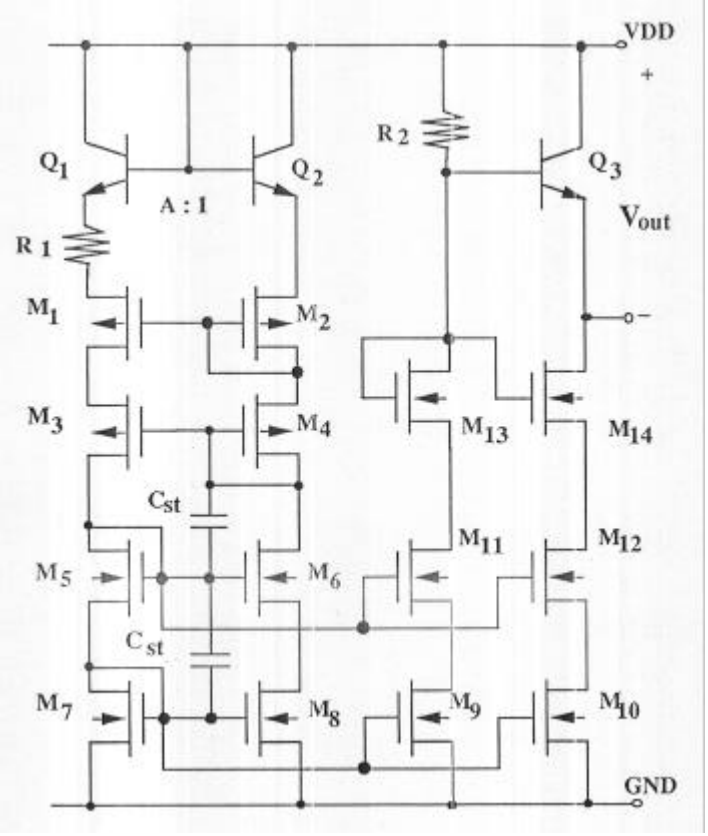


3. Type B structure

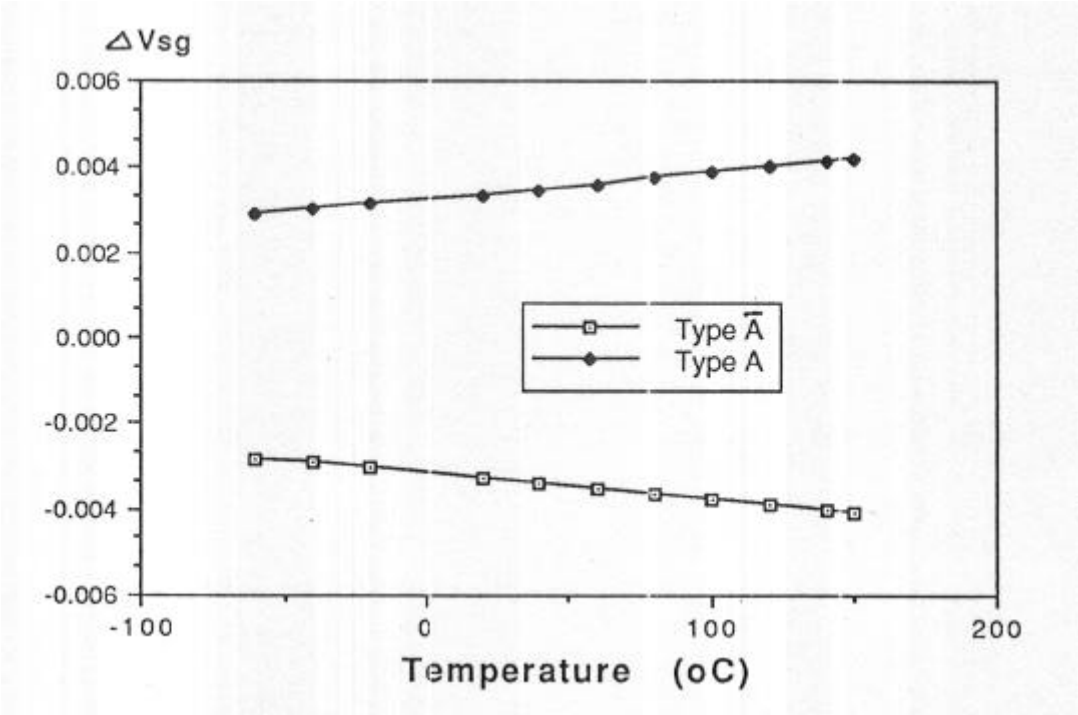


4. Type C structure

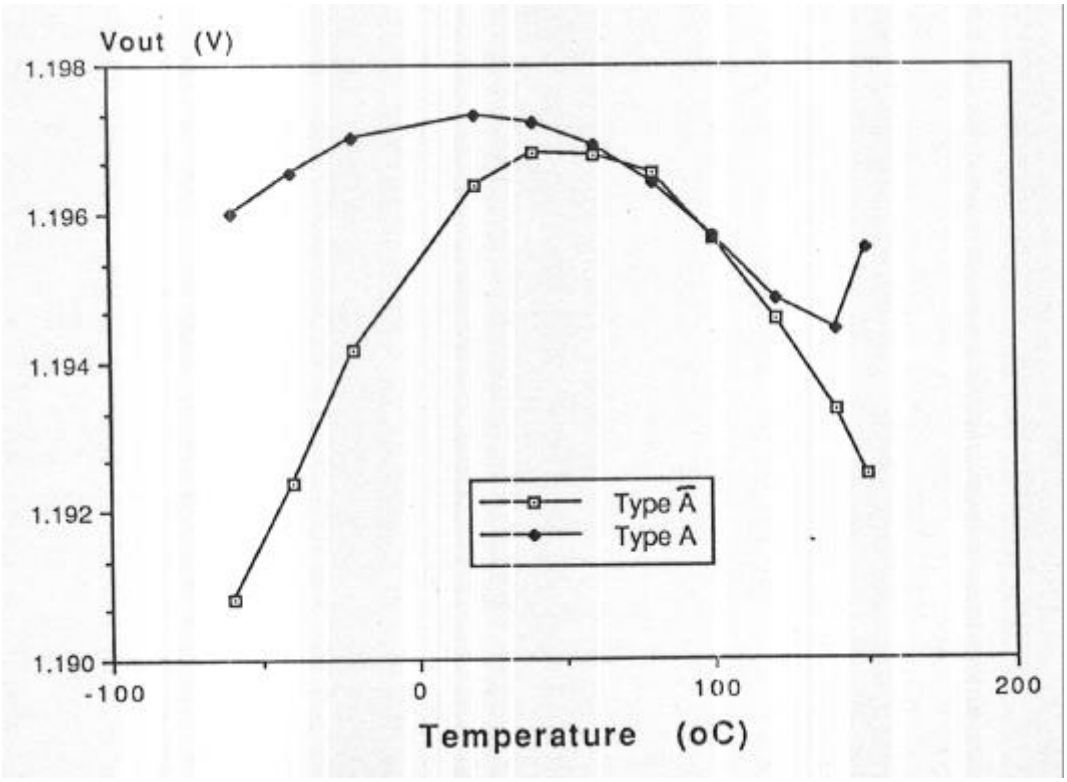
The cascode structure of BVR (Type C):



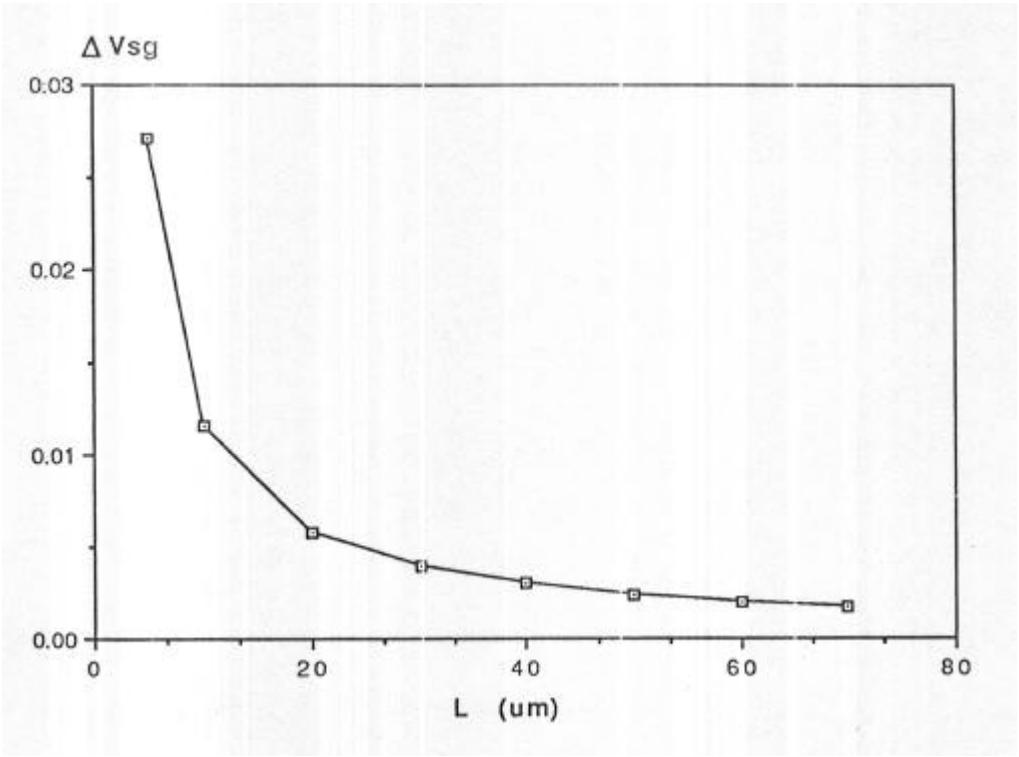
The variation of △Vsg versus temperature



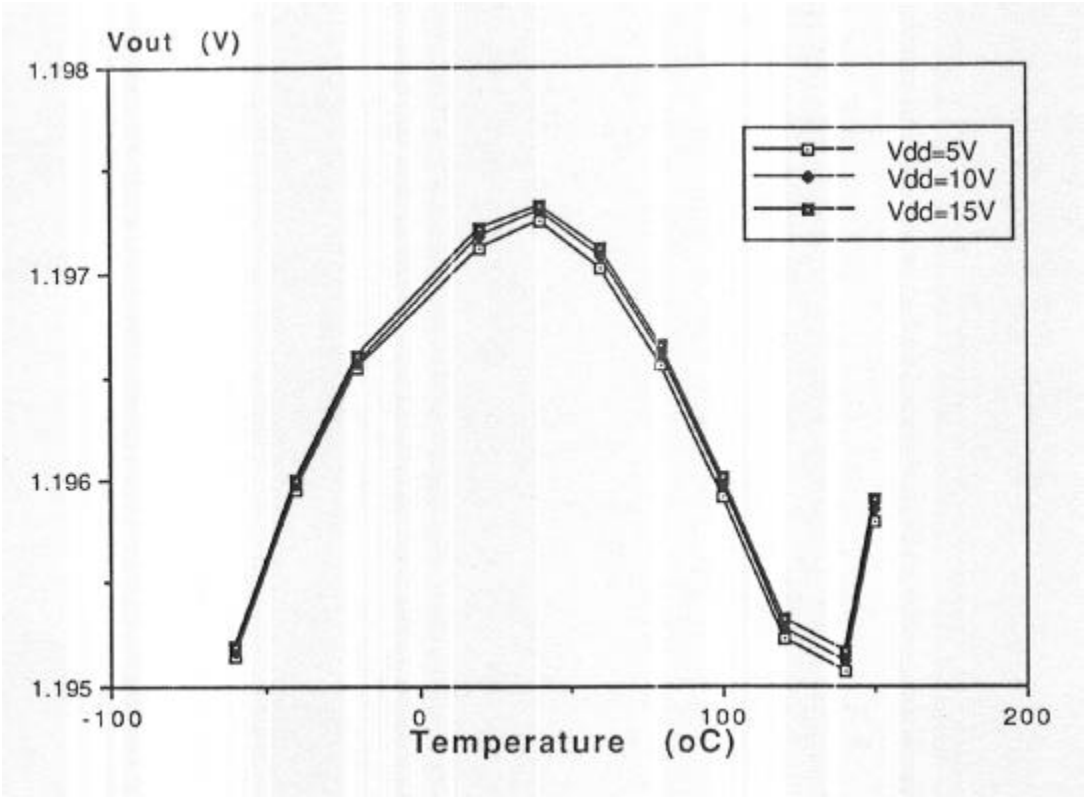
The simulated output voltages versus temperature in Type A and Type A $\bar{B}$VR



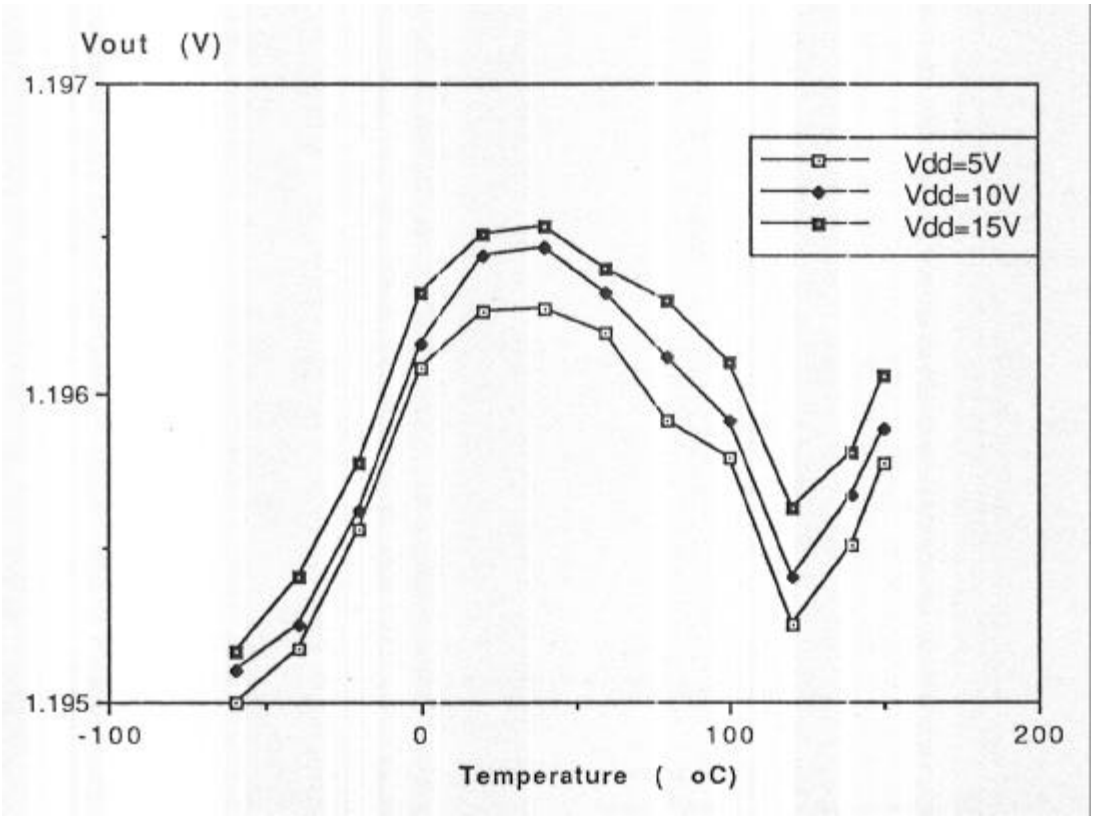
The variation of △Vsg versus MOS channel length in Type A BVR



The Spice simulated output voltages versus temperature in Type C BVR



The measured output voltages versus temperature in the fabricared cascaded-structure BVR(Type C)[3.5 ì m CMOS technology , R_1=1KÙ(external),R_2=25.9KÙ(external)]



* Average temperature drift

  5.5 ppm/^{o}C -60 ^{o}C ~ +150 ^{o}C

  5V~15V

* At 25 ^{o}C, average voltage drift 25ì V/V

  Vout=1.1963V ~ 1.1965V

  5V ~ 15V

* 2 mil^2 , 0.8 mW at 5V

§10-5 CMOS Bandgap Reference with Sub-1-V Operation

Ref.: IEEE JSSC, vol.34, pp.670~674, May 1999

Concept: * Convertional BGR $V_{ref} = 1.25V$

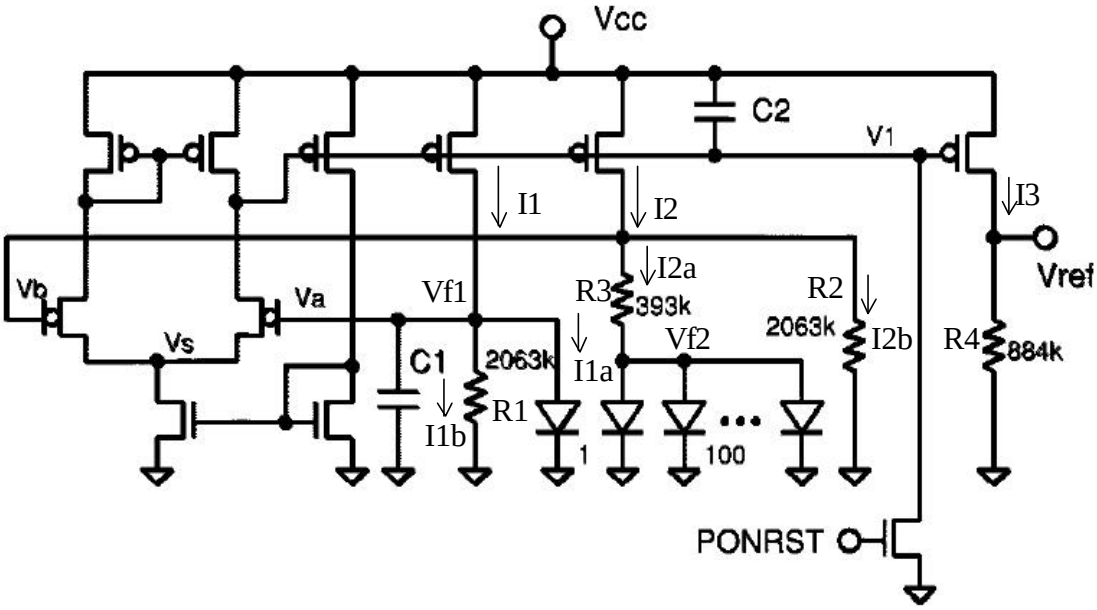
Can' t be operated below 1V supply.

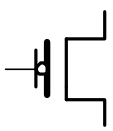
* The built-in voltage V_f of the diode $\rightarrow$ the current I_{2b}

The thermal voltage V_{therm} $\rightarrow$ the current I_{2a}

$(I_{2a} + I_{2b})R \rightarrow V_{ref} < 1V$

1.Schematic of the proposed BGR



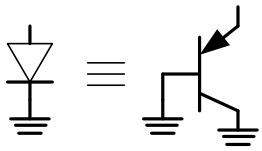


Native NMOS $V_{THI} = -0.2V$

NMOS $V_{THN} = +0.7V$

PMOS $V_{THP} = -1.0V$

*The diode is realized by the parasitic $P^+ / n-well / P-substract$ BJT as



*C_1 and C_2 are used to stabilized the circuit.

*The control signal PONRST is used to initialize the BGR circuit when the power is turned on.

* $R_1 = R_2$

$V_a = V_b$

$I_1 = I_2 = I_3$ and $I_{1a} = I_{2a}$, $I_{1b} = I_{2b}$

$dV_f = V_{f1} - V_{f2} = V_{therm} \ln(N)$, $N = 100$

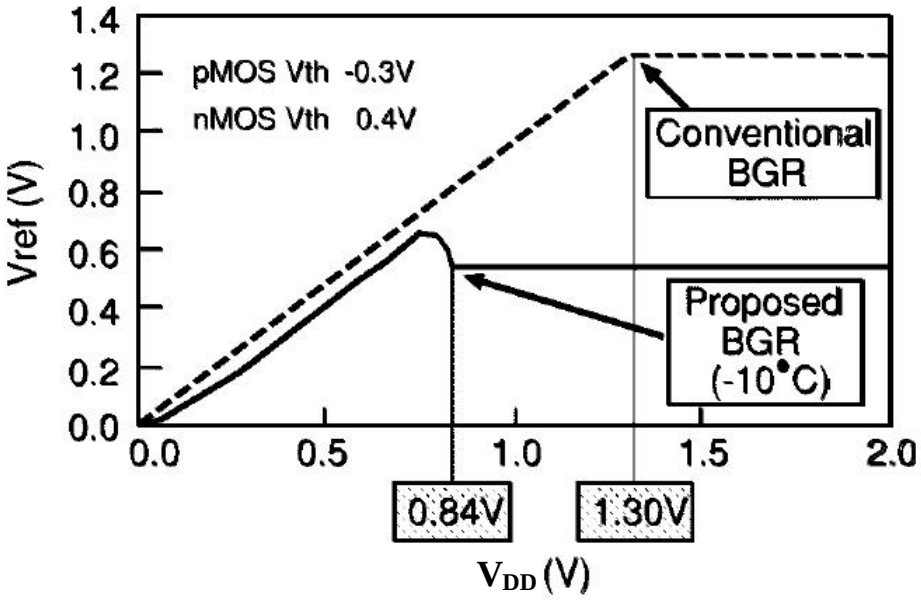
$$I_{2a} = \frac{dV_f}{R_3} \propto V_{therm}$$

$$I_{2b} = \frac{V_{f1}}{R_2} \propto V_f$$

$$I_3 = I_2 = I_{2a} + I_{2b}$$

$$V_{ref} = R_4 I_3 = \frac{R_4}{R_2} V_{f1} + \frac{R_4}{R_3} dV_f$$

2. Simulated V_{ref} characteristics



*$V_{ref} = 1.25V$ conventional BGR

*$V_{ref} = 0.84V$ proposed BGR

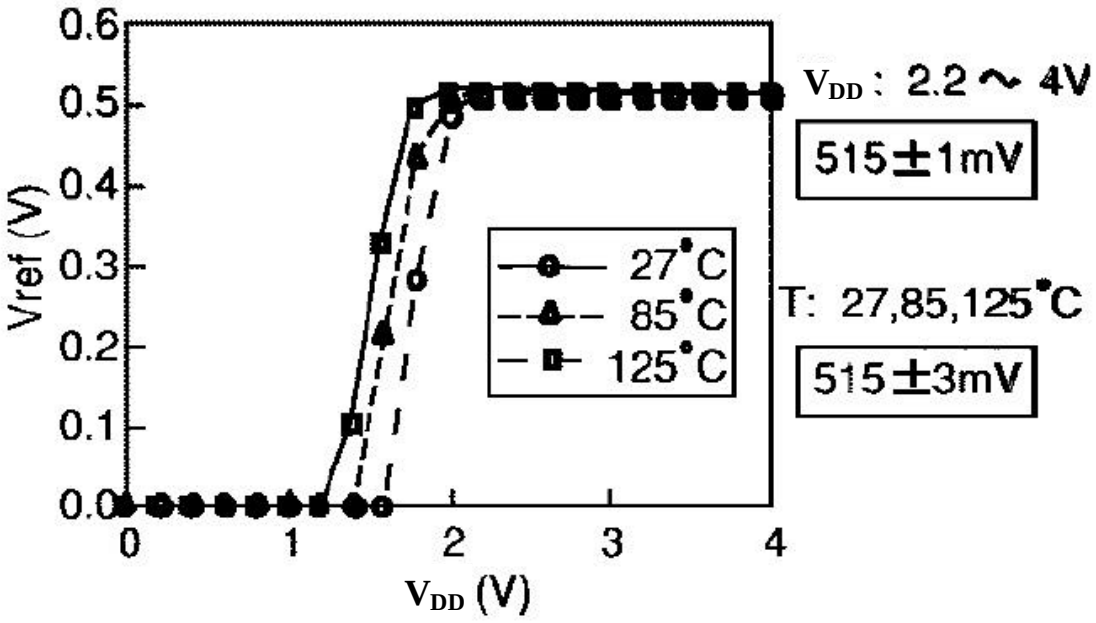
3.Minimum V_{DD}

$$\min\ V_1 \cong V_s \cong V_b - V_{THI} \cong V_f + |V_{THI}| \cong V_{DD} + V_{THP} = \min V_{DD} - |V_{THP}|$$

$$\Rightarrow \min V_{DD} = V_f + |V_{THI}| + |V_{THP}| \cong 0.8 \sim 1.0V$$

0.54 -0.2 -0.3

4.Measured results:



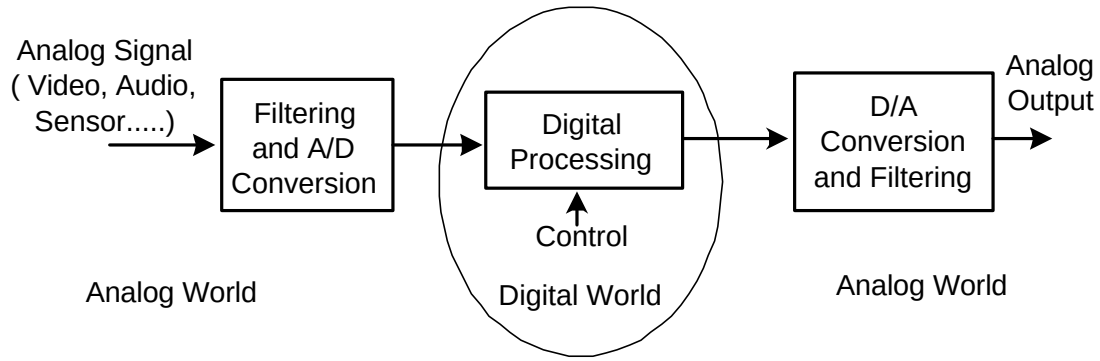
*$TC \cong 60\,ppm/^{O}C$ $27^{O} \sim 125^{O}C$

Voltage drift (average) $\cong 600mV/V$ 2.2V~4V

CH 11 Digital-to-Analog Converters (DACs) in CMOS Technology

§11-1 Introduction

1. Block diagram



(Digital signal processing has better noise immunity than analog signal processing.)

Fig. 11.1 A block diagram of a typical signal processing system

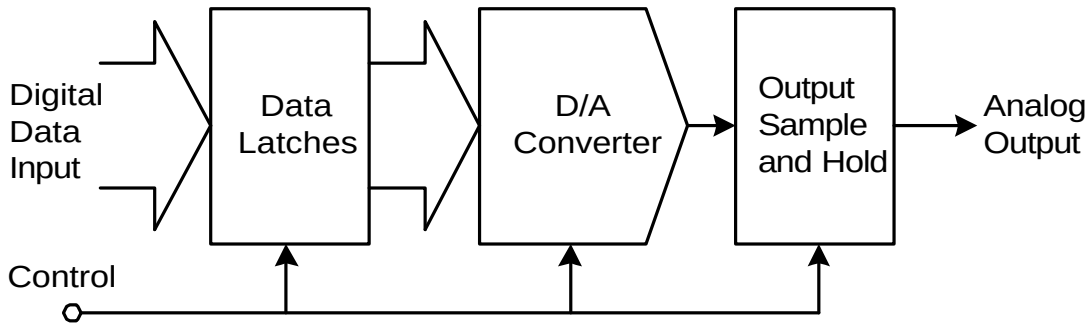


Fig. 11.2 Functional block diagram of a D/A converte

2. Ideal DAC:

Analog output signal $V_{out} = V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \text{----} + b_N 2^{-N})$

V_{ref}: analog reference signal

b_1 …… b_N : N-bit digital data input

The signal change when one LSB changes is V_{LSB}

$$V_{LSB} \equiv \frac{V_{ref}}{2^N}$$

If in LSB unit, 1LSB= $\frac{1}{2^N}$

3. DAC performance specifications

(1) Resolution: The number of distinct analog levels corresponding to the different digital words.

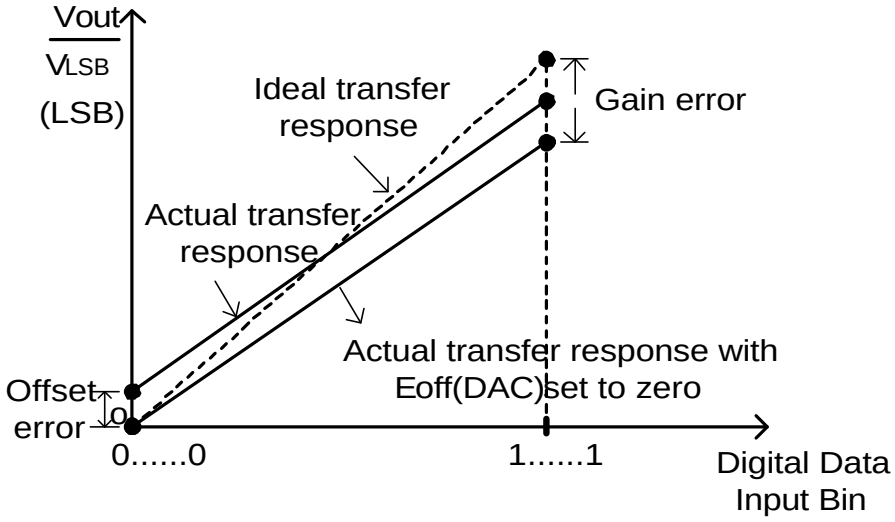
N-bit resolution $\rightarrow$ 2^Ndistinct analog levels.

(2) Offset error:

$$E_{off\,(DAC)} \equiv \frac{V_{out}}{V_{LSB}}\Big|_{0....0} \quad (\text{LSB})$$

(3) Gain error:

$$E_{gain\,(DAC)} \equiv [\frac{V_{out}}{V_{LSB}}\Big|_{1....1} - \frac{V_{out}}{V_{LSB}}\Big|_{0.....0}] - (2^N - 1) \qquad (\text{LSB})$$



(4) Accuracy

absolute accuracy: The difference between the expected and actual transfer response. It includes the offset, gain, and linearity errors.

relative accuracy: The accuracy after the offset and gain errors have been removed.

$\Rightarrow$ maximum integrated nonlinearity (INL) error

*Accuracy units: ・% of full-scale value.

・ effective number of bits

・ fraction of an LSB

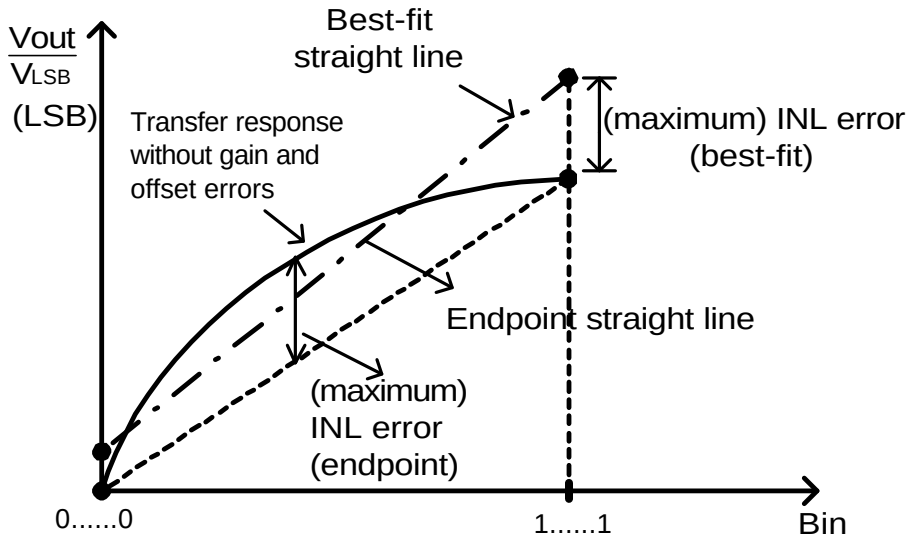
*12-bit accuracy $\Rightarrow$ all errors $<$ 1 LSB ($\frac{V_{out}}{2^{12}}$)

(5) Integral nonlinearity (INL) error

Definition: The deviation of actual transfer response from a straight line.

INL error (best-fit) and INL error (endpoint)

Usually, INL error is referred to as the maximum INL error.



(6) Differential nonlinearity (DNL) error

Definition: The variation in analog step sizes away from 1 LSB.
(usually, gain and offset errors have been removed)

(7) Monotonicity: The output signal magnitude always increases as the input digital code increases.

* Maximum DNL error $<$ 0.5 LSB $\Rightarrow$ monotonicity
* Many monotonic DAC may have a maximum DNL error $>$ 0.5 LSB
* Maximum INL error $<$ 0.5 LSB $\Rightarrow$ monotonicity

(8) Settling time

The time it takes for the DAC to settle to within some specified amount of the final value (usually 0.5 LSB)

(9) Sampling rate

The rate at which sample can be continuously converted.
(Typically the sampling rate is equal to the inverse of the settling time)

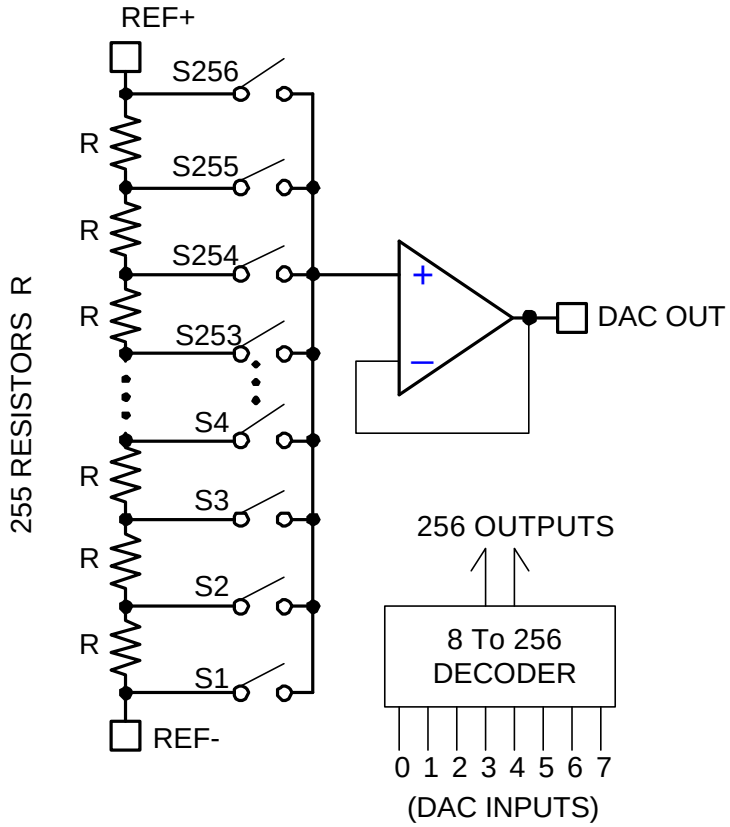
4. Types of DACs

(1) Decoder-based DAC
(2) Binary-weighted DAC
(3) Thermometer-code DAC
(4) Hybrid DAC
(5) Oversampling DAC

§11-2 Decoder-Based DAC

§11-2.1 Resistor-String DAC

1. Conceptual 8-bit resistor-string DAC.



2. Practical realization

R_0-R_{15}: To divide V_{REF}^+ to V_{REF}^- into 16 voltage intervals

H_0-H_{15}
L_0-L_{15}: To divide each of those intervals into 16

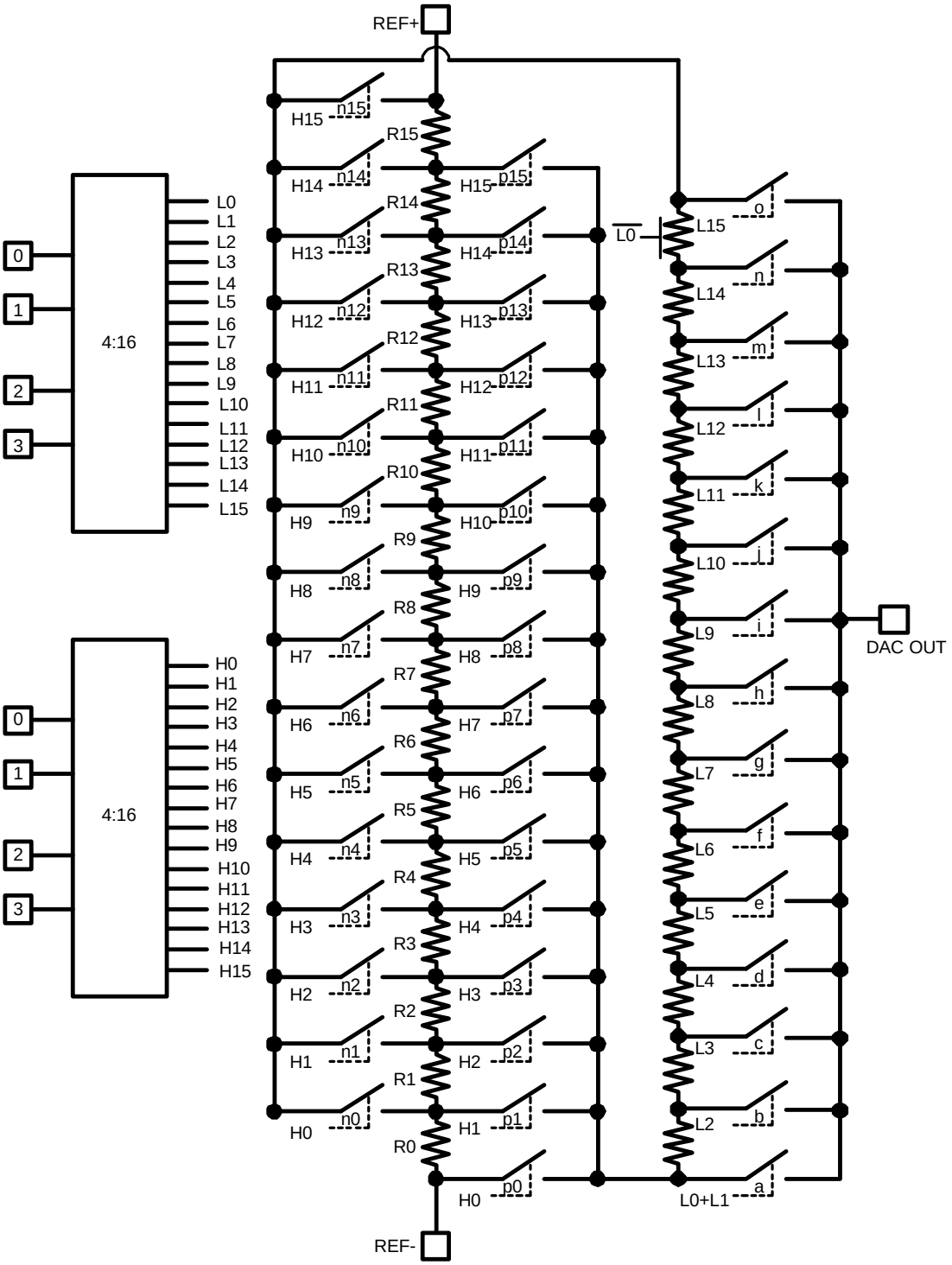
a - p subintervals

* To insure maximum uniformity of step size, i.e. linearity, the resistance of the transmission gates should be made as large as possible $\Rightarrow$ minimal loading.

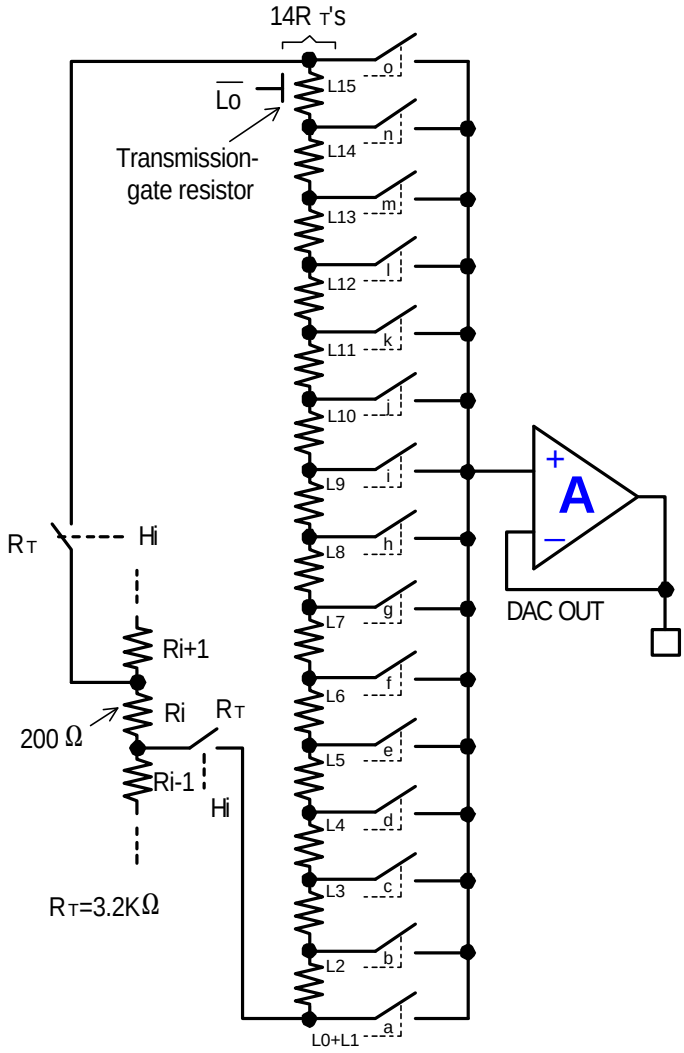
* For 8-bit DAC, the error due to loading can be held to less than 1 LSB.

if $16R_T > 2^N R_i$ ($R_i = 200\Omega$, $R_T > 3.2K\Omega$)

8-bit Resistor-String DAC (Multiple Resistor-String DAC)



Subinterval Generation:



* Transmission gate size: $24m/12m \rightarrow 3.2k\Omega = R_T$

* The raw speed of the DAC is limited by the resistance of transmission gates a-p and the capacitance of the output node, also by the operating speed of the output buffer.

* V_{DD} = +5V, $-V_{SS}$ = -5V, Vout : ±2.5V

  Maximum conversion rate 0 → full scale : 2.5MHz.

* For 8-bit DAC, the jump in step size can be held to less than 1 LSB if

  $16R_T \geq 2^N R_i$. $\quad \frac{\Delta R_i}{R_i} = \frac{R_i - \frac{16R_T R_i}{R_i + 16R_T}}{R_i} = \frac{R_i}{R_i + 16R_T} \leq \frac{1}{2^N}$

  $\Rightarrow 2^N R_i \leq 16R_T$ occurs when L_1=1

§11-2.2 Folded Multiple Resistor-String DAC

ISSCC 90 / FRIDAY, FEBRUARY 16, 1990 / CONTINENTAL BALLROOM 5-9 / 9:30 A.M.

FAM 12.2: A 50MHz 10-bit CMOS Digital-to-Analog Converter with 75Ω Buffer

Marcel Pelgrom
Philips Research Laboratories
Eindhoven, Netherlands

HIGH-SPEED DIGITAL-TO-ANALOG converters are usually designed with a current cell matrix. For resolutions higher than 8 bits required for new television standards, this approach requires either selection, trimming or calibration in the case of binary decoding, or accurate glitch matching and gradient compensation in CMOS if thermometer decoding is used[1,2]. Moreover, many current-cell based circuits dump on average half of the current and often require the virtual ground of an external amplifier for optimum linearity with sufficent output drive.

This trimless 10-bit 50MHz D/A converter is based on resistor strings. The voltage dependence and the mutual matching of large-area polysilicon resistors allow the design of a converter with high integral and differential linearity. However, in a single 1024-tap resistor ladder output settling requires such low tap resistors that accurate resistor matching and consequently linearity becomes a problem.

The solution to this problem is the combination of a dual ladder with a matrix organization for the fine ladder, a full decoding scheme, an on-chip 75Ω output buffer and an additional ladder for the reduction of distortion at high signal frequencies[3]. Figure 1 shows the ladder structure: the coarse ladder consists of two ladders each with 16 large-area 250Ω resistors connected anti-parallel to eliminate the first-order resistivity gradient. The coarse ladder determines 16 accurate tap voltages. A 1024-resistor fine ladder is arranged in a 32-by-32 matrix, where every 64th tap is connected to the coarse ladder taps. There are currents in the connections between the ladders only in the case of ladder inequalities. This reduces the effect of contact resistance variance. The current density in the polysilicon is kept constant to avoid field-dependent non-linearities. In operation, the tap voltages of the fine ladder are switched to the 16 output rails of the matrix. The digital input word is decoded by two sets of 5-to-32 decoders followed by two groups of latches, as shown in Figure 2. At every tap an AND gate performs the final decoding. In each transition one switch connects the ladder to the output rails, while another switch disconnects. This scheme minimizes ladder bounce caused by the switches, often observed in schemes where MSB decoding is combined with output rail multiplexing[4].

As the ladder of the D/A converter is designed for 2V unloaded output swing, second-order distortion will occur at high signal frequencies, due to the input-code-dependent switch-drive voltage which causes signal-dependent RC time constants on the output rails. In this circuit, the drive voltage is kept constant by feeding the final AND decoding gates from an additional ladder: (Figures 1, 2). The total ladder configuration can now be fed from the 5V analog power supply. One external capacitor decouples the signal ladders. The clock-feedthrough of the switches gives a linear signal contribution.

The multiplex circuit at the end of the 16 output rails connects only the active rail to the output, keeping the other rails at the corresponding middle tap voltage. This scheme reduces the load capacitance and minimizes the recharging of the matrix output lines.

The output buffer is a folded-cascode op amp where the output load is part of the output stage. The on-chip stop resistor allows a feedback path even for frequencies where the bondpad capacitance shorts the circuit output. The measured open-loop gain of the op amp into a 75Ω and 25pF load is 43dB with a unity gain bandwidth (UGBW) of 75MHz. (Figure 3).

Figures 4 and 5 show examples of performance with 75Ω and 25pF load. The lower side of the ladder is connected to give 0.1 volt minimum output voltage. The overall dc integral linearity curve is shown in Figure 4. The integral linearity was verified by measuring the distortion of low-frequency input signals. The total distortion is less than –60dB.

The 10%-to-90% transition time is 6ns. (Figure 5) The extrapolated settling to within one LSB is about 20ns. The most critical glitch energy occurs for codes where the position is switched from the coarse ladder tap to the 32nd position on the corresponding fine ladder; in code: xxxxx00000 to xxxxx11111. The difference in glitch area is lower than 100psV.

The D/A converter has been tested on computer-synthesized video pictures. Interference tests (9.6MHz input, at 27MHz clock) confirms the linearity specifications. The effect of the additional supply ladder has been measured at 4.433MHz signal frequency and 50MHz clock rate. After the supply ladder is disconnected from the signal ladder and connected to the positive power supply, the total distortion increases by 10dB. At 50MHz clock rate, 125°C and a 13MHz signal frequency the distortion increases to –40dB due to slew-rate limitations. Full-scale transitions have been measured up to a clock frequency of 100MHz, which shows the inherent speed of the ladder network.

Table 1 summarizes the performance. Power dissipation is measured with a full sinewave output signal, which consequently requires half of the top output current. Figure 6 shows a micrograph of the test chip.

---

[1] Schoeff J.A., "An Inherently Monotonic 12-bit DAC", *IEEE J. Solid-State Circuits*, Vol. SC-14, p. 904-911; Dec., 1979.

[2] Miki, T., et al., "An 80MHz 8-bit CMOS D/A Converter", *IEEE J. Solid-State Circuits*, Vol. SC-21, p. 983-988; Dec., 1986.

[3] Dingwall, A.G.F. and Zazzu, V., "An 8MHz CMOS Subranging 8-bit A/D Converter", *IEEE J. Solid-State Circuits*, Vol. SC-20, p. 1138-1143; Dec., 1985.

[4] Abrial, A., et al., "A 27MHz D/A Video Processor", *IEEE J. Solid-State Circuits*, Vol. SC-23, p. 1358-1369; Dec., 1988.

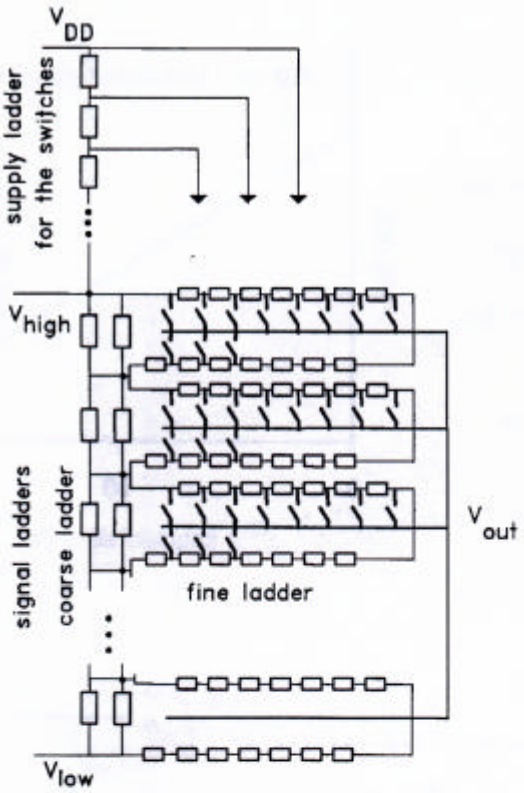


FIGURE 1—Resistor network for the video D/A.

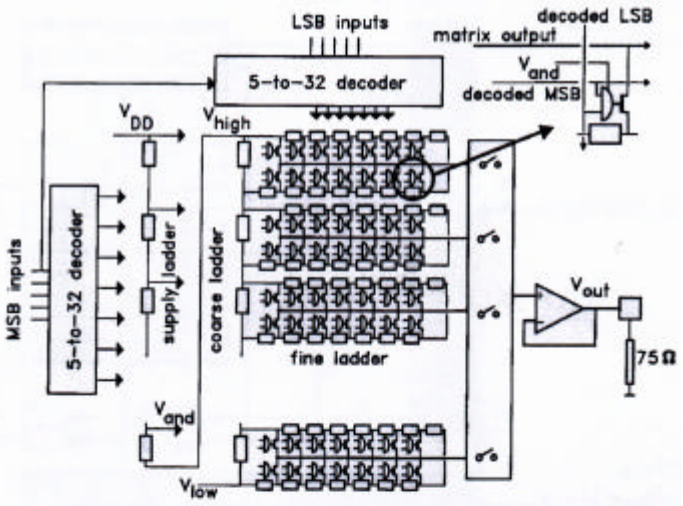
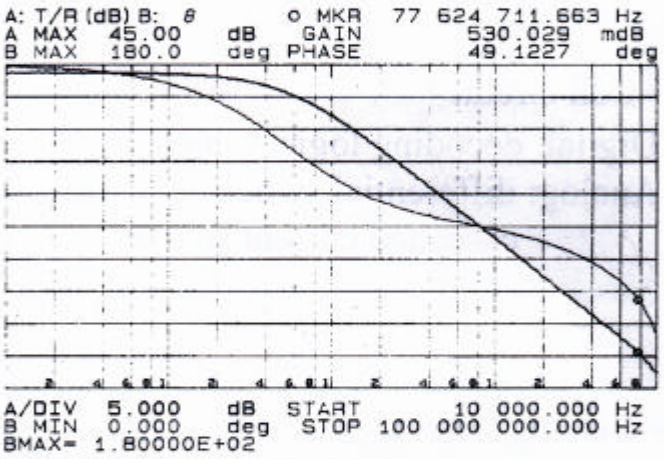


FIGURE 2—Block diagram of the D/A converter.



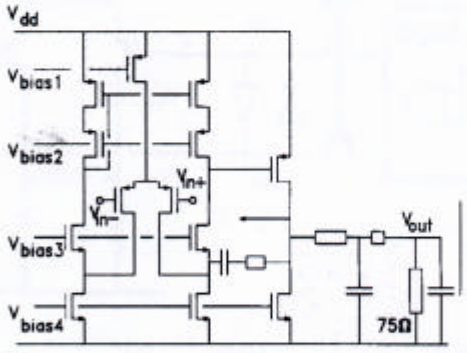


FIGURE 3—(*a*) folded cascode op amp circuit used for the buffer; (*b*) measured open-loop gain and phase on a 75Ω and 25pF load.

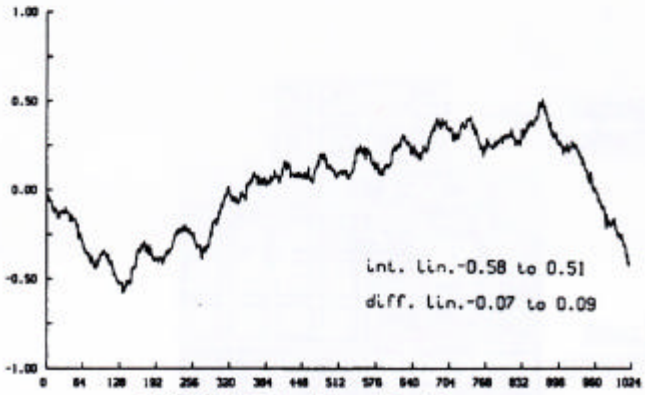


FIGURE 4—Integral linearity plot.

Process	1.6μm CMOS
DC resolution	10-bit
Differential linearity error	<0.1 LSB
Integral linearity error	±0.6 LSB
Glitch energy	100psV
Settling time (1 LSB)	20ns
Rise/Fall time (10%-90%)	6ns
Sample frequency	50MHz
Nominal power supply	5V
Output in 75Ω	1V
Power consumption (50MHz, 75Ω)	85mW
DAC size	2.5mm²

TABLE 1—Summary.

FIGURE 5, 6 — *See page 295*

(Continued from page 201)

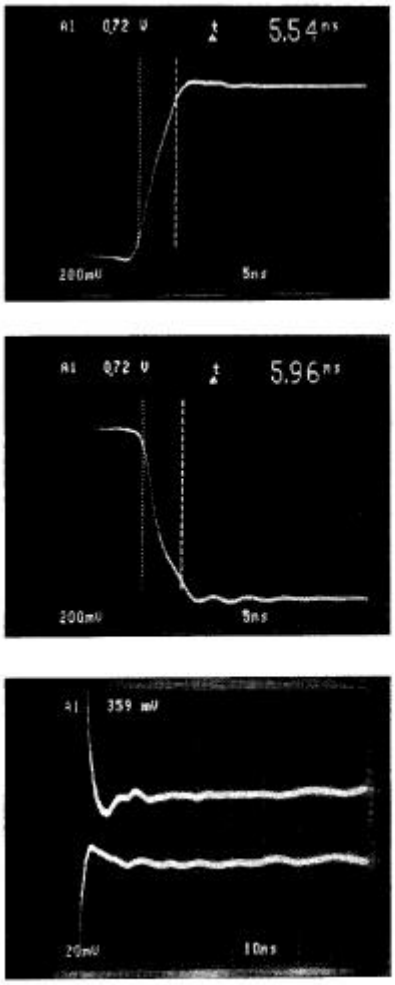


FIGURE 5—Photographs of the full-scale settling of the output.

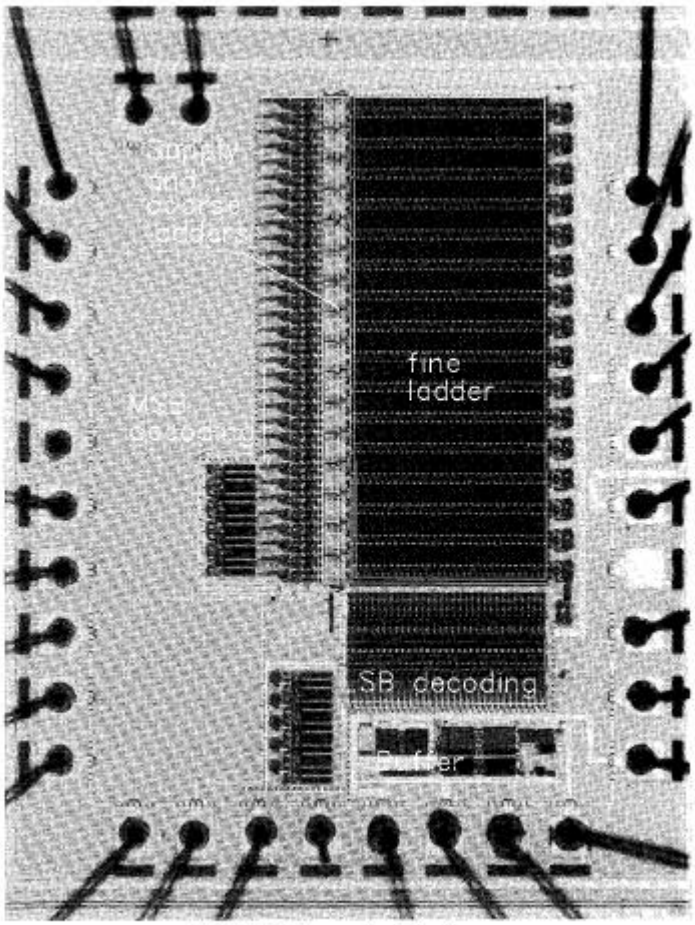
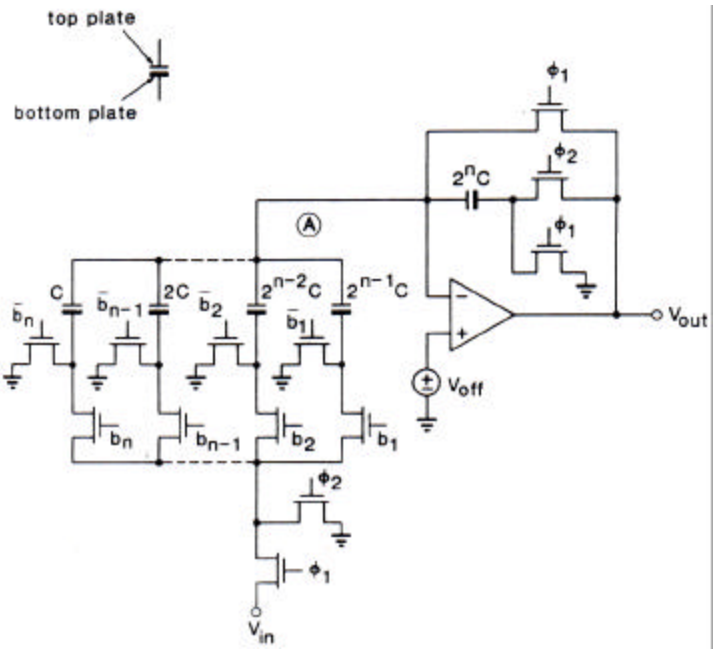


FIGURE 6—Micrograph of the die.

§11-3 Binary-Weighted DAC

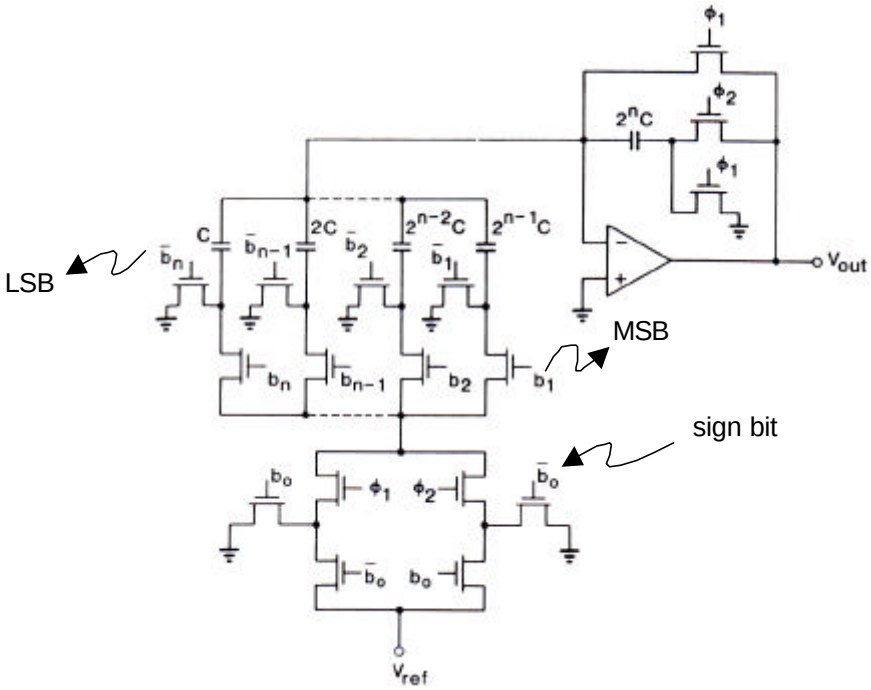
§11-3.1 Charge-Redistribution DAC

1. Multiplying DAC



* All top plates are connected to the OP AMP input
  ⇒ To reduce substrate noise voltage injection.
* Switched-induced errors are large.
* offset cancellation

2. Multiplying DAC with bipolar input



If bo = 0 ⇒ the signal Vin is positive
⇒ the same as 1.

If $b_0 = 1$ $\Rightarrow$ the signal Vin is negative.

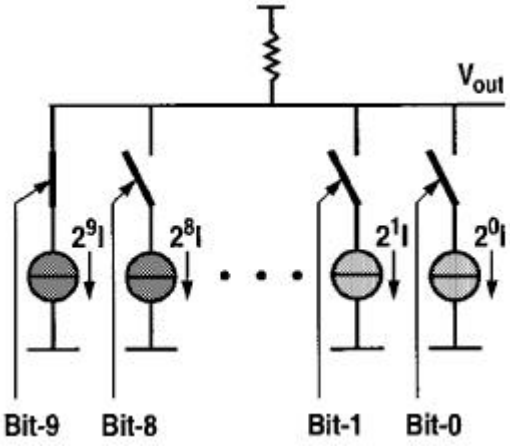
f_1, f_2 positions are exchanged.

$$\text{Vout} = -\text{Vin} \sum_{i=1}^{n} bi2^{-i}$$

3. General characteristics or features of charge-redistribution DAC:
   (1) The auto-calibration cycle can be performed to remove the effects of component ratio errors.
   (2) Good linearity and stability due to good linear capacitors.
   (3) Too large capacitance ratio is required for high-bit DAC.
   (4) Suitable for medium-speed DAC with 6-bit resolution or below.

§11-3.2 Weighted-Current-Source DAC (Current-Mode Binary-Weighted DAC)

Conceptual circuit:

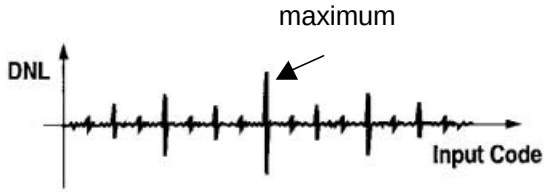


1. Conventional structure

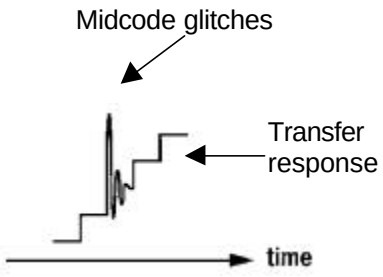
   * Simple circuit structure without decoding logic.

   * At the mid-code transition 011---1→ 10---0, the MSB current source needs to be matched to the sum of all the other current sources to within 0.5 LSB.
     $\Rightarrow$ difficult for large bit number.
     $\Rightarrow$ not guaranteed monotonic.

   * Low-accuracy matching causes inaccurate bit transition
     $\Rightarrow$ typical DNL plot as shown →

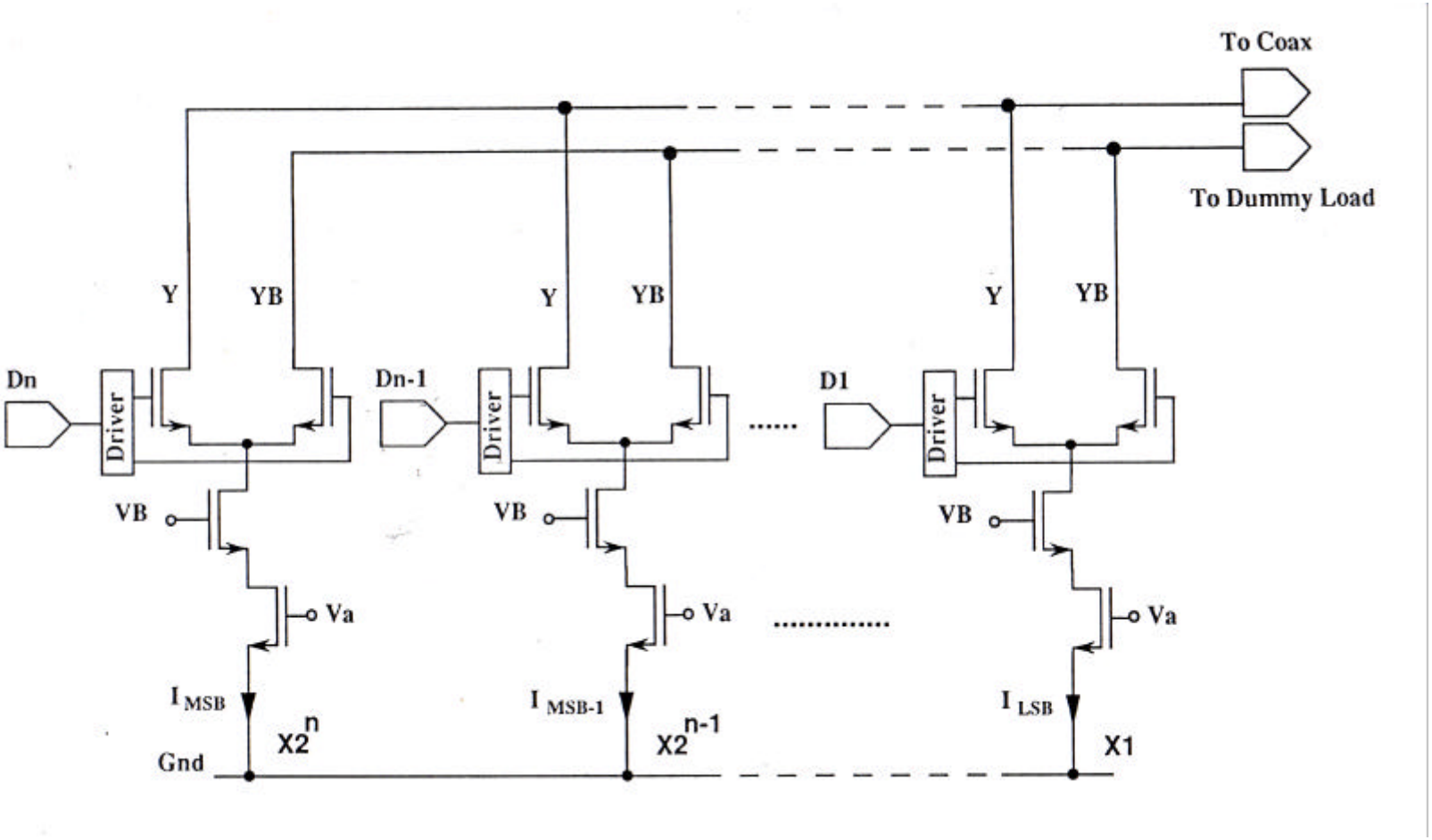


   * The errors caused by the dynamic behavior of the switches, such as charge injection and clock feedthrough, result in glitches which is most severe at the midcode transition, as all switches are switching simultaneously.
     $\Rightarrow$ contains highly nonlinear signal components
     $\Rightarrow$ manifest itself as spurs in the frequency domain.



Reference: IEEE Journal of Solid-State Circuits, vol.33, pp.1948-1958, Dec.1998.

Conventional Weighted-Current-Source D/A Converter



The Proposed 10-bit D/A Converter

Reference: IEEE JSSC, PP.635-639, June 1989.

1. Using Two-Stage Architecture:

   32 master & 32 slave current sources

   (Occupied small chip area but cause tight matching requirement among master current sources.)

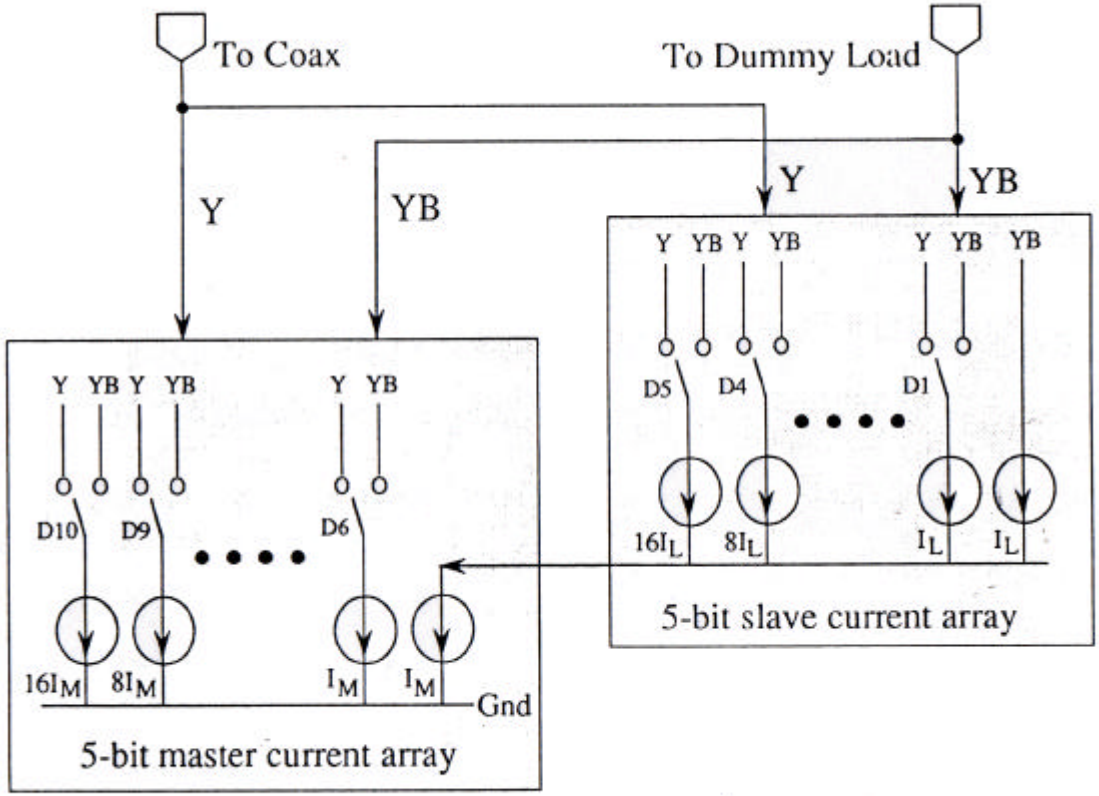
2. Using Threshold-Voltage Compensated Current Sources

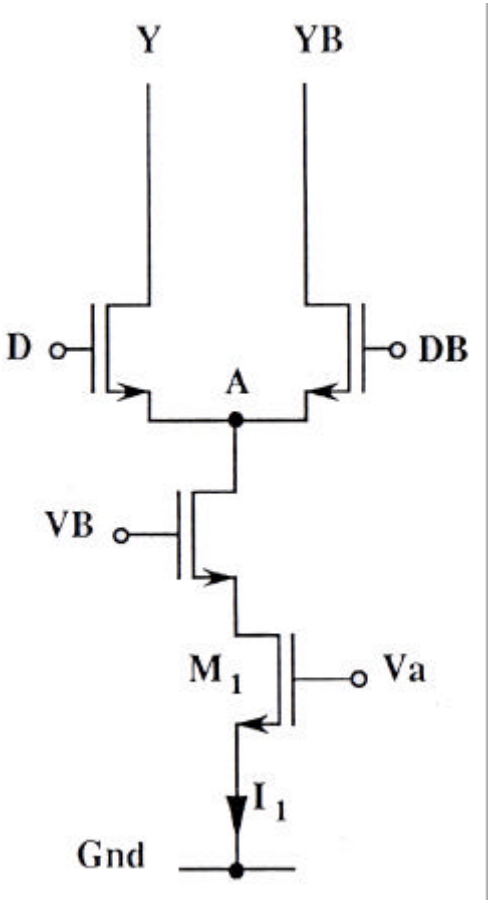
   to satisify tight matching requirement.

   Only need local match &

   do not need global match.

Two-Stage Weighted Current Array D/A Converter



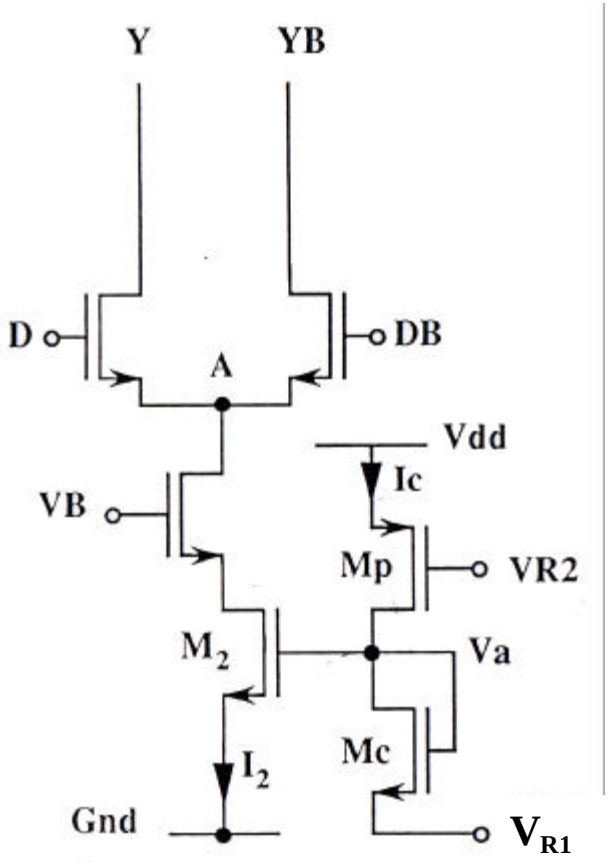


$I_1 = K\,(W/L)(Va\text{-}Vth_1)^2$

$I_N = K\,(W/L)(Va\text{-}Vth_N)^2$

$(Vth_N\text{-}Vth_1)$ may be as large as 80 mV due to the oxide thinning effect.

Conventional switched current source.

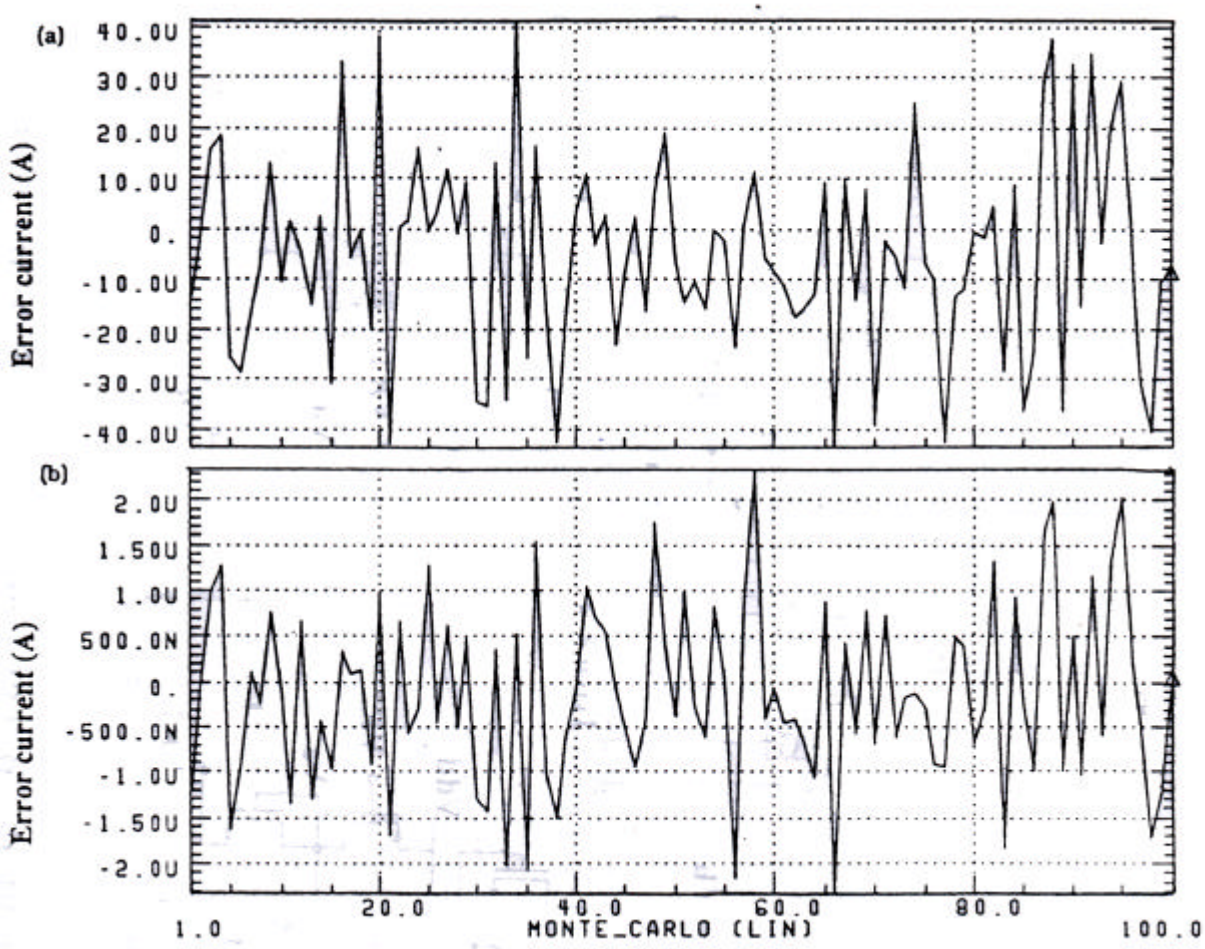


$$I_2 = K\frac{W}{L}(Va - Vth_2)^2$$
$$= K\frac{W}{L}(V_{R1} + Vth_c - Vth_2 + \sqrt{\frac{LcIc}{KWc}})^2$$

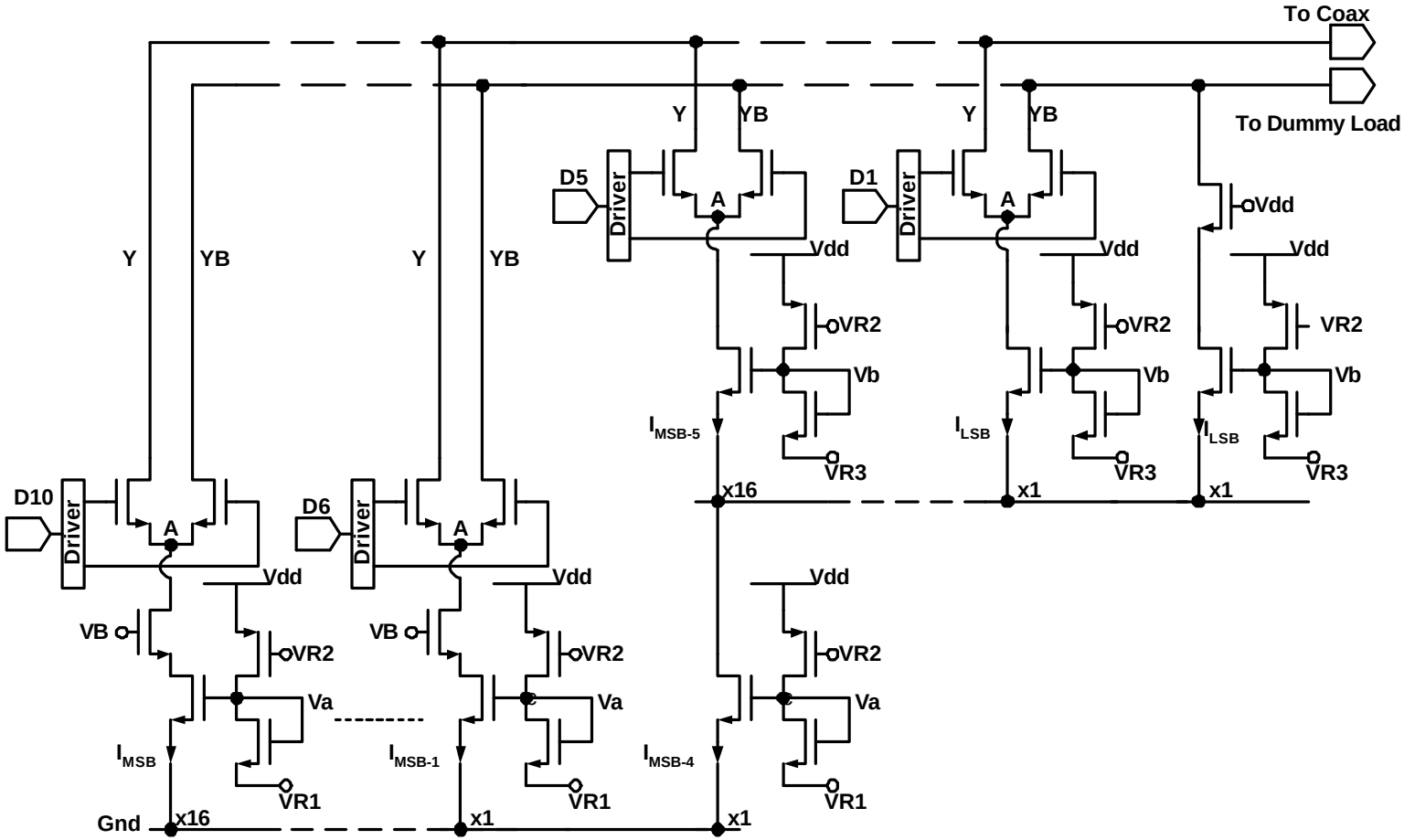
1. $I_2 >> I_C$
2. M_2 and M_C are locally matched

$$\Rightarrow I_2 \cong K\frac{W}{L}V_{R1}$$

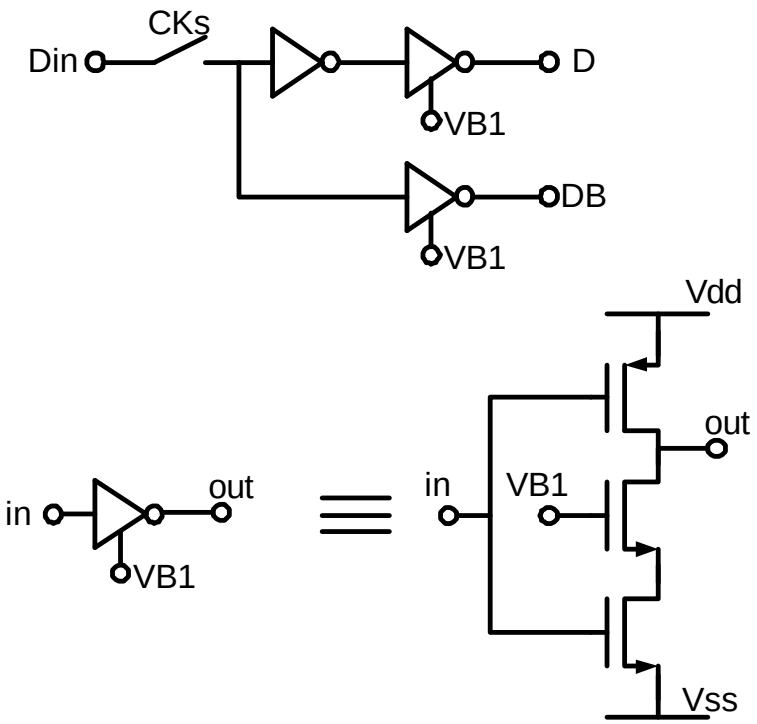
Switched current source with threshold-voltage compensation.



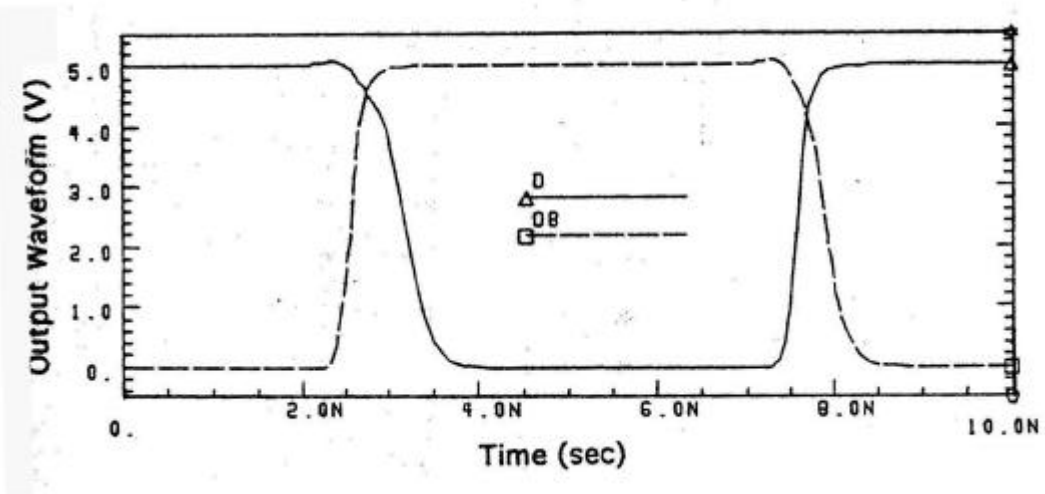
Spice Monte-Carlo simulation results for (a) Conventional weighted current sources; (b) current sources with threshold-voltage compensation.



Two-stage weighted-current-source D/A converter with threshold-voltage compensated current sources.

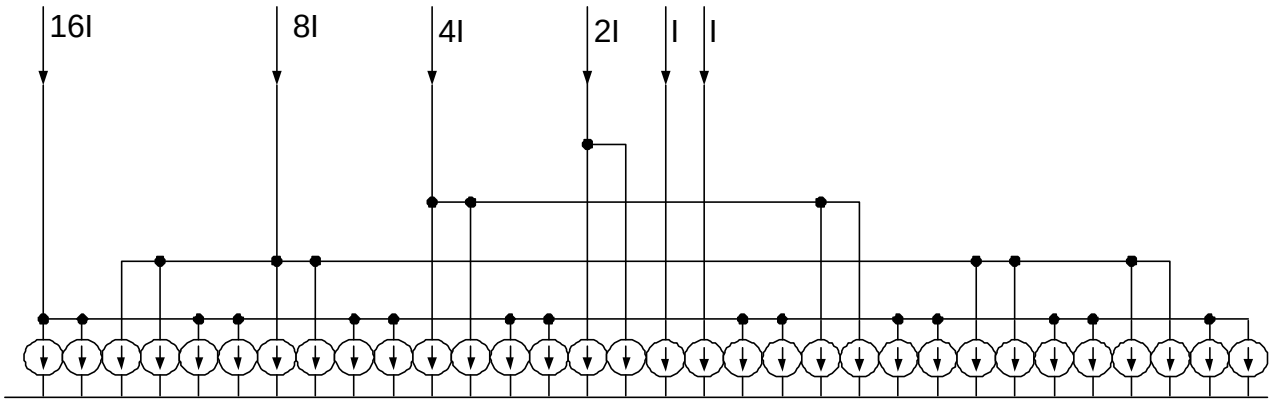


(a)

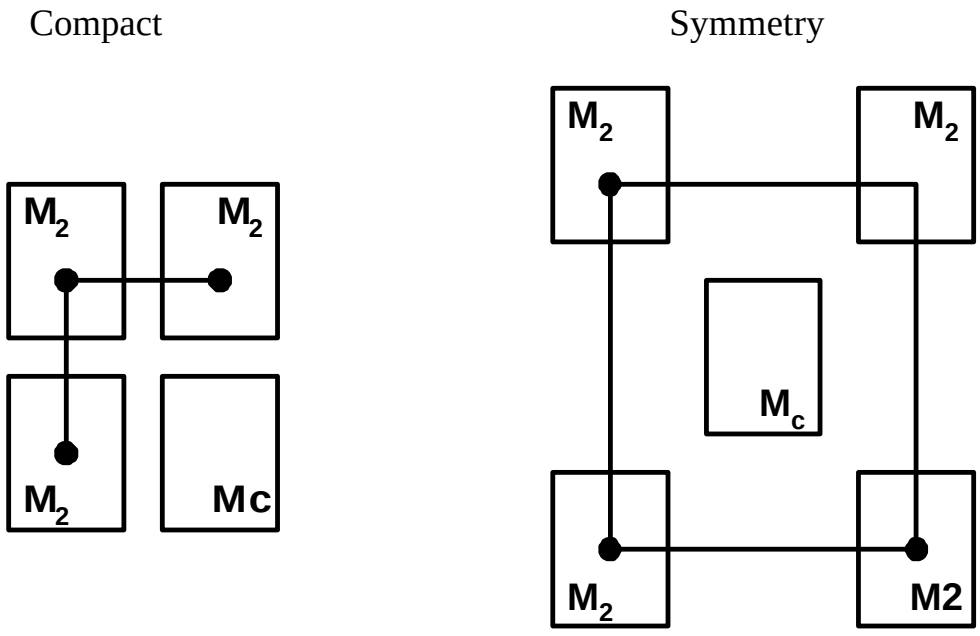


(b)

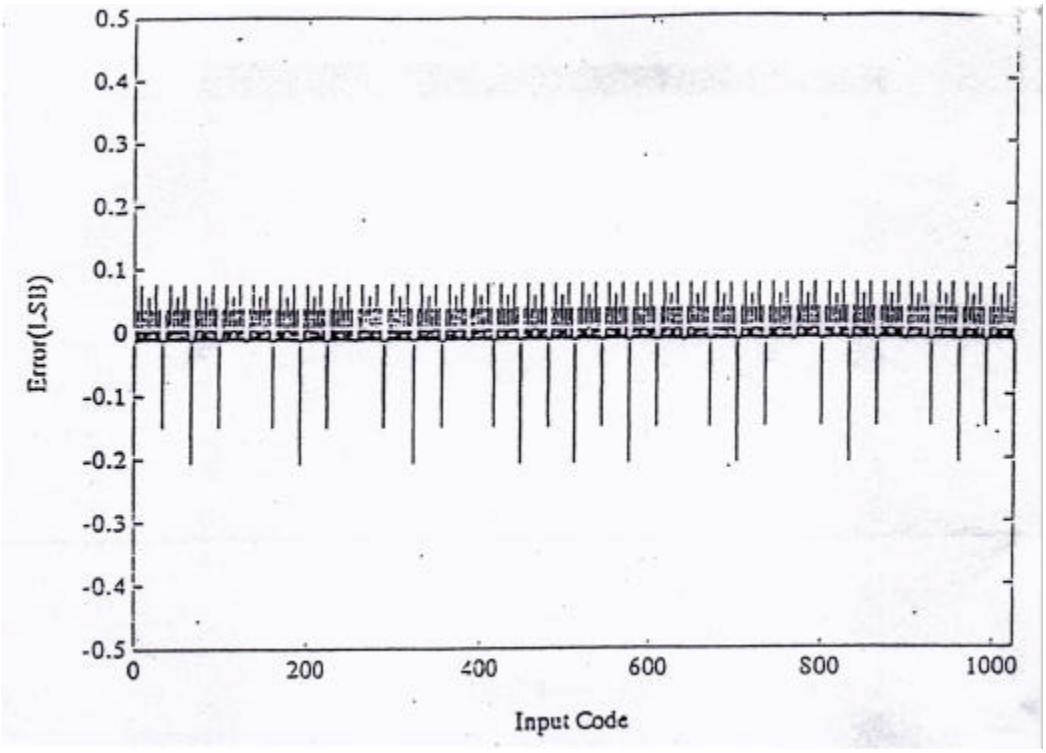
(a) The circuit; (b) The SPICE simulated output waveforms of the input driver with high logic-threshold.

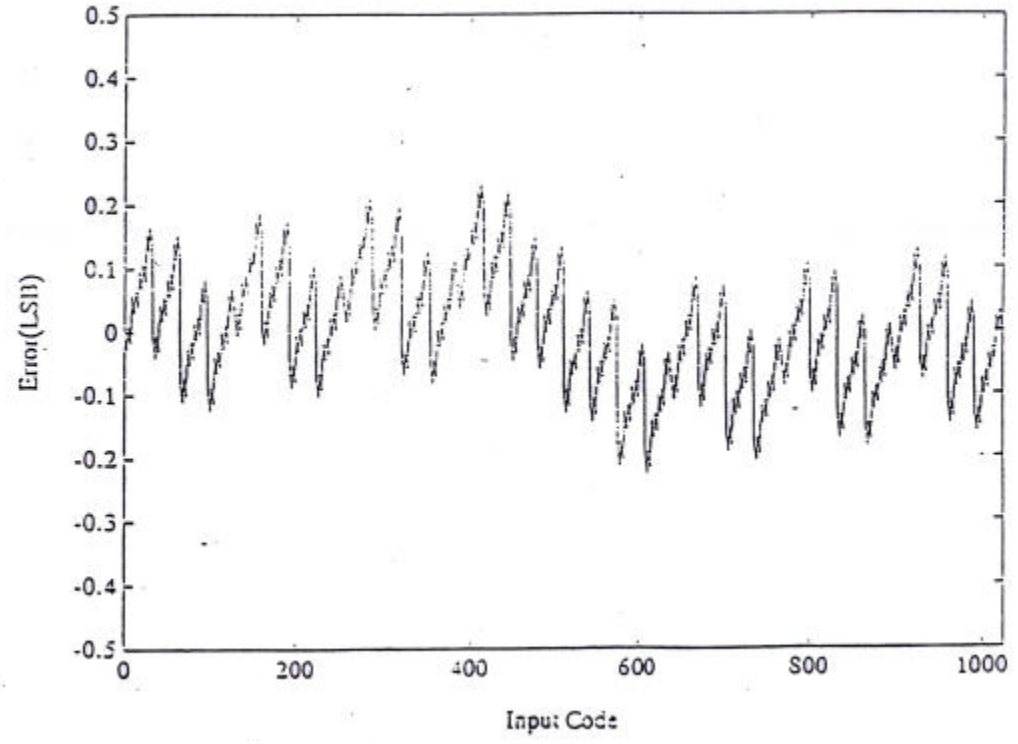


Symmetrical layout configuration of each 5-bit current array.



Different layout arrangement for the devices M2 and Mc in each current source: (a) 4-cell unit; (b) 5-cell unit.





Differential linearity error of the D/A converter
Integral linearity error of the D/A converter.

Differential and Integral linearity distribution of two kinds of layout methods for each current source.

Linearity Error	4-Cell Unit(%)	5-Cell Unit(%)
＜1/2 LSB	28.6	21.4
＜1 LSB	82.1	67.9
＜2 LSB	93.9	89.3

Characteristics of the D/A converter.

Resolution	10 bits
Differential Nonlinearity	0.21 LSB
Integral Nonlinearity	0.23 LSB
Conversion rate	125 MS/s
Settling Time (±1/2 LSB)	＜ 8 ns
Rise/Fall time (10-90%)	3 ns
Glitch Energy	40 psV
Power Dissipation	150 mWatts
Supply Voltage	5V
Process	0.8um CMOS
Chip Size (without pads)	1.8mm×1.0mm

SUMMARY

1. Using threshold-voltage compensated current sources.
2. Two-step weighted current array 32 *master, 32 slave unit current sources.*
3. 10 bits, 125MHz, INL＜±0.21 LSB, DNL＜±0.23 LSB, 150mW.
4. Few analog components & good performance.

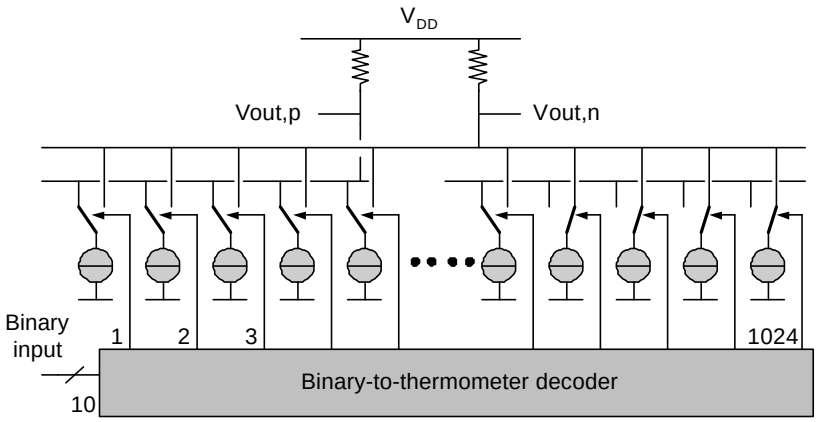
§11-4 Thermometer-Code DAC

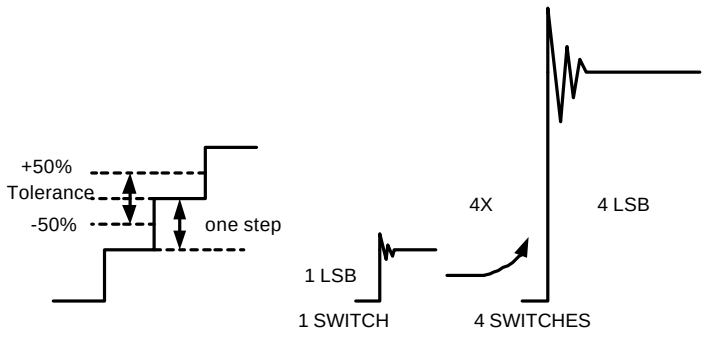
Current-mode thermometer-coded DAC; Current-cell-matrix DAC

1. Thermometer code (3 bit)

b_2	b_1	b_0		d_6	d_5	d_4	d_3	d_2	d_1	d_0
0	0	0	→	0	0	0	0	0	0	0
0	0	1	→	0	0	0	0	0	0	1
0	1	0	→	0	0	0	0	0	1	1
	.						.			
	.						.			
1	1	0	→	0	1	1	1	1	1	1
1	1	1	→	1	1	1	1	1	1	1

2. Conceptual circuit of thermometer-coded DAC





Advantages:

(1) Monotonicity is guaranteed.
(2) The matching requirement is much relaxed.
e.g. 50% matching→DNL＜0.5 LSB
(3) At the midcode transition the glitch is greatly reduced.
∵ only 1 LSB current source is switched.

(4) Glitches do not contribute much to nonlinearity.

Glitches $\propto$ switched LSB

$\Rightarrow$ Glitch/LSB $\cong$ constant

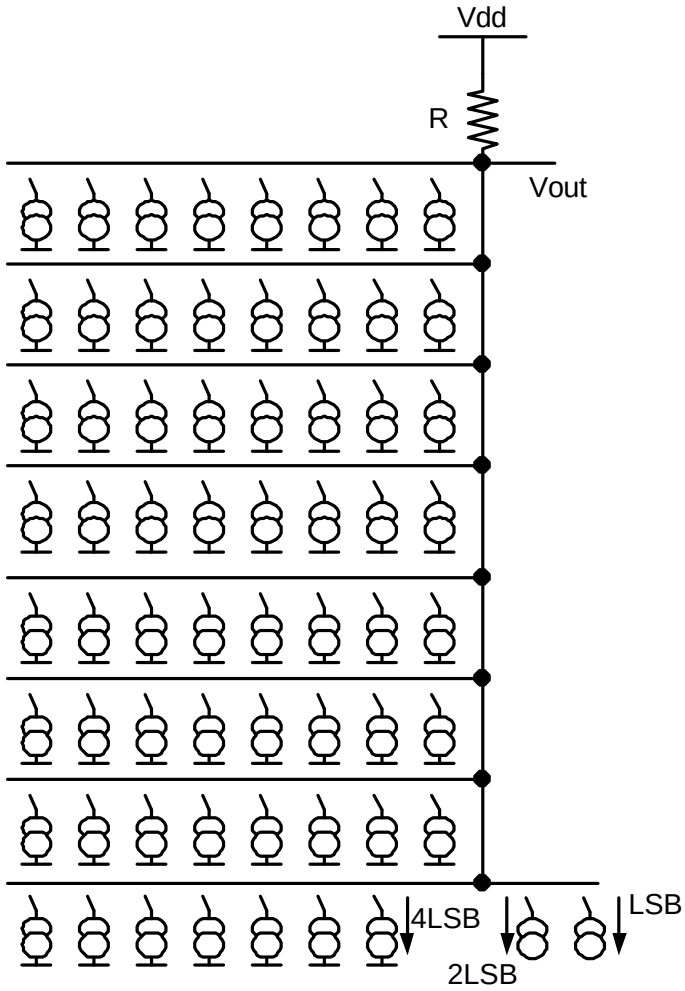
$\Rightarrow$ Good linearity.

Disadvantage: Area consuming

$\because$ Every LSB needs a current source, a switch, a decoding circuit, and the binary to thermometer decoder.

3. 8-bit current-mode thermometer-coded DAC

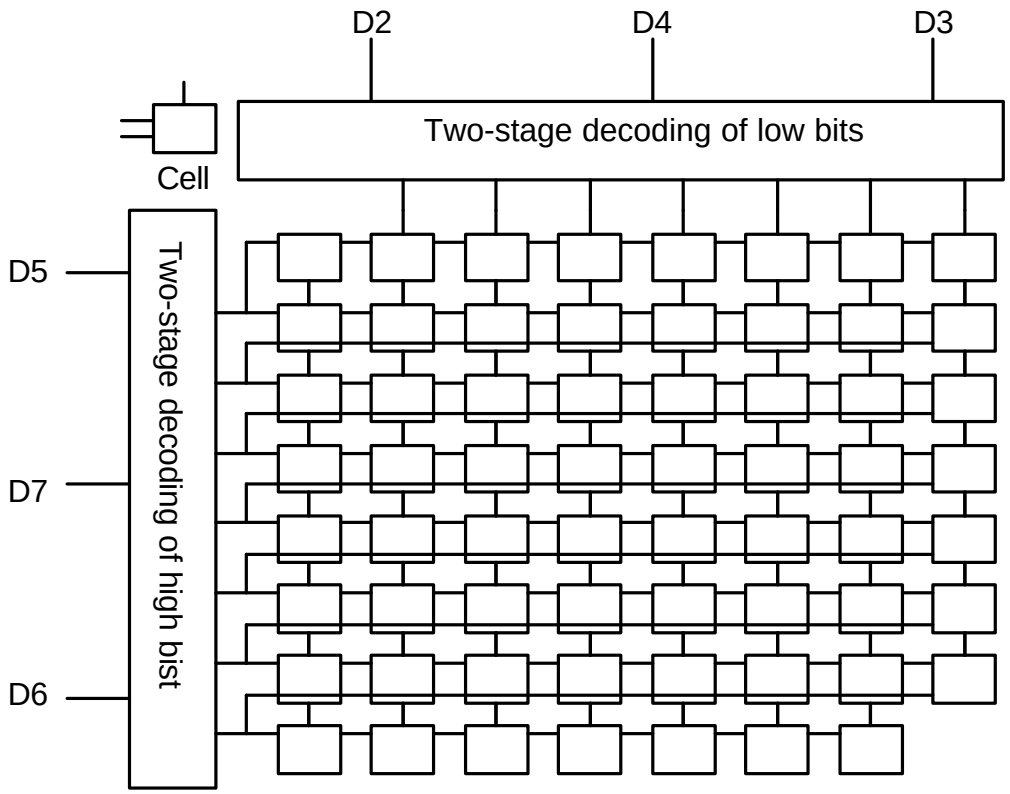
· Conceptual architecture



* The two LSB bits D0 and D1 are fed to two parallel three-stage pipelined latches directly.

* The six MSB bits are fed to the decoders. (D2, -----, D7)

・Segmented decoding structure of the DAC



・Decoding scheme:

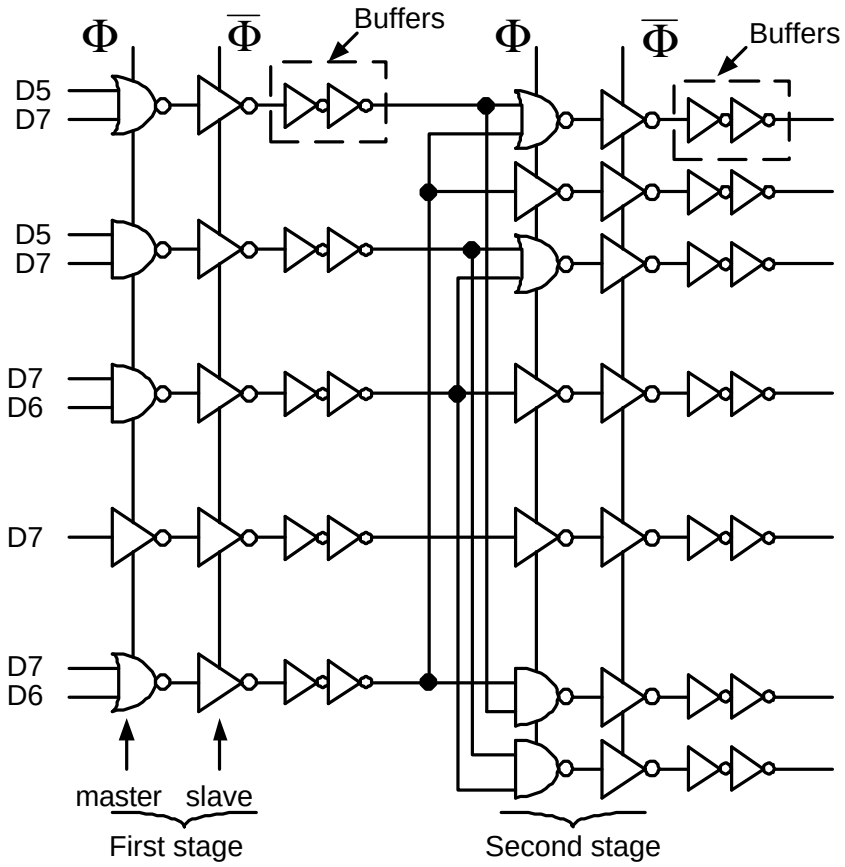
Column	Row
D4 D3 D2	D7 D6 D5
D4+D3+D2 = C1	D7+D6+D5 = R1
D4+D3 = C2	D7+D6 = R2
D4+D4D3+D3D2+D4D2 = C3	D7+D7D6+D7D5+D6D5 = R3
D4 = C4	D7 = R4
D4D3+D4D2 = C5	D7D6+D7D5 = R5
D4D3 = C5	D7D6 = R6
D4D3D2 = C7	D7D6D5 = R7

・Decoding of current-source matrix:

R1	R1+C1	R1+C2	R1+C3	R1+C4	R1+C5	R1+C6	R1+C7
R2	R2+R1C1	R2+R1C2	R2+R1C3	R2+R1C4	R2+R1C5	R2+R1C6	R2+R1C7
R3	R3+R2C1	R3+R2C2	R3+R2C3	R3+R2C4	R3+R2C5	R3+R2C6	R3+R2C7
R4	R4+R3C1	R4+R3C2	R4+R3C3	R4+R3C4	R4+R3C5	R4+R3C6	R4+R3C7
R5	R5+R4C1	R5+R4C2	R5+R4C4	R5+R4C4	R5+R4C5	R5+R4C6	R5+R4C7
R6	R6+R5C1	R6+R5C2	R6+R5C4	R6+R5C4	R6+R5C5	R6+R5C6	R6+R5C7
R7	R7+R6C1	R7+R6C2	R7+R6C4	R7+R6C4	R7+R6C5	R7+R6C6	R7+R6C7
	R7C1	R7C2	R7C3	R7C4	R7C5	R7C6	R7C7

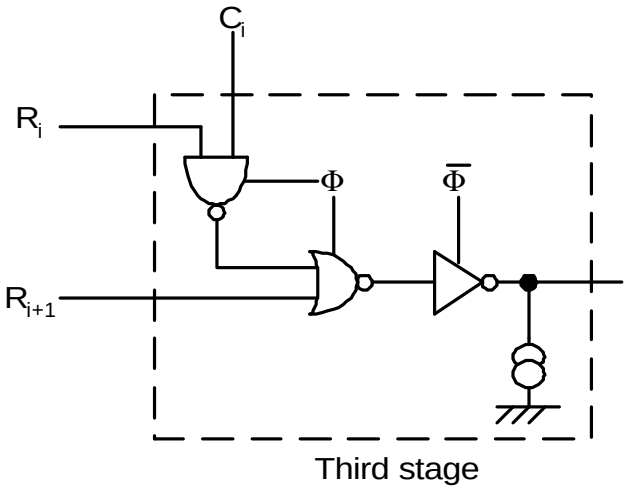
・Logic diagram of the segmented row decoder

* Clocked CMOS gates
* Pipelined structure with two stages.



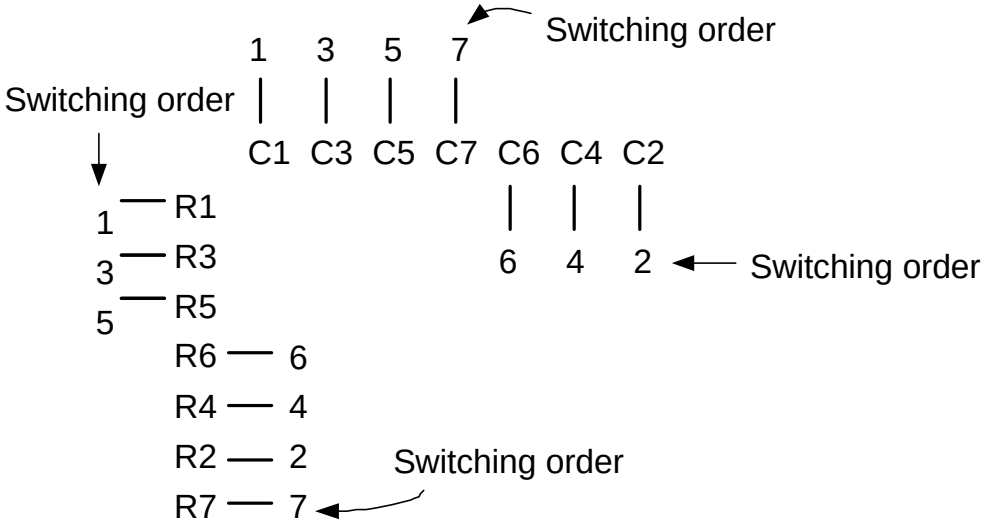
・Logic diagram of the segmented column decoder is similar to that of the row decoder.

・Current cell circuit

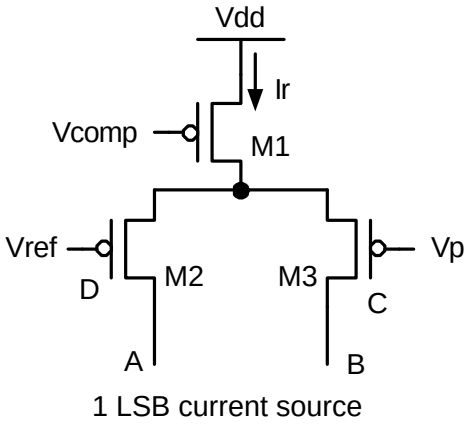


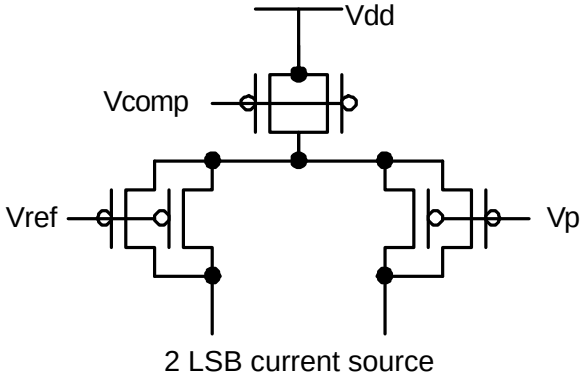
* The third stage of the pipelined circuit.

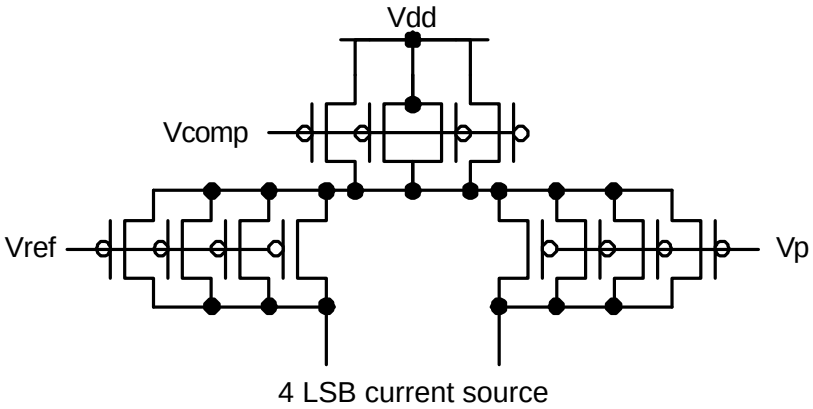
・Symmetrical switching sequence to reduce the gradient effect.



・Current source and current switch







・General characteristics/features of current-mode thermometer-coded DAC:

(1) No resistor or capacitor are used.

(2) Require special layout arrangement and complicated switching sequence to reduce the mismatches among current cells in the matrix $\Rightarrow$ complicated decoder

(3) Logic circuits and long delay.

(4) Complicated wiring

(5) Large chip area $\Rightarrow$ worse matching problem.

(6) Suitable for high-speed (video) and high-resolution (10-bit) CMOS DAC.

$\because$ Current switching and better matching than resistors.

§11-5 Hybrid DAC

Combined architecture: Resistor-string + charge-redistribution DAC
Weighted-current-source + current-mode thermometer-coded DAC

§11-6 Case study

Ref.: *IEEE JSSC, vol.33, PP.1948-1958, Dec.1998*

10-bit 500-MS/s CMOS DAC:

・Chip area comparison between weighted-current-source DAC and thermometer-coded DAC

TABLE I

AREA REOUIREMENT FOR BINARY-WEIGHTED AND THERMOMETER-CODED DAC

Requirement	Binary Weighted	Thermometer Coded
INL (10-bit)	$(0.5\sqrt{1024})s = 16s$	$16s$
DNL (10-bit)	$\sqrt{1024}s = 32s$	s
Area (INL=0.5-lsb)	$256*A_{unit}$	$256*A_{unit}$
Area (INL=1-lsb)	$64*A_{unit}$	$64*A_{unit}$
Area (DNL=0.5-lsb)	$1024*A_{unit}$	A_{unit}

s : standard deviation of current sources.

Aunit: minimum required area to obtain a DNL = 0.5 LSB for the thermometer-coded architecture.

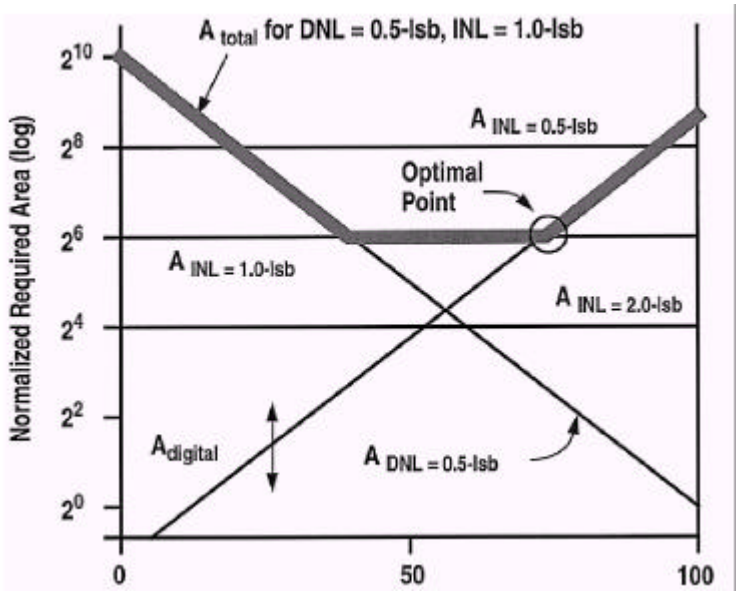
$$\text{Chip area} \propto \frac{1}{s^2}$$

・Normalized required chip versus percentage of segmentation and THD versus percentage of segmentation

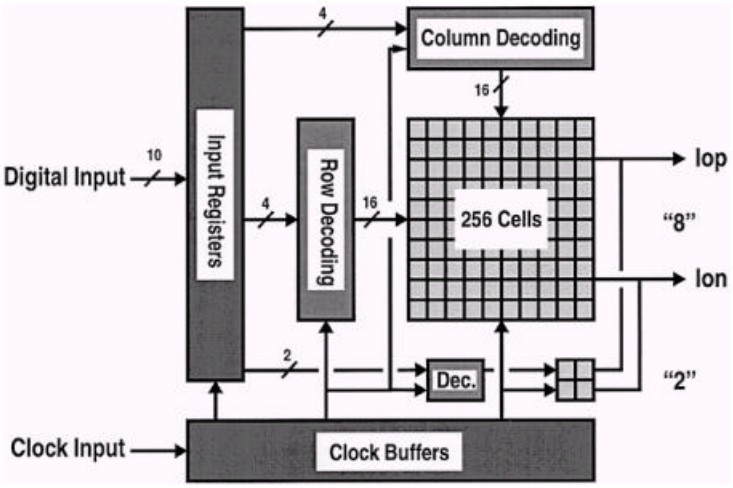
$\Rightarrow$Optimal point

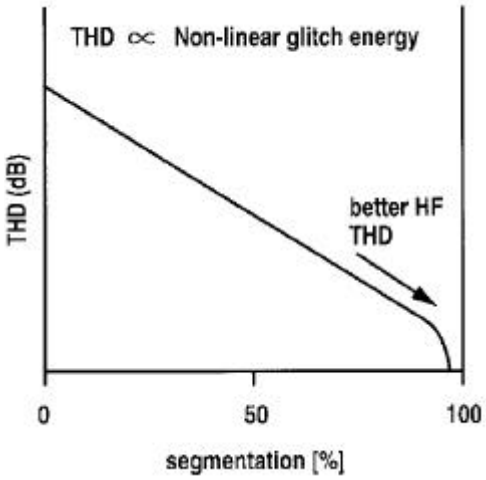
$A_{digital} = A_{INL} = 1.0$ lsb

THD $\downarrow$



・Block diagram: 8+2 segmentation

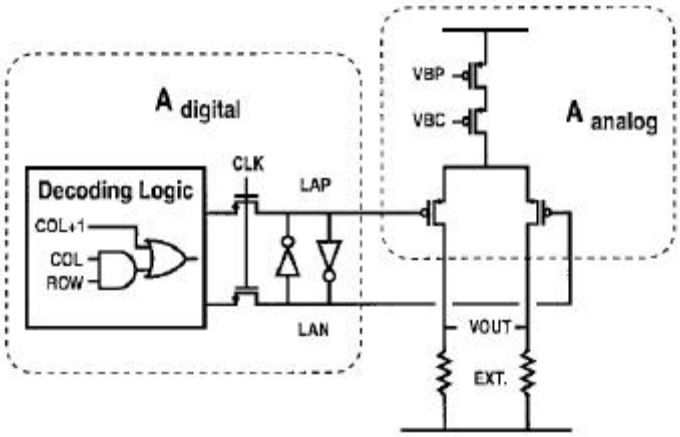




・Cell circuit

Digital: decoding logic + latch

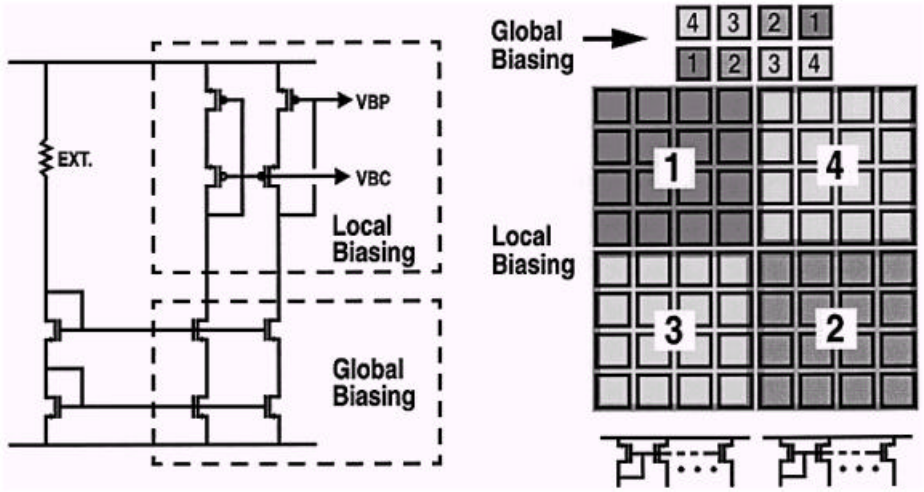
Analog: differential switch +
cascoded current source.



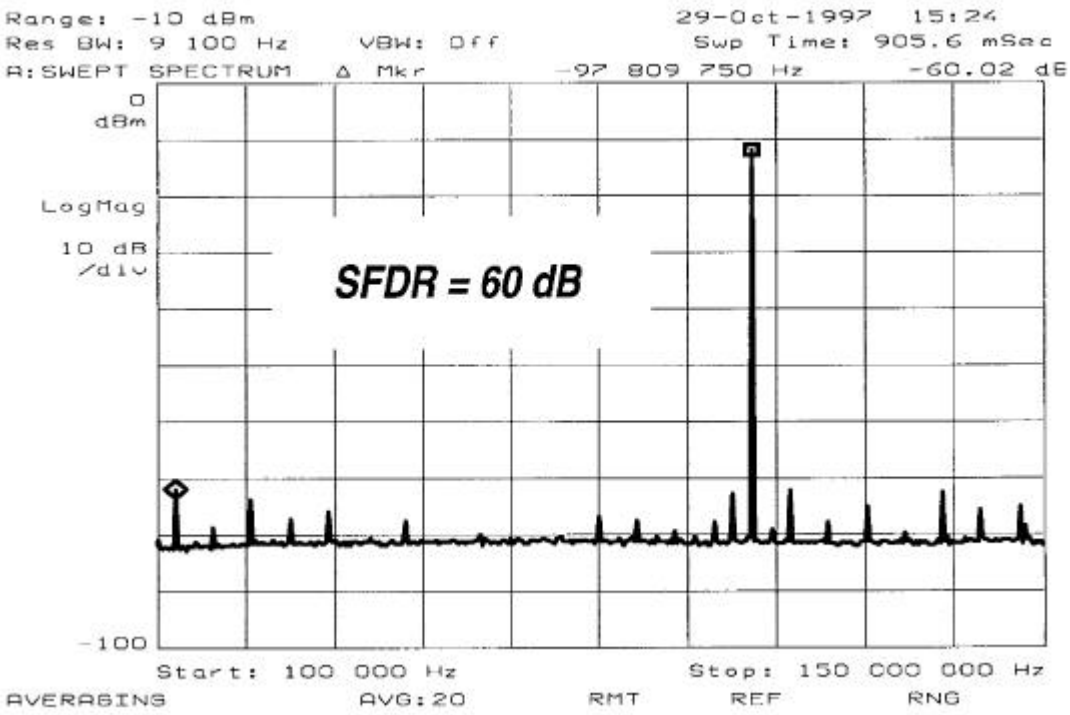
・Biasing scheme

Global biasing: common-centroid
layout

Local biasing: 4 quadrants
without direct connection between any two quadrants
$\Rightarrow$DNL $\downarrow$ and INL $\downarrow$

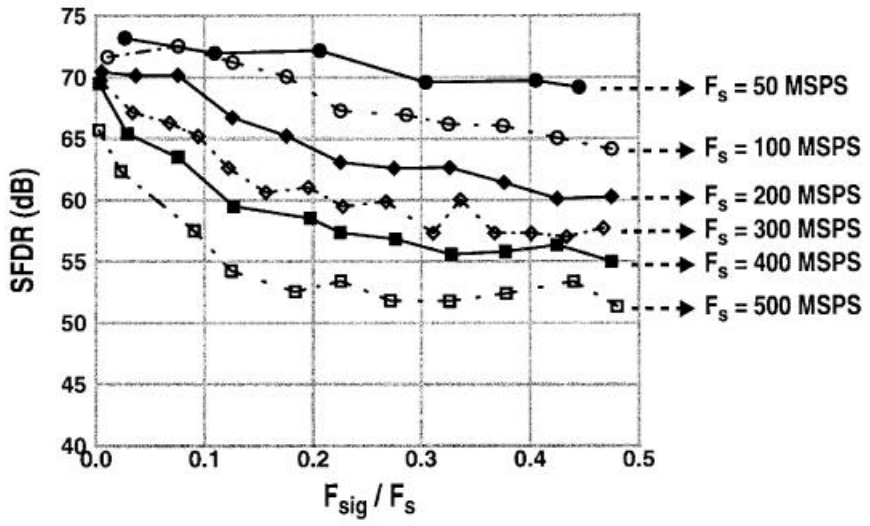


・Sinewave spectrum for Fs=300MS/s and Fsig=100MHz . SFDR=60dB



・SFDR versus Fsig/Fs

SFDR	Fs(MS/s)	Fsig(MHz)
73dB	100	8
60dB	300	100
51dB	500	240



・Summary

Technology	0.35μm (1P4M) pure digital CMOS
Area	$0.6mm^2$
Sampling Frequency	500 MSample/s
Ouput Swing (into 75Ω load)	$2V_{pp}$ (differential)
Power Disspation (at 500 MSample/s)	18mA (analog)
	20mA (digital)
	from 3.3V supply
DNL	0.1 LSB
INL	0.2 LSB

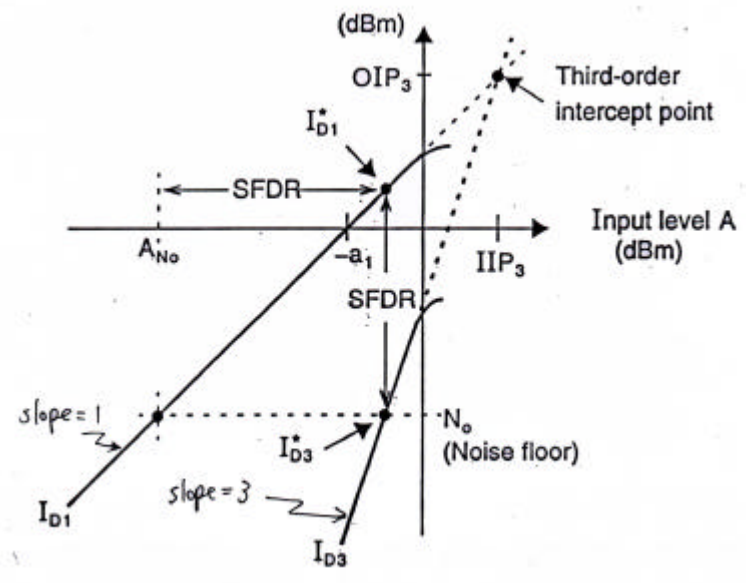
2. Definition of SFDR (Spurious-Free Dynamic Range)

SFDR: The signal-to-noise ratio when the power of the third-order intermodulation products equals the noise power.

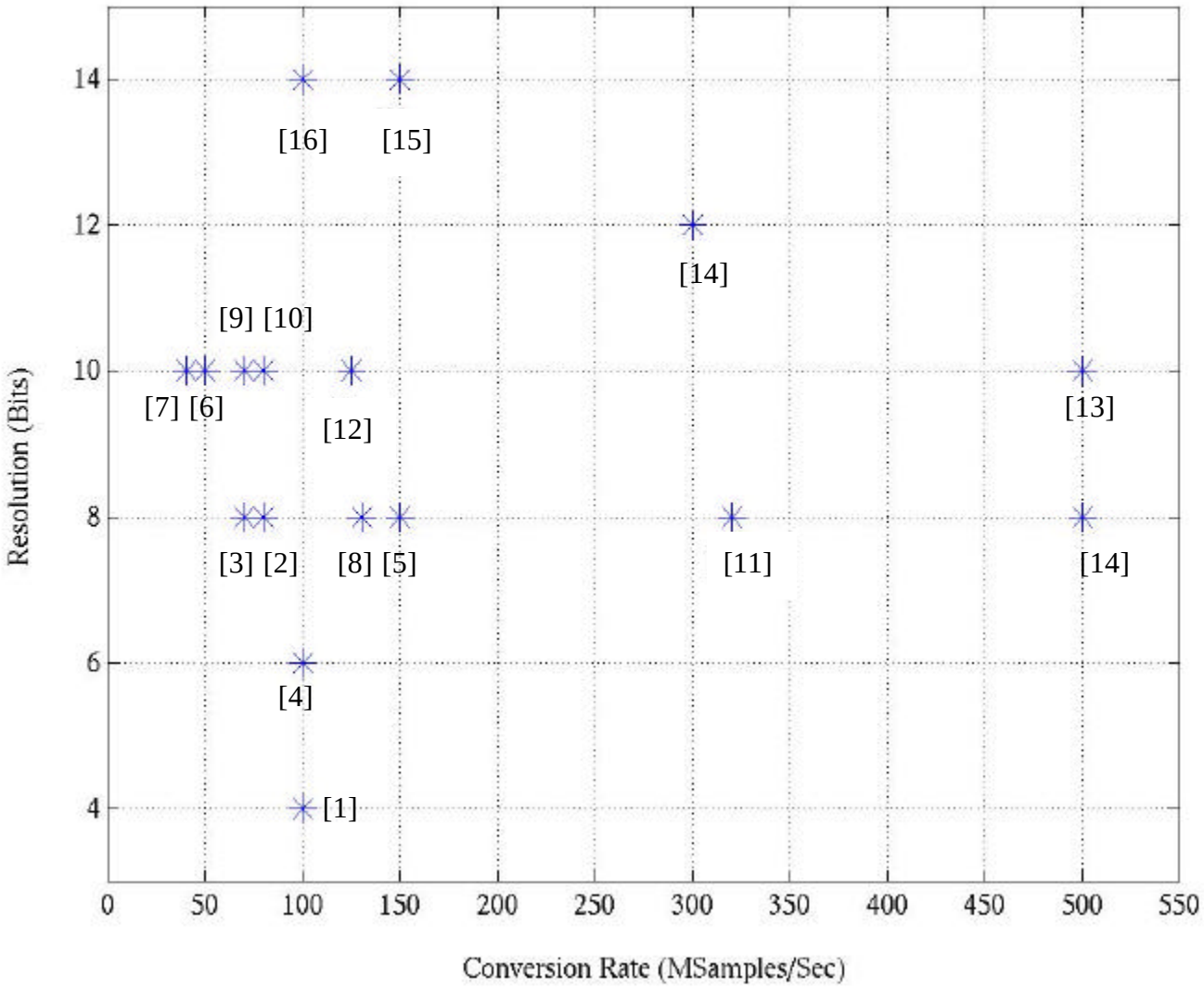
$SFDR = I_{D1}^{*} - I_{D3}^{*} = I_{D1}^{*} - N_0$ (dB)

∵ I_{D1} curve has a slope=1

$\Rightarrow$ $SFDR = A\big|_{I_{D3}=N0} - A_{N0}\big|_{I_{D1}=N_0}$



§11-7 Summary



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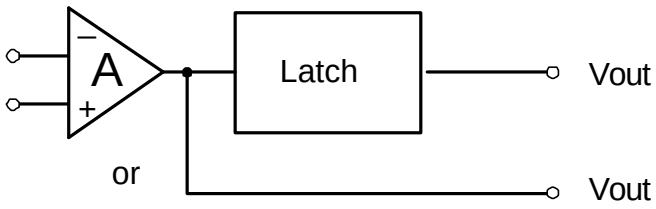
CH 12 CMOS Analog Comparators

§12-1 General Considerations

Purpose of Comparators: To compare two input voltages and produce a very large output voltage with an appropriate sign to indicate which of the two is large.

Types of MOS Comparators:

A. Differential-input OP AMP



The latch provides a large and fast output signal, whose amplitude and waveform are independent of those of the input signal. Well suited for the logic circuits usually following the latch.

If no latch: -1mV → +1mV input =＞-5V→+5V output

Gain＝5000, 74 dB

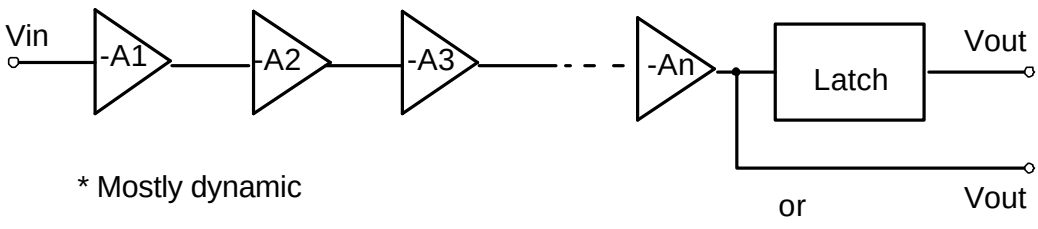
If use latch: The output voltage of A must be larger than the combined offset and threshold voltage of the latch, which is about 0.2V

＝＞Gain = 200

(1) Static configurations

(2) Dynamic configurations

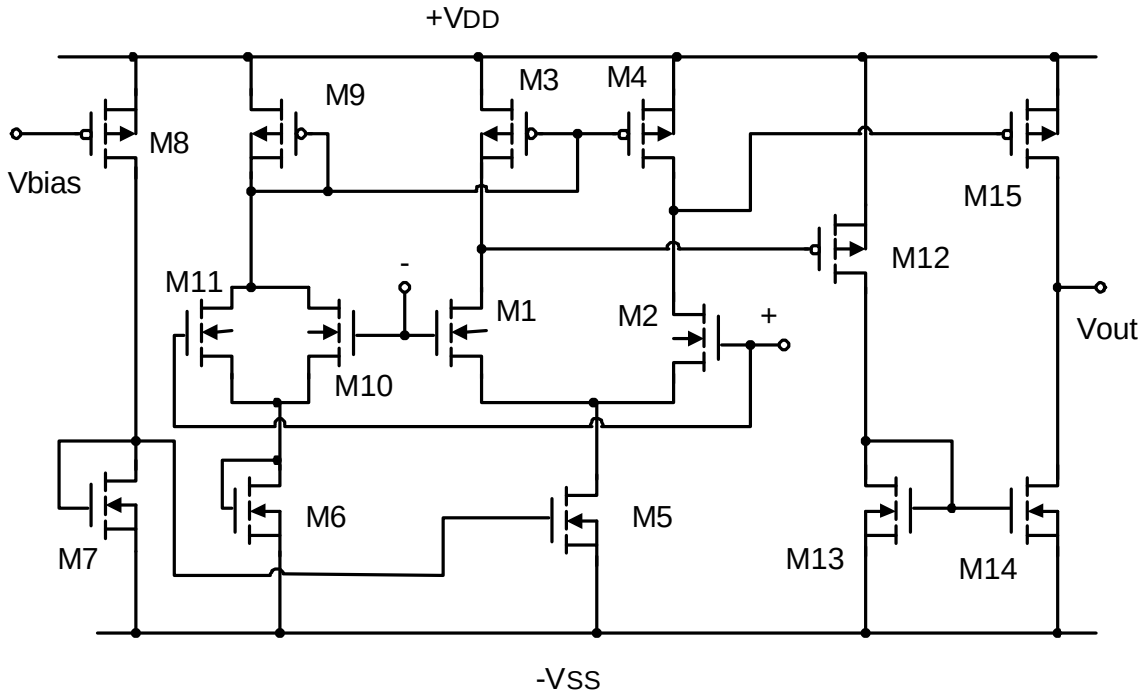
B. Cascaded inverter stages



§12-2 Differential-Input OP AMP Comparators

§12-2.1 Static Configurations without Latches

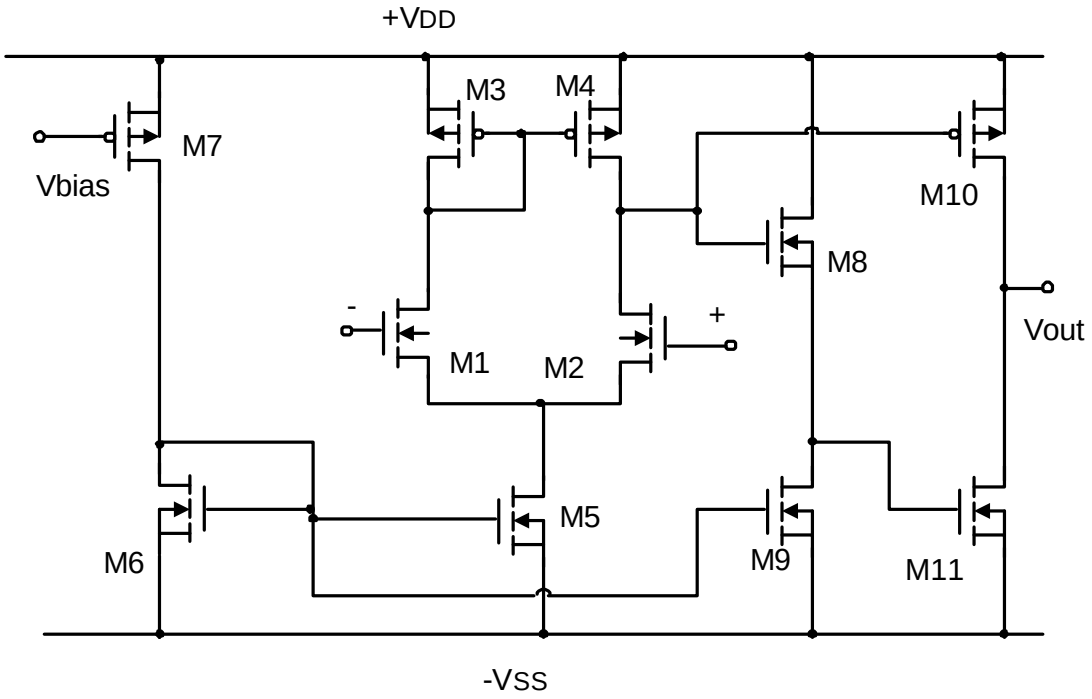
1.



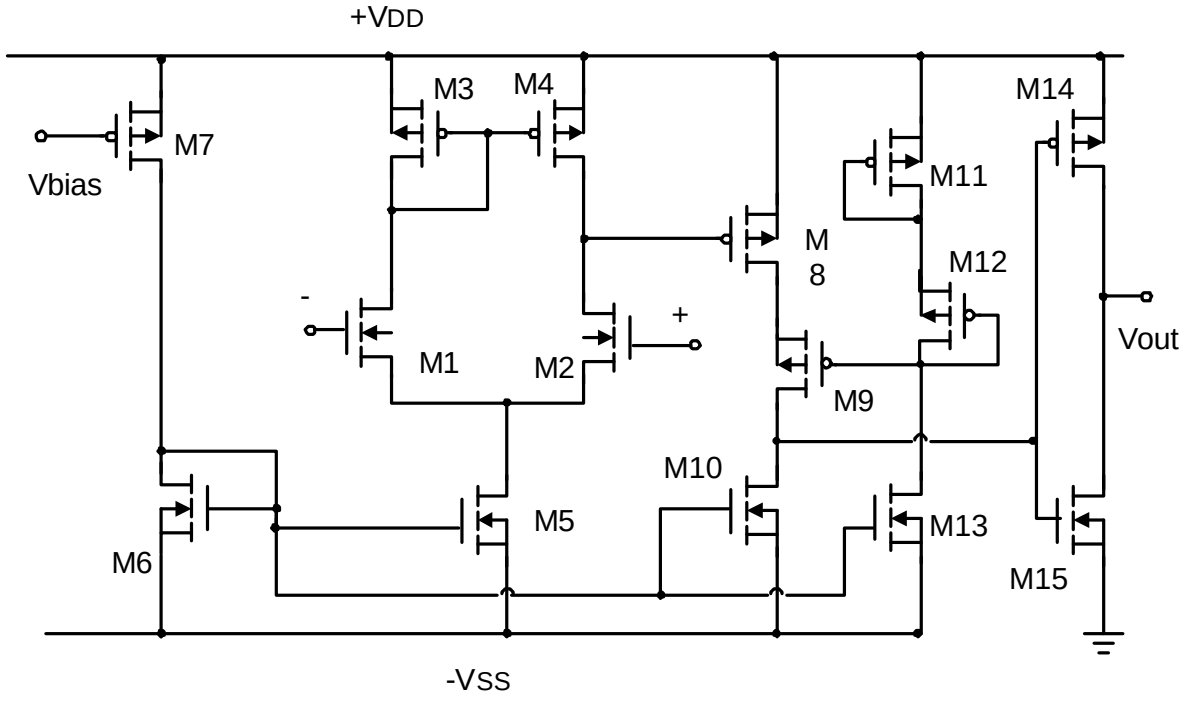
* High Speed Comparator
* Open loop gain: ~80dB
* Output Swing: ±5V
* Propagation Delay (±10mV Vin): ~1.2μs~2.4μs (15PF Load)
* Generally, compensation circuit is not needed since there is no feedback connection.
* Power Dissipation: ~10 mW

2. General-purpose comparators

* Propagation delay: (±10mV, 15PF) 1.0μs~2.8μs
* Power Dissipation: ~ 4mW



3. Comparator with level shift.



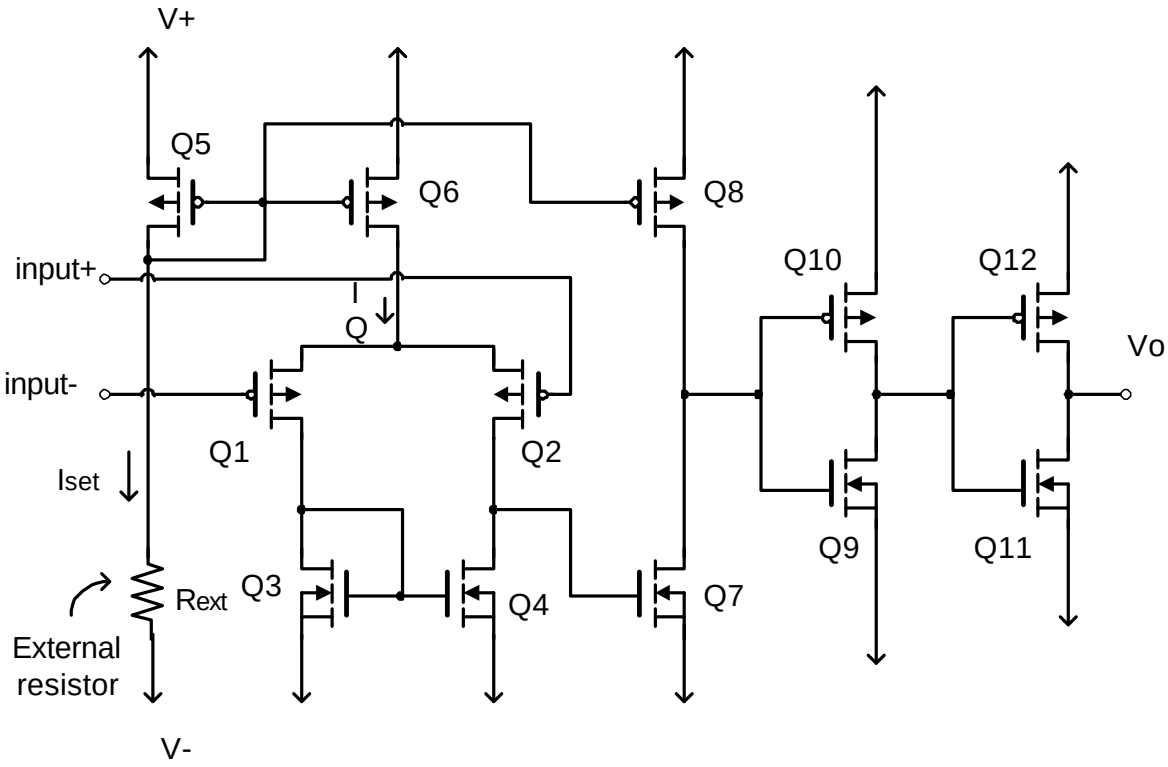
* Open loop gain: 60-80dB

* Output Swing: +5V→0V

* Propagation delay (±10mV, 15 PF): 1.0μs~0.8μs

* Power Dissipation: ~1.5mW

4. CMOS Voltage Comparator MC 14574 (Motorola)



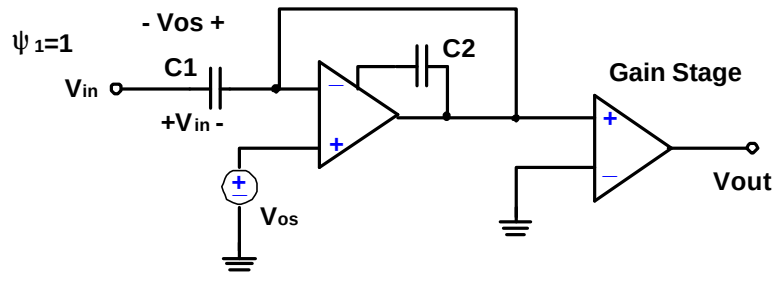
* Quad comparators
* Open loop gain (Iset＝I_Q＝50μA): 96dB
* Propagation delay: ~1μs

5. Fully differential OP-AMP Comparators.

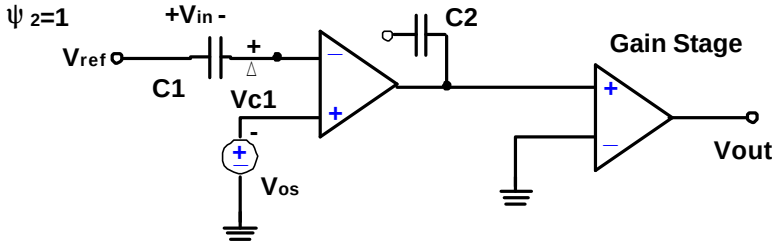
§12-2.2 Dynamic Configurations without Latches.

(1) Dynamic OP-AMP type comparator

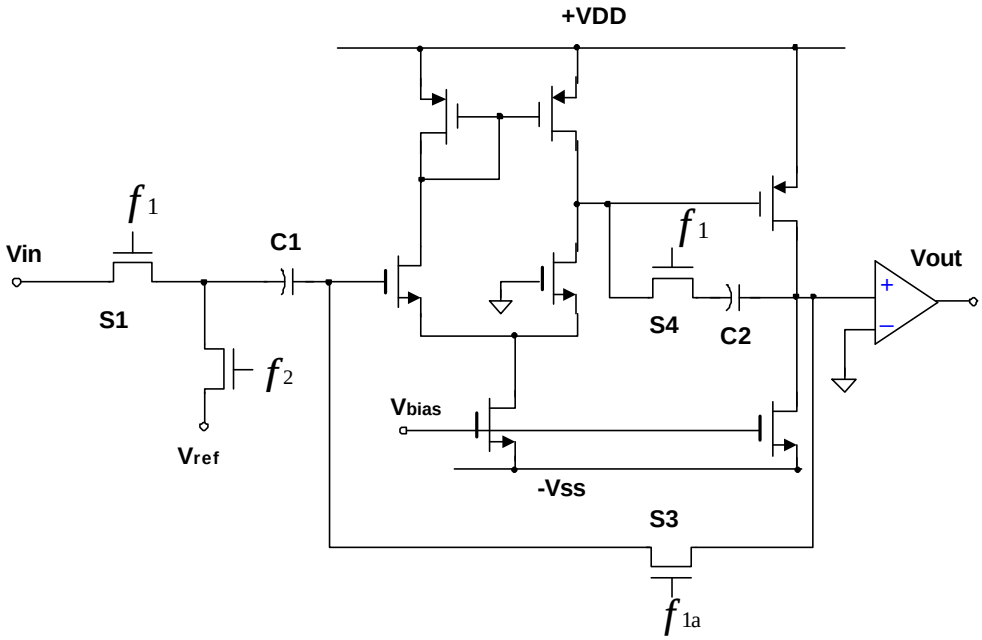
* Compensated by C_2
* Vc1=Vin-Vos
* offset memorization



* △Vc1＝Vref-Vin
* No compensation
* offset cancellation

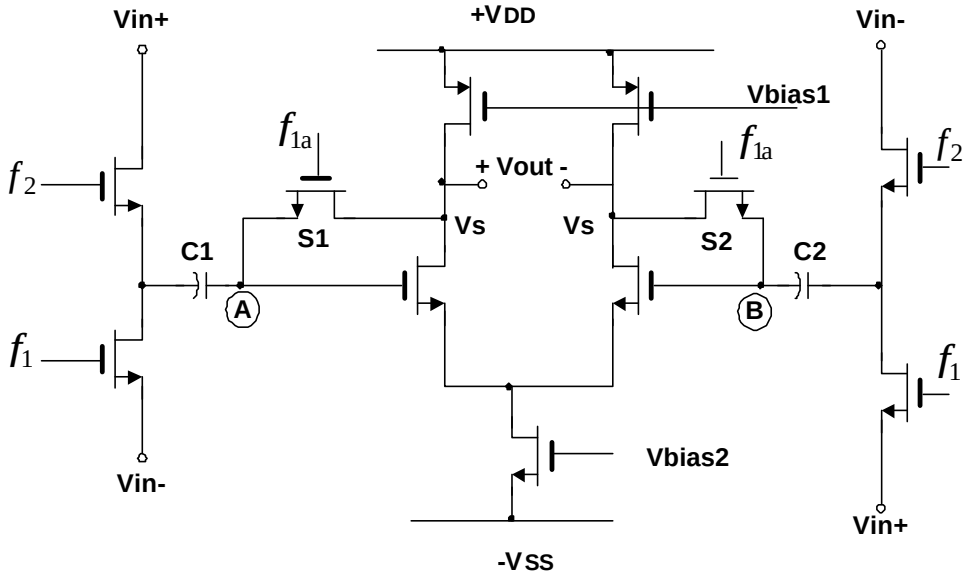


ψ1, ψ2 :nonoverlapping clocks



* Practically, ϕ_{1a} must go low first in advance of ϕ_1 to avoid the clock feedthrough effect of S_1 by ϕ_1.

(2) Dynamic fully differential comparator



C_1, C_2: Autozeroing capacitors

$\phi_1 = 1$ $\quad V_{c1} = Vin^- - Vs$, $\quad V_{C2} = Vin^+ - Vs$

$\phi_2 = 1$ $\quad \triangle V_{c1} = Vin^+ - Vin^-$, $\quad \triangle V_{C2} = Vin^- - Vin^+$

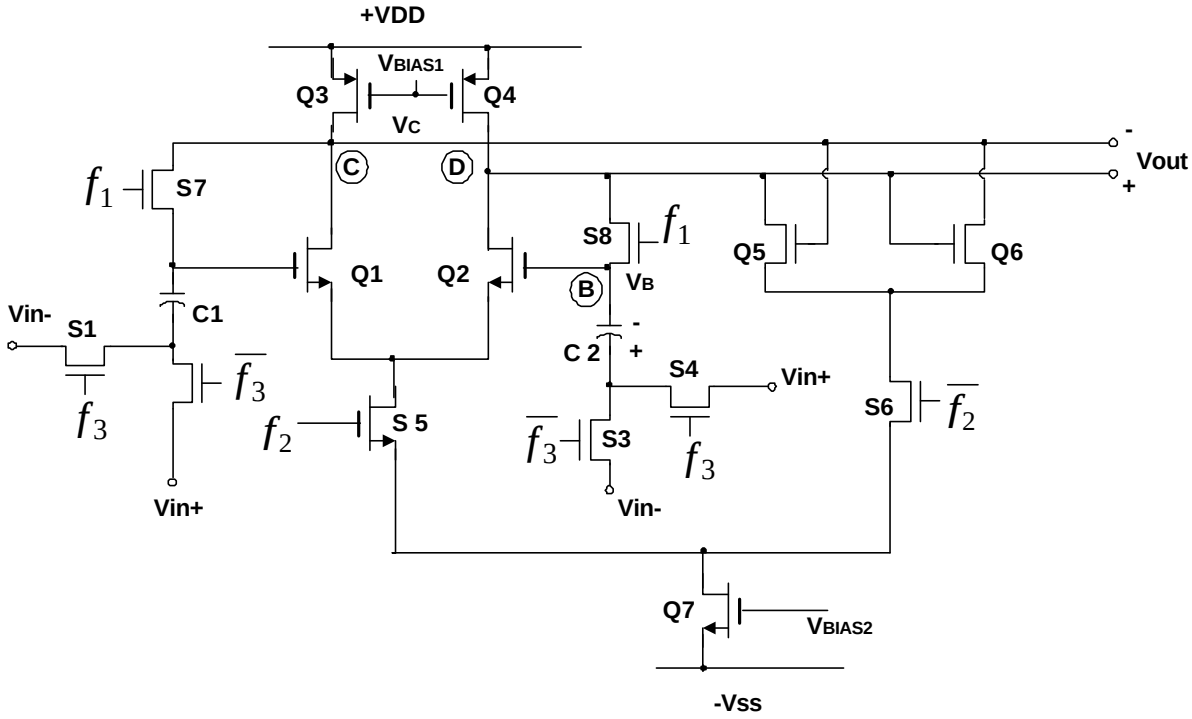
* S_1 and S_2 generate feedthrough voltages at Ⓐ and Ⓑ

$=>$ common-mode voltage

* CMRR can be promoted by using negative common-mode feedback circuit.

§12-2.3 Dynamic Configuration with Latches

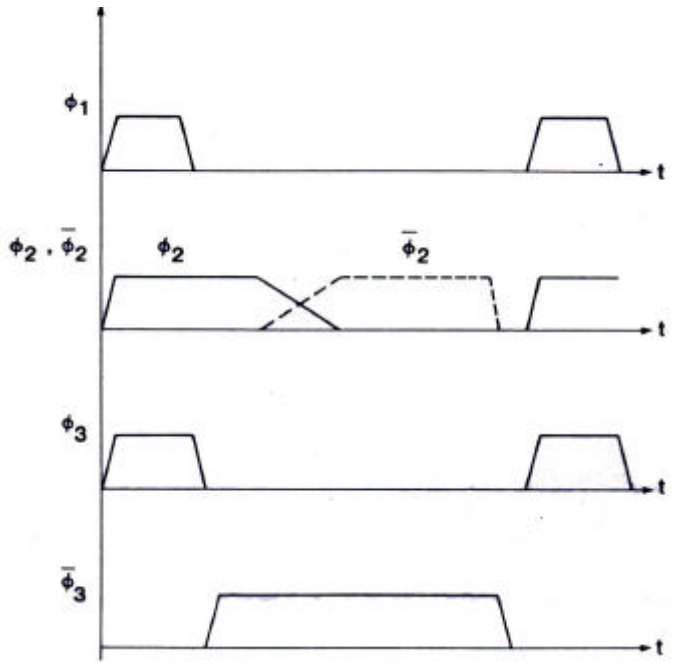
Preamplifier-latch combination



* $f_2 \rightarrow 1$, S_5 short $=>$ Q_1, Q_2, Q_3, Q_4 and Q_7 are differential amplifier.

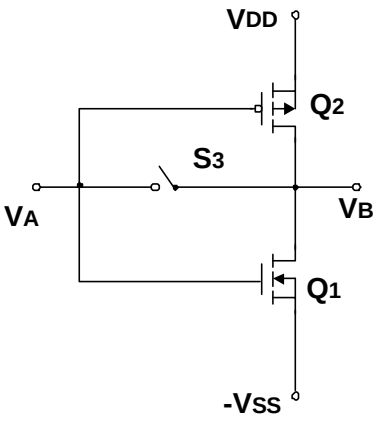
$\overline{f}_2 \rightarrow 1$, S_6 short $=>$ Q_3, Q_4, Q_5, Q_6 and Q_7 are a bistable latch.

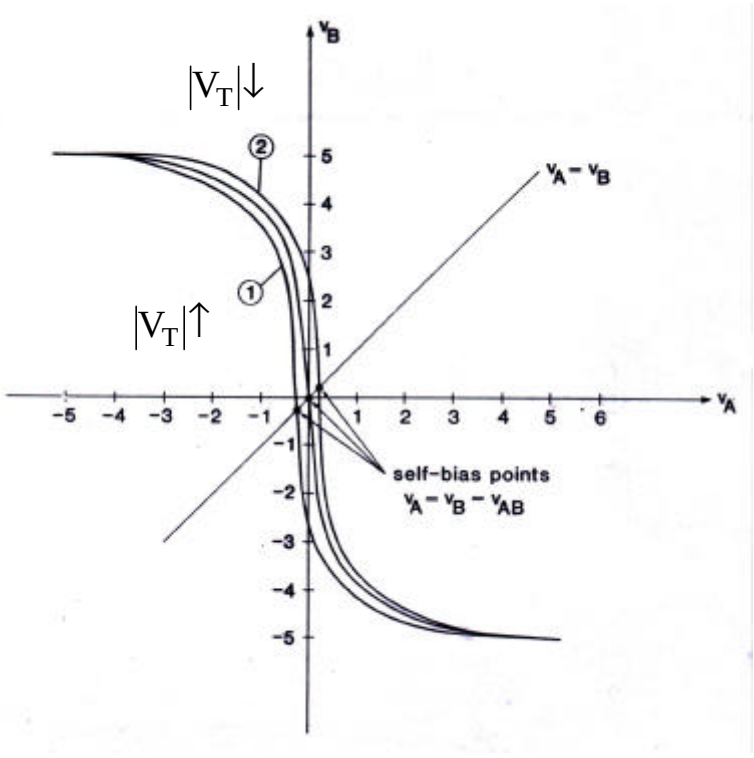
Operating clock waveforms:



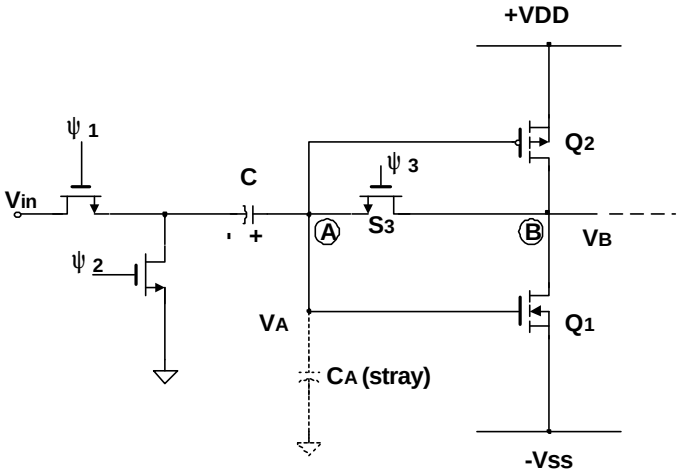
§12-3 Cascaded Inverter Stages

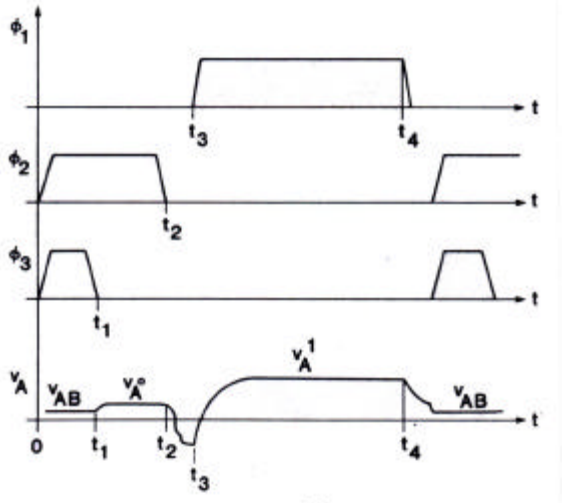
(1) Basic Structure





(a) (b)





(a) (b)

$\phi_2 \rightarrow 0$, $C_A << C$, $=>$ negligible feedthrough

$V_A^1 = Vin + V_A^o$

$\triangle V_A = Vin$

(2) CMOS Cascade Comparator.

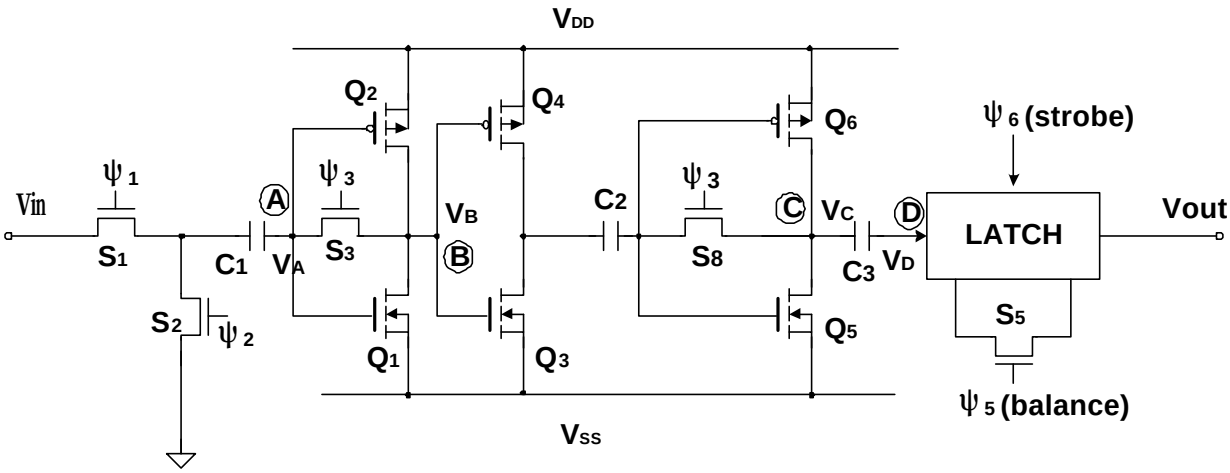
* $Q_1 \equiv Q_3$, $Q_2 \equiv Q_4$

* The speed of the cascaded inverter stages is limited by the RC times constants.

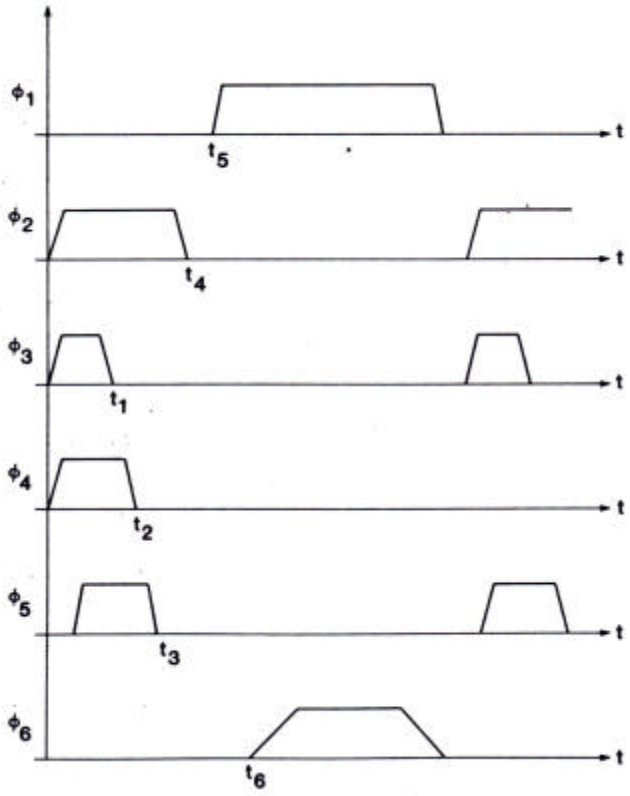
$$R = R_0 = r_{dsp} \| r_{dsn} \qquad \sim 100\,k\Omega$$

$$C_{in} = C_{gs} + C_{gd}(1 + |A|) \qquad \sim 0.5\ pF$$

$$A \sim 10$$



(a)

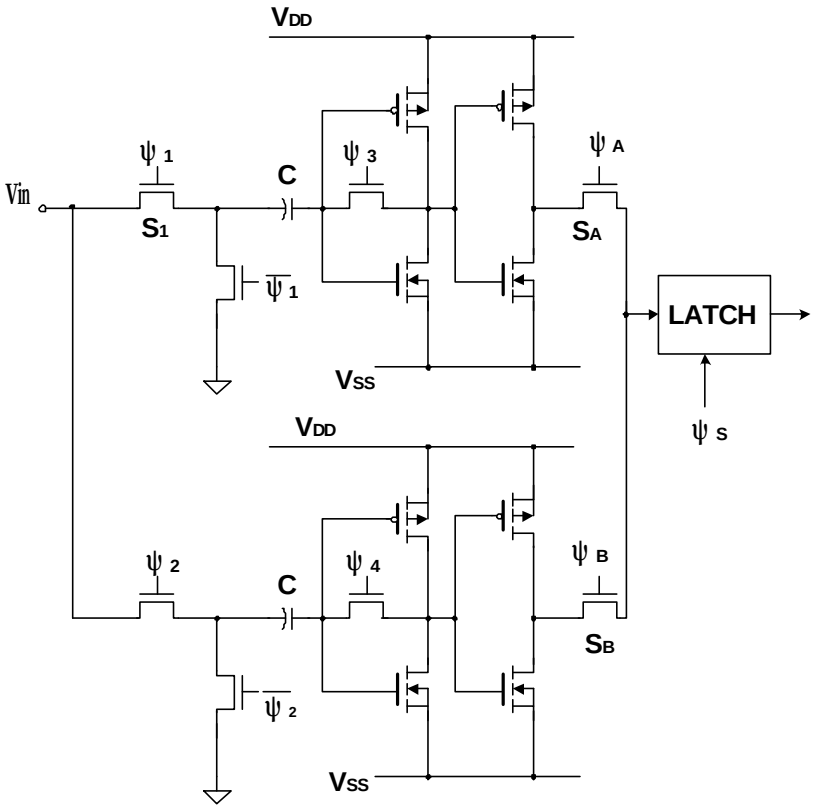


(b)

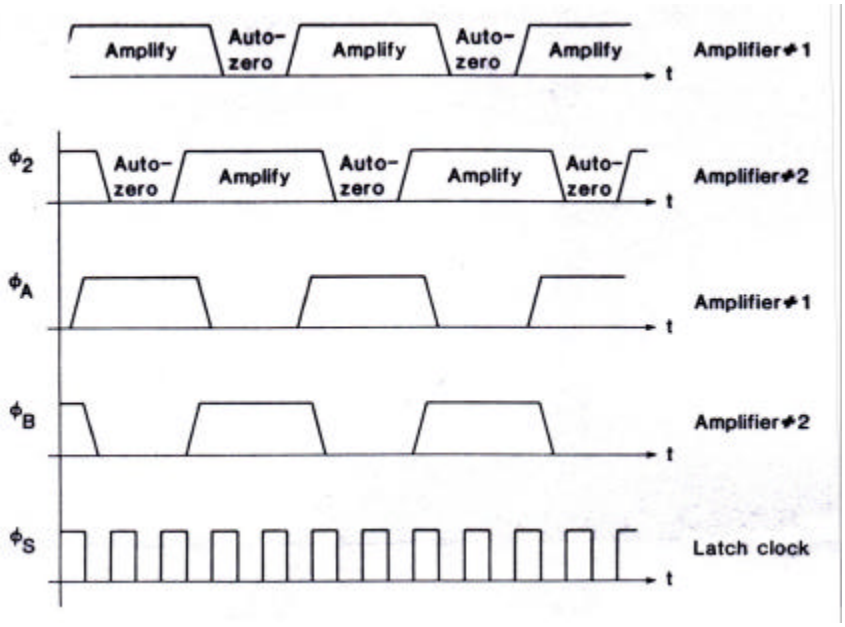
(3) Fast comparators with two amplifiers and a single latch.

* Usually, the speed of a latch is faster than that of a amplifier.

＝＞Two amplifiers share one latch.

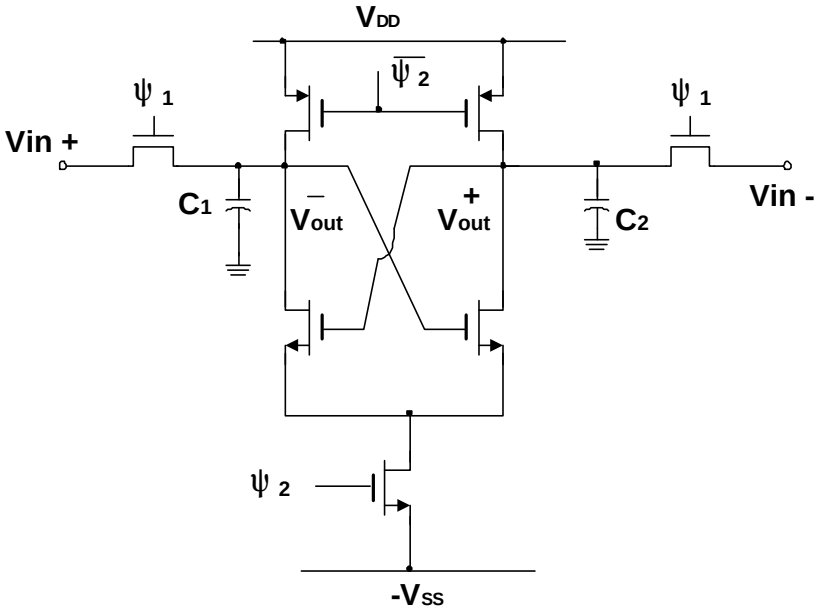


* Operating clock waveforms



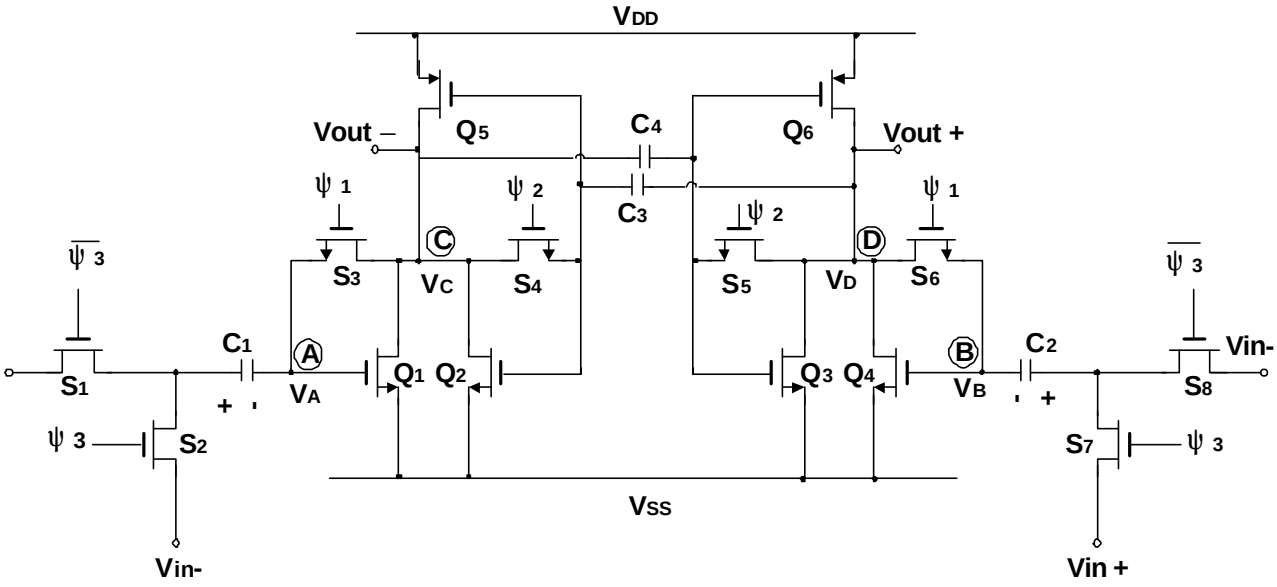
§12-4 CMOS Dynamic Latches for Comparators

1. Direct-coupled latch with differential input signals

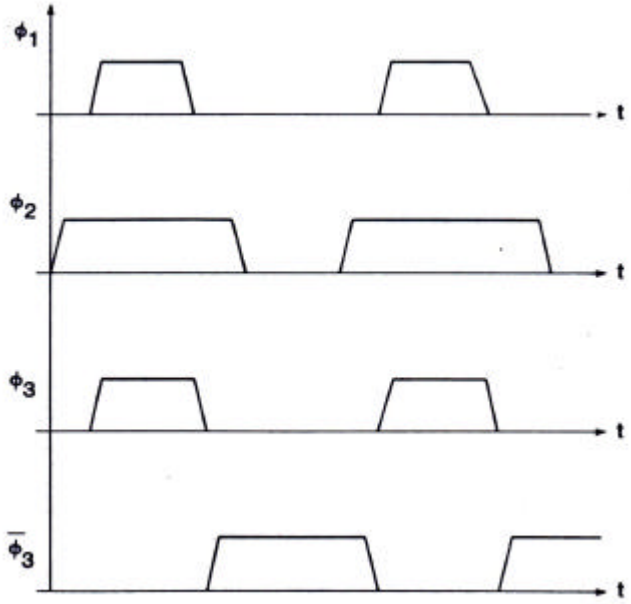


* For single-ended inputs, Vin^+ or Vin^- may be replaced by a threshold voltage or can be generated by self-biasing

2. Capacitively coupled latch with autozeroing input



(a)



* $\phi_2 \rightarrow 1$ ＝＞ inverters Q_2-Q_5 and Q_3-Q_6 are biased at their optimal points

C_3 and C_4 are also precharged such that any asymmetry between the two inverters is compensated by the slightly different bias voltages provided by C_3 and C_4.

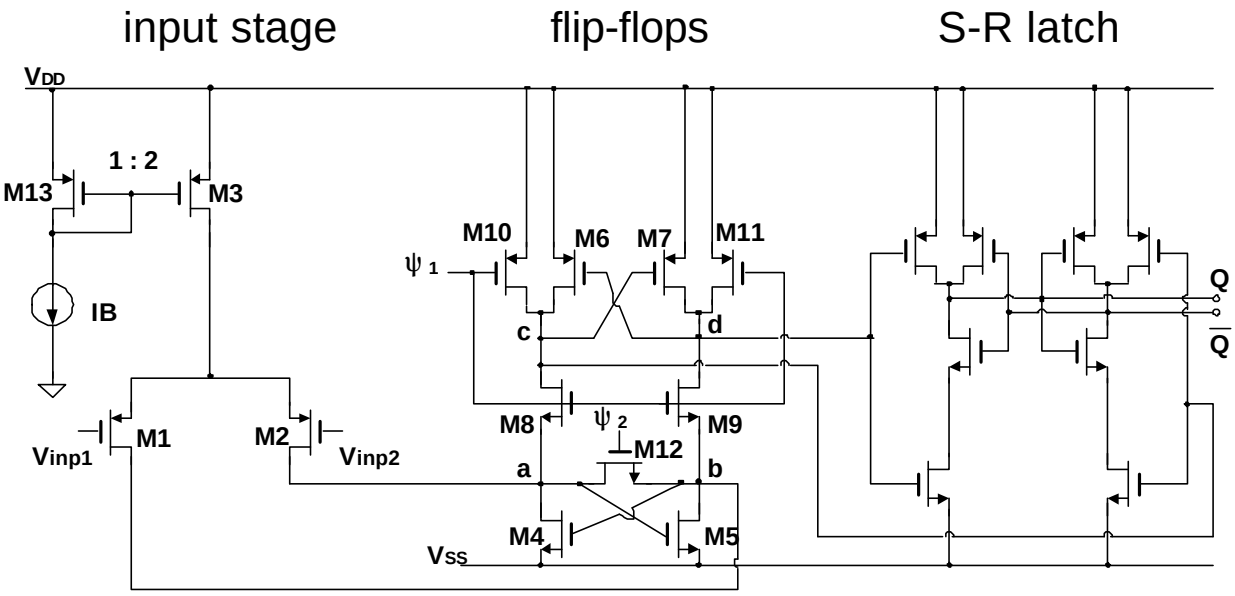
＝＞ loop gain of the latch＝1.

* Vin+ ＜ Vin- : V_C H, V_D L.

Vin- ＜ Vin+ : V_C L, V_D H.

§12-5 Case Studies

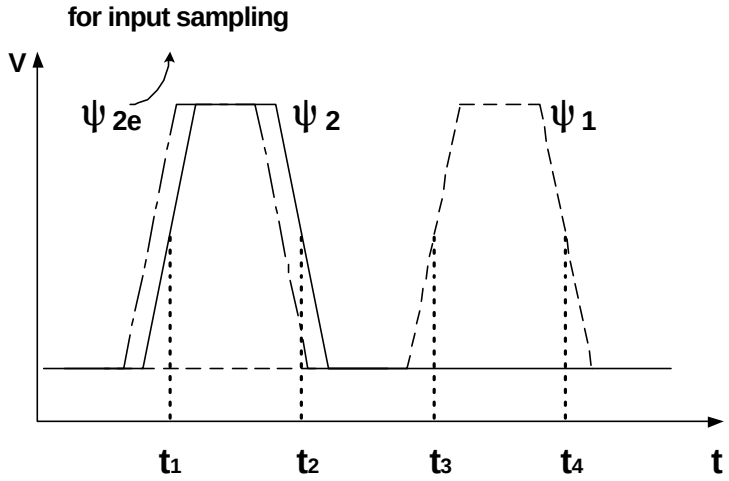
1. Differential-Input OP AMP Comparators with Dynamic Latches
   Ref. IEEE JSSC, vol. 27, pp. 208-211, Feb. 1992



t1~t2: M_{12} ON ($\phi_2 = 1$)
M_{10}-M_{11} ON, M_8-M_9 OFF ($\phi_1 = 0$)
$Va = Vb$, $Vc = Va$, $Q = \overline{Q}$
$Vinp_1$ and $Vinp_2$ settles

t2~t3: $Va \neq Vb$ established with some regeneration of M_4/M_5, M_{12} OFF

t3-t4: $\phi_1 = 1$, $\phi_2 = 0$ => M_{12} OFF, M_{10}, M_{11} OFF, M_8, M_9 ON
strong regeneration => $Vc \neq Va$, $Va = Vc$, $Vb = Vd$ => $Q, \overline{Q}$ established



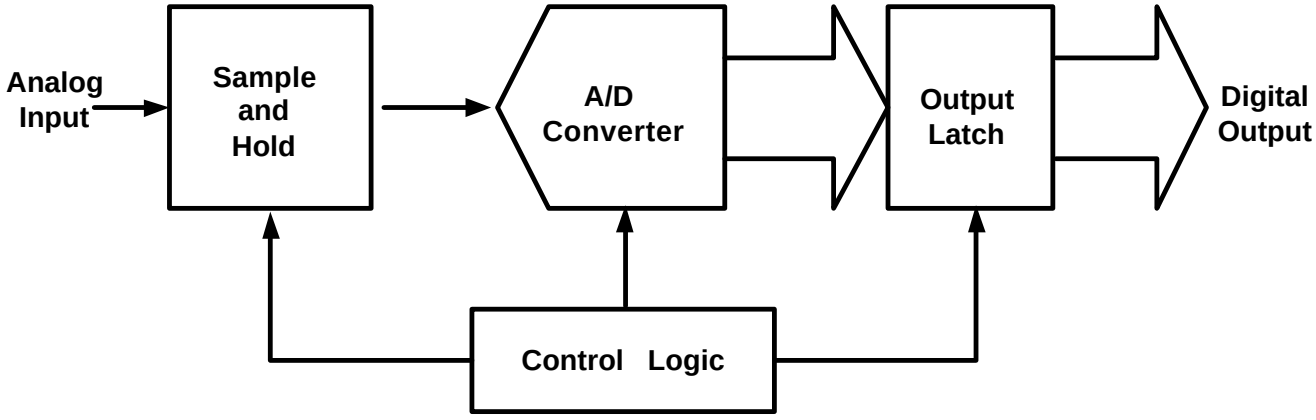
Performance:

Technology	1.5 um CMOS
Die size	140 x 100 um^2
Power supply	+2.5 / -2.5 V
Input dynamic range	2.5 V
Resolution	8 bits, 1LSB=9.8 mV
Sensitivity	10.6 mV (< 7 bits)
Sampling rate	65MHz
Offset voltage	3.3 mV
Input capacitance	30 fF

CH 13 CMOS Analog to Digital Converters (ADCs)

§13-1 Introduction

1. Functional block diagram of a A/D converter



2. Ideal A/D Converter (ADC)

$$V_{in} \pm V_x = V_{ref}(b_1 2^{-1} + b_2 2^{-2} + \cdots + b_N 2^{-N})$$

$$= \frac{V_{ref}}{2^N}(b_1 2^{N-1} + b_2 2^{N-2} + \cdots + b_{N-1} 2^1 + b_N 2^0)$$

where V_{in} is the input analog voltage or current

V_{ref} is the reference voltage or current

$b_1 \ldots\ldots b_N$ is the digital output

V_x is the tolerable input signal range

$$-\frac{1}{2}V_{LSB} \le V_x \le \frac{1}{2}V_{LSB}$$

2-bit ADC:

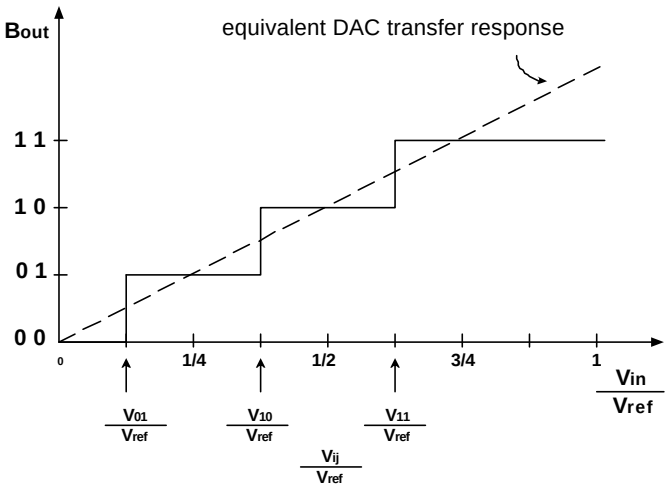
Input-output transfer curve:

Offset by $\frac{1}{2}V_{LSB}$ ($\frac{1}{2}$LSB)

$$V_{LSB} = \frac{1}{4}V_{ref} \rightarrow 1\,\text{LSB}$$

$$\frac{V_{LSB}}{V_{ref}} = \frac{1}{4} \rightarrow 1\,\text{LSB}$$

The input voltage or current should remain less than 3/4 V_{ref} + 1/8 V_{ref} =7/8 V_{ref} and greater than 0 - 1/8 V_{ref} = -1/8 V_{ref}.



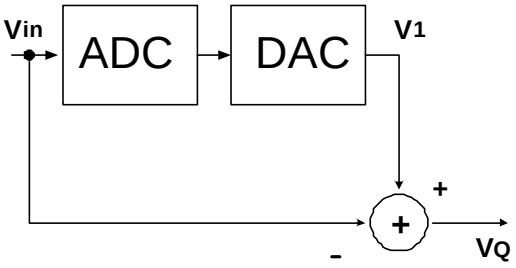
Overloaded ADC: When $V_{in} > V_{in}|_{ideal} + V_x$ or $V_{in} < V_{in}|_{ideal} - V_x$, the quantization error is greater than 1/2 V_{LSB}.

3. Quantization noise

Quantization error $\rightarrow$ Quantization noise.

$V_1 = V_{in} + V_Q$

$V_Q = V_1 - V_{in}$

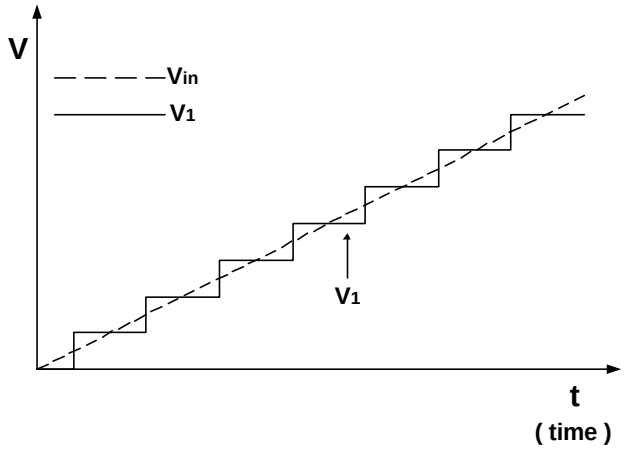


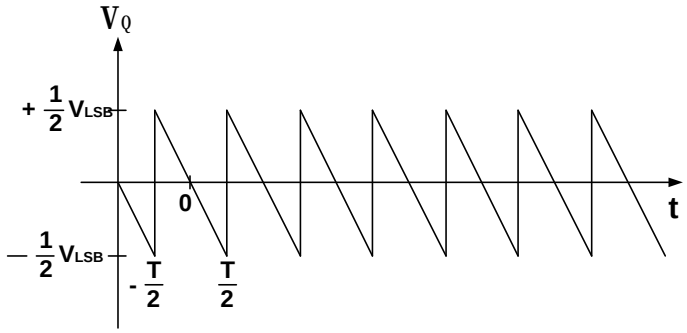
Quantization noise modeling:

(1) Deterministic approach

$$V_{Q(rms)} = \left[\frac{1}{T}\int_{-T/2}^{T/2} V_Q{}^2\, dt\right]^{1/2} = \left[\frac{1}{T}\int_{-T/2}^{T/2} V_{LSB}{}^2 (\frac{-t}{T})^2\, dt\right]^{1/2}$$

$$= \left[\frac{V_{LSB}{}^3}{T^3}\left(\frac{t^3}{3}\ \Big|_{-T/2}^{T/2}\right)\right]^{1/2} = \frac{V_{LSB}}{\sqrt{12}}$$

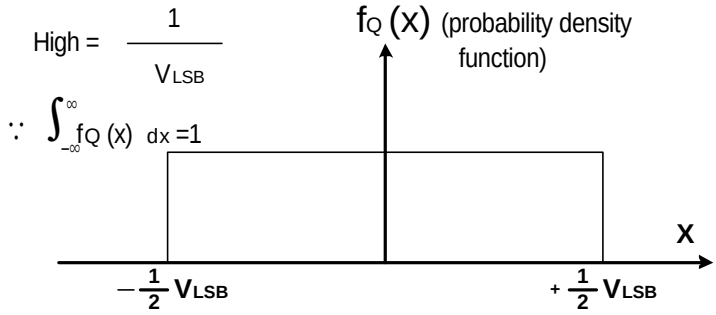




(2) Stochastic approach

$$V_{Q(rms)} = \left[\int_{-\infty}^{\infty} x^2 f_Q{}^2(x)\, dx\right]^{1/2}$$

$$= \left[\frac{1}{V_{LSB}{}^2}\left(\int_{-V_{LSB}/2}^{V_{LSB}/2} x^2\, dx\right)\right]^{1/2} = \frac{V_{LSB}}{\sqrt{12}}$$



4. Signal-to-Noise Ratio (SNR)

(1) V_{in} is a sawtooth of hight V_{ref} (or a random signal uniformly distribut between 0 and V_{ref})

$$\Rightarrow \text{SNR} = 20\log\left(\frac{V_{in(rms)}}{V_{Q(rms)}}\right) = 20\log\left(\frac{V_{ref}/\sqrt{12}}{V_{LSB}/\sqrt{12}}\right) = 20\log 2^N = 6.02\,N\ \text{dB}$$

(2) V_{in} is a sinusoidal waveform between 0 and V_{ref} .

$$\Rightarrow \text{SNR} = 20\log\frac{V_{in(rms)}}{V_{Q(rms)}} = 20\log\frac{V_{ref}/2\sqrt{2}}{V_{LSB}/\sqrt{12}} = 20\log\left(\frac{\sqrt{3}}{\sqrt{2}}\times 2^N\right) = 6.02\,N + 1.76\text{dB}$$

The above SNR is the best possible SNR for an N-bit ADC

$$V_{inpp} = V_{ref}\ (0\text{dB}) \rightarrow \text{SNR} = 6.02\,N + 1.76\,\text{dB}$$

$$V_{inpp} \Rightarrow -20\,\text{dB} \rightarrow \text{SNR} = (6.02\,N + 1.76)\,\text{dB} - 20\,\text{dB}$$

5. Performance specifications

(1) Missing codes (equivalent to monotonicity in DAC)

Maximum DNL < 0.5 LSB or maximum INL < 0.5 LSB

$\Rightarrow$ The ADC is guaranted not to have any missing code.

(2) Conversion time

The time taken for the ADC to complete a single measurement including acquisition time of the input signal.

(3) Sampling rate

The speed at which samples can be continuously converted. Typically, the sampling rate is equal to the inverse of the conversion time except in the case of pipelining structure or multiplexing structure.

(4) Sampling-time uncertainty or aperture jitter

Due to the effective sampling time changing from one sampling instance to the next.

Sinusoidal waveform case:

$$V_{in} = \frac{V_{ref}}{2}\sin(2\pi f_{in} t)$$

$$\frac{d}{dt}V_{in}\Big|_{max} = \pi f_{in} t \qquad \text{zero-crossing point}$$

If $\Delta V < 1\,V_{LSB}$ for some sampling-time uncertainty Δt,

$$\Delta t < \frac{V_{LSB}}{\pi f_{in} V_{ref}} = \frac{1}{2^N \pi f_{in}}$$

examples: 8-bit ADC, 250 MHz $\quad f_{in} \Rightarrow \Delta t < 5\,ps$

16-bit ADC, 1 MHz $\quad f_{in} \Rightarrow \Delta t < 5\,ps$

(5) Dynamic range

Dynamic range ≡

$$\frac{\textit{rms value of the maximum input (output) sinusoidal signal}}{\textit{rms value of the output noise plus the distortion when the same sinusoidal is present at the output}}$$

It is also called the signal-to-noise-and-distortion ratio (SNDR).

* Can be expressed as effective number of bits using the SNR formula on p. 13-3.

* Input frequency dependent.

6. Types of ADCs

Low-to-medium speed:
(1) Dual-slope or Integrating ADC
(2) Oversampling ADC
(3) Successive approximation ADC
(4) Algorithmic ADC

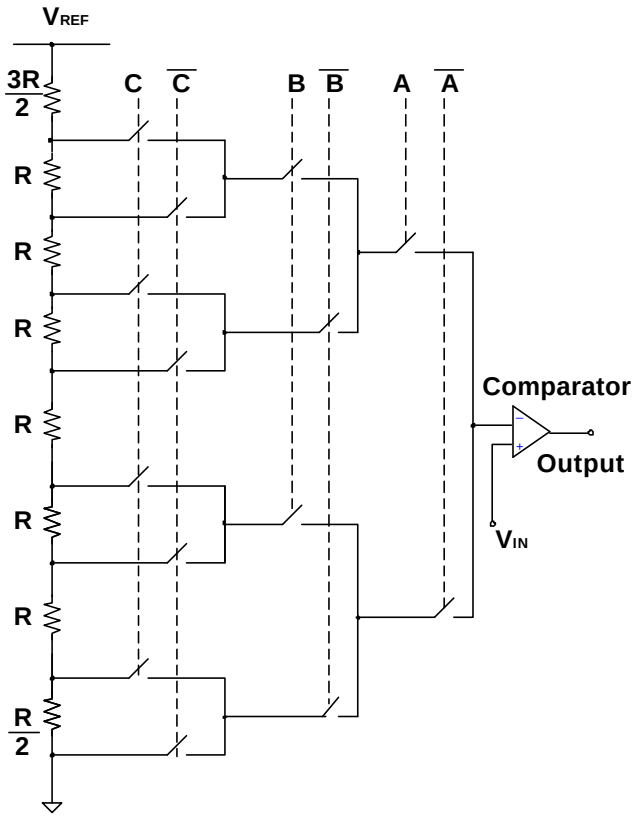
High speed:
(1) Flash ADC
(2) Two-step ADC
(3) Pipelined ADC
(4) Interpolating ADC
(5) Folding ADC
(6) Time-interleaved ADC

§13-2 Successive-Approximation (SA) ADC's

§13-2.1 Resistor-string SA MOS ADC

Ref. : IEEE J. Solid-State Circuits, vol. Sc-13, pp. 785-791, Dec. 1978.

Conceptual 3-bit unipolar ADC



Typical performance of a 8-bit ADC:

p-type resistor	Resolution	8 bit
100Ω/ □ .	Nonlinearity	$\pm\frac{1}{2}$LSB
	DNL	$\pm\frac{1}{10}$LSB
	Conversion time	20 μs
	Input resistance	>1000 MΩ
	Stability (0^o - 85^oC)	<1/4 LSB

Error Sources:

1. Resistor matching accuracy.

   * Dividing the string into several equal lengths and locating them in close proximity.

2. The reverse bias junction voltage of the diffused resistors causes nonlinearity.

   Bit capacity $\uparrow \Rightarrow \Omega/\square \downarrow$.

3. The small on resistance of the switches can decrease the settling time and reduce the feedthrough effect from the gate voltages. Similary, the switch feedthrough only effects the settling time.
4. Major error source: The feedthrough in the switch transistor Q_2.

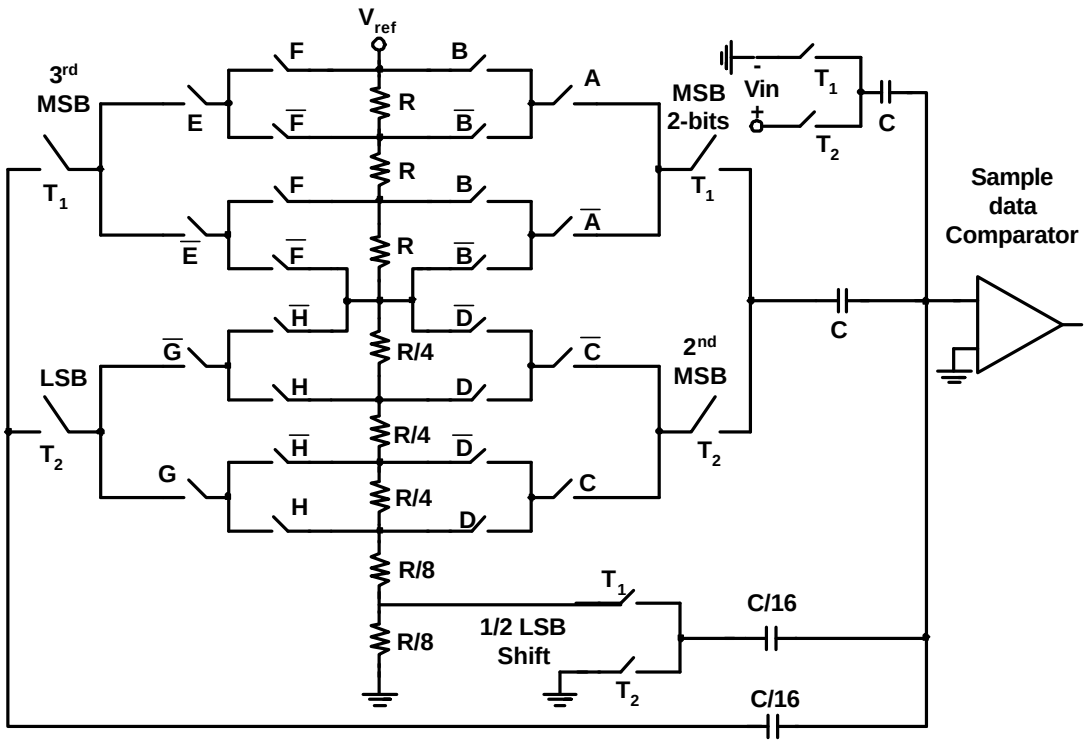
   1 MHz clock $\rightarrow$ 2 mV error.

5. Comparator offset error.

§13-2.2 Charge-Balancing SA MOS ADC

Ref. : IEEE J. Solid-State Circuits, pp. 912-920, Dec. 1979.

* Mixed resistor string and binary-weighed cap.



8-bit ADC C=20pF

Linearity	1/4LSB	Supply Voltage	4.5 - 6.3 V
Conversion Time	100 μs	Current Drain	1.8mA
640 KHz clock		V_{REF} Range	0 - 5 V
Analog Input	0 - V_{DD}	Clock Freq. Range	100 - 800 KHz
Components used:	8R's, 4C's, 32 switches.		

13-bit ADC with laser-cut programmable Si-Cr fuse PROM's.

Post-process triming	＝＞	Linearity	1/2 LSB
		Conversion Time	50 μs
		Analog input	－Vss ~ ＋Vcc
		Clock freq. range	0.1 ~ 3MHz
		Supply voltage	±4.5~±6.3V
		Current drain	5mA

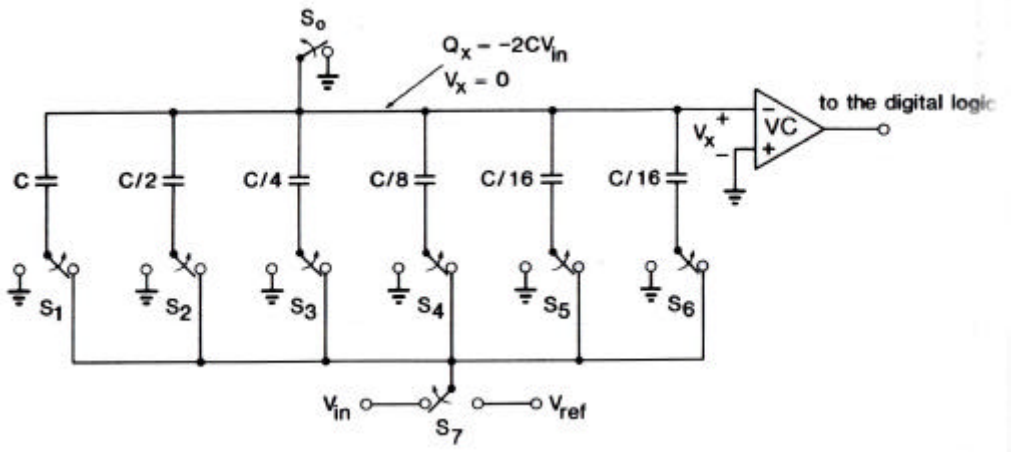
§13-2.3 Charge-Redistribution SA MOS ADC (CRSA ADC)

1. 10-bit CRSA ADC

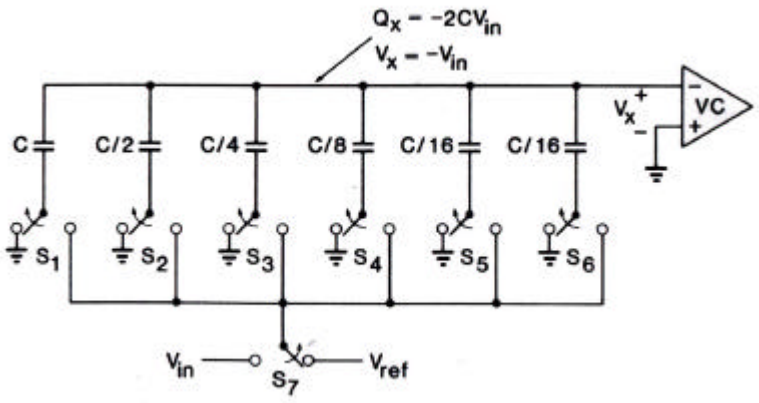
Ref: IEEE JSSC, vol. SC-10, pp. 371-379, 379-385, Dec.1975.

Operation Procedures

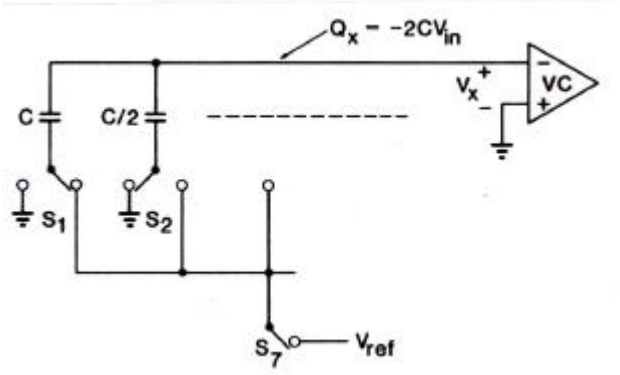
(a) Sample Mode:



(b) Hold Mode:



(c) Redistribution (Approximation) Mode:

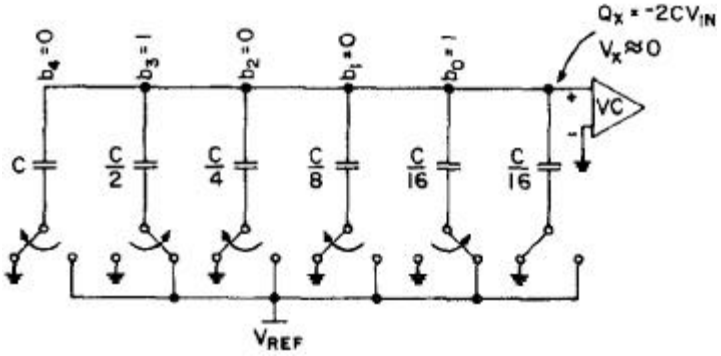


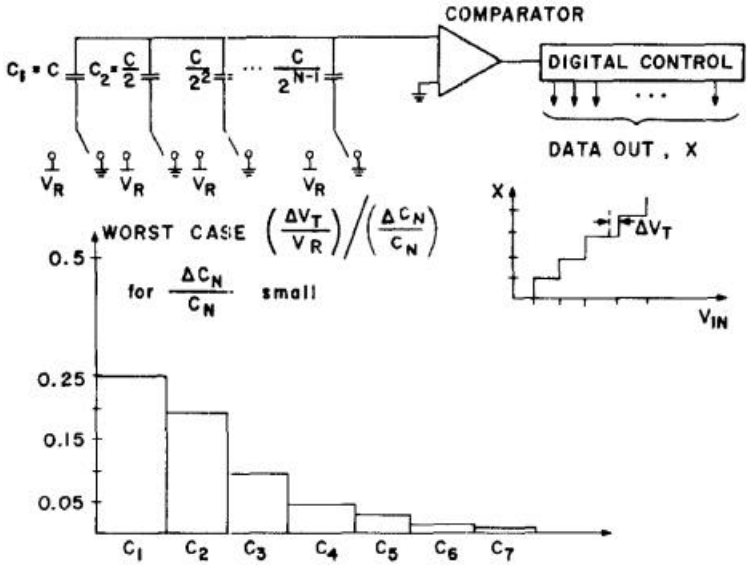
$S_1 \rightarrow V_{ref}$, $Vx = -Vin + V_{ref}/2$

If $Vx < 0$, logic 1 in MSB(b_4), $Vin > V_{ref}/2$

If $Vx > 0$, b_4(MSB)=0, $Vin < V_{ref}/2$ and $S_1 \rightarrow$ ground

Final Configuration:

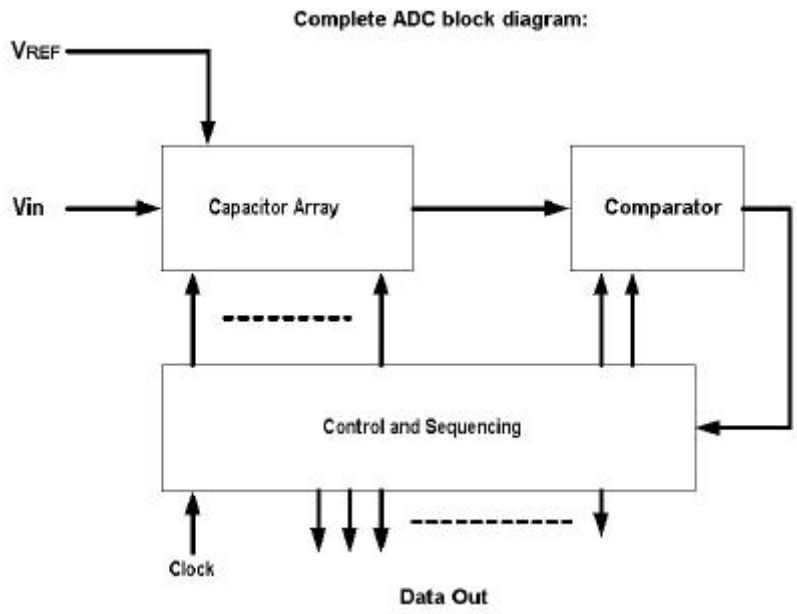




$$Vx = -Vin + V_{ref}\left(+\frac{b_4}{2^1}+\frac{b_3}{2^2}+\frac{b_2}{2^3}+\frac{b_1}{2^4}+\frac{b_0}{2^5}\right) \approx 0$$

$$Vx = -Vin + \frac{V_{ref}}{2^5}(2^4 b_4 + 2^3 b_3 + 2^2 b_2 + 2^1 b_1 + 2^0 b_0),\ V_{in} > 0$$

Complete ADC block diagram:

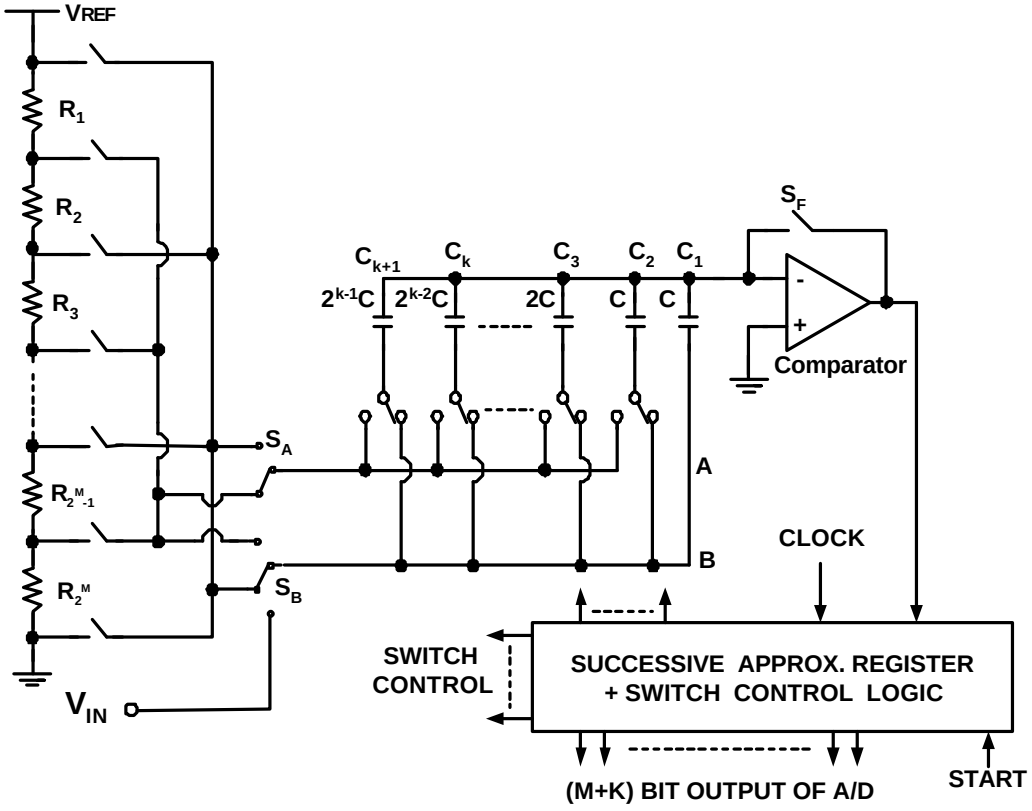


Measured Results:

Resolution	10 bits	Gain error	＜ 0.05 %
Linearity	$\pm\frac{1}{2}$ LSB	Sample mode acquisition time	2.3μs
Input Voltage	0-10 V	Total conversion time	22.8 μs
Input offset	2mV		

2. 12-bit modified CRSA ADC

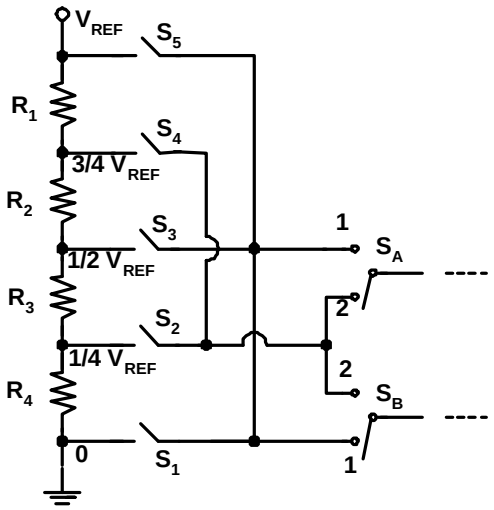
Ref.: IEEE J. Solid-State Circuits, vol. sc-14, pp. 920-926, Dec. 1979.



* SAMPLE

* HOLD

* CHOOSE V_{ref}



V_{in}	Voltage A-B	S_A	S_B	S_1	S_2	S_3	S_4	S_5
Larger	$\frac{V_{ref}}{4}$	-	2		ON	ON		
Smaller	$\frac{V_{ref}}{2}$	-	1			ON	ON	
	discharge	-	1	ON				
	set-up	2	1			ON	ON	
	redistribution	2	1			ON	ON	

Implement:

16 R, 8 ratioed capacitor, 37 MOS

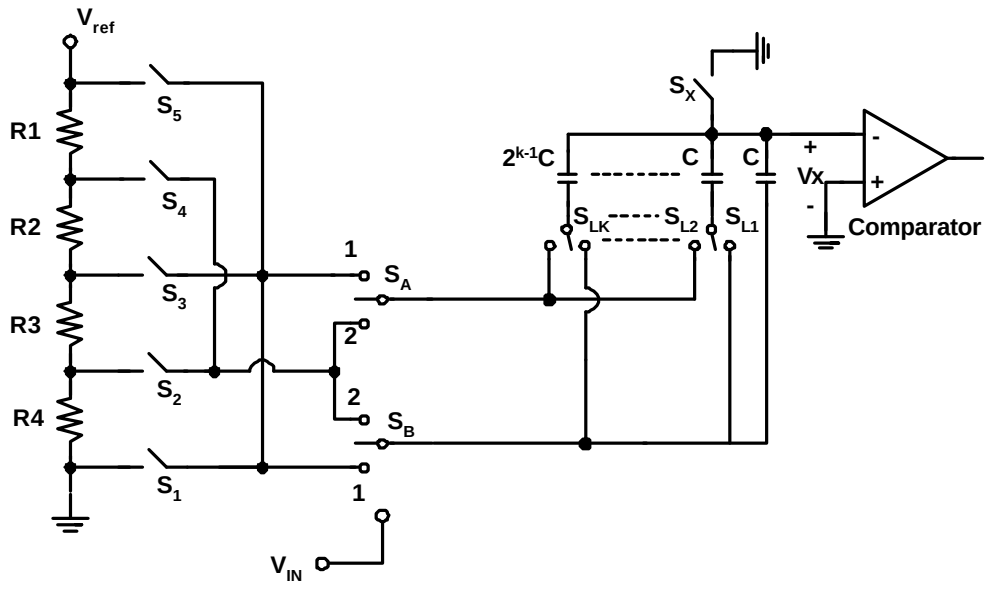
R: S/D diffusion, 18Ω/□ , 16 R= 9000 Ω

C: Unit capacitor, 400 μm^2, 0.1 pF

Measured data:

Resolution	12 Bits	Area	12,000 mil^2
Monotonicity	12 Bits	Power dissipation (15V)	40 mW
Integral Linearity	6 Bits	DNL	$\frac{1}{2}$ LSB
Input. Offset	5 mV	Total conversion time	50μs

Operational Principle:



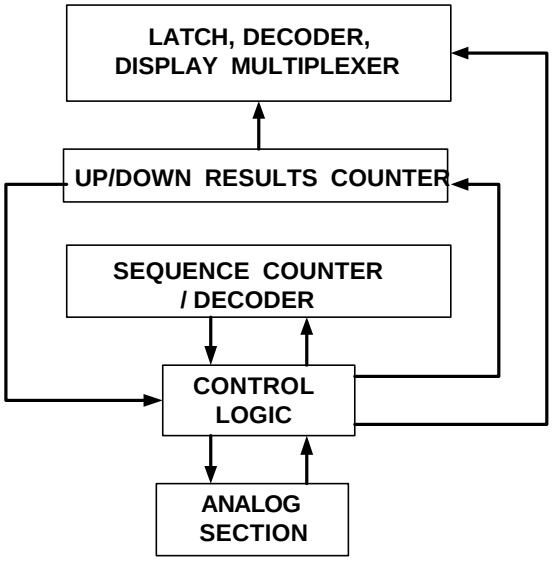
	S_A	S_B	S_1	S_2	S_3	S_4	S_5	S_{LK}	…	S_{L2}	S_{L1}	S_x	V_x
Sample	-	V_{in}	ON	OFF	OFF	OFF	OFF	B	…	B	B	ON	0
Hold	-	1 (0)	ON	ON	OFF	OFF	OFF	B	…	B	B	OFF	$-V_{in}$
Choose V_{ref}	-	2 ($V_{ref}/4$)	OFF	ON	ON	OFF	OFF	B	…	B	B	OFF	$-V_{in}+\frac{V_{ref}}{4}$
	-	1 ($V_{ref}/2$)	OFF	OFF	ON	ON	OFF	B	…	B	B	OFF	$-V_{in}+\frac{2V_{ref}}{4}$
	-	2 ($3V_{ref}/4$)	OFF	OFF	OFF	ON	OFF	B	…	B	B	OFF	$-V_{in}+\frac{3V_{ref}}{4}$
Discharge	-	1 (0)	ON	OFF	OFF	OFF	OFF	B	…	B	B	OFF	$-V_{in}$

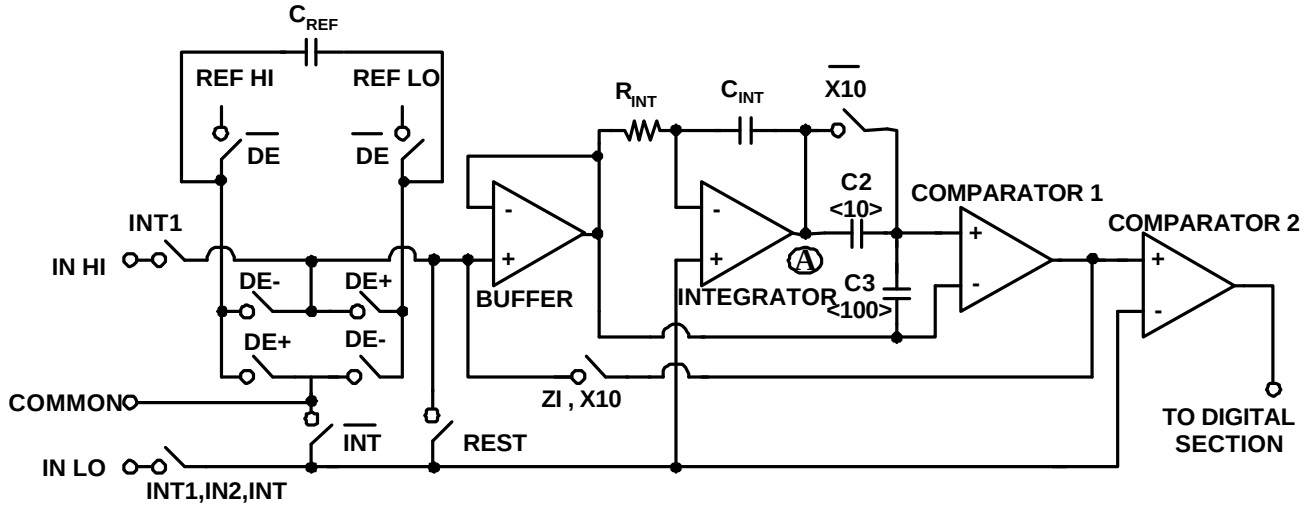
Set up	1 (V_{ref})	2 ($3V_{ref}/4$)	OFF	OFF	OFF	ON	ON	B	…	B	B	OFF	$-V_{in}+\frac{3V_{ref}}{4}$
Redistribution	$-V_{in}+(3/4)V_{ref} < V_x < -V_{in} + V_{ref}$												
	1	2	OFF	OFF	OFF	ON	ON	A	…	B	B	OFF	$-V_{in}+\frac{3V_{ref}}{4}+\frac{1}{8}V_{ref}$

* The last capacitor C is always connected to B.

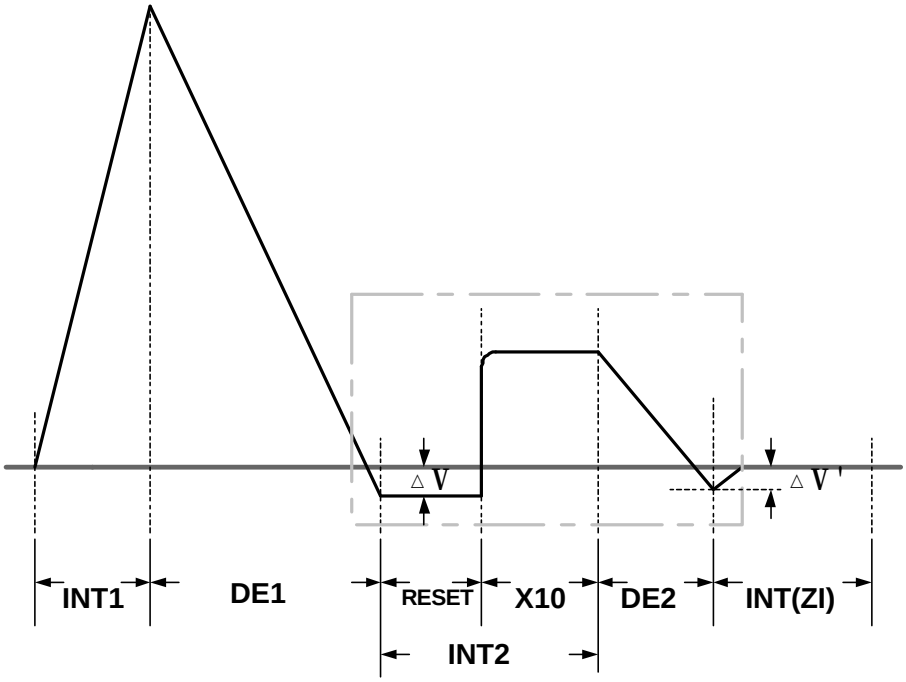
§13-3 Dual-Slope (Integrating; Charge-Balancing) MOS ADC's

$4\frac{1}{2}$ Digit ADC (Modified structure)





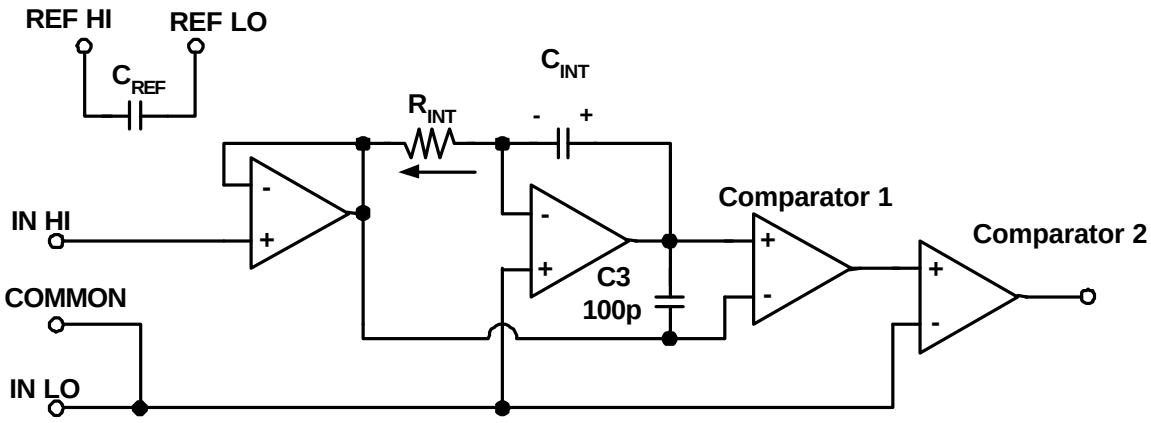
Waveforms observed at the node Ⓐ :



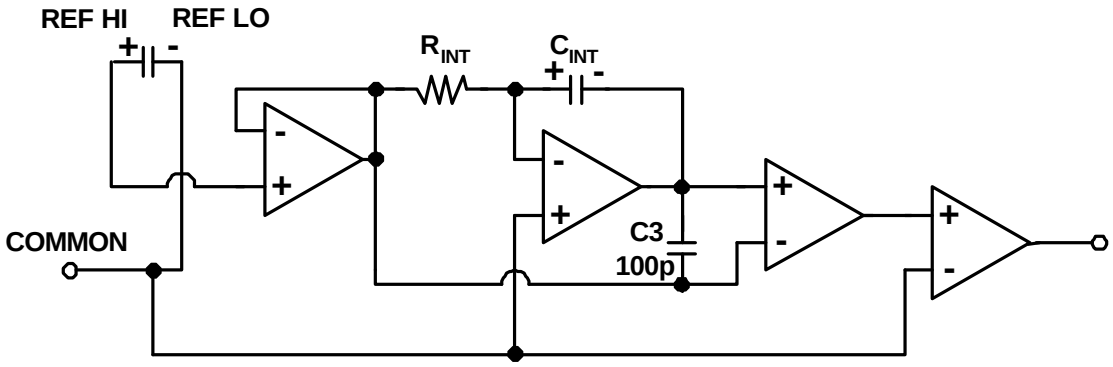
NOTE: ENCLOSED AREA GREATLY EXPENDED IN TIME AND AMPLITUDE

Operational principles:

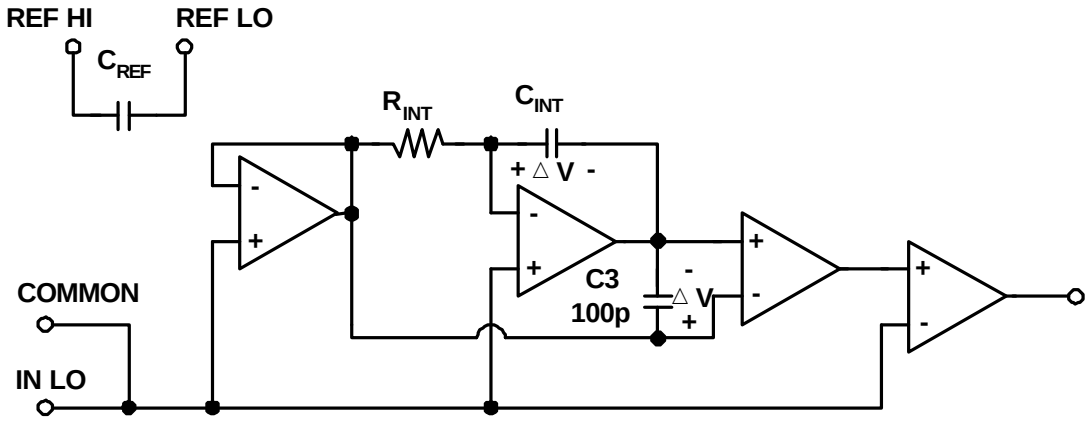
1. INT1



2. DE1

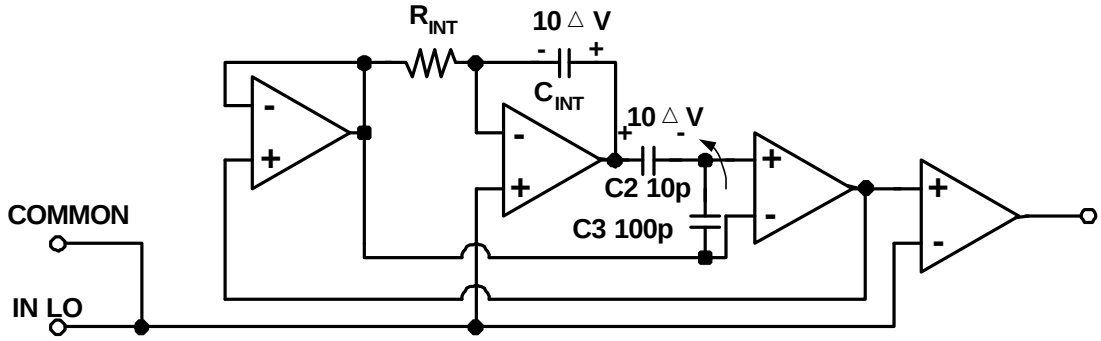


3. REST (INT2)



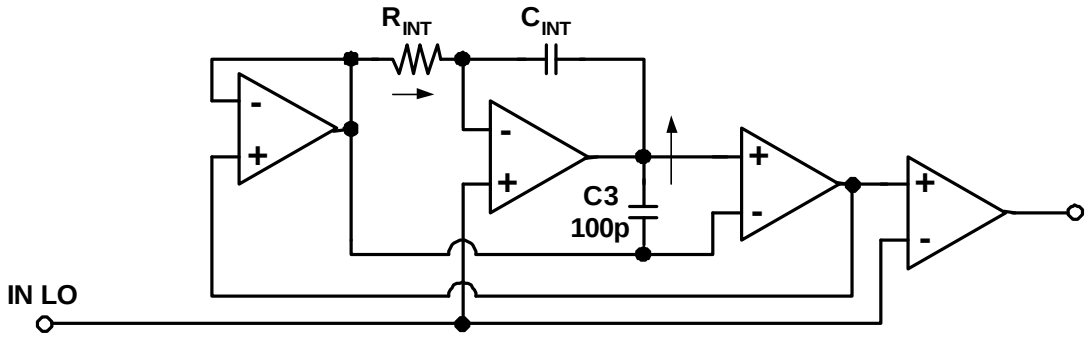
△V：Residual Voltage

4. ×10 (INT2)



5. DE2 (The same as DE1), $\Delta V'$: residual voltage

6. INT(ZI)



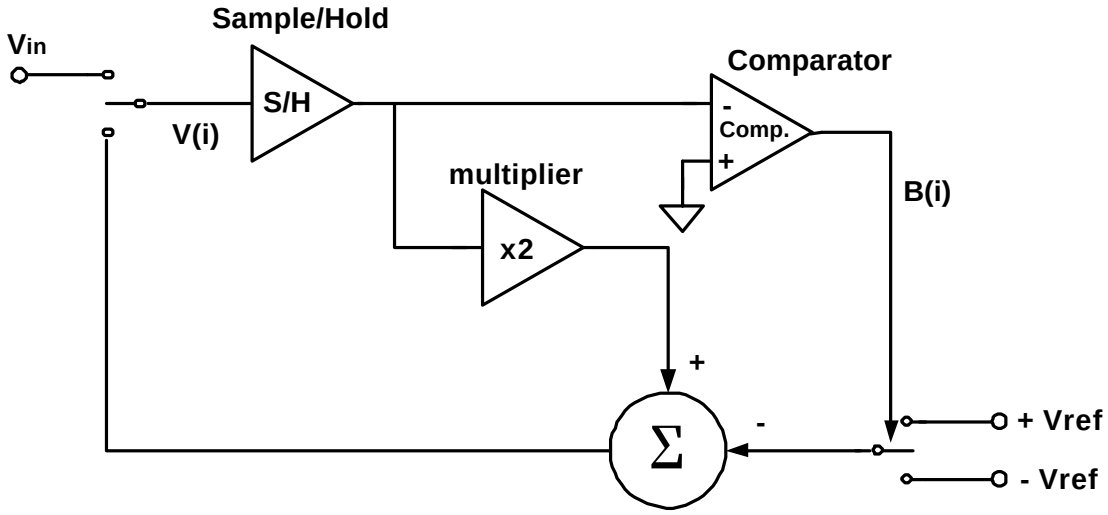
The final residual voltage $\Delta V'$ is effectively reduced to $\frac{1}{10}$ of the original residual voltage without amplification.

$\Rightarrow$ accuracy $\uparrow$

§13-4 Algorithmic ADC

Refs: 1. IEEE ISSCC, Digest of Papers, pp. 96-97, 1977

** 2. IEEE JSSC, vol. 31, no. 8, pp. 1201-1207, Aug. 1996*



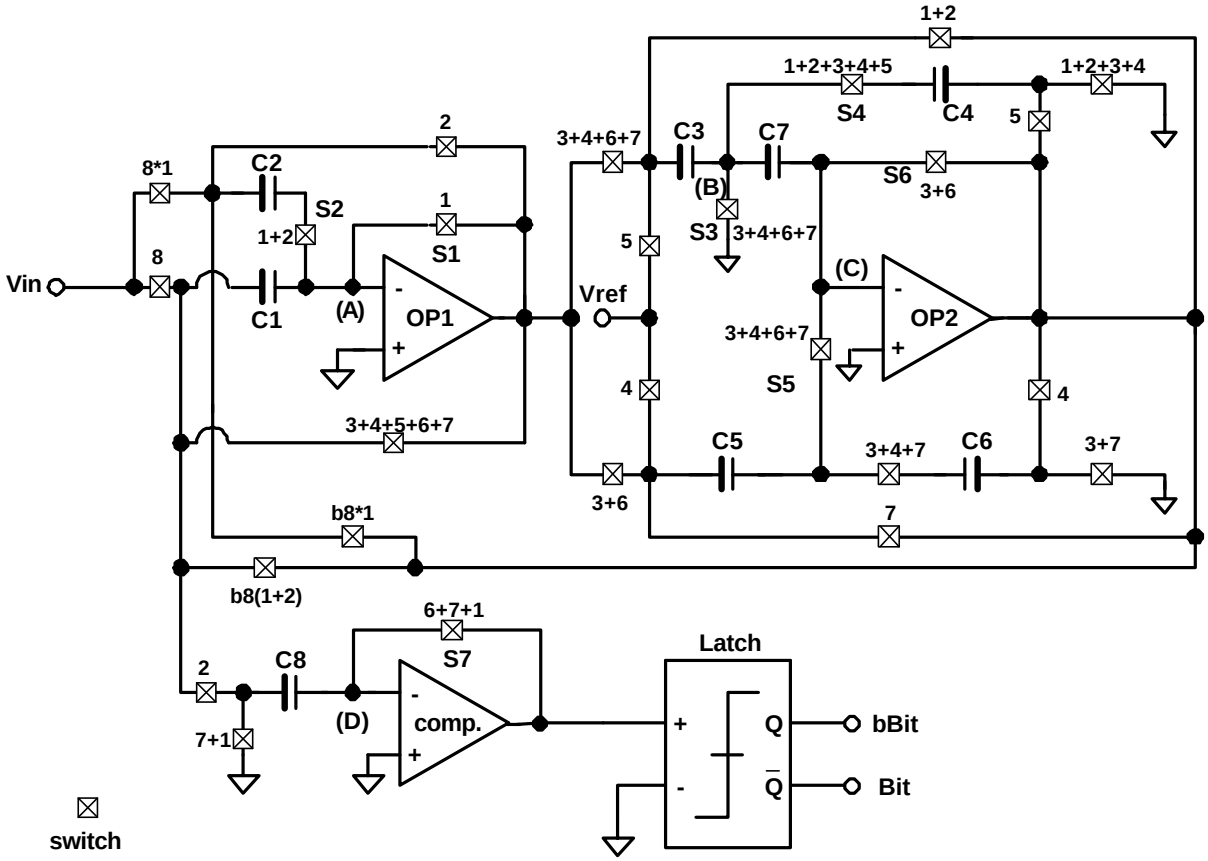
The conceptual block diagram of the algorithmic A/D converter

* The speed is limited by the settling time of OP AMPs used to implement the multiplier.

* For audio ADC applications, it could reach low-power low-voltage operation.

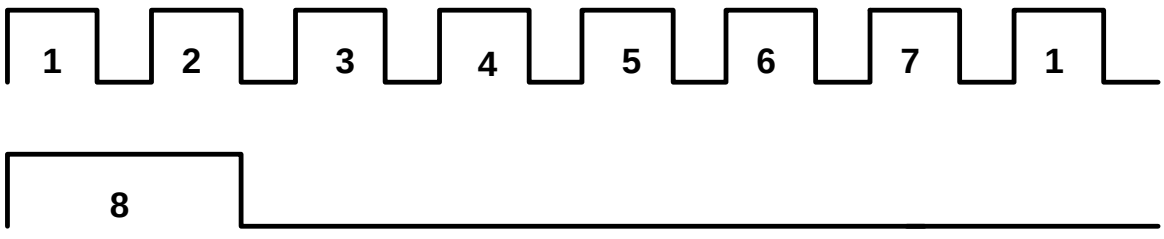
* Major error sources: (1) Capacitor ratio mismatches if SC circuits are used.
(2) Finite-gain error of OP amps.
(3) Offset voltage of OP amps.
(4) Capacitor feedthrough error by switches if SC circuits are used.

Complete circuit of the ratio-independent and gain-insensitive algorithmic ADCs



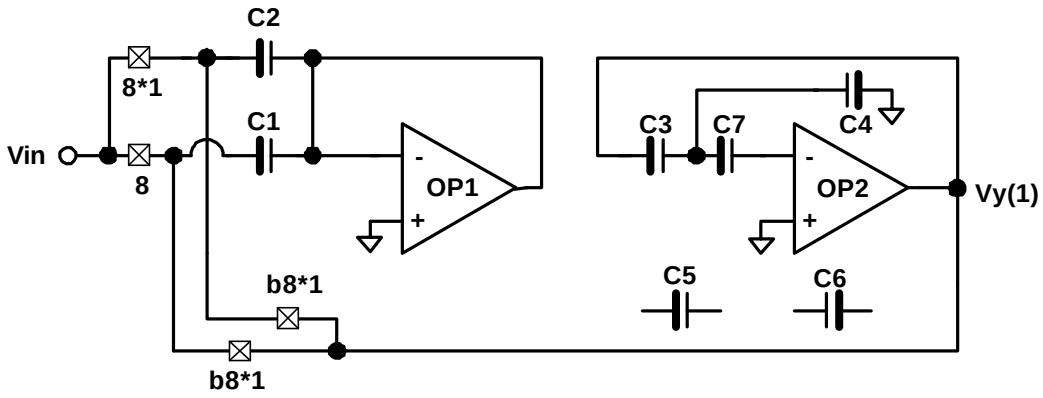
The complete circuit of the A/D converter

Clock waveforms:



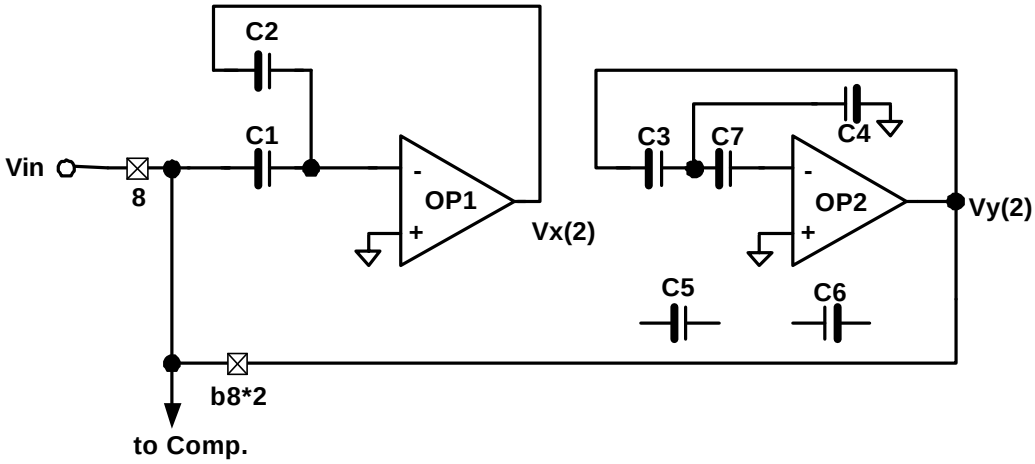
Operational principles:

Step 1:



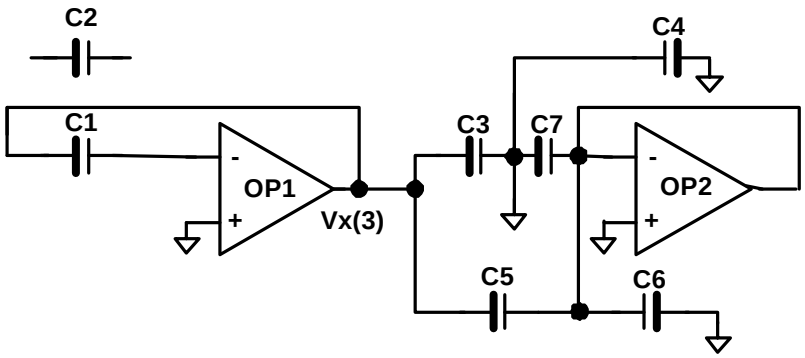
$$Vy(1)\cong\left(2-\frac{13A+20}{(A+2)^2}+\frac{13A+27}{(A+3)^2}\right)Vx(3)-\left(1-\frac{7A+8}{(A+2)^2}+\frac{7A+9}{(A+3)^2}\right)Vref$$

Step 2:



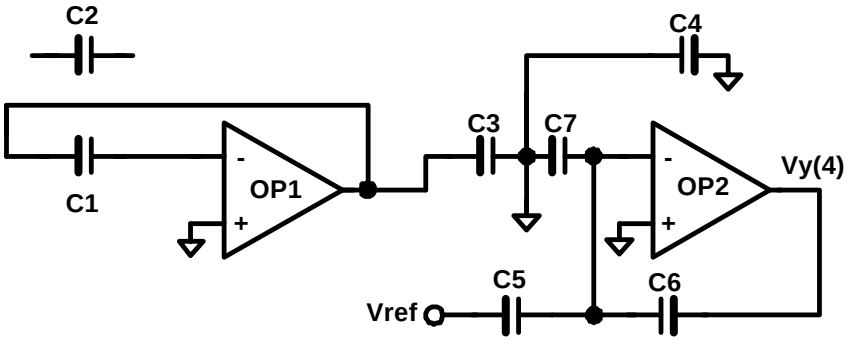
Vx (2) ≅ Vin / (1+2/A)

Step 3:



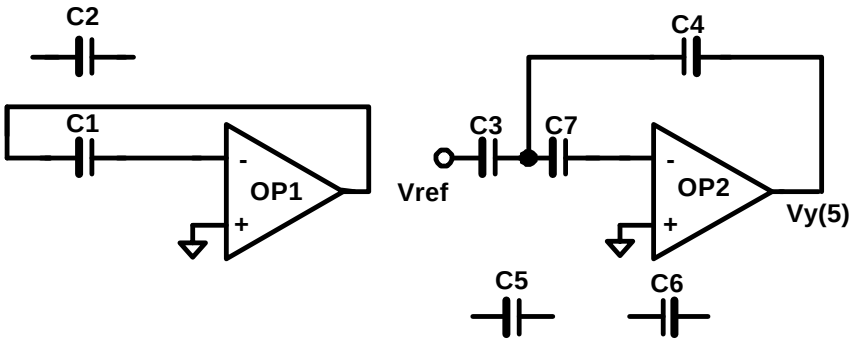
Vx (3) ≅ Vin [1-2/(A^2+3A+2)]

Step 4:



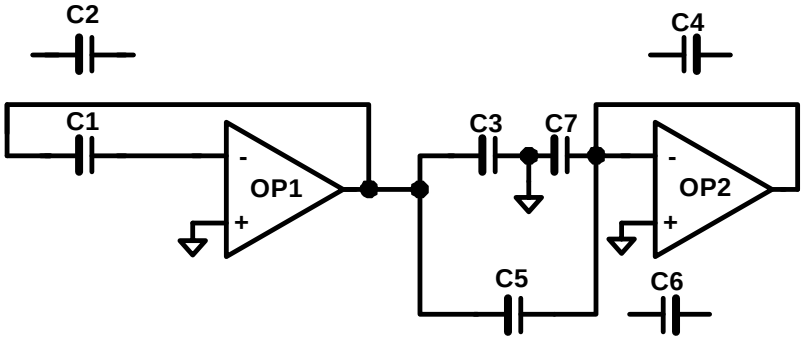
$$Vy(4) \cong \frac{C5}{C6}(Vx(3) - Vref)(1 + 3/A)$$

Step 5:

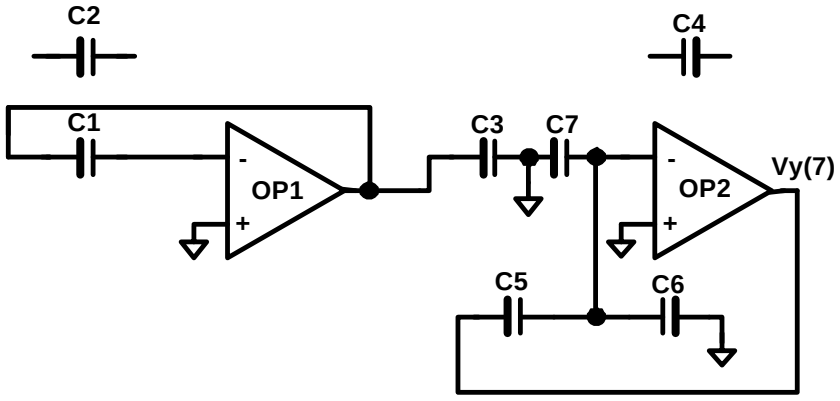


$$Vy(5) \cong \frac{C3}{C4}(Vx(3) - Vref)[1 + 6/(A^2 + 5A)]$$

Step 6:

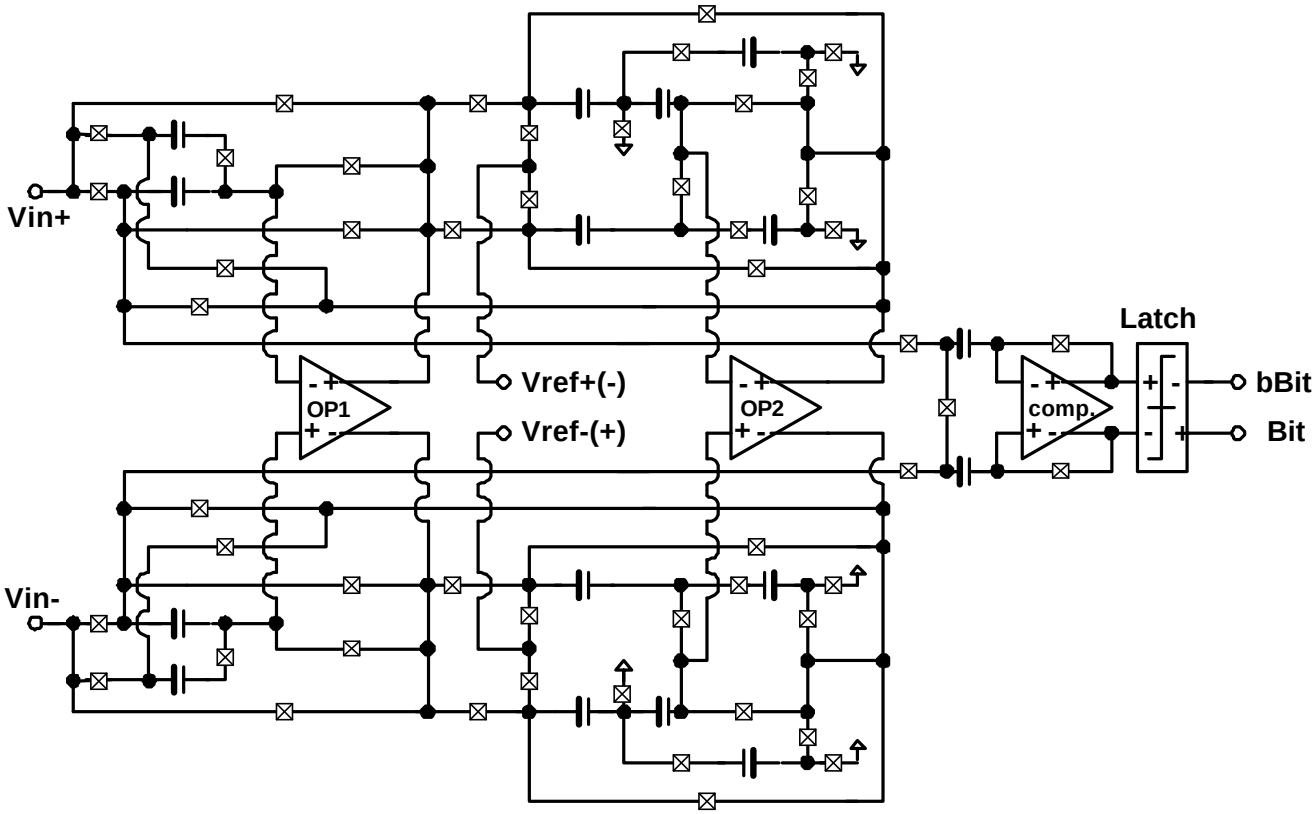


Step7:



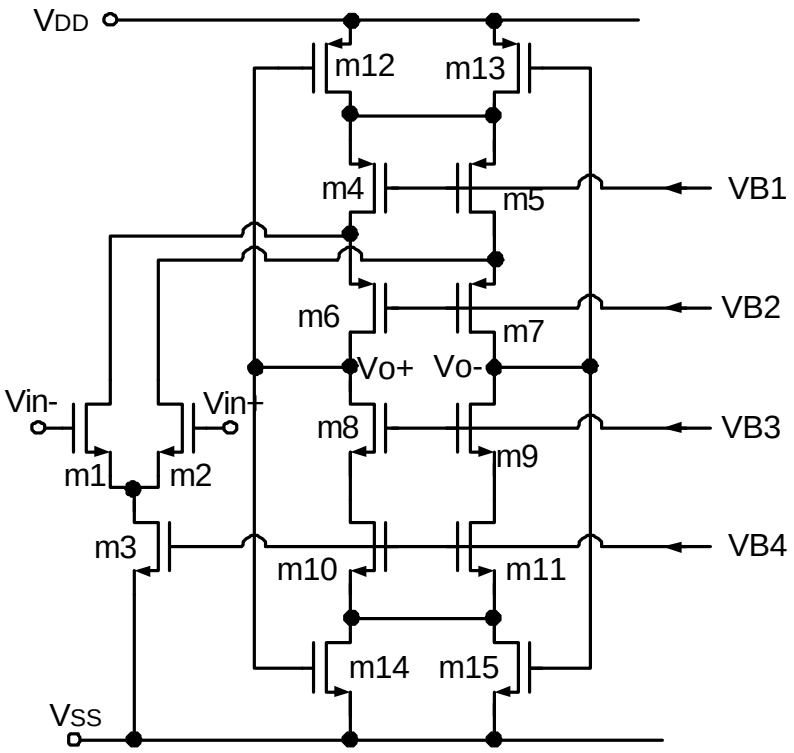
$$Vy(7) \cong \frac{(2-\frac{2}{A+3})Vx(3)-(1-\frac{2}{A+3})Vref}{1+3/A}$$

Fully differential circuits:

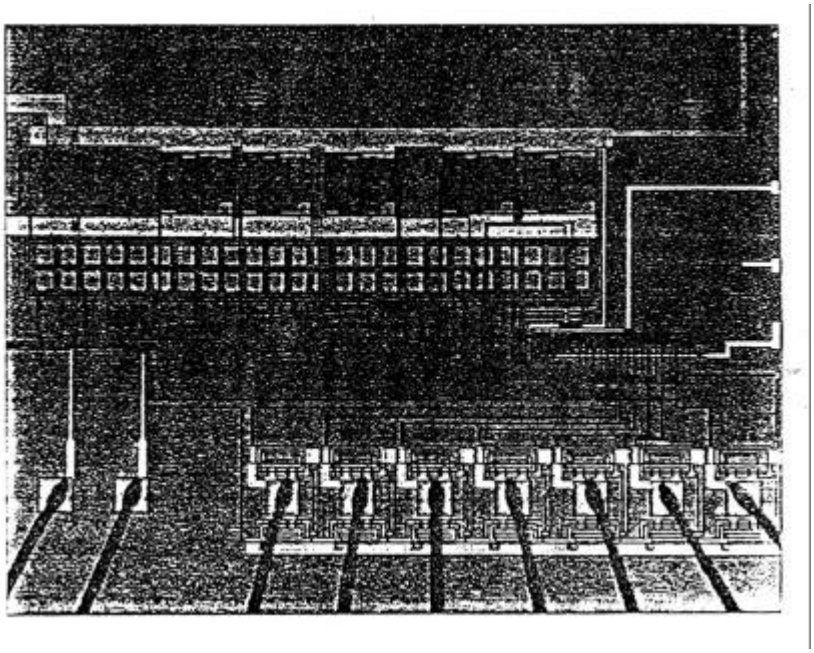


The complete fully-differential circuit of the A/D converter

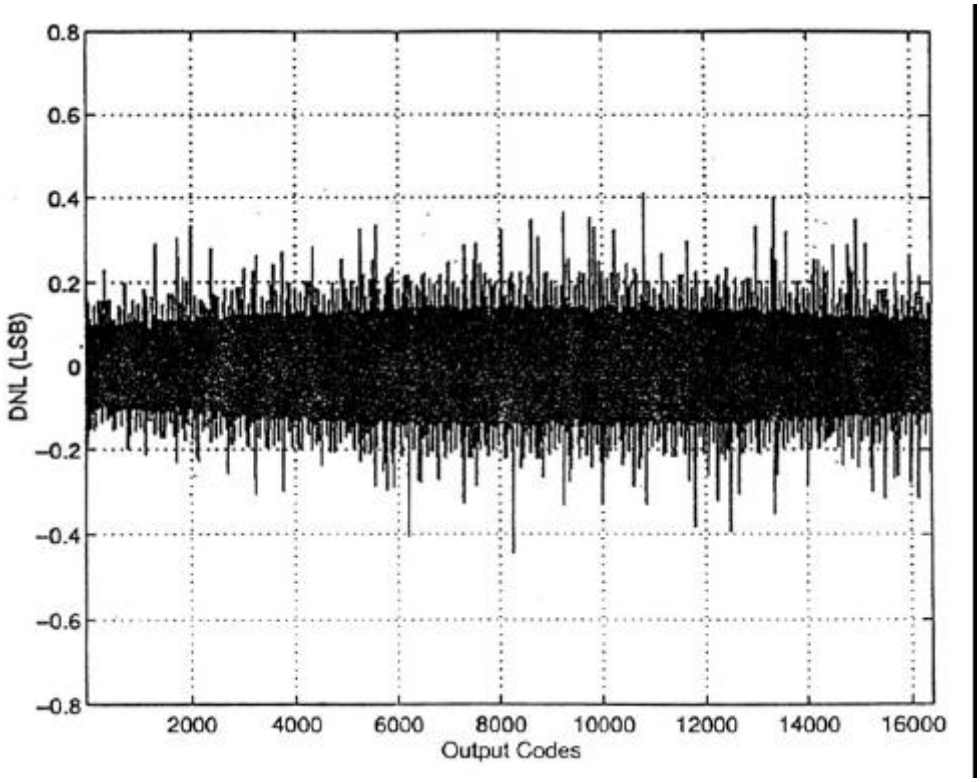
The folded-cascode fully-differential operational amplifier.



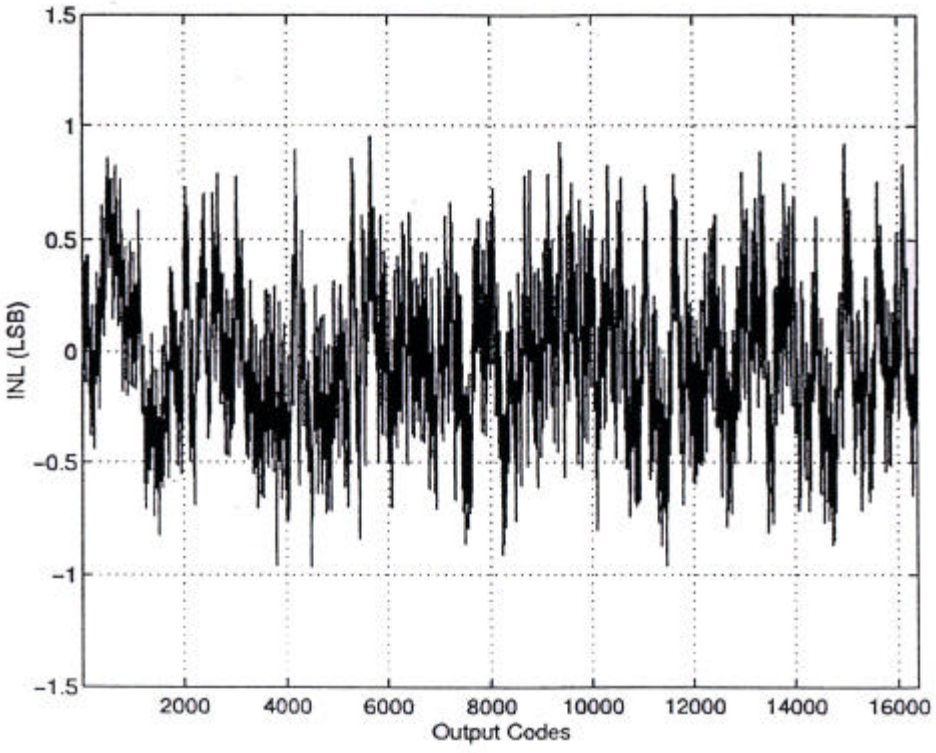
Chip photograph of the A/D converter.



A typical plot of the differential nonlinearity.



A typical plot of the integral nonlinearity.



A typical FFT plot of the A/D converter.

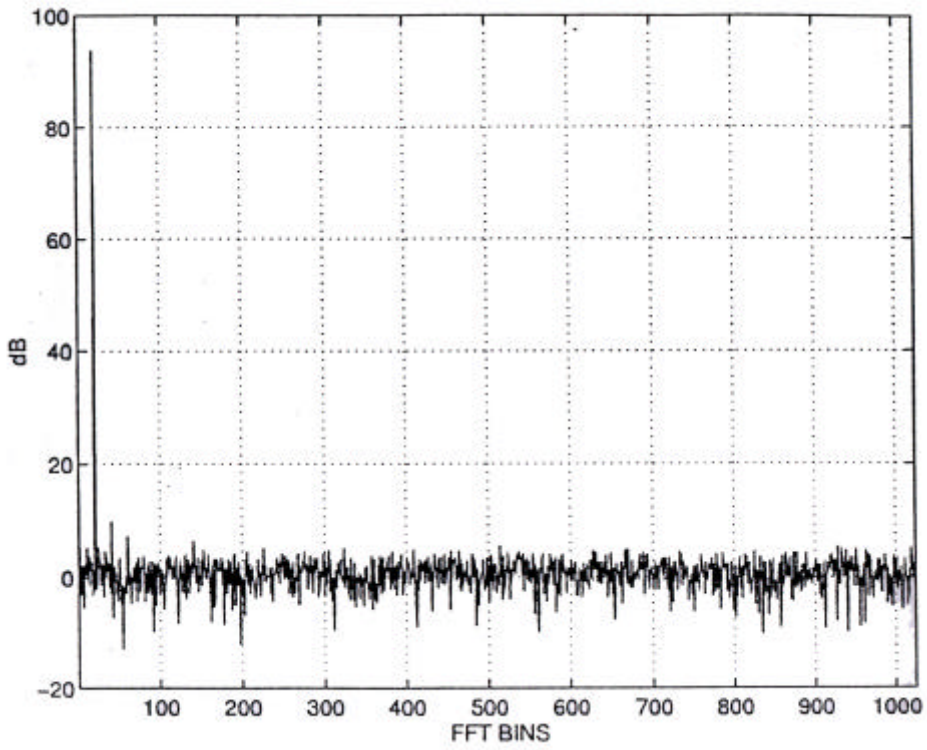


Table I The Experimental results of the proposed A/D converter.

Resolution	14 bits
Differential nonlinearity	＜ ± 1/2 LSB
Integral nonlinearity	＜ ± 1 LSB
Sampling frequency	10 KHz
Gain of op amp	60 dB
Power dissipation	50 mWatts
Supply voltage	± 2.5 V
Process	0.8 μm CMOS
Chip active area	2.1mm × 0.8mm

Table II Comparison of the proposed A/D converter with the previous ratio-independent A/D converters [4.4]-[4.5].

A/D converters / Performance	[4.4]	[4.5]	This work
Resolution (bits)	12	8	14
Absolute INL (LSB)	<= 1.5	<= 0.5	<= 1
OP amp dc Gain (dB)	92	84	60
Clock cycles for n bits	6n	3n	7n
Sampling rate (KHz)	8	8	10
Power dissipation (mW)	17	-	50

§13-5 Full Flash (Parallel)

* Need 2^N-1 comparators for N bits.

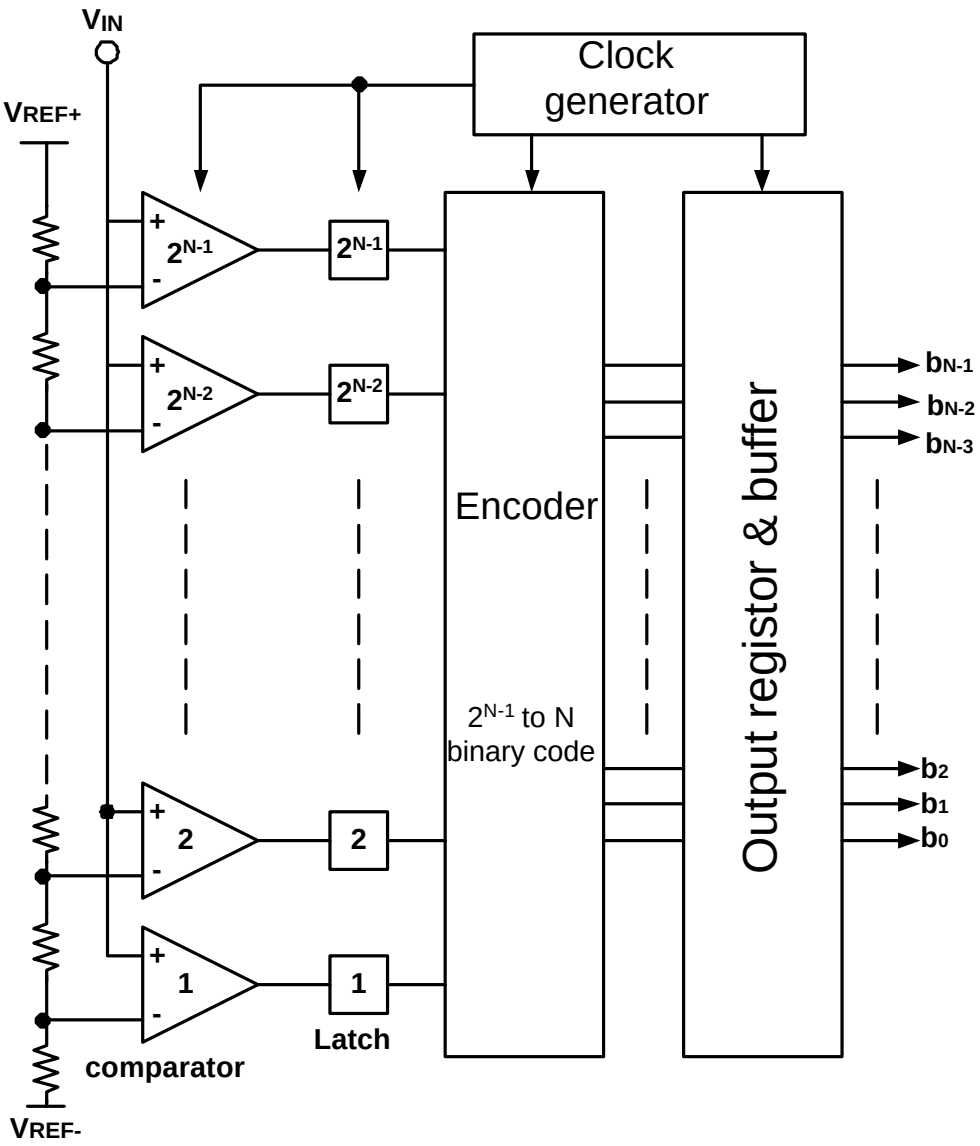
* Need 2^N-1 Resister (R) tapes for N bits.

* S/H usually combined with comparators. (No op amp is required)

? Large no. of analog elements.

? Large chip area & power consumption.

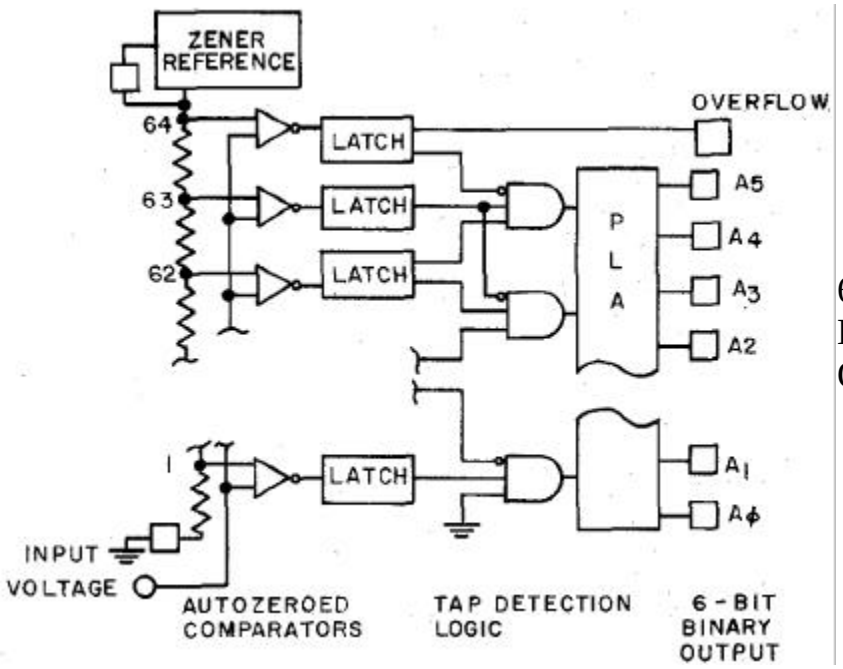
Full-flash A/D converter



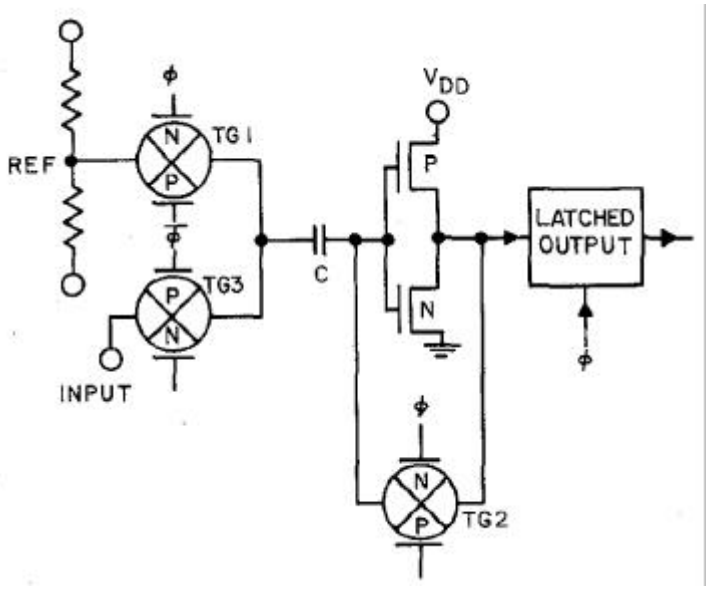
§13-5.1 MOS Flash ADC's

Ref.: IEEE JSSC, vol. sc-14, pp. 926-932, Dec. 1979.

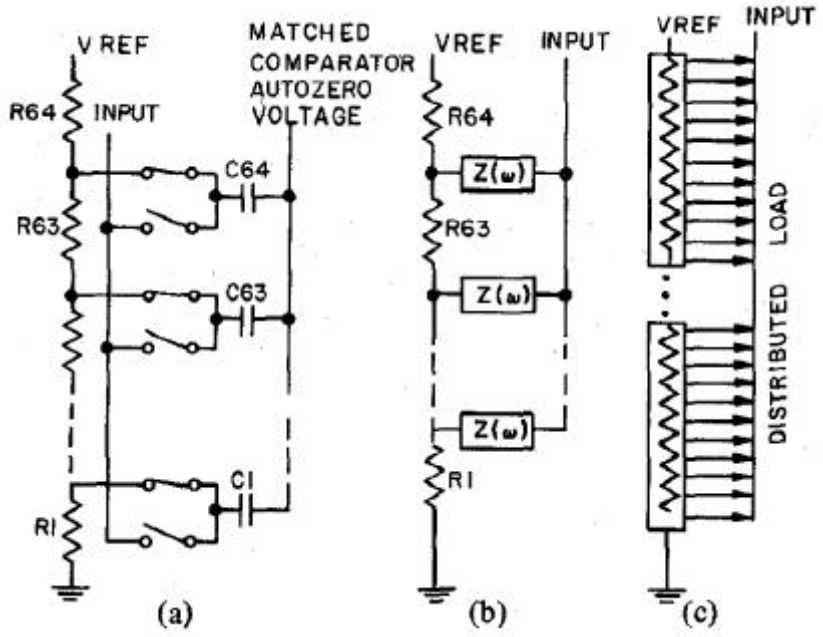
CMOS/SOS 6 bit 20 MHz ADC.



Block diagram of A/D converter chip.



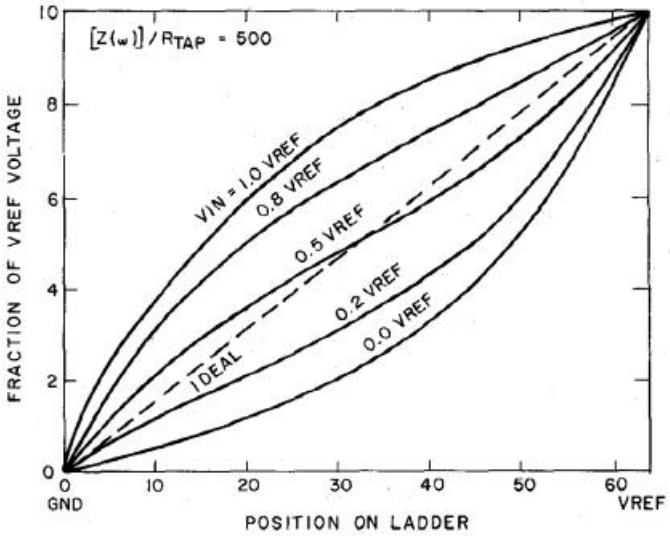
High speed autozeroed CMOS/SOS comparator.



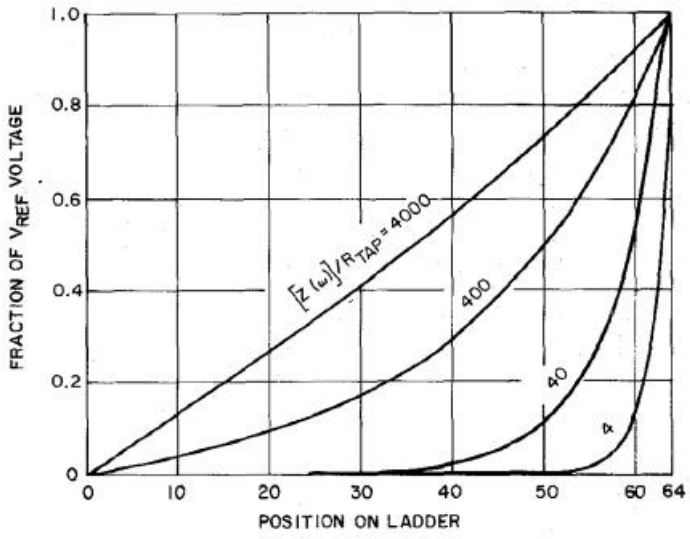
Discrete and distributed reference ladder models

$C_{comp} \leq 0.05$ pF, $R_{TAP} = 20\Omega$

$\left|Z(w)\right| / R_{TAP} \geq 50{,}000$ (< 10,000, don't work)



Reference ladder leading as a function of input voltage
(|Z|(W) /RTAP = 500)



Effect of loading ratio on reference ladder output.

Major source of error is the loading of the reference resistor ladder by the comparator bank.

Resistor ladder loading errors are of two types:

(1) "Transient error" associated with instantaneous ladder loading during a single measurement;

(2) Long-term "recovery error" associated with errors at a new input level after the ladder has been loaded for a long period by inputs at another level.

If the capacitor bypassing is performed at the externally accessable ladder midpoint tap,

$\Rightarrow$ transient impedance $\downarrow$ by a factor of more than 4.

$\Rightarrow$ Worst-case static loading which can't be bypassed makes recovery errors the significant error source.

* All the errors considered above are of this type.

Typical 6-bit A/D converter Performance:

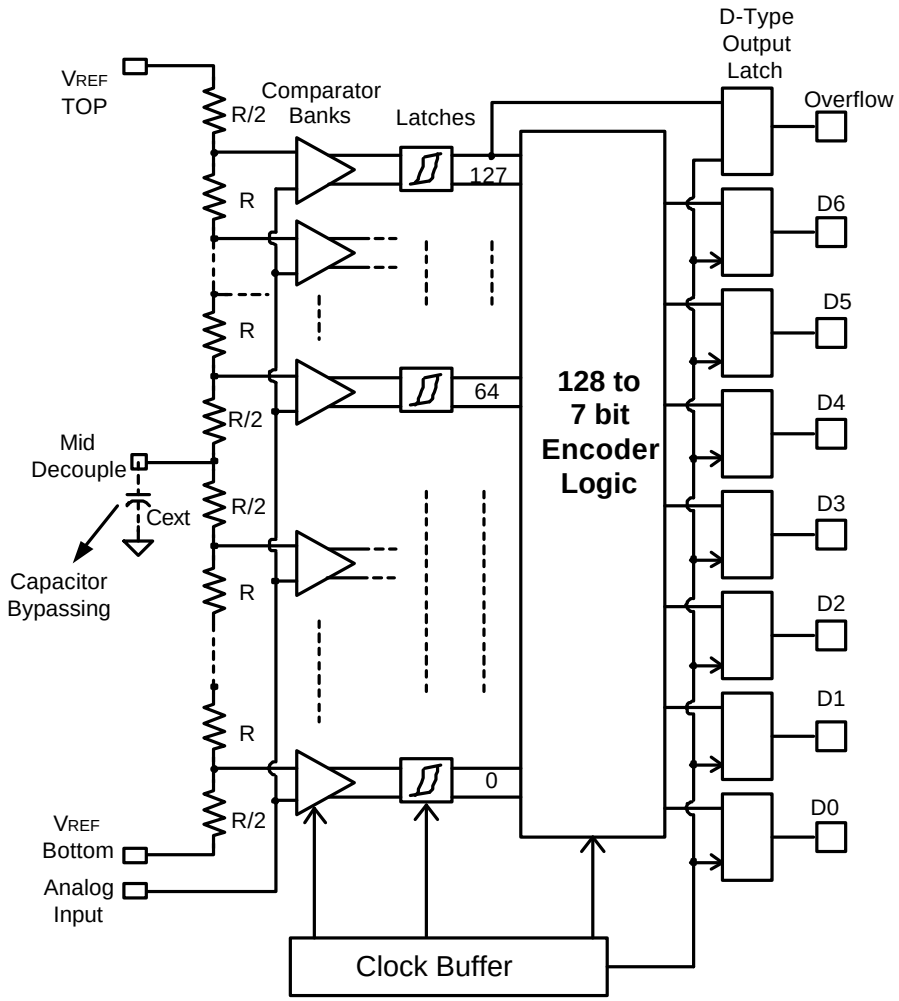
Power dissipation at 15 MHz clock, 20 pF/output.

	5V	8V
convert mode	50mW	145mW
Tracking mode	45mW	130mW
3.2V reference	9mW	9mW
Input Cap.	8 pF	8 pF
Recom. V_{ref}	3.2V	6.4V
On-chip Zener Reference	3.2V	6.4V
Input voltage source resistance	75Ω	75Ω
Accuracy 15MHz	$\frac{1}{2}$ LSB	$\frac{1}{2}$ LSB
20MHz	---	1 LSB
25MHz	---	1.5 LSB

§13-5.2 7-Bit CMOS Flash ADC for Video Applications

Ref.: IEEE J. Solid-State Circuits, vol. sc-21, pp. 436-440, June, 1986

Overall schematic:

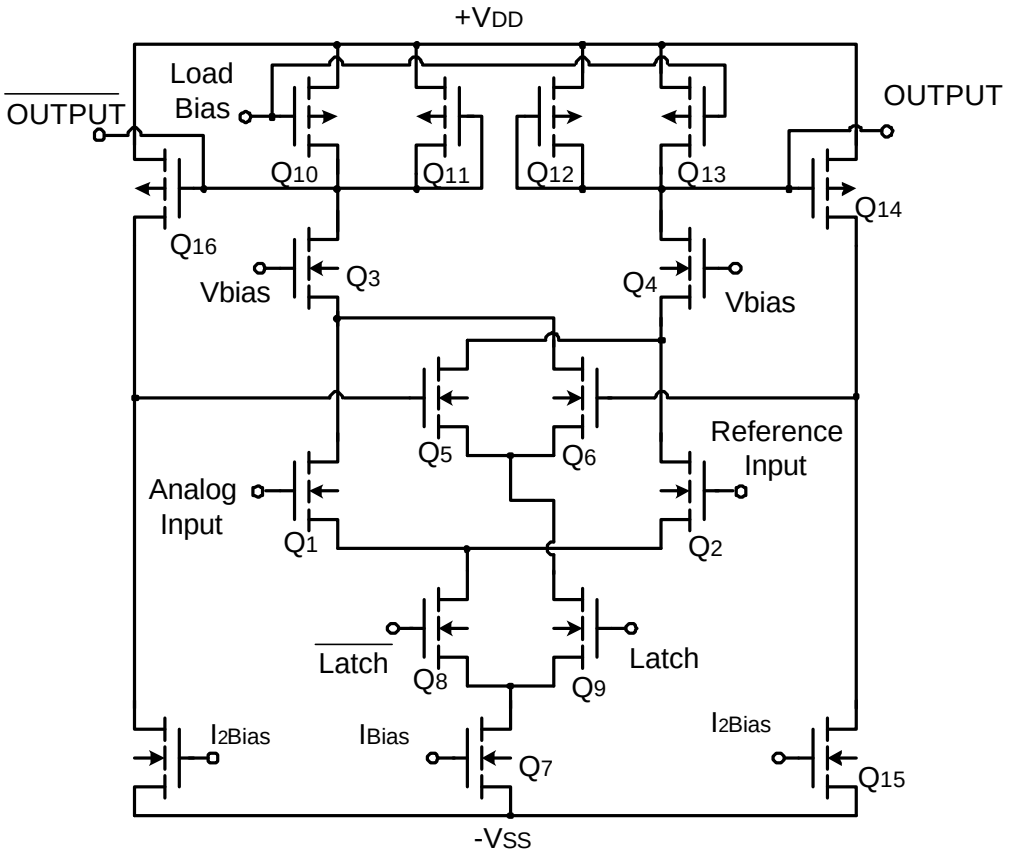


R: Polysilicon resistor, 10 Ω / bit

2μm Poly-gate VLSI CMOS

Overall ship area: 135×142 mil^2

Comparator and the primary latch



Gain: 18dB

Bandwidth: 40 MHz

Q_{10}, Q_{13}: Operated in linear region with on-chip low-power OP AMP and reference loop.

$\Rightarrow$ Ro$\downarrow$, fu$\uparrow$.

Q_5,Q_6: Positive feedback to form latch.

Q_{11}, Q_{12}: To limit the output swing and enable the comparator to recover much faster from the latched state.

The secondary latch is of the hysteresis type, because

(1) it can convert the limited logic swing of the primary latch to correct CMOS logic levels.

(2) it can reduce the amount of hysteresis to ~ 100mV by setting "Latch"

signal to High. Thus the latch always experiences an overdrive of 100 mV.

⇒ Avoid ambiguous state and increase the resolution time of the comparators.

⇒ Reduce metastability error probability

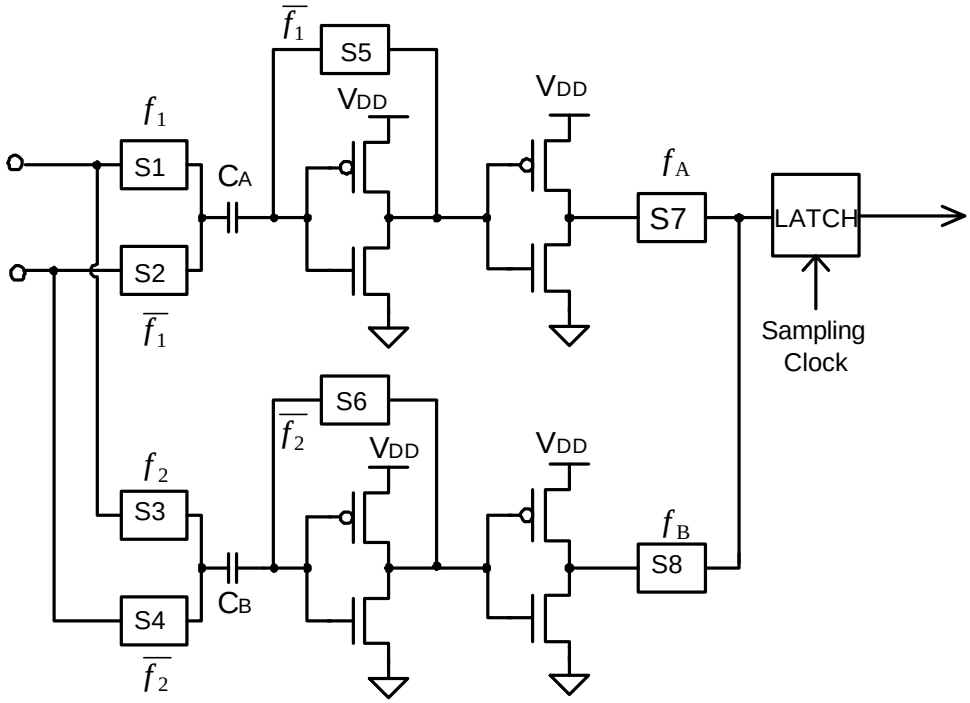
Performance characteristics:

7-bit inherently monotonic	
Accuracy: differential and integral	± 0.5 LSB.
Analog bandwidth	: -3dB 42 MHz; $-\frac{1}{2}$ LSB 5 MHz
Maximum sample rate	: > 22 MSPS, 30 MSPS typically
V_{DD}	: 5V ± 0.5V
Input range	: 1.5V~3.5V
Power consumption (25MSPS)	: 350 mW
Temp. range	: - 40°C to + 85°C

§13-5.3 CMOS 20 MS/S (Maga Samples /sec) 7-bit Flash ADC

Ref.: ISSCC 84, PP. 56-57, 315.

Nonsampling amplifier:

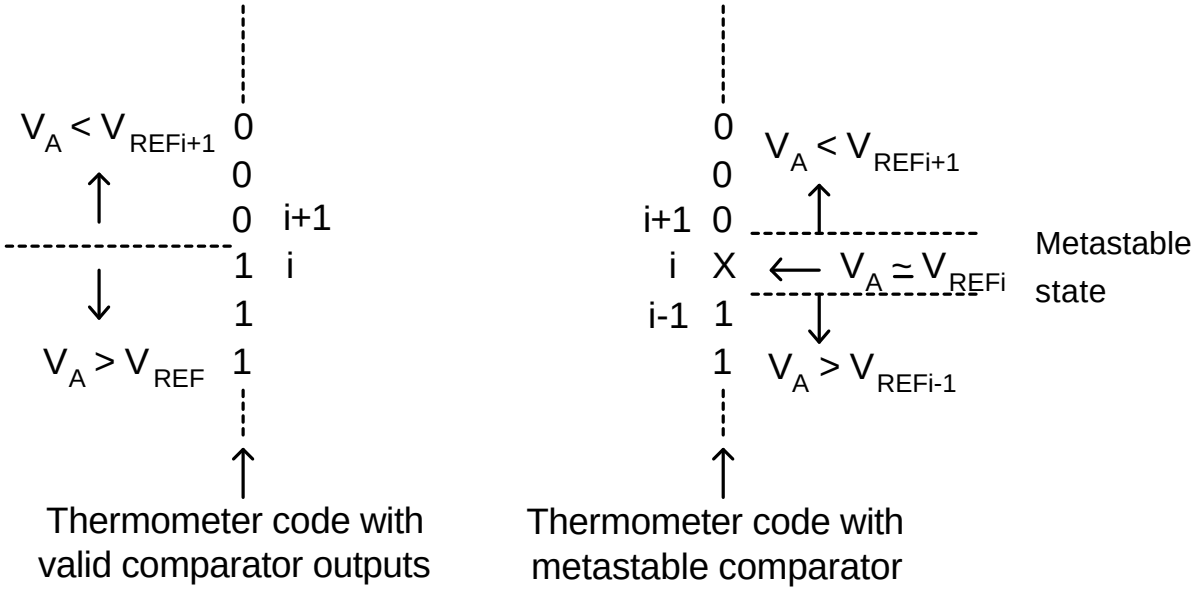


* Higher operating. frequency

§13-5.4 Metastability error

Ref.: IEEE JSSC, vol. 31, pp. 1132-1140, Aug. 1996, 7-b 80-MHz flash ADC

Metastability error: occurs in ADCs when undefined comparator outputs pass through the encoder to the converter output bits.



* Metastability error rate is an exponential function of the sampling frequency.
* It is nearly independent of the input frequency.
* At 70-MHz sampling frequeny, the metastability error rate is ~ 10^{-7} errors/cycle.
  $\Rightarrow$7 errors per second
* Can be improved to < 10^{-12} errors/cycle.

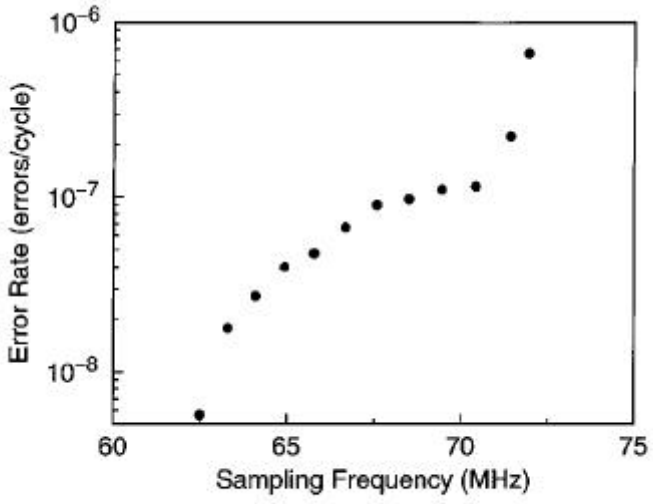
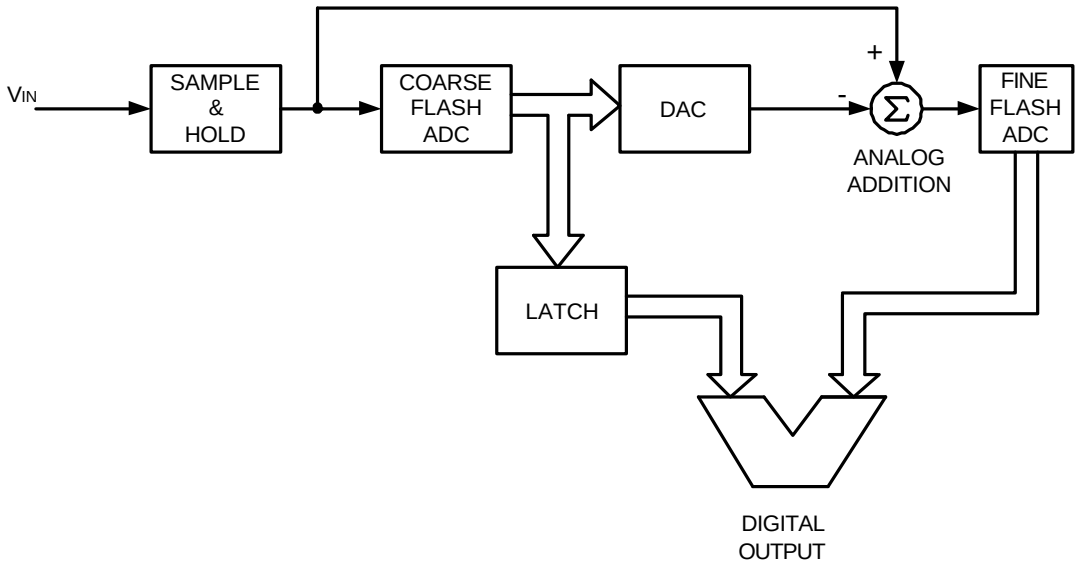


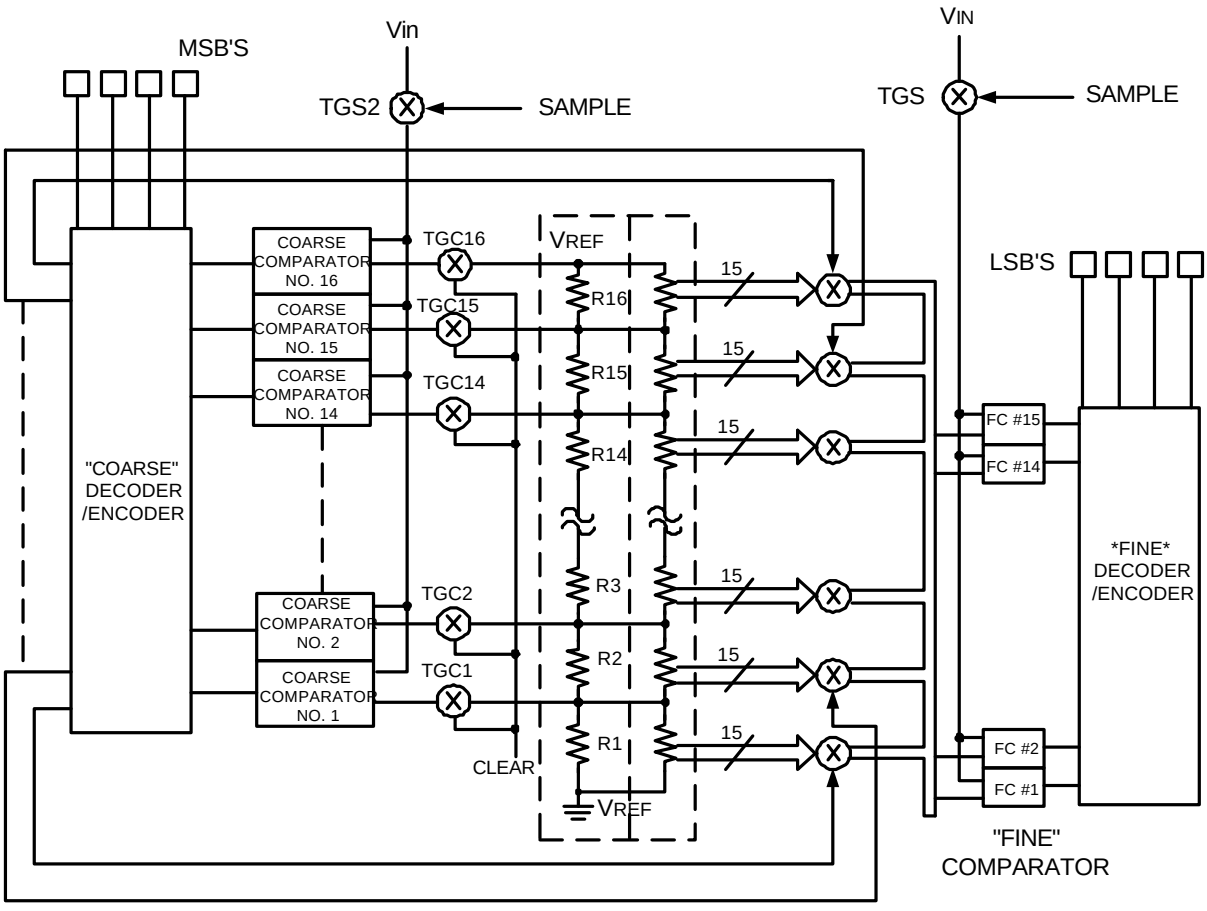
Fig. 2. Measured error rate versus sampling frequency for a 6-b CMOS flash converter with no error correction.

§13-6 Two-Step Flash or Subranging ADC

Conventional two-step A/D converter:



Two-step A/D converter with single resister ladder:



Two-Step Flash ADCs or Subranging ADCs with:

(1) Two Resistor (R) Ladders

* Need $2(2^{N/2}-1)$ comparators & R tapes.

* Need high-performance op amp.

? Nonlinearity caused by the mismatch of the two resister ladder.

? High-performance op amp is not easy to be achieved (especially for 3 V Vdd).

(2) Single Resistor Ladder

* Need 2^N-1 R tapes.

* Need $2(2^{N/2}-1)$ comparators.

? As many R tapes as full flash type.

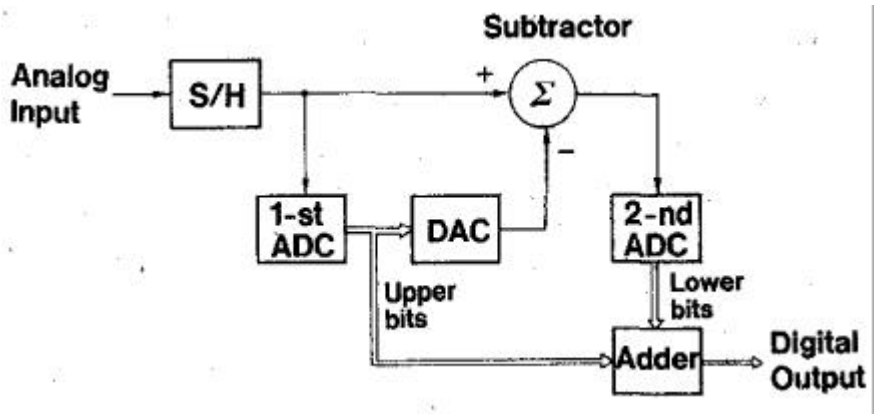
? No op amp is required.

§13-6.1 Subranging (Two-Step Flash) ADCs

8-bit 50MHz CMOS Subranging ADC with Pipelined Wide-Band S/H

Ref.: IEEE JSSC, pp. 1485-1491, Dec. 1989.

Conventional subranging A/D converter:



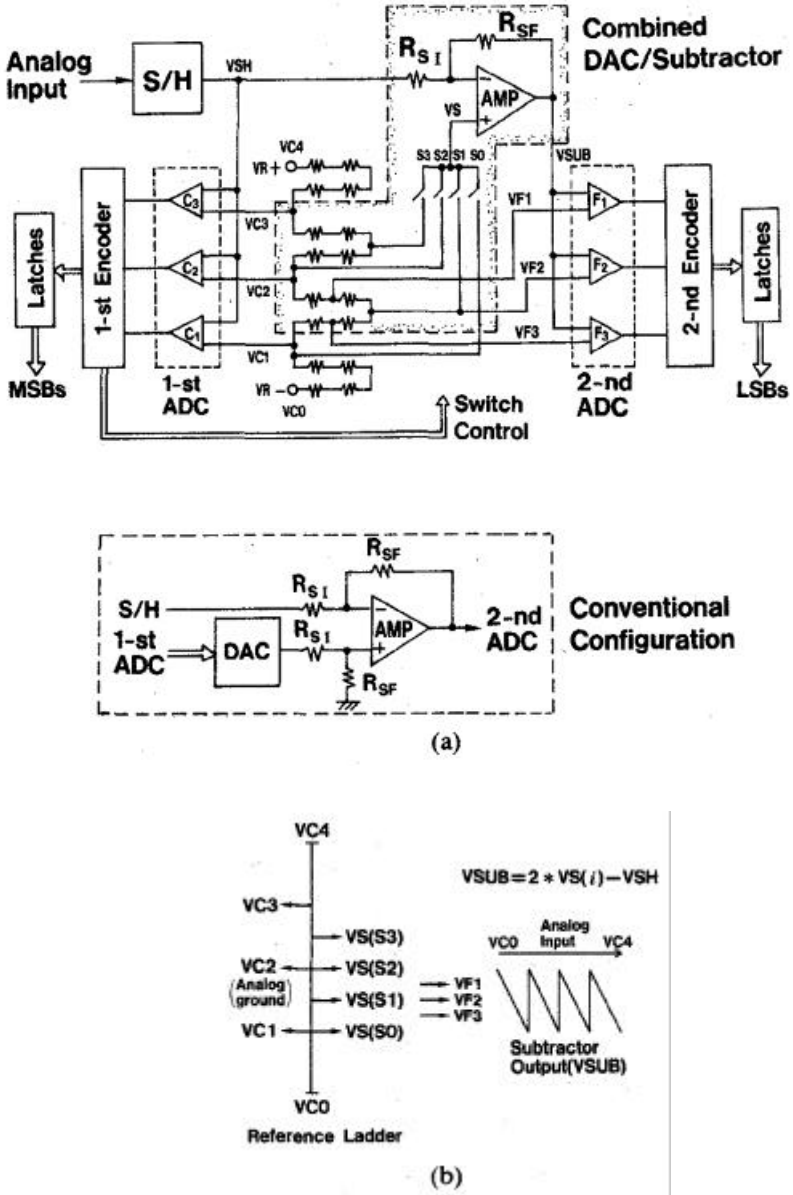
Trade-offs in Subranging and Flash 8-bit ADC

	Flash	Subranging
Total comparators	256	31
Clock cycles/conversion	1	2
Relative speed	1	0.5
Relative input loading	1	0.12
Relative power dissipation	1	0.2
Relative die size	1	0.4
Typ. Differential Linearity Error	0.4 LSB	0.3 LSB
Typ. Integral Linearity Error	0.7 LSB	0.5 LSB

* High accuracy is required only for the S/H circuit and the D/A subconverter. (S/H is to reduce the effect of signal delay differences in the large-area chip.)
* Very difficult to develop a high-speed (video) and high-accuracy MOS S/H circuit.

* The conversion rate degrades. (Pipelined structure may be used)
* The linearity of the complete converter depends on the accuracy of the gain matching among the first A/D, the D/A, and the second A/D subconverters.

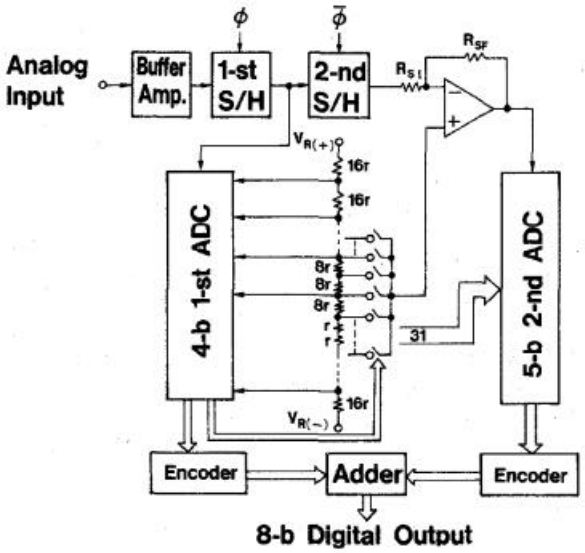
New structure: (4-bit conceptual structure)



Subranging A/D converter using combined DAC/subtraction technique: (a) block diagram and (b) subranging process

* Combined DAC/subtraction Technique
* No current flows through the switches ⇒ No degradation in linearity in DAC
* Amplifiors's settling time < 2 ns

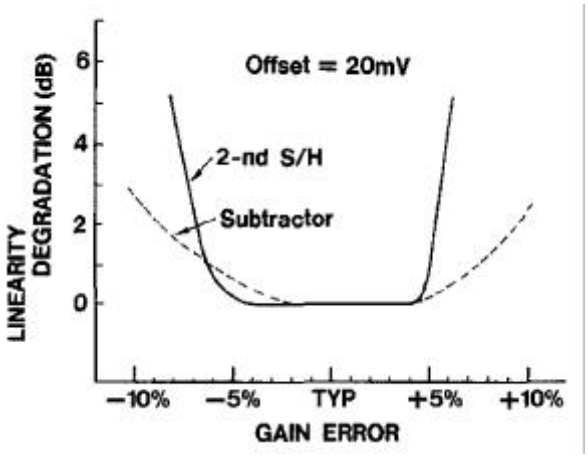
8bit actual ADC:



Block diagram of 8-bit subranging A/D converter

* The 2nd ADC has a fifth bit reserved for digital correction of nonlinearity caused by both offset voltages of the second S/H circuit and the subtractor and nonlinear errors in the first A/D subconverter.
* The two S/H circuits and two A/D subconverters operate in a pipelined manner ⇒ High conversion rate (≥ 2).
* The resistor string has more than 10-bit accuracy.

Gain Matching



Linearity degration caused by gain mismatches in pipelined S/H

Conventional MOS S/H:

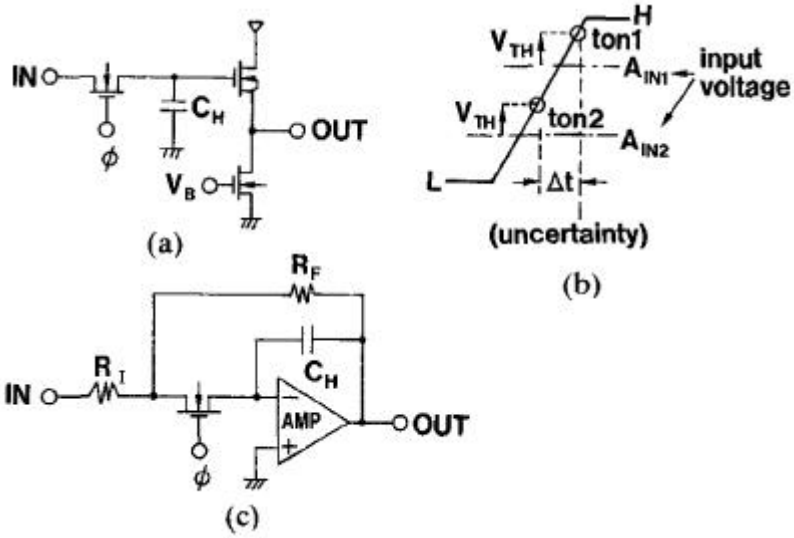
SF:

* The switch opening time is influenced by input voltages ⇒ severe distortion.
* Poor linearity.

Integrator-type S/H:

* The same switch closing time.
* Close loop configuration enhances the linearity.
* Difficult to obtain a fast-settling speed that ensures 8-bit accuracy.

Imposed by the relatively high output resistance of the amplifier and the clock feedthrough error of the MOS switch.

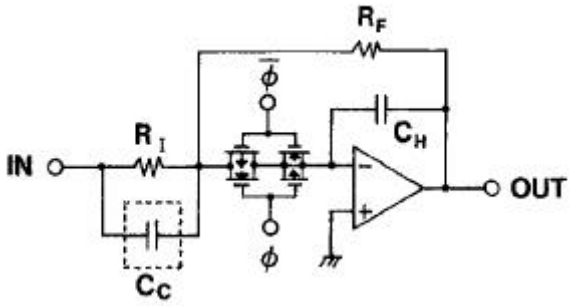


Conventional MOS S/H: (a) source follower type S/H, (b) waveform of clock ϕ and switch opening time deviation for source follower S/H, and (c) integrator-type S/H

New S/H:

* Bandwidth-enhanced integrator-type S/H circuit.
* CMOS transmission gate with dummy transistor (clock feedthrough ↓)
* Compensation

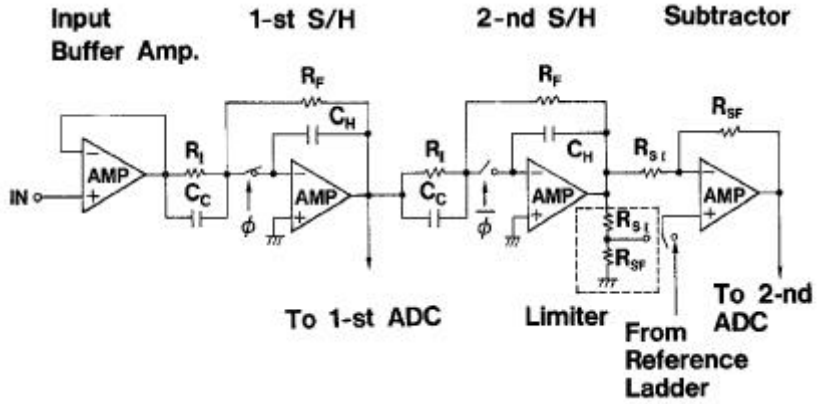
$C_C = \frac{R_F}{R_I} C_H \left(1 + \frac{R_{SW}}{R_1} + \frac{R_{SW}}{R_F}\right)$ pole-zero cancellation. ⇒ Bandwidth↑.



Bandwith-enhanced integrator-type S/H

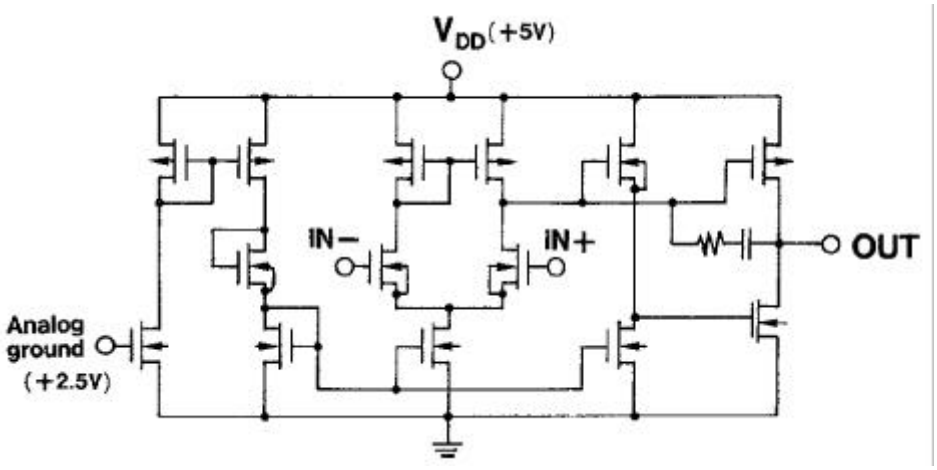
* C_H=1 pF, Cc=1.2 pF, $R_F = R_I$ = 1KΩ, R_{SW} = 100Ω ⇒ 8-bit, 50 MHz.

$T_{settling}$ = 12 ns ~ 8.5 ns for 2V step.



Block diagram of pipelined S/H and subtractor

* The output of the subtractor is set to analog ground by closing the switch for the limiter.

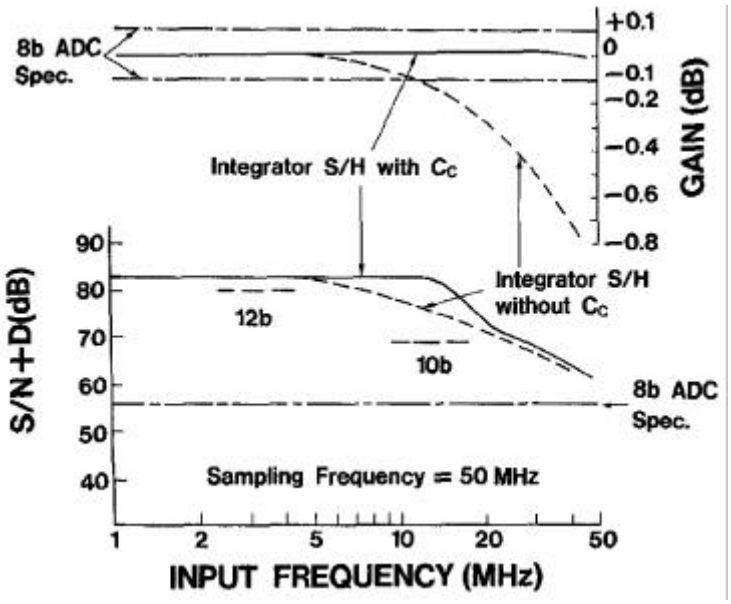


High-speed operational-amplifier circuit diagram

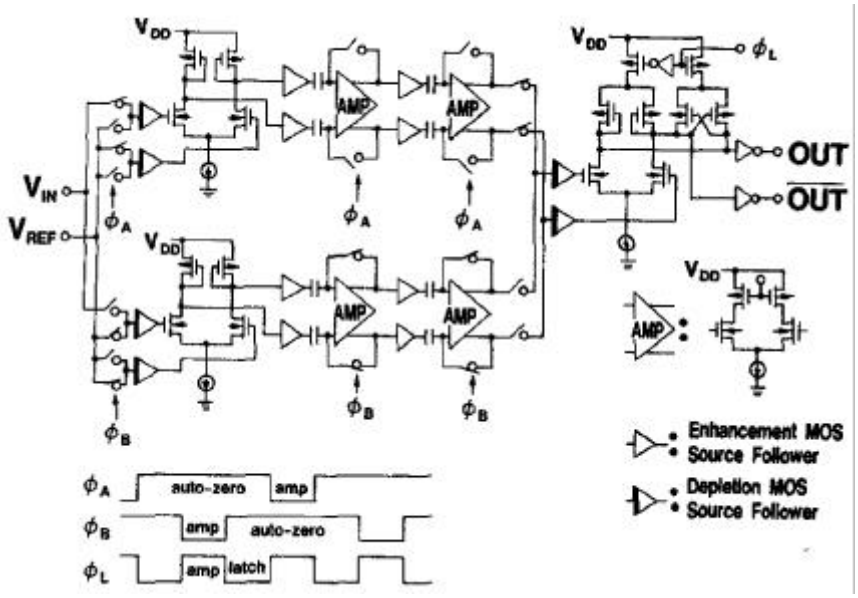
TABLE I
AMPLIFIER CHARACTERISTICS

D C Gain		53 dB
Unity Gain Frequency		380 MHz
Phase Margin		60 degree(*)
Settling Time (0.2%)	AMP	5.4 ns(*)
	S/H	8.5 ns(*)
Power Dissipation		83 mW

(*) Simulation



Simulated linearity characteristics for S/H circuits



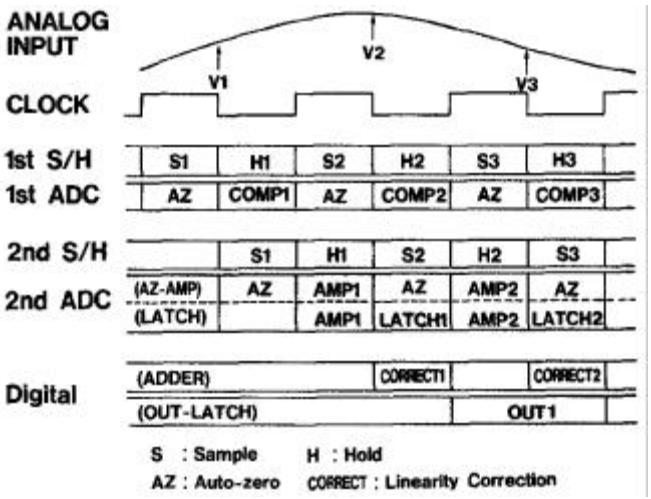
Comparator for the second A/D subconverter

* Comparators for the second A/D subconverter have an inaccuracy $\leq \frac{1}{4}$ LSB.

(3 mV at 3V input)

(FS)

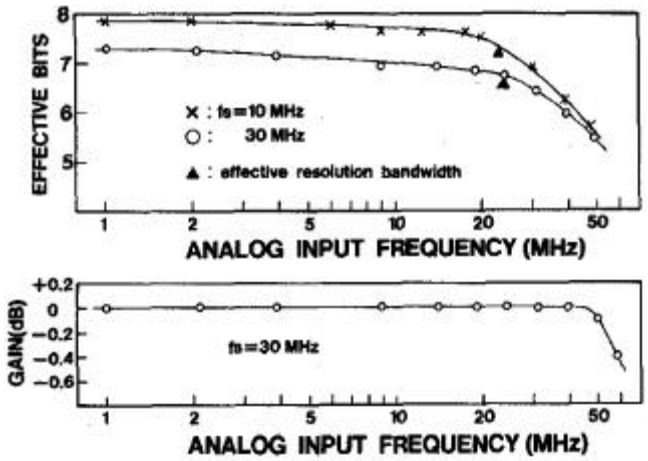
* ≥ 100 MHz with a 7-8 mW power dissipation.



Timing diagram for pipelined subranging A/D converter

Experimental results:

1 μm CMOS, 5V single power supply, sampling rate 50 MHz.



Effective bits and gain as a function of analog input frequency

TABLE II
CHIP PERFORMANCE

Resolution	8b
Conversion rate	50MHz
Effective bits	7.9b (10Msps) 7.3b (30Msps) 6.7b (50Msps)
Effective resolution bandwidth	25MHz
Input bandwidth	55MHz (−0.1dB)
Input capacitance	1.5pF
Power dissipation	600mW (5V power supply)
Chip size	3.2×4.3mm

§13-6.2 10-bit 5-MSPS CMOS Two-Step Flash ADC

Ref.: IEEE JSSC, vol. 24, no. 2, pp. 241-249, Apr. 1989.

1. Classical two-step flash ADC
 * Limited by matching between the MSB ADC and DAC transitions
 * Limited by op-amp settling time (conversion rate)

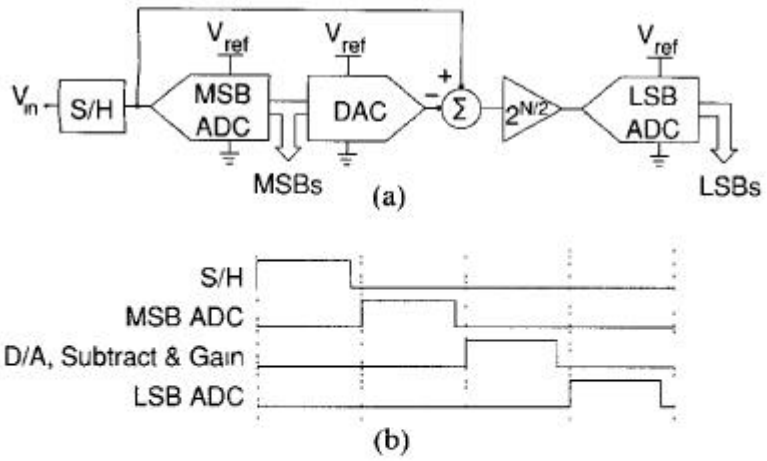


Fig. 2. (a) Classical two-step flash ADC block diagram limited to bipolar technology. Limitations include matching the MSB ADC and DAC transitions otherwise missing codes and nonlinearity may result. (b) Timing diagram for the classical two-step flash ADC. Although the four phases are shown as equal length, the subtraction and gain are the slowest. They are limited by op-amp settling time and limit the conversion rate.

2. New structure
 * No OP amps.
 * No gain block

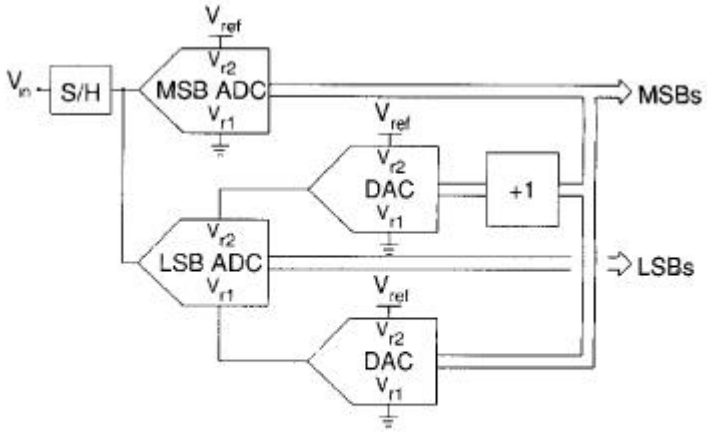


Fig. 3. Prototype subranging ADC block diagram. Notice that there are no op amps. The timing is similar to that in Fig. 2(b). The ADC's and DAC's share components to eliminate matching requirements among them.

3. Circuit implementation

TABLE I
CIRCUIT DESIGN PROBLEMS AND SOLUTIONS

Problem	Solution
Digital Compatibility	5-V Operation
Power Supply Noise	Fully Differential Circuits
Charge Injection Errors	Fully Differential Circuits
Monotonicity	Cancel Comparator Offset
Fast, High-Gain Comparator	Multistage Comparator

* Shared binary weighted capacitor array for the MSB ADC and DAC and the LSB ADC.
  ⇒ mismatches ↓

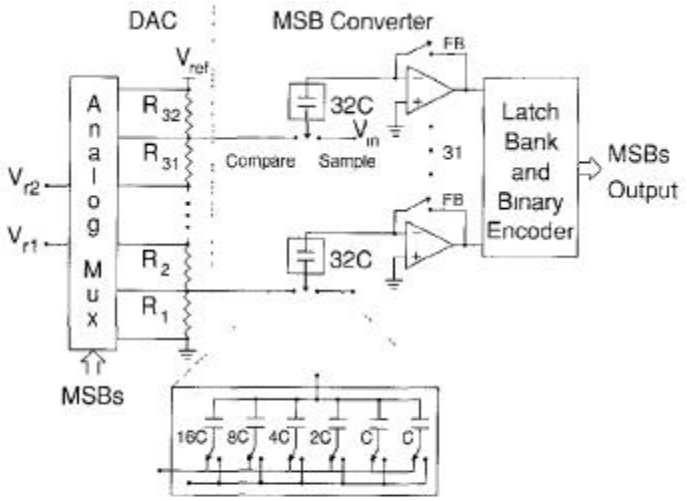


Fig. 4. Prototype converter's MSB ADC and DAC. It operates like a standard CMOS flash converter. The 32-C capacitor is used as part of an S/H. It is a 5-bit array used for subranging in the LSB conversion. The DAC and ADC transitions match each other since the same resistor string is used for both.

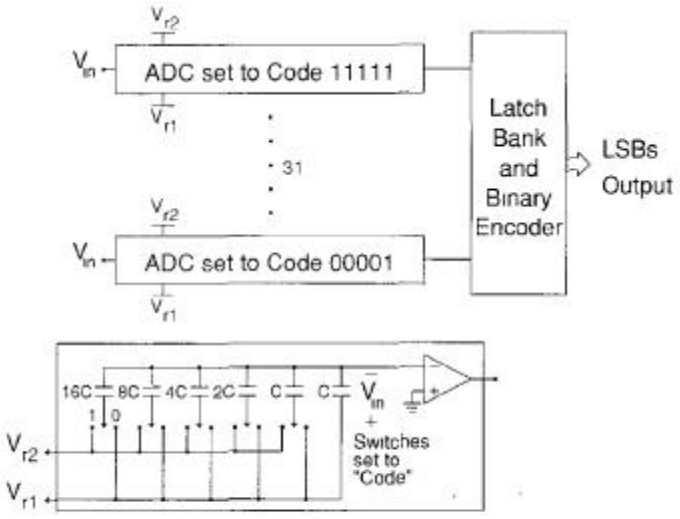


Fig. 5. Prototype converter's LSB ADC. Thirty-one ADC subsections each preset to codes 00001 through 11111 subdivide the region between V_{r1} and V_{r2} in the LSB's flash decision. The ADC subsections are 5-bit binary-weighted capacitor-array ADC's. The comparators, capacitors, latch bank, and encoder are the same ones used in the MSB ADC.

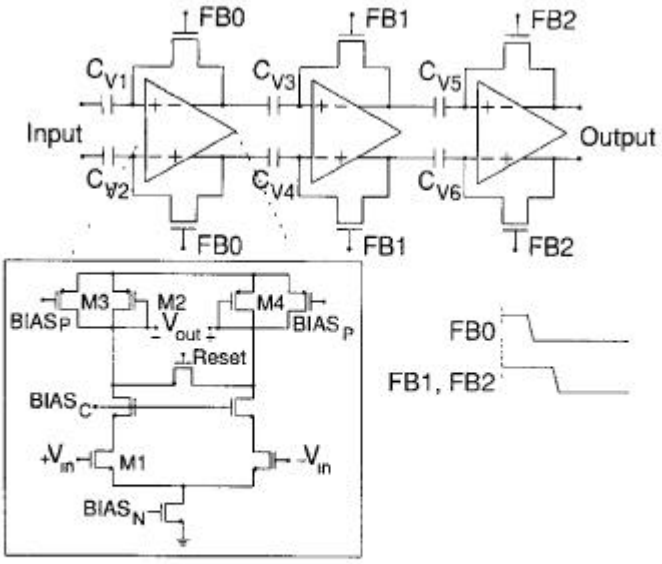


Fig. 7. Three-stage comparator is capacitor coupled to cancel each stage's offset voltage independently. The gain block is based on a differential pair input and diode-connected load devices that eliminate the need for CMFB that uses area, power, and time.

4. ADC Performance

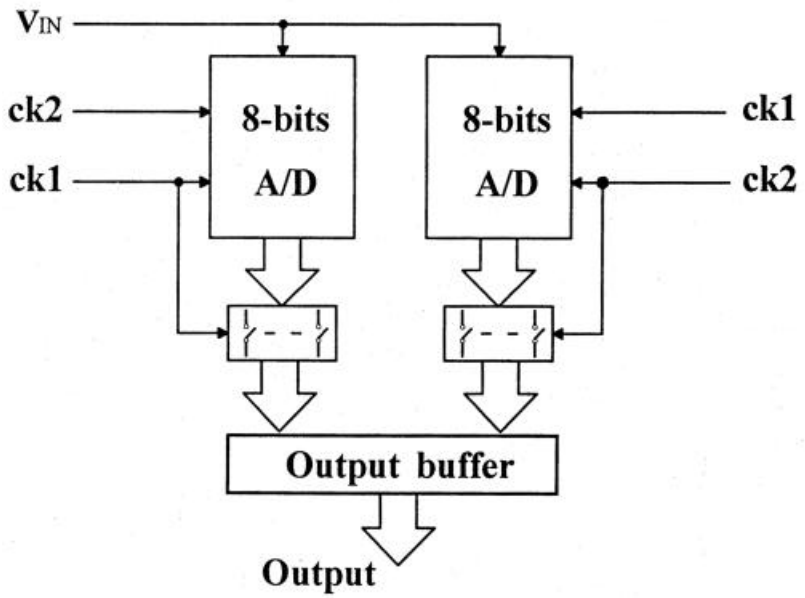
TABLE II
PROTOTYPE ADC PERFORMANCE AND SPECIFICATIONS

Summary	
Resolution	10 bits
Conversion Rate	5 Msamples/sec
Maximum DNL	0.6 LSB
Maximum INL (With comp.)	3.0 LSB
Maximum SNR (With comp.)	50 dB
Technology	1.6 μm CMOS
Input Capacitance	50 pF
Power Dissipation	350 mW
Area	54k mils^2

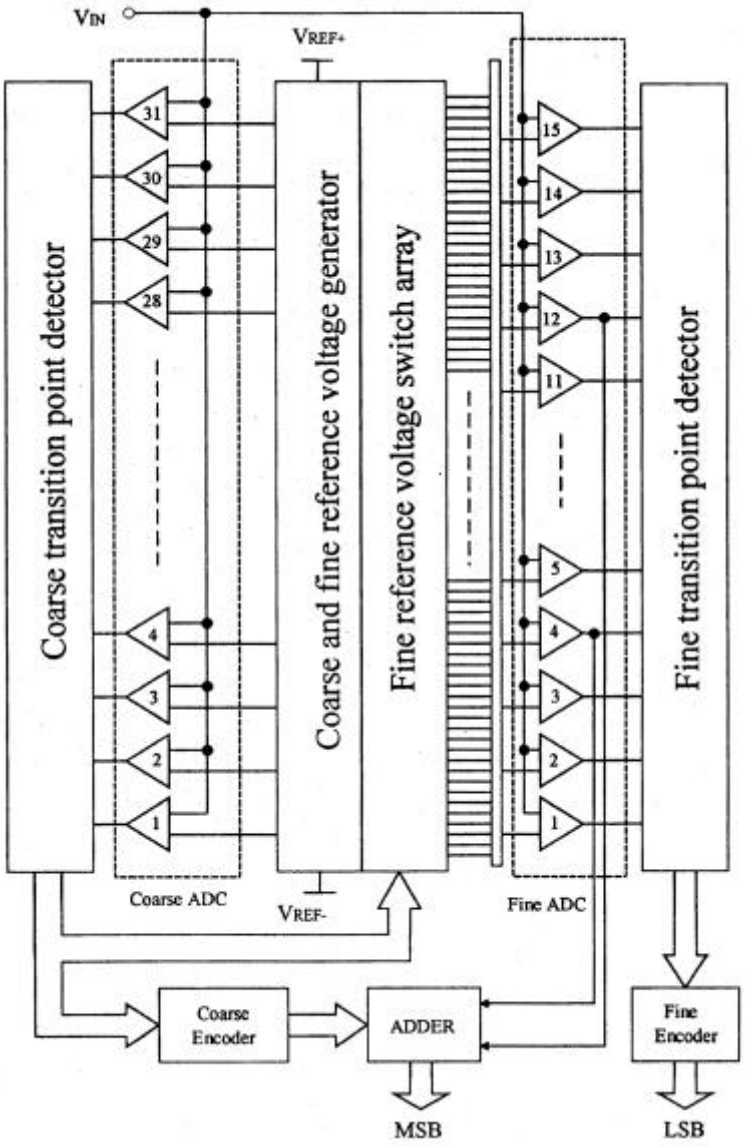
§13-6.3 The Proposed A/D Converter

1. Parallel processing with two 8-bit subconverters. (Time-interleaved ADC)
2. Two-step structure with single resister ladder.
3. Using 31 dynamic coarse and 15 fine comparators for 3V Vdd design.
   (No op amps is required)
4. 1-bit digital error correction.

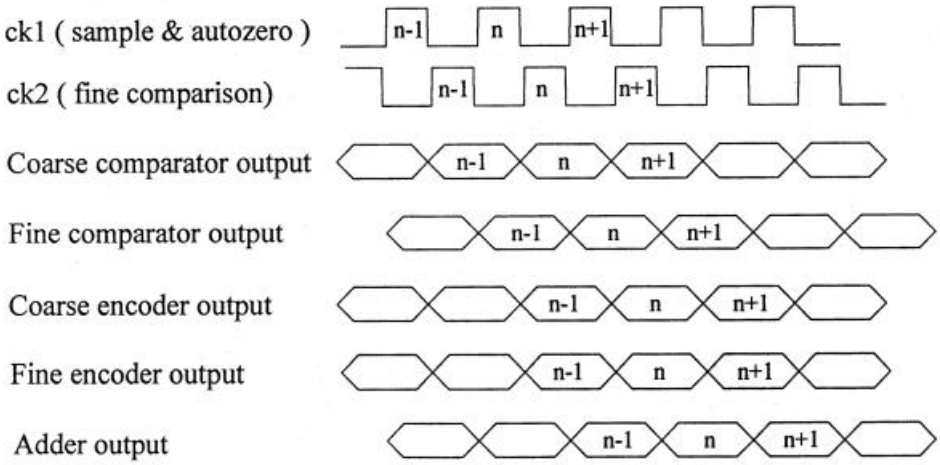
- The proposed A/D converter with parallel processing architecture.



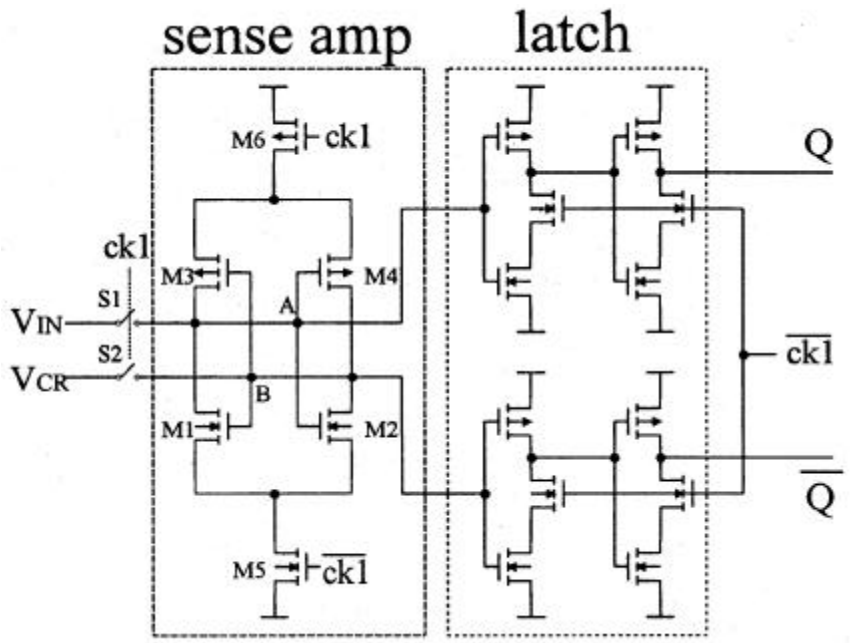
- The proposed 8-bit A/D subconverter.



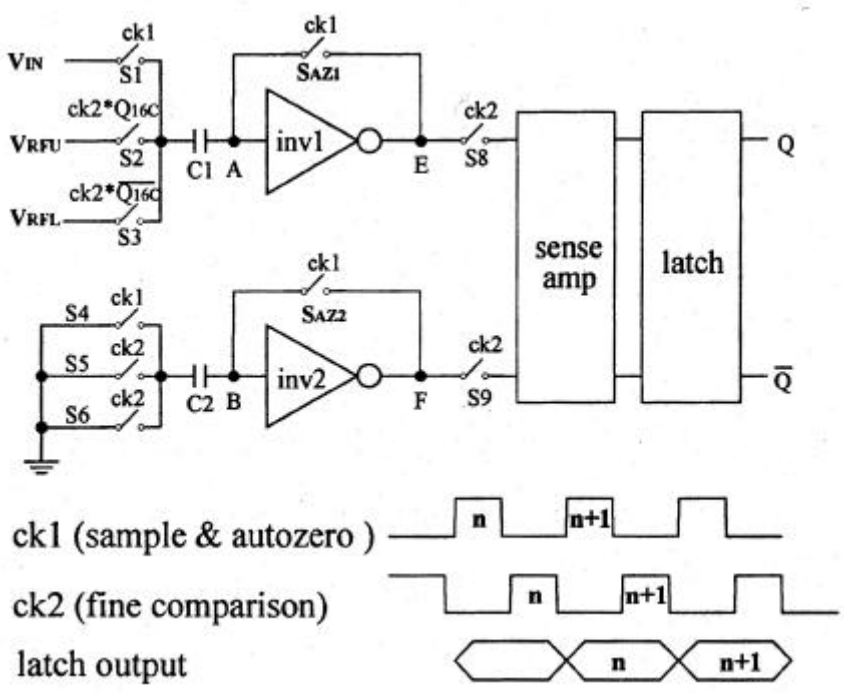
- The timing diagram of a 8-bit A/D subconverter.



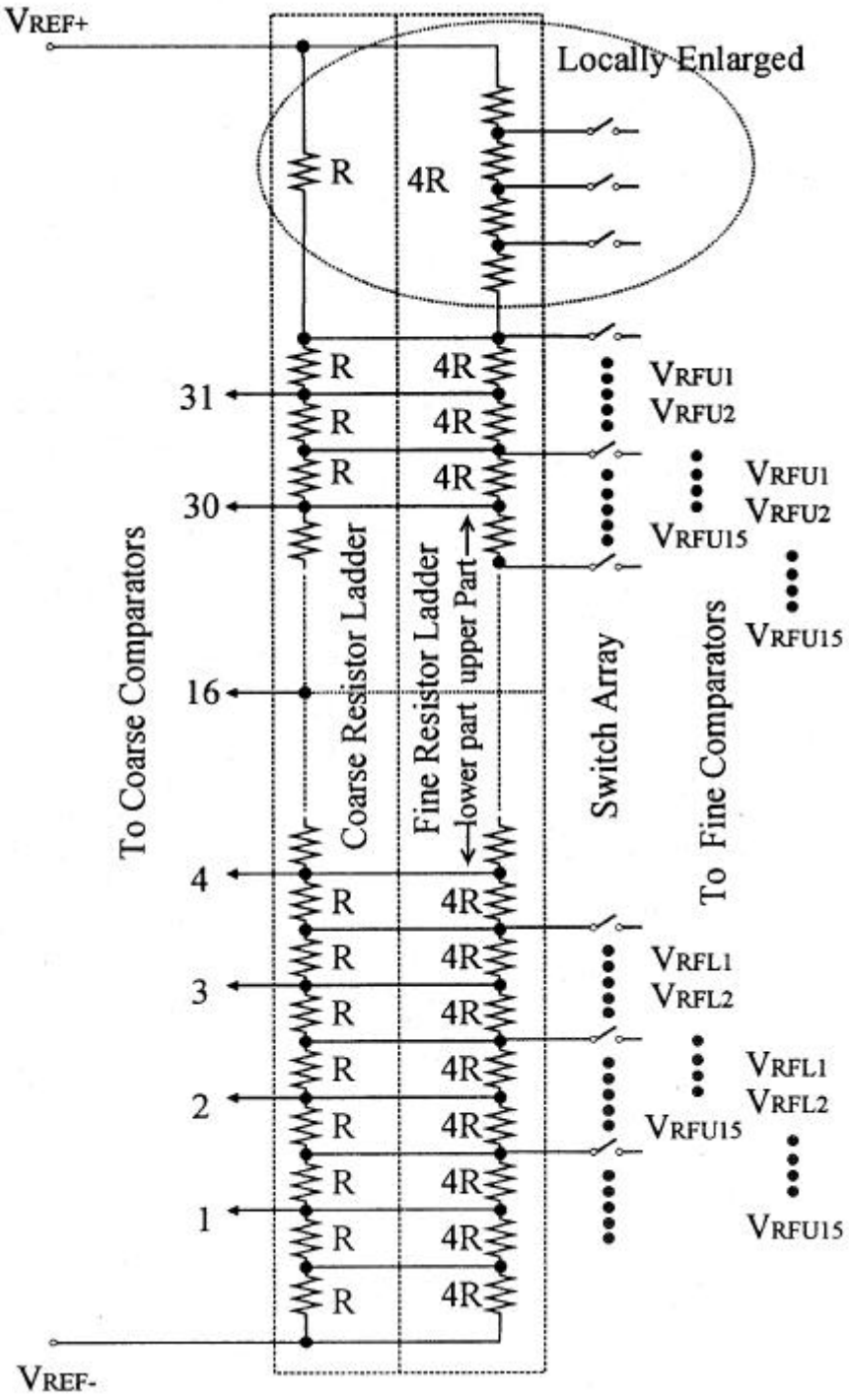
- The circuit of the coarse comparator.



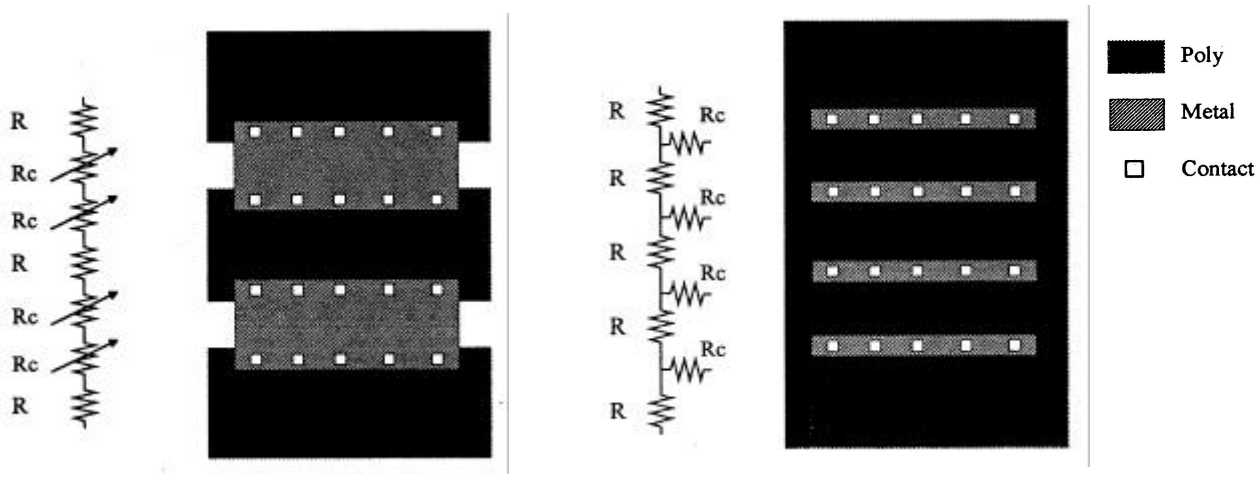
- Fine comparator and its clock sequences.



- Intermeshed resistor reference ladder.



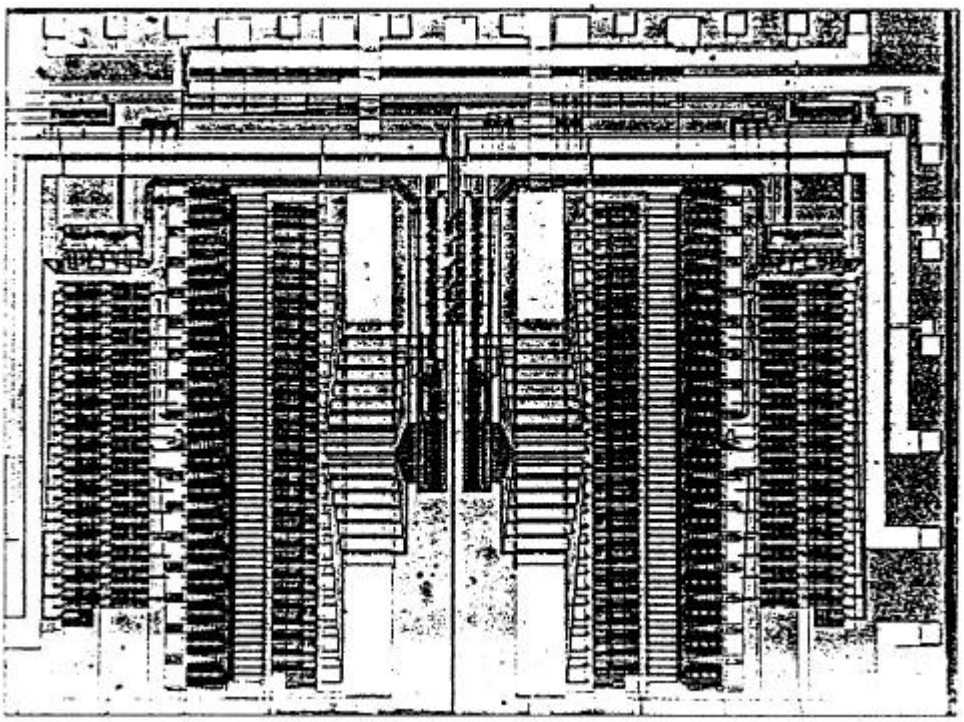
- The layouts and their equivalent circuits (a) with and (b) without separated unit resistors.



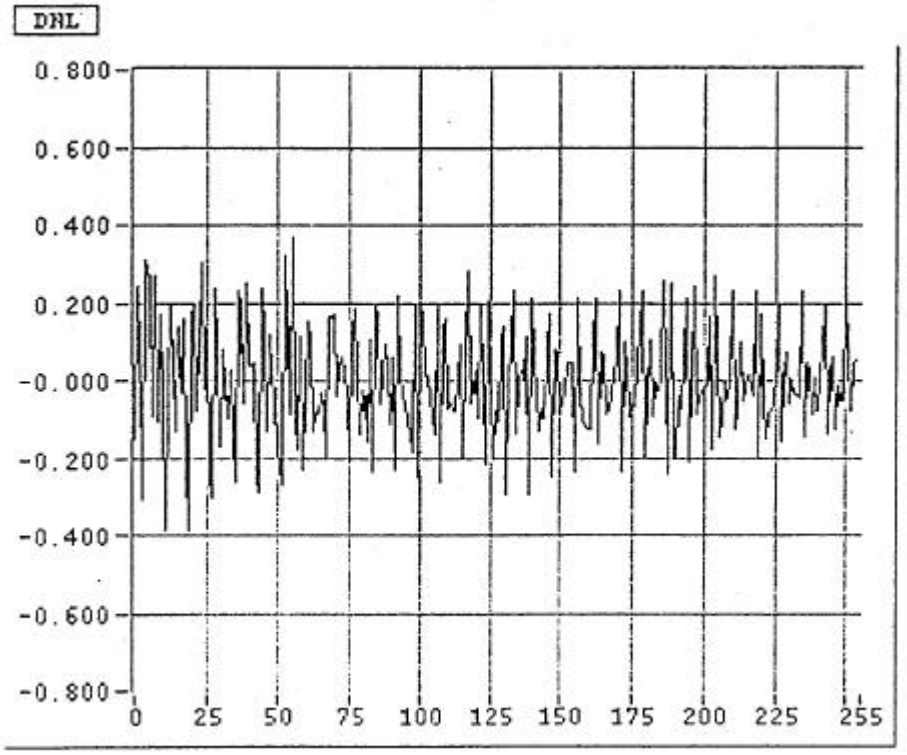
(a) (b)

Experimental Results:

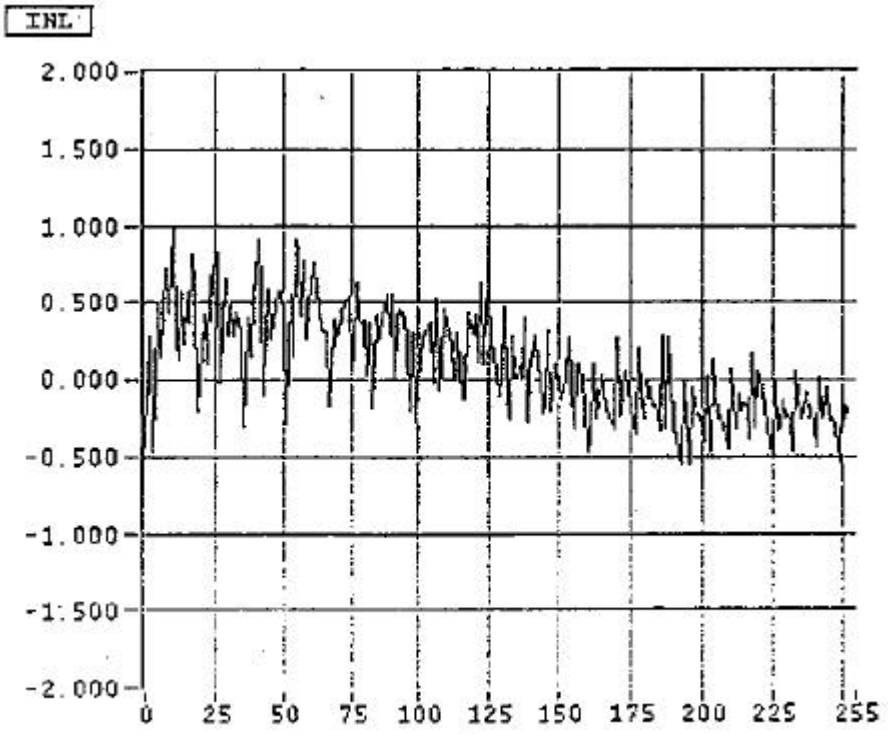
- Chip photograph of the fabricated A/D converter.



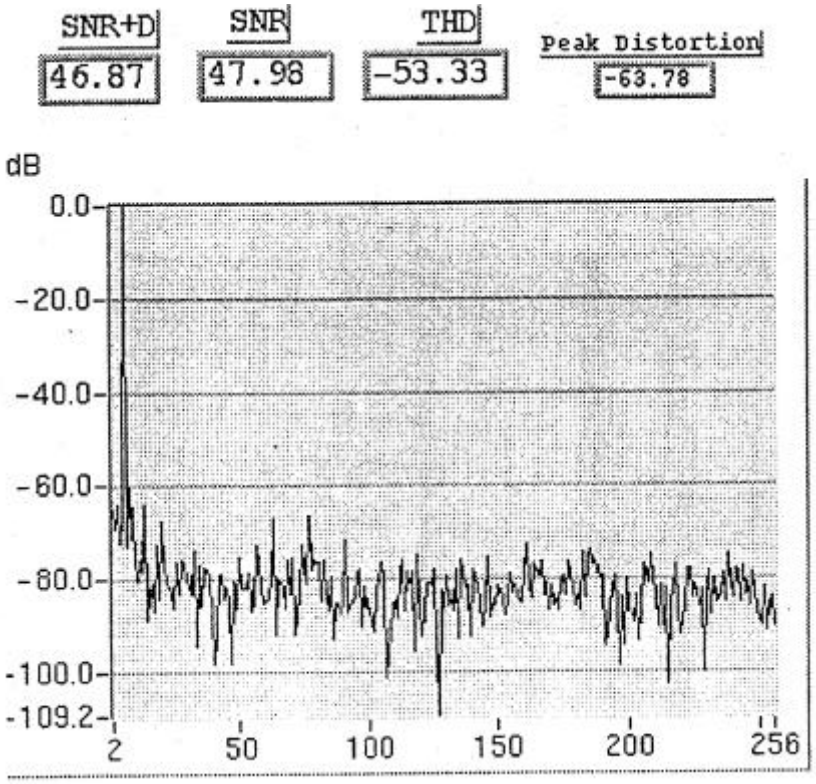
- A typical plot of the differential nonlinearity.



- A typical plot of the integral nonlinearity.



- The FFT spectrum for a 85 KHz sine-wave input signal



- The effective bits versus input frequency characteristics.

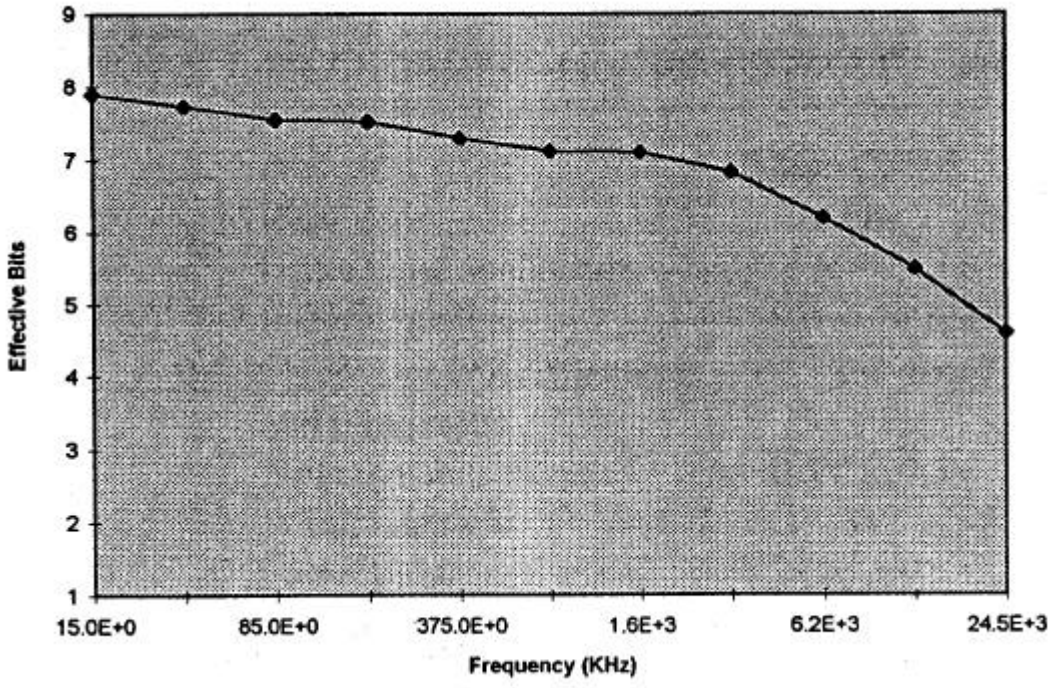


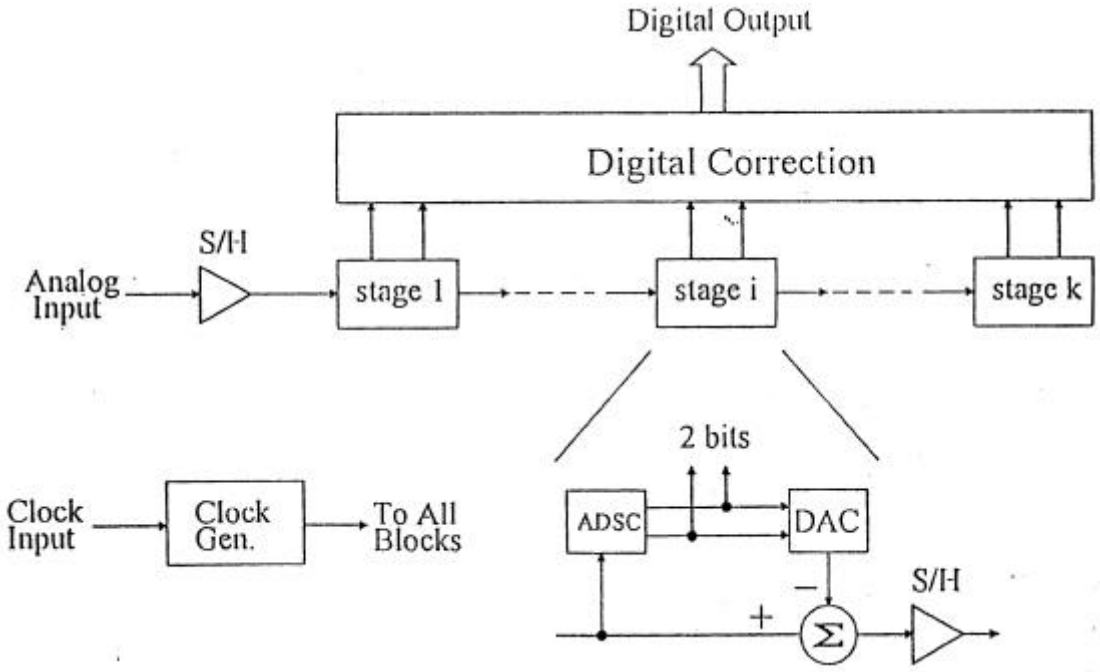
Table 1 Major characteristics of the A/D converter.

Process:	0.8μm CMOS
Resolution:	8bits
Differential nonlinearity:	-0.4 to + 0.4 LSB
Integral nonlinearity:	-0.6 to + 1 LSB
SNDR(for 85KHz input):	46.8 dB
Sampling rate:	50 MHz
Input dynamic range:	0.5V to 2.5V
Power supply:	3V
Power dissipation:	100 mW
Active area:	4950 um × 3790 μm

§13-7 Pipelined (Multistage) ADC

- ◆ Need $m(2^{N/m}-1)$ comparators & R tapes.
- ◆ Need m op amps for S/H & subtractors.
- ✧ High-performance op amp is not easy to be achieved (especially for 3V Vdd).

Block diagram of a pipelined A/D converter



Pipelined ADCs
§13-7.1 A Pipelined 5-Msps 9-bit ADC

Ref.: IEEE JSSC, vol. 22, no. 6, pp. 954-961, Dec. 1987.

1. General pipelined ADC

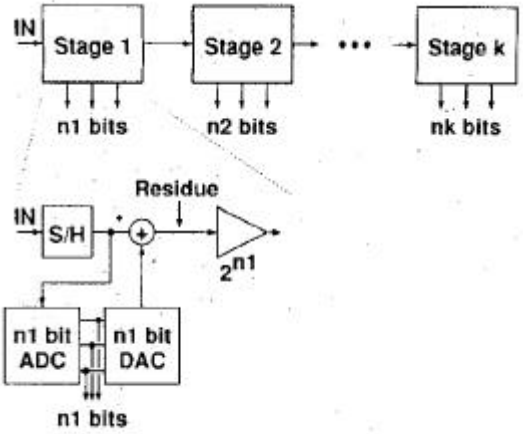


Fig. 1. Block diagram of a general pipelined A/D converter.

2. Two-stage pipelined ADC

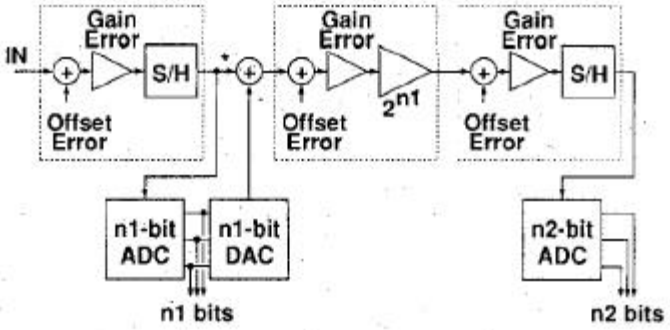


Fig. 2. Block diagram of a two-stage pipelined A/D converter with offset and gain errors.

3. Prototype

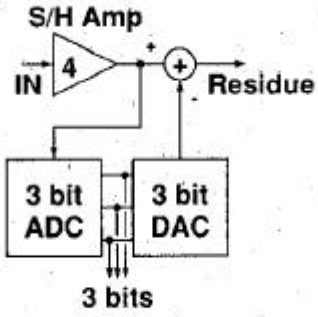


Fig. 5. Block diagram of one stage in the prototype.

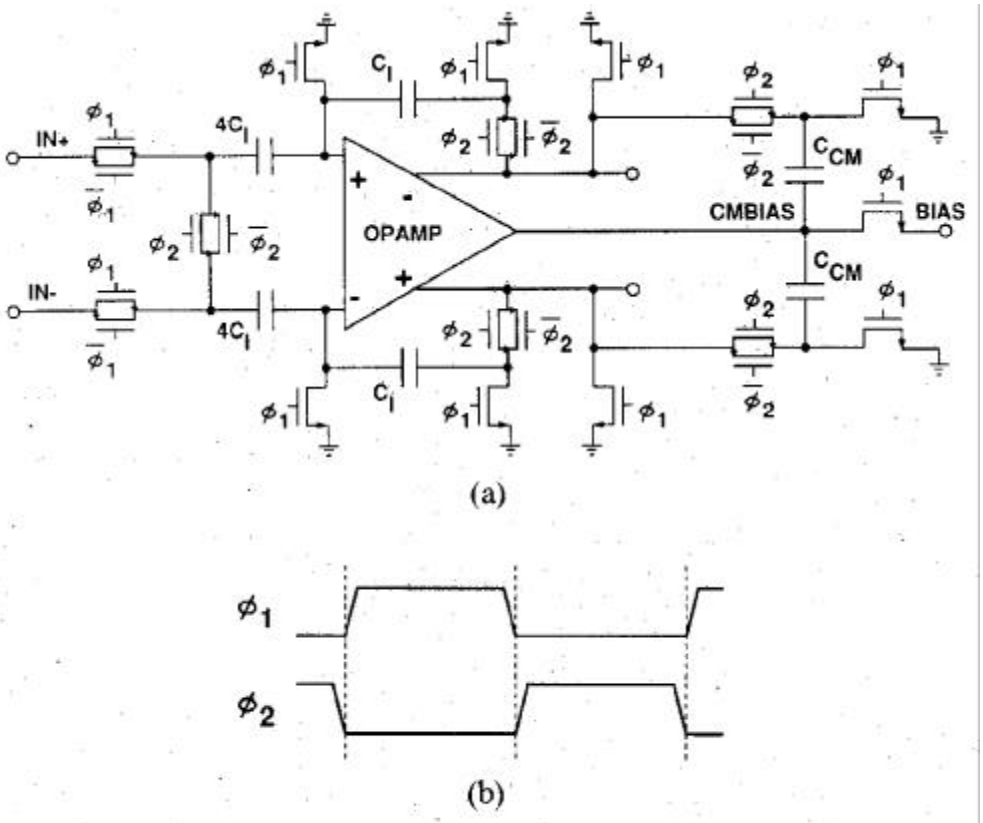


Fig. 6. (a) Schematic of S/H amplifier. (b) Timing diagram of a two-phase nonoverlapping clock.

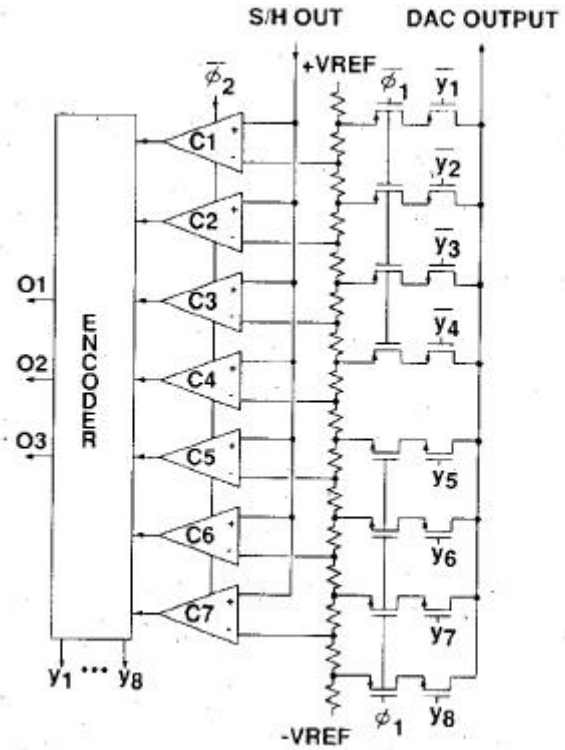


Fig. 8. Block diagram of A/D, D/A subsection.

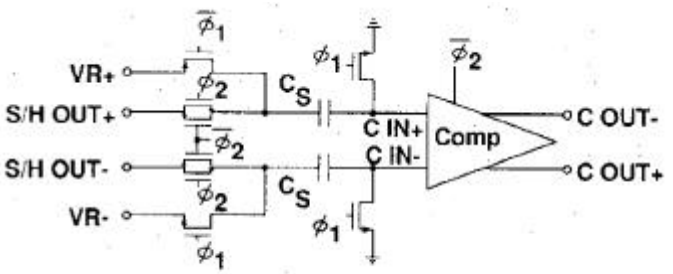


Fig. 9. Connection of comparator with A/D, D/A subsection.

- OP AMP:

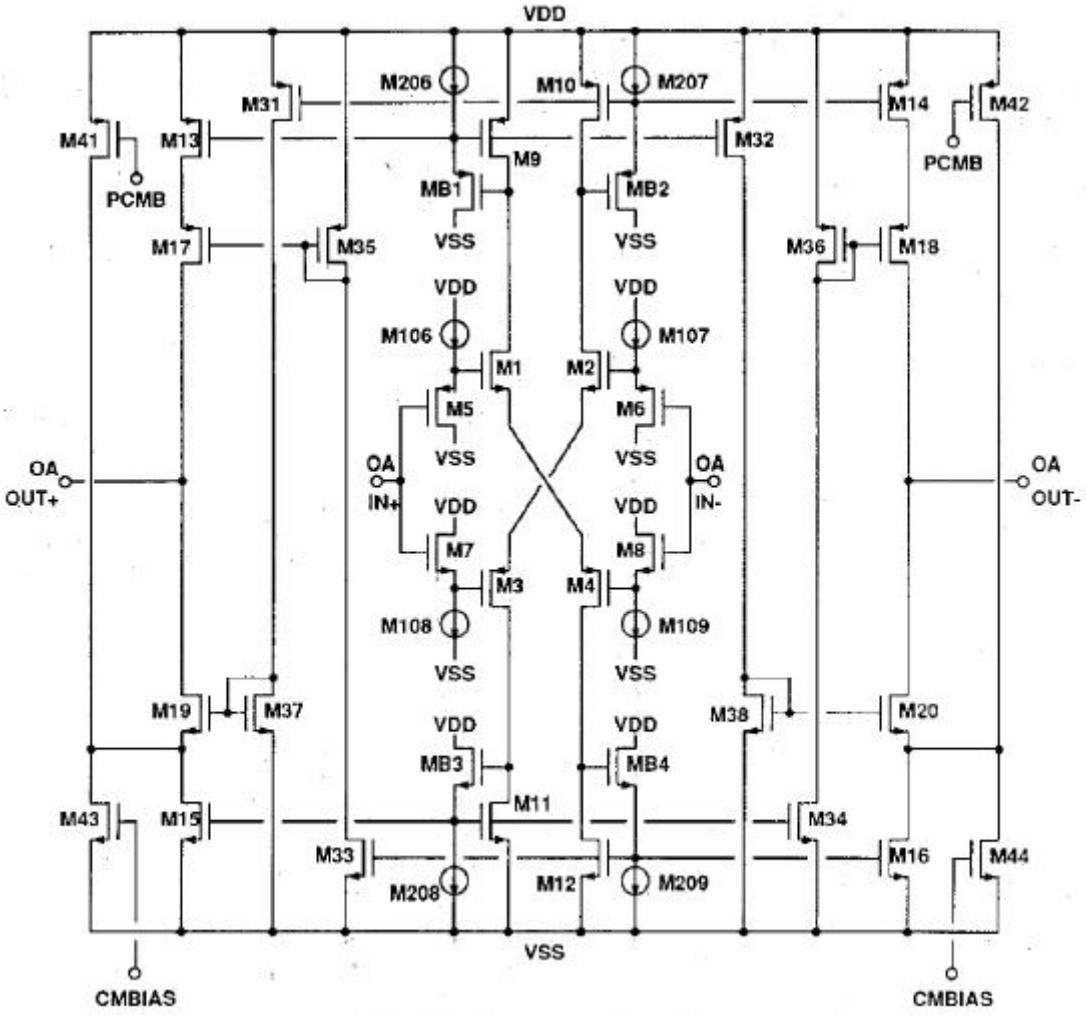


Fig. 7. Op-amp schematic.

- Comparators:

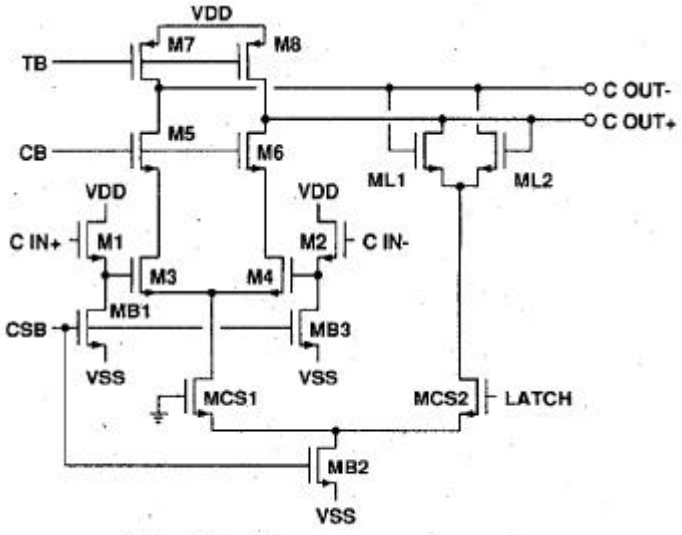


Fig. 10. Comparator schematic.

4. Measurement results:

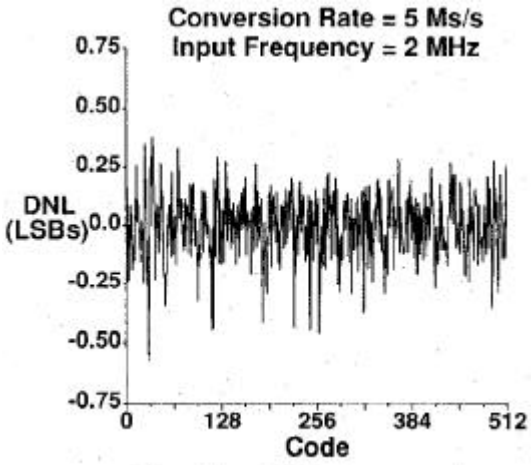


Fig. 11. DNL versus code.

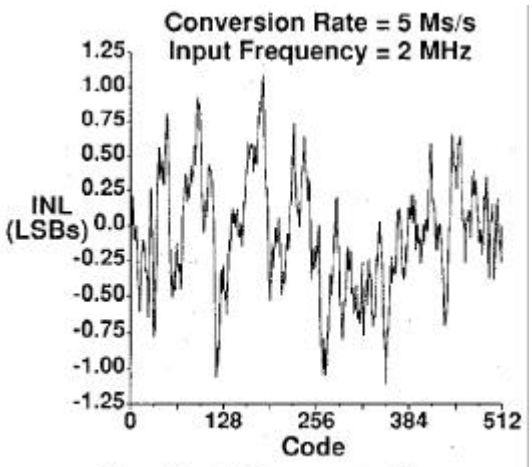


Fig. 12. INL versus code.

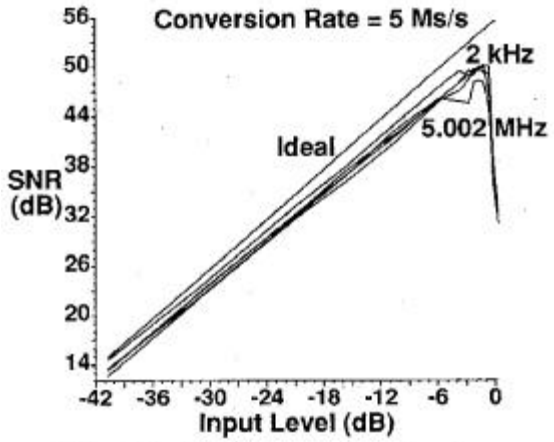


Fig. 13. SNR versus input level.

TABLE I
DATA SUMMARY OVER INPUT FREQUENCY VARIATION
9-bit Resolution; 5-Msample/s Conversion Rate; ±5-V Power Supplies

Input Frequency	2 kHz	2 MHz	5.002 MHz
Peak DNL (LSB)	0.5	0.6	0.5
Peak INL (LSB)	1.0	1.1	1.2
Peak SNR (dB)	50	50	49

TABLE II
TYPICAL PERFORMANCE: 25°C

Technology	3-u CMOS
Resolution	9 bits
Conversion Rate	5 Ms/s
Area*	8500 mils^2
Power Supplies	±5 V
Power Dissipation	180 mW
Input Capacitance	3 pF
Input Offset	< 1 LSB
CM Input Range	±5 V
DC PSRR	50 dB

*Does not include clock generator, bias generator, reference generator, digital error correction logic, and pads.

§13-7.2 A Pipelined 9-Stage Video-Rate ADC

Ref.: IEEE 1991 Custom Integrated Circuits Conference (CICC). pp. 26.4.1-26.4.4

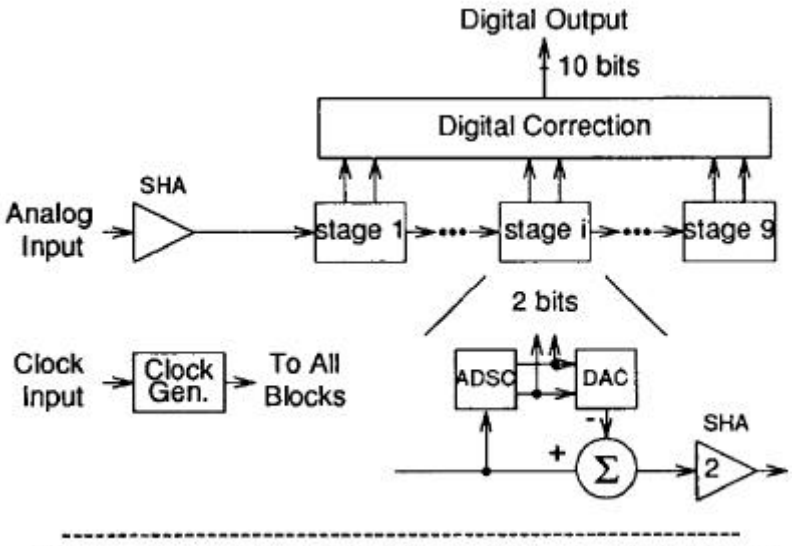


Fig. 1 - Analog-to-Digital Converter Block Diagram

DAC + $\sum$ + $\triangleright$2 SHA $\Rightarrow$ MDAC

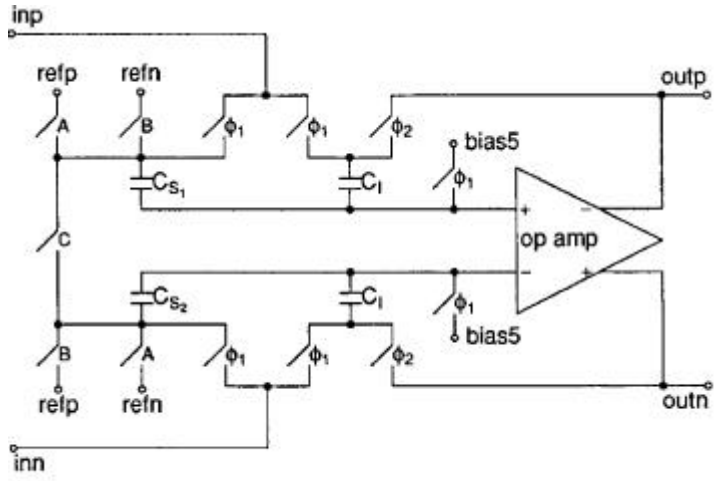


Fig. 5 - Multiplying Digital-to-Analog Converter Schematic

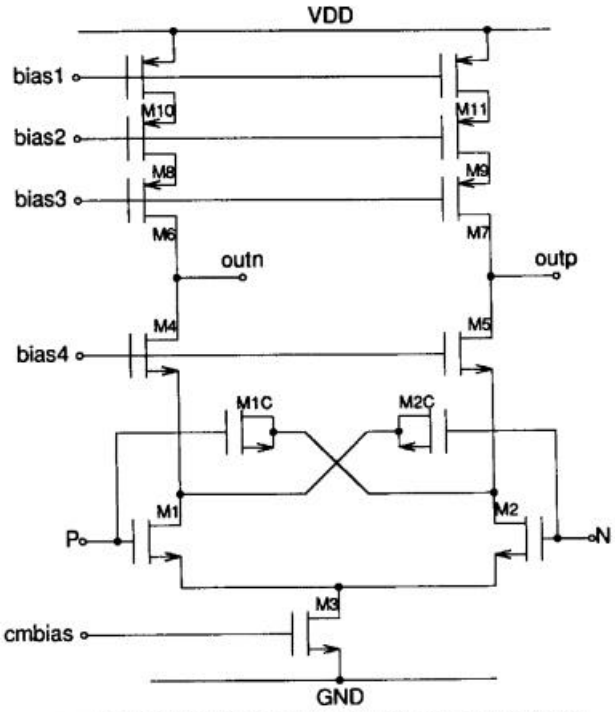


Fig. 6 - Operational-Amplifier Schematic

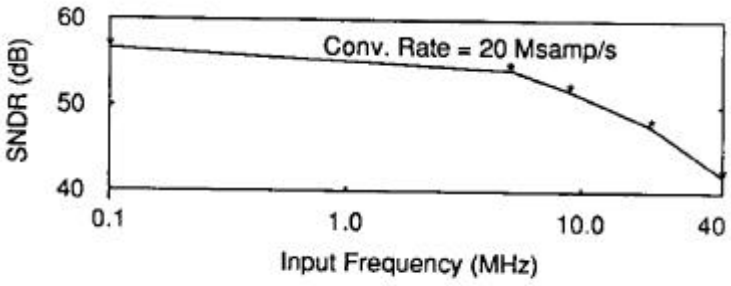


Fig. 11 - Signal-to-Noise-and-Distortion Ratio (SNDR) versus Input Frequency

Table 1 - ADC Performance: +5 V and 25°C

Technology	0.9-μm CMOS
Resolution	10 bits
Conversion Rate	20 Msamples/s
Area	9.3 mm²
Power Dissipation	300 mW
Input Offset	10 LSB
DNL	0.6 LSB
INL	1.1 LSB
SNDR (f_{in} = 100 kHz)	56.6 dB
SNDR (f_{in} = 5 MHz)	54.2 dB
DP	0.15 ° p-p
DG	0.23 % p-p
PSRR (1 kHz)	55 dB
CMRR (5 kHz)	70 dB

§13-7.3 A Single-Ended 12-bit 20 MS/s Self-Calibrating Pipeline ADC

Ref.: IEEE JSSC vol. 33, pp. 1898-1903, Dec. 1998.

Advantages: concurrent processing of analog signals

⇒ optimal speed and power dissipation

⇒ high speed and low power

Disadvantage: * Inherent passive component matching problem

⇒ hard to control and yield ↓

⇒ self-calibration and correction technique

* Latency ⇒ acceptable in most applications

1. The pipeline architecture

* CMOS SC implementation

⇒ conversion stage speed

∝ feedback factor

∝ (interstage gain)$^{-1}$

⇒ 1-bit/stage for power and speed optimization.

⇒ simple calibration.

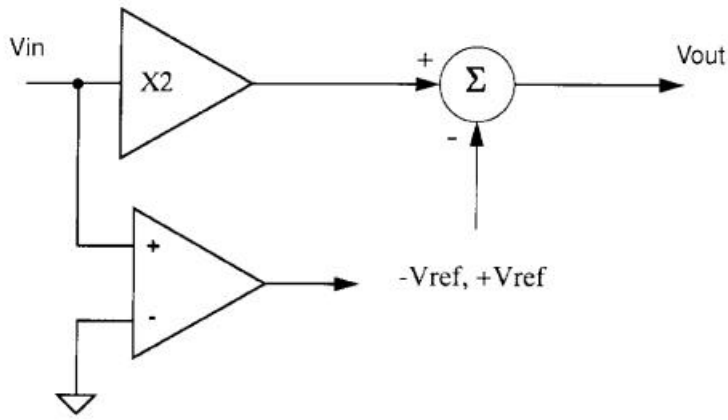


Fig. 1. Block diagram of the 1-bit converter stage.

* Transfer characteristic:

The output residue voltage Vout

Vout = 2Vin + D Vref

D = +1 for 0 < Vin < Vref

= -1 for -Vref < Vin < 0

* Digital correction technigue:

Very attractive for submicron CMOS (small chip area)

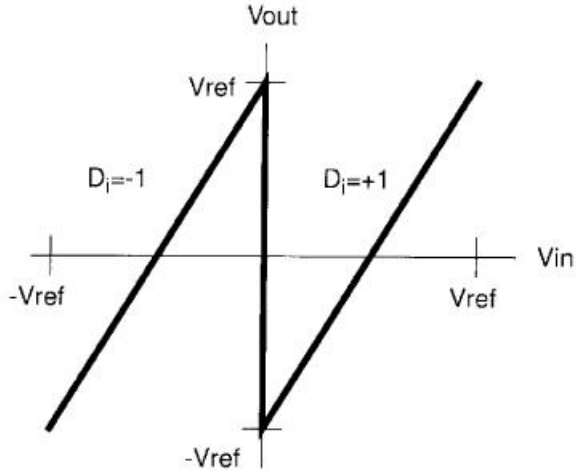


Fig. 2. Transfer characteristic for the 1-bit converter stage.

* The "radix = 2" overrange stage

To correct residues up to $\frac{1}{2}$Vref outside the nominal ±Vref range for Vin.

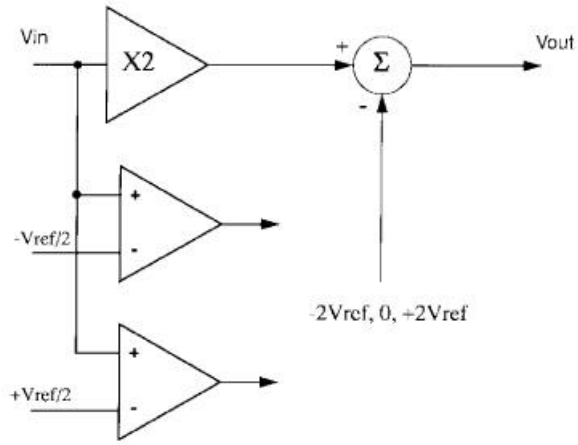


Fig. 3. Overrange stage implementation.

Transfer characteristic:

$$Vout = 2Vin + 2 \cdot D\ Vref$$

$$D = +1 \qquad \frac{1}{2}Vref < Vin < Vref$$

$$= 0 \qquad -\frac{1}{2}Vref < Vin < \frac{1}{2}Vref$$

$$= -1 \qquad -Vref < Vin < -\frac{1}{2}Vref$$

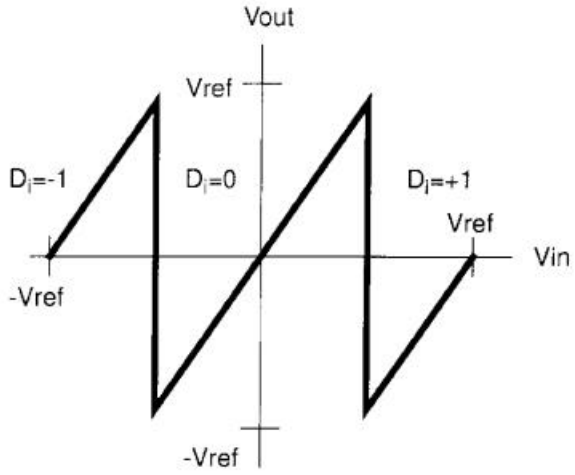


Fig. 4. Overrange stage transfer characteristic.

Lower feedback gain for the overrange stage
⇒ maximum operating frequency ↓

* Overall architecture only 3 overrange stages are used for digital correction.

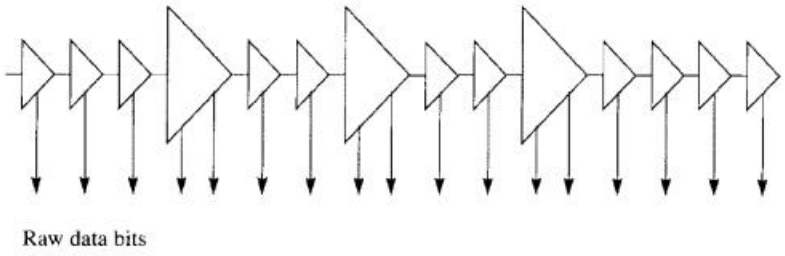


Fig. 5. Architecture of the ADC including three overrange stages.

2. Self-calibration and correction algorithm
   * Starting from the eleventh pipeline stage and working toward the MSB stage. The rest of the stages (12-15) are not calibrated.
   * For each calibration stage, the calibration consists of
     (1) forcing an analog input value of 0V (differential)
     (2) forcing the digital decision to the left and to the right of the transition.

* The calibration coefficient

Memi = code_l - code_h

Vout = Vref Code_l=0

Vout = -Vref Code_h=0

$\Rightarrow \text{Memi} = 2|\Delta\text{Vout}| \cong |\Delta\text{Vin}|$

one coefficient for regular stage.
two coefficients for overrange stage.

All the correction coefficients are stored in 15 registers.

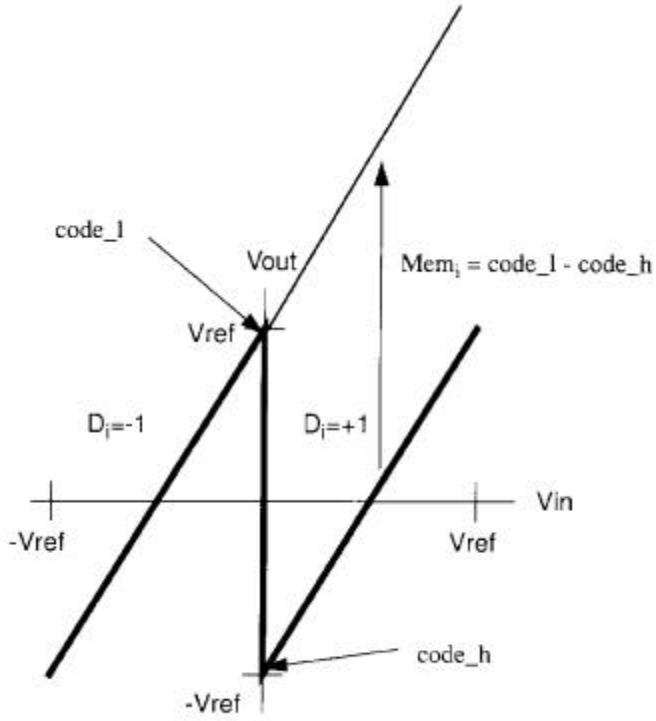


Fig. 6. Principle of digital self-calibration and correction.

* All the digital correction is performed in 16 bits, and the last 4 LSB's are truncated for the final 12-bit output code.

* Global offset and full-scale error can be calibrated.

3. Implementation of Analog Blocks.

* The single-ended to differential input S/H:

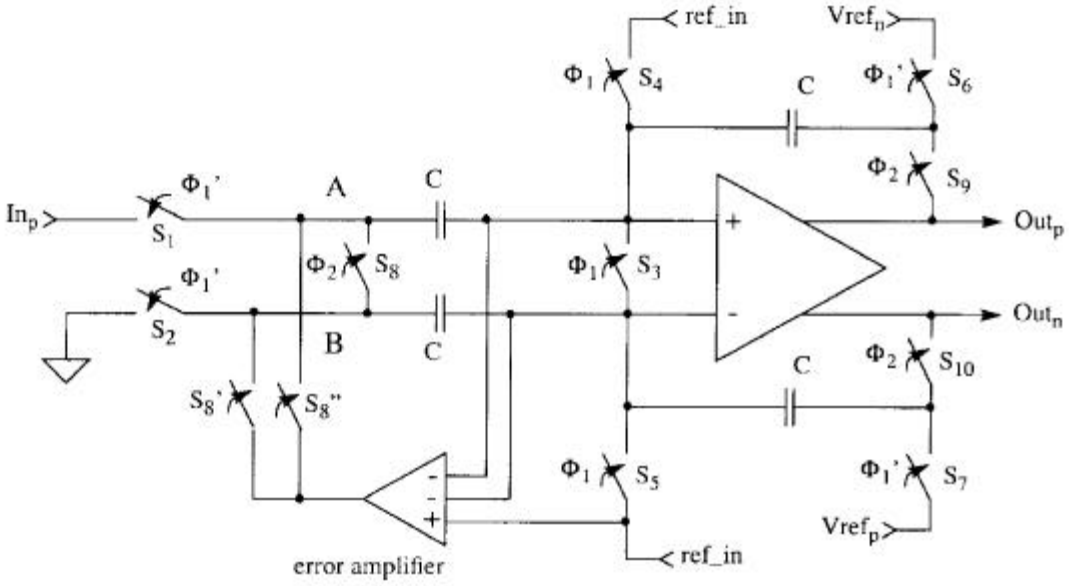


Fig. 9. Block diagram of the single-ended to differential input S/H.

* Input common-mode fb amp.

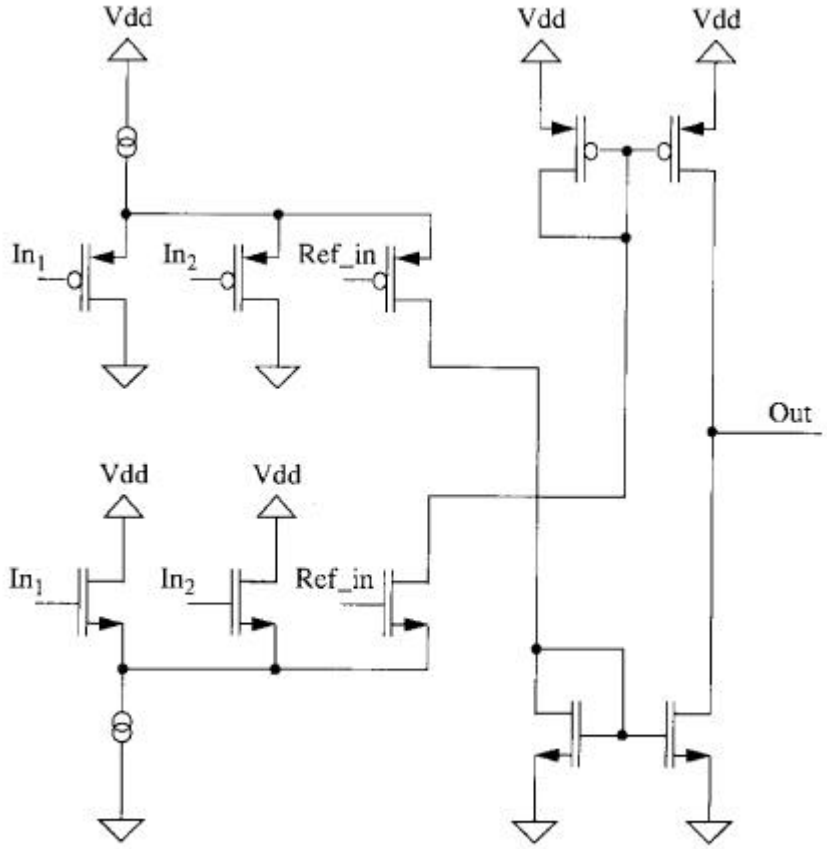


Fig. 10. Error amplifier in the input S/H.

* op amp
(telescopic op amp)

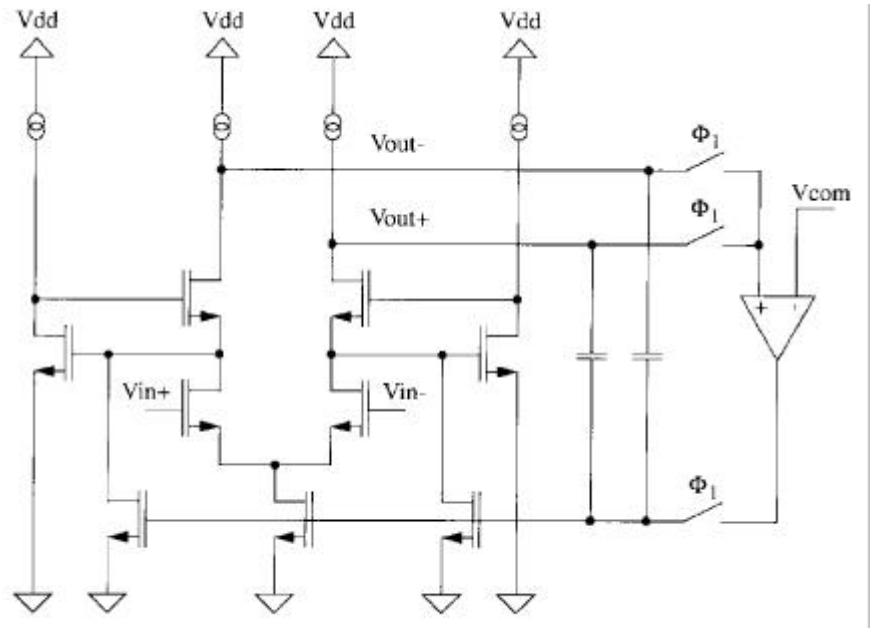


Fig. 8. Opamp circuit diagram, including output common-mode feedback.

4. Measurement results

DNL:

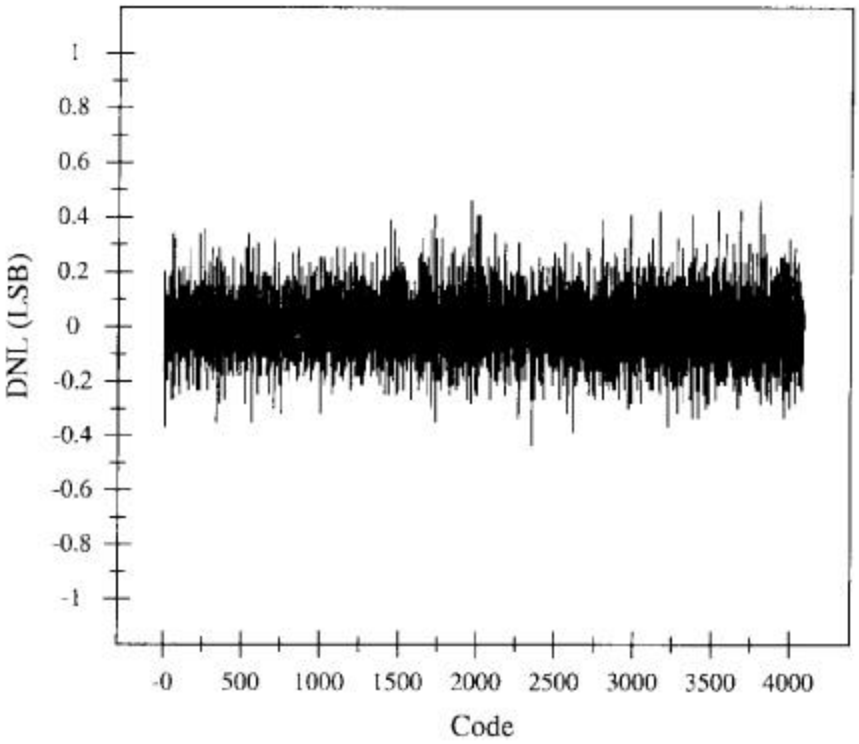


Fig. 12. Typical DNL plot.

INL:

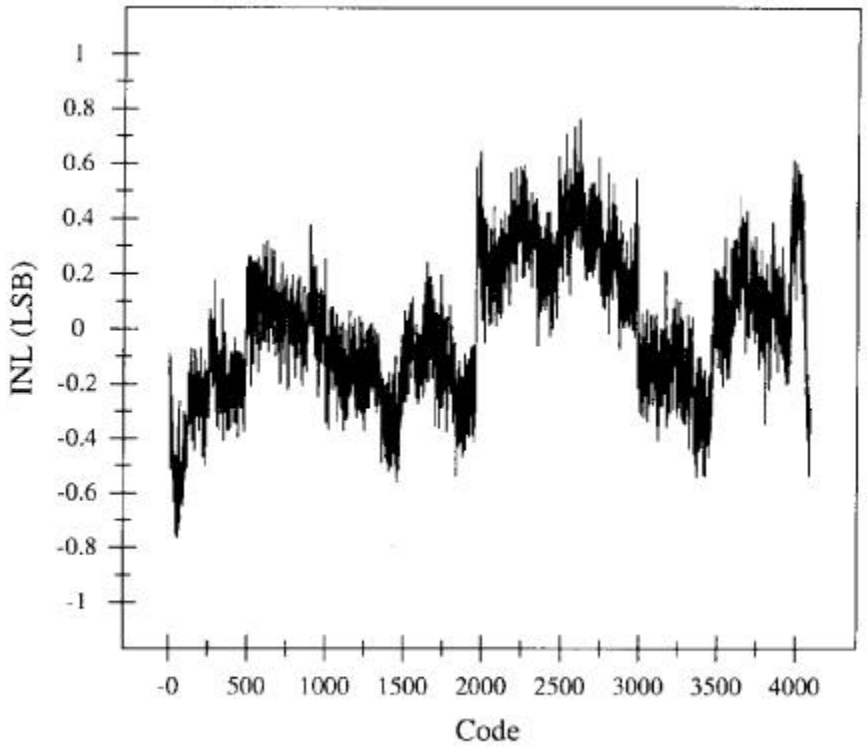


Fig. 13. Typical INL plot.

Spectrum:

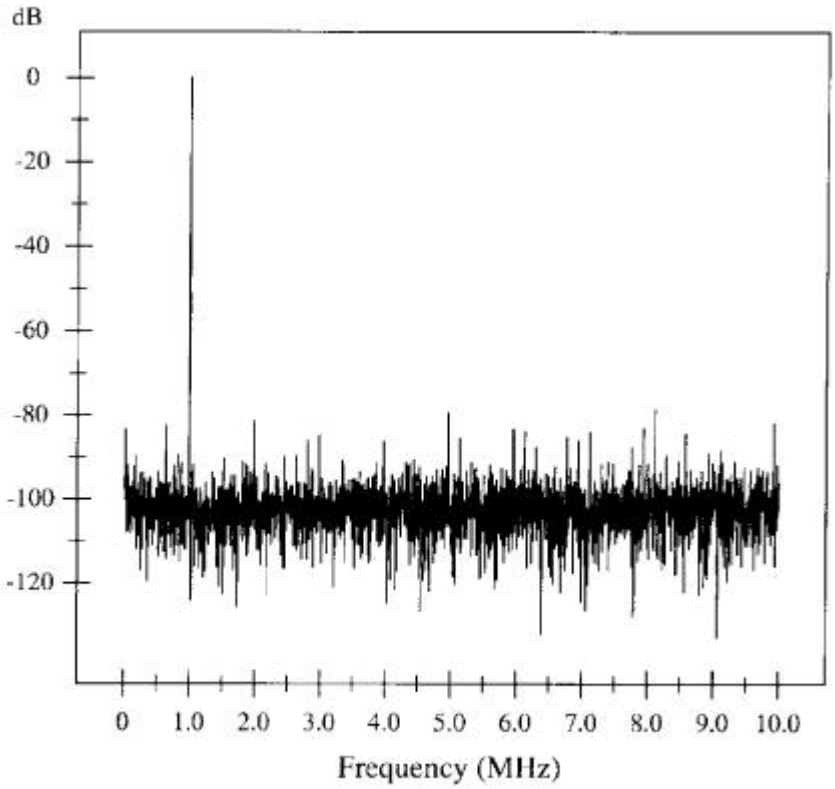


Fig. 14. Spectrum for a single-ended 2-Vpp 1-MHz input sine wave.

SNR & THD

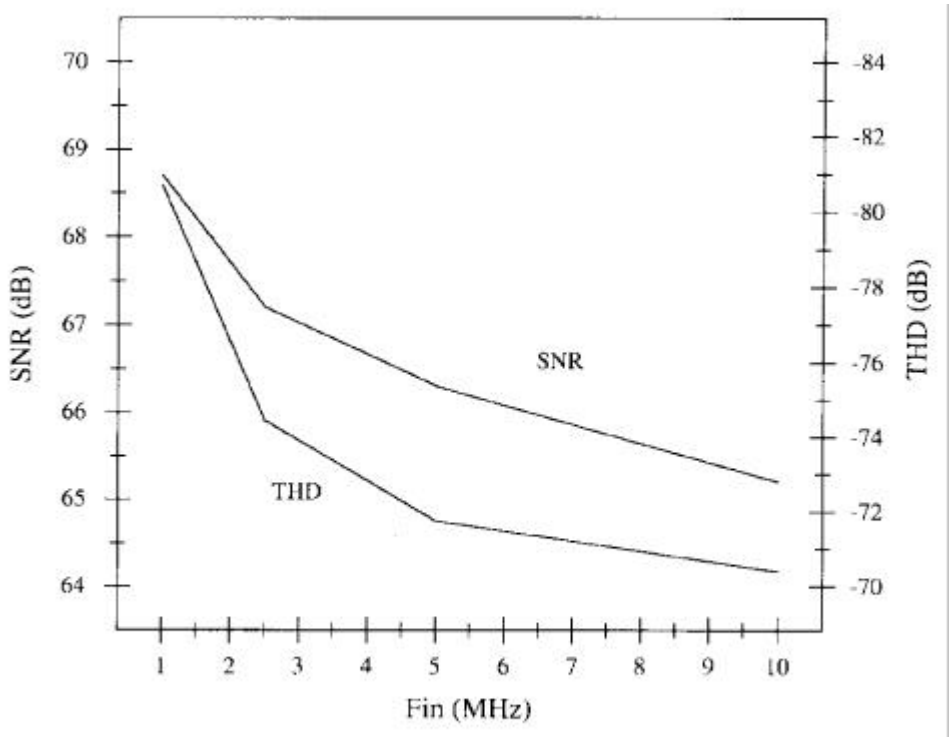


Fig. 15. Single-ended dynamic performance versus input frequency (20 Msample/s).

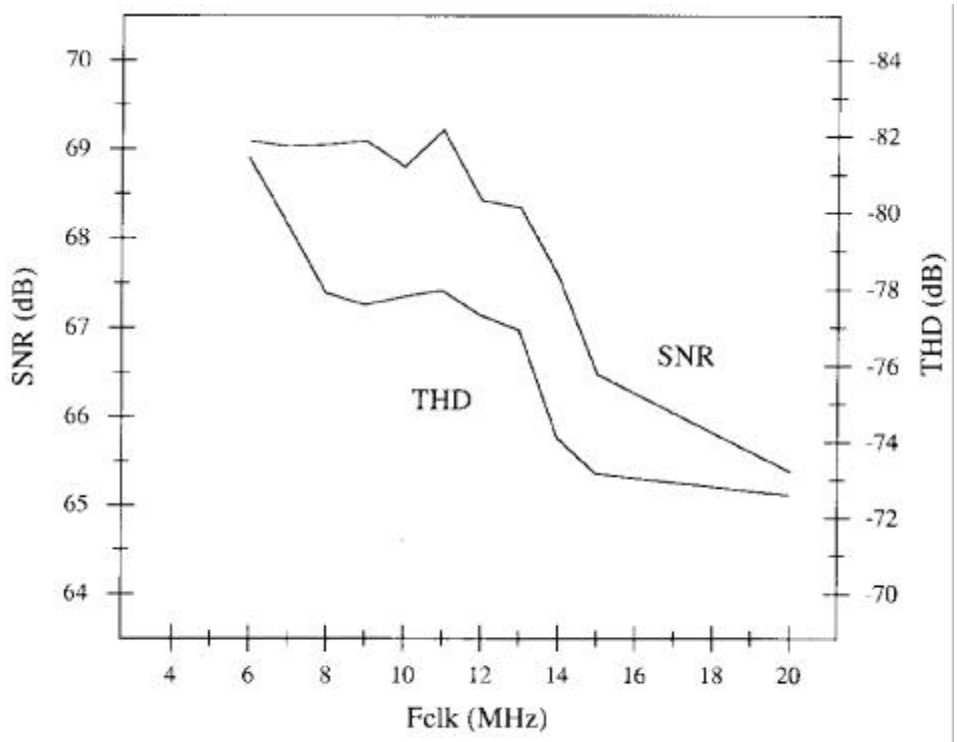


Fig. 16. Single-ended dynamic performance versus clock frequency (fin=1 MHz).

TABLE I
SUMMARY OF ADC PERFORMANCE

Sample rate	20 MHz
Resolution	12 bits
INL	0.75 LSB
DNL	0.45 LSB
SNR (Nyquist)	65.4 dB
THD (Nyquist)	-72.6 dB
Power dissipation	250 mW
Noise (rms)	0.36 LSB
Input range	0 to 2V

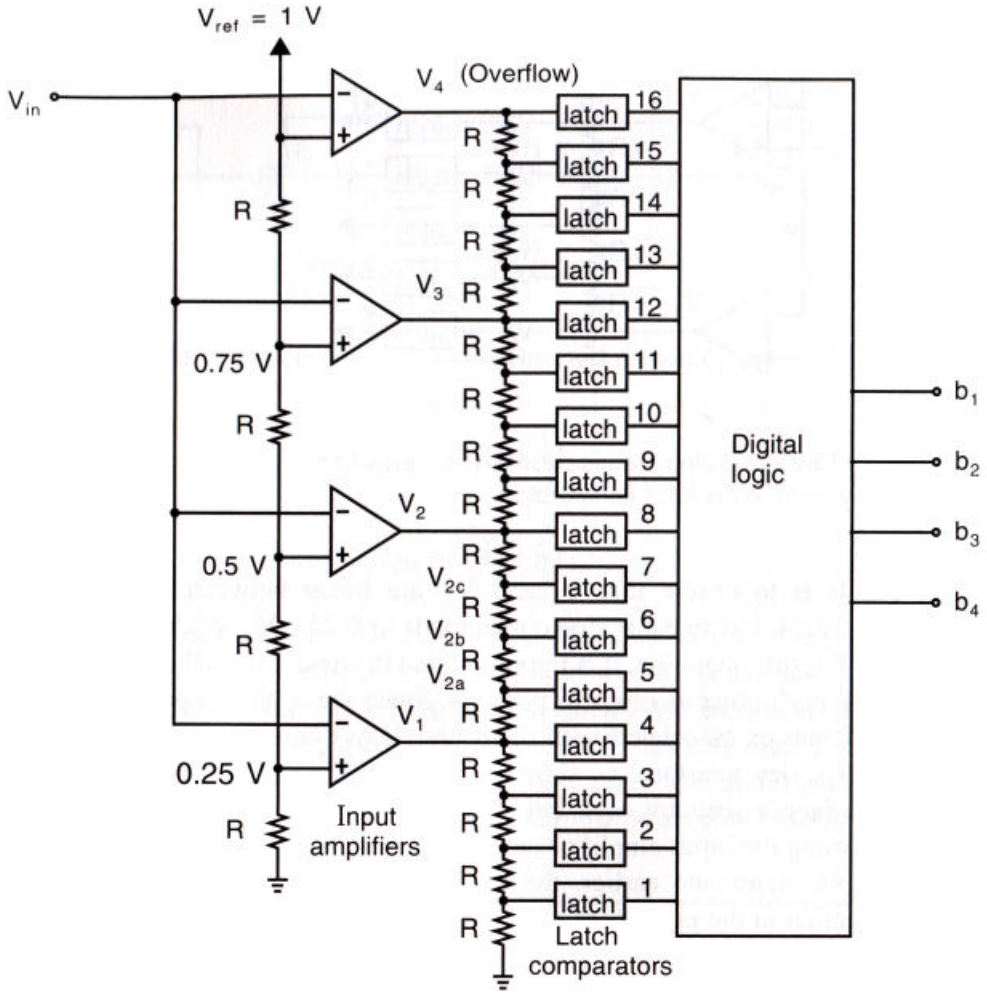
§13-8 Folding and Interpolating ADC

Ref.: Johns & Martin, Analog IC Design, pp. 516-523.

§13-8.1 Interpolating ADC

* The number of input amplifiers (or comparators as in flash ADC) attached to Vin can be significantly reduced by interpolating between adjacent output of these amplifiers.

A 4-bit interpolating ADC with interpolating factor of 4

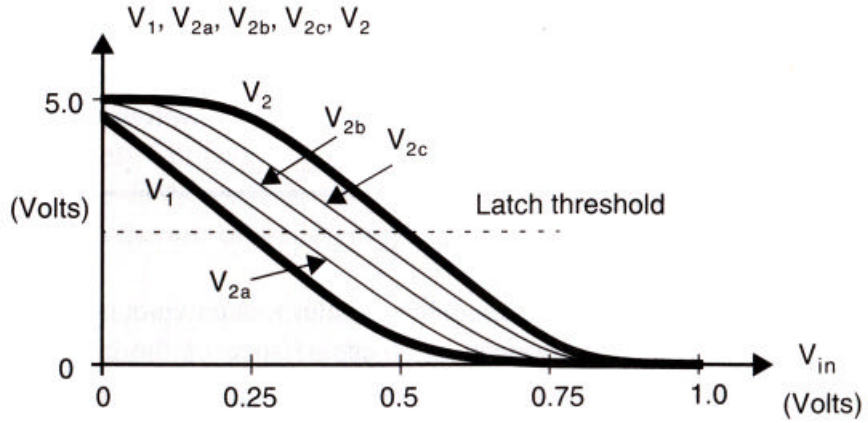


* Transfer response of V_1, V_{2a}, V_{2b}, V_{2c}, V_2 vs. Vin: Logic 1 = 5V, Logic 0 = 0V

  Gain of input amplifier = -10

  Latch threshold = 2.5V

  More reference levels between V_1 and V_2: V_{2a}, V_{2b}, V_{2c}.



Possible transfer responses for the input-comparator output signals, V_1 and V_2, and their interpolated signals

* If V_1 and V_2 are accurately linear between their own thresholds,

  i.e. 0.25V < Vin < 0.5V

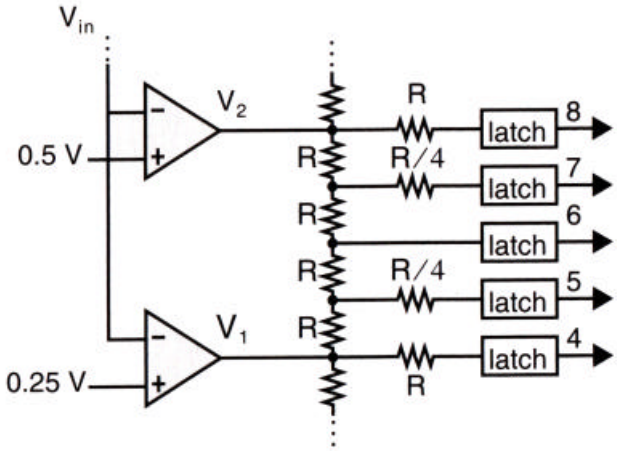
  ⇒ correct crossing points of the latch threshold.

  ⇒ linearity ↑.

  And the rest of the interpolated signal responses are of secondary importance.

* For fast operation, the delays of latches must be equalized by adding series resistors.

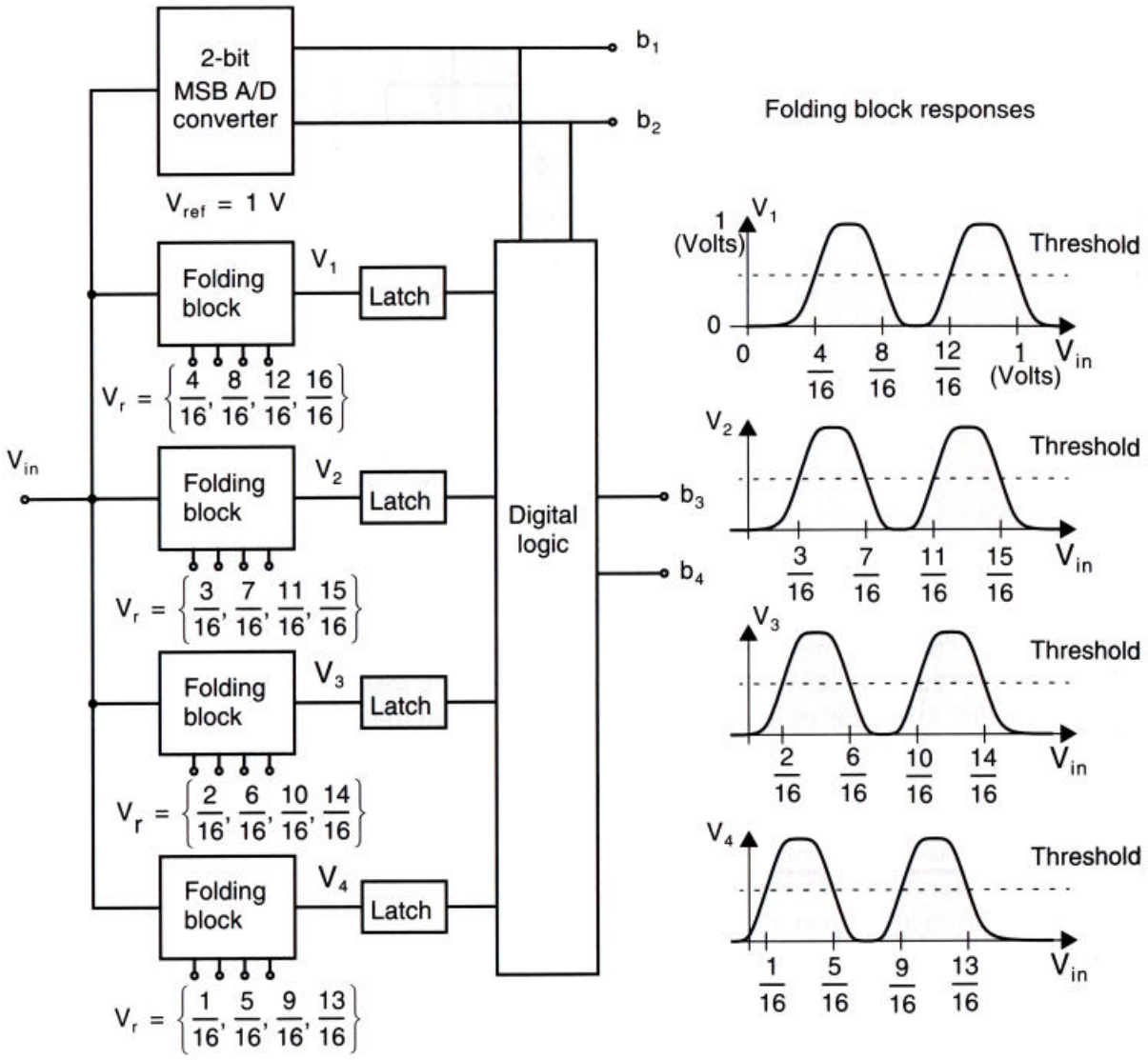
* Interpolation can be implemented by R string, current mirrors or capacitors.



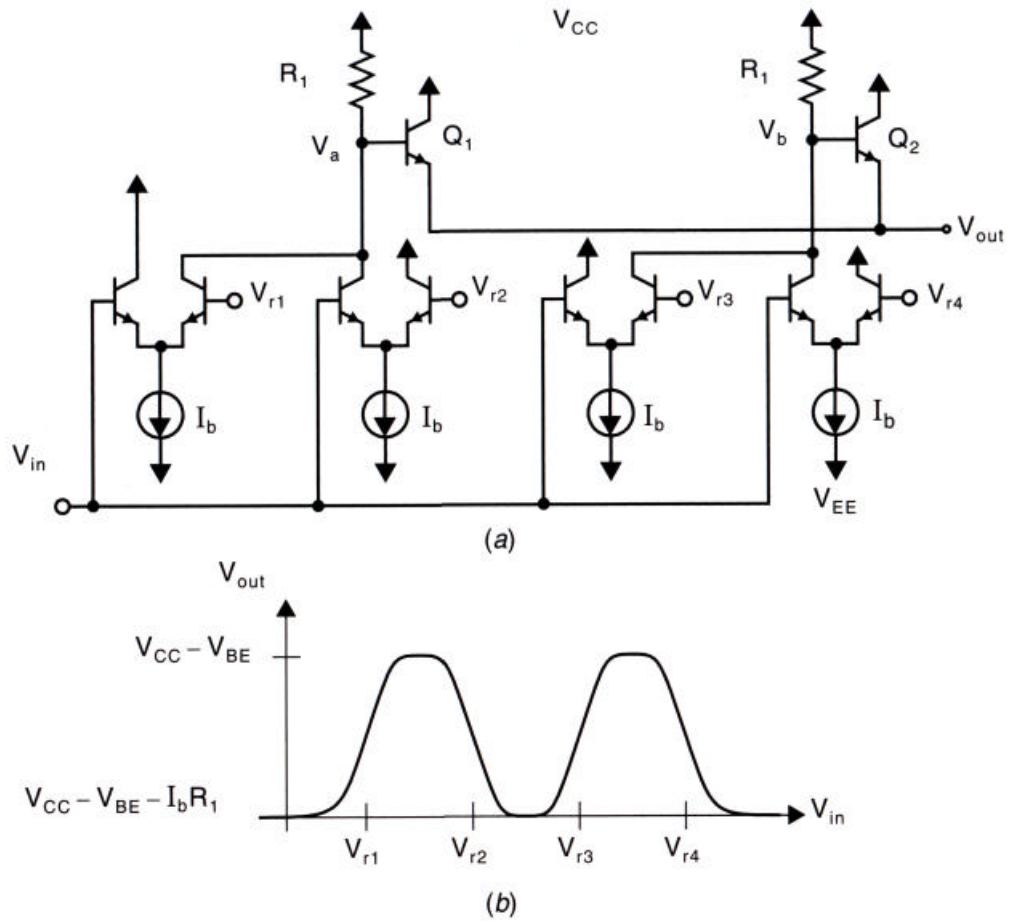
Adding series resistors to equalize delay times to the latch comparators

§13-8.2 Folding ADC

A 4-bit folding ADC with a folding rate of 4.



* The use of a folding architecture to reduce significantly the number of latch comparators (2^N in interpolating ADC).
* The use of analog preprocessing to determine the LSB set directly.
* Folding rate ≡ the number of output transitions for a single folding block as Vin is swept over its input range.



A folding block with a folding-rate of four. (a) A possible single-ended circuit realization; (b) input-output response.

* 4-bit folding ADC architecture:
  MSB 2-bit: flash
  LSB 2-bit: folding
  LSB: V_1, V_2, V_3, and V_4 produce a thermometer code for each of the four MSB regions.

* Examples: Vin: $0 \rightarrow 1/4$ V
  Thermometer code: 0000, 0001, 0011, 0111, 1111
  Vin: $1/4$ V $\rightarrow 1/2$ V
  Thermometer code: 1110, 1100, 1000, 0000

* Total number of latches: 8
  as compared to 16 in flash ADC.

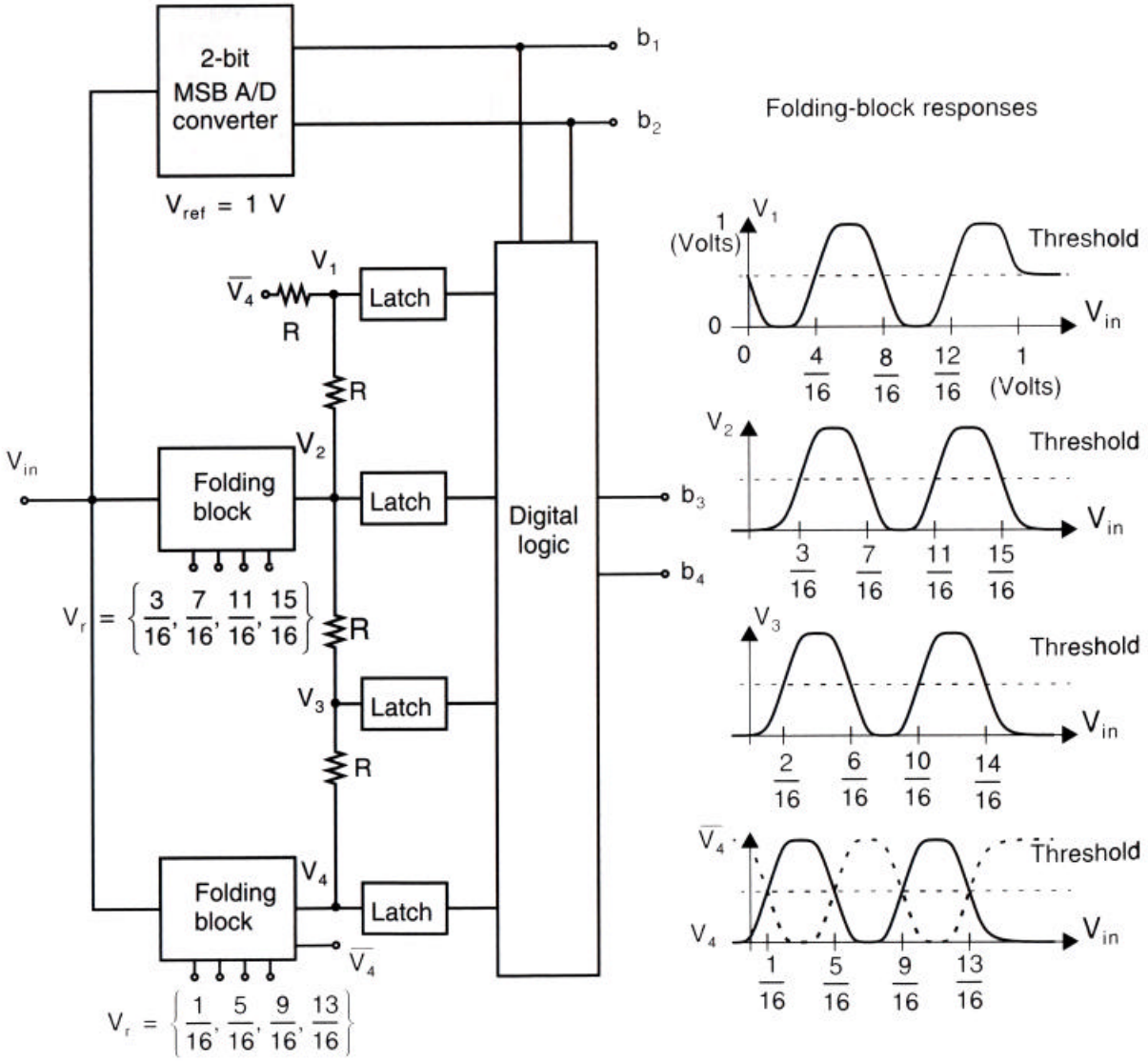
* No S/H is required.

* Folding blocks realized by BJT cross-coupled differential pairs as an example.

* Large input capacitance seen by Vin.

* The output signal frequency = input signal frequency $\times$ folding rate
  $\Rightarrow$ limits the practical folding rate used in high-speed converter.

§13-8.3 Folding and Interpolating ADC



A 4-bit folding A/D converter with a folding rate of four and an interpolate-by-two. (The MSB converter would usually be realized by combining some folding-block signals.)

* Folding rate: 4; Interpolation: 2
* $\overline{V_4}$ is a new inverted signal from V_4.
* Latch number ↓

  Input capacitance ↓
* Capable of > 100 MHz operation.
* Can be implemented in CMOS.

§13-8.4 A 400-Ms/s 6-bit CMOS Folding and Interpolating ADC

Ref.: IEEE JSSC, vol. 33, no. 12, pp. 1932-1938, Dec.1998

1. The structure of a folder with differential outputs.

   * A practical folder has 5 amplifiers.

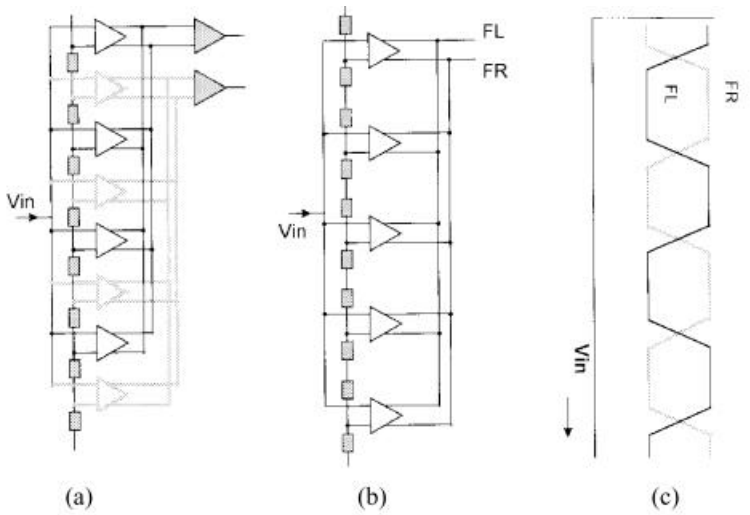


Fig. 2. (a) In this figure, a simple folder is highlighted. (b) A practical folder has an odd number of amplifiers. (c) The differential outputs are plotted.

2. A 3-bit folding converter and its cyclic code:

   * Folding rate N, full-scale sinusoid

   ⇒ Folded signal frequency $\approx \frac{p}{2}$ N·frequency Fin

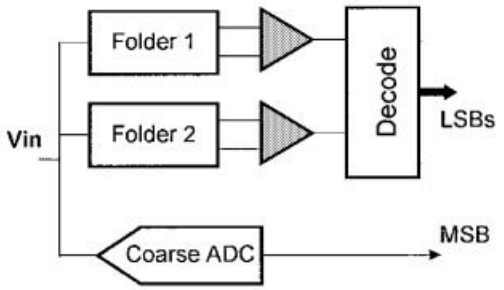


Fig. 3. A more complete diagram of a 3-bit folding converter.

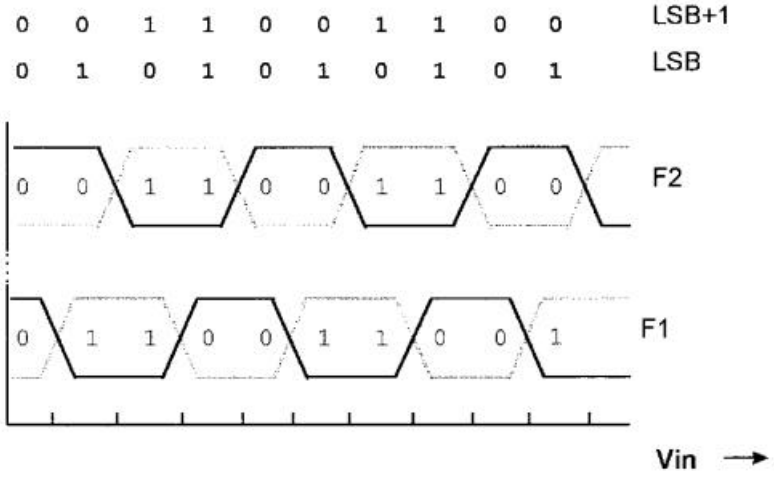


Fig. 4. The figure shows the cyclic code generated by the two comparators. The 2-bit decoded binary value is also shown.

3. The block diagram of the 6-bit converter

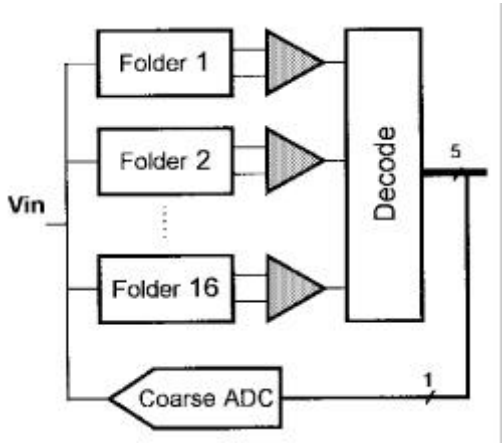


Fig. 5 Block diagram of the 6-bit converter

4. The folder structure:

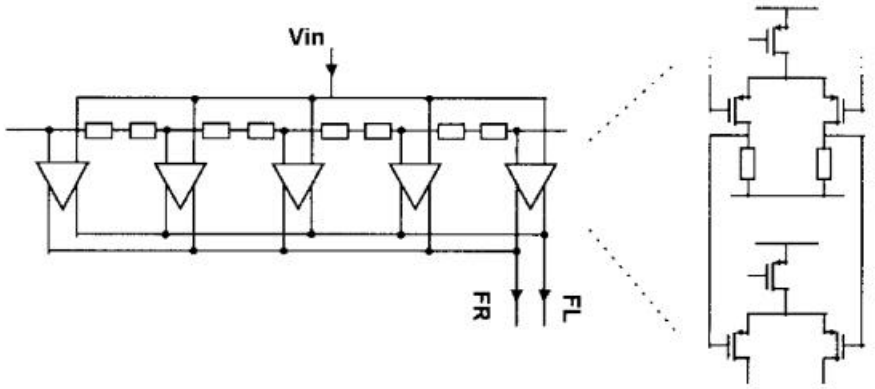


Fig. 6. The folder is made of five two-stage amplifiers. The reference ladder is shared among all the folders.

* Folding rate: 4

  Interpolation: 2

* 16 comparators and 16 folders → cyclic thermometer → 5 LSBs.

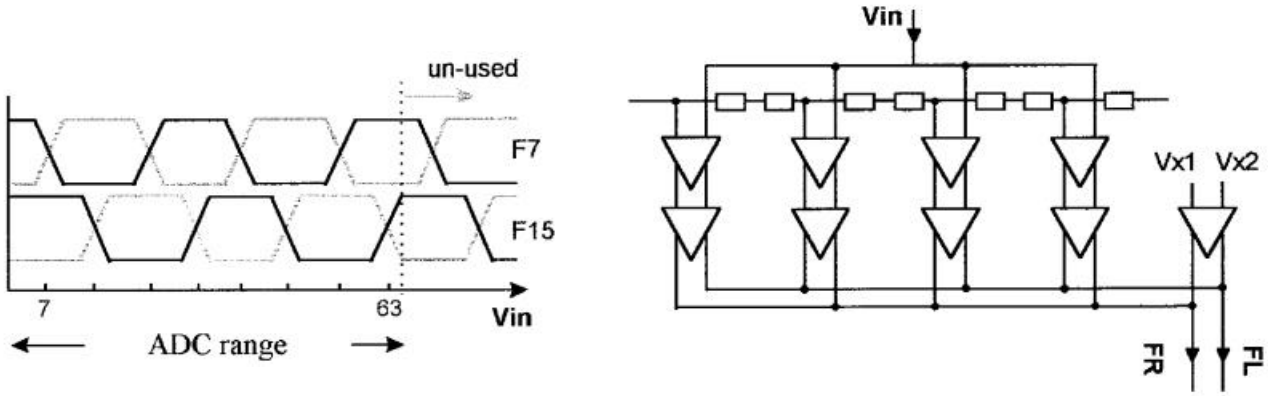
* 5 amplifiers are used

* Two stages → higher gm.

* Resistor load → better transient performance.

* Output current mode → speed ↑.

5. Practical folders:



(a) (b)

Fig. 7 (a) The contribution of the fifth amplifier goes unused.
(b) This redundancy is used to reduce the number of preamplifiers

* Vx1 and Vx2 are fixed voltages generated by a single preamplifier shared by all folders.

* Power dissipation ↓.

6. Interpolation with current-mode folder signals

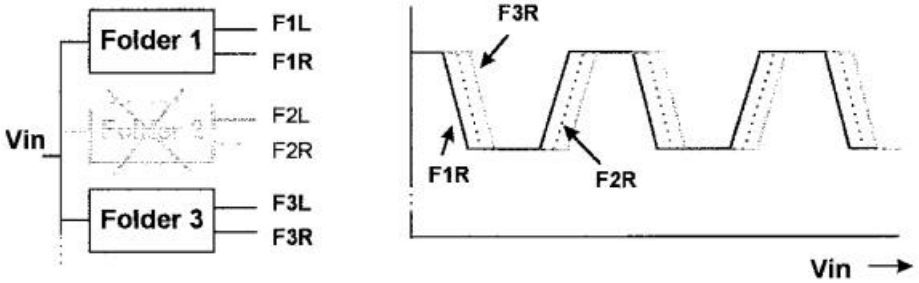


Fig. 8. Interpolation can be used to eliminate half or more of the folder blocks

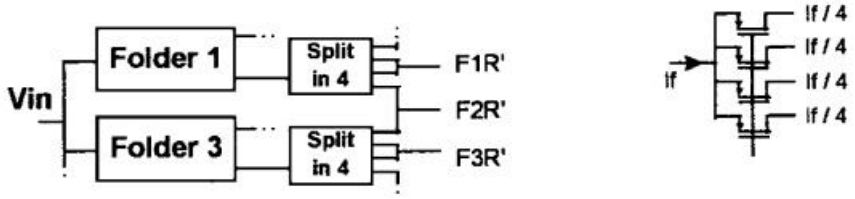


Fig. 9. Interpolation with current-mode folder signals. A current split-in-four block is shown on the right.

* The number of folders ↓. ⇒ 16 → 8

* Problems: (1) It adds an extra node to the signal path, reducing the bandwidth of the folder circuit.

(2) It does not work readily at low power supply voltages.

* Improved circuit:

Merge the current division within the folder.

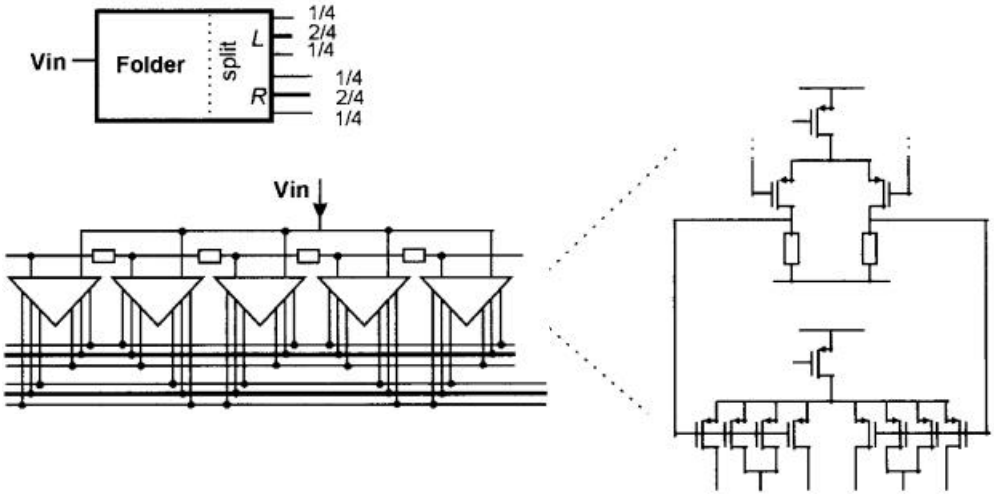


Fig. 10. The folder is modified to include current division. The modified amplifier is on the right. A block diagram for a modified folder is also shown.

* Fast operation and low-voltage operation.

7. Comparator design

(1) First stage:

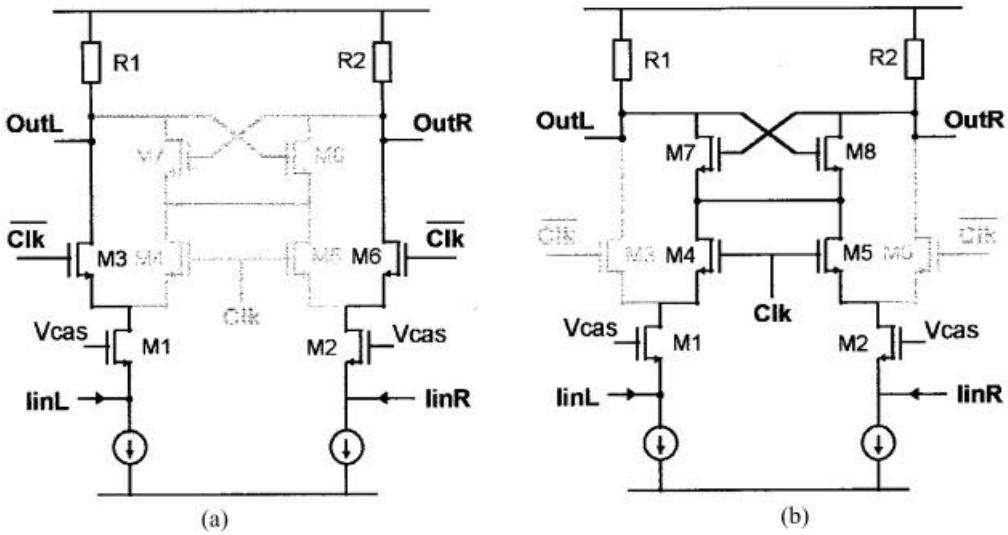


Fig. 12. The comparator core (a) tracking and (b) latching.

* Current-input voltage-output comparator.

* Resistor load.

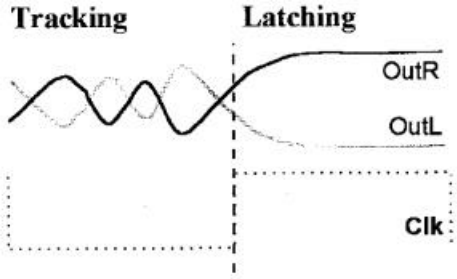


Fig. 13. Output voltage of comparator first stage during tracking and latching.

* Advantages:

(a) Currents are summed to drive the latch (i.e. Iin_L + Iin_R) ⇒ The input signal has very little effect after latching begins.

(b) Iin_L and Iin_R always flow from tracking to latching ⇒ The folders are little disturbed.

* Need the second-stage buffer and latch.

(2) Second stage:

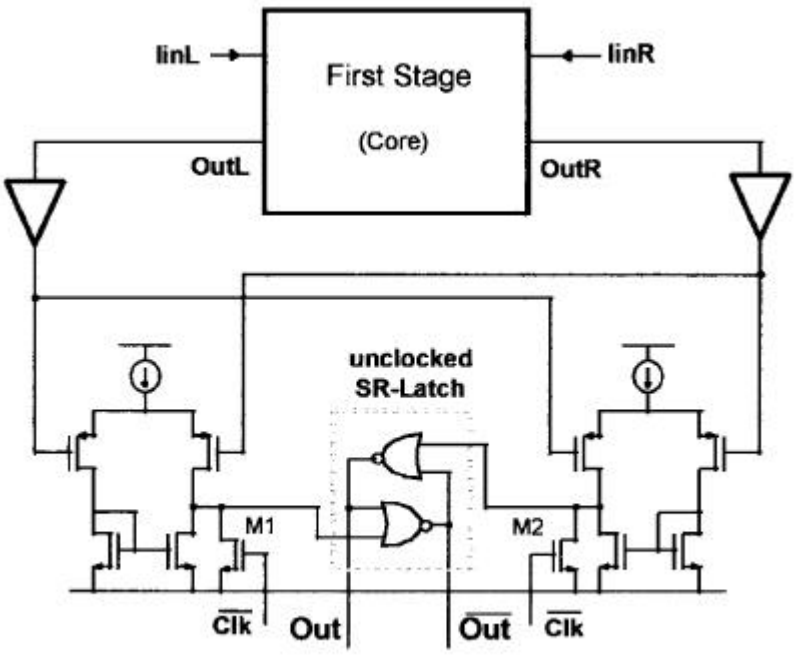


Fig. 14. Comparator second stage.

(3) Third stage to reduce metastability errors:

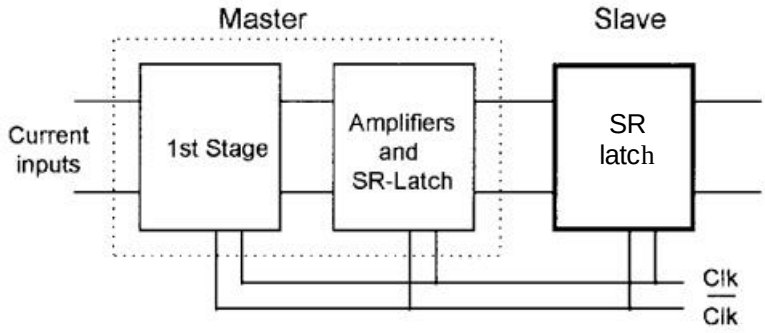


Fig. 15. Three comparator stages.

8. Complete ADC block diagram

The sync block: To suppress the delay mismatch between the coarse ADC and the rest of the circuitry (i.e. the fine converter)

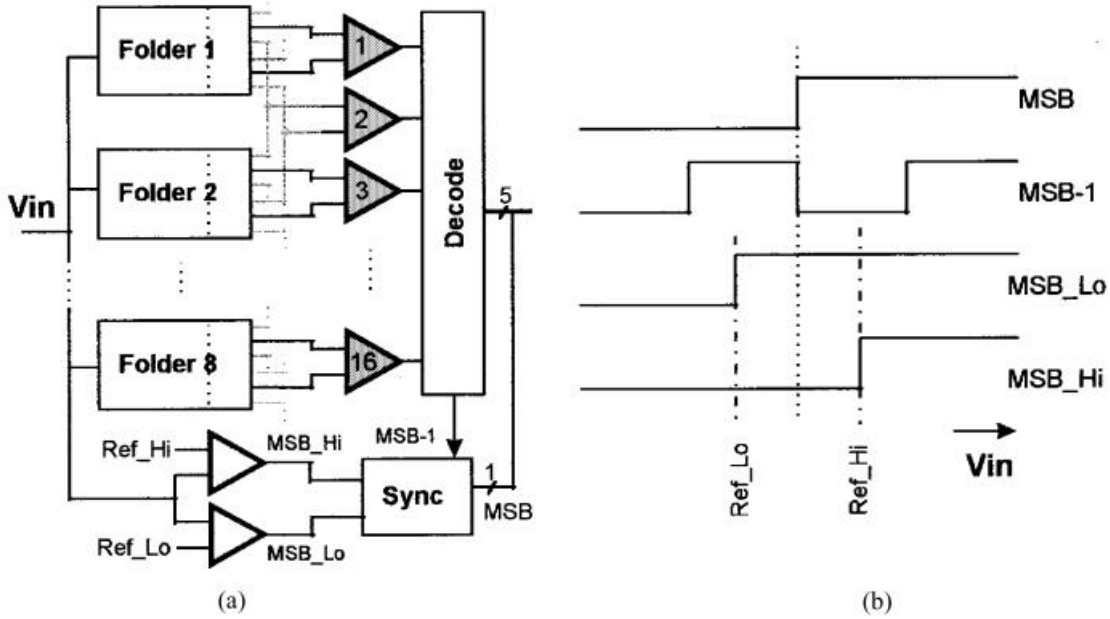


Fig. 16. (a) ADC block diagram with detail of coarse ADC. (b) Coarse ADC waveforms

* MSB-Lo and MSB-Hi are offset by $\frac{1}{8}$ Fs at either side of the MSB transition voltage.

* If MSB-1 = 0, MSB = MSB - Lo

  If MSB-1 = 1, MSB = MSB - Hi

* Can tolerate a relative offset of up to $\pm\frac{1}{8}$ Fs.

9. Measurement results:

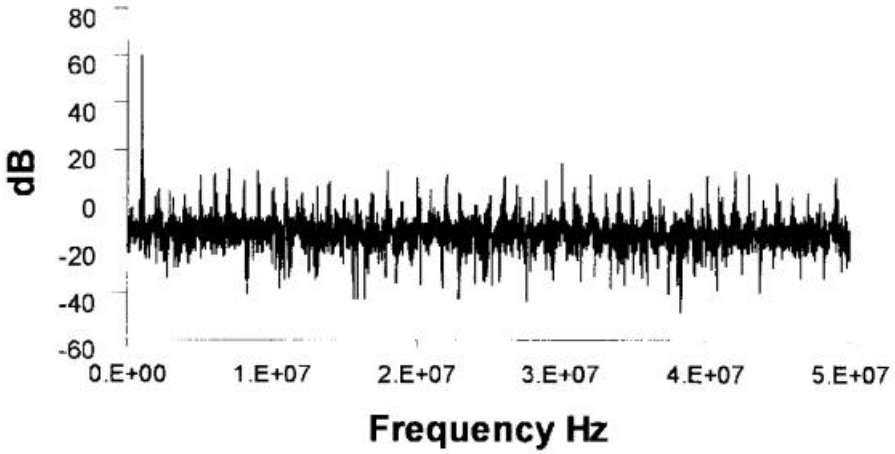


Fig. 17. FFT for 1-MHz sinusoid sampled at 400 Msample/s (decimated).

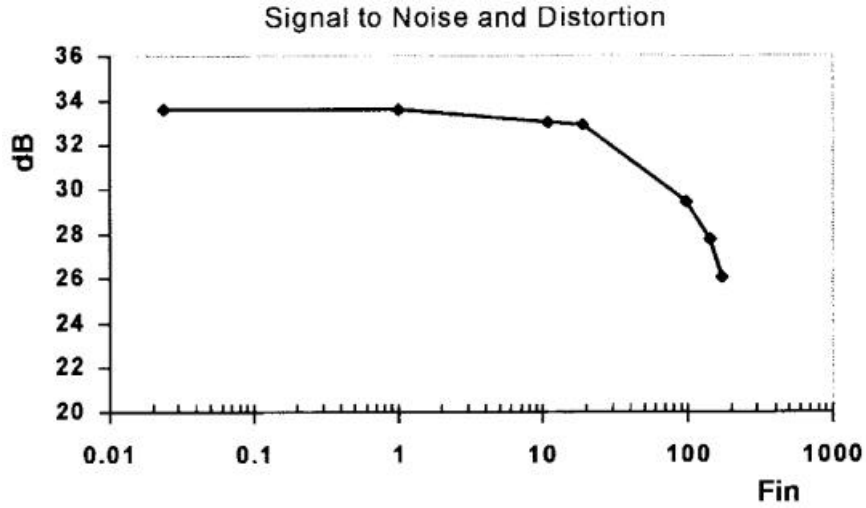


Fig. 18. SNDR versus input frequency at 400 Msample/s

TABLE I
PERFORMANCE SUMMARY

Technology	0.5mm BiCMOS (CMOS only)
SNDR (1MHz sine-wave)	33.6dB @ 400Msample/s 32.9dB @ 450Msample/s
Supply voltage	3.2V
Power	200mW
Area	0.6μm^2
Input capacitance	1.4pF

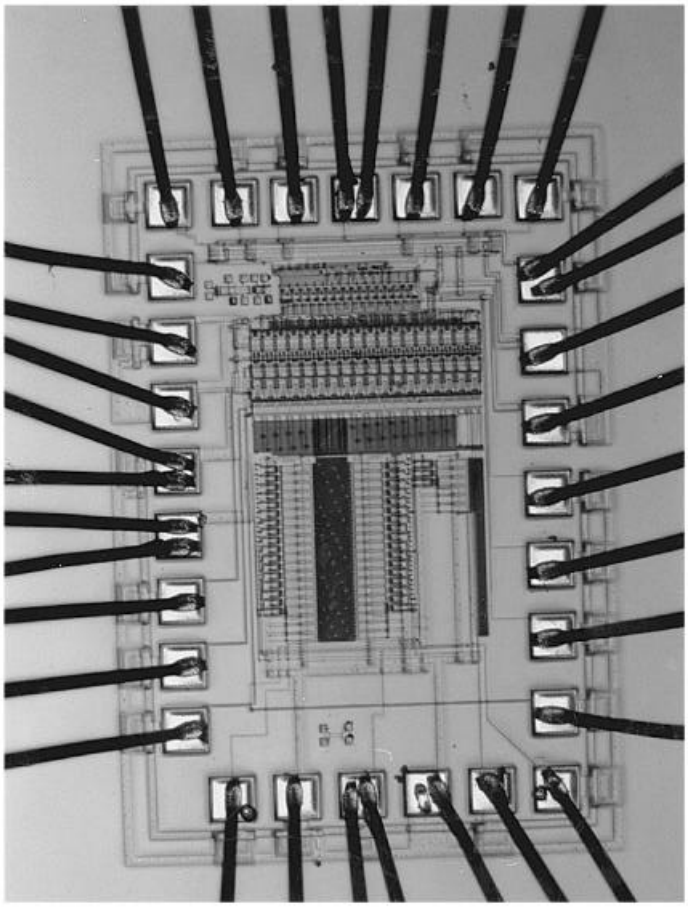
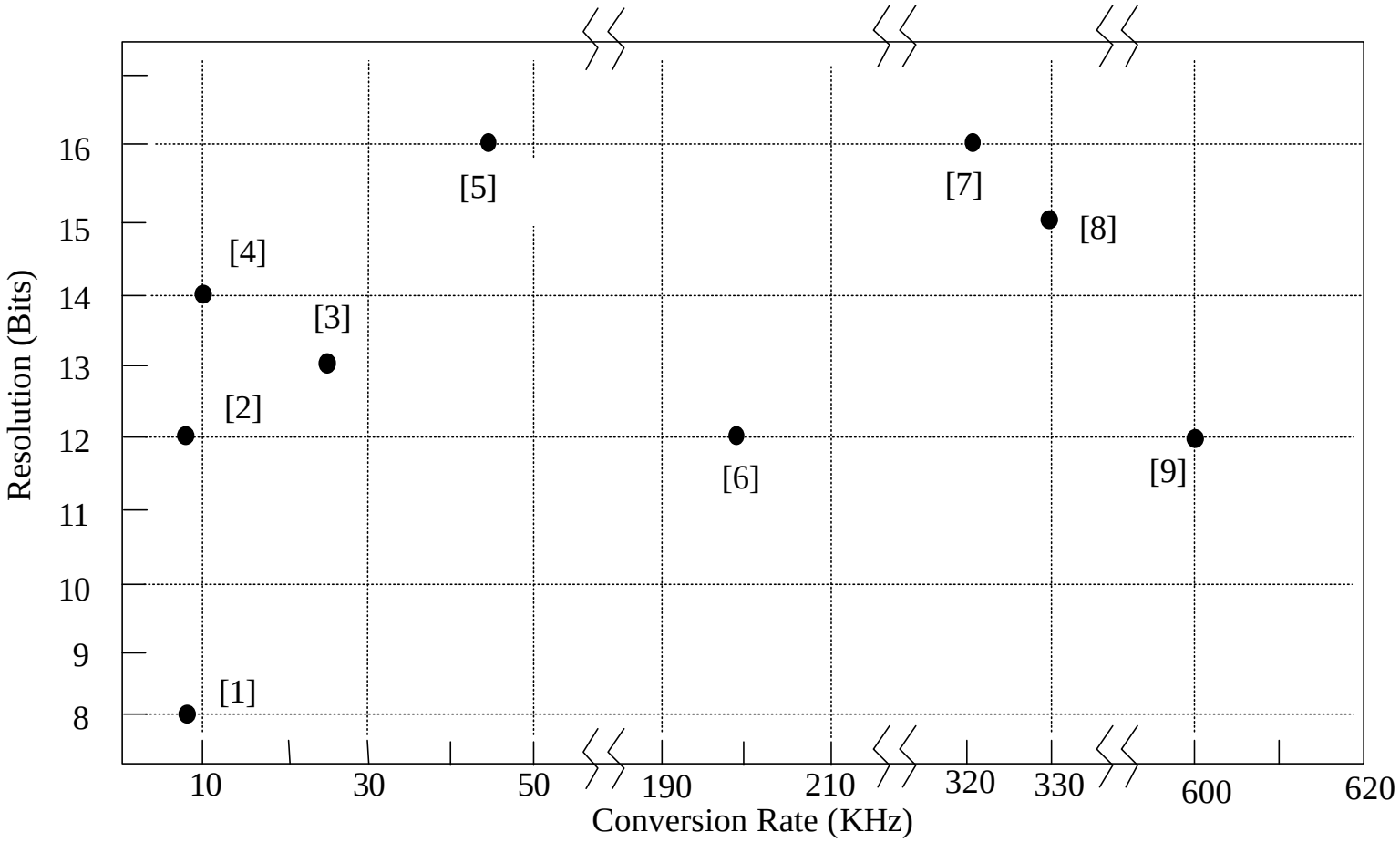
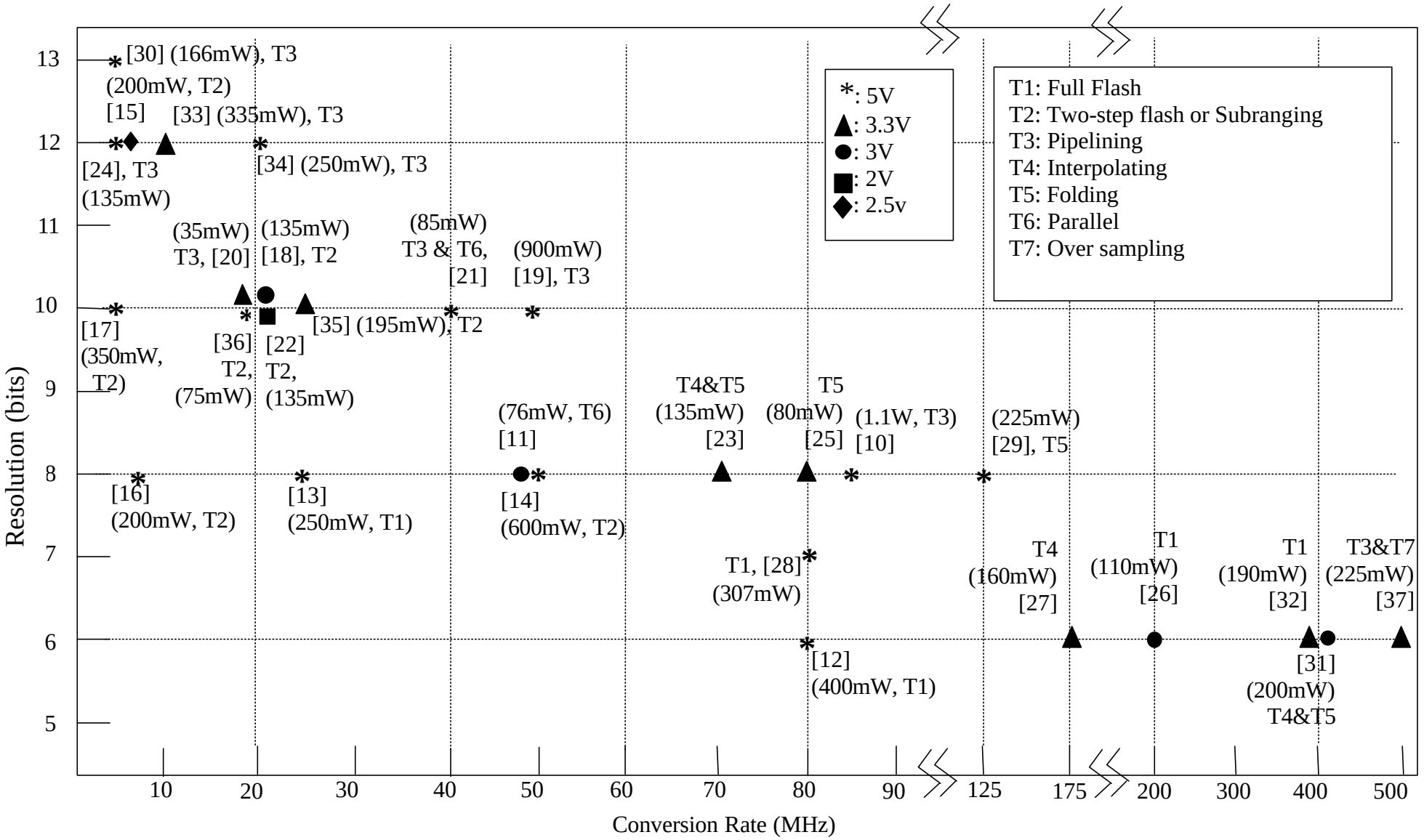


Fig. 19. Die photo

§13-9 Summary



Resolution versus sampling frequency plot of
recently reported CMOS audio A/D converters



Resolution versus sampling frequency plot of recently reported CMOS video A/D converters

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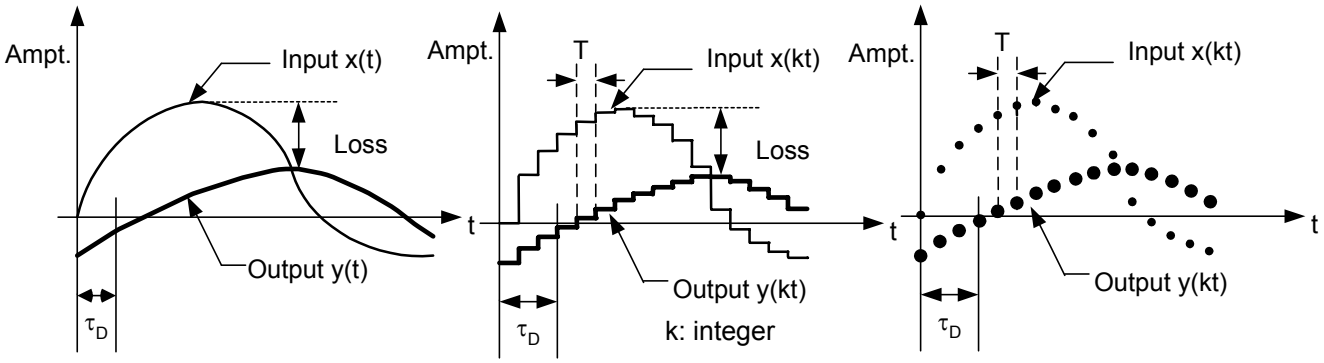
CH 14. MOS Switched-Capacitor Filter Design

§14--1 Preliminary Considerations

§14-1.1 Classification of systems and filters

1. Continuous-time, discrete-time, and sampled-data systems



continuous-time system — sampled-data system — discrete-time system

e.q.: analog Filter — e.q.: SCF — e.q.: digital filter

differential equations — difference equations

2. Tine-invariant systems and causal systems

T.I. : x(kt)→ y(kt) => x[(k-n)T]→ y[(k-n)T] for any x(kt) and n.

Causal : x(mt) => y(kT)=0 for k<m

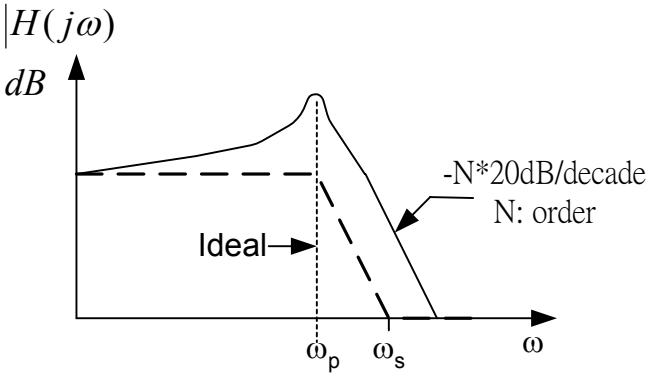
3. Filter types:

(1) Low-Pass(LP)

$$H(s)=\frac{K\omega_p^{\,2}}{S^2+(\omega_p/Q_p)S+\omega_p^2}$$

(biquad)

Two complex poles (LHP)



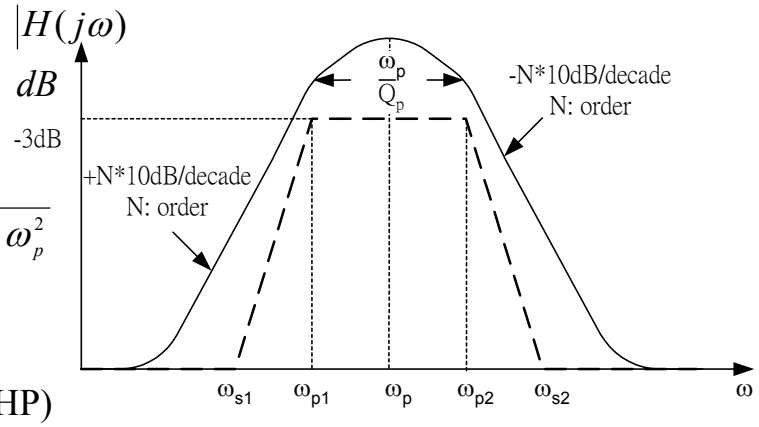
(2) High-Pass(HP)

$$H(s)=\frac{KS^2}{S^2+(\omega_p/Q_p)S+\omega_p^2}$$

Two complex poles(LHP)
Two zeros at S=0

3) Band-Pass(BP)

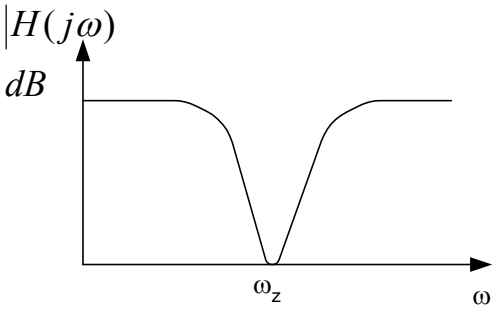
$$H(s)=\frac{K(\omega_p/Q_p)S}{S^2+(\omega_p/Q_p)s+\omega_p^2}$$



center freq. gain: k
center freq. ω_p
Two complex poles (LHP)
One zeros at S=0

4)Band-Reject(BR)

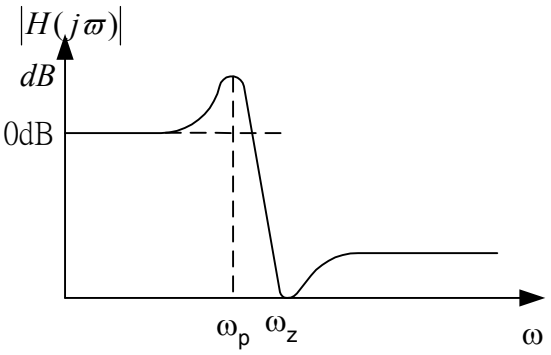
$$H(s)=\frac{K(S^2+\omega_z^2)}{S^2+(\omega_z/Q_p)s+\omega_p^2}$$



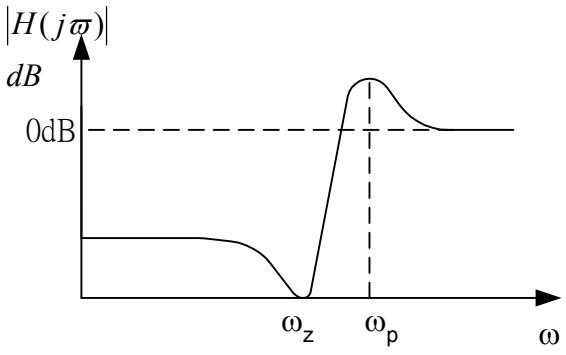
$\omega_p=\omega_z$
Two complex poles(LHP)
Two imaginary zeros

$\omega_p>\omega_z$ High-Pass Notch filter (HPN)
$\omega_p<\omega_z$ Low-Pass Notch filter (LPN)

(5)Low-Pass Notch (LPN)



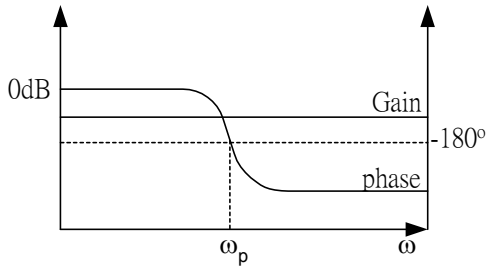
(6)High-Pass Notch



(7)ALL-Pass (Delay Equalizer)

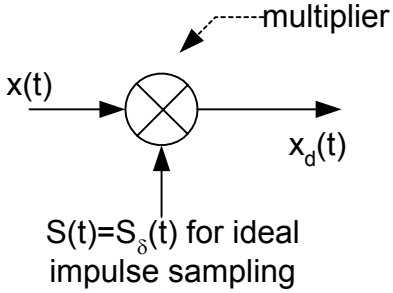
$$H(S)=\frac{S^2-(\omega_p/Q_p)S+\omega_p^2}{S^2+(\omega_p/Q_p)S+\omega_p^2}$$

Two complex poles (LHP)
Two complex zeros (RHP)
mirror-imaged



§14-1.2 Sampling Process

§ ideal impulse sampling:



$S(t)=S_\delta(t)=\sum_{k=-\infty}^{\infty}S(t-k\tau)$

τ: sampling period

$x_d(t)=x(t)S_\delta(t)=x(t)\sum_{K=-\infty}^{\infty}\delta(t-k\tau)=\sum_{k=-\infty}^{\infty}x(t)\delta(t-k\tau)$

remember: $\int_{-\infty}^{\infty}\delta(t-k\tau)dt=1$ $\delta(t-k\tau)=0$ for $t\neq k\tau$

$=> x_d(t)=\sum_{k=-\infty}^{\infty}x(k\tau)\delta(t-k\tau)$

Fourier transformation of $S_\delta(t)$: $S_F(t)=\sum_{k=-\infty}^{\infty}c_k e^{jk\omega_s t}$ $\omega_s\equiv\frac{2\pi}{\tau}$

Where $C_k\equiv\frac{1}{\tau}\int_{-\frac{\tau}{2}}^{\frac{\tau}{2}}s(t)\ e^{jk\omega_s t}\,dt=\frac{1}{\tau}$

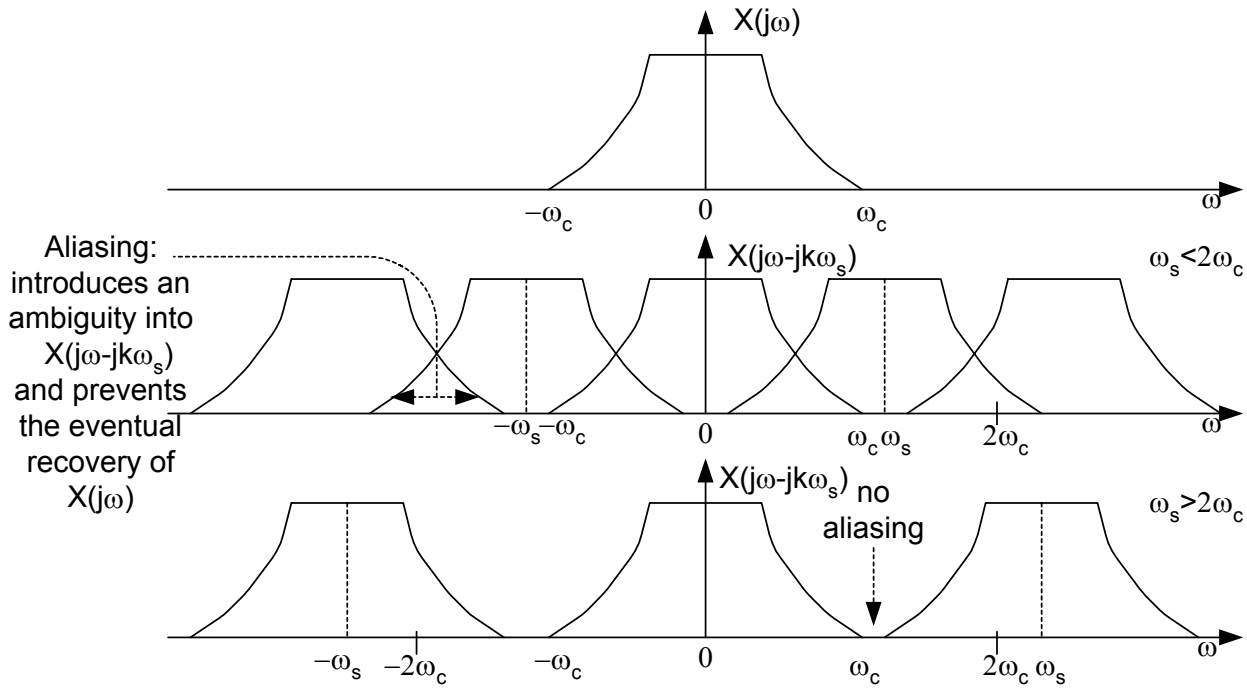
$=>x_d(t)=x(t)S_F(t)=\sum_{k=-\infty}^{\infty}C_k x(t)e^{jk\omega_s t}$

$F[x_d(t)]=F[\sum_{k=-\infty}^{\infty}C_k x(t)e^{jk\omega_s t}]=\sum_{k=-\infty}^{\infty}C_k F[x(t)e^{jk\omega_s t}]$

$=\sum_{k=-\infty}^{\infty}C_k\ X(j\omega-jk\omega_s)$ where $F[x(t)]\equiv X(j\omega)$, k=±integer

↓

base-band spectrum



Sampling Theorem:

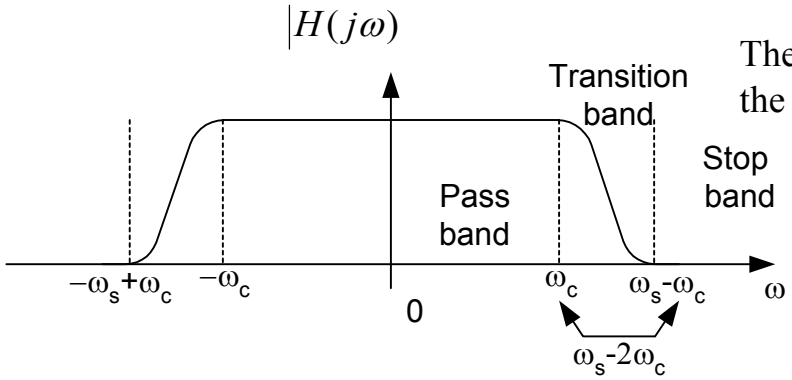
A function x(t) that has a Fourier spectrum X(jω) such that X(jω)=0 for $|\omega| \geq \omega_s/2$ is uniquely described by a knowledge of its values at uniformly spaced time instants, τ instants apart($\tau = 2\pi / w_s$)

$2\omega_c$: Nyquist rate.

Anti-aliasing filter is required.

Reconstruction filter is also required to recover x(t).

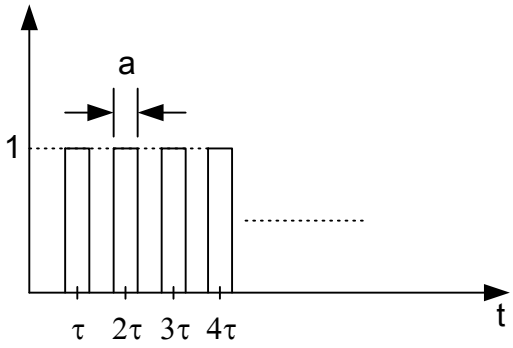
spec



The smaller the ω_s-$2\omega_c$ (TB), the higher the filter order!

§ Finite -Pulse Sampling (non-ideal sampling):

$$S_p(t)=\sum_{k=-\infty}^{\infty}[u(t-k\tau-\frac{a}{2})-u(t-k\tau+\frac{a}{2})] \quad a>0$$

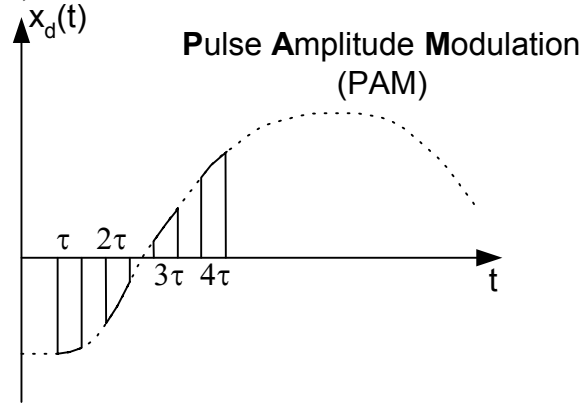


$$C_k=\frac{1}{\tau}\int_{-\frac{\tau}{2}}^{\frac{\tau}{2}} S_p(t)\ e^{-jk\omega_s t}\,dt$$

$$=\frac{1}{\tau}\int_{-\frac{a}{2}}^{\frac{a}{2}} e^{-jk\omega_s t}dt=\frac{a}{\tau}\frac{Sin(k\omega_s a/2}{k\omega_s a/2}$$

Now, we have $\sin\alpha/\alpha$ envelope onto X ($j\omega$-$jk\omega_s$)

$$\alpha\equiv k\omega_s a/2$$



§14-1.3 Z-Transformation

$$x_d(t)=\sum_{k=-\infty}^{\infty}x(k\tau)\delta(t-k\tau)$$

Laplace Transformation => $X_d(s)=L[x_d(t)]=\sum_{k=-\infty}^{\infty}x(k\tau)e^{-ks\tau}$

Let $\underbrace{z=e^{s\tau}}$ => $X(z)=\sum_{k=-\infty}^{\infty}X(k\tau)z^{-k}$ two-sided z-transform

$S=j\omega \quad z=e^{j\omega\tau}$

$X(z)=\sum_{k=0}^{\infty}X(k\tau)z^{-k}$ one-sided z-transform

example 1: $x(t)=u(t)=>x(k\tau)=1=>X(z)=\sum_{K=0}^{\infty}Z^{-k}=\frac{1}{1-z^{-1}} \quad |z|>1$

example 2: $x(t)=e^{-at}u(t)=>x(k\tau)=e^{-ak\tau}=>X(z)=\sum_{k=0}^{\infty}e^{-akz}z^{-k}=\frac{1}{1-e^{-a\tau}z^{-1}}$

for $|z|>e^{-a\tau}$

For single input/output, linear, time-invariant, sampled data (or discrete-time) system:

$$y(k\tau)+\sum_{n=1}^{N}b_n\,y[(k-n)\tau]=\sum_{n=0}^{M}a_n\,x[(k-n)\tau]$$

M.N: non-negative integers

Two cases:(1) $b_n = 0$ for all n => nonrecursive system

M+1 tap transversal filter
Finite-Duration Impulse Response(FIR)Filter

(2) $b_n \neq 0$ for $n \geq 1$ => Nth-order recursive system

Infinite Impulse Response(IIR) Filter

z-transform:

$$Y(z)(1+\sum_{n=1}^{N} b_n Z^{-n}) = X(z)\sum_{n=0}^{M} a_n z^{-n}$$

$$H(z)=\frac{Y(z)}{X(z)} = \frac{\sum_{n=0}^{M} a_n z^{-n}}{1+\sum_{n=1}^{N} b_n z^{-n}}$$ pulse transfer function

$$= \frac{a_\circ (1-\beta_1 Z^{-1})(1-\beta_2 Z^{-1}).....(1-\beta_N Z^{-1})}{(1-\alpha_1 Z^{-1})(1-\alpha_2 Z^{-1}).....(1-\alpha_N Z^{-1})}$$

$z=\alpha_i$: poles
$z=\beta_i$: zeros

Mapping between Z-plane and S-plane:

$z=e^{s\tau}$ $s=\sigma+j\omega$ => $z=e^{\sigma\tau}e^{j\omega\tau}$ $\tau=\frac{2\pi}{\omega_s}$

For $\omega_s>2\omega_0$, the base-band response $X(j\omega)$ over the range $-\frac{\omega_s}{2} \leq \omega \leq \omega_s/2$ is sufficient to determine $X(j\omega)$ for all ω.

* $-\frac{\omega_s}{2} \leq \omega \leq \omega_s/2$, $-\infty<\sigma<\infty$ => all Z-plane $\angle Z = -\pi \rightarrow \pi$

$-\frac{3\omega_s}{2} \leq \omega \leq -\frac{\omega_s}{2}$, $-\infty<\sigma<\infty$ => overlap on Z-plane $\angle Z = -3\pi \rightarrow -\pi$

$\frac{\omega_s}{2} \leq \omega \leq \frac{3\omega_s}{2}$, $-\infty<\sigma<\infty$ => overlap on Z-plane $\angle Z = \pi \rightarrow 3\pi$

* $\omega=\omega_1$, $-\infty<\sigma<\infty$ => a straight line from z=0 to $z=\infty$ with angle $\omega_1\tau$

* $j\omega$ axis => $\sigma=0$ => $|z|=1$ unit circle

* $\sigma>0$ $|z|>1$ for all ω => RHP $\rightarrow$ outside the $|z|=1$ circle

* $\sigma<0$ $|z|<1$ for all ω => LHP $\rightarrow$ inside the $|z|=1$ circle

* S=0 z=1 ; ω=0 $-\infty<\sigma<+\infty$ => Real Z axis (positive)

First-order transfer function:

$H(z)=\frac{1}{1-az^{-1}}$ Z=a is the pole

h(kτ) k=0, 1, 2, 3,…….

$z=a=e^{\sigma\tau}e^{j\omega\tau}$

(1)a>1, diverging unstable

(2)a=1 sequence of 1's unstable

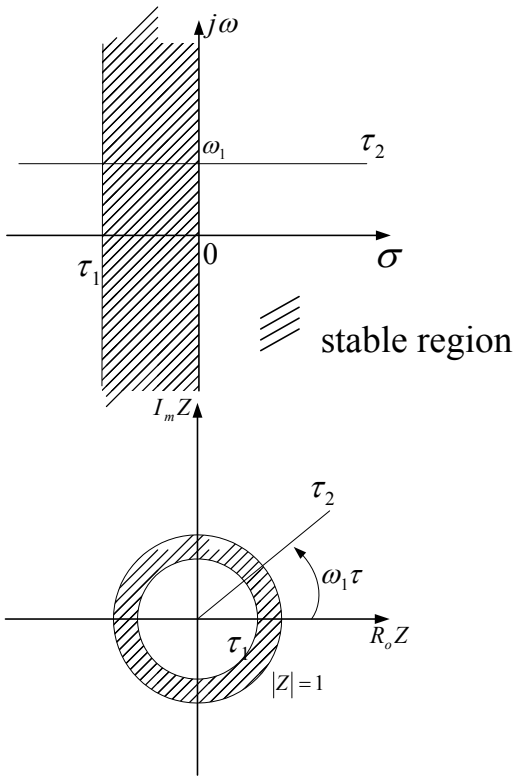
(3)$a\geq 0$ a<1 stable

(4)$-1<a\leq 0$ stable σ<0, ωτ=±π

ωkτ=±kπ

(5)a=−1 unstable

(6)a<−1 unstable



$G(\omega)=20\log[|H(Z)|_{z=e^{j\omega\tau}}]$ dB magnitude

$\phi(\omega)=\tan^{-1}\left.\frac{\mathrm{Im}\,H(Z)}{\mathrm{Re}\,H(Z)}\right|_{z=e^{j\omega\tau}}$ rad phase

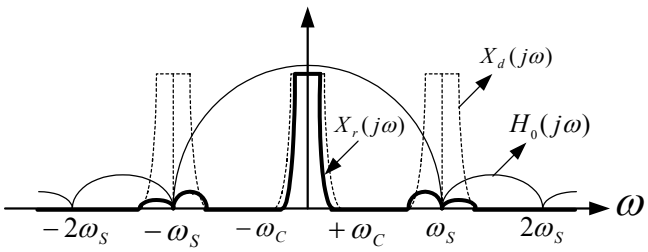
The magnitude and phase can be determined graphically in the same way as those determined from the s-plane poles & zeros.

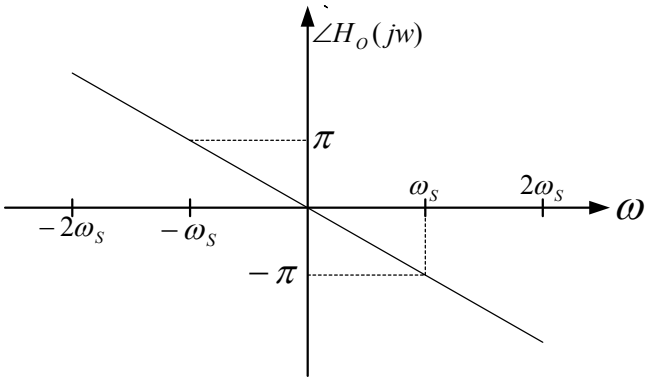
§14-1.4 Sample and Hold Circuit

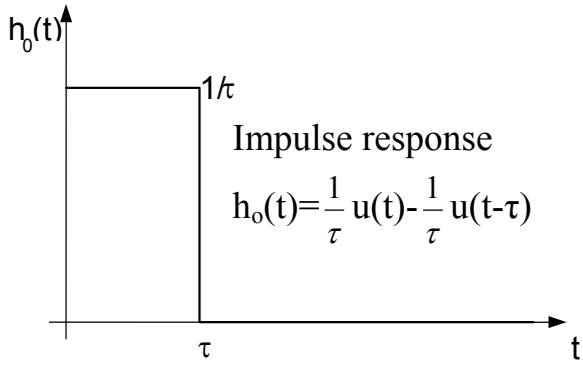
Zero-order hold or S/H function:

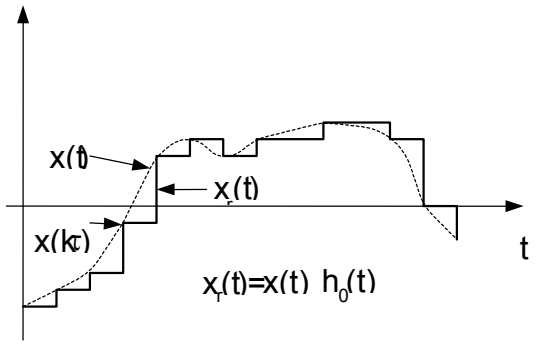
$H_o(s)=\frac{1-e^{-s\tau}}{s\tau}$

$H_o(j\omega)=e^{-j\omega\tau/2}\frac{\sin(\omega\tau/2)}{\omega\tau/2}$









* may serves as a reconstruction circuit

$X_r(j\omega)=X_d(j\omega)H_o(j\omega)$

* The different between $X_r(j\omega)$ & $X_d(j\omega)$ at $\omega \cong \pm\omega_c$ can be eliminated by setting $\omega_s/\omega_c >> 1$.

§14-2 Switched-Capacitor Network System

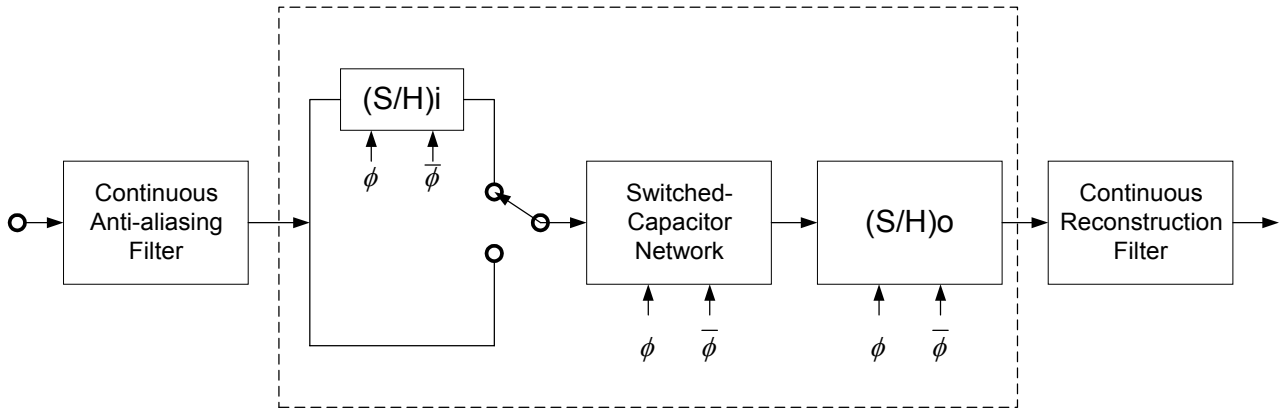
General Switched-Capacitor Network (SCN):

ideal capacitors, ideal voltage-controlled-voltage sources (VCVS's), ideal switches & sampled-data voltage inputs.

VCVS: freq. indep. gain amps or infinite gain OP amps.

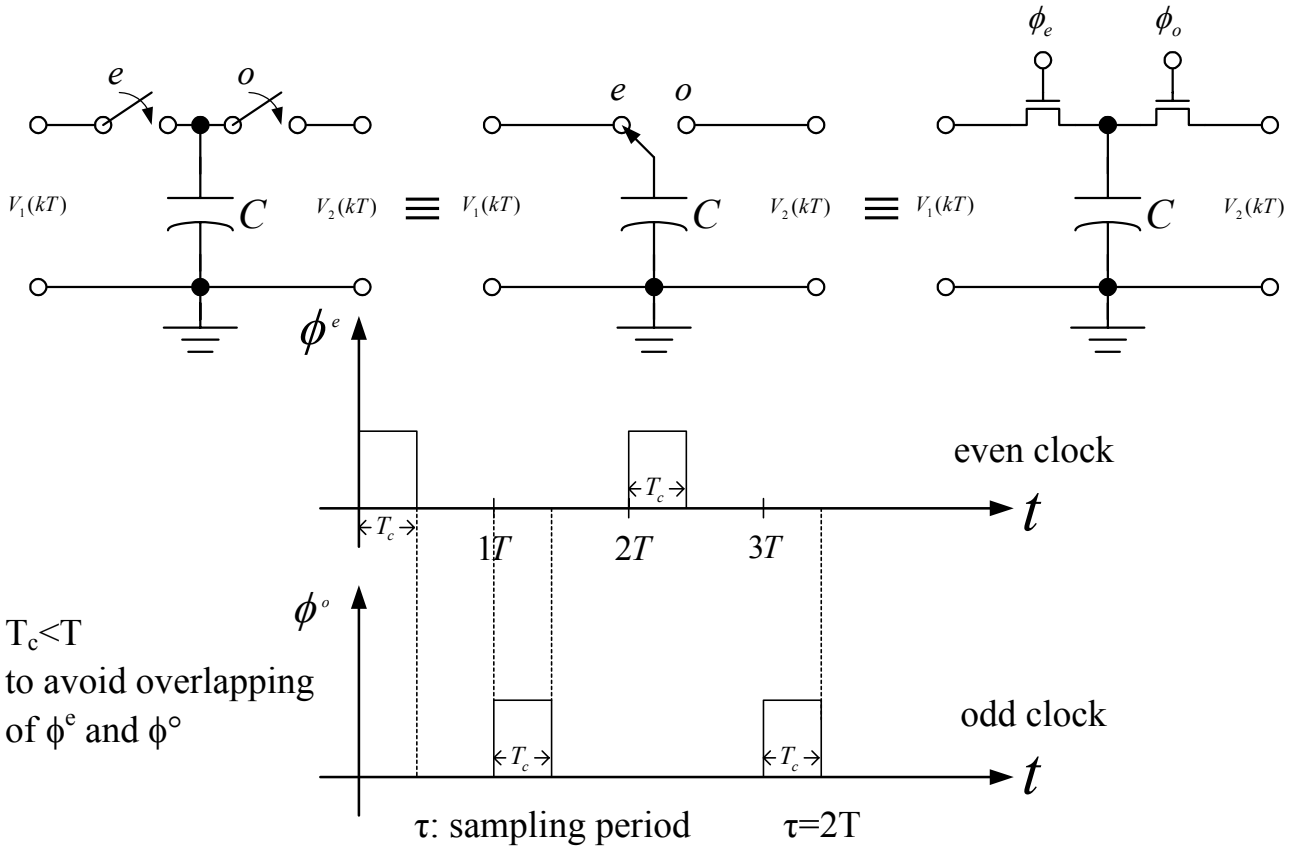
* Typically, the sampled-data voltage input is only single, not multiple.
* The input may be a continuous one.
* The effects of non-ideal switches, non-ideal OP amps, & non-ideal cap. should be considered as & second order effects.

Block diagram:



Switched-Capacitor Network
(Two-phase clock) (can be multi-phase)

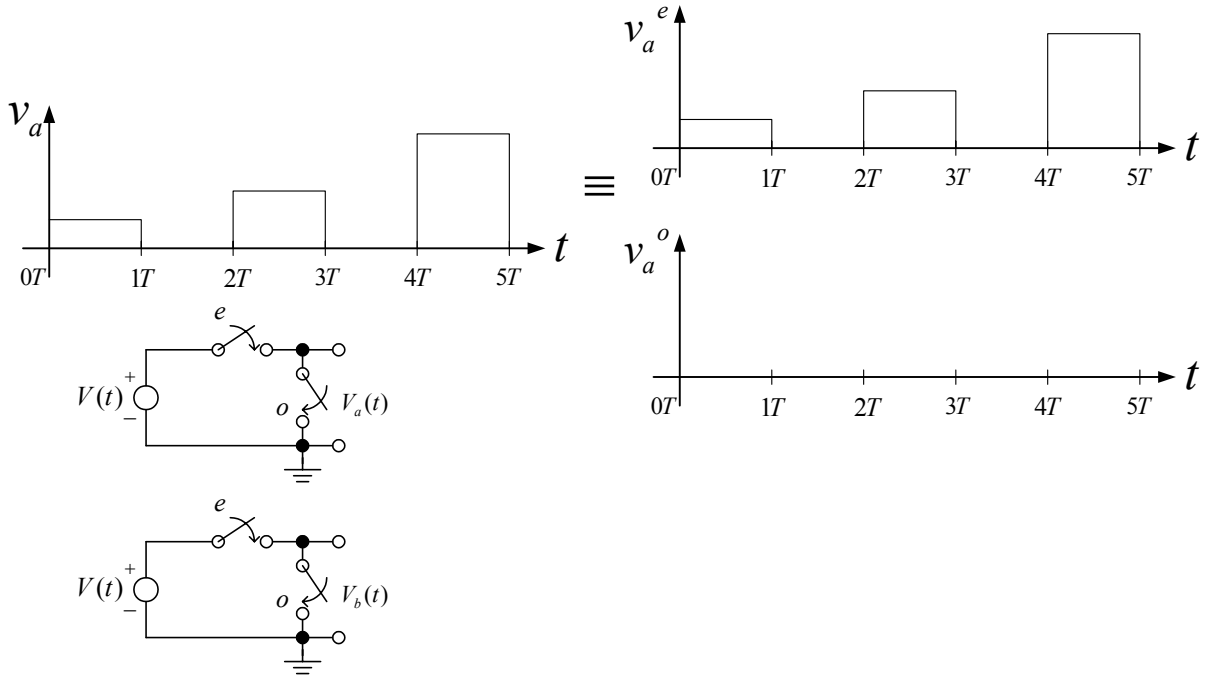
General symbols:



* Generally, SCN is time-variant since the network topology is different in the case of ϕ^e and ϕ°. However, if we separate the input/output sampled-data voltage into one even component and one odd component and separate the whole SCN into one even part and one odd part, then we have two time-invariant networks coupled together. Analysis thus can be performed.

Sampled-Data Waveforms

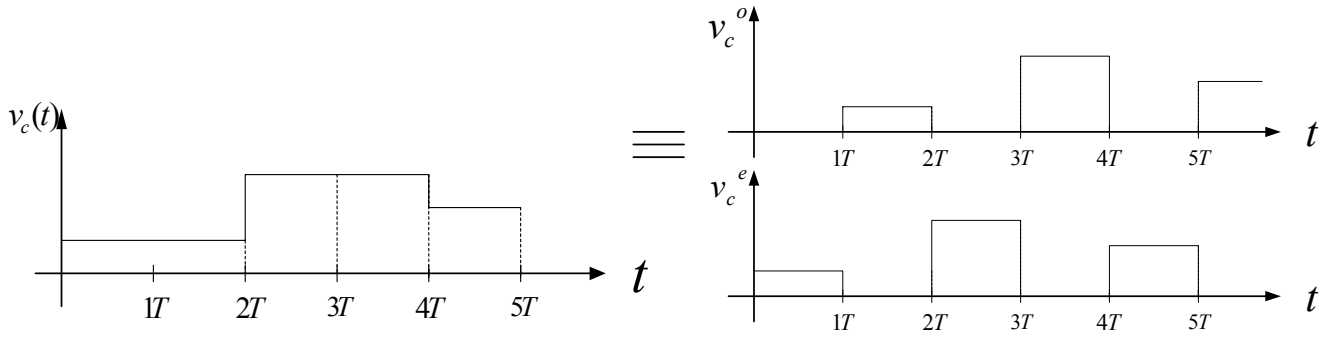
1. Return-to-zero waveforms



$V_a(z)=V_a^e(z)+V_a^0(z)=V_a^e(z)$ $\qquad V_a^0(z)=0$

Similarly, we have $V_b(z)=V_b^e(z)+V_b^0(z)=V_b^0(z)$ $\qquad V_b^e(z)=0$

2. Full-clock-period (Full-cycle) sample-and-hold waveforms

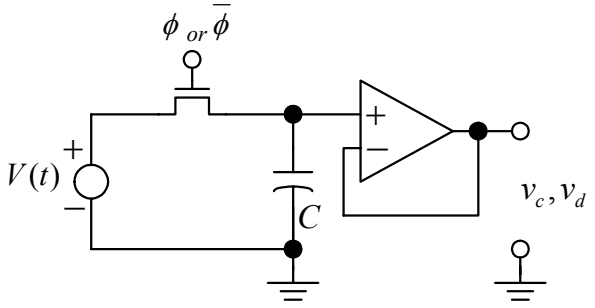


$V_c(z)=V_c^e(z)+V_c^0(z)$

$V_c^0(z)=Z^{-\frac{1}{2}}\ V_c^e(z)$ $(\because V_c^0(kT)=V_c^e[(k-1)T])$

Similarly, we have $V_d(z)=V_d^e(z)+V_d^0(z)$

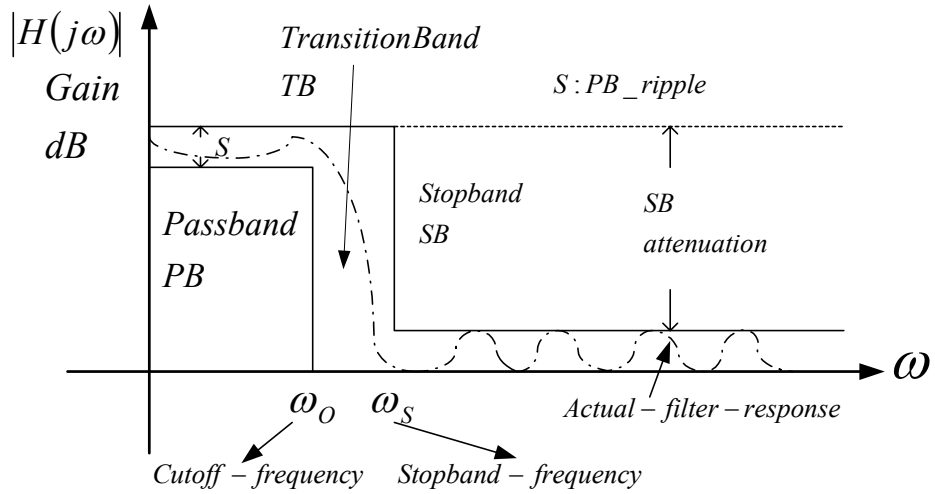
$$V_d^e(z)=Z^{-\frac{1}{2}}V_d^0(z)$$

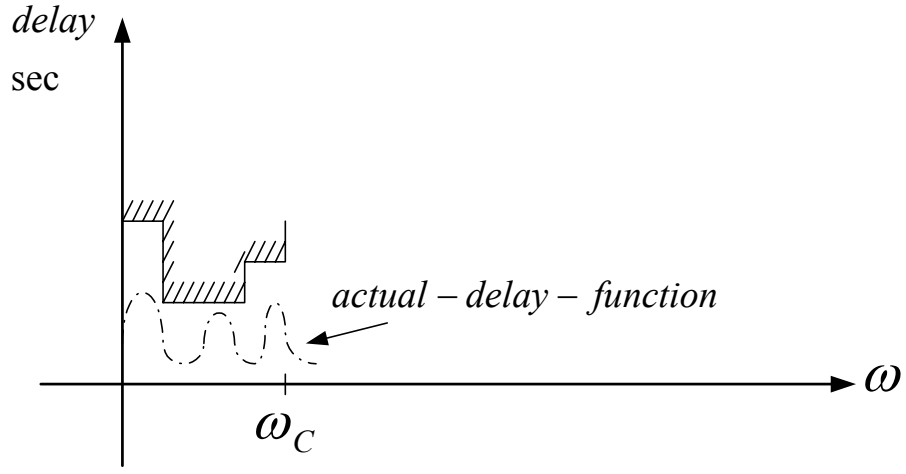


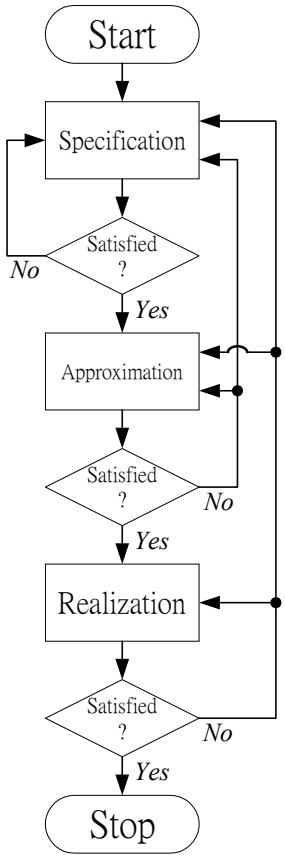
Full-cycle S/H circuit

§14-3 Filter Design Process

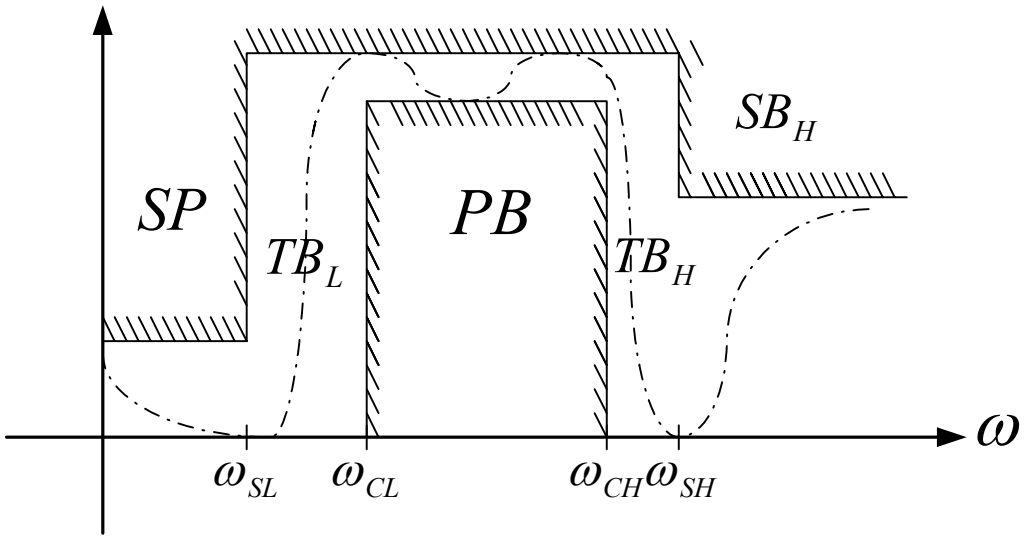
1. Specification
   (1) Low-Pass Filter
   Specification:







(2) Band-Pass Filter



2.Approximation

(1) Classical approximation

a. Butterworth

b. Chebyshev

c. Elliptic

d. Bessel

(2) Modern approximation

3.Realization

Two methods:

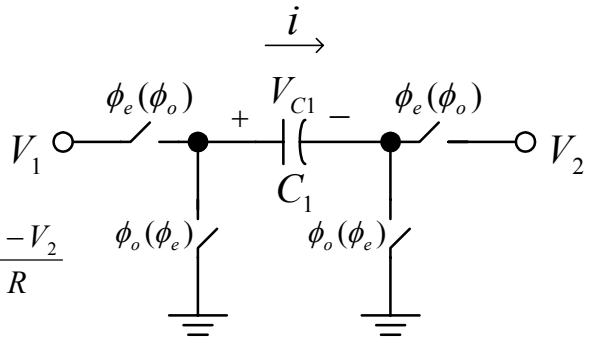
(1) Realization of the biquad (2^{nd} order filter)and the first-order filter＝>cascade or couple them to form a high-order filter.

(2) Realize H(s) using LC network＝>replace L by some integrated-circuit simulator or simulate the LC network using integrators.

* Low-sensitivity, high-performance

§14-4 SC Integrators via OP AMPS

§14-4.1 SC Inverting Integrator



$\phi_o(\phi_e)$: $V_{c1}=0$

$\phi_{e(}\phi_{o)}$: $V_{c1}=V_1-V_2$

$\Delta Q=C_1(V_1-V_2)$

$$\frac{\Delta Q}{T} \equiv i = C_1 \frac{V_1 - V_2}{T} = C_1 f (V_1 - V_2) \equiv \frac{V_1 - V_2}{R}$$

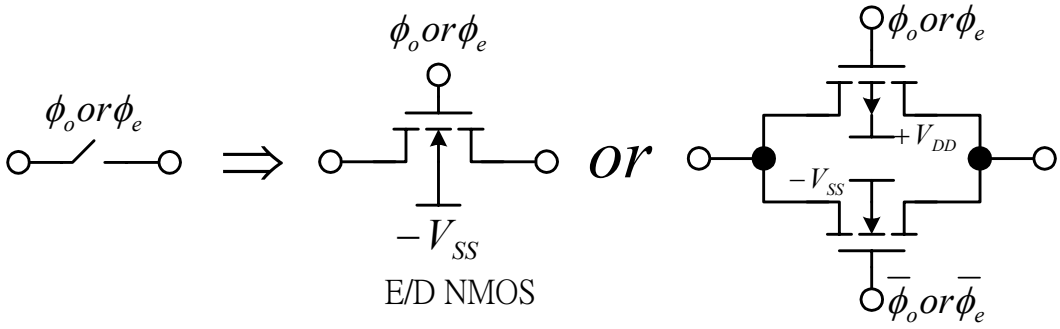
$=>R=\frac{1}{C_1 f}$ f: clock frequency

f=100KHz, C_1=10PF

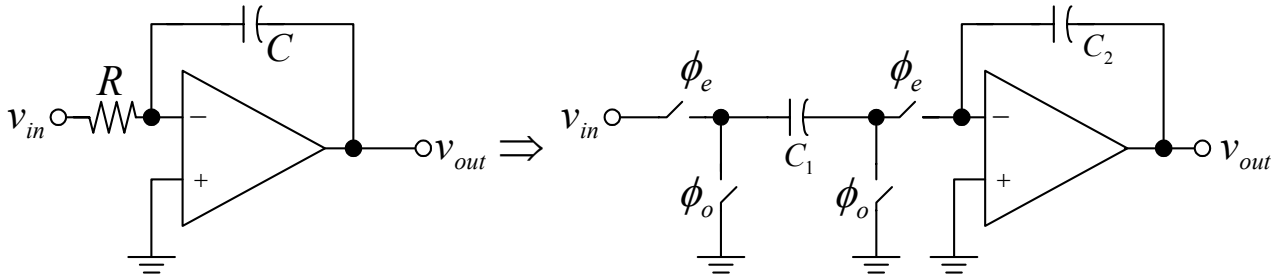
=>SC simulated positive resistor

=> R=1MΩ

Switch realizations:

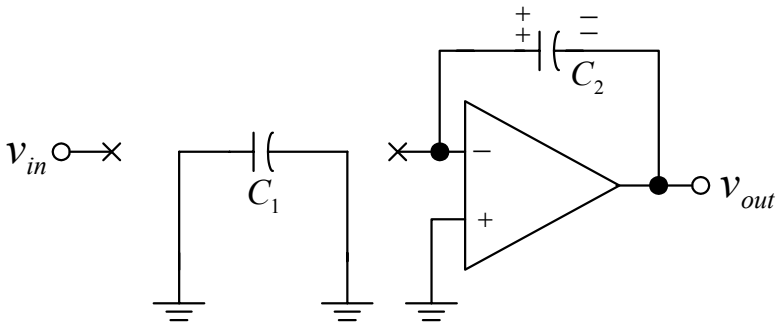


The inverting SC integrator

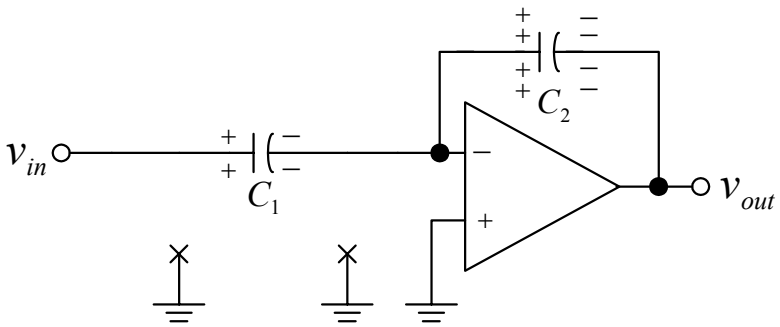


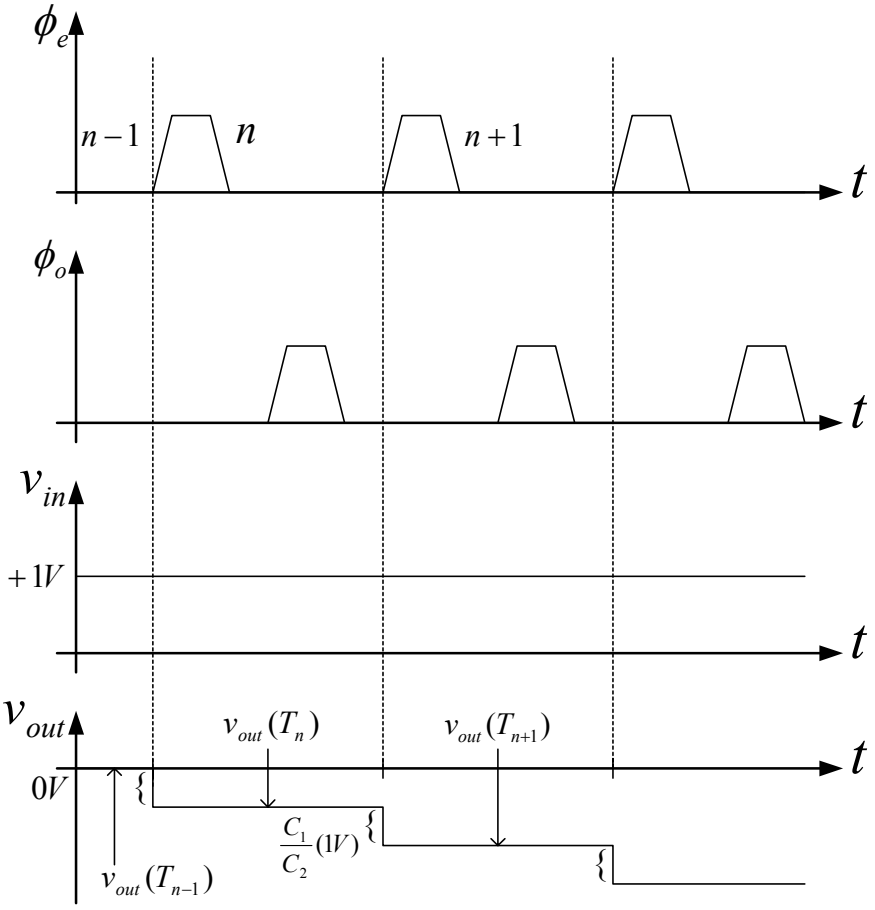
Operation:

(1)ϕ_o phase


v_{in}
C_1
C_2
v_{out}

(2)ϕ_e phase


v_{in}
C_1
C_2
v_{out}


ϕ_e
$n-1$
n
$n+1$
t
ϕ_o
t
v_{in}
$+1V$
t
v_{out}
$v_{out}(T_n)$
$v_{out}(T_{n+1})$
t
$0V$
$v_{out}(T_{n-1})$
$\frac{C_1}{C_2}(1V)$

"Ideal OP AMP"

$V_{out}(T_n)=V_{c2}(T_n)=V_{out}(T_{n-1})-\frac{C_1}{C_2}V_{in}(T_n)$

$$=>\frac{V_{out}(T_n)-V_{out}(T_{n-1})}{T}=-\frac{C_1}{TC_2}V_{in}(T_n)=-\frac{1}{R_1C_2}V_{in}(T_n)$$

$$=>\frac{d}{dt}V_{out}=-\frac{1}{R_1C_2}V_{in}=-\frac{1}{\frac{1}{C_1f}C_2}V_{in}=-\frac{1}{(C_2/C_1)(\frac{1}{f})}V_{in}$$

High-precision integrator time constant $RC=\frac{C_2}{C_1}\frac{1}{f}$

Z-domain Expression:

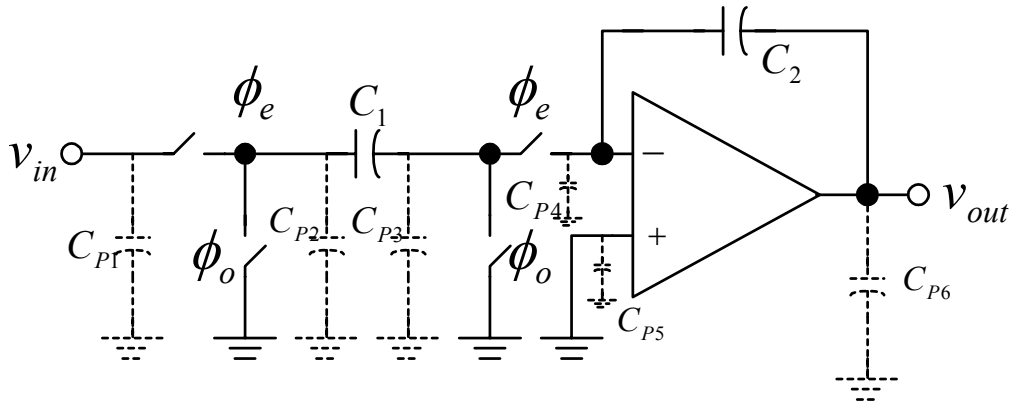
$$V_{out}(z)=V_{out}(z)Z^{-1}-\frac{C_1}{C_2}V_{in}(z)$$

$$=>H(z)\equiv\frac{V_{out}(z)}{V_{in}(z)}=-\frac{(C_1/C_2)}{(1-Z^{-1})}$$

Backward Euler Transformation: $S\rightarrow\frac{1-Z^{-1}}{T}$

$$H(S)=-\frac{1}{(C_2/C_1)TS}=-\frac{1}{R_1C_2S}$$

Parasitic-Free structure:



§14-4.2 Non-inverting SC Integrator

$\phi_e(\phi_o)$: $V_{c1}=+V_1$

$\phi_o(\phi_e)$: $V_{c1}=-V_2$

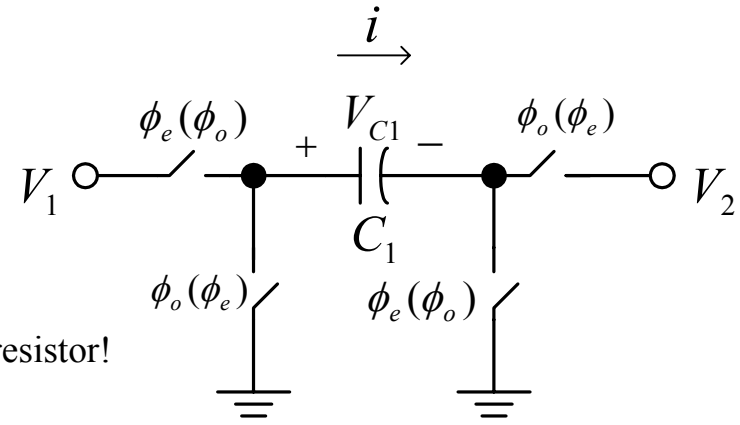
$\Delta Q=C_1(-V_1-V_2)$

$$\frac{\Delta Q}{T}=i=-C_1\frac{V_1+V_2}{T}$$

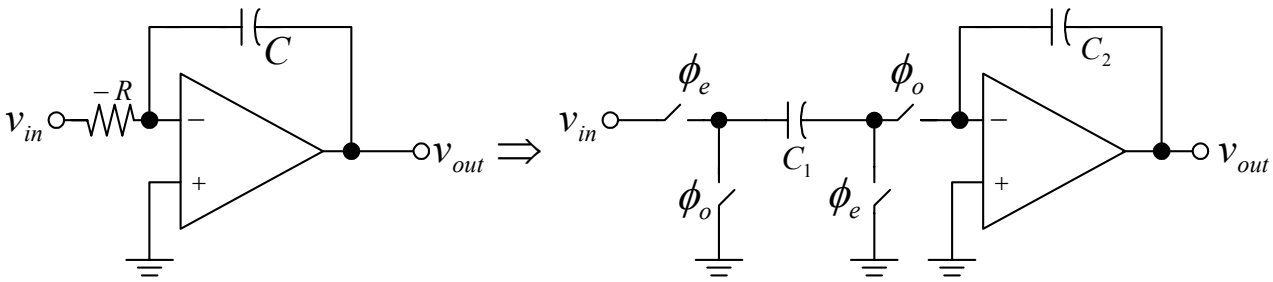
If $V_2=0$ $=>i=\frac{-C_1V_1}{T}=\frac{+V_1}{R}$

$=>$ $R=-\frac{T}{C_1}=-\frac{1}{C_1 f}$

$=>$ SC simulated negative resistor!

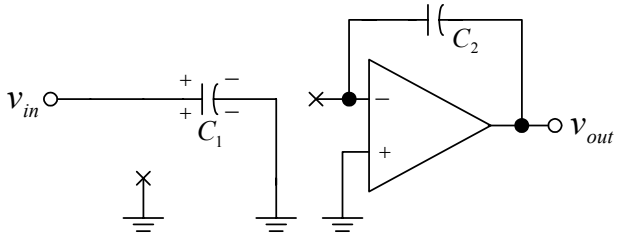


The non-inverting SC integrator:

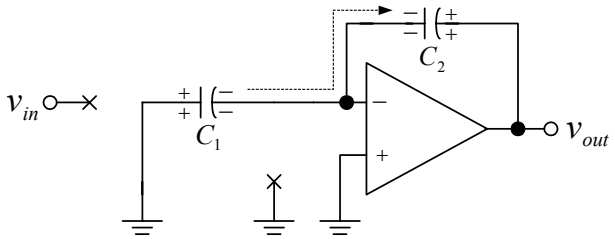


Operations:

(1)ϕ_e phase



(2) ϕ_o phase



$$V_{out}(T_n)=V_{out}(T_{n-1})+\frac{C_1}{C_2}V_{in}(T_{n-1})$$

$$=>\frac{d}{dt}V_{out}=\frac{1}{R_1C_2}V_{in}$$

$$=>\frac{V_{out}}{V_{in}}(s)\equiv H(s)=\frac{1}{R_1C_2S}=\frac{1}{\frac{C_2}{C_1}\frac{1}{f}S}$$

Z-domain expression:

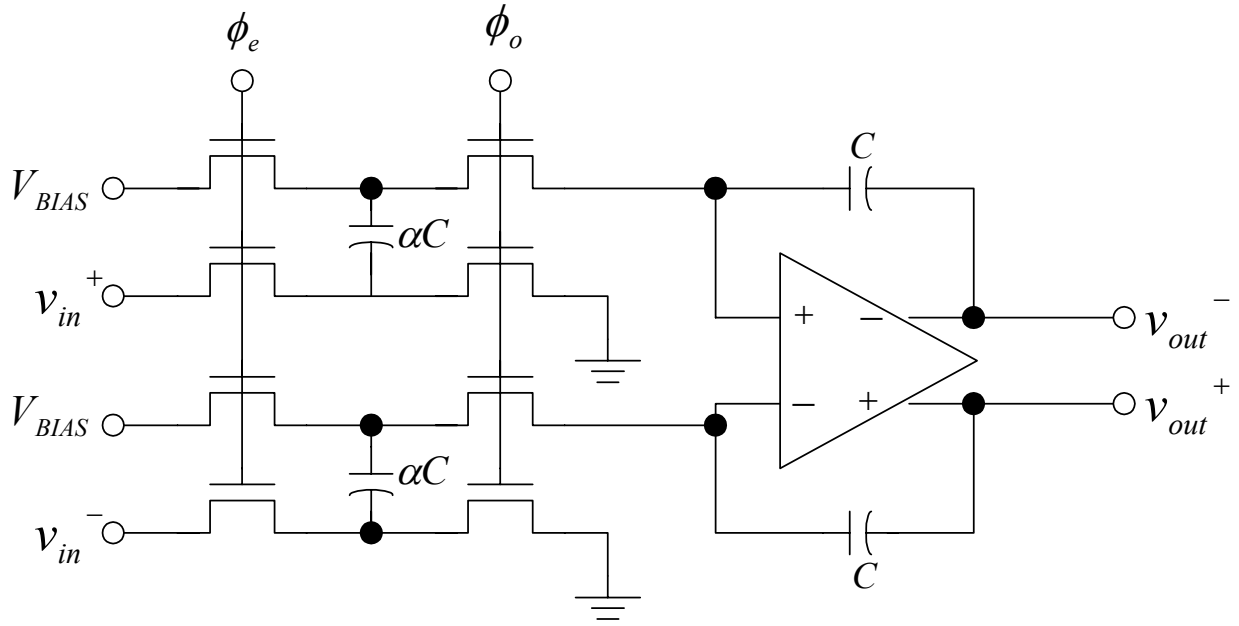
$$\mathrm{H(z)} \equiv \frac{V_{out}(z)}{V_{in}(z)} = \frac{Z^{-1}(\frac{C_1}{C_2})}{1 - Z^{-1}}$$

Forward Euler Transformation: $\mathrm{S} \rightarrow \frac{1 - Z^{-1}}{TZ^{-1}}$

$$\mathrm{H(s)} \equiv + \frac{1}{(\frac{C_2}{C_1})TS} = + \frac{1}{R_1 C_2 S}$$

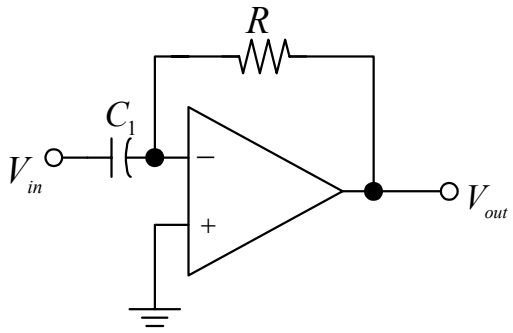
- Simpler non-inverting integrator!

§14-5 Fully Differential-Type SC Integrators Using OP AMPs.

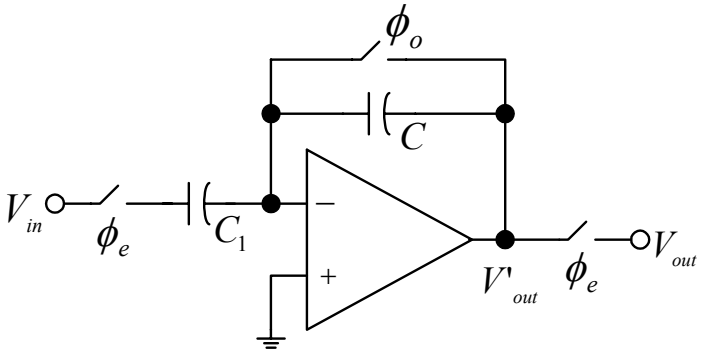


* Better noise rejection
* Better CMRR and PSRR
* Better Frequency response
* Better slew rate
** More components (switches, capacitor, OP AMPs)
** Thermal noise ↑ due to the added components and switching operations.
** Need common-mode feedback or common-mode bias circuit

§14-6 SC Differentiators Using OP AMPs



Inverting:



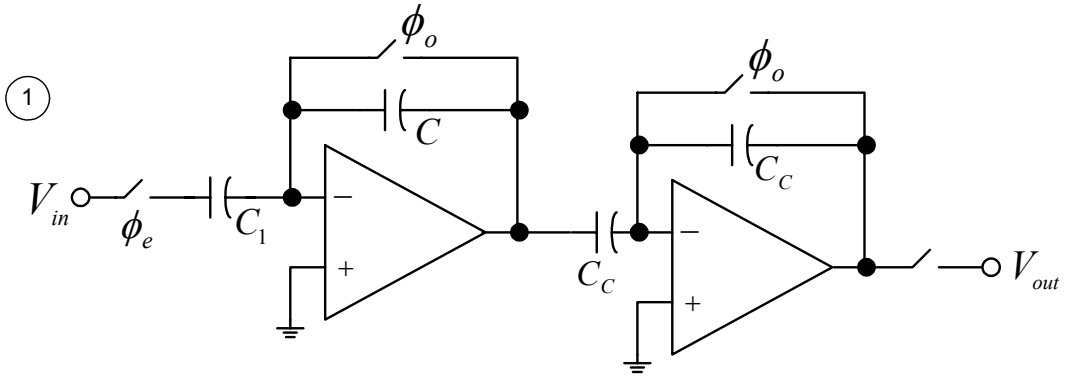
$$V_{out}(T_n)=V'_{out}(T_n)=-\frac{C_1}{C}[V_{in}(T_n)-V_{in}(T_{n-1})]$$

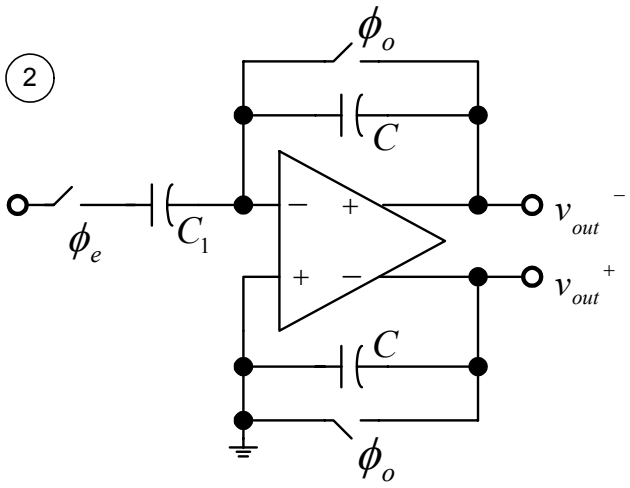
$$=>H(z)=-\frac{C_1}{C}(1-Z^{-1})$$

Backward-Euler Transformation: $S\rightarrow\frac{1-Z^{-1}}{T}$

$$H(S)=-S\frac{C_1}{C}T=-S\frac{C_1}{C}\frac{1}{f}=-SRC_1 \qquad R=\frac{1}{cf}$$

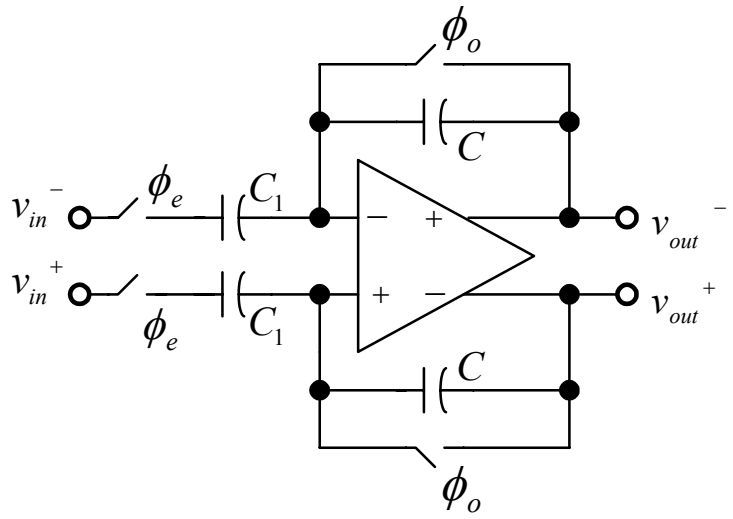
Noninverting:





$$H(z)=+\frac{C_1}{C}(1-Z^{-1})$$

Differential-Type SC Differentiator:



Characteristics of SC differentiators:

1. Parasitic-free structure.
2. No dc instability problem as in SC integrators.
3. No high-frequency-noise problem as in continuous-time differentiators.
4. Can be used to design filters as SC integrators.

Ref: IEEE JSSC vol.sc-24, pp.177-180, 1989.

§14-7 The Design of SC Biquads (Second-Order Filter)

$$H(S)=\frac{-(K_2S^2+K_1S+K_\circ)}{S^2+\frac{\omega_\circ}{Q}S+\omega_0^2}=\frac{V_{out}(s)}{V_{in}(s)}$$

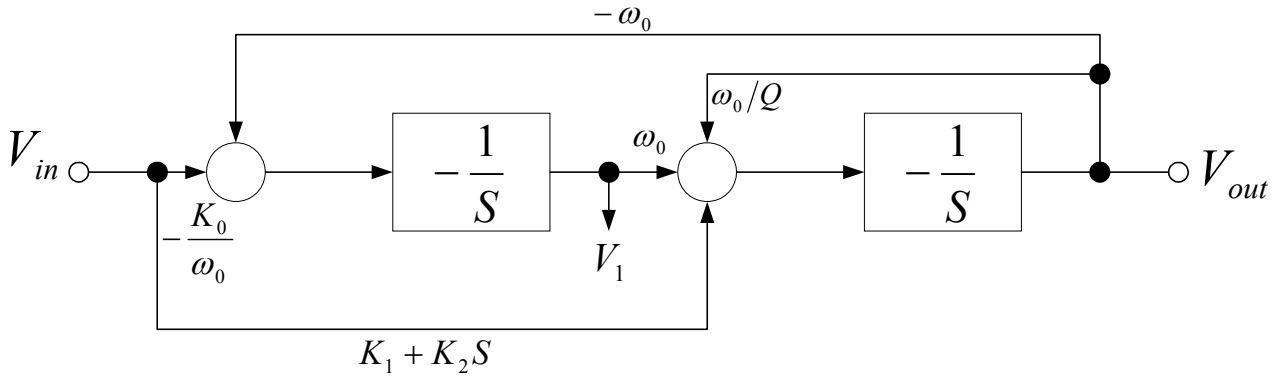
§14-7.1 Low-Q SC Biquads

Step 1: Flow diagram generation.

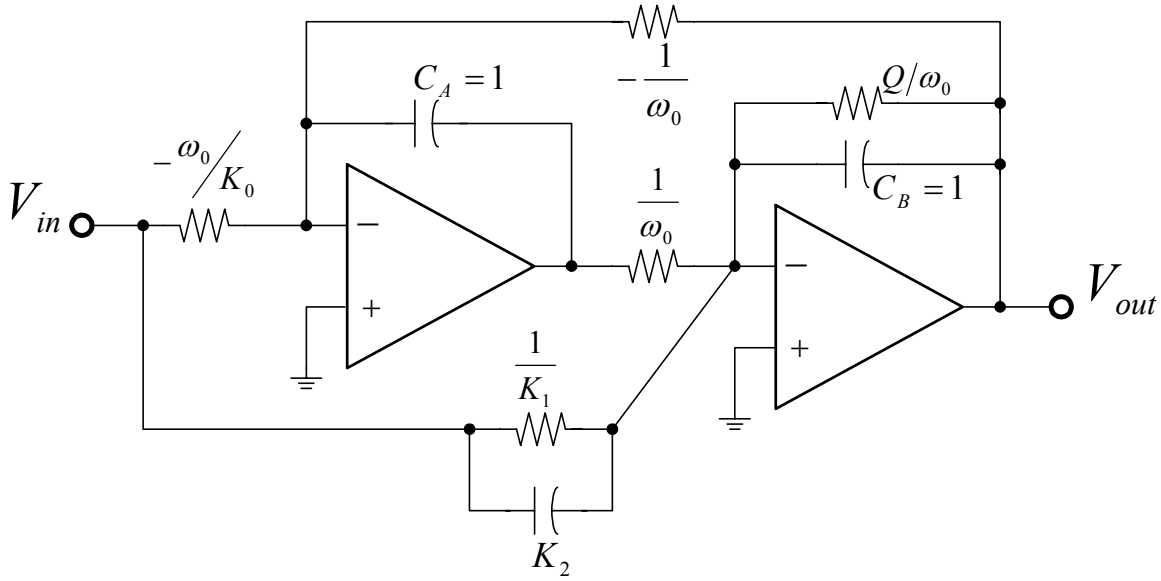
$$S^2V_{out}=-[K_2S^2+K_1S+K_o]\,V_{in}-(\omega_o\frac{S}{Q}+\omega_0^2)\bullet V_{out}$$

$$=>V_{out}=-\frac{1}{S}[(K_1+K_2S)V_{in}+(\frac{W_\circ}{Q})\bullet V_{out}+\omega_o\bullet V_1)$$

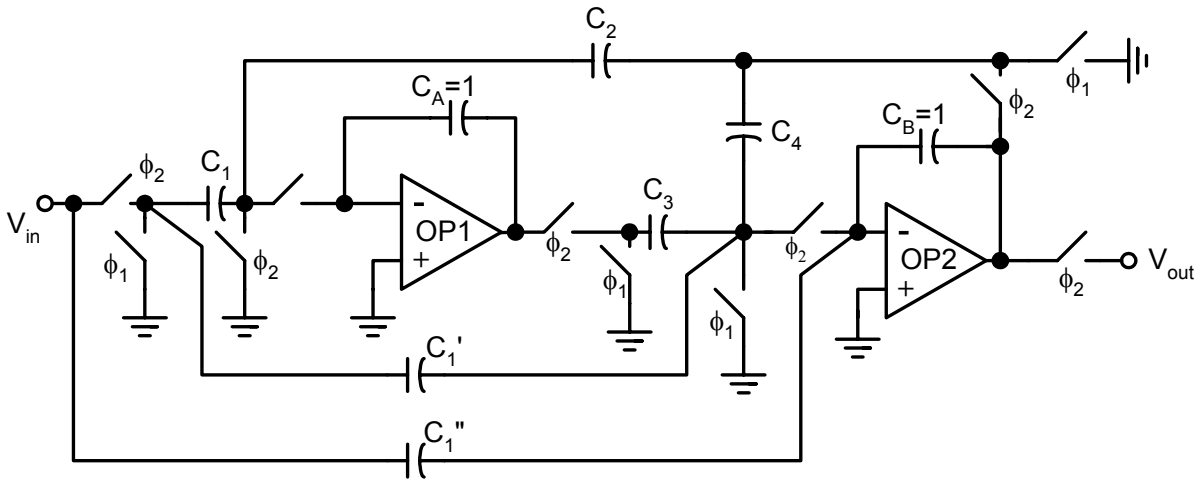
$$\text{where } V_1=\frac{1}{S}[(K_o/\omega_o)\bullet V_{in}+\omega_o\bullet V_{out}]$$



Step2: Active-RC design



Step 3: SCF



$C_1 = T * K_o/\omega_o = |A_{dc}| * \omega_o * T = |A_{dc}| \frac{1}{x}$ $\quad |A_{dc}| \cong \frac{K_o}{\omega_o^2}$

$C_2 = C_3 = \omega_o * T = \frac{1}{x}$

$C_4 = (\omega_o * T/Q) = \frac{1}{Qx} \Rightarrow \frac{Q}{\omega_o T} = \frac{C_A}{C_4}$ (not suitable for high Q)

$C_1' = K_1 * T = K_1 \frac{1}{\omega_o x}$

$C_1'' = K_2$

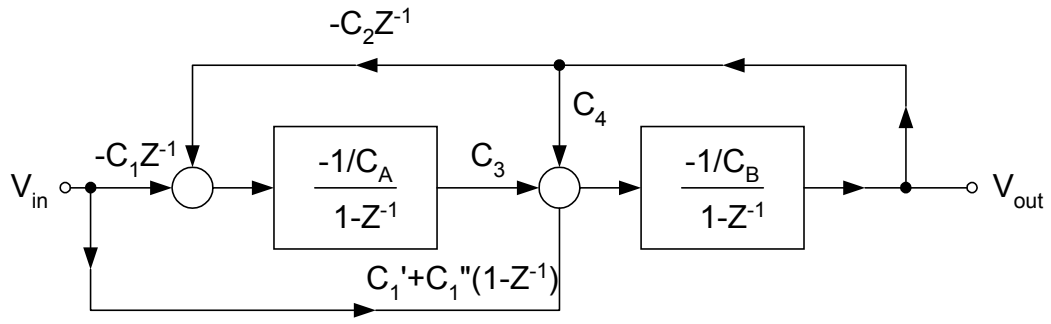
$C_A/C_2 = \frac{1}{\omega_o T}$

$X = \frac{1}{\omega_o T}$

$\Rightarrow \quad f_o = \frac{fs}{2\pi x}$ f_o: center (cutoff) frequency

Step 4: refinement

Z-domain block diagram (If the accuracy is not good, change to Z-domain diagram)



$C_1'' = a_0$

$C_1' = a_2 - a_0$

$C_1 = 1/C_3 * (a_0 + a_1 + a_2) = \frac{1}{C_3}(2C_1'' + C_1' \pm a_1)$

$C_4 = b_2 - 1$

$C_2 * C_3 = b_1 + b_2 + 1$

$C_2 = C_3$

In this diagram, each op-amp and its feedback capacitor (C_A or C_B) is replaced by its voltage-to-charge transfer function.

$$\frac{Q_{out}(z)}{V_{in}(z)} = \frac{-1/Cf}{1-z^{-1}} = \frac{V_{out}(z)\cdot C}{V_{in}(z)}$$

Here Cf is the feedback capacitor.

Similarly,

$C * (1-z^{-1})$ for an unswitched capacitor (e.g. C_1'')

C for a non-inverting capacitor (C_1', C_3, C_4)

$-C * z^{-1}$ for an inverting capacitor (C_1, C_2)

From the block diagram, the exact transfer function is

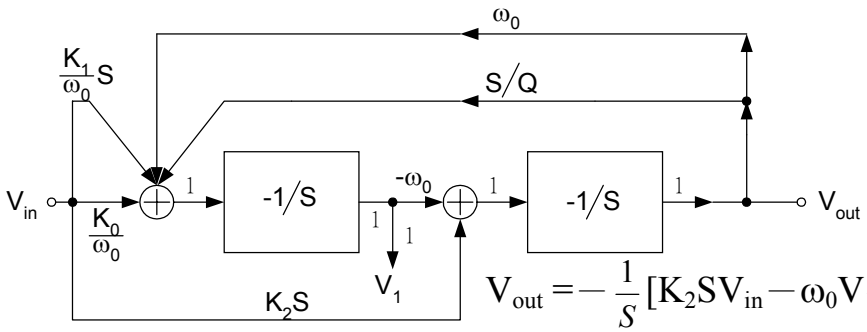
$$\frac{V_{out}(z)}{V_{in}(z)} = -\frac{(C_1'+C_1'')z^2 + (C_1C_3 - C_1' - 2C_1'')z + C_1''}{(1+C_4)z^2 + (C_2C_3 - C_4 - 2)z + 1}$$

As compared to H(z) specifications, the capacitances can be determined.

$$H(z) = -\frac{a_2 * z^2 + a_1 * z + a_0}{b_2 * z^2 + b_1 * z + 1}$$

TYPES	COEFFICIENTS
L-P CASE	$C_1'=C_1''=0$ $K_1=K_2=0 \quad a_0=a_2=0$
B-P CASE	$C_1=C_1''=0$ $K_0=K_2=0 \quad a_0=0, a_1=-a_2$
H-P CASE	$C_1=C_1'=0$ $K_0=K_1=0 \quad a_0=a_2=-\frac{a_1}{2}$
NOTCH CASE	$C_1'=0$ $K_1=0 \quad a_2=a_0$

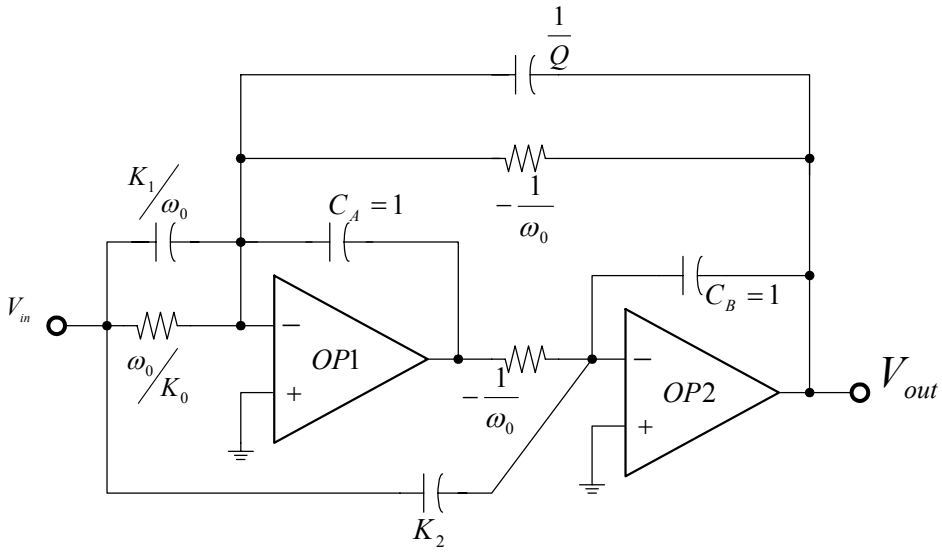
§14-7.2 High-Q SC Biquads



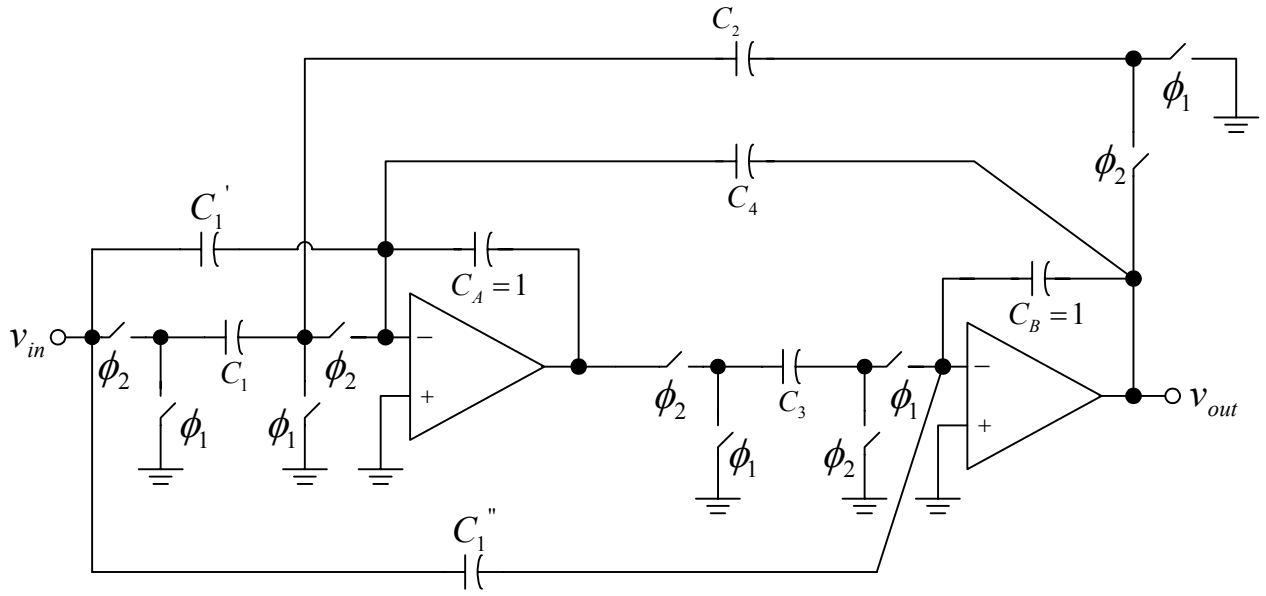
$$V_{out} = -\frac{1}{S}[K_2 S V_{in} - \omega_0 V_1]$$

Where $V_1 = -\frac{1}{S}[(\frac{K_0}{\omega_0} + \frac{K_1}{\omega_0} S)V_{in} + (\omega_0 + \frac{S}{Q})V_{out}]$

2. Active-RC design



3. SCF



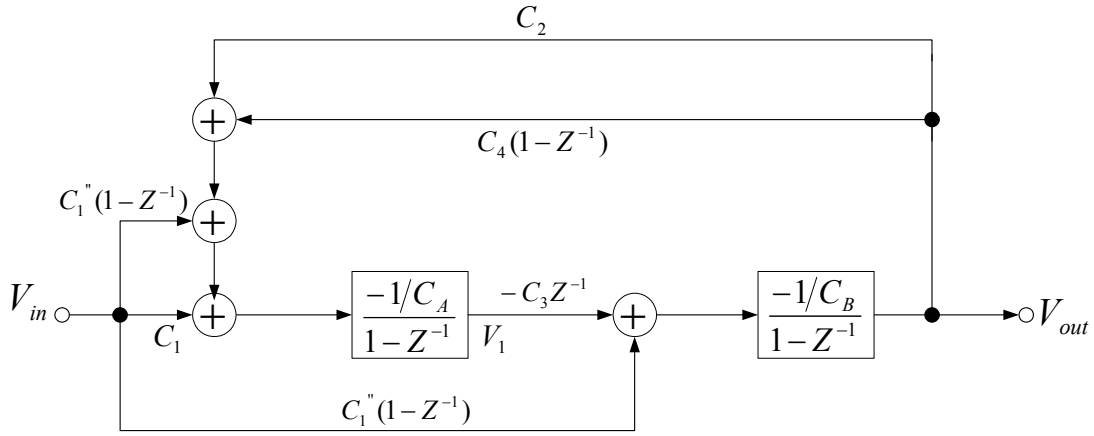
$C_1=K_0\ T/\omega_0 = (\frac{K_0}{\omega_0^2})\omega_o T = |A_{dc}|\omega_0 T$

$C_2 \cong C_3 \cong \omega_0 T$

$C_4 \cong \frac{1}{Q}$ (instead of $\frac{Q}{\omega_0 T}$)

$C_1' \cong K_1/\omega_0$
$C_1'' \cong K_2$

4. Z-domain block diagram of a high-Q biquad:



$$H(Z)=-\frac{C_1''Z^2+(C_1C_3+C_1'C_3-2C_1'')Z+(C_1''-C_1'C_3)}{Z^2+(C_2C_3+C_3C_4-2)Z+(1-C_3C_4)}$$

Choose $C_2=C_3$

Coefficient matching:

$C_1''=\frac{a_2}{b_2}$

$C_1'=(C_1''-\frac{a_\circ}{b_2})/C_3=\frac{a_2-a_\circ}{b_2c_3}$

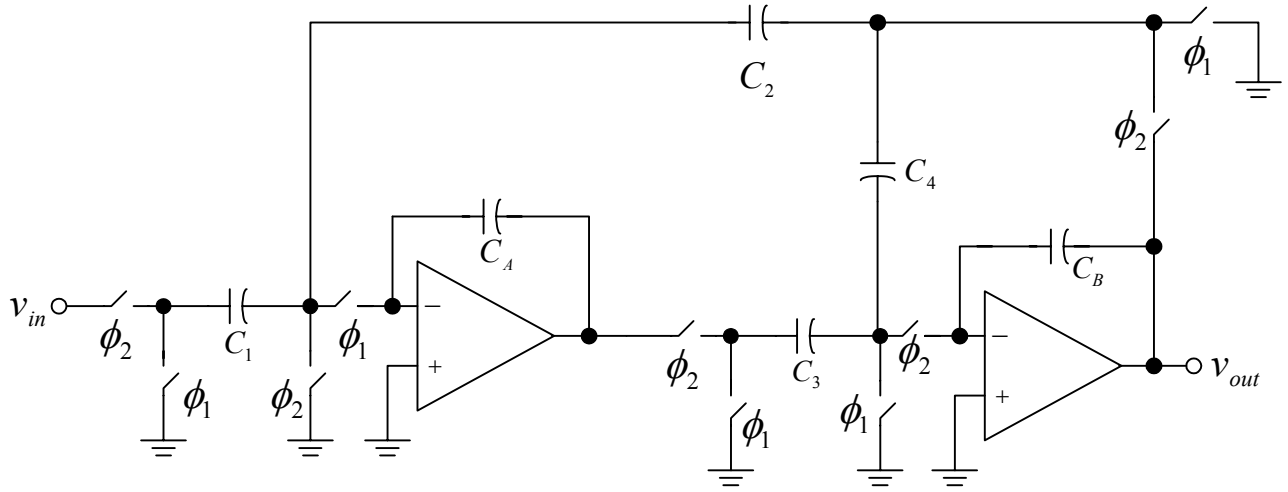
$C_1=(a_1/b_1-C_1'C_3+2C_1'')/C_3=(a_0+a_1+a_2)/(b_2c_3)$

$C_4=(1-\frac{1}{b_2})/C_3$

$C_3^2=C_2^2=(b_1/b_2-C_3C_4+2)=(b_1+b_2+1)/b_2$

§14-7.3 Design Examples

Example 1: Low-Q Lowpass SCF Biquad

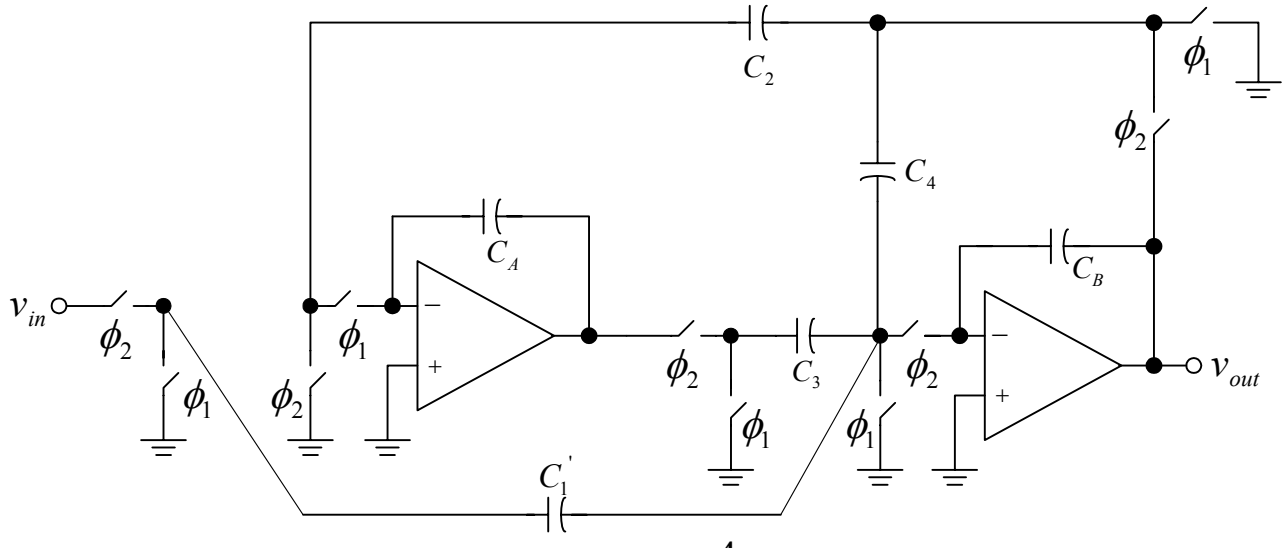


C_A=C_B=6.3 C_1=4 $$H(S)=\frac{4}{S^2+1.2S+1}$$

C_2=1 C_3=1 C_4=1.2 $$f_c=\frac{f_s}{2\bullet\pi\bullet C_A}$$

f_c: CENTER FRE.
f_s: SAMPLING FRE.

Example 2: Low-Q Bandpass SCF Biquad

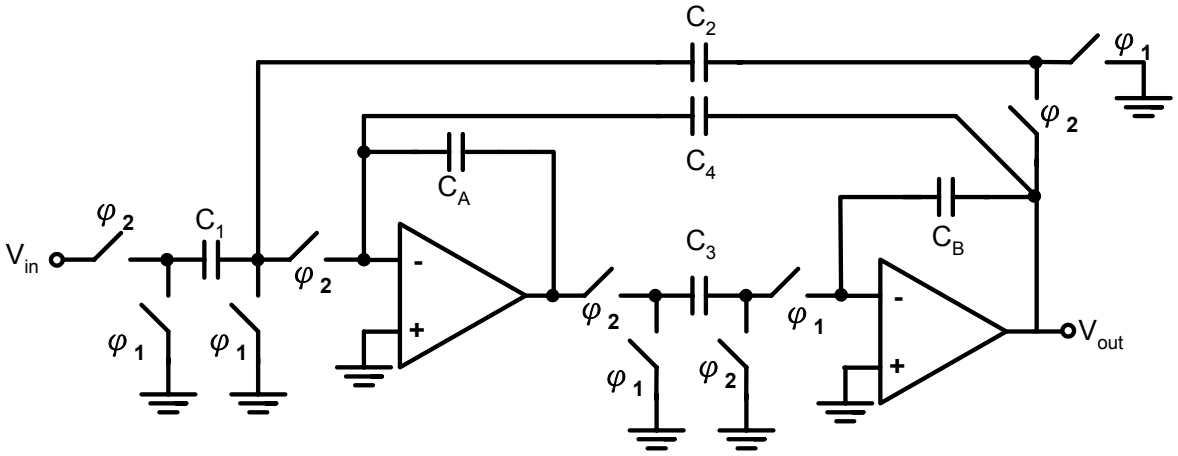


C_A=C_B=6.3 C_1'=2 $$H(S)=\frac{4}{S^2+1.2S+1}$$

C_2=1 C_3=1 C_4=1.2 $$f_c=\frac{f_s}{2\bullet\pi\bullet C_A}$$

f_c: CENTER FRE.
f_s: SAMPLING FRE.

Example 3: High-Q Low-pass SCF Biquad



C_A=C_B=6.3 C_1=4

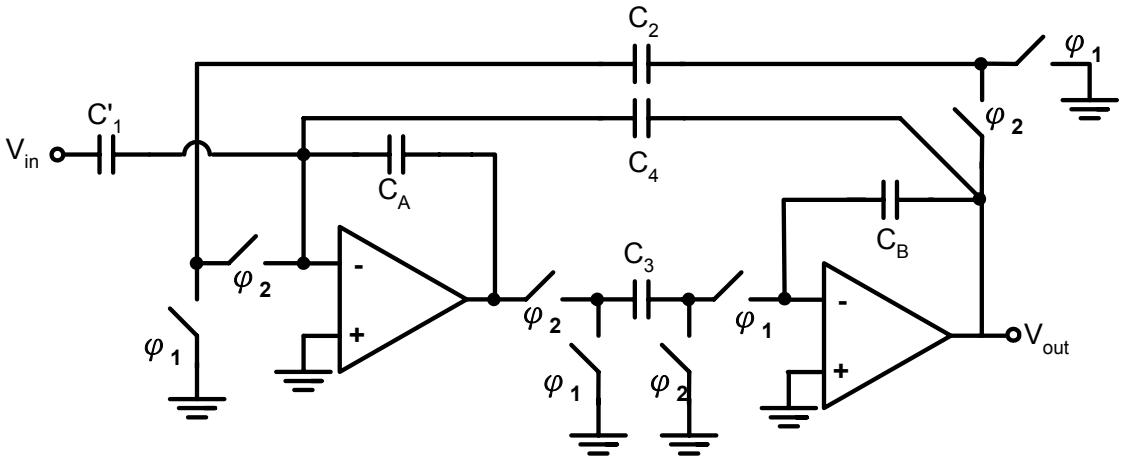
$$H(S)=\frac{4}{S^2+\frac{S}{5.25}+1}$$

C_2=1 C_3=1 C_4=1.2

$$f_c=\frac{f_s}{2\bullet\pi\bullet C_A}$$

f_c: CENTER FRE.
f_s: SAMPLING FRE.

Example 4: High-Q Band-pass SCF Biquad



C_A=C_B=6.3 C'_1=2

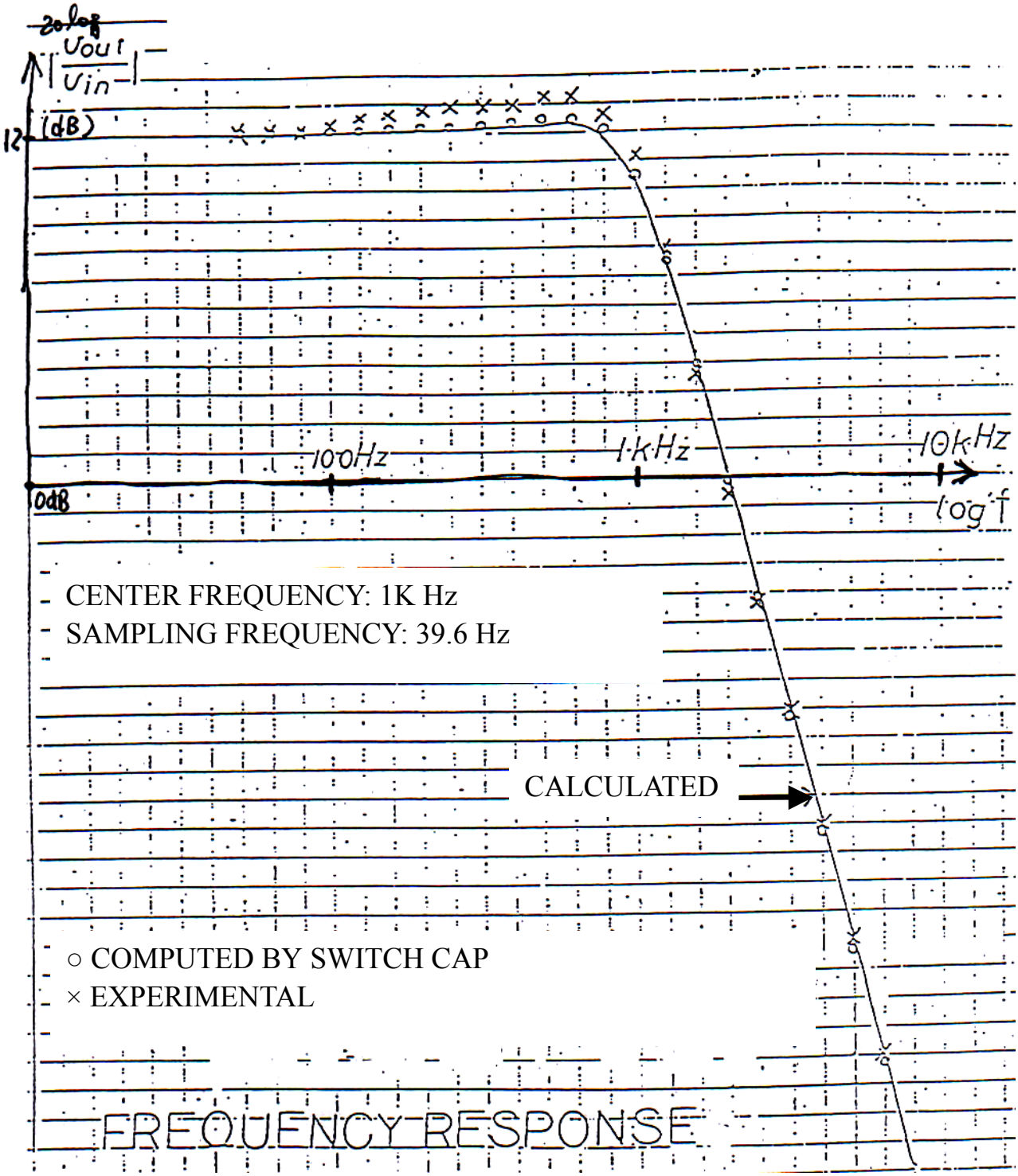
$$H(S)=\frac{2S}{S^2+1.2S+1}$$

C_2=1 C_3=1 C_4=1.2

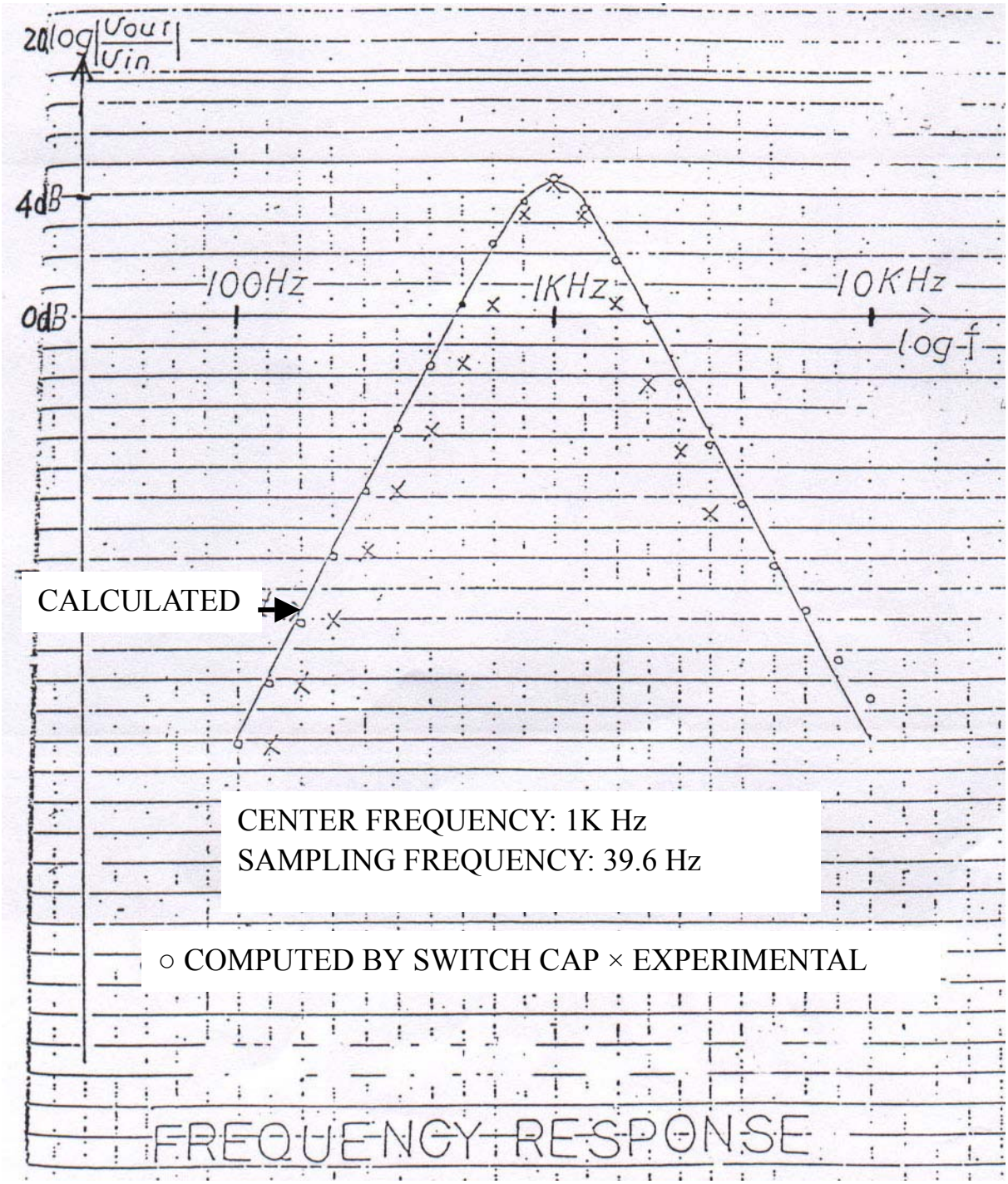
$$f_c=\frac{f_s}{2\bullet\pi\bullet C_A}$$

f_c: CENTER FRE.
f_s: SAMPLING FRE.

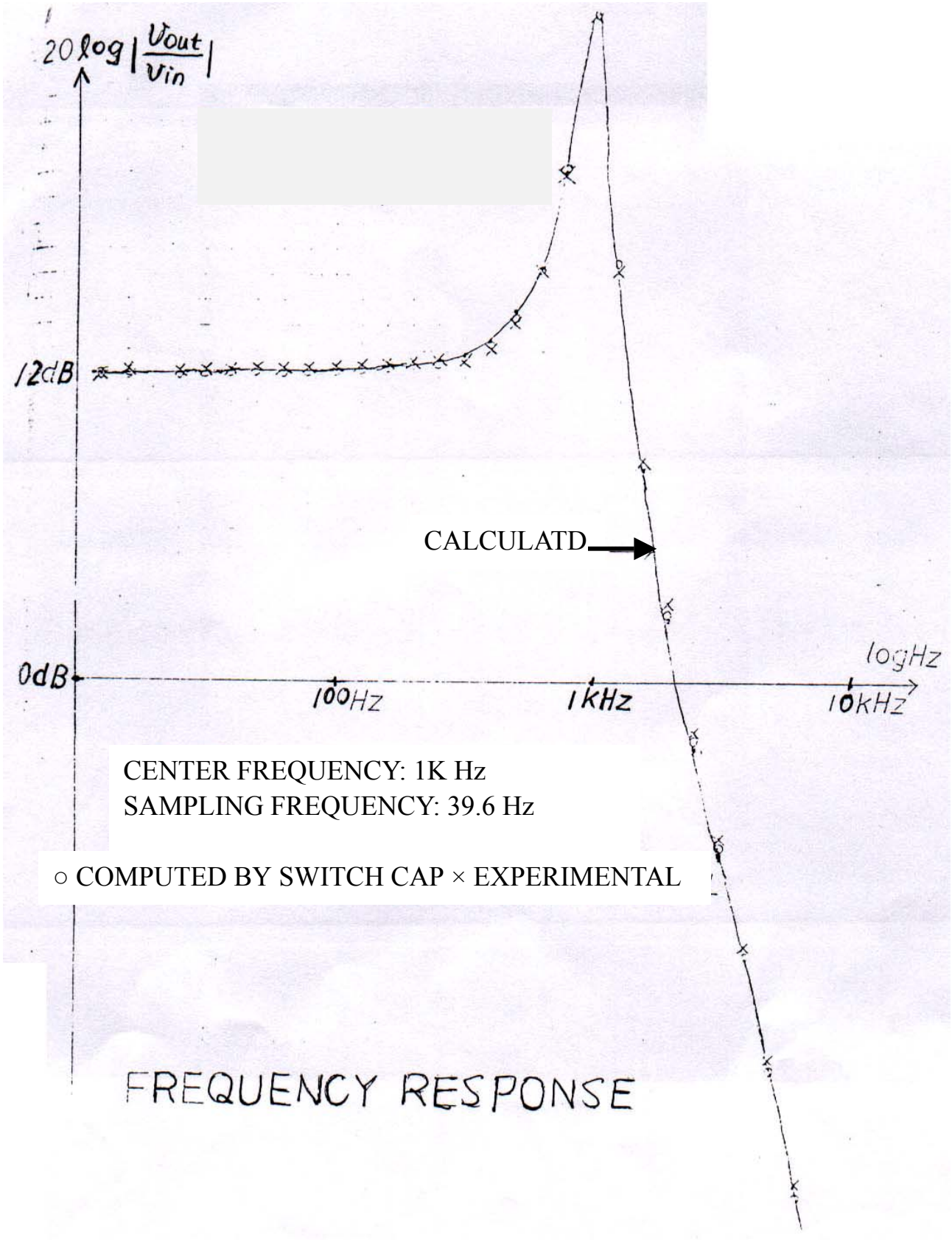
Frequency response of low-Q Low-pass SCF biquad



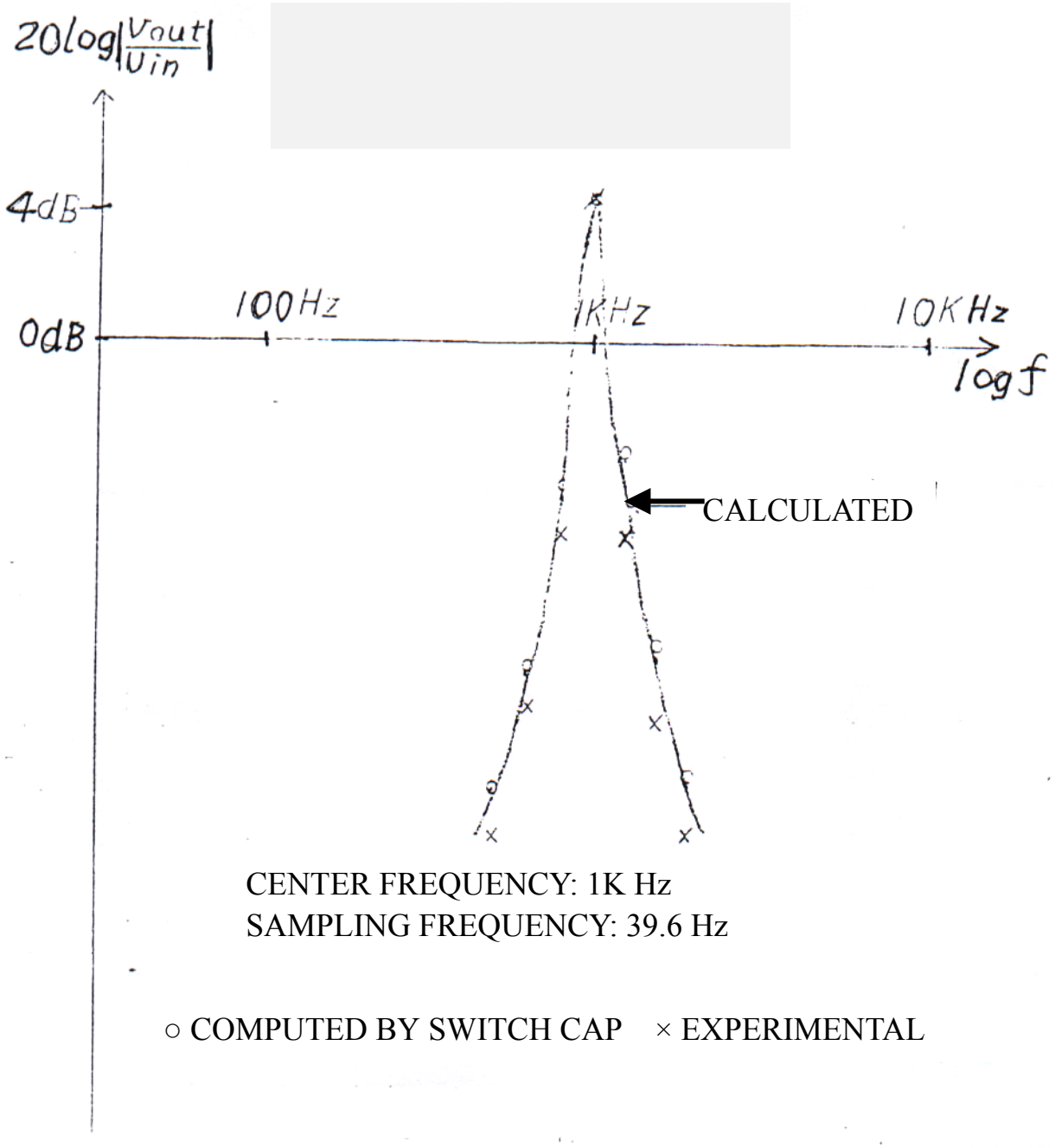
Frequency response of low-Q Band-pass SCF biquad



Frequency response of High-Q Low-pass SCF biquad



Frequency response of high-Q Band-pass SCF biquad



CENTER FREQUENCY: 1K Hz
SAMPLING FREQUENCY: 39.6 Hz

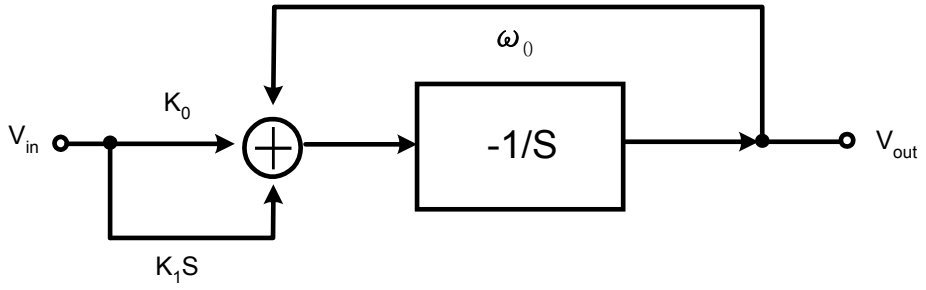
○ COMPUTED BY SWITCH CAP × EXPERIMENTAL

FREQUENCY RESPONSE

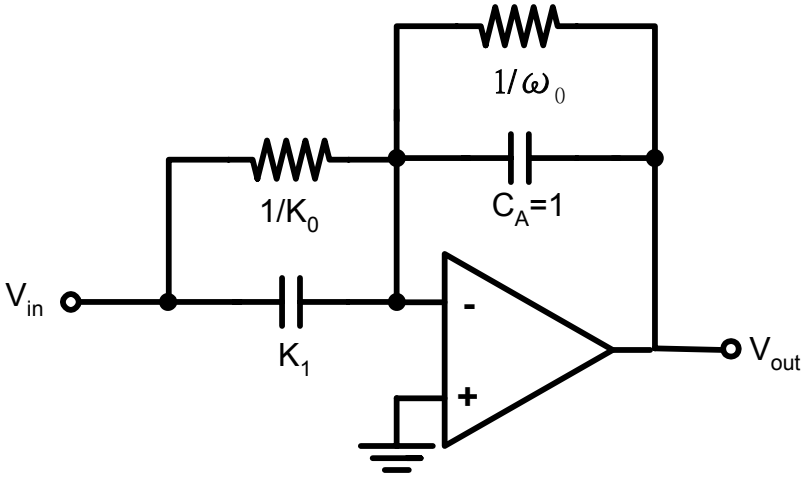
§14-8 First-Order SCFs

$H_a(s) = -\dfrac{K_1 S + K_0}{S + \omega_0}$ $\qquad$ $H(z) = -\dfrac{a_1 z + a_o}{b_1 z + 1}$

1. Flow diagram

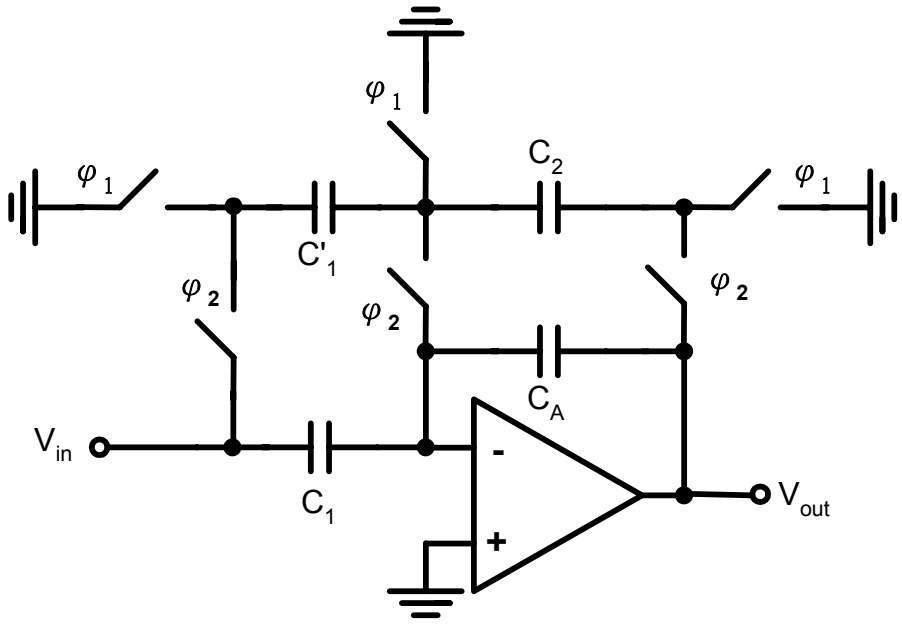


2. Active-RC design



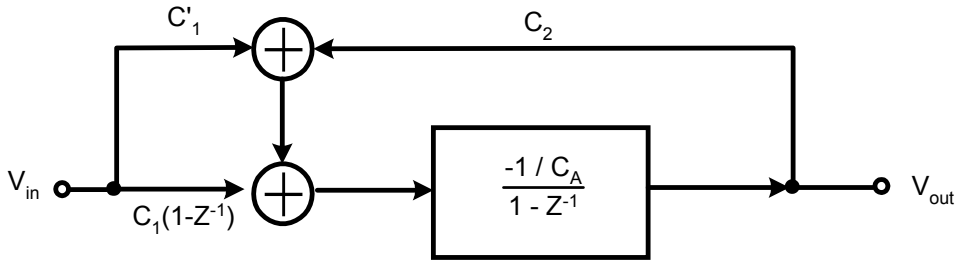
3. SCF

$C_1 \cong K_1$
$C_1' \cong TK_0$
$C_2 \cong \omega_0 T$
$f_c = \dfrac{f_s}{2\pi x}$



4. Z-domain block diagram

$$H(z)=\frac{V_{out}}{V_{in}}=-\frac{(C_1+C_1')z-C_1}{(1+C_2)z-1}$$



§14-9 Switched-Capacitor Ladder Filters

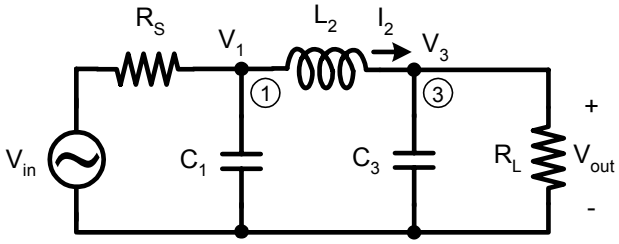
§14-9.1 Approximate Design of SC Ladder Filters

(1) Third-order low-pass filter without finite transmission zeros

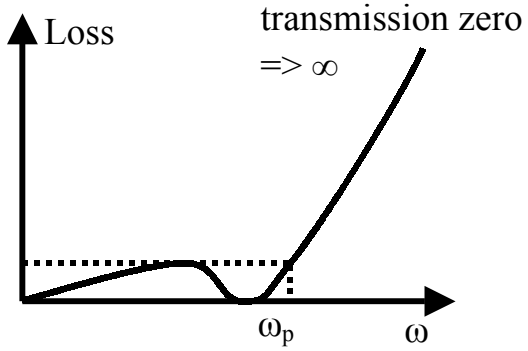
$$-V_1=-\frac{1}{SC_1}\left(\frac{V_{in}-V_1}{R_S}-I_2\right)$$

$$-I_2=\frac{-1}{SL_2}(V_1-V_3)$$

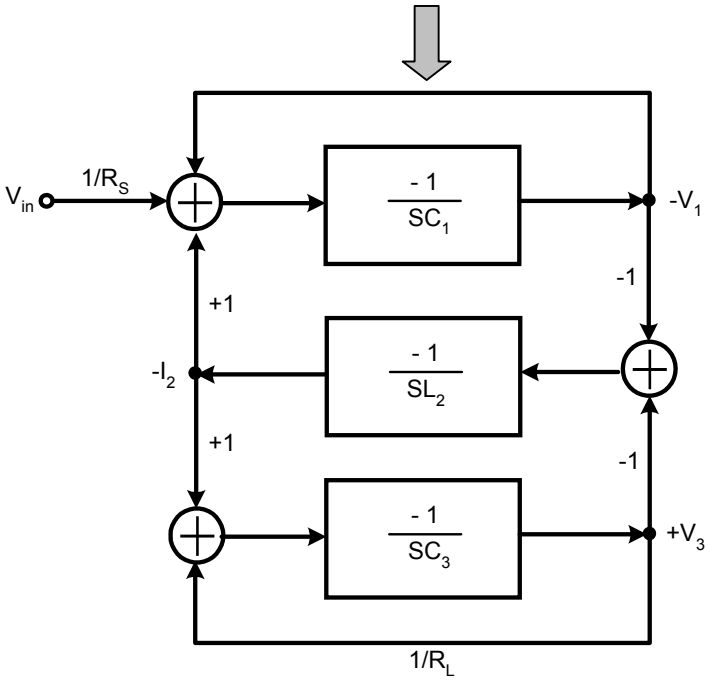
$$V_3=-\frac{1}{SC_3}\left(-I_2+\frac{V_3}{R_L}\right)$$



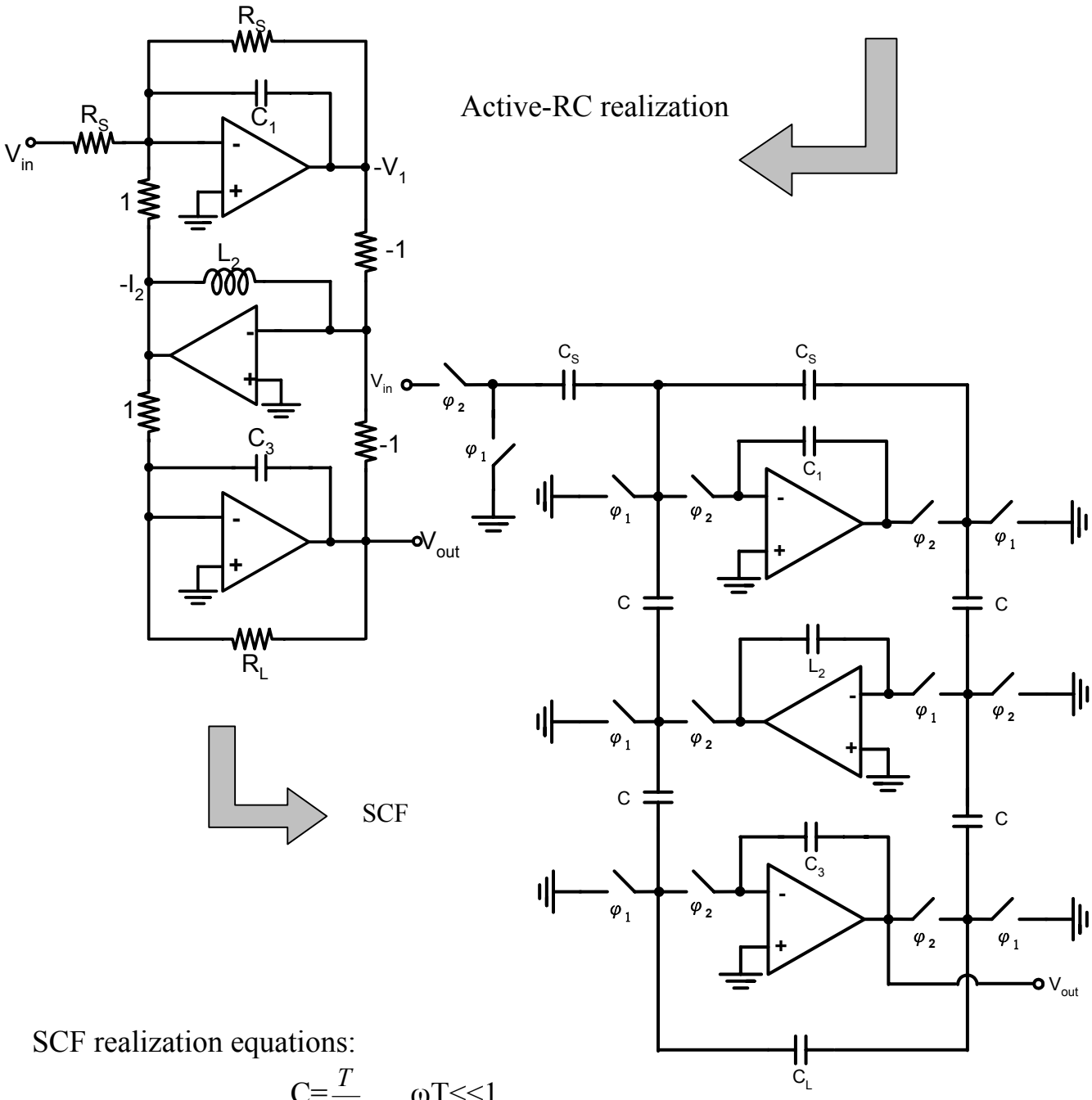
LCR prototype circuit



Loss response



Flow diagram



SCF realization equations:

$$C=\frac{T}{|R|} \qquad \omega T<<1$$

$$=> C_s \cong \frac{T}{Rs}$$

$$C \cong T$$

$$C_L \cong T / R_L$$

Due to the approximation made in finding C values, error still exists which may be refined by the z-domain analysis.

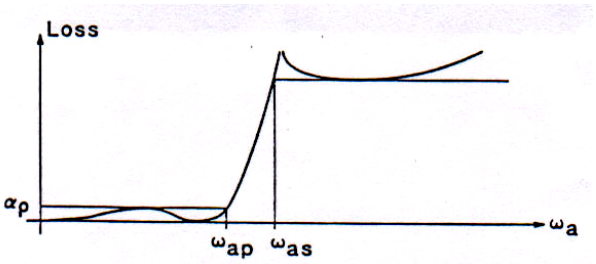
(2) Third-order low-pass filter with transmission zeros

$$\omega_{a1}=-\omega_{a2}=\sqrt{\frac{1}{L_2C_2}}$$

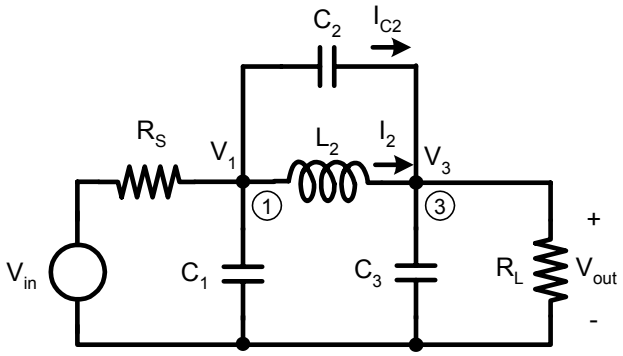
$$-V_1=\frac{-1}{s(C_1+C_2)}\left[\frac{V_{in}-V_1}{R_s}+sC_2V_3-I_2\right],$$

$$-I_2=\frac{-1}{sL_2}[V_1-V_3],$$

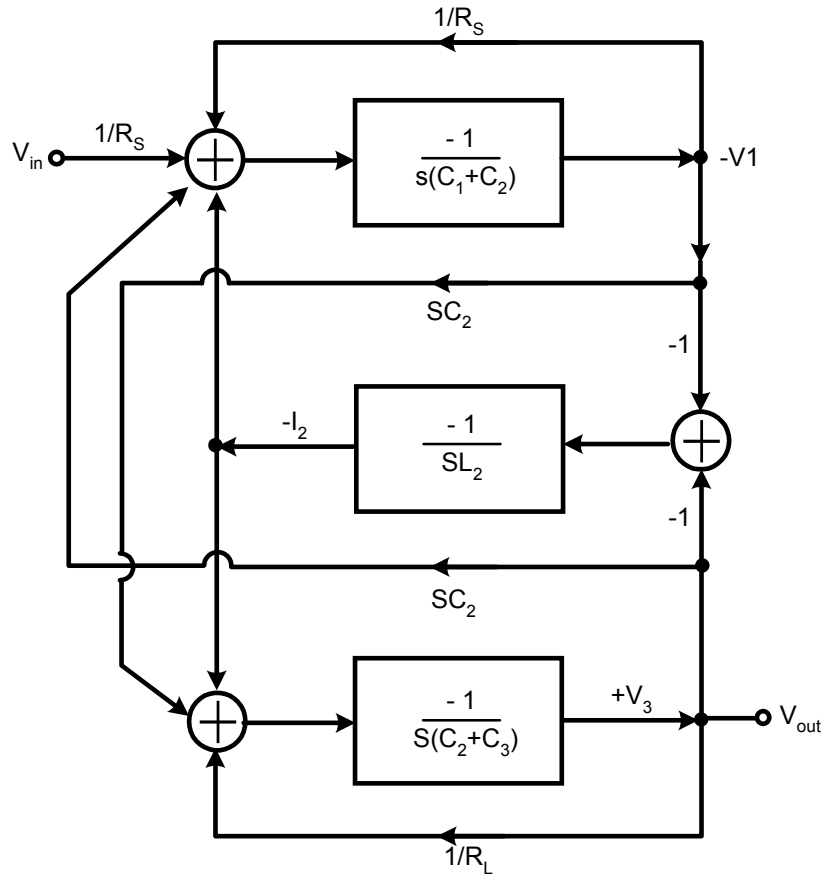
$$+V_3=\frac{-1}{s(C_2+C_3)}\left[-sC_2V_1-I_2+\frac{V_3}{R_L}\right]$$



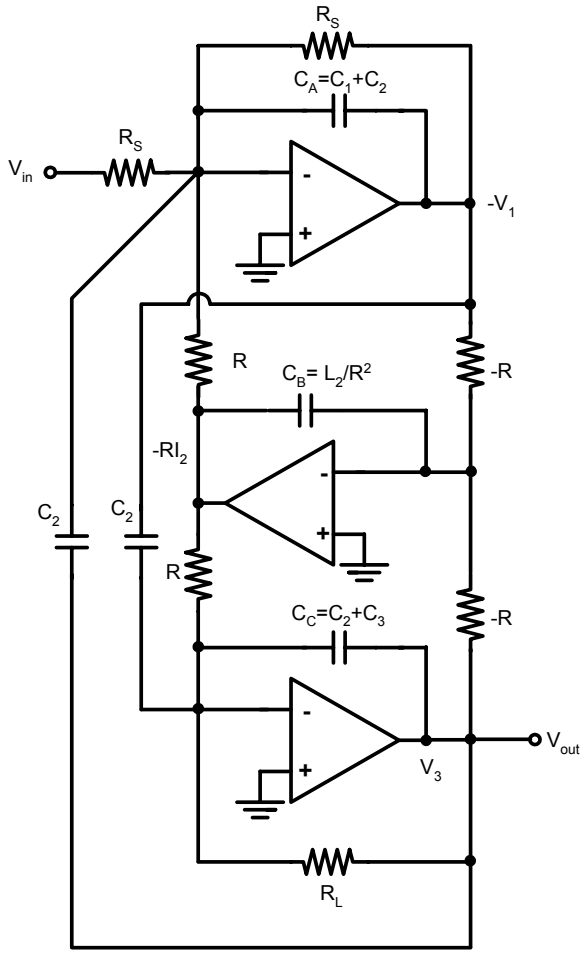
LCR Prototype circuit:



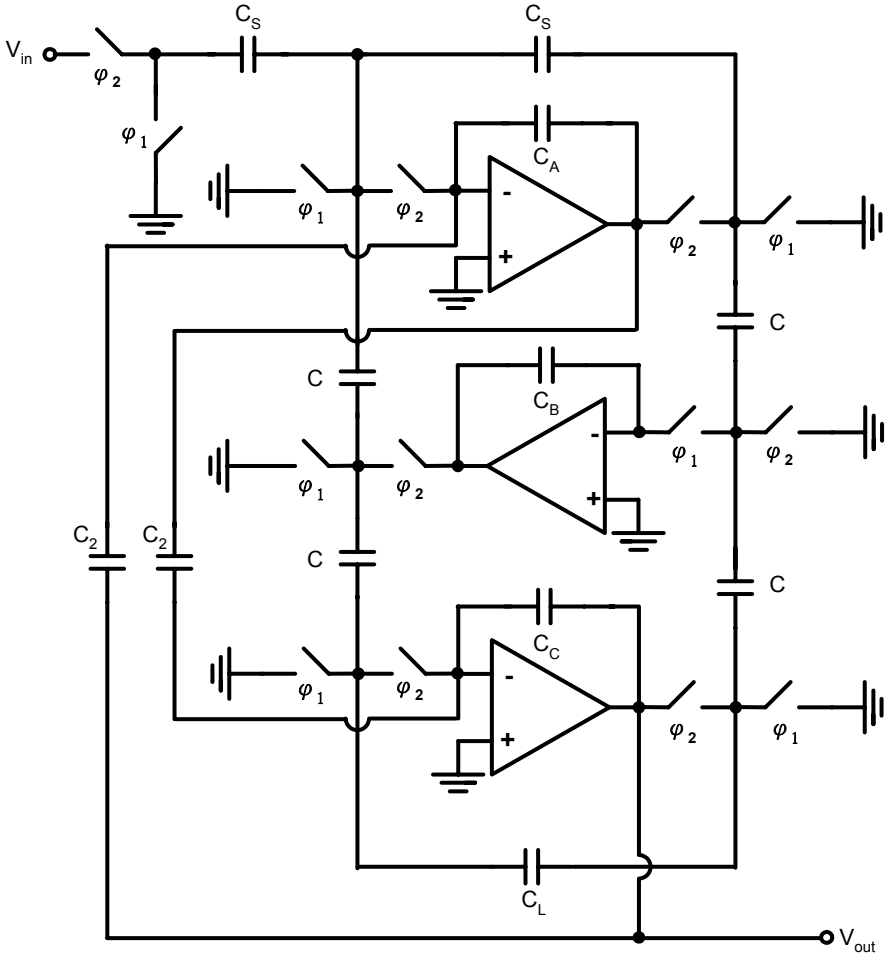
Flow diagram:



Active-RC Realization:



SCF:



$C_S \cong T / Rs$,

$C_A=C_1+C_2$,

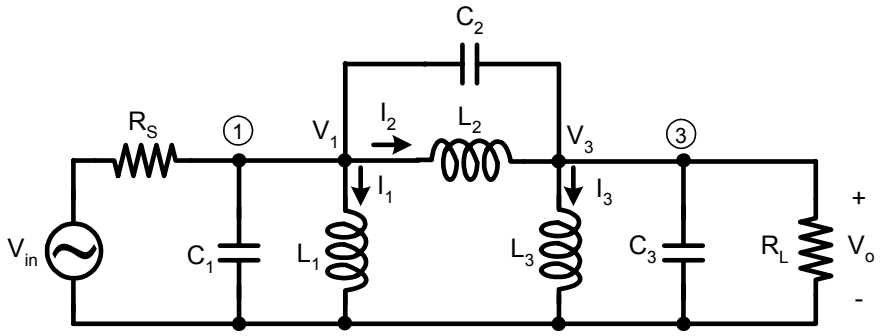
$C \cong T$,

$C_B=L_2$,

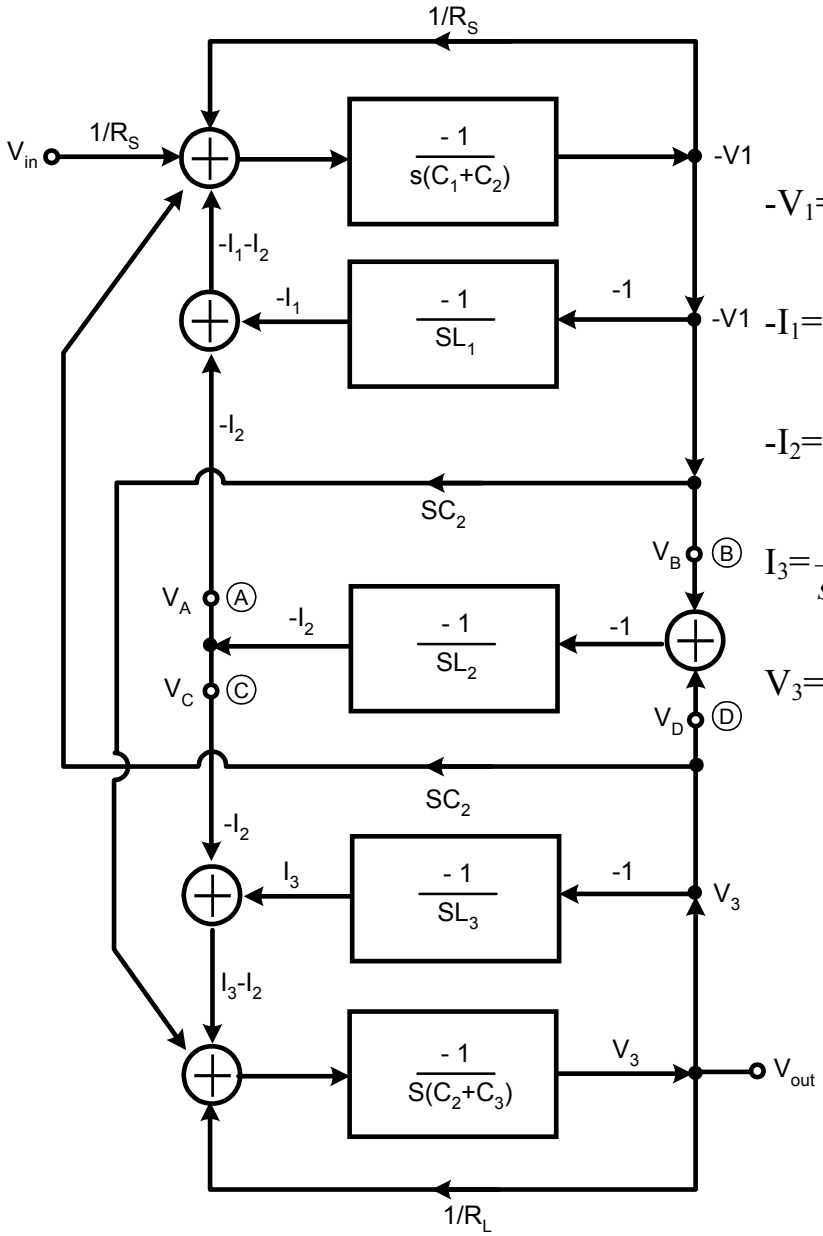
$Cc=C_2+C_3$,

$C_L \cong T / R_L$.

(3) Fourth-order Bandpass filter



LCR Prototype Circuit



$$-V_1=\frac{-1}{s(C_1+C_2)}\left[\frac{V_{in}-V_1}{R_S}+sC_2V_3-I_1-I_2\right],$$

$$-I_1=\frac{-V_1}{sL_1},$$

$$-I_2=\frac{-V_1+V_3}{sL_2},$$

$$I_3=\frac{V_3}{sL_3},$$

$$V_3=\frac{-1}{s(C_2+C_3)}\left[-sC_2V_1+I_3-I_2+\frac{V_3}{R_L}\right]$$

** The circuit has a stability problem at dc.
Due to inductor loops!

$$H_{AB} \equiv \left.\frac{V_B}{V_A}\right|_{\text{Circuits below Ⓐ and Ⓑ disconnected}} = \frac{-sL_1}{S^2 L_1(C_1+C_2)+SL_1/Rs+1}$$

$$H_{CD} \equiv \left.\frac{V_C}{V_D}\right|_{\text{Circuits below Ⓒ and Ⓓ disconnected}} = \frac{-sL_3}{S^2 L_3(C_2+C_3)+SL_3/R_L+1}$$

When $S\rightarrow 0$, $H_{AB}\rightarrow 0$, $H_{CD}\rightarrow 0$

=> There will be no dc feedback paths around the

center integrator which provides $-I_2$.

=> OP AMP will be in the open-circuit status with $A\rightarrow\infty$.

=> Saturation occurs

How to solve this problem?

Don't model the inductor loop currents separately.

i.e. I_1, I_2, I_3.

Only two inductive currents $I_{①}$ and $I_{③}$ entering nodes ① and ③ are modeled.

=> $V_{in}=0$ and $S\rightarrow 0$, $I_{①}=0$ and $I_{②}=0$

=>No any instability at dc.

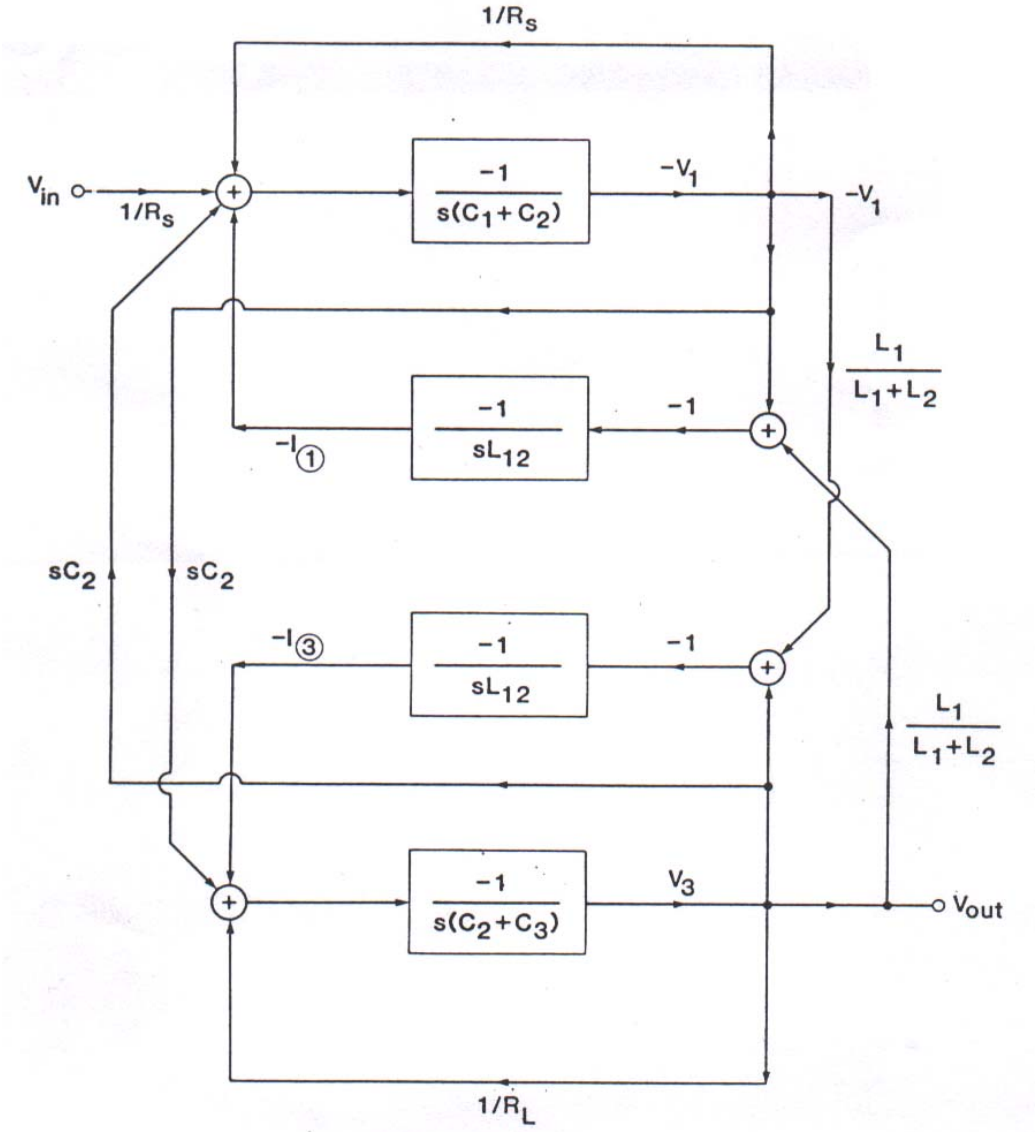
i.e.

Treat only two inductors as independent inductors.

$I_{①}=I_1+I_2$

$I_{③}=I_2-I_3$

New flow diagram:



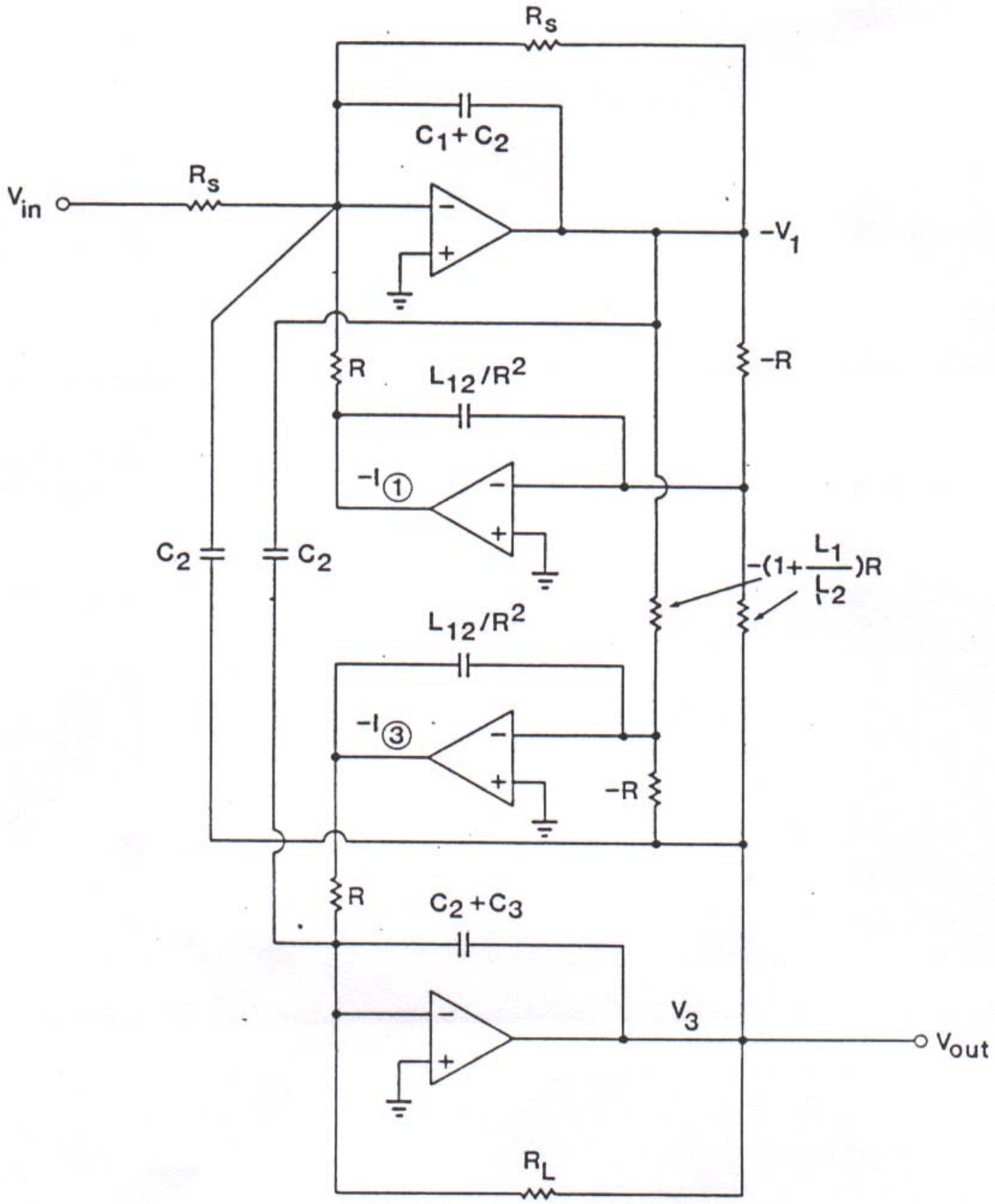
$$-V_1=\frac{-1}{s(C_1+C_2)}\left[\frac{V_{in}-V_1}{R_s}+sC_2V_3-I_{①}\right],$$

$$-I_{\bigcirc\!\!\!\!\!\!\Delta\!\!\!\!\!=}-(I_1+I_2)=\frac{-1}{sL_{12}}\left[V_1-\frac{L_1V_3}{L_1+L_2}\right],$$

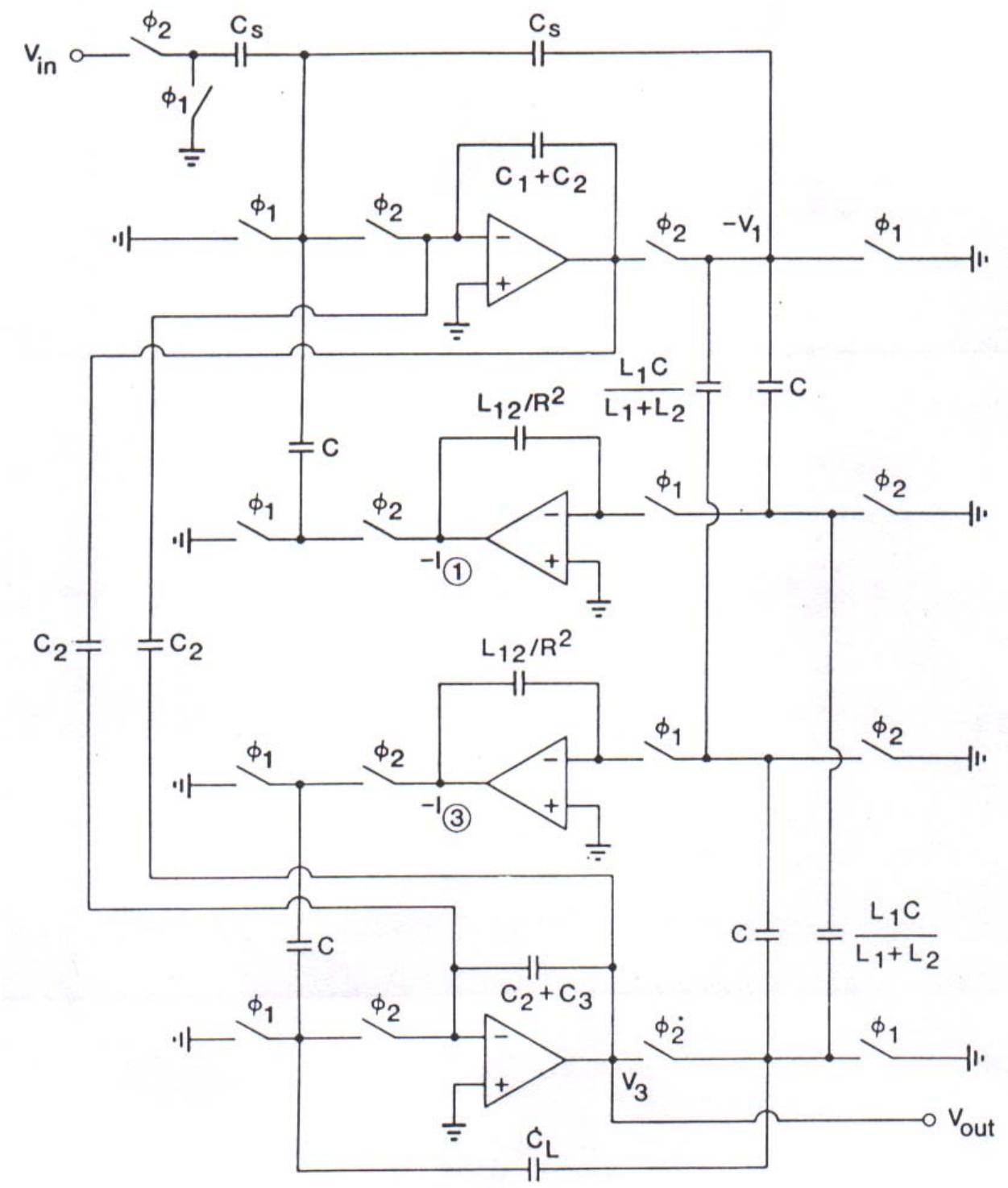
$$V3=\frac{-1}{s(C_2+C_3)}\left[-sC_2V_1-I_{③}+\frac{V_3}{R_L}\right],$$

$$-I_{\bigcirc\!\!\!\!\!\!\Delta\!\!\!\!\!=}I_3-I_2=\frac{-1}{sL_{12}}\left[-V_3+\frac{L_1V_1}{L_1+L_2}\right],$$

Where $L_{12}\underline{\Delta}L_1\|L_2=L_1L_2/(L_1+L_2)$


R_s
C_1+C_2
V_{in}
R_s
$-V_1$
R
L_{12}/R^2
$-R$
$-I_①$
C_2
C_2
$-(1+\frac{L_1}{L_2})R$
L_{12}/R^2
$-I_③$
$-R$
R
C_2+C_3
V_3
V_{out}
R_L

SCF:


V_{in}
ϕ_2
C_S
ϕ_1
C_S
C_1+C_2
ϕ_1
ϕ_2
ϕ_2
$-V_1$
ϕ_1
$\frac{L_1C}{L_1+L_2}$
C
L_{12}/R^2
C
ϕ_1
ϕ_2
ϕ_1
ϕ_2
$-I_①$
C_2
C_2
L_{12}/R^2
ϕ_1
ϕ_2
ϕ_1
ϕ_2
$-I_③$
C
$\frac{L_1C}{L_1+L_2}$
C_2+C_3
ϕ_1
ϕ_2
ϕ_2
ϕ_1
V_3
V_{out}
C_L

General Procedures for the approximate design of SC ladder filter

: 1. A doubly terminated LC two-port is designed from the SCF specifications can be prewarped using the relation:

$$W_a = \frac{2}{T}\sin(\frac{\omega T}{2})$$

which represents the frequency transformation due to the LDI transformation implicit in the design produce.

Inverting SC integrator + Noninverting SC integrator

$$H(z) = -\frac{(C_1/C_2)_{inv}}{1-z^{-1}}\,\frac{(C_1/C_2)_{noninv}\,z^{-1}}{1-z^{-1}}$$

$$= \frac{-Kz^{-1}}{(1-z^{-1})^2} = \frac{-K}{(z^{\frac{1}{2}} - z^{-\frac{1}{2}})^2}$$

Ton $z=e^{j\omega T}$

$$\Rightarrow H(e^{j\omega T}) = \frac{+K}{4\sin^2(\omega T/2)}$$

LDI mapping (Lossless discrete integrator):

$$S_a = \frac{1}{2T}(z - z^{-1})$$

If $\frac{T}{2}$ is used $\Rightarrow S_a = \frac{1}{T}(z^{\frac{1}{2}} - z^{-\frac{1}{2}})$

$$\Rightarrow \omega_a = \frac{1}{T/2}Sin(\omega\frac{T}{2})$$

2. The state equations of the LCR circuit are found. The signs of the voltage and current variables must be chosen such that inverting and noninverting integrators alternate in the implementation. If inductor loops exit, the inductive node currents can be used.

4. The block diagram or signal flow graph (SFG) is constructed from the state equations. It is then transformed (directly or via the active-RC circuit) into the SCF.

5. If necessary, additional circuit transformations can be performed to improve the response of SCF.

§14-10 Exact Design of SC Ladder Filters

* Ladder synthesis based on the bilinear S_a-to-z transformation

☆ $S_a=\frac{2}{T}\ \frac{z-1}{z+1}$ (1)$j\omega_a$─axis＝>unit circle

(2)preserves the flatness of PB and SB

§14-10.1 Third-order SCF (Low-pass with finite transmission zero)

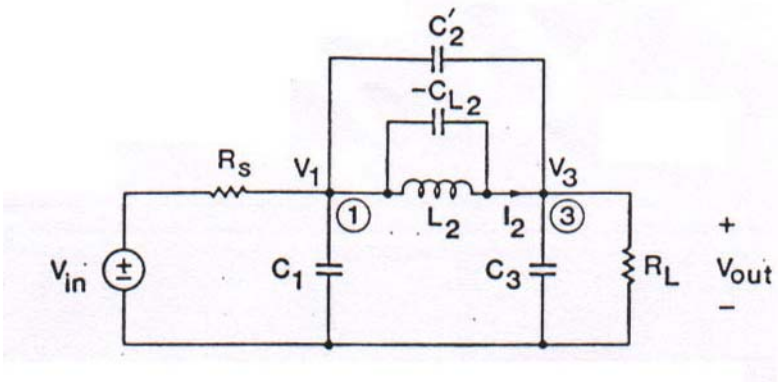
$$\begin{cases} C_2'=C_2+C_{L2} \\ -C_{L2}=\dfrac{-T^2}{4L_2} \end{cases}$$

$$-V_1=\frac{-1}{S_a(C_1+C_2')}\left[-\frac{V_1+V_{in}}{R_s}+s_aC_2'V_3-I_2\right],$$

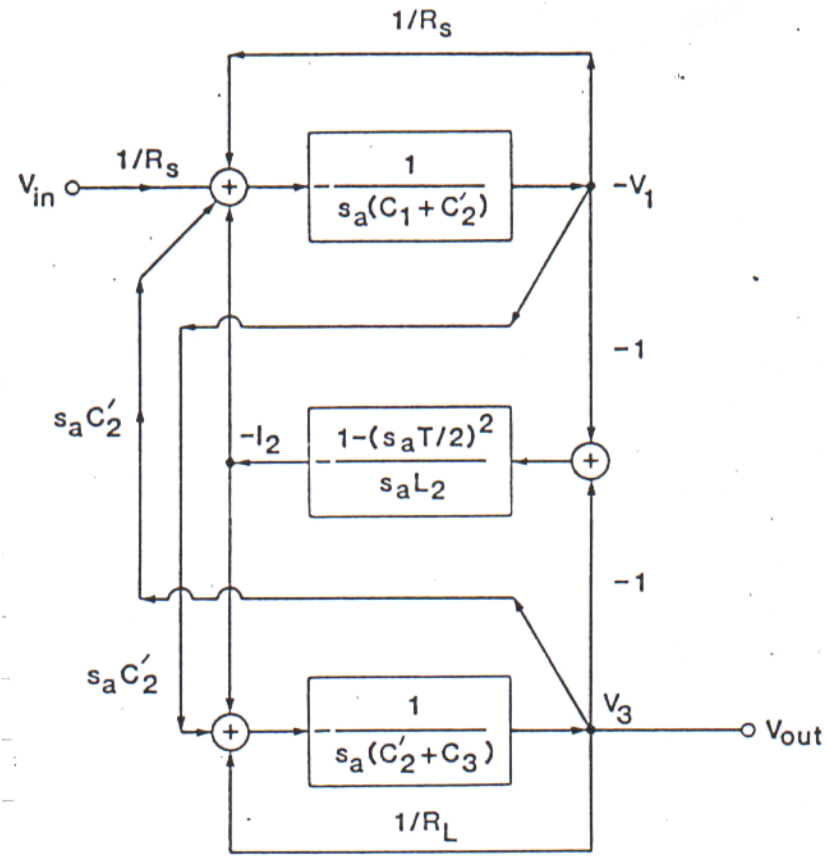
$$-I_2=\left[s_aC_{L2}-\frac{1}{s_aL_2}\right]\left[V_1-V_3\right],$$

$$V_3=\frac{-1}{s_a(C2'+C3)}\left[-s_aC_2'V_1-I_2+\frac{V_3}{R_L}\right].$$

LCR Prototype Circuit:



Flow diagram



The center block has the transfer function:

$$H(S_a)=S_aC_{L2}-\frac{1}{S_aL_2}=\frac{1-S_a^{\,2}L_2C_{L2}}{S_aL_2}=-\frac{1-(S_aT/2)^2}{S_aL_2}$$

Transformation of the blocks into SC circuits:

(1) Finding Q-V relations of all blocks and branches in the S_a domain.
(2) Transforming the Q-V relations into the z-domain.
(3) Realizing the transformed z-domain equations into SC circuits.

Five different blocks:

(a) The input branch $1/Rs$

$$Q_{in}(S_a)=\frac{1}{R_s}V_{in}\frac{1}{S_a}$$

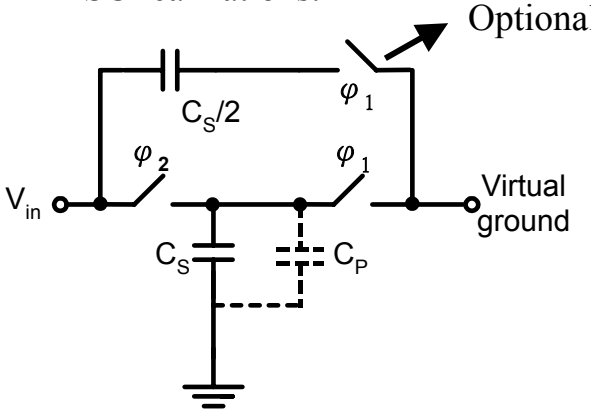
$$Q_{in}(z)=\frac{T}{2}\frac{z+1}{z-1}\frac{V_{in}(z)}{R_s}$$

$$=>(1-z^{-1})Q_{in}=\frac{T}{2R_s}(1+z^{-1})V_{in}(z)$$

$$q_{in}(t_n)-q_{in}(t_{n-1})=\frac{C_s}{2}[V_{in}(t_n)+V_{in}(t_{n-1})]$$

SC realizations:

Optional. To guarantee the charge flow only when $\phi_1=1$



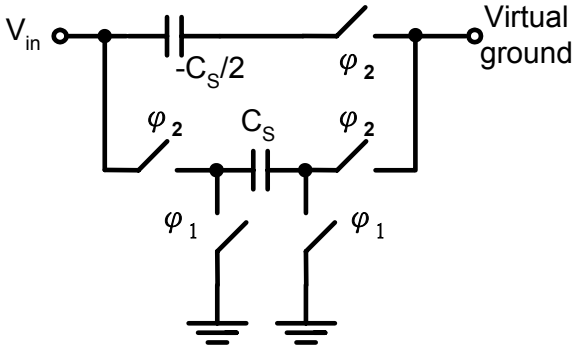
$$\frac{C_s}{2}:\frac{C_s}{2}[V_{in}(t_n)-V_{in}(t_{n-1})]$$

Cs : Cs V_{in} (t_{n-1})

* Not stray insensitive.

$C_p + C_s$ not C_s

(b) The feedback branch $1/R_s$, $1/R_L$



$$-\frac{C_s}{2}:-\frac{C_s}{2}[V_{in}(t_n)-V_{in}(t_{n-1})]$$

C_s: $C_s V_{in}(t_n)$

$\Downarrow$

$$\frac{Cs}{2}[V_{in}(t_n)+V_{in}(t_{n-1})]$$

* Stray insensitive.

(c)The branches S_aC

$$\frac{Q}{V}=CS_a\frac{1}{S_a}=C$$

Only a C is required.

(d) The blocks $-\frac{1}{S_aC}$

$$\frac{Q}{V}=-C \quad => \text{OP with a feedback capacitor C.}$$

(e) The center block

$$-I_2=-\frac{1-(S_a T/2)^2}{S_a L_2}(V_1-V_3)$$

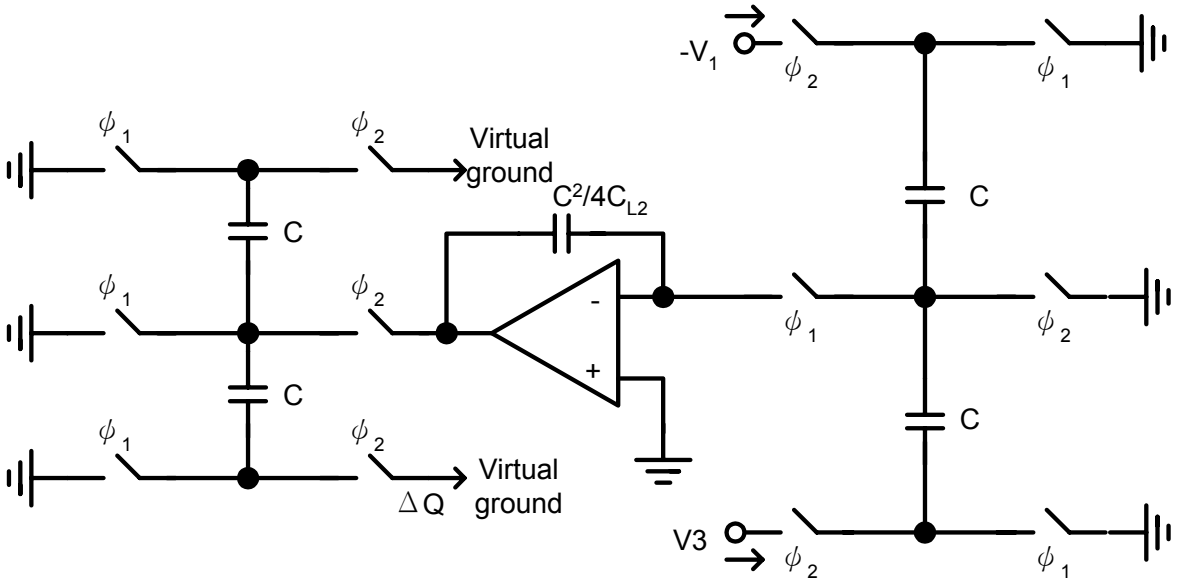
$$Q(S_a)=\frac{-I_2}{S_a}=-\frac{1-(S_a T/2)^2}{S_a^{\,2} L_2}(V_1-V_3)$$

$$=>\frac{Q(z)}{V_1(z)-V_3(z)}=-\frac{1-[(z-1)/(z+1)]^2}{(4L_2/T^2)[(z-1)/(z+1)]^2}=-\frac{4C_{L2}Z}{(z-1)^2}$$

$$\Delta Q(z)=(1-z^{-1})Q(z)=\frac{4C_{L2}}{z-1}(V_3-V_1)$$

$$\frac{\Delta Q(z)}{V_3-V_1}=\frac{4C_{L2}z^{-1}}{1-z^{-1}}=(-Cz^{-1})(\frac{-4C_{L2}/C^2}{1-z^{-1}})(C)$$

Realizations:



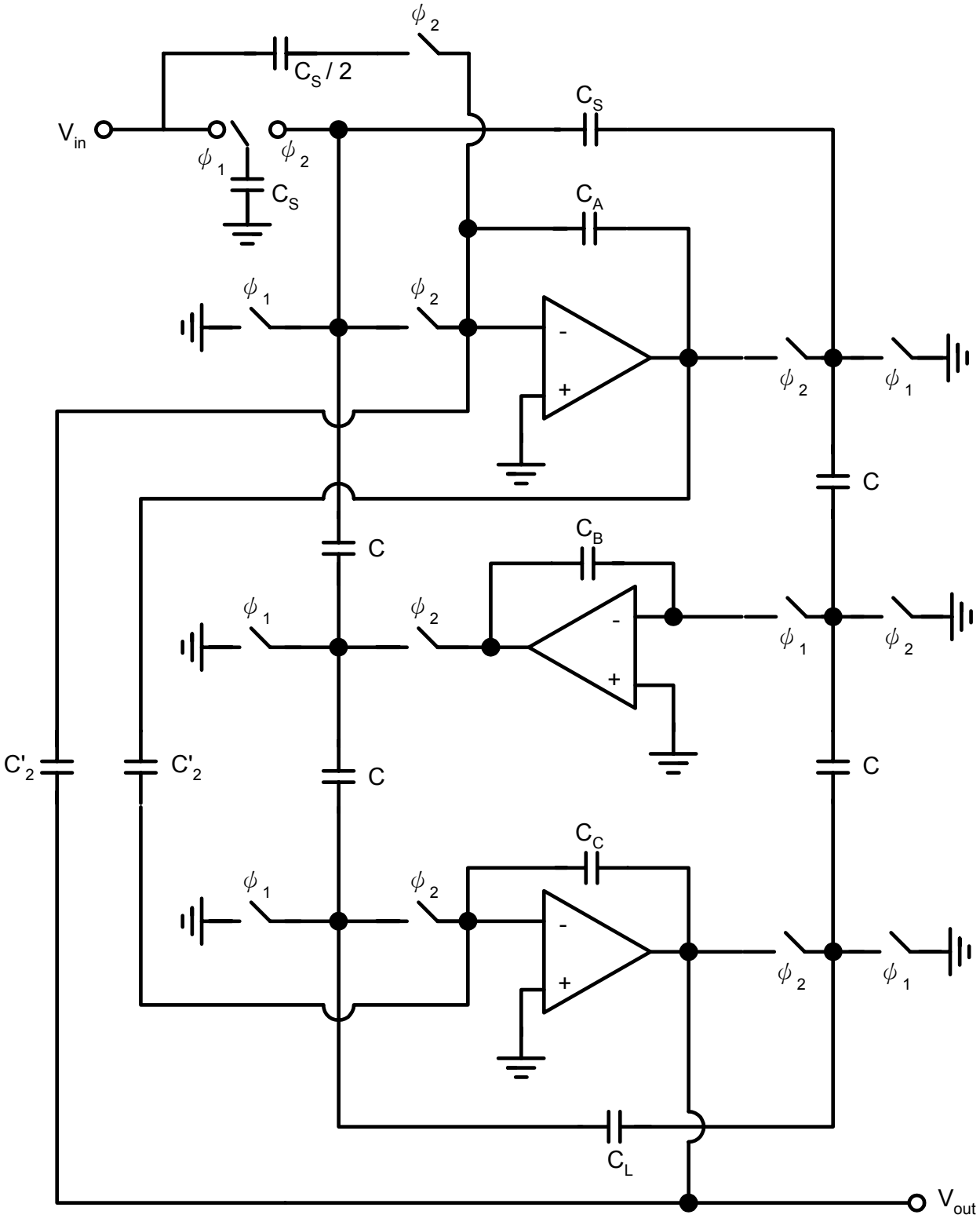
The final realization is shown in the next page.

* This circuit is not fully stray insensitive.
* The negative capacitor $-\frac{C_s}{2}$ has been merged into the feedback capacitors C_A and C_B, respectively.

$C_A=C_1+C_2'-\frac{C_s}{2}$ $\qquad$ $C_B=C_2'+C_3-\frac{C_s}{2}$

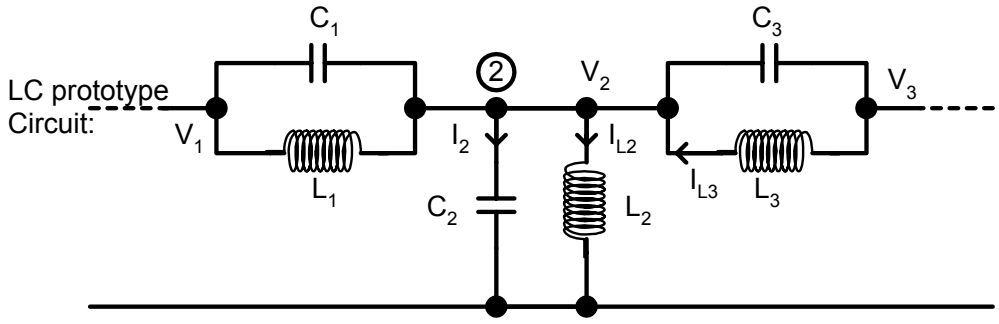
* Why C_2', $-C_{L2}$?
  To create a block which is realizable by SC circuit.

SCF:

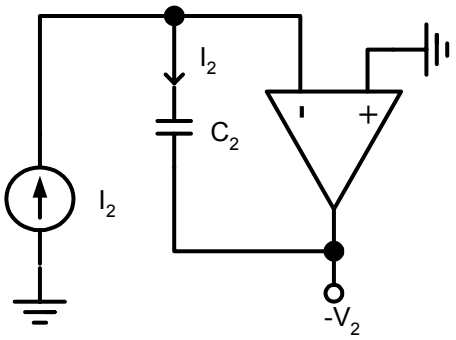


The complete bilinear ladder circuit equivalent to the LCR circuit

§14-10.2 Bandpass LCR filters



$-V_2$ can be produced as:



$$I_2=(SC_1+\frac{1}{SL_1})(V_1-V_2)+(SC_3+\frac{1}{SL_3})(V_3-V_2)-\frac{V_2}{SL_2}$$

Note that $\dfrac{1-(S_a T/2)^2}{S_a L}$ is realizable !

$$=>I_2(S)=S[(C_1+C_{L1})V1+(C_1+C_3+C_{L1}+C_{L3})(-V_2)+(C_3+C_{L3})V_3]$$

$$+(\frac{1}{S}-\frac{T^2 s}{4})[\Gamma_1 V_1+(\Gamma_1+\Gamma_2+\Gamma_3)(-V2)+\Gamma_3 V3]$$

Where $C_{Li}\equiv\dfrac{T^2}{4L_i}$, $\Gamma i=\dfrac{1}{L_i}$

First Term:

$Q_2'(S)=(C_1+C_{L1})V_1+(C_1+C_3+C_{L1}+C_{L3})(-V_2)+(C_3+C_{L3})V_3$

Can be realized by unswitched capacitors.

Second Term:

$$Q_2''(Z)=[(\frac{T}{2}\frac{z+1}{z-1})^2-\frac{T^2}{4}][\Gamma_1 V_1+(\Gamma_1+\Gamma_2+\Gamma_3)(-V_2)+\Gamma_3 V_3]$$

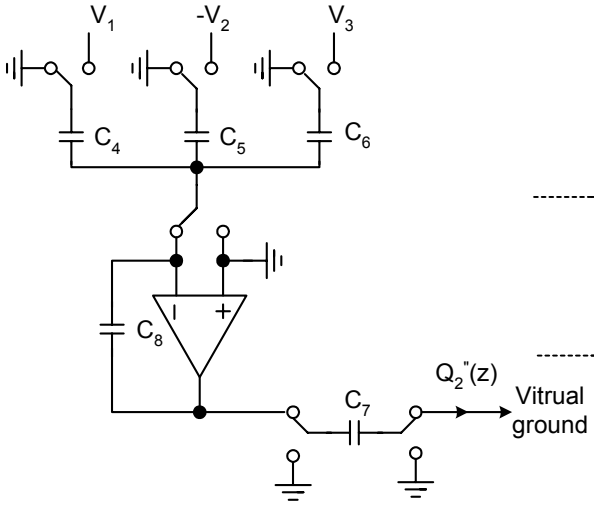
$$=\frac{T^2 z^{-1}}{(1-z^{-1})^2}[\Gamma_1 V_1+(\Gamma_1+\Gamma_2+\Gamma_3)(-V_2)+\Gamma_3 V_3]$$

The same as before but now three functions are superposed together. ($\Delta Q_2"/V_1, \Delta Q_2"/(-V_2), \Delta Q_2"/V_3$)

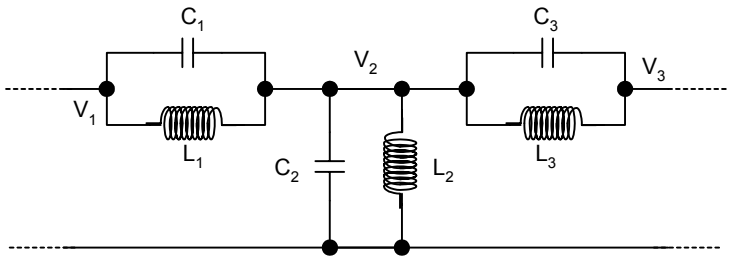
Conditions: $\frac{C_4 C_7}{C_8} = \frac{T^2}{L_1} = 4C_{L1}$; $\frac{C_5 C_7}{C_8} = T^2(\frac{1}{L_1}+\frac{1}{L_2}+\frac{1}{L_3}) = 4(C_{L1}+C_{L2}+C_{L3})$

$$\frac{C_6 C_7}{C_8} = \frac{T^2}{L_3} = 4C_{L3}$$

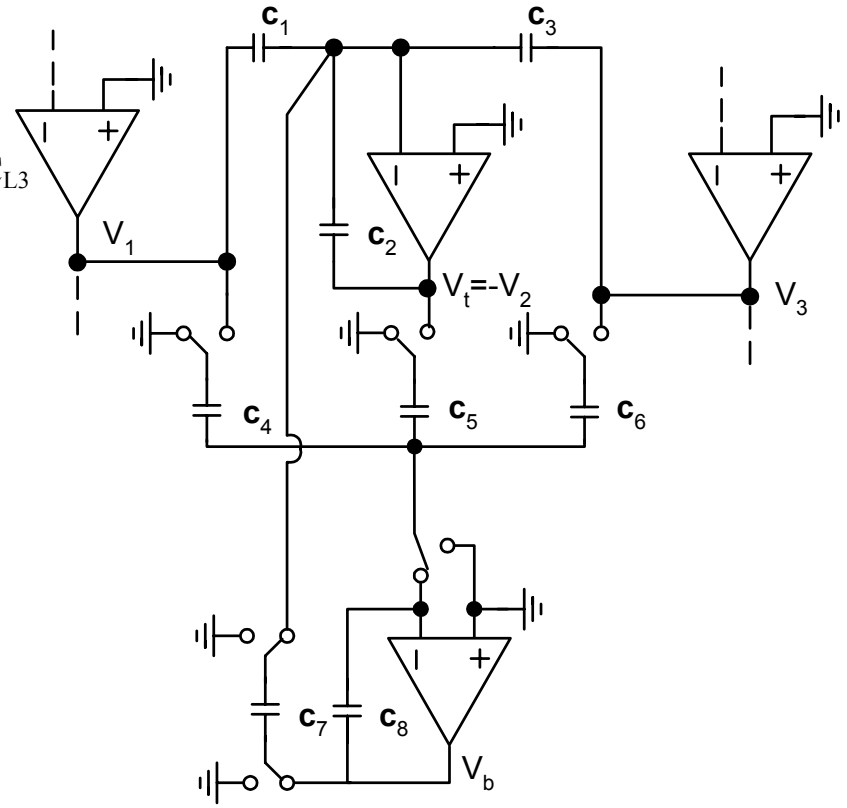
Stage providing $Q_2"(z)$:



LC prototype circuit:



SC realization:



Design equations:

$C_{L1}=T^2/(4L_i)$

$\mathbf{c}_1=C_1+C_{L1}$

$\mathbf{c}_2=C_1+C_2+C_3+C_{L1}+C_{L2}+C_{L3}$

$\mathbf{c}_3=C_3+C_{L3}$

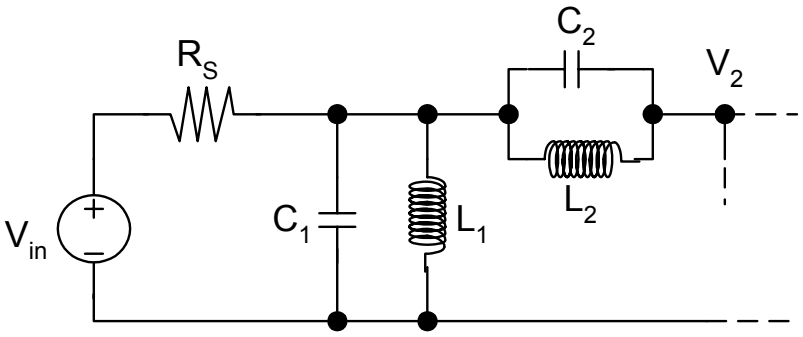
$\mathbf{c}_4=4\frac{c_8}{c_7}C_{L1}$

$\mathbf{c}_5=4\frac{c_8}{c_7}(C_{L1}+C_{L2}+C_{L3})$

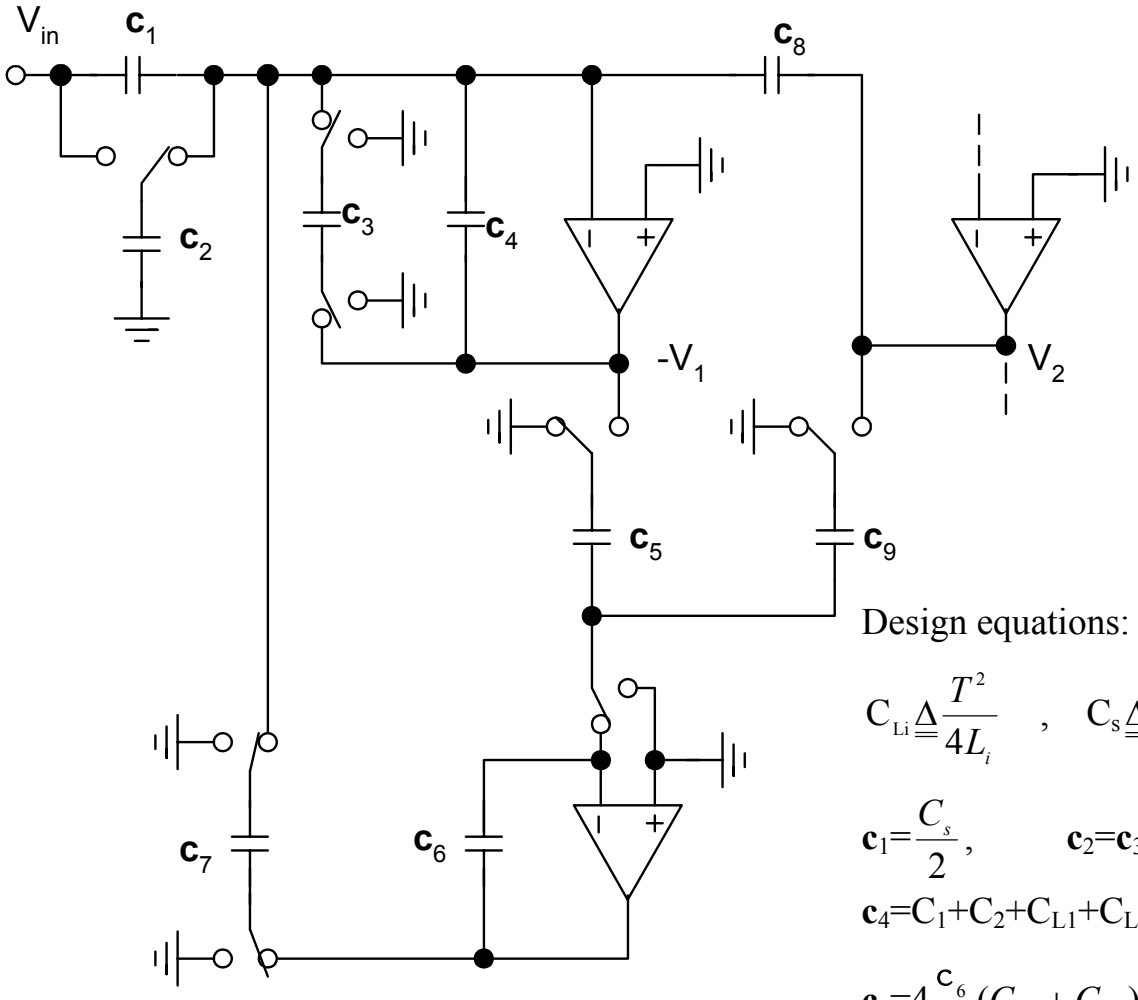
$\mathbf{c}_6=4\frac{c_8}{c_7}C_{L3}$

$\mathbf{c}_7$, $\mathbf{c}_8$ arbitrary

LC prototype circuit with R_S:



SC realization:



Design equations:

$C_{Li} \triangleq \frac{T^2}{4L_i}$, $C_s \triangleq \frac{T}{R_s}$

$\mathbf{c}_1 = \frac{C_s}{2}$, $\mathbf{c}_2 = \mathbf{c}_3 = C_9$

$\mathbf{c}_4 = C_1 + C_2 + C_{L1} + C_{L2} - C_S/2$

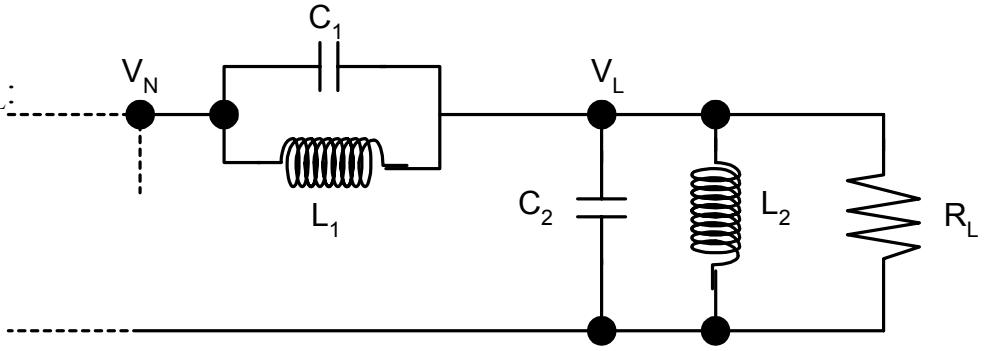
$\mathbf{c}_5 = 4\frac{\mathbf{c}_6}{\mathbf{c}_7}(C_{L1} + C_{L2})$

$\mathbf{c}_8 = C_2 + C_{L2}$

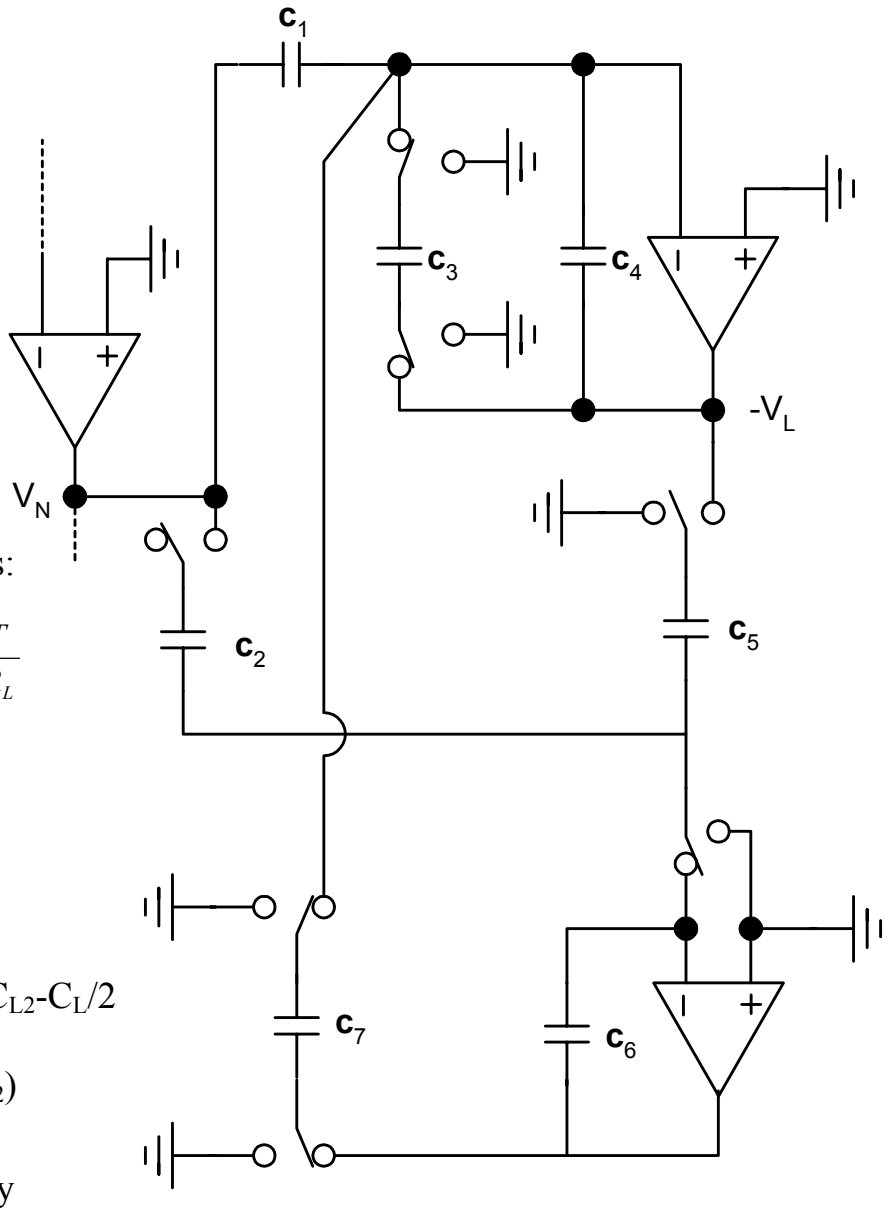
$\mathbf{c}_9 = 4\frac{\mathbf{c}_6}{\mathbf{c}_7} C_{L2}$

$\mathbf{c}_6$, $\mathbf{c}_7$ arbitrary

LC prototype circuit with R_L:



SC realization:



Design equations:

$C_{L1} \triangleq \frac{T^2}{4L_i}$, $C_L \triangleq \frac{T}{R_L}$

$\mathbf{c}_1 = C_1 + C_{L1}$

$\mathbf{c}_2 = 4\frac{\mathbf{c}_6}{\mathbf{c}_7} C_{L1}$

$\mathbf{c}_3 = C_L$

$\mathbf{c}_4 = C_1 + C_2 + C_{L1} + C_{L2} - C_L/2$

$\mathbf{c}_5 = 4\frac{\mathbf{c}_6}{\mathbf{c}_7}(C_{L1} + C_{L2})$

$\mathbf{c}_6$, $\mathbf{c}_7$ are arbitrary

Z-domain verifications:

Upper OP AMP:

$$C_1(1-z^{-1})V_1+C_3(1-z^{-1})V_3+C_2(1-z^{-1})V_t+C_7V_b=0$$

Lower OP AMP:

$$-C_4z^{-1}V_1-C_6z^{-1}V_3-C_5z^{-1}V_t+C_8(1-z^{-1})V_b=0$$

$$=> \quad V_t=-\frac{N_1V_1+N_3V_3}{D}$$

$$V_b=\frac{z^{-1}(1-z^{-1})[(C_2C_4-C_1C_5)V_1+(C_2C_6-C_3C_5)V_3]}{C_8D}$$

where

$$N_1(z)=C_1C_8[(1-z^{-1})^2+\frac{C_4C_7}{C_1C_8}z^{-1}]$$

$$N_3(z)=C_3C_8[(1-z^{-1})^2+\frac{C_6C_7}{C_3C_8}z^{-1}]$$

$$D(z)=C_2C_8[(1-z^{-1})^2+\frac{C_5C_7}{C_2C_8}z^{-1}]$$

* All poles and zeros of the transfer functions V_t/V_1, V_t/V_3, V_b/V_1, and V_b/V_3 are located on the unit circle.

After the bilinear s-to-z transformation,

$$V_t=-\frac{[(C_1C_8-C_4C_7/4)S^2+C_4C_7/T^2]V_1+V_3[(C_3C_8-C_6C_7/4)S^2+C_6C_7/T^2]}{(C_2C_8-C_5C_7/4)S^2+C_5C_7/T^2}$$

$$V_b=\frac{S(\frac{1}{T}-\frac{S}{2})[(C_2C_4-C_1C_5)V_1+(C_2C_6-C_3C_5)V_3]}{(C_2C_8-C_5C_7/4)S^2+C_5C_7/T^2}$$

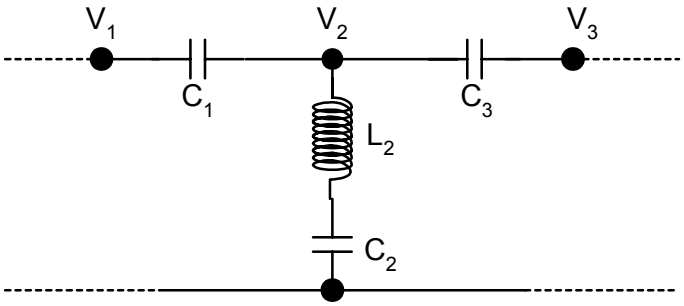
* The phase shift between V_t and V_1, as well as between V_t and V_3 are either 0° or 180° for $s=j\omega$

=>The same as for the LC prototype regardless of the element values C*i*.

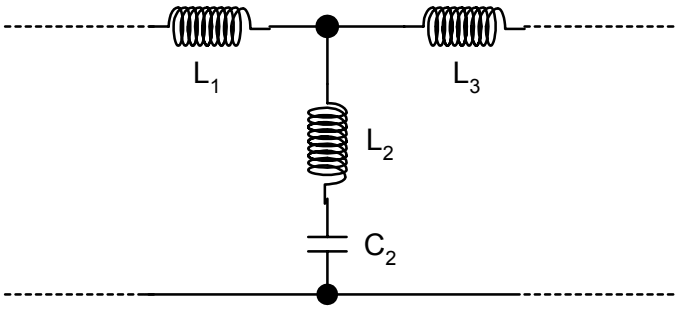
=>Can simulate a lossless LC with the same low sensitivity.

* It can also simulate the behavior of any LC ladder section which has a T configuration.

High-pass



Low-pass



$V_t=-V_2$

$$=> V_2=\frac{(aS^2+b)V_1+(cS^2+d)V_3}{eS^2+f}$$

* High-Pass Case :

At $Z=e^{j\omega T}=-1$, i.e. $\omega=\frac{\omega_c}{2}=\frac{2\pi/T}{2}$

If the loss is zero (i.e. passband),

$$=>(1-z^{-1})Q_{in}(z)=\frac{T}{2R_s}(1+z^{-1})V_{in}(z)$$

$$=0$$

$Q_{in}(z)=0$, but loss is zero

=>The other part of the circuit

should have an infinite gain.

=>unstable.

R_s input (i.e. input termination) is a problem!

* Inductor loop is O.K.

§14-10.3 Comparisons

LDI Realizations of Ladder Filters using SC Integrators

(1) Prewarping is required

(2) Inductor loop exists

=>Modified design

=>Component sensitivity ↑

Bilinear Realizations of Ladder Filters using SC Integrations

(1) Prewarping is not required.

(2) Low-pass, band-pass ladder filters are O.K.
But they are not fully stray insensitive.

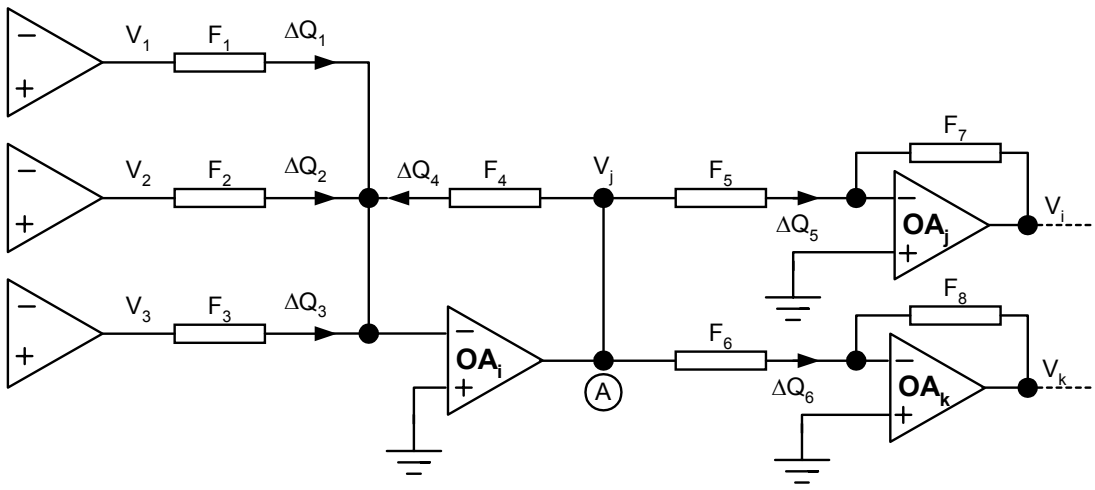
(3) Can't realize high-pass or band-reject filters.

=> Instability exists.

(4) Some modifications are proposed.
But they are not fully stray insensitive.

§14-11 The Scaling of High-Order SCF's.

Why scaling? (1) Improve the actual performance.
(2) Reduce the silicon area



SC filter section.

Let all branches connected to the output terminal of OA_i be modified such that their $\Delta Q/V$ transfer functions F_4, F_5, and F_6 are multiplied by a positive real constant factor k. This can be achieved simply by multiplying all capacitors in these branches by k_i.

Since the input branches and their voltages were left unchanged, the change flowing in the feedback branch is

$\Delta Q_4(z)=-\Delta Q_1(z)-\Delta Q_2(z)-\Delta Q_3(z)$ remains at its original value.

$=>$ $V_2'(z)=\Delta Q_4(z)/[k_iF_4(z)]=V_i(z)/k_i$

The new output voltage of OA_i — The old output voltage of OA_i

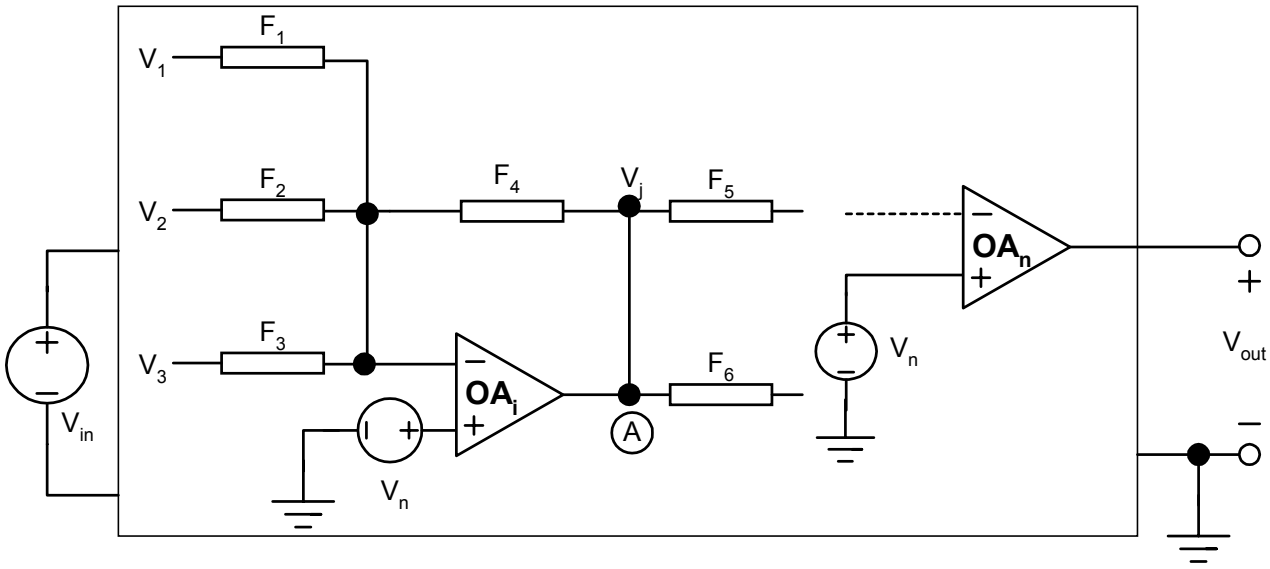
$V_i \rightarrow V_i/k_i$ due to scaling.

$$\Delta Q_5'=F_5'(z)V_i'(z)=k_iF_5(z)\frac{V_i(z)}{k_i}=F_5(z)V_i(z)=\Delta Q_5(z)$$

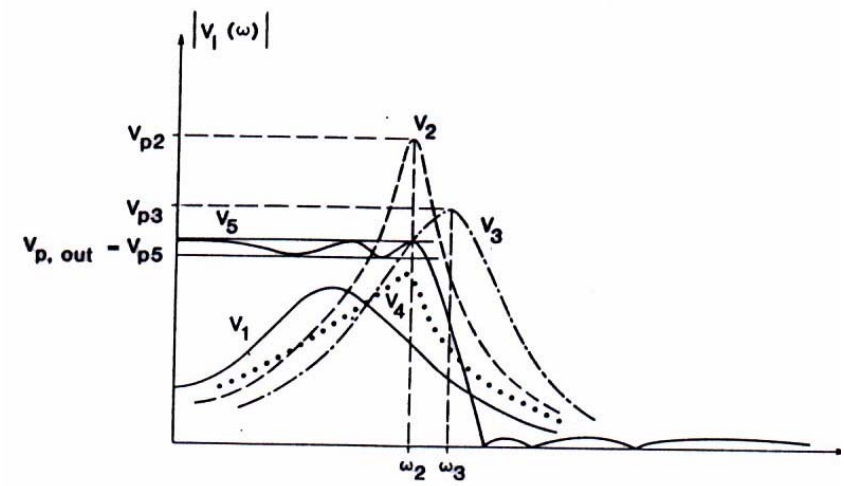
Voltage scaling does not change charge flowing from the scaled branch to the rest of the circuit.

$=>$Only V_i/k_i, all other voltages or changes are not affected.

Optimization of the dynamic range using scaling



$V_{max}/A_p \geq V_{in,\,max}$ A_p: passband gain.



Op-amp output voltage responses for a low-pass filter.

OA_2 will saturate before OA_5 because $|V_2| > |V_5|$ for $\omega \sim \omega_2$.

Now, we choose $V_{in,\,max}=V_{max}/A_2$

$A_2=\left|V_{p2}/V_{in}\right|$, $A_p=\left|V_{p5}/V_{in}\right|$

$A_2=A_p\left|V_{P2}/V_{P5}\right|$

$$V_{in,\,max}=\frac{V_{max}}{A_2}=\frac{V_{max}}{A_P}\frac{V_{P5}}{V_{P2}}<\frac{V_{max}}{A_P} \qquad \text{since } V_{P5}/V_{P2}<1$$

=>Maximum Vin ↓=> Dynamic range ↓

Reducing V_2 by scaling.

$V_2'(\omega)=V_2(\omega)/k_2$ $\qquad k_2=V_{P2}/V_{P5}$

=>V_2' has a peak value of V_{P2}' which is equal to V_{P5}.

=>$V_{in,\,max}=V_{max}/A_p$

Similarly, $k_3=V_{P3}/V_{P5}$. $k_1=V_{P1}/V_{P5}<1$, $k_4=V_{P4}/V_{P5}<1$.
It is not good to choose $k_2(k_3)> V_{P2}/V_{P5}(V_{P3}/V_{P5})$ because the noise will be increased.

=> dynamic range ↓.

CONCLUSION:

For maximum dynamic range, all op-amp outputs should be scaled such that each (at its own maximum frequency) saturates for the same input voltage level.

Let the transfer functions $F_j(z) \equiv \Delta Q_j / V_j$ of all branches connected to the input terminal of OA_i be multiplied by a positive real constant M_i => $C_i \rightarrow mC_i$

$$\Delta Q_n \quad , n=1, 2, \underbrace{3, 4}_{F_1, F_2, F_3, F_4} \rightarrow \Delta Q_n' = m_i \Delta Q_n$$

$$V_i' = \frac{\Delta Q_4'}{F_4'} = \frac{m_i \Delta Q_4}{m_i F_4} = \frac{\Delta Q_4}{F_4} = V_i \qquad V_i \text{ unchanged!}$$

The output charges ΔQ_5 and ΔQ_6 also remain the same

=>The above scaling by m_i leaves all op-amp output voltages in the SCF unchanged. Only the charges in the scaled branches get multiplied by m_i.

=>Effective in reducing the cap. spread and the total capacitance of a SCF.

$C_{i,\,min}$ among all capacitors contained in these four branches is located. =>All capacitors contained in these four branches are multiplied by $m_i = C_{min}/C_{i,\,min}$

=> The smallest capacitance becomes C_{min} and all op-amp voltages remain unaffected.

* Scaling for optimum dynamic range should be performed first, and scaling for minimum capacitance afterwards.

1. Scaling for Maximum Dynamic Range
   (a) Set $V_{in}(\omega)$ to the largest value for which the output op-amp does not saturate. Record $V_{in}(\omega)$ and $V_{i,\,max}$
   (b) Calculate V_{pi} for all internal op-amp output V_{pi} usually occur near the passband edges.
   (c) Multiply all capacitors connected or switched to the output terminal of op-amp i by $k_i = V_{pi}/V_{i,max}$ where $V_{i,max}$ is the saturation voltage at the output.
   (d)Repeat for all internal op-amps.

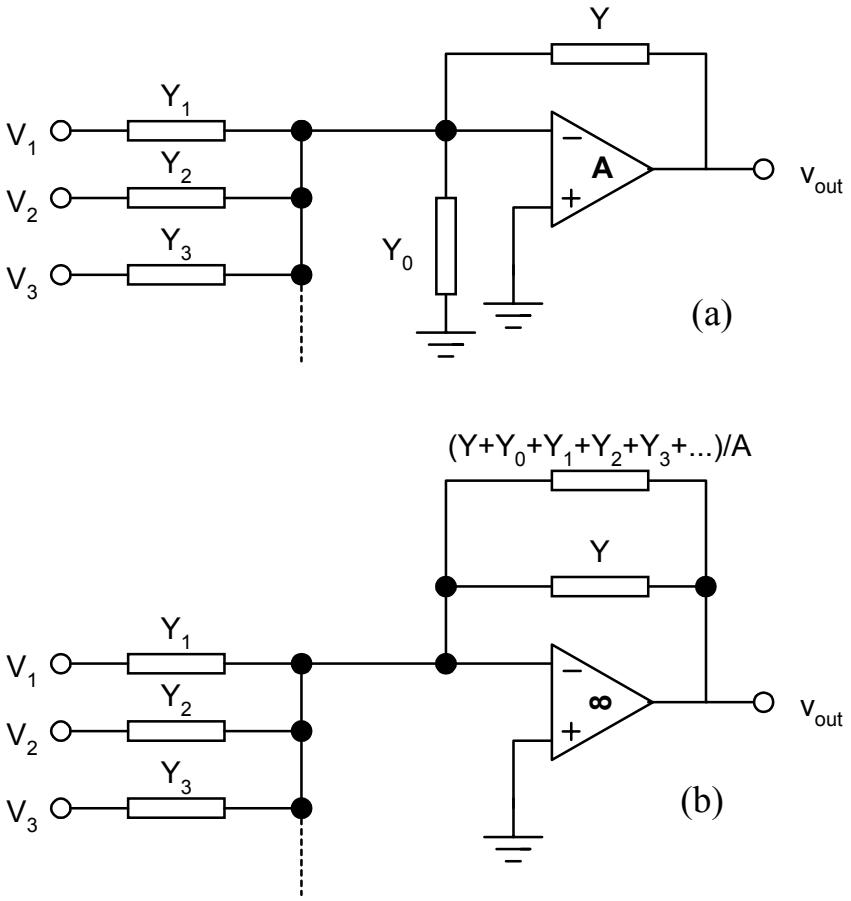
2.Scaling for Minimum Capacitance
   (a) Divide all capacitors in SCF into nonoverlapped sets. Capacitors in the i^{th} set S_i are connected or switched to the input terminal of

op-amp *i*.

(b) Multiply all capacitors in S_i by $m_i=C_{min}/C_{i,\,min}$.

(c) Repeat for all sets S_i.

* Scaling for optimum dynamic range may also reduce the sensitivity to finite op-amp gain effects.



The influence of finite op-amp gain: (a) actual circuits; (b) equivalent circuits.

3. The block diagram or signal flow graph (SFG) is constructed from the state equations. It is then transformed (directly or via the active-RC circuit) into the SCF.
4. If necessary, additional circuit transformations can be performed to improve the response of SCF.

§14-10 Design Examples on Cascaded SCF and LDI Ladder SCF

§14-10.1 Cascaded SCF

Filter Specification

Passband: 0 to f_p=1kHz
passband ripple $\alpha_p \le 0.05$dB
(Maximum allowable passband gain variation)

Stopband: $f_s \le 1.5$KHz to $f_c/2$
Minimum stopband loss $\alpha_s \ge 38$dB
(Maximum allowable gain value)

Sampling frequency: $f_c=\frac{1}{T}$=50KHz

Design Procedures:
1.S-domain transfer function H(s)
Frequency prewarping

$$\omega_{ap}=\frac{2}{T}\tan\frac{\omega_p T}{2}=6291.4667 \text{ rad/s}$$

$$\omega_{as}=\frac{2}{T}\tan\frac{\omega_s T}{2}$$

Selectivity parameter

$$k\equiv\frac{\omega_{ap}}{\omega_{as}}\cong 0.6656$$

Elliptic filter is chosen to minimize the filter order.

Results:

$$\hat{H}(S_a)=\left(\frac{\hat{k}}{\underset{(-\hat{a}_0)}{0.068}}\right)\left(\frac{S^2a+\hat{\omega}_1^{\,2}}{S_a^{\,2}+\underset{(-2\hat{a}_1)}{0.96934556}S_a+\hat{a}_1^{\,2}+\hat{b}_1^{\,2}}\right)$$

$$\left(\frac{S_a^{\,2}+\hat{\omega}_2^{\,2}}{S_a^{\,2}-2\hat{a}_2S_a+\hat{a}_2^{\,2}+\hat{b}_2^{\,2}}\right)$$

where $\hat{a}_1$=-0.48467278, $\hat{b}_1$=0.82815049, $\hat{a}_2$=-0.128006731,

$\hat{b}_2$=1.100351473, $\hat{w}_1$=1.5514948, $\hat{w}_2$=2.32131474

=> filter order=5

$\hat{w}_{ap}$=1 rad/s, $\hat{\alpha}_p$=0.044dB, $\hat{w}_{as}$=1.49448 rad/s,

$\hat{\alpha}_s$=39.57dB, $\hat{k}$=0.669

=> The specifications are satisfied with $\hat{H}_a(0)=1$

2. frequency denormalization and z-domain transfer function H(z)

Denormalization: $S_a \rightarrow S/\omega_p$

$\hat{H}(S_a) \rightarrow H(S)$

$$H(S)=K\frac{(S^2+\omega_1^{\,2})(S^2+\omega_2^{\,2})}{(S-a_0)(S^2-2a_1s+a_1^{\,2}+b_1^{\,2})(S^2-2a_2s+a_2^{\,2}+b_2^{\,2})}$$

Where K=428.247646, $\omega_1=9.76117788\times10^3$,

$\omega_2=1.46044744\times10^4$, $a_o=-4.91615278\times10^3$

$a_1=-3.04930266\times10^3$, $b_1=5.21028124\times10^3$

$a_2=-805.350086$, $b_2=6.92282466\times10^3$

Bilinear transformation: $S\rightarrow \frac{2}{T}\frac{z-1}{z+1}=10^5\frac{z-1}{z+1}$

$H(s) \rightarrow H(z)$

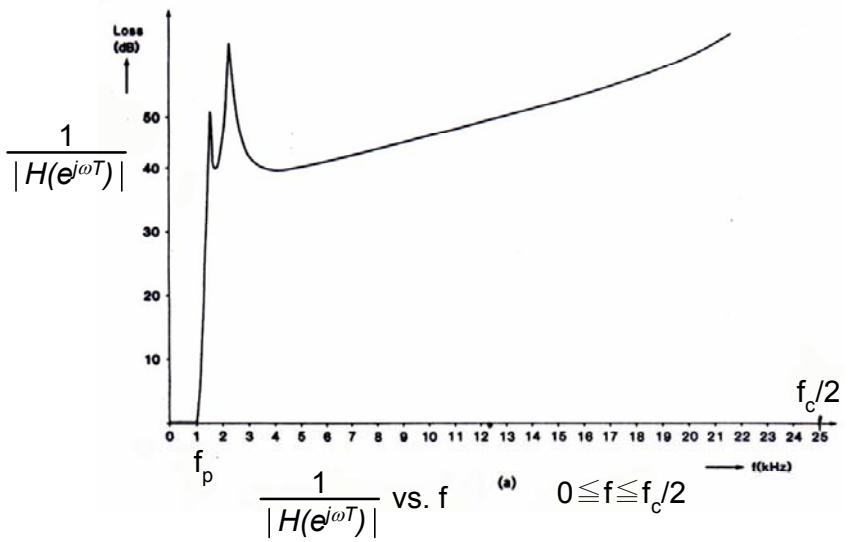
$$H(z)=(C\frac{z+1}{z+d_o})(\frac{z^2+C_1z+1}{z^2+e_1z+f_1})(\frac{z^2+C_2z+1}{z^2+e_2z+f_2})$$

Where $C=3.8719271\times10^{-3}$, C_1= -1.962247471, C_2= -1.916465445,

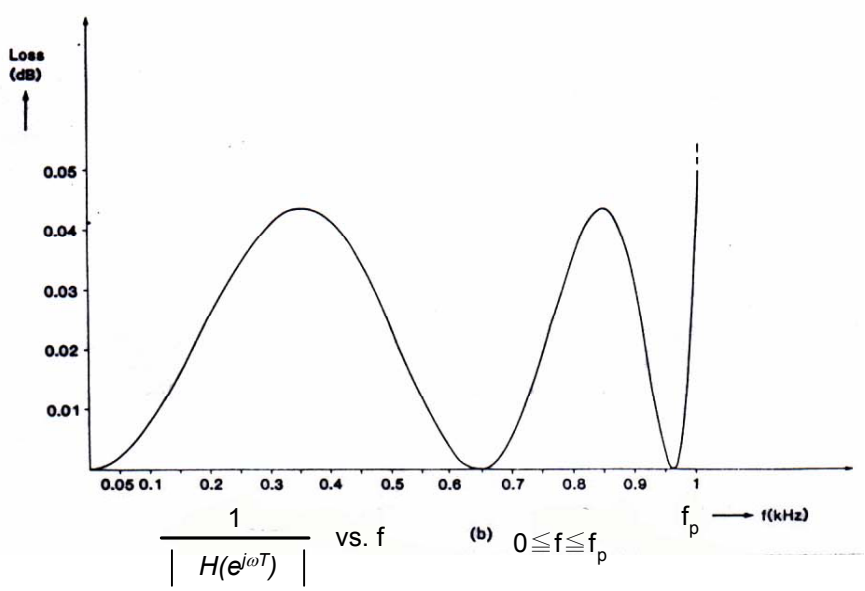
d_o=-0.906284158, e_1= -1.871739343, f_1=0.88543246,

e_2=-1.949416807, f_2=0.968447477.

Check: $\left|H(e^{j\omega T})\right|$ satisfies specifications.

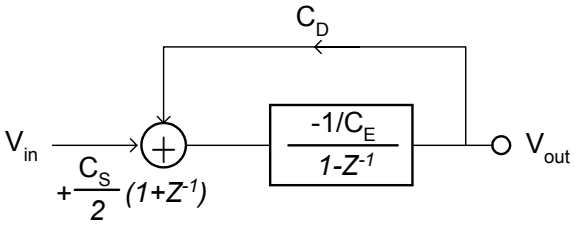


$\frac{1}{|H(e^{j\omega T})|}$ vs. f (a) $0 \leqq f \leqq f_c/2$



3. SC realization

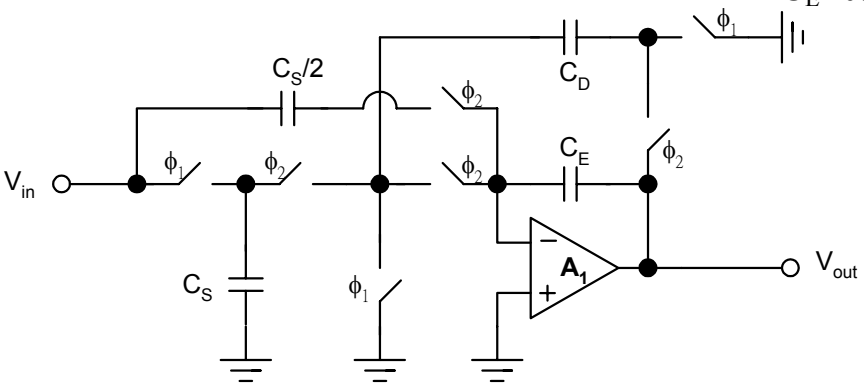
(1) $H_0(z)=\dfrac{z+1}{z-0.9063}$



$$H_0(z)=-\frac{Cs/2}{C_D+C_E}\times\frac{z+1}{z-C_E/(C_D+C_E)}$$

Cs=2 arbitrarily chosen

$\Rightarrow C_E=0.9063$, $C_D=0.0937$



(2) $H_1(z)=\dfrac{z^2+C_1z+1}{(1/f_1)z^2+(e_1/f_1)z+1}$

$Q_1=\dfrac{(a_1^{\,2}+b_1^{\,2})^{1/2}}{2|a_1|}\cong 0.99$ Low-Q

The SCF is shown on P.14-21.

The component values are: $C_1''=a_0=1$,

$C_1'=a_2-a_0=0$,

$C_2=C_3=\sqrt{b_1+b_2+1}=\sqrt{(e_1+1)/f_1+1}\cong 0.12436$,

$C_1=(a_0+a_1+a_2)/C_3 \cong 0.30358$,
$C_4=b_2-1=1/f_1-1 \cong 0.12939$,
$C_A=C_B=1$.

(3) $H_2(z)=\dfrac{z^2+C_2z+1}{(1/f_2)z^2+(e_2/f_2)z+1}$ $\quad Q_2=\dfrac{(a_2^2+b_2^2)^{1/2}}{2|a_2|} \cong 4.33$ =>High-Q

The SCF is shown on P.14-23.

The component values are:

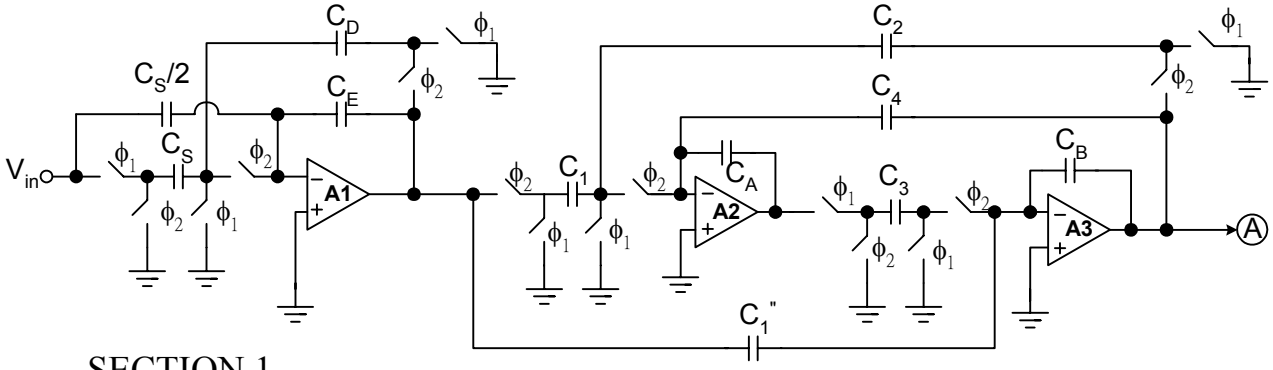
$C_1''=a_2/b_2=f_2 \cong 0.96845$ $\quad C_1'=(a_1-a_0)/b_2c_3=0$,

$C_2=C_3=\sqrt{(1+b_1+b_2)/b_2}=\sqrt{f_2+e_2+1} \cong 0.13795$,

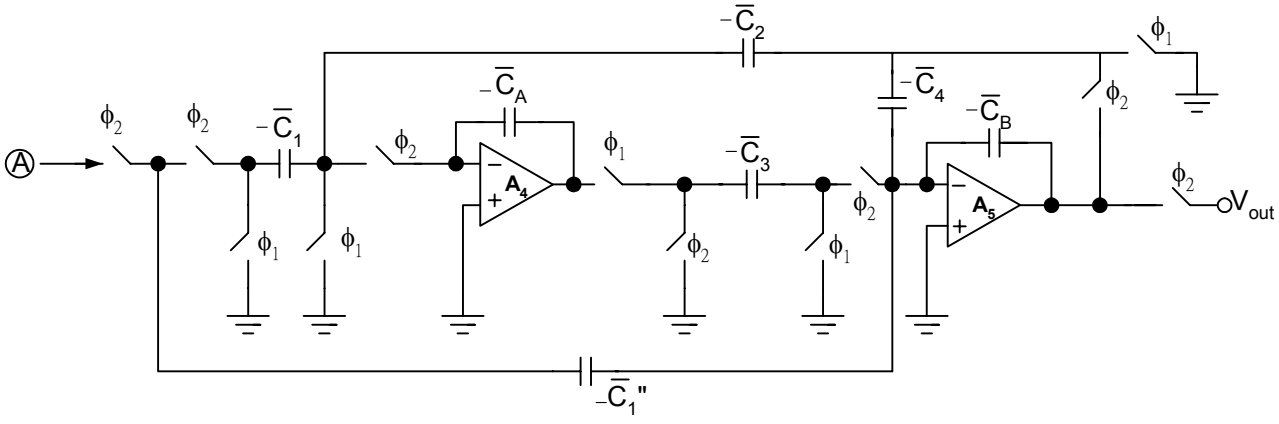
$C_1=(a_0+a_1+a_2)/b_2C_3=(2+c_2)f_2/C_3 \cong 0.58645$,
$C_4=(1-1/b_2)/C_3=(1-f_2)/C_3 \cong 0.22873$.

(4)Overall SCF

* Ho (low-pass linear section) is placed first
  =>High-frequency out-of-band signals and input noise can be attenuated.
  The antialiasing filter preceding the SCF has a lower requirement.
* H_2 (high-Q section) is placed to the center=>good signal-to-noise ratio



SECTION 1 SECTION 2 (HIGH Q)



SECTION 3 (LOW Q)

4. Scaling

1) V_{p1}=occurs at dc where $H_0(1)=-C_S/C_D=-21.345$

(1)We want an overall passband gain of 1. =>Ho(1)→-1

=> $C_D=C_S=2$, $C_E \cong 19.345$, C_1"20.672, $C_2 \cong 12.518$

(Multiplying all capacitors connected or switched to the output node of op-amp A_1 by 21.345)

(2)All capacitors at the input node of A_1 should be scaled so that the smallest ($Cs/2$) equals 1. (O.K.)

2) Vp_2 (peak output voltage of op-amp A_2) occurs around f_{p2}=1.10kHz

(1) $V_{p2} \cong 177.05$ for $V_{in}=1$

Reducing V_{p1}/V_{in} to 1

=>C_A and C_3 are multiplied by 177.05=> $C_A \cong 177.05$, $C_3 \cong 24.424$.

(2) $V_{p3} \cong 180.80$ at 1.07kHz

=>C_B,C_2, and C_4 are multiplied by 180.80=>$C_B \cong 180.80$, $C_2 \cong 24.941$, $C_4 \cong 41.354$.

(3) Minimize total capacitance=>C_1, C_2, C_4, and C_A at the input node of op-amp A_2 are scaled to make $C_1=1$

=>$C_1=1$, $C_2 \cong 1.9926$, $C_4 \cong 3.3036$, $C_A \cong 14.144$

(4) Similarly, C_1"=1, $C_3 \cong 1.1815$, $C_B \cong 8.7466$. (The input of A_3)

3) $Vp_4 \cong 503.57$ and $Vp_5 \cong 230.14$

Thought the same procedures, we have

$$\overline{C_A} \cong 17.666, \overline{C_B} \cong 7.7286$$

$$\overline{C_1} \cong 1.9926, \overline{C_2} = 1$$

$$\overline{C_3} \cong 2.1116, \overline{C_4} = 2$$

$$\overline{C_1^{"}} \cong 6.3085$$

5 Final Design

C_{min} is chosen as 0.5pF => C=1

op amp: gain 70dB bandwidth 3 MHz

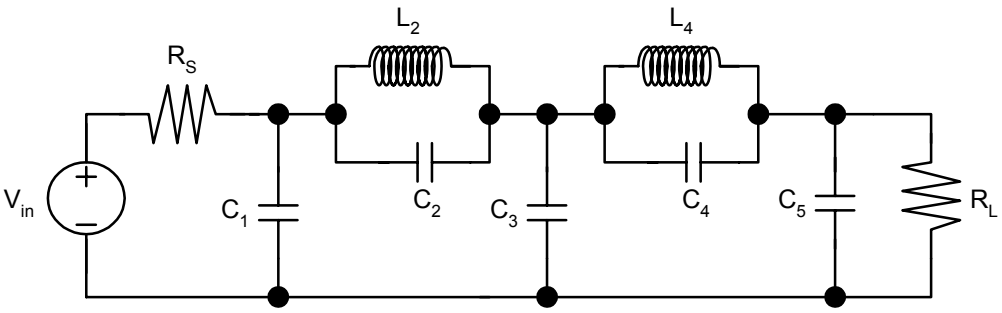
passband sensitivity to capacitance variation ≅ 0.2dB/1%

§14-12.2 Bilinear Ladder SCF Design

1. The same filter specification.

Elliptic ladder filter is chosen(fifth-order).

The result is



Normalized component values:

$Rs=R_L=1$ $C_1=0.85535$ $C_2=0.15367$ $L_2=1.20763$

$C_3=1.48438$ $C_4=0.46265$ $L_4=0.89794$ $C_5=0.63702$

$\hat{w}_{ap}=1$ rad/s

2. Frequency prewarping and denormalization

$$\omega_{ap} \cong \frac{2}{T}\tan\frac{\omega_p T}{2} = 2f_c \tan\frac{\pi f_p}{f_c} \cong 6291.4667 rad/s$$

Multiplying each resistor by z_0, each inductor by $L_0=z_0/\omega_{ap}$, and each capacitor by $C_0=1/z_0\ \omega_{ap}$.

Usually choose z_0=real source and termination resistance 50Ω 100Ω 600Ω

Here, $C_0=1$ is chosen => $z_0=\frac{1}{\omega_{ap}}$ and $L_0=\frac{1}{\omega_{ap}^2}$

We have the denormalized element values as:

$C_1=0.85535$, $C_2=0.15367$, $L_2=1.20763\times Lo=3.05090\times10^{-8}$,

$C_3=1.48438$, $C_4=0.46265$, $L_4=0.89794\times Lo=2.26851\times10^{-8}$,

$C_5=0.63702$, $Rs=R_L=z_0=1.58945\times10^{-4}$

3. SC realization

Using the exact design technique of SC ladder filter (Section 14-10), the state equations are

$$-V_1=-\frac{1}{sC'_1}\left(\frac{1}{R_S}(V_{in}-V_1)-I_2+sC'_2V_3\right),$$

$$-I_2=-\left(\frac{1}{sL_2}-sC_{L2}\right)(V_1-V_3),$$

$$V_3=\frac{1}{sC'_3}(-I_2-sC'_2V_1-sC_4'V_5+I_4),$$

$$I_4=(\frac{1}{sL_4}-sC_{L4})(V_3-V_5),$$

$$-V_5=\frac{-1}{sC'_5}(I_4+sC'_4V_3-\frac{V_5}{R_L}),$$

where

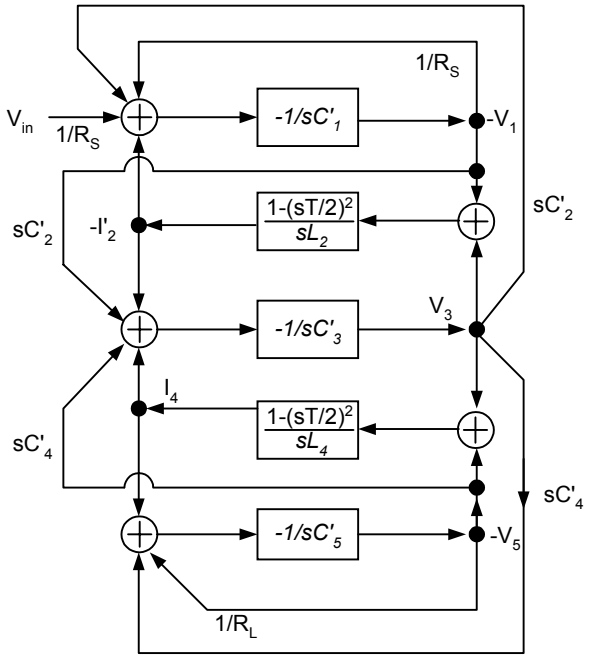
$$C_{L2}=\frac{T^2}{4L_2}=0.003278,$$

$C'_2=C_2+C_{L2}=0.15695,$
$C'_1=C_1+C'_2=1.01230,$

$$C_{L4}=\frac{T^2}{4L_4}=0.0044082,$$

$C'_4=C_4+C_{L4}=0.46706,$
$C'_3=C_3+C'_2+C'_4=2.10839,$
$C'_5=C_5+C'_4=1.10408.$

The signal flow diagram is:



SCF:

arbitrarily chosen

$C=C_{L2}=0.003278$ $C'=C_{L4}=0.004408$

$$C_S=\frac{T}{Rs}=0.1258293,$$

$$C_A=C_1+C_2+C_{L2}-\frac{C_s}{2}=0.94938,$$

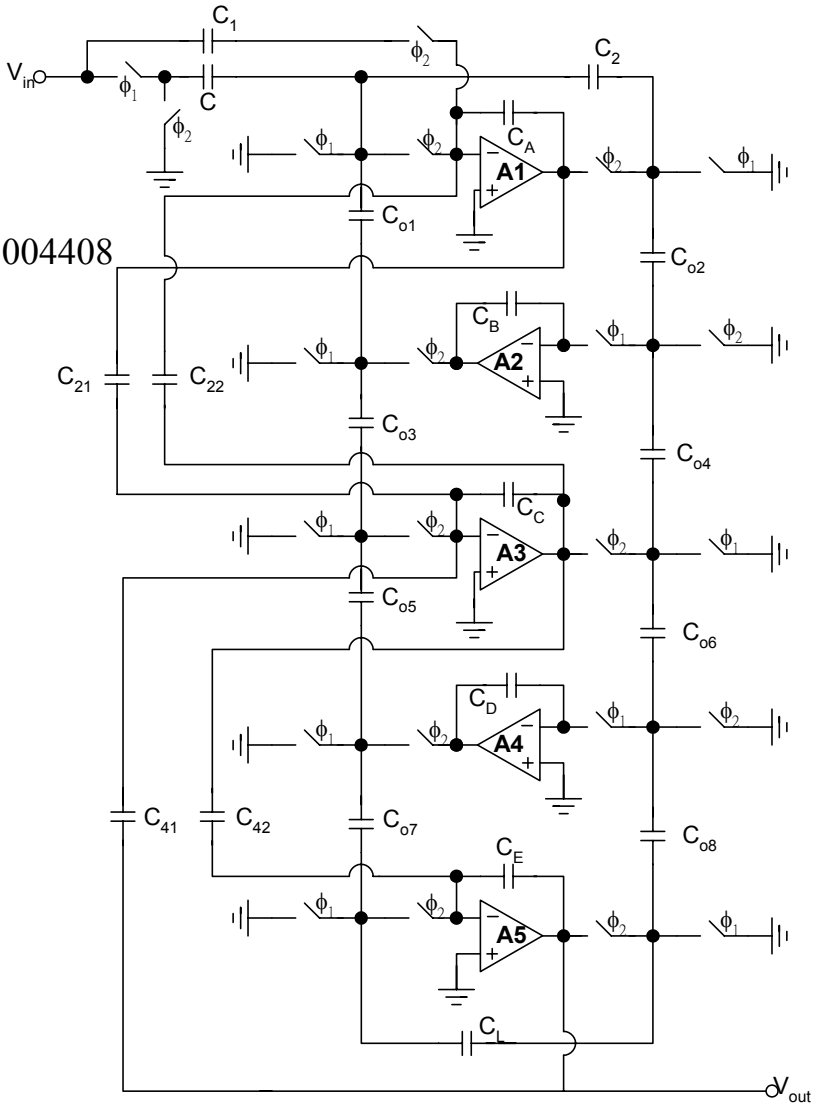
$$C_B=\frac{C^2}{4C_{L2}}=\frac{C_{L2}}{4}=0.0008195,$$

$C_c=C'_3=2.10839,$

$$C_D=\frac{C'^2}{4C_{L4}}=\frac{C_{L4}}{4}=0.001102,$$

$$C_E=C'_5-\frac{C_L}{2}=1.041165,$$

$$C_L=\frac{T}{R_L}=0.12583.$$



4.Scaling

V_{in}=1V, we have:

A_1: C_A,C_2,C_{21}, and C_{02} multiplied by Vp_1

A_2: C_3,C_{01}, and C_{03} multiplied by Vp_2

⋮

$V_{p1} \cong 0.92V$, $V_{p2} \cong 34V$, $V_{p3} \cong 0.764V$, $V_{p4} \cong 28.86V$, $V_{p5} \cong 0.5V$,

C_1=1.00000 C_2=1.83854 C_3=2.00000 C_A=13.87171 C_{01}=1.77112 C_{02}=1.20275 C_{03}=1.00000 C_{04}=1.00000 C_B=11.11901 Cc=14.46156

C_{05}=1.14172 C_{06}=1.52861 C_{07}=2.02212 C_{08}=1.00000 C_E=8.27441 C_D=14.43078 C_L=1.00000 C_{41}=2.09575 C_{42}=5.67396 C_{21}=1.29480 C_{22}=1.90667

for dynamic range scaling

minimum-capacitance scaling: $C_A \big/ C_s \big/ 2$ =13.87171

5.Final design

C_{min} , OP amp: 70dB 3 MHz

=>Passband ripple: 0.06dB minimum stopband loss $\cong 39.5dB$

Maximum sensitivity: $0.05dB \big/ \%$

§14-12.3 LDI Ladder SCF Design

1. LCR prototype circuit

Fifth-order elliptic LC ladder filter with the same lowpass specifications.

2. Frequency prewarping and denormalization

$\omega_{ap} \cong \omega_p$ (for simplicity)

z_0=1Ω => $C_0 = 1 \big/ (2\pi 10^3)$ F, $L_0 = \frac{1}{(2\pi 10^3)} H$

The denormalized element values:

R_s=1Ω,

C_1=136.13318μF, C_4=73.633034μF,

C_2=24.45734μF, L_4=142.91159μH,

L_2=192.20028μH, C_5=101.38488μH,

C_3=236.24641μF, R_L=1Ω.

State equations:

$$-V_1 = \frac{1}{s(C_1 + C_2)}\left(\frac{-V_1 + V_{in}}{Rs} + sC_2V_3 - I_2\right),$$

$$-I_2 = \frac{V_3 - V_1}{sL_2},$$

$$V_3 = -\frac{1}{s(C_2 + C_3 + C_4)}\left(-I_2 - sC_2V_1 - sC_4V_5 + I_4\right),$$

$$I_4 = \frac{V_3 - V_5}{sL_4},$$

$$-V_5 = -\frac{1}{s(C_4 + C_5)}\left(I_4 + sC_4V_3 - \frac{V_5}{R_L}\right).$$

3.SCF design

The flow diagram is shown on P.14-? whereas the active-RC circuit is given on P.14-?.

The SCF is shown on P.14-? where T=20μs is chosen and the component values are

$C_1+C_2=160.59\mu F$, $C_2+C_3+C_4=334.34\mu F$,

$C_S=\frac{T}{R_s}=20\mu F$, $C_4+C_5=175.018\mu F$,

$C=\frac{T}{1}=20\mu F$, $C_L=\frac{T}{R_L}=20\mu f$

4.Scaling

Dynamic range scaling with V_{pi} listed:

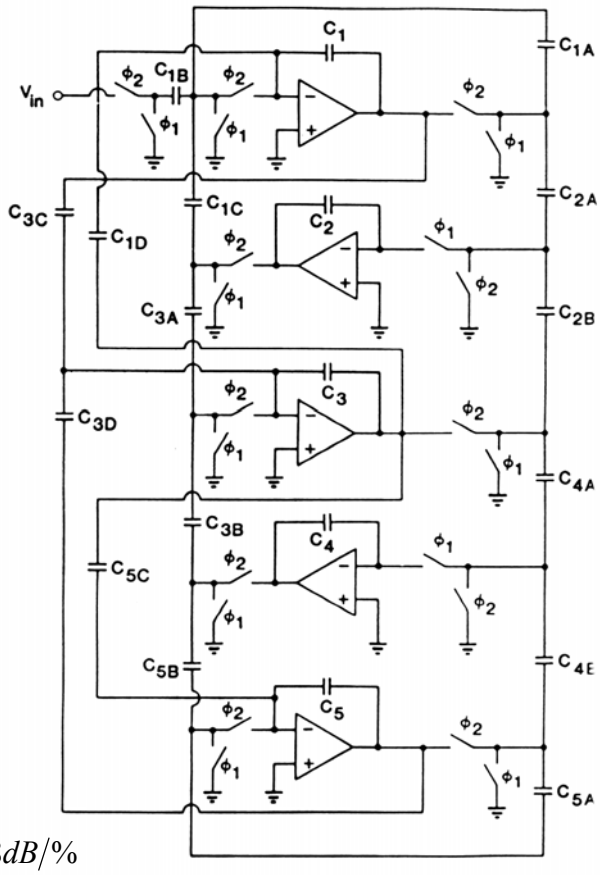
followed by minimum-capacitance scaling

for A_1:Vp_1=0.927 V at 1.182kHz.
for A_2:Vp_2=1.198 V at 1.121 kHz.
for A_3:Vp_3=0.857V at 1.061 kHz.
for A_4:Vp_4=1.105 V at 1.061 kHz.
for A_5:Vp_5=0.501 V at 967 kHz.

Element values:

C_1=8.03214, C_3=12.97271,
C_{1A}=1, C_{3A}=1.08390,
C_{1B}=1.07930, C_{3B}=1,
C_{1C}=1.29263, C_{3C}=1.02540,
C_{1D}=1.13212, C_{3D}=1.66885,
C_2=13.42236, C_4=15.76379,
C_{2A}=1.08053, C_{4A}=1.71203,
C_{2B}=1, C_{4B}=1,
C_5=8.75121,
C_{5A}=2.20614,
C_{5B}=1,
C_{5C}=6.29664.

SCF:



5.Final design

C_{min} Passband ripple: 0.095dB>0.044dB
Minimum stopband loss: 40.5dB
OP amp: 70dB, 3MHz

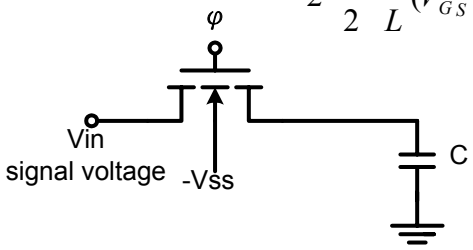
Maximum passband sensitivity: $0.08dB/\%$

§14-13 Nonideal Effects in Switched-Capacitor Filters

1. Switch Turn-On Resistance

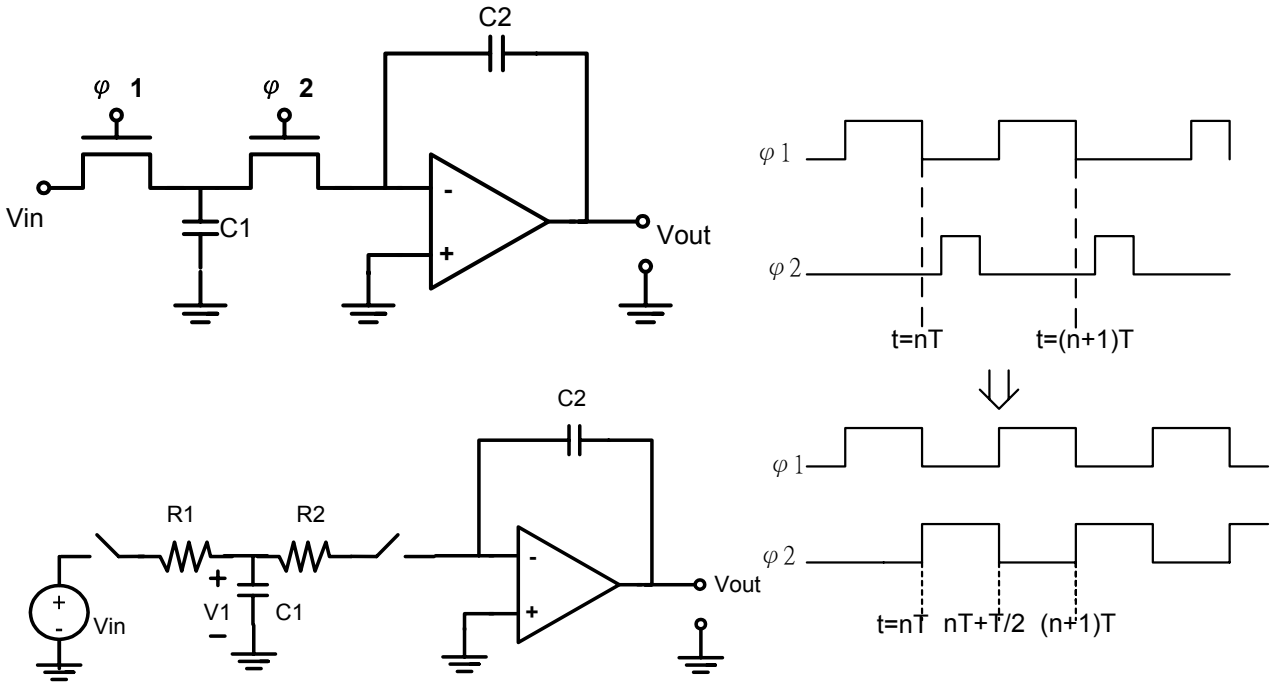
The turn-On resistance of a MOSFET can be written as

$$R_{on}=\frac{1}{2\frac{uc_o}{2}\frac{w}{L}(V_{GS}-V_T)}$$



* Nonlinear behavior

The R_{on} effect on the simple SC integrator:



At t=nT , $V_1(t)=V_1(nT)=V_{in}(nT)(1-e^{-T/2R_1C_1})$

Assume ϕ_1 and ϕ_2 are activated for $T/2$.

$$\Delta Q\left(nT+\frac{T}{2}\right)=C_1V_1(nT)(1-e^{-T/2R_2C_1})=[V_{out}(nT+T)-V_{out}(nT)]C_2$$

Let $R_1=R_2=R$

$$\Rightarrow H(z)=\frac{-(1-e^{-T/2RC_1})^2\,C_1/C_2}{z-1}$$

Ideal: $$H(z)=-\frac{C_1/C_2}{z-1}$$

Error: $\varepsilon=1-(1-e^{-T/2RC_1})^2 \cong 2e^{-T/2RC_1}$

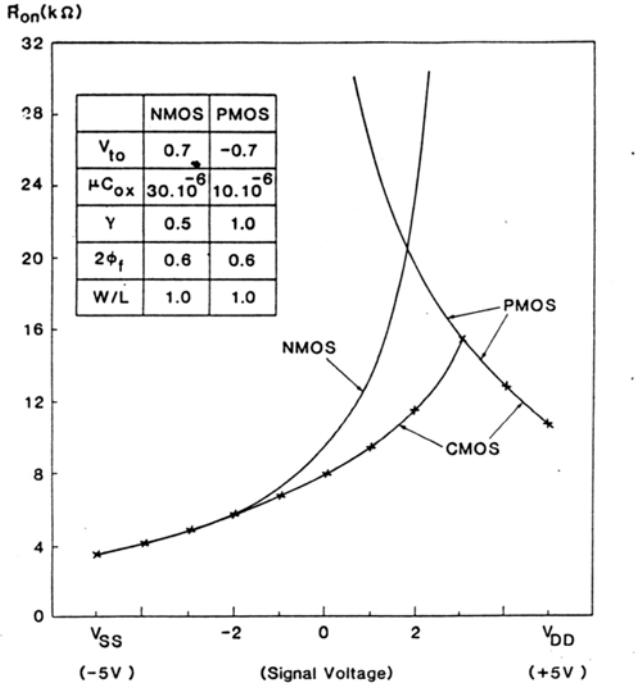
Usually $\varepsilon<0.1\%$(cap. ratio error) is acceptable.

$$2e^{-T/2RC_1} \le 10^{-4}$$

$$\Rightarrow \frac{RC_1}{T} = RC_1 f_c \le \frac{1}{2\ln 20000} \cong 0.05$$

$$\text{or } RC_1 \le \frac{T}{20} \left(= \frac{1}{20fc}\right)$$

f_c=500KHz, C_1=5pF $R \le 20K\Omega$; f_c=100MHz, C_1=2pF, $R \le 250\Omega$?

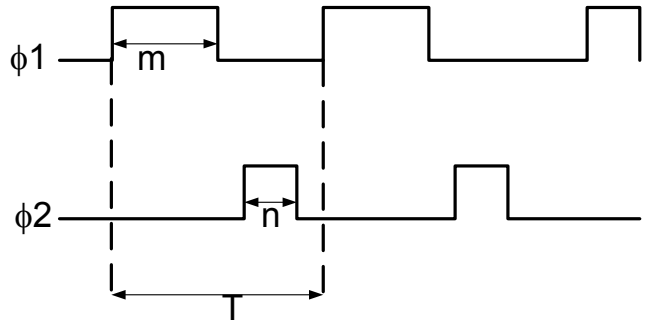


	NMOS	PMOS
V_{to}	0.7	-0.7
μC_{ox}	30.10^{-6}	10.10^{-6}
γ	0.5	1.0
$2\phi_f$	0.6	0.6
W/L	1.0	1.0

FIGURE 7.4. Variations in the small-signal ON resistance of several commonly used switch types vs changes in the voltage level v_{in} (from Ref. 6, © 1983 IEEE).

2.Clock Feedthrough Noise

* All switches directly connected to the integrating node generate clock feedthrough noises.



* All clock feedthrough noises are proportional to the sampling frequency. They may have a dc component.

* As soon as the clock feedthrough error voltage does not

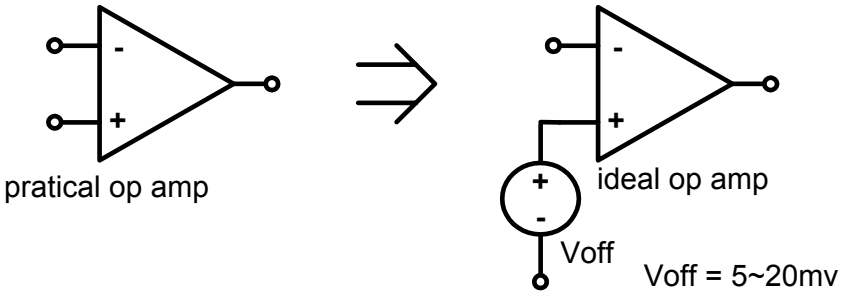
saturate the OP AMP, it can be eliminated at the output by reconstruction filters(LPF).

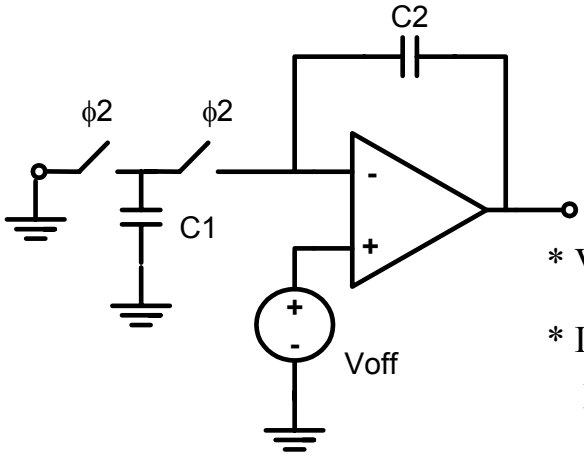
* The dc component cause offset voltage problems.

3.Junction Leakage

* Worst-case (100°C or 125°C) leakage at the integrating node: ~10 nA/mil^2 5μm×5μm junction => 400 pA leakage
* $f_{s,\,max}$ is about 25KHz in this case to avoid significant errors.
* The leakage cause dc offset voltages.

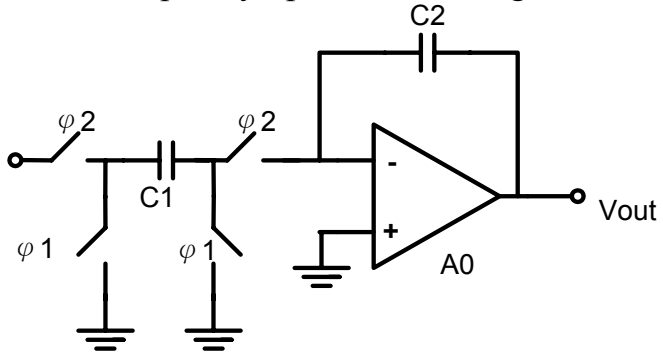
4. DC offset Voltage of the OP AMP





* $V_{out}=(1+\frac{C_1}{C_2})V_{off}$
* Integrator-based design may have a dc offset problem if no other negative feedback paths exist.
* Too-low-frequency operation is not good.

5. Finite Gain of the OP AMP.



$V_{out}(nT)=V_{c2}(nT)-\frac{1}{A_O}V_{out}(nT)$

$C_2[V_{c2}(nT)-V_{c2}(nT-T)]$

$+C_1[V_{in}(nT)+\frac{1}{A_O}V_{out}(nT)]=0$

$$=>H(z)=\frac{V_{out}(z)}{V_{in}(z)}=\frac{-(C_1/C_2)[1+(1+C_1/C_2)/A_O]^{-1}z}{z-(1+1/A_O)/[1+(1+C_1/C_2)/A_O]}$$

$$H(e^{j\omega T})=H_i(e^{j\omega T})\underbrace{\frac{1}{1+(1/A_O)(1+C_1/2C_2)-j(C_1/C_2)/2A_O\tan(\omega T/2)}}_{F(\omega)}$$

$$\downarrow$$

$$H_i(z)=\frac{-(C_1/C_2)}{z-1}$$

$$F(\omega)=\frac{1}{1-m(\omega)+j\theta(\omega)} \qquad m(\omega)=-\frac{1}{A_O}(1+\frac{C_1}{2C_2}) \qquad \theta(\omega)=\frac{C_1/C_2}{2A_o\tan(\omega T/2)}$$

$$\cong\frac{C_1/C_2}{A_o\omega T}$$

$$|F(\omega)|=\frac{1}{\sqrt{(1-m)^2+\theta^2}} \cong \frac{1}{1-m} \cong 1+m \longrightarrow \text{relative magnitude error}$$

($\theta<<1$)

$$\angle F(\omega)=-\tan^{-1}\frac{-\theta}{1-m} \cong \tan^{-1}\theta \cong \theta \longrightarrow \text{relative phase error}$$

($m<<1$, $\theta<<1$)

$\underbrace{\omega T<<1 \text{ , } A_o>1000}$, C_1/C_2 normal value.

$A_o\omega T>>1$ $\qquad$ Ao>1000=>0.1%

$$\omega>>\frac{1}{A_oT}=\frac{f_s}{A_o}$$ $\qquad$ Ao>100=>1%

=> m and θ are very small. $\longrightarrow$ <0.1%

But for $\omega<2/A_oT$, θ is large.

6. Finite Bandwidth of the OP AMP.

$$A(s)=\frac{-1}{1/A_o+S/\omega_o}$$ single-pole response

Similarly

$$m(\omega)=-e^{-k1}[1-K\cos\omega T] \qquad k=\frac{C_2}{C_1+C_2}$$

$$\theta(\omega)=-e^{-k1}K\sin\omega T \qquad k1\equiv K\ woT/2$$

If $\omega_oT/2=\pi\omega_o/\omega_c>>1$ => $m\rightarrow 0$, $\theta\rightarrow 0$.

** $\omega_o\cong 5\omega_c$ is adequate.

* The unity-gain bandwidth ω_o of the OP AMP should be (at least) five times as large as the clock frequency ω_c.

ω_o vs ω_c:

(1) Given ω_o, ω_c should be chosen low enough so that the OP AMPs have enough time to settle.

But ω_c should not be too low, or the noise aliasing effect becomes serious the antialiasing and smoothing filters must be too selective and too complex.

(2) Given ω_c, ω_o should be just high enough to assure that the stage can settle within each clock phase. Any higher value worsens unnecessarily the noise aliasing effect, and raises the dc power and chip area requirements of the op-amps.

(3) A_o=1000 (60dB), f_o=10MHz, f_{p1}=10KHz

choose f_c=2MHz, and f<40 KHz

Typically $f/f_c \cong 48$ i.e. $\omega_o T \fallingdotseq \frac{1}{4}$

7. Finite Slew Rate of the OP AMP

* The output voltage of the OP AMP must be settled down with the clock active duration.

$t_{slew} + t_{settle} < T_2$

* May cause nonlinear distortion.

8. Nonzero OP AMP Output Resistance

$$2R_o\left(\frac{C_1C_2}{C_1+C_2}+C_L\right) \cong T_1 < \frac{1}{7}T_{\Phi 2=1}$$

C_2: feedback cap ; C_1:input cap; C_L: load cap.

9. Overall considerations:

For an integrator settling error of 0.1% or less, we must have

$A_o \geq 5000$

$\omega_o/\omega_c \geq 4$

$T/R_{on}C_1 \geq 40$

10. Noise Generated in SC Circuits

(1) Clock feedthrough noise

(2) Noise coupled directly or capacitive from the power, clock, ground lines, and from the substrate.

(3) Thermal and flicker ($1/f$) noise generated in the switches and op-amps.

Thermal and flicker ($1/f$) noise:

* Internal sampling and holding=>If $1/f$ noise has no aliasing=>It can be eliminated.
* Thermal noise will be sampled and held with the OP AMP as a frequency limiting element.=> $\omega_o >> \omega_c$ is not suitable.
* The circuit noise ↓ if the circuit cap. ↑

CH 15. Continuous-Time Filters in CMOS

§15-1 Categories of continuous-time filter ICs

Amplifier Types		Continuous-Time Filter Types
Voltage OP AMP A_V	O	(Voltage-mode) Active RC filters
Current OP AMP A_I	Δ	(Current-mode) Active RC filters
Finite-gain voltage amp	Δ	(Voltage-mode) Active RC filters
Finite-gain current amp.	•	(Current-mode) Active RC filters
Infinite-gain Operational Transconductance Amp. (OTA) G_m		×
Finite-gain OTA or g_m amplifier	O	(Voltage-mode) G_m-C filters
Infinite-gain Operational Transimpedance Amp. R_m		×
Finite-gain Transimpedance Amp. or R_m amplifier	Δ	(Current-mode) R_m-C filters
Mixed G_m and R_m Amplifiers		?
Mixed A_V, A_I, G_m, and R_m Amplifiers		?
RF amplifier	Δ	Integrated LC filters

O : well developed
Δ : less developed but with great potential
• : much less developed
× : not explored
? : to be developed with potential

Common characteristics of continuous-time filters:

1. Not parasitic free
   =>Greater tolerance in performance.
2. No switches or clocks
   =>Lower noise (clock-induced) or simpler circuit.
3. Need tuning to accommodate the process variations on filter characteristics if high accuracy is required.
   =>Extra overhead and higher cost.
   =>Might not be needed if process-independent design is used and reasonable tolerance is allowed.

4. Could achieve higher-frequency operation in the VHF or UHF range if finite-gain amplifiers are used.
5. Could achieve GHz operation if deep submicron CMOS is used.

§15-2 Gm-C or OTA-C (Operational-Transconductance-Amplifier-C)

Filters

§15-2.1 Transconductor or OTA characteristics

Ideal characteristics:

$g_m=hI_{ABC}$ or $h'V_{ABC}$

$I_o=g_m(V^+-V^-)$

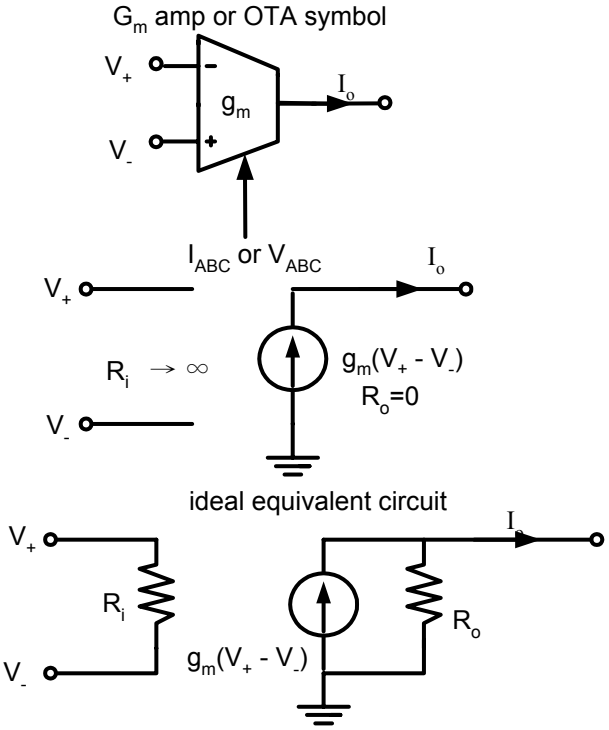
$R_i\rightarrow\infty$, $R_o=0$

h(h') is a constant.

Nonideal characteristics:

g_m is not linearly proportional to I_{ABC} or V_{ABC}.

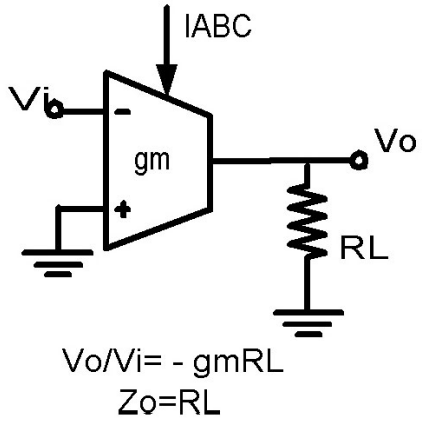
R_i and R_o are finite.



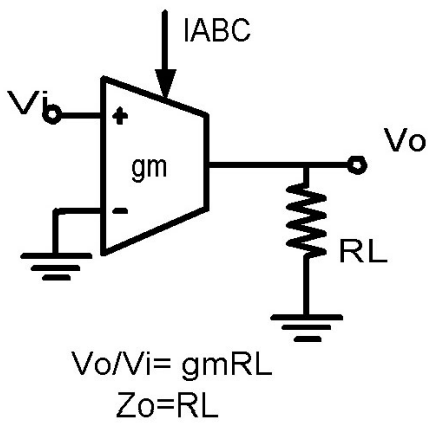
§15-2.2 Basic OTA building blocks

Ref.: IEEE Circuits and Device Magazine, pp.20-32, March 1985.

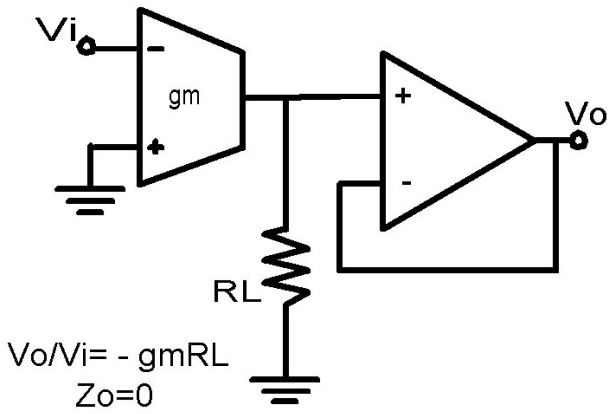
1. Voltage amplifiers G_m or op amp + resistors.



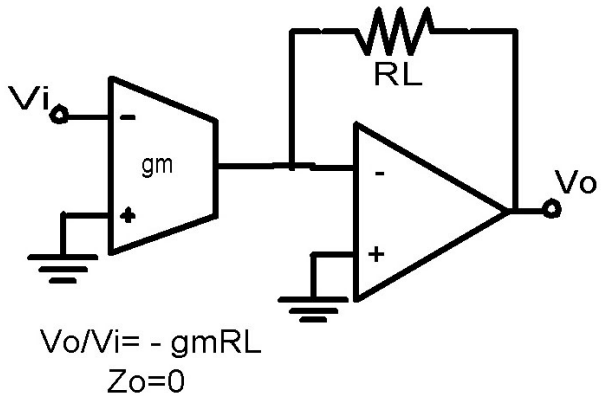
(a) Basic inverting



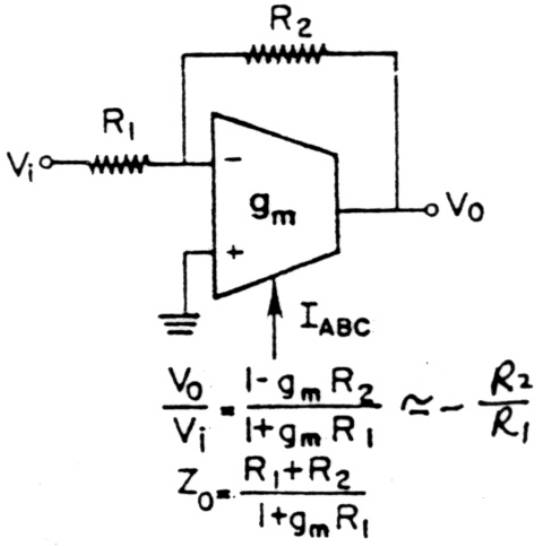
(b) Basic noninverting



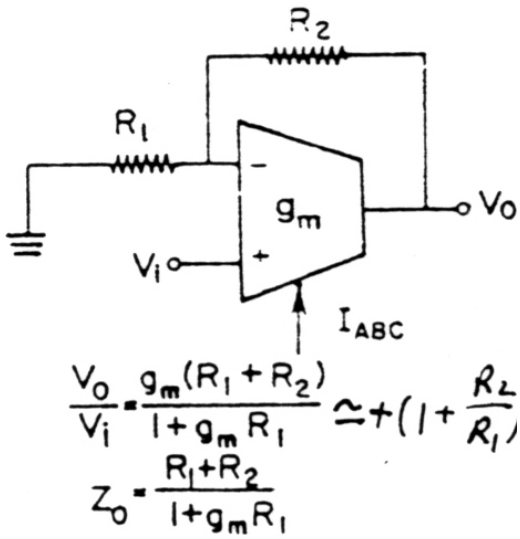
(c) Feedback amplifier



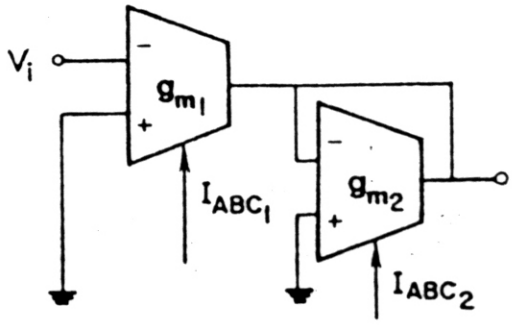
(d) Noninverting feedback amplifier



(e) Buffered amplifier



(f) Buffered VCVC feedback

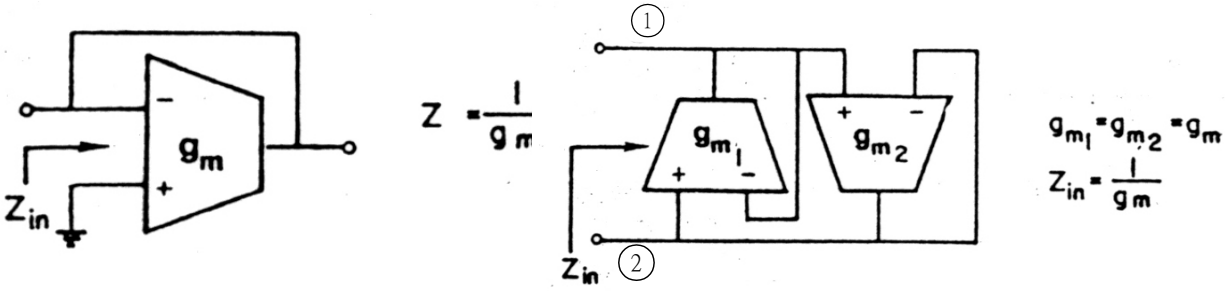


$$\frac{V_o}{V_i} = -\frac{g_{m1}}{g_{m2}}$$

$$Z_o = \frac{1}{g_{m2}}$$

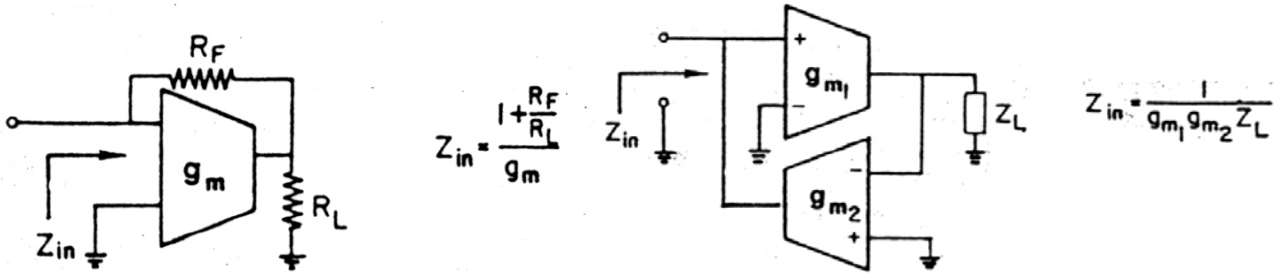
(g) All OTA amplifiers

2.Controlled impedance elements



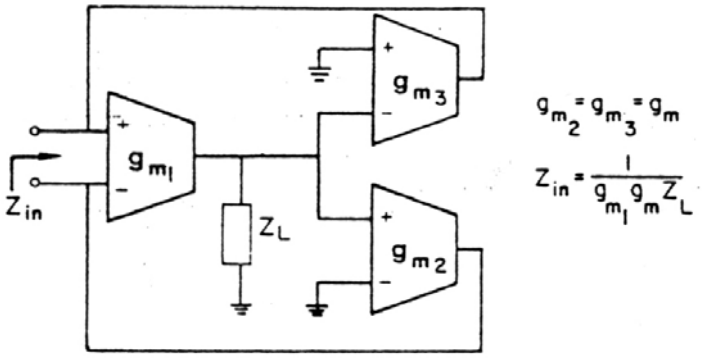
(a) Single-ended voltage variable resistor (VVR)

(b) Floating VVR

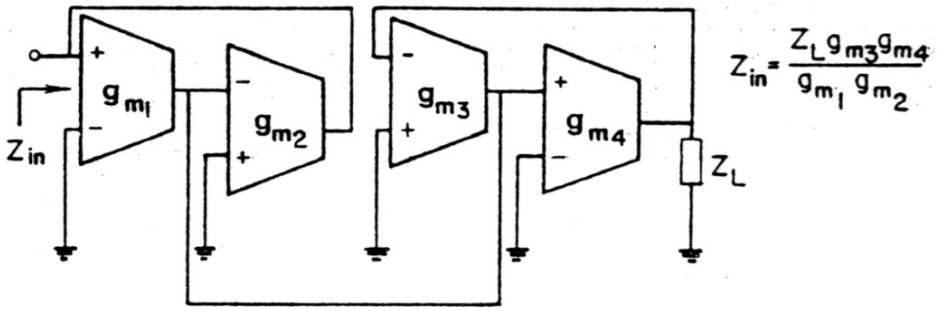


(c) Scaled VVR

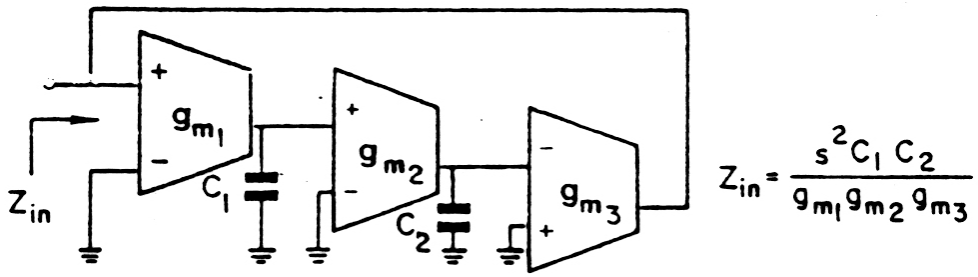
(d) Voltage variable impedance inverter



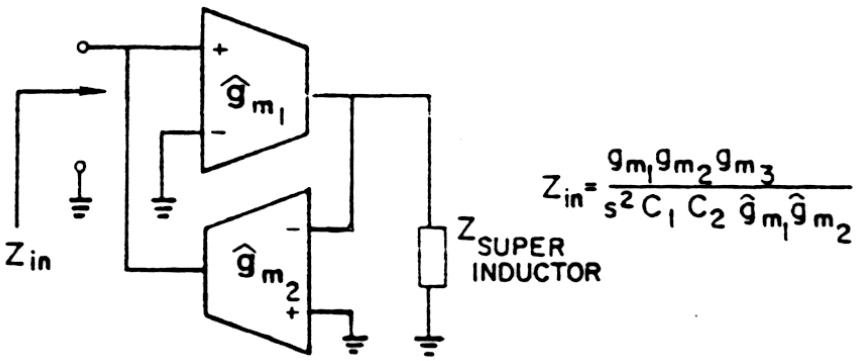
(e) Voltage variable floating impedance



(f) Impedance multiplier



(f) Super inductor



(f) FDNR

(d) Variable Impedance Inverter (VIC) or Gyrator

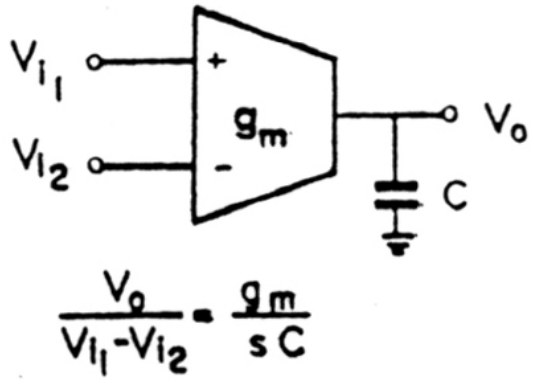
* Z_L is a capacitor=> Z_{in} is a inductor=>active inductor.
* Can be used in voltage-controlled oscillator (VCO)

(h) FDNR (Frequency Dependent Negative Resistance)

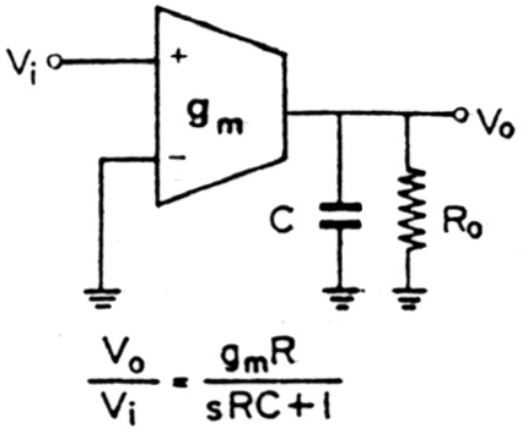
S=jω $Z_{in}(j\omega) = -\frac{R}{\omega^2}$

* Gyrator +super inductor.

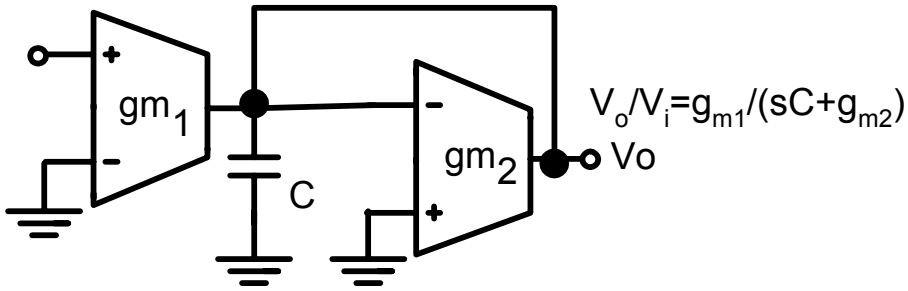
3. Integrators G_m or OTA + R or C



(a) Simple



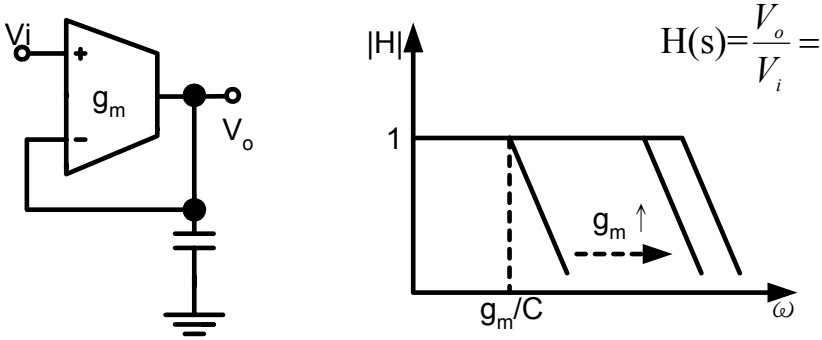
(b) Lossy



(b) Adjustable

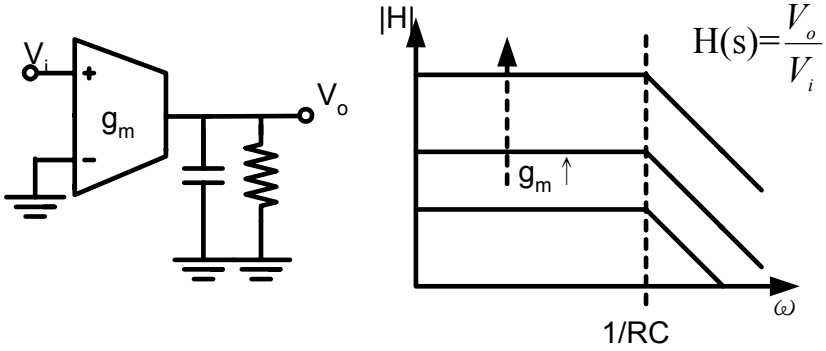
§15-2.3 Gm-C or OTA-C filters (first-order)

(a) First-order lowpass voltage-controlled filter, fixed dc gain, pole adjustable



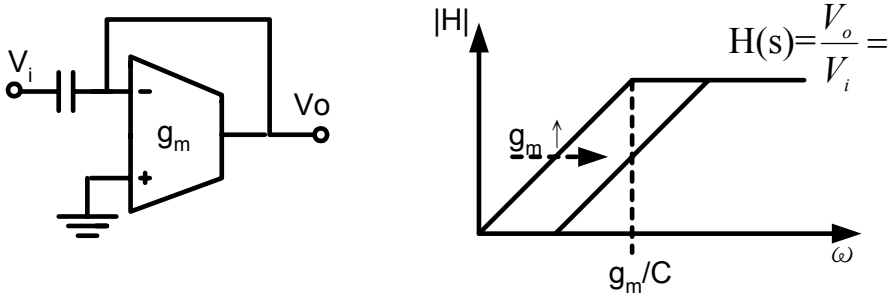
$$H(s)=\frac{V_o}{V_i}=\frac{g_m}{sc+g_m}$$

(b) Lowpass, fixed pole, adjustable dc gain



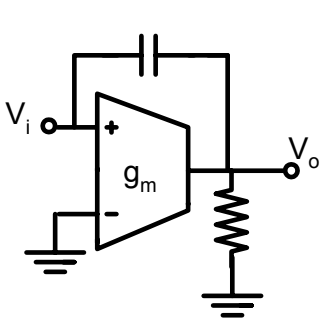
$$H(s)=\frac{V_o}{V_i}=\frac{g_m}{sc+\frac{1}{R}}$$

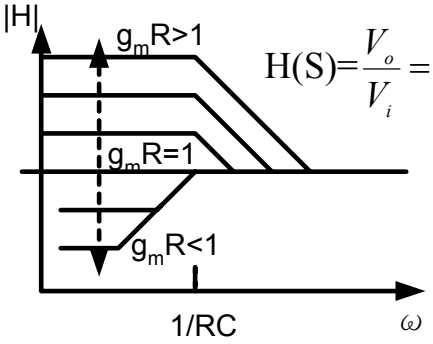
(c) Highpass, fixed high-frequency gain, adjustable pole



$$H(s)=\frac{V_o}{V_i}=\frac{sc}{sc+g_m}$$

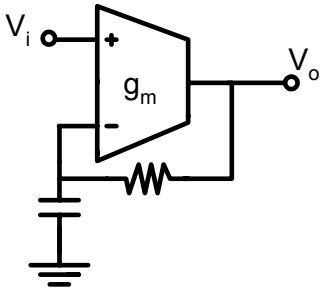
(d) Shelving equalizer, fixed high-frequency gain, fixed pole, adjustable zero

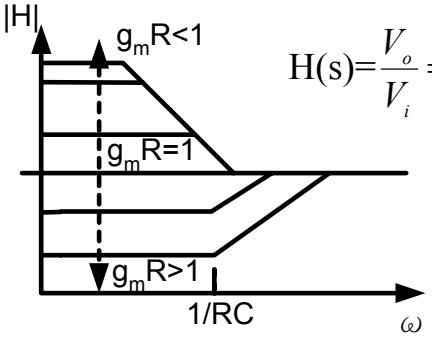




$$H(S)=\frac{V_o}{V_i}=\frac{R(sc+g_m)}{sRC+1}$$

(e) Shelving equalizer, fixed high-frequency gain, fixed zero, adjustable pole

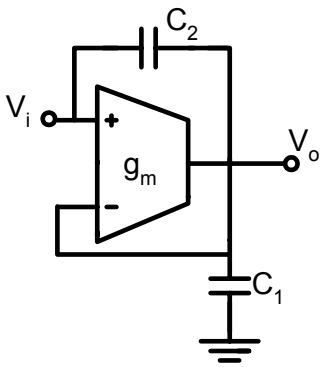


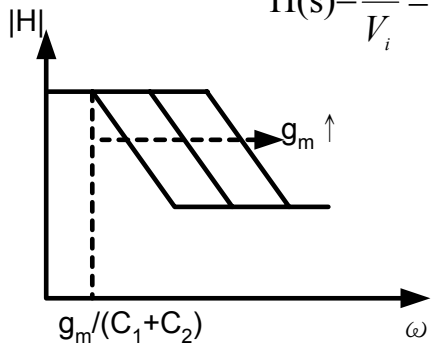


$$H(s)=\frac{V_o}{V_i}=\frac{g_m(1+sRC)}{sc+g_m}$$

(f) Lowpass filter, adjustable pole and zero

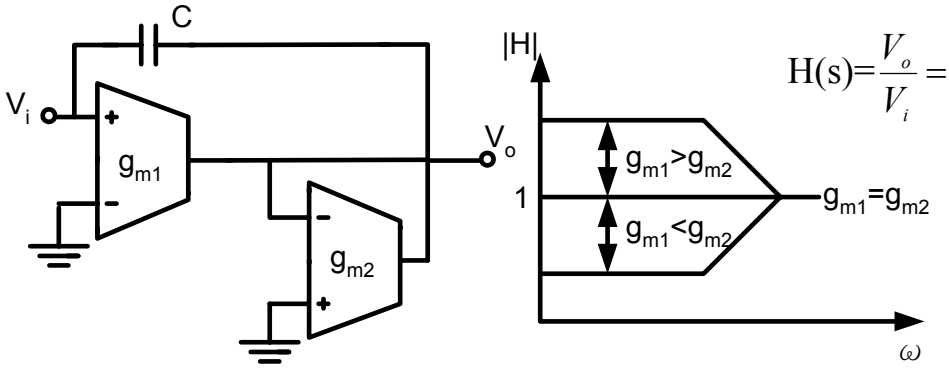
$$H(s)=\frac{V_o}{V_i}=\frac{sc_2+g_m}{s(c_1+c_2)g_m}$$



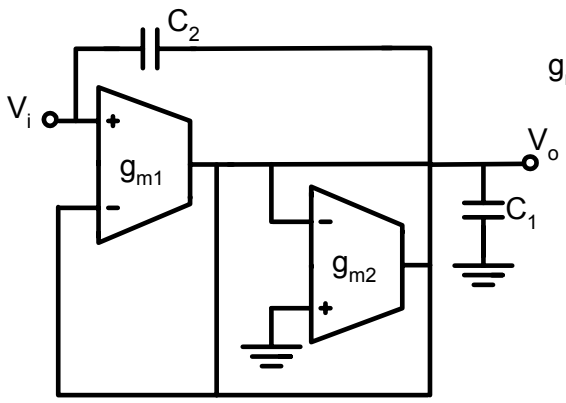


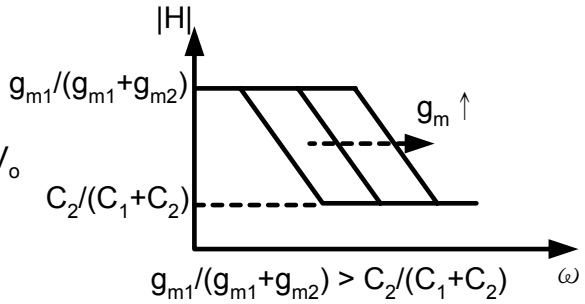
(g) Shelving equalizer, independently adjustable pole and zero

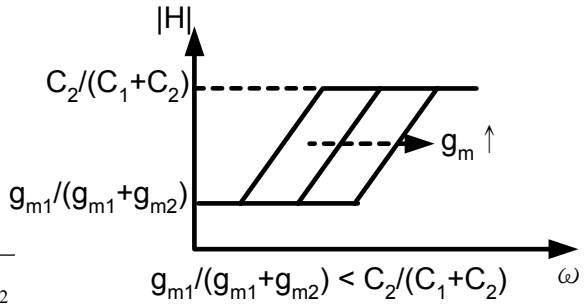
$$H(s)=\frac{V_o}{V_i}=\frac{sC+g_{m1}}{sC+g_{m2}}$$



(h) Lowpass or highpass filter, adjustable zero and pole, fixed ratio or independent adjustment

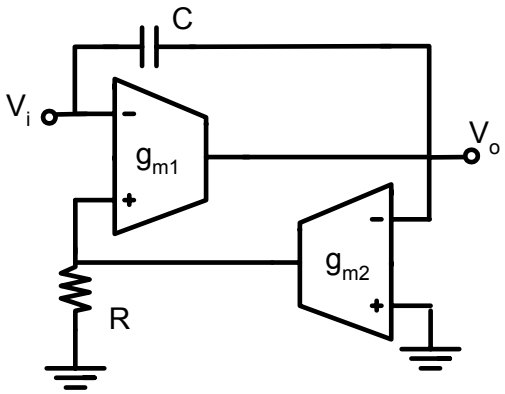




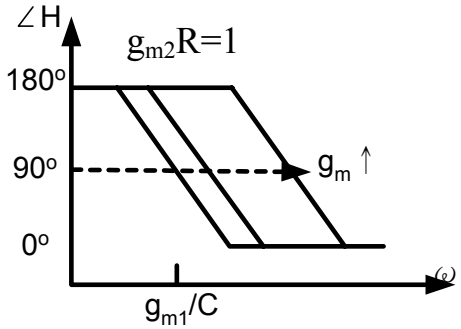


$$H(s)=\frac{V_o}{V_i}=\frac{g_{m1}+sC_2}{s(C_1+C_2)+g_{m1}+g_{m2}}$$

(i) Phase shifter, adjustable with g_m

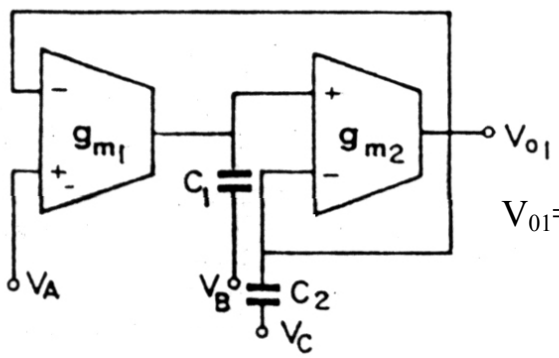


$$H(s)=\frac{V_o}{V_i}=\frac{sC-g_{m1}}{sC+g_{m1}g_{m2}R}$$



§15-2.4 Second-order Gm-Cor OTA-C filters

(a)

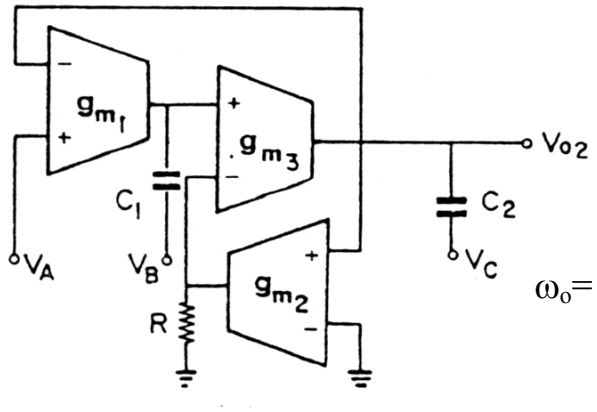


$$V_{01}=\frac{S^2C_1C_2V_C+SC_1g_{m2}V_B+g_{m1}g_{m2}V_A}{S^2C_1C_2+SC_1g_{m2}+g_{m1}g_{m2}}$$

Transfer functions for the biquadratic structure (a)

Circuit Type	Input Conditions	Transfer Function	If $g_{m1}=g_{m2}=g_m$	
			ω_o	Q (fixed)
ω_o Adjustable Lowpass	$V_i=V_A$ V_B and V_C Grounded	$\frac{g_{m1}g_{m2}}{s^2C_1C_2+sC_1g_{m2}+g_{m1}g_{m2}}$	$\frac{g_m}{\sqrt{C_1C_2}}$	$\sqrt{\frac{C2}{C1}}$
ω_o Adjustable Bandpass	$V_i=V_B$ V_A and V_C Grounded	$\frac{sc_1g_{m2}}{s^2C_1C_2+sC_1g_{m2}+g_{m1}g_{m2}}$	$\frac{g_m}{\sqrt{C_1C_2}}$	$\sqrt{\frac{C2}{C1}}$
ω_o Adjustable Highpass	$V_i=V_C$ V_A and V_B Grounded	$\frac{s^2C_1C_2}{s^2C_1C_2+sC_1g_{m2}+g_{m1}g_{m2}}$	$\frac{g_m}{\sqrt{C_1C_2}}$	$\sqrt{\frac{C2}{C1}}$
ω_o Adjustable Notch	$V_i=V_A=V_C$ V_B Grounded	$\frac{s^2C_1C_2+g_{m1}g_{m2}}{s^2C_1C_2+sC_1g_{m2}+g_{m1}g_{m2}}$	$\frac{g_m}{\sqrt{C_1C_2}}$	$\sqrt{\frac{C2}{C1}}$

(b)



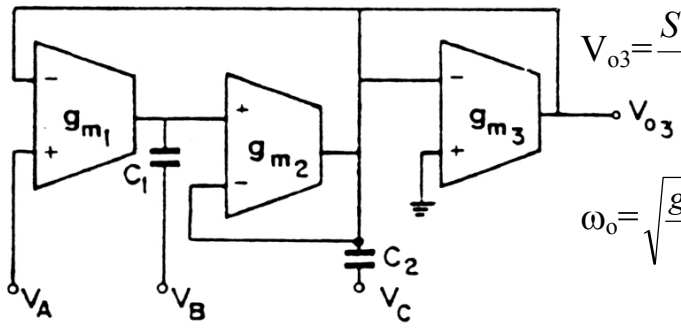
$$\omega_o=\sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}},\quad Q=\frac{1}{g_{m3}R}\sqrt{\frac{C_2g_{m1}}{C_1g_{m2}}}$$

* Can implement lowpass, bandpass, highpass, and notch.

* If g_{m3} is fixed and $g_{m1}=g_{m2}=g_m$ is adjusted, the poles can be moved in a constant-Q manner.

* If g_{m3} is adjusted with g_{m1} and g_{m2} fixed, the pole movement in a constant-ω_0 manner.

(c)

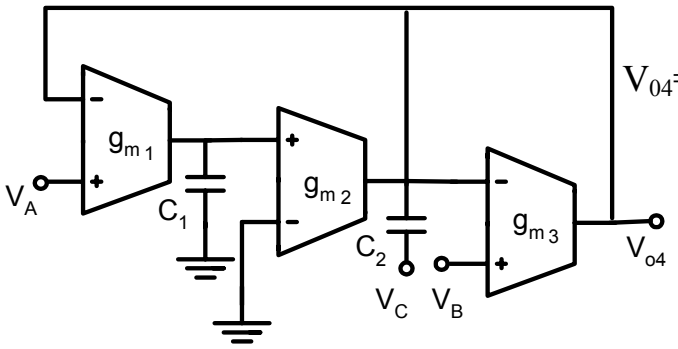


$$V_{o3}=\frac{S^2C_1C_2V_c+SC_1g_{m2}V_B+g_{m2}g_{m1}V_A}{S^2C_1C_2+Sg_{m3}C_1+g_{m1}g_{m2}}$$

$$\omega_o=\sqrt{\frac{g_{m1}g_{m2}}{C_1C_2}},\ Q=\left(\sqrt{\frac{C_2}{C_1}}\right)\sqrt{\frac{g_{m1}g_{m2}}{g_{m3}}}$$

* ω_o can be adjusted linearly with $g_{m1}=g_{m2}=g_m$ and g_{m3} constant
  => constant-bandwidth movement.
* If g_{m1}, g_{m2}, and g_{m3} are adjusted simultaneously, constant-Q pole movement.
* Interchanging "+" and "-" terminals of g_{m1} and g_{m2} and setting $V_A=V_B=V_C=V_i$, and making $g_{m1}=g_{m2}=g_{m3}=g_m$ => 2^{nd}-order g_m adjustable phase equalizer.

(d)

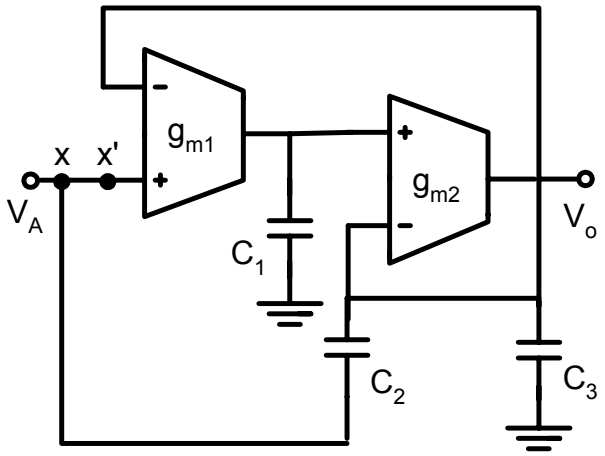


$$V_{04}=\frac{V_c C_1 C_2 S^2 + V_B g_{m3} s C_1 + g_{m1} g_{m2} V_A}{S^2 C_1 C_2 + S C_1 g_{m3} + g_{m1} g_{m2}}$$

$$\omega_o=\sqrt{\frac{g_{m1} g_{m2}}{C_1 C_2}},\quad Q=\frac{1}{g_{m3}}\sqrt{\frac{g_{m1} g_{m2} C_2}{C_1}}$$

* The adjustment of the bandpass version with $g_{m1}=g_{m2}=g_m$ will result in a constant bandwidth, constant gain response.

(e) Elliptic biquadratic filter

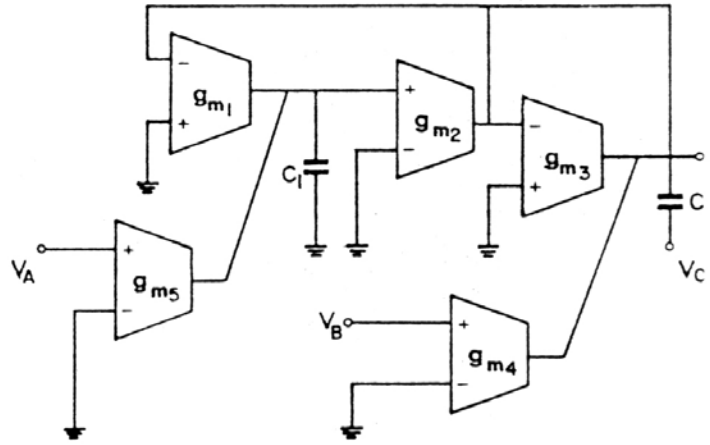


$$H(s)=\frac{V_o}{V_i}=\left(\frac{C_2}{C_2+C_3}\right)\left(\frac{S^2+g_{m1}/C_1C_2}{S^2+Sg_{m2}/(C_2+C_3)+g_{m1}g_{m2}/C_1(C_2+C_3)}\right)$$

* Can be applied to the realization of high-order voltage-controlled elliptic filters.
  =>Cascading these second-order blocks with interstage unity-gain buffers.
  All g_m's are made equal and adjusted simultaneously.
* The voltage-controlled amplifier of Fig. (g) on p.15-3 can be inserted between x and x'. The transconductance gain of the two OTAs in the

amplifier can be used as the control variable to adjust the ratio of the zero location to pole location.

(g) General biquadratic structure

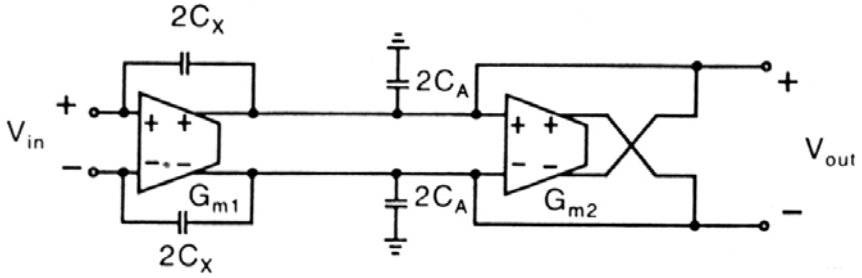


$$V_o=\frac{S^2C_1C_2V_c+SC_1g_{m4}V_B+g_{m2}g_{m5}V_A}{S^2C_1C_2+SC_1g_{m3}+g_{m2}g_{m1}}$$

* when $V_i=V_A=V_B=V_C$, the ω_o and Q for the poles and zeros can be adjusted by g_m's to any desired value.

§15-2.5 Fully Differential Gm-C or OTA-C Filters

1. General first-order filter

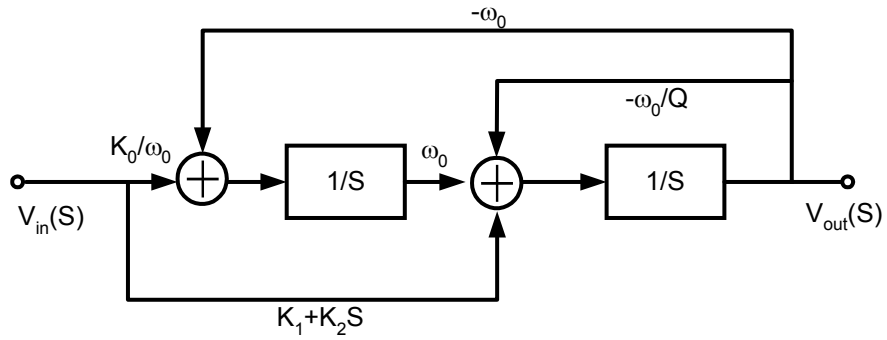


$$H(s)=\frac{V_{out}}{V_{in}}=\frac{K_1S+K_o}{S+\omega_o}$$

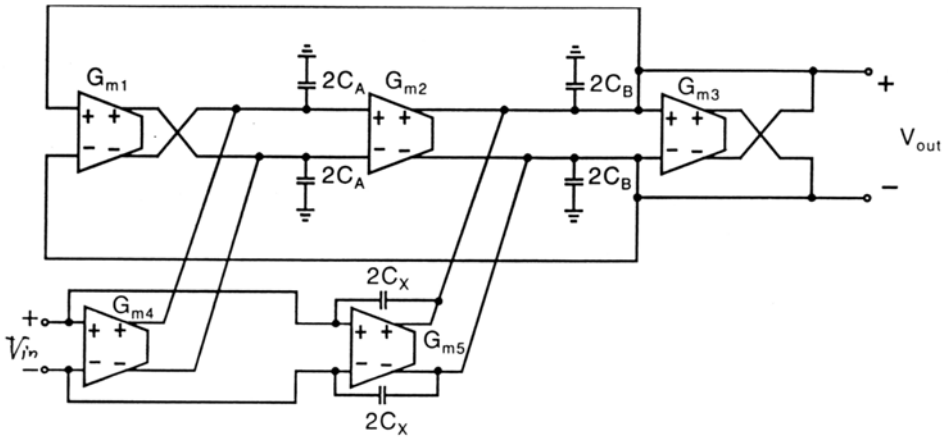
$$H(s)=\frac{SCx+G_{m1}}{S(C_A+C_X)+G_{m2}}=\frac{S(\frac{Cx}{C_A+Cx})+\frac{G_{m1}}{C_A+Cx}}{S+\frac{G_{m2}}{C_A+C_X}}$$

$$=>C_x=(\frac{K_1}{1-K_1})C_A,\ \ G_{m1}=K_o(C_A+C_X),\ G_{m2}=\omega_0(C_A+C_X)$$

2. General biquadratic filter



$$H(s)=\frac{V_{out}(s)}{V_{in}(s)}=\frac{K_2S^2+K_1S+K_o}{S^2+(\frac{\omega_o}{Q})S+\omega_o{}^2}$$



$$H(s)=\frac{V_{out}(s)}{V_{in}(s)}=\frac{S^2(\frac{G_X}{C_X+C_B})+S(\frac{G_{ms}}{C_X+C_B})+\frac{G_{m2}G_{m4}}{C_A(C_X+C_B)}}{S^2+S(\frac{G_{m3}}{C_X+C_B})+\frac{G_{m1}G_{m2}}{C_A(C_X+C_B)}}$$

Design equations: $C_X=C_B(\frac{K_2}{1-K_2})$ where $0\le K_2<1$

$G_{m1}=\omega_oC_A$

$G_{m2}=\omega_o(C_B+C_X)$

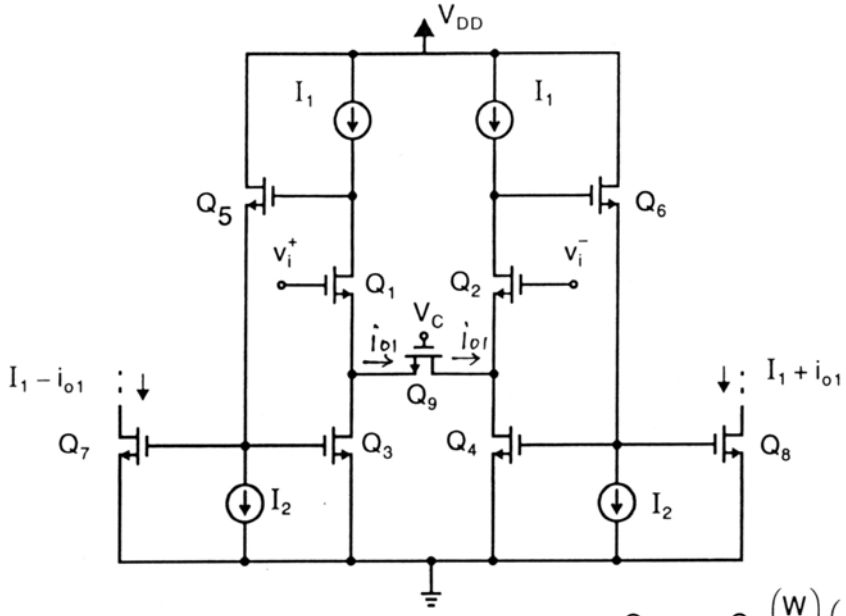
$$G_{m3}=\frac{\omega_o(C_B+C_X)}{Q}$$

$G_{m4}=(K_oC_A)/\omega_o$

$G_{m5}=K_1(C_B+C_X)$

§15-3 CMOS Transconductor or OTA

1. CMOS transconductor using triode transistor



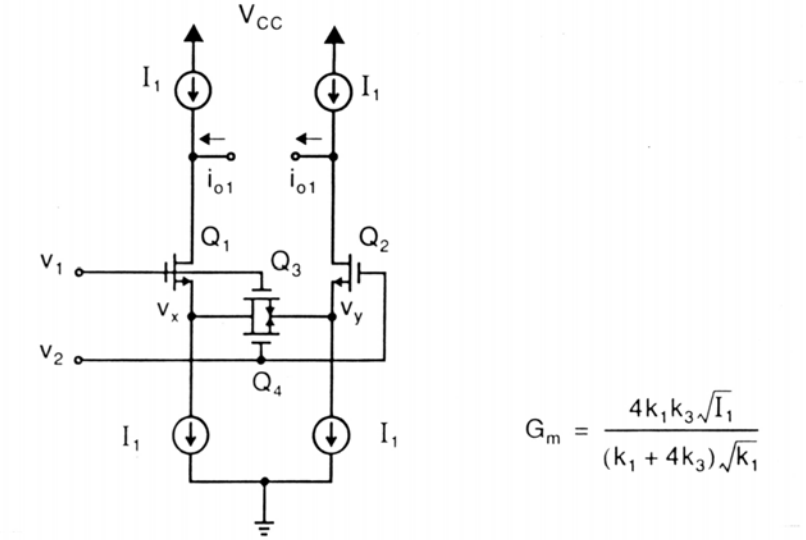
$$G_m = \mu_n C_{ox}\left(\frac{W}{L}\right)_9\left(v_{gs9} - V_{tn}\right)$$

* Q_9: operated in the triode region.

* G_m can be adjusted by V_{gs9} and scaled by the current mirrors Q_3/Q_7 and Q_4/Q_8.

* Q_5/Q_6 are feedback devices to set the drain voltages of Q_1/Q_2.

2. CMOS transconductor using varying bias-triode transistors.



$$G_m = \frac{4k_1k_3\sqrt{I_1}}{(k_1 + 4k_3)\sqrt{k_1}}$$

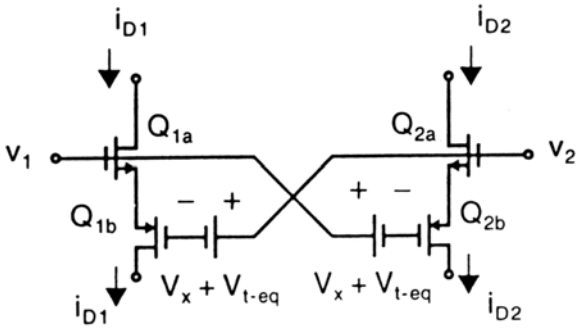
* Q_3 and Q_4 are in the triode region.

* $G_m = \dfrac{1}{r_{s1} + r_{s2} + (r_{ds3} \,||\, r_{ds4})}$ where $r_{ds3}=r_{ds4}=\dfrac{1}{2K_3(V_{GS1} - V_{tn})}$

$$r_{s1}=r_{s2}=\frac{1}{g_{m1}} = \frac{1}{2K_1(V_{GS1} - V_{tn})} \quad V_{GS1}-V_{tn}=\sqrt{\frac{I_1}{K_1}}$$

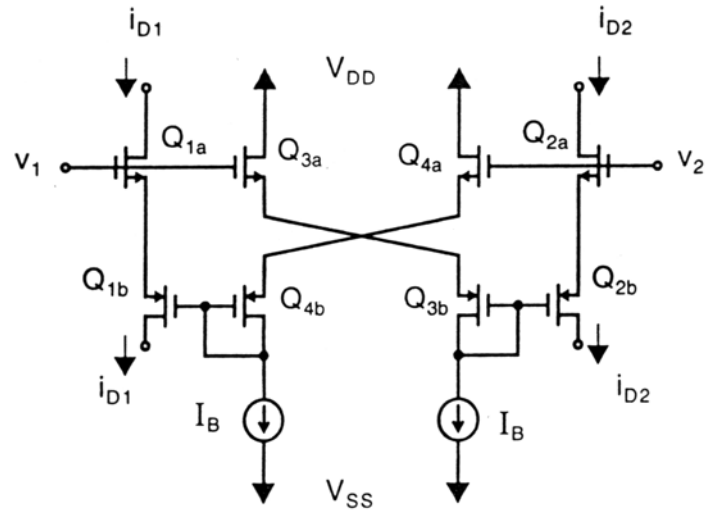
3. CMOS differential-pair transconductor with floating voltage supply.

Conceptual circuit:



$$(i_{D1} - i_{D2}) = 4K_{eq}V_x(v_1 - v_2)$$

Real circuit:

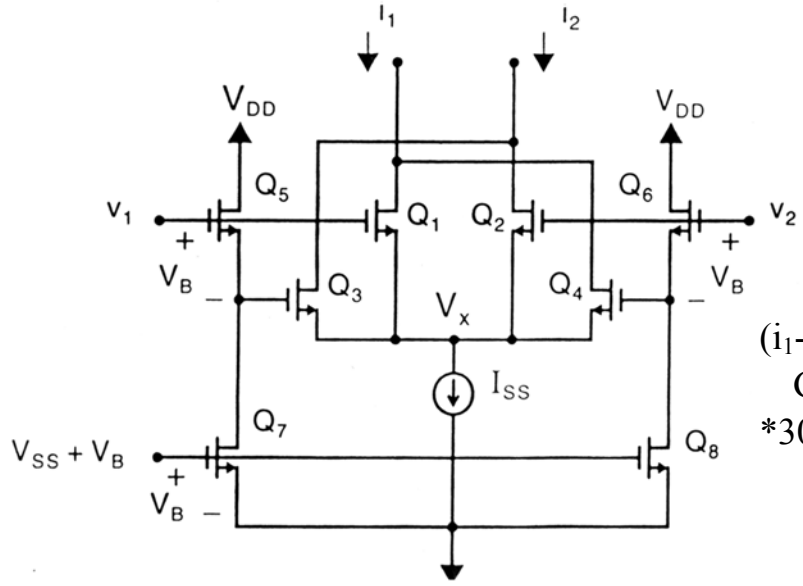


$(i_{D1}\text{-}i_{D2})=4\sqrt{K_{eq}I_B}(V_1 - V_2)$

$G_m=4\sqrt{K_{eq}I_B}$

* 30~50 dB linearity.

4. CMOS bias-offset cross-coupled transconductor.



$(i_1\text{-}i_2)=2KV_B(V_1\text{-}V_2)$

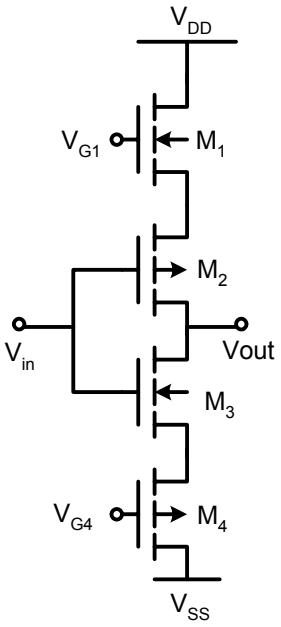
$G_m=2KV_B$

*30~50dB linearity

§15-4 Design Example of Gm-C or OTA-C Filters

Ref.: 1. IEEE Trans. Circuits and Systems, pp. 1132-1138, Nov. 1986
2. IEEE JSSC, pp.987-996, Aug. 1988

1. CMOS linear transconductance amplifier (CMOS inverter-based complementary differential-pair transconductor)



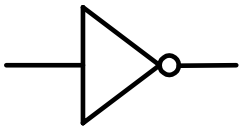
$g_m=2k_{eff}\,(V_{G1}+|V_{G4}|-\Sigma V_T)$

$\Sigma V_T=V_{Tn1}+V_{Tn3}+|V_{TP2}|+|V_{TP4}|$

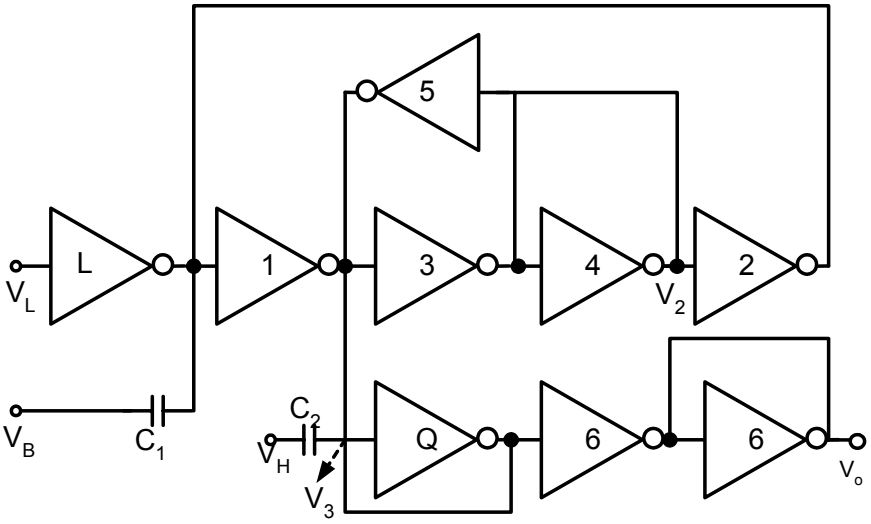
$k_{eff}=\dfrac{k_n k_p}{(\sqrt{k_n}+\sqrt{k_p})^2}$

$k_{n,p}=\dfrac{1}{2}(u_{eff}c_{ox}\times\dfrac{W}{L})_{n,p}$

Tunable g_m amplifier symbol:



2. Gm-C biquad (general)



$$H(s)=\frac{-C_1 g_m^{\,2} S N_{BP}+C_1 g_m S^2 N_{HP}+g_m^{\,2} N_{LP}+(C_1 C_2 g_m S^2+g_{mL} g_m)N_{BR}}{C_1 C_2 g_m S^2+C_1 g_m (g_{mQ}-g_m)S+g_m^{\,3}}$$

N_{BP}: $V_B\neq 0$, $V_L=V_H=0$
N_{HP}: $V_H\neq 0$, $V_L=V_B=0$
N_{LP}: $V_L\neq 0$, $V_H=V_B=0$
N_{BR}: $V_L=V_H=V_{BR}$, $V_B=0$

Experimental results on BP filter:

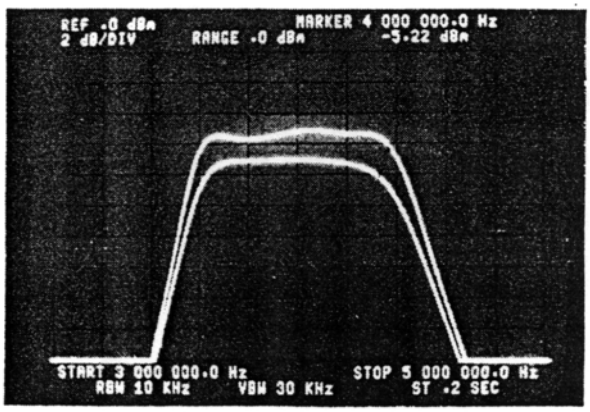


Fig. 10. Passband detail of the filter performance at 0°C (lower trace) and at 65°C.

Center frequency 4MHz

TABLE I
EXPERIMENTAL FILTER DATA

Control	Automatic	Manual
Passband ripple	1 dB	0.5 dB
Stopband attenuation	>60 dB	
Bandwidth	800 KHz	
S/N in passband	≈40dB	75dB
Distortion (for 0.5Vpp)	0.5%	
Max. signal level	1.2 V_{pp}	
Frequency control range	1 MHz	1.5 MHz
Q-control range	40%	unlimited
Offset (reference inverter)	1mV @ Gain ≈ 50	

§15-5 MOSFET-C Filters

* MOSFET-C filters are slower than Gm-C filters

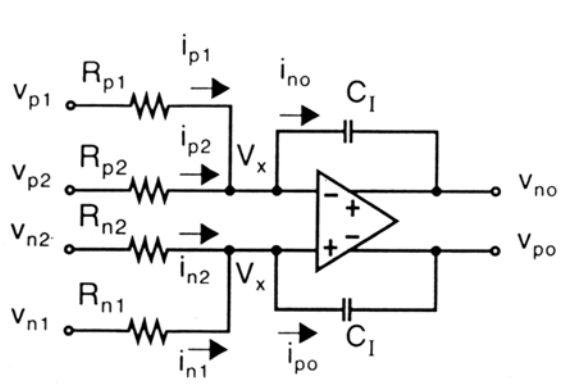
∵Miller integration.

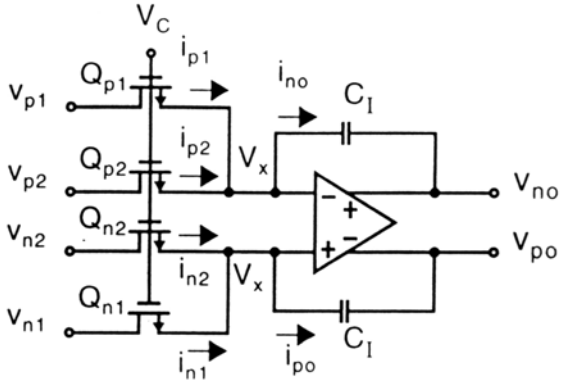
* Smaller speed

∵The load of op amps is resistive

* Straightforward design methodology

1. Two-transistor integrators.





(a) Active-RC integrator (b) Two-transistor MOSFET-C integrator

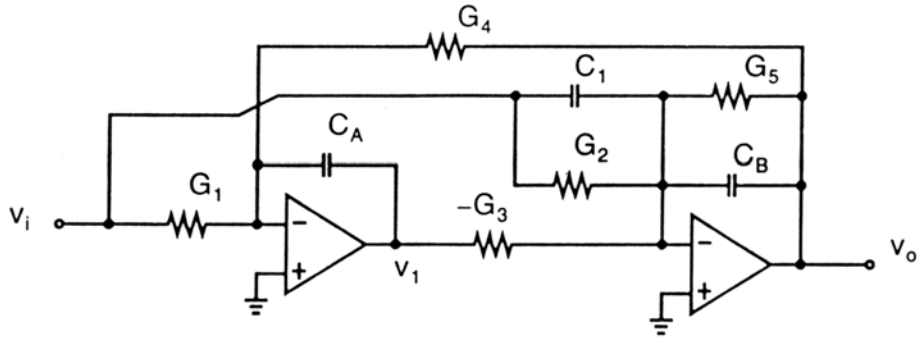
$$R_1 \equiv R_{p1} = R_{n1} \qquad R_2 \equiv R_{p2} = R_{n2}$$

$$V_{diff} \equiv V_{po} - V_{no} = \frac{i_{no} - i_{po}}{SC_1} = \frac{(i_{p1} + i_{p2}) - (i_{n1} + i_{n2})}{SC_1}$$

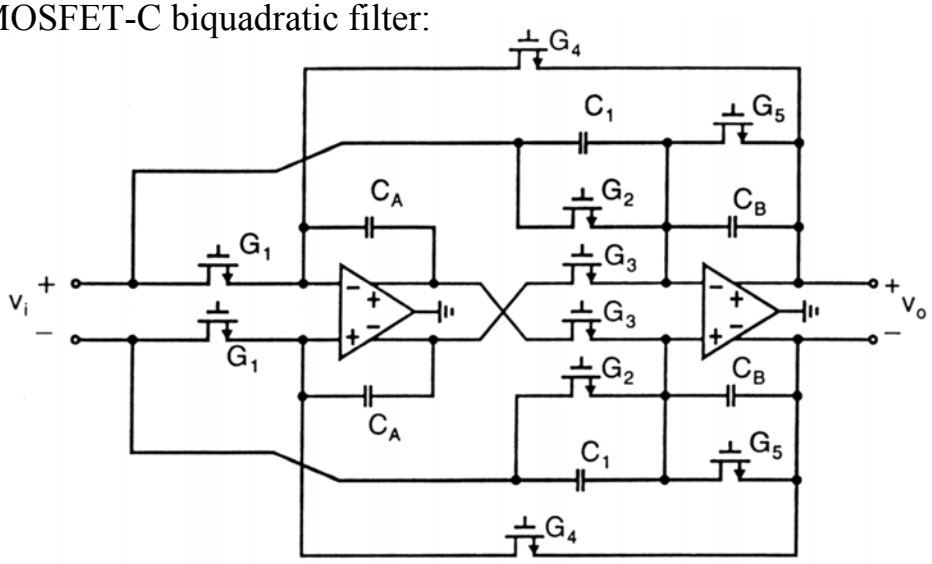
$$= \frac{1}{SR_1C_1}(V_{p1} - V_{n1}) + \frac{1}{SR_2C_1}(V_{p2} - V_{n2})$$

2.General biquadratic MOSFET-C filter

Active-RC circuit:



MOSFET-C biquadratic filter:

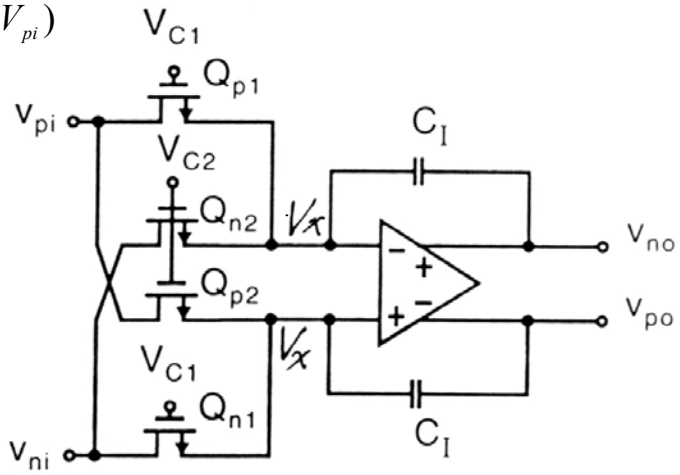


$$H(S)=\frac{V_o(s)}{V_i(s)}=\frac{(\frac{C_1}{C_B})S^2+(\frac{G_2}{C_B})S+\frac{G_1G_3}{C_AC_B}}{S^2+(\frac{G_1}{G_B})S+\frac{G_3G_4}{C_AC_B}}$$

3. Four-transistor integrators

$V_{diff} \equiv V_{po}-V_{no}$

$$=\frac{1}{sr_{DS1}c_1}(V_{pi}-V_{ni})+\frac{1}{sr_{DS2}c_1}(V_{ni}-V_{pi})$$



where $r_{DS1}=\frac{1}{u_nc_{ox}(\frac{W}{L})_1(V_{c1}-V_x-V_t)}$

$$r_{DS2}=\frac{1}{u_nc_{ox}(\frac{W}{L})_2(V_{c2}-V_x-V_t)}$$

All four transistors are matched

$$=>V_{diff}=\frac{1}{sr_{DS}c_1}(V_{pi}-V_{ni})$$

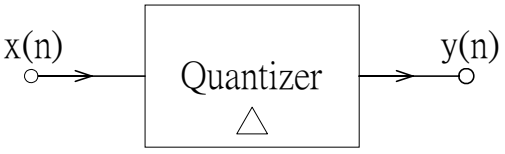
where $r_{DS}=\frac{1}{u_nc_{ox}(\frac{W}{L})(V_{c1}-V_{c2})}$

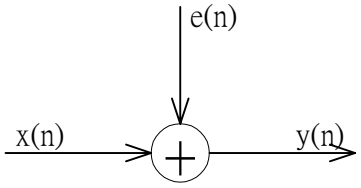
CH 16. Oversampling Data Converters

§16-1 Fundamental Concept

§16-1.1 Oversampling without noise shaping

1. Quantization noise modeling



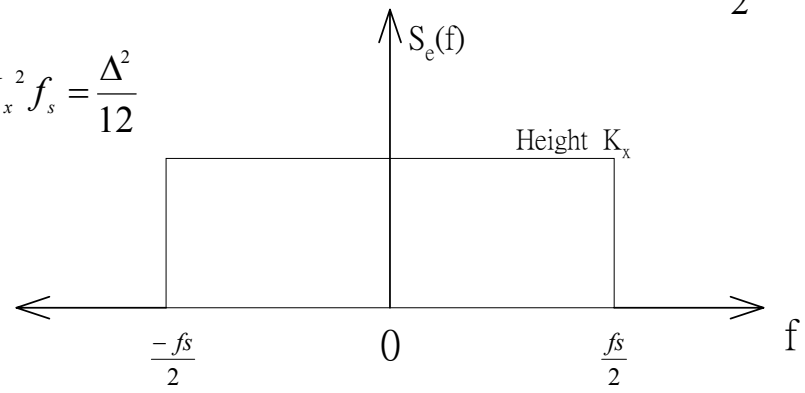


$$e(n) \equiv y(n) - x(n)$$

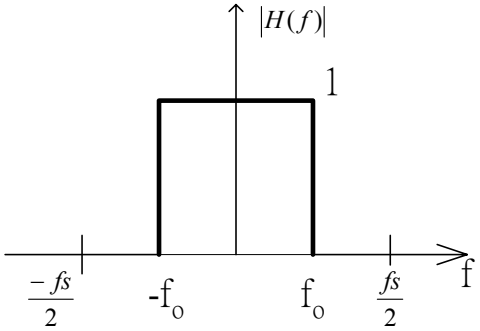
* e(n) can be approximated as an independent random variable uniformly distributed between $\pm\frac{\Delta}{2}$ where Δ is the difference between two adjacent quantization levels, i.e. V_{LSB}.
* The quantization noise power $= \frac{\Delta^2}{12} = P_e$
* The quantization noise power is independent of the sampling frequency f_s.
* The spectral density of e(n), $S_e(f)$ is white and all its power is within $\pm \frac{f_s}{2}$.

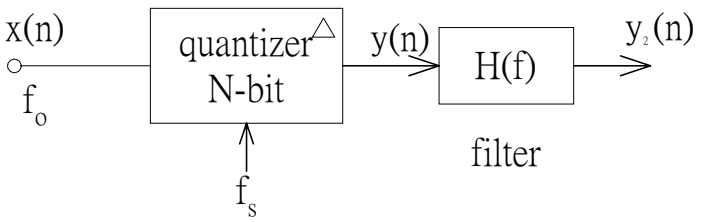
$$\int_{-\frac{fs}{2}}^{\frac{fs}{2}} S_e^2(f)df = \int_{-\frac{fs}{2}}^{\frac{fs}{2}} K_x{}^2 df = K_x{}^2 f_s = \frac{\Delta^2}{12}$$

$$=>K_x=(\frac{\Delta}{\sqrt{12}})\sqrt{\frac{1}{f_s}}$$



2. Oversampling Advantage





Oversampling ratio $OSR \equiv \frac{f}{2f_o}$

Assume that the input signal is a sinusoidal wave between 0 and $\Delta 2^N$.
The signal power P_s is

$$P_s=(\frac{\Delta 2^N}{2\sqrt{2}})^2=\frac{\Delta^2 2^{2N}}{8}$$

With H(f), P_s remains the same since the signal's frequency content is below f_o, but the quantization noise power P_e becomes

$$P_e=\int_{-\frac{fs}{2}}^{\frac{fs}{2}} S_e^2(f)\left|H(f)\right|^2 df=\int_{-fo}^{fo} K_x^{\ 2} df=\frac{2f_o}{f_s}\frac{\Delta^2}{12}=\frac{\Delta^2}{12}(\frac{1}{OSR})$$

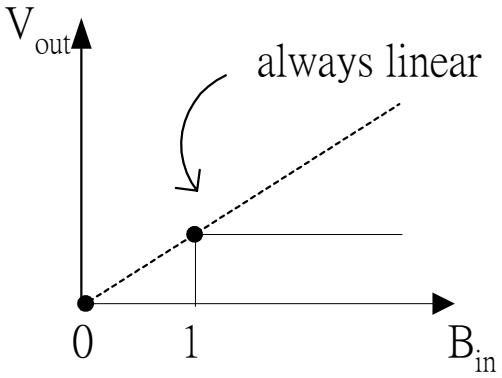
OSR $\uparrow\times 2$ => $P_e \downarrow \frac{1}{2}$ or -3dB, or 0.5 bits

$$SNR_{max}=10\log(\frac{P_s}{P_e})=10\log(\frac{3}{2}2^{2N})+10\log(OSR)$$

$$=6.02N+1.76+10\log(OSR)$$

=>SNR enhancement obtained from oversampling: 10log(OSR).
SNR improvement of 3 dB/octave or 0.5 bits/octave

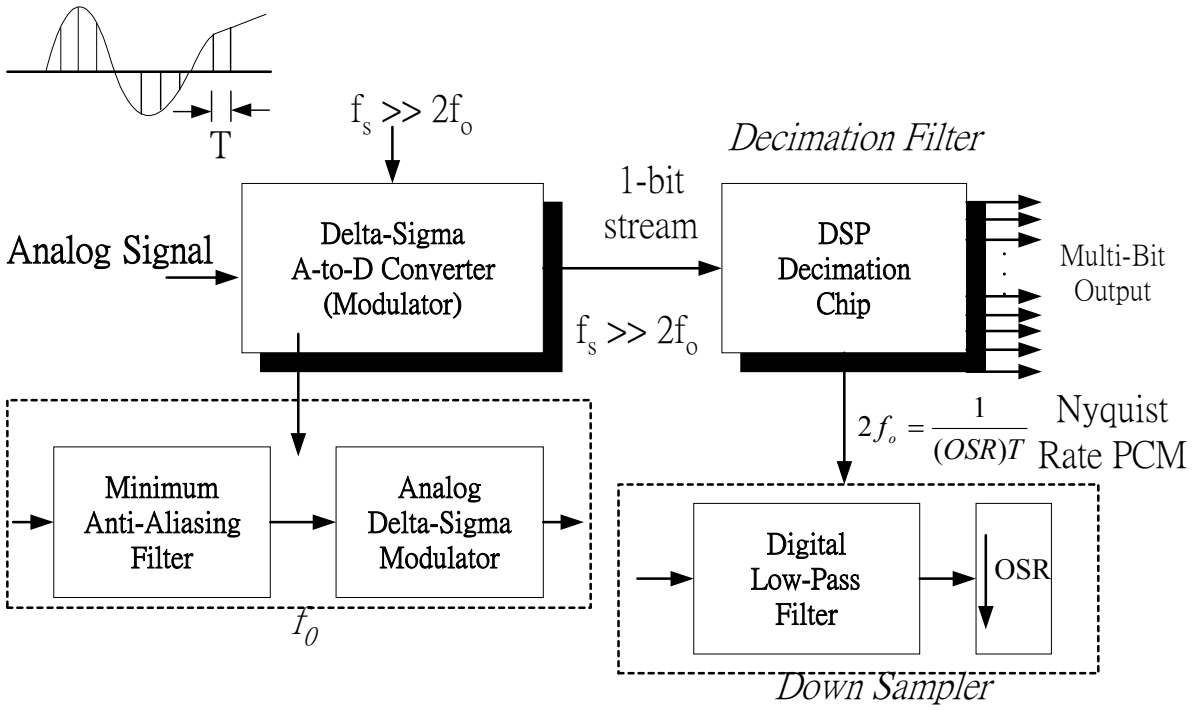
3.The advantage of 1-bit D/A converter
* Oversampling improves the SNR, but it does not improve linearity.
* Theoretically, 1-bit converter with f_o=25 KHz can obtain a 96-dB SNR(16 bits) if the sampling frequency f_s=54,000 GHz!
* The advantage of a 1-bit DAC is that it is inherently linear.



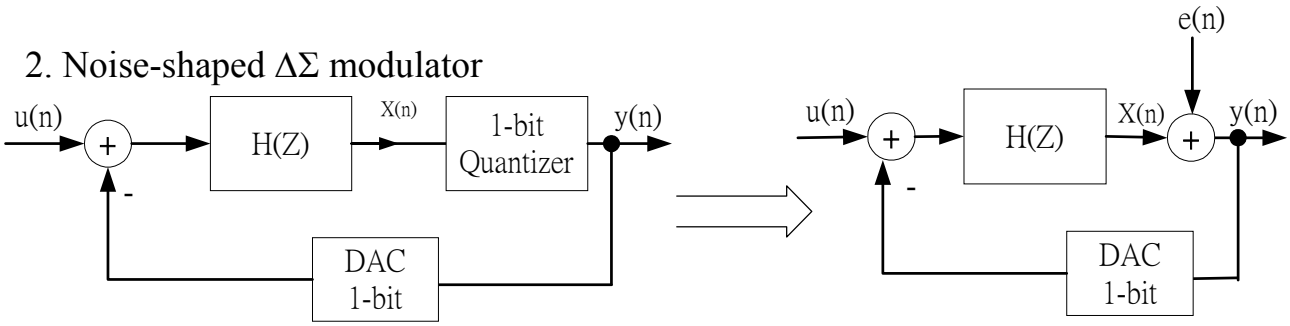
§16-1.2 Oversampling with noise shaping

1. The system architecture of a ΔΣ oversampling ADC is shown in the next page

Oversampling Delta-Sigma Analog-to-Digital Converters:



2. Noise-shaped ΔΣ modulator



Two independent inputs: U(z) and E(z)

Signal Noise

Signal transfer function $S_{TF}(z) \equiv \frac{Y(z)}{U(z)} = \frac{H(z)}{1+H(z)}$

Noise transfer function $N_{TF}(z) \equiv \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)}$

=>$Y(z)=S_{TF}(z)U(z)+N_{TF}(z)E(z)$

If $|H(z)| \to \infty$ for $0<f<f_o$ => $|S_{TF}(z)| \to 1$ and $|N_{TF}(z)| \to 0$

=> Quantization noise ↓ and signal unchanged.

3.First-order noise shaping:

$H(z)=\frac{z^{-1}}{1-z^{-1}}$ (Noniverting Forward-Euler SC integrator)

$\Rightarrow S_{TF}(z)=\frac{H(z)}{1+H(z)}=z^{-1}$

$N_{TF}(z)=\frac{1}{1+H(z)}=(1-z^{-1})$ $z=e^{j\omega T}=e^{j2\pi f/fs}$

$N_{TF}(f)=1-e^{-j2\pi f/fs}=\sin(\frac{\pi f}{f_s})\times(2j)\times(e^{-j\pi f/fs})$

$\left|N_{TF}(f)\right|=2\sin(\frac{\pi f}{f_s})$

The quantization power noise power over 0 to f_o is

$P_e=\int_{-fo}^{fo}S_e^2(f)\left|N_{TF}(f)\right|^2df=\int_{-fo}^{fo}(\frac{\Delta^2}{12})\frac{1}{f_s}[2\sin(\frac{\pi f}{f_s})]^2df$

Since $f_o << f_s$, i.e. OSR>>1, $\sin(\frac{\pi f}{f_s})\cong\frac{\pi f}{f_s}$

$\Rightarrow P_e\cong(\frac{\Delta^2}{12})(\frac{\pi^2}{3})(\frac{2f}{f_s})^3=\frac{\Delta^2\pi^2}{36}(\frac{1}{OSR})^3$

$P_s=\frac{\Delta^2 2^{2N}}{8}\Rightarrow SNR_{max}=10\log(\frac{P_s}{P_e})=10\log(\frac{3}{2}2^{2N})+10\log[\frac{3}{\pi^2}(OSR)^3]$

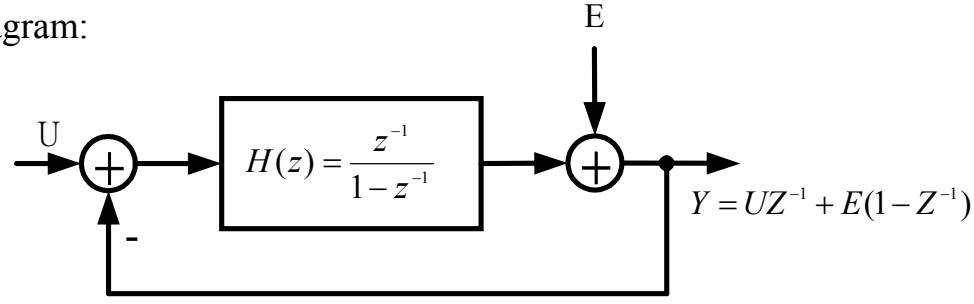
$\Rightarrow SNR_{max}=6.02N+1.76-5.17+30\log(OSR)$

Double OSR => SNR_{max} ↑ by 9dB or 1.5bits/octave

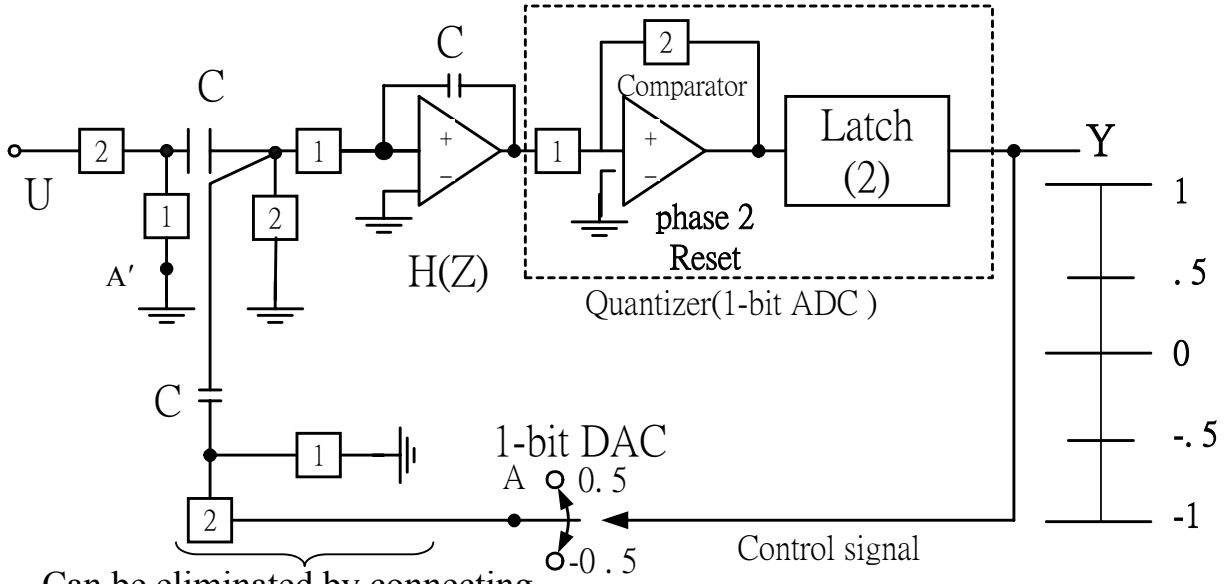
Without noise shaping: SNR_{max} ↑ by 3dB/ octave or 0.5bits/ octave.

$Y=Z^{-1}U+E(1-Z^{-1})$

Block diagram:

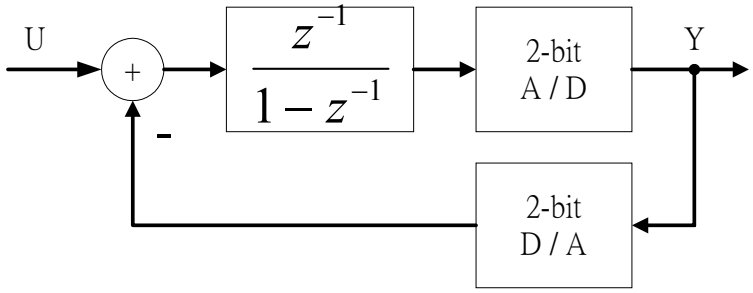


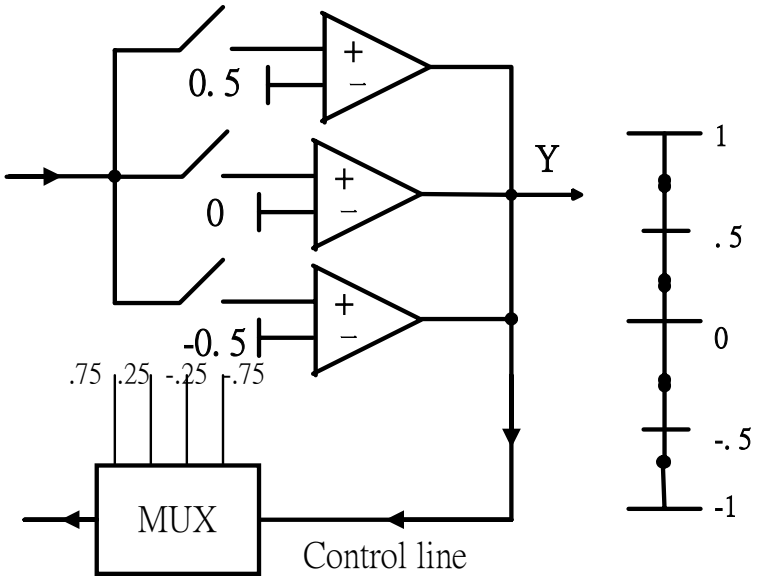
SC implementation:



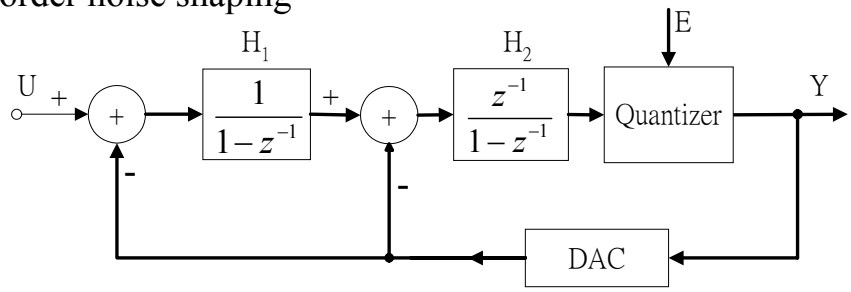
Can be eliminated by connecting the node A Directly to the node A'.

First-order noise shaping with 2-bit ADC and 2-bit DAC





4. Second-order noise shaping



$S_{TF}(Z)=Z^{-1}$ $N_{TF}(Z)=(1-Z^{-1})^2$ $Y=Z^{-1}U+(1-Z^{-1})^2E$

$$|N_{TF}(f)|=[2\sin(\frac{\pi f}{f_s})]^2$$

$$\Rightarrow P_e \cong \frac{\Delta^2\pi^4}{60}(\frac{1}{OSR})^5$$

$$SNR_{max}=10\log(\frac{P_s}{P_e})=10\log(\frac{3}{2}2^N)+10\log(\frac{5}{\pi^4})+10\log(OSR)^5$$

$=6.02N+1.76-12.9+50\log(OSR)$

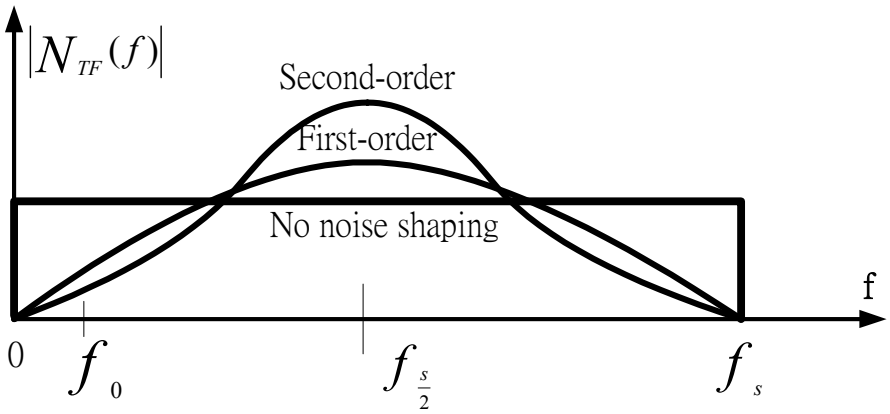
$OSR\times 2 \Rightarrow SNR_{max}\uparrow$ by 15dB/Octave or 2.5 bits/Octave

General formula of SNR_{max} with k-order noise shaping:

$$SNR_{max}=6.02N+1.76-10\log(\frac{2k+1}{\pi^4})+(2k+1)\,10\log(OSR)$$

$OSR\times 2 \Rightarrow SNR_{max}\uparrow$ by $3(2k+1)$dB/Octave or $0.5(2k+1)$bits/Octave

Noise-shaping transfer functions:



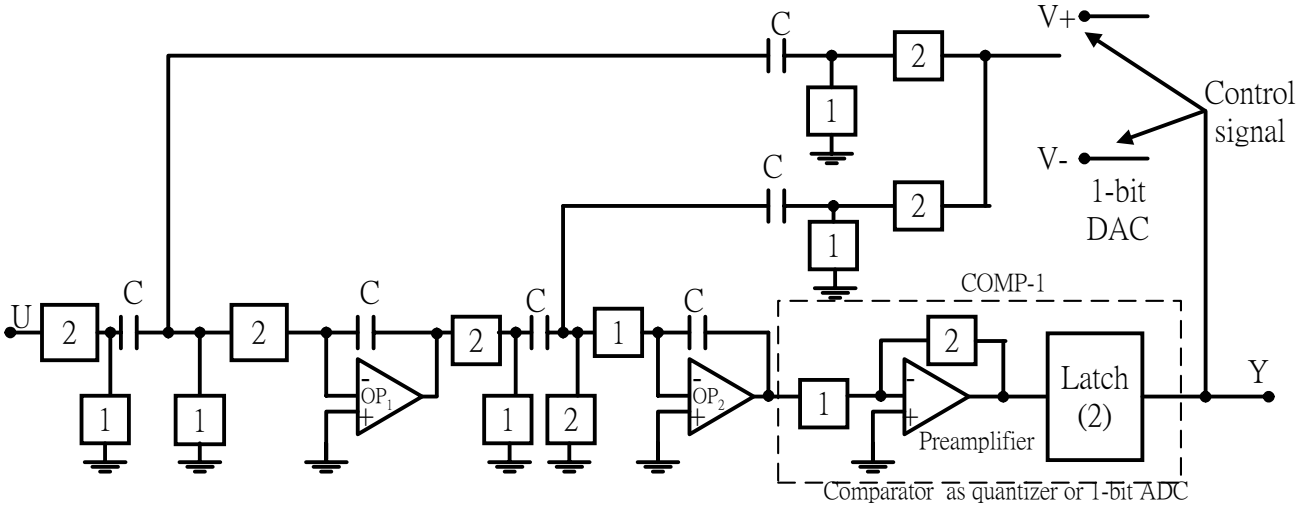
The SC implementation of the second-order ΔΣ modulator is shown in the next page.

* Single-ended structure
* Can be converted into fully differential structure for better noise rejection and

linearity.

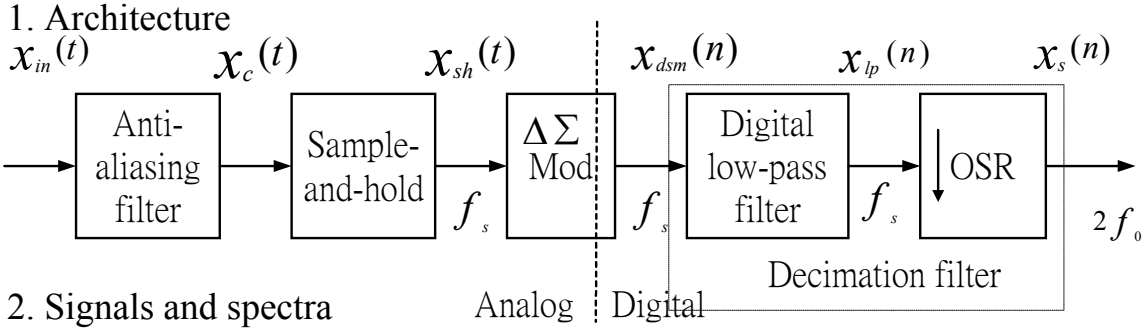
* The capacitor and switches in the feedback path to OP_2 can be reduced as shown on page 16-5.

SC implementation: Single-Ended type circuit diagram

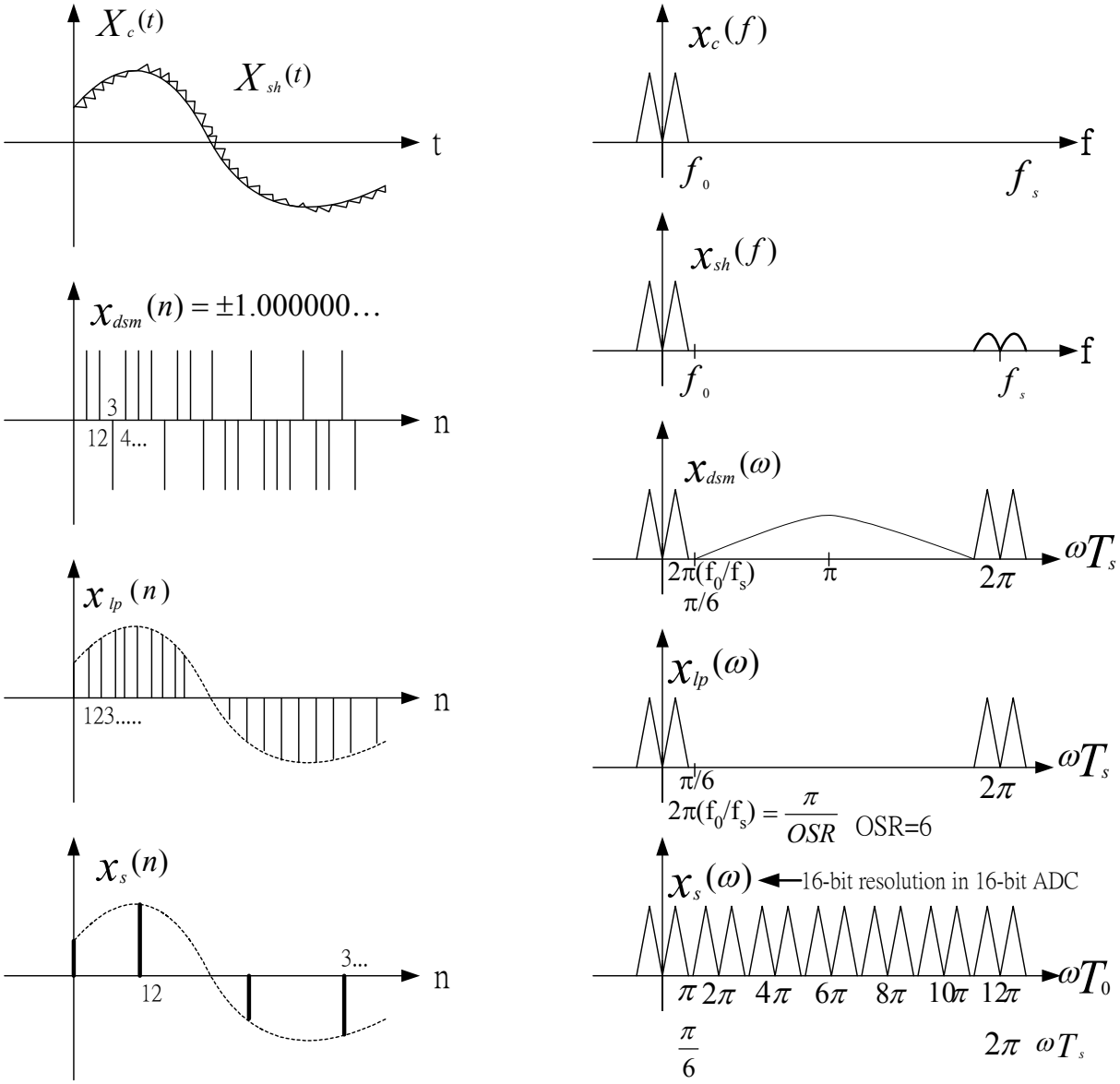


§16-2 System Architecture of Oversampling ΔΣ ADC

1. Architecture



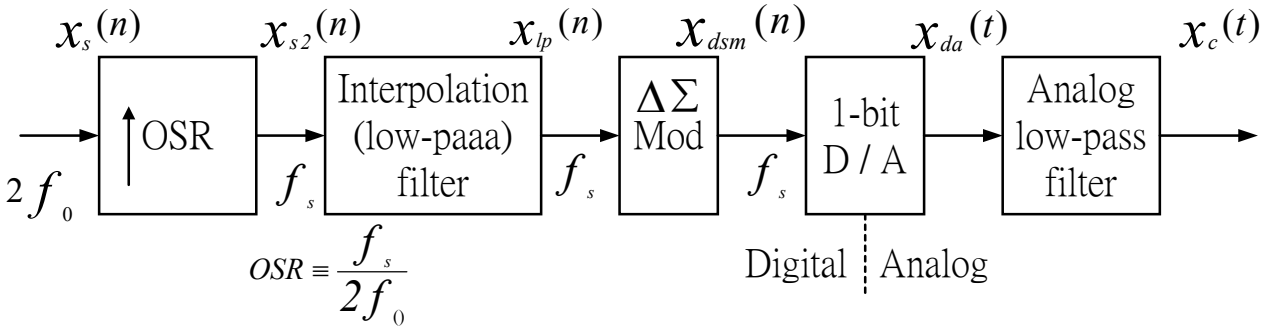
2. Signals and spectra



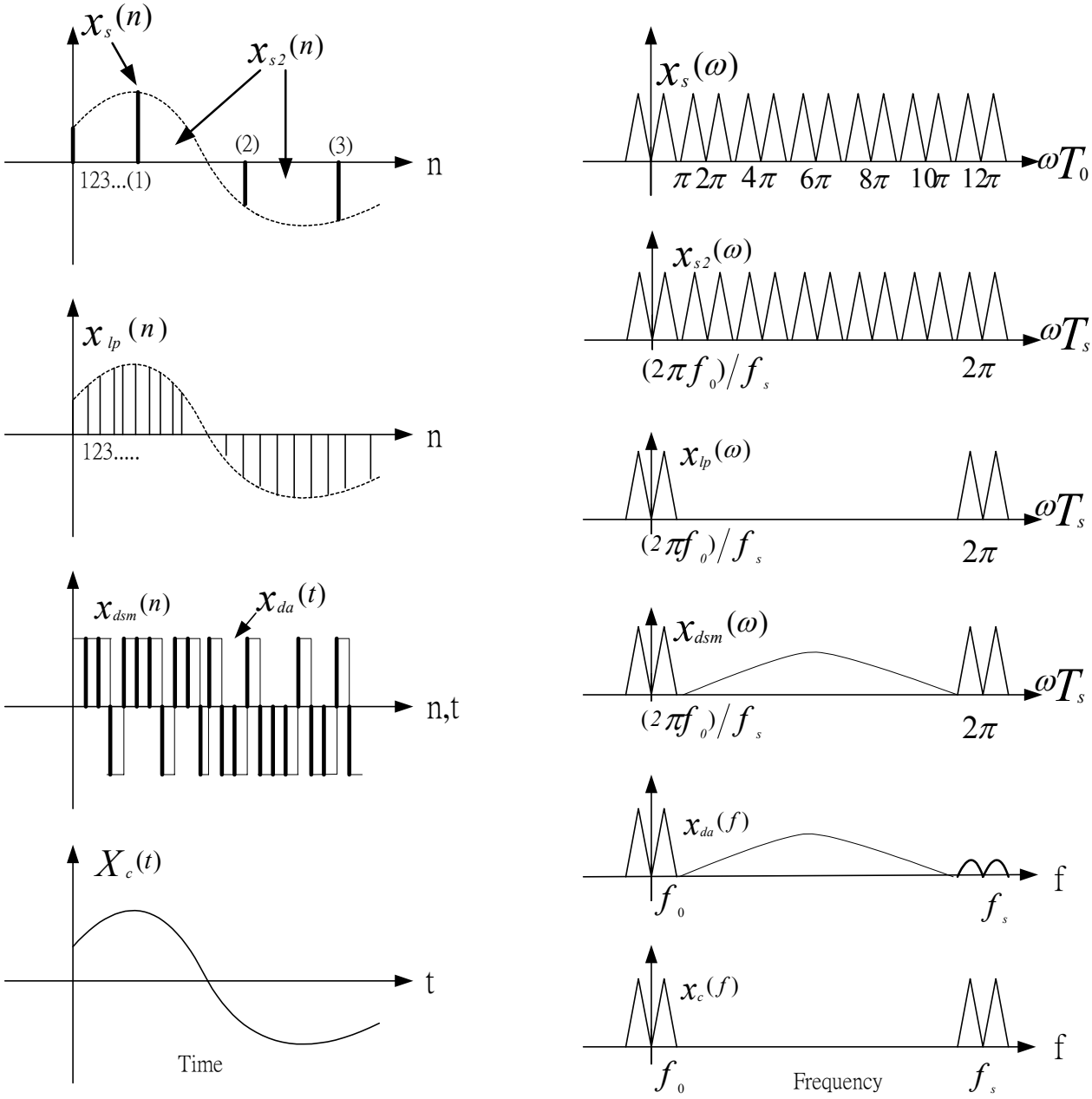
* The decimation process does not result in any loss of information, since the bandwidth of the original signal was assumed to be f_o. The spectral information is spread over $0\sim\frac{\pi}{6}$ in X_{ep} and $0\sim\pi$ in X_s.

§16-3 System Architecture of Oversampling ΔΣ DAC

1. Architecture



2. Signals and spectra

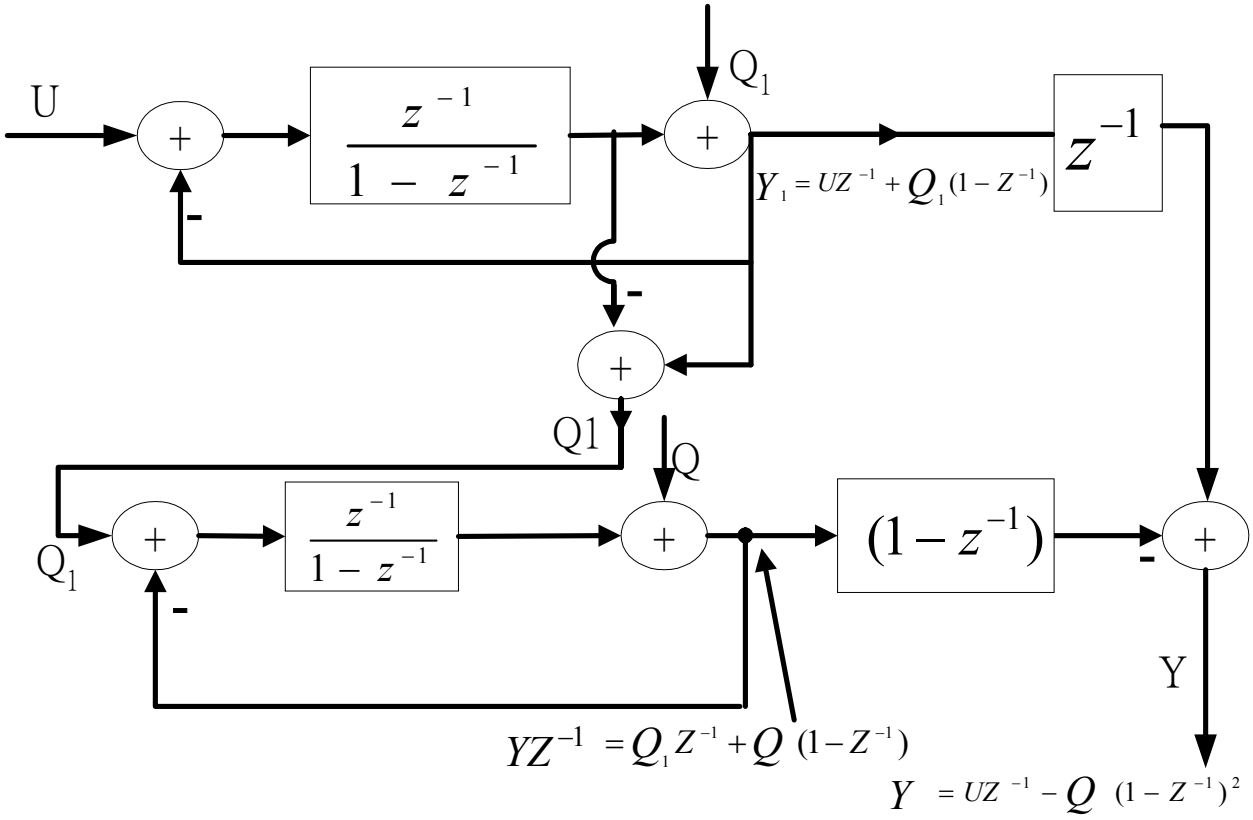


§16-4 High-Order Modulators

Multi-st**A**ge noise **SH**aping (MASH) architecture:

To use a cascade-type structure where the overall higher-order modulator is constructed using lower-order ones.

=> The stability could be maintained.



§16-5 Design Considerations

§16-5.1 Limitations on accuracy and linearity

A. Noise

- Thermal noise in resistors, conducing switches, op-amps. Usually aliased by sampling
- 1/f op-amp noise, dc offset
- Supply, ground and substrate noise
- clock feedthrough noise
- clock jitter noise
- quantization noise leakage

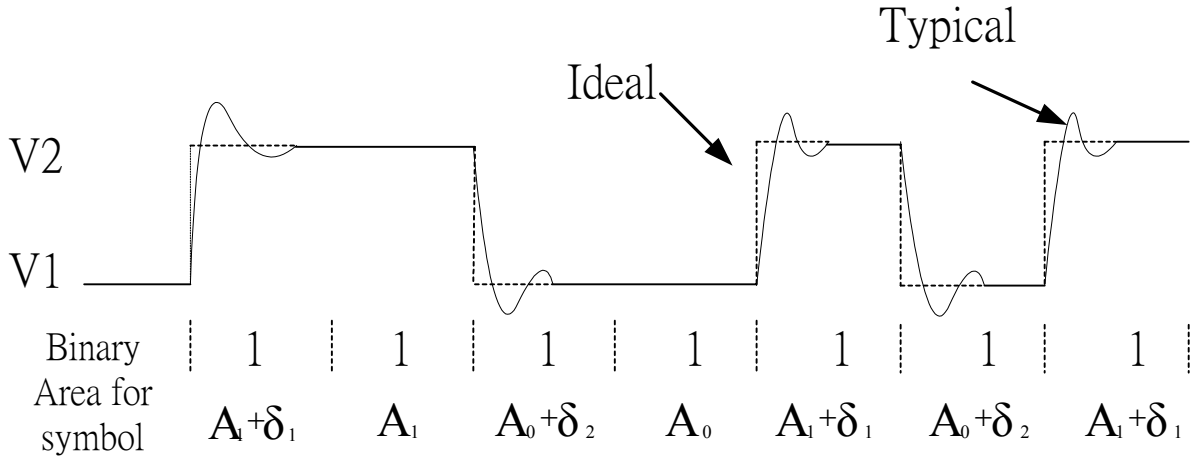
B. Nonlinear effects

- R&C nonlinearities
- Amplifier nonlinearities
- Finite op-amp slew rate
- Signal-dependent clock feedthrough noise
- Signal-dependent sampling aperture noise
- Internal A/D and D/A nonlinearities

Linearity of 1-bit DAC:

1. The two output levels somehow become functions of the low-frequency signals=> Linearity limitation
   - Power supply voltage are changed for different low-frequency signals to cause distortion.
     => must be well-regulated.
   - The clock feedthrough of the input switches is also dependent on the gate voltage and thus the supply voltage.
     => low-frequency input signal dependent
   - The clock jitter could be a function of the low-frequency input signals.

2.The memory between output levels also causes severe linearity limitation.



δ_1, δ_2: The area difference of the present binary state with different past states.

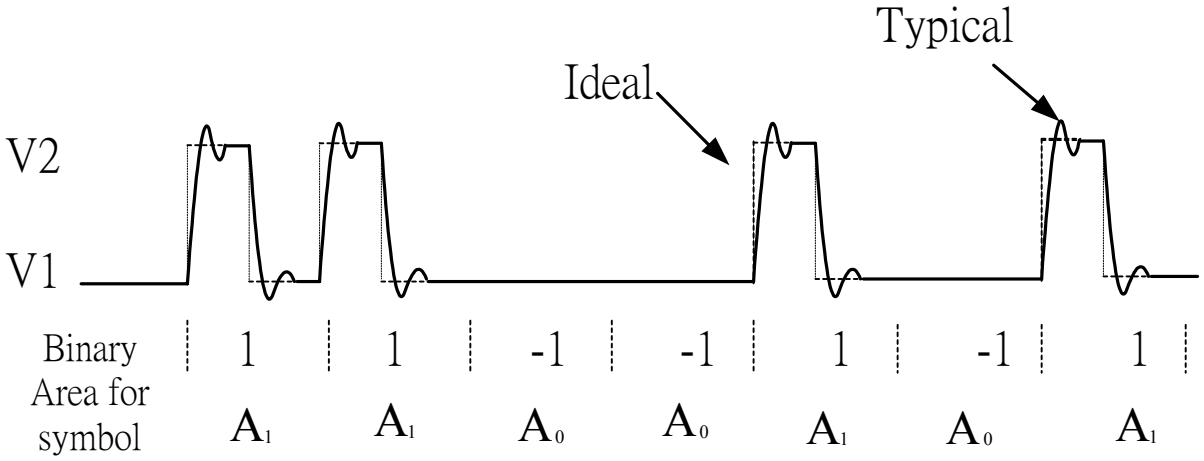
	-1→1: δ_1	1→-1: δ_2
Average 0 : 1, -1,1, -1,- - -		$\overline{Va(t)} = \frac{A_1 + A_O}{2} + \frac{\delta_1 + \delta_2}{2}$
Average $\frac{1}{3}$: 1, 1, -1, 1, -1, 1---		$\overline{Vb(t)} = \frac{2A_1 + A_O}{3} + \frac{\delta_1 + \delta_2}{3}$
Average $-\frac{1}{3}$: -1, -1, 1, -1, -1, 1, -1---		$\overline{Vc(t)} = \frac{A_1 + 2A_O}{3} + \frac{\delta_1 + \delta_2}{3}$

Ideal case: $\delta_1=\delta_2=0$, practical case: $\delta_1 \neq \delta_2 \neq 0$

=>Three averages do not lie on a straight line=>Nonlinear.

How to improve this nonlinearity?

1. δ1=-δ2 : To match falling and rising signals => Very difficult to achieve.
2. The use of memoryless coding scheme, i.e. return-to-zero (RTZ) coding scheme.



1 : -1→1 and 1→1 Every 1 has the same area.

-1 : -1→-1 Every -1 has the same area.

=> Better linearity.

3. Basically, SCF or SC circuits are memoryless if enough time is left for settling on each clock phase.

Idle tones phenomena

1-bit DAC

dc level $\frac{1}{3}$ => y(n)={1, 1, -1, 1, 1, -1…..}

periodic pattern with the power concentrated at dc and $\frac{f_s}{3}$.

After low-pass filter=> only dc level remains.

dc level $\frac{1}{3}+\frac{1}{24}=\frac{3}{8}$ => y(n)={1, 1, -1, 1, 1, -1, 1, 1, -1, 1, 1, -1, 1, 1, 1, -1, 1, 1, -1, 1,……}

periodic pattern with 16 cycles and some power at dc and $\frac{f_s}{16}$.

=> lowpass filter

=> dc level $\frac{3}{8}$ and $\frac{f_s}{16}$ tone

($\because f_o=\frac{f_s}{16}$ is assumed and lowpass filter will not attenuate $f_s/16$ signal)

=> Low-frequency tones cannot be filtered out by the lowpass filter and can lead to annoying tones in the audible range. They exist even in high-order modulators. There tones might be a signal varying over some frequency range in a random-like fashion.

Dithering technique to reduce idle tones.

- To add the dithering signal to the modulator just before its quantizer.
- The dithering signal has a white-noise type spectrum and is a random (psuedo-random) signal.
- The dithering signal breaks up the tones so that they never occur.
- Add about 3-dB extra in-band noise
- Require rechecking the modulator's stability.

§16-6 Advantages and Applications

Advantages of Delta-Sigma Converters:

- Low-Complexity Analog, High-Complexity Digital
- High-Resolution Conversion
- Low-Precision Analog (no trimming)
- Simple Anti-Aliasing Filters
- No Sample & Hold Needed
- Can be Built Completely In CMOS
- Overall Small Chip Area in Fine-Line Technology
- Can be Integrated on Chip With Other DSP Functions
- Ideally Suit for Rates up to and Including Audio Band

Commercial Applications Well-Suited for Delta-Sigma ADC

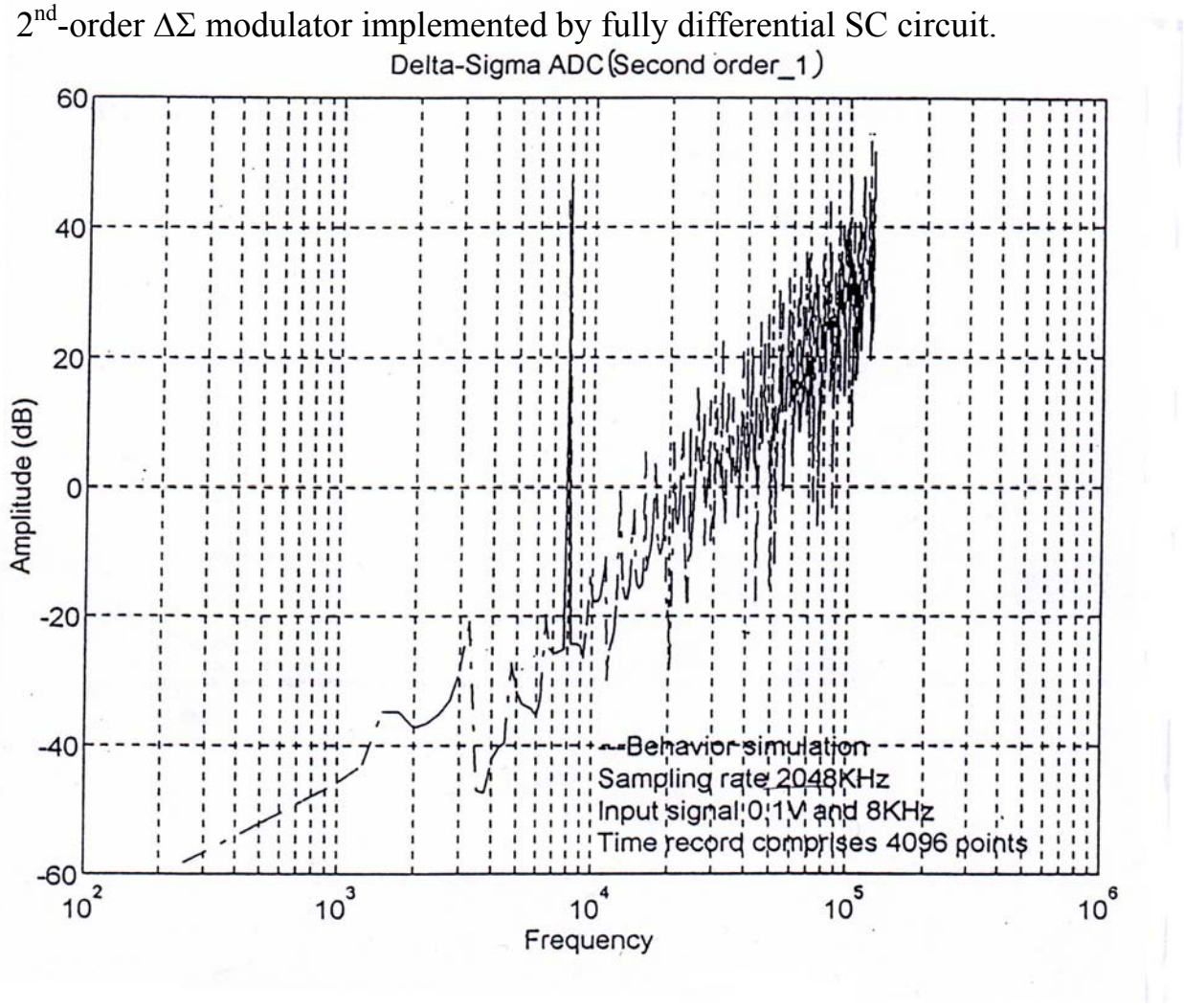
- Standard Voice Band Telephony
  13-bit dynamic range, 8-bit linearity (u/A-Law), 8KHz Sampling rate
- Digital Mobile Radio (same req. as above)

- High-Precision Voice-Band (CCITT V.32 9600-Baud Modems)
  14-15 bit dynamic range, 12-bit linearity, 3-4kHz BW, 9600 Sampling rate
- ISDN Wideband Speech (CCITT G.722)
  13-bit dynamic range, 16kHz Sampling rate
- ISDN U-Interface
  13-bit dynamic range, 80kHz Sampling rate, 160kb/s Transmission Rate
- Audio-Band (CD, DAT; stereo (2))
  16-18-bit (18-20 bit) resolution, 14-16 bit)(15-16bit) linearity, 48kHz Sampling Rate
- 5 1/2 Instrumentation A/D Converter
  20 bit resolution, 0.1-10Hz BW with Self-Calibration Circuit
- Integration with Digital Signal Processors
- Ideally Suited for Rates up to and Including Audio Band

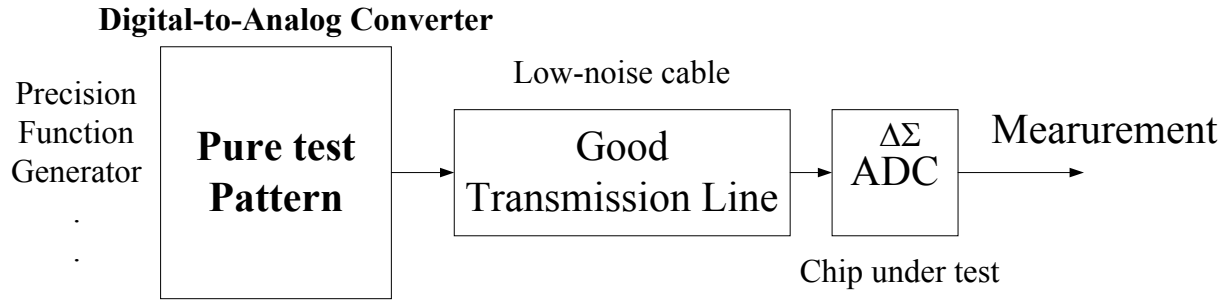
A variety of applications from voice-band through audio-band

§16-7 Examples

2^{nd}-order $\Delta\Sigma$ modulator implemented by fully differential SC circuit.

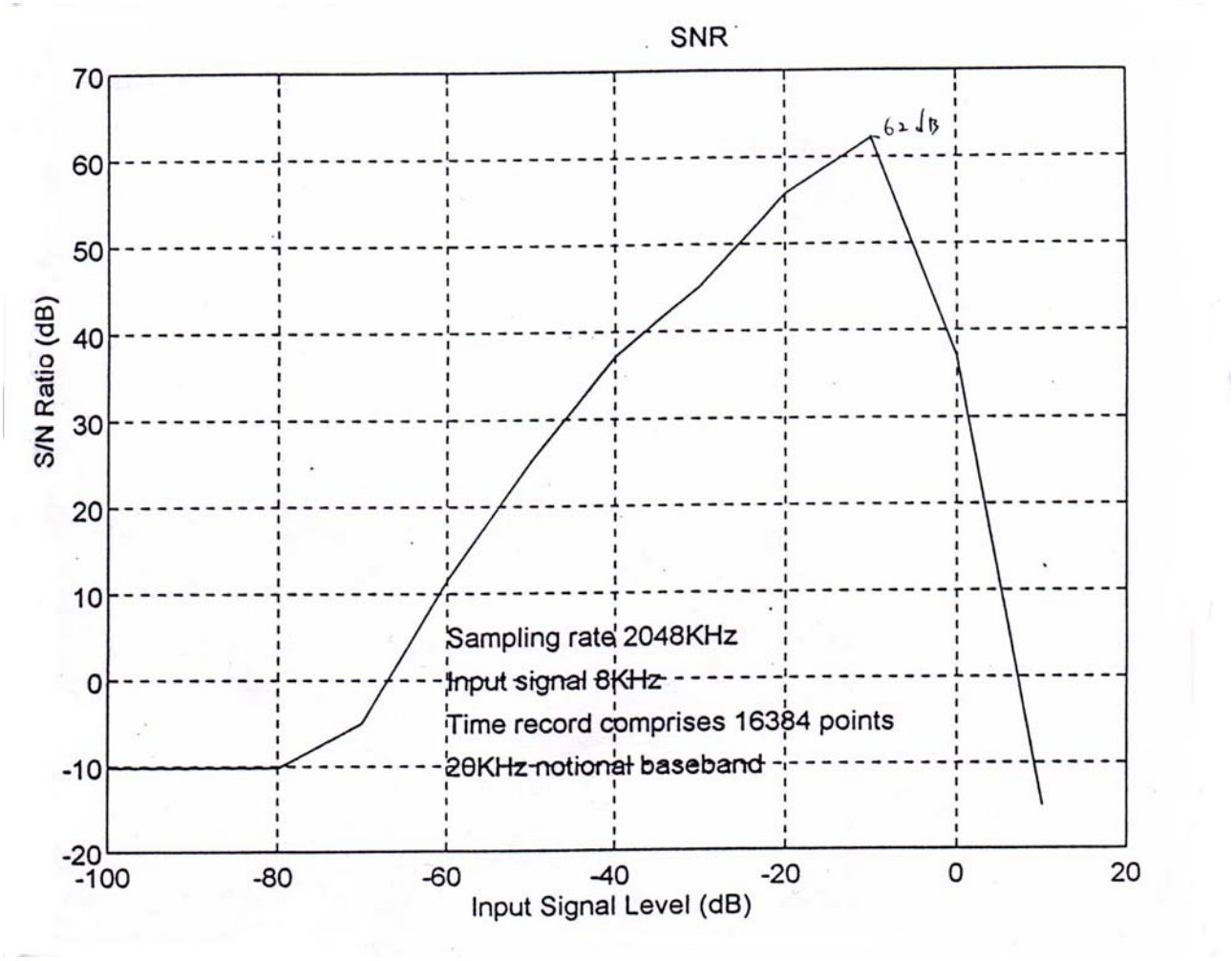


Testing Environment:



*Develop design-for-testability ADC and environment

The measured SNR versus input signal level.

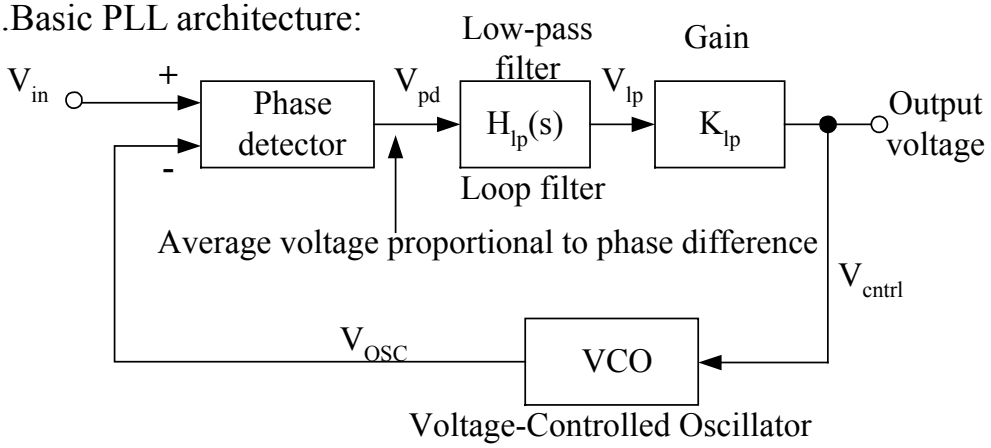


CH 17 Phase-Locked Loops (PLLs)

§17-1 General architecture and Operational Principle

1. Applications of PLLs: 1. Clock recovery in communication and digital systems.
2. Frequency synthesizer used in televisions or wireless communication systems to select different channels.
3. Demodulation of FM signals.

2.Basic PLL architecture:



If the phase detector is of analog-multiplier type, its output voltage V_{pd} can be written as

$$V_{pd}=K_M V_{in} V_{osc}=K_M E_{in} E_{osc}\sin(\omega t)\cos(\omega t-\phi_d)$$

where ϕ_d is the phase difference between the input signal V_{in} and the output V_{osc} of the VCO.

$$V_{pd}=K_M \frac{E_{in}E_{osc}}{2}[\sin(\phi_d)+\sin(2\omega t-\phi_d)]$$

Since the lowpass filter is to remove the high-frequency (2ω) term, the signal V_{cntl} is given by

$$V_{cntl}=K_{lp}K_M \frac{E_{in}E_{osc}}{2}\sin\phi_d$$

$$\cong K_{lp}K_M \frac{E_{in}E_{osc}}{2}\phi_d=K_{lp}K_{pd}\phi_d \qquad \text{where } K_{pd}\equiv K_M \frac{E_{in}E_{osc}}{2}$$

The frequency of VCO can be expressed as

$\omega_{osc}=K_{osc}V_{cntl}+\omega_{fr}$

where ω_{fr} is the free-running frequency of the VCO with its control voltage $V_{cntl}=0$.

$$\Rightarrow V_{cntl}=\frac{\omega_{in}-\omega_{fr}}{K_{osc}}$$

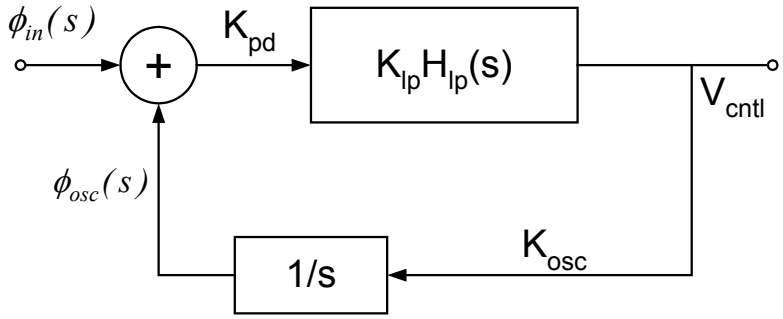
where ω_{in} is the frequency of the input signal, which is equal to the frequency of VCO output when the PLL is in the locked state.

$$\Rightarrow \phi_d = \frac{V_{cntl}}{K_{lP}K_{pd}} = \frac{\omega_{in} - \omega_{fr}}{K_{lP}K_{pd}K_{osc}}$$

3.Linearized small-signal analysis

When a PLL is in lock, its dynamic response to input-signal phase and frequency changes can be well approximated by a linear model, as long as these changes are slow and small about their operating point.

A signal-flow graph for the linearized small-signal model of a PLL when in lock:



$V_{cntl}(s)=K_{pd}K_{lp}H_{lP}(s)[\phi_{in}(s)-\phi_{osc}(s)]$

$\phi_{osc}(s)=K_{osc}(V_{cntl}(s)/s) \quad (\because \omega(t)=\frac{d\phi(t)}{dt} \quad \phi(s)=\frac{\omega(s)}{s})$

$$\Rightarrow \frac{V_{cntl}(s)}{\phi_{in}(s)} = \frac{SK_{pd}K_{lP}H_{lP}(s)}{S + K_{pd}K_{lP}K_{osc}H_{lP}(s)}$$

* General transfer function applicable to almost every PLL.

* Different PLLs => Different $H_{lp}(s)$, K_{pd}, K_{osc}.

If a lead-lag lowpass filter is used in $H_{lp}(s)$, we have

$$H_{lp}(s)=\frac{1+s\tau_z}{1+s\tau_p} \qquad \tau_z << \tau_p$$

$$\Rightarrow H(s) \equiv \frac{V_{cntl}(s)}{\phi_{in}(s)} = \frac{\frac{1}{K_{osc}}S(1+s\tau_z)}{1+S(\frac{1}{K_{pd}K_{lp}K_{osc}}+\tau_z)+\frac{s^2\tau_p}{K_{pd}K_{lp}K_{osc}}}$$

* $H(s)=0$ as $s\rightarrow 0$ => $\Delta\phi_{in}=0$ leads to $\Delta V_{cntl}=0$

$$\frac{V_{cntl}(s)}{\omega_{in}(s)} = \frac{\frac{1}{K_{osc}} S(1+s\tau_z)}{1+S(\frac{1}{K_{pd}K_{lp}K_{osc}}+\tau_z)+\frac{s^2\tau_p}{K_{pd}K_{lp}K_{osc}}}$$

$$* \frac{V_{cntl}(s)}{\omega_{in}(s)}\Big|_{s=0} = \frac{1}{K_{osc}}$$

The above second-order s-domain transfer functions have ω_o and Q as

$$\omega_o = \sqrt{\frac{K_{pd}K_{lp}K_{osc}}{\tau_p}} = \frac{K_{pll}}{\sqrt{\tau_p}}$$

$$Q = \frac{\sqrt{\tau_P}}{\frac{1}{\sqrt{K_{pd}K_{lp}K_{osc}}}+\tau_Z\sqrt{K_{pd}K_{lp}K_{osc}}} = \frac{\sqrt{\tau_P}}{\frac{1}{K_{pll}}+\tau_Z K_{pll}}$$

* $Q=\frac{1}{2} \rightarrow$ good settling behavior

$Q=\frac{1}{\sqrt{3}} = 0.577 \rightarrow$ maximally flat group delay

$Q=\frac{1}{\sqrt{2}} = 0.707 \rightarrow$ maximally flat amplitude response

* Usually $Q=\frac{1}{2}$ is recommended in PLLs

In most cases, when $\omega_o << \omega_{fr}$, we have

$$\tau_Z >> \frac{1}{K_{pll}^2}$$

$$\Rightarrow Q \cong \frac{\sqrt{\tau_P}}{\tau_z K_{pll}} = \frac{1}{\omega_o \tau_Z} = \frac{1}{2}$$

$$\Rightarrow \tau_Z = \frac{2\sqrt{\tau_P}}{K_{pll}} = \frac{2}{\omega_o}$$

The transient time constant τ_{pll} of the complete loop for small phase or frequency changes can be expressed as

$$\tau_{pll} \cong \frac{1}{\omega_o}$$

Design considerations: 1.Choosing K_{pd} and K_{osc} based on practical considerations
2.Choose τ_p to achieve the desired loop settling time
3.Choose τ_Z to obtain the desired Q of the loop

If $\tau_Z=0$, => $Q=\sqrt{\tau_P}\,K_{pll}$, $\omega_o=\frac{K_{pll}^{\ 2}}{Q}=\frac{K_{pd}K_{osc}}{Q}$ ($K_{lp}=1$)

4. Capture range and acquisition time

Capture range: The maximum difference between the input signals' frequency and the VCO free-running frequency where lock can eventually be attained.
The capture range is on the order of the pole frequency of the lowpass filter.

Acquisition time: The time required to attain lock If the initial difference between the input signal's frequency and the VCO frequency is moderately large, the acquisition time t_{acq} is

$$t_{acq}\cong\frac{Q(\omega_{in}-\omega_{osc})^2}{\omega_o^{\ 3}}$$

* If a PLL is designed to have a narrow loop bandwidth ω_o, t_{acq} can be quite large and lock is attained too slowly.

Solution: 1. To add a frequency detector that detect when ω_{in}-ω_{osc} is large. Then drive the loop toward lock much more quickly. When ω_{in}-ω_{osc} is small, the frequency detector and the driver are disabled.
2. To design the lowpass filter with a programmable pole frequency ω_o.
Initial acquisition: $\omega_o\uparrow$ speed up acquisition.
Lock : $\omega_o\downarrow$ increase noise rejection.
3. To sweep the VCO's frequency range during acquisition with the PLL disabled. When $\omega_{osc}\rightarrow\omega_{in}$, sweeping is disabled and PLL is activated.

5. Lock range

Lock range: Once lock is attained, the PLL remains in lock over a range as long as the input signal's frequency ω_{in} changes only slowly. This range is the lock range, which is much larger than the capture range.

$$V_{cntl\text{-}max}=K_{lp}\,K_M\frac{E_{in}E_{osc}}{2}=K_{lp}K_{pd}$$

$$\Rightarrow \omega_{lck}=\pm K_{osc}K_{lp}K_{pd}$$

§17-2 Phase Detectors in PLLs

Three categories: 1. Analog phase detectors (PDs) or multipliers:
Rely on the DC component when multiplying two sinusoidal waveforms of the same frequency.

2. Sequential circuits (e.g. EXOR and Flip-Flop PDs):
Operate on the information contained in the zero-crossings of the input signal to aid acquisition when the loop is out of lock. Also a sequential circuit actually.

3. Phase-frequency detector:
Provide a frequency sensitive signal to aid acquisition when the loop is out of lock. Also a sequential circuits actually.

§17-2.1 Multiplier PD

$V_{pd} = K_M E_{in} \sin(\omega_1 t+\theta_1) E_{osc} \cos(\omega_2 t+\theta_2)$

$= K_M \frac{E_{in} E_{osc}}{2} \{\sin[(\omega_1-\omega_2)t+\theta_1-\theta_2]+\sin[(\omega_1+\omega_2)t+\theta_1+\theta_2]\}$

At phase lock, $\omega_1=\omega_2$

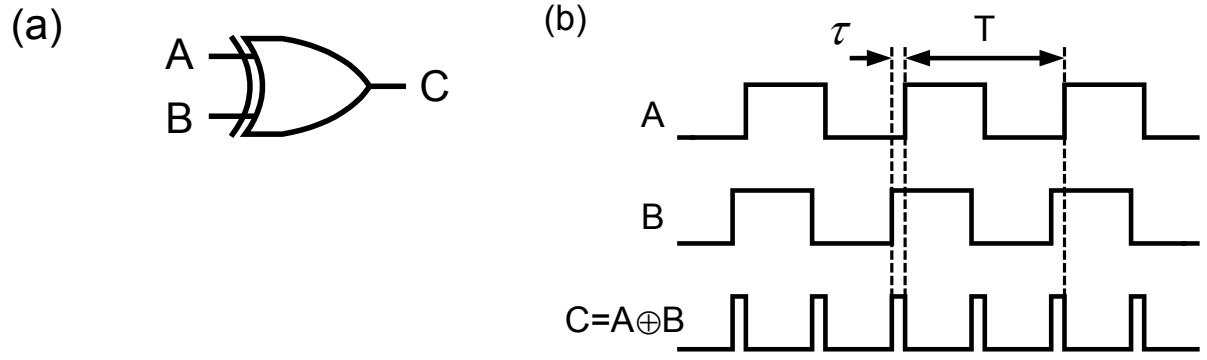
$\Rightarrow V_{pd} = K_M \frac{E_{in} E_{osc}}{2} [\sin(\theta_1-\theta_2)+\sin(2\omega t+\theta_1+\theta_2)]$

After the lowpass filter, we have

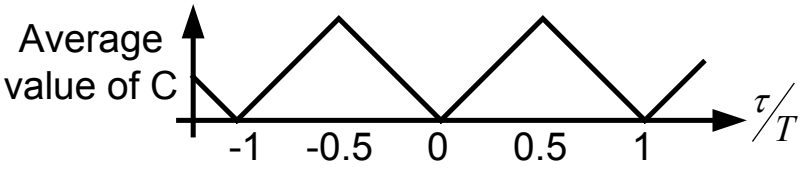
$V_{pd}=K_{lp}K_M \frac{E_{in} E_{osc}}{2} \sin(\theta_1-\theta_2)=K_M \frac{E_{in} E_{osc}}{2} \sin\theta_d \propto \theta_d$ if θ_d is small.

* The multiplier PD is especially useful in applications where the reference frequency is too high and where the loop bandwidth is sufficiently narrow so that the filtering of the undesired components can be effective.
* The loop could lock to harmonics of the input signal.
  =>False lock
* $\omega_1=\omega_2$ is required.

§17-2.2 EXOR PD



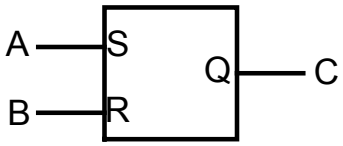
(c)



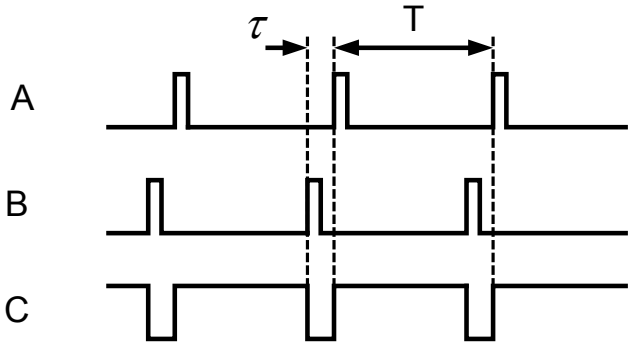
* when A(V_{in}) and B(V_{osc}) are 90° out of phase, the output V_{pd}(c) has $\omega=2\omega_{in}$ and 50% duty cycle. This is a reference point. $V_{pd} \propto \theta_d$ for $0^o<\theta_d<180°$.
* False lock could occur
* $\omega_1=\omega_2$ is required.

§17-2.3 Flip-Flop PD

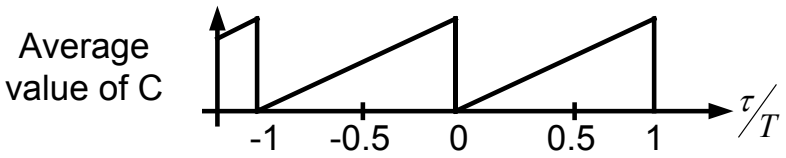
(a)



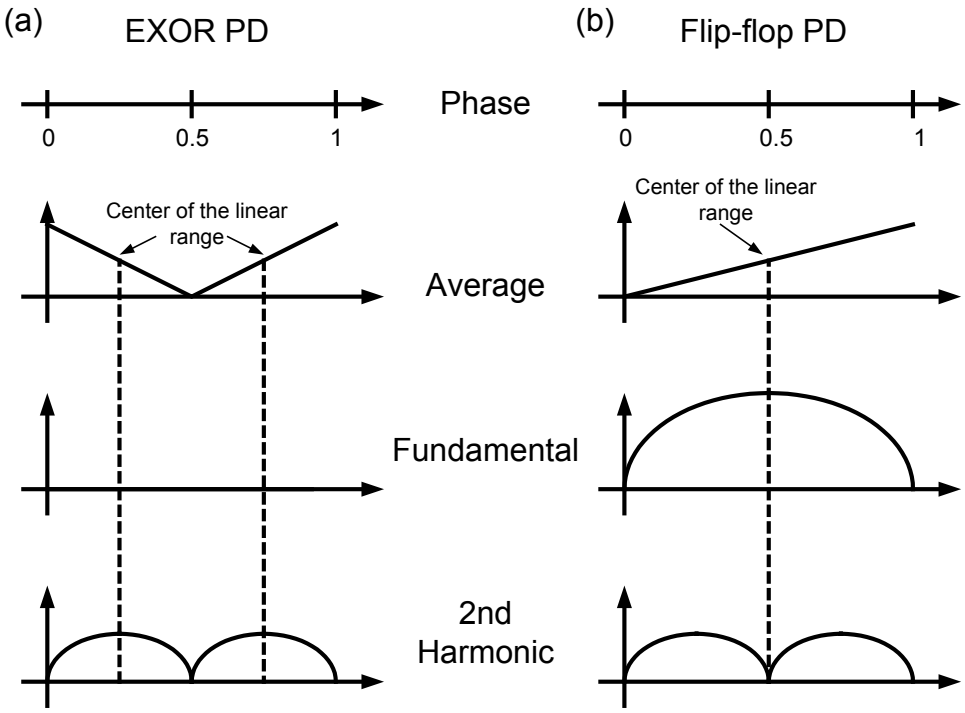
(b)



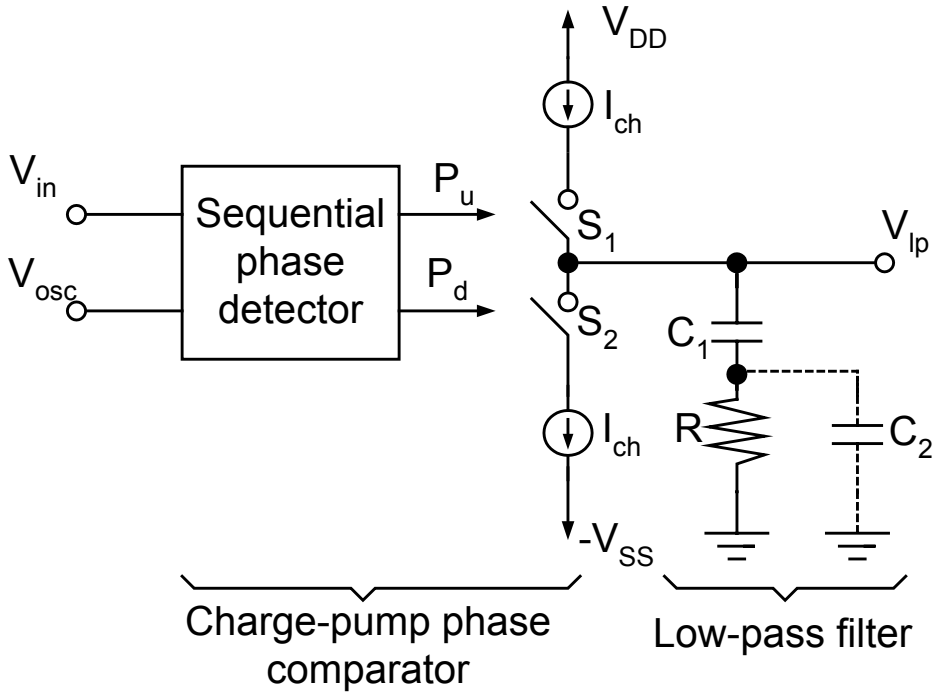
(c)



* The average value of V_{pd} or C has the shape of a saw tooth, with a linear range of a full cycle.
* At the center of the linear range of V_{pd} average, the most important harmonic is situated at the fundamental of the reference frequency as compared to the twice of reference frequency in the EXOR PD.

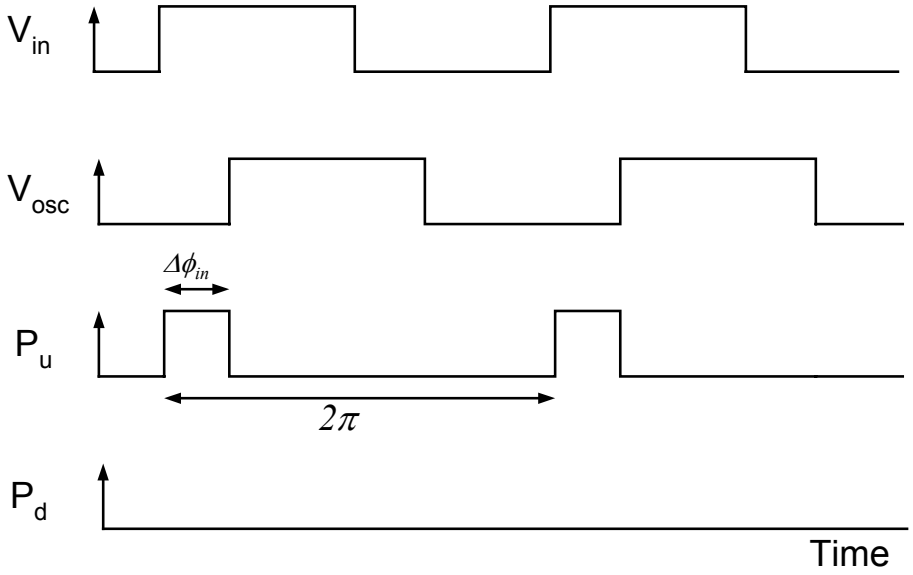


§17-2.4 Charge-pump PD



1. Desirable features: 1. It does not exhibit false lock.
   2. V_{in} and V_{osc} are exactly in phase when the loops in lock.
   3. The PLL attains lock quickly even when ω_{in} is quite different from ω_{fr}.

Some typical waveforms of a charge-pump PD



2.Small-signal analysis of a charge-pump PLL:

The average charge flow into the lowpass filter is

$$I_{avg}=\frac{\Delta\phi_{in}}{2\pi}I_{ch}$$

$$I_{avg}=K_{pd}(\phi_{in}-\phi_{osc})=K_{pd}\Delta\phi_{in}$$

$$\Rightarrow K_{pd}=\frac{I_{ch}}{2\pi}$$

For the lowpass filter R, C_1 has a transfer function $H_{lp}(s)$ as

$$H_{lp}(s)=\frac{V_{in}(s)}{I_{avg}(s)}=R+\frac{1}{SC_1}=\frac{1+SRC_1}{SC_1}$$

Substituting $H_{lp}(s)$ and K_{pd} into the transfer function $\frac{V_{lp}(s)}{\phi_{in}(s)}$,

we have

$$\frac{V_{lp}(s)}{\phi_{in}(s)}=\frac{1}{K_{osc}}\frac{S(1+SRC_1)}{1+SRC_1+\frac{S^2C_1}{K_{pd}K_{osc}}}$$

$$\Rightarrow \omega_o=\sqrt{\frac{K_{pd}K_{osc}}{C_1}}$$

$$Q=\frac{1}{RC_1\omega_o}=\frac{1}{R\sqrt{C_1K_{pd}K_{osc}}}=\frac{1}{R}\sqrt{\frac{2\pi}{C_1I_{ch}K_{osc}}}$$

3. Design Considerations:

(1) Choose I_{ch} based on practical consideration like power dissipation and speed.

(2) ω_o is chosen according to the desired transient settling-time constant τ_{pll} as

$$\omega_o = \frac{1}{\tau_{pll}}$$

(3) C_1 is chosen from the equation of ω_o whereas R is chosen using the equation of Q. The chosen Q value is slightly less than what is eventually desired. R↑ => Q↓

(4) Add C_2 to minimize glitches.

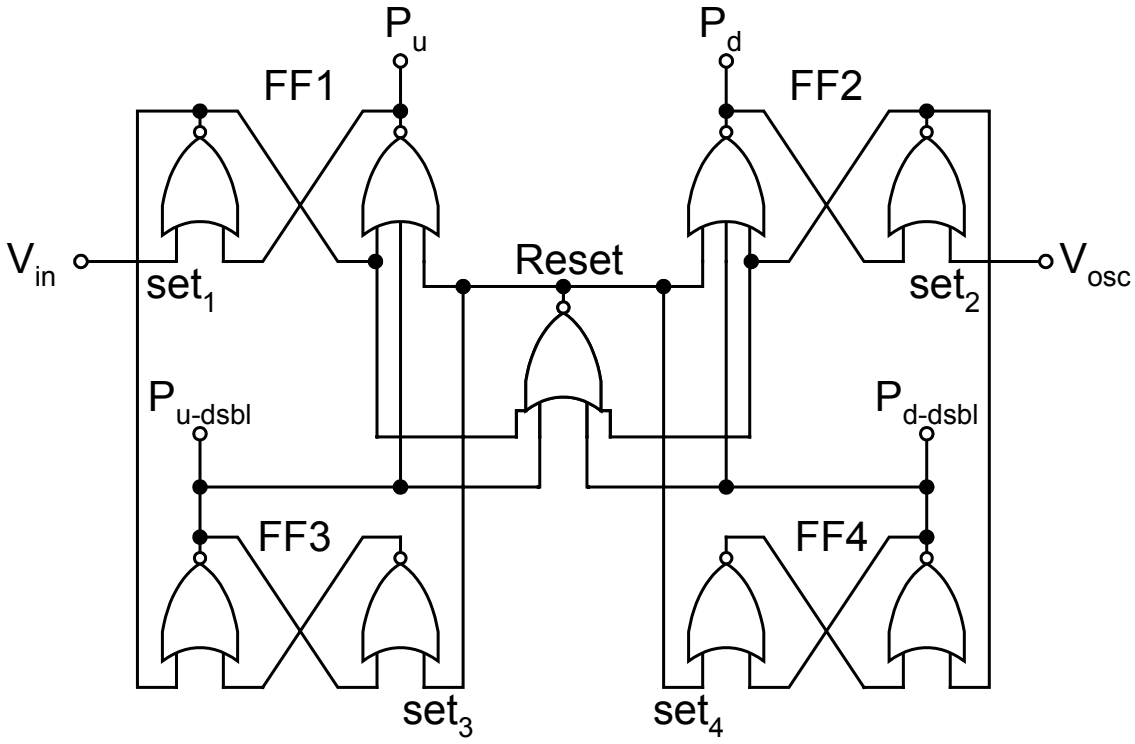
C_2 => Q↑ => chosen Q value is smaller => Exact Q.

$C_2 \cong \frac{1}{8} \sim \frac{1}{10}$ of C_1

$$\Rightarrow H_{lp}(s) = \frac{R}{1+SRC_2} + \frac{1}{SC_1}$$

4. Phase/Frequency detector (PFD)

* The most common sequential phase detector is the PFD.
* Asynchronous sequential logic circuit.
* 4 NOR-type RS flip-flops.
* Can also be realized in NAND gates.



* Basic operating principle:

Assume the PLL is in lock with V_{in} leading V_{osc}

Initial conditions: P_u=0, P_d=0, $P_{u\text{-}dsbl}$=0, $P_{d\text{-}dsbl}$=0, Reset=0 V_{in}=0, V_{osc}=0

inputs: 1001

$V_{in}\rightarrow 1$ => $P_u=1$ => Charge pumping starts and $V_{lp}\uparrow$=> $\omega_{osc}\uparrow$

$V_{osc}\rightarrow 1$ => Reset nor gate inputs: $0001\rightarrow 0000$ => Reset $0\rightarrow 1$

=> $P_u=0$ and $P_d=0$ after one gate-delay ; P_d $0\rightarrow 1\rightarrow 0$

$P_{u\text{-}dsbl}=1$ and $P_{d\text{-}dsbl}=1$ after two gate-delays.

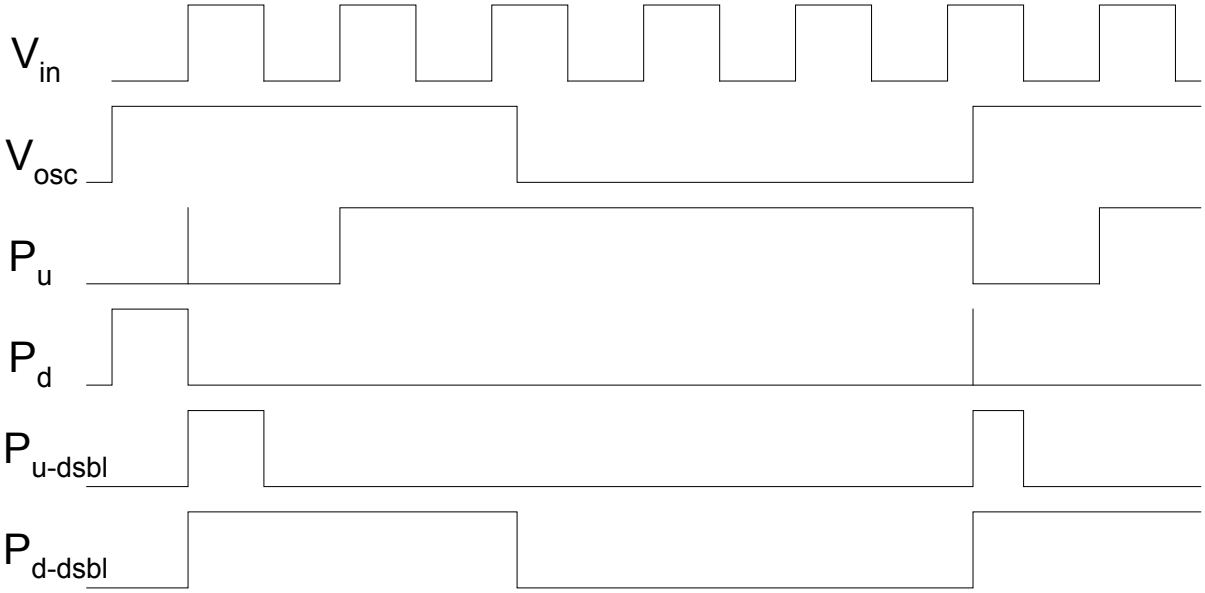
=> Reset $1\rightarrow 0$ after one gate-delay of $P_{u\text{-}dsbl}\rightarrow 1$ and $P_{d\text{-}dsbl}\rightarrow 1$ or after three gate-delays of $V_{osc}\rightarrow 1$.

=> Keeping $P_u=0$ and $P_d=0$ => No charge pumping.

It is only when V_{in} $1\rightarrow 0$ => FF3 is reset and $P_{u\text{-}dsbl}=0$

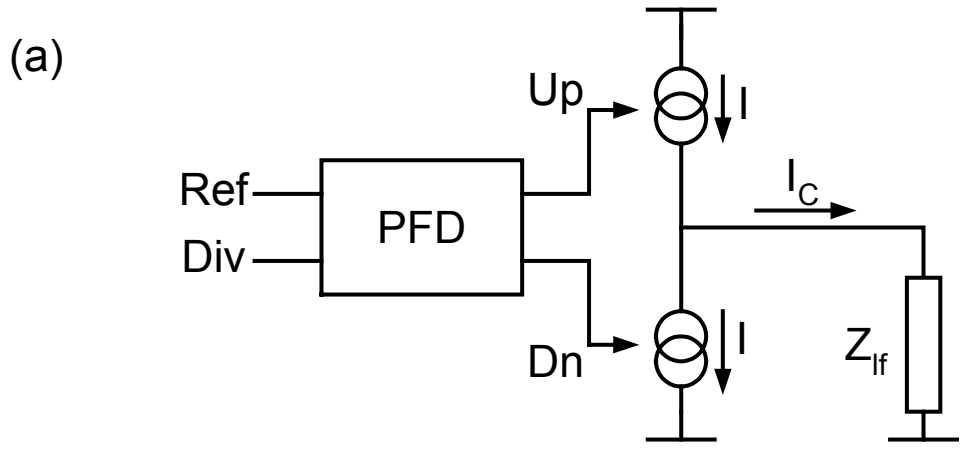
V_{osc} $1\rightarrow 0$ => FF4 is reset and $P_{d\text{-}dsbl}=0$

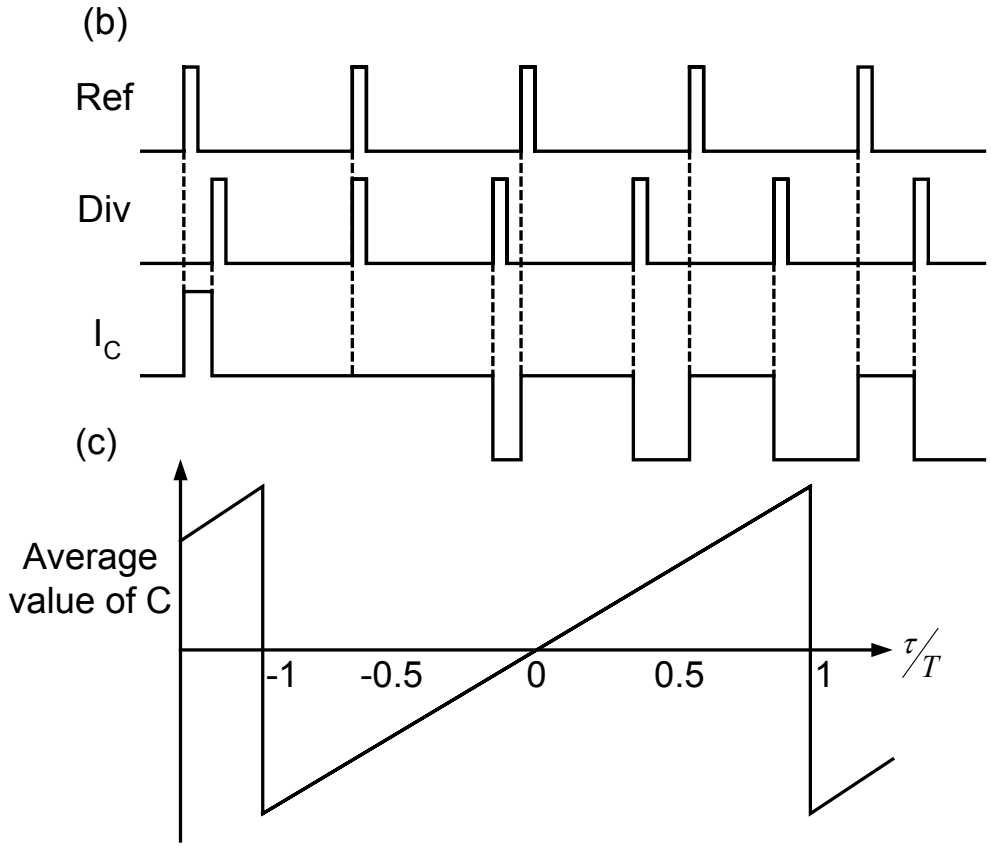
* The waveforms of a PFD when V_{in} is at a higher frequency than V_{osc}.



$\omega_{in}>\omega_{osc}$ => $P_u=1$ => Charge pumping to increase ω_{osc} until lock is achieved.

* Transfer characteristic of a charge-pumping PFD





§17-3 Loop Filters and Loop Gains

§17-3.1 First-order PLL with zero-order loop filter

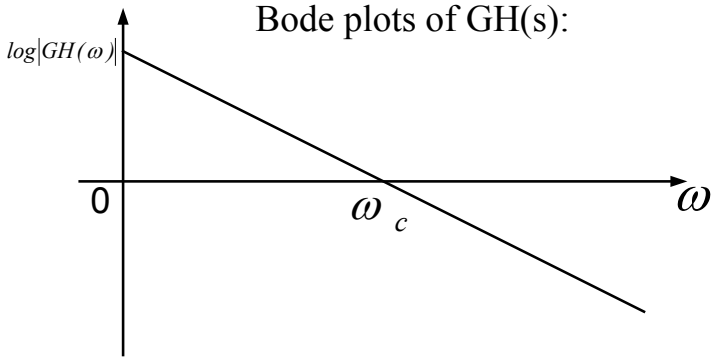
Loop gain of the feedback structure with $\phi_{in}(s)$ and $V_{cntl}(s)$

$$\text{Loop gain}=GH(s)=K_{pd}\,K_{lp}\,K_{osc}H_{lp}(s)\frac{1}{s}$$

Zero-order loop filter: $H_{lp}(s)=1$

$$\Rightarrow GH(S)=K_{pd}K_{lp}K_{osc}\frac{1}{s}$$

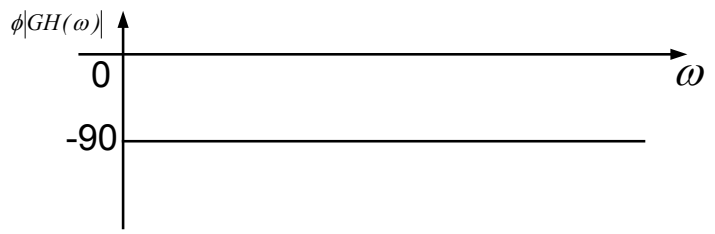
Bode plots of GH(s):



PLL with zero-order loop filter
=> First-order type-1 PLL

$$\frac{V_{cntl}(s)}{\phi_{in}(s)}=\frac{SK_{pd}K_{lp}}{S+K_{pd}K_{lp}K_{osc}}$$

close-loop transfer function

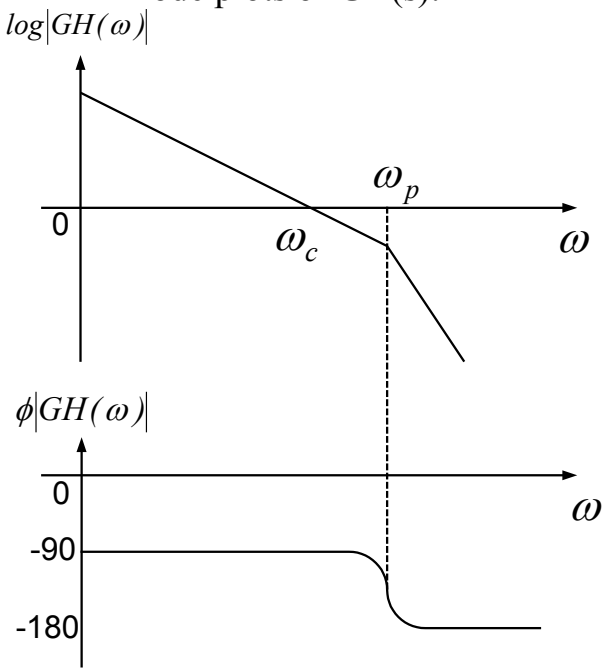


§17-3.2 Second-order PLL with first-order loop-filter

First-order loop filter: $H_{lp}(s)=\frac{1}{1+S/\omega_p}$

$$\Rightarrow GH(s)=\frac{K_{pd}K_{lp}K_{osc}}{S(1+S/\omega_p)}=\frac{\omega_p K_{pd}K_{lp}K_{osc}}{S^2+\omega_p S}$$

Bode plots of GH(s):



PLL with first-order loop filter
=> 2nd-order type-1 PLL

$$\frac{V_{cntl}(s)}{\phi_{in}(s)}=\frac{S\omega_p K_{pd}K_{lp}}{S^2+\omega_p S+\omega_p K_{pd}K_{lp}K_{osc}}$$

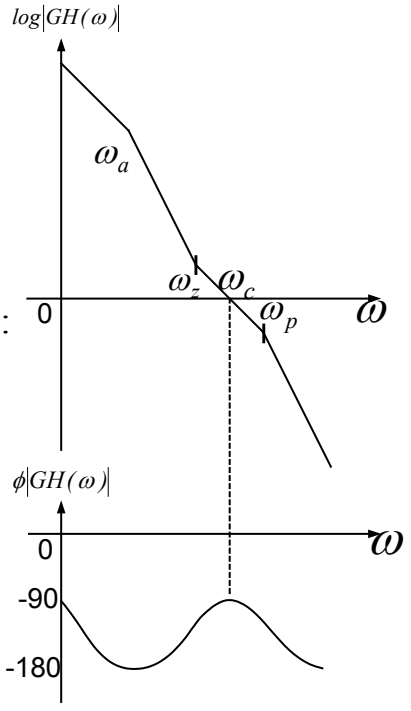
§17-3.3 Third-order PLL with second-order loop filter

To improve the transient characteristics of the PLL, a low-frequency pole ω_a is introduced in the loop filter. => Extra phase shift of 90°.
To compensate the extra phase shift, a compensating zero ω_z must be introduced in order to keep the phase margin high enough.

2nd-order loop filter: $H_{lp}(s)=\frac{(1+S/\omega_z)}{(1+S/\omega_p)(1+S/\omega_a)}$

$$\Rightarrow GH(S)=\frac{K_{pd}K_{lp}K_{osc}(1+S/\omega_z)}{S(1+S/\omega_p)(1+S/\omega_a)}$$

Bode plots of GH(S):



=> Third-order type-1 PLL

$$\frac{V_{cntl}(s)}{\phi_{in}(s)}=\frac{S(1+S/\omega_z)K_{pd}K_{lp}}{S(1+S/\omega_p)(1+S/\omega_a)+K_{pd}K_{lp}K_{osc}(1+S/\omega_z)}$$

If $\omega_a=0$
=> Third-order type-2 PLL.

§17-3.4 Third-order type-2 charge-pump PLL

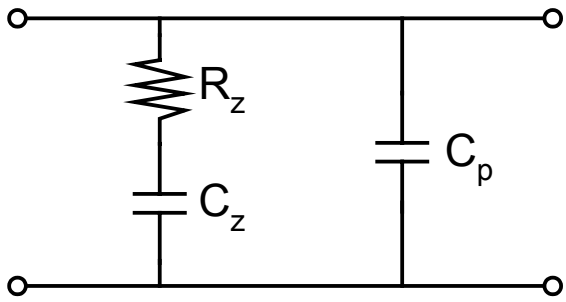
$$H_{lp}(s)=\frac{1+s\tau_z}{s(C_Z+C_p)[1+s\tau_p]}$$

$\tau_z = R_zC_z$

$\tau_p = R_z(C_z^{-1}+C_p^{-1})^{-1}$

$$\Rightarrow GH(s)=\frac{K_{pd}K_{lp}K_{osc}(1+s\tau_z)}{S^2(C_z+C_p)(1+s\tau_p)}$$

Loop filter:



§17-4 Voltage-Controlled Oscillators (VCOs)

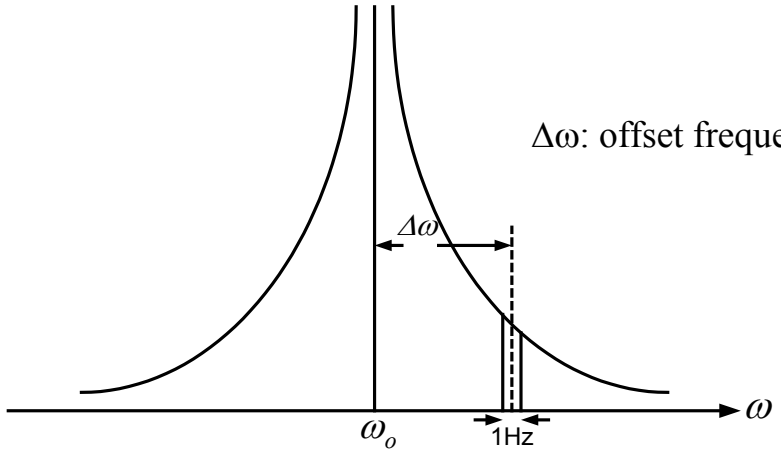
Basic VCO specifications/requirements:

1. phase stability:

The output spectrum of the VCO should approximate as good as possible the theoretical Dirac-impulse of a single sine wave, i.e. low phase noise.

The definition of phase noise:

$$L\{\Delta\omega\}=10\log\left(\frac{\text{noise power in a 1-Hz bandwidth at freq. } \omega+\Delta\omega}{\text{carrier power}}\right) \text{ units: dBc/Hz}$$



VCO output

2. Electrical tuning range

The VCO must be able to cover the complete required frequency band of the application, including initial frequency offsets due to process variations.

3. Tuning linearity

To simplify the design of the PLL, the VCO gain K_{osc} should be

constant.

4. Frequency pushing (MHz/V)

The dependency of the center frequency on the power supply voltage.

5. Frequency pulling

The dependence of the center frequency

6. Low cost

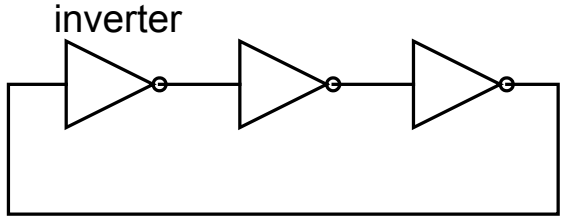
§17-4.1 Relaxation oscillator as VCO

* Multivibrator-based nonlinear oscillator.
* f_{osc}~in the order of a few 100 MHz
* In CMOS, phase noise value of -90dBc/Hz at 500KHz offset.
  Ref.: IEEE JSSC, vol.23, pp.1386-1393, Dec. 1988.

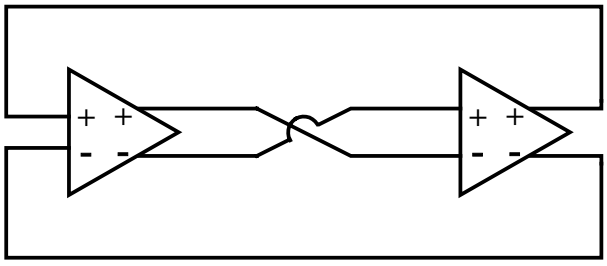
§17-4.2 Ring oscillator as VCO

* $T_{osc}=2n \bullet T_d$ n: number of inverters; T_d: one inverter delay.
* Tuning: varying the current of the inverters.
* High phase noise: ∵switching action introduces a lot of disturbances.
* Power consumption ↑ linearly => phase noise↓
* Typical phase noise:
  -94dBc/Hz at 1 MHz offset from a 2.2GHz carrier.
  -83dBc/Hz at 100 KHz offset from a 900MHz carrier.
* Circuit structure

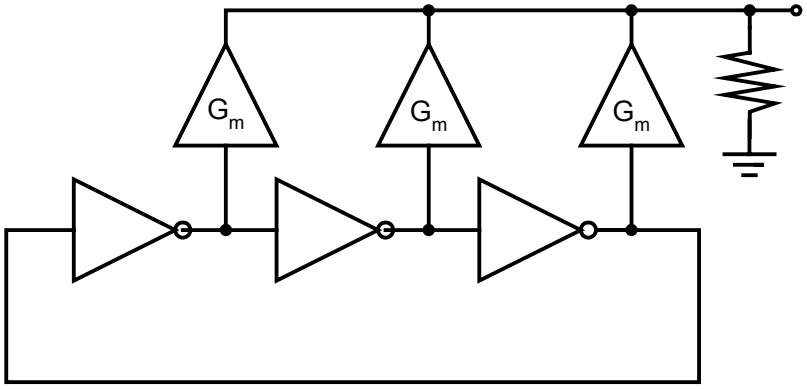
1. Three-stage ring oscillator



2. Differential two-stage ring oscillator



3. 1-stage-delay ring oscillator



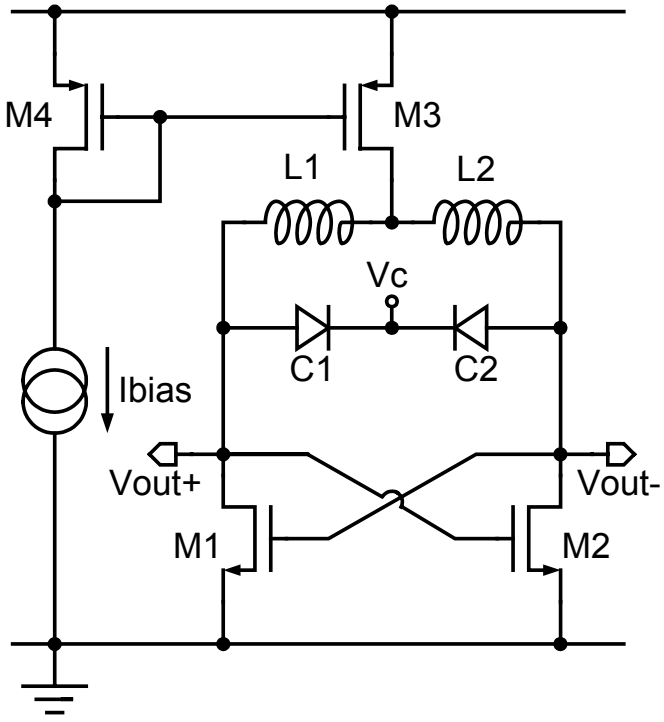
* f_{osc} MHz ~ GHz

Ref.: 1. Proc. of IEEE 1995 Custom Integrated Circuits Conference (CICC), pp.331-334.
2. IEEE JSSC, vol.31, pp.331-334, March 1996.

§17-4.3 LC-oscillator as VCO

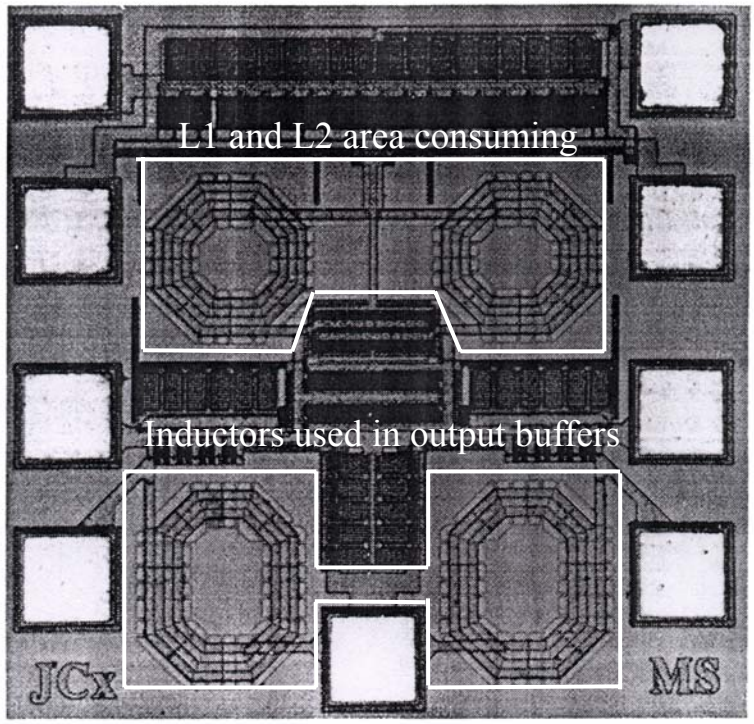
* Typically a 20dB better phase noise obtained over ring and relaxation oscillators.
* High-speed operation is possible due to the simple working principle.
* The realization of the inductor is the key point.

Design example: 0.7μm CMOS planar-LC VCO.



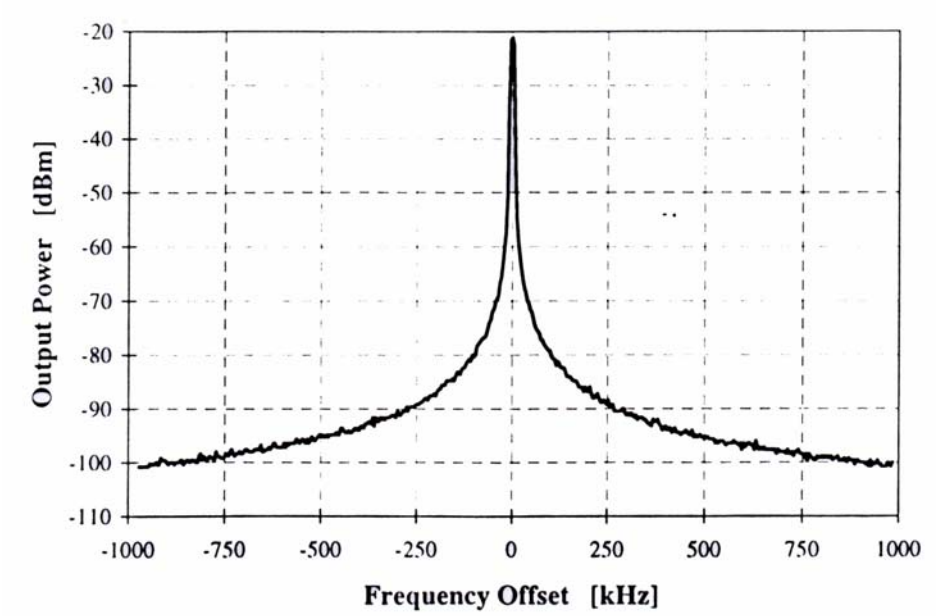
* Constant current => To limit power dissipation
* M_1 and M_2: To provide a negative resistance for oscillation
* L_1=L_2=3.2nH planar spiral inductors
* p^+ – n-well junction diodes C_1 and C_2 as varactors for frequency tuning by V_c.
  C_1=$C_2 \cong$ 1pF
* Different output voltage.

Chip photograph of the VCO. (Die size 750×750 μm^2)

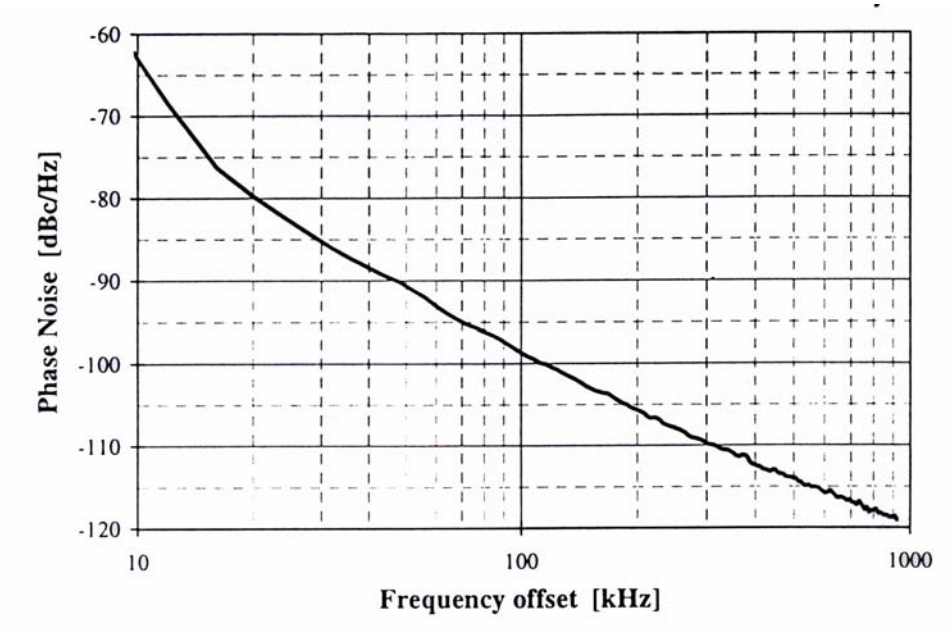


Measurement results:

1. Measured output spectrum for a carrier frequency of 1.81 GHz.

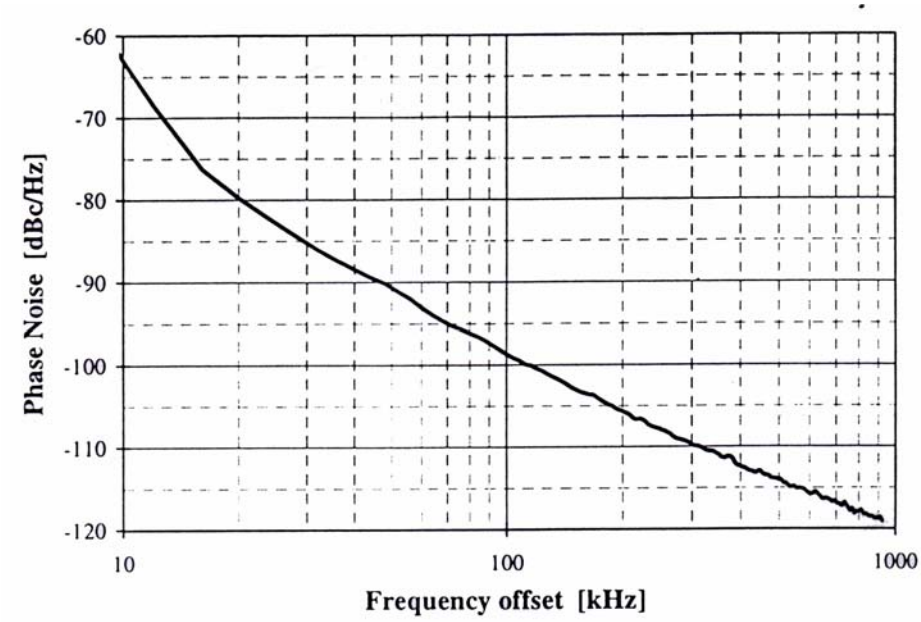


2. Measured phase noise w.r.t. frequency offset



Phase noise: -116dBc/Hz at 600 KHz offset

3. Measured frequency tuning characteristics



* At V_c=0.5V, the diode varactors C_1 and C_2 have a larger leakage current => Phase noise ↑ 3dB.

§17-4.4 Comparisons of Integrated VCOs

Reference	Technology [-]	Freq. [GHz]	Power [mW]	Tuning [%]	Phase noise [dBc/Hz]		Remarks
					reported	equiv.*	
Relaxation oscillators							
[Banu JSSC88]	0.75-um CMOS	0.56	50	100	-90 @500kHz	-81	Tuning from 100kHz to1GHz
[Sneep JSSC90]	3-GHz Bip	0.1	30	100	-118 @1MHz	-90	Tuning from low freq. to 150MHz
[Dobos CICC94]	9-GHz Bip	0.4	?	100	-110 @1MHz	-92	Tuning from 800kHz to 800MHz; Fast start-up
Ring oscillators							
[Kwasn CICC95]	1.2-um CMOS	0.74	6.5	6	- 89 @100kHz	-97	Comparison of 3 designs
[Razav JSSC96]	0.5-um CMOS	2.2	NA	NA	-94 @1MHz	-91	Three-stage; differential gain stage
[vd Tan ISSCC97]	9-GHz BiCMOS	2.0	NA	95	-106 @2MHz	-96	Two-stage CCO; stacked with mixer
LC-tuned oscillators							
[Nguye JSSC92]	10-GHz Bip	1.8	70	10	-88 @100kHz	-104	High-ohmic substrate; tuning with 2 tanks
[Based ESSC94]	1-um CMOS	1.0	16	0	-95 @100kHz	-105	Wide metal turns; substrate back-etched
[Soyue JSSC96a]	12-GHz BiCMOS	2.4	50	0	-92 @100kHz	-110	4-level, extra thick metal; high-ohmic substrate
[Ali ISSCC96]	25-GHz Bip	0.9	10	N.A.	-101 @100kHz	-110	Complete PLL; planar inductors

*at 600 kHz offset from a 1.8-GHz carrier

Reference	Technology [-]	Freq. [GHz]	Power [mW]	Tuning [%]	Phase noise [dBc/Hz]		Remarks
					reported	equiv.	
LC-tuned oscillators(cont'd)							
[Rofou ISSCC96]	1-um CMOS	0.9	10..40	14	-85 @ 100kHz	-95	Front-etched inductors; quadrature signals
[Soyue JSSC96b]	0.5-um BiCMOS	4.0	12	9	-106 @ 1MHz	-109	Thick metal (2.1 μm) and field oxide (11μm)
[Razav ISSCC97]	0.6-um CMOS	1.8	15	7	-100 @ 500kHz	-102	Linear tuning; quadrature signals
[Dauph ISSCC97]	11-GHz BiCMOS	1.5	40	10	-105 @ 100kHz	-119	Hollow rectangular coils standard process
[Janse ISSCC97]	15-GHz Bip	2.2	43	11	-99 @ 100kHz	-116	High-Q MIS capacitor and varactor
[Parke CICC97]	0.6-um CMOS	1.6	NA	12	-105 @ 200kHz	-114	Full PLL circuit; capacitor bank for extended tuning
Presented designs							
[Steya EL94]	6-GHz Bip	1.1	1	0	-75 @ 10kHz	-106	Bonding wire inductor
[Crani JSSC95]	0.7-um CMOS	1.8	24	5	-115 @ 200kHz	-124	Bonding wire inductor; enhanced LC-tank
[Crani JSSC97]	0.7-um CMOS	1.8	6	14	-116 @ 600kHz	-116	2-level metal; conductive substrate; standard CMOS
[Crani CICC97]	0.4-um CMOS	1.8	11	20	-113 @ 200kHz	-122	2-level metal; standard CMOS

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