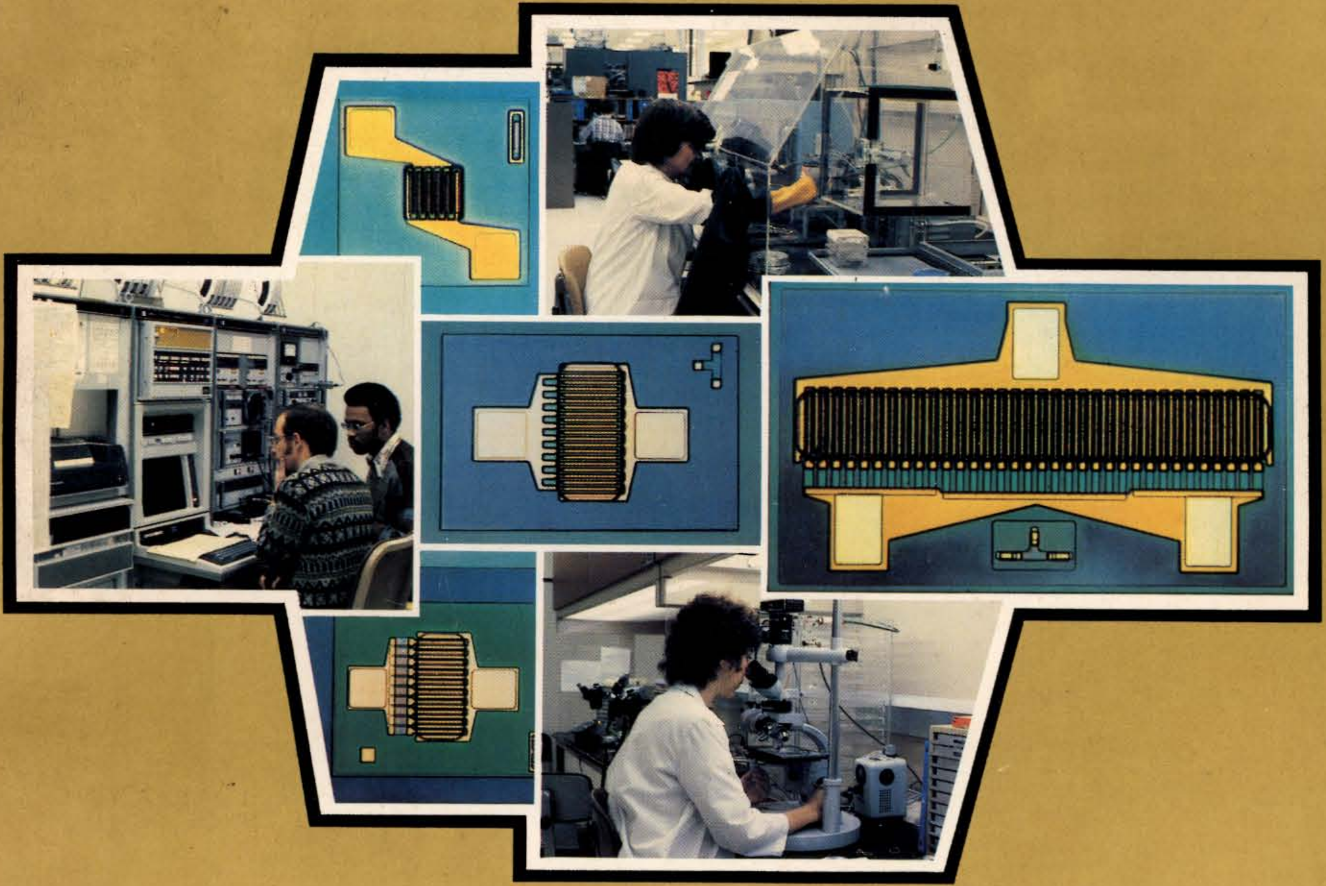


Diode and Transistor Designer's Catalog 1980

HEWLETT hp PACKARD

COMPONENTS

1980 Diode and Transistor Designer's Catalog

Table of Contents

NEW Identifies newly introduced products or capabilities. New products are also indicated by boldface listings in the Numeric Index.

A Brief Sketch

Hewlett-Packard is one of the world's leading designers and manufacturers of electronic, medical, analytical, and computing instruments and systems, diodes, transistors, integrated products, and optoelectronic products. Since its founding in Palo Alto, California, in 1939, HP has done its best to offer only products that represent significant technological advancements.

To maintain its leadership in instrument and component technology, Hewlett-Packard invests heavily in new product development. Research and development expenditures traditionally average about 10 percent of sales revenue, and 1,500 engineers and scientists are assigned the responsibilities of carrying out the company's various R and D projects.

HP produces more than 3,500 products at 30 domestic divisions in California, Colorado, Oregon, Idaho, Massachusetts, New Jersey and Pennsylvania and at overseas plants located in the German Federal Republic, Scotland, France, Japan, Singapore, Malaysia and Brazil.

However, for the customer, Hewlett-Packard is no further away than the nearest telephone. Hewlett-Packard currently has sales and service offices located around the world.

These field offices are staffed by trained engineers, each of whom has the primary responsibility of providing technical assistance and data to customers.

A vast communications network has been established to link each field office with the factories and with corporate offices. No matter what the product or the request, a customer can be accommodated by a single contact with the company.

Hewlett-Packard is guided by a set of written objectives. One of these is "to provide products and services of the greatest possible value to our customers". Through application of advanced technology, efficient manufacturing, and imaginative marketing, it is the customer that the more than 40,000 Hewlett-Packard people strive to serve. Every effort is made to anticipate the customer's needs, to provide the customer with products that will enable more efficient operation, to offer the kind of service and reliability that will merit the customer's highest confidence, and to provide all of this at a reasonable price.

To better serve its many customers broad spectrum of technological needs, Hewlett-Packard publishes several catalogs. Among these are:

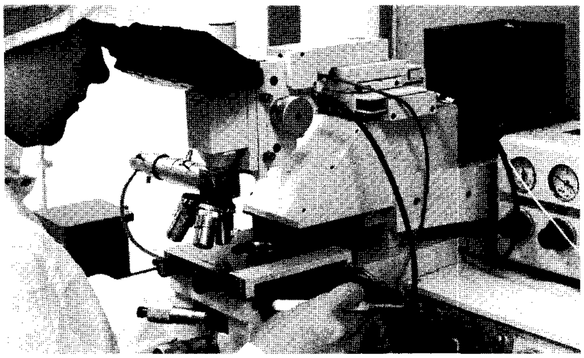
- Electronic Instruments and Systems for Measurement/Computation (General Catalog)
- DC Power Supply Catalog
- Medical Instrumentation Catalog
- Analytical Instruments for Chemistry Catalog
- Coax, and W/G Measurement Accessories Catalog
- Optoelectronics Designer's Catalog
- Integrated Products Catalog

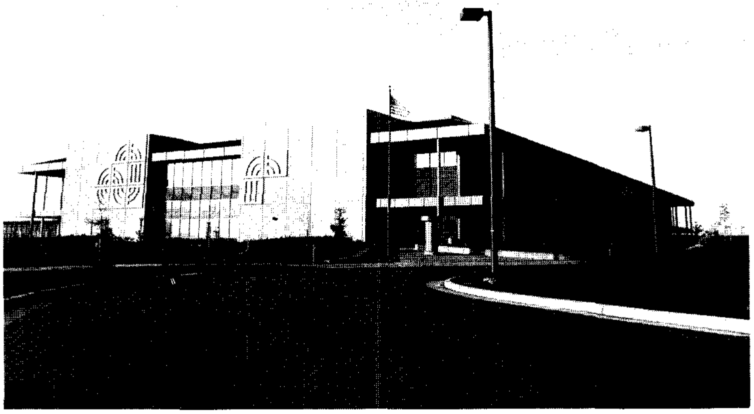
All catalogs are available at no charge from your local HP sales office, or write: Inquiries Mgr., Hewlett-Packard, 1507 Page Mill Road, Palo Alto, CA 94304.

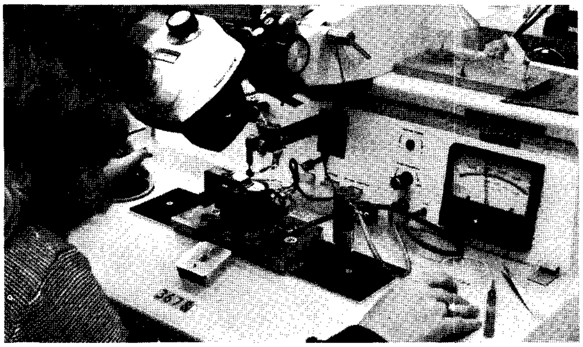
RF and Microwave Semiconductors

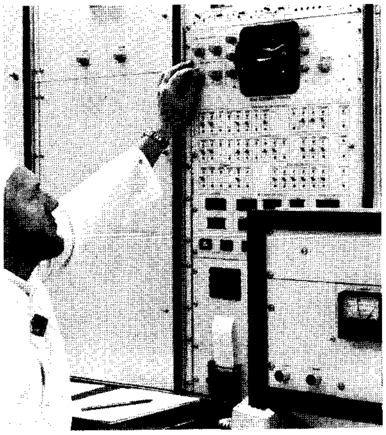
Hewlett-Packard has invested in a new 180,000 square foot manufacturing plant in San Jose, California. It houses modern equipment such as a computer controlled wafer fabrication facility which includes projection mask aligning and automation handling systems.

Ion implantation, new evaporation and wet processing systems, and scanning electron microscopy provide the basis for quality and dependability for the entire product line.









About This Catalog

This Diode and Transistor Designer's Catalog contains detailed and up-to-date specifications of our complete line of RF and microwave products. The catalog is divided into 8 product sections: Silicon Bipolar Transistors, Gallium Arsenide Field Effect Transistors, Schottky Barrier and High Conductance Diodes, PIN Diodes, IMPATTS and Step Recovery Diodes, Devices for Hybrid Integrated Circuits and High Reliability Devices. At the end of each section, a selection of application notes pertaining to the use of those products is included.

Also included in each section where possible are the equivalent circuits of each product. These will be of use in the computer-aided design circuits.

All chip, beam lead, LID and ministrip products are in the section Devices for Hybrid Integrated Circuits, and in general, contain references to equivalent packaged parts.

In all of the transistor product data sheets, two tables for maximum ratings are shown. Recommended Maximum Continuous Operating Conditions indicate the conditions within which the device should be operated in order to meet the MTBF design goals for the device. The Absolute Maximum Ratings table indicates the limits of the device. Operation in excess of any of these conditions may result in permanent damage to the device. Package outlines are included in the Appendix. Also included are some commonly used Engineering tables.

The catalog also provides a complete index of microwave semiconductor application notes on page 250 which are available from any of the Franchised Distributors listed on page 255.

How To Use This Catalog

Three methods are incorporated for locating components:

- A table of contents that allows you to locate devices by their general description.
- An alphanumeric index that lists all devices by part number plus generic chip part numbers.
- Selection guides at the beginning of each product section generally grouping products by major specification, frequency, etc.

Although product information and illustrations in these catalogs were current at the time it was approved for printing, Hewlett-Packard, in a continuing effort to offer excellent products at a fair value, reserves the right to change specifications, designs, and models without notice.

Other Literature Available

Each HP product is completely described on a Technical Data Sheet. Technical measurement information is contained in a comprehensive series of Application Notes. Various Application Notes of interest to those working in the RF and Microwave field are referenced on page 250.

The HP Journal is a monthly journal of technical information from the laboratories of HP, and is available upon request. Measurement/Computation News, published six times per year, may be requested if you want announcements of new products.

Ordering Information, After Sales Services

How To Order

Hewlett-Packard people at the field office will be pleased to provide assistance in selecting the HP equipment most appropriate to your needs, and help you prepare your order.

The information in this catalog will, in many cases, be sufficient for you to purchase a particular HP product. In those instances, a telephone call to the HP office will provide you with (1) information on product availability, and (2) the product's price, delivered to your location.

We want to be sure the product delivered is the one you want. Therefore, when placing your order, please specify the product's catalog part number, as well as the product's name. Be as complete as possible when ordering.

NOTE: Minimum order in USA $20, except where cash is received with order.

Terms of Sale

Inside the USA: Terms are net 30 days from invoice date. Unless credit with Hewlett-Packard has already been established, shipments will be made COD or on receipt of cash in advance.

Outside the USA: Terms of orders from customers outside the United States of America which are placed with Hewlett-Packard Company, Hewlett-Packard S.A., or Hewlett-Packard Inter-Americas, are irrevocable letters of credit or cash in advance — unless other terms have been previously arranged. Terms of orders placed with authorized Hewlett-Packard representatives or distributors are mutually determined between the customer and the representative or distributor organization.

Warranty

As an expression of confidence in our products to continue meeting the high standards of reliability and performance that customers have come to expect, Hewlett-Packard Microwave Semiconductor Products carry the following warranty contained in the operating and service manual provided with the product:

HP's Components are warranted against defects in material and workmanship for a period of one year from the date of shipment. HP will repair or, at its option, replace Components that prove to be defective in material or workmanship under proper use during the warranty period. This warranty extends only to HP customers.

No other warranties are expressed or implied. HP specifically disclaims the implied warranties of merchantability and fitness for a particular purpose.

EXCLUSIVE REMEDIES

The remedies provided herein are buyer's sole and exclusive remedies. HP shall not be liable for any direct, indirect, special, incidental, or consequential damages, whether based on contract tort or any other legal theory.

Certification

Some customers are especially interested in the test and quality assurance programs that HP applies to its products. These Hewlett-Packard programs are documented in a Certificate of Conformance which is available upon request at the time of purchase. This certification states:

We certify that the Microwave Semiconductor Division devices listed below were duly tested and inspected prior to shipment and that they met all of the published specifications for these devices.

Hewlett-Packard's calibration measurements are traceable to the National Bureau of Standards to the extent allowed by the Bureau's calibration facilities.

The Hewlett-Packard Quality Program satisfies the requirements of MIL-Q-9858A, MIL-I-45208A, MIL-C-45662A, and NASA 5300.4 (I.C.).

Service

We firmly believe that our obligation to you as a customer goes much beyond just the delivery of your new HP product. This philosophy is implemented by Hewlett-Packard in two basic ways: (1) by designing and building excellent products with good serviceability, and (2) by backing up those products with a customer service program which can respond to your needs with speed and completeness.

The HP customer service program is one of the most important facets of our worldwide operations, providing a local service capability in many of our field offices (listed on page 257). Indeed, this customer service program is one of the major factors in Hewlett-Packard's reputation for integrity and responsibility towards its customers.

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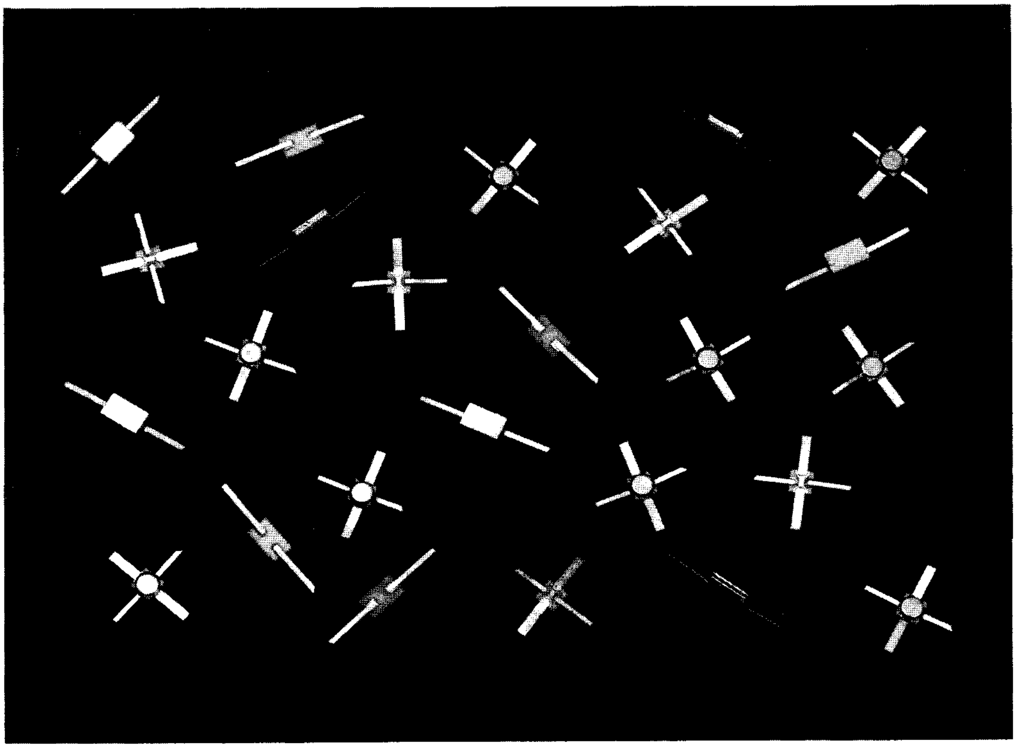
Microwave GaAs FETS



GaAs Field Effect Transistor Selection Guide

LOW NOISE FETS

Part Number HFET-	Chip Equivalent HFET-	Typical Noise Figure	Typical Associated Gain	Frequency	Package HPAC-	Page Number
2201	2001	2.4 dB	9.2 dB	10 GHz	170	6
2202	2001	1.1 dB	13.6 dB	4 GHz	100A	9
1102	1001	1.4 dB	12 dB	4 GHz	100A	3
(2N6680) 1101	1001	1.6 dB	11 dB	4 GHz	100A	3

GENERAL PURPOSE FETS

Part Number	Chip Equivalent HFET-	Typical Gain	Typical P_{1dB}	Frequency	Package HPAC-	Page Number
2N6680 (HFET-1101)	1001	16 dB	15.5 dBm	4 GHz	100A	3

HEWLETT PACKARD
COMPONENTS

MICROWAVE GaAs FETS

NEW

2N6680
(HFET-1101)
HFET-1102

48.44
68.31

Features

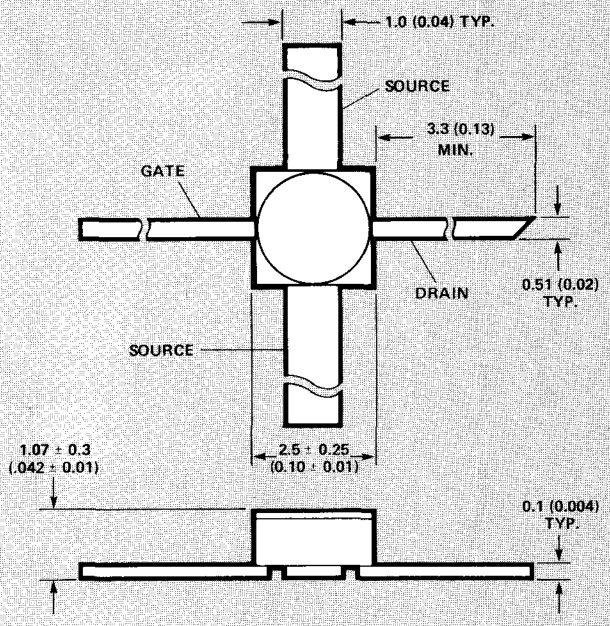
LOW NOISE FIGURE
- **1.6 dB Typical at 4 GHz (2N6680)**
- **1.7 dB Maximum at 4 GHz (HFET-1102)**
  - **1.5 dB Typical**

HIGH GAIN
- **16 dB Typical at 4 GHz**

HIGH OUTPUT POWER
- **15.5 dBm Typical Linear Power Output at 4 GHz**

USABLE TO 12 GHz

RUGGED HERMETIC PACKAGE



DIMENSIONS IN MILLIMETERS (INCHES).

HPAC-100A Package Outline

Description/Applications

The 2N6680 (HFET-1101) and the HFET-1102 are gallium arsenide Schottky gate field effect transistors in a package suitable for narrow band operations to 12 GHz. Their superior microwave performance in noise figure and gain make them useful for applications such as land and satellite communications, and radar.

2N6680 (HFET-1101) and HFET-1102 are supplied in the HPAC-100A, a rugged metal/ceramic hermetic package, and are capable of meeting the requirements of MIL-S-19500.

The HFET-1102 is a low noise and gain selection of the 2N6680.

Electrical Specifications at $T_{CASE} = 25°C$

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
I_{DSS}	Saturated Drain Current, $V_{DS} = 4.0V$, $V_{GS} = 0V$	mA	40		120
V_{GSP}	Pinch Off Voltage, $V_{DS} = 4.0V$, $I_{DS} = 100\ \mu A$	V	-1.5		-5.0
g_m	Transconductance, $V_{DS} = 4.0V$, $\Delta V_{GS} = 0V$ to $-0.5V$	mmho	30	40	
$G_{a(max)}$	Maximum Available Gain $V_{DS} = 4.0V$, $V_{GS} = 0$ f = 4 GHz	dB		16	
F_{MIN}	Noise Figure 2N6680: f = 4 GHz HFET-1102: 4 GHz	dB		1.6 1.4	2.2 1.7
G_a	Associated Gain 2N6680: f = 4 GHz HFET-1102: 4 GHz $V_{DS} = 3.5V$, $I_{DS} = 15\%\ I_{DSS}$ (Typ. 12 mA)	dB	9.5 11.0	11.0 12.0	
P_{1dB}	Power at 1 dB Compression, $V_{DS} = 5.0V$, $I_{DS} = 50\%\ I_{DSS}$ f = 4 GHz Tuned for Maximum Output Power at +5 dBm Input 8 GHz	dBm		15.5 14.0	

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Values
V_{DS}	Drain to Source Voltage $-5.0V \le V_{GS} \le 0.0V$	5V
V_{GS}[2]	Gate to Source Voltage $5.0V \ge V_{DS} \ge 0.0V$	-5V
T_{CH}[3]	Maximum Channel Temperature	175°C
T_{STG}	Storage Temperature	-65°C to +175°C

1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device mean time between failure (MTBF) to below the design goal of 1 x 10^7 hours at T_{CH} = 150°C (assumed Activation Energy = 1.6 eV). Corresponds to Maximum Ratings for 2N6680.
2. Maximum Continuous Forward Gate Current should not exceed 2.5 mA.
3. Θ_{jc} — Thermal resistance, channel to case = 200°C/W.

Absolute Maximum Ratings[1]

Symbol	Parameter	Limits
V_{DS}	Drain to Source Voltage $-10V \le V_{GS} \le 0.0V$	11V
V_{GS}[2]	Gate to Source Voltage $10.0V \ge V_{DS} \ge 0.0V$	-10V
T_{CH}	Maximum Channel Temperature	300°C
$T_{STG(MAX)}$	Maximum Storage Temperature	250°C
Lead Soldering Temperature[3] 250°C for 10 sec. each lead.		

1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. Maximum forward Gate Current should not exceed 3 mA.
3. See Handling and Use Precautions. (page 13).

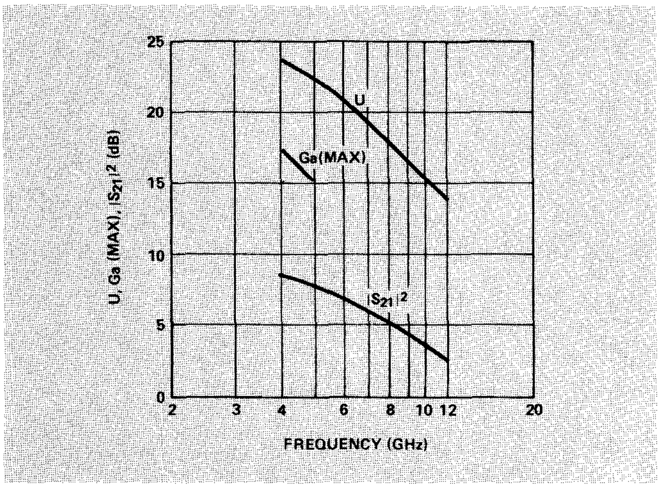


Figure 1. Typical Mason's Gain (U), $G_{a\ (max)}$, and $|S_{21}|^2$ vs. Frequency at V_{DS} = 4.0V, I_{DS} = 100% I_{DSS}.

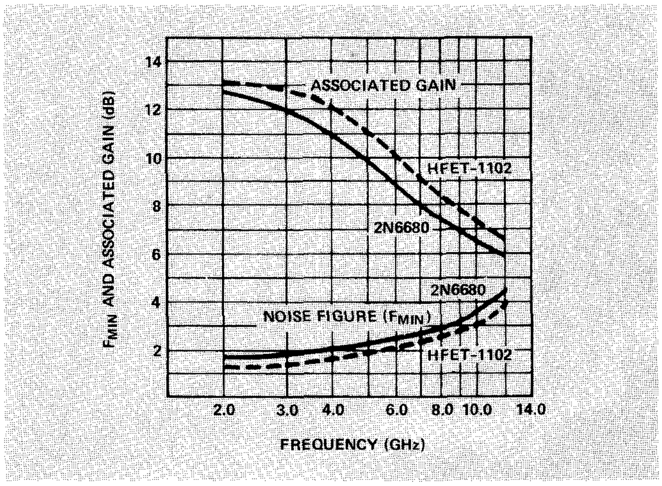


Figure 2. Typical Noise Figure (F_{MIN}) and Associated Gain vs. Frequency. V_{DS} = 3.5V, I_{DS} = 15% I_{DSS}.

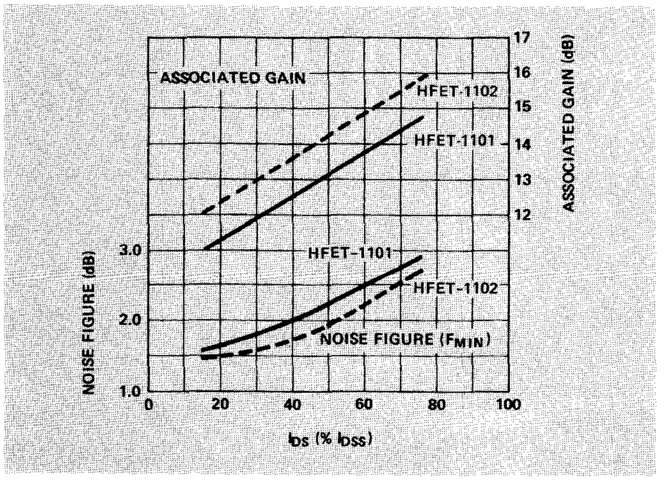


Figure 3. Typical Noise Figure and Associated Gain vs. Drain Current (I_{DS}) at 4 GHz, V_{DS} = 3.5V.

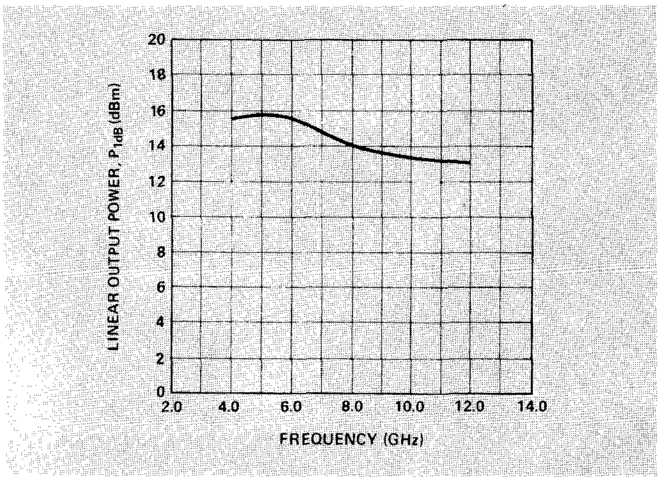


Figure 4. Typical Output Power at 1 dB Compression vs. Frequency. V_{DS} = 4.0V, I_{DS} = 50% I_{DSS}. Tuned for Maximum Output Power at +5 dBm Input.

Typical S-Parameters

High Gain Bias: $V_{DS} = 4.0V$, $V_{GS} = 0V$

Frequency, GHz	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
2.0	.894	-60.6	3.122	123.6	.020	62.4	.781	-27.6
3.0	.801	-88.9	2.863	98.9	.025	55.8	.755	-40.5
4.0	.720	-116.2	2.597	75.6	.028	56.7	.732	-54.0
5.0	.662	-142.2	2.391	53.8	.034	62.0	.723	-67.7
6.0	.614	-167.4	2.187	32.4	.046	65.0	.716	-83.0
7.0	.588	169.3	1.985	12.1	.061	61.6	.711	-100.1
8.0	.580	148.1	1.807	-7.2	.083	54.8	.708	-118.2
9.0	.585	128.9	1.650	-25.6	.103	40.4	.720	-136.5
10.0	.593	110.9	1.535	-43.9	.121	31.1	.744	-155.5
11.0	.589	94.0	1.433	-62.6	.145	17.9	.765	-174.3
12.0	.574	76.6	1.329	-81.9	.164	2.4	.779	167.0

Linear Power Bias: $V_{DS} = 4.0V$, $I_{DS} = 50\%\ I_{DSS}$

Frequency, GHz	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
2.0	.912	-57.8	2.836	125.2	.033	56.3	.705	-29.2
3.0	.829	-87.2	2.668	99.7	.044	41.7	.662	-43.7
4.0	.750	-116.5	2.458	74.5	.050	30.2	.632	-59.3
5.0	.683	-144.1	2.259	51.1	.054	21.5	.610	-76.3
6.0	.641	-171.3	2.053	28.5	.057	16.3	.572	-95.7
7.0	.625	164.1	1.847	6.3	.061	13.6	.556	-115.1
8.0	.621	142.7	1.664	-14.0	.069	9.8	.554	-133.0
9.0	.626	124.9	1.510	-33.1	.080	3.5	.589	-155.0
10.0	.627	108.4	1.382	-51.3	.095	-3.7	.609	-175.8
11.0	.615	92.4	1.257	-70.1	.106	-14.4	.614	166.3
12.0	.598	76.6	1.155	-88.0	.123	-26.1	.624	150.6

Minimum Noise Figure Bias: $V_{DS} = 3.5V$, $I_{DS} = 15\%\ I_{DSS}$

Frequency, GHz	S11		S21		S12		S22	
	Mag	Ang	Mag	Ang	Mag	Ang	Mag	Ang
2.0	.935	-51.9	2.166	128.3	.045	54.6	.733	-30.5
3.0	.862	-77.1	2.070	104.4	.060	39.3	.697	-45.4
4.0	.792	-102.4	1.955	81.1	.070	26.0	.659	-60.8
5.0	.733	-127.2	1.860	58.7	.074	14.8	.630	-76.0
6.0	.674	-152.0	1.740	36.4	.075	6.2	.600	-92.6
7.0	.631	-175.5	1.599	15.2	.074	1.3	.578	-110.8
8.0	.607	162.8	1.469	-4.4	.077	.5	.565	-129.5
9.0	.601	143.0	1.352	-23.4	.087	-6.2	.570	-148.4
10.0	.602	124.5	1.261	-41.8	.091	-10.3	.585	-167.6
11.0	.594	107.3	1.180	-60.5	.104	-16.4	.600	173.5
12.0	.575	90.0	1.101	-79.5	.119	-27.0	.613	154.6

Typical Noise Parameters[1]

2N6680 (HFET-1101) and HFET-1102

Frequency (GHz)	Γ_o		$\Gamma_L = [S_{22}']^*$		F_{MIN} (dB)	R_N (Ohms)
	Mag.	Ang.	Mag.	Ang.		
2.0	.730	60°	.829	44°	1.25	19.40
4.0	.618	98°	.656	75°	1.60	23.14
6.0	.575	138°	.601	104°	2.20	6.64
8.0	.617	-170°	.644	137°	2.80	1.88
10.0	.610	-128°	.693	-170°	3.60	25.47
12.0	.660	-87°	.749	-157°	4.50	49.10

Note:
1. Optimum Input Reflection Coefficient (Γ_o) Output Match for Minimum Noise (Γ_L), Associated Noise Figure (F_{MIN}) and Noise Resistance (R_N) at $V_{DS} = 3.5V$, $I_{DS} = 15\%\ I_{DSS}$.

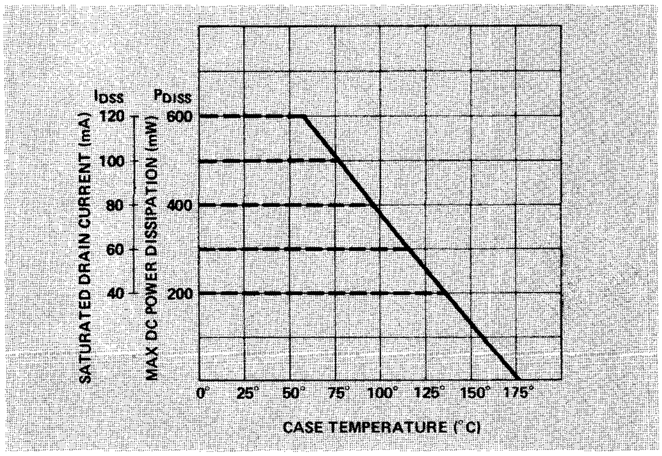


Figure 5. P_{DISS} vs. Temperature, Power Derating Curve at $V_{DS} = 5V$. Maximum power dissipation is a function of device I_{DSS}. Begin derating at P_{DISS} corresponding to individual device I_{DSS}, following a horizontal line until it intersects with solid diagonal line.

HEWLETT hp PACKARD
COMPONENTS

NEW

LOW NOISE BROADBAND MICROWAVE GaAs FET

HFET-2201

¥ 139.73

Features

LOW NOISE FIGURE
2.4 dB Typical NF at 10 GHz
3.1 dB Typical NF at 14 GHz

HIGH MAXIMUM AVAILABLE GAIN
14.5 dB Typical $G_{a(max)}$ at 10 GHz

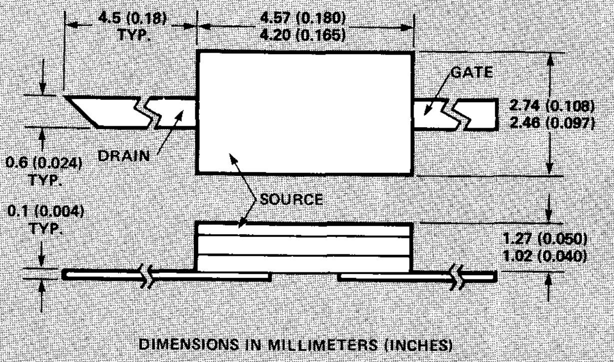
HIGH OUTPUT POWER
12 dBm Linear Power at 10 GHz

CHARACTERIZED TO 18 GHz

HERMETIC MICROSTRIP WIDEBAND PACKAGE

HIGH TRANSDUCER GAIN TO 18 GHz

0.5 MICROMETER GATE



HPAC-170 Package Outline

Description/Applications

The HFET-2201 is a gallium arsenide Schottky gate field effect transistor. It features a rugged, hermetic, microstrip compatible package that is designed for consistent broadband or narrow-band operation over the frequency range of 2 GHz to 18 GHz. The device's superior noise and gain performance, coupled with its wide dynamic range capability make it ideally suited for such applications as ECM, wideband surveillance, and warning systems.

In addition, its characteristics lend themselves to ease of circuit design in applications such as radar and communications equipment.

The HFET-2201 is packaged in the HPAC-170. The part is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

Electrical Specifications at $T_{CASE}=25°C$

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
I_{DSS}	Saturated Drain Current, V_{DS} = 3.5V, V_{GS} = 0V		mA	25	45	90
V_{GSP}	Pinch Off Voltage, V_{DS} = 3.5V, I_{DS} <500μA		V	-0.5	-2.0	-4.0
g_m	Transconductance, V_{DS} = 3.5V, ΔV_{GS} = 0V to -0.5V		mmho	20	32	45
$G_{a(max)}$	Maximum Available Gain V_{DS} = 3.5V, V_{GS} = 0V	f= 8GHz	dB		16.0	
		10GHz	dB		14.5	
		12GHz	dB		12.5	
F_{MIN}	Minimum Noise Figure V_{DS} = 3.5V, I_{DS} = 15% I_{DSS} (Typ. 7.5mA)	f= 4GHz	dB		1.2	
		10GHz	dB		2.4	2.8
		14GHz	dB		3.1	
G_a	Associated Gain At N.F. Bias	f= 4GHz	dB		14.1	
		10GHz	dB	8.0	9.2	
		14GHz	dB		8.0	
P_{1dB}	Power at 1dB Compression V_{DS} = 3.5V, I_{DS} = 50% I_{DSS} (0 dBm Input Matching, Tuned for Max. Output)	f=10GHz	dBm		12.0	

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Values
V_{DS}	Drain to Source Voltage $-4.0V \le V_{GS} \le 0.0V$	4V
V_{GS}[2]	Gate to Source Voltage $4.0V \ge V_{DS} \ge 0.0V$	-4V
T_{CH}[3]	Maximum Channel Temperature	125°C
T_{STG}	Storage Temperature	-65°C to +125°C

1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device mean time between failure (MTBF) to below the design goal of 1 x 10^7 hours at T_{CH} = 125°C (assumed Activation Energy = 1.6 eV).
2. Maximum Continuous Forward Gate Current should not exceed 1.5 mA.
3. Θ_{jc} — Thermal resistance, channel to case = 230°C/W.

Absolute Maximum Ratings[1]

Symbol	Parameter	Limits
V_{DS}	Drain to Source Voltage $-4V \le V_{GS} \le 0.0V$	10V
V_{GS}[2]	Gate to Source Voltage $4V \ge V_{DS} \ge 0.0V$	-6V
T_{CH}	Maximum Channel Temperature	300°C
$T_{STG(MAX)}$	Maximum Storage Temperature	250°C
LID and Lead Soldering Temp.[3] 250°C for 10 sec. each item.		

1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. Maximum forward Gate Current should not exceed 2 mA.
3. See Handling and Use Precautions. (page 13).

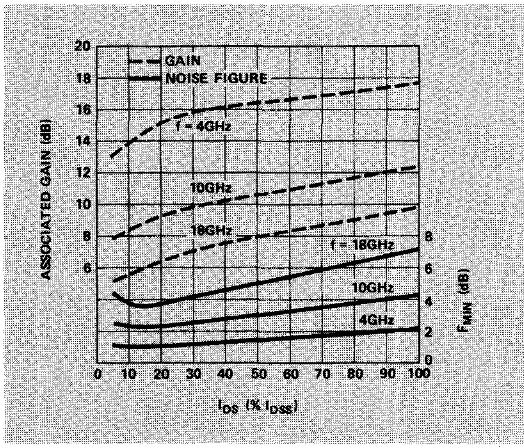


Figure 1. Typical Associated Gain and Noise Figure (F_{min}) vs. I_{DS} as a percentage of I_{DSS} when tuned for minimum noise figure. Frequency from 4 GHz to 18 GHz, V_{DS} = 3.5V.

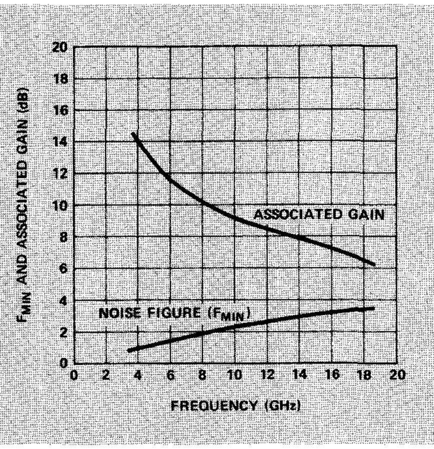


Figure 2. Typical Noise Figure (F_{min}) and Associated Gain vs. Frequency, V_{DS} = 3.5V, I_{DS} = 15% I_{DSS}.

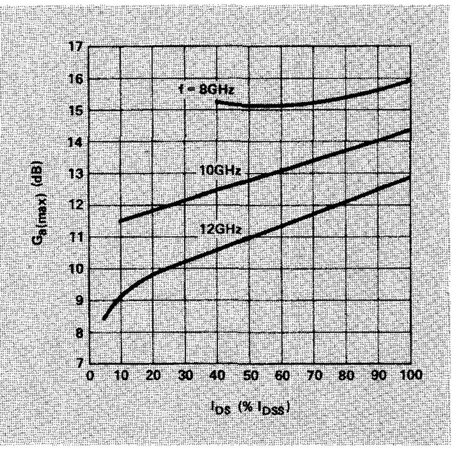


Figure 3. Typical $G_{a(max)}$ vs. I_{DS} as a percentage of I_{DSS}. Frequency = 8, 10, and 12 GHz, V_{DS} = 3.5V.

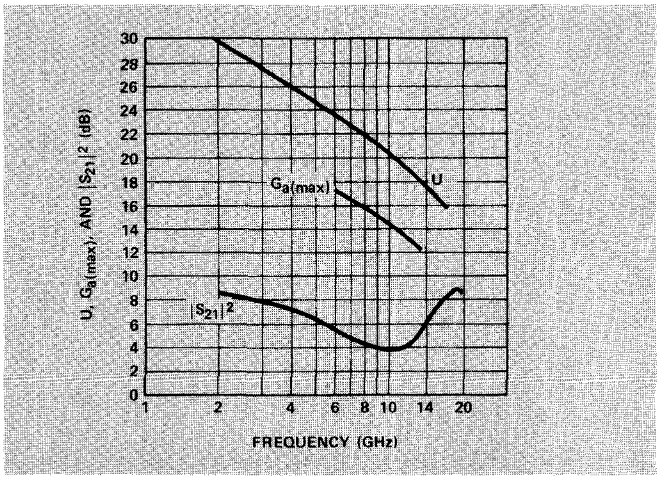


Figure 4. Mason's Gain (U), $G_{a(max)}$ and $|S_{21}|^2$ vs. Frequency. V_{DS} = 3.5V, V_{GS} = 0.0V.

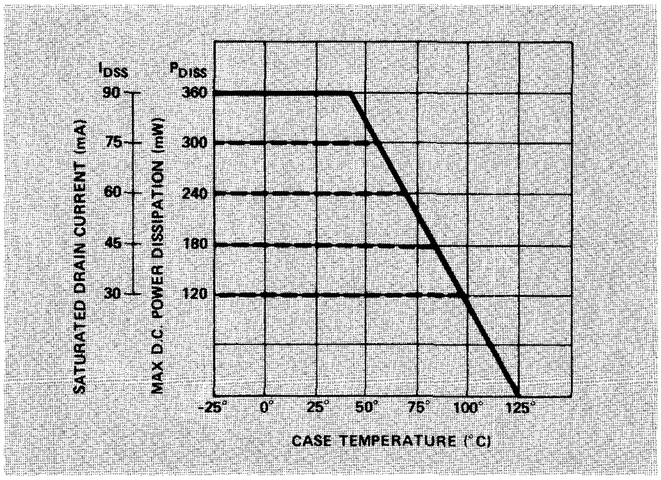


Figure 5. P_{DISS} vs. Temperature, Power Derating Curve at V_{DS} = 4V. Maximum power dissipation is a function of device I_{DSS}. Begin derating at P_{DISS} corresponding to individual device I_{DSS}, following a horizontal line until it intersects with the solid diagonal line.

Typical S-Parameters Minimum Noise Figure Bias V_{DS} = 3.5V, I_{DS} = 15% I_{DSS}

Freq. (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang
2.00	0.98	-58	5.67	1.92	127	-31.09	0.03	45	0.79	-34
3.00	0.96	-82	5.07	1.79	103	-28.37	0.04	26	0.77	-50
4.00	0.96	-106	4.52	1.68	81	-26.62	0.05	9	0.77	-66
5.00	0.92	-127	3.91	1.57	59	-25.76	0.05	-8	0.74	-82
6.00	0.91	-146	3.28	1.46	39	-25.39	0.05	-24	0.71	-97
7.00	0.90	-164	2.72	1.37	19	-24.99	0.06	-37	0.69	-113
8.00	0.89	-178	2.23	1.29	0	-24.81	0.06	-49	0.68	-130
9.00	0.88	170	1.82	1.23	-17	-24.62	0.06	-62	0.67	-147
10.00	0.87	159	1.68	1.21	-34	-24.28	0.06	-74	0.66	-162
11.00	0.86	148	1.80	1.23	-51	-24.17	0.06	-84	0.62	-175
12.00	0.84	138	2.25	1.30	-68	-23.37	0.07	-93	0.57	174
13.00	0.81	125	3.01	1.41	-88	-21.70	0.08	-106	0.49	161
14.00	0.77	108	4.04	1.59	-111	-20.34	0.10	-125	0.36	144
15.00	0.70	87	4.77	1.73	-138	-19.12	0.11	-147	0.17	120
16.00	0.60	61	5.24	1.83	-169	-18.28	0.12	-169	0.08	-57
17.00	0.48	30	5.01	1.78	158	-17.29	0.14	162	0.35	-95
18.00	0.36	-8	3.99	1.58	124	-17.58	0.13	130	0.60	-124

Typical S-Parameters Maximum Gain Bias V_{DS} = 3.5V, I_{DS} = 100% I_{DSS}

Freq. (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
2.00	0.97	-64	8.83	2.76	124	-35.40	0.02	44	0.80	-33
3.00	0.94	-91	8.03	2.52	99	-32.94	0.02	30	0.79	-49
4.00	0.93	-116	7.25	2.30	77	-31.57	0.03	14	0.79	-64
5.00	0.90	-137	6.48	2.11	56	-30.97	0.03	0	0.76	-79
6.00	0.88	-156	5.73	1.93	36	-30.99	0.03	-12	0.74	-95
7.00	0.86	-173	5.06	1.79	16	-30.69	0.03	-18	0.72	-110
8.00	0.85	173	4.50	1.68	-2	-30.29	0.03	-24	0.73	-126
9.00	0.84	161	4.03	1.59	-19	-30.15	0.03	-30	0.72	-143
10.00	0.83	151	3.90	1.57	-35	-28.93	0.04	-35	0.72	-158
11.00	0.80	140	3.98	1.58	-52	-28.16	0.04	-41	0.69	-170
12.00	0.78	129	4.39	1.66	-69	-26.36	0.05	-47	0.65	179
13.00	0.75	116	5.15	1.81	-88	-24.15	0.06	-57	0.61	168
14.00	0.72	99	6.29	2.06	-110	-21.76	0.08	-73	0.55	151
15.00	0.70	76	7.41	2.35	-135	-19.29	0.10	-95	0.43	125
16.00	0.67	45	8.39	2.63	-167	-17.50	0.13	-121	0.25	79
17.00	0.65	4	8.65	2.71	156	-15.79	0.16	-151	0.23	-23
18.00	0.62	-42	7.83	2.46	116	-14.78	0.18	169	0.55	-89

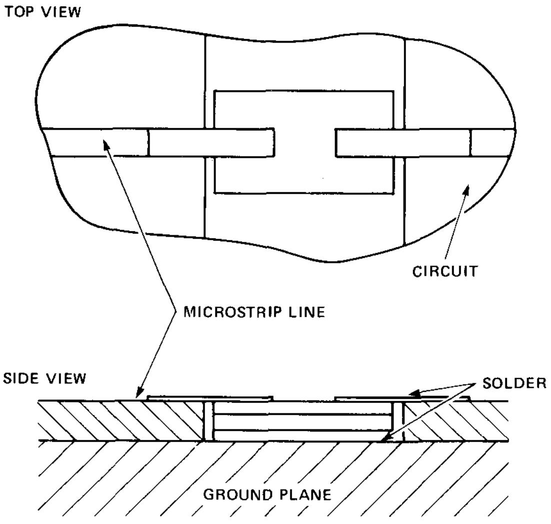
Typical Noise Parameters[1]

Frequency (GHz)	Γ_o		$\Gamma_L = [S'_{22}]^*$		F_{MIN} (dB)	R_N (Ohms)
	Mag.	Ang.	Mag.	Ang.		
4.0	.847	92	.556	76.8	1.12	47
6.0	.779	142	.650	112.4	1.7	14
8.0	.789	168	.572	143.7	2.0	2
10.0	.814	-172	.530	172.5	2.4	8
12.0	.645	-153	.479	-165.7	2.7	30
14.0	.600	-114	.255	-117	3.1	43
18.0	.329	-36	.668	126.5	3.4	—

Note:
1. Optimum Input Reflection Coefficient (Γ_O), Output Match for Minimum Noise (Γ_L), Associated Noise Figure (F_{MIN}) and Noise Resistance (R_N) at V_{DS} = 3.5V, I_{DS} = 15% I_{DSS}.

Mounting Instructions

THE USE OF CONVENTIONAL LEAD-TIN SOLDER IS RECOMMENDED FOR PACKAGE MOUNTING. CARE SHOULD BE TAKEN TO INSURE GOOD SOLDER WETTING TO MINIMIZE SOURCE INDUCTANCE AND THERMAL RESISTANCE.



For more information on mounting the HPAC-170 see Application Bulletin 24, pg. 16.

HEWLETT PACKARD
COMPONENTS

LOW NOISE MICROWAVE GaAs FET

NEW

HFET-2202

Features

LOW NOISE FIGURE
1.1 dB Typical NF at 4 GHz, 1.4 dB Maximum
1.9 dB Typical NF at 8 GHz

HIGH ASSOCIATED GAIN
13.6 dB Typical G_a at 4 GHz, 12.0 dB Minimum
9.6 dB Typical at 8 GHz

HIGH OUTPUT POWER
14.5 dBm Linear Power at 4 GHz

CHARACTERIZED TO 12 GHz

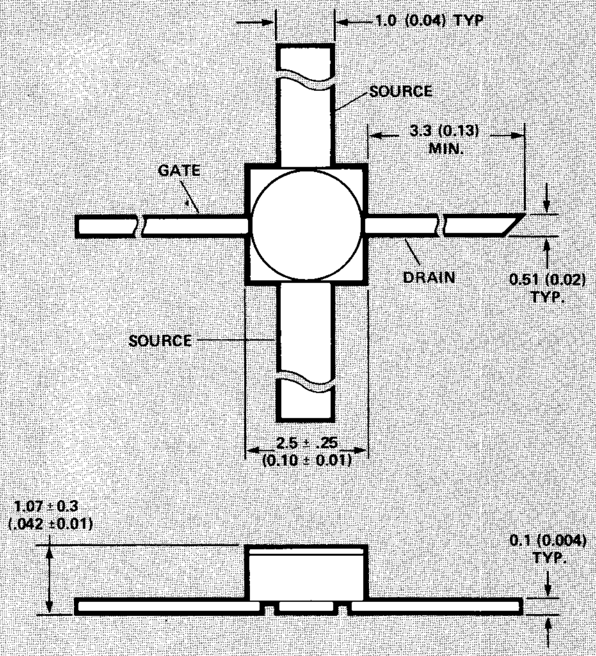
RUGGED HERMETIC PACKAGE

0.5 MICROMETER GATE

Description/Applications

The HFET-2202 is a gallium arsenide Schottky gate field effect transistor. It features a rugged, hermetic package that is designed for consistent operation over the frequency range of 2 GHz to 12 GHz. The device's superior noise and gain performance, coupled with its wide dynamic range capability, make it ideally suited for such applications as land and satellite communications and radar.

The HFET-2202 is packaged in the HPAC-100A. The part is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.



DIMENSIONS IN MILLIMETERS (INCHES).

HPAC-100A Package Outline

Electrical Specifications at $T_{CASE} = 25°C$

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
I_{DSS}	Saturated Drain Current, $V_{DS} = 3.5V$, $V_{GS} = 0V$		mA	25	45	90
V_{GSP}	Pinch Off Voltage, $V_{DS} = 3.5V$, $I_{DS} < 500\ \mu A$		V	-0.5	-2.0	-4.0
g_m	Transconductance, $V_{DS} = 3.5V$, $\Delta V_{GS} = 0V$ to $-0.5V$		mmho	20	32	45
$G_{a(max)}$	Maximum Available Gain $V_{DS} = 3.5V$, $V_{GS} = 0V$	f = 6 GHz 8 GHz	dB		16.0 13.0	
F_{MIN}	Minimum Noise Figure $V_{DS} = 3.5V$, $I_{DS} = 15\%\ I_{DSS}$ (Typ. 7.5 mA)	f = 4 GHz 6 GHz 8 GHz	dB		1.1 1.4 1.9	1.4
G_a	Associated Gain at N.F. Bias	f = 4 GHz 6 GHz 8 GHz	dB	12.0	13.6 11.3 9.6	
P_{1dB}	Power at 1 dB Gain Compression	f = 4 GHz	dBm		14.5	
G_{1dB}	Associated 1 dB Compressed Gain $V_{DS} = 4.0V$, $I_{DS} = 50\%\ I_{DSS}$ (0 dBm Input Matching, Tuned for Maximum Output)	f = 4 GHz	dB		13.3	

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Values
V_{DS}	Drain to Source Voltage, -4 V ≤ V_{GS} ≤ 0V	4V
V_{GS}[2]	Gate to Source Voltage 4V ≥ V_{DS} ≥ 0V	-4V
T_{CH}[3]	Maximum Channel Temperature	125° C
T_{STG}	Storage Temperature	-65° C to +125° C

Notes:

1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device mean time between failure (MTBF) to below the design goal of 1 x 10^7 hours at T_{CH} = 125°C (assumed Activation Energy = 1.6 eV).
2. Maximum continuous forward gate current should not exceed 1.5 mA.
3. Θ_{jc} — Thermal resistance, channel to case = 260° C/W.

Absolute Maximum Ratings[1]

Symbol	Parameter	Limits
V_{DS}	Drain to Source Voltage -4V ≤ V_{GS} ≤ 0V	10V
V_{GS}[2]	Gate to Source Voltage 4V ≥ V_{DS} ≥ 0V	-6V
T_{CH}	Maximum Channel Temperature	300° C
$T_{STG(max)}$	Maximum Storage Temperature	250° C
Lead Soldering Temperature[3] 250° C for 10 sec. each lead.		

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. Maximum forward gate current should not exceed 2 mA.
3. See Handling and Use Precautions (page 13).

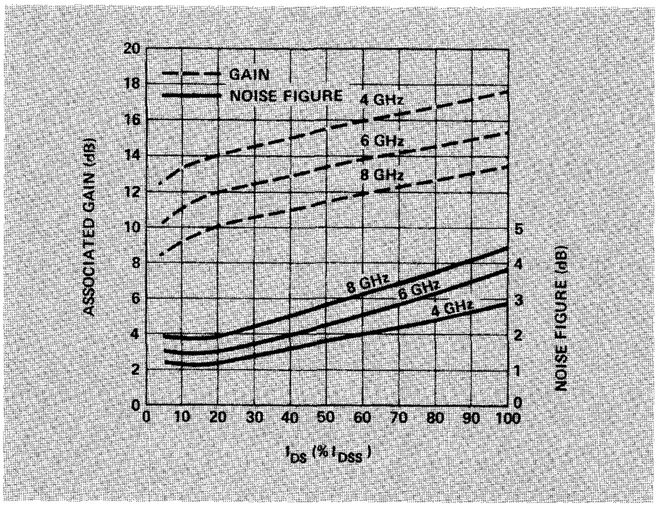


Figure 1. Typical Associated Gain and Noise Figure (F_{MIN}) vs. I_{DS} as a percentage of I_{DSS} when tuned for minimum noise figure. Frequency from 4 GHz to 8 GHz, V_{DS} = 3.5V.

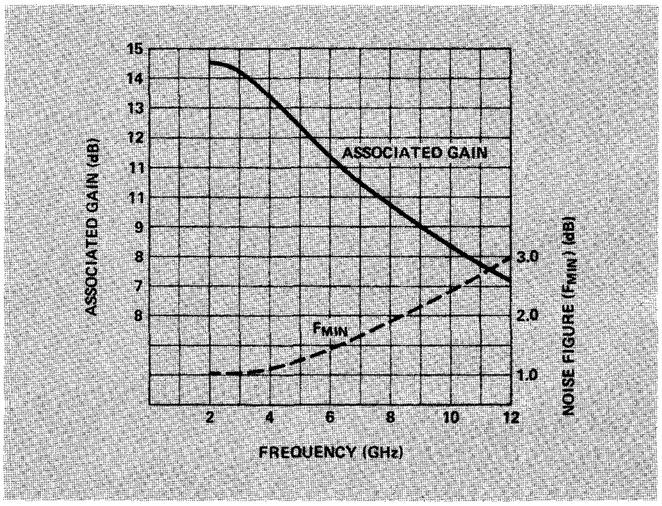


Figure 2. Typical Noise Figure (F_{MIN}) and Associated Gain vs. Frequency. V_{DS} = 3.5V, I_{DS} = 15% I_{DSS}.

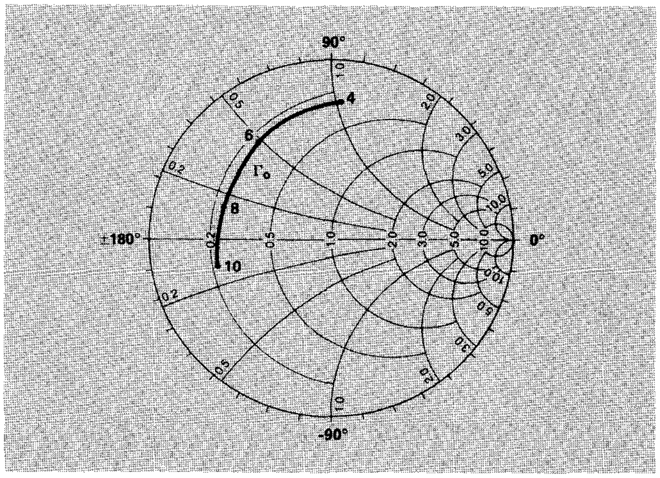


Figure 3. Typical Γ_o in the 4 to 10 GHz range for V_{DS} = 3.5V, I_{DS} = 15% I_{DSS}. (Γ_o = Input Match for Minimum Noise).

TABLE I. HFET-2202 Typical Noise Parameters[1]

Frequency	Γ_o	$\Gamma_L = [S'_{22}]^*$	F_{MIN} (dB)	R_N (Ω)
4 GHz	.75 ∠ 86°	.74 ∠ 70°	1.1	45
6 GHz	.63 ∠ 119°	.65 ∠ 93°	1.4	21
8 GHz	.62 ∠ 161°	.64 ∠ 124°	1.9	7
10 GHz	.62 ∠ -168°	.65 ∠ 159°	2.5	4

Note:

1. Optimum Input Reflection Coefficient (Γ_o), Output Match for Minimum Noise (Γ_L), Associated Noise Figure (F_{MIN}) and Noise Resistance (R_N) at V_{DS} = 3.5V, I_{DS} = 15% I_{DSS}.

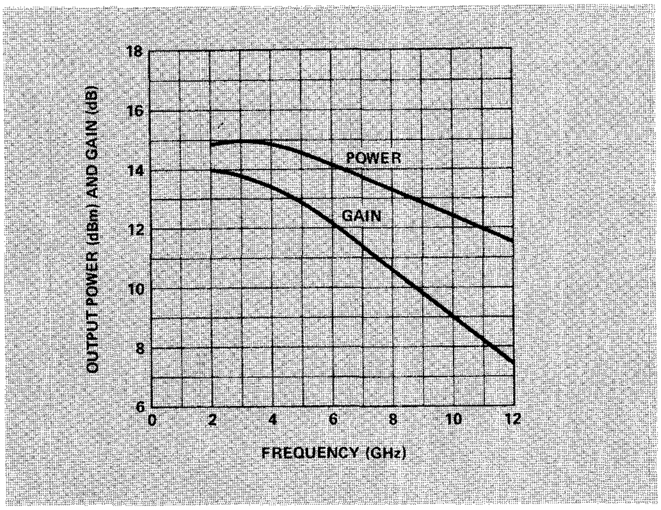


Figure 4. Typical P_{1dB} Linear Power and Associated 1dB Compressed Gain vs. Frequency at V_{DS} = 4.0V, I_{DS} = 50% I_{DSS}.

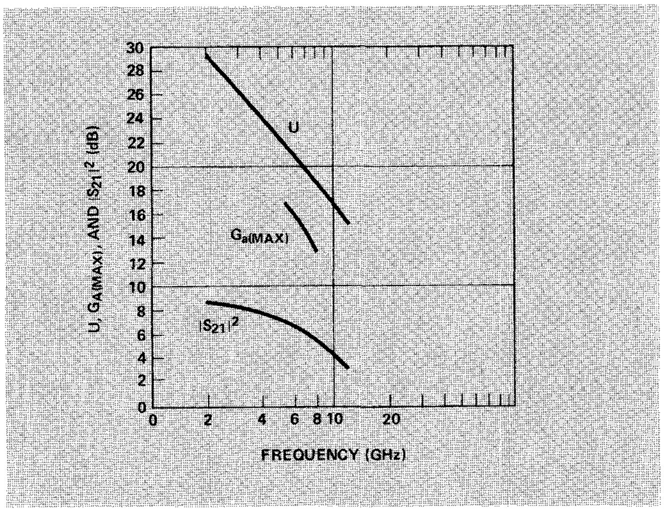


Figure 5. Mason's Gain (U), $G_{a(max)}$ and $|S_{21}|^2$ vs. Frequency, V_{DS} = 3.5V, V_{GS} = 0.0V.

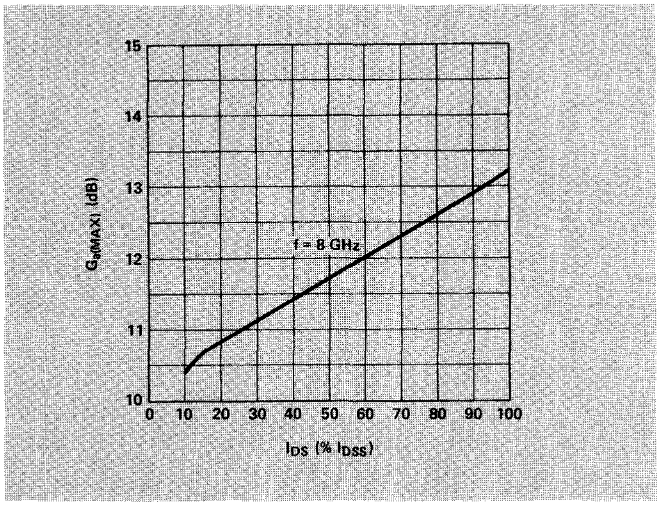


Figure 6. Typical $G_{a(max)}$ vs. I_{DS} as a percentage of I_{DSS}. Frequency = 8 GHz. V_{DS} = 3.5V.

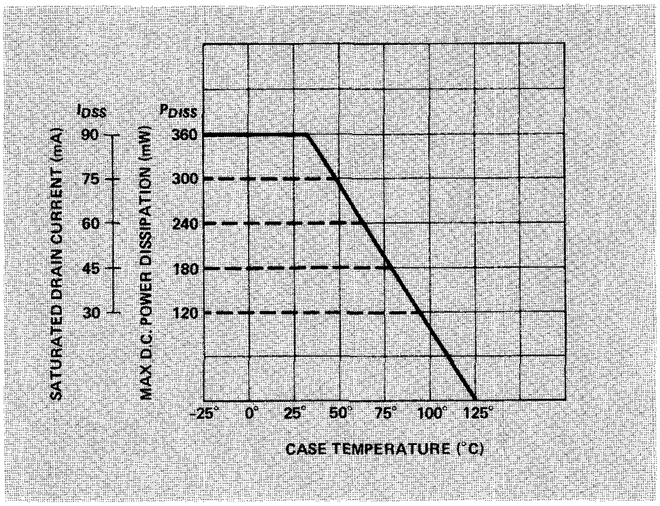


Figure 7. P_{DISS} vs. Temperature, Power Derating Curve at V_{DS} = 4V. Maximum power dissipation is a function of device I_{DSS}. Begin derating at P_{DISS} corresponding to individual device I_{DSS}, following a horizontal line until it intersects with the solid diagonal line.

Typical S-Parameters

MINIMUM NOISE FIGURE BIAS $V_{DS} = 3.5V$, $I_{DS} = 15\%\ I_{DSS}$

Freq. (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
2.0	0.98	-44	5.23	1.83	138	-29.6	0.03	58	0.80	-24
3.0	0.93	-66	5.02	1.78	118	-26.6	0.05	43	0.77	-37
3.5	0.91	-77	4.94	1.77	108	-25.5	0.05	36	0.76	-44
3.6	0.91	-79	4.96	1.77	106	-25.2	0.06	35	0.75	-46
3.7	0.90	-81	4.95	1.77	104	-25.2	0.06	34	0.75	-47
3.8	0.90	-83	4.88	1.75	102	-25.0	0.06	32	0.74	-49
3.9	0.89	-85	4.87	1.75	100	-24.7	0.06	30	0.74	-50
4.0	0.89	-88	4.88	1.75	98	-24.6	0.06	29	0.74	-52
4.1	0.89	-91	4.88	1.75	96	-24.6	0.06	28	0.74	-52
4.2	0.89	-92	4.80	1.74	94	-24.4	0.06	27	0.73	-53
4.3	0.88	-95	4.78	1.73	91	-24.3	0.06	25	0.73	-55
4.4	0.88	-97	4.81	1.74	89	-24.2	0.06	24	0.73	-56
4.5	0.87	-99	4.77	1.73	88	-24.1	0.06	23	0.73	-58
5.0	0.86	-109	4.63	1.71	77	-23.5	0.07	15	0.71	-65
6.0	0.83	-130	4.40	1.66	57	-23.1	0.07	2	0.69	-81
7.0	0.78	-150	3.87	1.56	37	-23.1	0.07	-9	0.66	-97
8.0	0.74	-169	3.32	1.47	19	-23.2	0.07	-18	0.63	-114
9.0	0.73	174	2.80	1.38	1	-23.6	0.07	-24	0.61	-132
10.0	0.72	157	2.38	1.32	-16	-23.6	0.07	-29	0.61	-151
11.0	0.71	142	1.93	1.25	-34	-22.2	0.08	-34	0.62	-168
12.0	0.67	126	1.44	1.18	-52	-23.0	0.07	-38	0.62	175

HIGH GAIN BIAS $V_{DS} = 3.5V$, $V_{GS} = 0V$

Freq. (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
2.0	0.96	-51	8.72	2.73	134	-34.4	0.02	61	0.79	-23
3.0	0.89	-75	8.27	2.59	113	-31.7	0.03	49	0.76	-35
3.5	0.87	-87	8.07	2.53	103	-31.1	0.03	43	0.76	-41
3.6	0.86	-89	8.04	2.52	101	-30.8	0.03	43	0.75	-43
3.7	0.86	-92	8.01	2.52	99	-30.7	0.03	43	0.75	-44
3.8	0.85	-94	7.92	2.49	97	-30.5	0.03	41	0.74	-46
3.9	0.84	-97	7.89	2.48	94	-30.5	0.03	40	0.74	-47
4.0	0.84	-99	7.85	2.47	93	-30.5	0.03	40	0.74	-48
4.1	0.84	-102	7.83	2.46	91	-30.5	0.03	38	0.74	-49
4.2	0.84	-104	7.74	2.44	88	-30.2	0.03	38	0.74	-50
4.3	0.83	-107	7.69	2.43	86	-29.9	0.03	36	0.74	-51
4.4	0.82	-109	7.69	2.43	84	-29.9	0.03	36	0.73	-52
4.5	0.82	-111	7.64	2.41	82	-29.9	0.03	35	0.73	-54
5.0	0.80	-122	7.35	2.34	72	-29.4	0.03	31	0.72	-61
6.0	0.76	-143	6.90	2.21	52	-29.1	0.04	29	0.71	-75
7.0	0.72	-164	6.21	2.04	33	-28.4	0.04	27	0.68	-91
8.0	0.68	178	5.51	1.88	15	-27.1	0.04	27	0.67	-107
9.0	0.68	159	4.91	1.76	-3	-25.7	0.05	25	0.65	-124
10.0	0.67	143	4.36	1.65	-20	-23.9	0.06	20	0.66	-142
11.0	0.65	128	3.83	1.55	-37	-21.6	0.08	4	0.67	-160
12.0	0.62	112	3.24	1.45	-55	-21.1	0.09	1	0.68	-176

LINEAR POWER BIAS $V_{DS} = 4.0V$, $I_{DS} = 50\%\ I_{DSS}$

Freq. (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
2.0	0.97	-47	7.78	2.45	136	-32.8	0.02	61	0.78	-23
3.0	0.91	-71	7.42	2.35	115	-30.2	0.03	47	0.75	-35
3.5	0.88	-82	7.27	2.31	105	-29.1	0.04	41	0.74	-42
3.6	0.88	-85	7.26	2.31	103	-28.9	0.04	40	0.73	-44
3.7	0.87	-87	7.23	2.30	101	-28.9	0.04	39	0.73	-45
3.8	0.87	-89	7.16	2.28	99	-28.6	0.04	37	0.73	-47
3.9	0.86	-92	7.13	2.27	97	-28.6	0.04	36	0.73	-48
4.0	0.86	-94	7.12	2.27	95	-28.4	0.04	36	0.72	-49
4.1	0.86	-96	7.10	2.26	93	-28.4	0.04	35	0.72	-49
4.2	0.86	-99	7.02	2.24	91	-28.2	0.04	34	0.72	-51
4.3	0.85	-101	6.98	2.23	89	-28.0	0.04	33	0.72	-52
4.4	0.85	-103	6.98	2.23	87	-28.0	0.04	32	0.72	-53
4.5	0.84	-105	6.94	2.22	85	-28.0	0.04	31	0.72	-55
5.0	0.83	-116	6.72	2.17	75	-27.5	0.04	24	0.70	-62
6.0	0.79	-137	6.34	2.08	55	-27.3	0.04	19	0.68	-76
7.0	0.74	-158	5.72	1.93	35	-26.9	0.05	14	0.66	-92
8.0	0.70	-176	5.08	1.79	17	-26.4	0.05	11	0.64	-108
9.0	0.69	166	4.52	1.68	-1	-25.7	0.05	10	0.62	-126
10.0	0.68	150	4.02	1.59	-18	-24.3	0.06	7	0.63	-144
11.0	0.67	135	3.53	1.50	-35	-22.3	0.08	-6	0.64	-161
12.0	0.63	119	2.96	1.41	-53	-21.9	0.08	-9	0.65	-178

Handling And Use Precautions

The GaAs FETs are subject to damage caused by switching transients and static discharge, and must be handled with caution. Hewlett-Packard recommends the following precautions.

1. Assembly and test personnel, as well as tweezers or any other pick-up tool, should be grounded to the test or assembly station, preventing the build-up of static charge which can damage the gate area if the charge is allowed to pass through it. During the package mounting procedure, insure assembly equipment is adequately grounded.

   Static discharge during handling, testing, and assembly can induce increased reverse gate leakage of a resistive nature.

   To prevent the buildup of static charge on the package during storage, the device should be held in a conductive medium (e.g., metal container, conductive foam).
2. Spurious pulses generated by test equipment (i.e. contact bounce during switching, induced voltage in the leads, etc.) must be eliminated. Avoid turning instrument power on and off, or switching between instrument ranges when bias is applied to the device.
3. Inductive pickup from large transformers, switching power supplies, inductive ovens, etc., must also be eliminated. Use shielded signal and power cables.
4. Assembly equipment (i.e., soldering irons) must be adequately grounded.
5. Application of bias. When applying bias to the FET, first apply the gate voltage, then the drain voltage. When removing bias, remove the gate voltage last.

NOTES

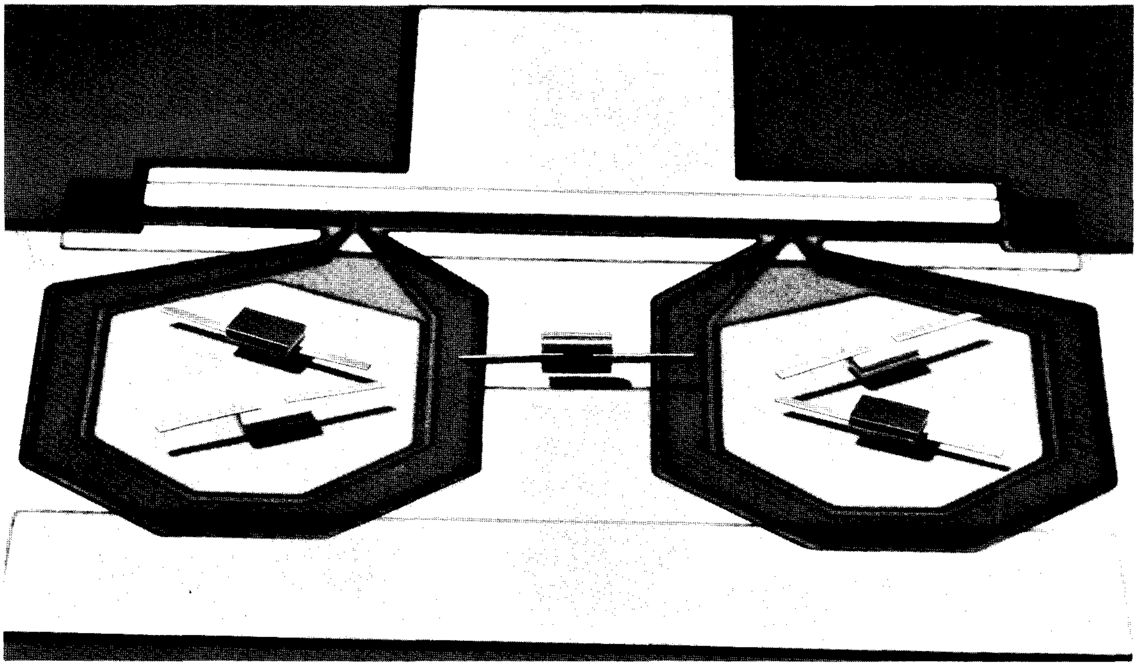
Applications for Microwave GaAs FETS

NEW

HEWLETT hp PACKARD
COMPONENTS

APPLICATION BULLETIN 24

Selecting a Design Medium for the HFET-2201 GaAs Field Effect Transistor



INTRODUCTION

The Hewlett-Packard HFET-2201 is a low noise, broadband Gallium Arsenide Field Effect Transistor. The package, HPAC-170 (Fig. 1), was designed to enhance the RF characteristics of the chip and thereby offers broadband capability in the 2 to 18 GHz range. This is accomplished by lowering the parasitic capacitance along with the source inductance within the package. (Parasitic capacitance and source inductance both tend to degrade performance).

This bulletin reports the results of mounting the HFET-2201 in two different microstrip environments: RT/Duroid[1] and Alumina. In both cases the HFET-2201 was first measured for S-Parameters, using a specially designed test fixture which is constructed for minimum loss. Then the device was mounted on a 50Ω microstrip line, and again measured for S-Parameters. All the S-Parameter measurements were made on the Hewlett-Packard 8542B Automatic Network Analyzer.

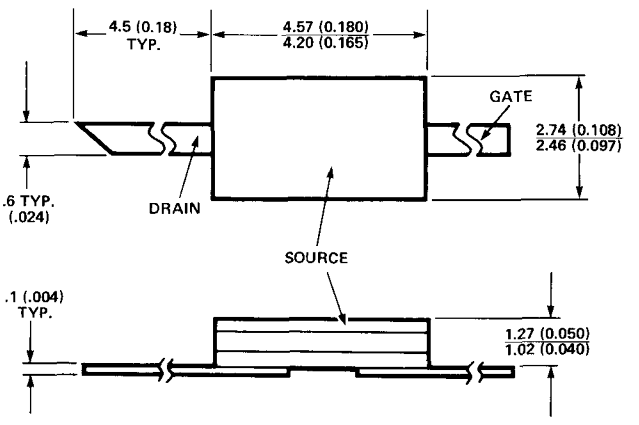


Figure 1. HPAC-170 Package Outline.

A Comparison of the S-Parameters of the HFET-2201 Mounted In a Fixture and on Duroid Circuit

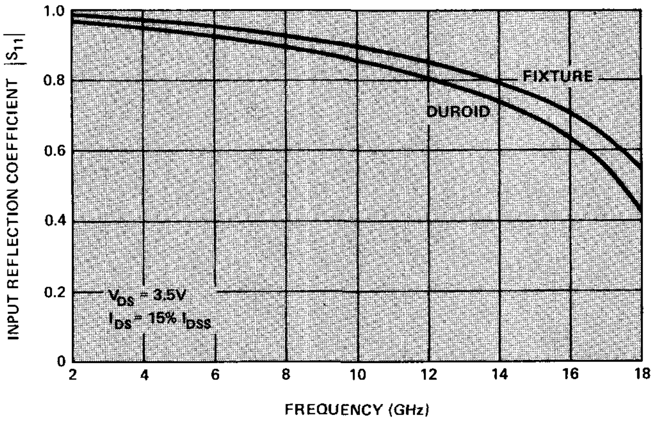


Figure 4. Input Reflection Coefficient, $|S_{11}|$ vs. Frequency.

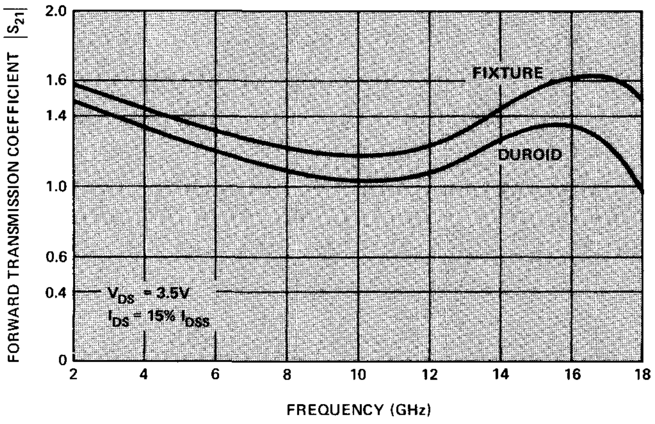


Figure 5. Forward Transmission Coefficient, $|S_{21}|$ vs. Frequency.

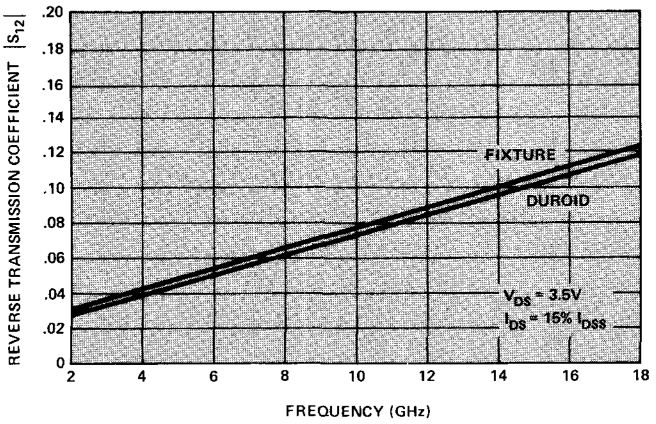


Figure 6. Reverse Transmission Coefficient, $|S_{21}|$ vs. Frequency.

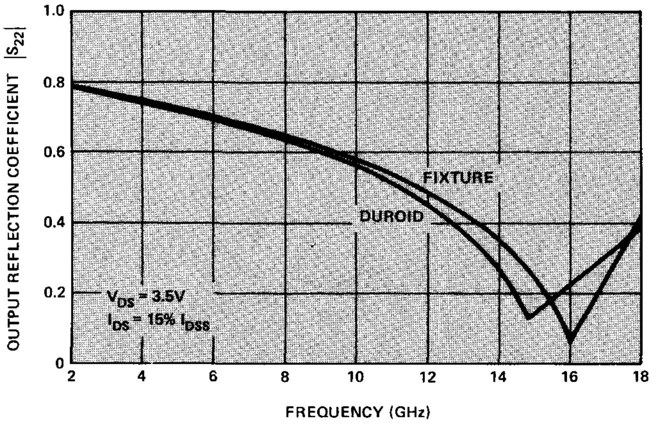


Figure 7. Output Reflection Coefficient, $|S_{22}|$ vs. Frequency.

DUROID

Fifty ohm lines were etched on 0.031" RT/Duroid board (ϵ_r = 2.25). The board was mounted in a "Modpak"[2] box #7011, 34.13mm (1.344 inches) x 34.13mm (1.344 inches) (See Figure 2a and photo 2b). A hole, 4.57mm (.180 inches) x 3.05mm (.120 inches), was cut in the electrical center of the 50Ω line, for device placement. Solder used was lead/tin (36% Pb, 60% Sn, 4% Ag). SMA connectors were OSM #220.

To dampen moding effects, "Poly-Iron" strips were placed parallel to the device on each side, and on the inside top cover.

S-Parameters for the device, measured in the test fixture and mounted on Duroid are shown in Figures 4, 5, 6, and 7.

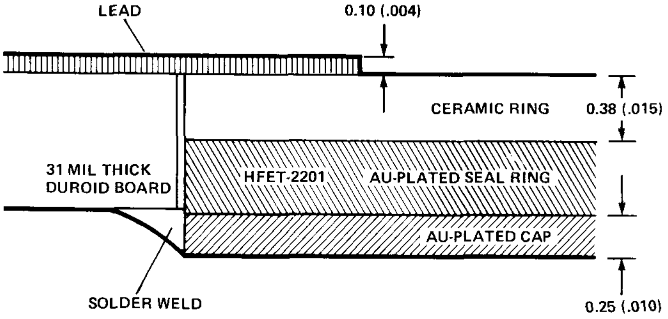


Figure 2a. Cross Sectional Drawing of Duroid Mounting.

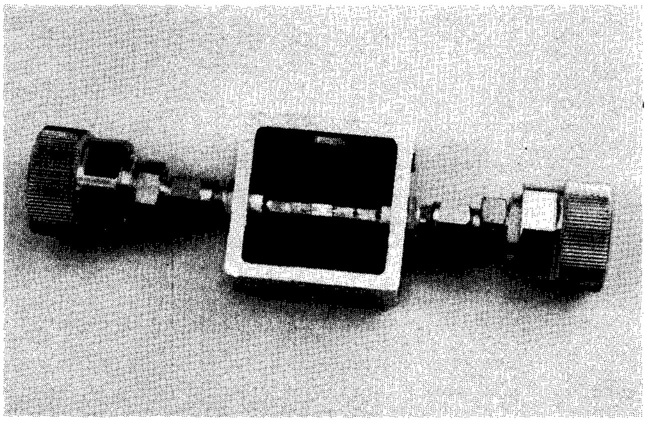


Figure 2b. Duroid Test Circuit and Housing.

ALUMINA

The alumina substrates were 2.54mm (.100 inches) x 5.97mm (.235 inches) x .64mm (.025 inches) with a 50Ω line on each. Substrates and device were mounted on a carrier (see Figures 3a and 3b) The substrates were die attached to the carrier while the device was silver (conductive) epoxy bonded. Ribbon bonding was used to attach the device leads to the 50Ω lines. The carrier, with device and substrates, was placed inside an amplifier housing (photo Figure 3c). The SMA connectors used were the flange type from Sealectro[3] (#50-645-4545-31).

Results of the S-Parameter measurements on the device are shown in Figures 8, 9, 10, and 11.

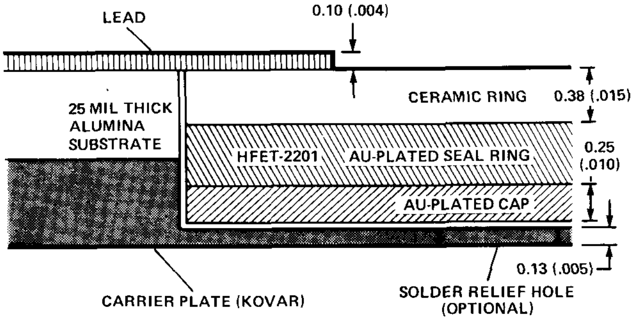


Figure 3a. Cross-Sectional Drawing of Alumina Mounting.

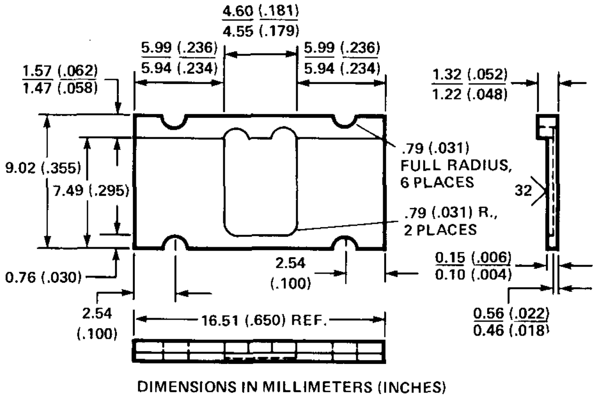


Figure 3b. Kovar Circuit Carrier.

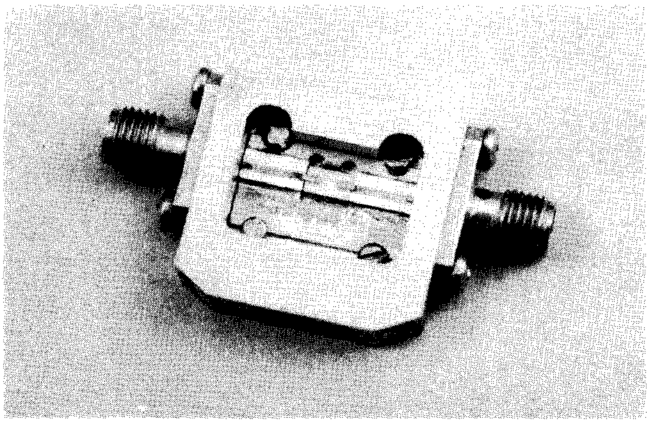


Figure 3c. Alumina Test Circuit and Housing.

CONCLUSION

Mounting the HFET-2201 on alumina will result in less loss (S_{21} and S_{12}) at frequencies greater than 8 GHz. The use of Duroid, especially above 8 GHz, results in greater losses.

REFERENCES

1. RT/Duroid manufactured by Rogers Corp., Chandler, Arizona.
2. Modpak manufactured by Adams-Russell Co., Waltham, Massachusetts.
3. Sealectro Corp., Mamaroneck, New York.

A Comparison of the S-Parameters of the HFET-2201 Mounted In a Fixture and on Alumina Circuit

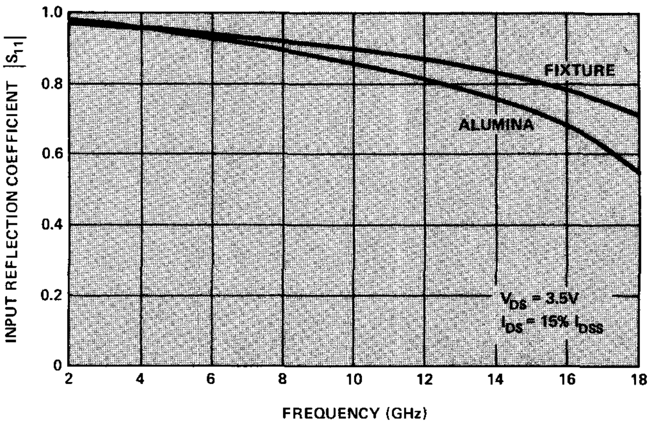


Figure 8. Input Reflection Coefficient, |S11| vs. Frequency.

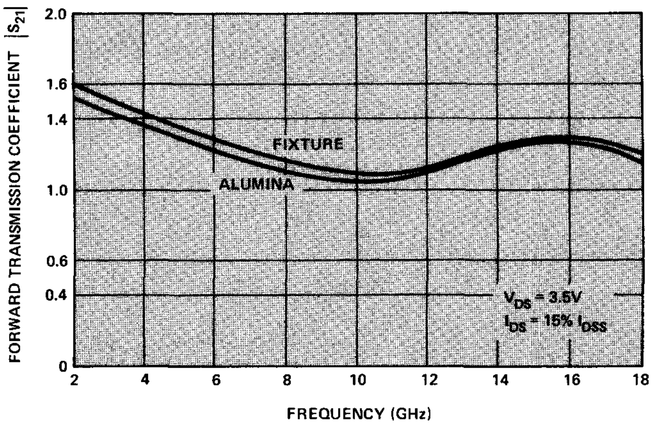


Figure 9. Forward Transmission Coefficient, |S21| vs. Frequency.

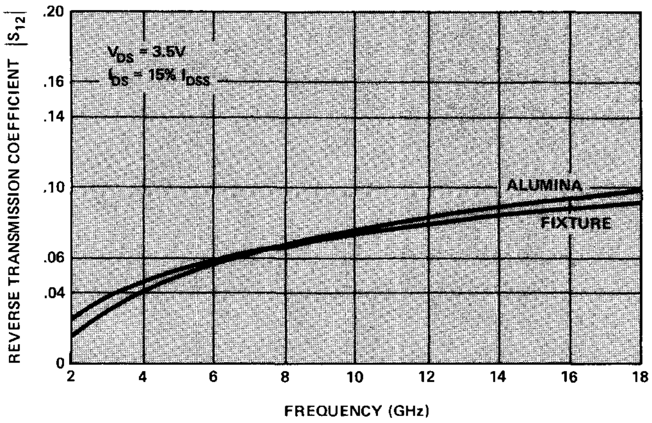


Figure 10. Reverse Transmission Coefficient, |S12| vs. Frequency.

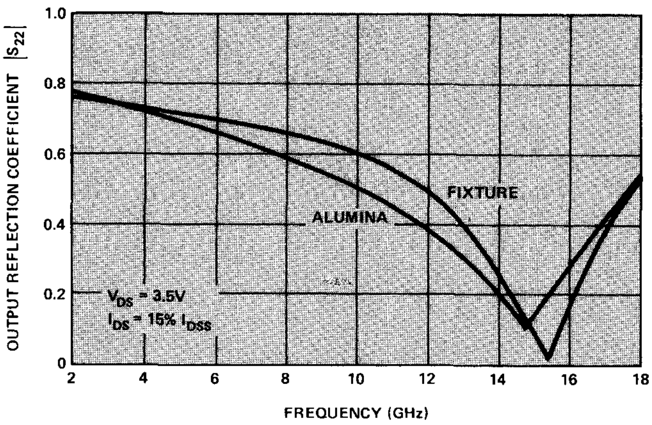


Figure 11. Output Reflection Coefficient, |S22| vs. Frequency.

HEWLETT PACKARD
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APPLICATIONS FOR MICROWAVE GaAs FETS

A 6 GHz Amplifier Using the 2N6680 HFET-1101 GaAs FET

(Portion of Application Note 970)

INTRODUCTION

The Hewlett-Packard 2N6680 (HFET-1101) is a device designed for good noise, gain and power output characteristics when used as an amplifier. The purpose of this application note is to highlight some of the design tradeoffs when using a GaAs FET. The example is an amplifier for use in the 5.9 to 6.4 GHz telecommunications band. The amplifier's performance over this band is excellent, with a maximum noise figure of 3.3 dB, a minimum associated gain of 10.9 dB, a flatness of ±0.4 dB and a 9.5 dBm minimum power output at 1 dB gain compression. The maximum input and output SWR are 2.67:1 and 1.90:1 respectively.

DESIGN TRADE-OFFS

The first choice facing a designer is biasing. In comparison to silicon bipolars, GaAs FETs require more current at a lower voltage, with the net result being about the same power dissipation. Power supply requirements should reflect this characteristic.

With any single stage amplifier design, there are three performance parameters that require different optimum bias settings.

They are:

1. Minimum noise figure
   V_{DS} = 3.5 Volts, I_{DS} = 15% I_{DSS}
2. Linear power output
   V_{DS} = 4.0 Volts, I_{DS} = 50% I_{DSS}
3. Maximum Gain
   V_{DS} = 4.0 Volts, I_{DS} = 100% I_{DSS}

For the three critical bias settings above, the input and output matching data are available from the scattering(1), noise(2), power(2) and gain(3) parameters. The linear power bias point of V_{DS} = 4.0 Volts and I_{DS} = 50% I_{DSS} provides a good compromise between minimum noise figure and maximum gain. At this bias point the scattering, noise, power and gain parameters can be measured by various known techniques(4). Typical parameters at 6 GHz for the 2N6680 are:

Scattering Parameters

S_{11} = 0.641/-171.3°
S_{12} = 0.057/16.3°
S_{21} = 2.058/28.5°
S_{22} = 0.572/-95.7°

Gain Parameters

K = 1.504
G_a (max.) = 11.38 dB
Γ_{MS} = 0.762/177.3°
Γ_{ML} = 0.718/103.9°

Noise Parameters

F_{MIN} = 2.9 dB
R_n = 9.42 ohms
Γ_O = 0.542/141°
Γ_L = 0.575/104.5°

Power Parameters @ P_{TUNE} = 5 dBm

P_{1dB} = 15.5 dBm
G_p = 8.2 dB
Γ_{PS} = 0.729/166°
Γ_{PL} = 0.489/101°

Even at this compromise bias point, the input matching network has four performance trade-offs that can be juggled. They are: noise figure; available power gain; power output; and input SWR.

Since most low noise receivers work in a small signal environment, the design engineer is typically concerned with compromising gain and input SWR for noise figure. Moving from Γ_O toward Γ_{MS} along a straight line, input SWR improves to 1.0:1 at Γ_{MS}, assuming the output to be conjugately matched. At the same time, noise figure and available gain are increasing. Table I shows corresponding values for noise, gain and input SWR.

TABLE I

	Γ_S Mag/Ang	Γ_L Mag/Ang	N.F. [dB]	Ga [dB]	Input SWR	Output SWR
Γ_O →	0.542/141°	0.575/104°	2.90	9.33	3.82:1	1.00:1
	0.572/152°	0.601/105°	2.97	10.04	2.91:1	1.00:1
	0.614/160°	0.627/106°	3.14	10.55	2.28:1	1.00:1
	0.678/169°	0.667/105°	3.57	11.10	1.61:1	1.00:1
Γ_{MS} →	0.762/177°	0.718/104°	4.44	11.38	1.00:1	1.00:1

From Table I, a very good compromise input match condition is Γ_S = 0.614/160° and the corresponding output conjugate match condition is Γ_L=0.627.106°. In comparison to the minimum noise match conditions the noise figure is increased by 0.24 dB but the associated gain is increased by 1.22 dB and the input, SWR is improved by 40% to 2.28:1.

With the choice of Γ_S and Γ_L discussed above, it is now possible to synthesize the input and output matching networks.

INPUT MATCHING NETWORK

1. The impedance Z_S, corresponding to Γ_S = 0.614/160° is:

$$Z_S = \frac{(1 - |\Gamma_S|^2)\,50}{1 + |\Gamma_S|^2 - 2\,|\Gamma_S|\,\mathrm{Cos}\,\underline{/\Gamma_S}} + j\,\frac{100\,|\Gamma_S|\,\mathrm{Sin}\,\underline{/\Gamma_S}}{1 + |\Gamma_S|^2 - 2\,|\Gamma_S|\,\mathrm{Cos}\,\underline{/\Gamma_S}}$$

$$Z_S = 12.31 + j8.30$$

2. $Y_S = \dfrac{1}{Z_S} = 0.056 - j0.038$

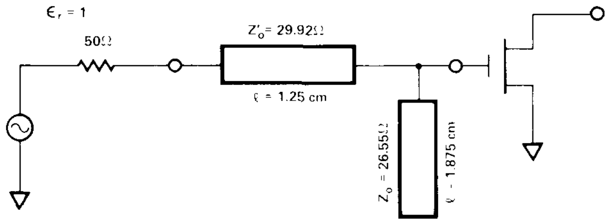
3. An open circuited stub looks like a shunt admittance $Y = jY_o \tan \beta\ell$. Therefore, an open circuited stub that is three-eights wavelength long looks like a shunt inductor of admittance $-jY_o$. Hence:

$$Z_o = \frac{1}{Y_o} = \frac{1}{I_m\,[Y_S]} = 26.55\Omega$$

4. Since the driving source impedance is 50Ω, a quarter-wave transformer of characteristic impedance

$$Z'_o = \sqrt{50\left[\frac{1}{R_e\left[Y_S\right]}\right]} = 29.92\Omega$$

completes the input matching network.



OUTPUT MATCHING NETWORK

1. The impedance Z_L, corresponding to $\Gamma_L = 0.627/106°$ is:

$$Z_L = \frac{(1-|\Gamma_L|^2)\,50}{1+|\Gamma_L|^2-2|\Gamma_L|\cos\angle\Gamma_L} + j\,\frac{100\,|\Gamma_L|\sin\angle\Gamma_L}{1+|\Gamma_L|^2-2|\Gamma_L|\cos\angle\Gamma_L}$$

$$Z_L = 17.45 + j34.66$$

2. $Y_L = \frac{1}{Z_L} = 0.012 - j0.023$

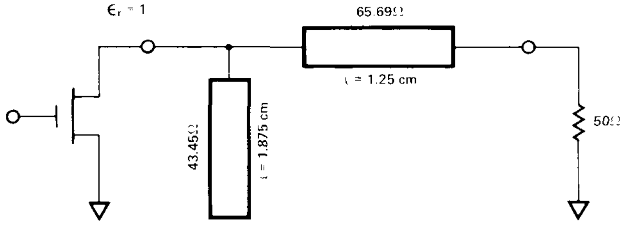
3. The output matching network is similar to the input matching network. An open circuited stub that is three-eighths wavelength long looks like a shunt inductor of admittance $-jY_o$. Hence:

$$Z_o = \frac{1}{Y_o} = \frac{1}{I_m\left[Y_L\right]} = 43.45\Omega$$

4. Since the load impedance is 50Ω, a quarter-wave transformer of characteristic impedance:

$$Z'_o = \sqrt{50\left[\frac{1}{R_e\,Y_L}\right]} = 65.69\Omega$$

completes the output matching network.



PERFORMANCE

An amplifier was constructed using the design derived above. A comparison of the computer simulation with measured amplifier performance at 6 GHz is shown below.

Parameter	Measured Performance	Computer Simulation
Gain	11.50 dB	10.55 dB
Input SWR	2.67:1	2.28:1
Output SWR	1.90:1	1.00:1
Isolation	-23 dB	-20.60 dB
Noise Figure	3.27 dB	3.14 dB

The performance of the amplifier was measured over the 5.9 to 6.4 GHz band. Figures 1, 2, 3, 4 and 5 show the room temperature performance.

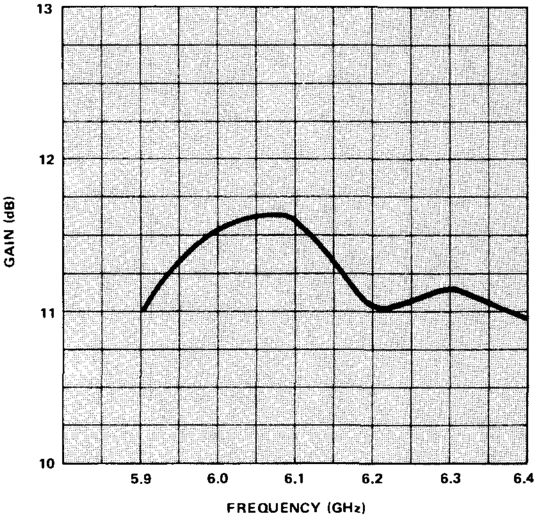


Figure 1. Gain Performance.

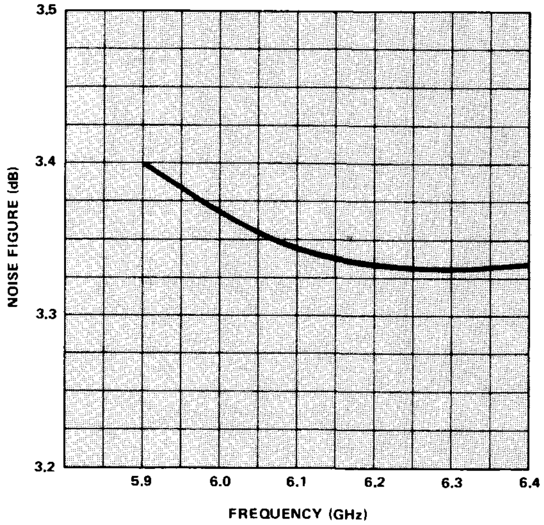


Figure 2. Noise Performance.

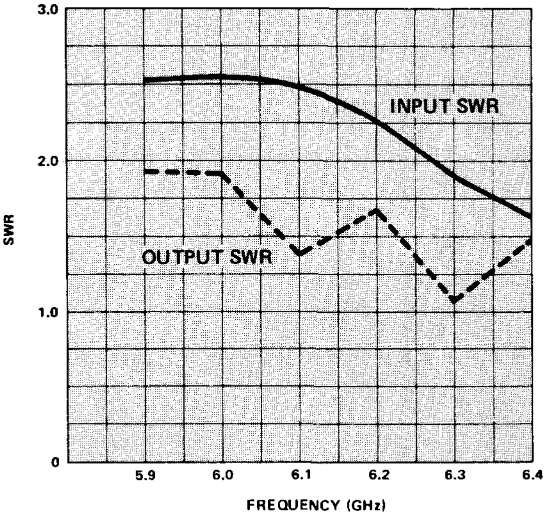


Figure 3. Input-Output SWR Performance.

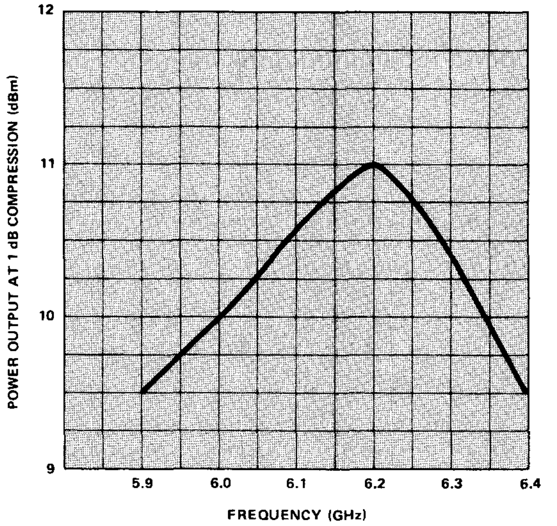


Figure 4. Power Output Performance.

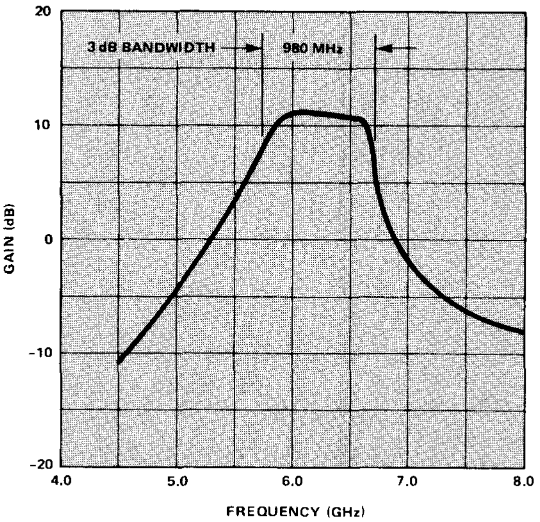


Figure 5. Wideband Gain Performance.

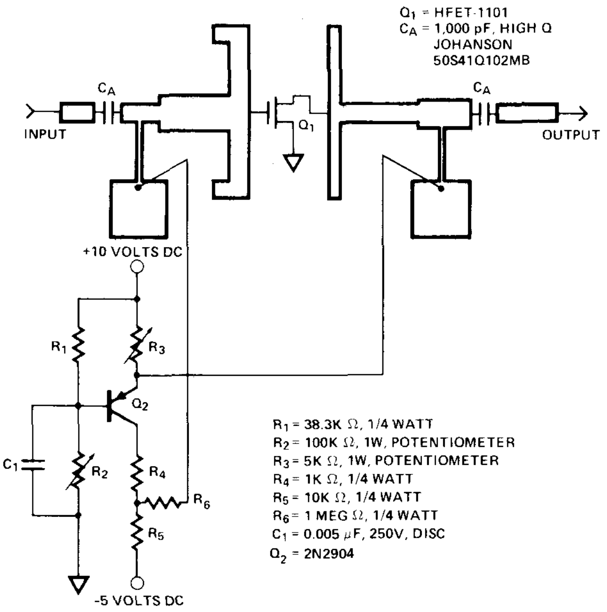
CONSTRUCTION

The board material is 0.031" RT/Duroid 120-061 (D5880) (Manufactured by Roger Corp. in Chandler, AZ), with 1oz. copper clad on two sides. The relative dielectric constant (ϵ_r) is 2.23. Duroid was chosen because of its low loss tangent. The thickness of 0.031" was chosen so the source top cap could be soldered to the RF ground, thereby taking advantage of the low source inductance.

To minimize transition interactions the shunt stubs were balanced along the series transmission lines. The bias network is fed at the quarter-wavelength point of a half-wavelength open circuited stub.

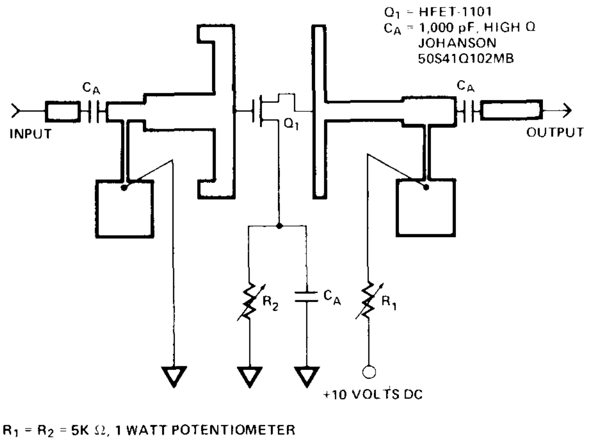
Two different types of biasing networks were used with the same result. A schematic of the complete amplifier and biasing circuit can be seen in the diagram that follows. The differences between the biasing networks are:

1. Schematic I is an active network which requires a dual polarity supply with an active pulse recovery loop.
2. Schematic II is a self-biasing network which requires a very good source by-passing capacitor. It has a lower component count with a single supply requirement. It is, however, more subject to oscillations.



The quiescent point is controlled by R_2 and R_3. R_2 is adjusted to provide the proper V_{DS} and R_3 is adjusted to supply the correct drain current (I_{DS}).

Schematic I Complete Amplifier



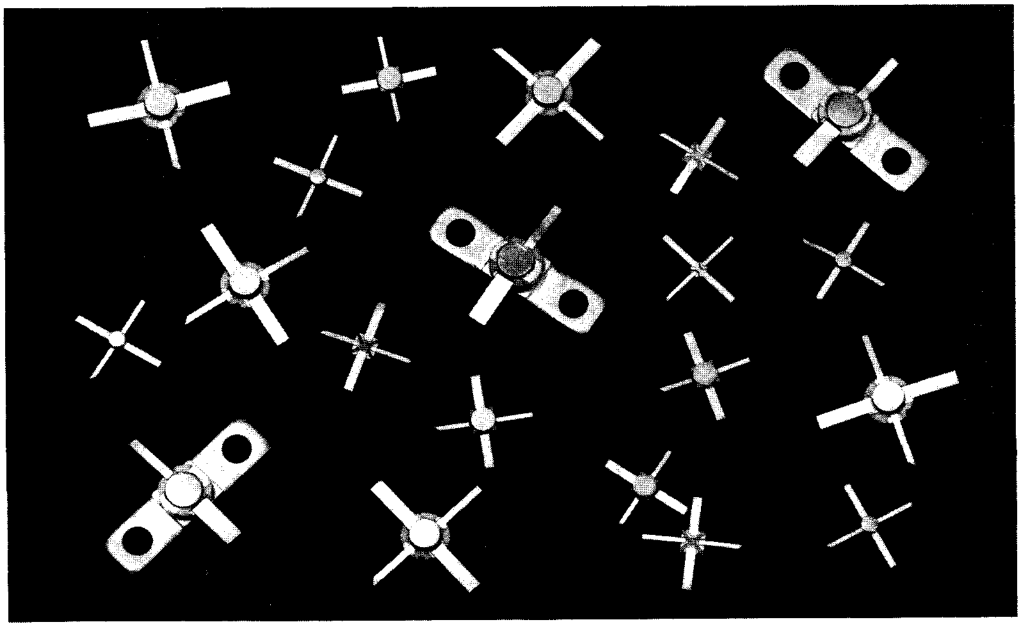
The quiescent point is controlled by R_1 and R_2. R_1 is adjusted to provide the proper V_{DS} and R_2 is adjusted to supply the correct drain current (I_{DS}).

Schematic II Complete Amplifier

REFERENCES

1. 2N6680 (HFET-1101), Microwave GaAs FET data sheet. (Publication No. 5952-9889).
2. Hewlett-Packard Application Bulletin 19, "Noise and Power Parameters for the HFET-1101".
3. Hewlett-Packard Application Note 95-1, "S-Parameter Techniques for Faster, More Accurate Network Design", September 1968.
4. Hewlett-Packard Application Bulletin 10, "Transistor Noise Figure Measurements". Publication 5952-9846.

Bipolar Transistors



Silicon Bipolar Transistor Selection Guide

LOW NOISE TRANSISTORS

Part Number HXTR-	Typical Noise Figure	Typical Associated Gain	Frequency	Package HPAC-	Chip Equivalent HXTR-	Page Number
6101 (2N6617)	2.8 dB	9.0 dB	4 GHz	70 GT	6001	45
6102	2.5 dB	9.0 dB	4 GHz	70 GT	6001	45
6103 (2N6618)	1.8 dB	12.0 dB	2 GHz	100	6001	48
6104	1.4 dB	14.0 dB	1.5 GHz	100	6001	51
6105	3.8 dB	9.0 dB	4 GHz	100	2001	54
6106	2.5 dB	11.5 dB	2 GHz	70 GT	2001	57

GENERAL PURPOSE TRANSISTORS

Part Number HXTR-	Typical Gain	Typical P_{1dB}	Frequency	Package HPAC-	Chip Equivalent HXTR-	Page Number
2101 (2N6679)	10.5 dB	18.5 dBm	4 GHz	100	2001	25
2102	15.0 dB	20.0 dBm	2 GHz	70 GT	2001	27
5101 (2N6701)	7.5 dB	22.0 dBm	4 GHz	100	5001	29
5103	11.0 dB	23.0 dBm	2 GHz	200	5001	37

LINEAR POWER TRANSISTORS

Part Number HXTR-	Typical P_{1dB}	Typical Gain	Frequency	Package HPAC-	Chip Equivalent HXTR-	Page Number
5101 (2N6701)	22.0 dBm	7.5 dB	4 GHz	100	5001	29
5102	27.5 dBm	7.0 dB	4 GHz	200 GB/GT	5002	33
5103	23.0 dBm	11.0 dB	2 GHz	200	5001	37
5104	29.0 dBm	9.0 dB	2 GHz	200	5002	41

Hewlett-Packard also supplies microwave bipolar transistors from the 35800 series for use in existing systems. Designers selecting transistors for use in new designs are encouraged to consider the superior performance of the HXTR series of devices available from Hewlett-Packard.

HEWLETT PACKARD
COMPONENTS

NEW

GENERAL PURPOSE TRANSISTOR

2N6679 (HXTR-2101)

上 11.18

Features

HIGH GAIN
10.5 dB Typical at 4 GHz

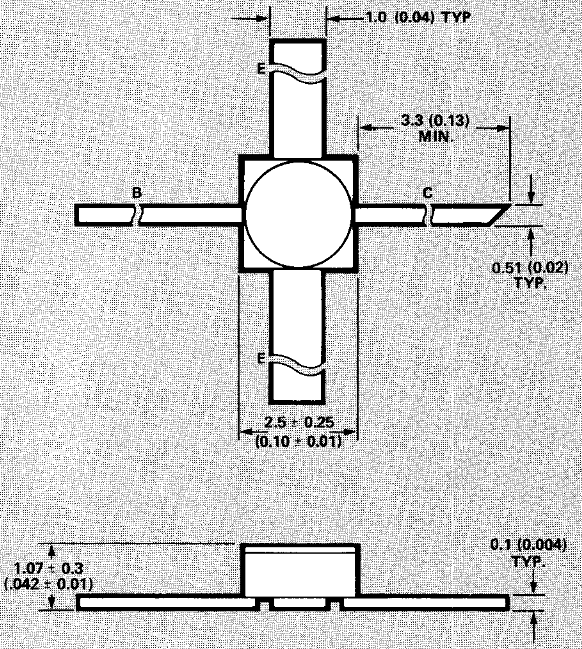
WIDE DYNAMIC RANGE

RUGGED HERMETIC PACKAGE

Description

The 2N6679 (HXTR-2101) is an NPN bipolar transistor designed for high gain and output power at 4 GHz. The device utilizes ion implantation techniques and Ti/Pt/Au metallization in its manufacture. The chip is provided with a dielectric scratch protection over its active area.

The 2N6679 is supplied in the HPAC-100, a rugged metal/ceramic hermetic package, and is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.



DIMENSIONS IN MILLIMETERS (INCHES).

HPAC-100 Package Outline

Electrical Specifications at $T_{CASE} = 25°C$

Symbol	Parameters and Test Conditions	MIL-STD-750 Test Method	Units	Min.	Typ.	Max.
BV_{CES}	Collector-Emitter Breakdown Voltage $I_C=100\mu A$	3011.1*	V	30		
I_{CEO}	Collector-Emitter Leakage Current at $V_{CE}=15V$	3041.1	nA			500
I_{CBO}	Collector Cutoff Current at $V_{CB}=15V$	3036.1	nA			100
h_{FE}	Forward Current Transfer Ratio $V_{CE}=15V, I_C=15mA$	3076.1*	—	50	120	220
G_T	Tuned Gain		dB	9.0	10.5	
P_{1dB}	Power Output at 1 dB Compression Bias Conditions for Above: $V_{CE}=15V, I_C=25mA$, Frequency = 4 GHz		dBm		18.5	

*300 μs wide pulse measurement ≤2% duty cycle.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage[2]	25V
V_{CEO}	Collector to Emitter Voltage[2]	16V
V_{EBO}	Emitter to Base Voltage[2]	1.0V
I_C	DC Collector Current[2]	35mA
P_T	Total Device Dissipation[3]	450 mW
T_J	Junction Temperature	200° C
T_{STG}	Storage Temperature	-65° C to +200° C

Notes:
1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device mean time between failure (MTBF) to below the design goal of 1 x 10^7 hours at T_J = 175° C (assumed Activation Energy = 1.5 eV). Corresponds to maximum rating for 2N6679.
2. T_{CASE} = 25° C.
3. Derate at 4.8 mW/° C, $T_C \geq 106°$ C.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	30V
V_{CEO}	Collector to Emitter Voltage	20V
V_{EBO}	Emitter to Base Voltage	1.5V
I_C	DC Collector Current	70 mA
P_T	Total Device Dissipation	900 mW
T_J	Junction Temperature	300° C
$T_{STG(MAX)}$	Maximum Storage Temperature	250° C
—	Lead Temperature (Soldering 10 seconds each lead)	+250° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

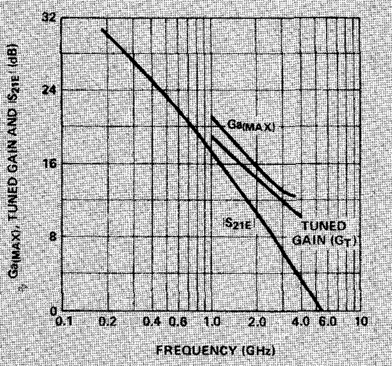


Figure 1. Typical $G_{a(MAX)}$ and Tuned Gain vs. Frequency at V_{CE}=15V, I_C=25 mA

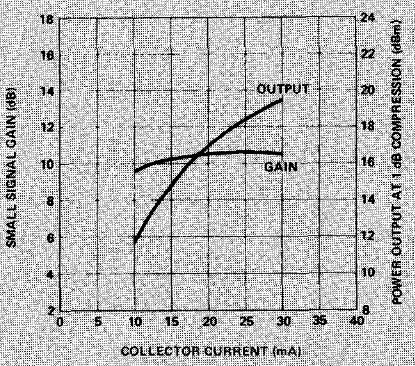


Figure 2. Typical Power Output at 1 dB Compression and Small Signal Gain vs. Collector Current at 4 GHz for V_{CE} = 15V.

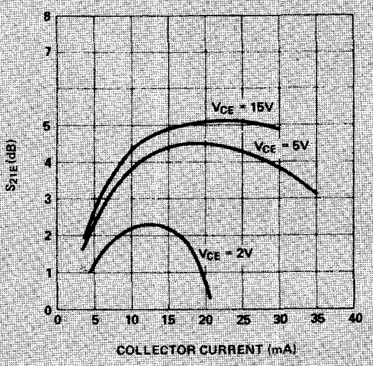


Figure 3. Typical $|S_{21E}|^2$ vs. Bias at 4 GHz.

Typical S-Parameters V_{CE} = 15V, I_C = 25mA

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (MHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	0.59	-66	30.8	34.6	146	-40.0	0.01	69	0.86	-18
500	0.58	-150	22.1	12.7	96	-33.2	0.02	44	0.51	-27
1000	0.59	-175	16.7	6.86	78	-30.5	0.03	51	0.44	-32
1500	0.59	173	13.3	4.61	64	-28.0	0.04	55	0.45	-39
2000	0.60	162	11.0	3.53	53	-25.7	0.05	55	0.44	-49
2500	0.61	156	8.9	2.79	43	-24.2	0.06	55	0.47	-60
3000	0.62	146	7.3	2.32	33	-22.6	0.07	56	0.48	-67
3500	0.63	139	5.9	1.96	22	-21.2	0.09	53	0.52	-79
4000	0.62	131	4.8	1.73	11	-19.7	0.10	50	0.55	-84
4500	0.61	123	3.5	1.50	1	-18.8	0.12	48	0.59	-93
5000	0.60	116	2.6	1.35	-9	-17.0	0.14	44	0.65	-102
5500	0.62	109	1.8	1.23	-19	-15.9	0.16	36	0.66	-113
6000	0.62	103	0.9	1.11	-28	-15.6	0.17	32	0.66	-123
6500	0.62	93	0.0	1.02	-37	-13.7	0.20	28	0.67	-131

HEWLETT hp PACKARD
COMPONENTS

NEW

GENERAL PURPOSE TRANSISTOR

HXTR-2102

Features

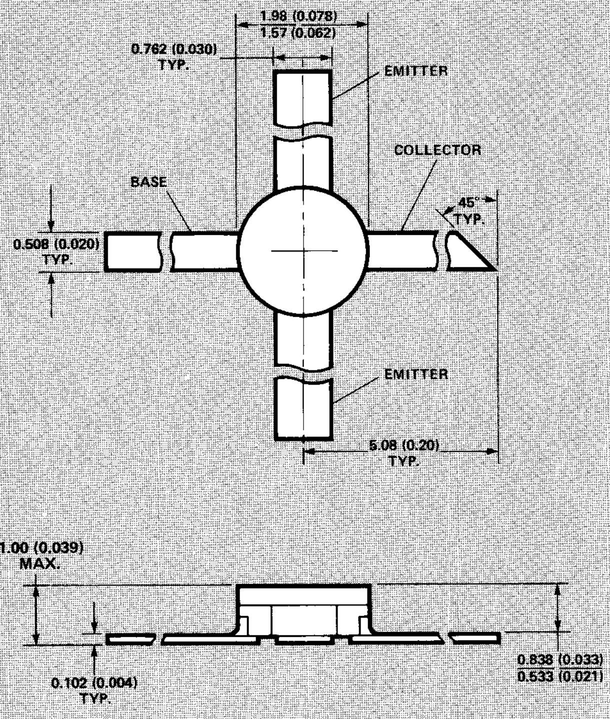
HIGH GAIN

- **15 dB Typical at 2 GHz**
- **11 dB Typical at 4 GHz**

WIDE DYNAMIC RANGE

RUGGED HERMETIC PACKAGE

- **Co-fired Metal/Ceramic Construction**



OUTLINE HPAC-70GT

DIMENSIONS IN MILLIMETERS (INCHES).

Description

The HXTR-2102 is an NPN bipolar transistor designed for high gain and wide dynamic range up to 6 GHz. The device utilizes ion implantation techniques and Ti/Pt/Au metallization in its manufacture. The chip is provided with a dielectric scratch protection over its active area.

The HXTR-2102 is supplied in the HPAC-70GT, a rugged metal/ceramic hermetic package, and is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

Electrical Specifications at $T_{CASE} = 25°C$

Symbol	Parameters and Test Conditions		MIL-STD-750 Test Method	Units	Min.	Typ.	Max.
BV_{CES}	Collector-Emitter Breakdown Voltage at $I_C = 100\mu A$		3011.1*	V	30		
I_{CEO}	Collector-Emitter Leakage Current at $V_{CE} = 15V$		3041.1	nA			500
I_{CBO}	Collector Cutoff Current at $V_{CB} = 15V$		3036.1	nA			100
h_{FE}	Forward Current Transfer Ratio at $V_{CE} = 15V$, $I_C = 15mA$		3076.1*	—	50	120	220
G_T	Tuned Gain	f=2 GHz 4 GHz		dB	13	15 11	
P_{1dB}	Power Output at 1 dB Compression	f=2 GHz 4 GHz		dBm		20 18.5	
	Bias Conditions for Above: $V_{CE} = 15V$, $I_C = 25mA$						

*300μs wide pulse measurement ≤2% duty cycle.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage[2]	25V
V_{CEO}	Collector to Emitter Voltage[2]	16V
V_{EBO}	Emitter to Base Voltage[2]	1.0V
I_C	DC Collector Current[2]	35 mA
P_T	Total Device Dissipation[3]	450 mW
T_J	Junction Temperature	200° C
T_{STG}	Storage Temperature	-65° C to +200° C

Notes:

1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device mean time between failure (MTBF) to below the design goal of 1 x 10^7 hours at T_J = 175° C (assumed Activation Energy = 1.5 eV).
2. T_{CASE} = 25° C.
3. Derate at 5.4 mW/° C, $T_C \geq 117°$ C.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	30V
V_{CEO}	Collector to Emitter Voltage	20V
V_{EBO}	Emitter to Base Voltage	1.5V
I_C	DC Collector Current	70 mA
P_T	Total Device Dissipation	900 mW
T_J	Junction Temperature	300° C
$T_{STG(MAX)}$	Maximum Storage Temperature	250° C
—	Lead Temperature (Soldering 10 seconds each lead)	+250° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

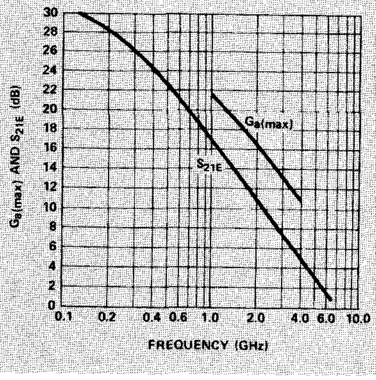


Figure 1. Typical $G_{a(max)}$ and S_{21E} vs. Frequency at V_{CE}=15V, I_C=25 mA.

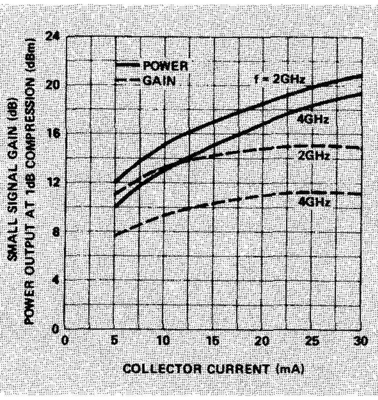


Figure 2. Typical Power Output at 1dB Compression and Small Signal Gain vs. Current for V_{CE}=15V

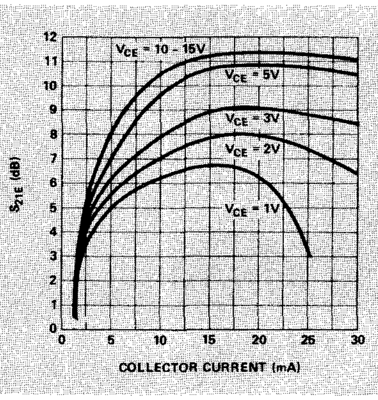


Figure 3. Typical S_{21E} vs. Current at 2 2 GHz.

Typical S-Parameters V_{CE} = 15V, I_C = 25mA

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (MHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	0.63	-58	30.5	33.4	149	-39.2	0.011	62	0.88	-16
200	0.63	-99	28.4	26.2	128	-35.9	0.016	49	0.72	-25
300	0.64	-122	26.1	20.3	115	-34.9	0.018	45	0.61	-28
400	0.64	-136	24.2	16.2	107	-33.6	0.021	42	0.54	-29
500	0.64	-146	22.6	13.4	101	-32.8	0.023	42	0.50	-31
600	0.64	-153	21.2	11.5	96	-32.4	0.024	43	0.48	-32
700	0.64	-158	19.9	9.9	92	-32.0	0.025	43	0.47	-33
800	0.64	-162	18.8	8.8	88	-31.7	0.026	45	0.47	-34
900	0.64	-166	17.8	7.8	85	-31.4	0.027	44	0.48	-34
1000	0.64	-170	16.9	7.0	83	-30.8	0.029	46	0.47	-35
1500	0.66	179	13.5	4.7	70	-29.1	0.035	49	0.44	-40
2000	0.65	172	11.1	3.6	60	-27.1	0.044	53	0.46	-50
2500	0.67	165	9.1	2.9	50	-25.7	0.052	55	0.47	-59
3000	0.64	161	7.6	2.4	40	-24.3	0.061	57	0.52	-66
3500	0.72	156	6.4	2.1	32	-23.3	0.068	53	0.51	-79
4000	0.69	149	5.3	1.8	22	-22.6	0.074	48	0.56	-85
4500	0.70	141	4.4	1.7	14	-21.8	0.081	44	0.55	-92
5000	0.72	136	3.3	1.5	6	-21.3	0.086	39	0.58	-101
5500	0.70	128	2.5	1.3	-3	-20.7	0.092	34	0.62	-109
6000	0.75	122	1.7	1.2	-11	-20.1	0.098	30	0.63	-118
6500	0.70	119	0.8	1.1	-20	-19.6	0.105	26	0.70	-127

HEWLETT PACKARD
COMPONENTS

NEW

LINEAR POWER TRANSISTOR

2N6701
(HXTR-5101)

太16.15

Features

HIGH P_{1dB} LINEAR POWER
23 dBm Typical at 2 GHz
22 dBm Typical at 4 GHz

HIGH P_{1dB} GAIN
13 dB Typical at 2 GHz
7.5 dB Typical at 4 GHz

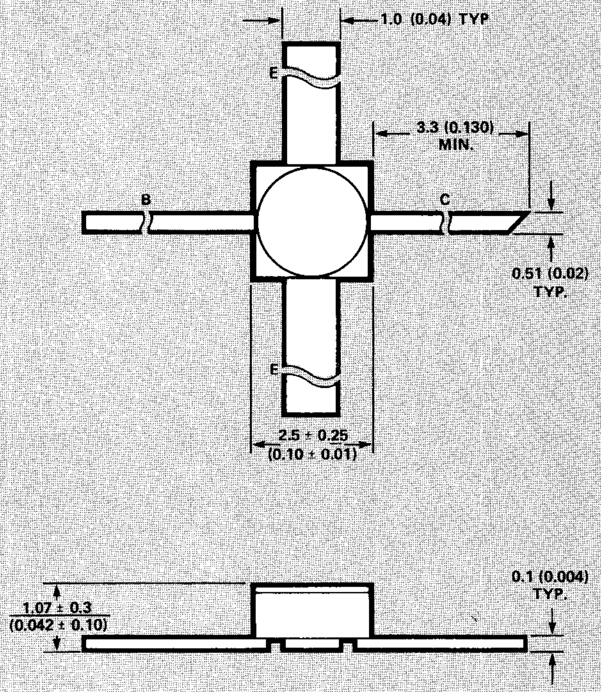
LOW DISTORTION

HIGH POWER-ADDED EFFICIENCY

MATCHING CONDITIONS INDEPENDENT OF OUTPUT POWER

INFINITE SWR TOLERANCE ABOVE 2 GHz

RUGGED HERMETIC PACKAGE



DIMENSIONS IN MILLIMETERS (INCHES).

HPAC-100 Package Outline

Description/Applications

The 2N6701 (HXTR-5101) is an NPN bipolar transistor designed for high output power and gain up to 5 GHz. To achieve excellent uniformity and reliability, the manufacturing process utilizes ion implantation, self-alignment techniques and Ti/Pt/Au metallization. The chip has a dielectric scratch protection over its active area and Ta_2N ballast resistors for ruggedness.

The superior gain, power, and distortion performance of the 2N6701 commend it for applications in radar, ECM, space, and commercial and military telecommunications. The 2N6701 features both guaranteed power output and associated gain at 1 dB gain compression.

The 2N6701 is supplied in the HPAC-100, a metal/ceramic hermetic package, and is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

Electrical Specifications at $T_{CASE} = 25°C$

Symbol	Parameters and Test Conditions		Test MIL-STD-750	Units	Min.	Typ.	Max.
BV_{CBO}	Collector-Base Breakdown Voltage at $I_C = 3mA$		3001.1*	V	40		
BV_{CEO}	Collector-Emitter Breakdown Voltage at $I_C = 15mA$		3011.1*	V	24		
BV_{EBO}	Emitter-Base Breakdown Voltage at $I_B = 30\mu A$		3026.1*	V	3.3		
I_{EBO}	Emitter-Base Leakage Current at V_{EB}=2V		3061.1	μA			2
I_{CES}	Collector-Emitter Leakage Current at V_{CE}=32V		3041.1	nA			200
I_{CBO}	Collector-Base Leakage Current at V_{CB}=20V		3036.1	nA			100
h_{FE}	Forward Current Transfer Ratio at V_{CE}=18V, $I_C = 30mA$		3076.1*		15	40	75
P_{1dB}	Power Output at 1dB Gain Compression	f=2GHz		dBm		23	
		4GHz			21	22	
G_{1dB}	Associated 1dB Compressed Gain	2GHz		dB		13	
		4GHz			6.5	7.5	
P_{SAT}	Saturated Power Output (8dB Gain)	2GHz		dBm		25.5	
	(3dB Gain)	4GHz				25	
η	Power-Added Efficiency at 1dB Compression	2GHz		%		35	
		4GHz				24	
IMD	Third Order Intermodulation Distortion (Reference to either tone), at P_O(PEP)= 22dBm	4GHz		dB		-30	
	Tuned for Maximum Output Power at 1dB Compression V_{CE}=18V, I_C=30mA						

*300μs wide pulse measurement at ≤2% duty cycle.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage[2]	40V
V_{CEO}	Collector to Emitter Voltage[2]	24V
V_{EBO}	Emitter to Base Voltage[2]	3.3V
I_C	DC Collector Current[2]	50 mA
P_T	Total Device Dissipation[3]	700 mW
T_J	Junction Temperature	200°C
T_{STG}	Storage Temperature	-65°C to +200°C

Notes:

1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device mean time between failure (MTBF) to below the design goal of 1 x 10^7 hours at T_J = 175°C (assumed Activation Energy = 1.5 eV). Corresponds to maximum rating for 2N6701.
2. T_{CASE} = 25°C.
3. See Figure 7 for derating conditions.

Absolute Maximum Ratings *

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	45V
V_{CEO}	Collector to Emitter Voltage	27V
V_{EBO}	Emitter to Base Voltage	4V
I_C	DC Collector Current	100 mA
P_T	Total Device Dissipation	1.1 W
T_J	Junction Temperature	300°C
$T_{STG(MAX)}$	Maximum Storage Temperature	250°C
—	Lead Temperature (Soldering 10 seconds each lead)	+250°C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

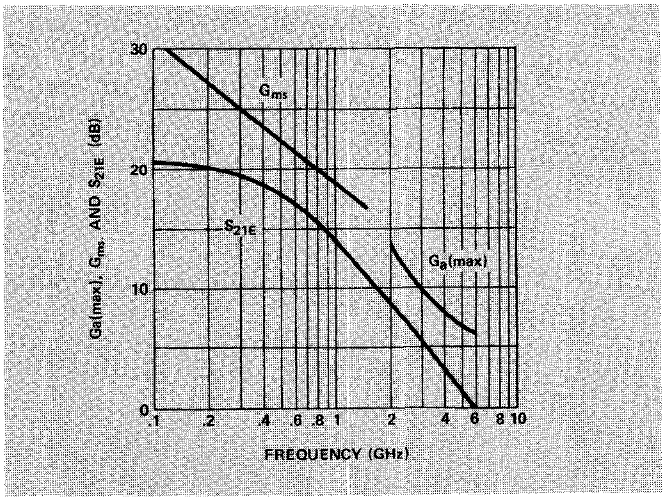


Figure 1. Typical Ga(max), Maximum Stable Gain (Gms), and S_{21E} vs. Frequency at V_{CE} = 18V, I_C = 30mA.

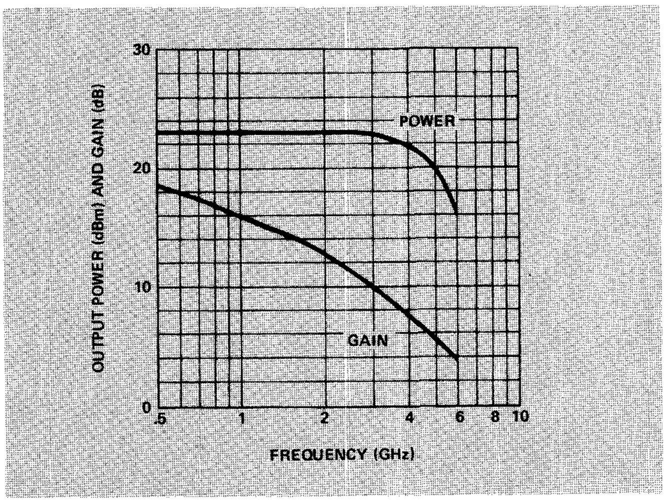


Figure 3. Typical P_{1dB} Linear Power and Associated 1dB Compressed Gain vs. Frequency at V_{CE} = 18V, I_C = 30mA.

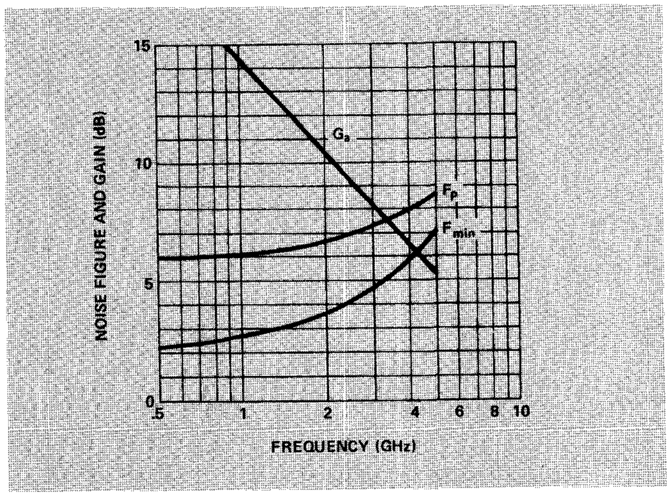


Figure 5. Typical Noise Figure (Fmin) and Associated Gain (Ga) when tuned for Minimum Noise vs. Frequency at V_{CE} = 18V, I_C = 10mA. Typical Noise Figure (Fp) when tuned for Max P_{1dB} at V_{CE} = 18V, I_C = 30mA.

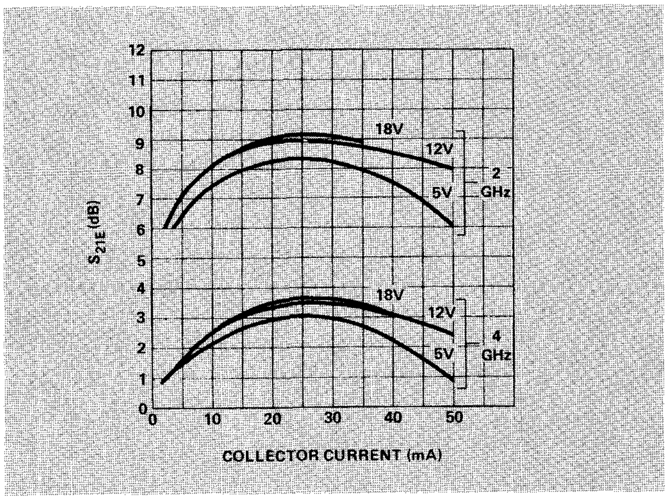


Figure 2. Typical S_{21E} vs. Current at 2 and 4GHz.

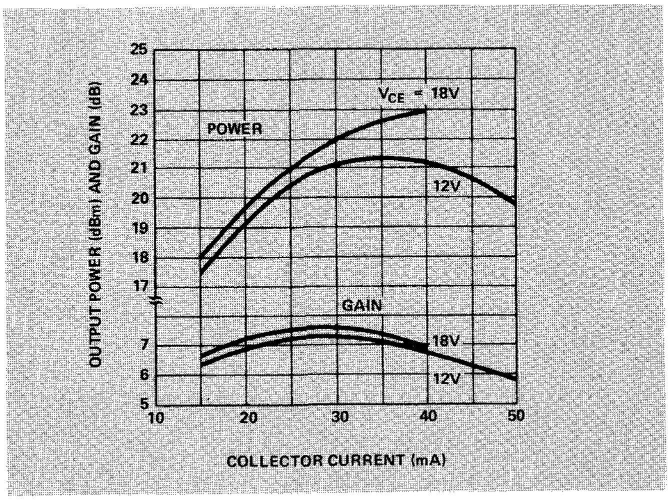


Figure 4. Typical P_{1dB} Linear Power and Associated 1dB Compressed Gain vs. Current at V_{CE} = 12 and 18V at 4GHz.

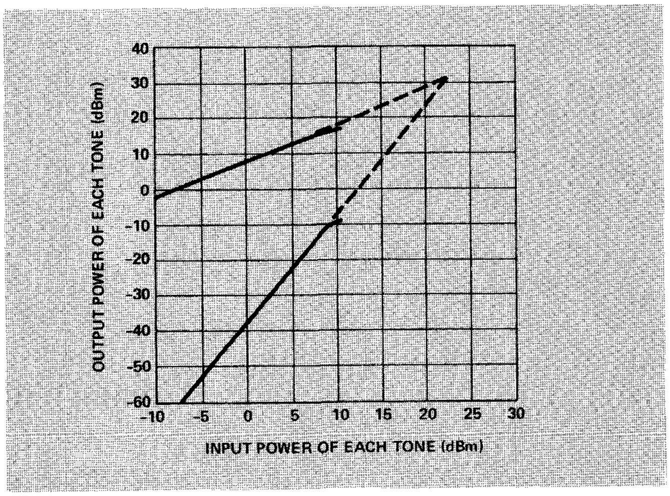


Figure 6. Typical Two Tone 3rd Order Intermodulation Distortion at 4GHz for a frequency separation of 5MHz at V_{CE} = 18V, I_C = 30mA.

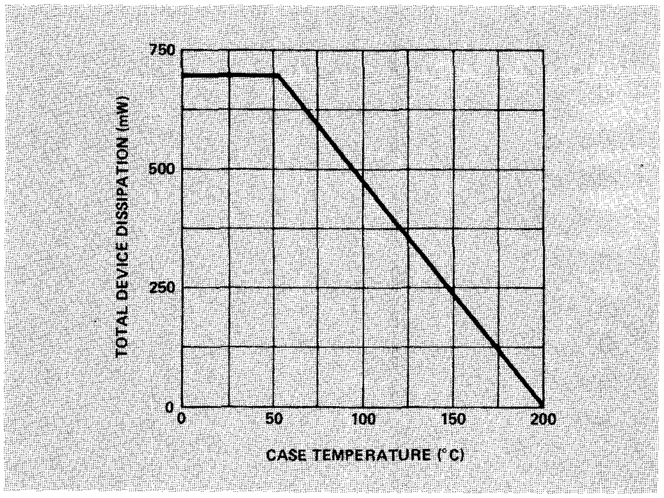


Figure 7. Maximum Power Dissipation Curve for θ_{jc} = 210° C/W, T_{jMAX} = 200° C.

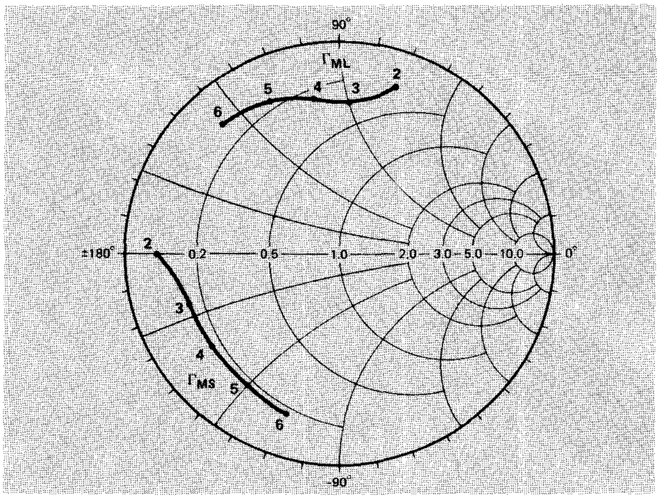


Figure 8. Typical Γ_{MS}, Γ_{ML}, (calculated from the average S-parameters) in the 2 to 6GHz frequency range, at V_{CE} = 18V, I_C = 30mA.

Typical S-Parameters V_{CE} = 18V, I_C = 30mA

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (MHz)	**Mag.**	**Ang.**	**(dB)**	**Mag.**	**Ang.**	**(dB)**	**Mag.**	**Ang.**	**Mag.**	**Ang.**
100	0.80	-19	20.6	10.7	165	-37	0.01	77	0.98	-8
200	0.78	-37	20.1	10.2	154	-31	0.03	67	0.94	-15
300	0.75	-53	19.5	9.44	143	-28	0.04	60	0.88	-21
400	0.72	-68	18.7	8.63	133	-27	0.05	53	0.83	-26
500	0.68	-81	17.9	7.87	124	-26	0.05	47	0.78	-30
600	0.66	-92	17.0	7.15	117	-25	0.06	42	0.73	-33
700	0.64	-102	16.2	6.52	110	-24	0.06	39	0.69	-36
800	0.62	-111	15.5	5.96	104	-24	0.07	36	0.66	-38
900	0.61	-119	14.8	5.49	99	-23	0.07	33	0.64	-41
1000	0.60	-126	14.1	5.08	94	-23	0.07	31	0.61	-43
1500	0.56	-151	11.2	3.64	75	-23	0.08	25	0.55	-51
2000	0.55	-169	8.9	2.80	59	-22	0.08	22	0.52	-61
2500	0.56	179	7.2	2.29	45	-21	0.09	21	0.53	-72
3000	0.55	168	5.7	1.93	33	-21	0.09	21	0.52	-79
3500	0.56	158	4.5	1.69	21	-20	0.10	20	0.55	-89
4000	0.54	148	3.5	1.50	10	-19	0.11	19	0.58	-96
4500	0.54	137	2.5	1.33	0	-19	0.11	18	0.58	-106
5000	0.52	128	1.6	1.21	-11	-18	0.13	16	0.62	-113
5500	0.54	115	1.0	1.12	-23	-17	0.14	14	0.60	-122
6000	0.54	108	0.0	1.01	-32	-17	0.15	11	0.64	-132

Typical S-Parameters V_{CE} = 15V, I_C = 15mA

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (MHz)	**Mag.**	**Ang.**	**(dB)**	**Mag.**	**Ang.**	**(dB)**	**Mag.**	**Ang.**	**Mag.**	**Ang.**
100	0.80	-18	19.4	9.35	166	-37	0.01	78	0.98	-7
200	0.78	-35	19.1	9.07	155	-31	0.02	69	0.95	-14
300	0.76	-50	18.5	8.44	145	-28	0.03	61	0.91	-20
400	0.73	-64	17.8	7.79	135	-26	0.04	55	0.86	-25
500	0.69	-77	17.1	7.16	127	-25	0.05	49	0.81	-29
600	0.67	-88	16.3	6.56	119	-24	0.06	44	0.76	-32
700	0.64	-97	15.5	6.02	113	-23	0.06	40	0.72	-35
800	0.62	-107	14.8	5.54	107	-23	0.06	37	0.69	-38
900	0.60	-115	14.2	5.13	101	-23	0.07	34	0.66	-40
1000	0.60	-122	13.5	4.76	96	-23	0.07	32	0.63	-43
1500	0.57	-148	10.8	3.47	76	-22	0.08	24	0.57	-53
2000	0.55	-166	8.6	2.69	60	-21	0.08	21	0.54	-63
2500	0.56	-178	6.9	2.21	46	-21	0.09	19	0.55	-75
3000	0.56	171	5.1	1.80	36	-20	0.09	21	0.50	-85
3500	0.56	160	4.3	1.65	21	-20	0.10	18	0.56	-91
4000	0.53	151	3.3	1.47	10	-19	0.11	18	0.59	-99
4500	0.53	141	2.3	1.30	0	-19	0.11	17	0.59	-108
5000	0.50	130	1.5	1.18	-10	-18	0.12	15	0.62	-116
5500	0.52	118	0.8	1.10	-22	-17	0.14	13	0.61	-124
6000	0.53	110	0.0	0.99	-31	-16	0.15	11	0.64	-135

HEWLETT hp PACKARD
COMPONENTS

NEW

LINEAR POWER TRANSISTOR

HXTR-5102

46-48

Features

HIGH P_{1dB} LINEAR POWER
29 dBm Typical at 2 GHz
27.5 dBm Typical at 4 GHz

HIGH P_{1dB} GAIN
11.5 dB Typical at 2 GHz
7 dB Typical at 4 GHz

PARTIAL MATCHING FOR BROADBAND OPERATION

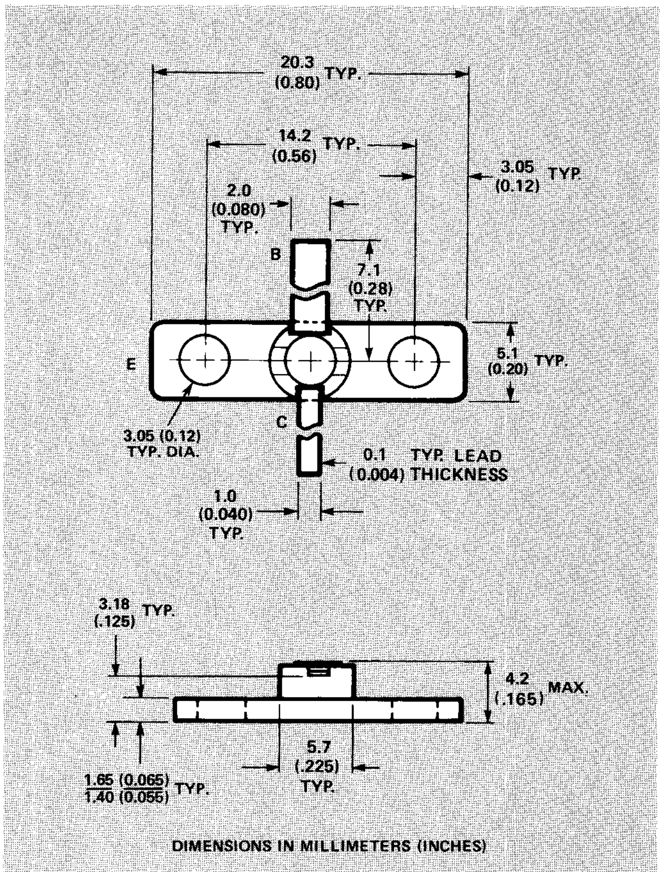
LOW DISTORTION

HIGH POWER-ADDED EFFICIENCY

MATCHING CONDITIONS INDEPENDENT OF OUTPUT POWER

INFINITE SWR TOLERANCE ABOVE 2 GHz

RUGGED HERMETIC PACKAGE



DIMENSIONS IN MILLIMETERS (INCHES)

HPAC-200 GB/GT Package Outline

Description/Applications

The HXTR-5102 is an NPN bipolar transistor designed for high output power and gain up to 5 GHz. To achieve excellent uniformity and reliability, the manufacturing process utilizes ion implantation, self-alignment techniques and Ti/Pt/Au metallization. The chip has dielectric scratch protection over its active area and Ta_2N ballast resistors for ruggedness. A silicone conformal coating protects the chip and matching network.

The superior power, gain and distortion performance of the HXTR-5102 commend it for use in broad and narrowband commercial and military telecommunications, radar and ECM applications. Additionally, its partial internal matching makes it ideal for broad bandwidth designs in the 2 to 5 GHz frequency range with minimal sacrifice of output power and gain.

The HXTR-5102 is supplied in the HPAC-200GB/GT, a metal/ceramic hermetic package with a BeO heat conductor, and is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

Electrical Specifications at T_{CASE} =25°C

Symbol	Parameters and Test Conditions		Test MIL-STD-750	Units	Min.	Typ.	Max.
BV_{CBO}	Collector-Base Breakdown Voltage at I_C=10 mA		3001.1*	V	40		
BV_{CEO}	Collector-Emitter Breakdown Voltage at I_C=50 mA		3011.1*	V	24		
BV_{EBO}	Emitter-Base Breakdown Voltage at I_B=100 μA		3026.1*	V	3.3		
I_{EBO}	Emitter-Base Leakage Current at V_{EB}=2 V		3061.1	μA			5
I_{CES}	Collector-Emitter Leakage Current at V_{CE}=32 V		3041.1	nA			200
I_{CBO}	Collector-Base Leakage Current at V_{CB}=20 V		3036.1	nA			100
h_{FE}	Forward Current Transfer Ratio at V_{CE}=18 V, I_C=110 mA		3076.1*		15	40	75
P_{1dB}	Power Output at 1dB Gain Compression	f=2 GHz		dBm		29	
		4 GHz			26.5	27.5	
G_{1dB}	Associated 1dB Compressed Gain	2 GHz		dB		11.5	
		4 GHz			6.0	7.0	
P_{SAT}	Saturated Power Output (8 dB Gain)	2 GHz		dBm		31.0	
	(3 dB Gain)	4 GHz				29.5	
η	Power-Added Efficiency at 1 dB Compression	2 GHz		%		37	
		4 GHz				23	
IMD	Third Order Intermodulation Distortion (Reference to either tone), at P_O(PEP)=.5 W	4 GHz		dB		-30	
	Tuned for Maximum Output Power at 1dB Compression V_{CE}=18 V, I_C=110 mA						

*300 μs wide pulse measurement at ≤2% duty cycle.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage[2]	40V
V_{CEO}	Collector to Emitter Voltage[2]	22V
V_{EBO}	Emitter to Base Voltage[2]	3.3V
I_C	DC Collector Current[2]	150 mA
P_T	Total Device Dissipation[3]	2.7 W
T_J	Junction Temperature	200°C
T_{STG}	Storage Temperature	-65°C to +200°C

Notes:
1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device mean time between failure (MTBF) to below the design goal of 1 x 10^7 hours at T_J = 175°C (assumed Activation Energy = 1.5 eV).
2. T_{CASE} = 25°C.
3. See Figure 7 for derating conditions.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	45V
V_{CEO}	Collector to Emitter Voltage	27V
V_{EBO}	Emitter to Base Voltage	4V
I_C	DC Collector Current	250 mA
P_T	Total Device Dissipation	4W
T_J	Junction Temperature	300°C
$T_{STG(MAX)}$	Maximum Storage Temperature	250°C
—	Lead Temperature (Soldering 10 seconds each lead)	+250°C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

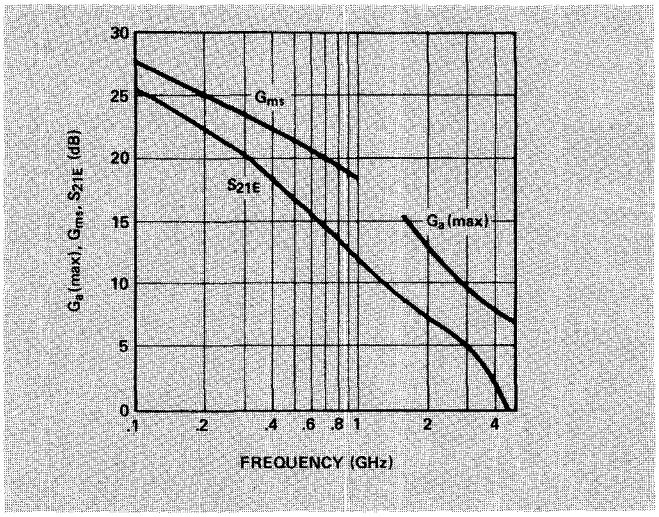


Figure 1. Typical G_a(max), Maximum Stable Gain (G_{ms}), and S_{21E} vs. Frequency at V_{CE} = 18V, I_C = 110mA.

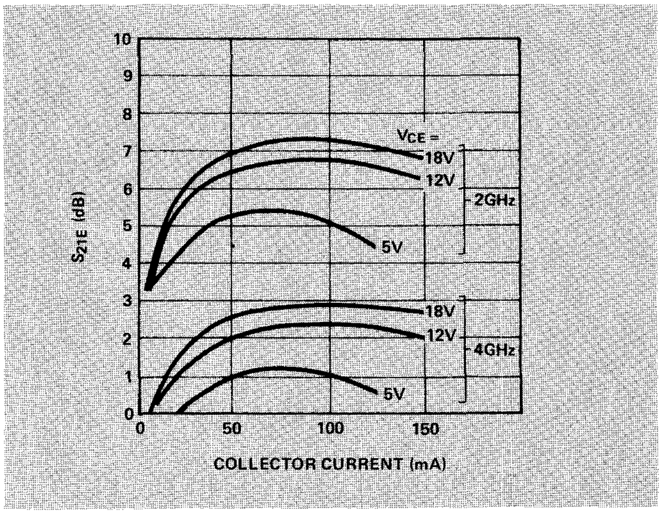


Figure 2. Typical S_{21E} vs. Current at 2 and 4GHz.

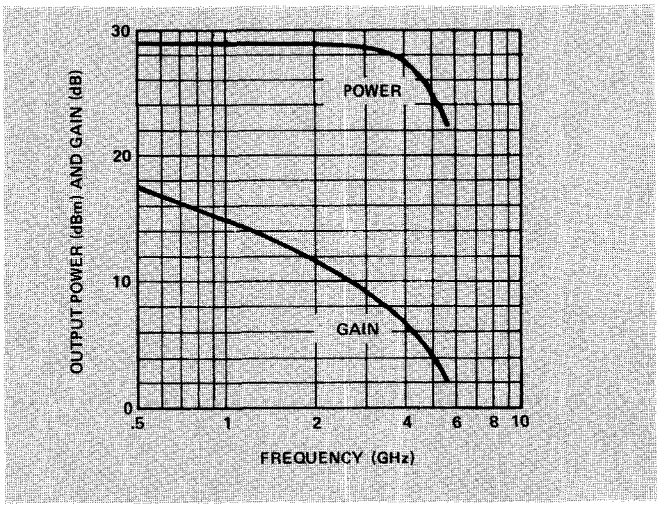


Figure 3. Typical P_{1dB} Linear Power and Associated 1dB Compressed Gain vs. Frequency at V_{CE} = 18V, I_C = 110mA.

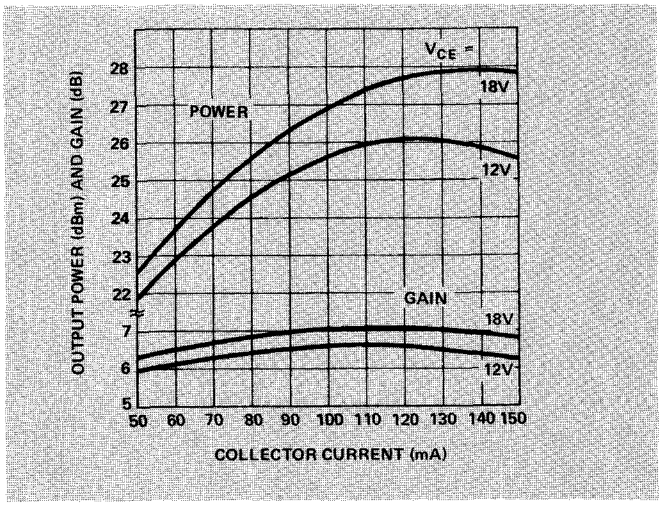


Figure 4. Typical P_{1dB} Linear Power and Associated 1dB Compressed Gain vs. Current at V_{CE} = 12 and 18V at 4GHz.

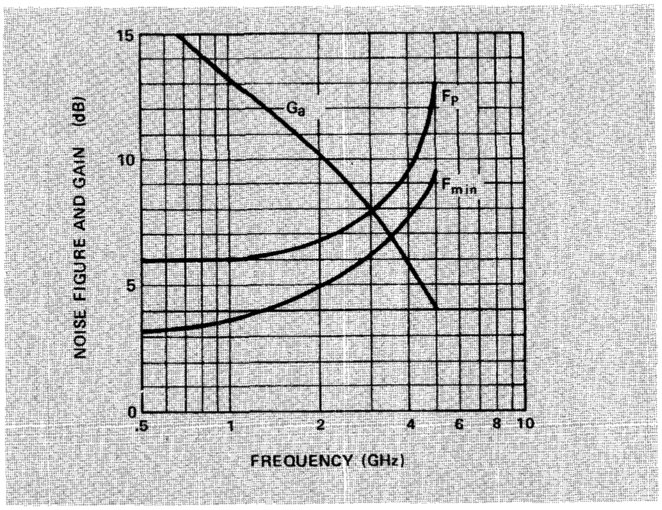


Figure 5. Typical Noise Figure (Fmin) and Associated Gain (G_a) when tuned for Minimum Noise vs. Frequency at V_{CE} = 18V, I_C = 25mA. Typical Noise Figure (Fp) when tuned for Max P_{1dB} at V_{CE} = 18V, I_C = 110mA.

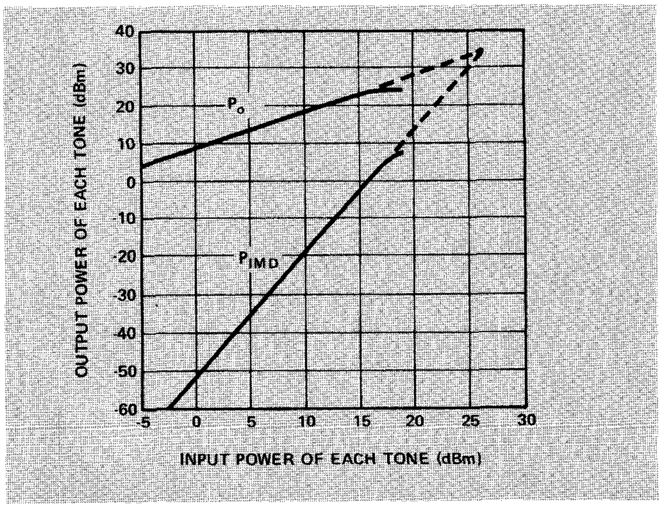


Figure 6. Typical Two Tone 3rd Order Intermodulation Distortion at 4GHz for a frequency separation of 5MHz at V_{CE} = 18V, I_C = 110mA.

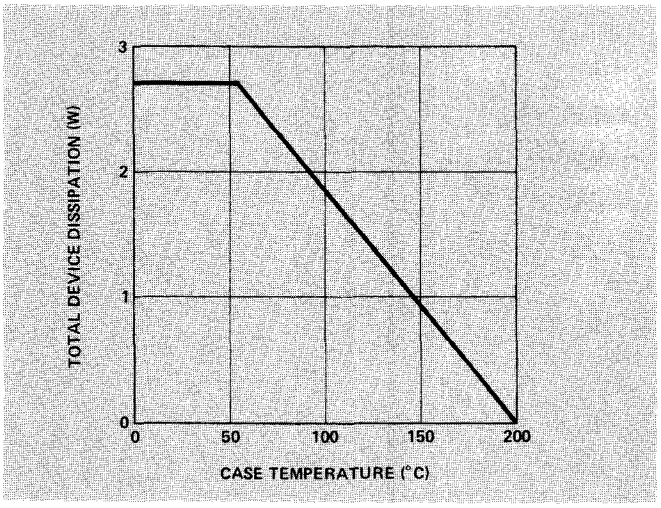


Figure 7. Maximum Power Dissipation Curve for θ_{jc} = 55° C/W, T_{jMAX} = 200° C.

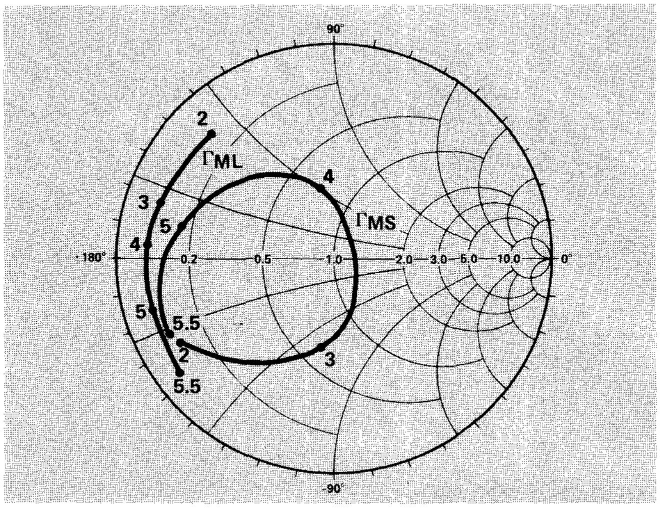


Figure 8. Typical Γ_{MS}, Γ_{ML} (calculated from the average S-parameters) in the 2 to 5.5GHz frequency range, for V_{CE} = 18V, I_C = 110mA.

Typical S-Parameters V_{CE} = 18 V, I_C = 110 mA

	S11		S21			S12			S22	
Freq. (MHz)	**Mag.**	**Ang.**	**(dB)**	**Mag.**	**Ang.**	**(dB)**	**Mag.**	**Ang.**	**Mag.**	**Ang**
100	0.55	-74	25.4	18.6	146	-31	0.03	56	0.85	-29
200	0.65	-109	22.7	13.6	123	-28	0.04	39	0.68	-47
300	0.70	-134	20.8	10.9	108	-27	0.05	28	0.55	-59
400	0.72	-144	18.6	8.47	97	-26	0.05	21	0.48	-65
500	0.74	-158	17.2	7.22	88	-26	0.05	17	0.42	-74
600	0.73	-160	15.6	5.99	81	-25	0.05	13	0.41	-75
700	0.74	-167	14.6	5.39	76	-25	0.05	11	0.39	-79
800	0.74	-170	13.4	4.66	69	-25	0.06	8	0.39	-82
900	0.74	-175	12.7	4.32	64	-25	0.06	8	0.38	-86
1000	0.74	-178	11.8	3.91	59	-25	0.06	7	0.37	-92
1500	0.71	166	9.0	2.82	34	-24	0.06	-2	0.43	-107
2000	0.64	153	7.3	2.32	10	-23	0.07	-8	0.51	-119
2500	0.52	140	6.3	2.07	-17	-22	0.08	-22	0.61	-133
3000	0.32	129	5.4	1.86	-49	-21	0.09	-42	0.73	-148
3500	0.15	158	3.8	1.55	-83	-20	0.09	-67	0.77	-165
4000	0.32	-145	2.8	1.38	-113	-22	0.08	-98	0.80	-177
4500	0.52	-158	0.0	1.00	-142	-24	0.06	132	0.82	171
5000	0.70	176	-1.9	0.81	-170	-28	0.04	50	0.87	159
5500	0.78	155	-3.0	0.71	161	-28	0.04	85	0.83	142
6000	0.85	119	-3.9	0.64	121	-19	0.11	16	0.93	121

HEWLETT PACKARD
COMPONENTS

LINEAR POWER TRANSISTOR

HXTR-5103

NEW

T 17-08

Features

HIGH P_{1dB} LINEAR POWER
23 dBm Typical at 2 GHz

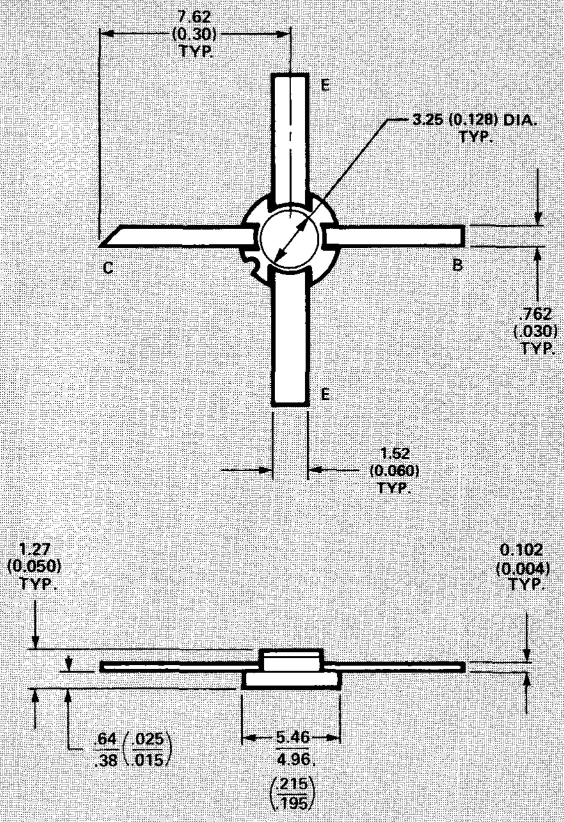
HIGH P_{1dB} GAIN
11 dB Typical at 2 GHz

LOW DISTORTION

HIGH POWER-ADDED EFFICIENCY

MATCHING CONDITIONS INDEPENDENT OF OUTPUT POWER

RUGGED HERMETIC PACKAGE



ALL DIMENSIONS ARE IN MILLIMETERS (INCHES).

HPAC-200 PACKAGE OUTLINE

Description/Applications

The HXTR-5103 is an NPN bipolar transistor designed for high gain and linear output power up to 5 GHz. To achieve excellent uniformity and reliability, the manufacturing process utilizes ion implantation, self-alignment techniques, and Ti/Pt/Au metallization. The chip has dielectric scratch protection over its active area and Ta_2N ballast resistors for ruggedness.

The superior power, gain and distortion performance of the HXTR-5103 commend it for use in RF and IF applications in radar, ECM, space, and other commercial and military communications.

The HXTR-5103 utilizes the HPAC-200, a metal/ceramic hermetic package with a BeO heat conductor, and is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

Electrical Specifications at $T_{CASE}=25°C$

Symbol	Parameters and Test Conditions	Test MIL-STD-750	Units	Min.	Typ.	Max.
BV_{CBO}	Collector-Base Breakdown Voltage at $I_C=3mA$	3001.1*	V	40		
BV_{CEO}	Collector-Emitter Breakdown Voltage at $I_C=15mA$	3011.1*	V	24		
BV_{EBO}	Emitter-Base Breakdown Voltage at $I_B=30\mu A$	3026.1*	V	3.3		
I_{EBO}	Emitter-Base Leakage Current at $V_{EB}=2V$	3061.1	μA			2
I_{CES}	Collector-Emitter Leakage Current at $V_{CE}=32V$	3041.1	nA			200
I_{CBO}	Collector-Base Leakage Current at $V_{CB}=20V$	3036.1	nA			100
h_{FE}	Forward Current Transfer Ratio at $V_{CE}=18V$, $I_C=30mA$	3076.1*		15	40	75
P_{1dB}	Power Output at 1dB Gain Compression f= 2GHz		dBm	22	23	
G_{1dB}	Associated 1dB Compressed Gain 2GHz		dB	9.5	11	
P_{SAT}	Saturated Power Output (Gain=5dB) 2GHz		dBm		25	
η	Power-Added Efficiency at 1dB Compression 2GHz		%		34	
IMD	Third Order Intermodulation Distortion (Reference to either tone), at $P_O(PEP)=.2W$ 2GHz		dB		-30	
	Tuned for Maximum Output Power at 1dB Compression $V_{CE}=18V$, $I_C=30mA$					

*300μs wide pulse measurement at ≤2% duty cycle.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage[2]	40V
V_{CEO}	Collector to Emitter Voltage[2]	24V
V_{EBO}	Emitter to Base Voltage[2]	3.3V
I_C	DC Collector Current[2]	50 mA
P_T	Total Device Dissipation[3]	700 mW
T_J	Junction Temperature	200°C
T_{STG}	Storage Temperature	-65°C to +200°C

Notes:
1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device mean time between failure (MTBF) to below the design goal of 1×10^7 hours at $T_J = 175°C$ (assumed Activation Energy = 1.5 eV).
2. $T_{CASE} = 25°C$.
3. See Figure 7 for derating conditions.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	45V
V_{CEO}	Collector to Emitter Voltage	27V
V_{EBO}	Emitter to Base Voltage	4.0V
I_C	DC Collector Current	100 mA
P_T	Total Device Dissipation	1.4 W
T_J	Junction Temperature	300°C
$T_{STG(MAX)}$	Maximum Storage Temperature	250°C
—	Lead Temperature (Soldering 10 seconds each lead)	+250°C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

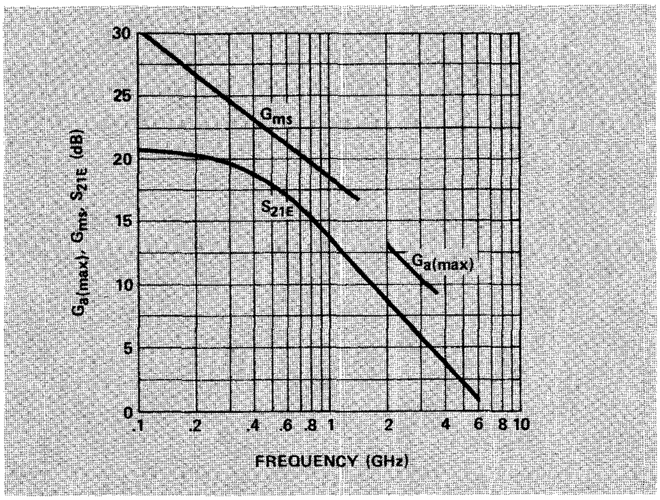


Figure 1. Typical G_a(max), Maximum Stable Gain (G_{ms}), and S_{21E} vs. Frequency at V_{CE} = 18V, I_C = 30mA.

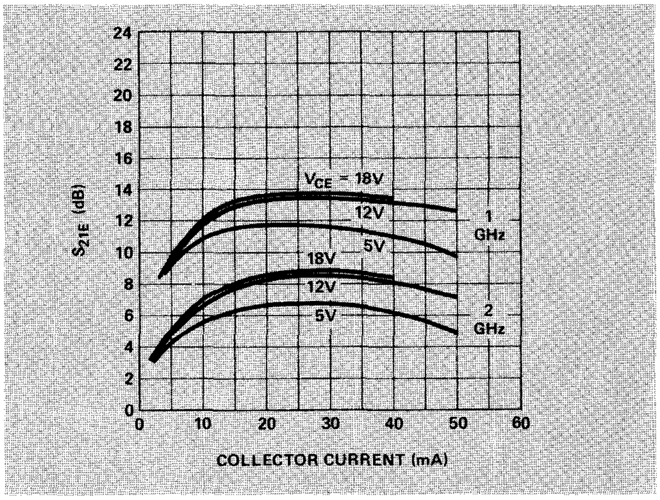


Figure 2. Typical S_{21E} vs. Current at 1 and 2GHz.

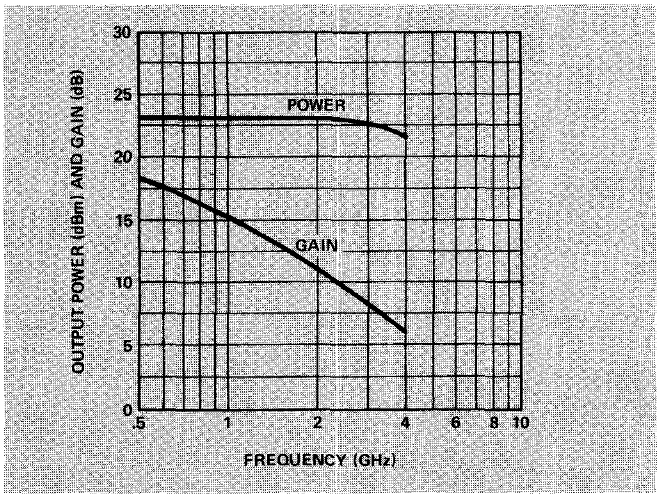


Figure 3. Typical P_{1dB} Linear Power and Associated 1dB Compressed Gain vs. Frequency at V_{CE} = 18V, I_C = 30mA.

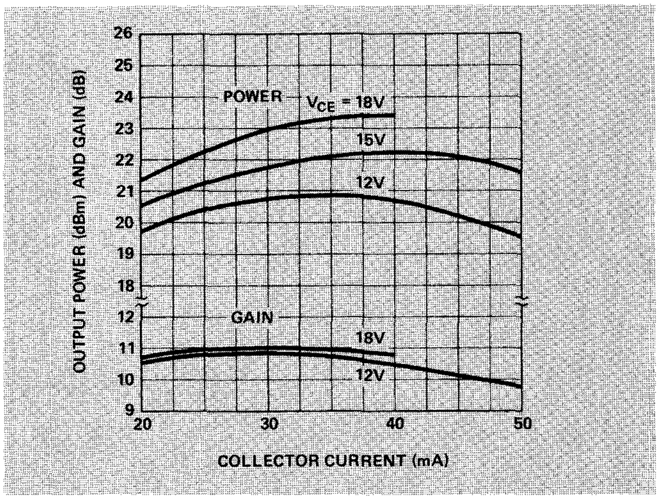


Figure 4. Typical P_{1dB} Linear Output Power and Associated 1dB Compressed Gain vs. Current at 2 GHz.

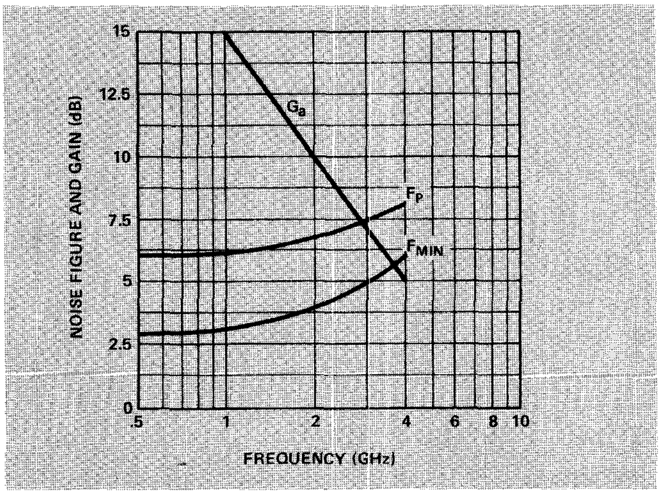


Figure 5. Typical Noise Figure (Fmin) and Associated Gain (G_a) vs. Frequency when tuned for Minimum Noise at V_{CE} = 18V, I_C = 10mA. Typical Noise Figure (Fp) when tuned for Max P_{1dB} at V_{CE} = 18V, I_C = 30mA.

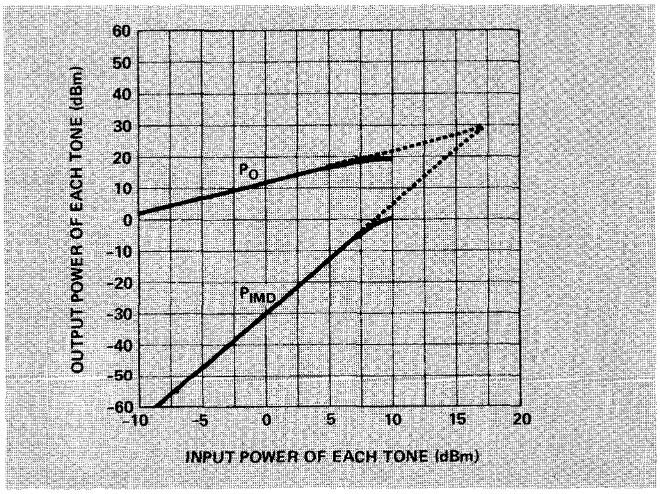


Figure 6. Typical Two Tone 3rd Order Intermodulation Distortion at 2GHz for a frequency separation of 5MHz at V_{CE} = 18V, I_C = 30mA.

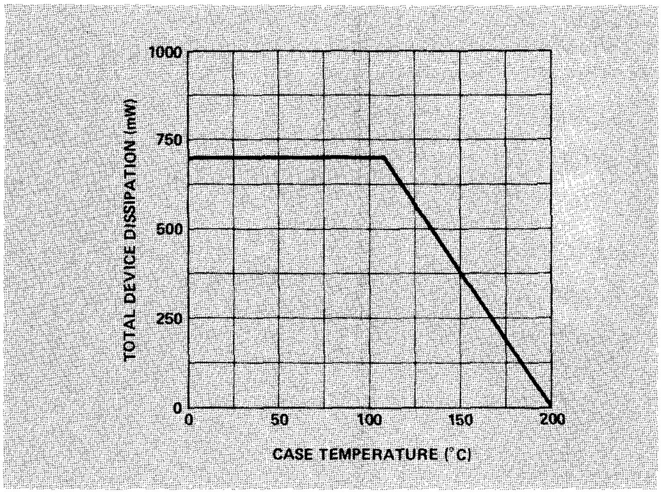


Figure 7. Power Dissipation Curve for θ_{jc} = 125°C/W, T_{jMAX} = 200°C.

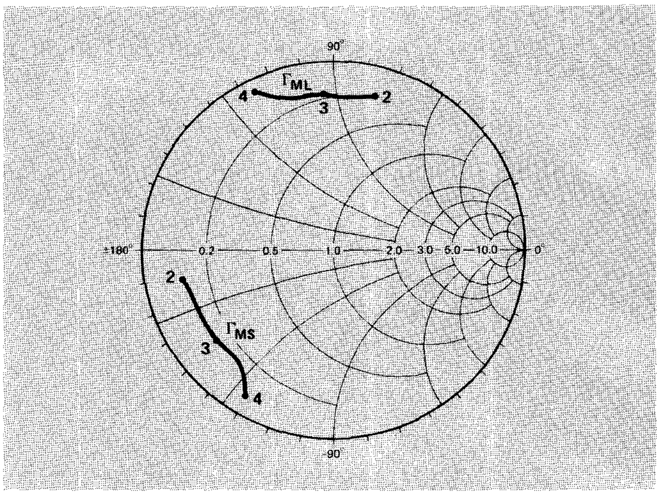


Figure 8. Typical Γ_{MS}, Γ_{ML} (Calculated from the Average S-Parameters) in the 2 to 4GHz Frequency Range for V_{CE} = 18V, I_C = 30mA.

Typical S-Parameters V_{CE} = 18V, I_C = 30mA

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (MHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	0.74	-20	20.7	10.9	165	-37	0.01	79	0.98	-9
200	0.71	-40	20.3	10.3	152	-32	0.03	68	0.94	-17
300	0.68	-57	19.6	9.49	140	-29	0.04	62	0.89	-23
400	0.65	-72	18.7	8.65	130	-27	0.04	55	0.84	-28
500	0.62	-86	17.8	7.77	121	-26	0.05	49	0.79	-33
600	0.60	-97	16.9	7.01	113	-25	0.06	44	0.75	-37
700	0.58	-108	16.2	6.43	106	-25	0.06	41	0.71	-40
800	0.55	-116	15.4	5.87	100	-24	0.06	38	0.68	-42
900	0.54	-124	14.6	5.38	94	-24	0.07	35	0.65	-44
1000	0.52	-131	13.8	4.91	88	-23	0.07	33	0.63	-46
1500	0.49	-159	11.0	3.53	66	-22	0.08	25	0.58	-59
2000	0.47	-179	8.8	2.77	48	-21	0.09	22	0.56	-67
2500	0.47	165	7.1	2.27	32	-20	0.10	18	0.56	-81
3000	0.45	151	5.8	1.95	17	-19	0.11	15	0.59	-90
3500	0.45	138	4.7	1.71	2	-18	0.12	10	0.59	-103
4000	0.42	123	3.7	1.54	-11	-17	0.14	4	0.64	-111
4500	0.41	110	3.2	1.44	-24	-16	0.16	1	0.65	-121
5000	0.39	89	2.2	1.29	-38	-15	0.17	-6	0.69	-131
5500	0.39	74	1.4	1.18	-53	-14	0.19	-12	0.69	-139
6000	0.37	55	0.7	1.09	-64	-13	0.22	-17	0.69	-148

Typical S-Parameters V_{CE} = 15V, I_C = 15mA

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (MHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	0.74	-19	19.1	9.05	164	-37	0.01	81	0.98	-8
200	0.70	-37	18.8	8.76	152	-31	0.03	68	0.94	-15
300	0.67	-54	18.2	8.16	141	-28	0.04	60	0.90	-21
400	0.63	-69	17.5	7.52	130	-27	0.05	53	0.85	-26
500	0.60	-83	16.8	6.90	121	-26	0.05	48	0.80	-31
600	0.58	-95	16.0	6.32	113	-25	0.06	43	0.76	-35
700	0.57	-105	15.2	5.78	107	-24	0.06	40	0.73	-38
800	0.55	-113	14.5	5.29	101	-24	0.07	37	0.70	-40
900	0.54	-121	13.8	4.88	95	-23	0.07	34	0.67	-43
1000	0.52	-128	13.0	4.48	89	-23	0.07	31	0.65	-45
1500	0.48	-156	10.2	3.23	66	-22	0.08	25	0.60	-55
2000	0.46	-177	8.0	2.51	48	-21	0.09	21	0.56	-65
2500	0.46	167	6.3	2.00	31	-20	0.10	18	0.57	-77
3000	0.45	153	5.0	1.78	16	-19	0.11	16	0.59	-86
3500	0.44	140	3.8	1.56	0	-18	0.12	12	0.60	-98
4000	0.43	126	2.8	1.38	-13	-17	0.14	8	0.64	-106
4500	0.41	112	1.9	1.24	-26	-16	0.15	4	0.64	-114
5000	0.38	93	1.0	1.12	-40	-15	0.17	-1	0.68	-123
5500	0.39	74	0.8	1.09	-55	-14	0.20	-6	0.70	-130
6000	0.37	56	-0.3	0.96	-67	-13	0.23	-12	0.69	-139

HEWLETT PACKARD

COMPONENTS

LINEAR POWER TRANSISTOR

HXTR-5104

26-70

NEW

Features

HIGH P_{1dB} LINEAR POWER
29 dBm Typical at 2 GHz

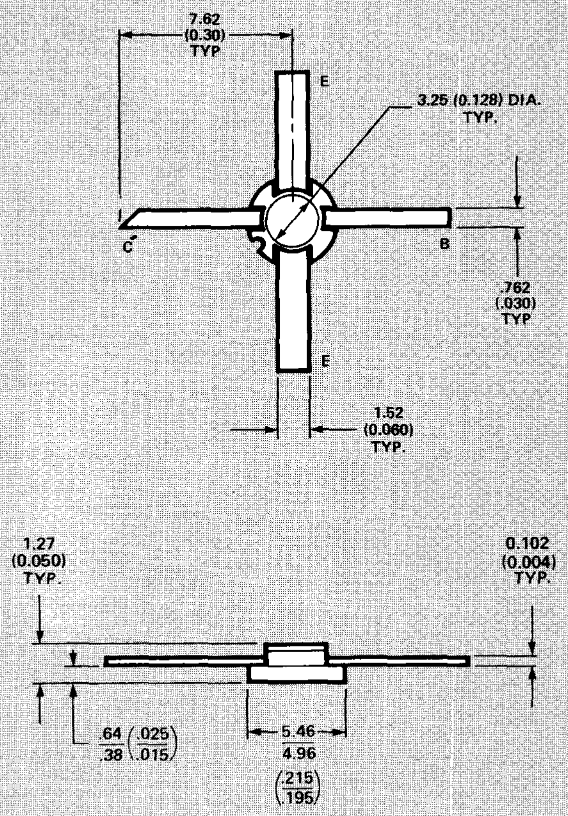
HIGH P_{1dB} GAIN
9 dB Typical at 2 GHz

LOW DISTORTION

HIGH POWER-ADDED EFFICIENCY

MATCHING CONDITIONS INDEPENDENT OF OUTPUT POWER

RUGGED HERMETIC PACKAGE



ALL DIMENSIONS ARE IN MILLIMETERS (INCHES).

HPAC-200 PACKAGE OUTLINE

Description/Applications

The HXTR-5104 is an NPN bipolar transistor designed for high gain and linear output power up to 4 GHz. To achieve excellent uniformity and reliability, the manufacturing process utilizes ion implantation, self-alignment techniques, and Ti/Pt/Au metallization. The chip has dielectric scratch protection over its active area and Ta_2N ballast resistors for ruggedness.

The superior power, gain and distortion performance of the HXTR-5104 commend it for use in RF and IF applications in radar, ECM, space, and other commercial and military communications.

The HXTR-5104 utilizes the HPAC-200, a metal/ceramic hermetic package with a BeO heat conductor, and is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

Electrical Specifications at $T_{CASE}=25°C$

Symbol	Parameters and Test Conditions	Test MIL-STD-750	Units	Min.	Typ.	Max.
BV_{CBO}	Collector-Base Breakdown Voltage at $I_C=10mA$	3001.1*	V	40		
BV_{CEO}	Collector-Emitter Breakdown Voltage at $I_C=50mA$	3011.1*	V	24		
BV_{EBO}	Emitter-Base Breakdown Voltage at $I_B=100\mu A$	3026.1*	V	3.3		
I_{EBO}	Emitter-Base Leakage Current at $V_{EB}=2V$	3061.1	µA			10
I_{CES}	Collector-Emitter Leakage Current at $V_{CE}=32V$	3041.1	nA			200
I_{CBO}	Collector-Base Leakage Current at $V_{CB}=20V$	3036.1	nA			100
h_{FE}	Forward Current Transfer Ratio at $V_{CE}=18V$, $I_C=110mA$	3076.1*		15	40	75
P_{1dB}	Power Output at 1dB Gain Compression f= 2GHz		dBm	28	29	
G_{1dB}	Associated 1dB Compressed Gain 2GHz		dB	8	9	
P_{SAT}	Saturated Power Output (Gain=5dB) 2GHz		dBm		31	
η	Power-Added Efficiency at 1dB Compression 2GHz		%		35	
IMD	Third Order Intermodulation Distortion (Reference to either tone), at $P_O(PEP)=0.7W$ 2GHz		dB		-30	
	Tuned for Maximum Output Power at 1dB Compression $V_{CE}=18V$, $I_C=110mA$					

*300µs wide pulse measurement at ≤2% duty cycle.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage[2]	40V
V_{CEO}	Collector to Emitter Voltage[2]	22V
V_{EBO}	Emitter to Base Voltage[2]	3.3V
I_C	DC Collector Current[2]	150 mA
P_T	Total Device Dissipation[3]	2.7 W
T_J	Junction Temperature	200°C
T_{STG}	Storage Temperature	-65°C to +200°C

Notes:
1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device mean time between failure (MTBF) to below the design goal of 1 x 10^7 hours at $T_J = 175°C$ (assumed Activation Energy = 1.5 eV).
2. $T_{CASE} = 25°C$.
3. See Figure 7 for derating conditions.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	45V
V_{CEO}	Collector to Emitter Voltage	27V
V_{EBO}	Emitter to Base Voltage	4V
I_C	DC Collector Current	250 mA
P_T	Total Device Dissipation	4 W
T_J	Junction Temperature	300°C
$T_{STG(MAX)}$	Maximum Storage Temperature	250°C
—	Lead Temperature (Soldering 10 seconds each lead)	+250°C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

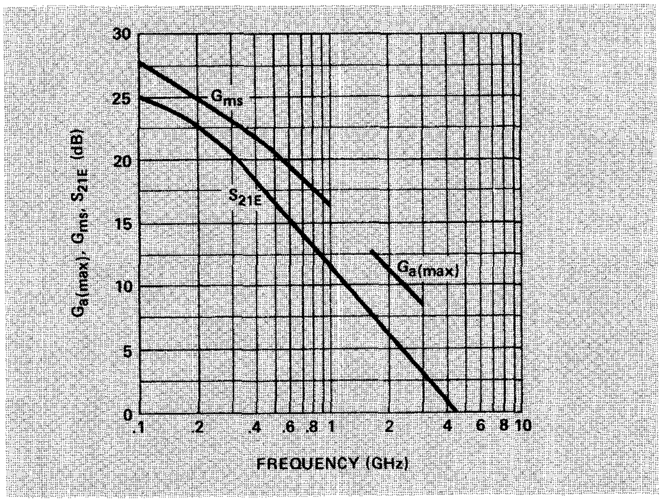


Figure 1. Typical $G_{a(max)}$, Maximum Stable Gain (G_{ms}), and S_{21E} vs. Frequency at V_{CE} = 18V, I_C = 110mA.

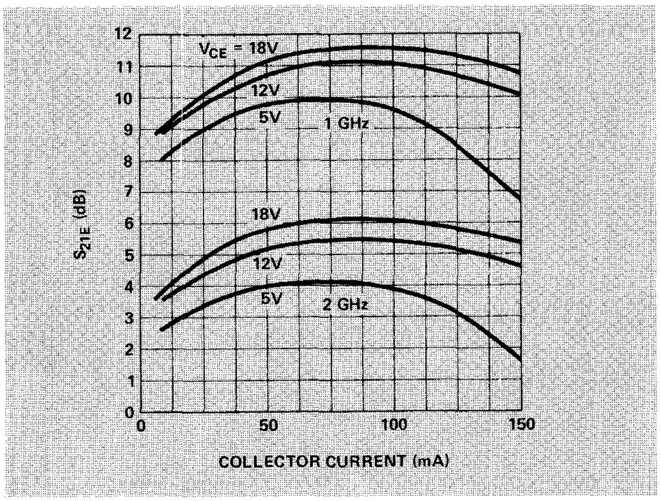


Figure 2. Typical S_{21E} vs. Current at 1 and 2GHz.

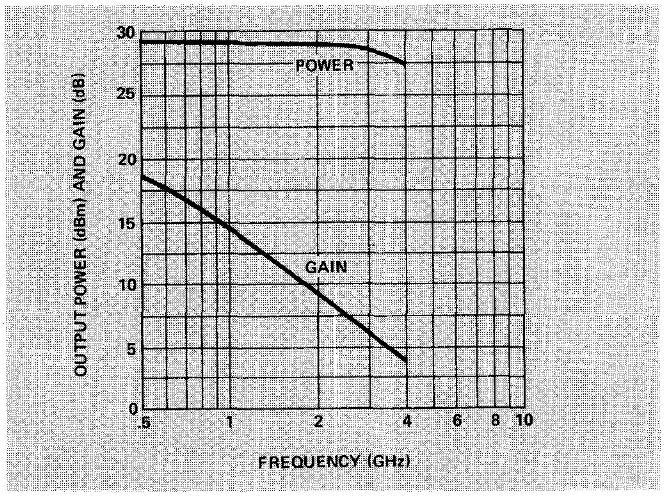


Figure 3. Typical P_{1dB} Linear Power and Associated 1dB Compressed Gain vs. Frequency at V_{CE} = 18V, I_C = 110mA.

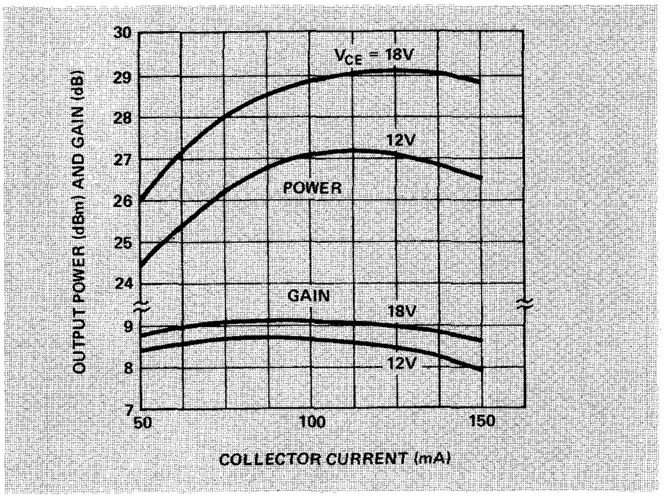


Figure 4. Typical P_{1dB} Linear Power and Associated 1dB Compressed Gain vs. Current at V_{CE} = 12 and 18V at 2 GHz.

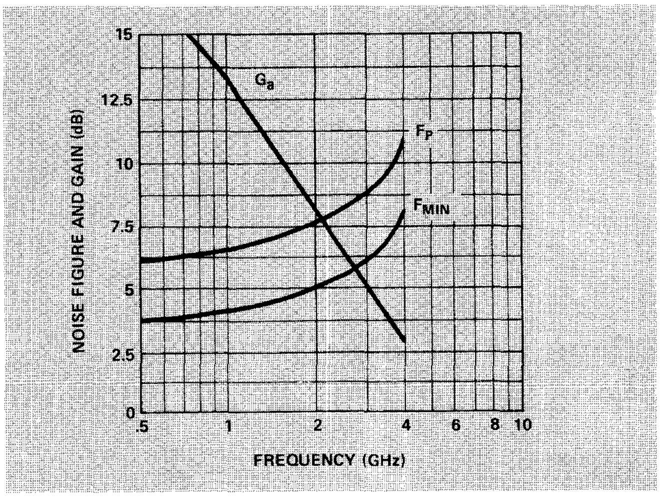


Figure 5. Typical Noise Figure (Fmin) and Associated Gain (G_a) vs. Frequency when tuned for Minimum Noise at V_{CE} = 18V, I_C = 25mA. Typical Noise Figure (Fp) when tuned for Max P_{1dB} at V_{CE} = 18V, I_C = 110mA.

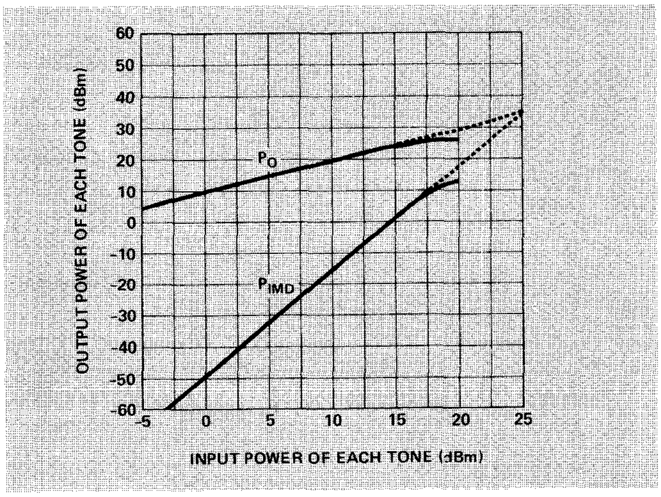


Figure 6. Typical Two Tone 3rd Order Intermodulation Distortion at 2GHz for a frequency separation of 5MHz at V_{CE} = 18V, I_C = 110mA.

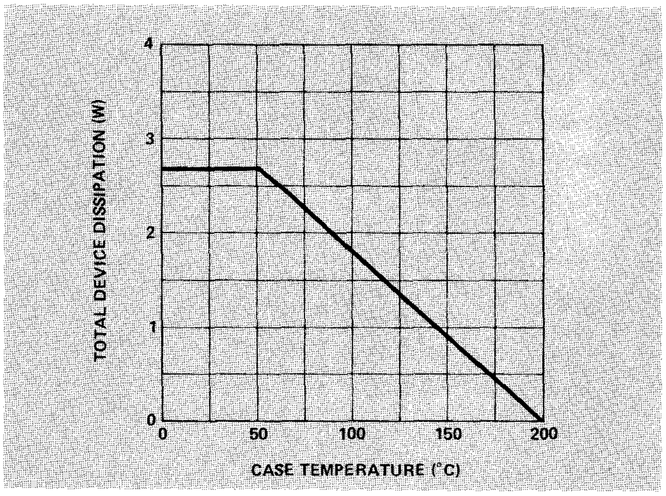


Figure 7. Maximum Power Dissipation Curve for θ_{jc} = 55°C/W, T_{jMAX} = 200°C.

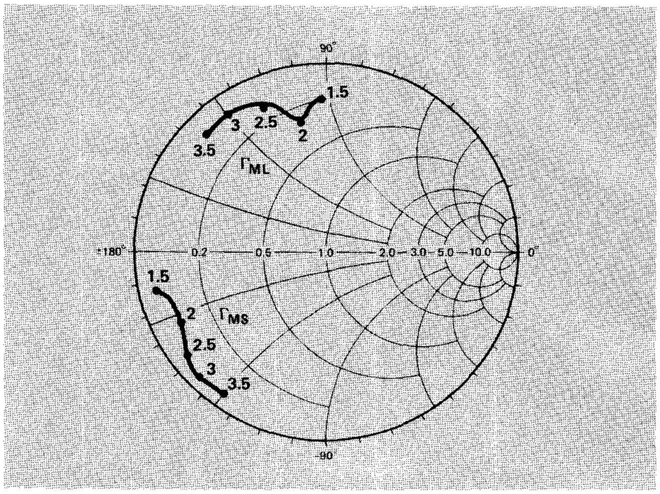


Figure 8. Typical Γ_{MS}, Γ_{ML} (calculated from the average S-parameters) in the 1.5 to 3.5GHz frequency range, at V_{CE} = 18V, I_C = 110mA.

Typical S-Parameters V_{CE} = 18V, I_C = 110mA

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (MHz)	**Mag.**	**Ang.**	**(dB)**	**Mag.**	**Ang.**	**(dB)**	**Mag.**	**Ang.**	**Mag.**	**Ang.**
100	0.48	-68	24.8	17.3	140	-31	0.03	62	0.86	-27
200	0.54	-109	22.6	13.5	127	-27	0.04	48	0.69	-46
300	0.59	-132	20.4	10.5	112	-26	0.05	40	0.55	-58
400	0.61	-146	18.5	8.43	102	-25	0.06	36	0.47	-66
500	0.63	-155	16.9	7.02	94	-24	0.06	34	0.41	-71
600	0.64	-162	15.5	5.98	88	-24	0.06	33	0.38	-76
700	0.65	-168	14.3	5.21	83	-24	0.07	33	0.35	-80
800	0.65	-172	13.3	4.62	78	-23	0.07	33	0.34	-84
900	0.65	-176	12.4	4.15	73	-23	0.07	33	0.32	-87
1000	0.64	179	11.5	3.70	69	-22	0.08	32	0.32	-90
1500	0.65	169	8.2	2.57	50	-20	0.10	31	0.32	-104
2000	0.65	151	6.0	1.99	33	-19	0.11	30	0.33	-118
2500	0.66	139	4.3	1.64	17	-17	0.14	25	0.39	-130
3000	0.65	128	2.9	1.40	2	-16	0.16	20	0.42	-140
3500	0.64	115	1.8	1.23	-13	-15	0.19	14	0.46	-152
4000	0.63	103	0.9	1.11	-27	-13	0.22	5	0.51	-161
4500	0.61	87	0.2	1.03	-41	-12	0.26	-2	0.53	-172
5000	0.59	72	-0.7	0.93	-54	-11	0.29	-12	0.57	179
5500	0.58	53	-1.6	0.84	-67	-10	0.34	-22	0.57	167
6000	0.58	38	-2.3	0.77	-79	-9	0.37	-31	0.60	155

HEWLETT PACKARD
COMPONENTS

LOW NOISE TRANSISTOR

2N6617 (NEW)
(HXTR-6101) 31-05
HXTR-6102 43-47

Features

LOW NOISE FIGURE
2.8dB at 4GHz, Typical (2N6617)
2.5dB at 4GHz, Typical (HXTR-6102)

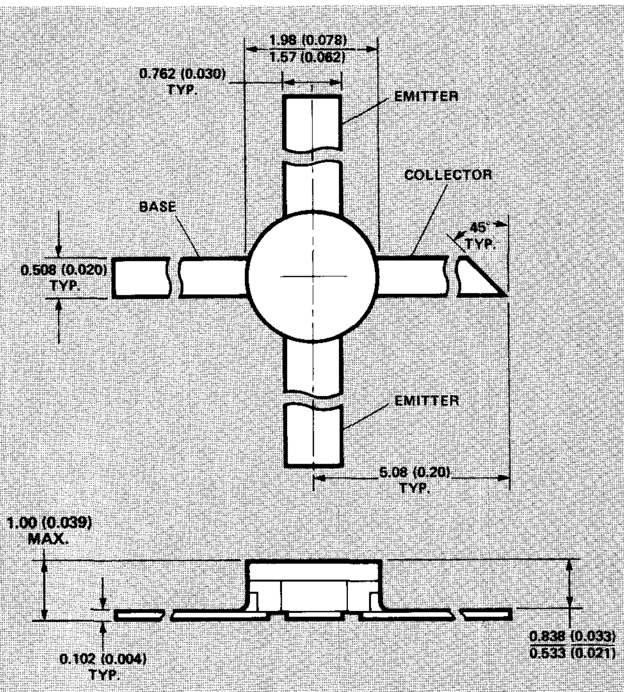
HIGH GAIN
9.0dB Typical Gain at NF Bias Conditions

RUGGED HERMETIC PACKAGE
Co-fired Metal/Ceramic Construction

Description

The 2N6617 (HXTR-6101) is an NPN bipolar transistor designed for minimum noise figure at 4 GHz. The device utilizes ion implantation techniques in its manufacture and the chip is also provided with scratch protection over its active area. The device is supplied in the HPAC-70GT, a rugged metal/ceramic hermetic package, and is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

The HXTR-6102 is a lower noise selection of the 2N6617.



OUTLINE HPAC-70GT

DIMENSIONS IN MILLIMETERS (INCHES).

Electrical Specifications at $T_{CASE} = 25°C$

Symbol	Parameters And Test Conditions	Test MIL-STD-750	Units	Min.	Typ.	Max.
BV_{CES}	Collector-Emitter Breakdown Voltage at $I_C = 100\mu A$	3001.1*	V	30		
I_{CEO}	Collector-Emitter Leakage Current at $V_{CE} = 10V$	3041.1	nA			500
I_{CBO}	Collector Cutoff Current at $V_{CB} = 10V$	3036.1	nA			100
h_{FE}	Forward Current Transfer Ratio at $V_{CE} = 10V$, $I_C = 4mA$	3076.1*	–	50	150	250
F_{MIN}	Minimum Noise Figure f = 4 GHz (2N6617) 1.5 GHz (2N6617) 4 GHz (HXTR-6102)	3246.1	dB		 2.8 1.6 2.5	 3.0 2.7
G_a	Associated Gain f = 4 GHz 1.5 GHz Bias Conditions for Above: $V_{CE} = 10V$, $I_C = 4mA$		 dB dB	 8.0	 9.0 15	
M_{MIN}**	Minimum Noise Measure (2N6617) $V_{CE} = 10V$, $I_C = mA$, f = 4GHz (HXTR-6102)				3.1 2.8	3.4 3.1

*300μs wide pulse measurement at ≤2% duty cycle.

**$M_{MIN} = 10 \text{ Log}\left(1 + \frac{F_{MIN} - 1}{1 - 1/G_a}\right)$ Noise measure (M_{MIN}) is the system noise figure of an infinite cascaded chain of identical amplifier stages. F_{MIN} and G_a specified as power ratios.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage[2]	25V
V_{CEO}	Collector to Emitter Voltage[2]	16V
V_{EBO}	Emitter to Base Voltage[2]	1.0V
I_C	DC Collector Current[2]	10 mA
P_T	Total Device Dissipation[3]	150 mW
T_J	Junction Temperature	200° C
T_{STG}	Storage Temperature	-65° C to +200° C

Notes:

1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device mean time between failure (MTBF) to below the design goal of 1 x 10^7 hours at T_J = 175° C (assumed Activation Energy = 1.5 eV). Corresponds to maximum rating for 2N6617.
2. T_{CASE} = 25° C.
3. Derate at 4 mW/° C, $T_C \geq 163°$ C.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	35V
V_{CEO}	Collector to Emitter Voltage	20V
V_{EBO}	Emitter to Base Voltage	1.5V
I_C	DC Collector Current	20 mA
P_T	Total Device Dissipation	300 mW
T_J	Junction Temperature	300° C
$T_{STG(MAX)}$	Maximum Storage Temperature	250° C
—	Lead Temperature (Soldering 10 seconds each lead)	+250° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

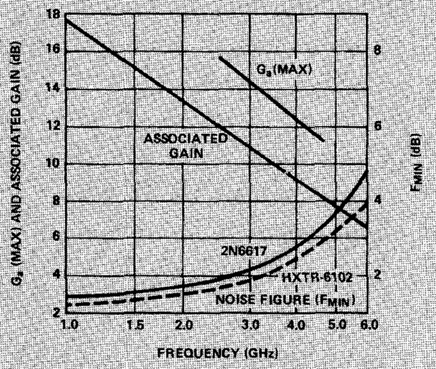


Figure 1. Typical $G_{a(MAX)}$, F_{MIN} and Associated Gain vs. Frequency at V_{CE} = 10V, I_C = 4 mA.

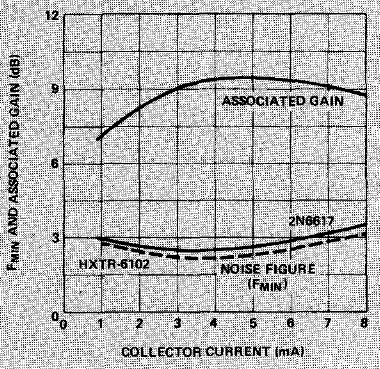


Figure 2. Typical F_{MIN} and Associated Gain vs. I_C at 4 GHz for V_{CE} = 10V (Tuned for F_{MIN}).

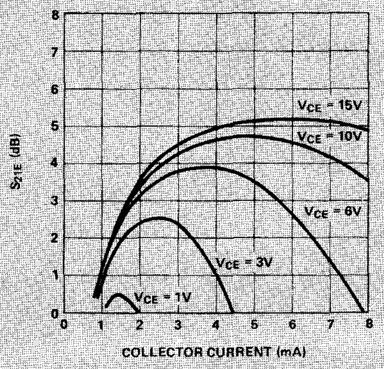


Figure 3. Typical $|S_{21E}|^2$ vs. Bias at 4 GHz, for the HXTR-6101/6102.

Typical S-Parameters V_{CE} = 10V, I_C = 4mA

	S_{11}		S_{21}		S_{12}		S_{22}	
Freq. (MHz)	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.	Mag.	Ang.
100	0.917	-11	7.149	168	0.007	79	0.991	-4
500	0.782	-54	6.277	135	0.026	54	0.901	-18
1000	0.635	-98	5.037	113	0.037	33	0.787	-30
1500	0.598	-127	3.881	87	0.039	28	0.763	-35
2000	0.589	-149	3.148	71	0.042	26	0.754	-43
2500	0.570	-163	2.646	59	0.042	25	0.760	-50
3000	0.575	-173	2.209	48	0.043	25	0.773	-58
3500	0.560	180	1.948	37	0.046	25	0.795	-64
4000	0.548	173	1.665	29	0.049	24	0.816	-71
4500	0.530	167	1.450	20	0.053	24	0.850	-76
5000	0.518	160	1.346	11	0.058	23	0.860	-84
5500	0.500	152	1.210	1	0.060	22	0.880	-92
6000	0.489	146	1.076	-7	0.063	20	0.877	-99
7000	0.491	132	0.897	-23	0.069	15	0.872	-108

Typical Noise Parameters

Freq. (MHz)	Γ_o (Mag./Ang.)	R_N (Ohms)	F_{MIN} (dB) HXTR-6102
1000	.480/23°	23.31	1.45
1500	.450/61°	15.57	1.49
2000	.410/88°	15.73	1.61
3000	.425/121°	10.72	2.06
4000	.475/166°	3.50	2.60
5000	.530/-164°	2.81	3.34
6000	.520/-131°	7.23	4.21

Figure 4. Typical Noise Parameters for the 2N6617/HXTR-6102 at V_{CE} = 10V, I_C = 4 mA.

Low Power Bias Performance

Bias						
V_{CE} V	I_C mA	F_{MIN} dB	G_a dB	R_N Ohms	Γ_o Mag./Ang.	Γ_L Mag./Ang.
3	0.25	2.25	8.5	60.5	.805/31°	.788/25°
3	0.50	1.87	12.7	25.5	.713/38°	.779/29°
3	1.00	1.55	15.7	13.9	.571/39°	.774/29°

Figure 5. Noise Parameters at 1 GHz for the 2N6617 (HXTR-6101)

BIAS		Frequency							
		1000 MHz		1500 MHz		2000 MHz		3000MHz	
V_{CE} V	I_C mA	F_{MIN} dB	G_a dB	F_{MIN} dB	G_a dB	F_{MIN} dB	G_a dB	F_{MIN} dB	G_a dB
3	0.25	2.25	8.5	2.67	5.0	2.83	4.7	3.88	4.1
3	0.50	1.87	12.7	2.06	9.9	2.23	7.9	2.93	6.4
3	1.0	1.55	15.7	1.73	11.7	1.79	10.2	2.38	8.1

Figure 6. Noise Performance vs. Frequency and Bias for the 2N6617 (HXTR-6101)

TYPICAL S-PARAMETERS V_{CE} = 3V, I_C = 0.25mA

Freq. (MHz)	S_{11}		S_{21}			S_{12}			S_{22}		K
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang	
500	.988	-22	-6.9	.451	152	-28.2	.039	72	.993	-12	.220
1000	.956	-42	-7.2	.438	127	-23.1	.070	55	.975	-22	.464
1500	.929	-65	-7.5	.423	106	-20.6	.093	38	.956	-33	.586
2000	.910	-81	-7.7	.412	89	-19.7	.104	27	.945	-42	.679
3000	.888	-112	-8.1	.394	56	-19.3	.108	6	.938	-59	.821

V_{CE} = 3V, I_C = 0.50mA

Freq. (MHz)	S_{11}		S_{21}			S_{12}			S_{22}		K
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.	
500	.976	-24	-0.8	.991	152	-28.4	.038	70	.986	-13	.220
1000	.929	-47	-1.3	.863	128	-23.6	.066	52	.955	-24	.423
1500	.887	-72	-2.0	.792	107	-21.4	.085	35	.920	-34	.583
2000	.856	-89	-2.5	.747	91	-20.6	.093	24	.906	-43	.682
3000	.818	-121	-3.3	.688	60	-20.1	.099	7	.889	-60	.816

V_{CE} = 3V, I_C = 1.0mA

Freq. (MHz)	S_{11}		S_{21}			S_{12}			S_{22}		K
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.	
500	.952	-25	4.4	1.67	149	-28.6	.037	66	.972	-14	.328
1000	.884	-54	3.7	1.54	125	-24.3	.061	47	.919	-25	.492
1500	.821	-82	2.7	1.36	104	-23.1	.070	31	.873	-36	.664
2000	.775	-102	1.9	1.25	88	-22.6	.074	23	.854	-43	.793
3000	.738	-133	.77	1.09	59	-22.1	.079	10	.842	-59	.908

HEWLETT hp PACKARD
COMPONENTS

LOW NOISE TRANSISTOR

2N6618 NEW
(HXTR-6103)

T-29-19

Features

GUARANTEED LOW NOISE FIGURE
2.2 dB Max. at 2 GHz, 1.8 dB Typical

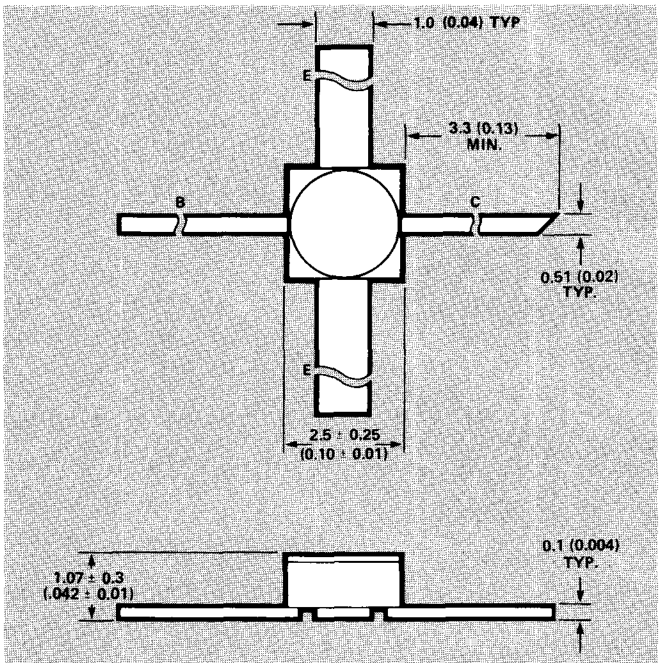
HIGH GAIN
12.0 dB Typical Gain at NF Bias Conditions

RUGGED HERMETIC PACKAGE
Co-fired Metal/Ceramic Construction

Description

The 2N6618 (HXTR-6103) is an NPN bipolar transistor designed for minimum noise figure at 2 GHz. The device utilizes ion implantation techniques and Ti/Pt/Au metallization in its manufacture. The chip is provided with scratch protection over its active area.

These devices are supplied in the HPAC-100, a rugged metal/ceramic hermetic package, and are capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.



DIMENSIONS IN MILLIMETERS (INCHES).

HPAC-100 Package Outline

Electrical Specifications at $T_{CASE} = 25°C$

Symbol	Parameters And Test Conditions	Test MIL-STD-750	Units	Min.	Typ.	Max.
BV_{CES}	Collector Emitter Breakdown Voltage at $I_C = 100\mu A$	3011.1*	V	30		
I_{CEO}	Collector Emitter Leakage Current at $V_{CE} = 10V$	3041.1	nA			500
I_{CBO}	Collector Cut Off Current at $V_{CB} = 10V$	3036.1	nA			100
h_{FE}	Forward Current Transfer Ratio at $V_{CE}=10V, I_C=3mA$	3076.1*	–	50	150	250
F_{MIN}	Minimum Noise Figure at 2 GHz	3246.1	dB		1.8	2.2
G_a	Associated Gain at 2 GHz Bias for above: $V_{CE} = 10V$, $I_C = 3$ mA		dB	11.0	12.0	
M_{MIN}**	Minimum Noise Measure $V_{CE} = 10V$, $I_C = 3$ mA, f= 2 GHz				1.90	2.35

*300 μs wide pulse measurement at ≤ 2% duty cycle.

** $M_{MIN} = 10 \text{ Log} \left(1 + \frac{F_{MIN} - 1}{1 - 1/G_a}\right)$ Noise measure (M_{MIN}) is the system noise figure of an infinite cascaded chain of identical amplifier stages. F_{MIN} and G_a specified as power ratios.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage[2]	25V
V_{CEO}	Collector to Emitter Voltage[2]	16V
V_{EBO}	Emitter to Base Voltage[2]	1.0V
I_C	DC Collector Current[2]	10 mA
P_T	Total Device Dissipation[3]	150 mW
T_J	Junction Temperature	200° C
T_{STG}	Storage Temperature	-65° C to +200° C

Notes:

1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device mean time between failure (MTBF) to below the design goal of 1 x 10^7 hours at T_J = 175° C (assumed Activation Energy = 1.5 eV). Corresponds to maximum rating for 2N6618.
2. T_{CASE} = 25° C.
3. Derate at 3.3 mW/° C, $T_C \geq$ 155° C.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	35V
V_{CEO}	Collector to Emitter Voltage	20V
V_{EBO}	Emitter to Base Voltage	1.5V
I_C	DC Collector Current	20 mA
P_T	Total Device Dissipation	300 mW
T_J	Junction Temperature	300° C
$T_{STG(MAX)}$	Maximum Storage Temperature	250° C
—	Lead Temperature (Soldering 10 seconds each lead)	+250° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

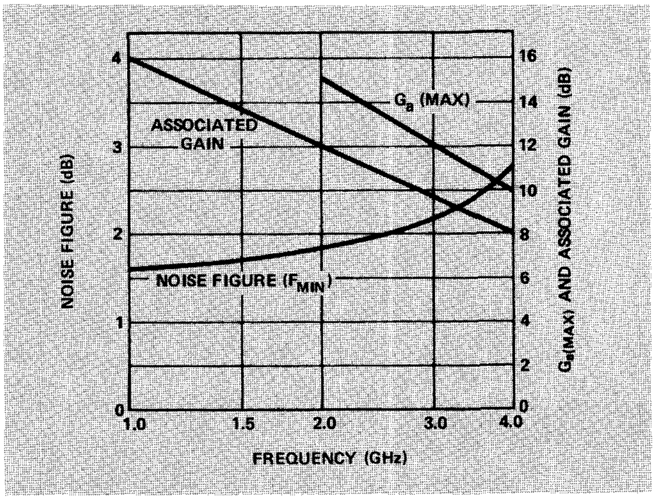


Figure 1. Typical $G_{a(max)}$, F_{MIN} and Associated Gain vs. Frequency at V_{CE} = 10V, I_C = 3 mA.

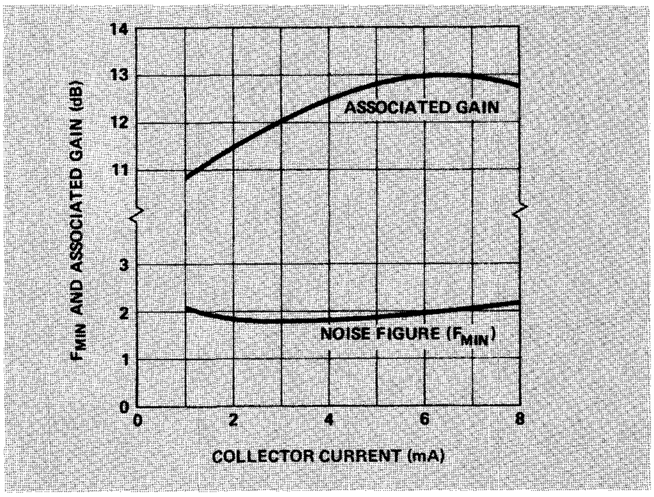


Figure 2. Typical F_{MIN} and Associated Gain vs. Collector Current at 2 GHz for V_{CE} = 10V (Tuned for F_{MIN}).

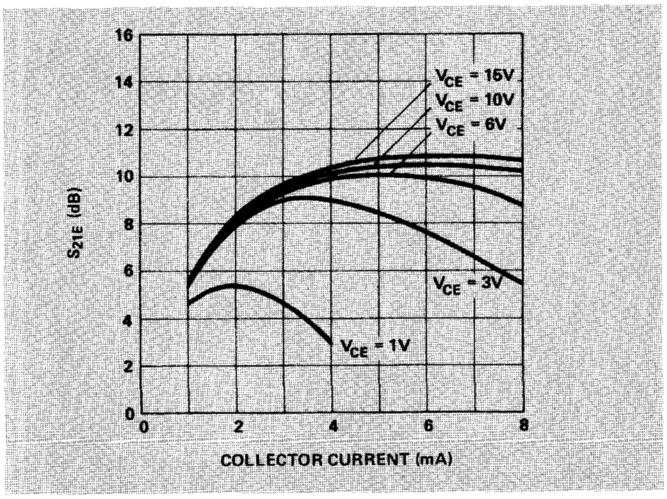


Figure 3. Typical S_{21E} vs. Bias at 2 GHz.

Typical Noise Parameters

Freq. (MHz)	Γ_o (Mag./Ang.)	R_N (Ohms)	F_{MIN} (dB)
1000	.465/36°	25.09	1.55
1500	.369/67°	22.47	1.65
2000	.323/94°	23.31	1.80

Figure 4. Typical Noise Parameters at V_{CE} = 10V, I_C = 3 mA.

Typical S- Parameters V_{CE} = 10V, I_C = 3 mA

Freq. (MHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	0.93	-11.5	16.2	6.46	168.0	-42.0	0.01	77.0	0.99	-4.0
200	0.89	-23.0	17.1	7.13	158.0	-37.0	0.01	77.0	0.97	-8.0
300	0.86	-34.0	16.4	6.58	149.0	-34.0	0.02	66.0	0.94	-12.0
400	0.83	-44.0	15.9	6.26	142.0	-32.0	0.03	60.0	0.92	-16.0
500	0.79	-54.0	15.6	6.02	135.0	-30.0	0.03	55.0	0.89	-19.0
600	0.75	-65.0	15.4	5.91	128.0	-29.0	0.04	51.0	0.87	-21.0
700	0.71	-73.0	15.0	5.62	121.0	-29.0	0.04	48.0	0.85	-24.0
800	0.68	-81.0	14.4	5.25	116.0	-28.0	0.04	45.0	0.84	-25.0
900	0.65	-91.0	14.0	4.99	111.0	-28.0	0.04	43.0	0.83	-27.0
1000	0.62	-97.0	13.5	4.72	106.0	-27.0	0.04	41.0	0.81	-28.0
1500	0.52	-129.0	11.4	3.71	84.0	-27.0	0.05	32.0	0.74	-35.0
2000	0.50	-151.0	9.3	2.93	69.0	-26.0	0.05	31.0	0.72	-43.0
2500	0.50	-169.0	7.8	2.45	55.0	-26.0	0.05	31.0	0.69	-51.0
3000	0.49	175.0	6.5	2.12	42.0	-26.0	0.06	33.0	0.68	-57.0
3500	0.54	165.0	5.4	1.87	29.0	-25.0	0.06	35.0	0.65	-68.0
4000	0.52	156.0	4.5	1.67	19.0	-24.0	0.06	37.0	0.68	-76.0
5000	0.53	140.0	2.6	1.35	-3.0	-23.0	0.08	35.0	0.71	-96.0
6000	0.48	120.0	0.9	1.11	-22.0	-21.0	0.09	34.0	0.73	-112.0

HEWLETT PACKARD
COMPONENTS

LOW NOISE TRANSISTOR

HXTR-6104

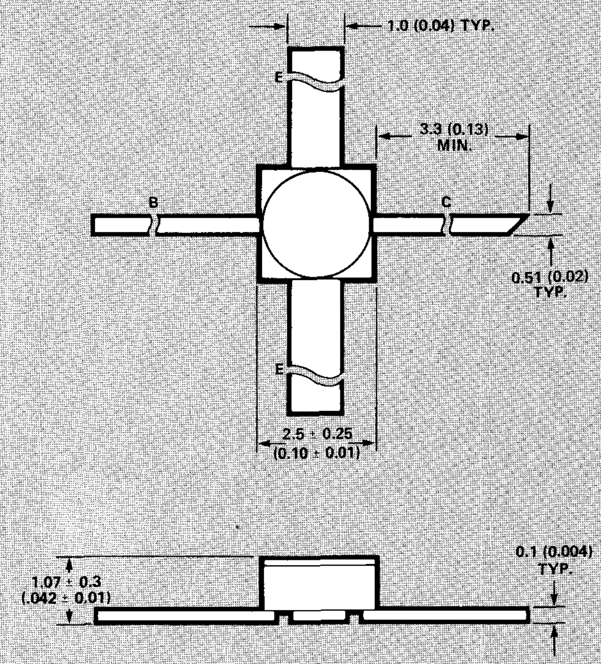
43-47

Features

GUARANTEED LOW NOISE FIGURE
1.6 dB Max. at 1.5 GHz

HIGH GAIN
14.0 dB Typical Gain at NF Bias Conditions

RUGGED HERMETIC PACKAGE
Co-fired Metal/Ceramic Construction



DIMENSIONS IN MILLIMETERS (INCHES).

HPAC-100 Package Outline

Description

The HXTR-6104 is an NPN bipolar transistor designed for minimum noise figure at 1.5 GHz. The device utilizes ion implantation techniques and Ti/Pt/Au metallization in its manufacture. The chip is provided with scratch protection over its active area.

The HXTR-6104 is supplied in the HPAC-100, a rugged metal/ceramic hermetic package, and is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

Electrical Specifications at $T_{CASE} = 25°C$

Symbol	Parameters And Test Conditions	Test MIL-STD-750	Units	Min.	Typ.	Max.
BV_{CES}	Collector Emitter Breakdown Voltage at $I_C = 100\mu A$	3011.1*	V	30		
I_{CEO}	Collector Emitter Leakage Current at $V_{CE} = 10V$	3041.1	nA			500
I_{CBO}	Collector Cut Off Current at $V_{CB} = 10V$	3036.1	nA			100
h_{FE}	Forward Current Transfer Ratio at $V_{CE}=10V, I_C=3mA$	3076.1*	–	50	150	250
F_{MIN}	Minimum Noise Figure f = 1.5 GHz	3246.1	dB		1.4	1.6
G_a	Associated Gain f = 1.5 GHz Bias for above: $V_{CE} = 10V$, $I_C = 3$ mA		dB	13.0	14.0	
M_{MIN}**	Minimum Noise Measure $V_{CE} = 10V$, $I_C = 3$ mA, f = 1.5 GHz				1.45	1.67

*300 μs wide pulse measurement at ≤ 2% duty cycle.

**$M_{MIN} = 10 \text{ Log} \left(1 + \dfrac{F_{MIN} - 1}{1 - 1/G_a}\right)$ Noise measure (M_{MIN}) is the system noise figure of an infinite cascaded chain of identical amplifier stages. F_{MIN} and G_a specified as power ratios.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage[2]	25V
V_{CEO}	Collector to Emitter Voltage[2]	16V
V_{EBO}	Emitter to Base Voltage[2]	1.0V
I_C	DC Collector Current[2]	10 mA
P_T	Total Device Dissipation[3]	150 mW
T_J	Junction Temperature	200° C
T_{STG}	Storage Temperature	-65° C to +200° C

Notes:

1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device mean time between failure (MTBF) to below the design goal of 1 x 10^7 hours at $T_J = 175°C$ (assumed Activation Energy = 1.5 eV).
2. $T_{CASE} = 25°C$.
3. Derate at 3.3 mW/° C, $T_C \geq 155°C$.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	35V
V_{CEO}	Collector to Emitter Voltage	20V
V_{EBO}	Emitter to Base Voltage	1.5V
I_C	DC Collector Current	20 mA
P_T	Total Device Dissipation	300 mW
T_J	Junction Temperature	300° C
$T_{STG(MAX)}$	Maximum Storage Temperature	250° C
—	Lead Temperature (Soldering 10 seconds each lead)	+250° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

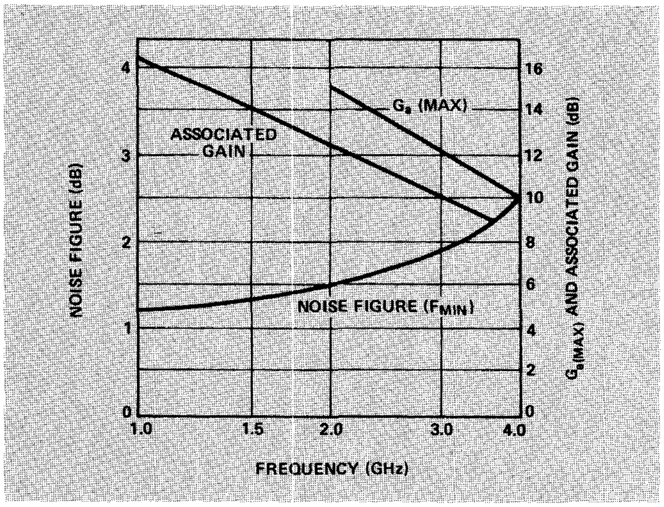


Figure 1. Typical $G_{a(max)}$, F_{MIN} and Associated Gain vs. Frequency at $V_{CE} = 10V$, $I_C = 3$ mA.

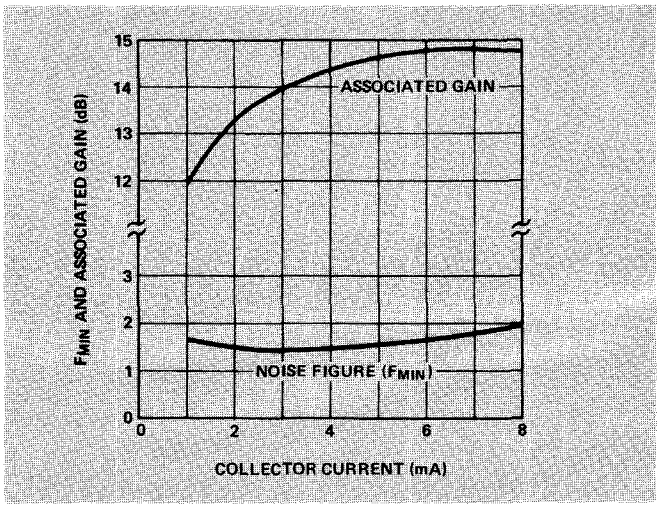


Figure 2. Typical F_{MIN} and Associated Gain vs. I_C at 1.5 GHz for $V_{CE} = 10V$ (Tuned for F_{MIN}).

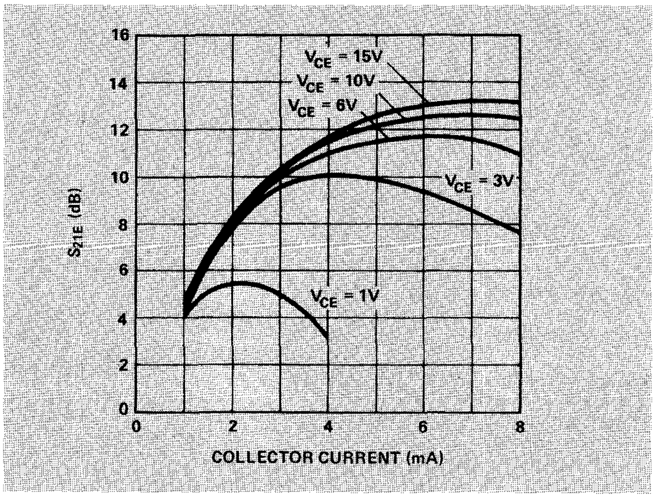


Figure 3. Typical S_{21E} vs. Bias at 1.5 GHz.

HEWLETT *hp* PACKARD
COMPONENTS

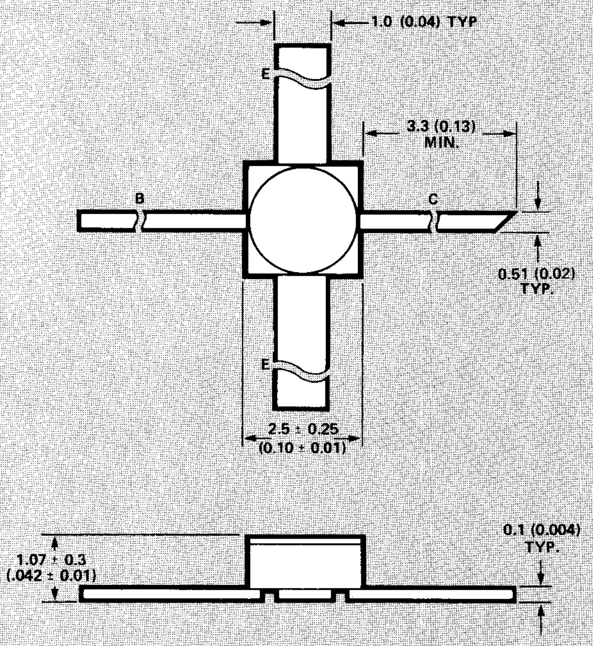
LOW NOISE TRANSISTOR

HXTR-6105

T 17-39

Features

LOW NOISE FIGURE
  4.2 dB Maximum at 4 GHz Guaranteed
HIGH GAIN
  9 dB Typ. at NF Bias Conditions
WIDE DYNAMIC RANGE
RUGGED HERMETIC PACKAGE
  Co-fired Metal/Ceramic Construction



DIMENSIONS IN MILLIMETERS (INCHES).

HPAC-100 Package Outline

Description

The HXTR-6105 is an NPN bipolar transistor designed for low noise at 4 GHz with high output dynamic range. This transistor also features high output power and high gain at the NF bias and tuning conditions.

The device utilizes ion implantation techniques and Ti/Pt/Au metallization in its manufacture,and the chip is provided with a dielectric scratch protection over its active area.

The HXTR-6105 is supplied in the HPAC-100, a rugged metal/ceramic hermetic package, and is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

Electrical Specifications at $T_{CASE} = 25°C$

Symbol	Parameters and Test Conditions	MIL-STD-750 Test Method	Units	Min.	Typ.	Max.
BV_{CES}	Collector-Emitter Breakdown Voltage $I_C = 100\mu A$	3011.1 *	V	30		
I_{CEO}	Collector-Emitter Leakage Current at $V_{CE} = 15V$	3041.1	nA			500
I_{CBO}	Collector Cut Off Current at $V_{CB} = 15V$	3036.1	nA			100
h_{FE}	Forward Current Transfer Ratio at $V_{CE} = 15V$, $I_C = 15mA$	3076.1*	—	50	120	220
F_{MIN}	Minimum Noise Figure f = 4 GHz = 1.5 GHz	3246.1	dB		3.8 2.2	4.2
G_a	Associated Gain f = 4 GHz = 1.5 GHz		dB	8.0	9.0 15.0	
P_{1dB}	Associated Power Output at 1dB Compression at 4 GHz $V_{CE} = 15V$, $I_C = 15mA$		dBm		14	
M_{MIN}**	Minimum Noise Measure $V_{CE} = 15V$, $I_C = 15mA$, f = 4 GHz		dB		4.2	4.7

*300 μs wide pulse measurement at ≤ 2% duty cycle.

**$M_{MIN} = 10 \text{ Log} \left(1 + \frac{F_{MIN} - 1}{1 - 1/G_a}\right)$ Noise measure (M_{MIN}) is the system noise figure of an infinite cascaded chain of identical amplifier stages. F_{MIN} and G_a specified as power ratios.

Typical Noise Parameters

Freq. (MHz)	Γ_o (Mag./Ang.)	R_N (Ohms)	F_{MIN} (dB)
1000	.465/36°	25.09	1.20
1500	.369/67°	22.47	1.30
2000	.323/94°	23.31	1.50

Figure 4. Typical Noise Parameters at V_{CE} = 10V, I_C = 3 mA.

Typical S-Parameters V_{CE} = 10V, I_C = 3 mA

Freq. (MHz)	S_{11} Mag.	S_{11} Ang.	S_{21} (dB)	S_{21} Mag.	S_{21} Ang.	S_{12} (dB)	S_{12} Mag.	S_{12} Ang.	S_{22} Mag.	S_{22} Ang.
100	0.93	-11.5	16.2	6.46	168.0	-42.0	0.01	77.0	0.99	-4.0
200	0.89	-23.0	17.1	7.13	158.0	-37.0	0.01	77.0	0.97	-8.0
300	0.86	-34.0	16.4	6.58	149.0	-34.0	0.02	66.0	0.94	-12.0
400	0.83	-44.0	15.9	6.26	142.0	-32.0	0.03	60.0	0.92	-16.0
500	0.79	-54.0	15.6	6.02	135.0	-30.0	0.03	55.0	0.89	-19.0
600	0.75	-65.0	15.4	5.91	128.0	-29.0	0.04	51.0	0.87	-21.0
700	0.71	-73.0	15.0	5.62	121.0	-29.0	0.04	48.0	0.85	-24.0
800	0.68	-81.0	14.4	5.25	116.0	-28.0	0.04	45.0	0.84	-25.0
900	0.65	-91.0	14.0	4.99	111.0	-28.0	0.04	43.0	0.83	-27.0
1000	0.62	-97.0	13.5	4.72	106.0	-27.0	0.04	41.0	0.81	-28.0
1500	0.52	-129.0	11.4	3.71	84.0	-27.0	0.05	32.0	0.74	-35.0
2000	0.50	-151.0	9.3	2.93	69.0	-26.0	0.05	31.0	0.72	-43.0
2500	0.50	-169.0	7.8	2.45	55.0	-26.0	0.05	31.0	0.69	-51.0
3000	0.49	175.0	6.5	2.12	42.0	-26.0	0.06	33.0	0.68	-57.0
3500	0.54	165.0	5.4	1.87	29.0	-25.0	0.06	35.0	0.65	-68.0
4000	0.52	156.0	4.5	1.67	19.0	-24.0	0.06	37.0	0.68	-76.0
5000	0.53	140.0	2.6	1.35	-3.0	-23.0	0.08	35.0	0.71	-96.0
6000	0.48	120.0	0.9	1.11	-22.0	-21.0	0.09	34.0	0.73	-112.0

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage[2]	25V
V_{CEO}	Collector to Emitter Voltage[2]	16V
V_{EBO}	Emitter to Base Voltage[2]	1.0V
I_C	DC Collector Current[2]	35 mA
P_T	Total Device Dissipation[3]	450 mW
T_J	Junction Temperature	200° C
T_{STG}	Storage Temperature	-65° C to +200° C

Notes:

1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device mean time between failure (MTBF) to below the design goal of 1 x 10^7 hours at T_J = 175° C (assumed Activation Energy = 1.5 eV).
2. T_{CASE} = 25° C.
3. Derate at 4.8 mW/° C, $T_C \geq 106°$ C.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	30V
V_{CEO}	Collector to Emitter Voltage	20V
V_{EBO}	Emitter to Base Voltage	1.5V
I_C	DC Collector Current	70 mA
P_T	Total Device Dissipation	900 mW
T_J	Junction Temperature	300° C
$T_{STG(MAX)}$	Maximum Storage Temperature	250° C
—	Lead Temperature (Soldering 10 seconds each lead)	+250° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

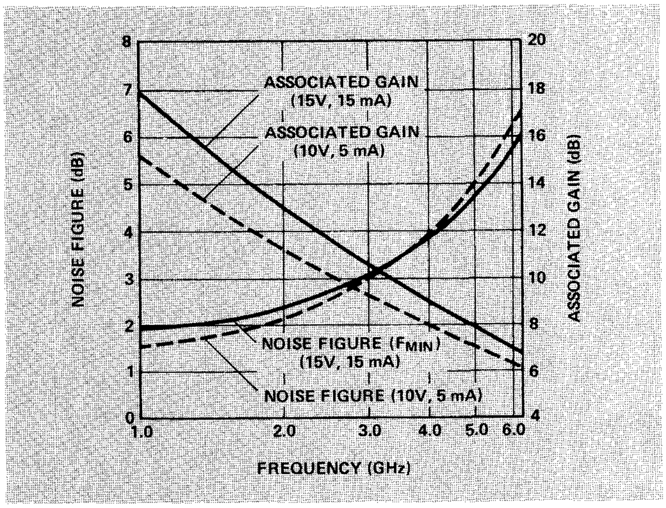


Figure 1. Typical F_{MIN} and Associated Gain vs. Frequency.

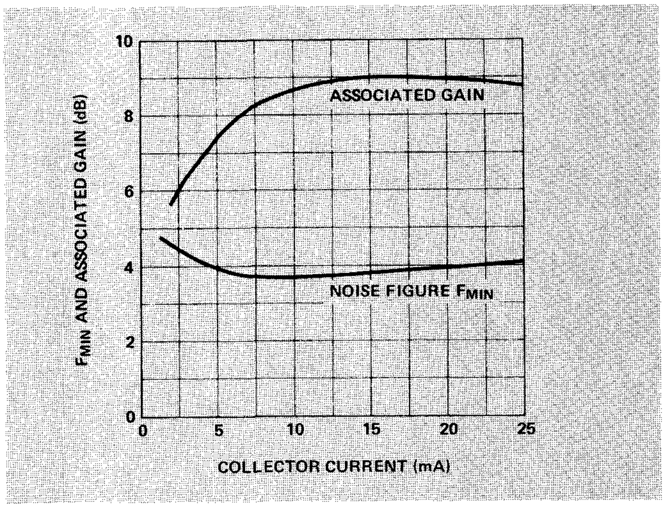


Figure 2. Typical F_{MIN} and Associated Gain vs. I_C at 4 GHz for V_{CE}=15V (Tuned for F_{MIN}).

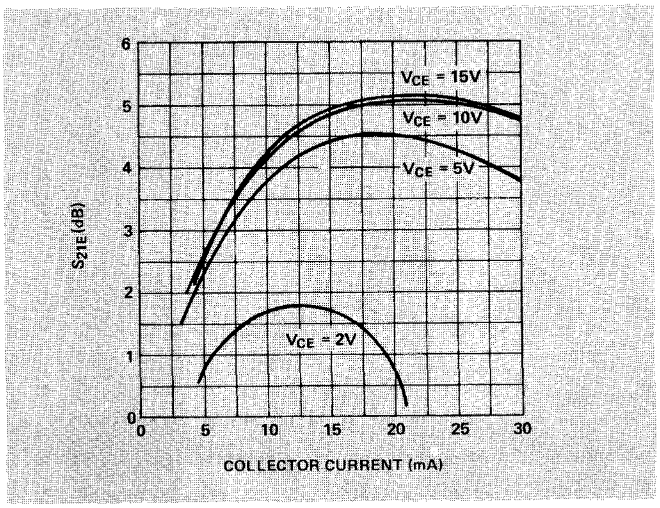


Figure 3. Typical S_{21E} vs. Current at 4 GHz.

Typical Noise Parameters

Freq. (MHz)	Γ_o (Mag./Ang.)	R_N (Ohms)	F_{MIN} (dB)
1000	.238/123°	6.81	1.80
1500	.385/142°	5.33	2.15
2000	.429/173°	5.04	2.25
3000	.541/-158°	6.54	3.01
4000	.628/-135°	15.54	3.81
5000	.624/-107°	60.14	4.75

Figure 4. Typical Noise Parameters at V_{CE}=15V, I_C=15mA.

Typical S-Parameters V_{CE} = 15V, I_C = 15mA

Freq. (MHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	0.66	-52	29.0	28.3	152	-39.2	0.01	69	0.90	-16
500	0.59	-139	22.0	12.5	101	-37.7	0.03	41	0.55	-33
1000	0.59	-169	16.5	6.71	80	-29.6	0.03	45	0.47	-37
1500	0.59	177	13.1	4.54	65	-27.5	0.04	49	0.47	-41
2000	0.61	165	10.8	3.48	53	-25.5	0.05	50	0.47	-50
2500	0.60	159	8.8	2.75	43	-24.0	0.06	51	0.49	-61
3000	0.62	148	7.2	2.28	32	-22.7	0.07	52	0.50	-68
3500	0.62	141	5.7	1.93	21	-21.4	0.09	49	0.54	-80
4000	0.62	132	4.6	1.70	10	-20.0	0.10	47	0.57	-85
4500	0.60	126	3.5	1.50	0.0	-19.0	0.11	45	0.60	-94
5000	0.60	118	2.6	1.35	-9	-17.2	0.14	42	0.65	-102
5500	0.61	112	1.8	1.23	-20	-16.8	0.14	35	0.66	-112
6000	0.62	104	0.9	1.11	-29	-16.1	0.16	31	0.67	-122

HEWLETT hp PACKARD
COMPONENTS

NEW

LOW NOISE TRANSISTOR

HXTR-6106

± 20-49

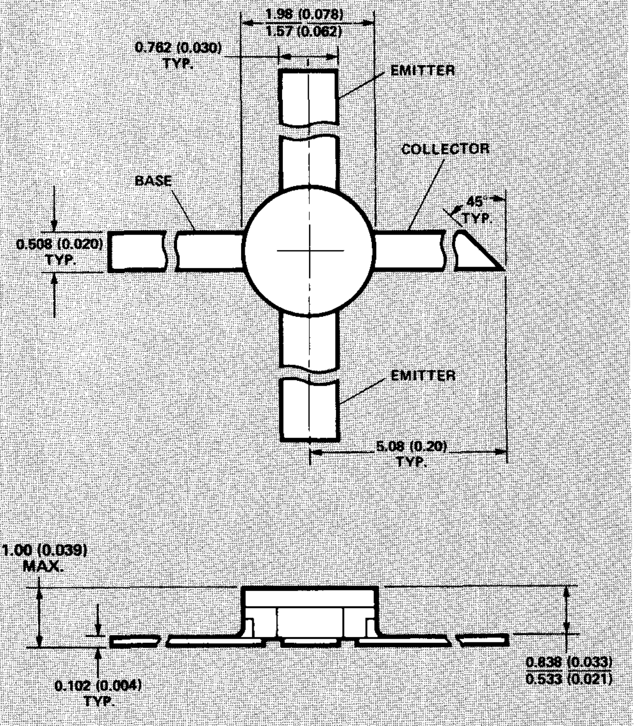
Features

GUARANTEED LOW NOISE FIGURE
2.7 dB at 2 GHz Max., 2.5 dB Typical
3.8 dB at 4 GHz Typical

HIGH ASSOCIATED GAIN
11.5 dB Typical at 2 GHz

WIDE DYNAMIC RANGE

RUGGED HERMETIC PACKAGE
Co-fired Metal/Ceramic Construction



OUTLINE HPAC-70GT

DIMENSIONS IN MILLIMETERS (INCHES).

Description

The HXTR-6106 is an NPN bipolar transistor designed for low noise up to 6 GHz with wide dynamic range. This transistor also features high output power and high gain at the NF bias and tuning conditions.

The device utilizes ion implantation techniques and Ti/Pt/Au metallization in its manufacture, and the chip is provided with a dielectric scratch protection over its active area.

The HXTR-6106 is supplied in the HPAC-70GT, a rugged metal/ceramic hermetic package, and is capable of meeting the environmental requirements of MIL-S-19500 and the test requirements of MIL-STD-750/883.

Electrical Specifications at $T_{CASE} = 25°C$

Symbol	Parameters and Test Conditions		MIL-STD-750 Test Method	Units	Min.	Typ.	Max.
BV_{CES}	Collector-Emitter Breakdown Voltage at $I_C = 100\mu A$		3011.1*	V	30		
I_{CEO}	Collector-Emitter Leakage Current at $V_{CE} = 15V$		3041.1	nA			500
I_{CBO}	Collector Cutoff Current at $V_{CB} = 15V$		3036.1	nA			100
h_{FE}	Forward Current Transfer Ratio at $V_{CE} = 15V$, $I_C = 15mA$		3076.1*	—	50	120	220
F_{MIN}	Minimum Noise Figure	f=2 GHz	3246.1	dB		2.5	2.7
		4 GHz				3.8	
G_a	Associated Gain	f=2 GHz			10.0	11.5	
		4 GHz				9.0	
P_{1dB}	Associated Power Output at 1dB Compression $V_{CE} = 15V$, $I_C = 10mA$	f=2 GHz		dBm		15	
M_{MIN}	Minimum Noise Measure $V_{CE} = 15V$, $I_C = 10mA$, f = 2GHz			dB		2.6	3.0

*300μs wide pulse measurement ≤2% duty cycle.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage[2]	25V
V_{CEO}	Collector to Emitter Voltage[2]	16V
V_{EBO}	Emitter to Base Voltage[2]	1.0V
I_C	DC Collector Current[2]	35 mA
P_T	Total Device Dissipation[3]	450 mW
T_J	Junction Temperature	200° C
T_{STG}	Storage Temperature	-65° C to +200° C

Notes:

1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device mean time between failure (MTBF) to below the design goal of 1 x 10^7 hours at $T_J = 175°C$ (assumed Activation Energy = 1.5 eV).
2. $T_{CASE} = 25°C$.
3. Derate at 5.4 mW/°C, $T_C \geq 117°C$.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	30V
V_{CEO}	Collector to Emitter Voltage	20V
V_{EBO}	Emitter to Base Voltage	1.5V
I_C	DC Collector Current	70 mA
P_T	Total Device Dissipation	900 mW
T_J	Junction Temperature	300° C
$T_{STG(MAX)}$	Maximum Storage Temperature	250° C
—	Lead Temperature (Soldering 10 seconds each lead)	+250° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

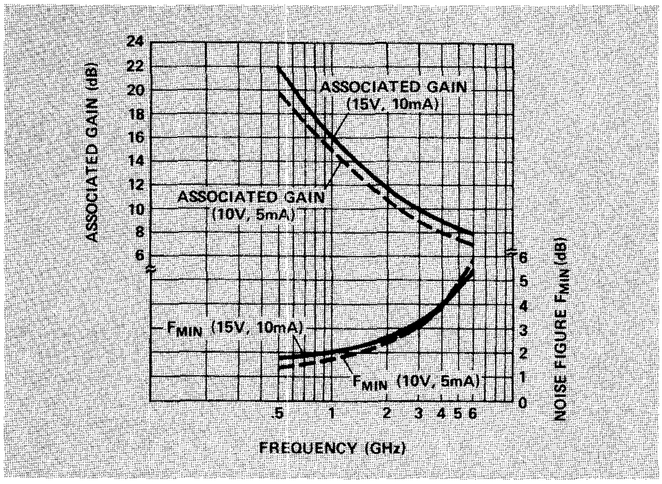


Figure 1. Typical Noise Figure (F_{MIN}) and Associated Gain vs. Frequency.

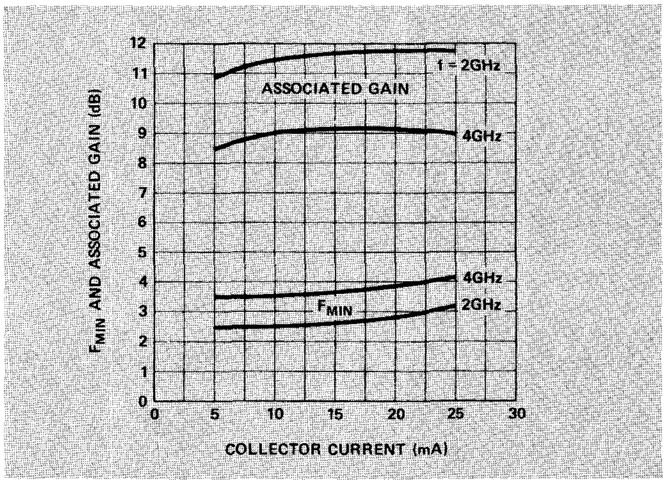


Figure 2. Typical Noise Figure (F_{MIN}) and Associated Gain vs. Current at 2 GHz and 4 GHz at $V_{CE} = 15V$ (Tuned for F_{MIN}).

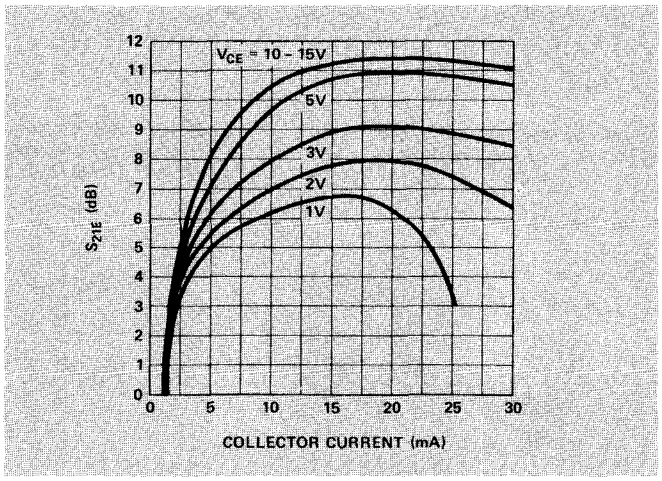


Figure 3. Typical S_{21E} vs. Current at 2 GHz.

Typical S-Parameters V_{CE} = 15V, I_C = 10mA

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (MHz)	**Mag.**	**Ang.**	**(dB)**	**Mag.**	**Ang.**	**(dB)**	**Mag.**	**Ang.**	**Mag.**	**Ang.**
100	0.77	-36	26.4	20.8	157	-38.4	0.012	67	0.93	-12
200	0.72	-70	25.6	19.0	139	-34.0	0.020	55	0.82	-21
300	0.70	-95	24.1	16.0	125	-32.0	0.025	46	0.71	-26
400	0.70	-113	22.7	13.6	115	-31.0	0.028	41	0.64	-29
500	0.69	-126	21.3	11.6	108	-30.5	0.030	37	0.59	-31
600	0.68	-136	20.1	10.1	102	-29.9	0.032	36	0.56	-33
700	0.67	-143	19.0	8.9	97	-29.6	0.033	35	0.54	-34
800	0.66	-149	18.0	7.9	93	-29.4	0.034	35	0.54	-35
900	0.66	-154	17.0	7.0	91	-29.1	0.035	34	0.53	-36
1000	0.66	-159	16.1	6.4	86	-28.9	0.036	35	0.53	-36
1500	0.68	-174	12.8	4.3	72	-27.0	0.040	36	0.48	-41
2000	0.66	177	10.5	3.3	61	-27.1	0.044	40	0.50	-51
2500	0.68	169	8.5	2.6	50	-26.2	0.049	42	0.50	-60
3000	0.67	163	7.0	2.2	39	-25.0	0.056	44	0.54	-67
3500	0.69	156	5.6	1.9	31	-24.1	0.062	46	0.54	-77
4000	0.68	152	4.5	1.7	21	-23.1	0.070	46	0.60	-85
4500	0.69	142	3.6	1.5	12	-22.2	0.078	47	0.60	-92
5000	0.71	138	2.5	1.3	4	-21.2	0.087	46	0.62	-102
5500	0.70	130	1.8	1.2	-5	-20.5	0.094	42	0.66	-111
6000	0.76	124	0.9	1.1	-13	-19.7	0.103	42	0.67	-120
6500	0.71	121	0.0	1.0	-23	-19.1	0.111	38	0.75	-129

NOTES

Applications for Silicon Bipolar Transistors

HEWLETT PACKARD
COMPONENTS

APPLICATIONS FOR SILICON BIPOLAR TRANSISTORS

Two Telecommunications Power Amplifiers for 2 and 4 GHz Using the HXTR-5102 Silicon Bipolar Power Transistor (Portion of Application Note 972)

POWER AMPLIFIERS FOR THE TELECOMMUNICATION BANDS

The HXTR-5102 is a good candidate for power amplifiers in the 1.7 to 2.3 GHz and 3.7 to 4.2 GHz telecommunications bands. Based on the data sheet specifications, the following performance goals are realizable for such amplifiers:

Power at 1 dB Gain Compression	= 0.5 Watt
Gain at 1 dB Gain Compression	= 10 dB (2 GHz)
	= 6 dB (4 GHz)
Gain Flatness	= 2 dB

Input and output SWR's should be reasonable but they need not be perfect, since the use of circulators or the balanced amplifier configuration is assumed.

POWER CONTOURS

Figure 1 is the output power contour graph for the HXTR-5102 transistor at 2 GHz. The output loading was changed and the loci of points of equal P_{1dB} were plotted. The input was matched conjugately at all times. Note that the points of best P_{1dB} and output conjugate match were close.

Figure 2 is the input power contour at 2 GHz. For this measurement, the output was conjugately matched at all times. The input tolerance to mismatch was much less severe than the output tolerance. The points of input conjugate match and best P_{1dB} were close.

S-PARAMETERS—SMALL OR LARGE SIGNAL?

Gain performance is indicated by the S-parameters. Whether small or large signal S-parameters are to be used depends on the linearity of the transistor.

A simple linearity test was performed with the HXTR-5102 transistor. Using the P_{1dB} test as shown in Figure 2, the transistor was simultaneously conjugately matched for small signal. The transistor was then driven into gain compression of 1, 2 and 3.3 dB. In each case the input and output were retuned from the small signal match for better gain. For the 1 and 2 dB gain compression cases, less than 0.2 dB gain improvement was observed. For the 3.3 dB gain compression case, an increase of 0.2 dB of gain was noted. This was a good indication of the lack of change of input and output impedances of the transistor under gain compression.

It was therefore decided that the amplifier circuit designs would use small signal S-parameters.

CIRCUIT DESIGN OF THE 2 GHz AMPLIFIER

The sequence of circuit design is as follows:

1. Design of output circuit for power.
2. Design of input circuit for gain and gain flatness.
3. Computer circuit analysis and optimization.
4. Conversion to microstrip on Duroid.[1]
5. Output and input circuit loading check.

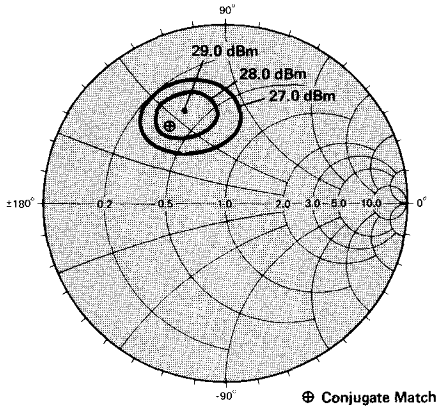


Figure 1. Output Power Contour at 2 GHz, V_{CE} = 18V, I_C = 110 mA.

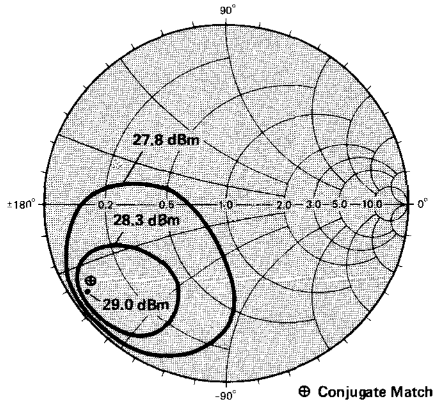


Figure 2. Input Power Contour at 2 GHz, V_{CE} = 18V, I_C = 110 mA.

The output circuit was designed at band center, 2 GHz, according to Figure 3. The 50-ohm output load was transformed to a resistance of 13.5 ohms by a quarter wave transformer.

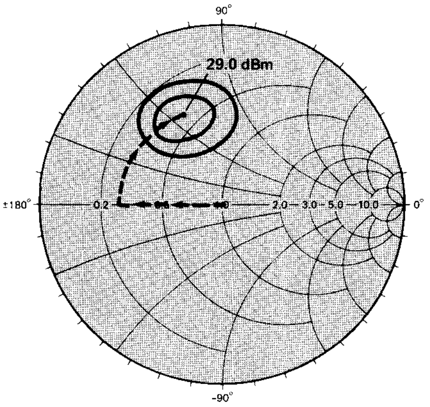


Figure 3. Output Matching on Smith Chart at 2 GHz.

The characteristic impedance, Z_o, of the quarter wave line was given by:

$$Z_o = \sqrt{50 \times 13.5} = 26 \text{ ohms}$$

A rotation by a 50-ohm transmission line of 32° electrical length completed the impedance transformation. The output circuit schematic is shown in Figure 4.

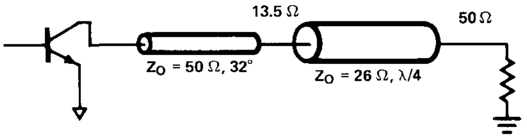


Figure 4. Output Circuit for 2 GHz Amplifier.

The input circuit was designed at the upper band edge, 2.3 GHz. The gain of the transistor was lowest at 2.3 GHz so conjugate match was used at this frequency at the input. The progressive input mismatch from 2.3 down to 1.7 GHz should help to level the gain.

To calculate the input conjugate point at 2.3 GHz the reflection coefficient of the output circuit was noted. This output loading was mapped by the S-parameters of the transistor at 2.3 GHz to an input impedance, the conjugate of which was the required input circuit loading.

Reflection coefficient of output circuit, Γ_L, at 2.3 GHz : $0.56\angle 95°$

Transistor S-parameters at 2.3 GHz :

$$S_{11} = 0.58\angle\ 146°$$
$$S_{21} = 2.16\angle\ -5.6°$$
$$S_{12} = 0.076\angle\ -15.0°$$
$$S_{22} = 0.57\angle\ -127°$$

Load to source mapping formula (from HP-67 E.E. Pac 1)[2]:

$$\Gamma_{MS} = \left[S_{11} + \frac{S_{12}\, S_{21}}{\frac{1}{\Gamma_L} - S_{22}} \right]^*$$

where

Γ_{MS} is the input conjugate match

and

* represents the conjugate.

The input conjugate match, Γ_{MS}, at 2.3 GHz, was calculated to be:

$$0.60\angle\ -134° \ (42\ \Omega \text{ in shunt with } -j\,31\ \Omega).$$

Figure 5 shows the input conjugate match point in admittance Smith Chart coordinates. A shunt capacitive element brought the 50-ohm input load very closely to the conjugate point. The required shunt capacitance at 2.3 GHz was 31 ohms. An open stub transmission line of characteristic impedance Z_o and electrical length 45° ($\lambda/8$) has a reactance equal to $-j\, Z_o \tan 45°$. In other words, it has a capacitance equal to Z_o. So a shunt stub with Z_o equal to 31 ohms was chosen for input matching. The resistive component was close enough to 50 ohms and was not matched. Figure 6 is the schematic of the input circuit.

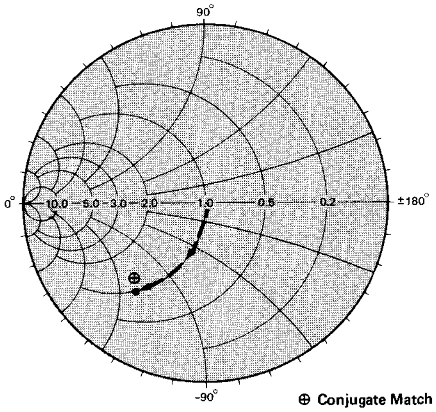


Figure 5. Input Matching on Smith Chart at 2.3 GHz.

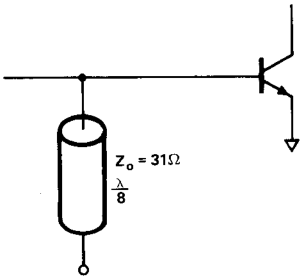


Figure 6. Input Circuit for 2 GHz Amplifier.

The circuit was analyzed on the computer-aided design program COMPACT.[3]

The amplifier performance was as follows:

Frequency (GHz)	Input Reflection Coefficient	Output Reflection Coefficient	Small Signal Gain (dB)	K Factor
1.7	0.73∠159°	0.38∠ 131°	10.02	1.08
2.0	0.52∠137°	0.09∠ −8°	10.83	1.15
2.3	0.10∠169°	0.58∠−116°	9.51	1.19

Input stub : Z_o = 31Ω, 45° at 2.3 GHz
Output lines : Z_o = 50Ω, 32° at 2.0 GHz
Z_o = 26Ω, 90° at 2.0 GHz

Table 1. Initial Amplifier Performance at 2 GHz.

Keeping in mind the main amplifier performance criteria were power output and gain; and that the best P_{1dB} point at the output was very close to the conjugate match point, the circuit was then optimized using COMPACT with equal weighting factors for output reflection coefficient and gain. The variables of optimization were the characteristic impedances of the three transmission line sections.

The optimized amplifier performance was as follows:

Frequency (GHz)	Input Reflection Coefficient	Output Reflection Coefficient	Small Signal Gain (dB)	K Factor
1.7	0.72∠161°	0.48∠ 124°	9.83	1.08
2.0	0.52∠142°	0.19∠ 28°	10.75	1.15
2.3	0.13∠163°	0.53∠ −99°	9.83	1.21

Input stub : Z_o = 30.4Ω, 45° at 2.3 GHz
Output lines : Z_o = 45.2Ω, 32° at 2.0 GHz
Z_o = 27.4Ω, 90° at 2.0 GHz

Table 2. Optimized Amplifier Performance at 2 GHz.

The amplifier performance on paper was observed to be satisfactory. The next step was to convert the transmission lines to microstrip lines on Duroid, the circuit board material used for this amplifier. Card 14A from EE Pac 1 for the HP-67 calculator was used for the conversion. Figure 7 shows the dimensions of the various circuit elements.

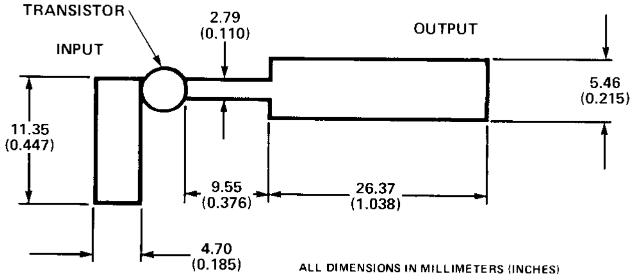


Figure 7. 2 GHz Amplifier Circuit Dimensions on Duroid.

AMPLIFIER PERFORMANCE

The amplifier was fabricated and the measured performance in gain, power output, input and output return loss and reverse isolation, all at 1 dB gain compression, was indicated in Figures 8, 9 and 10. Tuning of the amplifier did not improve the overall performance.

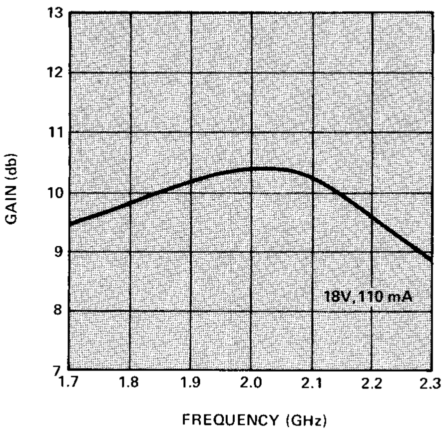


Figure 8. Gain at 1 dB Gain Compression vs. Frequency at 2 GHz, V_{CE} = 18V, I_C = 110 mA.

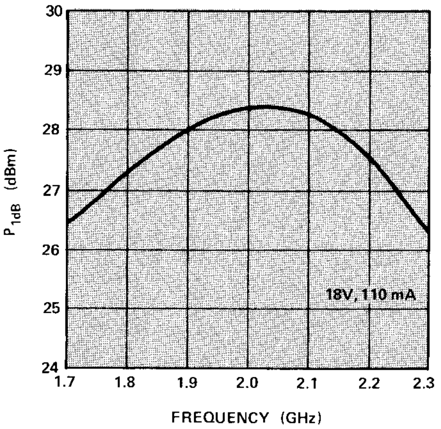


Figure 9. Power Output at 1 dB Gain Compression vs. Frequency at 2 GHz, V_{CE} = 18V, I_C = 110 mA.

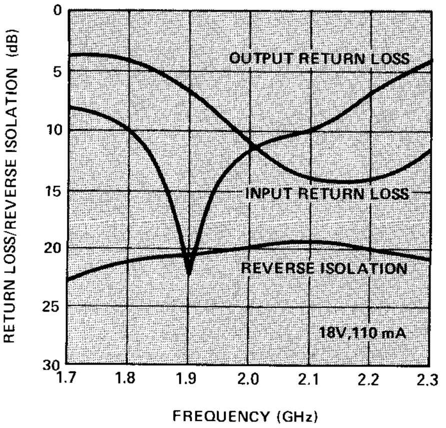


Figure 10. Input and Output Return Loss; Reverse Isolation, at 1 dB Gain Compression vs. Frequency at 2 GHz, V_{CE} = 18V, I_C = 110 mA.

Two tone intermodulation distortion was also measured and plotted in Figure 11.

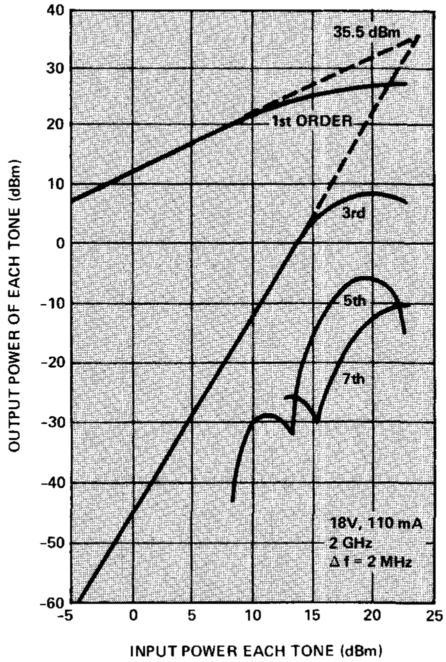


Figure 11. Two Tone Intermodulation Distortion Performance at 2 GHz, V_{CE} = 18V, I_C = 110 mA.

BIAS AND DISTORTION

The dc bias condition of 18V and 110 mA was chosen for best gain and P_{1dB} performance. It was, however, felt that the 110 mA collector current might be too high for symmetrical current clipping.

A linearity test was performed. The collector-emitter voltage was set to 18 volts. The transistor was subjected to a small signal input and kept simultaneously conjugately tuned, while the collector current was varied. The gain was recorded. The collector currents at 1 dB gain fall off points were noted, Table 3.

Gain (dB)	Ic (mA)
11.9	110
10.9	20
10.9	162

Table 3. Small Signal Gain vs. Collector Current at 2 GHz, V_{CE} = 18V.

It appeared that for symmetrical clipping a current of about 90 mA, half-way between 20 and 162 mA, would be ideal.

The transistor was biased to 18V and 90 mA, but the gain was slightly lower. The collector-emitter voltage was raised to 22V to restore the gain. The same linearity test was performed at 22 volts. The result is indicated in Table 4. A midpoint current of 85 mA was arrived at.

Gain (dB)	Ic (mA)
12.2	85
11.2	22
11.2	145

Table 4. Small Signal Gain vs. Collector Current at 2 GHz, V_{CE} = 22V.

AMPLIFIER PERFORMANCE WITH LOW DISTORTION BIAS

Two tone measurements were made with the bias of 22V and 85 mA, Figure 12. Significant improvement of third order distortion was observed at high output levels. The third order intercept, which was obtained from low level signal extrapolation, remained the same.

The AM to PM conversion of the amplifier is plotted in Figure 13.

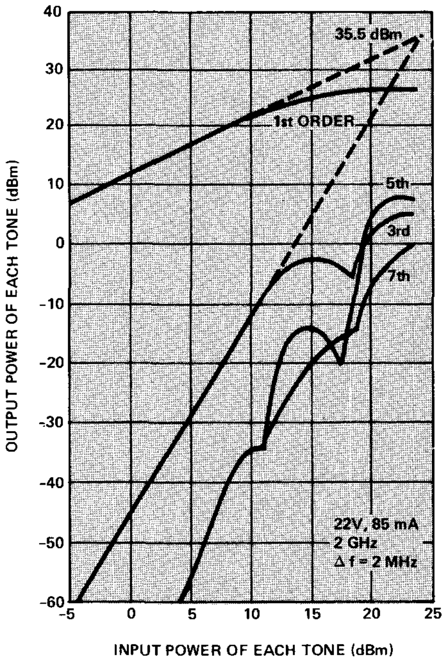


Figure 12. Two Tone Intermodulation Distortion Performance at 2 GHz, V_{CE} = 22V, I_C = 85 mA.

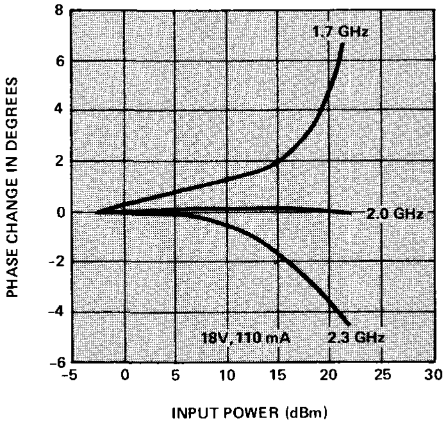


Figure 13. AM to PM Conversion vs. Input Power at 2 GHz, V_{CE} = 18V, I_C = 110 mA.

CIRCUIT DESIGN OF THE 4 GHz AMPLIFIER

The design of the 3.7 to 4.2 GHz amplifier was made easier due to the internal input matching in the transistor around 4 GHz. Figures 14 and 15 are the output and input power contours.

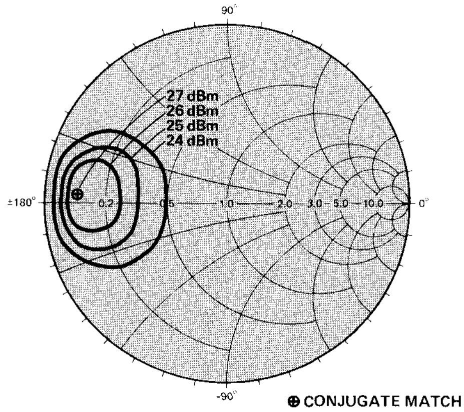


Figure 14. Output Power Contour at 4 GHz, V_{CE} = 18V, I_C = 110 mA.

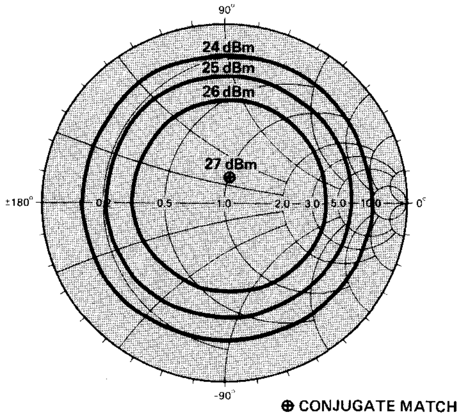


Figure 15. Input Power Contour at 4 GHz, V_{CE} = 18V, I_C = 110 mA.

Output matching is shown in Figure 16. The 50-ohm impedance was matched to the output resistance of 5 ohms. The small output reactance was ignored and not matched. The output circuit schematic is shown in Figure 17.

The input power contours were large circles, indicating the relative insensitivity of power output performance to input tuning, a desirable feature. Together with the internal input matching, it was felt that external input matching was unnecessary for this amplifier.

The circuit was converted to microstrip dimensions. Due to the simplicity of the circuit, computer analysis and optimization was not performed. Figure 18 is the initial amplifier circuit.

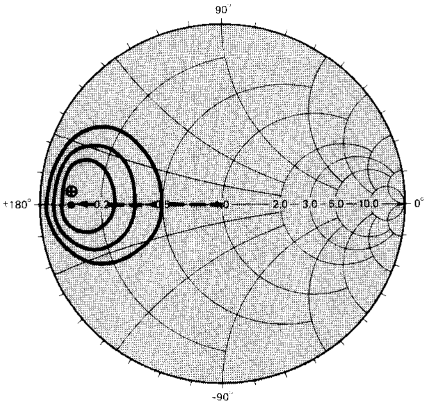


Figure 16. Output Matching on Smith Chart at 4 GHz.

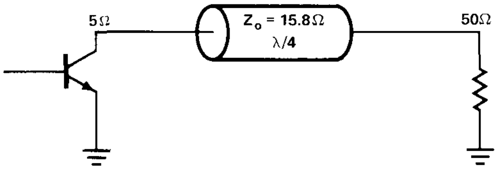


Figure 17. Output Circuit for 4 GHz Amplifier.

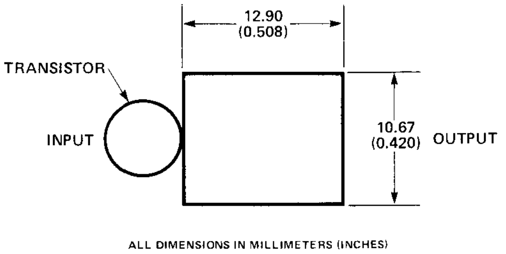


Figure 18. 4 GHz Amplifier Initial Circuit Dimensions on Duroid.

Tuning and Amplifier Performance

Tuning was performed on the amplifier. The criteria for tuning were: first, P_{1dB} performance; then, gain and gain flatness. Figure 19 is the amplifier in its final form.

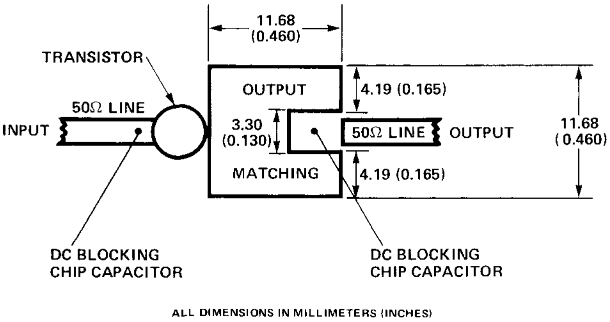


Figure 19. 4 GHz Amplifier Final Circuit Dimensions on Duroid.

Gain and gain flatness at 1 dB gain compression are shown in Figure 20. The gain flatness is good, even in the absence of external input matching.

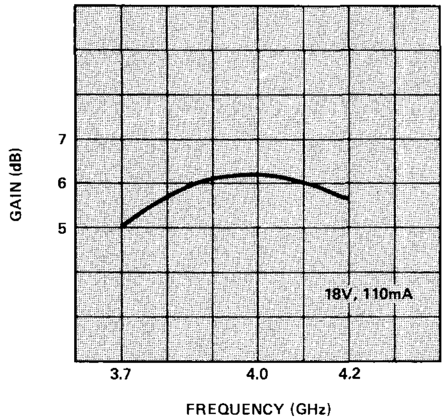


Figure 20. Gain at 1 dB Gain Compression vs. Frequency at 4 GHz, V_{CE} = 18V, I_C = 110 mA.

The power at 1 dB gain compression is shown in Figure 21 input and output return loss, and reverse isolation are shown in Figure 22. The output was tuned to 4.1 GHz to obtain equal power output performance at both band edges.

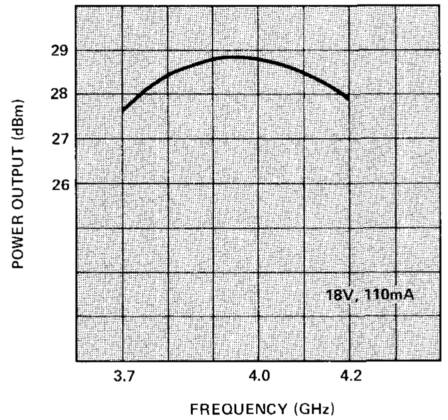


Figure 21. Power Output at 1 dB Gain Compression vs. Frequency at 4 GHz, V_{CE} = 18V, I_C = 110 mA.

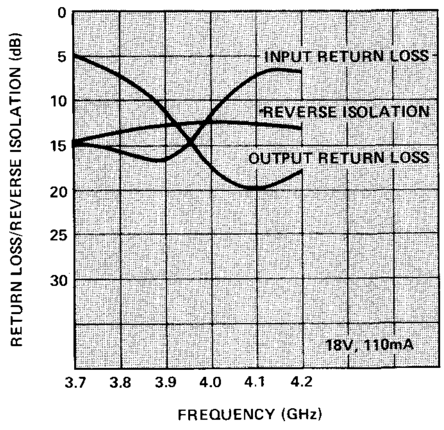


Figure 22. Input and Output Return Loss, Reverse Isolation, at 1 dB Gain Compression, vs Frequency at 4 GHz, V_{CE} = 18V, I_C = 110 mA.

Bias and Distortion

Two tone intermodulation distortion is presented in Figures 23 and 24. The best power output bias is 18V and 110 mA. The best distortion bias is 22V and 85 mA. As in the case of the 2 GHz amplifier the intercept point is unchanged while intermodulation distortion at high output levels is significantly improved.

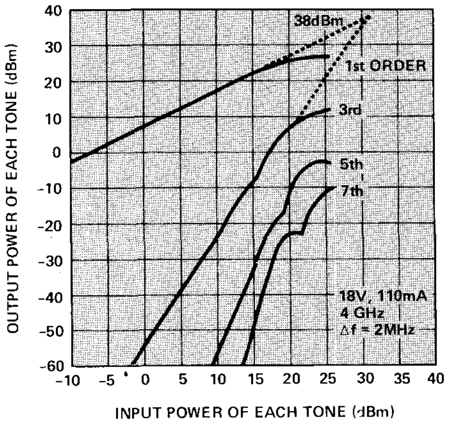


Figure 23. Two Tone Intermodulation Distortion Performance at 4 GHz, V_{CE} = 18V, I_C = 110 mA.

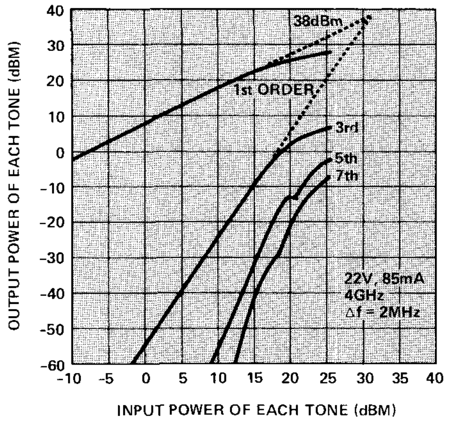


Figure 24. Two Tone Intermodulation Distortion Performance at 4 GHz, V_{CE} = 22V, I_C = 85 mA.

The AM to PM conversion performance of the amplifier is shown in Figure 25.

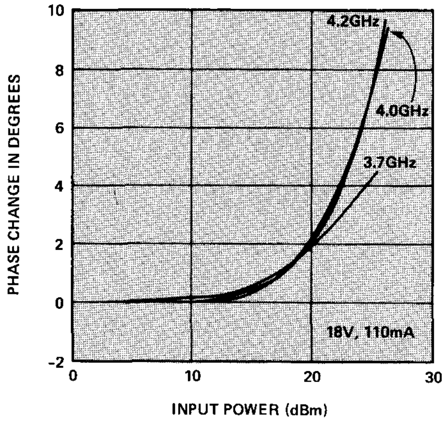
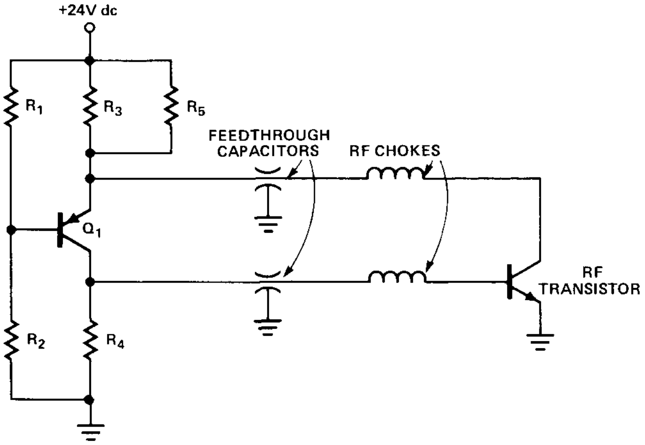


Figure 25. AM to PM Conversion vs. Input Power at 4 GHz, $V_{CE} = 18V$, $I_C = 110$ mA.

Bias Circuit

The same bias circuit was used for both amplifiers. The schematic is in Figure 26. Care should be taken in the circuit layout to avoid oscillations in the bias circuit.



R1	680Ω	¼W
R2	1780Ω	¼W
R3	47Ω	1W
R4	100Ω	½W
R5	*	½W
Q1	2N3251	

* FOR COLLECTOR CURRENT TRIMMING

Figure 26. Active Bias Circuit for both the 2 GHz and the 4 GHz Amplifier.

Bias Insertion

The bias insertion points are points of low impedance. If such a point is electrically disturbed (for example, by a pair of hand-held tweezers) little or no change of amplifier performance is detected. These points were found and used for the 2 GHz amplifier. Due to the compact size of the 4 GHz amplifier completely "null" points were not found and physically convenient points were used instead. The RF chokes were made of 5 to 10 turns of #32 gauge magnet wire, wound to a 0.1 inch coil diameter. Quarter wave line lengths were not used.

AMPLIFIER CONSTRUCTION

The amplifier was constructed of RT/Duroid, 1/32 inch thick, with one ounce copper clad on both sides. The circuit was hand cut and etched in ferric chloride. All dc blocking capacitors used were 1000 pF chip capacitors made by Dielectric Laboratories, Inc.[4], part number Di 6B 102 K 300 L. The two amplifiers, minus the bias supplies, are shown in Figure 27.

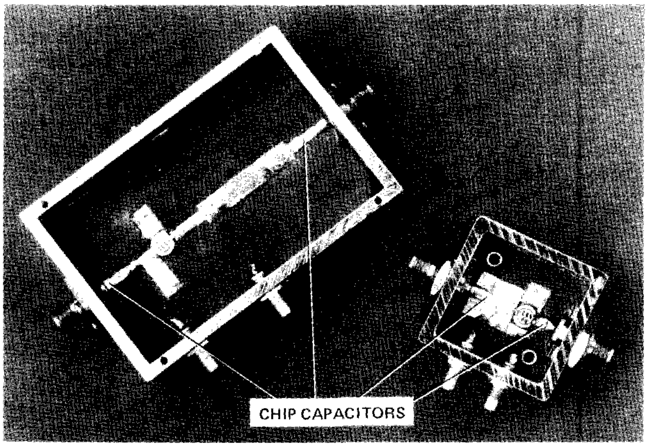


Figure 27. Top View of the 2 and 4 GHz Amplifiers.

REFERENCES

1. Rogers Corporation, Rogers, Connecticut 06263, (203) 774-9605.
2. Hewlett-Packard, 1000 N.E. Circle Blvd., Corvallis, Oregon 97330.
3. Compact Engineering, Inc., 1088 Valley View Court, Los Altos, California 94022.
4. Dielectric Laboratories, Inc., 64 Clinton Road, Fairfield, New Jersey 07006.
5. Hewlett-Packard Application Note 95-1, "S-Parameter Techniques for Faster, More Accurate Network Design", September 1968.
6. Hewlett-Packard Application Note 154, "S-Parameter Design", April 1972.
7. Hewlett-Packard Application Note 967, "A Low Noise 4 GHz Transistor Amplifier Using the HXTR-6101 Silicon Bipolar Transistor", May 1976.

A Low Noise 4 GHz Transistor Amplifier Using the 2N6617 (HXTR-6101) Silicon Bipolar Transistor (Portion of Application Note 967)

DESIGN DATA

Plotted in Figure 1 is the typical noise figure, noise measure* and associated gain of the 2N6617 (HXTR-6101) product as a function of collector current at 4 GHz.

From Figure 1, it can be seen that the minimum noise measure of the device is obtained at a collector current of 3 to 4 mA. However, the associated gain at noise figure is higher at 4 mA, therefore a bias point of V_{CE} = 10 volts and I_C = 4 mA is chosen for low noise measure operation. At these bias conditions, the scattering, gain(1) and noise(2) parameters for the particular device used in this amplifier are:

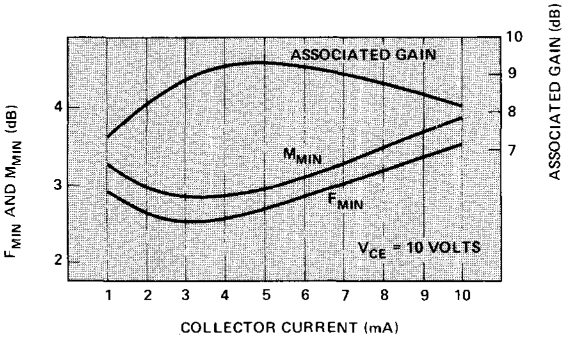


Figure 1. Typical Noise Measure (M_{MIN}), Noise Measure (F_{MIN}) and Associated Gain vs. Collector Current.

Scattering Parameters

S_{11} = 0.552/169°
S_{12} = 0.049/23°
S_{21} = 1.681/26°
S_{22} = 0.839/-67°

Gain Parameters

k = 1.012
$G_{a(max)}$ = 14.7 dB
Γ_{MS} = .941/-154°
Γ_{ML} = .979/70°

Noise Parameters

F_{MIN} = 2.5 dB
Γ_O = .475/166°
R_n = 3.5 ohms

Using the Gain and Noise Parameters above, the available power gain and noise contours are plotted in Figure 2. The contours are mapped onto the source impedance plane(2).

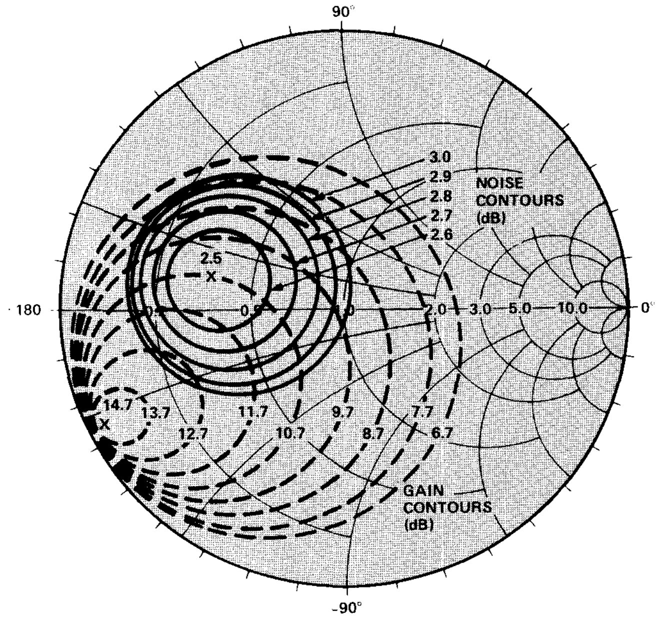


Figure 2. Noise and Gain Contours

Taking a closer look at the Noise Contours, it is seen that the optimum source reflection coefficient (Γ_O) for minimum noise figure (F_{MIN}) is not very sensitive to matching error. The diameter of the first noise contour corresponds to a change in reflection coefficient magnitude of .37 with a noise figure increase of 0.1dB. This characteristic of the 2N6617 is very advantageous to circuit designers trying to match for minimum noise figure. From the two sets of contours, it appears that the associated gain at minimum noise figure will be approximately 11 dB with the output seeing a conjugate match.

Since the design goal is to construct a low noise amplifier, the optimum noise measure bias condition is selected. There is also an optimum bias condition for maximum gain and another for output power. Even at the optimum noise measure bias there are trade-offs between noise figure, gain and power output due to source and load impedance.

At the optimum noise measure bias of V_{CE} = 10 volts and I_C = 4mA, the source and load reflection coefficients for lowest noise figure, maximum gain and greatest power are tabulated and plotted in Figure 3. Figure 3 is plotted for the particular device used in this amplifier design. The source and load reflection coefficients are mapped onto the source or load impedance plane.

---

*The system noise figure of an infinite cascaded chain of identical amplifier stages. For further explanation, see Hewlett-Packard Application Bulletin #9.

$$M_{MIN} = 10 \log_{10} \left[1 + \frac{F_{MIN} - 1}{1 - \frac{1}{Ga}} \right]$$

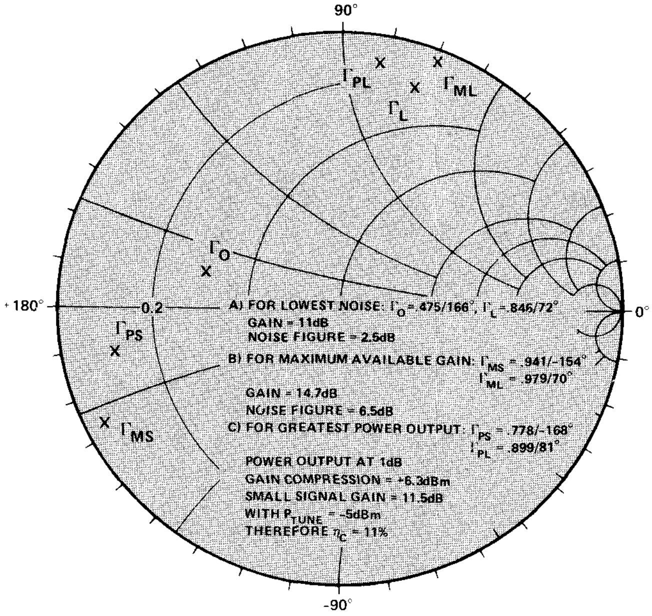


Figure 3. Matching Tradeoffs

INPUT MATCHING NETWORK

The main purpose of the input matching network is to provide the optimum source impedance for minimum noise figure. The basic design philosophy in realizing this network is:

1) Convert the optimum source reflection coefficient (Γ_O) to impedance.
2) From this impedance determine the equivalent admittance.
3) The susceptance component is realized with a short circuited eighth-wave ($\frac{\lambda}{8}$) length stub.
4) The conductance component is realized with a quarter-wave ($\frac{\lambda}{4}$) length impedance transformer.

The realization and Smith Chart mapping for this input matching network is described below and shown in Figure 4.

1) The impedance Z_{NF}, corresponding to Γ_O = .475/166° is:

$$Z_{NF} = \frac{(1 - |\Gamma_O|^2)\,50}{1 + |\Gamma_O|^2 - 2\,|\Gamma_O|\,\mathrm{Cos}\,\underline{/\Gamma_O}} + \frac{j\,(2\,|\Gamma_O|\,\mathrm{SIN}\,\underline{/\Gamma_O})\,50}{1 + |\Gamma_O|^2 - 2\,|\Gamma_O|\,\mathrm{Cos}\,\underline{/\Gamma_O}}$$

$$Z_{NF} = 18.0 + j\,5.35$$

2) $Y_{NF} = \dfrac{1}{Z_{NF}} = 0.0510 - j\,0.0152$

3) A short circuited stub less than a quarter-wave length long looks like a shunt inductor of impedance $Z = jZ_O \tan \beta\ell$. Hence a short circuited stub that is an eighth-wave length long looks like a shunt inductor of impedance jZ_O where Z_O is the characteristic impedance of the stub. Hence

$$Z_O = \frac{1}{.0152} = 65.8 \text{ ohms.}$$

4) Since the driving source impedance is 50Ω, a quarter-wave transformer of characteristic impedance:

$$Z'_O = \sqrt{(50)\,(19.6)} = 31.31\Omega$$

completes the input matching network.

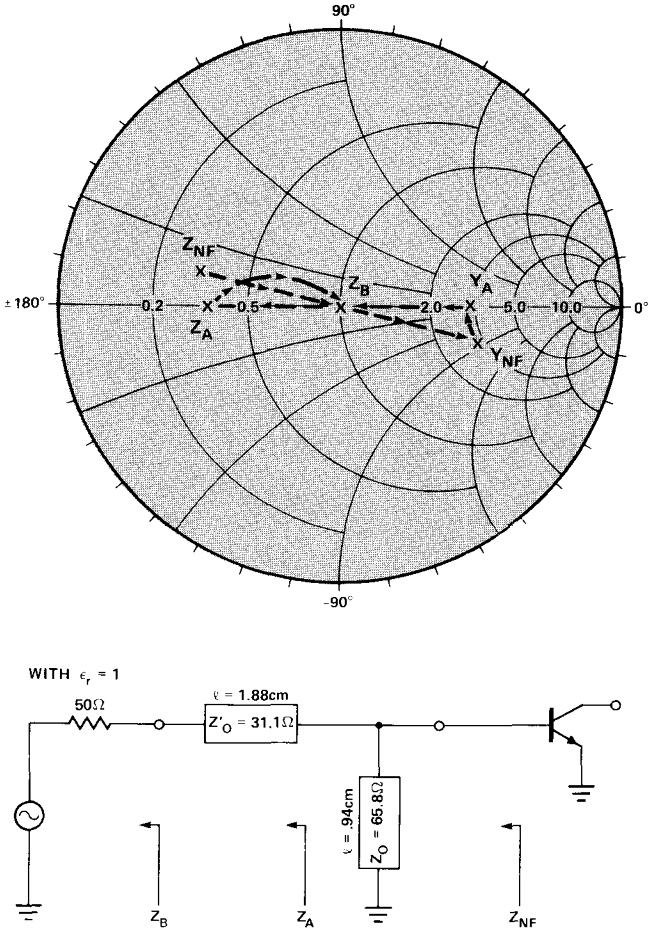


Figure 4. Input Matching Network

OUTPUT MATCHING NETWORK

With one of the design goals being an output VSWR of less than 1.5:1, the output matching network is designed to provide a conjugate match with the source impedance, Z_{NF}. The basic design procedure is:

1) Calculate S'_{22}, the output reflection coefficient with the source reflection coefficient being Γ_O.
2) Provide a conjugate match for the output with a load reflection coefficient equal to $S'_{22}{}^*$. ($\Gamma_L = S'_{22}{}^*$)
3) The matching section could be realized with a shunt stub and a series transformer similar to the input network. However, in order to increase the tuning capabilities of the network, an extra section of matching is used.

The realization and Smith Chart mapping of this output network is described below and shown in Figure 5.

1) From the S-Parameters on the device, S'_{22} can be calculated as follows:

$$S'_{22} = S_{22} + \frac{S_{21}\,S_{12}\,\Gamma_O}{1 - S_{11}\,\Gamma_O}$$

$$\therefore S'_{22} = .846 \angle\!\underline{-72^\circ}$$

Now, providing a conjugate match to S_{22}' for a good output VSWR, the load reflection coefficient (Γ_L) should be:

$$\Gamma_L = .846\angle\!\underline{72^\circ}$$

2) A problem with the output is the relatively high Q. This can cause problems in supplying a conjugate load match to obtain a good output VSWR because of sensitivity to small dimensional changes. Calculating this output Q gives us,

$$Q\,(S'_{22}) = 5.65$$

With this dominant Q, the calculated 3 dB bandwidth (B.W.) is:

$$100 \times \frac{\text{B.W.}}{f_O} = \frac{100}{Q\,(S'_{22})} = 18\%$$

This bandwidth equals 720 MHz with a center frequency (f_O) of 4 GHz.

3) A 0.61 cm ($2\beta\ell = 59^\circ$) equivalent air length of $Z_O = 50\Omega$ transmission line was added to the output to provide an output soldering area. The rotated output reflection coefficient is:

$$\Gamma_1 = .846/\!-131^\circ$$

The corresponding impedance, Z_1, is

$$Z_1 = \frac{(1 - |\Gamma_1|^2)\,50}{1 + |\Gamma_1|^2 - 2|\Gamma_1|\,\mathrm{Cos}\,\angle\!\underline{\Gamma_1}} + \frac{j\,(2\,|\Gamma_1|\,\mathrm{S_{in}}\,\angle\!\underline{\Gamma_1})\,50}{1 + |\Gamma_1|^2 - 2|\Gamma_1|\,\mathrm{Cos}\,\angle\!\underline{\Gamma_1}}$$

$$Z_1 = 5.03 - j\,22.6$$

$$Y_1 = \frac{1}{Z_1} = 9.35 \times 10^{-3} + j.0422$$

4) A short circuited stub an eighth-wave length long looks like a shunt inductor of admittance, $-j\,Y_O$. The purpose of this shunt stub is to tune out most of the susceptance component in the admittance Y_1. A tuning section will be added to further match the output.

A convenient characteristic admittance, $Y_O = 0.0345$ ℧ is used for the shunt stub.

$$Y_2 = 9.35 \times 10^{-3} + j\,.0422 - j\,.0345 = 9.35 \times 10^{-3} + j\,.0077$$

$$Z_2 = \frac{1}{Y_2} = 63.7 - j\,52.5$$

5) The next element is a transformer to obtain an admittance with real part matched to the 50 ohm load. This is accomplished with an 80 ohm line 1.35 cm long. ($\epsilon_r = 1$) ($\beta\ell = 64.8^\circ$)

$$Z_3 = \frac{Z_O\,(Z_2 + j\,Z_O \tan\beta\ell)}{(Z_O + j\,Z_2 \tan\beta\ell)}$$

$$Z_3 = 39.12 + j\,21.1$$

$$Y_3 = \frac{1}{Z_3} = .02 - j\,.0107$$

6) An open stub is chosen to provide some tuning capability. An *open circuited* stub less than a quarter-wave length long looks like a shunt admittance $Y = j\,Y_O \tan\beta\ell$. An open circuited stub of characteristic admittance $Y_O = .039$ ℧ and length 0.4 cm ($\epsilon_r = 1$) ($\beta\ell = 19.2^\circ$) is added.

Its susceptance is $.039 \tan 19.2^\circ = .0136\ \Omega$

$$Y_4 = .02 - j\,.0107 + j\,.0136 = .02 + j\,.0029$$

$$Z_4 = \frac{1}{Y_4} = 50 - j\,7.1$$

7) Now Z_4 is matched with a transformer with a characteristic impedance of 80 Ω and length of .19 cm ($\epsilon_r = 1$) ($\beta\ell = 9.12^\circ$)

$$Z_5 = \frac{Z_O\,(Z_4 + j\,Z_O \tan\beta\ell)}{(Z_O + j\,Z_4 \tan\beta\ell)} = 50\Omega$$

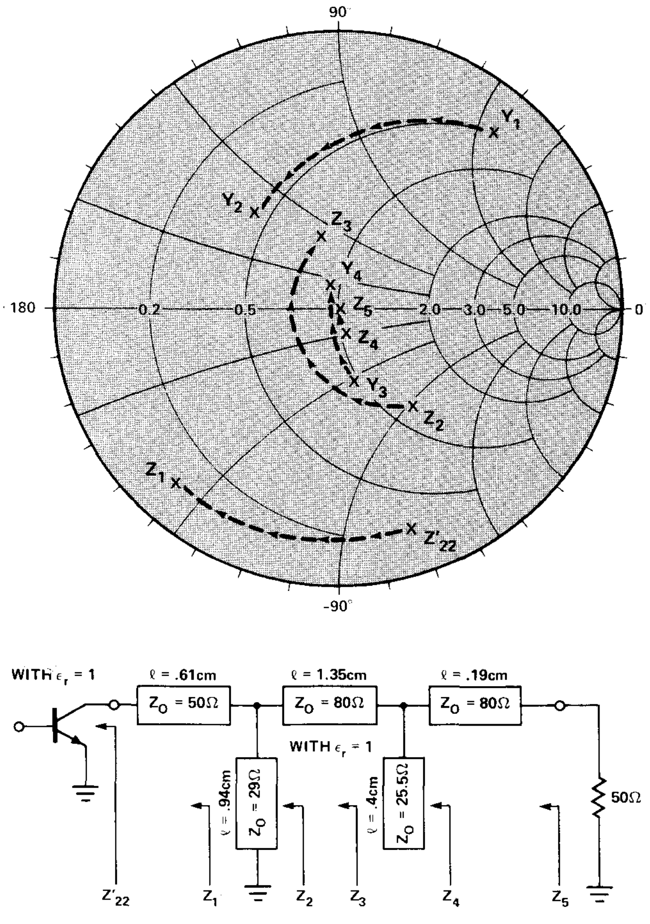


Figure 5. Output Matching Network

The output tuning section as described has the flexibility for tuning in four areas:

- Adjusting the length of the *series line*
- Changing the width or characteristic impedance of the open circuited shunt stub
- Modifying the length of the shunt stub
- Varying the length of the final series line

This completes the design of the output matching network.

Figures 6, 7 and 8 show the room temperature performance of the amplifier.

Phase Linearity - Phase linearity is ±5° over the entire 500 MHz band width.

Isolation - Isolation is better than -24 dB over the entire 3.7 to 4.2 GHz band.

AM to PM Conversion - With an output power level of - 13 dBm, the input power level is referenced. At this input reference level, the input power is varied ± 10dBm. Over the 3.7 to 4.2 GHz band, the AM to PM conversion is less than 0.13°/dB.

Third Order Intercepts - With two fundamental signals injected into the input at 3.95 and 4.05 GHz, the output power level for each fundamental signal is set at 0 dBm. The third order intermodulation products are both -34 dB below the two fundamentals at the output. Therefore, the third order intercept point is + 17 dBm.

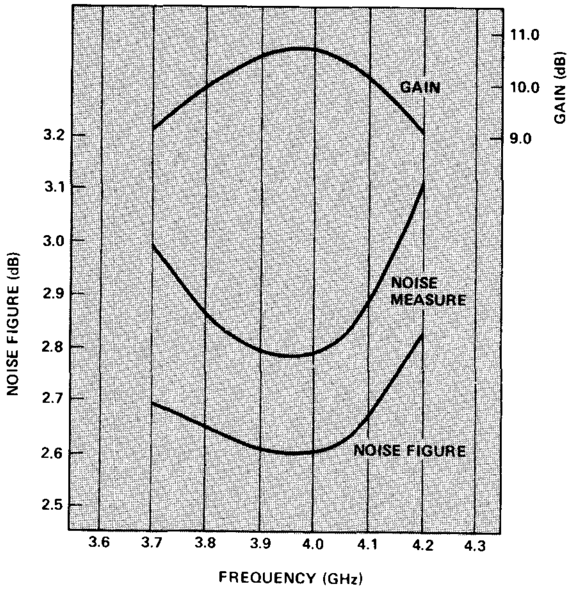


Figure 6. Noise and Gain Performance.

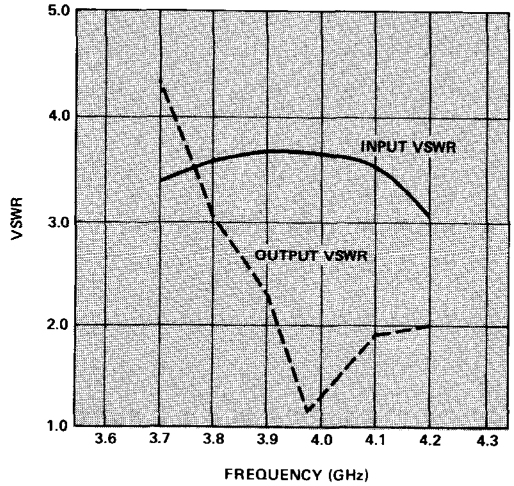


Figure 7. Input — Output VSWR Performance.

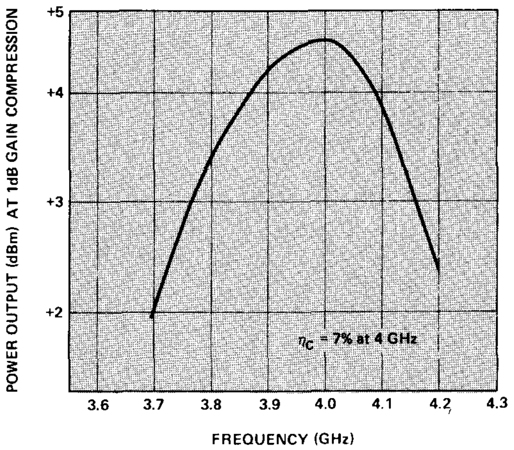


Figure 8. Power Output Performance.

Spurious Outputs - With a 4 GHz, 0 dBm input signal injected into the amplifier, no spurious signals were detected above -60 dBm over the 2 to 6 GHz band.

Group Delay - The group delay over the entire 500 MHz bandwidth is less than .53 n sec.

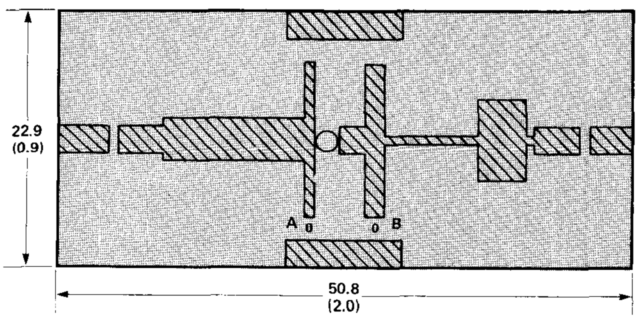
CONSTRUCTION

The board material is .031" RT/Duroid 120-061, with 1 oz copper clad on two sides. The relative dielectric constant (ϵ_r) is 2.23. Duroid was chosen because of its low loss tangent. The thickness of .031" was chosen so the emitter top cap could be soldered to the RF ground, thereby taking advantage of the low emitter inductance.

To minimize transition interactions between the series transmission lines and shunt stubs, the shunt stubs were balanced along the series transmission lines.

Some tuning on the output matching network was required. The final realization of this circuit on Duroid is shown in Figure 9. The RF board size is 2 inches by 0.9 inches.

A schematic of the complete amplifier and biasing circuit can be seen in Figure 10.



DIMENSIONS IN MILLIMETERS (INCHES).

Figure 9. R.F. Board Layout.

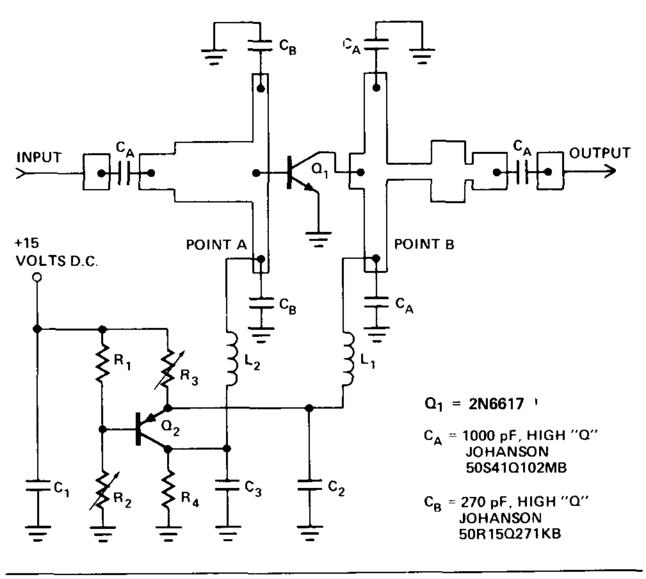


Figure 10. **Complete Amplifier Schematic, with Bias Circuit Elements.**

Element	Value
R_1	100 KΩ,¼W
R_2	200 KΩ, 1W, potentiometer
R_3	5 KΩ, 1W, potentiometer
R_4	2.61 KΩ, ¼W
C_1	.01μF, 100v, disc.
C_2	.002μF, 250v, disc.
C_3	.01μF, 100v, disc.
L_1	2 turns #36 enameled wire on .1" core (air)
L_2	2 turns #36 enameled wire on .1" core (air)
Q_2	$h_{FE} \geqslant 75$, $f_T > 150$ MHz, $BV_{CEO} \geqslant$ 30V, $I_{C\,max} \leqslant 50$mA, $P_D \leqslant 300$ mW, PNP Silicon, Plastic.

A picture of the assembled amplifier can be seen in Figure 11. The amplifier draws 4.4 mA from a 15 volt DC power supply.

The quiescent point is adjusted by R_2 and R_3. R_2 is adjusted to provide the proper V_{CE} voltage and R_3 is adjusted to supply the correct collector current (I_C).

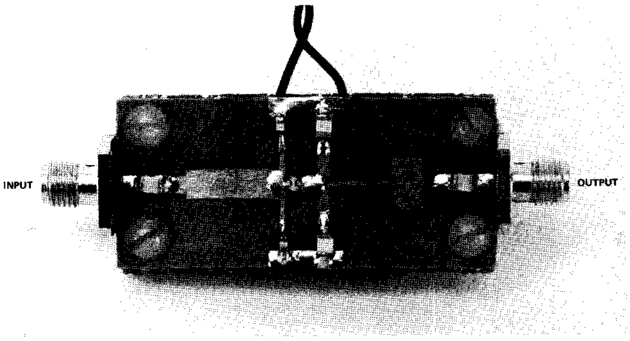


Figure 11. Amplifier – Top View.

REFERENCES

1. Hewlett-Packard Application Note 95-1, "S-Parameter Techniques for faster, more accurate Network Design", September 1968, Page 12.
2. Hewlett-Packard Application Note 154, "S-Parameter Design", April 1972, Pages 26 and 27.

NOTES

SUPPLEMENTARY READINGS FOR BIPOLAR TRANSISTORS

A. Bipolar Transistor Theory

1. Streetman, *Solid State Electronic Devices,* Prentice-Hall, Inc.

*2. H. F. Cooke, "Microwave Transistors — Theory and Design," *Proc. IEEE,* vol. 59, No. 8, pp. 1163-1181, August 1971.

*3. E.O. Johnson, "Physical Limitations on Frequency and Power Parameters of Transistors," *RCA Review,* vol. 26, No. 2, pp. 163-177, June 1965.

*4. N.J. Gri, "Microwave Transistors — From Small Signal to High Power," *The Microwave Journal,* Vol. 14, No. 12, pp. 45-50, February 1971.

B. Bipolar Transistor Design

*5. J.A. Archer, "Design and Performance of Small-Signal Microwave Transistors," *Solid State Electronics,* Vol. 15 pp. 249-258, 1972.

*6. J.A. Benjamin, "New Design Concepts for Microwave Power Transistors," *The Microwave Journal,* Vol. 16, No. 10, pp. 10-14, October 1973.

7. T.H. Hsu and C.P. Snapp, "Low-Noise Microwave Bipolar Transistor with Sub-half-micron Emitter Width," *IEEE Transaction on Electron Devices,* June 1978.

C. Circuit Design

8. *Hewlett-Packard* Application Note 95-1, "S-Parameter Techniques for Faster, More Accurate Network Design."

10. *Hewlett-Packard Components* Application Note 967, "A Low Noise 4 GHz Transistor Amplifier Using the HXTR-6101 Silicon Bipolar Transistor."

11. *Hewlett-Packard Components*, Application Note 972, "Two Telecommunications Power Amplifiers for 2 and 4 GHz using the HXTR-5102 Silicon Bipolar Power Transistor."

*12. O. Pitzalis, Jr., "Broad-Band Microwave Class-C Transistor Amplifiers," *IEEE Transactions on Microwave Theory and Techniques,* MTT-21, No. 11, pp. 660-668, November 1973.

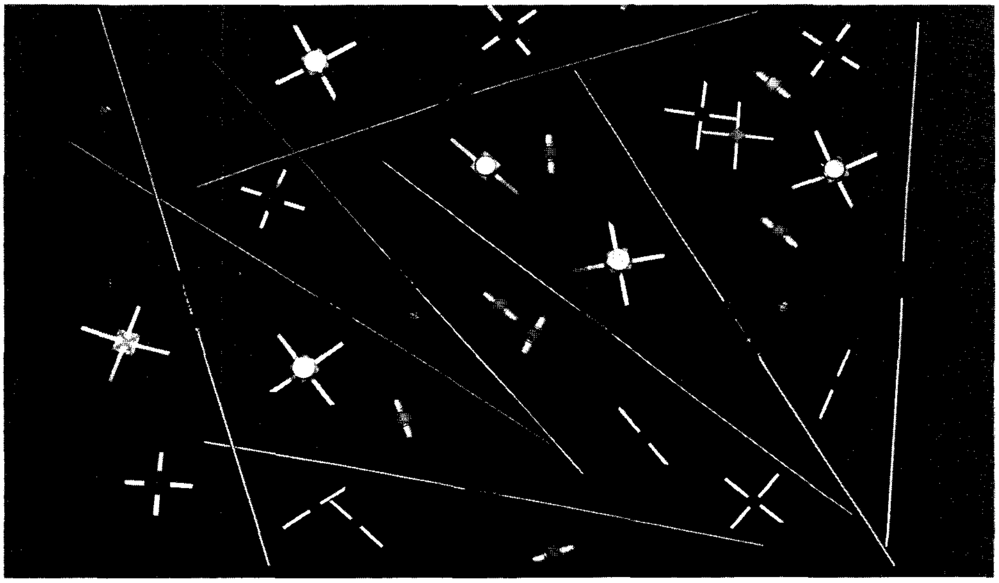
D. Computer Aided Design

13. *COMPACT Manual, AMPSYN Manual,* Available from Les Besser, Compact Engineering, Inc. 1651 Jolly Court, Los Altos, CA 94022.

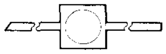
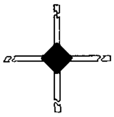
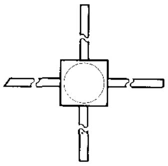
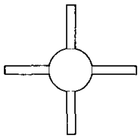
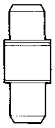
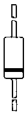
* These papers are found in a collection of transistor papers in *Microwave Transistors*, by Dr. E.D. Graham, Jr., and Dr. C.W. Gwyn, Artech House, Inc.

NOTES

Schottky Barrier and High Conductance Diodes



Schottky Diodes Selection Guide

Package Outline	Application	Mixer (Pg. No.)	Detector (Pg. No.)	Zero Bias Detector (Pg. No.)	General Purpose (Pg. No.)
	C2	88	—	—	—
	H2				
	C4	96	—	—	—
	H4				
	E1				
	44	98	110	105	—
	49				
	15				79
	12	—	—	—	80

Detailed specifications are given on the pages listed. The primary applications are shown in this guide. Other applications are discussed in the text.

HEWLETT hp PACKARD
COMPONENTS

SCHOTTKY BARRIER DIODES FOR GENERAL PURPOSE APPLICATIONS

5082-2301/02/03/05
5082-2800(1N5711)
5082-2810(1N5712)
5082-2811(1N5713) NEW
5082-2835
5082-2900
HSCH-1001(1N6263)

Features

LOW TURN-ON VOLTAGE: .34V AT 1mA
PICO-SECOND SWITCHING SPEED
HIGH BREAKDOWN VOLTAGE: UP TO 70V
UNIFORM FORWARD TRACKING

Description/Applications

The 5082-2800, 2810, 2811 are passivated Schottky barrier diodes which use a patented "guard ring" design to achieve a high breakdown voltage. They are packaged in a low cost glass package. They are well suited for high level detecting, mixing, switching, gating, log or A-D converting, video detecting, frequency discriminating, sampling and wave shaping.

The 5082-2835 is a passivated Schottky diode in a low cost glass package. It is optimized for low turn-on voltage. The 5082-2835 is particularly well suited for UHF mixing.

The 5082-2300 and 2900 Series devices are unpassivated Schottky diodes in a glass package. These diodes have extremely low 1/f noise and are ideal for low noise mixing, and high sensitivity detecting. They are particularly well suited for use in Doppler or narrow band video receivers.

The HSCH-1001 is a Hybrid Schottky diode sealed in a rugged double stud Outline 12 glass package suitable for automatic insertion. The low turn-on voltage, fast switching speed, and low cost of these diodes make them ideal for general purpose switching.

Application Bulletins 13, 14, 15, and 16 describe applications in which these diodes are used for speed up of a transistor, clipping, clamping, and sampling, respectively.

Maximum Ratings at T$_{CASE}$=25°C

Junction Operating and Storage Temperature Range

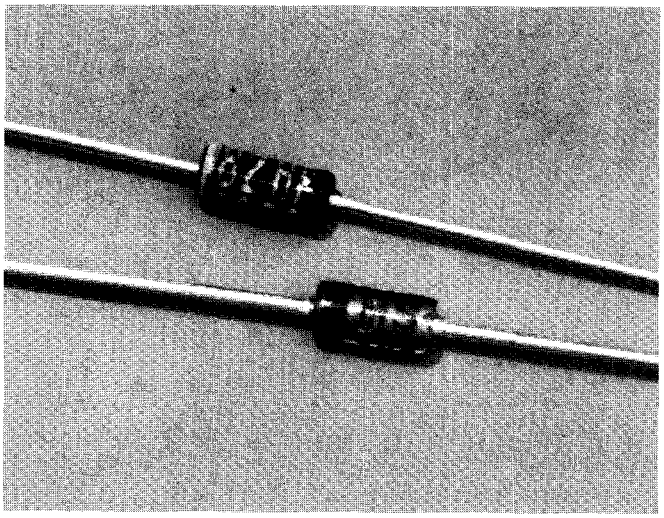
5082-2305, 2301, 2302, 2303, 2900	-60°C to +125°C
5082-2800, 2810, 2811, HSCH-1001	-65°C to +200°C
5082-2835	-60°C to +150°C

Operation of these devices within the above temperature ratings will assure a device Mean Time Between Failure (MTBF) of approximately 1 x 10^7 hours.

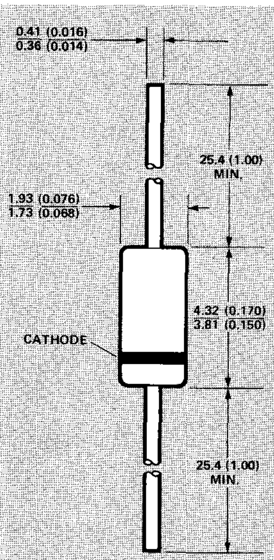
DC Power Dissipation (Measured in an infinite heat sink)
Derate linearly to zero at maximum rated temperature

5082-2305, 2301, 2302, 2303, 2900	125 mW
5082-2800, 2810, 2811	250 mW
5082-2835	150 mW
HSCH-1001	400 mW

Peak Inverse Voltage .... V$_{BR}$

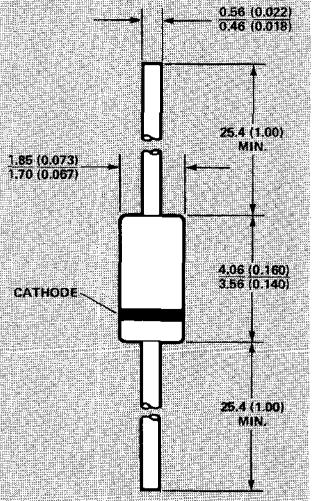


Package Dimensions



OUTLINE 15

DIMENSIONS IN MILLIMETERS AND (INCHES)



OUTLINE 12 (DO-35)

Electrical Specifications at $T_A = 25°C$

	Part Number 5082-	Package Outline	Minimum Breakdown Voltage V_{BR} (V)	Maximum Forward Voltage V_F (mV)	V_F = 1V Max at Forward Current I_F (mA)	Maximum Reverse Leakage Current I_R (nA)	at V_R (V)	Maximum Capacitance C_T (pF)
0.75	2800	15	70	410	15	200	50	2.0
0.75	1N5711[1]	15	70	410	15	200	50	2.0
·80	2305	15	30	400	75	300	15	1.0
6-83	2301[2]	15	30	400	50	300	15	1.0
78	2302[2]	15	30	400	35	300	15	1.0
3·11	2303[2]	15	20	400	35	500	15	1.0
0-90	2810	15	20	410	35	100	15	1.2
0-90	1N5712[1]	15	20	550	35	150	16	1.2
0-75	2811	15	15	410	20	100	8	1.2
0-75	1N5713[1]	15	15	410	20	100	8	1.2
1-43	2900	15	10	400	20	100	5	1.2
0-68	2835	15	5*	340	10†	100	1	1.0
0-47	HSCH-1001[1] (1N6263)	12 (DO-35)	60	410	15	200	50	2.2
	Test Conditions		$I_R = 10\ \mu A$ $^*I_R = 100\ \mu A$	$I_F = 1$ mA	$^\dagger V_F = .45V$			$V_R = 0$ V f = 1.0 MHz

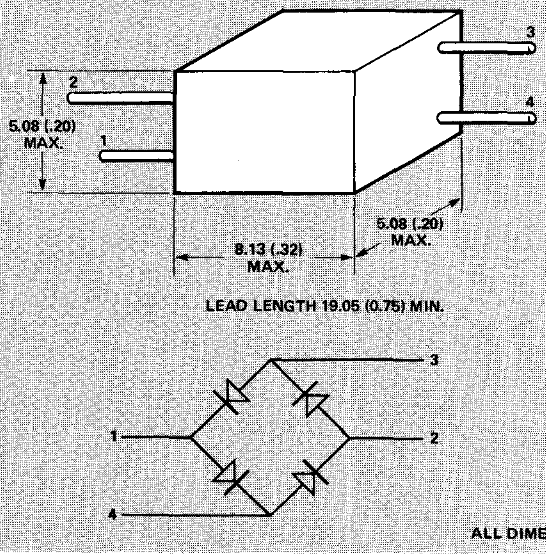
Notes:

1. Effective Minority Carrier Lifetime (τ) for all these diodes is 100 ps maximum measured with Krakauer method at 20 mA except for HSCH-1001 (1N6263), 1N5711, 1N5712, and 1N5713 which are measured at 5 mA.
2. 5082-2301 = 1N5165, 5082-2302 = 1N5166, 5082-2303 = 1N5167.

Matched Pairs and Quads

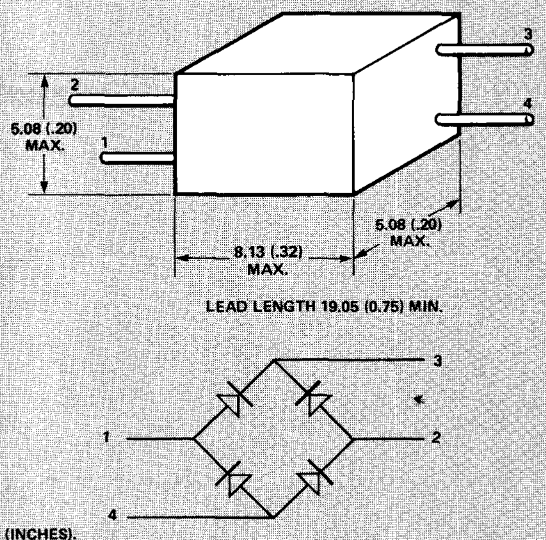
	Basic Part Number 5082-	Matched Pair Unconnected	Matched Quad Unconnected	Matched Ring Quad Encapsulated G-1 Outline	Matched Bridge Quad Encapsulated G-2 Outline	Batch Matched	Test Conditions
6-83	2301	5082-2306 14-28 $\Delta V_F = 20$ mV $\Delta Co = 0.2$ pF					ΔV_F at I_F = 0.75–20 mA ΔCo at f = 1.0 MHz
3-11	2303	5082-2308 8-07 $\Delta V_F = 20$ mV $\Delta Co = 0.2$ pF	5082-2370 24 93 $\Delta V_F = 20$ mV $\Delta Co = 0.2$ pF	5082-2396 29-8 $\Delta V_F = 20$ mV $\Delta Co = 0.2$ pF	5082-2356 29-8 $\Delta V_F = 20$ mV $\Delta Co = 0.2$ pF		ΔV_F at I_F = 0.75–20 mA ΔCo at f = 1.0 MHz
1-43	2900	5082-2912 3-48 $\Delta V_F = 30$ mV	5082-2970 8-71 $\Delta V_F = 30$ mV	5082-2996 17-39 $\Delta V_F = 30$ mV	5082-2997 17-42 $\Delta V_F = 30$ mV		ΔV_F at I_F = 1.0–10 mA
0-75	2800	5082-2804 1-68 $\Delta V_F = 20$ mV	5082-2805 3-32 $\Delta V_F = 20$ mV			5082-2836 1-15 $\Delta V_F = 20$ mV $\Delta C_O = 0.1$ pF	ΔV_F at I_F = 0.5–5 mA ΔC_O at f = 1.0 MHz
0.75	2811		5082-2815 3-32 $\Delta V_F = 20$ mV	5082-2814 7-82 $\Delta V_F = 20$ mV	5082-2813 7-82 $\Delta V_F = 20$ mV	5082-2826 1-15 $\Delta V_F = 10$ mV $\Delta C_O = 0.1$ pF	ΔV_F at I_F = 10 mA ΔC_O at f = 1.0 MHz
0.68	2835					5082-2080 1-08 $\Delta V_F = 10$ mV $\Delta C_O = 0.1$ pF	ΔV_F at I_F = 10 mA ΔC_O at f = 1.0 MHz

Outline G-1



LEAD	COLOR
1	BROWN
2	RED
3	ORANGE
4	YELLOW

Outline G-2



ALL DIMENSIONS IN MILLIMETERS (INCHES).

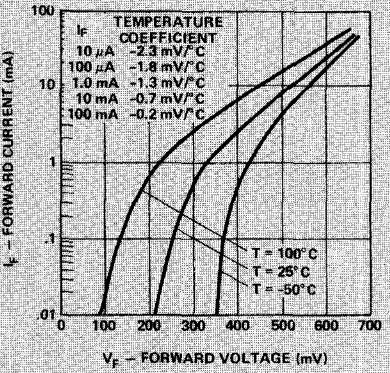


Figure 1. I-V Curve Showing Typical Temperature Variation for 5082-2300 Series Schottky Diodes.

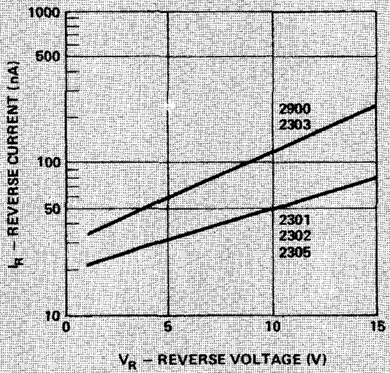


Figure 2. 5082-2300 and 5082-2900 Series Typical Reverse Current vs. Reverse Voltage at T_A = 25°C.

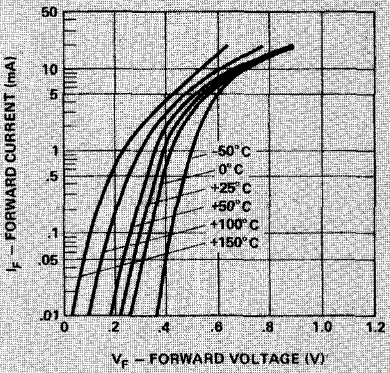


Figure 3. I-V Curve Showing Typical Temperature Variation for 5082-2800 or 1N5711 Schottky Diodes.

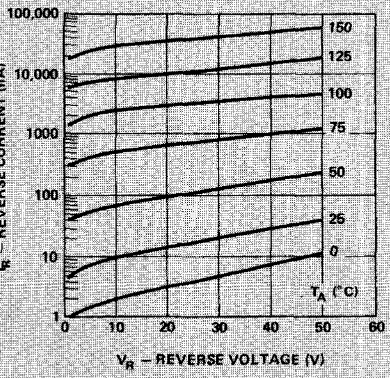


Figure 4. (5082-2800 or 1N5711) Typical Variation of Reverse Current (I_R) vs. Reverse Voltage (V_R) at Various Temperatures.

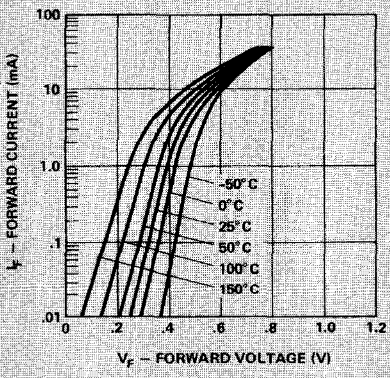


Figure 5. I-V Curve Showing Typical Temperature Variation for the 5082-2810 or 1N5712 Schottky Diode.

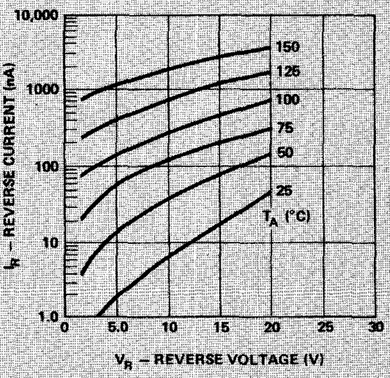


Figure 6. (5082-2810 or 1N5712) Typical Variation of Reverse Current (I_R) vs. Reverse Voltage (V_R) at Various Temperatures.

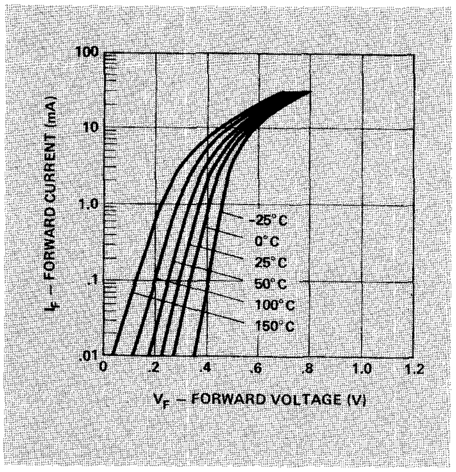


Figure 7. I-V Curve Showing Typical Temperature Variation for 5082-2811 Schottky Diode.

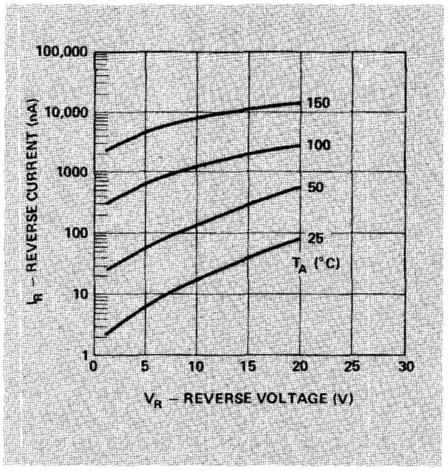


Figure 8. (5082-2811) Typical Variation of Reverse Current (I_R) vs. Reverse Voltage (V_R) at Various Temperatures.

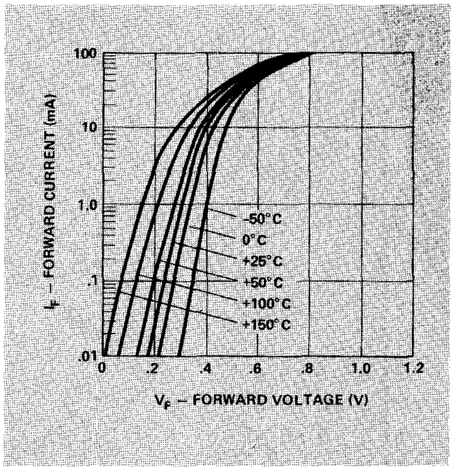


Figure 9. I-V Curve Showing Typical Temperature Variations for 5082-2835 Schottky Diode.

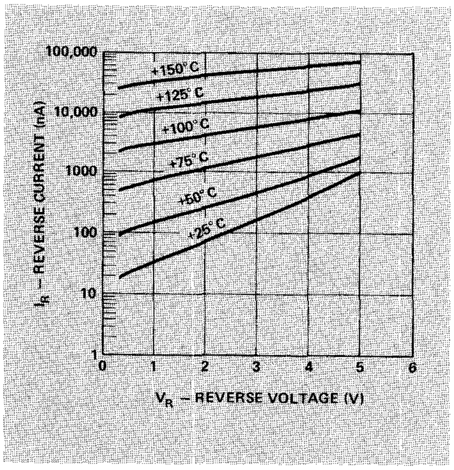


Figure 10. (5082-2835) Typical Variation of Reverse Current (I_R) vs. Reverse Voltage (V_R) at Various Temperatures.

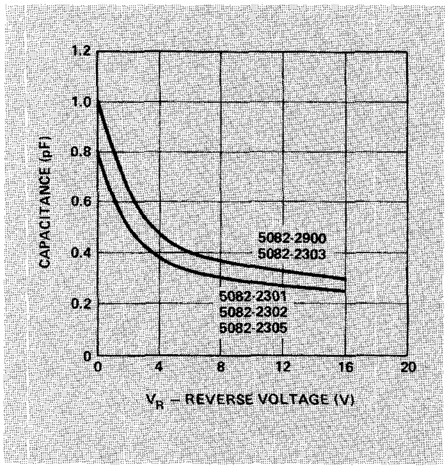


Figure 11. 5082-2300 and -2900 Series Typical Capacitance vs. Reverse Voltage.

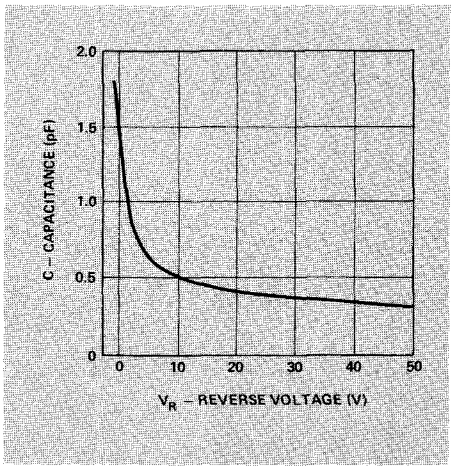


Figure 12. (5082-2800 or 1N5711) Typical Capacitance (C) vs Reverse Voltage (V_R).

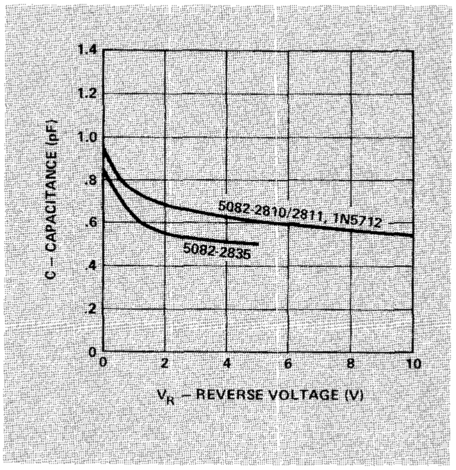


Figure 13. Typical Capacitance (C) vs. Reverse Voltage (V_R).

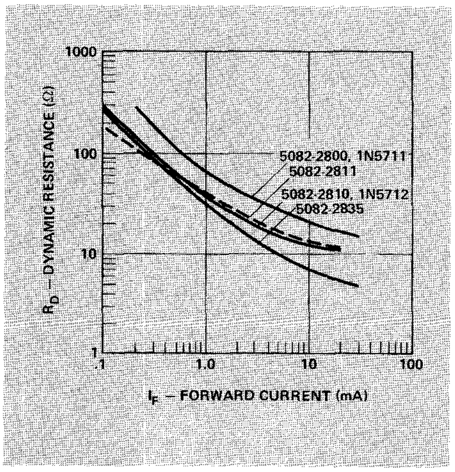


Figure 14. Typical Dynamic Resistance (R_D) vs. Forward Current (I_F).

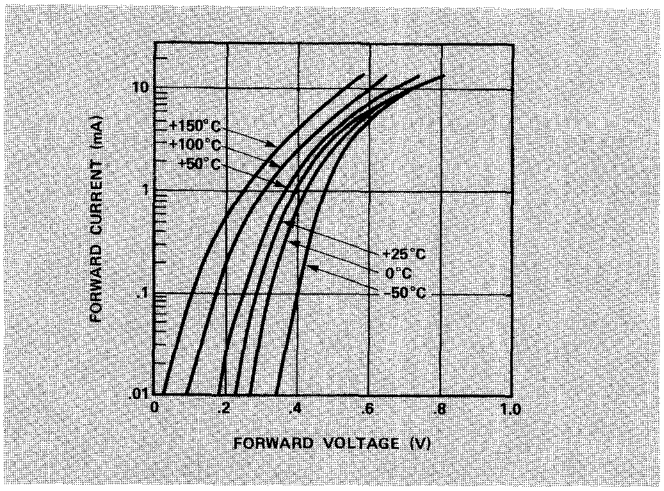


Figure 15. Typical Variation of Forward Current (I_F) vs. Forward Voltage (V_F) at Various Temperatures for the HSCH-1001.

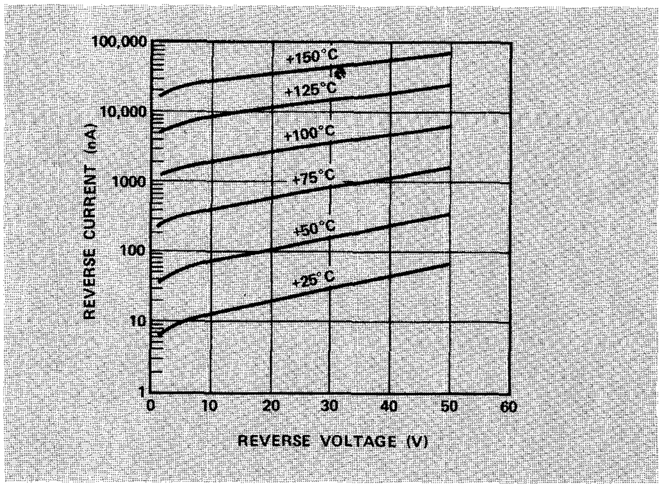


Figure 16. Typical Variation of Reverse Current (I_R) vs. Reverse Voltage (V_R) at Various Temperatures for the HSCH-1001.

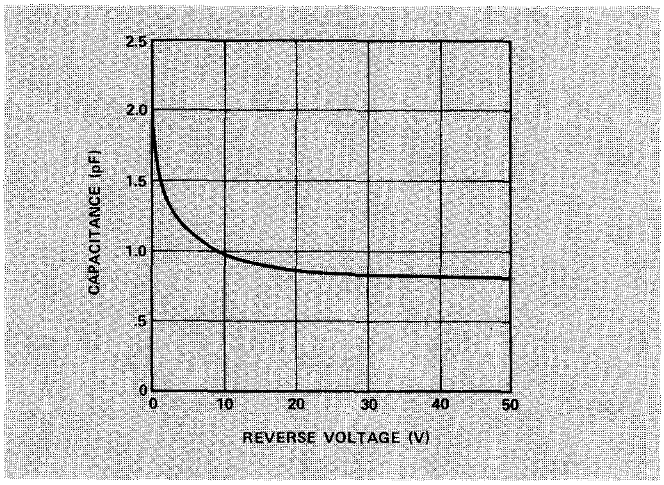


Figure 17. Typical Capacitance (C) vs. Reverse Voltage (V_R) for the HSCH-1001.

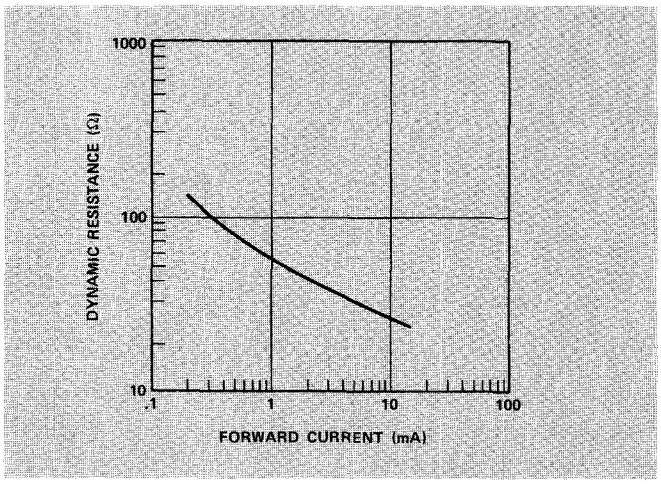


Figure 18. Typical Dynamic Resistance (R_D) vs. Forward Current (I_F) at T_A = 25° C for the HSCH-1001.

Mechanical Specifications

	Outline 15	**Outline 12 (DO-35)**
Lead Material:	Dumet	Dumet
Lead Finish:	2800 Series: Tin 2300, 2900 Series: Gold	Tin
Maximum Soldering Temperature:	230° C for 5 sec.	260° C for 10 sec.
Minimum Lead Strength:	4 lb. Pull	10 lb. Pull
Typical Package Inductance:	2800 Series: 2.0 nH 2300, 2900 Series: 3.0 nH	1.8 nH
Typical Package Capacitance:	2800 Series: 0.2 pF 2300, 2900 Series: 0.07 pF	0.25 pF
	The leads on the Outline 15 package should be restricted so that the bend starts at least 1/16 inch from the glass body.	

HEWLETT PACKARD

COMPONENTS

HIGH CONDUCTANCE DIODES

5082-1001 (1N 4456)
5082-1002 4-32
5082-1003 3-79
5082-1004 3-97
5082-1006 4-97

Features

FAST SWITCHING
LOW CAPACITANCE
HIGH CURRENT CAPABILITY

Description/Applications

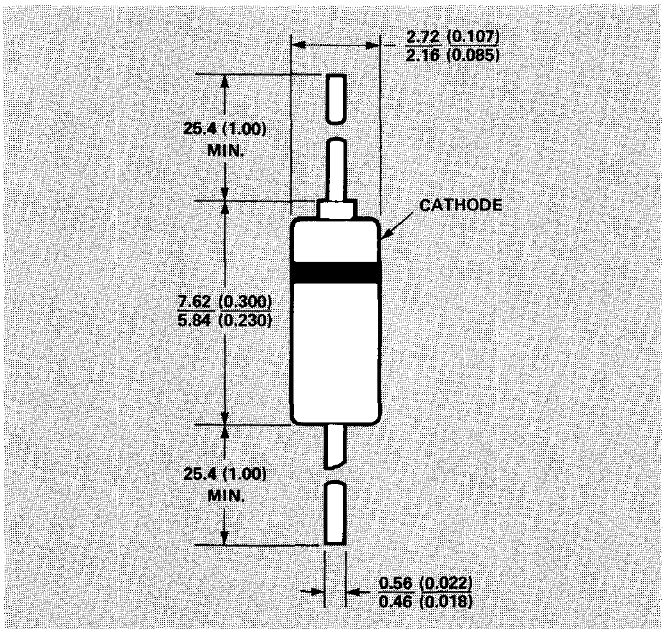
The 5082-1000 series of diodes feature planar silicon epitaxial construction to provide high conductance, low capacitance, and nanosecond turn-on and turn-off. Process control of the diode manufacturing enables specification of effective minority carrier lifetime. Turn-on time and voltage overshoot are minimized in these diodes of low conductivity modulation.

These diodes are ideally suited for applications such as core drivers, pulse generators, input gates or wherever high conductance without loss of speed is required.

Maximum Ratings at $T_{CASE}=25°C$

WIV — Working Inverse Voltage	
1006	40 Volts
1001/1002	30 Volts
1003/1004	20 Volts
I_F (Surge) — Forward Current Surge, 1.0 Second Duration	0.75 Amp
I_F (Surge) — Forward Current Surge, 1.0 Microsecond Duration	7.50 Amp
P_{DISS} — Power Dissipation[1]	500 mW
T_A — Operating Temperature Range	-65° C to +175° C
T_{STG} — Storage Temperature Range	-65° C to +200° C

Operation of these devices within the above temperature ratings will assure a device Mean Time Between Failure (MTBF) of approximately 1 x 10^7 hours.



OUTLINE 11

DIMENSIONS IN MILLIMETERS AND (INCHES)

Mechanical Specifications

The HP Outline 11 package has a glass hermetic seal with dumet leads. The package will meet MIL-STD-750, Method 2036, Condition A (2 lbs. tension for 15 sec.) and E. The maximum soldering temperature is 230°C for 5 seconds. Outline 11 package capacitance and inductance are typically 0.15 pF and 4 nH respectively.

Electrical Specifications at $T_A=25°C$

Part Number 5082-	Minimum Breakdown Voltage V_{BR} (V)	Minimum Forward Current I_F (mA)	Minimum Forward Current I_F (mA)	Maximum Reverse Leakage Current I_R (nA)	Maximum Reverse Leakage Current I_R (µA)	Maximum Total Capacitance C_O (pF)	Maximum Reverse Recovery Time t_{rr} (ns)	Maximum Turn-On Time t_{on} (ns)
1001 (1N4456)	35	150	500	200	200	1.5	1.5	2.5
1002	35	300	800	200	200	3.0	2.0	2.5
1003	25	100	300	200	200	2.0	1.5	2.0
1004	25	200	600	200	200	4.0	2.0	2.0
1006	50	150	500	200	200	1.1	1.5	—
Test Conditions	$I_R=10\mu A$	$V_F=1.0V$ [2]	$V_F=1.4V$ [2]	[3]	150° C[3]	$V_R=0V$, f=1.0 MHz	(Figure 9)	(Figure 10)

NOTES:
1. Mounted on a printed circuit board in still air.
2. Measured at a repetition rate not to exceed the power dissipation.
3. $V_R=35V$ for 1006; $V_R=30V$ for 1001, 1002; $V_R=20V$ for 1003, 1004.
4. Inductance measured at the edge of the glass package seal is typically 4.0 nH for all devices.
5. Rectification Efficiency is typically 65% for all devices (Figure 8).

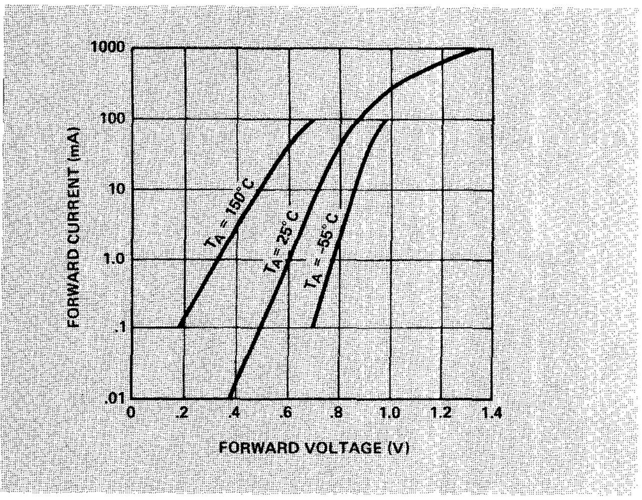


Figure 1. Typical Forward Conduction Characteristics, 5082-1001, 1003, and 1006.

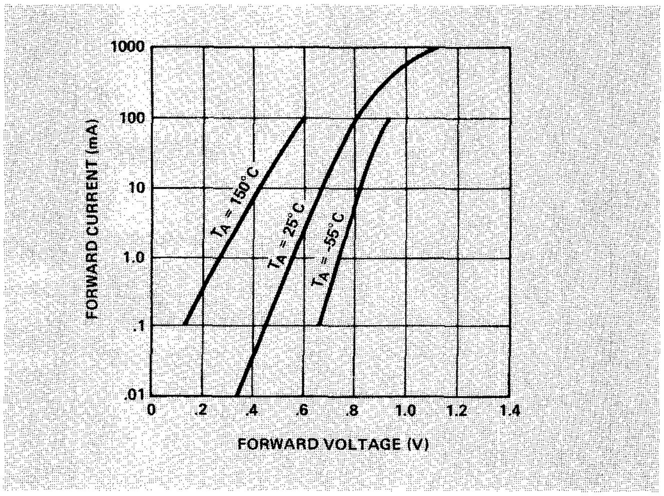


Figure 2. Typical Forward Conduction Characteristics, 5082-1002 and 1004.

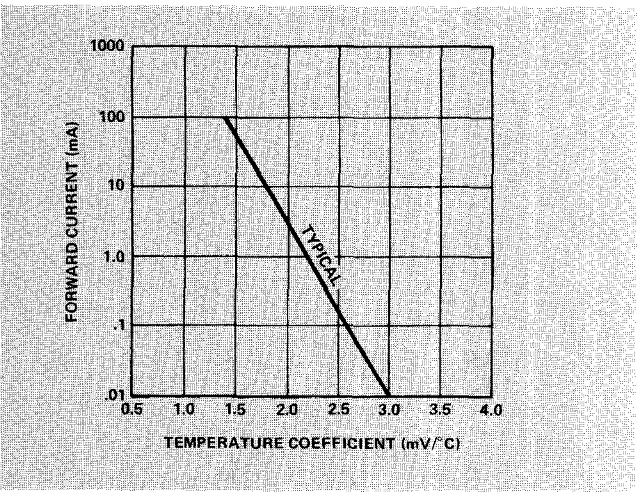


Figure 3. Typical Forward Current Temperature Coefficient.

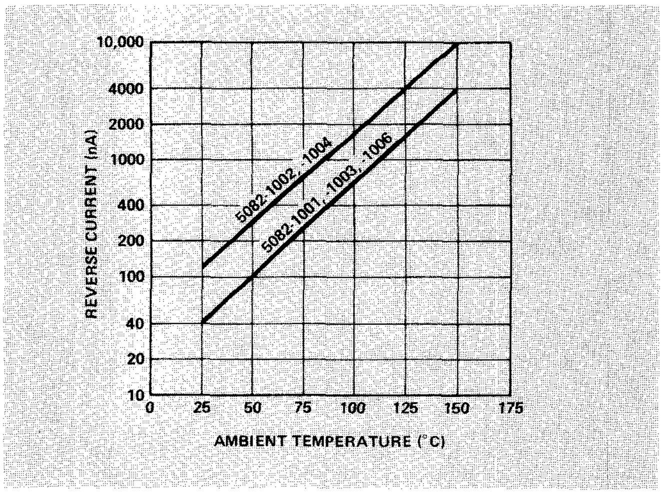


Figure 4. Typical Reverse Current at Specified V_R vs. Increasing Temperature.

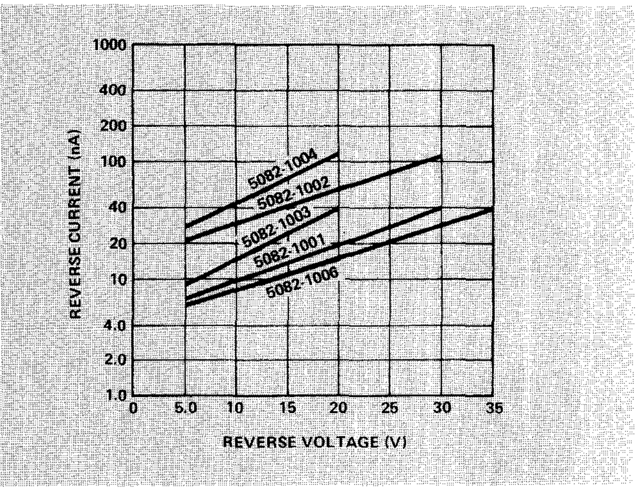


Figure 5. Typical Reverse Current vs. Reverse Voltage.

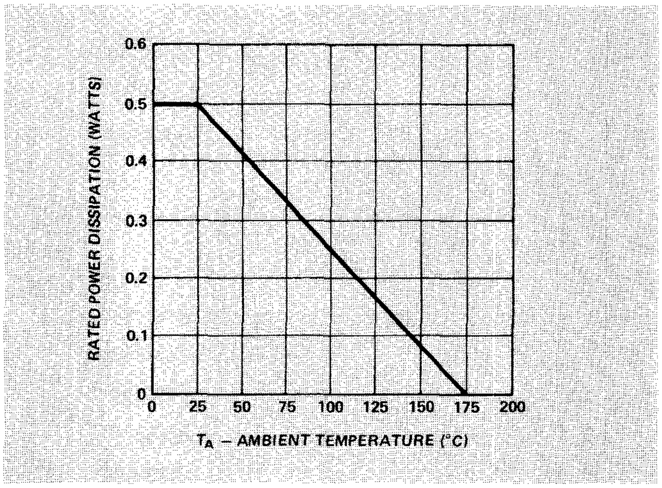


Figure 6. Power Dissipation Derating Characteristics.

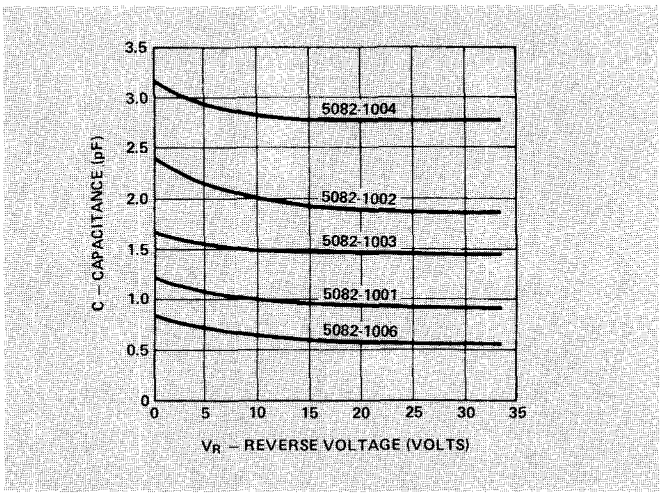


Figure 7. Typical Capacitance vs. Reverse Voltage Characteristics.

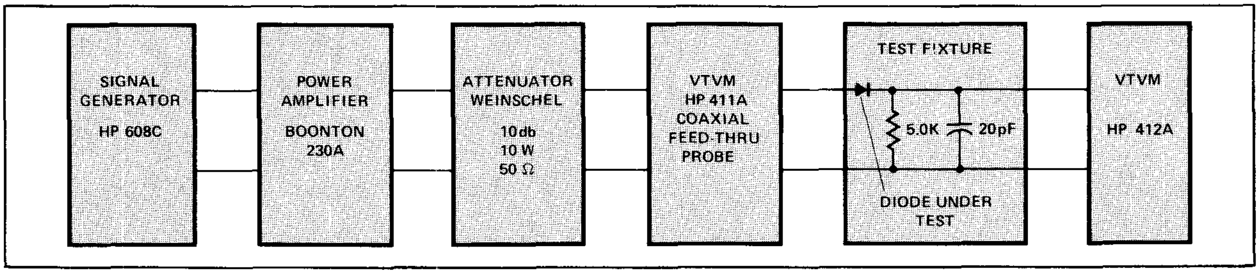


Figure 8. Test Circuit for Measuring the Rectification Efficiency. Signal source is adjusted to 100 MHz and 2V RMS as read on the 411A. The rectification efficiency calculated from the DC output voltage by RE = V_{DC}/2.83 is typically 65% for all devices.

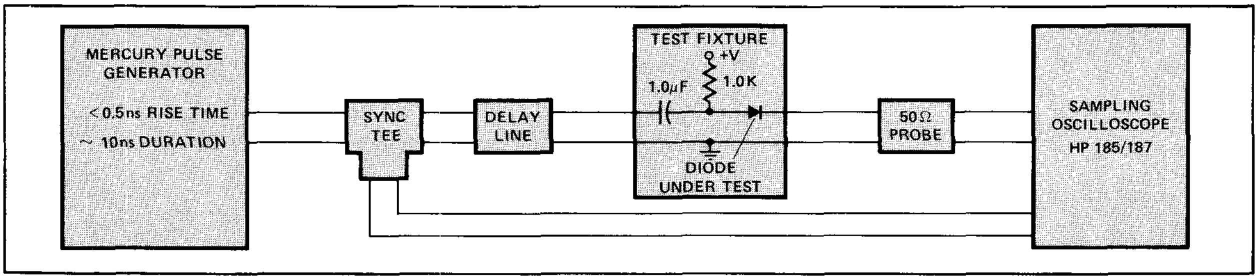


Figure 9. Test Circuit for Measuring Reverse Recovery Time. I_F is set equal to I_R (anywhere from 10 to 400 mA). t_{RR} is measured as the time required to recover to 0.1 I_R as timed from the zero crossover. The observed waveform will be determined more by diode capacitance than by minority carrier storage.

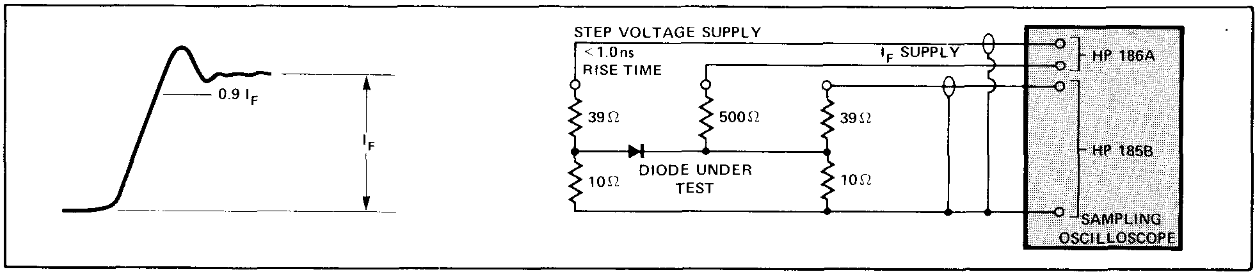


Figure 10. Test Circuit for Measuring Turn-On Time. I_F is adjusted for 10 mA after applying the step voltage. t_{ON} is measured as the time required to reach 0.9 I_F from initial application of the step voltage. For high excitation levels the t_{ON} value is significantly lower than the value specified, i.e., at 100 mA t_{ON} is typically less than 1.0 ns.

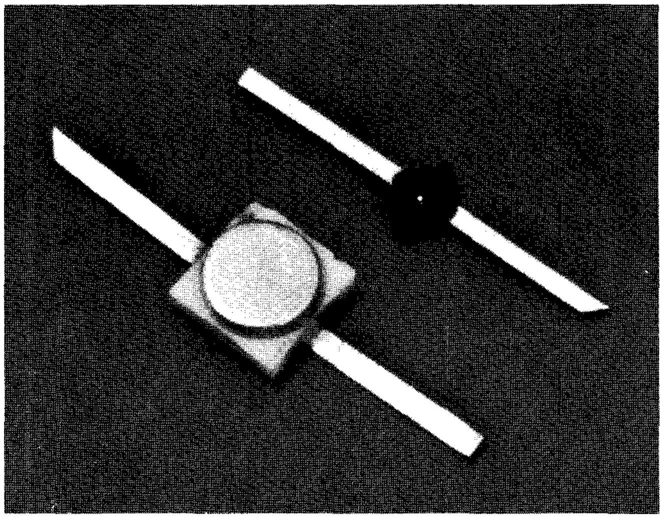
HEWLETT PACKARD
COMPONENTS

SCHOTTKY BARRIER DIODES FOR STRIPLINE, MICROSTRIP MIXERS AND DETECTORS

5082-2200/01/02/03
5082-2207/08/09/10
5082-2765/66
5082-2774/75
5082-2785/86
5082-2794/95

Features

- **SMALL SIZE**
- **LOW NOISE FIGURE**
  6 dB Typical at 9 GHz
- **RUGGED DESIGN**
- **HIGH UNIFORMITY**
- **HIGH BURNOUT RATING**
  1 W RF Pulse Power Incident
- **BOTH MEDIUM AND LOW BARRIER AVAILABLE**



Description/Applications

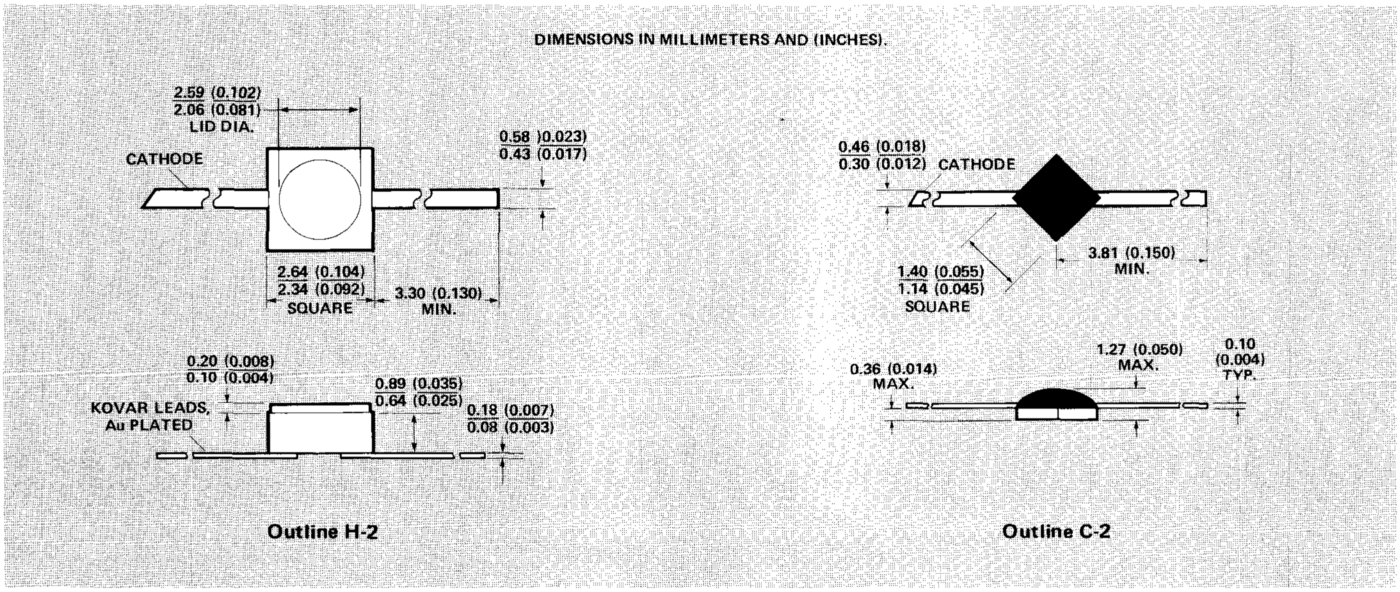
This family consists of medium barrier and low barrier beam lead diodes mounted in easily handled carrier packages. Low barrier diodes provide optimum noise figure at low local oscillator drive levels. Medium barrier diodes provide a wider dynamic range for lower distortion mixer designs. The family provides a range of both dc and rf specified diodes. Application Note 940 gives recommended handling and bonding techniques. Application Note 963 presents impedance matching techniques for mixer and detector circuits.

Mechanical Specifications

The HP outlines C2 and H2 are designed for microstrip and stripline use. The leads provide good continuity of transmission line impedance to the diode. Outline C2 is a plastic on ceramic package. Outline H2 has a metal ceramic hermetic seal. The ceramic is alumina. Metal parts are gold plated kovar.

The hermetic package, outline H2, is capable of passing many of the environmental tests of MIL-STD-750. The applicable solderability test is reference 2031.1: 260° C, 10 seconds.

Package Dimensions



RF Electrical Specifications at $T_A = 25°C$

Part Number 5082-	Batch Matched 5082-	Recommended Frequency	Barrier	Maximum Noise Figure NF (dB)	IF Impedance Z_{IF} (Ω) Min.	Max.	Maximum SWR	Package	Typical Capacitance C_T (pF)
17-61 2200	2201	38-75 1-12 GHz	Medium	6.0	200	400	1.5:1	H-2	.3
14-75 2202	2203	32-29	Medium	6.5	200	400	2.0:1		
17.65 2765	2766	38-75	Low	6.0	100	250	1.5:1		
14.75 2785	2786	32.29	Low	6.5	100	250	2.0:1		
12.11 2207	2208	26.64 1-18 GHz	Medium	6.0	250	500	1.5:1	C-2	.22
9.63 2209	2210	21.18	Medium	6.5	250	500	2.0:1		
12.11 2774	2775	26.84	Low	6.0	200	400	1.5:1		
9.63 2794	2795	21.18	Low	6.5	200	400	2.0:1		
Test Conditions	ΔNF≤0.3dB $\Delta Z_{IF} \leq 25\Omega$	L.O. Test Frequency 9.375 GHz	DC Load Resistance = 0Ω L.O. Power = 1 mW IF = 30 MHz, 1.5 dB NF						V = 0

Typical Detector Parameters

Parameter	Symbol	Typical Value	Units	Test Conditions
Tangential Sensitivity	TSS	-54	dBm	20 μA Bias
Voltage Sensitivity	γ	6.6	mV/μW	Video Bandwidth = 2 MHz R_L = 100KΩ
Video Resistance	R_V	1400	Ω	f = 10 GHz

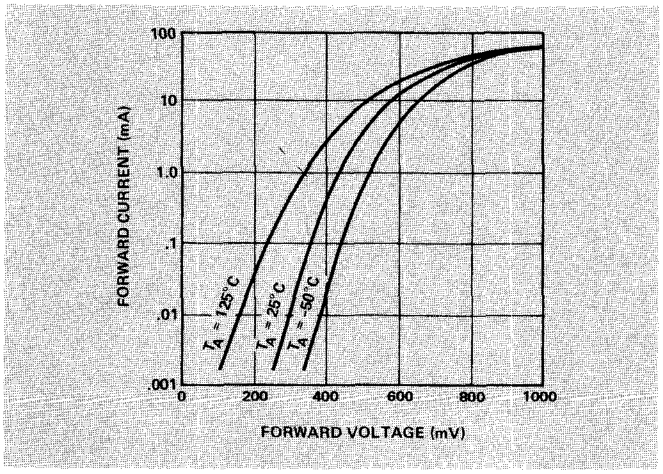


Figure 1. Typical Forward Characteristics, 5082-2200, -2207.

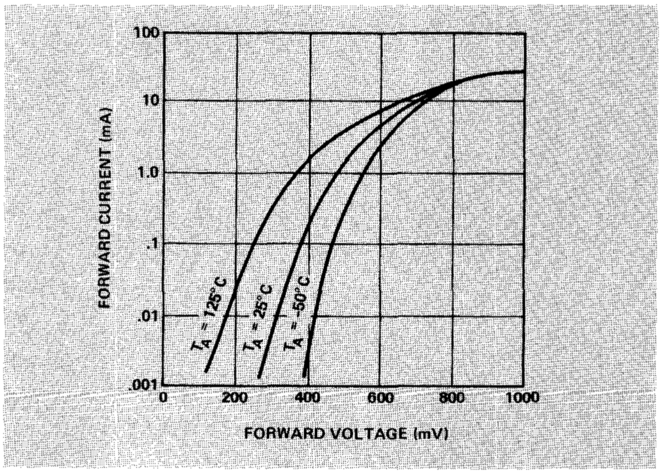


Figure 2. Typical Forward Characteristics, 5082-2202, -2209.

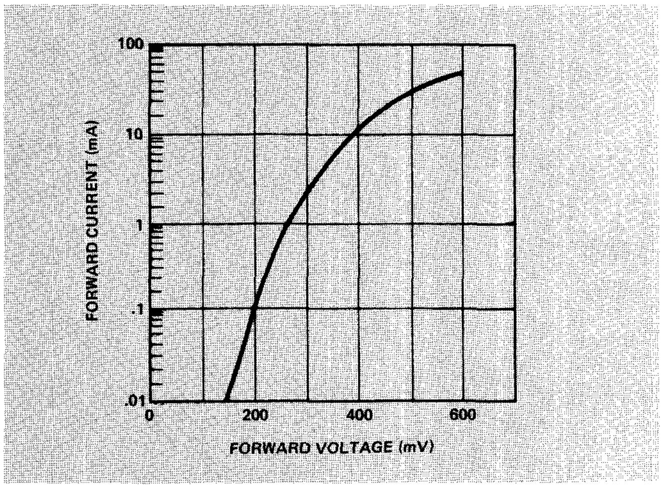


Figure 3. Typical Forward Characteristics, 5082-2765, -2774 at T_A = 25° C.

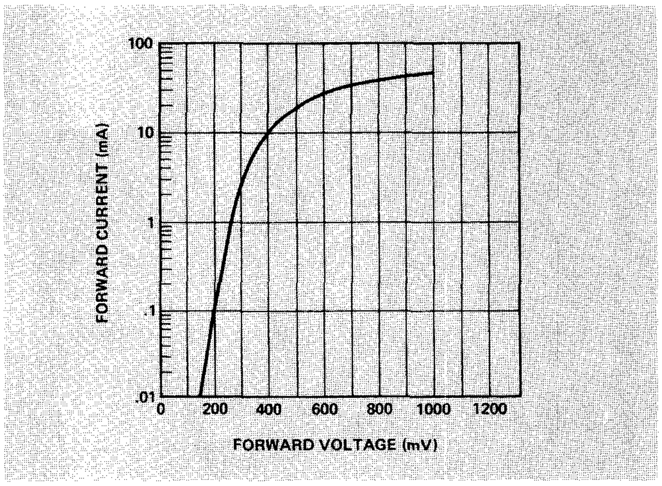


Figure 4. Typical Forward Characteristics, 5082-2785 -2794 at T_A = 25° C.

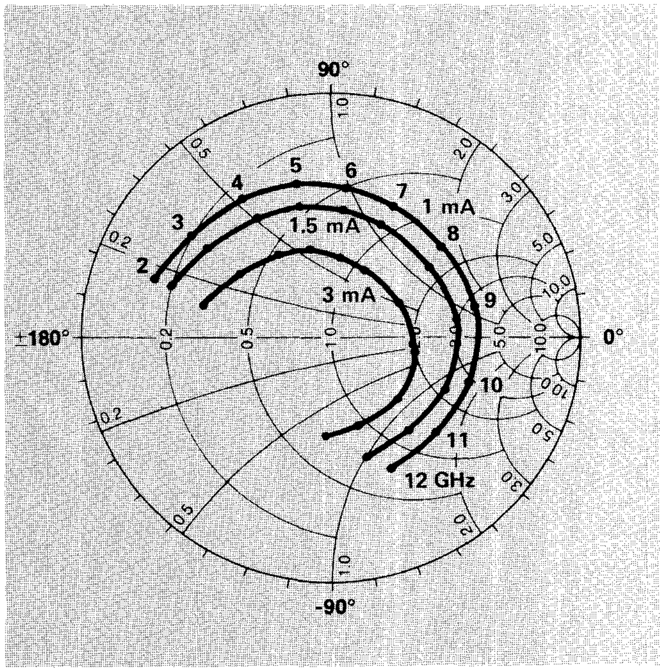


Figure 5. Typical Admittance Characteristics, 5082-2200 with self bias.

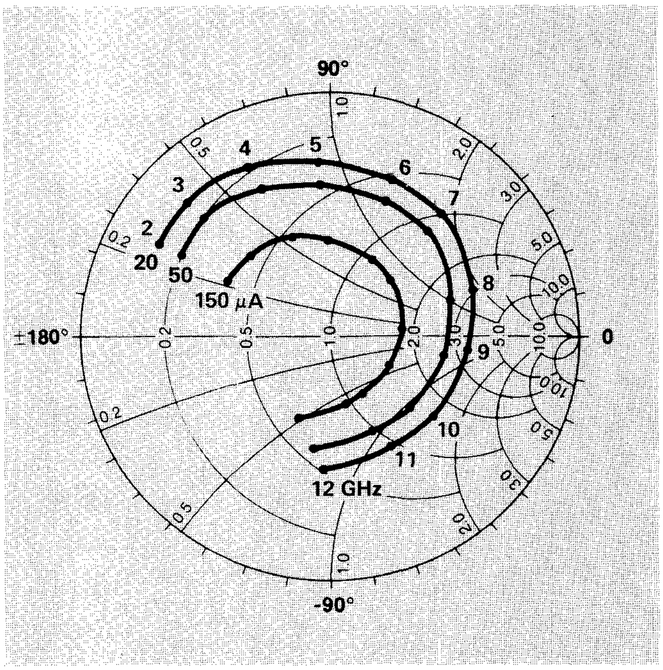


Figure 6. Typical Admittance Characteristics, 5082-2200 with external bias.

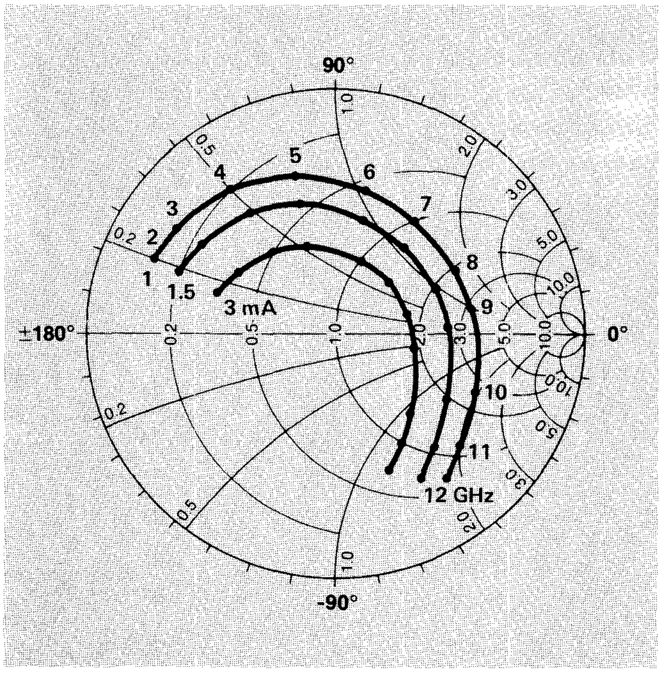


Figure 7. Typical Admittance Characteristics, 5082-2202 with self bias.

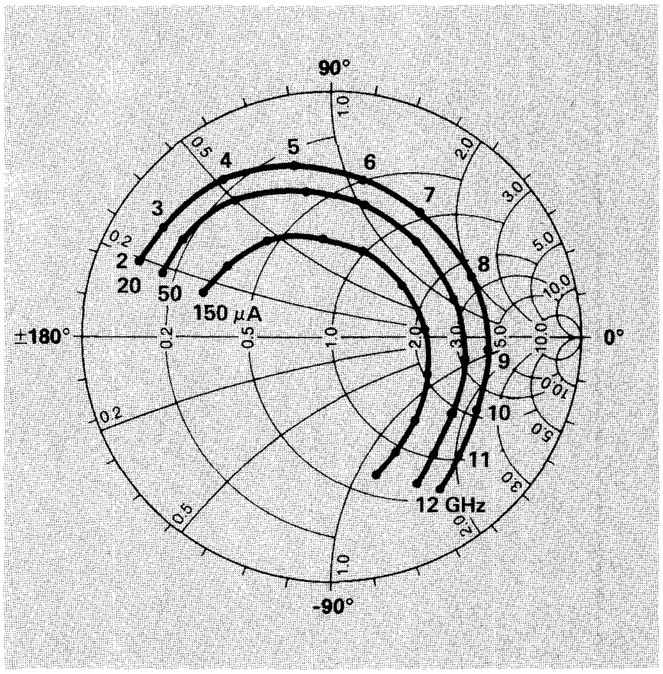


Figure 8. Typical Admittance Characteristics, 5082-2202 with external bias.

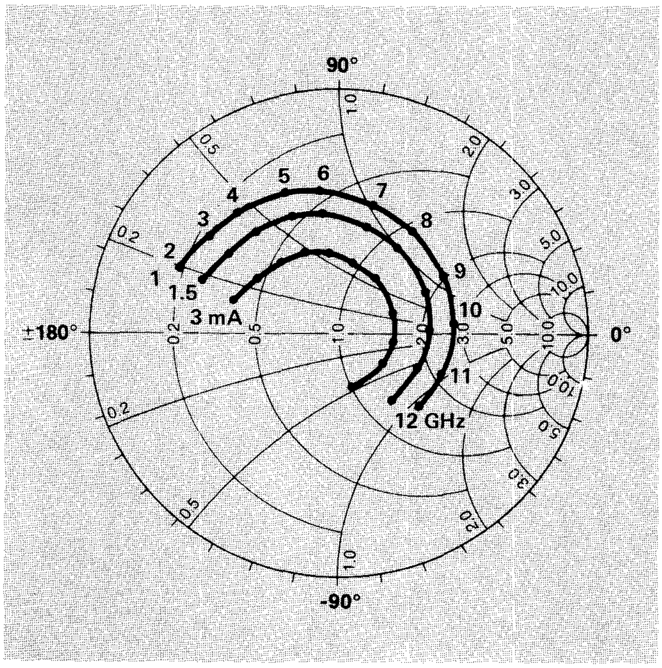


Figure 9. Typical Admittance Characteristics, 5082-2765 with self bias.

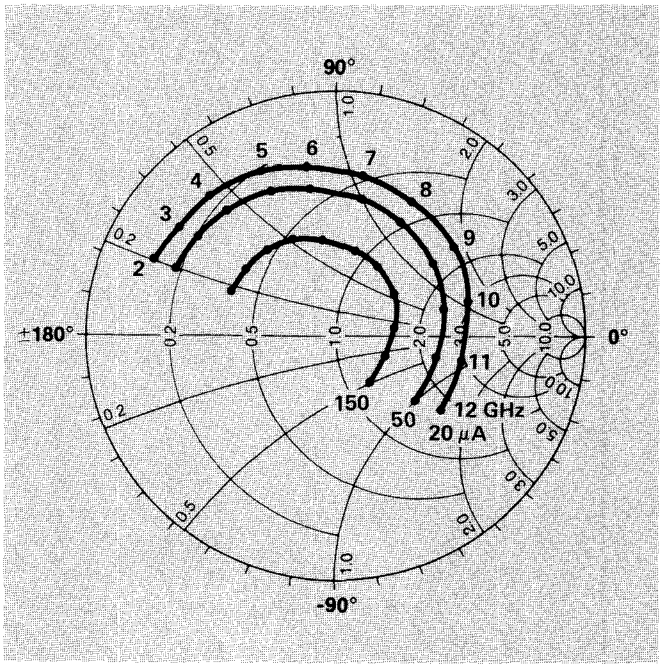


Figure 10. Typical Admittance Characteristics, 5082-2765 with external bias.

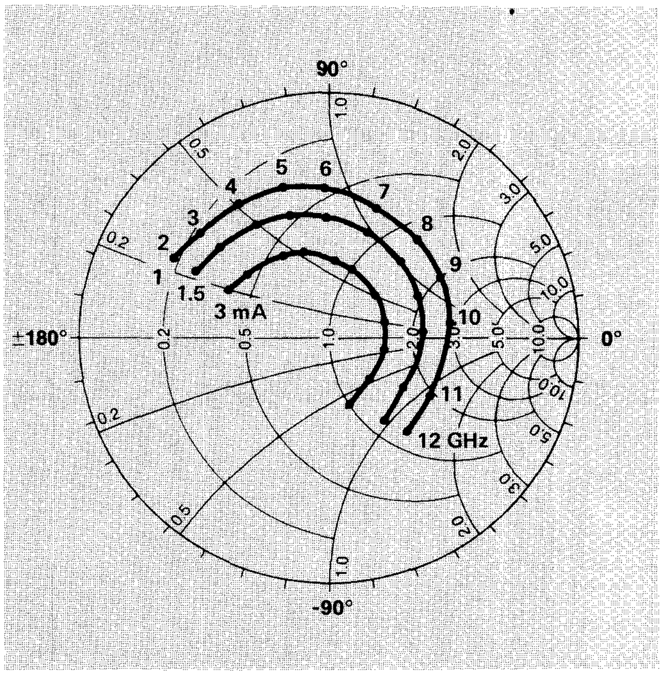


Figure 11. Typical Admittance Characteristics, 5082-2785 with self bias.

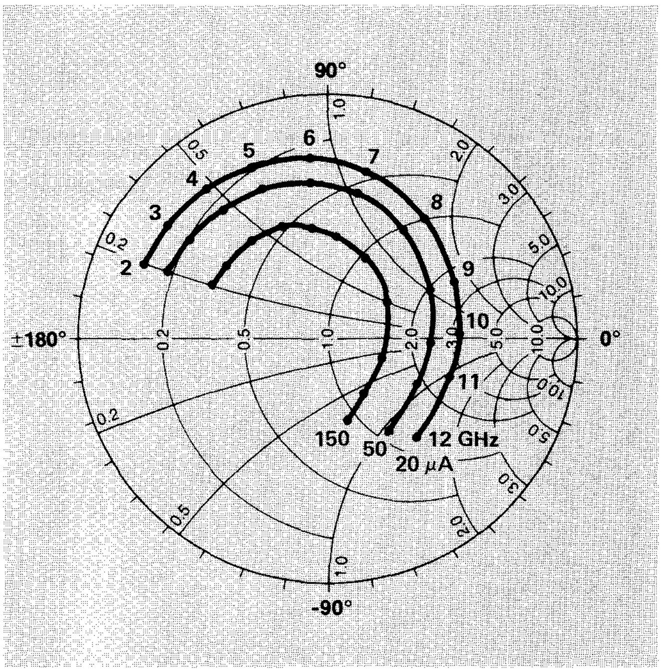


Figure 12. Typical Admittance Characteristics, 5082-2785 with external bias.

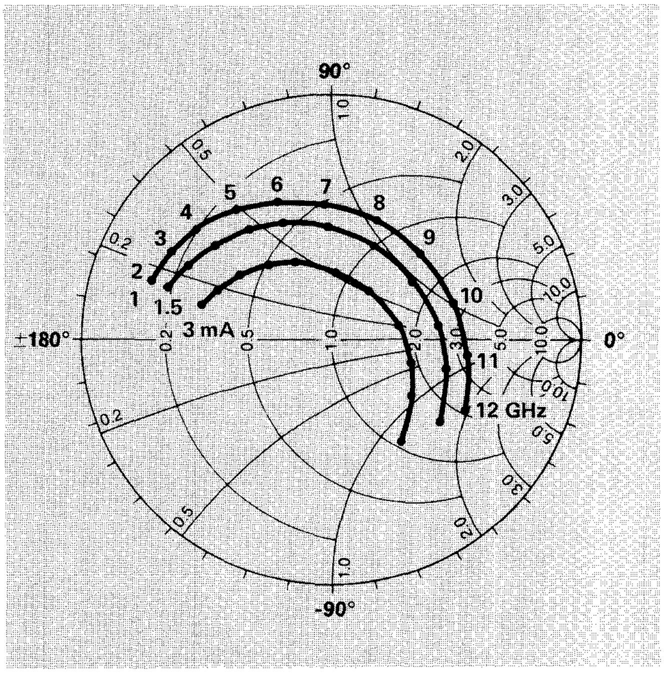


Figure 13. Typical Admittance Characteristics, 5082-2207 with self bias.

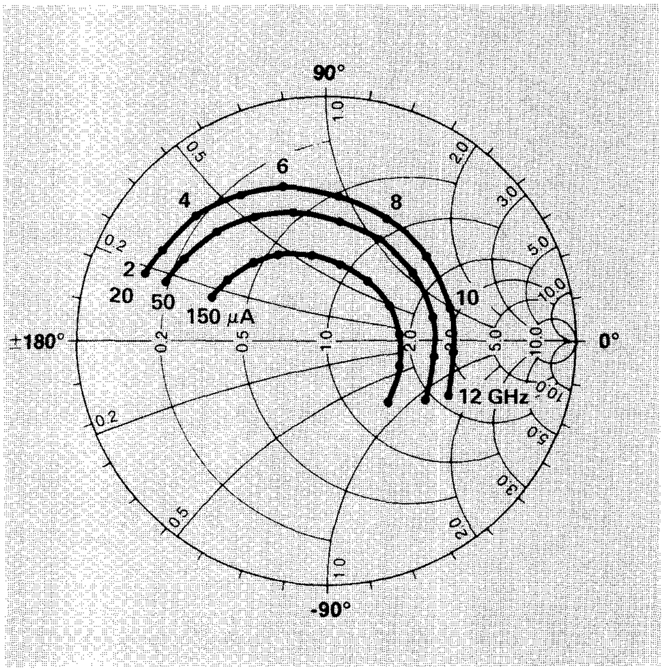


Figure 14. Typical Admittance Characteristics, 5082-2207 with external bias.

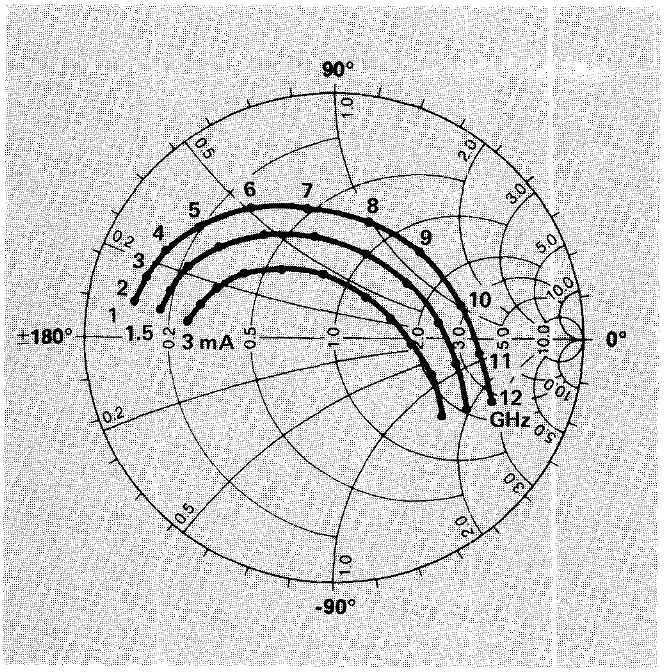


Figure 15. Typical Admittance Characteristics, 5082-2209 with self bias.

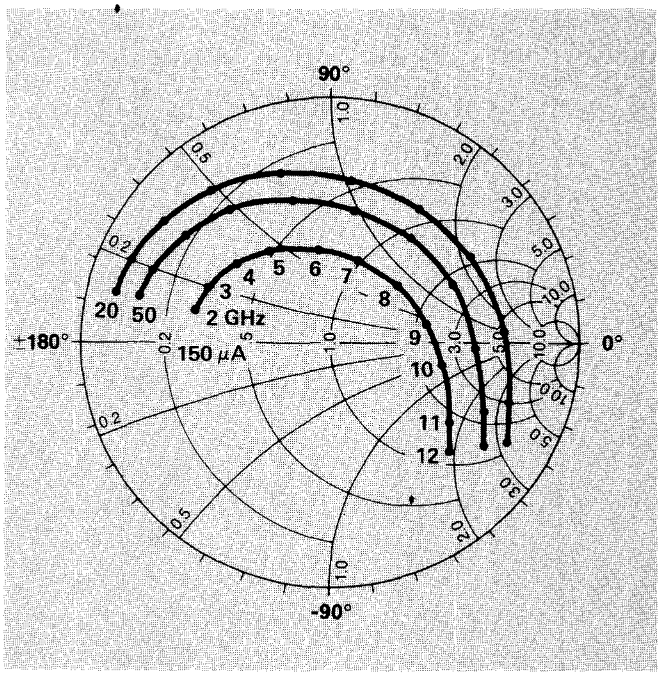


Figure 16. Typical Admittance Characteristics, 5082-2209 with external bias.

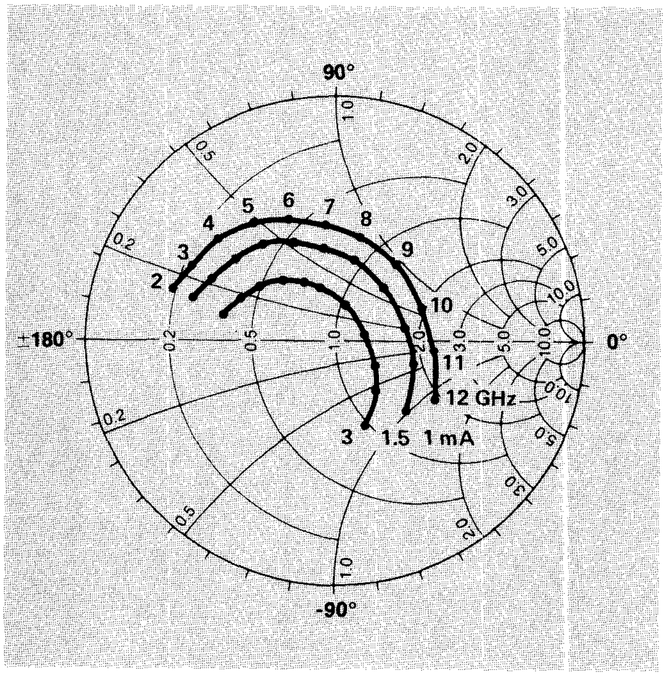


Figure 17. Typical Admittance Characteristics, 5082-2774 with self bias.

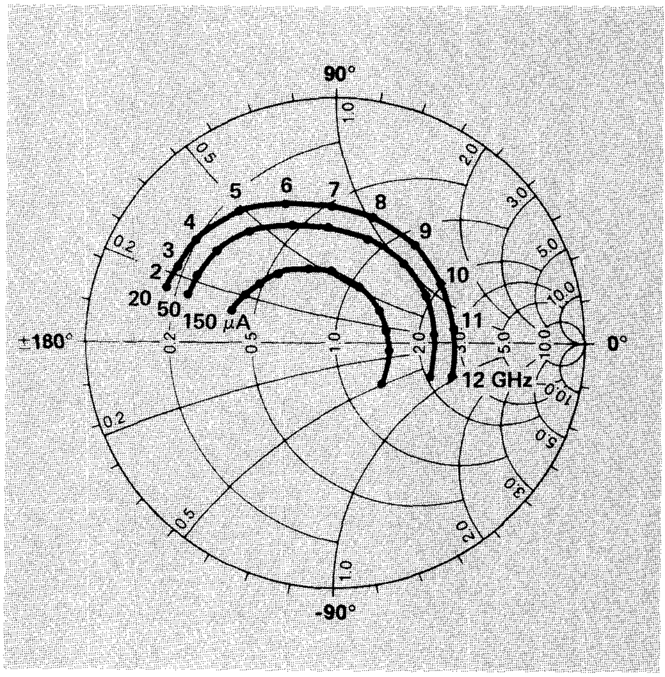


Figure 18. Typical Admittance Characteristics, 5082-2774 with external bias.

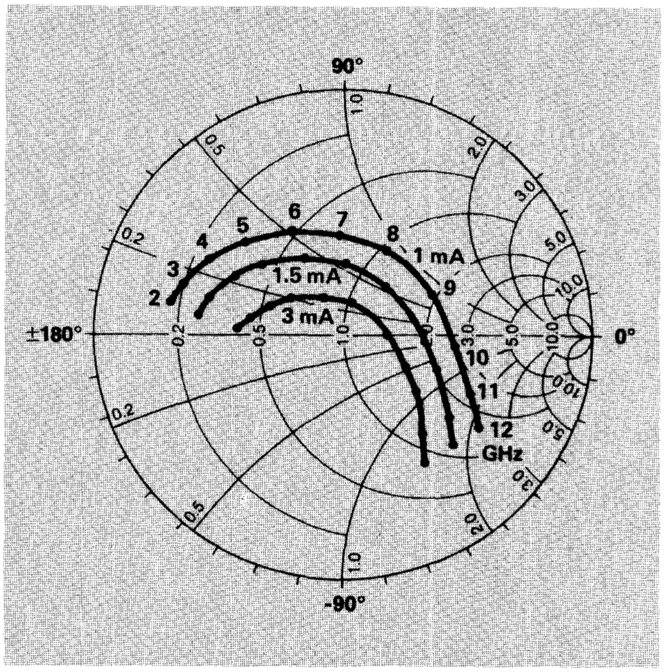


Figure 19. Typical Admittance Characteristics, 5082-2794 with self bias.

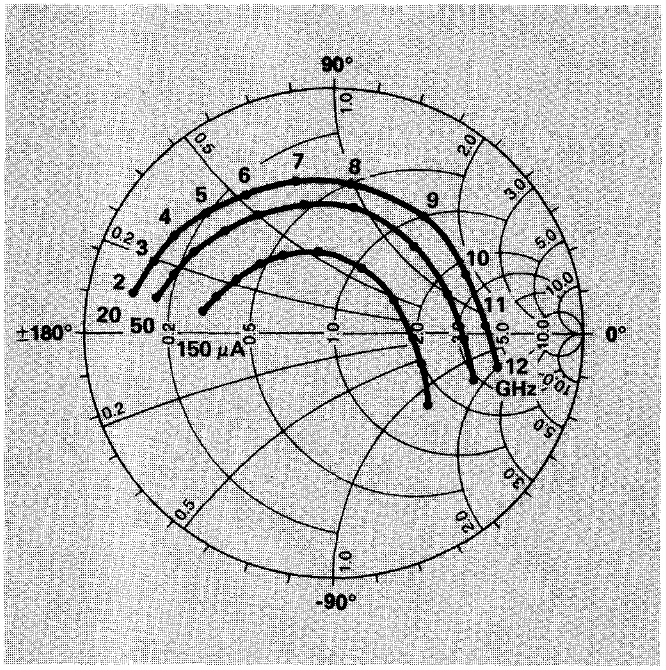


Figure 20. Typical Admittance Characteristics, 5082-2794 with external bias.

Maximum Ratings at T_{CASE}=25°C

Pulse Power Incident .... 1 W
(1 µs pulse, Du = .001 for 1 minute)

CW Power Dissipation
(Mounted in infinite Heat Sink) .... 125 mW
(Derate linearly to Zero at Maximum Operating Temperature)

Junction Operating and Storage Temperature Range
C-2 Packaged Diodes .... -65°C to +125°C
H-2 Packaged Diodes .... -65°C to +150°C

Operation of these devices within the above temperature ratings will assure a device Mean Time Between Failure (MTBF) of approximately 1 x 10^7 hours.

Diode Mounting Temperature
C-2 and H-2 Packaged
Diodes .... 235°C for 10 sec. max.

Peak Inverse Voltage .... 3 V

These diodes are pulse sensitive. Handle with care to avoid static discharge through the diode.

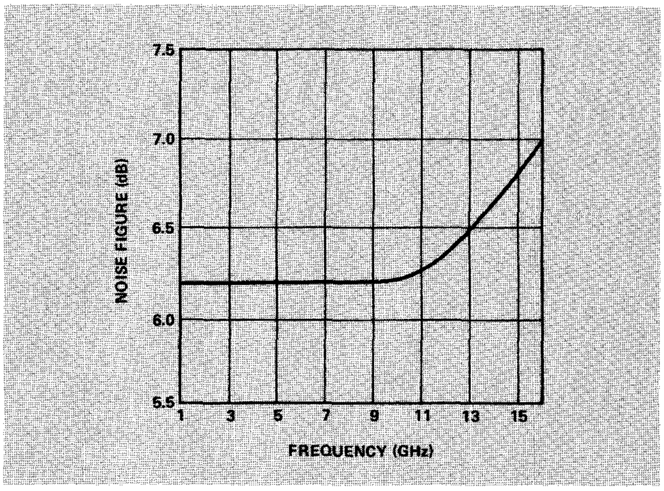
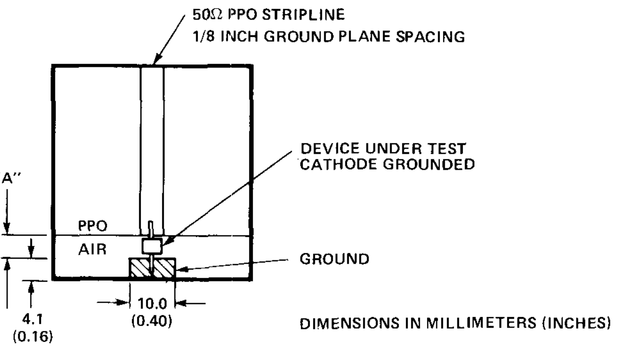


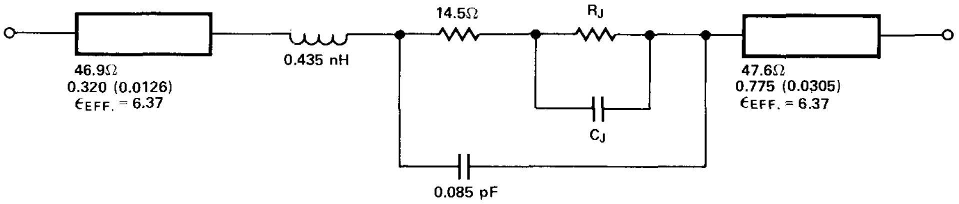
Figure 21. Typical Noise Figure vs. Frequency for 5082-2202, -2209, -2785, -2794



PACKAGE	DIMENSION "A"
C-2	1.91 ± 0.05 (0.075 ± 0.002)
H-2	2.67 ± 0.05 (0.105 ± 0.002)

Figure 22. Admittance Test Circuit for C2 and H2 Diodes.

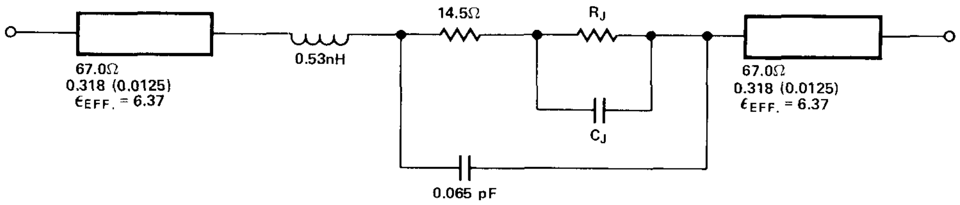
MODEL FOR H2 DIODES



DIMENSIONS IN MILLIMETERS (INCHES)

Parameter	Symbol	1 mA Rect. Current		20 μA Ext. Bias		Units
		5082-2200	5082-2765	5082-2200	5082-2765	
Junction Resistance	R_J	258	290	545	495	Ohms
Junction Capacitance	C_J	0.255	0.189	0.302	0.173	pF

MODEL FOR C-2 DIODES



DIMENSIONS IN MILLIMETERS (INCHES)

Parameter	Symbol	1 mA Rect. Current		20 μA Ext. Bias		Units
		5082-2207	5082-2774	5082-2207	5082-2774	
Junction Resistance	R_J	338	255	421	340	Ohms
Junction Capacitance	C_J	0.189	0.180	0.195	0.168	pF

HEWLETT hp PACKARD
COMPONENTS

SCHOTTKY BARRIER DIODE QUADS FOR DOUBLE BALANCED MIXERS

5082-2231/33
5082-2261/63
5082-2271/72
5082-2276/77
5082-2279/80
5082-2291/92
5082-2293/94
5082-2830/31

Features

SMALL SIZE
Eases Broad Band Designs

TIGHT MATCH
Improves Mixer Balance

IMPROVED BALANCE OVER TEMPERATURE

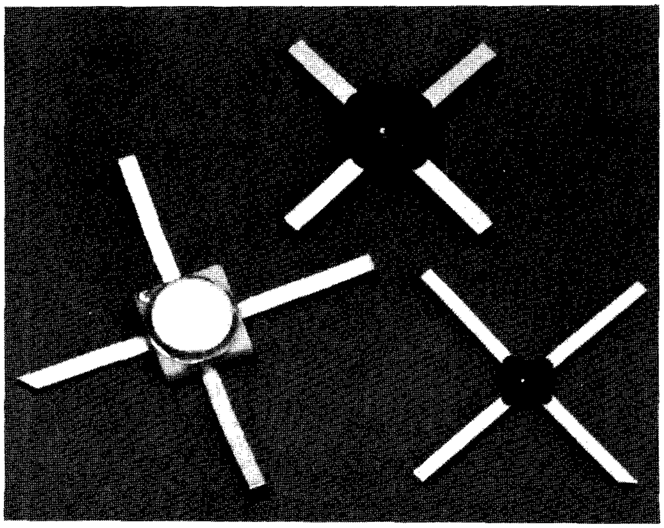
RUGGED DESIGN

BOTH MEDIUM AND LOW BARRIER DIODES AVAILABLE

Description / Applications

These matched diode quads use a monolithic array of Schottky diodes interconnected in ring configuration. The relative proximity of the diode junction on the wafer assures uniform electrical characteristics and temperature tracking.

These diodes are designed for use in double balanced mixers, phase detectors, AM modulators, and pulse modulators requiring wideband operation and small size. The low barrier diodes allow for optimum mixer noise figure at lower than conventional local oscillator levels. The wider dynamic range of the medium barrier diodes allows for better distortion performance.



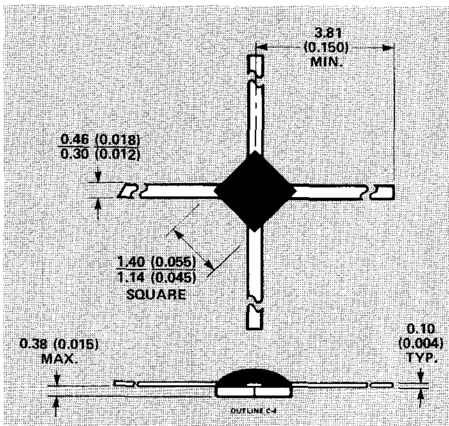
Maximum Ratings at $T_{CASE}=25°C$

Junction Operating and Storage Temperature Range:
H-4 Packaged Diodes .... -65°C to +150°C
E-1 and C-4 Packaged Diodes .... -65°C to +125°C

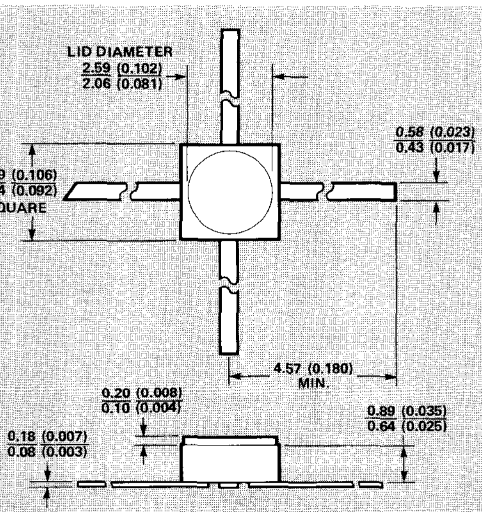
Operation of these devices within the above temperature ratings will assure a device Mean Time Between Failure (MTBF) of approximately 1 x 10^7 hours.

DC Power Dissipation .... 75 mW per Junction
Derate linearly to zero at maximum rated temperature. (Measured in infinite heat sink.)
Soldering Temperature .... 220°C for 10 s.

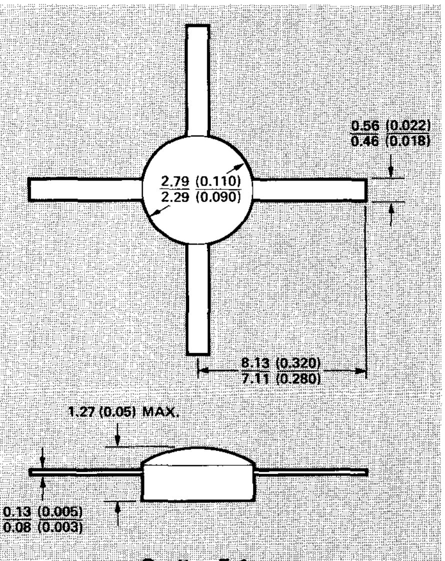
Package Dimensions



Outline C-4



Outline H-4



Outline E-1

DIMENSIONS IN MILLIMETERS AND (INCHES).

Selection Guide

Frequency / Package Outline	Barrier	To 2 GHz	2-4 GHz	4-8 GHz	8-12 GHz	12-18 GHz
E-1	Medium	5082-2830	5082-2276	5082-2277		
Low Cost	Low	5082-2831				
H-4	Medium	5082-2261	5082-2261	5082-2263		
Hermetic	Low	5082-2231	5082-2231	5082-2233		
C-4	Medium	5082-2291	5082-2291	5082-2292	5082-2293	5082-2294
Broadband	Low	5082-2271	5082-2271	5082-2272	5082-2279	5082-2280

Electrical Characteristics at $T_A=25°C$

	Part Number 5082-	Package	Barrier	Maximum Capacitance C_T (pF)	Maximum Capacitance Difference ΔC_T (pF)
.42	2231	H-4 √	Low	0.60	0.10
3.84	2233			0.50	0.05
.42	2261		Medium	0.60	0.10
.84	2263			0.45	0.05
.25	2830	E-1		0.5 (Typ.)	0.20
.25	2831		Low	0.5 (Typ.)	0.20
.74	2276		Medium	0.60	0.10
.51	2277			0.50	0.10
.21	2271	C-4	Low	0.60	0.10
.42	2272			0.45	0.10
.63	2279			0.25	0.05
3.84	2280			0.20	0.05
.21	2291		Medium	0.60	0.10
.42	2292			0.40	0.10
.63	2293			0.25	0.05
3.84	2294			0.20	0.05
	Test Conditions			$V_R=0$ f=1 MHz[1]	

Typical Parameters

Forward Voltage V_F (V)[2]	Dynamic Resistance R_D (Ω)
0.25	11
0.30	13
0.35	13
0.45	13
0.35	10
0.25	10
0.35	13
0.35	16
0.25	11
0.25	13
0.30	15
0.30	15
0.35	11
0.35	13
0.45	15
0.45	15
I_F=1mA Measured between Adjacent Leads	I_F=5mA between Adjacent Leads

Notes:
1. Measured between diagonal leads.
2. Maximum ΔV_F = 20 mV at I_F = 5mA measured between adjacent leads.

Dynamic and Series Resistance

Schottky diode resistance may be expressed as series resistance, R_S, or as dynamic resistance, R_D. The two terms are related by the equation

$$R_D = R_S + R_j$$

where R_j is the resistance of the junction. Junction resistance of a diode with DC bias is quite accurately calculated by

$$R_j = 26/I_B \quad \text{where}$$

I_B is the bias current in milliamperes. The series resistance is independent of current.

The dynamic resistance is more easily measured. If series resistance is specified it is usually obtained by subtracting the calculated junction resistance from the measured dynamic resistance.

HEWLETT hp PACKARD
COMPONENTS

SCHOTTKY BARRIER DIODES FOR MIXERS AND DETECTORS

5082-2273/74
5082-2285-88/95-98
5082-2350/51
5082-2400/01
5082-2520/21/65/66
5082-2701/02/06/07
5082-2711-14/21-24
5082-2817/18

Features

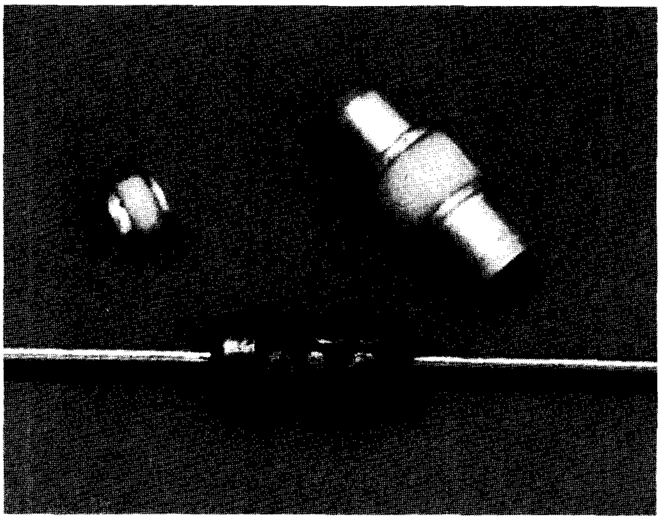
LOW AND STABLE NOISE FIGURE

HIGH BURNOUT RATING
15 W RF Pulse Power Incident

RUGGED DESIGN

HIGH UNIFORMITY

BOTH MEDIUM AND LOW BARRIER DIODES AVAILABLE



Description / Applications

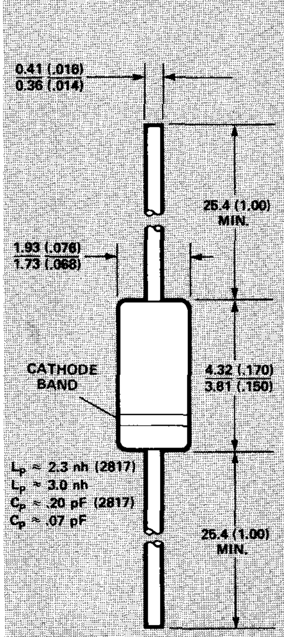
These Schottky diodes are optimized for use in broad band and narrow band microstrip, coaxial, or waveguide mixer assemblies operating to 18 GHz. The low barrier diodes give optimum noise figure performance at low local oscillator drive levels. Medium barrier diodes provide a wider dynamic range for lower distortion mixer designs. The 5082-2350, -2400, -2520 and -2565 have extremely low 1/f noise, making them ideal for use as Doppler mixers.

Maximum Ratings at $T_{CASE} = 25°C$

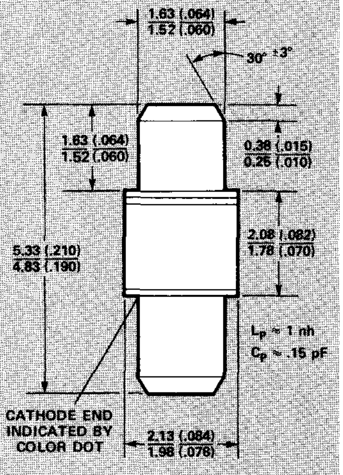
Junction Operating and Storage Temperature Range	
5082-2400, 2401, 2565, 2566, 2350, 2351, 2520, 2521	-60°C to +125°C
All other diodes	-60°C to +150°C
Operation of these devices within the above temperature ratings will assure a device Mean Time Between Failure (MTBF) of approximately 1 x 10^7 hours.	
CW Power Dissipation	200 mW
Derate linearly to 0 W at max. rated temperature (Measured in an infinite heat sink).	
Pulse Power Dissipation	
Peak power absorbed by the diode. 1 µs pulse, Du = .001	
5082-2400, 2350	15W
5082-2565, 2520	4W
All other diodes	1W
Soldering Temperature	230°C for 5 sec.

Note: The 5082-2200 and -2700 series are pulse sensitive. Handle with care to avoid static discharge through the diode.

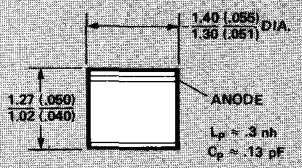
Package Dimensions



Outline 15



Outline 49



DIMENSIONS IN MILLIMETERS AND (INCHES).

Outline 44

Electrical Specifications at $T_A = 25°C$

	Part Number 5082-	Matched Pair 5082-	Barrier	LO Test Frequency (GHz)	Maximum SSB Noise Figure NF (dB)	IF Impedance Z_{IF} (Ω) Min.	IF Impedance Z_{IF} (Ω) Max.	Maximum SWR	Package Outline
1.15	2817	2818	Medium	2.0	6.0	250	400	1.5:1	15
16.15	2400	2401	Medium	2.0	6.0	150	250	1.3:1	
11.80	2350	2351	Medium	2.0	7.0	150	250	1.5:1	
7.35	2565	2566	Medium	3.0	6.0	100	250	1.5:1	
6.83	2520	2521	Medium	3.0	7.0	100	250	1.5:1	
19.87	2713	2714	Medium	9.375	6.0	200	400	1.5:1	49
14.38	2711	2712	Medium	9.375	6.5	200	400	2.0:1	
19.87	2285	2286	Low	9.375	6.0	100	250	1.5:1	
14.38	2287	2288	Low	9.375	6.5	100	250	2.0:1	
34.16	2701	2706	Medium	9.375	6.0	200	400	1.5:1	44
23.60	2702	2707	Medium	9.375	6.5	200	400	1.5:1	
33.53	2295	2296	Low	9.375	6.0	100	250	1.5:1	
23.60	2297	2298	Low	9.375	6.5	100	250	2.0:1	
27.63	2723	2724	Medium	16	6.5	200	400	1.5:1	49
17.64	2721	2722	Medium	16	7.0	200	400	2.0:1	
39.03	2273	2274	Medium	16	6.5	200	400	2.0:1	44
	Test Conditions	$\Delta NF \leq 0.3dB$ $\Delta Z_{IF} \leq 25\Omega$		LO Power = 1 mW IF=30 MHz, 1.5 dB NF Zero DC Load Resistance (100Ω for 5082-2817)		Same as for NF except IF = 10 KHz		Same as for NF	

Typical Parameters

Junction Capacitance C_{JO} (pF)	Breakdown Voltage V_{BR} (V)
1.0	15
0.7	30
0.9	30
0.5	5
0.7	5
.15	3
.15	3
.12	3
.12	3
V = 0	$I_R < 10\mu A$

Typical Parameters

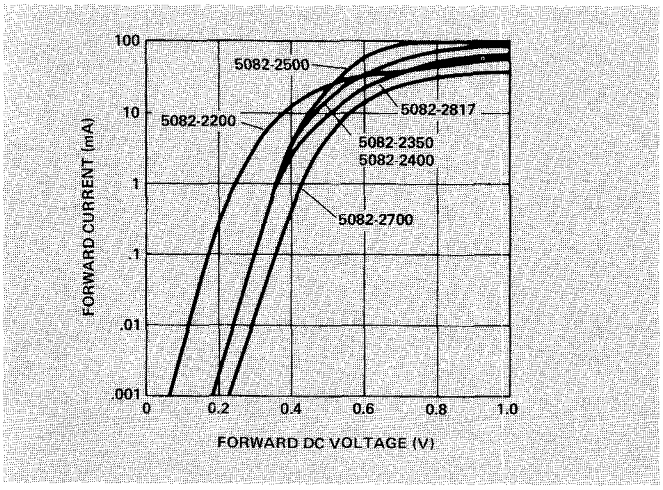


Figure 1. Typical Forward Characteristics at $T_A = 25°C$.

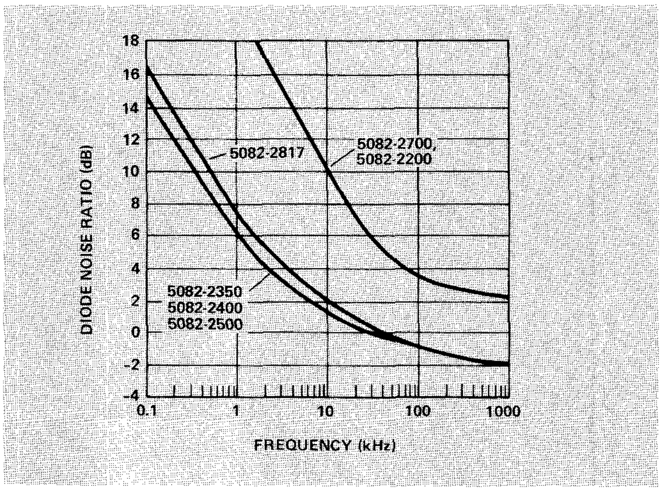


Figure 2. Typical Diode Noise Ratio vs. Frequency at 1 mA Current.

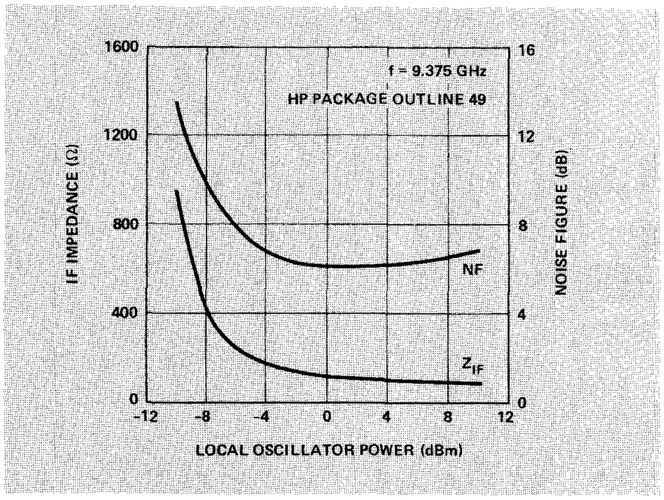


Figure 3. Typical Noise Figure and IF Impedance vs. Local Oscillator Power, 5082-2285 through -2288. Diode unmatched in 50Ω line.

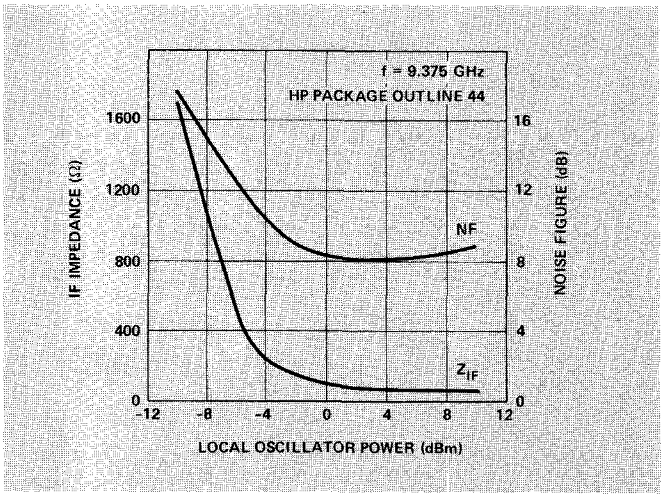


Figure 4. Typical Noise Figure and IF Impedance vs. Local Oscillator Power, 5082-2295 through -2298. Diode unmatched in 50Ω line.

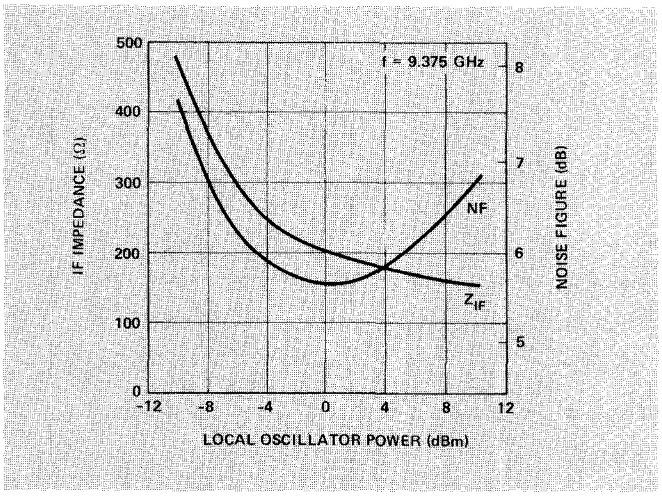


Figure 5. Typical Noise Figure and IF Impedance vs. Local Oscillator Power. Diode matched at each local oscillator power level (5082-2285, 2295).

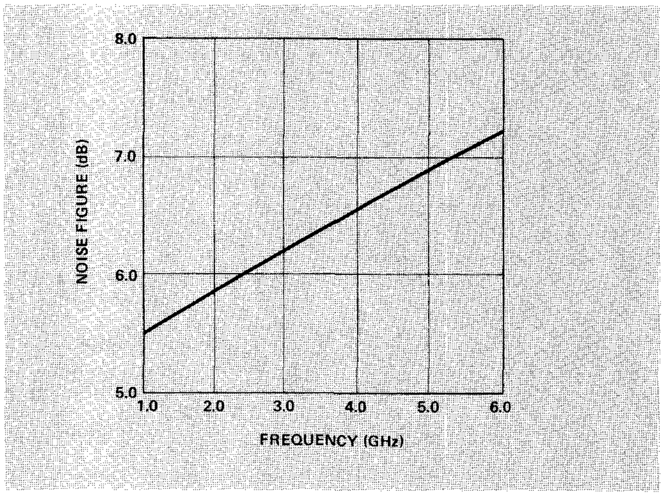


Figure 6. Typical HP 5082-2400 Noise Figure vs. Frequency with P_{LO} = 1.0 mW, f_{IF} = 30 MHz, and NF_{IF} = 1.5 dB. Mount tuned at each frequency.

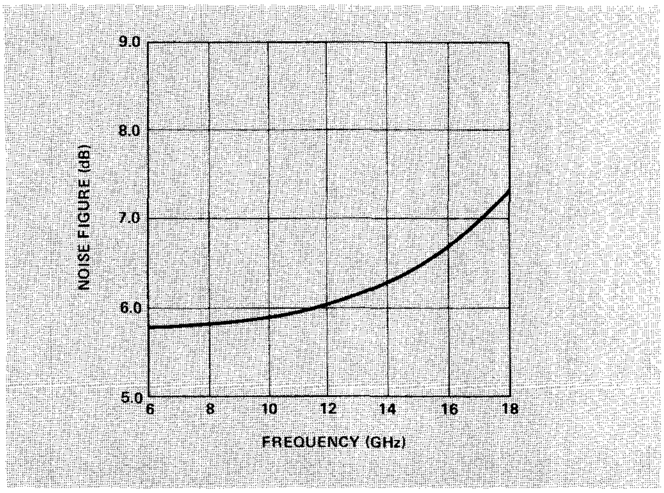


Figure 7. Typical Noise Figure vs. Frequency. IF = 30 MHz, NF_{IF} = 1.5 dB, P_{LO} = 1 mW. Diode matched at each frequency (5082-2200, 2700 series).

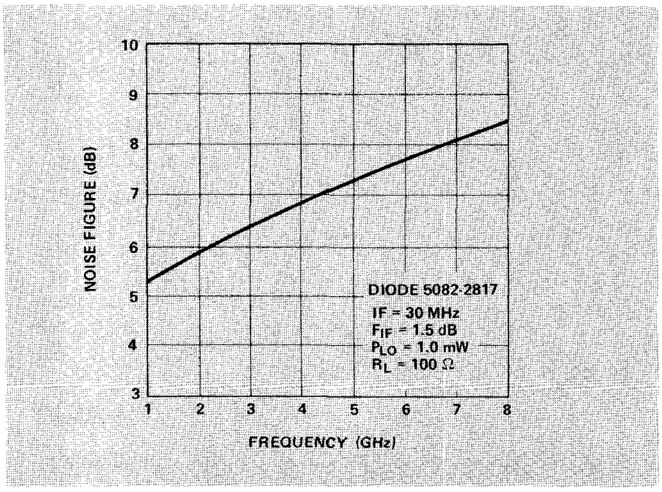


Figure 8. Typical Noise Figure vs. Frequency. The mount is tuned for minimum noise figure at each frequency.

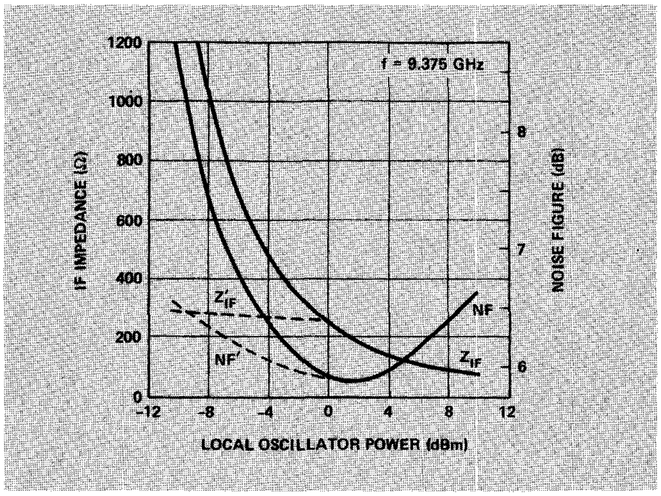


Figure 9. Typical Noise Figure and IF Impedance for 5082-2711 vs. Local Oscillator Power. Note the improved performance at low levels of LO power when dc bias is superimposed (dashed curves).

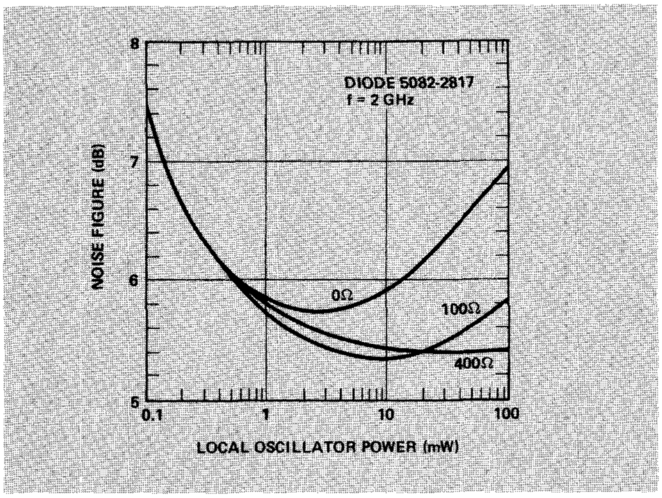


Figure 10. Single Sideband Noise Figure (including an IF-amplifier noise figure of 1.5 dB) vs. Incident LO Power for Various dc-load Resistances R_L. (The mount is tuned for minimum noise figure at each LO power level).

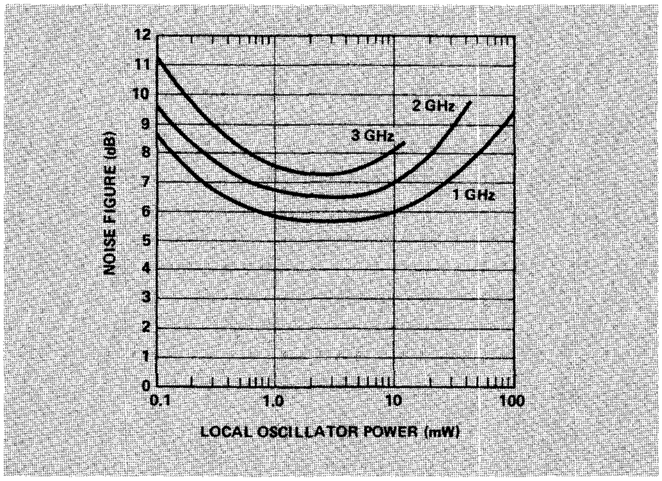


Figure 11. Typical 5082-2350 Noise Figure vs. Local Oscillator Power at 1.0, 2.0 and 3.0 GHz with IF = 30 MHz and NF_{IF} = 1.5 dB.

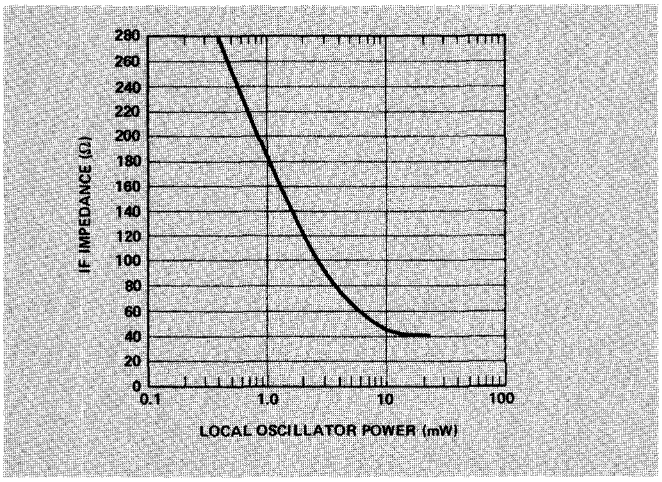


Figure 12. Typical 5082-2300 and 2400 Series IF Impedance vs. Local Oscillator Power with f_{LO} = 2.0 GHz and IF = 30 MHz.

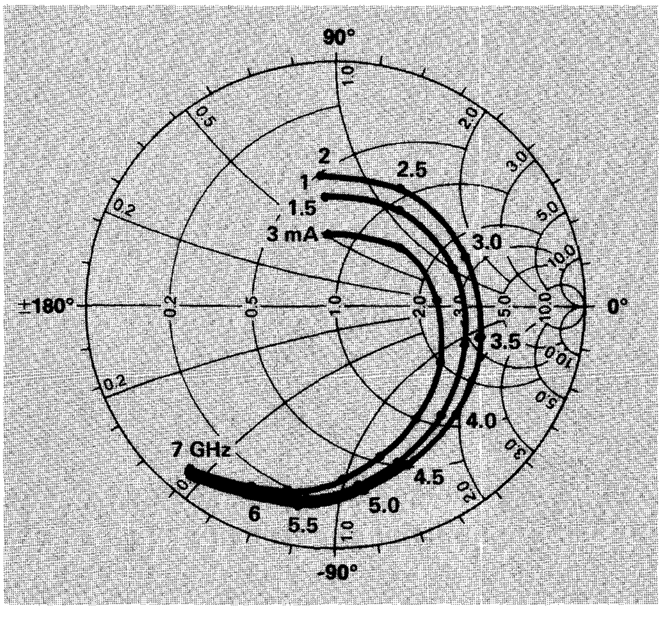


Figure 13. Typical Admittance Characteristics, 5082-2817 with self bias.

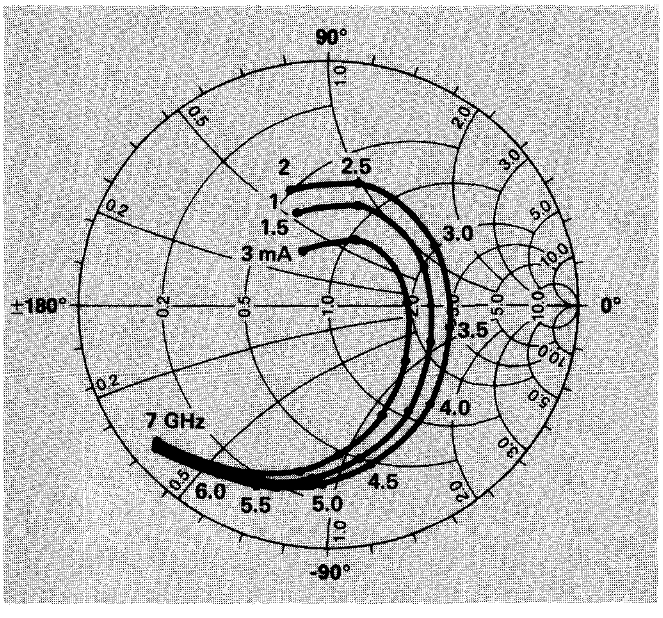


Figure 14. Typical Admittance Characteristics, 5082-2400 with self bias.

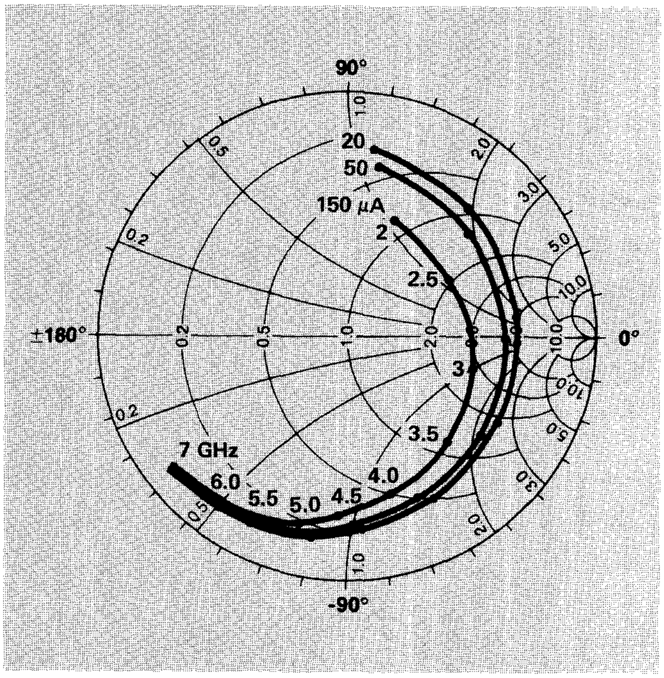


Figure 15. Typical Admittance Characteristics, 5082-2400 with external bias.

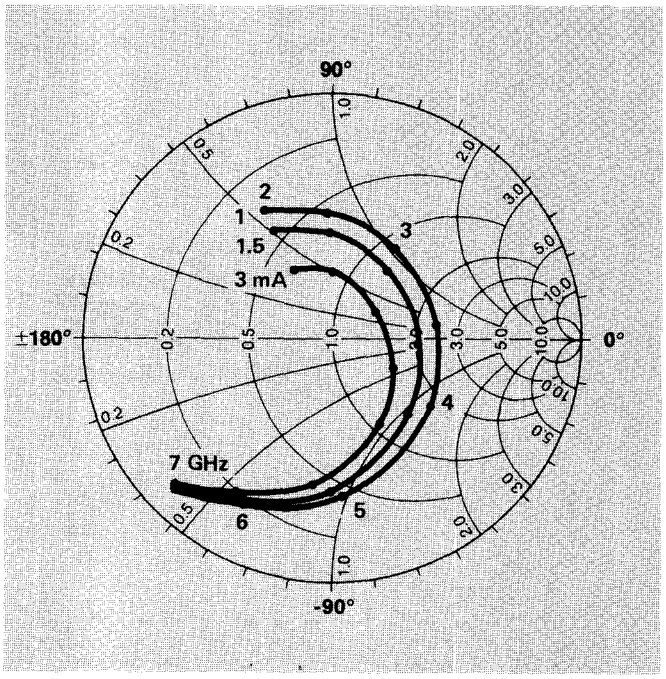


Figure 16. Typical Admittance Characteristics, 5082-2350 with self bias.

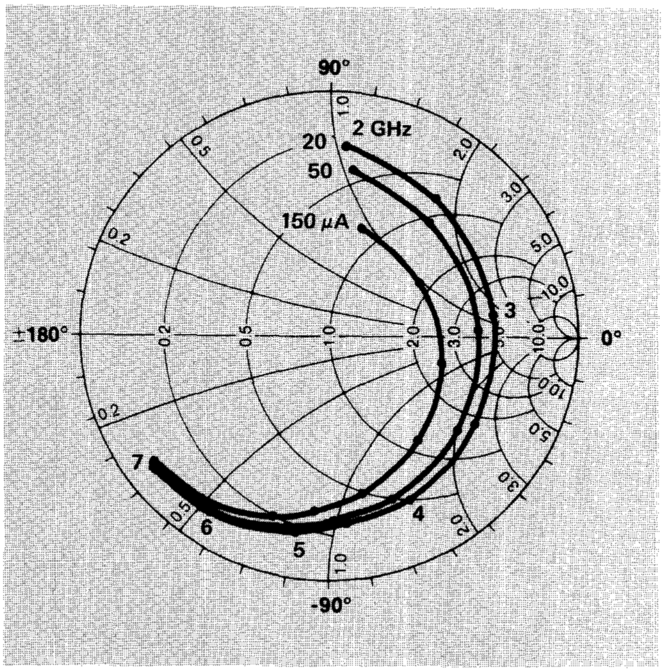


Figure 17. Typical Admittance Characteristics, 5082-2350 with external bias.

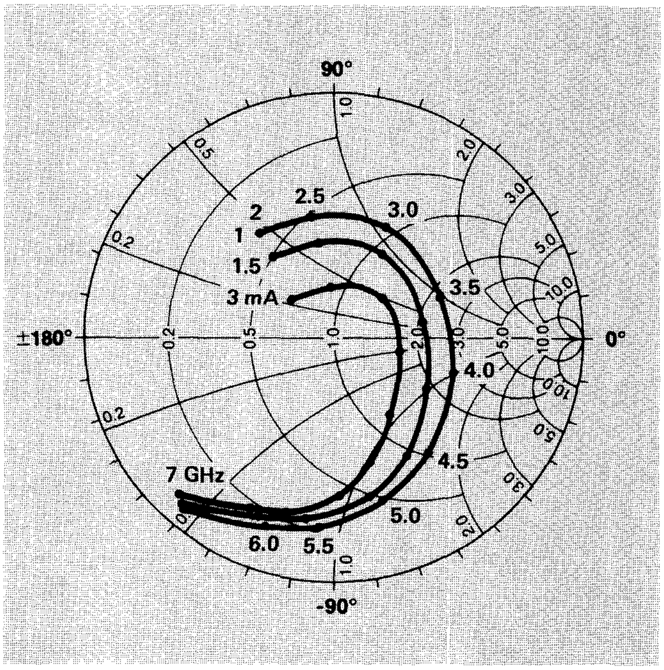


Figure 18. Typical Admittance Characteristics, 5082-2565 with self bias.

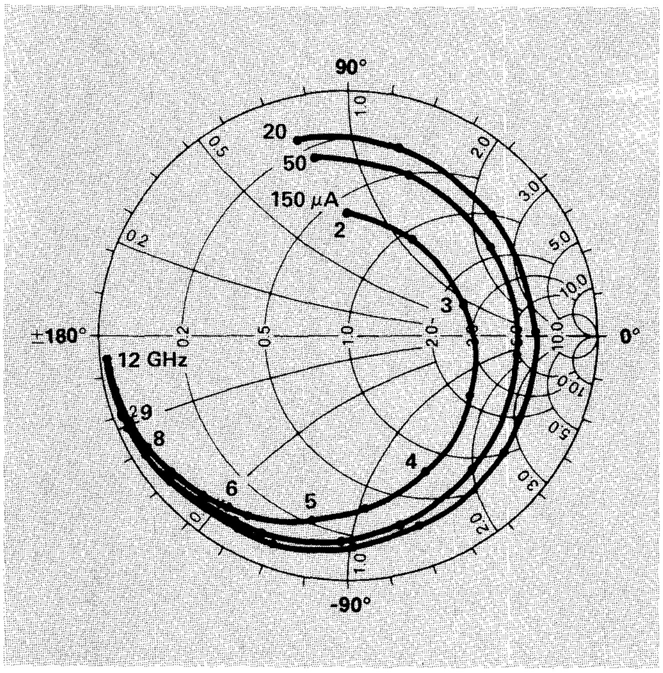


Figure 19. Typical Admittance Characteristics, 5082-2565 with external bias.

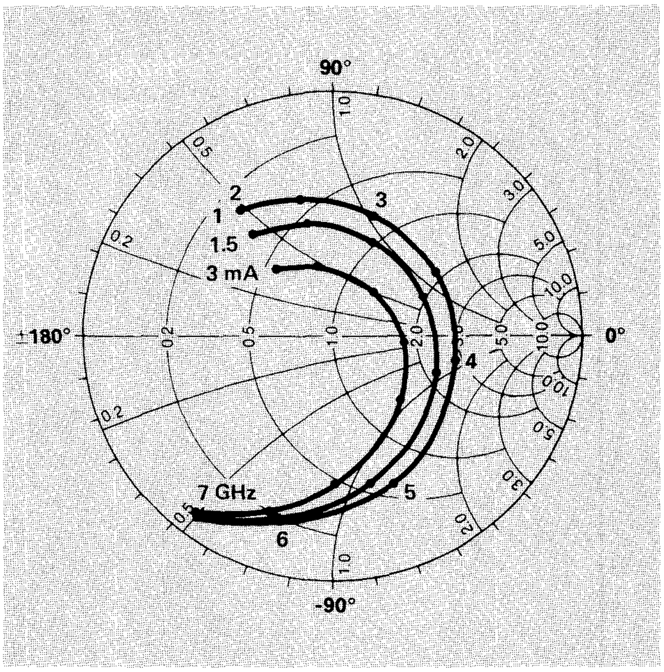


Figure 20. Typical Admittance Characteristics, 5082-2520 with self bias.

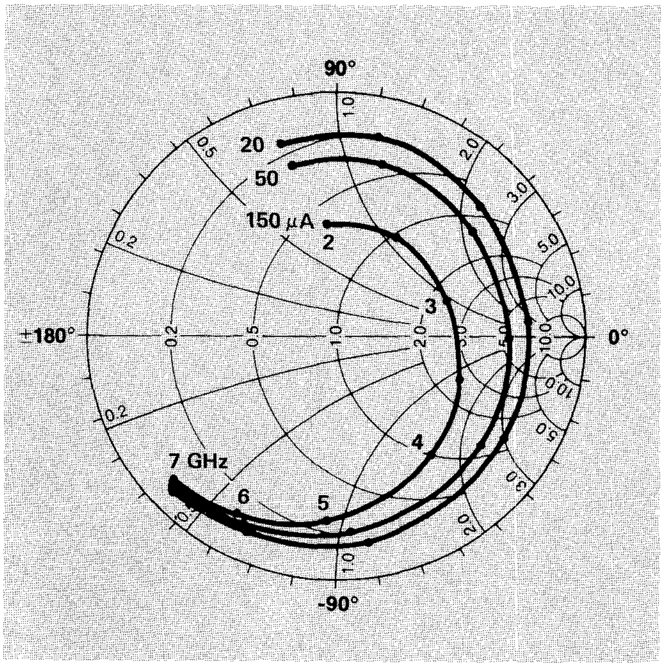


Figure 21. Typical Admittance Characteristics, 5082-2520 with external bias.

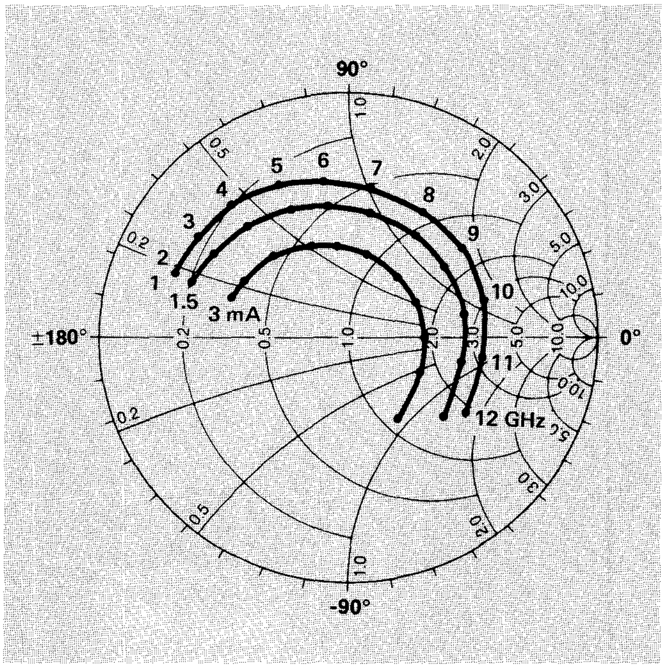


Figure 22. Typical Admittance Characteristics, 5082-2713 with self bias.

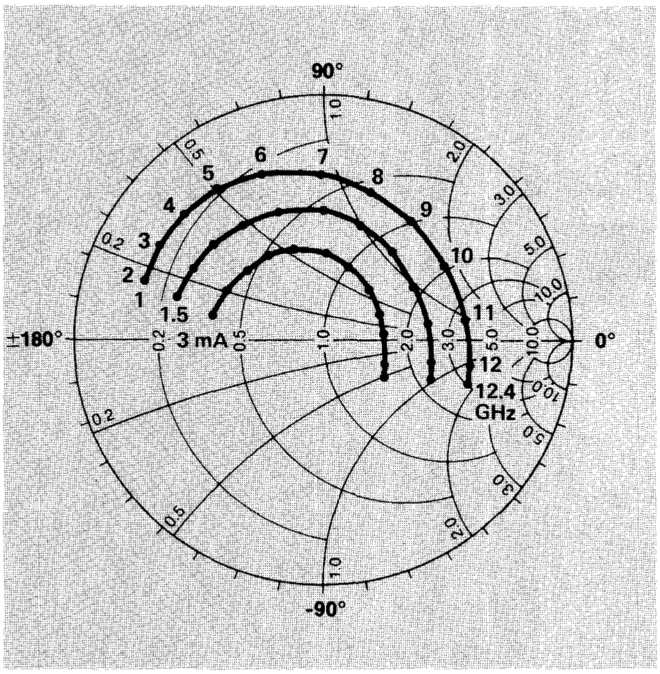


Figure 23. Typical Admittance Characteristics, 5082-2711 with self bias.

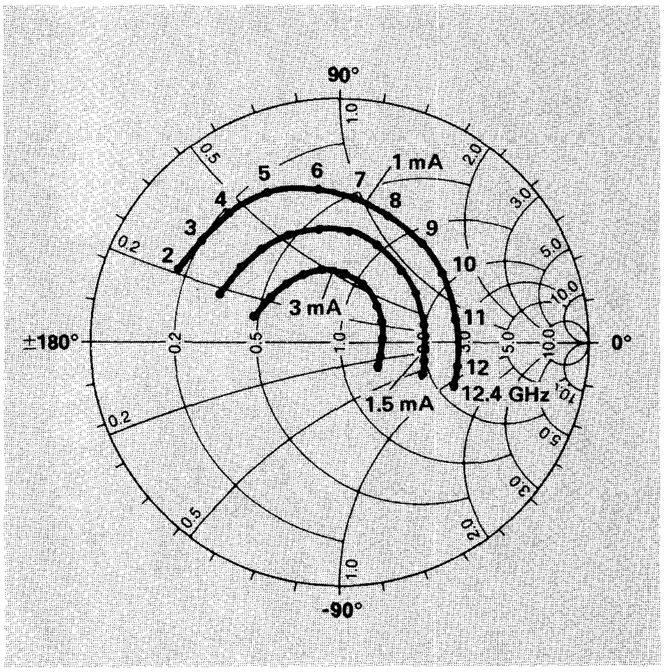


Figure 24. Typical Admittance Characteristics, 5082-2285 with self bias.

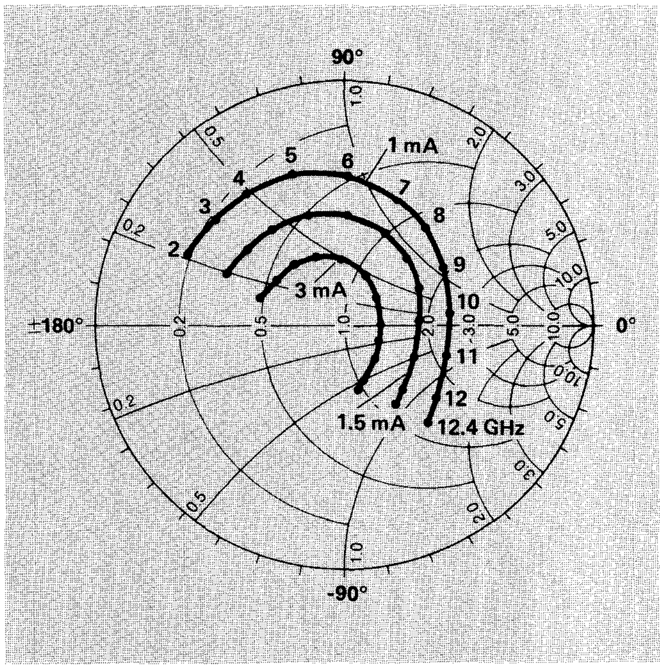


Figure 25. Typical Admittance Characteristics, 5082-2287 with self bias.

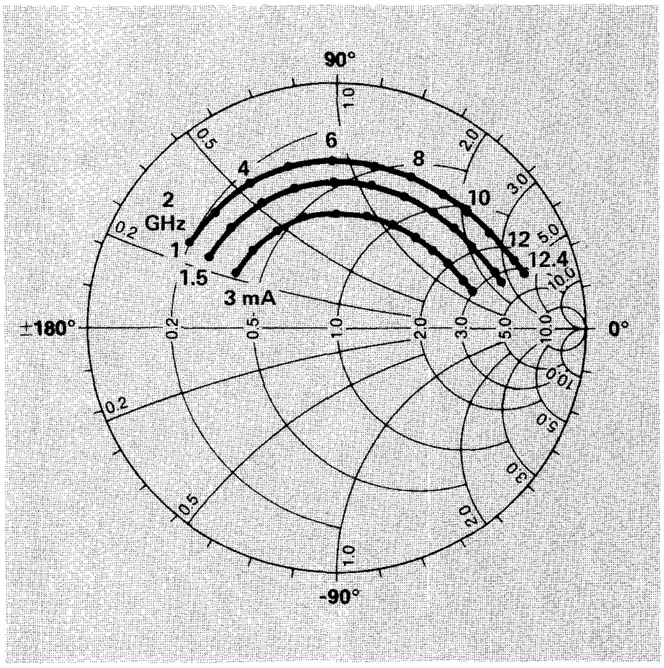


Figure 26. Typical Admittance Characteristics, 5082-2701 with self bias.

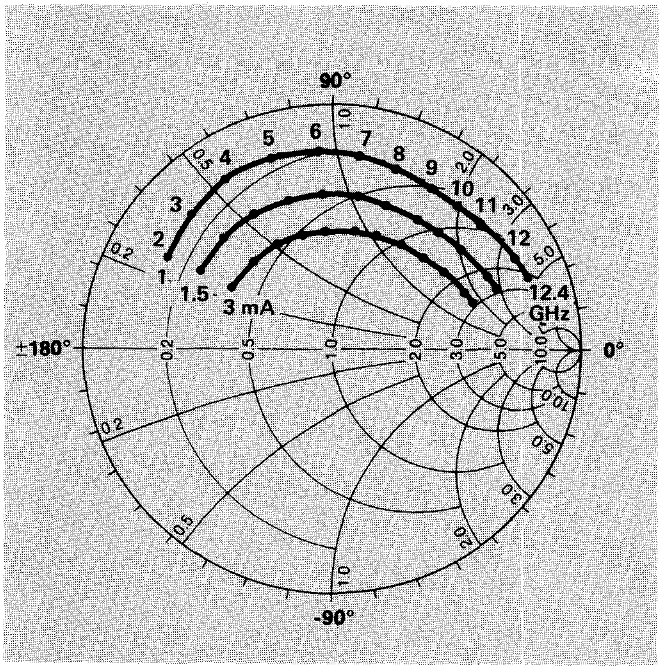


Figure 27. Typical Admittance Characteristics, 5082-2702 with self bias.

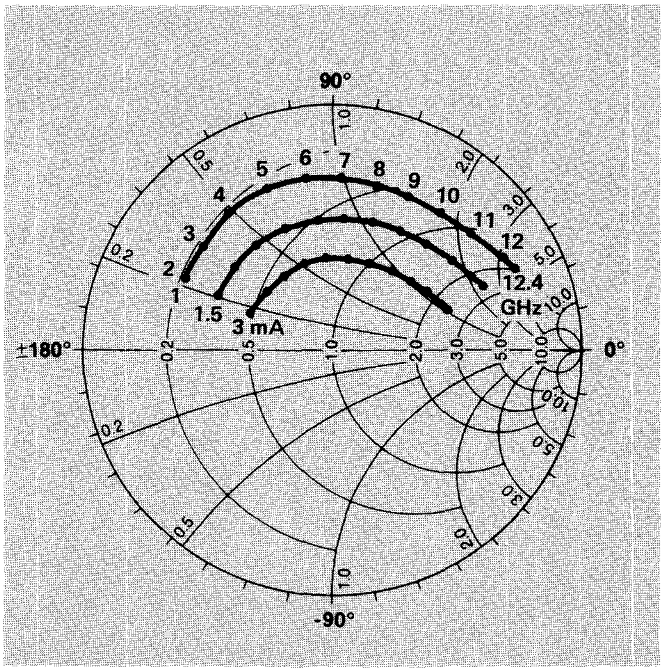


Figure 28. Typical Admittance Characteristics, 5082-2295 with self bias.

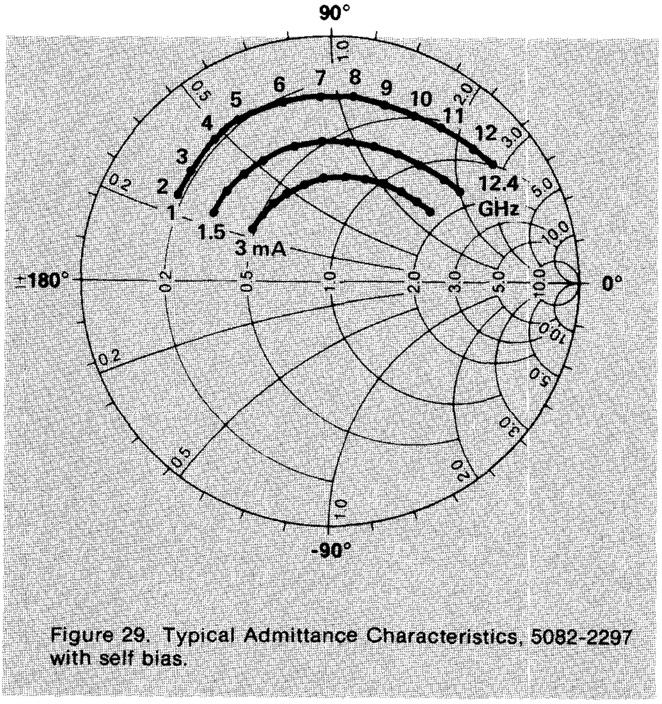


Figure 29. Typical Admittance Characteristics, 5082-2297 with self bias.

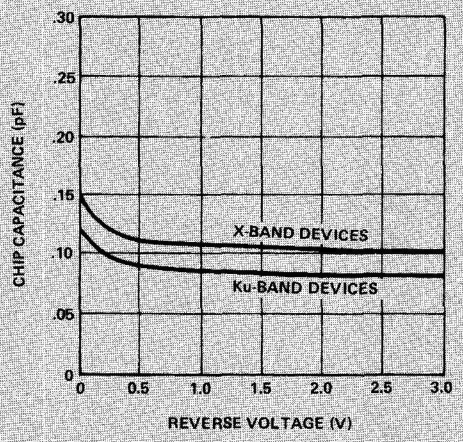


Figure 30. Typical Chip Capacitance vs. Reverse Voltage, 2700 Series.

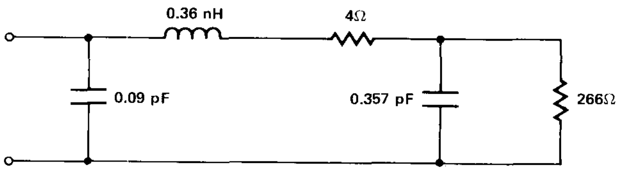


Figure 31. Model for 5082-2701 Mixer Diodes — Rectified Current 1.5 mA.

HEWLETT hp PACKARD
COMPONENTS

ZERO BIAS SCHOTTKY DETECTOR DIODES

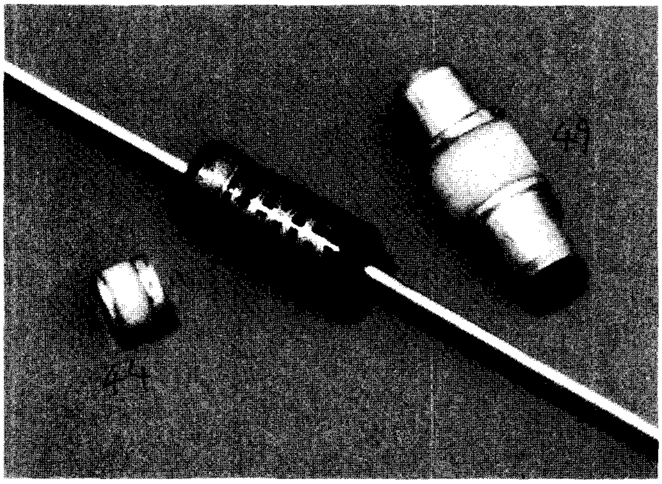
HSCH-3171
HSCH-3206/07
HSCH-3486
HSCH-5018/19 NEW

Features

HIGH VOLTAGE SENSITIVITY

NO BIAS REQUIRED

CHOICE OF HIGH OR LOW VIDEO IMPEDANCE



Description/Applications

The high zero bias voltage sensitivity of these Schottky Barrier diodes makes them ideally suitable for narrow bandwidth video detectors, ECM receivers, and measurement equipment. These diodes also make excellent mixers for use with low power LO.

Maximum Ratings at $T_A = 25°C$

Operating Temperature	-65°C to +150°C
Storage Temperature	-65°C to +150°C

Operation of these devices within the above temperature ratings will assure a device Mean Time Between Failure (MTBF) of approximately 1 x 10^7 hours.

Part Number HSCH-	CW Power Dissipation[1] (mW)	Peak Pulse Power Incident[2] (W)
3486	300	1
5018	500	2
5019	500	3
3171	150	0.5
3207	200	1
3206	200	1

Notes:
1. Derate linearly to zero at 150°C.
2. Pulse width = 1 microsecond. Duty cycle = 0.001.

Electrical Specifications at $T_A = 25°C$

Part Number	Package Outline	Maximum Tangential Sensitivity TSS (dBm)	Minimum Voltage Sensitivity γ (mV/μW)	Video Resistance R_V (KΩ) Min.	Max.	Typical Total Capacitance C_T (pF)
HSCH-3171 11-81	15	-48	30	80	300	0.25
HSCH-3207 17-85	44 ✓	-42	8	80	300	0.30
HSCH-3206 17-85	49 ✓	-42	10	100	300	0.30
HSCH-3486 8-69	15	-54	7.5	2	8	0.30
HSCH-5018 18-63	44 ✓	-53	7	2	8	0.45
HSCH-5019 18-63	49 ✓	-54	7	2	8	0.47
Test Conditions		Video Bandwidth = 2 MHz f_{test} = 10 GHz	Power in = -40 dBm f_{test} = 10 GHz			$V_R = 0$ V f = 1 MHz

Note: For HSCH-3171, -3207, -3206, $I_R = 10\ \mu A$ (max) at $V_R = 3V$ at $T_A = 25°C$. For reverse characteristics of HSCH-3486, -5018, -5019 see Figure 3.

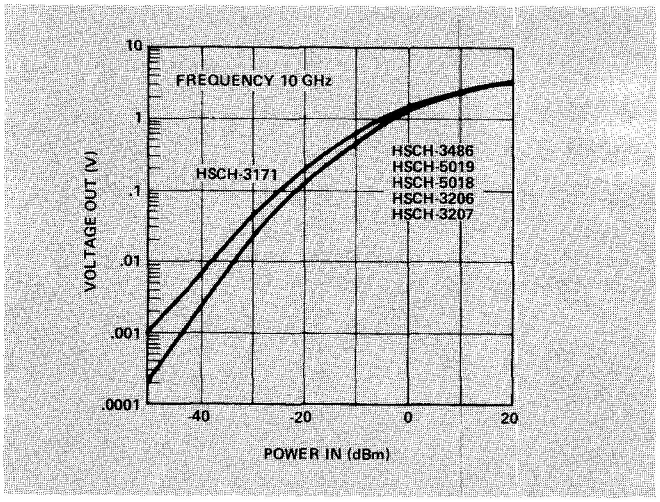


Figure 1. Typical Dynamic Transfer Characteristics.

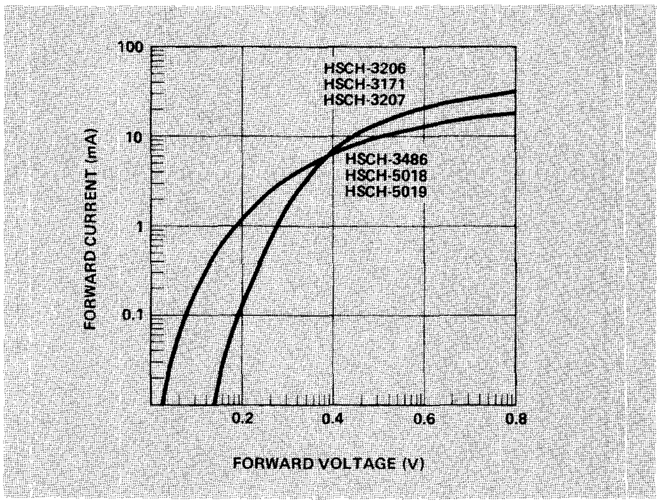


Figure 2. Typical Forward Characteristics at $T_A = 25°C$.

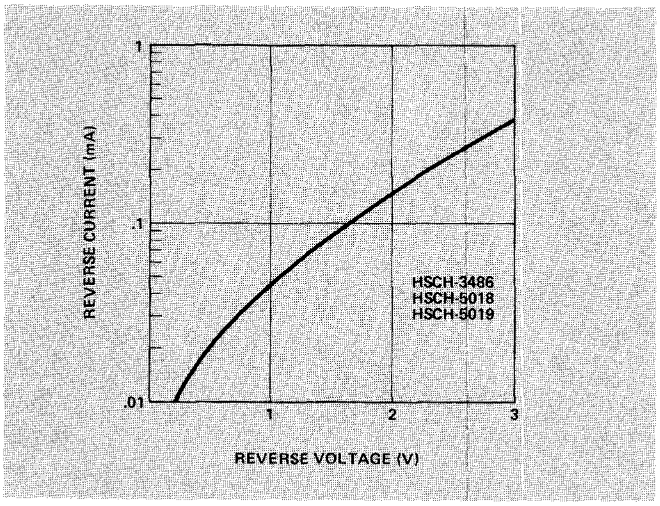


Figure 3. Typical Reverse Characteristics at $T_A = 25°C$.

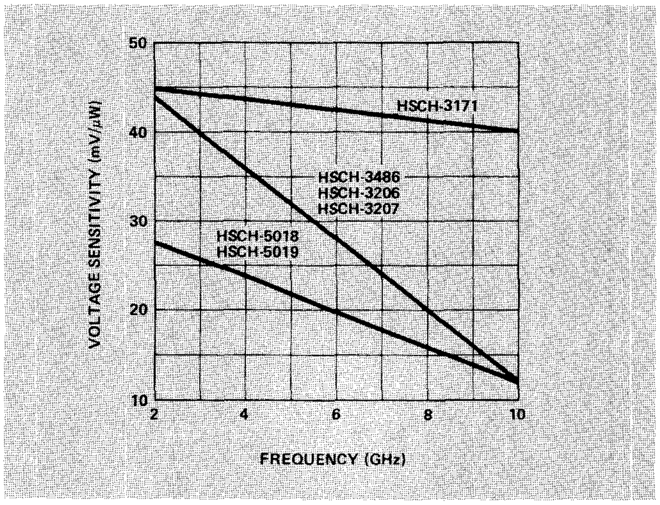


Figure 4. Typical Voltage Sensitivity vs. Frequency.

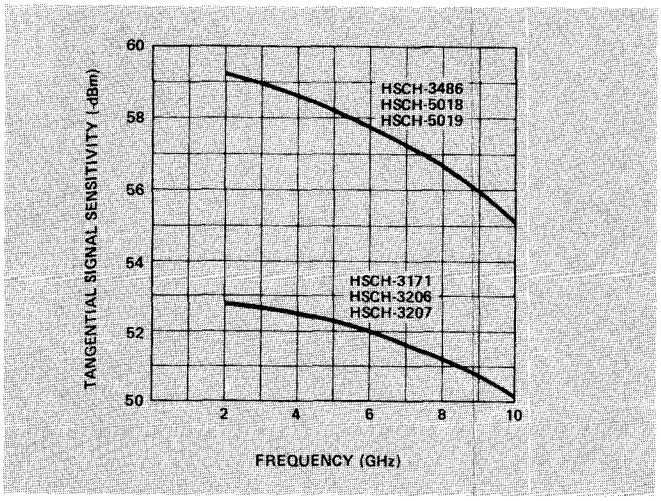


Figure 5. Typical Tangential Sensitivity vs. Frequency.

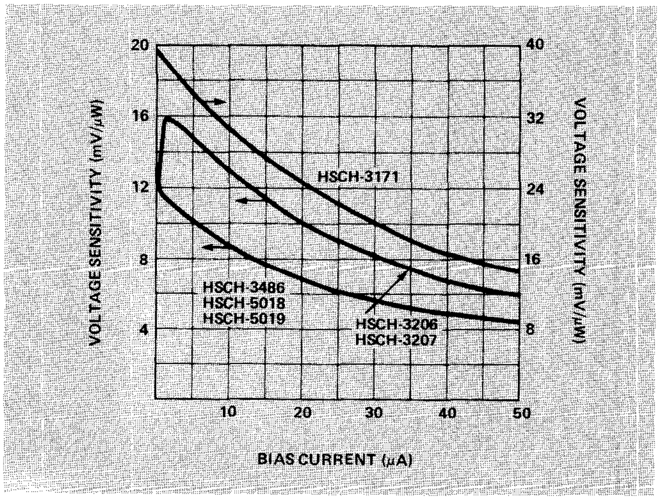


Figure 6. Typical Voltage Sensitivity vs. Bias Current.

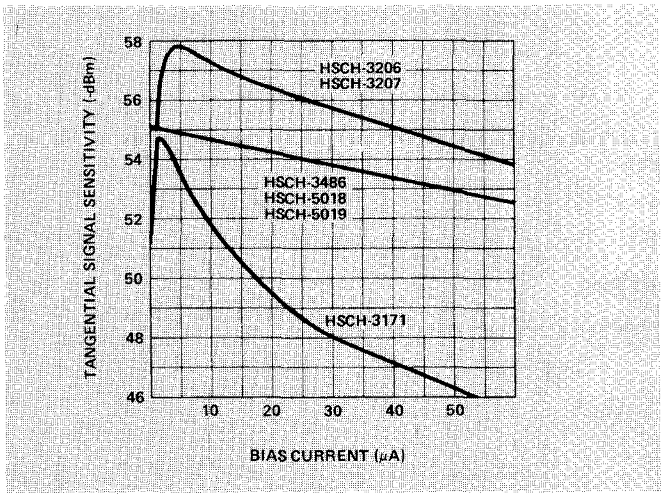


Figure 7. Typical Tangential Sensitivity vs. Bias Current.

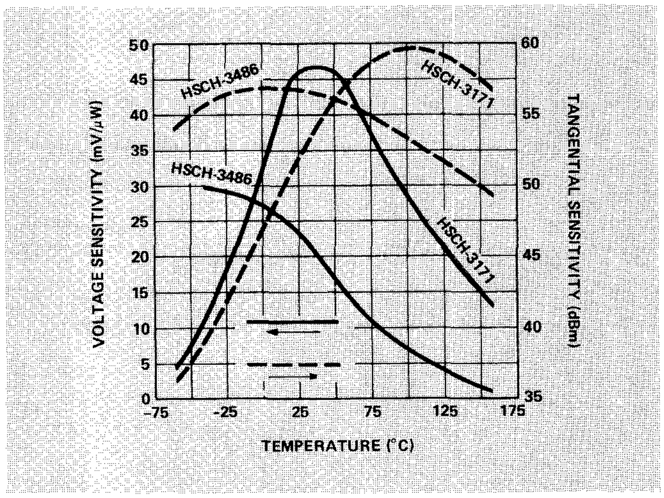


Figure 8. Effect of Temperature.

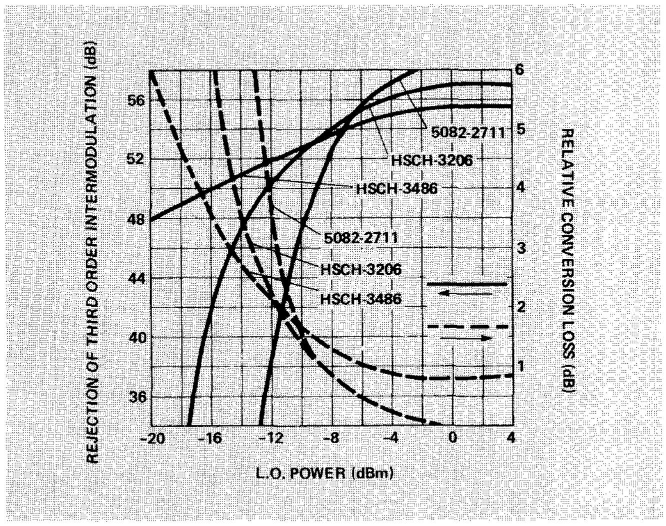


Figure 9. Mixer Performance.

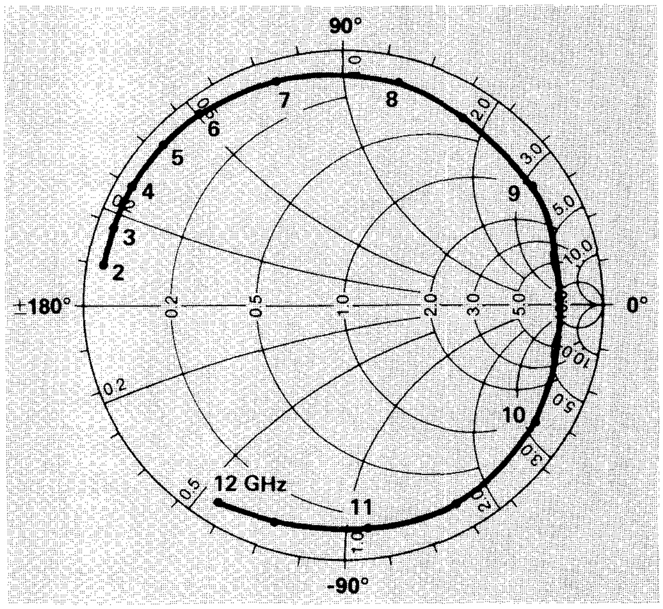


Figure 10. Typical Admittance Characteristics. HSCH-3171.

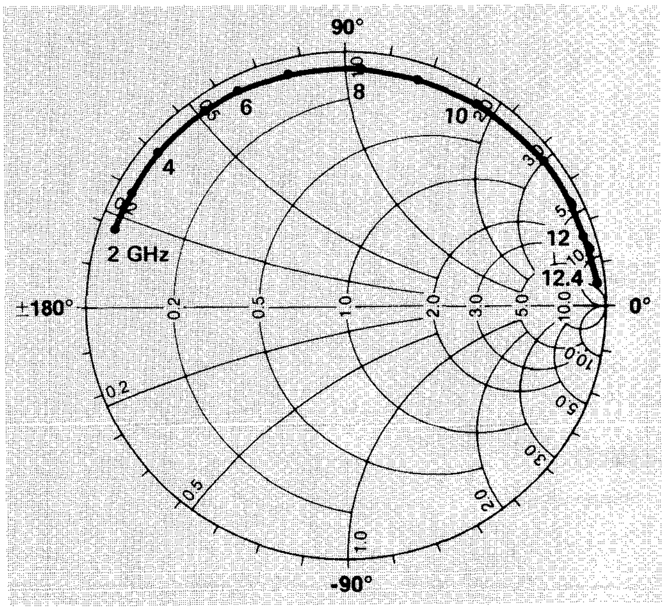


Figure 11. Typical Admittance Characteristics, HSCH-3206.

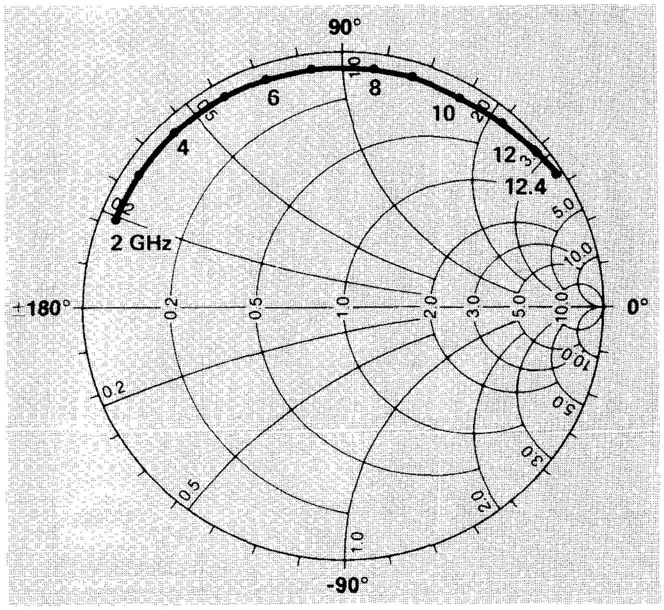


Figure 12. Typical Admittance Characteristics, HSCH-3207.

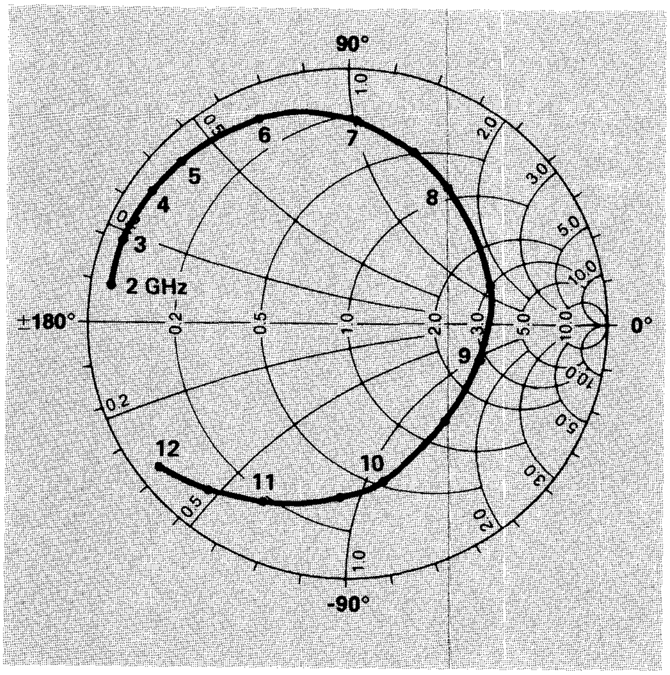
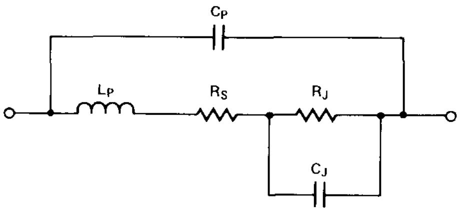


Figure 13. Typical Admittance Characteristics, HSCH-3486.



DIODE MODEL

Parameter	Symbol	Units	HSCH-3486	HSCH-3171
Package Capacitance	C_P	pF	0.063	0.060
Package Inductance	L_P	nH	2.23	2.28
Series Resistance	R_S	Ω	10	4.13
Junction Resistance	R_J	Ω	4588	171K
Junction Capacitance	C_J	pF	0.148	0.12

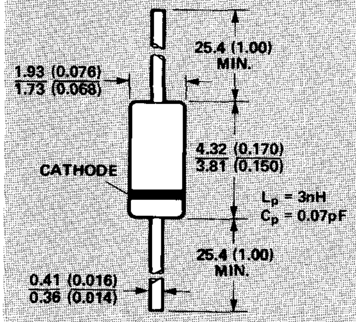
Package Characteristics

The HP Outline 15 package has a glass hermetic seal with Dumet leads which should be retricted so that the bend starts at least 1/16" (1.6 mm) from the glass body. With this restriction, it will meet MIL-STD-750, Method 2036, Conditions A and E (4 lb. [1.8 kg] tension for 30 minutes). The maximum soldering temperature is 230°C for 5 seconds. Marking is by digital coding with a cathode band.

The HP Outline 49 package has a metal-ceramic hermetic seal. The anode and cathode studs are gold-plated Kovar. The maximum soldering temperature is 230°C for 5 seconds. Stud-stud T/R is 0.010" max.

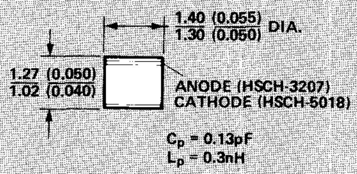
The HP Outline 44 package is a hermetically sealed ceramic package. The anode and cathode are gold-plated Kovar. The maximum soldering temperature is 230°C for 5 seconds.

Package Dimensions



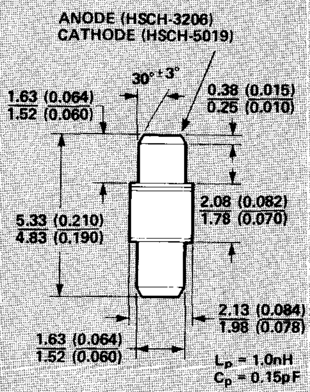
Outline 15

HSCH-3171
HSCH-3486



Outline 44

HSCH-3207
HSCH-5018



Outline 49

HSCH-3206
HSCH-5019

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SCHOTTKY BARRIER DIODES FOR DETECTORS

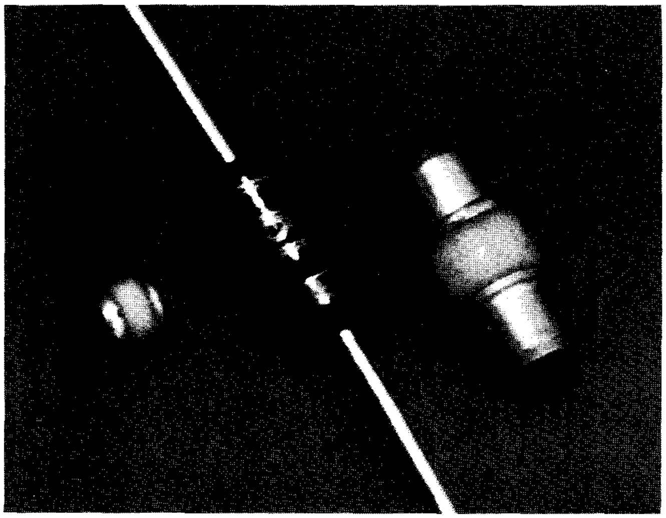
5082-2750/51
5082-2755 10-96
5082-2787 3-91
5082-2824 4.91

Features

IMPROVED DETECTION SENSITIVITY
TSS OF -55 dBm at 10 GHz

LOW 1/f NOISE
Typical Noise-Temperature Ratio = 4 dB at 1 kHz

HIGH PEAK POWER DISSIPATION
4.5 W RF Peak Pulse Power



Description / Applications

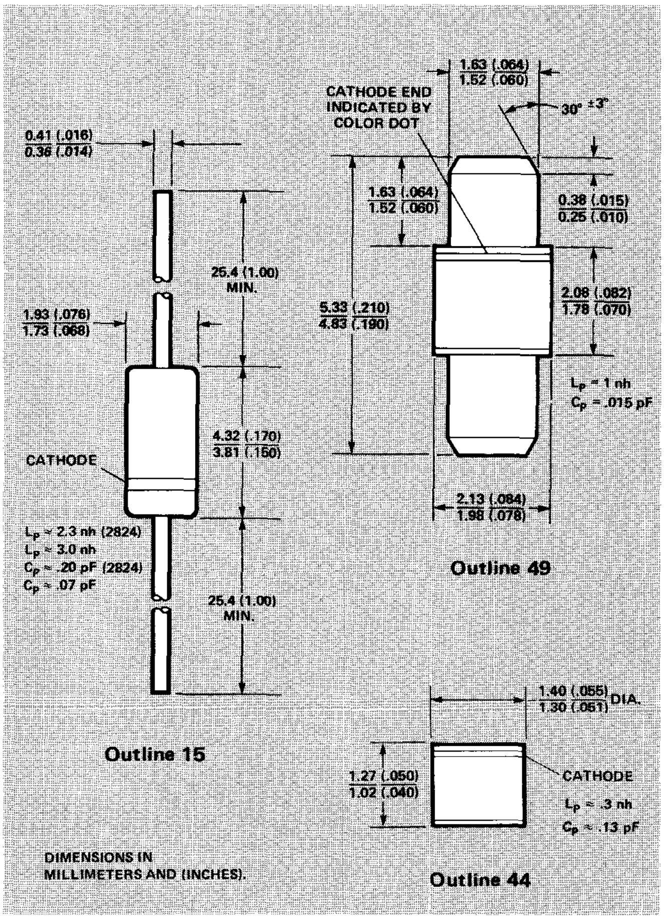
The low 1/f noise and high voltage sensitivity make these Schottky barrier diodes ideally suitable for narrow bandwidth video detectors, and Doppler mixers as required in Doppler radar equipment, ECM receivers, and measurement equipment.

Maximum Ratings at $T_{CASE} = 25°C$

Junction Operating and Storage Temperature Range	
5082-2824	-65°C to +200°C
All Others	-60°C to +150°C
Operation of these devices within the above temperature ratings will assure a device Mean Time Between Failure (MTBF) of approximately 1 x 10^7 hours.	
DC Power Dissipation — Power Absorbed by Diode	
Derate Linearly to zero at Maximum Temperature	
5082-2824 (Applied for 1 minute)	1 W
5082-2824 (Continuous)	250 mW
All Others (Continuous)	100 mW
Soldering Temperature	230°C for 5 sec.
RF Peak Pulse Power	
Pulse Width = 1 μs, Du = .001, R_L = 38KΩ (Applied for 1 minute)	
5082-2824 (Power Absorbed by Diode)	4.5 W
All Others (Power Incident)	2.0 W
Maximum Peak Inverse Voltage (PIV)	V_{BR}

Note: The 2700 series diodes are pulse sensitive. Handle with care to avoid static discharge through the diode.

Package Dimensions



DIMENSIONS IN MILLIMETERS AND (INCHES).

Electrical Specifications at $T_A = 25°C$

Part Number 5082-	Package Outline	Maximum Tangential Sensitivity TSS (dBm)	Voltage Sensitivity Minimum γ (mV/µW)	Video Resistance R_V (kΩ) Min.	Video Resistance R_V (kΩ) Max.
2824	15	-56	6.0	1.2	1.5
2787*		-52	3.5	1.2	1.6
2755		-55	5.0	1.2	1.6
2751	49	-55	5.0	1.2	1.6
2750	44	-55	5.0	1.2	1.6
Test Conditions		Video Bandwidth = 2 MHz f_{RF} = 2 GHz for 5082-2824, 10 GHz for all others I_{BIAS}=20 µA; Video Amp Eq. Noise, R_A = 500Ω.	Same as for TSS at RF Signal Power Level of -40 dBm Load Resistance = 100KΩ		

*RF Parameters for the 5082-2787 are sample tested only.

Typical Parameters

Noise Temperature Ratio at f (dB)	Breakdown Voltage V_{BR} (V)	Junction Capacitance C_{JO} (pF)
2 at 20 kHz 8 at 1 kHz	15	1.0
5.0 at 20 kHz 15.0 at 1 kHz	4	.12
	5	.12
	5	.12
	5	.12
R_V = 50Ω	I_R = 10 µA	V = 0

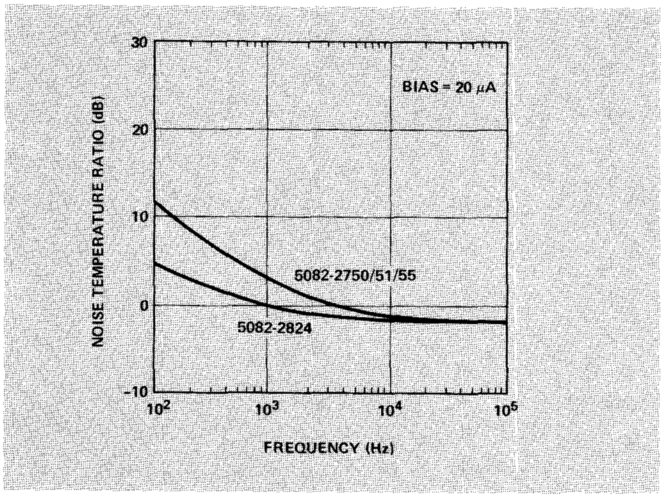


Figure 1. Typical Flicker (1/f) Noise vs. Frequency.

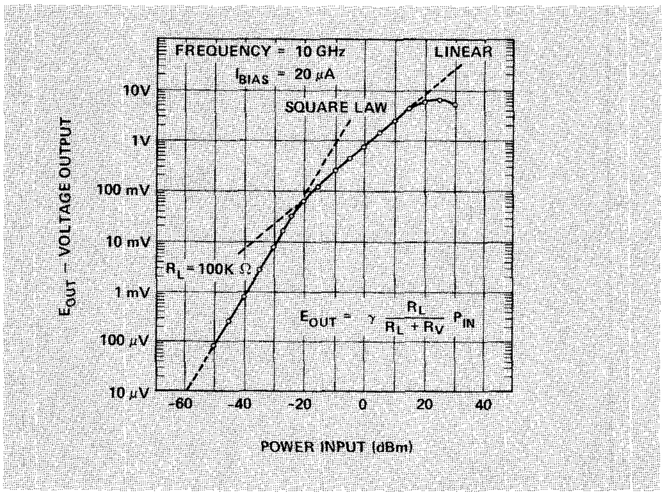


Figure 2. Typical Dynamic Transfer Characteristic. (5082-2750 Series).

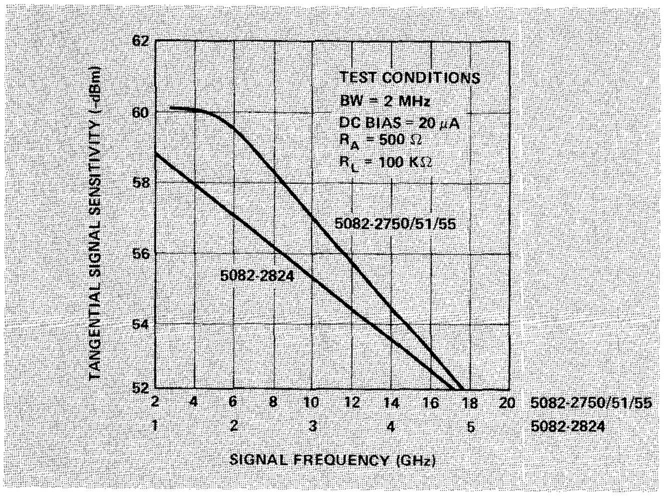


Figure 3. Typical TSS vs. Frequency.

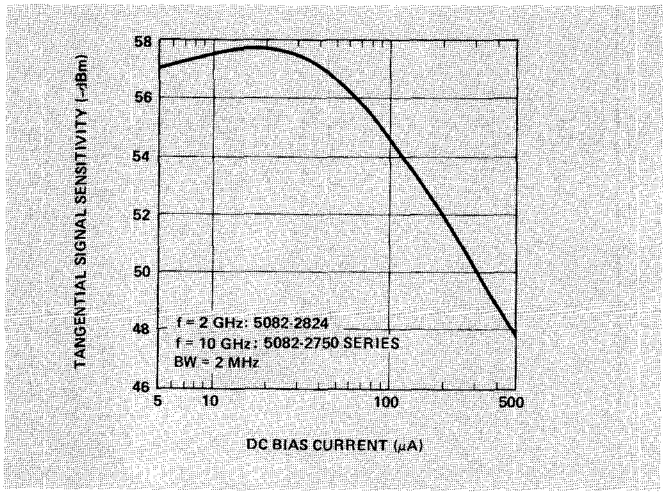


Figure 4. Typical TSS vs. Bias.

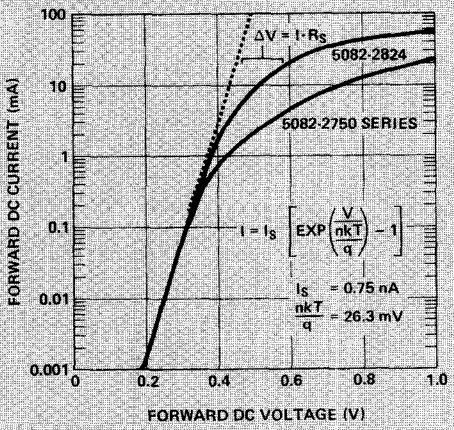


Figure 5. Typical Forward Characteristics at $T_A = 25°C$.

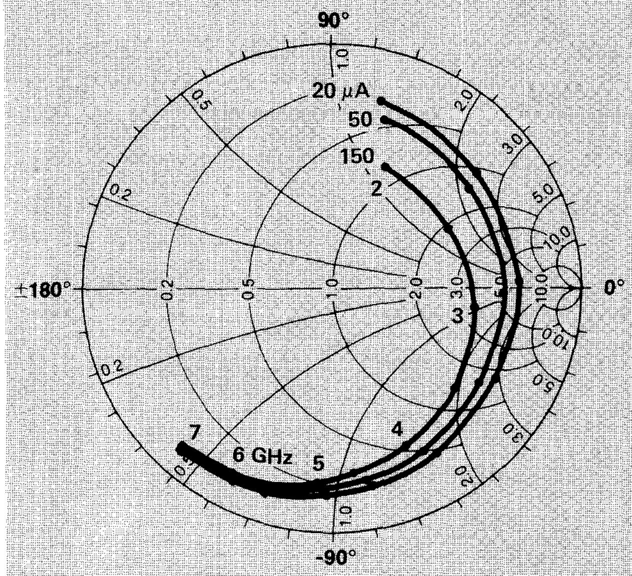


Figure 6. Typical Admittance Characteristics, 5082-2824 with external bias.

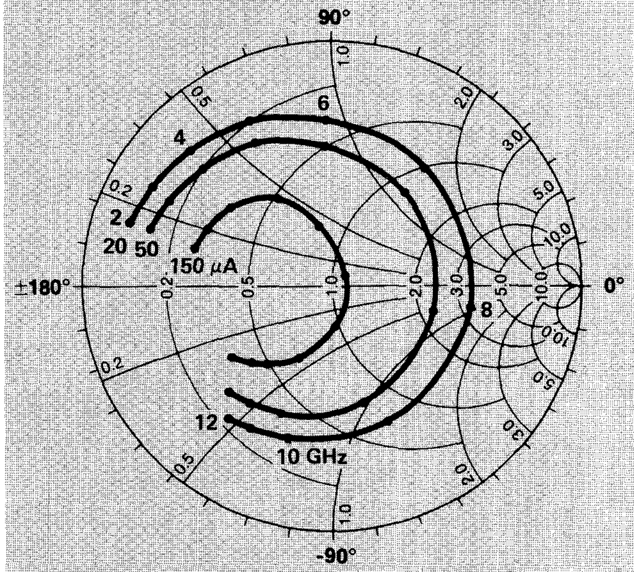


Figure 7. Typical Admittance Characteristics, 5082-2755 with external bias.

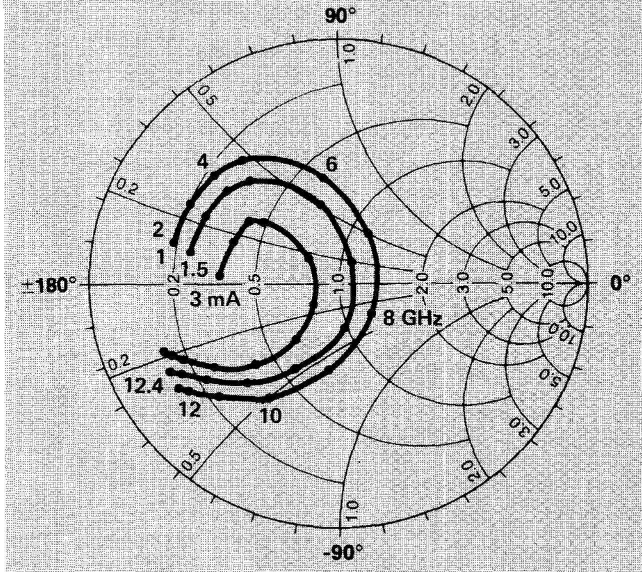


Figure 8. Typical Admittance Characteristics, 5082-2755 with self bias.

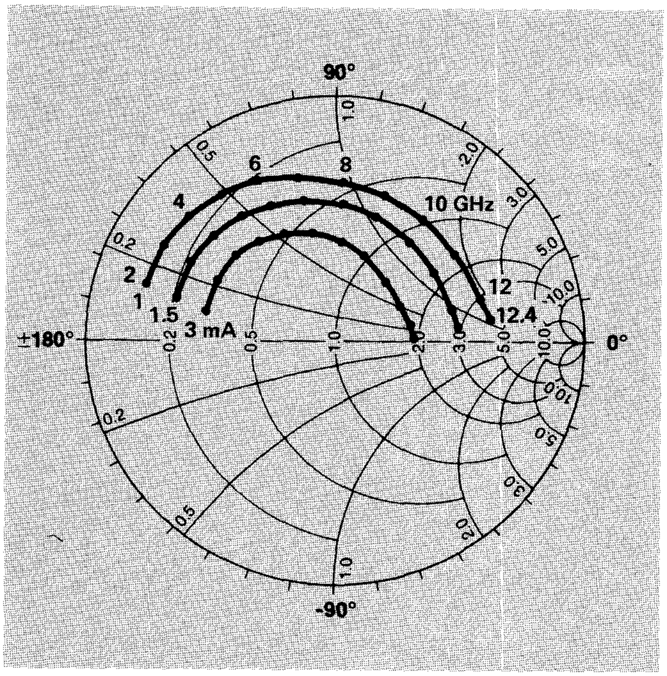


Figure 9. Typical Admittance Characteristics, 5082-2751 with self bias.

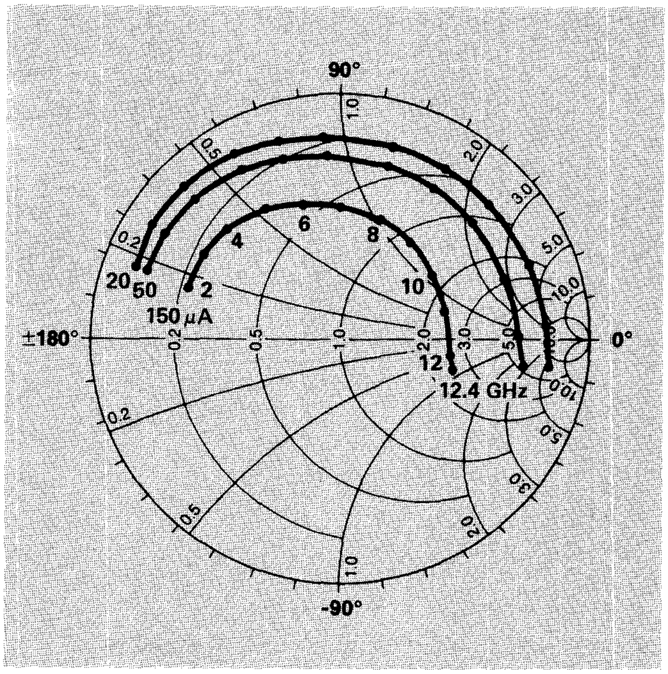


Figure 10. Typical Admittance Characteristics, 5082-2751 with external bias.

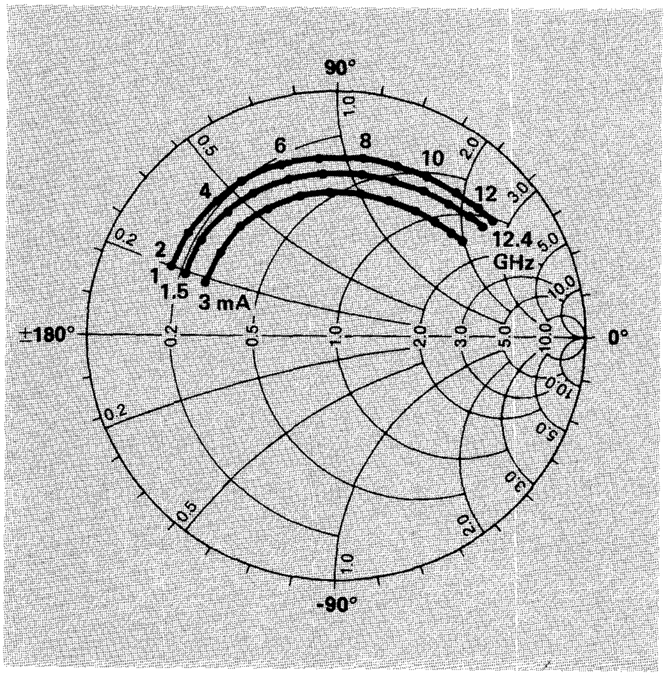


Figure 11. Typical Admittance Characteristics, 5082-2750 with self bias.

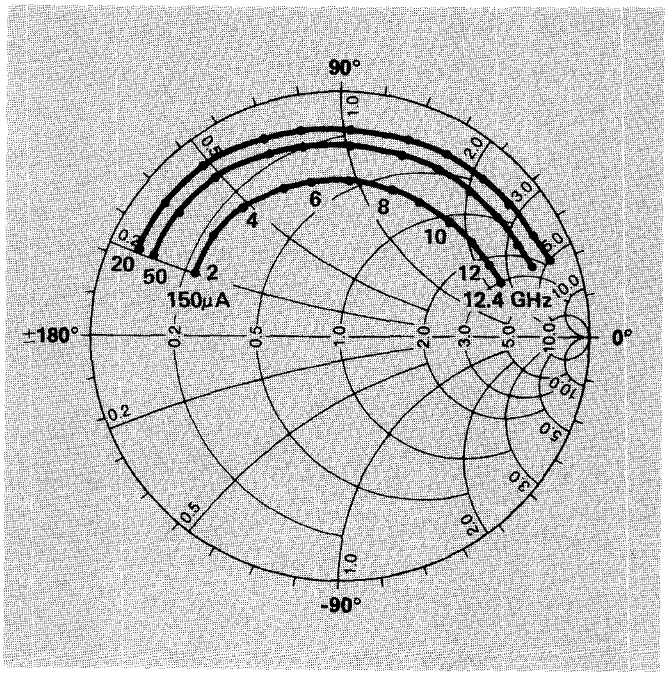


Figure 12. Typical Admittance Characteristics, 5082-2750 with external bias.

Applications for Schottky Diodes

HEWLETT PACKARD
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APPLICATIONS FOR SCHOTTKY DIODES

The Criterion for the Tangential Sensitivity Measurement

(Application Note 956-1)

A tangential signal is defined on a CRT display as a pulse whose bottom level coincides with the top level of the noise on either side of the pulse (Figure 1). Although the corresponding signal-to-noise ratio depends on many system factors, the generally accepted ratio of 8 dB at the output correlates well with the tangential appearance on the oscilloscope for practical systems.

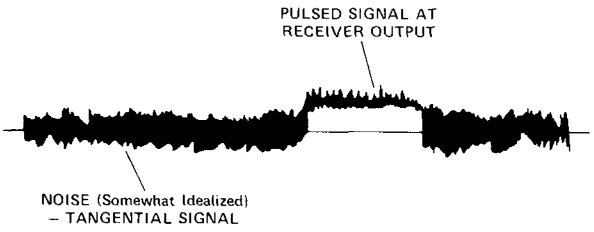


Figure 1.

The often asked question concerning whether 8 dB refers to voltage or power is not a valid one. The number of decibels is defined as 10 $\log_{10}$ ($P_1 \div P_2$) where P_1 and P_2 are power levels to be compared. If output voltages are to be compared, the ratio $(V_1 \div V_2)^2$ may be substituted for ($P_1 \div P_2$). In this case the number of decibels is 20 $\log_{10}$ ($V_1 \div V_2$). The number of decibels determines both ($V_1 \div V_2$) and ($P_1 \div P_2$). The terms "voltage dB" and "power dB" are not significant. For example, the 8 dB output ratio corresponds to a power ratio of 6.3 and a voltage ratio of 2.5.

Another source of confusion is the relationship between input ratios and output ratios. Because the detector is a square law device, the output voltage is proportional to the square of the input voltage, or to the input power. A signal-to-noise voltage ratio of 2.5 at the output thus corresponds to an input power ratio of 2.5. Since 10 log 2.5 = 4, the equivalent input signal-to-noise ratio for tangential sensitivity is 4 dB.

A useful production test system (Figure 2) uses an RMS voltmeter to compare signal output to noise output. The noise level is observed on the meter with RF signal off, but with d.c. bias applied to the Device Under Test. Then the specified tangential signal level is applied and the increase in RMS voltmeter reading must correspond to 8 dB or more.

The use of square wave modulation and AC coupling introduce another source of confusion to this measurement. The increase in reading on the RMS voltmeter corresponding to the 8 dB criterion is 4.1 dB. The 8 dB criterion means that the peak signal voltage is 2.5 times the RMS noise voltage V_m. Because the RMS meter uses AC coupling, the square wave is symmetrical with amplitude 1.25 V_m. The square of this voltage combines with the square of the noise voltage to give the total voltage on the RMS meter.

$$V_T^2 = V_N^2 + (1.25\ V_N)^2 = 2.56\ V_N^2$$

This ratio corresponds to 4.1 dB.

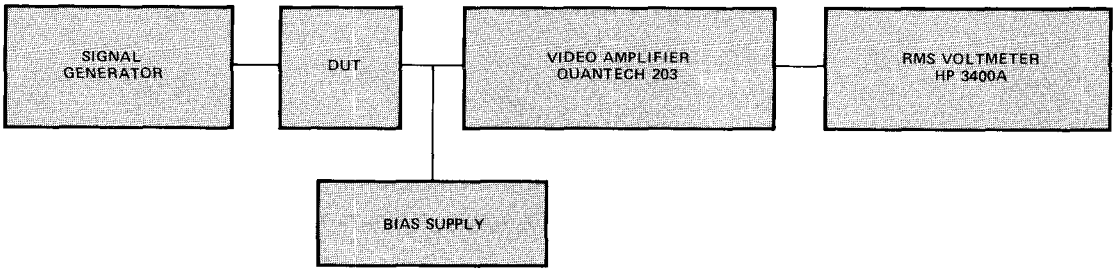


Figure 2. TSS Test System

Flicker Noise in Schottky Diodes (Portion of Application Note 956-3)

INTRODUCTION

At frequencies above a few megahertz, Schottky barriers emit noise at a power level which is half as much[1] as the familiar Johnson noise of a resistor. The presence of series resistance in the diode substrate and contacts makes the effective noise output comparable to resistor noise. The ratio of diode noise power to resistor noise power, the noise temperature ratio, is close to unity.

At lower frequencies, diode noise gradually increases and soon reaches an inverse frequency [2] behavior. This excess noise contribution is called flicker noise. The frequency at which the extended inverse frequency line crosses unity noise temperature ratio is called the noise corner frequency. All Schottky diodes have lower corner frequencies than those of either pn junctions or point contact diodes.

SCHOTTKY DIODE TYPES

There are four types of Schottky barrier diodes, each with different noise corner frequencies. Figures 1 & 2 show typical characteristics of these diodes.

Silicon dioxide passivated diodes with n-doped epitaxial layers have the highest corner frequencies among Schottky diodes. This type of diode is used primarily for X and P Band mixers. For most applications the intermediate frequency is well above the corner frequency and the flicker noise does not degrade the performance. The HP 5082-2701 diode is an example of this type.

Improved flicker noise performance in passivated diodes is obtained by substituting p-type doping for n-type. The Hewlett-Packard X-band 5082-2750 detector diode is an example. The improvement in detection sensitivity over that of an n-type diode is noticed when a significant portion of the video bandwidth extends below the corner frequency.

Even lower flicker noise is obtained with the hybrid (guard ring) diode[3], such as the 5082-2824. These diodes are optimized for performance up to 2 GHz.

The lowest flicker noise in Schottky diodes, or for that matter any type of diode, is found in the mesh diode, such as the HP 5082-2565. These diodes will give the best performance in applications requiring low flicker noise at frequencies below 3 GHz.

DOPPLER MIXERS

Doppler system intermediate frequencies usually extend into the flicker noise region, so a diode with low flicker noise is often the optimum Doppler mixer diode. However, conversion loss, L, will be higher when S band diodes are used in X band mixers, so the trade-off between flicker noise and conversion loss must be considered. The choice may be made by comparing the overall noise figure of the mixer diode, $L_m\ (F_{IF} - 1 + t_m)$, with the corresponding expression for the detector or mesh diode, $L_d\ (F_{IF} - 1 + t_d)$. F_{IF} is the IF noise figure. The detector or mesh diode will provide better Doppler mixing when

$$\frac{L_D}{L_M} < \frac{F_{IF} - 1 + t_m}{F_{IF} - 1 + t_d}$$

When the Doppler frequency is so low that $t_d \gg F_{IF} - 1$, the criterion may be considered as

$$\frac{L_D}{L_M} < \frac{t_m}{t_d}$$

In other words, the diode noise figure Lt is the proper criterion.

This criterion makes it possible to consider the low flicker noise mesh diode at frequencies above its normal operating range. For example, at an operating frequency of 8 GHz and a Doppler frequency of 100 Hz, the 5082-2701, the usual mixer diode for this frequency, has a diode noise figure of 9 dB, the 5082-2750, the detector diode for this frequency, has a diode noise figure of 8 dB, and the 5082-2565, the 3 GHz mesh diode, has a diode noise figure of 7.5 dB. In this case, the detector diode would be better than the mixer diode and the S band mesh diode would be best of all.

Another technique for optimizing Doppler mixer performance is the adjustment of local oscillator level to trade off flicker noise for conversion efficiency. Figure 2 compared to Figure 1 shows how the flicker noise level drops with decreasing diode current. Unfortunately, conversion efficiency degrades as L.O. power drops. The optimum level is best found empirically. By optimizing the bias load line[4], further reductions in L.O. level are possible.

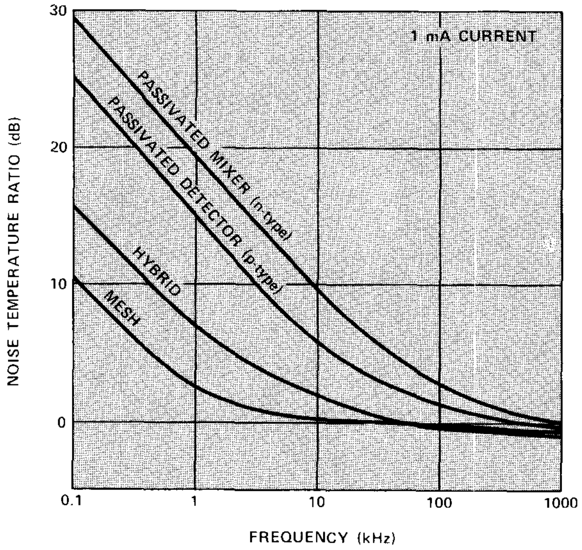


Figure 1. Typical Mixer Noise

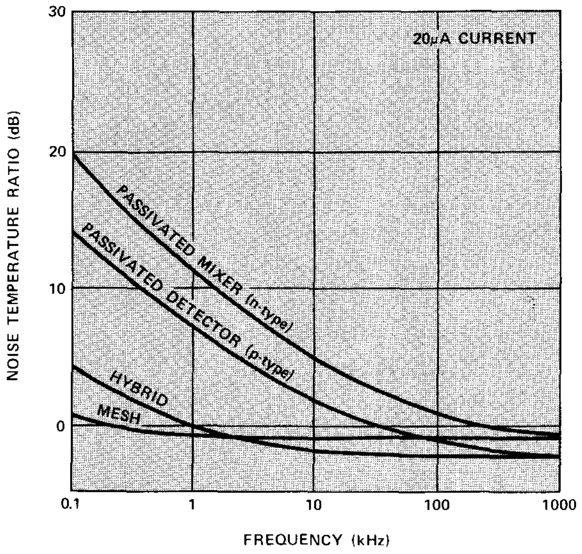


Figure 2. Typical Detector Noise

REFERENCES

1. A.M. Cowley and R.A. Zettler, "Shot Noise in Silicon Schottky Barrier Diodes", IEEE Transactions Electron Devices, Vol. ED-15, pp 761-769. October 1968.
2. H.A. Watson, Microwave Semiconductor Devices & Their Circuit Applications, McGraw-Hill, 1969, pp 378-379.
3. R.A. Zettler and A.M. Cowley, "PN Junction-Schottky Barrier Hybrid Diode", IEEE Trans. Electron Devices, Vol. ED-16, pp 58-63, Jan. 1969.
4. Carl W. Gerst, Jr., "New Mixer Designs Boost D/F Performance", Microwaves, Vol. 12, No. 10, October 1973, p. 60.

Dynamic Range Extension of Schottky Detectors (Application Note 956-5)

Detectors are essentially low sensitivity receivers which function on the basis of direct rectification of the RF signal through the use of a non-linear resistive element – a diode. Generally detectors can be classified into two distinct types: the small-signal type, also known as square-law detectors; and the large-signal type, also known as linear or peak detectors.

The small-signal detector operation is dependent on the slope and curvature of the VI characteristic of the diode in the neighborhood of the bias point. The output of the detector is proportional to the power input to the diode, that is, the output voltage (or current) is proportional to the square of the input voltage (or current), hence the term "square law" (see Figure 1).

The large-signal detector operation is dependent on the slope of the VI characteristic in the linear portion, consequently the diode functions essentially as a switch. In large-signal detection, the diode conducts over a portion of the input cycle and the output current of the diode follows the peaks of the input signal waveform with a linear relationship between the output current and the input voltage.

The square law dynamic range may be defined as the difference between the power input for 1dB deviation from the ideal square law response (compression point) and the power input corresponding to the tangential signal sensitivity (TSS).

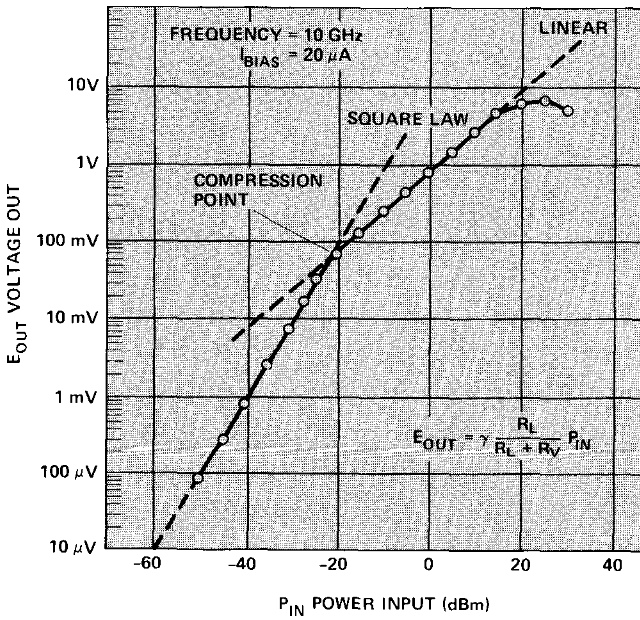


Figure 1. Typical Detector Output Voltage vs. Input Power.

Normal operating conditions for the Schottky detector call for a large load resistance (100KΩ) and a small bias current (20μA). These normal conditions assure the minimum value of TTS input level, but not the maximum value of compression level.

The compression level can be raised by reducing the value of R_L, the load resistance. However, the sensitivity degrades by the factor

$$\frac{R_L}{R_L + R_V},$$

where R_V is the diode's video resistance. This degradation in TSS exceeds the improvement in compression, so there is no improvement in square law dynamic range.

Another technique for raising the compression level is to increase the bias current. This also degrades the sensitivity, but the improvement in compression exceeds this degradation so square law dynamic range is increased.

Figure 2 illustrates the effect of bias current level on a Hewlett-Packard 5082-2751 detector, measured at 10 GHz. The diode impedance was matched to the 50 ohm system at each bias level. The tuner was adjusted at an input level of -30dBm.

The improvement in dynamic range is evident by the increased spacing between the TSS and compression curves.

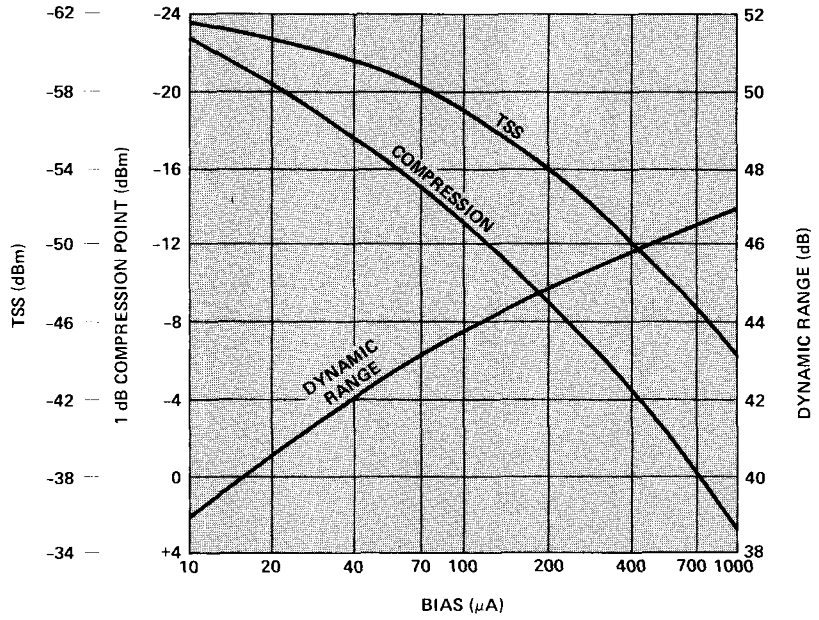


Figure 2. Dynamic Range Improvement with Bias.

Temperature Dependence of Schottky Detector Voltage Sensitivity

(Application Note 956-6)

Although Schottky barrier diodes are less sensitive to temperature changes than are point-contact diodes[1], the effect on detector voltage sensitivity may be significant. Performance improves at lower temperatures in a predictable manner. In fact, a second diode can be used in a compensating circuit[2] to cancel out the temperature effects.

Typical behavior of voltage sensitivity vs. temperature is shown in Figure 1. This spread of values (approximately 1dB) was obtained from 10 Hewlett-Packard 5082-2750 Schottky detector diodes chosen at random from 2 different lots.

The temperature dependence of current sensitivity was studied by Cowley and Sorensen[3], but the analysis was not extended to voltage sensitivity. For the ideal diode with infinite cutoff frequency (zero series resistance and/or zero junction capacitance) there is no temperature effect on voltage sensitivity. The inverse temperature behavior of current sensitivity is balanced by the direct temperature variation of the diode barrier resistance. That is, for current sensitivity:

$$\beta = \frac{q}{2\,nkT} = \frac{5400}{T} \qquad (1)$$

and for diode junction resistance:

$$R_j = \frac{nkT}{qI} = \frac{T}{11\,I} \qquad (2)$$

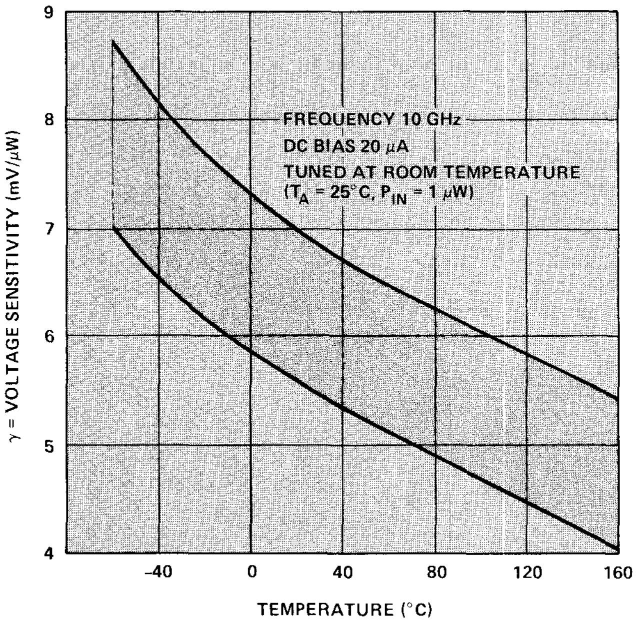


Figure 1. Typical Voltage Sensitivity vs. Temperature.

In these equations, T is temperature in degrees Kelvin, I is bias current in milliamperes and n, q, and k are constants[3]. When the load resistance is much greater than diode resistance, the voltage sensitivity, γ_o, is the product of current sensitivity and junction resistance and is independent of temperature:

$$\gamma_o = \beta R_j = \frac{490}{I} \tag{3}$$

In practical cases, however, the voltage sensitivity is reduced by the presence of both junction capacitance and series resistance, i.e.:

$$\gamma = \frac{\gamma_o}{1 + 4\pi^2 f^2 C_j^2 R_s R_j} \tag{4}$$

The temperature dependence shows up in the R_j term (equation 2). Using typical values of $I = .02\text{mA}$, $R_s = 25$ ohms, $C_j = 0.1\text{pF}$, and $f = 10$ GHz, the effect of temperature on voltage sensitivity is:

$$\gamma = \frac{\gamma_o}{1 + .0045\,T} \tag{5}$$

For a typical voltage sensitivity of 6.5mV/μW at T = 293°K, $\gamma_o = 15.1\text{mV}/\mu\text{W}$. Figure 2 shows this theoretical curve in excellent agreement with experimental data from a typical diode.

However, when f = 1 GHz, equation (4) predicts a response nearly independent of temperature:

$$\gamma = \frac{\gamma_o}{1 + 4.5T \times 10^{-5}} \tag{6}$$

Measurements at this frequency are not in good agreement with this prediction. Figure 3 shows considerable improvement in performance over temperature, but there is still a 25% variation.

A theoretical model of the temperature behavior of a Schottky detector is in excellent agreement with 10GHz measurements. Further refinement of the theory is necessary to extend the model to lower frequencies.

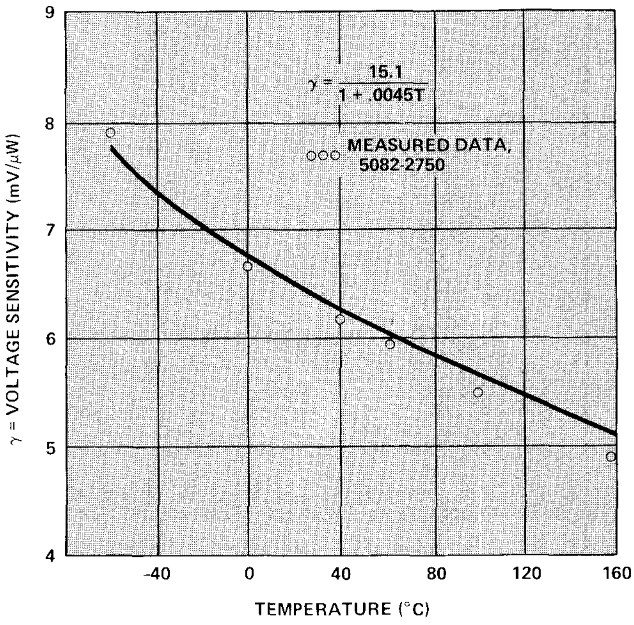


Figure 2. Voltage Sensitivity vs. Temperature at 10 GHz.

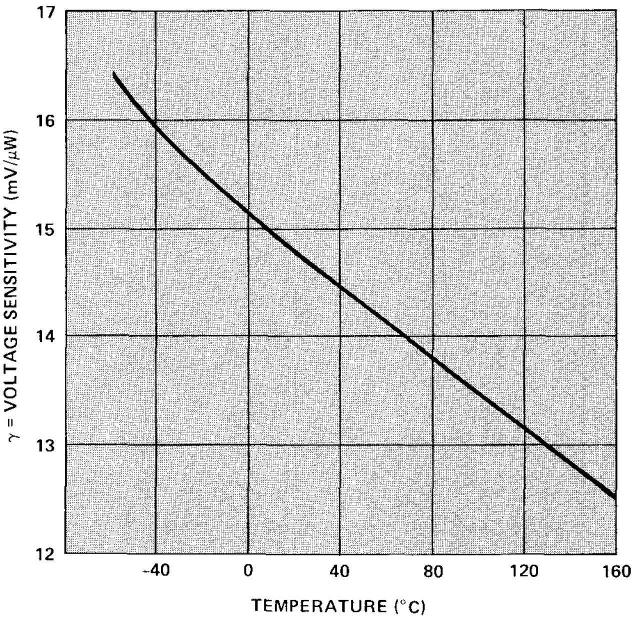


Figure 3. Voltage Sensitivity vs. Temperature at 1 GHz.

REFERENCES

1. R. Bayliss, et.al., "Why a Schottky-Barrier? Why a Point-Contact?", Microwaves, pp. 34-45, March 1968.
2. R.J. Turner, "Schottky Diode Pair Makes an rf Detector Stable", Electronics, pp. 94-95, May 2, 1974.
3. A.M. Cowley and H.O. Sorensen, "Quantitative Comparison of Solid-State Microwave Detectors", IEEE Trans. on MTT, Vol. MTT-14, No. 12, pp. 588-602, December 1966.

An Optimum Zero Bias Schottky Detector Diode (Portion of Application Note 969)

INTRODUCTION

A conventional Schottky diode detector such as the Hewlett-Packard 5082-2750 or 5082-2824 requires no bias for high level input power — above one milliwatt. However, at low levels, a small amount of dc bias is required for detection to take place. Even though this bias current is at the microampere level, this requirement is often difficult to supply. A new Schottky diode has been developed to eliminate this need for dc bias. This new diode is also 2 or 3 times more efficient as a detector compared to conventional biased detectors.

FORWARD VOLTAGE CHARACTERISTIC

Since all diodes in this discussion are Schottky diodes, the forward current obeys the equation:

$$I = I_S \left(e^{\frac{q}{nkT}(V - IR_S)} - 1 \right)$$

The ideality factor, n, is close to unity for these diodes, so the equation may be written:

$$I = I_S \left(e^{\frac{V - IR_S}{.026}} - 1 \right)$$

where the values for the constants q, electron charge, T, room temperature, and k, Boltzmann's constant, have been inserted. The main difference in the behavior of the different types of diodes is embodied in I_S, the saturation current. There may also be minor differences in R_S, the series resistance.

Figure 1 shows the forward current characteristics of the 5082-2750 detector diode and two versions of zero bias diodes, HSCH-3171 and HSCH-3486. These curves are close to the curves predicted by the diode equation with the constants shown in Table 1.

Table 1

Diode	I_S (amperes)	R_S (ohms)
5082-2750	7×10^{-10}	32
HSCH-3171	7×10^{-8}	15
HSCH-3486	6×10^{-6}	15

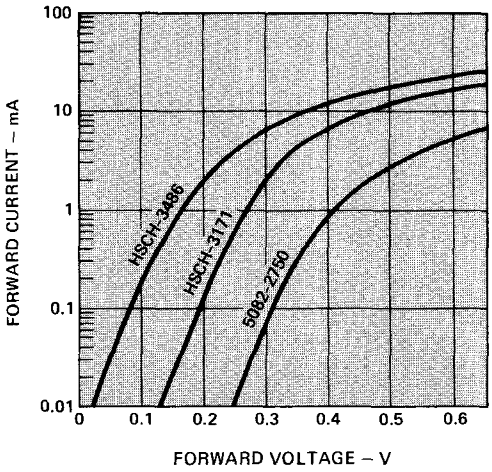


Figure 1. Forward Characteristics of Detector Diodes.

VOLTAGE SENSITIVITY

A detector diode may be treated as a current generator across the diode video resistance.(1) The voltage sensitivity, γ, is the product of the current sensitivity, β, and the video resistance, the inverse of the derivative of current with respect to voltage.

The Perfect Detector

Neglecting parasitic and reflection losses:

$$\gamma = \beta \,/\, \frac{\partial I}{\partial V}$$

For small values of current:

$$I = I_S \left(e^{\frac{V}{.026}} - 1 \right)$$

and $$\frac{\partial I}{\partial V} = \frac{I + I_S}{.026}$$

The theoretical current sensitivity is 20 amperes per watt(2) so:

$$\gamma = \frac{0.52}{I + I_S}$$

or, for zero bias current:

$$\gamma = \frac{0.52}{I_S}$$

This analysis indicates no improvement in using the new diodes because sensitivity varies inversely as saturation current and the standard 5082-2750 diode has the lowest saturation current. In fact, no improvement is needed since the sensitivity is:

$$\gamma = \frac{0.52}{7 \times 10^{-10}} = 750 \times 10^{6} \text{ volts per watt}$$

or 750,000 millivolts per microwatt.

Since the actual sensitivity of the 5082-2750 detector with zero bias is close to zero, some major corrections in the analysis are needed. Consideration of the effects of junction capacitance, load resistance, and reflection loss will bring this analysis close to reality.

The Real Detector

The application note considers these effects in some detail. They modify the value of sensitivity to the more reasonable levels shown in Figure 2.

The package parasitics of outlines 44, 49 and 15 were considered at 1, 3 and 10 GHz. The results were all quite close to Curve A in Figure 2 with the exception of outline 15 at 10 GHz. At this frequency the high package inductance of outline 15 nearly resonates the circuit capacitance so that the reflection losses are not so severe.

With the addition of tuning to overcome some of the reflection losses, the measured sensitivity of the Hewlett-Packard zero bias detectors usually exceeds the values of Figure 2. However, the reflection losses for the 5082-2750 detector are so great that tuners do not help much. These diodes are not useful without bias. The measured sensitivity of the HSCH-3486 is less than the value predicted by **Figure 2**. Apparently a more complete analysis would shift the curve to the left.

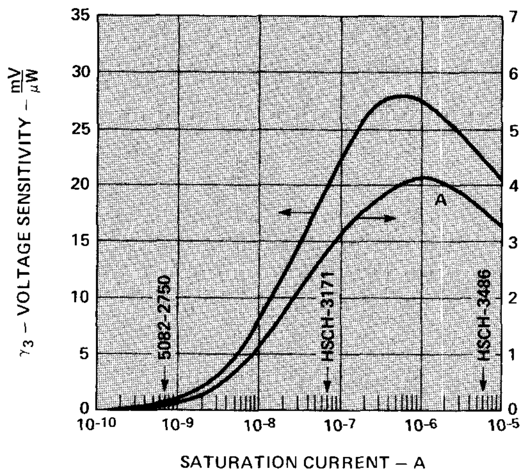


Figure 2. Effect of Mismatch, Load Resistance and Capacitance on Sensitivity.

TEMPERATURE EFFECT

Conventional Schottky diode detectors improve at colder temperatures. This behavior is similar to that of the HSCH-3486 diode. The sensitivity varies inversely as saturation current, improving at low temperatures. However, the HSCH-3171 diode has maximum sensitivity just above room temperature, degrading at cold as well as at hot temperatures. The high temperature behavior is expected from the higher value of saturation current. The low temperature behavior indicates that the room temperature value of saturation current is nearly optimum for this diode. At lower temperatures the reduced value of saturation current is not able to improve sensitivity because the corresponding large diode resistance causes a large mismatch loss which cannot be tuned out. At low temperatures, diode HSCH-3171 approaches the behavior of diode 5082-2750, the standard biased detector.

SUMMARY

Detector diodes are most sensitive at zero bias when the saturation current is small, corresponding to large video resistance. However, there is a limit to sensitivity when the resistance is so large that it cannot be matched. An optimum diode is designed to have the proper saturation current. Choice of saturation current involves a compromise between sensitivity due to large resistance and loss due to matching.

REFERENCES

1. Torrey, H. C. and Whitmer, C. A., "Crystal Rectifiers", MIT Radiation Laboratory Series, Vol. 15, McGraw-Hill (New York) 1948.
2. Watson, H. A., "Microwave Semiconductor Devices and Their Circuit Applications", p. 379, McGraw-Hill, 1969.

Transistor Speed Up Using Schottky Diodes (Portion of Application Bulletin 13)

NONSATURATING TRANSISTOR SWITCHES

The operation of a transistor switching circuit in the saturation region produces fast turn-on times, but slow turn-off times as a result of storage delay. Excess base current needed to drive the transistor into saturation causes an accumulation of stored charge in the base region, which must be removed before the transistor switch can turn off. Various schemes have been devised to overcome the storage delay and speed up switching time by not allowing the transistor to saturate and minimizing turn-off delay.

A very effective way of preventing saturation, using Hewlett-Packard diodes, is illustrated in the circuit in Figure 1.

Significant reduction in transistor switching delay time can be achieved by adding a Schottky diode (5082-2811), (or HSCH-1001) and a PIN diode (5082-3077) to the transistor switch.

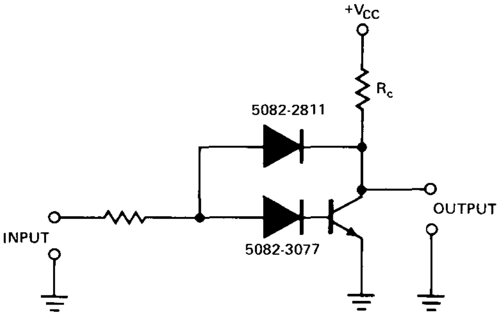


Figure 1. The Use of Diodes as Feedback Elements to Avoid Saturation in a Transistor Switch.

Waveform Clipping with Schottky Diodes (Portion of Application Bulletin 14)

CLIPPING CIRCUITS

Clipping circuits are used to restrict the transmission of a voltage waveform to that portion which lies above or below a specified reference voltage level. Because of their functions, they are sometimes referred to as voltage limiters or amplitude selectors.

Design requirements of clipping circuits and characteristics of diodes needed to achieve the required performance in these circuits are discussed in this application bulletin.

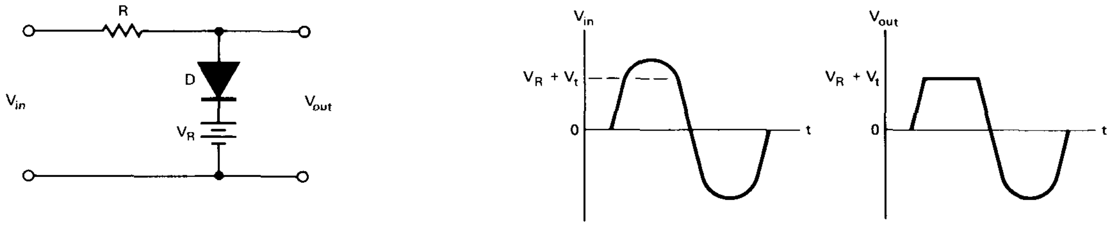


Figure 1. **Shunt Connected Diode Clipping Circuit for Clipping Top of Waveform.**

Waveform Clamping with Schottky Diodes (Portion of Application Bulletin 15)

CLAMPING CIRCUIT

In general, when a point in a circuit is connected through a low impedance path (such as through a forward biased diode) to a reference voltage V_R, that point is said to be clamped to V_R, since the voltage at that point cannot deviate very much from V_R, except perhaps for a small voltage drop across the diode. In this sense, diode clipping circuits are also clamping circuits.

A basic clamping circuit together with its input and output waveforms is illustrated in Figure 1. If the diode were removed, the output waveform would have both positive and negative swings from the dc level at zero regardless of the dc level of the input, because of the capacitor. The presence of the diode in the polarity shown permits only negative excursions of the output waveform with the positive peaks clamped at zero (or more precisely V_t volts above zero, if the diode drop is taken into account).

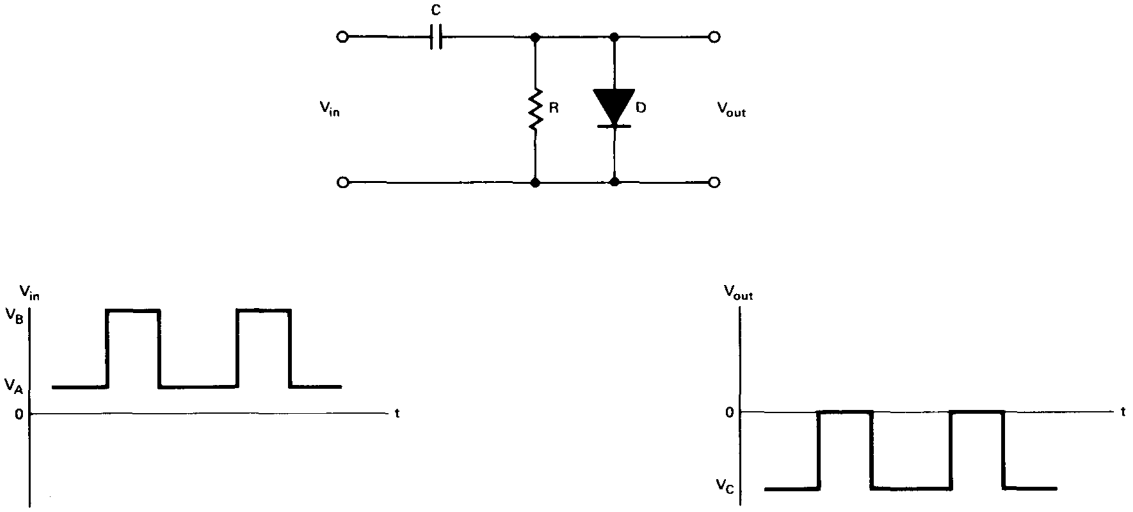


Figure 1. **Basic Clamping Circuit with Input and Output Waveforms.**

Waveform Sampling with Schottky Diodes (Portion of Application Bulletin 16)

SAMPLING GATE

This four diode sampling gate, shown in Figure 1 is the most commonly used. In a sampling system, it would be situated between the input source and the input capacitor of an amplifier. The diodes are normally reverse biased, so that the input signal does not cause them to conduct. Sampling is initiated with very narrow pulses, which overcome the reverse bias and switch the diodes into conduction. The low impedance paths allow the amplifier input capacitor to be charged to a voltage proportional to the input voltage.

Both dc and ac balance of the sampling gate bridge are essential in achieving the symmetry required for optimum performance of the sampler. The conditions of balance require that the four sampling diodes be matched, the two reverse bias voltages be equal and opposite, and the sampling gate control voltage be identical in waveshape except for polarity.

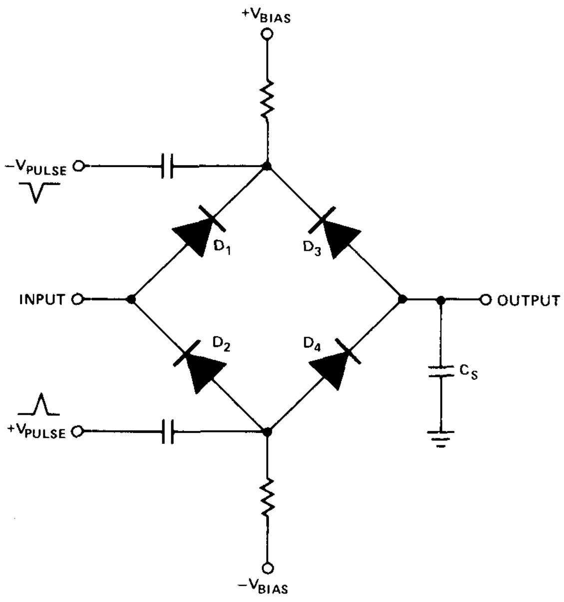
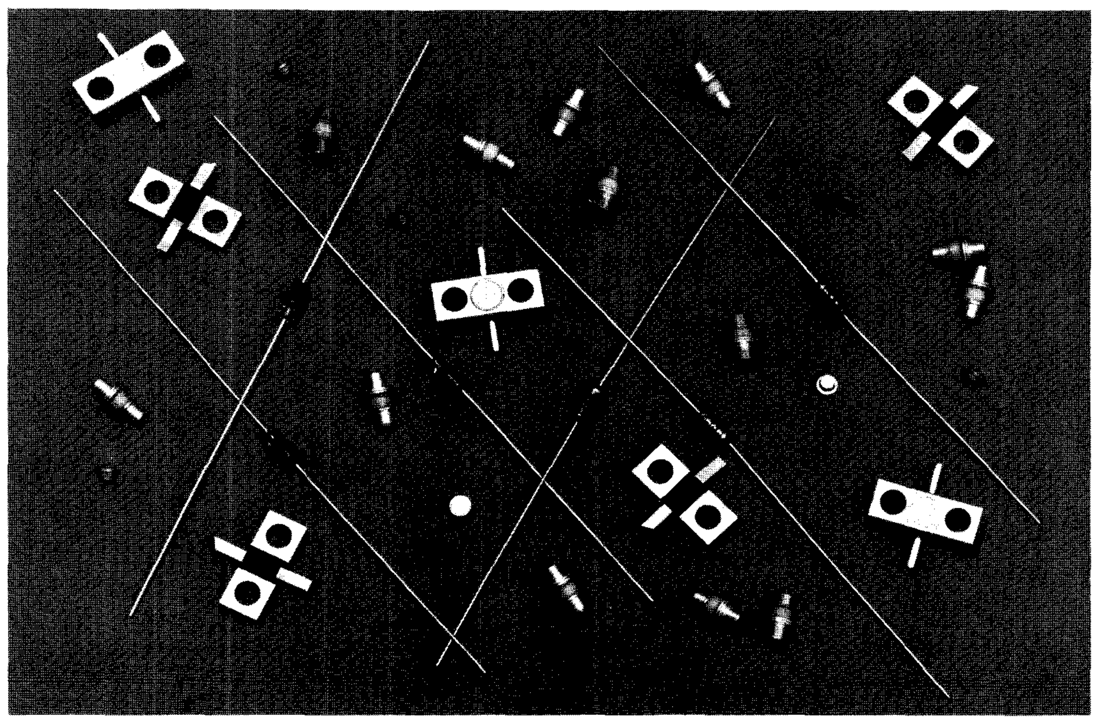


Figure 1. Four Diode Sampling Gate.

PIN Diodes



PIN Diodes Selection Guide

(Devices listed in the order of increasing junction capacitance)
All part numbers, 5082- (except HPND- as noted)

Typical Junction Capacitance C_{jVR} (pF) (Note 1)	Typical RF Resistance R_S (Ω) (Note 3)	Chip	Packaged Devices Containing Similar Chips (Package Outline)								
			Beam Lead (05)	LID (50)	Mini Strip (72)	Post (74)	Glass (15)	Ceramic (31)	Ceramic (38)	Stripline (60)	Stripline (61)
0.02***	6.0†		3900								
0.07	0.8	0012		3005	3000	3259	3001 3002 3039 3077 1N5719 HPND-4165 HPND-4166	3201 3202	3101 3102	3140	3040
0.07	0.8	0030			3309			3303 3304	3301 3302	3170	3340
0.07*	1.8†††		HPND-4001								
0.09	0.6	0047									
0.09	0.6	9882									
0.10	1.5	0025		3085	3086		3080 1N5767				
0.10	2.0	0039					3081				
0.12**	0.8††	0001		3045	3010	3258	3042 3043	3306	3305	3141	3041 3071
0.12	0.6	0049									3046
0.12**	1.3†††		HPND-4050								
0.8	0.4†††	0034					3168 3188				
Package Capacitance (pF)			(Note 2)	.18	.13	.13	.13	.2	.2	.03	.03
Pages		189	183	189	189	189	125	129	129	134	134

Notes:

1. All capacitance measured with $V_R = 50$ volts, except:
   *$V_R = 30$ volts
   **$V_R = 20$ volts
   ***$V_R = 0$ volt
2. Capacitance of beam lead devices includes package capacitance.
3. RF resistance measured with $I_F = 100$ mA, except:
   †$I_F = 50$ mA
   ††$I_F = 20$ mA
   †††$I_F = 10$ mA

HEWLETT PACKARD

COMPONENTS

PIN DIODES FOR RF SWITCHING AND ATTENUATING

5082-3001/02
HPND-4165/66 NEW
5082-3039(1N5719)
5082-3042/43
5082-3077
5082-3080(1N5767)
5082-3081
5082-3168/88

Features

LOW HARMONIC DISTORTION

LARGE DYNAMIC RANGE

LOW SERIES RESISTANCE

LOW CAPACITANCE

LOW TEMPERATURE COEFFICIENT
Typically Less Than 20% Resistance Change from 25°C to 100°C

Description / Applications

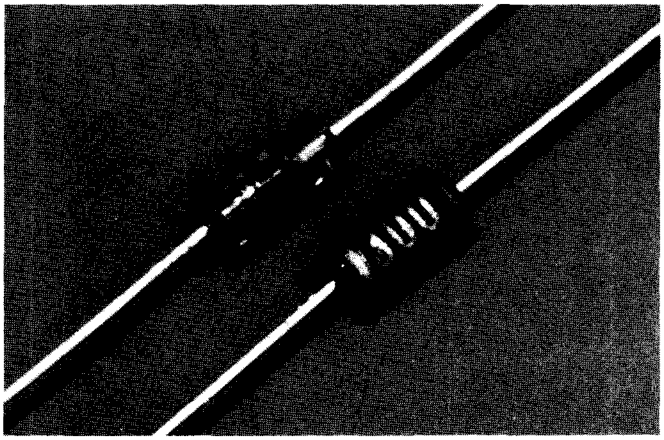
These general purpose switching diodes are intended for low power switching applications such as RF duplexers, antenna switching matrices, digital phase shifters, and time multiplex filters. The 5082-3168/3188 are optimized for VHF/UHF bandswitching.

The RF resistance of a PIN diode is a function of the current flowing in the diode. These current controlled resistors are specified for use in control applications such as variable RF attenuators, automatic gain control circuits, RF modulators, electrically tuned filters, analog phase shifters, and RF limiters.

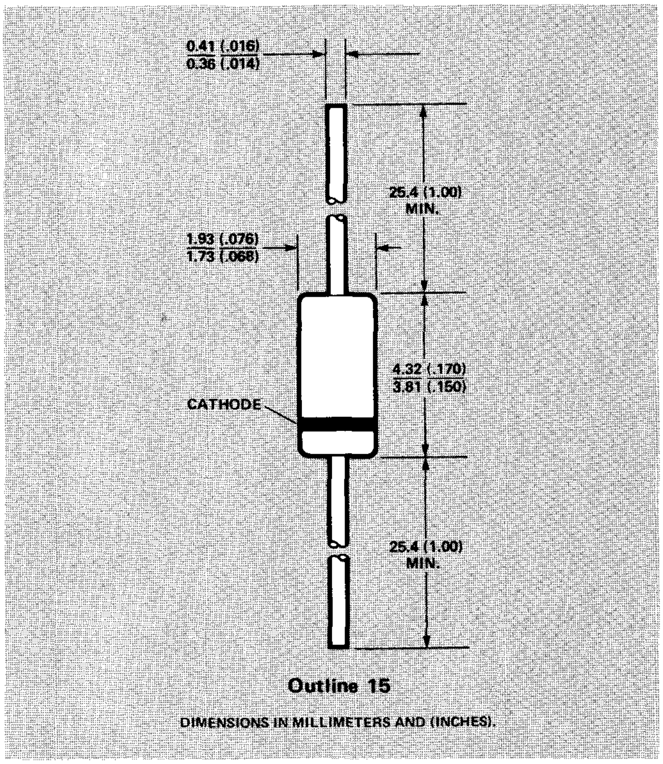
	Lead Finish	Body Finish
5082-3001/02	Tin	Painted
HPND-4165/66	Tin	Painted
5082-3039 (1N5719)	Tin	Painted
5082-3042/43	Gold	Painted
5082-3077	Tin	Clear
5082-3080 (1N5767)	Tin	Clear
5082-3081	Tin	Clear
5082-3168/88	Tin	Clear

Mechanical Specifications

The HP Outline 15 package has a glass hermetic seal with dumet leads. The leads on the Outline 15 package should be restricted so that the bend starts at least 1/16 inch (1.6mm) from the glass body. With this restriction, Outline 15 package will meet MIL-STD-750, Method 2036, Conditions A (4 lbs., [1.8 kg.], tension for 30 minutes) and E. The maximum soldering temperature is 230° C for five seconds. Typical package inductance and capacitance are 2.5 nH and 0.13pF, respectively. Marking is by digital coding with a cathode band.



Package Dimensions



Outline 15

DIMENSIONS IN MILLIMETERS AND (INCHES).

Maximum Ratings at $T_{CASE} = 25°C$

Junction Operating and Storage Temperature Range .... -65°C to +150°C

Operation of these devices within the above temperature ratings will assure a device Mean Time Between Failure (MTBF) of approximately 1 x 10^7 hours.

Power Dissipation 250mW
(Derate linearly to zero at 150°C)

Peak Inverse Voltage (PIV) .... V_{BR}

General Purpose Diodes
Electrical Specifications at $T_A = 25°C$

	Part Number 5082-	Maximum Total Capacitance C_T (pF)	Minimum Breakdown Voltage V_{BR} (V)	Maximum Residual Series Resistance R_S (Ω)	Minimum Effective Carrier Lifetime τ (ns)	Maximum Reverse Recovery Time t_{rr} (ns)
	GENERAL PURPOSE SWITCHING AND ATTENUATING					
£9.94	3002	0.2	300	1.0	100	100 (typ)
£9.00	3001	0.25	200	1.0	100	100 (typ)
£4.16	3039	0.25	150	1.25	100	100 (typ)
£4.16	IN5719	0.3**	150	1.25	100	100 (typ)
£2.08	3077	0.3	200	1.5	100	100 (typ)
	FAST SWITCHING					
£9.00	3042	0.4*	70	1.0*	15 (typ)	5
£5.65	3043	0.4*	50	1.5*	15 (typ)	10
	BAND SWITCHING					
£0.56	3188	1.0*	35	0.6**	40 (typ)	12 (typ)
£0.47	3168	2.0*	35	0.5**	40 (typ)	12 (typ)
	Test Conditions	$V_R = 50V$ $*V_R = 20V$ $**V_R = 100V$ f = 1 MHz	$V_R = V_{BR}$ Measure $I_R \leqslant 10\mu A$	$I_F = 100mA$ $*I_F = 20mA$ $**I_F = 10mA$ f = 100 MHz	$I_F = 50mA$ $I_R = 250mA$	$I_F = 20mA$ $V_R = 10V$ 90% Recovery

Note: Typical CW power switching capability for a shunt switch in a 50Ω system is 2.5W.

RF Current Controlled Resistor Diodes
Electrical Specifications at $T_A = 25°C$

	Part Number	Minimum Effective Carrier Lifetime τ	Minimum Breakdown Voltage V_{BR}	Maximum Residual Series Resistance R_S	Maximum Total Capacitance C_T	High Resistance Limit, R_H		Low Resistance Limit, R_L		Maximum Difference in Resistance vs. Bias Slope, Δx
						Min.	Max.	Min.	Max.	
	HPND-4165	100	100	1.5	0.3	1100	1660	16	24	.04
	HPND-4166	100	100	1.5	0.3	830	1250	12	18	.04
£1.89	5082-3080*	1300(typ)	100	2.5	0.4	1000	–		8**	
£2.11	5082-3081	2000(typ)	100	3.5	0.4	1500			8**	
	Units	ns	V	Ω	pF	Ω		Ω		–
	Test Conditions	$I_F = 50mA$ $I_R = 250mA$	$V_R = V_{BR}$, Measure $I_R \leqslant 10\mu A$	$I_F = 100mA$ f=100mHz	$V_R = 50V$ f=1mHz	$I_F = 0.01mA$ f=100mHz		$I_F = 1.0mA$ $**I_F = 20mA$ f=100mHz		Batch Matched at $I_F = 0.01mA$ and 1.0mA f=100mHz

*The 1N5767 has the additional specifications:
τ = 1.0 µsec minimum
I_R = 1 µA maximum at $V_R = 50V$
V_F = 1V maximum at $I_F = 100mA$.

Typical Parameters

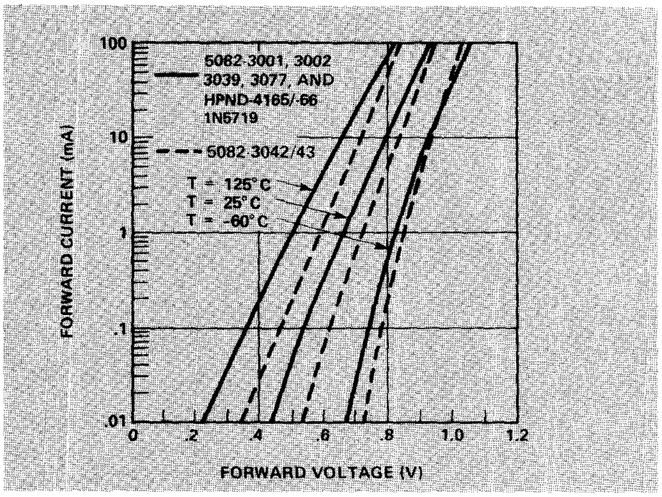


Figure 1. Typical Forward Current vs. Forward Voltage.

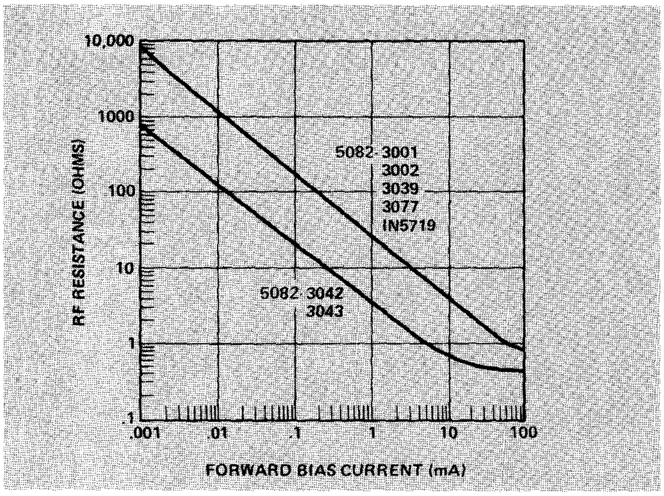


Figure 2. Typical RF Resistance vs. Forward Bias Current.

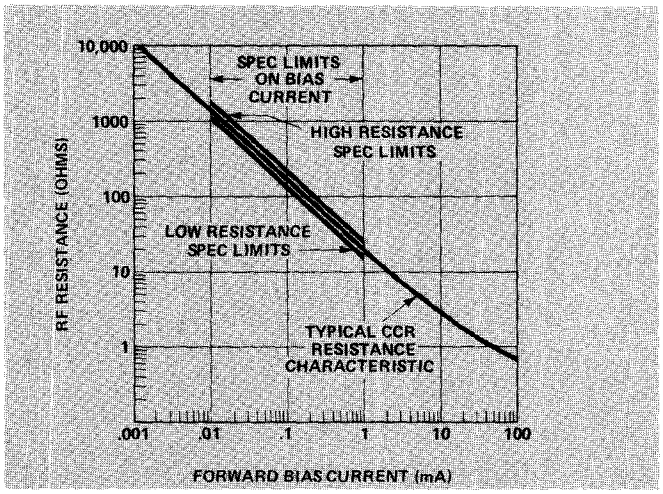


Figure 3. Typical RF Resistance vs. Bias for HPND-4165.

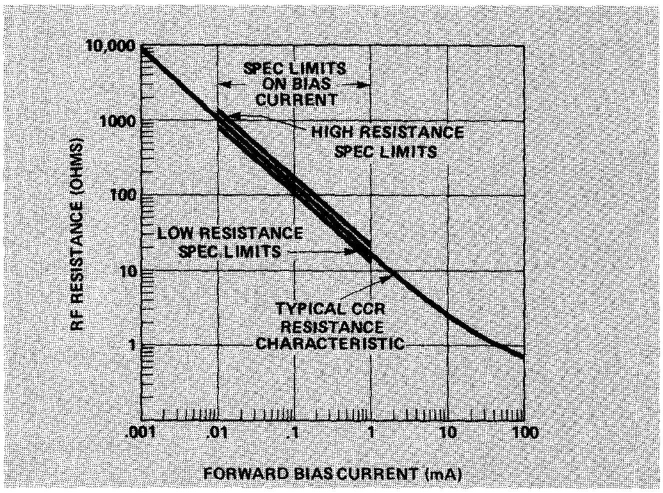


Figure 4. Typical RF Resistance vs. Bias for HPND-4166.

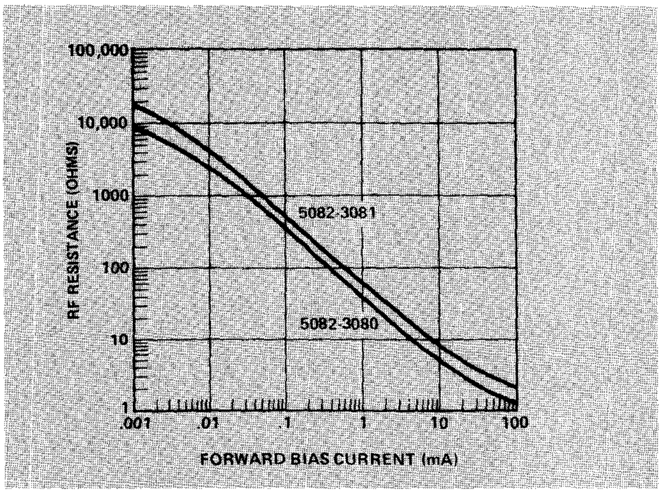


Figure 5. Typical RF Resistance vs. Forward Bias Current.

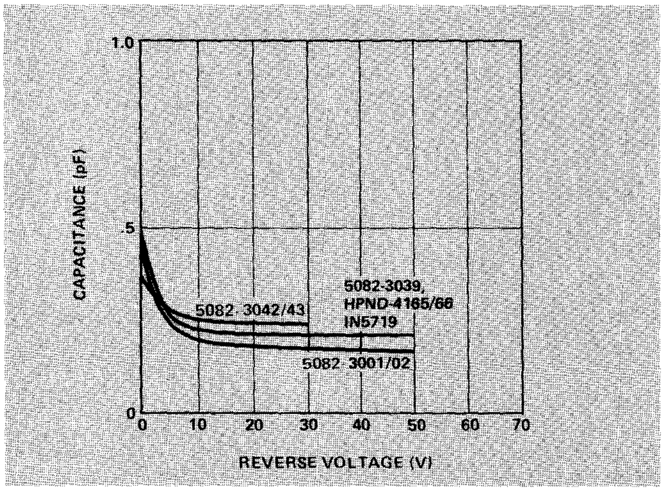


Figure 6. Typical Capacitance vs. Reverse Voltage.

Typical Parameters (Continued)

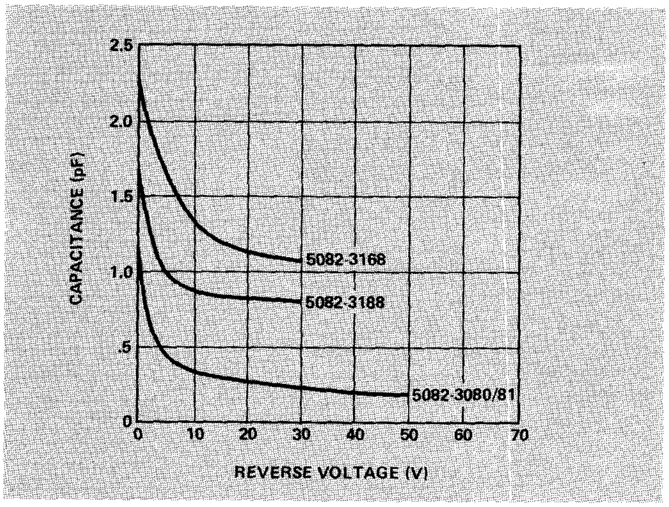


Figure 7. Typical Capacitance vs. Reverse Voltage 5082-3080, 3081, 3168, 3188.

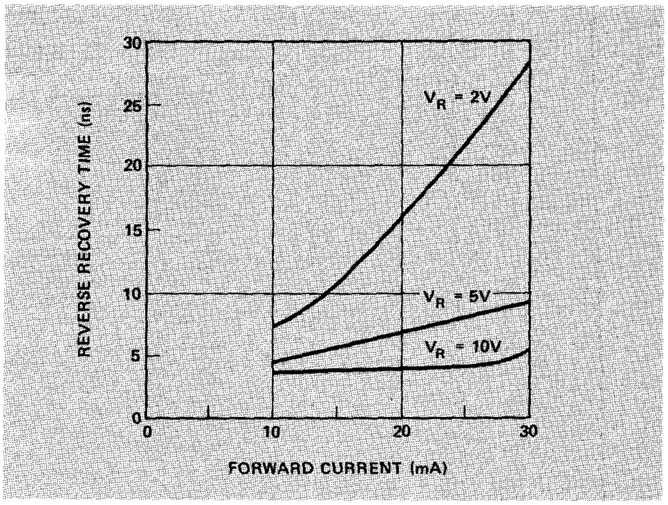


Figure 8. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages, 5082-3042, 3043.

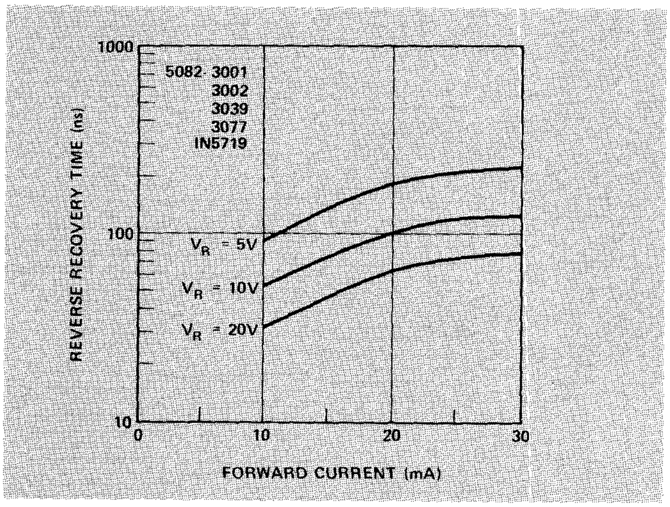


Figure 9. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages.

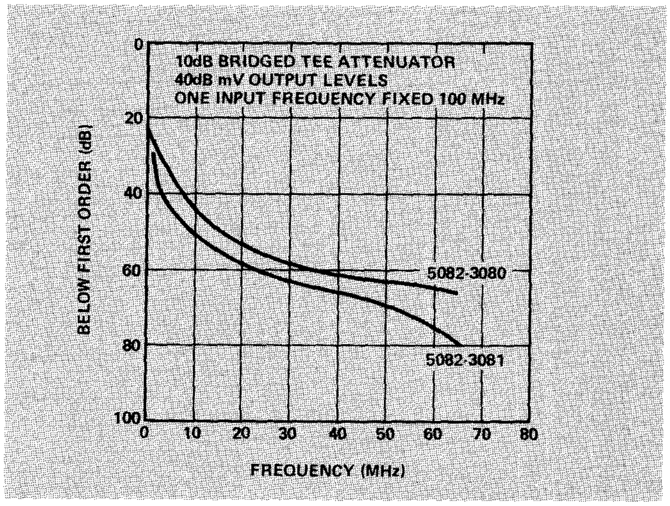


Figure 10. Typical Second Order Intermodulation Distortion.

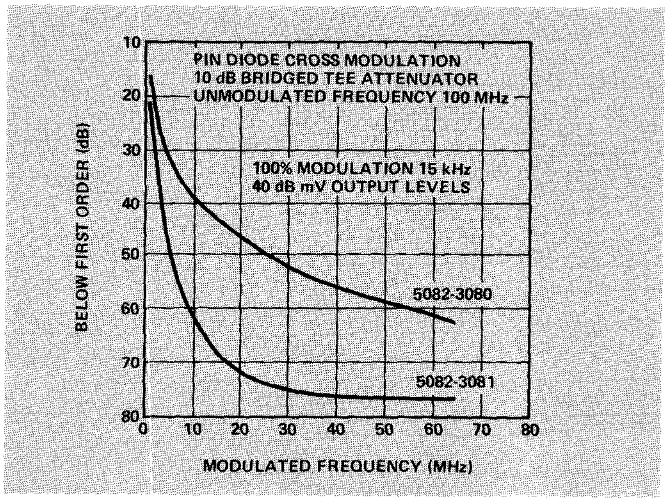


Figure 11. Typical Cross Modulation Distortion.

HEWLETT PACKARD
COMPONENTS

PIN DIODES FOR FAST SWITCHING RF POWER SWITCHING AND ATTENUATION

5082-3101/02
5082-3201/02
5082-3301/02
5082-3303/04
5082-3305/06

RF POWER SWITCHING/ATTENUATING

Features

- **HIGH ISOLATION**
  Greater Than 25 dB
- **LOW INSERTION LOSS**
- **HIGH CONTROL SIGNAL DYNAMIC RANGE**
  10,000: 1 RF Resistance Change
- **LOW HARMONIC DISTORTION LIFETIME**
  Greater Than 100 ns
- **BOTH ANODE AND CATHODE HEAT SINK MODELS AVAILABLE**

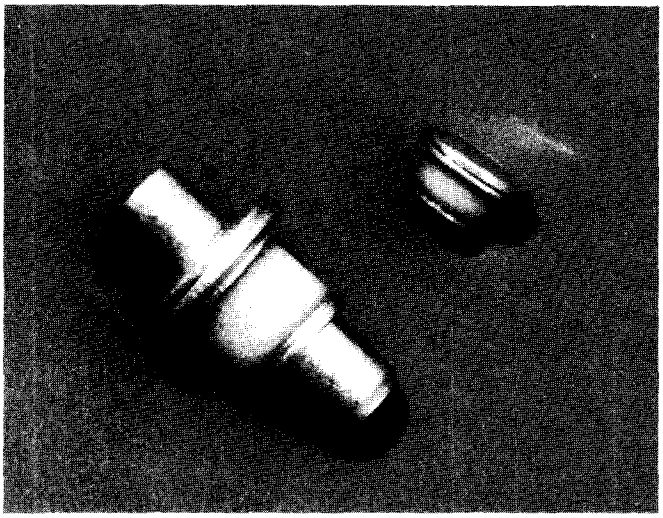
Description/Applications

HP 5082-3101/02, 5082-3201/02, 5082-3301/02/03/04 PIN diodes are silicon devices manufactured using modern processing techniques to provide optimum characteristics for RF switching, signal conditioning and control. These devices are of planar passivated design. Both anode and cathode heat sink models are available.

PIN diodes provide a variable RF resistance with DC bias current. The main advantages of a PIN diode over PN switching diodes are the low forward resistance and the low device capacitance.

These HP PIN Diodes are intended for use in RF switching, multiplexing, modulating, phase shifting, and attenuating applications from approximately 10 MHz to frequencies well into the microwave region. Due to their low parasitic capacitance and inductance, both HP Package Outline 31 and 38 are well suited for broadband circuits up to 1 GHz and for resonated circuits up to 8 GHz. Broad band designs above 1 GHz are usually more economical using stripline PIN diodes (HP Package Outlines 60 and 61) or devices for microstrip circuits (HP Package Outlines 72 and 74).

These devices are especially useful where the lowest residual series resistance and junction capacitance are required for high on-to-off switching ratios. At constant bias the RF resistance is relatively insensitive to temperature, increasing only 20% for a temperature change from +25°C to +100°C.



FAST SWITCHING/ATTENUATING

Features

- **NANOSECOND SWITCHING TIME**
  Typically Less Than 5 ns
- **LOW RESIDUAL SERIES RESISTANCE**
  Less Than 1Ω
- **LOW DRIVE CURRENT REQUIRED**
  Less Than 20 mA for 1Ω R_S
- **CATHODE HEAT SINK**

Description/Applications

The HP 5082-3305 and 5082-3306 are passivated silicon PIN diodes of mesa construction. Precisely controlled processing provides an exceptional combination of fast RF switching and low residual series resistance.

These HP PIN diodes provide unique benefits in the high isolation to insertion loss ratio afforded by the low residual resistance at low bias currents and the ultra-fast recovery realized through lower stored charge. Where low drive power is desired these diodes provide excellent performance at very low bias currents.

The HP 5082-3305 and 5082-3306 ceramic package PIN diodes are intended for controlling and processing microwave signals up to Ku band. Typical applications include single and multi-throw switches, pulse modulators, amplitude modulators, phase shifters, duplexers, diplexers and TR switches.

Maximum Ratings at T_{CASE} = 25°C

Junction Operating and Storage Temperature Range .... -65°C to +150°C

Operation of these devices within the above temperature ratings will assure a device Mean Time Between Failure (MTBF) of approximately 1 x 10^7 hours.

DC Power Dissipation (Derate linearly to zero at 150°C)

HP 5082-3305	0.7 W
HP 5082-3306	1.25W
HP 5082-3101, 3102, 3301, 3302	1.0 W
HP 5082-3201, 3202, 3303, 3304	3.0 W

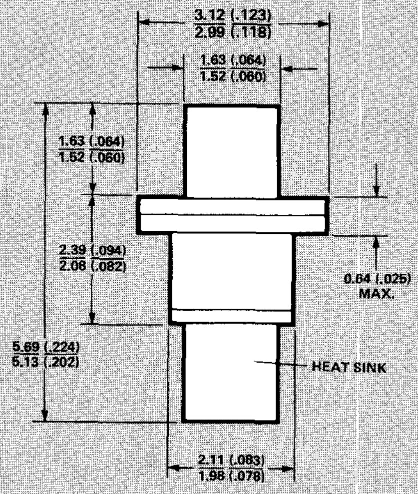
Mechanical Specifications

The HP Package Outline 31 has a metal ceramic hermetic seal. The heat sink stud is gold-plated copper. The opposite stud is gold-plated kovar. Typical package inductance is 1.0 nH and typical package capacitance is 0.2 pF.

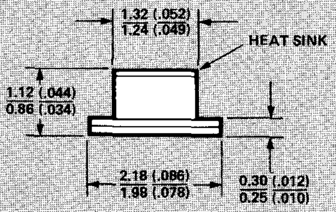
The HP Package Outline 38 also has a metal ceramic hermetic seal. The heat sink contact is gold plated copper. The opposite contact is gold-plated kovar. Typical package inductance is 0.4 nH and typical package capacitance is 0.2 pF.

The maximum soldering temperature for diodes in either package is 230°C for 5 seconds.

Package Dimensions



Outline 31



Outline 38

DIMENSIONS IN MILLIMETERS AND (INCHES).

RF POWER SWITCHING/ATTENUATING
Electrical Specifications at $T_A = 25°C$

Part Number 5082-	Package Outline	Heat Sink	Minimum Breakdown Voltage V_{BR}	Maximum Total Capacitance C_T	Maximum Residual Series Resistance R_S	Minimum Carrier Lifetime τ	Typical Reverse Recovery Time t_{rr}	Typical CW Power Handling Capability P_A
3101	38	Anode 13.69	200	0.32	1.2	100	150	40
3102	38	17.08	300	0.30	0.8	100	150	60
3201	31	13.69	200	0.35	1.2	100	150	120
3202	31	17.08	300	0.32	0.8	100	150	180
3301	38	Cathode 13.69	200	0.40	1.2	100	150	40
3302	38	17.08	300	0.32	0.8	100	150	60
3303	31	13.69	200	0.40	1.2	100	150	120
3304	31	17.08	300	0.32	0.8	100	150	180
Units			V	pF	Ω	ns	ns	W
Test Conditions			$V_R = V_{BR}$, meas. $I_R \leq 10\mu A$	$V_R = 50V, f = 1MHz$	$I_F = 100mA$ $f = 100MHz$	$I_F = 50mA$ $I_R = 250mA$	$I_F = 20mA$, $V_R = 10V$ 90% Recovery	Series* Switch in 50Ω System

*Divide by four for a shunt switch.

FAST SWITCHING/ATTENUATING
Electrical Specifications at $T_A = 25°C$

Part Number 5082-	Package Outline	Heat Sink	Minimum Breakdown Voltage V_{BR}	Maximum Total Capacitance C_{VR}	Maximum Series Resistance R_S	Maximum Reverse Recovery Time t_{rr}
3305	38 13.66	Cathode	70	0.4	1.0	10.0
3306	31		70	0.45	1.0	10.0
Units			V	pF	Ω	ns
Test Conditions			$V_R = V_{BR}$, meas. $I_R \leq 10\,\mu A$	$f = 1$ MHz $V_R = 20V$	$f = 100$ MHz $I_F = 20mA$	$I_F = 20mA$ $V_R = 10V$ 90% Recovery

FAST SWITCHING/ATTENUATING
Typical Parameters (5082-3305 and -3306)

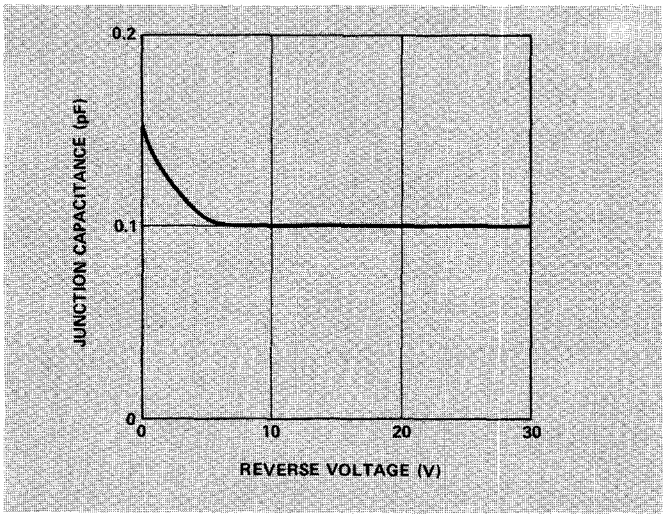


Figure 1. Typical Junction Capacitance vs. Reverse Voltage.

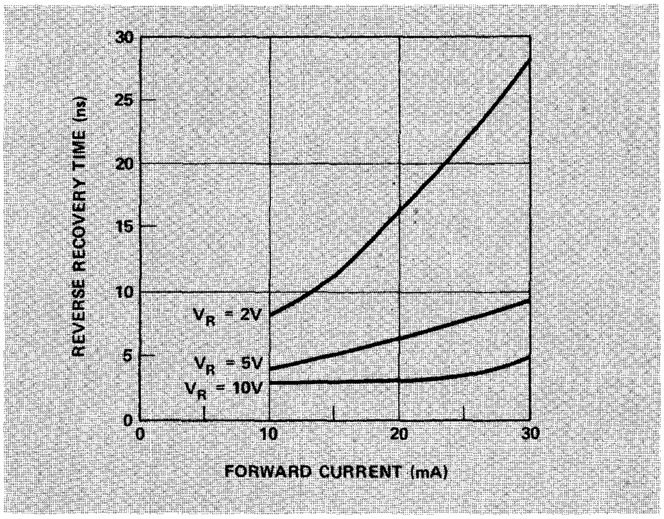


Figure 2. Typical Reverse Recovery Time vs. Forward Current for *Various Reverse Driving Voltages. For further discussion of* switching characteristics, see 5082-3041 data sheet.

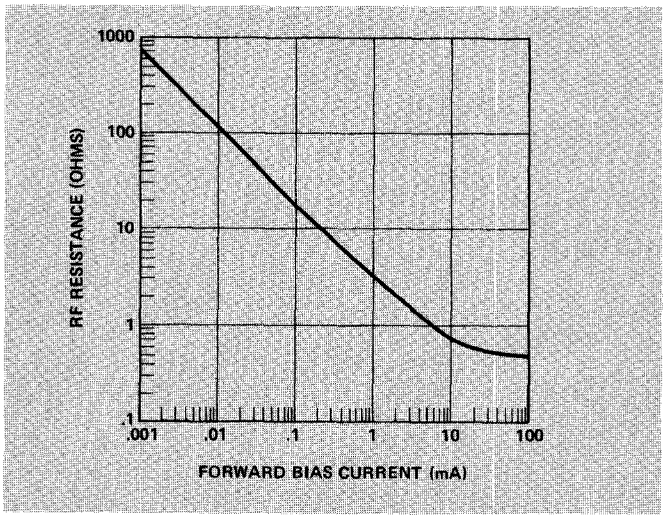


Figure 3. Typical RF Resistance vs. Forward Bias Current.

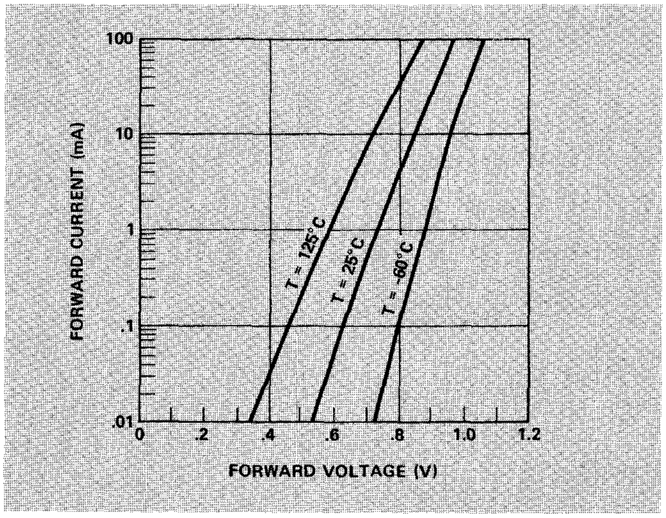


Figure 4. Typical Forward Current vs. Forward Voltage.

RF POWER SWITCHING/ATTENUATING

Typical Parameters (5082-3101, -3102, -3201, -3202, -3301, -3302, -3303, -3304)

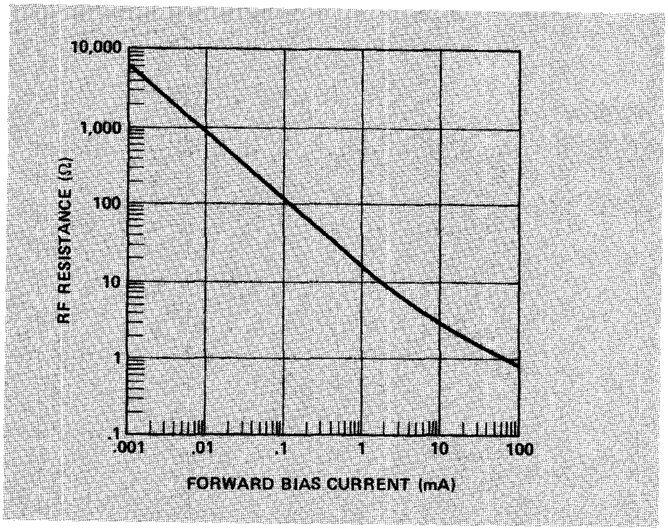


Figure 5. Typical RF Resistance vs. Forward Bias Current.

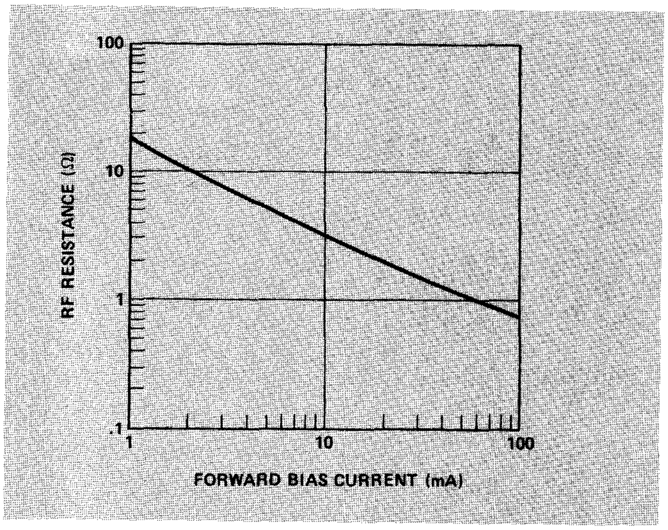


Figure 6. Typical RF Resistance vs. Forward Bias Current.

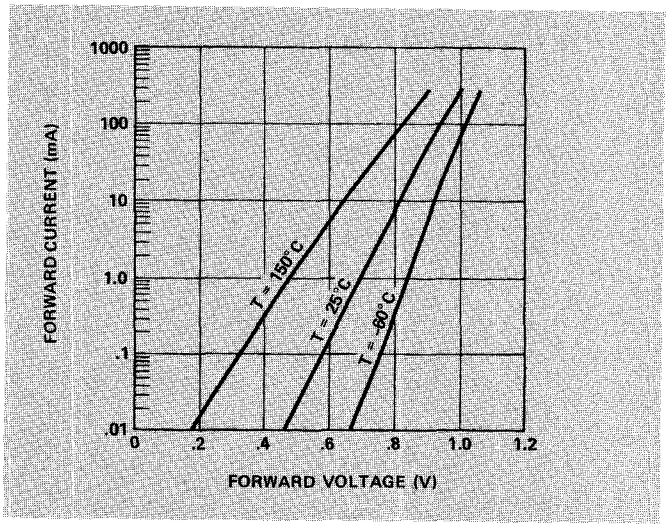


Figure 7. Typical Forward Characteristics.

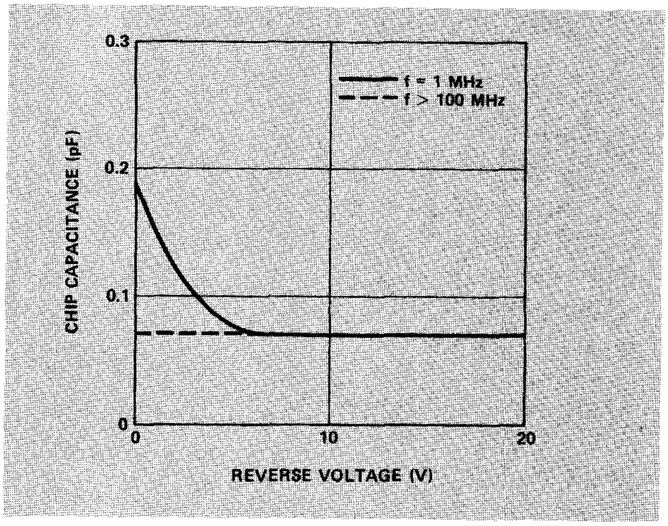
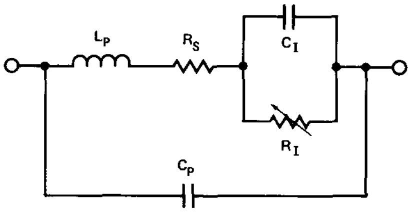


Figure 8. Typical Chip Capacitance vs. Reverse Voltage.



C_P = Package Capacitance
L_P = Package Inductance
R_S = Residual Series Resistance
R_I = I-Layer Resistance
C_I = I-Layer Capacitance

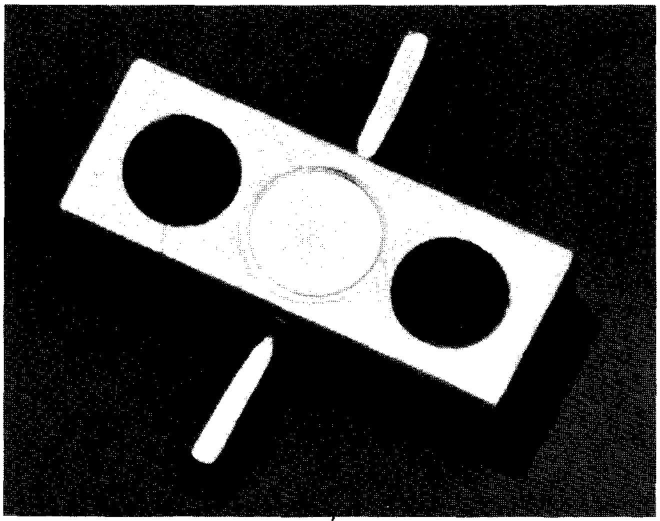
TYPICAL VALUES FOR C_P AND L_P ARE GIVEN UNDER "MECHANICAL SPECIFICATIONS". WITH REVERSE BIAS, $R_I \cong 10k\ \Omega$. TOTAL CAPACITANCE IS C_T AND IS GIVEN IN "ELECTRICAL SPECIFICATIONS". WITH FORWARD BIAS C_I IS NO LONGER PRESENT. R_I DECREASES WITH INCREASING FORWARD BIAS TO APPROXIMATELY ZERO AT 100 mA.

Figure 9. Device Equivalent Circuit.

HEWLETT hp PACKARD
COMPONENTS

PIN DIODES FOR STRIPLINE AND MICROSTRIP SWITCHES ATTENUATORS AND LIMITERS

5082-3040/41
5082-3046
5082-3071
5082-3140/41
5082-3170
5082-3340



Features

HERMETIC
(5082-3140, 3141, 3170)

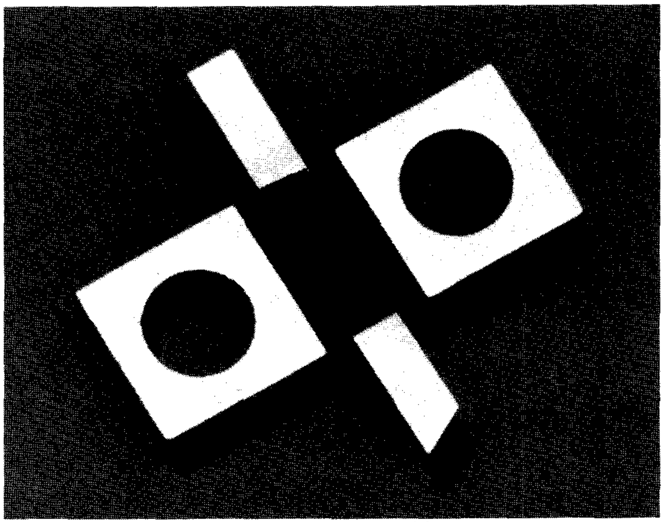
BROADBAND OPERATION
HF through X-band

LOW INSERTION LOSS
Less than 0.5 dB to 10 GHz (5082-3140, 3170)

HIGH ISOLATION
Greater than 20 dB to 10 GHz (5082-3140, 3170)

FAST SWITCHING/MODULATING
5 ns typical (5082-3141)

LESS DRIVE CURRENT REQUIRED
Less than 20 mA for 20 dB isolation (5082-3141)



Features

LOW COST TO USE
Designed for easy mounting

BROADBAND OPERATION
HF through Ku-band

LOW INSERTION LOSS
Less than 0.5 dB to 10 GHz (5082-3040, 3340)

LOW DRIVE CURRENT REQUIRED
Less than 20 mA for 20 dB isolation (5082-3041)

FAST SWITCHING MODULATION
5 ns typical (5082-3041)

HIGH POWER LIMITING
50 W peak pulse power (5082-3071)

Description

When forward biased these PIN diodes will appear as current variable resistors in shunt with a 50 ohm transmission line. The resistance varies between less than 1 ohm at high forward bias to greater than 10,000 ohms at zero or reverse bias.

The HP 5082-3040, -3046, -3340, -3140 and -3170 are passivated planar devices. The HP 5082-3041, -3071 and -3141 are passivated mesa devices. All of the devices are in a shunt configuration in stripline packages. These diodes are optimized for good continuity of characteristic impedance which allows a continuous transition when used in 50 ohm microstrip or stripline circuits.

Of these devices, the HP 5082-3040, -3041, -3046, -3071 and -3340 are in HP Package Outline 61.

The HP 5082-3140, -3141 and -3170 are in HP Package Outline 60. This package is hermetic and can be used for Hi-Rel applications. The HP 5082-3140, -3141 and -3170 are direct mechanical replacements for Outline 61 (with top cap in place) diodes HP 5082-3040, -3041, and -3340 respectively. The only electrical difference is the location of the chip in each package. Except in those few applications where the difference in phase relationship is important, the Outline 60 devices can be used as replacements.

The HP 5082-3071 passive limiter chip is functionally integrated into a 50 ohm transmission line to provide a broadband, linear, low insertion loss transfer characteristic for small signal levels. At higher signal levels self-rectification reduces the diode resistance to provide limiting as shown in Figure 6. Limiter performance is practically independent of temperature over the rated temperature range.

Applications

SWITCHES/ATTENUATORS

These diodes are designed for applications in microwave and HF-UHF systems using stripline, or microstrip transmission line techniques.

Typical circuit functions performed consist of switching, duplexing, multiplexing, leveling, modulating, limiting, or gain control functions as required in TR switches, pulse modulators, phase shifters, and amplitude modulators operating in the frequency range from HF through Ku-Band.

These diodes provide nearly ideal transmission characteristics from HF through Ku-Band.

The 5082-3340 and 4082-3170 are reverse polarity devices with characteristics similar to the 5082-3040 and 5082-3140 respectively.

The 5082-3041 and 5082-3141 are recommended for applications requiring fast switching or high frequency modulation of microwave signals, or where the lowest bias current for maximum attenuation is required.

The 5082-3046 has been developed for high peak pulse power handling as required in TR switches for distance measurement and TACAN equipment. The long effective minority carrier lifetime provides for low intermodulation products down to 10 MHz.

More information is available in HP Application Note 922 (Applications of PIN Diodes) and 929 (Fast Switching PIN Diodes).

LIMITER

The 5082-3071 limiter module is designed for applications in telecommunication equipment, ECM receivers, distance measuring equipment, radar receivers, telemetry equipment, and transponders operating anywhere in the frequency range from 500 MHz through 10 GHz. An external dc return is required for self bias operation. This dc return is often present in the existing circuit, i.e. inductively coupled antennas, or it can be provided by a $\lambda/4$ resonant shunt transmission line. Selection of a high characteristic impedance for the shunt transmission line affords broadband operation. Another easy to realize dc return consists of a small diameter wire connected at a right angle to the electric field in a microstrip or stripline circuit. A 10 mA forward current will actuate the PIN diode as a shunt switch providing approximately 20 dB of isolation.

HP Package Outline 61 Cover Channel

The cover channel supplied with each diode should be used in balanced stripline circuits in order to provide good electrical continuity from the upper to the lower ground plane through the package base metal. Higher order modes will be excited if this cover is left off or if poor electrical contact is made to the ground plane.

The package transmission channel is filled with epoxy resin which combines a low expansion coefficient with high chemical stability.

Maximum Ratings at $T_{CASE} = 25°C$

Part No. 5082-	-3140 24.84 -3170 "	24.84 -3141	-3040 22.36 -3340 "	22.36 -3041	24 57 -3046	33.22 -3071
Junction Operating and Storage Temperature Range	-65°C to 150°C	-65°C to 150°C	-65°C to 125°C	-65°C to 125°C		
Power Dissipation[1]	2.5 W	1.0 W	2.5 W	1.0 W	4.0 W	1.0 W
Peak Incident Pulse Power[2]	225 W	50 W	225 W	50 W	2000 W	50 W
Peak Inverse Voltage	150 V	70 V	150 V	70 V	450 V	50 V
Soldering Temperature	230°C for 5 sec.					

Notes:

1. Device properly mounted in sufficent heat sink, derate linearly to zero at maximum operating temperature.
2. $t_p = 1\ \mu s$, f = 10 GHz, Du - .001, $Z_o = 50\Omega$. (Exception: -3071 is tested at 9.4 GHz.)

Electrical Specifications at $T_A = 25°C$ - Attenuator Diodes

	Part Number 5082-	Package Outline	Heat Sink	Minimum Isolation (dB)	Maximum Insertion Loss (dB)	Maximum SWR	Maximum Reverse Recovery Time t_{rr} (ns)	Typical Carrier Lifetime τ (ns)	Typical CW Power Switching Capability P_A (W)
24.84	3140	60	Anode	20	0.5	1.5	–	500	30
24.84	3141	60	Cathode	20	1.0	1.5	10	15	13
24.84	3170	60	Cathode	20	0.5	1.5	–	500	30
7-36	3040	61	Anode	20	0.5	1.5	–	500	30
36	3041	61	Cathode	20	1.0	1.5	10	15	13
20.55	3046	61	Anode	20	1.0	1.5	–	1000	50
22.36	3340	61	Cathode	20	0.5	1.5	–	500	30
	Test Conditions (Note 3)	–	–	I_F=100mA (Except 3041,3141; I_F=20mA)	$I_F = 0$ P_{in} = 1mW	$I_F = 0$ P_{in} = 1mW	I_F = 20mA V_R = 10V Recovery to 90%	I_F = 50mA I_R = 250mA	–

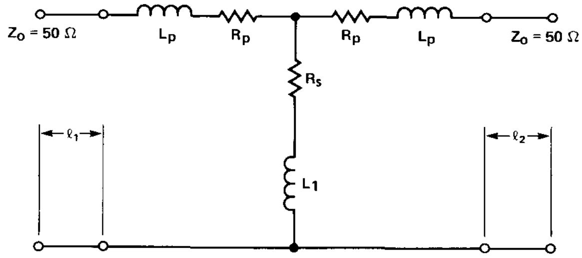
Note 3: Test Frequencies: 8 GHz 5082-3041, -3046 and -3141. 10 GHz 5082-3040, -3140, 3170 and -3340.

Electrical Specifications at $T_A = 25°C$ - Limiter Diode

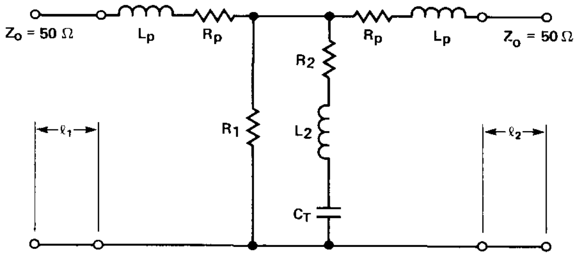
	Part Number 5082-	Package Outline	Heat Sink	Maximum Insertion Loss (dB)	Maximum SWR	Maximum RF Leakage Power (W)	Typical Recovery Time (ns)
33.22	3071	61	Cathode	1.2	2.0	1.0	100
	Test Conditions	–	–	P_{in} = 0 dBm f = 9.4GHz	P_{in} = 0 dBm f = 9.4GHz	P_{in} = 50 W	P_{in} = 50 W

Equivalent Circuits

Forward Bias (Isolation State)



Zero Bias (Insertion Loss State)



Typical Equivalent Circuit Parameters - Forward Bias

Part Number 5082-	Lp (pH)	Rp (Ω)	Rs (Ω)	L₁ (pH)	ℓ₁ (mm)	ℓ₂ (mm)
3040, 3340	200	0.25	1.0	20	2.4	5.0
3041	220	0.25	1.0	20	2.4	5.0
3046	220	0.25	0.6	17	2.4	5.0
3140, 3170	150	0.0	0.95	30	3.8	3.8
3141	150	0.0	0.8	20	3.8	3.8

Typical Equivalent Circuit Parameters - Zero Bias

Part Number 5082-	Lp (pH)	Rp (Ω)	R₁ (KΩ)	L₂ (pH)	R₂ (KΩ)	C_T (pF)	ℓ₁ (mm)	ℓ₂ (mm)
3040, 3340	200	0.25	∞	0	5.0	0.10	2.4	5.0
3041	220	0.25	∞	0	1.5	0.15	2.4	5.0
3046	220	0.25	∞	0	1.5	0.15	2.4	5.0
3140, 3170	30	0.0	1.2	16	0.0	0.20	5.3	5.3
3141	200	0.0	∞	0	0.4	0.14	4.4	4.4

Typical Parameters

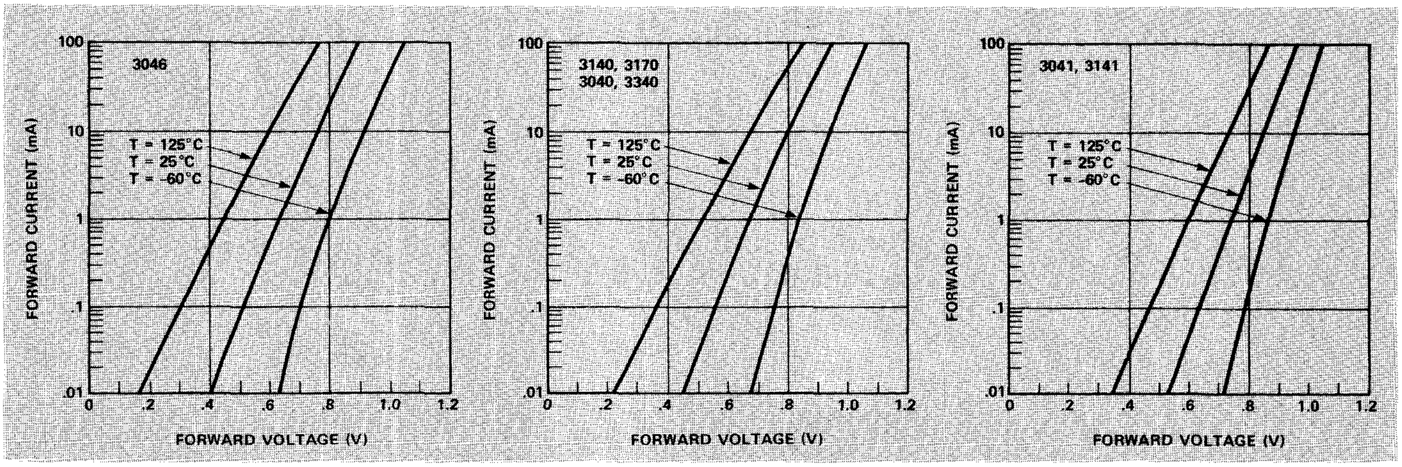


Figure 1. Typical Forward Characteristics.

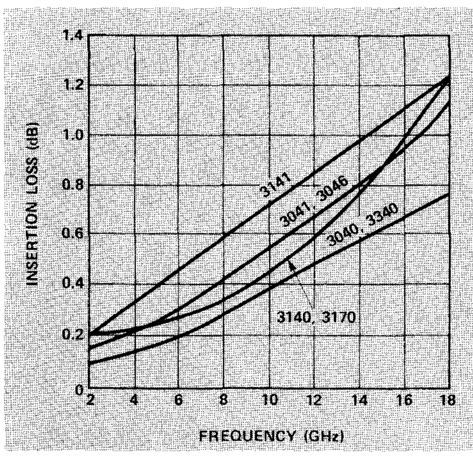


Figure 2. Typical Insertion Loss vs. Frequency.

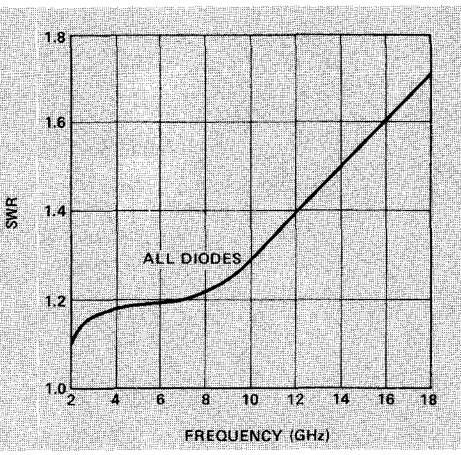


Figure 3. Typical SWR vs. Frequency.

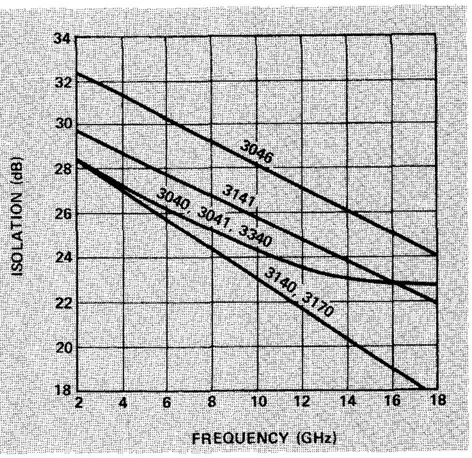


Figure 4. Typical Isolation vs. Frequency.

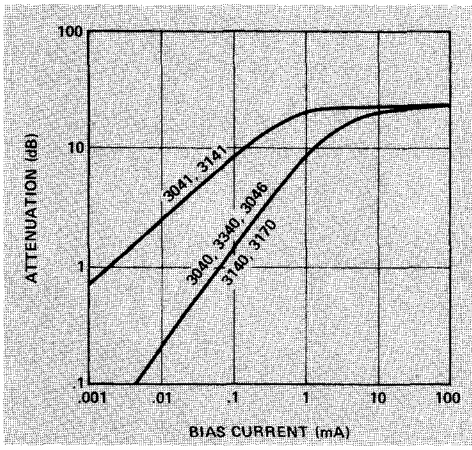


Figure 5. Typical Attenuation Above Zero Bias Insertion Loss vs. Bias Current at f = 8 GHz.

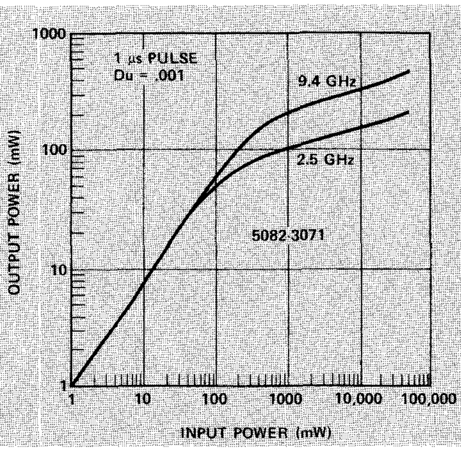
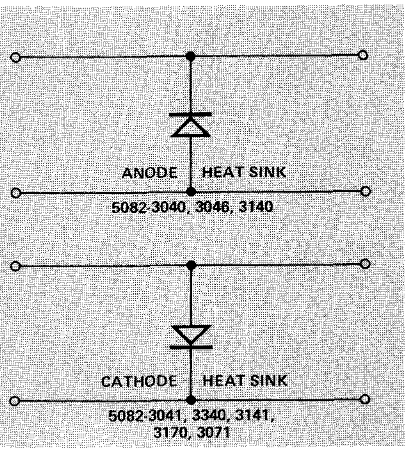
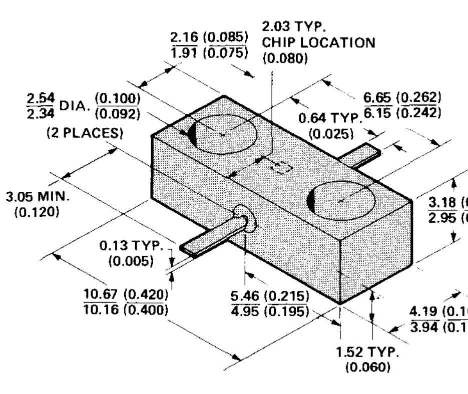


Figure 6. Typical Pulse Limiting Characteristics.



HEAT SINK POLARITY



DIMENSIONS IN MILLIMETERS AND (INCHES).

Figure 7. HP Package 60 Outline.

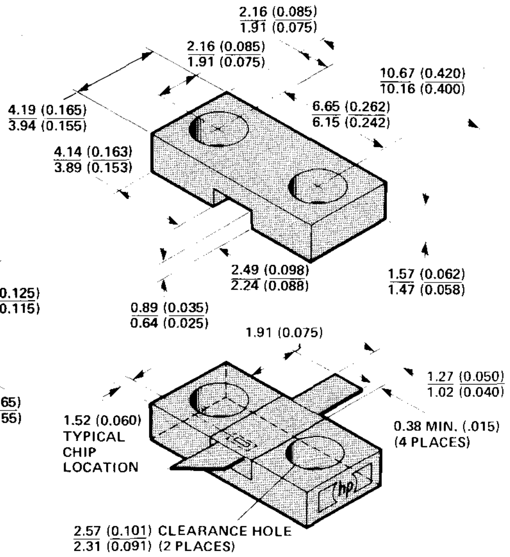


Figure 8. HP Package 61 Outline.

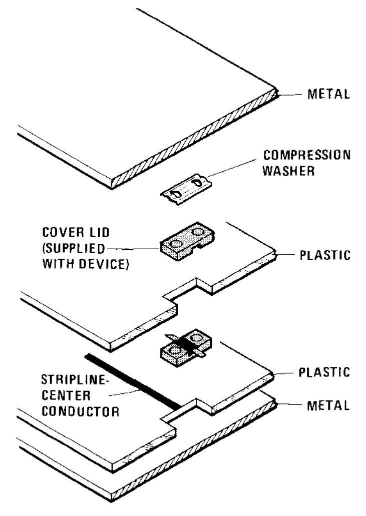


Figure 9. Suggested Stripline Assembly.

Typical Switching Parameters

RF SWITCHING SPEED

HP 5082-3141 and HP 5082-3041

The RF switching speed of the HP 5082-3141 and HP 5082-3041 may be considered in terms of the change in RF isolation at 2 GHz. This switching speed is dependent upon the forward bias current, reverse bias drive pulse, and characteristics of the pulse source. The RF switching speed for the shunt-mounted stripline diode in a 50Ω system is considered for two cases: one driving the diode from the forward bias state to the reverse bias state (isolation to insertion loss), second, driving the diode from the reverse bias state to the forward bias state (insertion loss to isolation).

The total time it takes to switch the shunt diode from the isolation state (forward bias) to the insertion loss state (reverse bias) is shown in Figure 10. These curves are for three forward bias conditions with the diode driven in each case with three different reverse voltage pulses (V_{PR}). The total switching time for each case includes the delay time (pulse initiation to 20 dB isolation) and transition time (20 dB isolation to 0.9 dB isolation). Slightly faster switching times may be realized by spiking the leading edge of the pulse or using a lower impedance pulse driver.

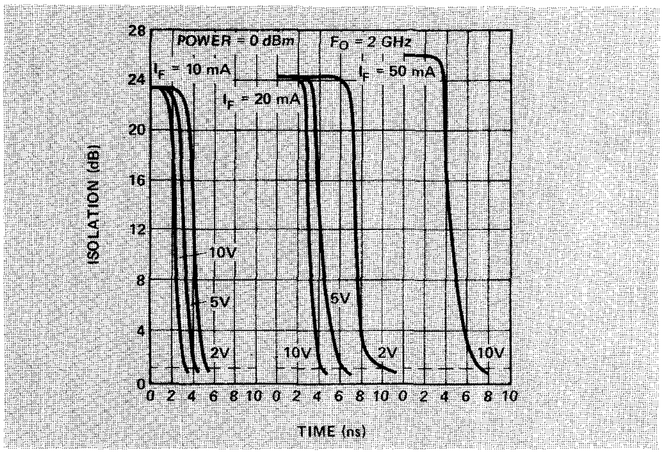


Figure 10. Isolation vs. Time (Turn-on) for HP 5082-3141 and HP 5082-3041. Frequency, 2 GHz.

The time it takes to switch the diode from zero or reverse bias to a given isolation is less than the time from isolation to the insertion loss case. For all cases of forward bias generated by the pulse generator (positive pulse), the RF switching time from the insertion loss state to the isolation state was less than 2 nanoseconds. A more detailed treatise on switching speed is published in AN929; Fast Switching PIN Diodes.

REVERSE RECOVERY TIME

Shown below is reverse recovery time, (t_{rr}) vs. forward current, (I_F) for various reverse pulse voltages V_{PR}. The circuit used to measure t_{rr} is shown in Figure 11.

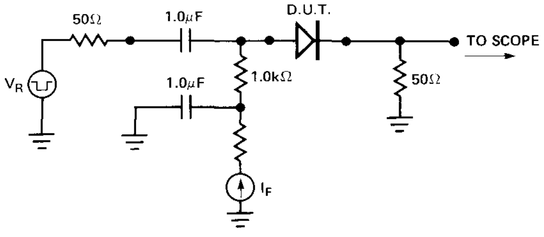


Figure 11. Basic t_{rr} Test Setup.

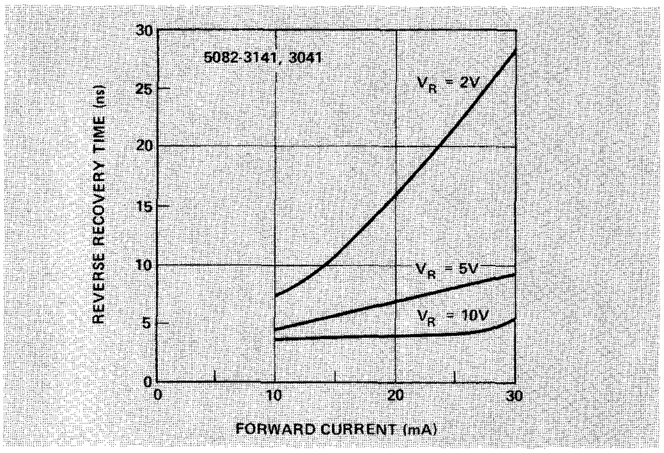


Figure 12. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages, 5082-3141, -3041.

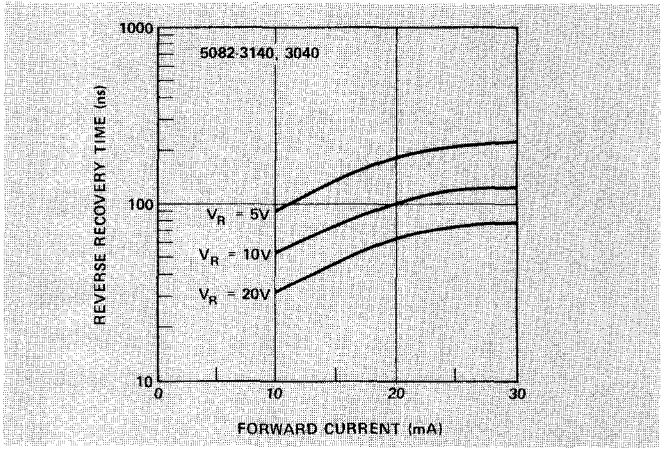


Figure 13. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages, 5082-3140, -3040.

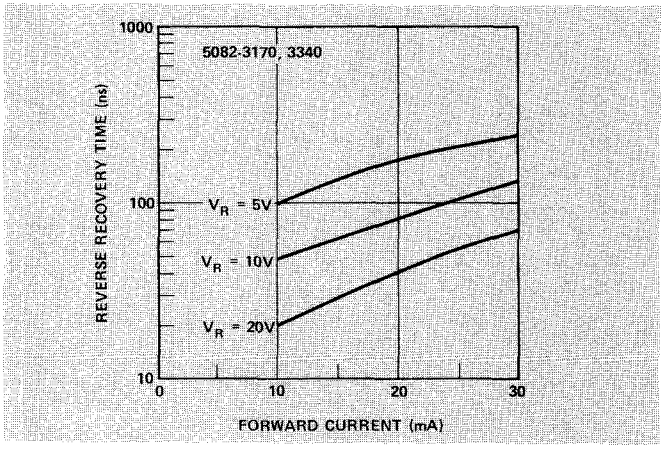


Figure 14. Typical Reverse Recovery Time vs. Forward Current for Various Reverse Driving Voltages, 5082-3170, -3340.

NOTES

Applications for PIN Diodes

HEWLETT PACKARD
COMPONENTS

APPLICATIONS FOR PIN DIODES

Applications of PIN Diodes (Portion of Application Note 922)

The most important property of the PIN diode is the fact that it appears as an almost pure resistance at RF whose resistance value can be varied over a range of approximately 1 to 10,000 ohms by a direct or low frequency control current.

When the control current is varied continuously, the PIN diode is useful for attenuating, leveling and amplitude modulating an RF signal. When the control current is switched "on" and "off" or in discrete steps, the device is useful for switching, pulse modulating, and phase shifting of an RF signal.

In addition, the PIN's small size, weight, high switching speed, and freedom from parasitic elements make it ideally suited for use in miniature, broadband RF signal control components.

This application note describes the important properties of the PIN diode and illustrates how it can be applied in a variety of RF control circuits. Topics discussed include the following:

Characteristics of the PIN Diode
- (a) Low and High Frequency Equivalent Circuits
- (b) The RF Resistance Characteristic
- (c) Effects of Package Parasitics

PIN Diode Applications
- (a) Design of Broadband Reflective Switches and Attenuators
- (b) Design of Resonant Switches
- (c) Design of Multiple Diode and Multi-throw Switches and Attenuators
- (d) Design of Constant Impedance Switches and Attenuators
- (e) PIN Diode Phase Shifters

PIN Diode Power Handling

Fast Switching PIN Diodes (Portion of Application Note 929)

SWITCHING SPEED

The switching speed of a PIN diode may be defined and measured in a number of ways. Ideally, we would like to think of it as the time it takes the device to make the transition from the minimum insertion loss case to the maximum isolation case or vice versa. Because of the charge nonlinearities during switching of the device and the need for reasonable measurement techniques, we often settle for some definitions less than ideal.

A figure of switching capability commonly used by industry is the reverse recovery time (t_{rr}). Figure 1a shows the diode in the RF test circuit. Figure 1b shows the monitored current through the diode used to determine the reverse recovery time.

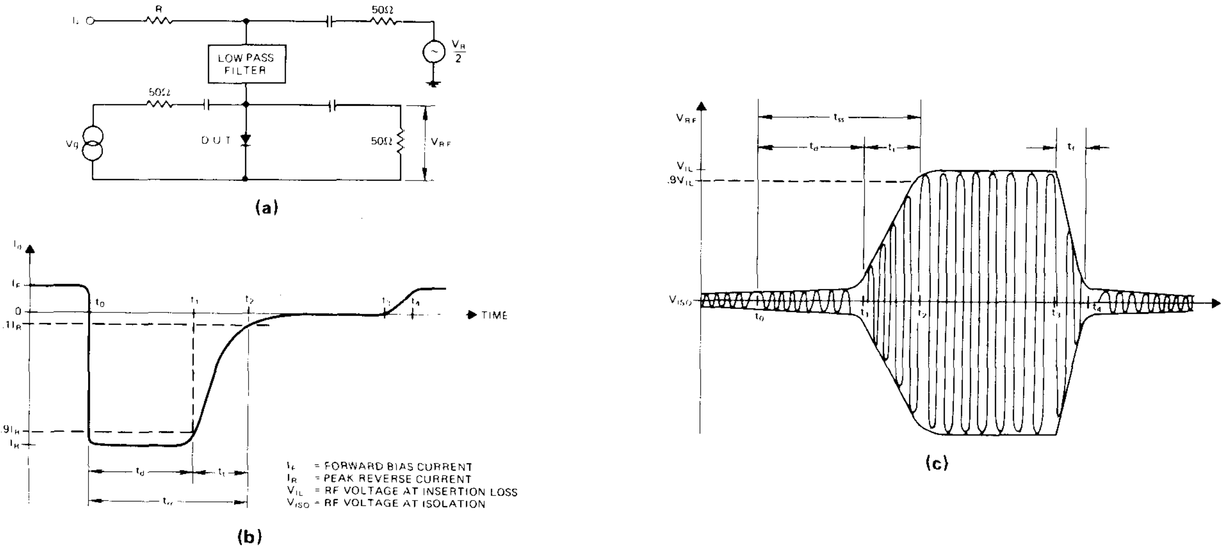


Figure 1. Switching Time Test Circuit with Drive Current Waveform and Switched RF Voltage

Following a general discussion of the switching speed of a PIN diode and the considerations which affect switching capability, this application note outlines basic drive requirements (Figure 2) and comments on a few practical switching circuits for the HP 5082-3041/3042 fast switching PIN diodes. Considerations involved in the design of filters required for use with the diodes are also discussed.

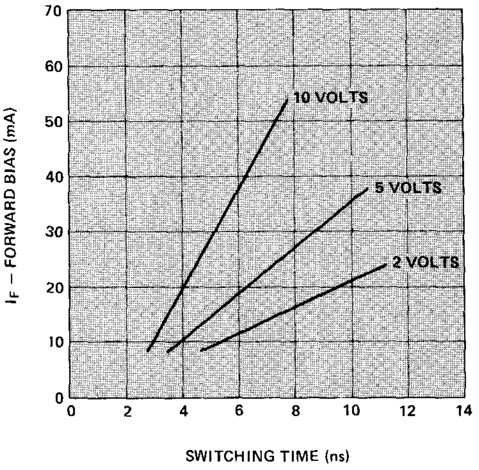


Figure 2. Switching Time vs. Forward Bias for Peak Reverse Voltage as a Parameter

High Performance PIN Attenuator for Low Cost AGC Applications

(Portion of Application Note 936)

PIN diodes offer an economic way of achieving excellent performance in AGC circuits. Significant improvements in cross-modulation and intermodulation distortion performance compared to transistors are obtained. (Table 1).

Automatic gain control in a transistorized circuit requires that the optimum operating point of the AGC transistor be shifted. This produces a drastic change in the impedance level, which severely affects the adjoining tuned circuit.

The use of a PIN diode attenuator as the AGC control element as shown in Figure 1 will provide the required gain control without the attendant problems of large impedance shift. The result is minimum distortion in the output.

Other advantages of PIN diodes, such as good low frequency operation, constant impedance levels, and low power consumption are discussed in this application note.

Table 1. Distortion Performance Comparison of AGC Circuits

	PIN Diode		Transistor
	5082-3080	5082-3081	
Power Consumption, mW	35	35	120
2nd Order Intermod, dB (−20 dBm output)	−59	−64	−55
Crossmodulation (−20 dBm output)	−68	−59	−37

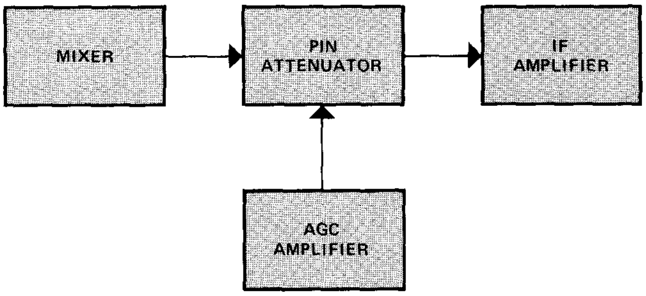


Figure 1. The Use of a PIN Attenuator for AGC.

Broadbanding the Shunt PIN Diode SPDT Switch (Portion of Application Note 957-1)

The bandwidth of the shunt diode SPDT switch can be improved by the simple impedance matching technique shown in Figure 1. A third transmission line, a quarter wavelength long at f_o, is placed between the common junction and R.F. Port 3. In addition, the impedance of all three lines is set to some value, Z, below 50 ohms. The specific value of impedance that is chosen will determine the SWR and bandwidth of the switch. Figure 2 gives the SWR vs. bandwidth for five values of Z. For example, setting the impedance of the three transmission lines to 35 ohms results in a 1.43:1 SWR bandwidth of 100%. The data shown on Figure 2 was computed assuming a resistance of 0.5 ohms for D_1 and 1000 ohms for D_2.

By selecting the impedance for the transmission line of Port 3 to be slightly different from the other two, small additional improvements in SWR can be made. This variation of the broadbanding technique is beyond the scope of this note, but it can be easily and quickly evaluated by means of one of the many microwave circuit analysis programs available on time-shared computers.

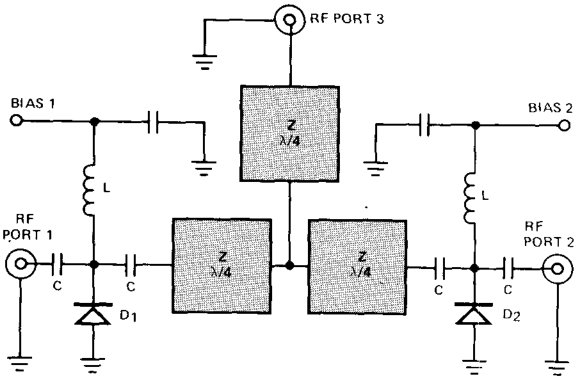


Figure 1. Broadband Shunt SPDT Switch.

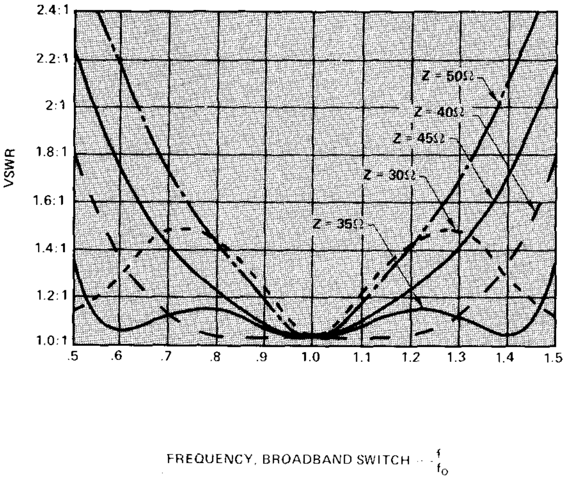


Figure 2. VSWR vs. Frequency Ratio, Broadband Switch.

Reducing the Insertion Loss of a Shunt PIN Diode (Application Note 957-2)

A shunt PIN diode is often used as a switch or attenuator. The upper frequency limitation is determined by the increase in insertion loss as the diode capacitance starts to short out the load. Figure 1 shows a symmetrical matching circuit that extends this frequency limitation by incorporating the diode capacitance, C, into a low pass filter. Figure 2 shows the filter response when the inductance value, L, is chosen to form a Chebyshev equal ripple filter.

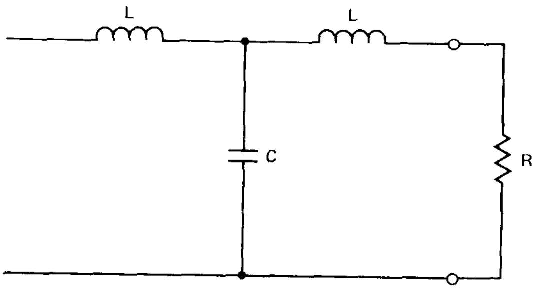


Figure 1. Low pass matching circuit.

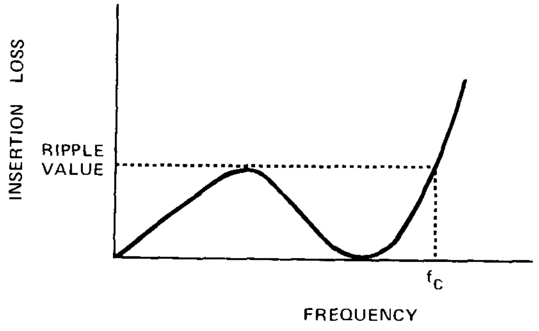


Figure 2. Chebyshev Response

$$L = R^2C\frac{g(1)}{g(2)}$$

The constants g(1) and g(2) are low pass prototype element values, available in the literature[1,2] as a function of the ripple value shown in Figure 2. This filter is designed to operate between equal generator and load resistances, R.

The cutoff frequency, f_c, shown in Figure 2, is determined by the diode capacitance, the ripple value, and R.

$$f_c = \frac{g(2)}{2\pi RC}$$

For convenience in design, inductance and cutoff frequency are plotted in Figure 3 in terms of VSWR and in Figure 4 in terms of insertion loss. For example, the HP 5082-0001 PIN diode has a zero bias capacitance of 0.18 pF. If a cutoff frequency of 16 GHz is desired, the insertion loss ripple will be .007 dB and the VSWR ripple will be 1.072, corresponding to $f_cC = 2.88$. The value of L is .28 nH corresponding to

$$\frac{L}{C} = 1.54.$$

Higher cutoff frequencies or lower ripple may be obtained by lowering the diode capacitance with reverse bias. The capacitance of the 5082-0001 PIN diode is reduced to 0.12 pF with a reverse bias of 20 volts. This increases the cutoff frequency for the same ripple to 24 GHz.

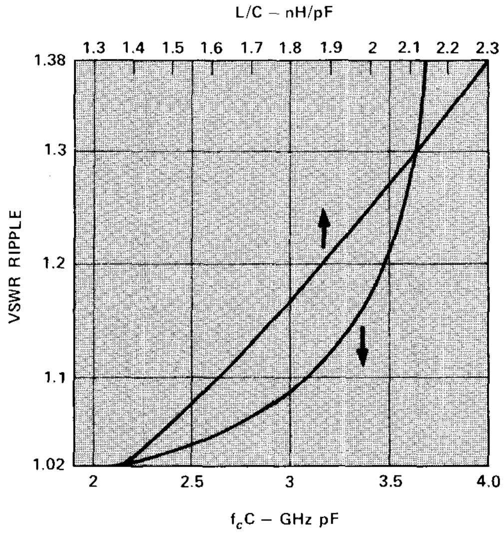


Figure 3. Filter design curves.

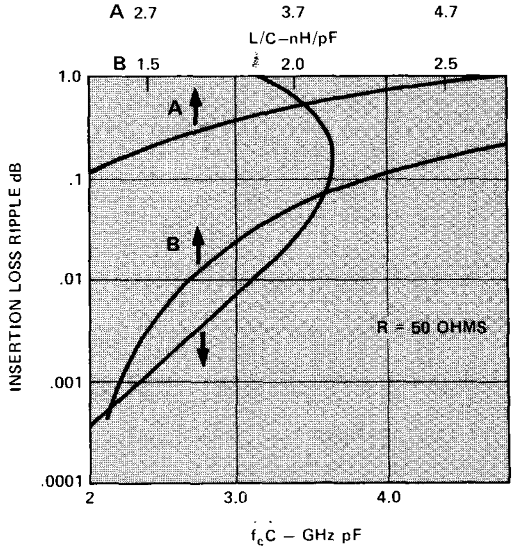


Figure 4. Filter design curves.

REFERENCES

1. L. Weinberg, "Network Analysis and Synthesis", McGraw-Hill, 1962.
2. N. Chitre and M. O'Donovan, "A Unified Design Chart for Small VSWR Filters", Microwave Journal, April 1967, pp 79-84.

Rectification Effects In PIN Attenuators (Portion of Application Note 957-3)

Attenuation values of PIN diodes are changed by high incident power levels. The effect is most noticeable at intermediate attenuation levels in fast switching diodes. The variation in attenuation may be minimized by proper choice of bias resistance.

An ideal PIN diode acts as a variable resistor controlled by dc current. In attenuation applications, the performance is independent of carrier power level or frequency. The performance of a real PIN diode, however, is limited by both carrier level and frequency because of rectification effects. The effects are more serious at low frequencies because the period is closer to the lifetime of the charge carriers in the diode intrinsic layer. There is sufficient time for these charges to be influenced by the changing rf voltage.

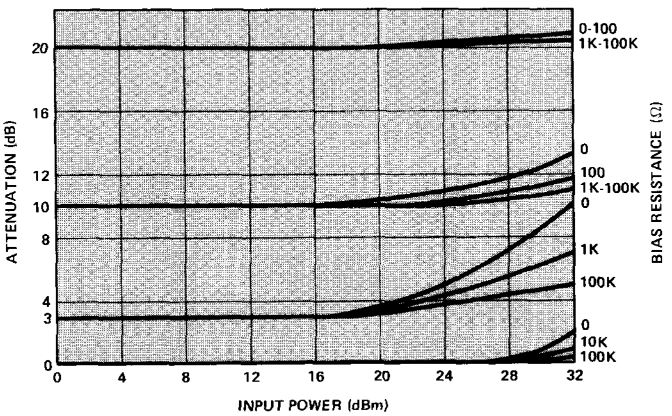


Figure 1. Attenuation at 2 GHz vs. Input Power with Bias Resistance as a Parameter. 5082-3140

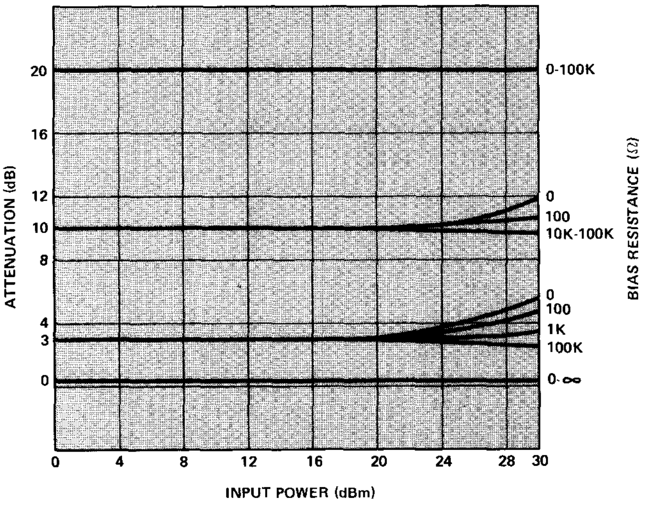


Figure 2. Attenuation at 10 GHz vs. Input Power with Bias Resistance as a Parameter. 5082-3140

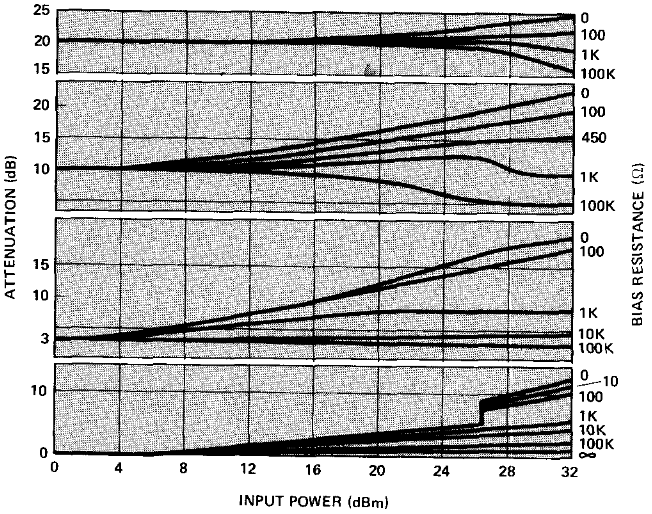


Figure 3. Attenuation at 2GHz vs Input Power with Bias Resistance as a Parameter. 5082-3141

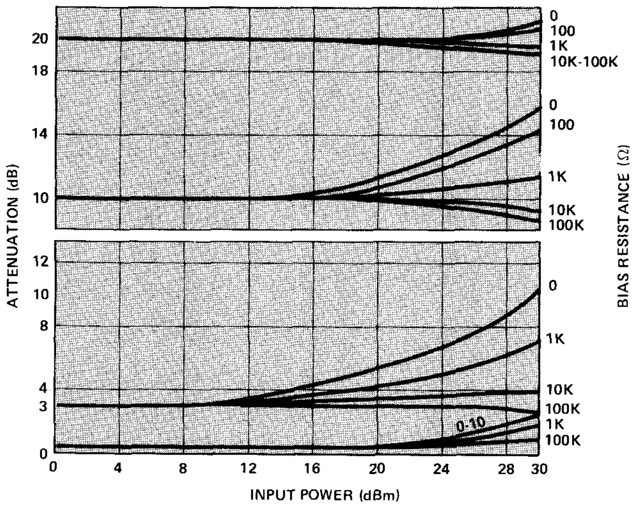


Figure 4. Attenuation at 10 GHz vs. Input Power with Bias Resistance as a Parameter. 5082-3141

PIN Diode RF Resistance Measurement (Portion of Application Bulletin 6)

INTRODUCTION

In order to correctly determine the resistance characteristic of a PIN diode, several test methods have been suggested and devised by various sources. Many of these methods are inaccurate or time-consuming. This Application Bulletin describes how the RF resistance of a PIN diode can be measured reliably and efficiently with the use of the HP 4815 Vector Impedance Meter.

RF RESISTANCE MEASUREMENT

The resistance measurement method to be described utilizes a tunable fixture to tune out the reactive part of the impedance, leaving the real part to be measured by the Vector Impedance Meter. A block diagram of the test equipment is shown in Fig. 1. The diode under test (D.U.T.) in the test fixture receives the proper bias from the current source. The fixture is tuned for a zero phase indication on the Vector Impedance Meter. The resistance is then read on the Vector Impedance Meter or (for better resolution at low resistance levels) on a Digital Voltmeter which is connected to the recorder output of the Vector Impedance Meter. Use of the Precision Power Source to provide a stable low voltage for offsetting the short circuit resistance is described in the Appendix of this Application Bulletin.

With some diodes a single tunable test fixture will tune out the diode reactance for all forward currents. For other diodes more than one test fixture may be necessary.

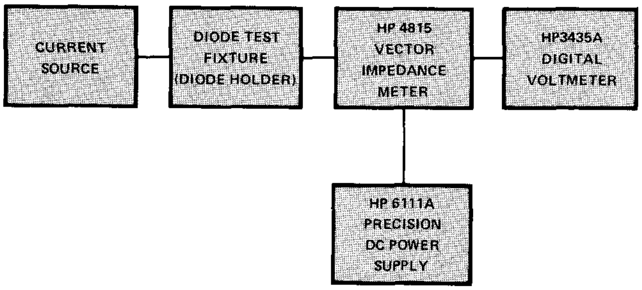


Figure 1. Block Diagram of Test Equipment for RF Resistance Measurement of a PIN Diode.

With the reactive part of the impedance tuned out, the Vector Impedance Meter will essentially see the measured resistance, R_m, as the series combination of the diode resistance, R_s, and the short circuit resistance, R_{sc}, in parallel with the open circuit resistance, R_{oc} as illustrated in Fig. 2. In other words, the measured resistance,

$$R_m = \frac{R_{oc}\,(R_s + R_{sc})}{R_{oc} + R_s + R_{sc}} \quad (1)$$

The diode resistance is then

$$R_s = \frac{R_m\,(R_{oc} + R_{sc}) - R_{oc}\,R_{sc}}{R_{oc}\,R_m} \quad (2)$$

or since $R_{sc} << R_{oc}$

$$R_s = \frac{R_{oc}\,(R_m - R_{sc})}{R_{oc} - R_m} \qquad (3)$$

If the measured resistance is low ($R_m << R_{oc}$), then the diode resistance

$$R_s = R_m - R_{sc} \qquad (4)$$

For high resistance ($R_m >> R_{sc}$)

$$R_s = \frac{R_{oc}\,R_m}{R_{oc} - R_m} \qquad (5)$$

The resistance vs. bias slope on a log-log plot is

$$\chi = \frac{\log R_{s_2} - \log R_{s_1}}{\log I_2 - \log I_1} \qquad (6)$$

where I_1 and I_2 are respectively specified low and high current levels, and R_{s_1} and R_{s_2}, the diode resistances corresponding to those bias levels.

The slopes of the HPND-4165 and HPND-4166 PIN diodes are batch matched between 10 µA and 1 mA. In this case equation (6) reduces to

$$\chi = -\frac{1}{2}\log\frac{R_{10\mu A}}{R_{10mA}} \qquad (7)$$

Details of the test procedure are contained in the Appendix of this Application Bulletin.

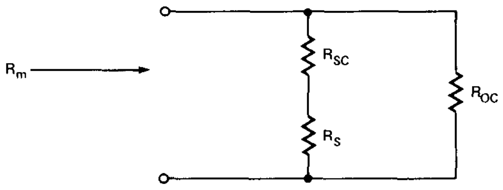


Figure 2. The Measured Resistance R_m as Seen by the Vector Impedance Meter When the Reactive Part of the Diode Impedance is Tuned Out.

TEST FIXTURE

The test fixture contains a circuit (Fig. 3) which tunes out the diode reactance. The essential components are a tunable inductor and tunable capacitor in the tuning section and an RF choke and bypass capacitor in the bias section. Detailed drawings of this test fixture are available upon request from Hewlett-Packard, Applications Department, San Jose, CA 95131.

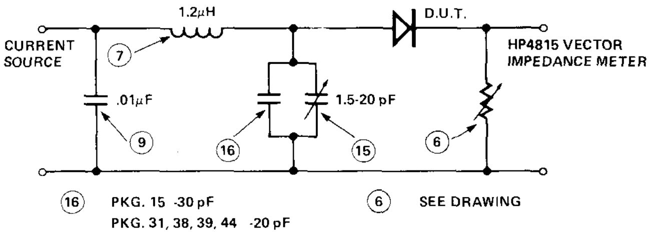


Figure 3. Schematic of Test Circuit for RF Resistance Measurement of a PIN Diode.

Switching Performance Parameters

For a good approximation, the PIN diode in a switch is essentially a resistor in the forward biased state and a capacitor in the reverse biased state.

Insertion Loss

The loss of signal attributed to the diode when the switch is ON (transmission state) is insertion loss. The insertion loss is primarily determined in a series switch by the forward biased resistance of the diode (Figure 1) and in a shunt switch both by the diode capacitance and signal frequency (Figure 2). In either case it is the diode impedance in relation to the source and load impedance, (generally 50 Ohms). For low insertion loss, low resistance is needed in a series switch. Low capacitance (particularly at high frequencies) is needed in a shunt switch.

Isolation

Isolation is the measure of RF leakage between the input and output when the switch is OFF. For high isolation, low capacitance (especially at high frequencies) is required in a series switch (Figure 3). Low resistance is required in a shunt switch (Figure 4).

Switching Speed

Reverse recovery time (Figure 5) is a measure of switching time, and is dependent on the forward and reverse bias applied. With forward bias current, I_F, charge is stored in the I-layer. When reverse biased, reverse current, I_R, will flow for a short period of time, known as delay time, t_d. When a sufficient number of carriers have been removed, the current begins to decrease. The time required for the reverse current to decrease from 90% to 10% is called the transition time, t_t. The sum, $t_d + t_t$, is the reverse recovery time, which is a good indication of the time it takes to switch the diode from ON to OFF. (A more detailed discussion on switching speed is available in AN 929 and the data sheet on the 5082-3040 Series of Stripline PIN Diodes.)

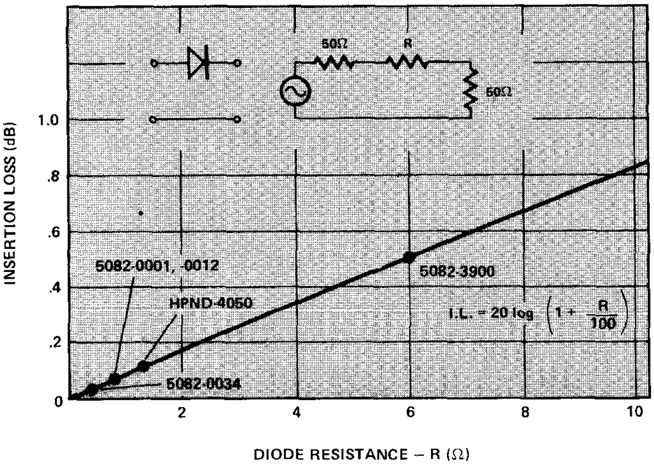


Figure 1. Insertion Loss of Series Diode Switch.

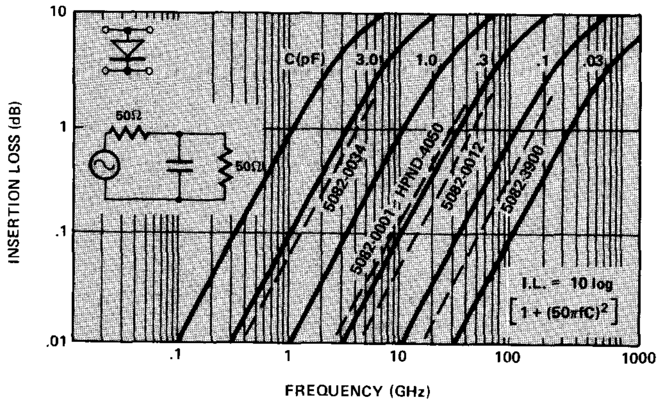


Figure 2. Insertion Loss of Shunt Diode Switch.

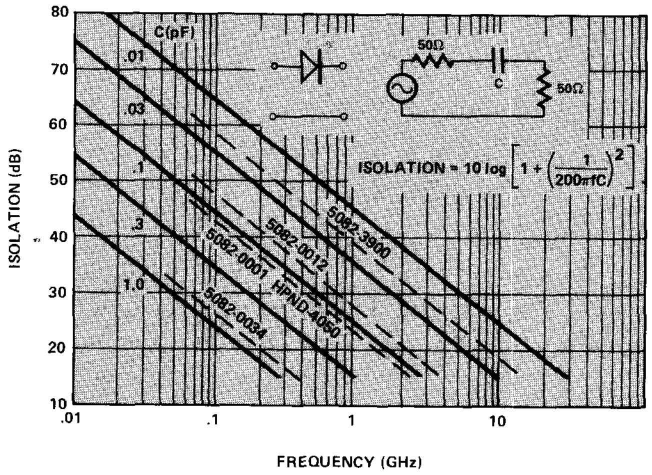


Figure 3. Isolation of Series Diode Switch.

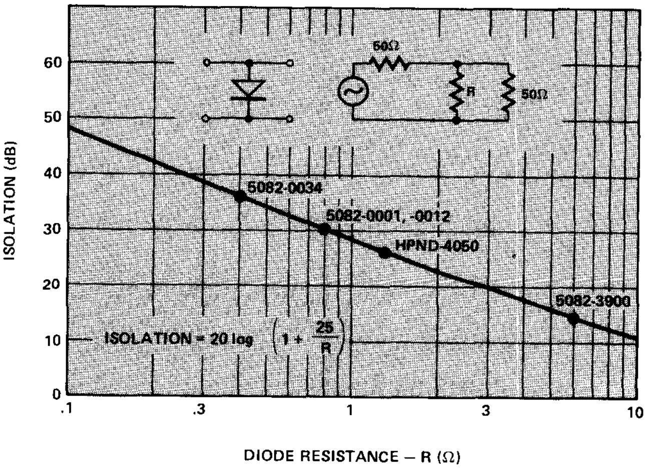


Figure 4. Isolation of Shunt Diode Switch.

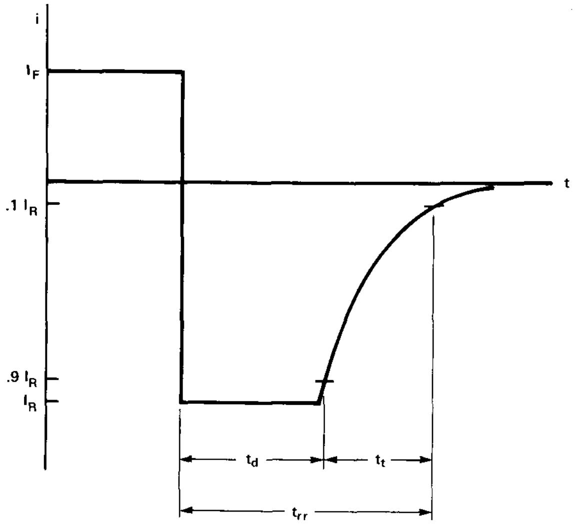


Figure 5. Reverse Recovery Time.

Standing Wave Ratio

Standing Wave Ratio (SWR) which is a measure of the RF impedance match, is particularly important in high frequency applications. Since the SWR of most package styles depends on the mounting arrangement, it is only specified for diodes in 50 Ohm stripline packages.

Voltage Rating

The maximum signal voltage the switch can handle without damage is determined by the breakdown voltage of the diode.

Power Handling Capability

The RF power (CW or pulse), that can be handled safely by a diode switch is limited by two factors—the breakdown voltage of the diode, and thermal considerations, which involve maximum diode junction temperature and the thermal resistance of the diode and packaging. Other factors affecting power handling capability are ambient temperature, frequency, attenuation level (diode resistance) pulse width, and pulse duty cycle. A first order approximation of the power handling capability of a PIN diode switch can be determined by using the procedure outlined below.

Calculation of Power Handling Capability of PIN Diode Attenuators and Switches: This summary of equations for power handling calculations is intended to provide the tools for a first order analysis of the RF power handling capability of TR switches, phase shifters, or attenuators. It is assumed that parasitic circuit elements are negligible or tuned out.

Summary of Symbols:

P_A — Power in transmission line (maximum available power to load).

P_R — Power dissipated in PIN diode, may be as high as P_{DISS} max specified for the device under consideration.

R — Resistance of PIN diode in "on" or "off" condition, whichever creates higher P_R.

V_{BR} — Breakdown voltage of PIN diode.

A — Attenuation ratio of series or parallel diode inserted into transmission line.

CALCULATION SEQUENCE:

1. Read P_{DISS} max from the absolute maximum ratings.
2. Determine the CW Power Multiplier from Equation (1) for a shunt circuit, or Equation (4) for a series circuit. Alternatively, Figure 8 can be used if diode resistance is known, or Figure 9 can be used if circuit attenuation is known.
3. Multiply P_{DISS} max by the CW Power Multiplier to determine CW power handling capability.
4. Determine the Pulse Power Multiplier, if applicable, from Figure 10.
5. Multiply the CW power handling capability by the Pulse Power Multiplier to determine pulse power handling capability.
6. Check for power handling limit due to V_{BR} by using Equation (3) for shunt circuits and Equation (6) for series circuits.

Shunt Circuit

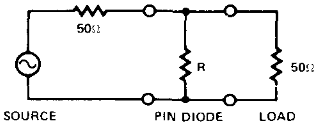


Figure 6. Shunt Attenuator/Switch Circuit.

Power Multiplier: $$\frac{P_A}{P_R} = \frac{(25 + R)^2}{50R} \qquad (1)$$

Attenuation: $$A = 20 \log_{10} \left(1 + \frac{25}{R}\right), \text{dB} \qquad (2)$$

Breakdown Voltage Limit: $$P_A\,(\text{max}) = \frac{(V_{BR} - V_R)^2}{100}, \text{W} \qquad (3)$$

Series Circuit

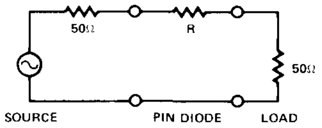


Figure 7. Series Attenuator/Switch Circuit.

Power Multiplier: $$\frac{P_A}{P_R} = \frac{(100 + R)^2}{200R} \qquad (4)$$

Attenuation: $$A = 20 \log_{10} \left(1 + \frac{R}{100}\right), \text{dB} \qquad (5)$$

Breakdown Voltage Limit: $$P_A\,(\text{max}) = \frac{(V_{BR} - V_R)^2}{400}, \text{W} \qquad (6)$$

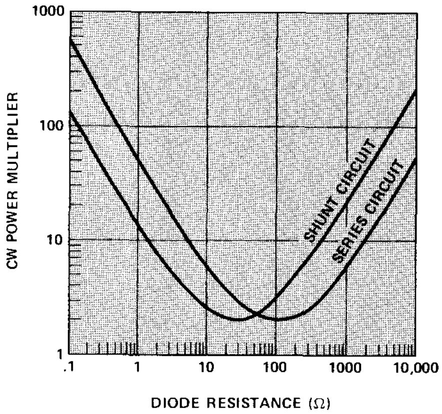


Figure 8. CW Power Multiplier vs. Diode Resistance.

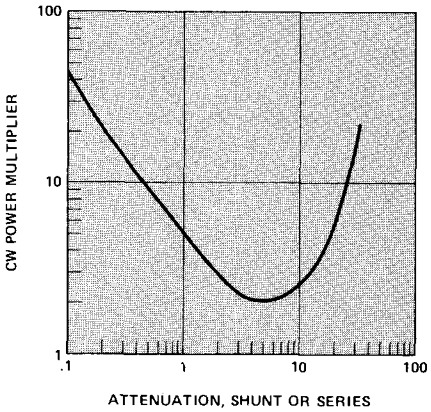


Figure 9. CW Power Multiplier vs. Series or Shunt Attenuation.

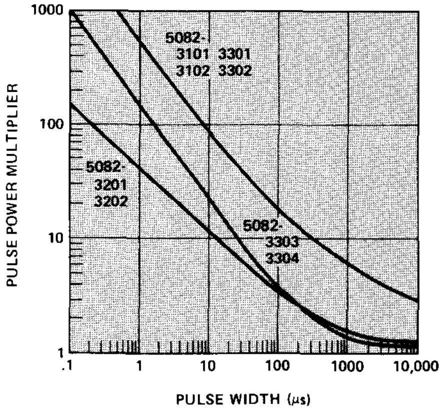
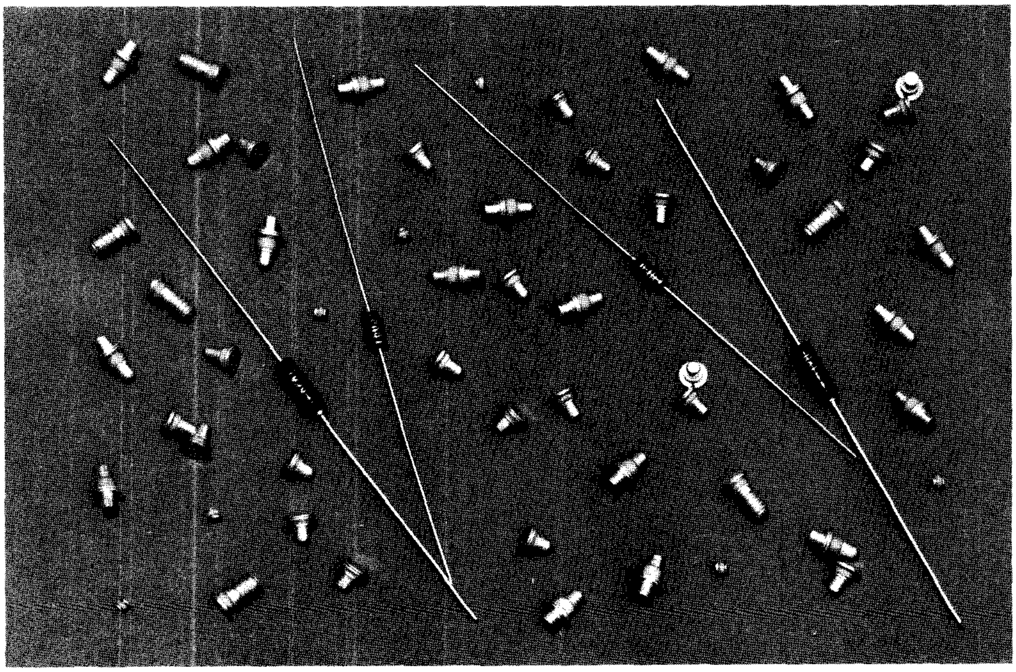


Figure 10. Pulse Power Multiplier vs. Pulse Width.

NOTES

IMPATT and Step Recovery Diodes



Microwave Source Diodes Selection Guide

DOUBLE DRIFT PULSED IMPATT DIODES

Peak Power Out/ Center Frequency	Part Number 5082-	Page Number
12W 10 GHz	-0710	155.25 166
9W 16.5 GHz	-0716	155.25

DOUBLE DRIFT CW IMPATT DIODES

Power Out/ Center Frequency	Part Number 5082-	Page Number
1.75W 7 GHz	-0607	124.20 157
3.00 W 8 GHz	-0608	192.51
1.5 W 10 GHz	-0610	108.68 161
2.5 W 11 GHz	-0611	167.67

STEP RECOVERY DIODES (PAGE 153)

Typical Output Frequency Range, GHz	High Efficiency Multiplier Versions 5082-	RF Tested Versions 5082-	DC Tested Versions 5082-
.4-1.5	0803 7.45 0815 7.45 0825 7.45 0833 " 0840 "		0180 0112 0114 0151
1-3	0800 17.70 0801 " 0802 "	0300 0303	0241
3-5	0805 " 0806 " 0807 "	0310	0132
5-8	0810 " 0811 " 0812 "	0310	0132
7-10	0820 " 0821 " 0822 "		0243
8-12	0830 " 0831 "	0320	0253
10-20	0835 " 0836 " 0885 20.7	0335	

Chips and other devices for MIC shown on page 171.

HEWLETT PACKARD
COMPONENTS

STEP RECOVERY DIODES

5082-0100 SERIES
5082-0200 SERIES
5082-0300 SERIES
5082-0800 SERIES

Features

OPTIMIZED FOR BOTH LOW AND HIGH ORDER MULTIPLIER DESIGNS FROM UHF THROUGH Ku BAND

PASSIVATED CHIP FOR MAXIMUM STABILITY AND RELIABILITY

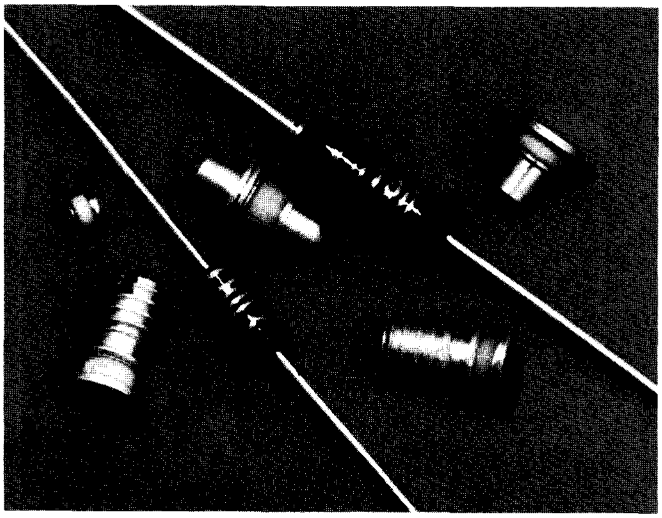
AVAILABLE IN A VARIETY OF PACKAGES

SPECIAL ELECTRICAL SELECTIONS AVAILABLE UPON REQUEST

Description/Applications

These diodes are manufactured using modern epitaxial growth techniques. The diodes are passivated with a thermal oxide for maximum stability. The result is a family of devices offering highly repeatable, efficient and reliable performance. These diodes are designed to meet the general requirements of MIL-S-19500.

The 5082-0800 Series diode is designed to maximize cut-off frequency while maintaining a fast transition time. This characteristic leads to excellent performance in either low or high order multipliers and in comb generators. All ceramic package diodes in the 5082-0800 Series are supplied with measured data.



Maximum Ratings at $T_{CASE} = 25°C$

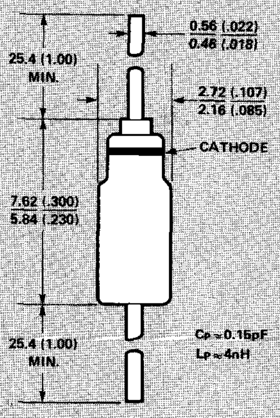
Junction Operating and Storage Temperature . . . . -65°C to 200°C

Operation of these devices within the above temperature ratings will assure a device Mean Time Between Failure (MTBF) of approximately 1 x 10^7 hours.

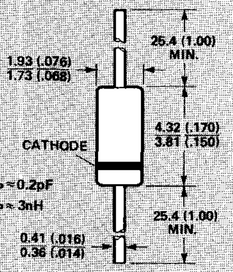
DC Power Dissipation . . . . $\dfrac{200°C - T_{case}}{\theta_{jc}}$

Soldering Temperature . . . . 230°C for 5 sec.

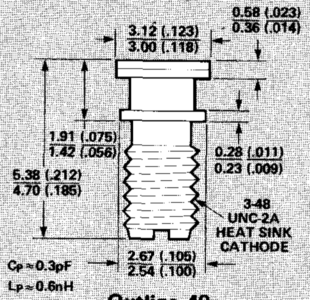
Package Dimensions



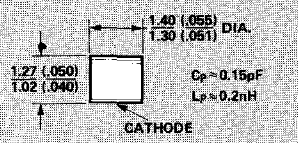
Outline 11



Outline 15

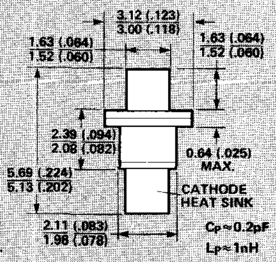


Outline 40

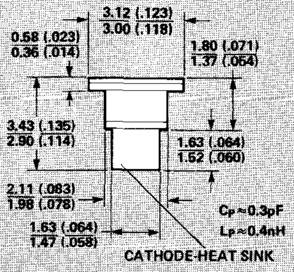


Outline 56

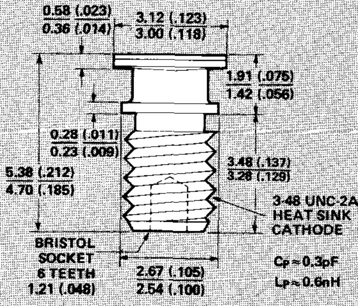
DIMENSIONS IN MILLIMETERS AND (INCHES).



Outline 31



Outline 41



Outline 65

Mechanical Specifications

Hewlett-Packard's step recovery diodes are available in a variety of packages. Special package configuration is available upon request. Contact your local HP Field Office for additional information.

The metal-ceramic packages are hermetically sealed. The anode studs and flanges are gold-plated Kovar. The cathode studs are gold-plated copper. The maximum soldering temperature is 230°C for 5 seconds.

The HP outline 15 and 11 packages have glass hermetic seals with dumet leads. The maximum soldering temperature is 230°C for 5 seconds. The leads on outline 15 should be restricted so that any bend starts at least 1.6 mm (.063 in.) from the glass body.

Diodes for High Efficiency Multipliers (All Specifications at T_A = 25°C)

Ceramic Packaged Diodes

ELECTRICAL SPECIFICATIONS

Part Number 5082-	Junction Capacitance at -6V, $C_{j(-6)}$ *[1] [pF]		Minimum Breakdown Voltage, V_{BR} * at $I_R = 10\mu A$ [V]	Minimum Cutoff Frequency, f_c[2] [GHz]	Package Outline
	Min.	Max.			
0800	3.5	5.0	75	100	40
0801					31
0802					41
0805	2.5	3.5	60	140	31
0806					40
0807					41
0810	1.5	2.5	60	140	31
0811					40
0812					41
0820	0.7	1.5	45	160	31
0821					41
0822					40
0830	0.35	1.2	25	200	31
0831					41
0835	0.1	0.5	15	350	31
0836					41
0885					56

*Data supplied with each diode includes measured V_{BR} and $C_{T(-6)}$

TYPICAL PARAMETERS

Output Frequency Range [GHz]	Output Power, P_o[3] [W]	Lifetime, τ [ns]	Transition Time		Thermal Resistance, Θ_{jc} [°C/W]
			t_t [ps]	Charge Level [pC]	
1-3	10	250	350	1500	15
3-5	6	100	250	1500	20
5-8	4	100	200	1000	25
7-10	2.5	50	100	300	30
8-12	1.0	20	75	300	45
10-20	0.3	10	50	100	60

Glass Packaged Diodes (Outline 15)[4]

ELECTRICAL SPECIFICATIONS

Part Number 5082-	Maximum Junction Capacitance at -6V, $C_{j(-6)}$[1] [pF]	Minimum Breakdown Voltage, V_{BR} at $I_R = 10\mu A$ [V]	Minimum Cutoff Frequency, f_c [2] [GHz]
0803	6.0	70	100
0815	4.0	50	140
0825	2.0	45	160
0833	1.6	25	175
0840	0.6	15	300

TYPICAL PARAMETERS

Lifetime, τ [ns]	Transition Time	
	t_t [ps]	Charge Level [pC]
250	350	1500
60	250	1500
50	95*	300
30	75*	300
10	50*	100

*The transition times shown for the package 15 devices are limited by the package inductance to a minimum of 100 ps. The lower transition times shown for the -0825, -0833 and -0840 are based on the performance of the chip.

RF Tested Diodes (All Specifications at T_A = 25° C)

ELECTRICAL SPECIFICATIONS | TYPICAL PARAMETERS

Part Number 5082-	Output Frequency, f_o [GHz]	N Order	Minimum Output Power, P_o[5] [W]	Junction Capacitance at -10V, C_j[1] [pF]		Breakdown Voltage at I_R=10µA V_{BR} [V]		Maximum Thermal Resistance, θ_{jc} [°C/W]	Package Outline	Transition Time		Lifetime, τ [ns]
				Min.	Max.	Min.	Max.			t_t [ps]	Charge Level [pc]	
0300	2	X 10	2.0	3.2	4.7	75	100	14	40	450	2400	200
0303	2	X 10	2.0	3.2	4.7	75	100	14	65[6]	450	2400	200
0310	6	X 10	0.4	1.6	2.7	40	60	30	41	160	1000	75
0320	10	X 5	0.23	0.35	1.0	25	40	60	41	75	300	20
0335	16	X 8	0.03	0.25	0.5	20	30	75	31	60	100	15

DC Tested Diodes (All Specifications at T_A = 25° C)

ELECTRICAL SPECIFICATIONS | TYPICAL PARAMETERS

Part Number 5082-	Maximum Junction Capacitance at -10V, $C_{j(-10)}$[1] [pF]	Minimum Breakdown Voltage at I_R=10µA V_{BR} [V]	Maximum Transition Time		Package Outline	Lifetime τ [ns]	Thermal Resistance Θ_{jc} [°C/W]
			t_t [ps]	Charge Level [pC]			
0113[7]	4.85	35	250	1500	11	100	300
0241	4.6	65	275	1500	31	150	20
0180	4.45	50	225	1500	11	150	300
0114[7]	3.85	35	225	1500	11	100	300
0112	1.55	35	175	1000	11	50	300
0132	1.5	35	175	1000	31	50	40
0243	1.2	35	110	600	31	40	50
0151	0.65	15	90	200	15	20	600
0253[7]	0.6	25	80	200	31	20	75
0153	0.4	25	90	200	15	20	600

Suggested output frequency, $f_{o(max)} \leqslant 1/t_t$

NOTES:
1. Capacitance selection is available upon request. Contact your local sales office.
2. $f_c = \dfrac{1}{2\pi R_s C_{j(-6)}}$
3. As a doubler at midband.
4. For package outline 15 typical thermal resistance is 600° C/W with adequate heat sink.
5. Guaranteed multiplier tested results.
   Input power is: 5082-0300 15W, 5082-0320 2W, 5082-0310 4W, 5082-0335 0.65W
6. Package 65 is a modified version of the package 40. It features a 6-tooth, 1.21mm (.048 in) Bristol socket rather than a screw driver slot. A Bristol socket wrench is shipped with each order for 5082-0303.
7. The 5082-0113, -0114 and -0253 are also available by EIA registration numbers 1N5163, 1N5164 and 1N4547 respectively.

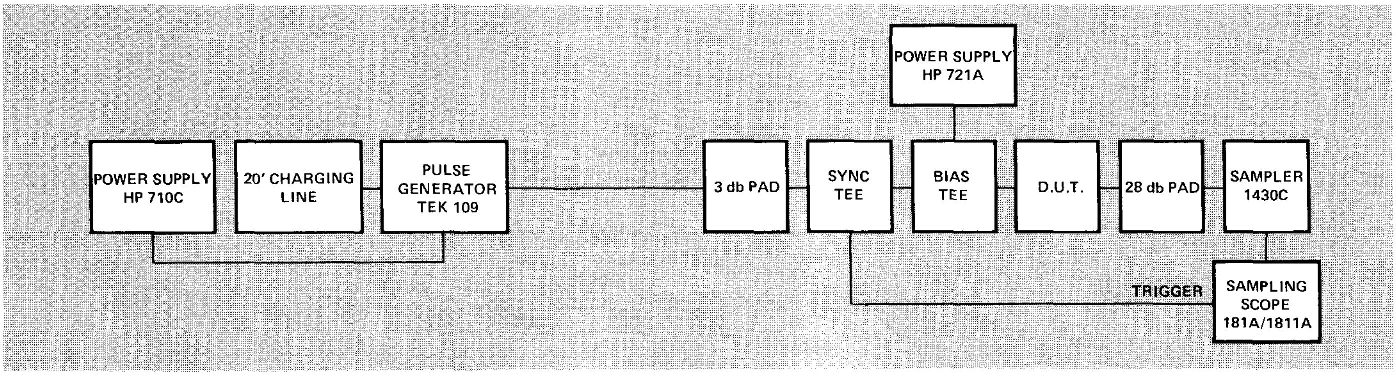


Figure 1. Test circuit for transition time. The pulse generator circuit is adjusted for a 0.5 A pulse when testing 5082-0151, 0253, 0335, 0835, 0836, 0885 and 0840. A pulse of 1.0 A is used for all other diodes. The bias current is adjusted for the specified stored charge level. The transition time is read between the 20% and the 80% points on the oscilloscope.

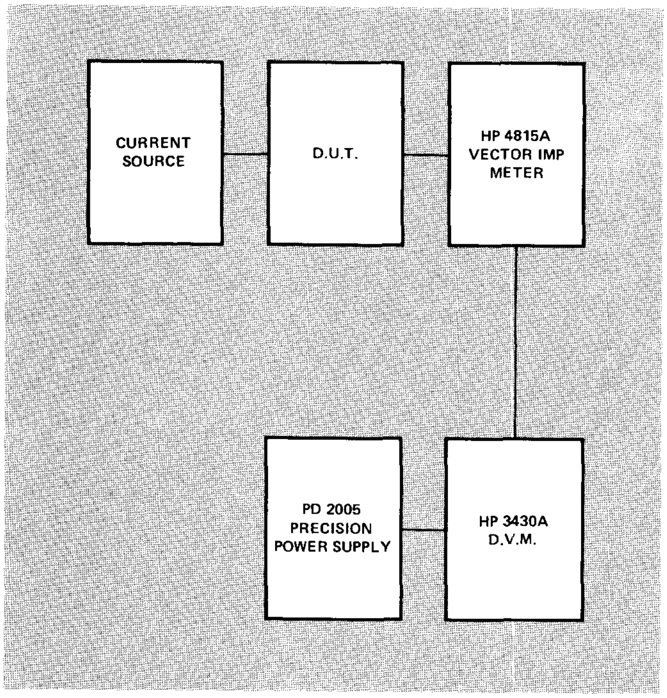


Figure 2. Test set-up for measurement of series resistance. The D.U.T. is forward biased (I_F) and the real part of the diode impedance is measured at 100 MHz. The D.V.M. is set up to read the real part on the Vector Voltmeter. The precision power supply is used to offset the test circuit resistance. R_S is measured at I_F = 100mA except 0800, 0801, 0802, 0803 where I_F = 500mA.

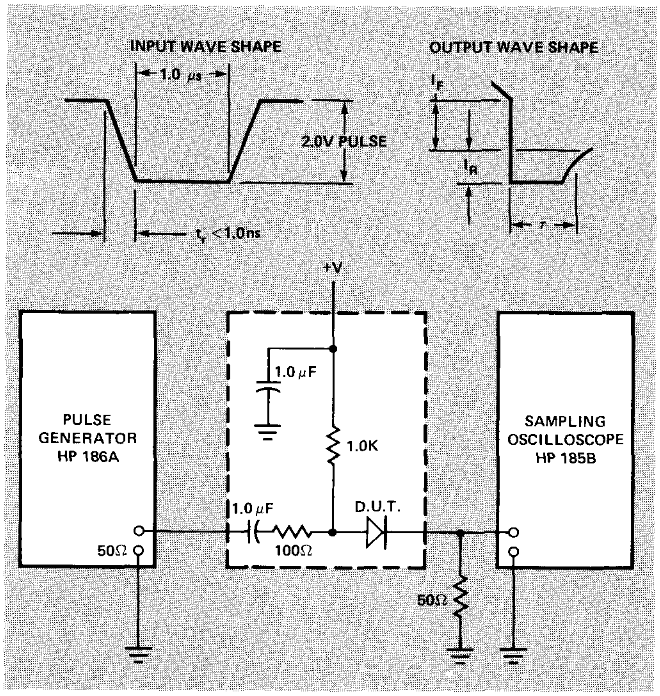


Figure 3. The Circuit for Measurement of the Effective Minority Carrier Lifetime. The value of the reverse current (I_R) is approximately 6 mA and the forward current (I_F) is 1.71 I_R. The lifetime (τ) is measured across the 50% points of the observed wave shape. The input pulse is provided by a pulse generator having a rise time of less than one nanosecond. The output pulse is amplified and observed on a sampling oscilloscope.

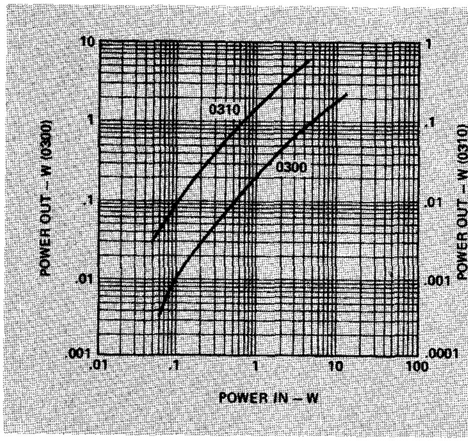


Figure 4. Typical Output Powers vs. Input Power at T_A = 25°C. The 5082-0300 is measured in a x 10 multiplier with P_{IN} at 0.2 GHz and P_O at 2.0 GHz. The 5082-0310 is measured in a x 10 multiplier with P_{IN} at 0.6 GHz and P_O at 6.0 GHz.

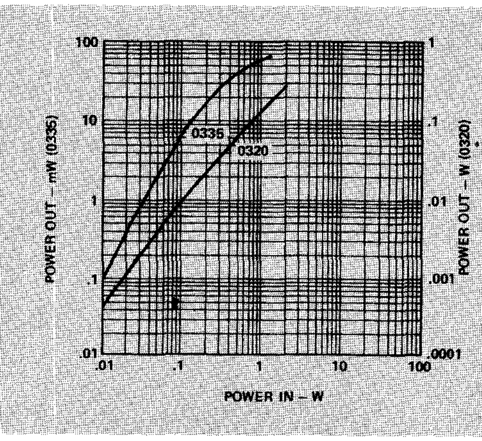


Figure 5. Typical Output Power vs. Input Power at T_A = 25°C. The 5082-0335 is measured in a x 8 multiplier with P_{IN} at 2 GHz and P_O at 16 GHz. The 5082-0320 is measured in a x 5 multiplier with P_{IN} at 2.0 GHz and P_O at 10 GHz.

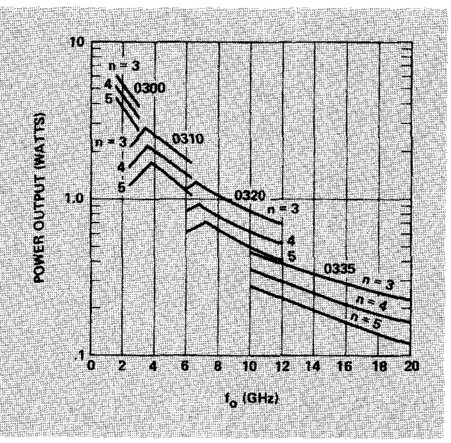


Figure 6. Predicted power output curves for 03XX step recovery diodes in X3, X4, and X5 multiplier applications. These results were obtained using computer organization programs.

HEWLETT hp PACKARD
COMPONENTS

SILICON DOUBLE DRIFT IMPATT DIODES FOR CW POWER SOURCES (5.9-8.4 GHz)

5082-0607
5082-0608

Features

HIGH POWER OUTPUT
Typically: 3W from 5.9 to 8.4 GHz

HIGH EFFICIENCY

LOW NOISE

HIGH AMBIENT OPERATION
Specified Output Power Available at 50° C Ambients

HIGH RELIABILITY
Designed to Exceed the Requirements of MIL-S-19500

Description/Applications

Double drift silicon IMPATT (IMPact Ionization Avalanche Transit Time) diodes are junction devices operated with reverse bias sufficient to cause avalanche breakdown. Holes and electrons generated in the avalanche region travel across their respective drift regions and are collected at the contacts. The phase delay between voltage and current resulting from the avalanche process in combination with the drift time produces negative resistance at microwave frequencies.

Double drift IMPATT diodes offer advantages of higher power and efficiency, lower junction capacitance per unit area, and lower fm noise, as compared to single drift silicon IMPATT diodes.

Because of their high output power, efficiency and reliability, these devices are ideally suited for use as the active element in oscillators and amplifiers in point-to-point telecommunications links and CW Doppler radar. For more information see HP AN 962 Silicon Double Drift IMPATT Diodes for high power CW microwave applications and HP AN 968 IMPATT Amplifier.

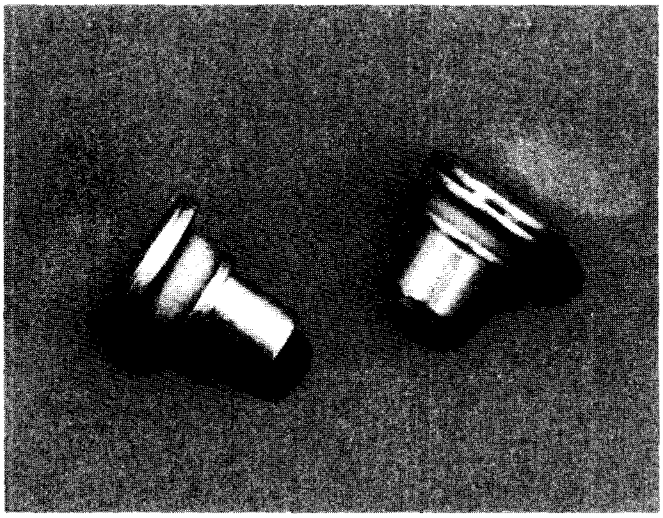
Maximum Ratings at $T_{CASE}=25°C$

Junction Operating Temperature ..... -65°C to +250°C
Junction Temperature Rise, ΔT_j .... 200°C
Storage Temperature .... -65°C to +150°C

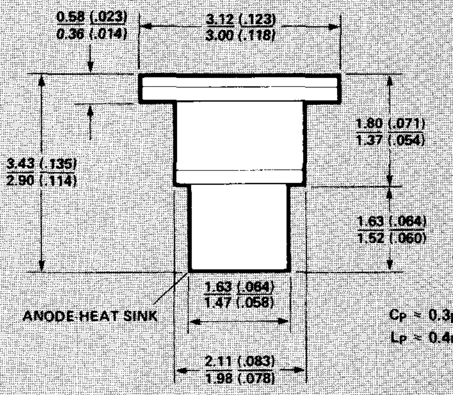
Operation of these devices within the above temperature ratings will assure a device Mean Time Between Failure (MTBF) of approximately 1 x 10^7 hours.

Power Dissipation .... $\frac{200°C}{\Theta_T}$

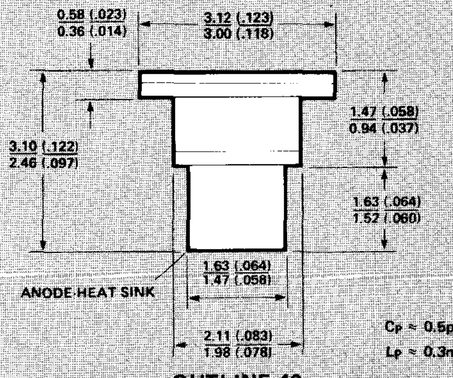
Soldering Temperature .... 220°C for 5 sec.



Package Dimensions



OUTLINE 41
5082-0607



OUTLINE 46
5082-0608

DIMENSIONS IN MILLIMETERS AND (INCHES).

Mechanical Specifications

Hewlett-Packard's IMPATT diodes are available in a variety of packages. Special package configuration is available upon request. Contact your local HP Field Office for additional information.

These metal-ceramic packages are hermetically sealed. The cathode studs and flanges are gold-plated Kovar. The anode studs are gold-plated copper. The maximum soldering temperature is 230°C for 5 seconds.

Electrical Specifications at $T_A = 25°C$

Parameter	Symbol	5082-0607	5082-0608	Units	Notes
Minimum CW Output Power	P_O	1.75	3.0	W	1,2 (Fig. 9)
Test Frequency	f_O	7.2		GHz	1

Typical Parameters

Parameter	Symbol	5082-0607	5082-0608	Units	Notes
Efficiency	η	11	10.5	%	$\eta = \frac{P_O}{P_{IN}} \times 100$
Operating Voltage	V_{OP}	180	180	V	
Operating Current	I_{OP}	95	165	mA	
Breakdown Voltage	V_{BR}	150	150	V	$I_R = .5$ mA
Junction Capacitance at Breakdown	$C_{J(VBR)}$	0.35	0.7	pF	f = 1 MHz
Thermal Resistance	Θ_T	11	6.5	°C/W	3
Package Outline	—	41	46	—	—

Notes:
1. Output power measured as an oscillator. Junction temperature is less than 225°C with an ambient temperature of 25°C. Typical diodes satisfy the minimum specification throughout the operating frequency range. Special models tested at other frequencies are available upon special request.
2. The mount for an IMPATT diode must provide an adequate heat flow path away from the diode stud. The junction temperature rise will be: $\Delta T_j = \Theta_T (P_{IN} - P_O)$.
3. Θ_T is measured with the diode mounted in a copper heatsink using the dc avalanche resistance method (see HP AN 935, page 6). Θ_{jc}, use $\Theta_{jc} = \Theta_T - 1.5°C/W$ (1.5°C/W has been found to be a nominal value for a good heat flow path in the diode mount).

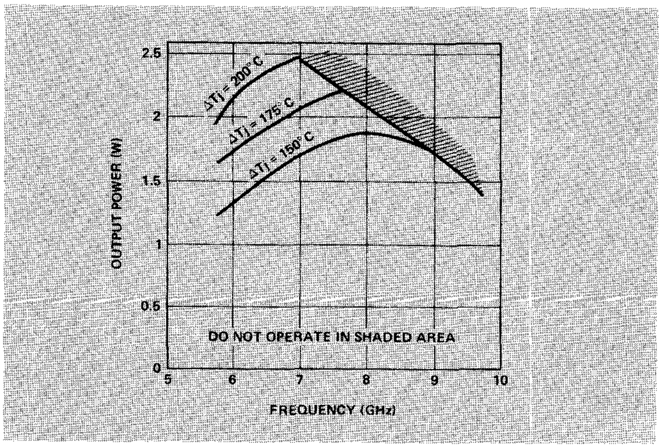


Figure 1. Typical Output Power vs. Frequency, 5082-0607. Output power maximized at each frequency.

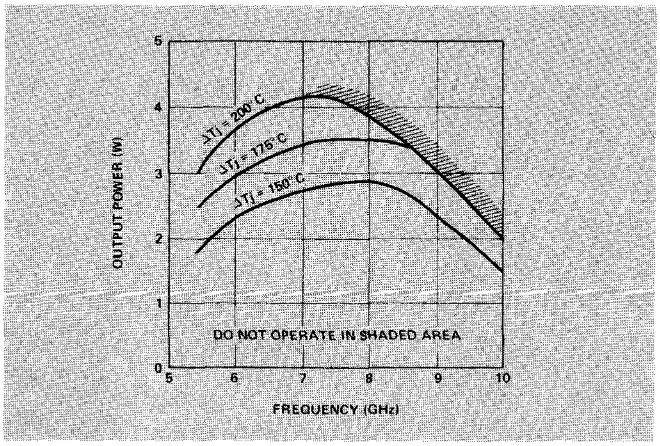


Figure 2. Typical Output Power vs. Frequency, 5082-0608. Output power maximized at each frequency.

CAUTION: *Performance in shaded region may be characterized by power saturation and noisy output spectrum. Operation under these conditions can result in diode failure (See HP AN 959-1).*

Typical Parameters, 5082-0607

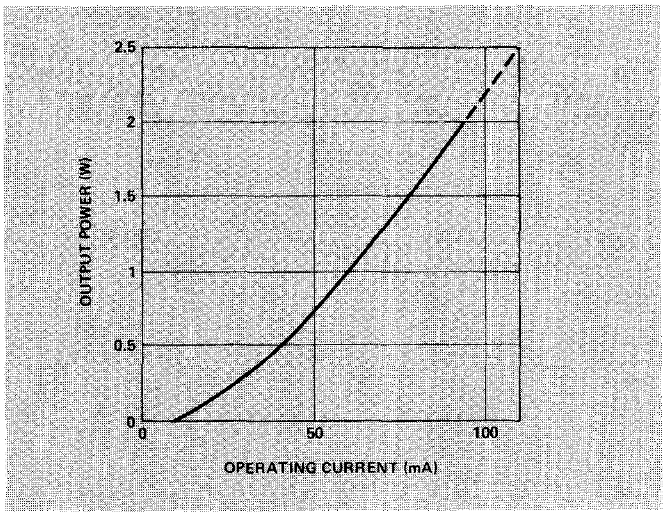


Figure 3. Typical Output Power vs. Operating Current at 7.2 GHz, 5082-0607. Output power maximized at each current level.

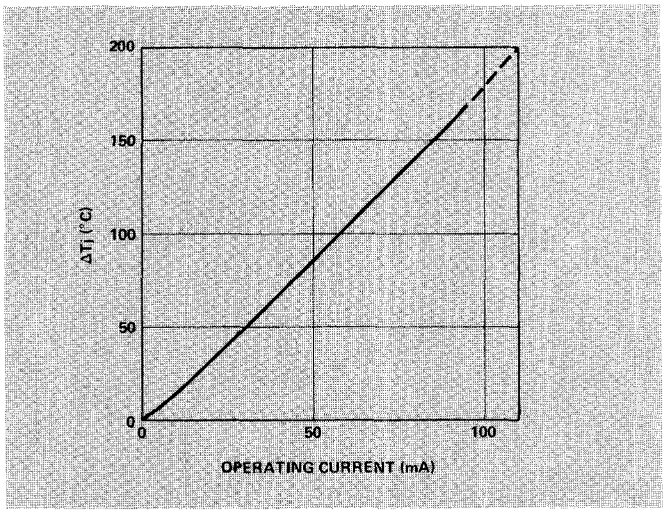


Figure 4. Typical Junction Operating Temperature Rise (ΔTj) vs Operating Current at 7.2 GHz, 5082-0607. Output power maximized at each current level.

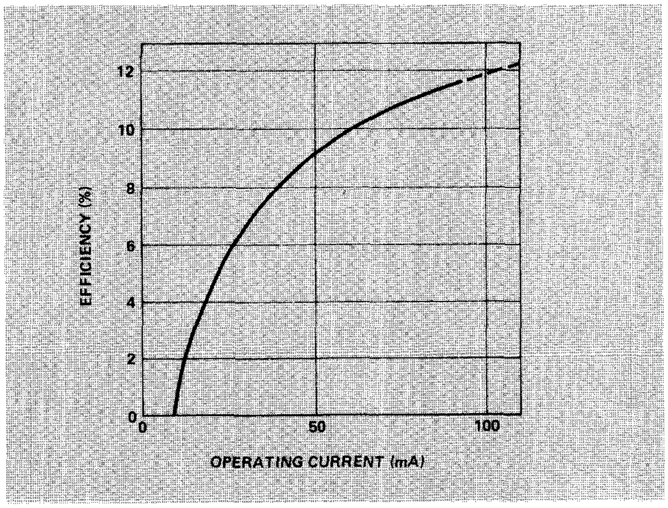


Figure 5. Typical Efficiency vs. Operating Current at 7.2 GHz, 5082-0607. Output power maximized at each current level.

Typical Parameters, 5082-0608

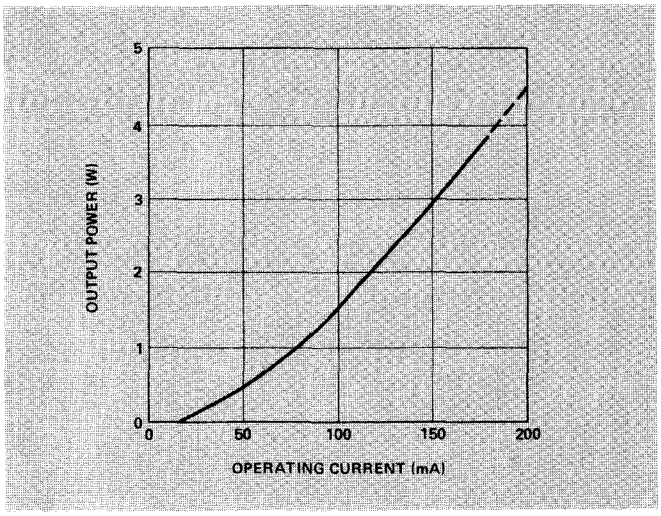


Figure 6. Typical Output Power vs. Operating Current at 7.2 GHz, 5082-0608. Output power maximized at each current level.

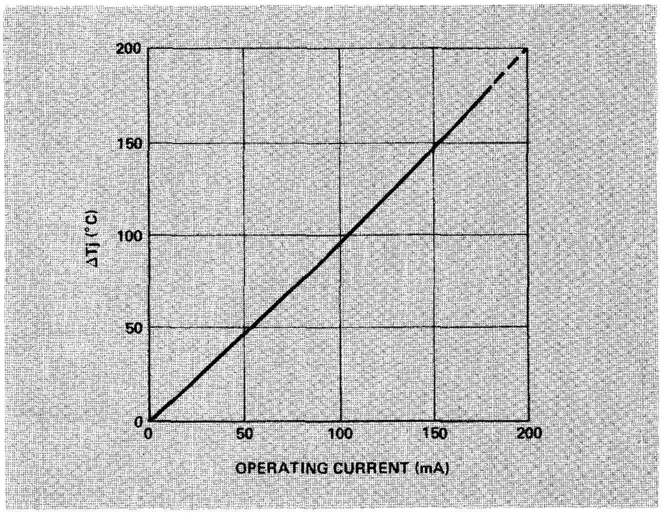


Figure 7. Typical Junction Operating Temperature Rise (ΔTj) vs. Operating Current at 7.2 GHz, 5082-0608. Output power maximized at each current level.

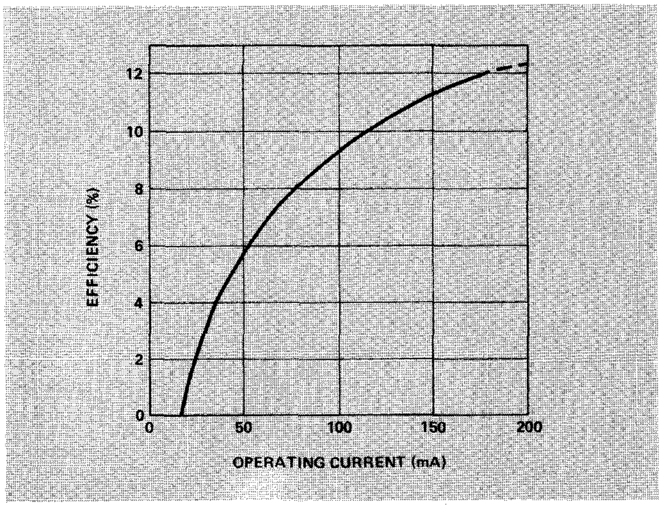


Figure 8. Typical Efficiency vs. Operating Current at 7.2 GHz, 5082-0608. Output power maximized at each current level.

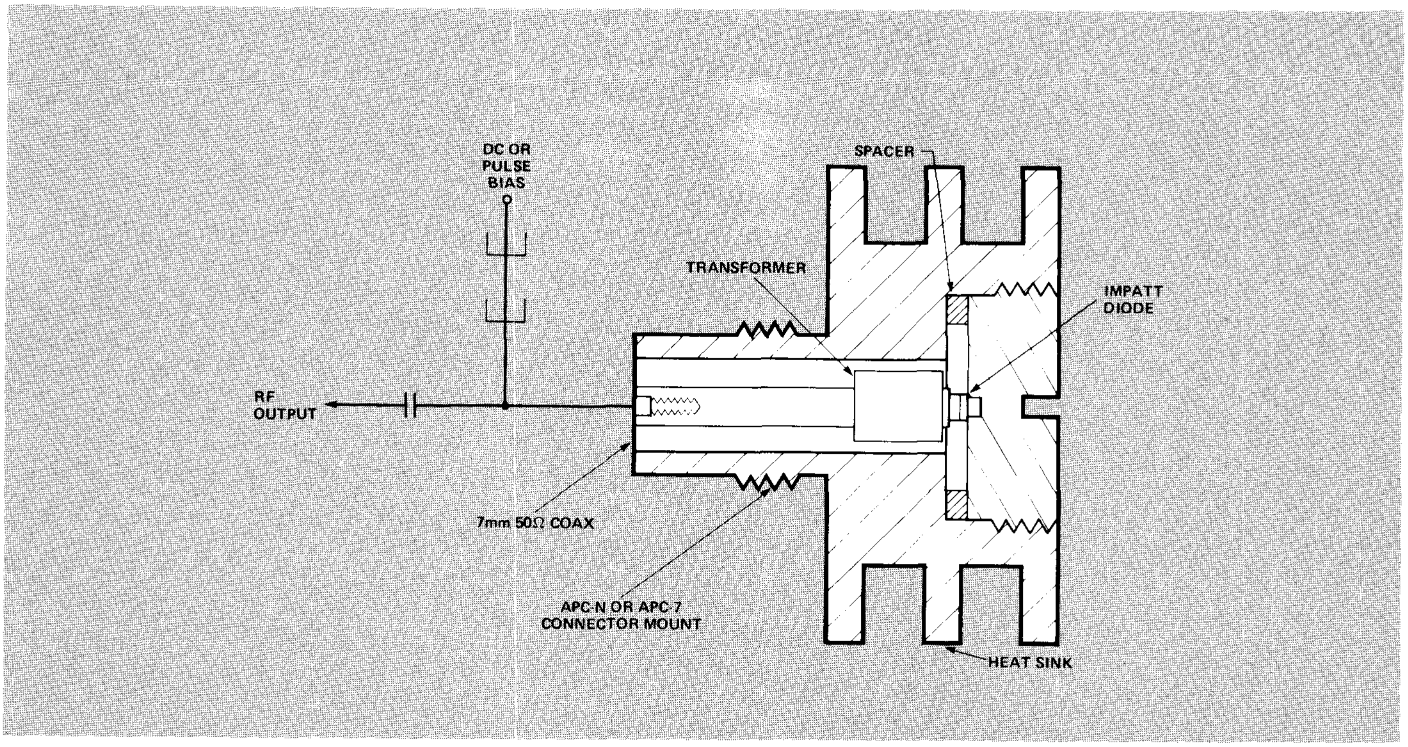


Figure 9. Simplified Drawing of Coaxial Cavity. Detailed mechanical drawings are available on request. A tuning screw should be used with this cavity. The use of fixed tuned cavities is not recommended for IMPATT Diodes. Minor variations of diode impedance among production units require some tuning capability.

HEWLETT **hp** PACKARD

COMPONENTS

HIGH POWER, HIGH EFFICIENCY, SILICON DOUBLE DRIFT IMPATT DIODES FOR CW POWER SOURCES (10-14 GHz)

5082-0610
5082-0611

Features

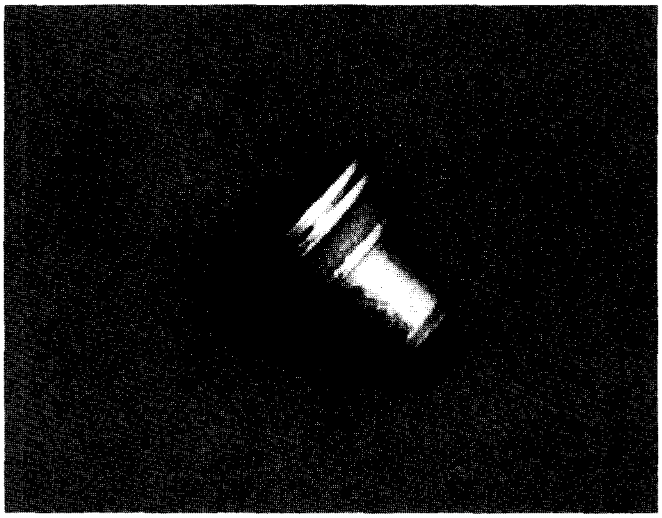
HIGH POWER OUTPUT
Typically: 2.5W from 10 to 14 GHz

HIGH EFFICIENCY

LOW NOISE

HIGH AMBIENT OPERATION
Specified Output Power Available at 50° C Ambients

HIGH RELIABILITY
Designed to Exceed the Requirements of MIL-S-19500



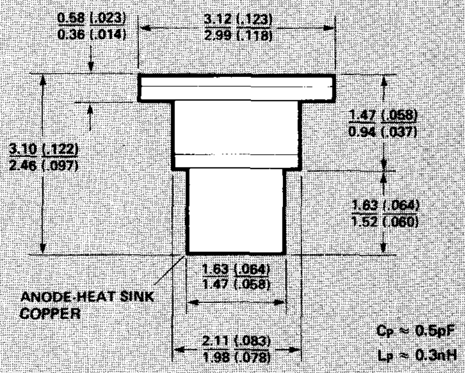
Description/Applications

Double drift silicon IMPATT (IMPact Ionization Avalanche Transit Time) diodes are junction devices operated with reverse bias sufficient to cause avalanche breakdown. Holes and electrons generated in the avalanche region travel across their respective drift regions and are collected at the contacts. The phase delay between voltage and current resulting from the avalanche process in combination with the drift time produces negative resistance at microwave frequencies.

Double drift IMPATT diodes offer advantages of higher power and efficiency, lower junction capacitance per unit area, and lower fm noise, as compared to single drift silicon IMPATT diodes.

Because of their high output power, efficiency and reliability, these devices are ideally suited for use as the active element in oscillators and amplifiers in point-to-point telecommunications links and CW Doppler radar. For more information see HP AN 962 Silicon Double Drift IMPATT Diodes for high power CW microwave applications and HP AN 968 IMPATT Amplifier.

Package Dimensions



DIMENSIONS IN MILLIMETERS AND (INCHES).

OUTLINE 46

Maximum Ratings at $T_{CASE} = 25°C$

Junction Operating Temperature . . . . . -65°C to +250°C

Junction Temperature Rise, ΔT_j . . . . 200°C

Storage Temperature . . . . -65°C to +150°C

Operation of these devices within the above temperature ratings will assure a device Mean Time Between Failure (MTBF) of approximately 1 x 10^7 hours.

Power Dissipation . . . . $\frac{200°C}{\Theta_T}$

Soldering Temperature . . . . 220°C for 5 sec.

Mechanical Specifications

Hewlett-Packard's IMPATT diodes are available in a variety of packages. Special package configuration is available upon request. Contact your local HP Field Office for additional information.

These metal-ceramic packages are hermetically sealed. The cathode studs and flanges are gold-plated Kovar. The anode studs are gold-plated copper. The maximum soldering temperature is 230°C for 5 seconds.

Electrical Specifications at T_A=25°C

Parameter	Symbol	5082-0610	5082-0611	Units	Notes
Minimum CW Output Power	P_O	1.5	2.5	W	1,2 (Fig. 15)
Test Frequency	f_O	11.2		GHz	1

Typical Parameters

Parameter	Symbol	5082-0610	5082-0611	Units	Notes
Efficiency	η	10	10	%	$\eta = \frac{P_O}{P_{IN}} \times 100$
Operating Voltage	V_{OP}	120	120	V	
Operating Current	I_{OP}	130	210	mA	
Breakdown Voltage	V_{BR}	99	99	V	I_R = .5 mA
Junction Capacitance at Breakdown	$C_{J(VBR)}$	0.35	0.7	pF	f = 1 MHz
Thermal Resistance	Θ_T	14	8	°C/W	3
Package Outline	—	46	46	—	—

Notes:
1. Output power measured as an oscillator. Junction temperature is less than 225°C with an ambient temperature of 25°C. Typical diodes satisfy the minimum specification throughout the operating frequency range. Special models tested at other frequencies are available upon special request.
2. The mount for an IMPATT diode must provide an adequate heat flow path away from the diode stud. The junction temperature rise will be: $\Delta T_j = \Theta_T (P_{IN}-P_O)$.
3. Θ_T is measured with the diode mounted in a copper heatsink using the dc avalanche resistance method (see HP AN 935, page 6). Θ_{jc}, use $\Theta_{jc} = \Theta_T$ - 1.5°C/W (1.5°C/W has been found to be a nominal value for a good heat flow path in the diode mount).

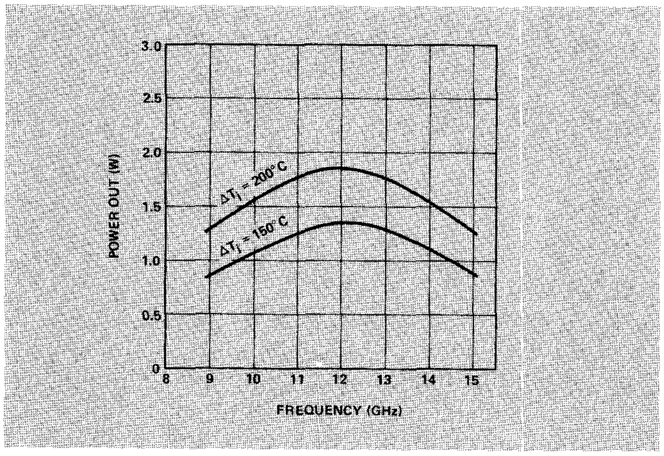


Figure 1. Typical Output Power vs. Frequency, 5082-0610. Output power maximized at each frequency.

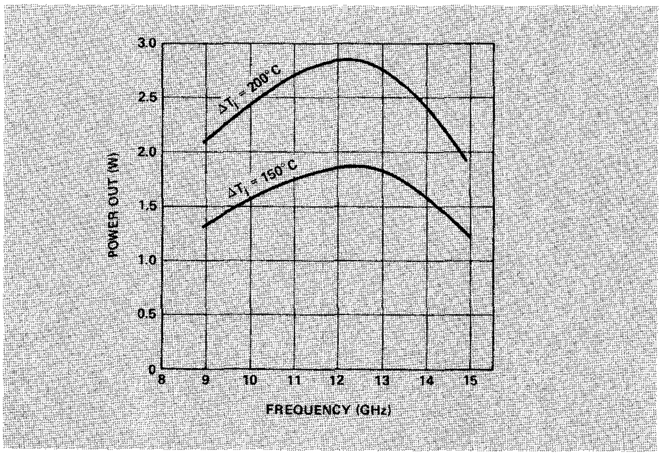


Figure 2. Typical Output Power vs. Frequency, 5082-0611. Output power maximized at each frequency.

Typical Parameters, 5082-0610

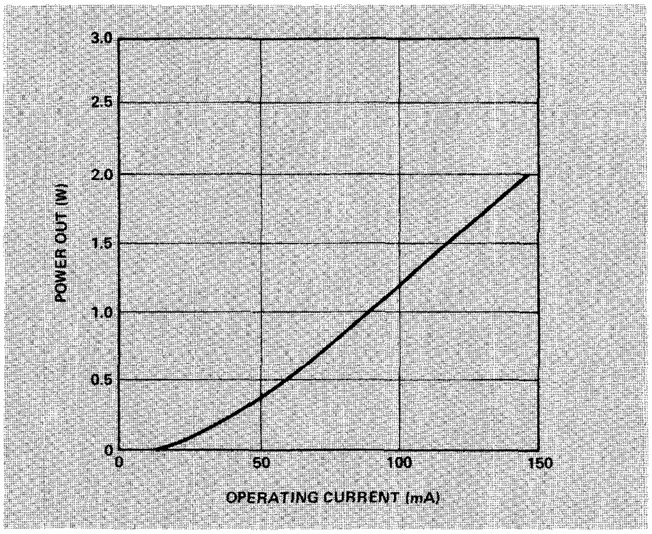


Figure 3. Typical Output Power vs. Operating Current at 11.5 GHz, 5082-0610. Output power maximized at each current level.

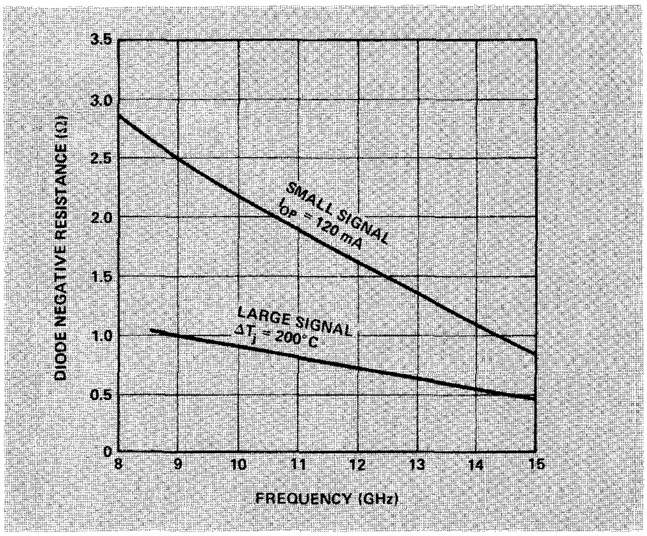


Figure 4. Typical Diode Negative Resistance vs. Frequency, 5082-0610. Large signal values derived with output power maximized at each frequency.

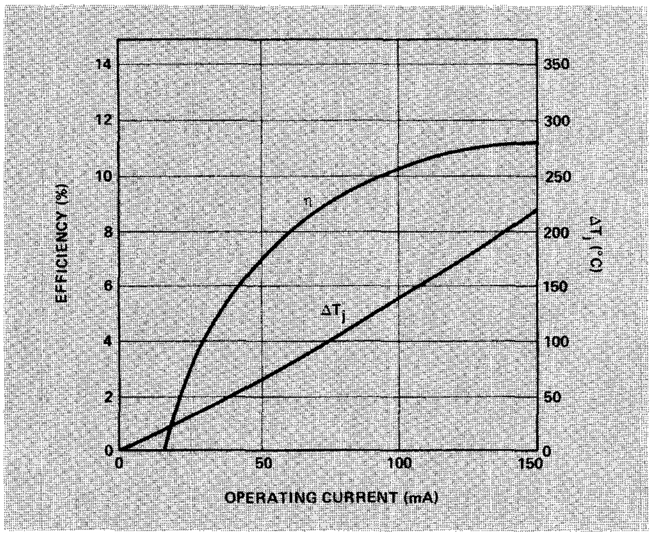


Figure 5. Typical Efficiency and Junction Operating Temperature Rise (ΔTj) vs. Operating Current at 11.5 GHz, 5082-0610. Output power maximized at each current level.

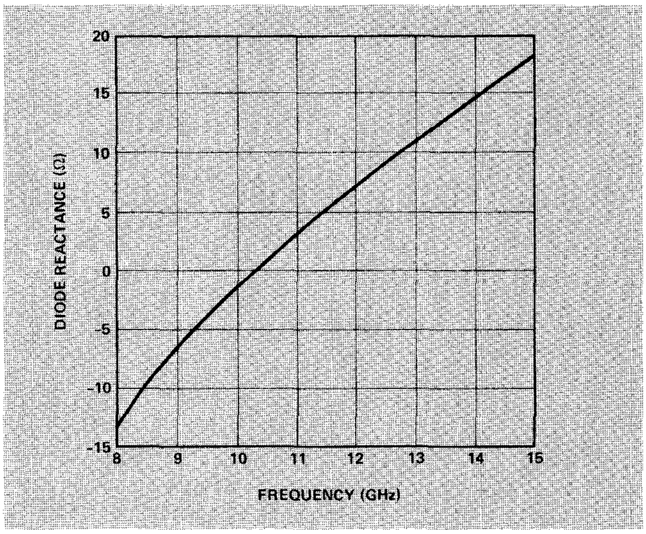


Figure 6. Typical Diode Reactance vs. Frequency, 5082-0610.

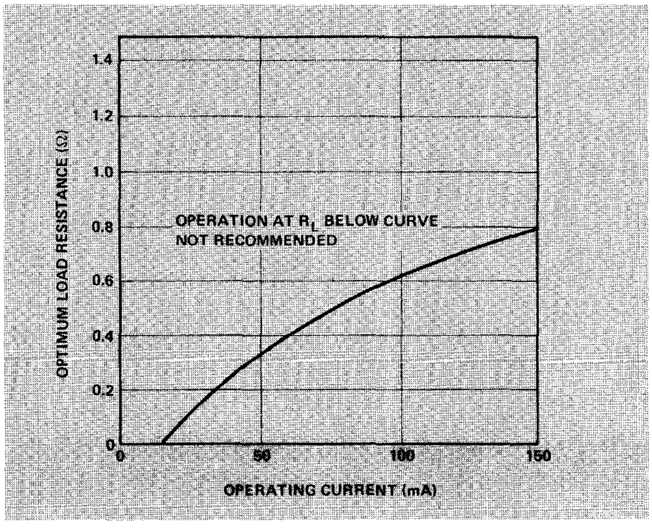


Figure 7. Typical Load Resistance vs. Operating Current at 11.5 GHz, 5082-0610. Output power maximized at each current level.

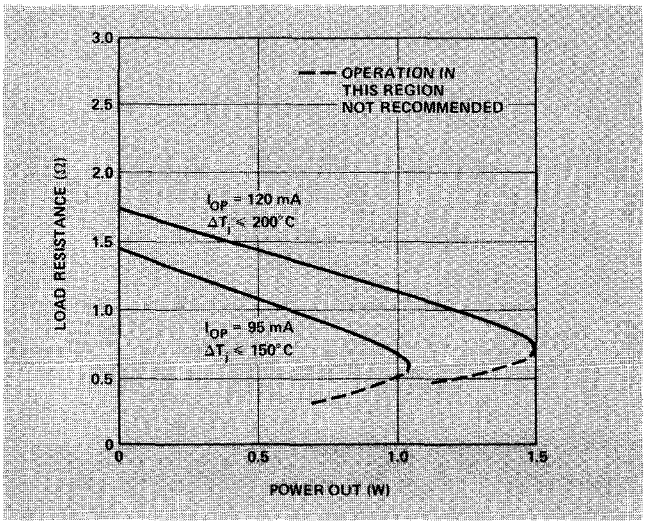


Figure 8. Typical Load Resistance vs. Output Power at 11.5 GHz with ΔTj as a parameter, 5082-0610.

Typical Parameters, 5082-0611

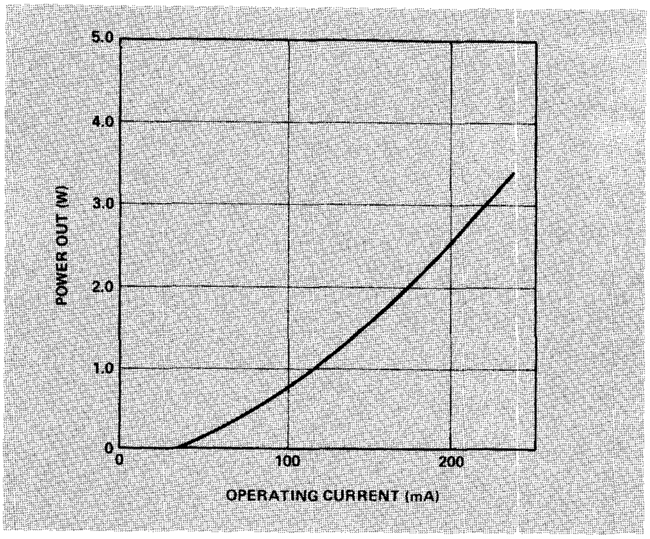


Figure 9. Typical Output Power vs. Operating Current at 11.5 GHz, 5082-0611. Output power maximized at each current level.

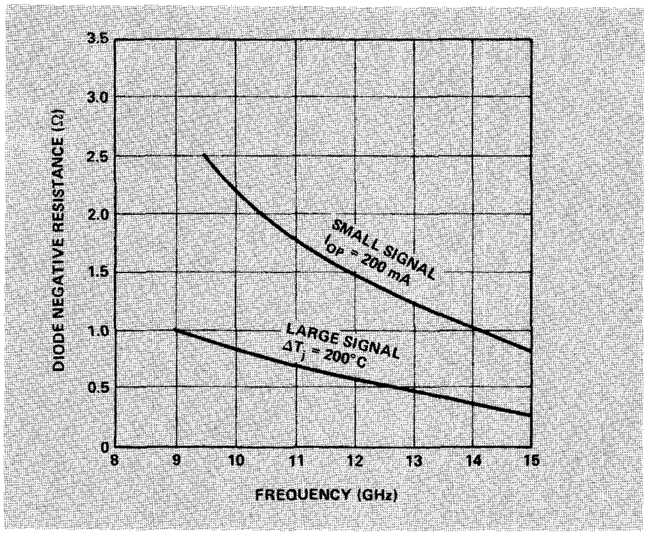


Figure 10. Typical Diode Negative Resistance vs. Frequency, 5082-0611. Large signal values derived with output power maximized at each frequency.

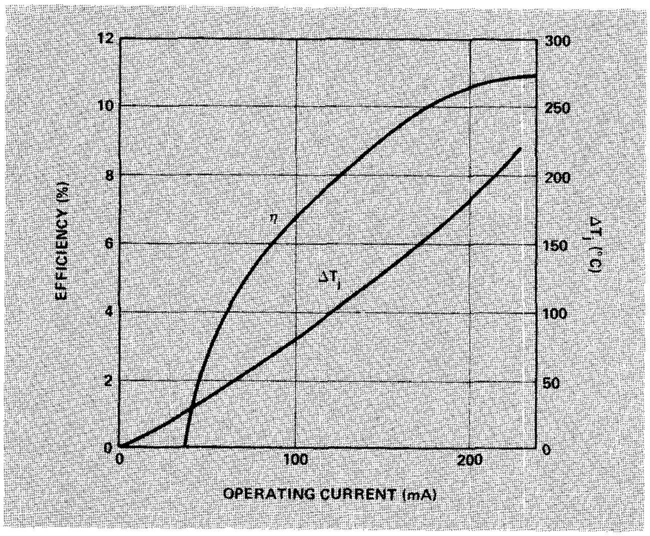


Figure 11. Typical Efficiency and Junction Operating Temperature Rise (ΔTj) vs. Operating Current at 11.5 GHz, 5082-0611. Output power maximized at each current level.

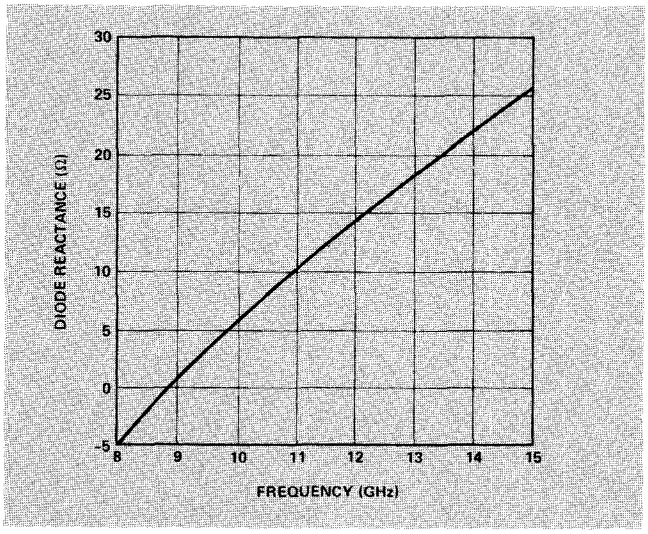


Figure 12. Typical Diode Reactance vs. Frequency, 5082-0611.

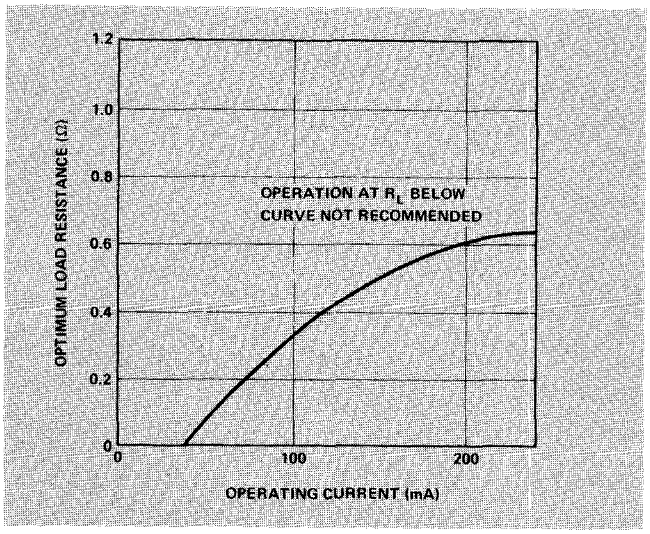


Figure 13. Typical Load Resistance vs. Operating Current at 11.5 GHz, 5082-0611. Output power maximized at each current level.

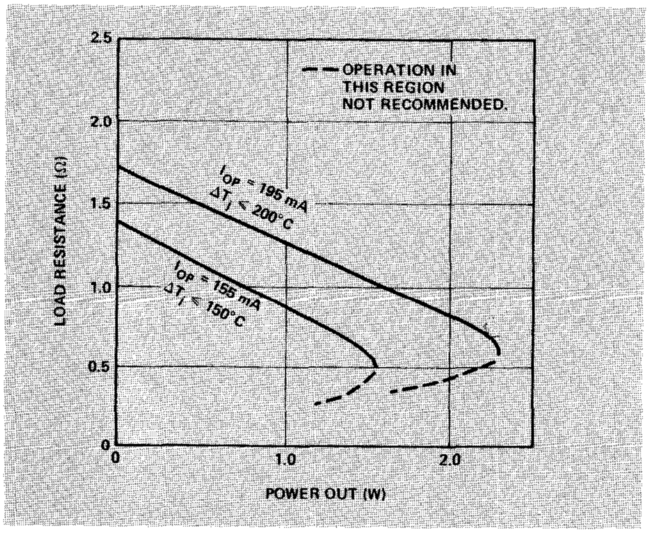


Figure 14. Typical Load Resistance vs. Output Power at 11.5 GHz with ΔTj as a parameter, 5082-0611.

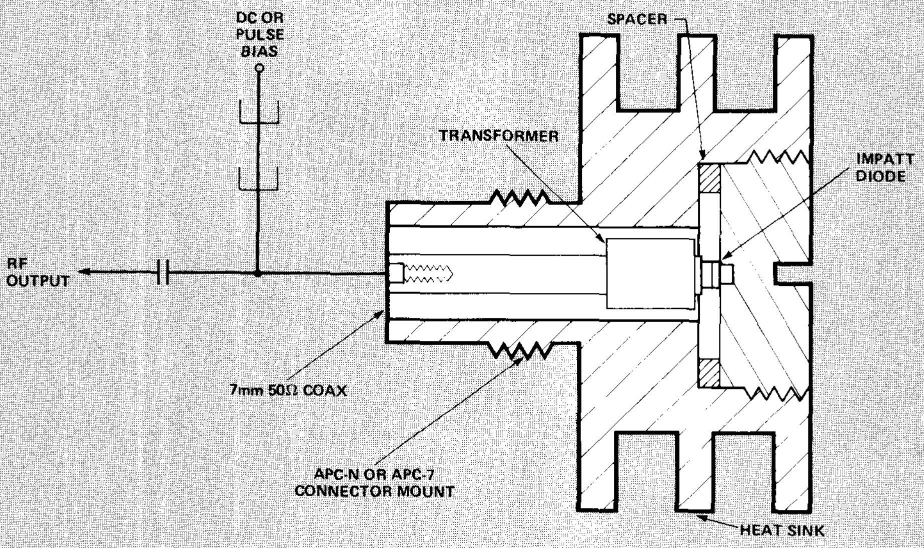


Figure 15. Simplified Drawing of Coaxial Cavity. Detailed mechanical drawings are available on request. A tuning screw should be used with this cavity. The use of fixed tuned cavities is not recommended for IMPATT Diodes. Minor variations of diode impedance among production units require some tuning capability.

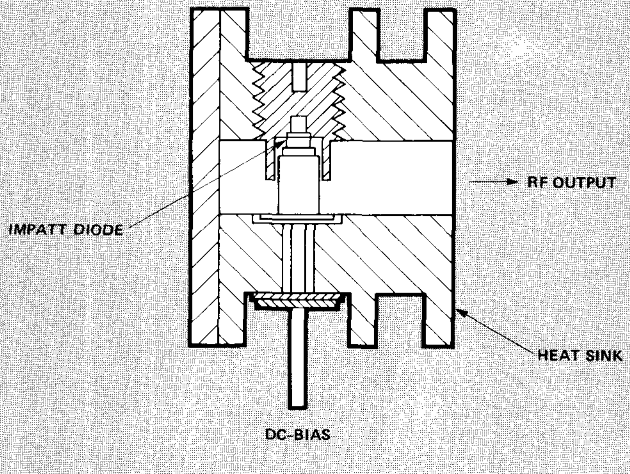


Figure 16. Waveguide Cavity.

HEWLETT PACKARD
COMPONENTS

SILICON DOUBLE DRIFT IMPATT DIODES FOR PULSED POWER SOURCES

5082-0710
X-BAND
5082-0716
Ku-BAND

Features

HIGH PEAK POWER
Typically Greater Than 14W Peak at 10 GHz, and 11W Peak at 16 GHz

HIGH AVERAGE POWER
25% Duty Cycle at Peak Power Rating

HIGH EFFICIENCY
Typically 11%

$\frac{\textbf{SIN x}}{\textbf{x}}$ **SPECTRUM**

HIGH RELIABILITY
Designed to Meet the Requirements of MIL-S-19500

Description/Applications

Silicon double drift IMPATT (IMPact Ionization Avalanche Transit Time) diodes are junction devices operated with reverse bias sufficient to cause avalanche breakdown. Holes and electrons generated in the avalanche region travel across their respective drift regions and are collected at the contacts. The phase delay between voltage and current resulting from the avalanche process in combination with the drift time produces negative resistance at microwave frequencies.

Double drift IMPATTs offer advantages of higher power and efficiency, lower junction capacitance per unit area, and lower fm noise as compared to single drift silicon IMPATTs.

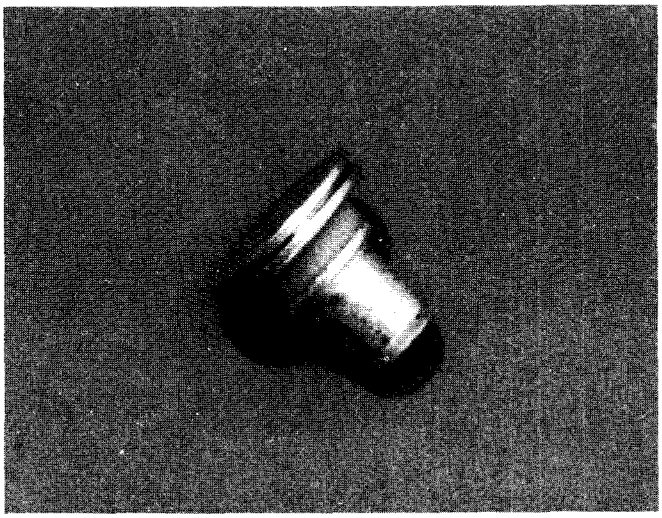
Stable operation at high peak power levels make these devices ideally suited for X and Ku-band pulsed radar applications such as missile guidance systems, lightweight man-pack radar, and active phased array radar. For more information, see AN961, Silicon Double-Drift IMPATT Diodes for Pulse Applications.

Maximum Ratings at $T_{CASE} = 25°C$

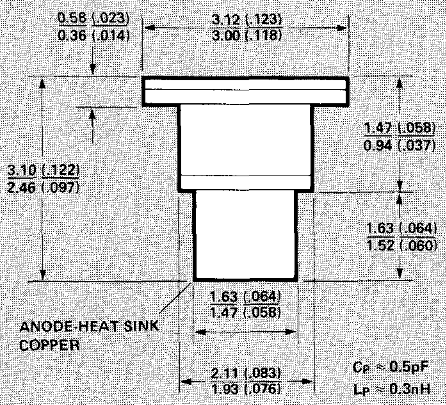
Average Junction Operating Temperature .... -65°C to +225°C
Average Junction Temperature Rise, ΔT_j .... 200°C
Storage Temperature .... -65°C to +150°C

Operation of these devices within the above temperature ratings will assure a device Mean Time Between Failure (MTBF) of approximately 1 x 10⁷ hours.

Power Dissipation .... $\frac{200°C}{\Theta_T}$
Soldering Temperature .... 220°C for 5 sec.



Package Dimensions



ALL DIMENSIONS IN MILLIMETERS AND (INCHES).

OUTLINE 46

Mechanical Specifications

Hewlett-Packard's IMPATT diodes are available in a variety of packages. Special package configuration is available upon request. Contact your local HP Field Office for additional information.

This metal-ceramic package is hermetically sealed. The cathode flange is gold-plated Kovar. The anode stud is gold-plated copper. The maximum soldering temperature is 230°C for 5 seconds.

Electrical Specifications at $T_A = 25°C$

Parameter	Symbol	5082-0710	5082-0716	Units	Notes
Center Frequency	f_O	10	16.5	GHz	1
Minimum Peak Output Power at Center Frequency	P_P	12	9	W	1,2
Minimum Average Output Power at Center Frequency	P_{AVG}	3	2.25	W	1,2

Typical Parameters at $T_A = 25°C$

Parameter	Symbol	5082-0710	5082-0716	Units	Notes
Efficiency	η	11	11	%	1,2
Pulsed Operating Voltage	V_{OP}	145	100	V	
Pulsed Operating Current	I_{OP}	900	900	mA	
Breakdown Voltage	V_{BR}	115	78	V	$I_R = .5mA$
Junction Capacitance at Breakdown	$C_{J(VBR)}$	1.25	0.8	pF	f = 1 MHz
Thermal Resistance	Θ_T	6.5	8.5	°C/W	3

NOTES:

1. Average output power is measured as an oscillator at approximately f_O. Average junction temperature is less than 225°C with an ambient temperature of 25°C. Peak power is calculated using the relationship:

$$P_P = \frac{P_{AVG}}{\text{duty cycle}}$$

2. Measured at a pulse width of 800 ns and a duty cycle of 25%.
3. Θ_T is measured with the diode mounted in a copper heatsink using the dc avalanche resistance method (see HP Application Note 935, page 6).

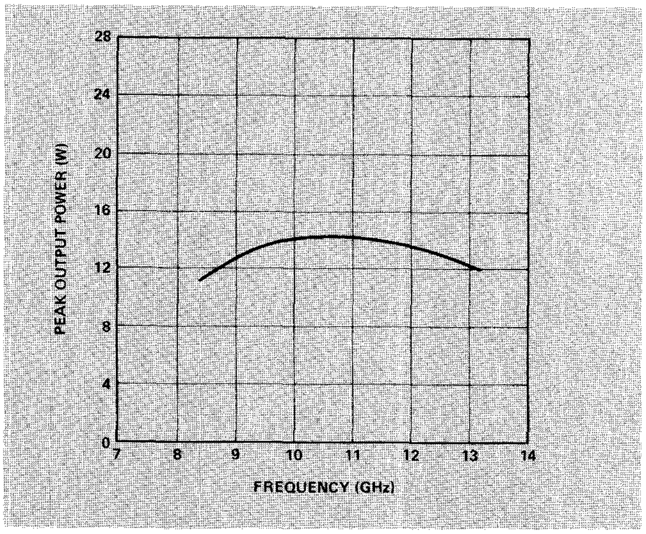


Figure 1. Typical Peak Power Output vs. Frequency, 5082-0710. 800 ns pulse width, 25% duty cycle, $\Delta T_{j\,(avg)} = 175°C$. Output power maximized at each frequency.

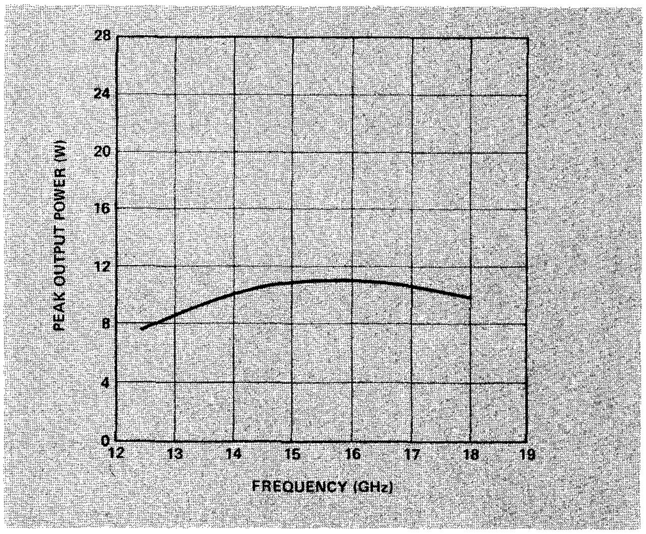


Figure 2. Typical Peak Power Output vs. Frequency, 5082-0716. 800 ns pulse width, 25% duty cycle, $\Delta T_{j\,(avg)} = 175°C$. Output power maximized at each frequency.

Typical Parameters, 5082-0710

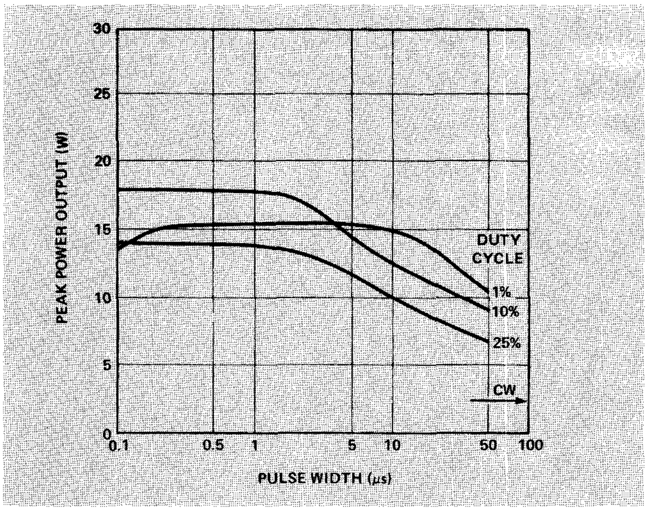


Figure 3. Typical Peak Power Output vs. Pulse Width at 10.5 GHz with duty cycle as a parameter, 5082-0710. ΔTj less than 200°C.

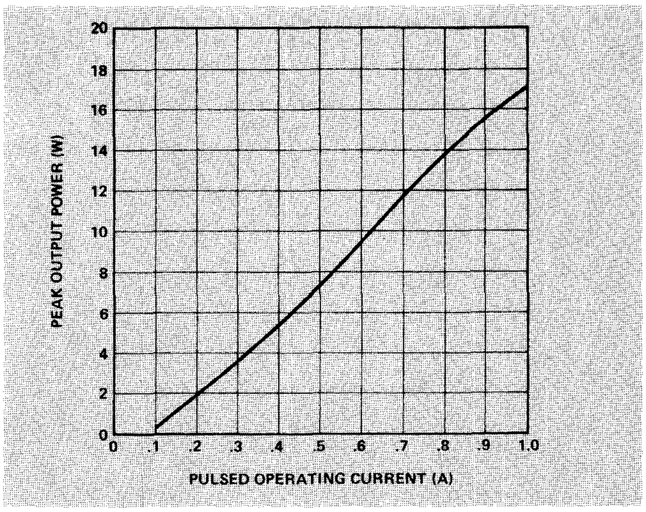


Figure 4. Typical Peak Power Output vs. Pulsed Operating Current, 5082-0710. 800 ns pulse width, 25% duty cycle, 10.5 GHz. Output power maximized at each current level.

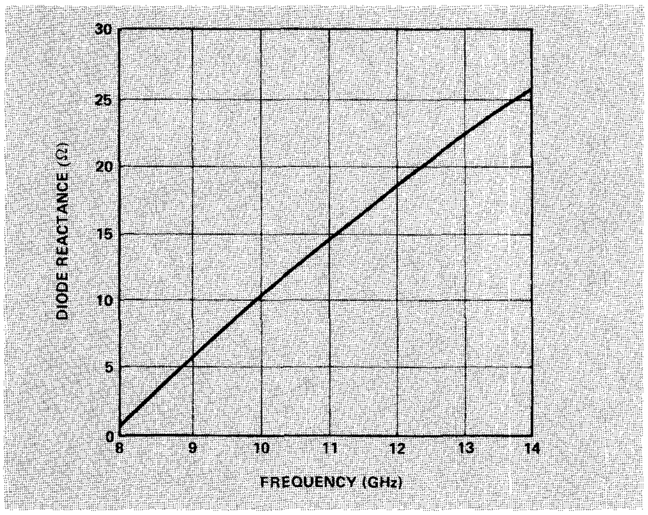


Figure 5. Typical Diode Reactance vs. Frequency, 5082-0710.

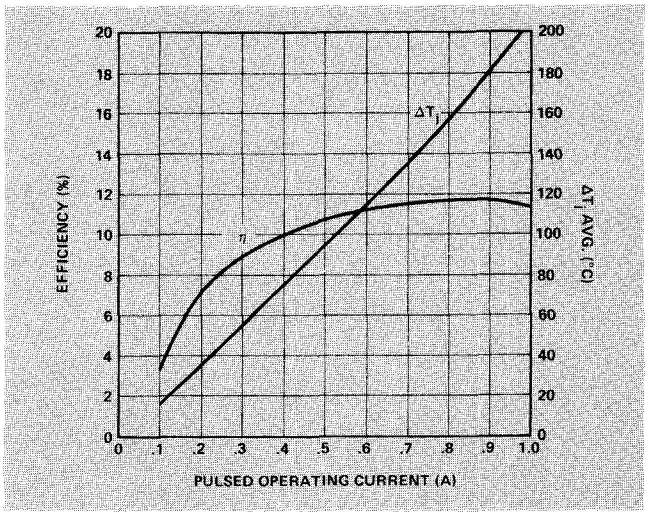


Figure 6. Typical Efficiency and ΔTj (avg) vs. Pulsed Operating Current, 5082-0710. 800 ns pulse width, 25% duty cycle, 10.5 GHz. Output power maximized for each current level.

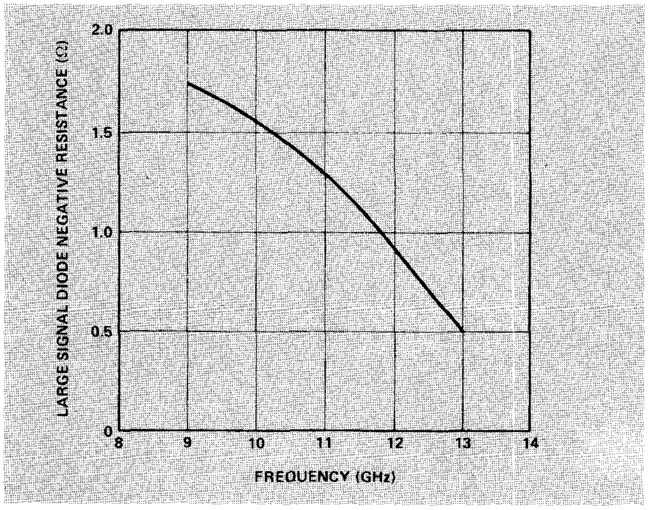


Figure 7. Typical Large Signal Diode Negative Resistance vs. Frequency, 5082-0710.

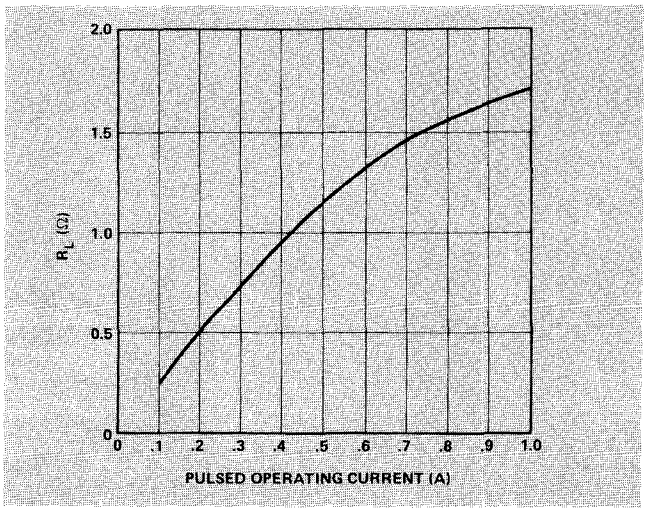


Figure 8. Typical Load Resistance vs. Pulsed Operating Current, 5082-0710. 800 ns pulse width, 25% duty cycle, 10.5 GHz. Output power maximized for each current level.

Typical Parameters, 5082-0716

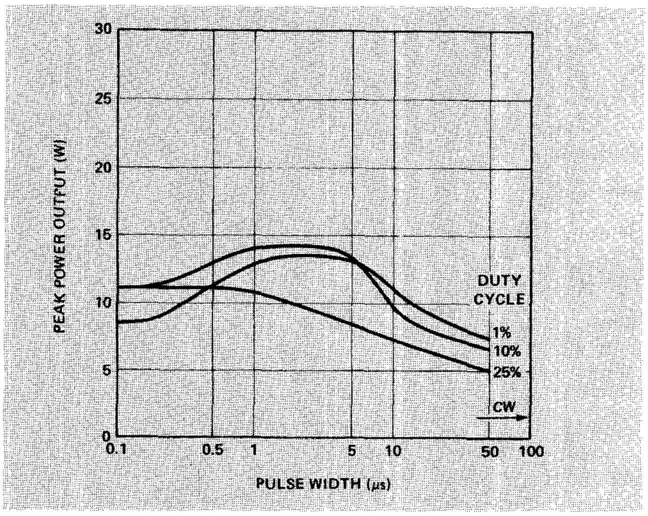


Figure 9. Typical Peak Power Output vs. Pulse Width at 16.5 GHz with duty cycle as a parameter, 5082-0716. Tj less than 200°C.

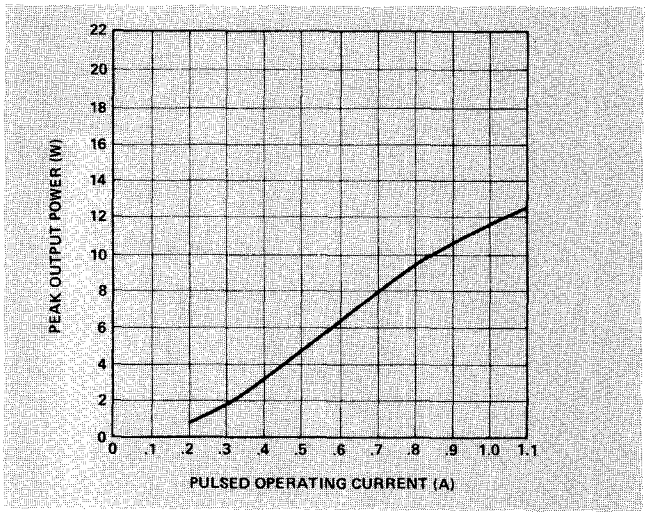


Figure 10. Typical Peak Power Output vs. Pulsed Operating Current, 5082-0716. 800 ns pulse width, 25% duty cycle, 16.5 GHz. Output power maximized at each current level.

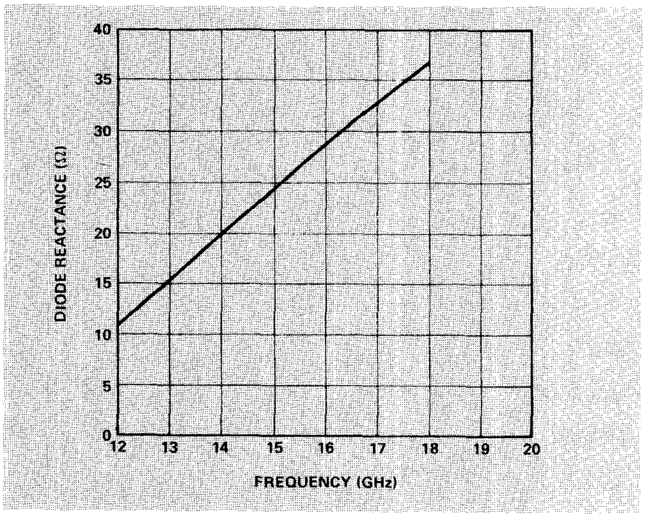


Figure 11. Typical Diode Reactance vs. Frequency, 5082-0716.

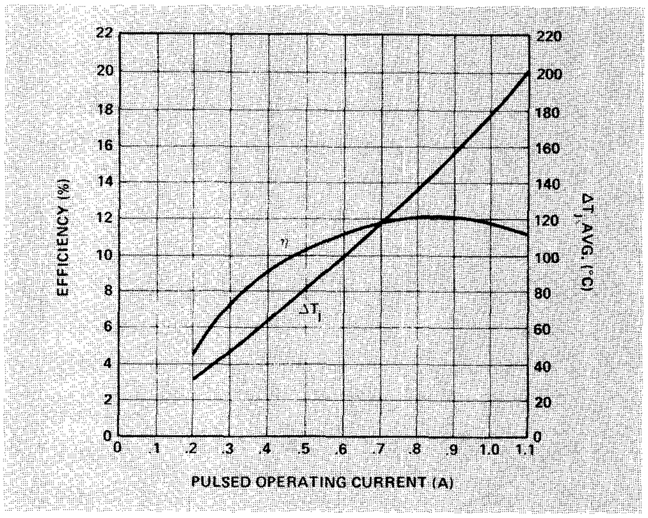


Figure 12. Typical Efficiency and ΔT_j (avg) vs. Pulsed Operating Current, 5082-0716. 800 ns pulse width, 25% duty cycle, 16.5 GHz. Output power maximized for each current level.

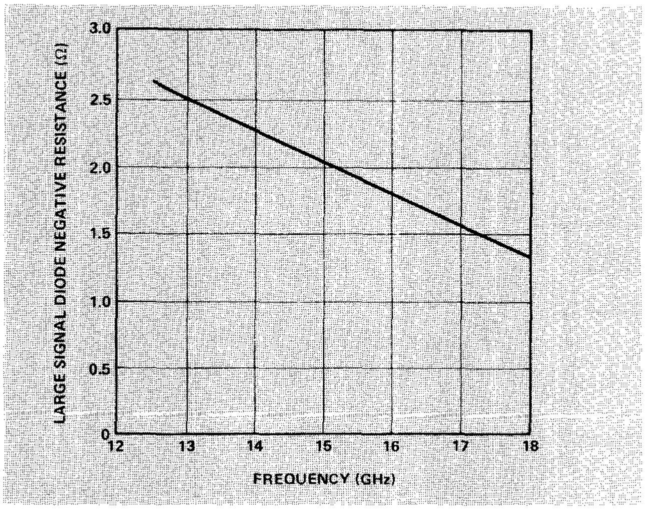


Figure 13. Typical Large Signal Diode Negative Resistance vs. Frequency, 5082-0716.

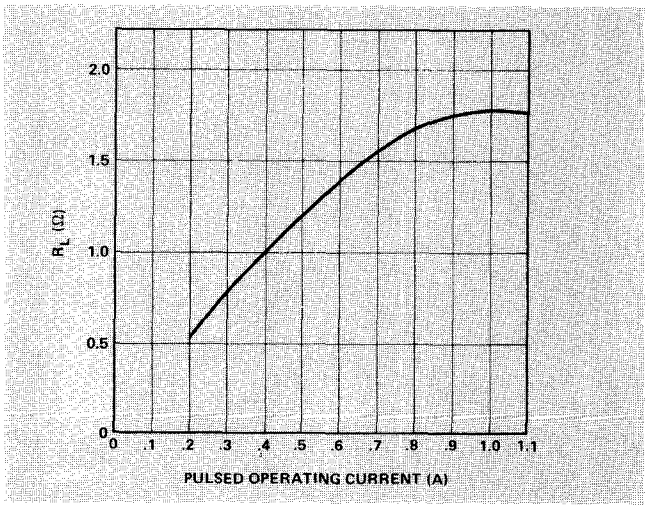


Figure 14. Typical Load Resistance vs. Pulsed Operating Current, 5082-0716. 800 ns pulse width, 25% duty cycle, 16.5 GHz. Output power maximized for each current level.

NOTES

Devices for Hybrid Integrated Circuits

Hewlett-Packard offers a complete line of RF, microwave and switching semiconductor diodes and transistors in forms especially designed for hybrid integrated circuits.

Diodes included are Schottky barrier diodes for RF and microwave switches, mixers and detectors; PIN diodes for RF and microwave switches and AGC attenuators, step recovery diodes for comb generators and frequency multipliers. Bipolar transistors for low noise and linear power, GaAs FETs for low noise and medium power.

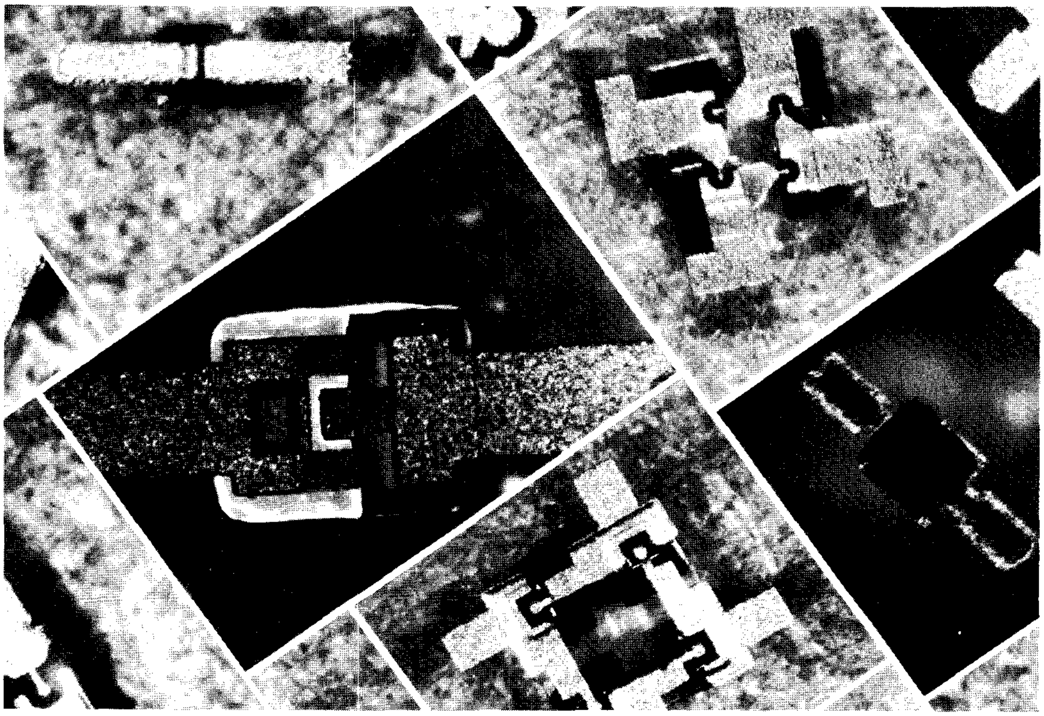
In addition to chips, package forms include the LID (Leadless Inverted Device), Ministrip, Microstrip Post and Beam Lead.

Although all devices offered are passivated, it is recommended that the end item be hermetically sealed for maximum stability and reliability.

Most DC and RF parameters can be specially tested and guaranteed. Contact your local HP sales office for assistance if special specification is required.

Although not all are listed, most Hewlett-Packard diodes are available in chip form. Any available chip can be supplied in any of the carriers listed. Contact your local HP sales office for price, availability, and specifications of any special device.

Beam Leads



Beam Lead Selection Guide

SINGLE MICROWAVE SCHOTTKY DIODES (PAGE 176)

Recommended Freq. Limit	Barrier	D.C. Specified 5082-	R.F. Specified 5082-
12.4 GHz	Low	2229	—
	Medium	2709	2768
18 GHz	Low	2299	—
	Medium	2716	2769
100 GHz	Low	2264	—
	Medium	2767	—

MICROWAVE SCHOTTKY QUADS (PAGE 181)

	Recommended Frequency	To 2 GHz	2-4 GHz	4-8 GHz	8-12 GHz	12-18 GHz
Part No. 5082-	Low Barrier	9697	9697	9395	9397	9399
	Medium Barrier	9696	9696	9394	9396	9398

MICROWAVE PIN DIODES

Series Resistance	Capacitance	Part Number	Page Number
1.3Ω at 10 mA	0.12 pF at 20V	HPND-4050	185
1.8Ω at 10 mA	0.07 pF at 30V	HPND-4001	
6Ω at 50 mA	0.02 pF at 0V	5082-3900	183

HEWLETT hp PACKARD
COMPONENTS

BEAM LEAD SCHOTTKY DIODE

5082-2837

Features

LOW COST

FAST SWITCHING

HIGH BREAKDOWN

Description

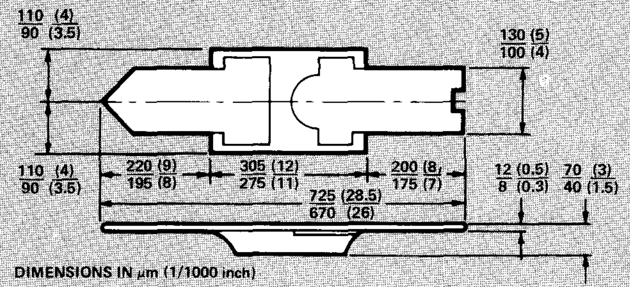
The HP 5082-2837 is an epitaxial planar passivated Beam Lead Diode whose construction utilizes a unique combination of both a conventional PN junction and a Schottky barrier. This manufacturing process results in a device which has the high breakdown and temperature characteristics of silicon, the turn-on voltage of germanium and the speed of a Schottky diode majority carrier device.

This device is intended for high volume, low cost applications, and is the beam lead equivalent of the HP 5082-2800 glass packaged diode.

Applications

High level detection, switching, or gating; logarithmic or A-D converting; sampling or wave shaping are jobs the 5082-2837 will do better than conventional PN junction diodes. The low turn-on voltage and subnanosecond switching makes it extremely attractive in digital circuits for DTL gates, pulse shaping circuits or other low level applications. Its high PIV allows wide dynamic range for fast high voltage sampling gates.

The 5082-2837 low turn-on voltage gives low offsets. The extremely low stored charge minimizes output offsets caused by the charge flow in the storage capacitor. At UHF, the diodes exhibit 95% rectification efficiencies. Both their low loss and their high PIV allow the diodes to be used in mixer and modulator applications which require wide dynamic ranges.



DIMENSIONS IN μm (1/1000 inch)

Outline 10

The combination of these technical features with the low price make these devices the prime consideration for any hybrid dc or RF circuit requiring nonlinear elements.

Absolute Maximum Ratings at T_A=25°C

Operating Temperature Range	-60°C to +150°C
Storage Temperature Range	-60°C to +150°C
Maximum Lead Pull	2 Gms

Operation of these devices within the above temperature ratings will assure a device Mean Time Between Failure (MTBF) of approximately 1 x 10^7 hours.

Electrical Specifications at T_A=25°C

Specification	Symbol	Min.	Max.	Units	Test Conditions
Breakdown Voltage	V_{BR}	70	–	Volts	I_R = 10μA
Forward Voltage	V_{F1}	–	410	mV	I_{F1} = 1mA
Forward Voltage	V_{F2}	–	1.0	V	I_{F2} = 15mA
Reverse Leakage Current	I_R	–	200	nA	V_R = 50V
Capacitance	C_o	–	2.0	pF	V_R = 0V and f= 1MHz
Effective Minority Carrier Lifetime	τ	–	100 *	pS	I_F = 5mA Krakauer Method

* Typical

Bonding Recommendations

Beam lead devices are silicon chips with coplanar plated gold tabs that extend parallel to the top surface of the chip approximately 8 mils beyond the edge. The leads are approximately 4 mils wide by 1/2 mil thick and are mounted by thermocompression bonding to the substrate metallization. The bonding is accomplished by placing the device face down with the tabs resting flat on the pad area and using heated wedge (and/or substrate), or parallel-gap (spot-welding) techniques.

The heated wedge may be continuously heated, as in most standard equipment, or it may be pulse resistance heated where a high current, short duration pulse is used to raise the wedge to the required temperature. In the spot-welding operation, current is passed through the substrate metallization and the device lead. Most of the heat is generated at the interface between the two, where the bond is formed.

The major advantage of pulse heating techniques is that a cold ambient may be used, generating only localized heating in the vicinity of the bond itself. The electrodes (or wedge) can be placed on the device lead while the bond area is cold, and maintain a constant force through the heating and cooling cycle.

Handling Instructions

The mechanical and electrical performance characteristics of beam lead diodes require careful and considerate handling during inspection, testing, and assembly. The handling techniques described here are necessary so that the diodes will not be mechanically or electrically damaged, particularly where reverse voltages approach the diode breakdown rating.

Visual Inspection

The enclosed beam lead diodes may be viewed through the transparent underside of the shipping tray without its being opened.

Unloading

1. Open the lid, remove the foam pad, and carefully lift off the antistatic fabric liner.

2. A vacuum pickup with a #27 tip is recommended for picking up single beam lead devices. This should be done under 20X magnification for accurate positioning of the tip on the die.

3. Replace the fabric and pad for storage of unused devices.

HEWLETT PACKARD
COMPONENTS

BEAM LEAD SCHOTTKY DIODES FOR MIXERS AND DETECTORS (1-18 GHz)

5082-2229 5082-2716
5082-2264 5082-2767
5082-2299 5082-2768
5082-2509 5082-2769
5082-2510 5082-2778
5082-2709 5082-2779

Features

PLANAR SURFACE
Easier Bonding, Stronger Leads

PASSIVATED
Stable, Reliable Performance

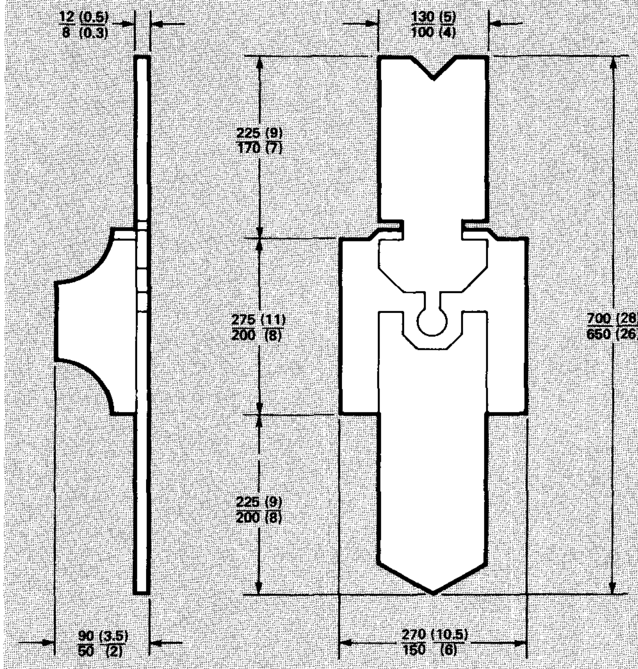
LOW NOISE FIGURE
6 dB Typical at 9 GHz

HIGH UNIFORMITY
Tightly Controlled Process Insures Uniform RF Characteristics

Description

These beam lead diodes are constructed using a metal-semiconductor Schottky barrier junction. Advanced epitaxial techniques and precise process control insure uniformity and repeatability of this planar passivated microwave semiconductor.

During manufacturing, gold leads are deposited onto a glass passivation layer before the wafer is separated into dice. This provides exceptional lead strength.



DIMENSIONS IN µm (1/1000 inch)

Outline 05

Applications

The beam lead diode is ideally suited for use in stripline or microstrip circuits. Its small physical size and uniform dimensions give it low parasitics and repeatable RF characteristics through Ku-band.

The basic medium barrier devices in this family are DC tested 5082-2709, -2716, and -2767. Batch matched versions are available as the 5082-2509 and -2510. Equivalent low barrier devices are 5082-2229, -2299 and -2264.

For applications requiring guaranteed RF performance, the 5082-2768 is selected for 6.5 dB maximum noise figure at 9.375 GHz, with RF matched pairs available as the 5082-2778. The 5082-2769 is rated at 7.5 dB maximum noise figure at 16 GHz with RF matched pairs available as the 5082-2779.

Application Note 963 is a treatise on impedance matching for mixer and detector circuits using the -2709 as an example.

Maximum Ratings

Pulse Power Incident at $T_A = 25°C$	1W
CW Power Dissipation at $T_A = 25°C$	300mW
T_{OPR} — Operating Temperature Range	-60°C to +150°C
T_{STG} — Storage Temperature Range	-60°C to +150°C
Maximum Pull On Any Lead	2 grams
Diode Mounting Temperature	220°C for 10 sec. max.

Operation of these devices within the above temperature ratings will assure a device Mean Time Between Failure (MTBF) of approximately 1 x 10^7 hours.

DC Electrical Specifications at $T_A = 25°C$

MEDIUM BARRIER

Parameter	Symbol	5082-2709/† -2768/-2778	5082-2716/ -2769/-2779	5082-2767	Units	Test Conditions
Minimum Breakdown Voltage	V_{BR}	3	3	3	V	$I_R = 10\mu A$
Maximum Forward Voltage	V_F	1.0			V	$I_F = 20$ mA
Maximum Total Capacitance	C_T	0.25	0.15	0.10	pF	$V_R = 0V$, f = 1MHz
Typical Forward Voltage	V_F		450		mV	$I_F = 1mA$
DC Batch Matched Units*	—	5082-2509 †	5082-2510	—	—	$\Delta V_F \leq 15mV$ at 5mA

† $I_F = 30mA$

LOW BARRIER

Parameter	Symbol	5082-2229	5082-2299	5082-2264	Units	Test Conditions
Minimum Breakdown Voltage	V_{BR}	3	3	3	V	$I_R = 10\mu A$
Maximum Forward Voltage	V_F	1V at 30mA	1V at 20mA	1V at 20mA	V	I_F — as shown
Maximum Total Capacitance	C_T	0.25	0.15	.10	pF	$V_R = 0V$, f = 1MHz
Typical Forward Voltage	V_F	250			mV	$I_F = 1mA$

RF Electrical Specifications at $T_A = 25°C$

MEDIUM BARRIER

Parameter	Symbol	5082-2768	5082-2769	Units	Test Conditions
Maximum Noise Figure	NF_{SSB}	6.5 at 9.375 GHz	7.5 at 16 GHz	dB	1mW L.O. Power IF = 30 MHz, 1.5 dB NF
Maximum SWR	SWR	1.5:1	1.5:1	—	
IF Impedance	Z_{IF}	250-500	250-500	Ω	
RF Batch Matched Units*	—	5082-2778	5082-2779	—	$\Delta NF \leq 0.3$ dB, $\Delta Z_{IF} \leq 25\Omega$

*Minimum batch size 20 units.

Typical Detector Characteristics at $T_A = 25°C$

MEDIUM BARRIER

Parameter	Symbol	Typical Value	Units	Test Conditions
Tangential Sensitivity	TSS	-54	dBm	20μA Bias Video Bandwidth = 2 MHz f = 10 GHz
Detection Sensitivity	γ	6.6	mV/μW	
Video Resistance	R_V	1400	Ω	

LOW BARRIER

Parameter	Symbol	Typical Value	Units	Test Conditions
Tangential Sensitivity	TSS	-42	dBm	Zero Bias Video Bandwidth = 2 MHz f = 10 GHz
Detection Sensitivity	γ	8	mV/μW	
Video Resistance	R_V	400	kΩ	

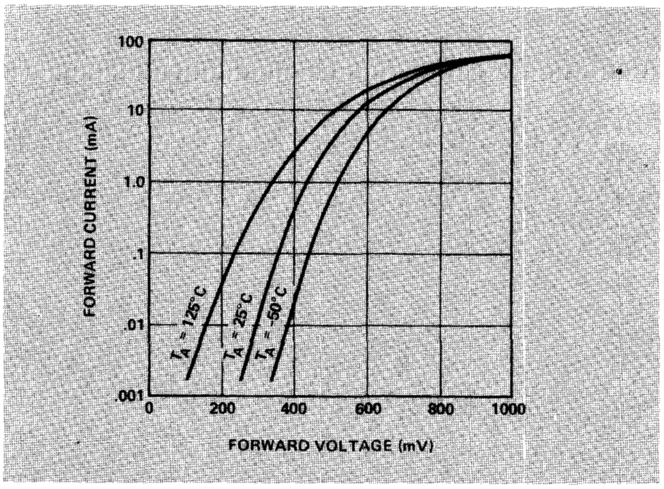


Figure 1. Typical Forward Characteristics, 5082-2709, -2509, -2768 and -2778.

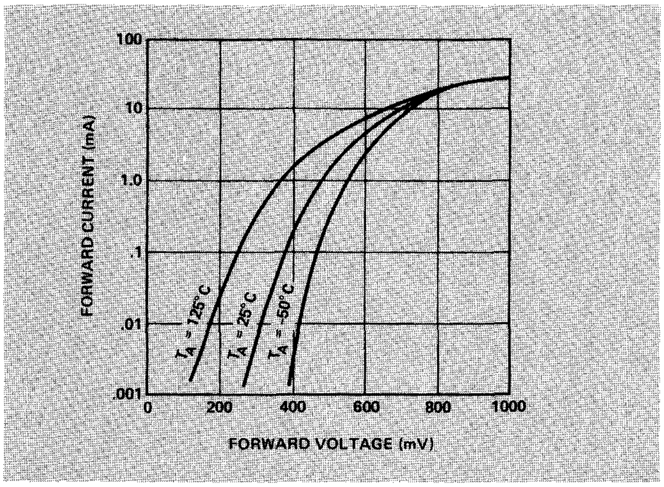


Figure 2. Typical Forward Characteristics, 5082-2716, -2510, -2767, -2769 and -2779.

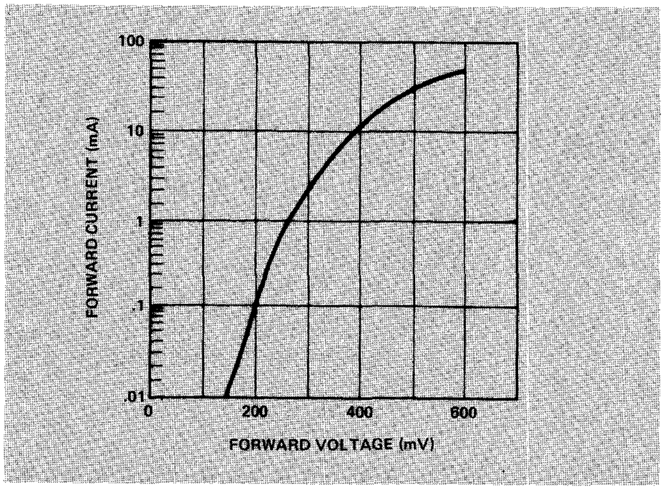


Figure 3. Typical Forward Characteristics, 5082-2229, at 25° C.

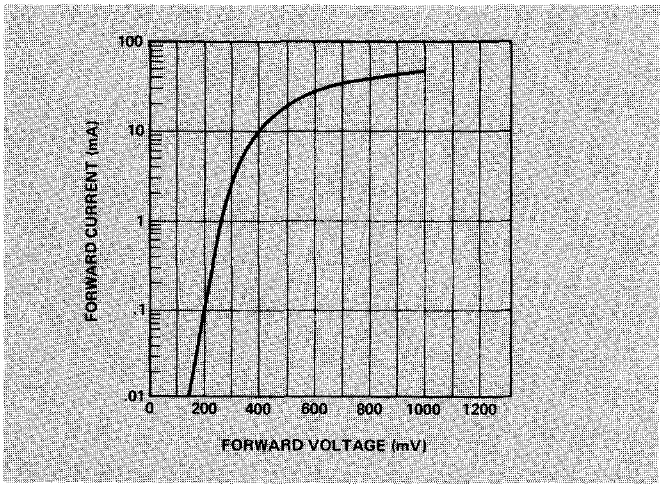
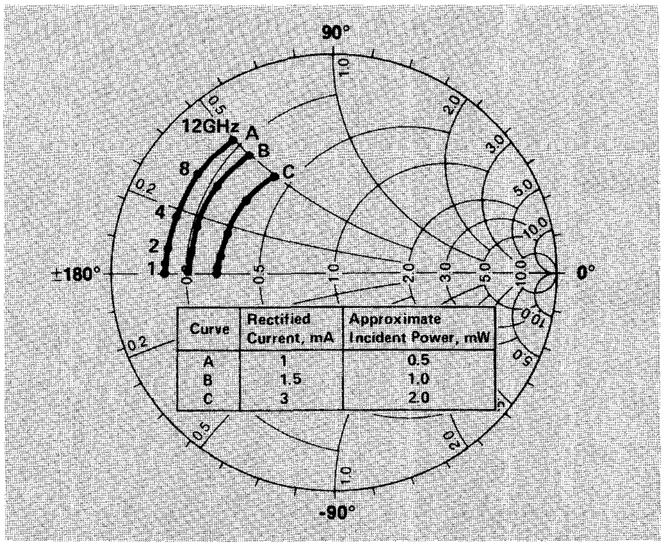


Figure 4. Typical Forward Characteristics, 5082-2299, -2264 at 25° C.



Curve	Rectified Current, mA	Approximate Incident Power, mW
A	1	0.5
B	1.5	1.0
C	3	2.0

Figure 5. Typical Admittance Characteristics, 5082-2709, -2509, -2768 and -2778 with Self Bias.

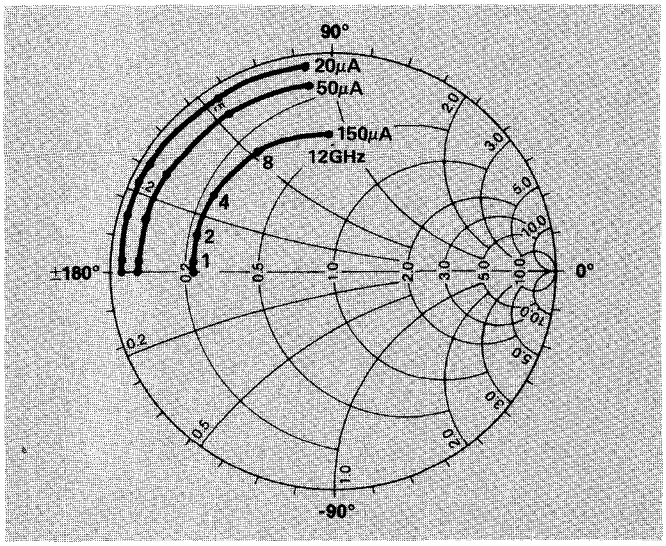
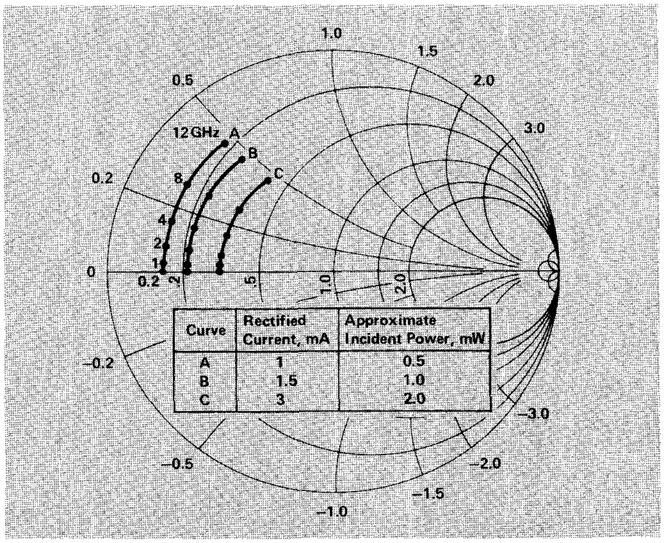


Figure 6. Typical Admittance Characteristics, 5082-2709, -2509, -2768 and -2778 with External Bias.



Curve	Rectified Current, mA	Approximate Incident Power, mW
A	1	0.5
B	1.5	1.0
C	3	2.0

Figure 7. Typical Admittance Characteristics, 5082-2716, -2510, -2767, -2769 and -2779 with Self Bias.

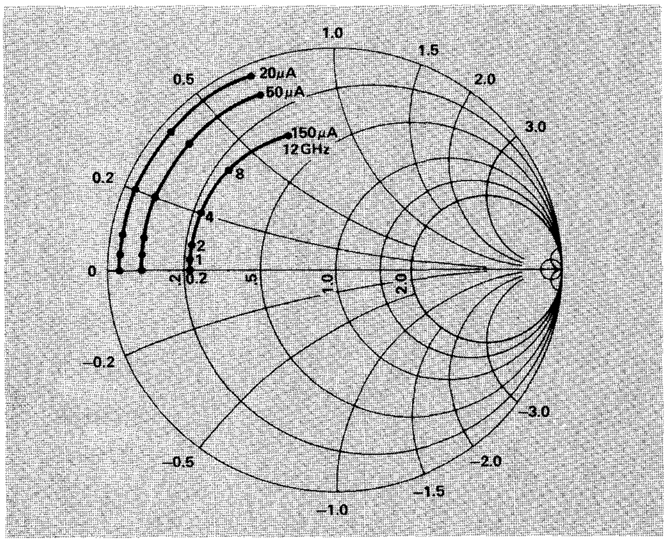


Figure 8. Typical Admittance Characteristics, 5082-2716, -2510, -2767, -2769 and -2779 with External Bias.

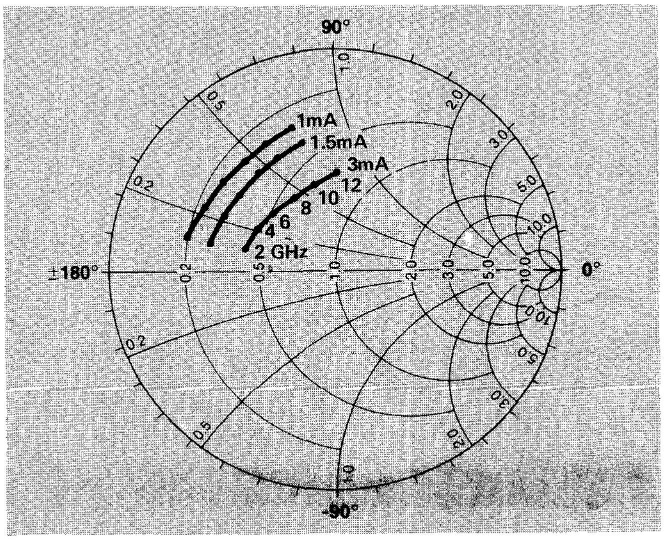


Figure 9. Typical Admittance Characteristics, 5082-2229 with Self Bias.

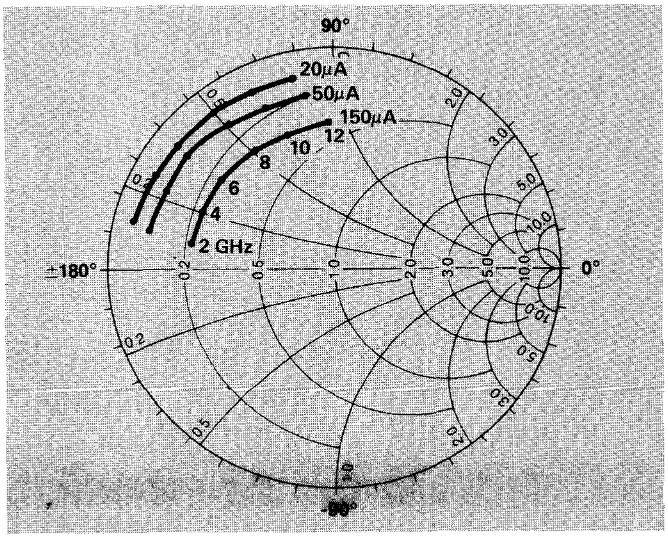


Figure 10. Typical Admittance Characteristics, 5082-2229 with External Bias.

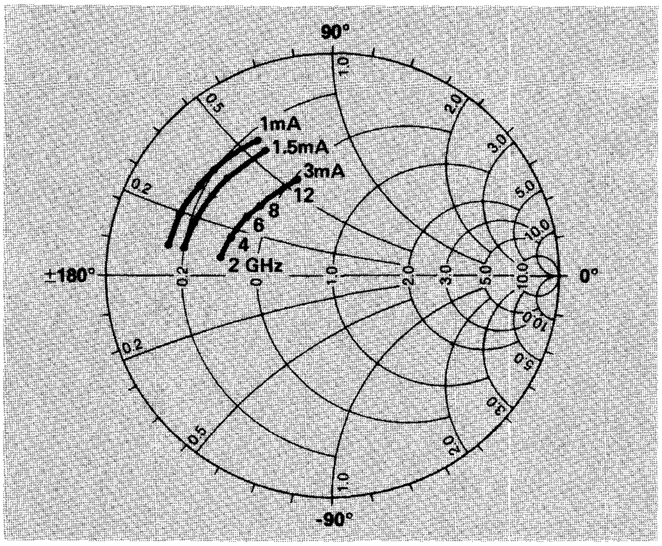


Figure 11. Typical Admittance Characteristics, 5082-2299, -2264, with Self Bias.

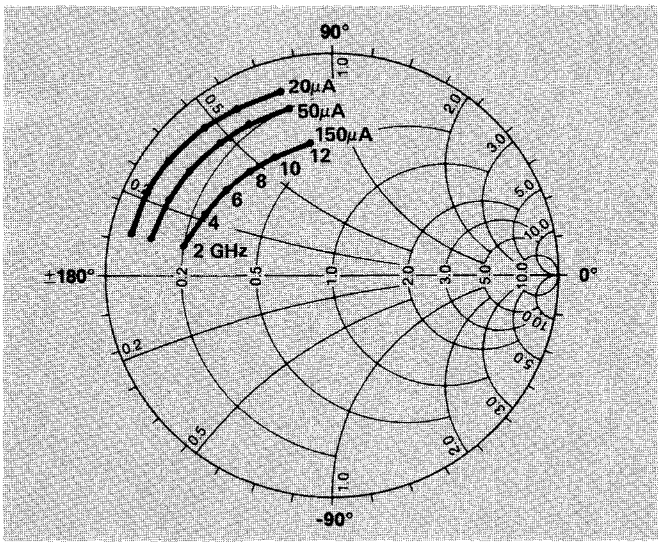


Figure 12. Typical Admittance Characteristics, 5082-2299, -2264, with External Bias.

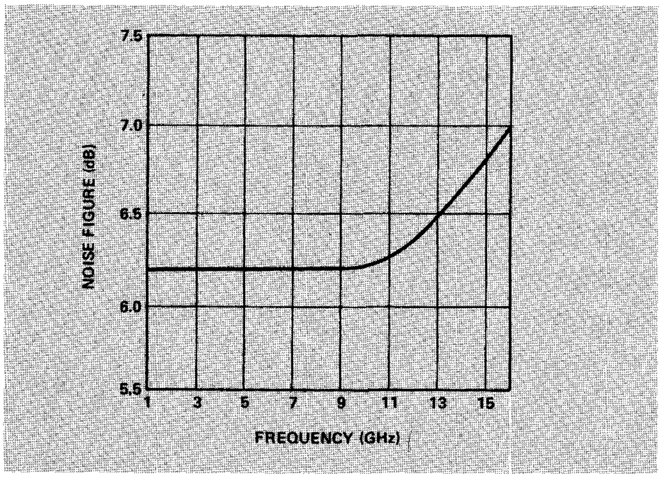


Figure 13. Typical Noise Figure vs. Frequency.

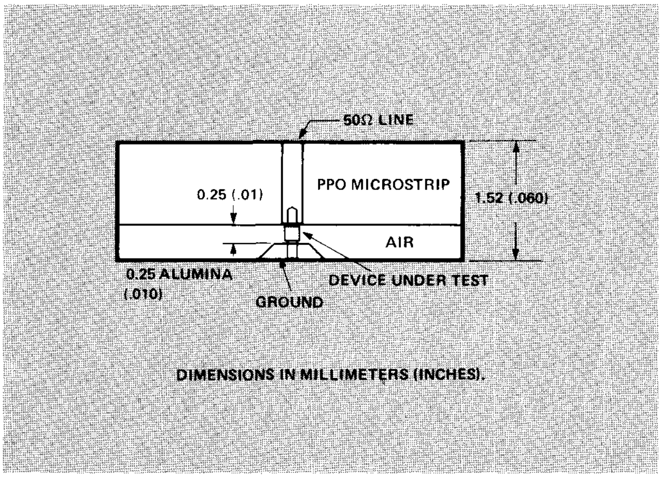
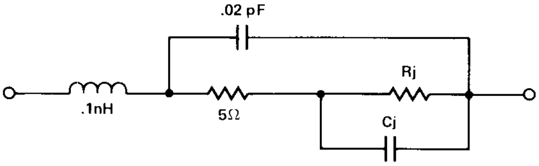


Figure 14. Admittance Test Circuit.

Notes: 1. 1 μs pulse, Du = .001.

2. Power absorbed by the diode. DC load resistance <1Ω.

MODELS FOR BEAM LEAD SCHOTTKY DIODES



Medium Barrier Diodes

Diode	1.5mA Self Bias		20μADC Bias	
	Rj(Ω)	Cj(pF)	Rj(Ω)	Cj(pF)
5082-2768	230	.12	2770	.19
5082-2769	230	.09	2440	.14

SEE PAGE 182 FOR HANDLING AND BONDING RECOMMENDATIONS.

Low Barrier Diodes

Diode	1.5mA Self Bias		20μADC Bias	
	Rj(Ω)	Cj(pF)	Rj(Ω)	Cj(pF)
5082-2229	175	.16	1010	.17
5082-2299	220	.13	900	.15

HEWLETT hp PACKARD

COMPONENTS

BEAM LEAD SCHOTTKY DIODE QUADS FOR DOUBLE BALANCED MIXERS (1-18 GHz)

5082-9394-9399
5082-9696-9697

Features

PLANAR SURFACE
Easier Bonding, Stronger Leads

PASSIVATED
Stable, Reliable Performance

HIGH UNIFORMITY
Tightly Controlled Process Insures Uniform RF Characteristics

Description

These beam lead diodes are constructed using a metal-semiconductor Schottky barrier junction. Advanced epitaxial techniques and precise process control insure uniformity and repeatability of this planar passivated microwave semiconductor.

During manufacturing, gold leads are deposited onto a glass passivation layer before the wafer is separated. This provides exceptional lead strength.

These monolithic arrays of Schottky diodes are interconnected in ring configuration. The relative proximity of the diode junctions on the wafer assures uniform electrical characteristics among the four diodes which constitute a matched quad. They are designed for microstrip or stripline use. The leads provide a good continuity of transmission line impedance to the diode.

Applications

These diodes are designed for use in double balanced mixers, phase detectors, AM modulators, and pulse modulators requiring wideband operation and small size.

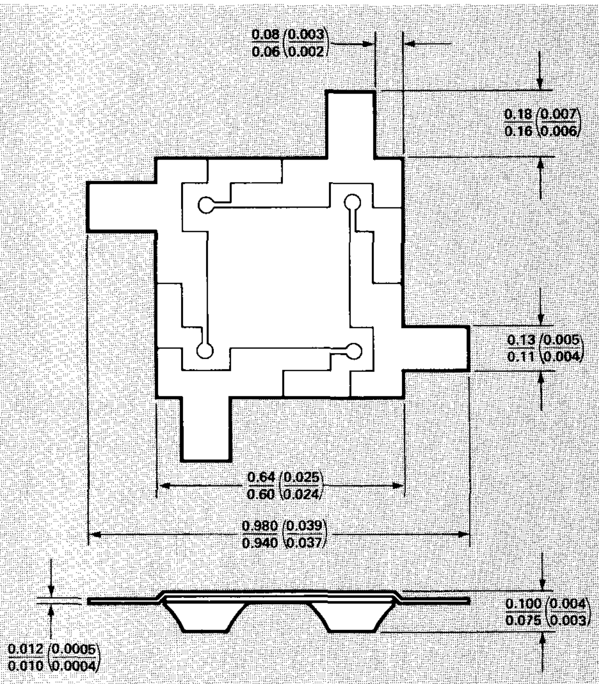
Maximum Ratings

Junction Operating and Storage Temperature Range .... -65° C to +150° C

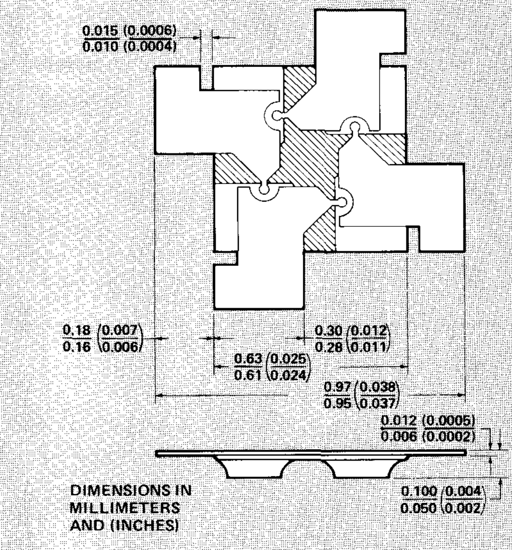
DC Power Dissipation at 25° C .... 75 mW/Junction

Derate linearly to zero at $T_{j(op)}$ max.
(Measured in infinite heat sink)

Operation of these devices within the above temperature ratings will assure a device Mean Time Between Failure (MTBF) of approximately 1 x 10⁷ hours.



Outline 08



Outline 03

Selection Guide

Frequency Package Outline	Barrier	To 2 GHz	2-4 GHz	4-8 GHz	8-12 GHz	12-18 GHz
Beam Lead	Medium	5082-9696	5082-9696	5082-9394	5082-9396	5082-9398
	Low	5082-9697	5082-9697	5082-9395	5082-9397	5082-9399

Electrical Characteristics at T_A=25°C

Part Number 5082-	Outline	Maximum Capacitance C_T (pF)	Maximum Capacitance Difference ΔC_T (pF)
9697	08	0.55	0.10
9395	08	0.35	0.10
9397	03	0.20	0.05
9399	03	0.15	0.05
9696	08	0.55	0.10
9394	08	0.35	0.10
9396	03	0.20	0.05
9398	03	0.15	0.05
Test Conditions		$V_R = 0$ f = 1 MHz[1]	

Typical Parameters

Forward Voltage V_F(V)[2]	Dynamic Resistance R_S (Ω)
0.25	11
0.25	13
0.30	13
0.30	15
0.35	11
0.35	13
0.45	13
0.45	15
I_F = 1 mA Measured Between Adjacent Leads.	I_F = 5 mA Measured Between Adjacent Leads

Notes:

1. Measured between diagonal leads.
2. Maximum ΔV_F = 20mV at I_F = 5 mA measured between adjacent leads.

Handling Instructions

The mechanical and electrical performance characteristics of beam lead diodes require careful and considerate handling during inspection, testing, and assembly. The handling techniques described here are necessary so that the diodes will not be mechanically or electrically damaged. The diodes are very small and magnification may be necessary to see them inside the shipping container.

Hewlett-Packard beam lead diodes are shipped in a flat, plastic container. The inside bottom surface of the container is coated with a thin layer of silicone to which the diodes adhere. They are covered with anti-static silk. A vacuum pickup with a #27 tip is recommended for picking up single beam lead devices. This should be done under 20x magnification for accurate positioning of the tip on the die.

A beam lead diode can be destroyed electrically by a static discharge through the diode. Hence, they must be handled so static discharges cannot occur.

If a vacuum pickup is not used, it is recommended that a wooden toothpick or sharpened Q-tip dipped in alcohol be used as a handling probe. A diode will adhere to the end of the wooden probe without danger of mechanically or electrically damaging the diode. It can then be placed where needed.

If tweezers are used, they must be electrically grounded to the surface upon which the device is being placed. The tweezer part should be dulled and used as a probe to lift the diodes and should not be used to grasp the diode. If used as tweezers to hold the diode, the gold tabs can be deformed.

Bonding Recommendations

Beam lead devices are silicon chips with coplanar plated gold tabs that extend parallel to the top surface of the chip approximately 8 mils beyond the edge. The leads are approximately 4 mils wide by 1/2 mil thick and are mounted by thermocompression bonding to the substrate metallization. The bonding is accomplished by placing the device face down with the tabs resting flat on the pad area and using heated wedge (and/or substrate)* or parallel-gap (spot-welding) techniques.

The heated wedge may be continuously heated, as in most standard equipment, or it may be pulse resistance heated where a high current, short duration pulse is used to raise the wedge to the required temperature. In the spot-welding operation, current is passed through the substrate metallization and the device lead. Most of the heat is generated at the interface between the two, where the bond is formed.

The major advantage of pulse heating techniques is that a cold ambient may be used, generating only localized heating in the vicinity of the bond itself. The electrodes (or wedge) can be placed on the device lead while the bond area is cold, and maintain a constant force through the heating and cooling cycle.

*Typical conditions for thermal compression bonding are:
Stage Temperature: 130°C-190°C
Wedge Temperature: 300°C
Pressure: 125 Grams
Time: 3 seconds maximum

HEWLETT hp PACKARD
COMPONENTS

BEAM LEAD PIN DIODE

5082-3900

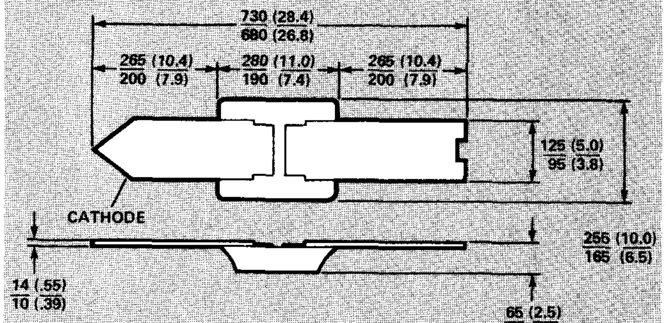
Features

HIGH BREAKDOWN VOLTAGE
200 V

LOW CAPACITANCE
0.02 pF

RUGGED CONSTRUCTION
2 Grams Minimum Lead Pull

NITRIDE PASSIVATED



DIMENSIONS IN µm (1/1000 inch)

Outline 06

Description/Applications

The HP 5082-3900 Beam Lead PIN diodes are constructed to offer exceptional lead strength while achieving excellent electrical performance at microwave frequencies.

The HP 5082-3900 Beam Lead PIN diode is designed for use in stripline or microstrip circuits using welding or thermocompression bonding techniques. PIN applications include switching, attenuating, phase shifting, limiting and modulating at microwave frequencies.

Maximum Ratings at $T_{CASE} = 25°C$

Junction Operating Temperature .... -65° C to +150° C
Storage Temperature .... -65° C to +150° C

Operation of these devices within the above temperature ratings will assure a device Mean Time Between Failure (MTBF) of approximately 1 x 10^7 hours.

Diode Mounting Temperature ... 220° C for 10 sec. max.
Power Dissipation .... 250 mW
(Derate linearly to zero at 150° C)
Minimum Lead Strength ... 2 Grams Pull on Either Lead

Electrical Specifications at $T_A = 25°C$

Parameter	Symbol	Min.	Typ.	Max.	Units	Conditions
Breakdown Voltage[1]	V_{BR}	150	200	–	V	$I_r = 10\mu A$
Series Resistance[1]	Rs	–	6	8	ohm	I_f= 50mA, f= 100MHz
Capacitance	C_o	–	.02	.025	pF	V = 0V, f = 3GHz
Minority Carrier Lifetime	τ	–	150	–	ns	I_f= 50mA, I_r = 250mA

Note 1: Higher V_{BR} or Lower Rs units available for special requirements.

Typical Parameters

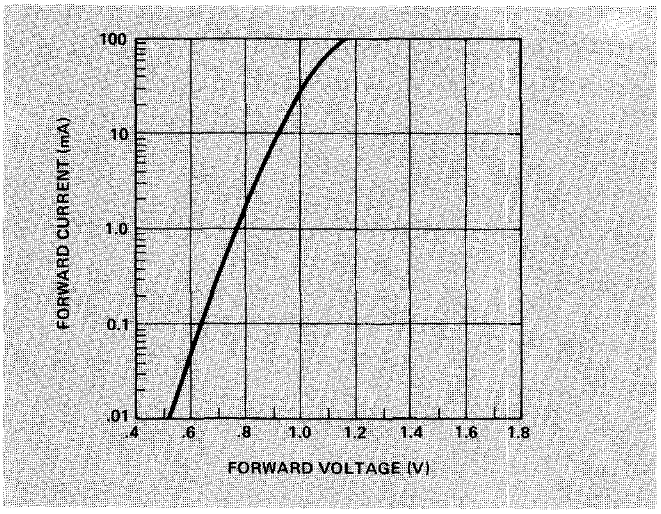


Figure 1. Typical Forward Conduction Characteristics.

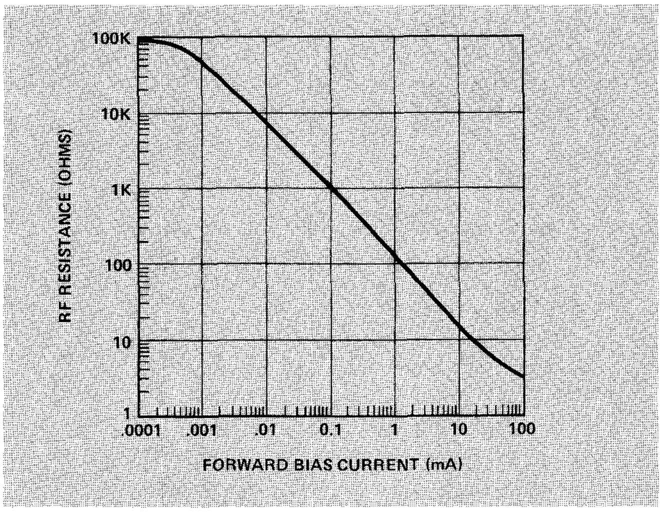


Figure 2. Typical RF Resistance vs. DC Bias Current.

HEWLETT PACKARD

COMPONENTS

NEW

LOW LOSS BEAM LEAD PIN DIODES

HPND-4001
HPND-4050

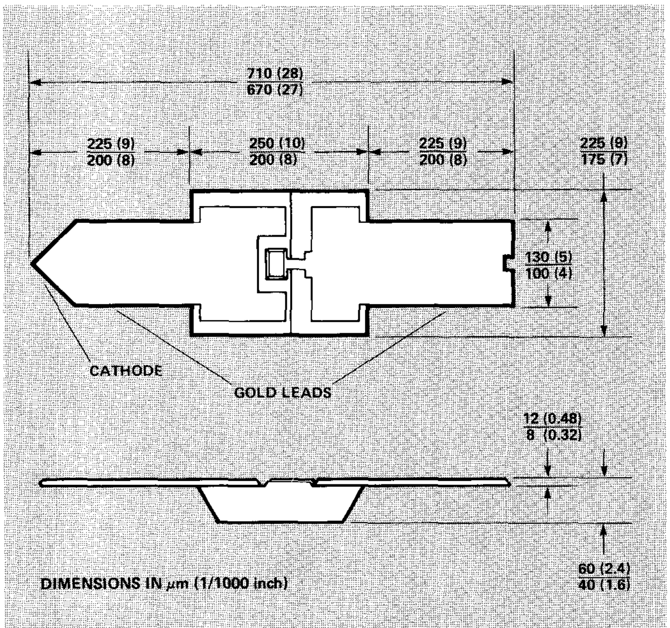
Features

LOW SERIES RESISTANCE
1.3Ω Typical

LOW CAPACITANCE
0.07 pF Typical

FAST SWITCHING
2 ns Typical

RUGGED CONSTRUCTION
4 Grams Minimum Lead Pull



Outline 07

Description/Applications

The HPND-4001 and -4050 are beam lead PIN diodes designed specifically for low capacitance, low series resistance and rugged construction. The new HP mesa process allows the fabrication of beam lead PINs with a very low RC product. A nitride passivation layer provides immunity from contaminants which would otherwise lead to I_R drift. A deposited glass layer (glassivated) provides scratch protection.

The HPND-4001 and -4050 beam lead PIN diodes are designed for use in stripline or microstrip circuits. Applications include switching, attenuating, phase shifting and modulating at microwave frequencies. The low capacitance and low series resistance at low current make these devices ideal for applications in the shunt configuration.

Bonding Techniques

Thermocompression bonding is recommended. The stage should be heated to 220°C and the bonding tool to 300°C maximum. Bonding time should not exceed 10 seconds. Either welding or ultrasonic bonding could also be used. For additional information, see Application Note 971, "The HPND-4050 Beam Lead Mesa PIN in Shunt Applications."

Electrical Specifications at T_A=25°C

Part Number	Breakdown Voltage V_{BR} (V)		Series Resistance R_S (Ω)		Capacitance C_T (pF)		Minority Carrier Lifetime τ (ns)	Reverse Recovery Time t_{rr} (ns)
	Min.	Typ.	Typ.	Max.	Typ.	Max.	Typ.	Typ.
HPND-4001	50	80	1.8	2.2	0.07*	0.08*	30	3
HPND-4050	30	40	1.3	1.7	0.12	0.15	15	2
Test Conditions	$V_R = V_{BR}$ Measure $I_R \leq 10\ \mu A$		$I_F = 10$ mA f = 100 MHz		$V_R = 20V$ $^*V_R = 30V$ f = 1 MHz		$I_F = 10$ mA $I_R = 6$ mA	$I_F = 10$ mA $V_R = 10V$

Maximum Ratings at $T_{CASE} = 25°C$

Operating Temperature	-65°C to +175°C
Storage Temperature	-65°C to +200°C

Operation of these devices within the above temperature ratings will assure a device Mean Time Between Failure (MTBF) of approximately 1 x 10^7 hours.

Power Dissipation	250 mW (Derate linearly to zero at 175°C)
Minimum Lead Strength	4 grams pull on either lead

Typical Parameters

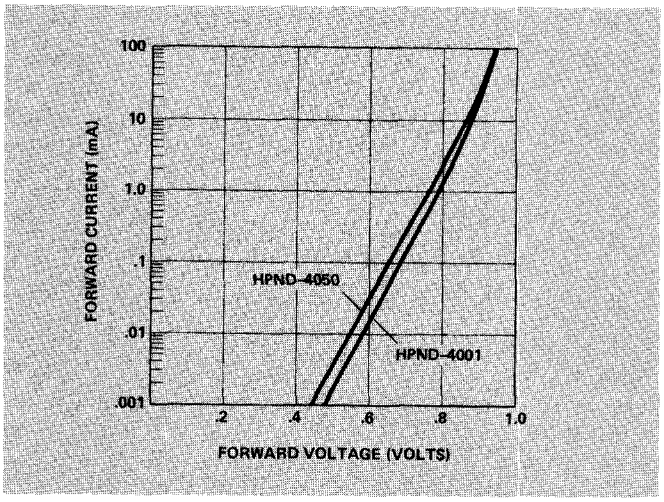


Figure 1. Typical Forward Characteristics.

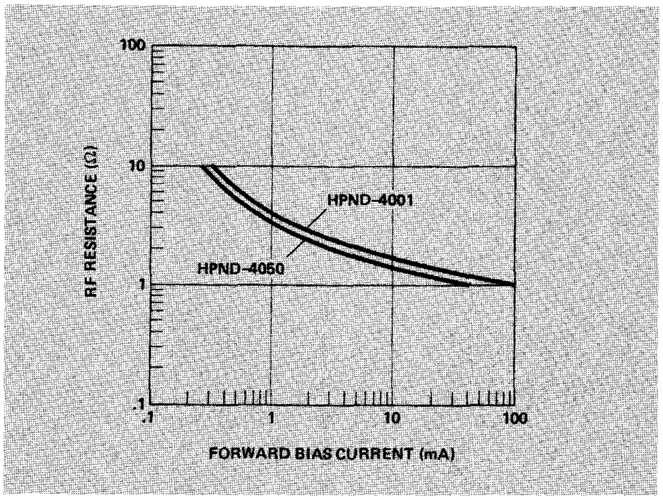


Figure 2. Typical RF Resistance vs. Forward Bias Current.

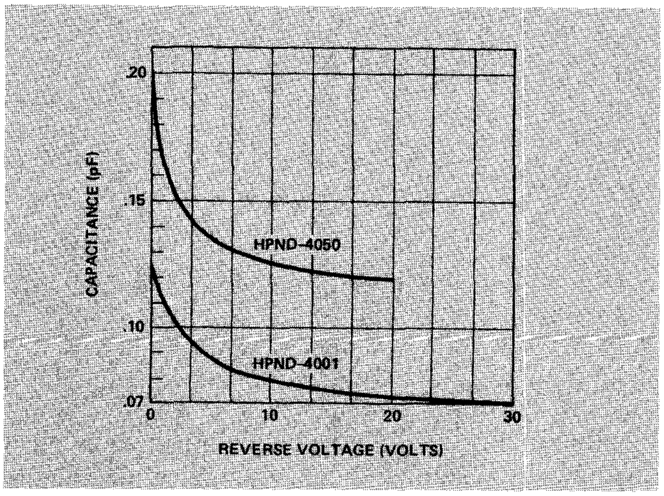


Figure 3. Typical Capacitance vs. Reverse Voltage.

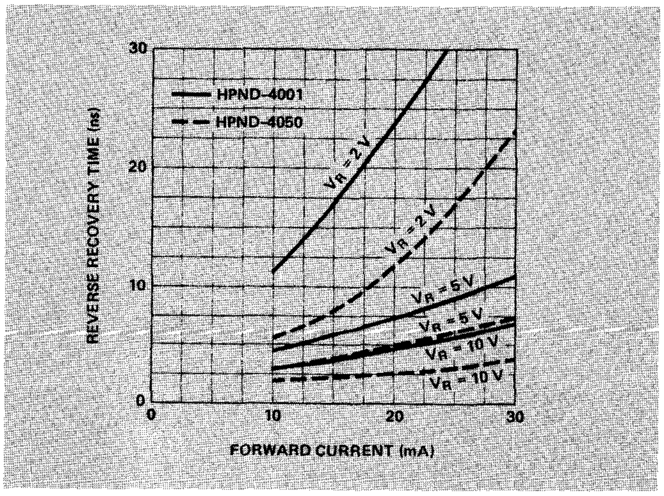
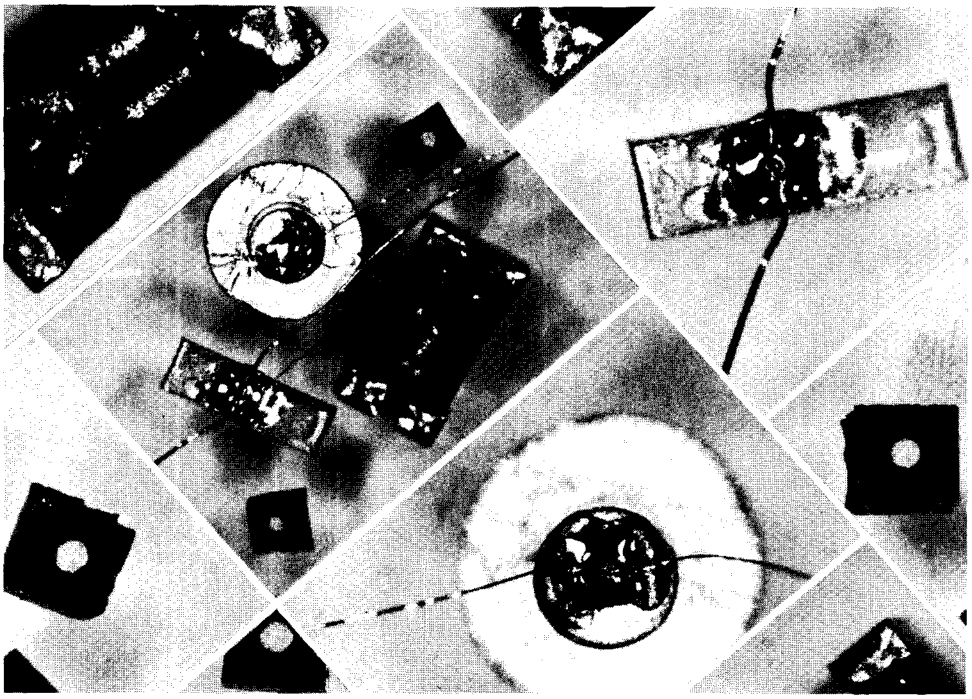


Figure 4. Typical Reverse Recovery Time vs. Forward Current (Shunt Configuration)

Diode Chips, Ministrips, and LIDs



Schottky Barrier Diodes

SCHOTTKY BARRIER DIODES FOR GENERAL PURPOSE APPLICATIONS

ELECTRICAL SPECIFICATIONS AT $T_A = 25°C$

Part Number 5082-				Nearest Equivalent Packaged Part No. 5082-	Nearest Equivalent Beam Lead Part No. 5082-	Minimum Breakdown Voltage, V_{BR} (V)	Minimum Forward Current I_F (mA)	Maximum Junction Capacitance C_{jo} (pF)
Chip For Epoxy Or Solder Die Attach	Chip For Eutectic Die Attach	LID (Outline 50)	Ministrip (Outline 72)					
0024	0094	2802	2801	2800	2837	70	15	1.7
0087	0057			2810		20	35	1.0
0097	0058	2844	2845	2811		15	20	1.1
0031				2835		5	10*	0.8
300°C 1 Min.	400°C 1 Min.	250°C 5 Sec.	250°C 5 Sec.	Soldering Conditions	—	—	—	—
Notes: [2,9,10]	[2,9]	[6,7] C_P = .18 pF	[4] C_P = .13 pF			$I_R = 10\ \mu A$	$V_F = 1V$ $^*V_F = 0.45V$	$V_R = 0V$ f = 1 MHz

Note: Total Capacitance: $C_{TO} = C_{jo} + C_P$.

SCHOTTKY BARRIER DIODES FOR MIXING AND DETECTING

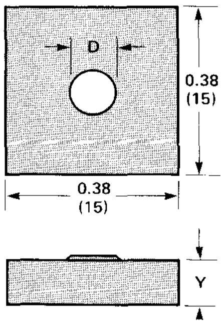
ELECTRICAL SPECIFICATIONS AT $T_A = 25°C$

TYPICAL PARAMETERS

Part Number 5082-			Nearest Equivalent Packaged Part No. 5082-	Nearest Equivalent Beam Lead Part No. 5082-	Maximum Junction Capacitance C_{jo} (pF)	Typical Noise Figure NF (dB)[B]	Typical Tangential Sensitivity TSS (dBm)
Chip	LID (Outline 50)	Ministrip (Outline 71)					
0023	2705	2710	2713	2709	0.18	6.0	-54
0029	—	—	2721	2716	0.14	7.0*	-54
0013[A,C]	—	—	HSCH-3206[C] -2285[A]	2299[A,C]	—	—	-42[C] -54[A]
HSCH-5017[C]	—	—	HSCH-5019[C]	—	0.45	—	-54
0009	2754	2753	2750	—	0.14	7.0	-55
250°C, 1 Min. or 300°C, 15 Sec.	250°C 5 Sec.	250°C 5 Sec.	Soldering Conditions	—	—	—	—
Notes [1,2]	[1,7,8] C_P = .18 pF	[1,4] C_P = .13 pF	—	—	$V_R = 0V$ f = 1 MHz	f = 9.375 GHz *f = 16 GHz	$I_{BIAS} = 20\ \mu A$ f = 10 GHz BW = 2 MHz

Notes: A. Low V_F Schottky Barrier Diodes. B. NF includes 1.5 dB for the IF Amplifier. C. Zero bias.

Outline Drawings



ALL DIMENSIONS IN mm AND (1/1000 inch)

For LID and Ministrip drawings see page 191. The 5082 prefix does not apply to part numbers containing HSCH.

Dimension	HP Part Number 5082-				
	0024 0094	0057, 0058, 0087, 0097	0031	0013, 0023,* 0029	HSCH-5017 0009*
D	0.10 (4)	0.08 (3)	0.06 (2.5)	0.02 (0.80)	
Y	0.13 (5)			0.10 (4)	
Top Contact	Au, Anode	Au, Anode	Au, Anode	Au, Anode	Au, Cathode
Bottom Contact	Au, Cathode	Au, Cathode	Au, Cathode	Au, Cathode	Au, Anode
Oper. & Stg. Temp. Range	-65°C to +200°C		-65°C to +150°C		

DIMENSIONS IN MILLIMETERS (1/1000 inch)

*9 contact versions are available as 5082-0041 (5082-0023) and 5082-9891 (5082-0009).

PIN Diodes

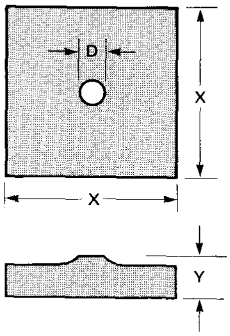
ELECTRICAL SPECIFICATIONS AT $T_A = 25°C$ **TYPICAL PARAMETERS**

Part Number 5082-									
Chip	LID (Outline 50)	Ministrip (Outline 72)	Post (Outline 74)	Nearest Equivalent Packaged Part No. 5082-	Minimum Breakdown Voltage, V_{BR}(V)	Typical Junction Capacitance C_{jVR}(pF)	Typical Series Resistance $R_S(\Omega)$	Typical Lifetime τ(ns)	Typical Reverse Recovery Time, t_{rr} (ns)
0012	3005	3000	3259	3001	150	0.07	0.8	400	100
0030	—	3309	—	3301	150	0.07	0.8	400	100
0047	—	—	—	3001	150	0.09	0.6	400	100
9882	—	—	—	3301	150	0.09	0.6	400	100
0025	3085	3086	—	3080	100	0.10	1.5	1300	1000
0039	—	—	—	3081	100	0.10	2.0	2000	1000
0001*	3045	3010	3258	3041	70	0.12*	0.8*	15	5
0049	—	—	—	3046	400	0.12	0.6	800	200
0034	—	—	—	3168	35	0.80*	0.4**	40	12
425°C 1 Min. *300°C 1 Min.	250°C 5 Sec.	325°C 5 Sec.	250°C 5 Sec.	Soldering Conditions					
[3,*2]	[6,7] C_P = .18 pF	[4] C_P = .13 pF	[8] C_P = .13 pF		$I_R = 10\ \mu A$	$V_R = 50V$ $^*V_R = 20V$ f = 1 MHz	$I_F = 100$ mA $^*I_F = 20$ mA $^{**}I_F = 10$ mA f = 100 MHz	$I_F = 50$ mA $I_R = 250$ mA	$I_F = 20$ mA $V_R = 10V$

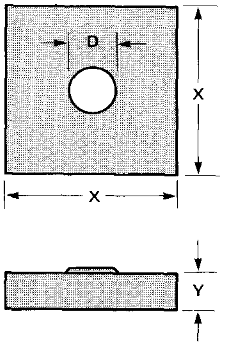
Note: Total capacitance $C_{TO} = C_{jVR} + C_p$.

Outline Drawings

5082-0001



ALL OTHER CHIPS



Dimension	HP Part Number 5082-						
	0012 0047	0030 9882	0034	0025	0039	0049	0001
D	0.10 (4)			0.23 (9)	0.24 (9.5)		0.06 (2.5)
X	0.38 (15)			0.51 (20)			0.38 (15)
Y	0.09 (3.5)		0.13 (5)	0.15 (6)	0.23 (9)	0.08 (3.2)	0.11 (4.5)
Top Contact	Au, Cathode	Au, Anode	Au, Anode	Ag, Cathode			Ag, Anode
Bottom Contact	Au, Anode	Au, Cathode		Au, Anode			Au, Cathode

DIMENSIONS IN MILLIMETERS (1/1000 inch)

Operating and Storage Temperature Range -60°C to +150°C

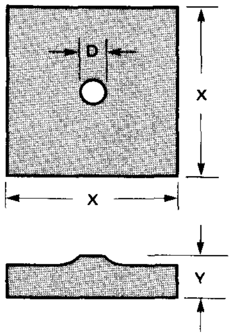
For LID and Ministrip drawings see page 191.

Step Recovery Diodes

ELECTRICAL SPECIFICATIONS AT $T_A = 25°C$ **TYPICAL PARAMETERS**

Part Number 5082-								
Chip	LID (Outline 50)	Ministrip (Outline 72)	Minimum Breakdown Voltage, V_{BR}(V)	Chip Capacitance C_{jVR}(pF)	Lifetime τ(ns)	Transition Time t_t(ps)	Charge Level (pc)	Nearest Equivalent Packaged Part No. 5082-
0020	0316	0305	25	0.4-1.0	20	75	300	0830
0008	0318	0340	15	0.15-0.5	10	50	100	0835
0032	0313	0307	65	4.0	150	250	1500	0241
0090	—	—	45	1.0	50	100	300	0820
0021	0317	0308	40	2.0	75	150	1000	0310
0015	0312	0306	35	1.2	50	150	1000	0132
0017	0314	0364	75	4.0	200	450	2400	0300
0018	0105	0309	25	0.5	20	70	200	0253
300°C 1 Min.	250°C 5 Sec.	250°C 5 Sec.	—	—	—	—	—	Soldering Conditions
[3]	[6,7] $C_P = .18$ pF	[4] $C_P = .13$ pF	$I_R = 10\ \mu A$	$V_R = 10V$ $f = 1$ MHz	—	—	—	Notes

Outline Drawings



DIMENSIONS IN MILLIMETERS (1/1000 inch)

	5082-							
Dimension	0200	0008	0015	0017	0018	0021	0032	0090
D	0.10 (4)	0.06 (2.5)	0.15 (6)	0.39 (15.5)	0.05 (2)	0.22 (8.5)	0.32 (12.5)	0.15 (6)
X	0.38 (15)	0.38 (15)	0.38 (15)	0.64 (25)	0.38 (15)	0.51 (20)	0.51 (20)	0.38 (15)
Y	0.11 (4.5)	0.11 (4.5)	0.11 (4.5)	0.11 (4.5)	0.11 (4.5)	0.11 (4.5)	0.11 (4.5)	0.11 (4.5)

Top Contact: Ag, Anode

Bottom Contact: Au, Cathode

Operating and Storage Temperature Range
-60°C to +200°C

LID and Ministrip see page 191.

Notes:

1. Handle with grounded tweezers and grounded bonding equipment. These diodes are pulse sensitive and may be damaged by electrostatic charges.
2. Use standard thermocompression bonding techniques. Ultrasonic bonding is not recommended.
3. Either ultrasonic or thermocompression bonding techniques can be employed.
4. Ministrip Handling and Mounting Techniques. The Ministrips may be mounted by using conductive epoxy such as Hysol K20 or Dupont 5504. Conventional soldering techniques may also be used.

   Direct heating or resistive heating of the substrate using a parallel gap welder are acceptable methods. High temperature solder preforms such as gold-tin (280° Eutectic) may be used for the Step Recovery and PIN diodes. Low temperature solder preforms such as tin-lead should be used with the Schottky barrier diodes. The composition of the solder preform should be compatible with the techniques and materials used in the *substrate and conductive land patterns.*

   The leads may be attached by using ultrasonic or thermocompression bonding methods. A parallel gap welder may also be used (Figure 1). Conventional soldering techniques are not recommended for the gold leads.
5. Reverse Polarity. Anode is the bottom contact and the Cathode is the top contact.

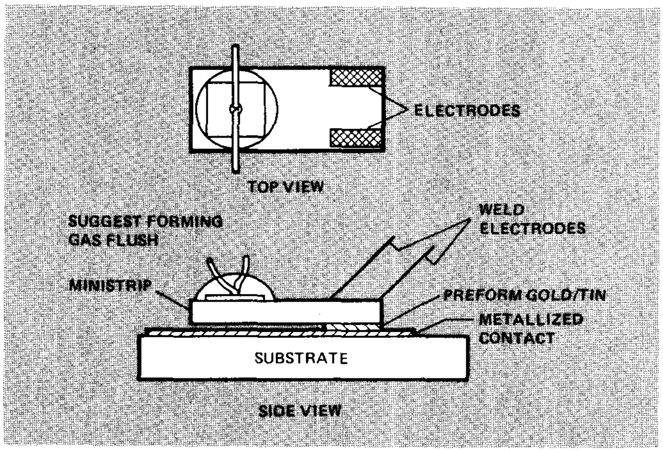
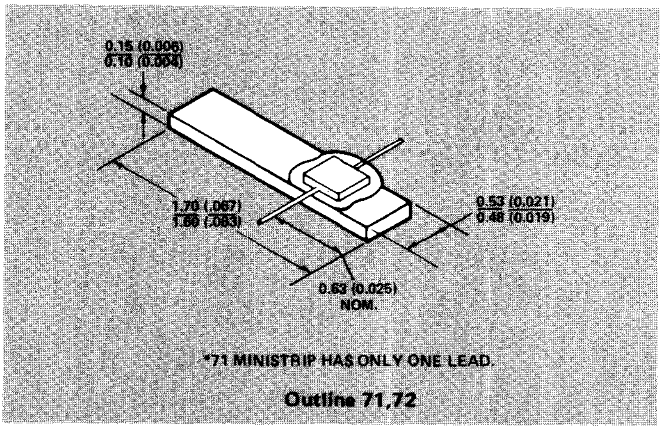


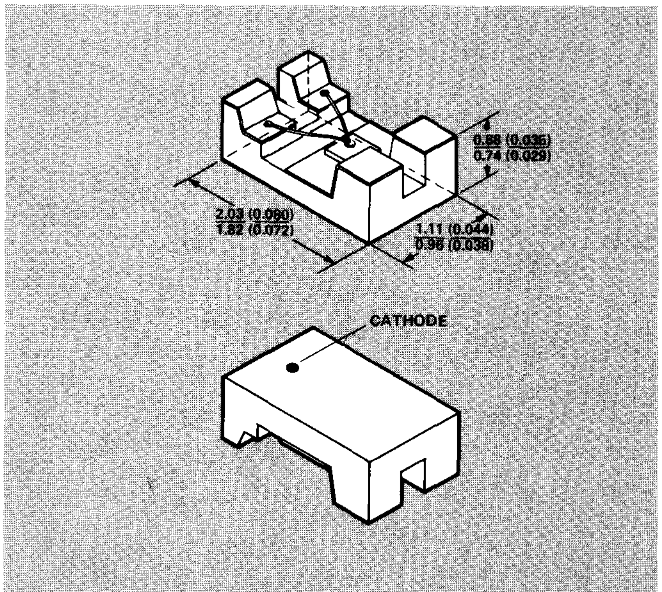
Figure 1. Resistance Heating the Ministrip



*71 MINISTRIP HAS ONLY ONE LEAD.

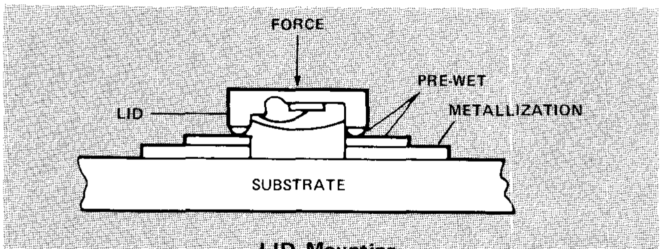
Outline 71,72

ALL DIMENSIONS IN MILLIMETERS AND (INCHES).

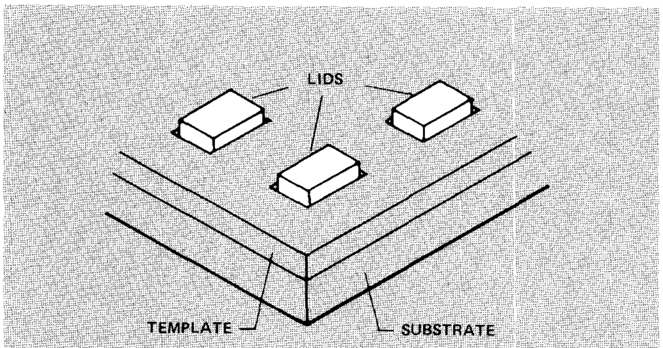


Outline 50 (LID Package)

6. Polarity Designation on LID's. See Outline 50 (LID Package).
7. Leadless Inverted Device (LID). Mounting recommendations: the LID may be mounted by individually soldering each device or batch flow soldered as illustrated below:



LID Mounting



Batch Reflow Soldering of LIDs

Prior to soldering it is advisable to tin each device. Scrub the pads of the LID with a Pink Pearl eraser to remove any dirt or other foreign matter. Then rinse the LID in TCE (Trinchloroethylene).

Dip the LID in Alpha 711 Flux using titanium tweezers. With those tweezers. With those tweezers, place the unit in a solder bath of 62% Sn, 36% Pb, and 2% Ag, for 30 seconds and remove. Note, the solder bath must be maintained at a temperature of 220° C plus or minus 5° C through the process.

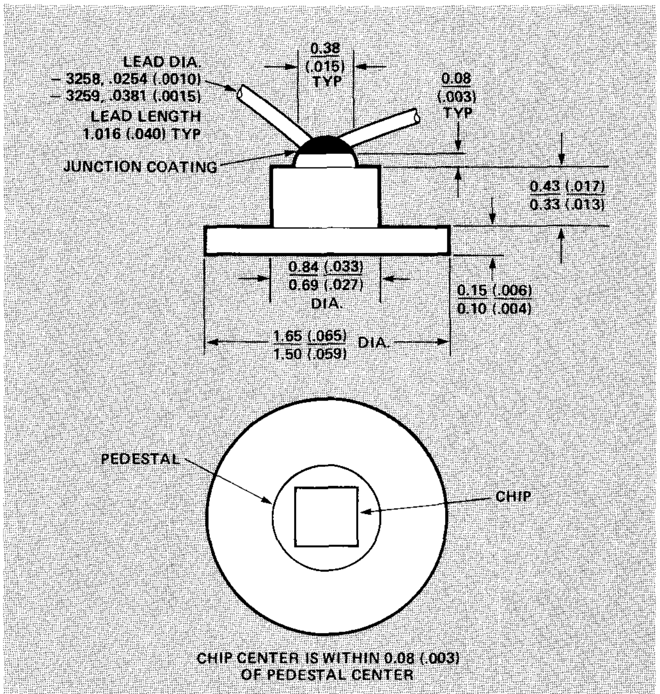
Dip the LID in the solder bath again for 3 seconds. When removing the LID, hold it 1/8 inch above the solder pot for 5 seconds to obtain thermal equilibrium. Wait 10 seconds before rinsing in TCE. Brush off the TCE with an artist's brush.

Now inspect each LID under a microscope to see if the tin covers over 90% of the contact pad area and if this area appears to have a shiny, bright, continuous homogeneous solder casting. If the LID appearance fails to meet the inspection criteria, repeat the tinning process, starting with the flux dip.

8. The HP package outline 74 consists of a gold plated copper pedestal. The top contact wire exhibits an inductance (Lp) of approximately .5 nH for a typical connecting wire length of approximately 20 mils.

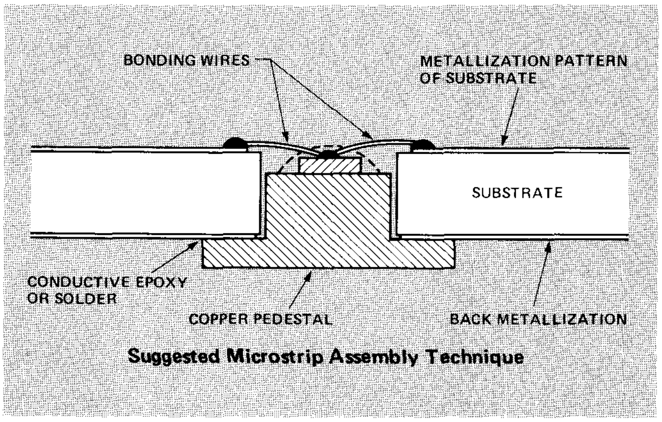
   The polarity of the 5082-3258 is cathode on heat sink. The polarity of the 5082-3259 is anode on heat sink.

   After attachment of a gold wire, the chip is covered with a thin layer of silicone junction coating for protection against mechanical damage. The connecting wires are bent upwards for transportation and easy circuit insertion.



ALL DIMENSIONS IN MILLIMETERS AND (INCHES).

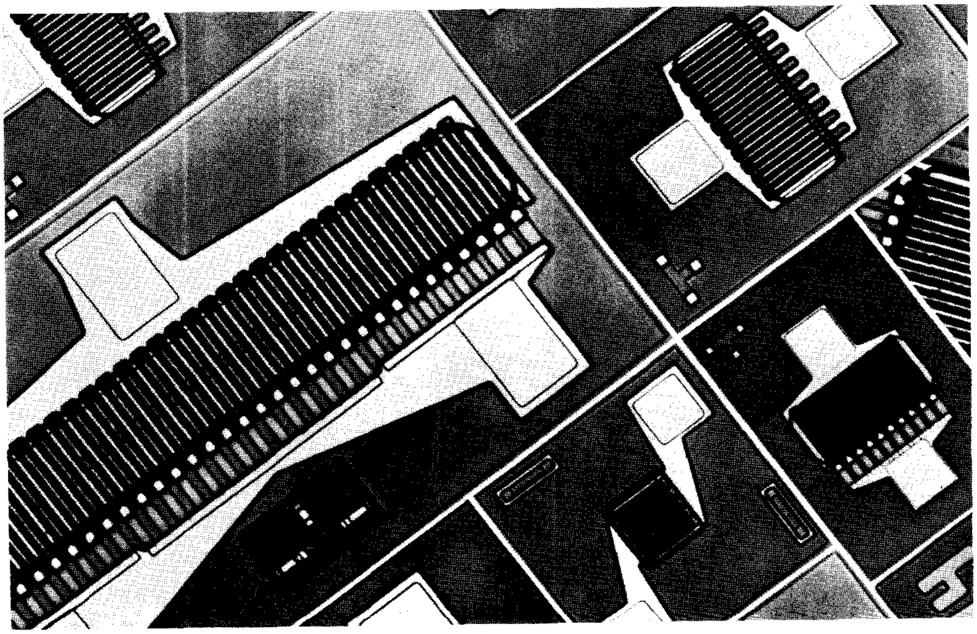
Outline 74 (Post)



Suggested Microstrip Assembly Technique

9. Thermal compression bonding is recommended for attaching wires or mesh to Schottky barrier diode chips. The carrier should be placed on a stage heated to 220° C-240° C. Heat and pressure may be applied to the wire by the edge of a capillary such as Tempress 5102-20 heated to 280° C-300° C. A force of 25-30 grams should be applied for 5 seconds.
10. Eutectic bonding or die attaching may damage the chip. A preform must be used.

Silicon Bipolar Transistor Chips



Silicon Bipolar Transistor Chip Selection Guide

The line of four silicon bipolar transistor chips covers the majority of bipolar amplifier applications. The following table lists the transistor part numbers with their performance features.

Features	Typical Performance at 4 GHz	Part Number HXTR-	Page Number
Low Noise Figure High Associated Gain	2.7 dB 9.0 dB	6001	201
High Maximum Available Gain High Output Power (P_{1dB}) Low Noise Figure	11.5 dB 18.5 dBm 3.8 dB	2001	195
High Output Power (P_{1dB}) High Gain (at P_{1dB})	22 dBm 8.0 dB	5001	197
High Output Power (P_{1dB}) High Gain (at P_{1dB})	27.5 dBm 7.5 dB	5002	199

These transistors are available in a variety of package styles, as indicated in the following table.

Chip Part Number HXTR-	Packaged Part Number HXTR-	Package Style HPAC-
2001	2101 (2N6679)	100
	2102	70 GT
	6105	100
	6106	70 GT
5001	5101 (2N6701)	100
	5103	200
5002	5102	200 GB/GT
	5104	200
6001	6101 (2N6617)	70 GT
	6102	70 GT
	6103 (2N6618)	100
	6104	100

HEWLETT hp PACKARD
COMPONENTS

GENERAL PURPOSE TRANSISTOR CHIP

HXTR-2001

NEW

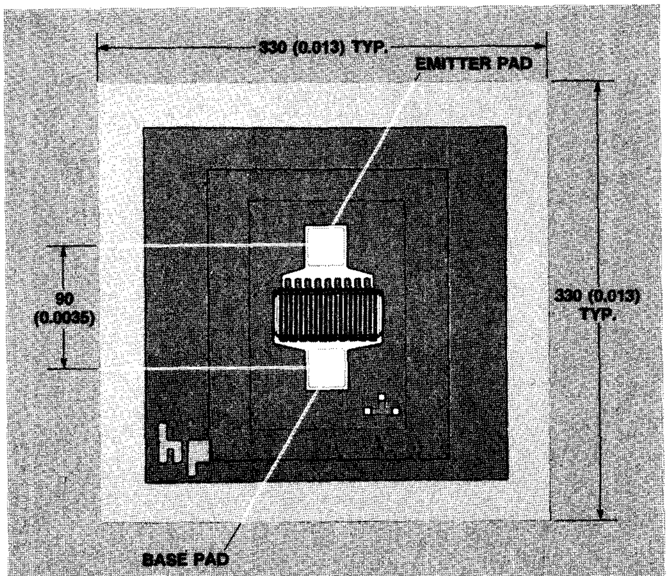
Features

HIGH GAIN
17.5 dB Typical at 2 GHz

HIGH OUTPUT POWER
20.0 dBm P_{1dB} Typical at 2 GHz

LOW NOISE FIGURE
3.8 dB Typical at 4 GHz

WIDE DYNAMIC RANGE



Chip Outline
Dimensions in Micrometers (inches)

Gold Bonding Pad Dimensions:	25 (0.001) x 25 (0.001) Typical
Chip Thickness:	89 (0.0035) Typical
Collector Back Contact:	Silicon-Gold Eutectic

Description/Applications

The HXTR-2001 is an NPN bipolar transistor chip intended for use in hybrid applications requiring superior UHF and microwave performance. Use of ion implantation and self-alignment techniques in its manufacture produce uniform devices requiring little or no individual circuit adjustment. The HXTR-2001 features a Ti/Pt/Au metallization system and a dielectric scratch protection over its active area to insure reliable operation.

Electrical Specifications at $T_A = 25°C$

Symbol	Parameters and Test Conditions		MIL-STD-750 Test Method	Units	Min.	Typ.	Max.
BV_{CES}	Collector-Emitter Breakdown Voltage at $I_C=100\mu A$		3011.1*	V	30		
I_{CEO}	Collector-Emitter Leakage Current at $V_{CE}=15V$		3041.1**	nA			500
I_{CBO}	Collector Cutoff Current at $V_{CB}=15V$		3036.1**	nA			100
h_{FE}	Forward Current Transfer Ratio at $V_{CE}=15V$, $I_C=15mA$		3076.1*	—	50	120	220
$G_{a(max)}$	Maximum Available Gain	f=2GHz 4GHz		dB		17.5 11.5	
P_{1dB}	Power Output at 1dB Gain Compression Conditions for above: $V_{CE} = 15V$, $I_C = 25$ mA, $\theta_{JA} = 210°C/W$	f=2GHz 4GHz		dBm		20.0 18.5	
F_{MIN}	Minimum Noise Figure Conditions for above: $V_{CE} = 15V$, $I_C = 15$ mA, $\theta_{JA} = 210°C/W$	f=1.5GHz 4GHz	3246.1	dB		2.2 3.8	

*300μs wide pulse measurement <2% duty cycle.
**Measured under low ambient light conditions.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage	25V
V_{CEO}	Collector to Emitter Voltage	16V
V_{EBO}	Emitter to Base Voltage	1.0V
I_C	DC Collector Current	35 mA
P_T	Total Device Dissipation[2]	450 mW
T_J	Junction Temperature	200° C
T_{STG}	Storage Temperature	-65° C to +200° C

Notes:

1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device mean time between failure (MTBF) to below the design goal of 1 x 10^7 hours at T_J = 175°C (assumed Activation Energy = 1.5 eV).
2. Power dissipation derating should include a Θ_{JB} (Junction-to-Back contact thermal resistance) of 125°C/W.

   Total Θ_{JA} (Junction-to-Ambient) will be dependent upon the heat sinking provided in the individual application.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	30V
V_{CEO}	Collector to Emitter Voltage	20V
V_{EBO}	Emitter to Base Voltage	1.5V
I_C	DC Collector Current	70 mA
P_T	Total Device Dissipation	900 mW
T_J	Junction Temperature	300° C
$T_{STG(MAX)}$	Maximum Storage Temperature	300° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

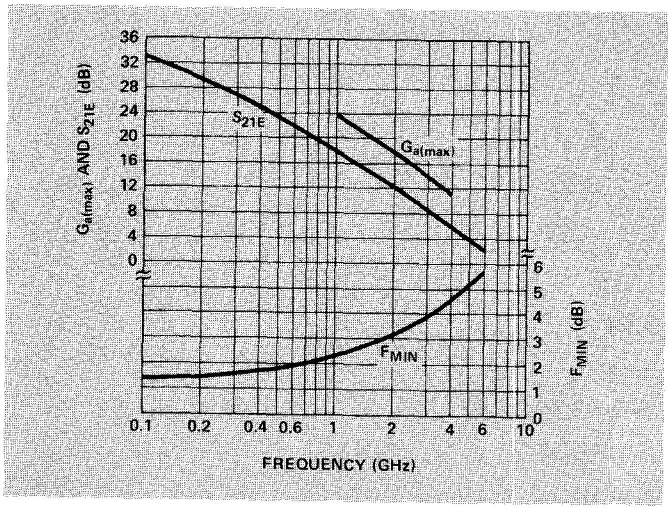


Figure 1. Typical $G_{a(max)}$, S_{21E}, and Noise Figure (F_{MIN}) vs. Frequency at V_{CE} = 15V, I_C = 25mA.

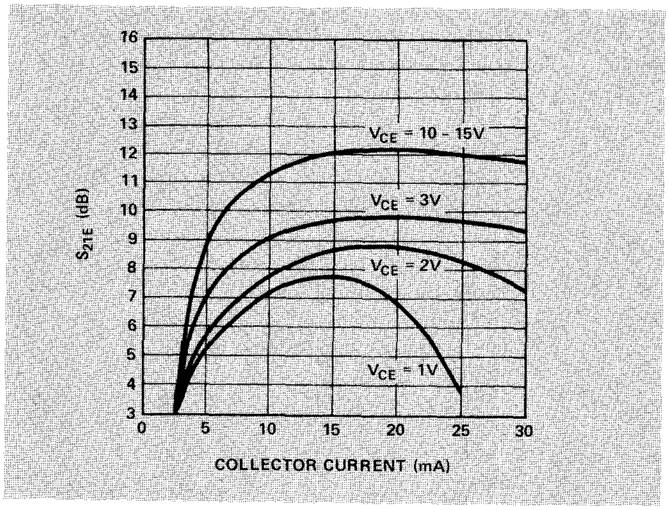


Figure 2. Typical S_{21E} vs. Current at 2GHz.

Typical S-Parameters* V_{CE} = 15V, I_C = 25mA

Freq. (MHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	0.57	-88	33.3	46.2	144	-42	0.008	58	0.85	-20
200	0.68	-124	30.2	32.5	123	-39	0.011	43	0.67	-26
300	0.72	-141	27.6	23.9	113	-38	0.013	37	0.56	-26
400	0.74	-150	25.4	18.7	106	-37	0.014	35	0.51	-24
500	0.75	-156	23.7	15.3	102	-37	0.014	35	0.48	-22
600	0.76	-160	22.2	12.9	99	-36	0.015	36	0.46	-21
700	0.76	-163	20.8	11.0	97	-36	0.015	37	0.45	-20
800	0.76	-165	19.9	9.8	95	-36	0.016	38	0.44	-19
900	0.76	-167	18.8	8.7	93	-36	0.016	40	0.44	-18
1000	0.76	-168	18.0	7.9	91	-35	0.017	42	0.44	-18
1500	0.77	-172	14.5	5.3	85	-34	0.021	49	0.43	-18
2000	0.77	-175	12.0	4.0	81	-32	0.025	54	0.43	-20
2500	0.77	-176	10.1	3.2	77	-31	0.029	58	0.43	-23
3000	0.77	-177	8.6	2.7	73	-29	0.034	60	0.43	-26
3500	0.77	-178	7.2	2.3	69	-28	0.038	61	0.44	-29
4000	0.76	-179	6.0	2.0	66	-27	0.043	62	0.44	-32
4500	0.76	-179	5.1	1.8	63	-26	0.048	62	0.45	-35
5000	0.76	-179	4.1	1.6	59	-26	0.052	62	0.45	-38
5500	0.76	-180	3.5	1.5	56	-25	0.057	62	0.46	-41
6000	0.76	-180	2.9	1.4	53	-24	0.062	61	0.47	-44

*Values do not include any parasitic bonding inductances and were generated by use of a computer model.

HEWLETT PACKARD
COMPONENTS

NEW

LINEAR POWER TRANSISTOR CHIP

HXTR-5001

Features

HIGH P_{1dB} LINEAR POWER
23 dBm Typical at 2 GHz
22 dBm Typical at 4 GHz

HIGH P_{1dB} GAIN
13.5 dB Typical at 2 GHz
8.0 dB Typical at 4 GHz

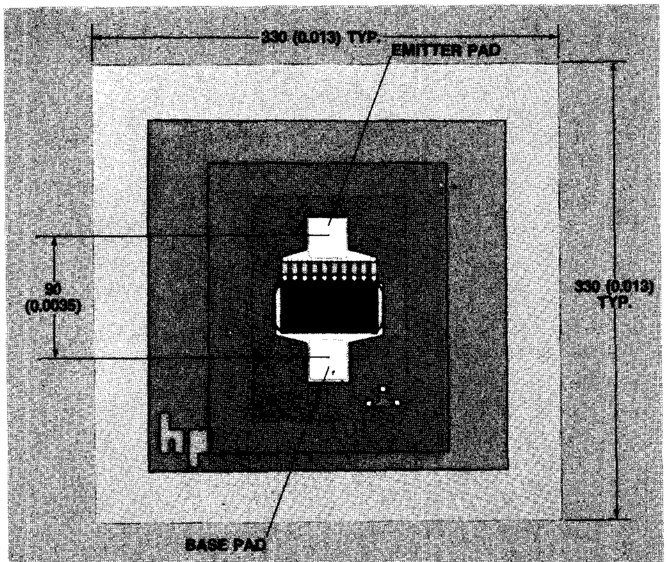
LOW DISTORTION

HIGH POWER-ADDED EFFICIENCY

Description/Applications

The HXTR-5001 is an NPN bipolar transistor chip designed for high output power and gain to 5 GHz. To achieve excellent uniformity and reliability, the manufacturing process utilizes ion implantation, self-alignment techniques and Ti/Pt/Au metallization. The chip has a dielectric scratch protection over its active area and Ta_2N ballast resistors for ruggedness.

The superior power, gain and distortion performance of the HXTR-5001 commend it for use in broad and narrow band commercial and military communications, radar, and ECM hybrid applications. Programs requiring hermetically packaged devices with similar performance should employ the HXTR-5101 and the HXTR-5103 which utilize this chip.



Chip Outline
Dimensions in Micrometers (Inches)

Gold Bonding Pad Dimensions:	25 (0.001) x 25 (0.001) Typical
Chip Thickness:	89 (0.0035) Typical
Collector Back Contact:	Silicon-Gold Eutectic

Electrical Specifications at T_A=25°C

Symbol	Parameters and Test Conditions		Test MIL-STD-750	Units	Min.	Typ.	Max.
BV_{CBO}	Collector-Base Breakdown Voltage at I_C = 3 mA		3001.1*	V	40		
BV_{CEO}	Collector-Emitter Breakdown Voltage at I_C = 15 mA		3011.1*	V	24		
BV_{EBO}	Emitter-Base Breakdown Voltage at I_B = 30 μA		3026.1*	V	3.3		
I_{EBO}	Emitter-Base Leakage Current at V_{EB} = 2 V		3061.1	μA			2
I_{CES}	Collector-Emitter Leakage Current at V_{CE} = 32 V		3041.1**	nA			200
I_{CBO}	Collector-Base Leakage Current at V_{CB} = 20 V		3036.1**	nA			100
h_{FE}	Forward Current Transfer Ratio at V_{CE} = 18 V, I_C = 30 mA		3076.1*		15	40	75
P_{1dB}	Power Output at 1 dB Gain Compression	f = 2 GHz 4 GHz		dBm		23 22	
G_{1dB}	Associated 1 dB Compressed Gain	f = 2 GHz 4 GHz		dB		13.5 8	
P_{SAT}	Saturated Power Output (8 dB Gain) (3 dB Gain)	f = 2 GHz 4 GHz		dBm		25.5 25	
η	Power-Added Efficiency at 1 dB Compression	f = 2 GHz 4 GHz		%		35 25	
IMD	Third Order Intermodulation Distortion (Reference to either tone), at P_O(PEP) = 22 dBm	f = 4 GHz		dB		-30	
	Tuned for Maximum Output Power at 1dB Compression V_{CE} = 18 V, I_C = 30 mA, θ_{JA} = 210°C/W						

*300 μs wide pulse measurement at ≤2% duty cycle.
**Measured under low ambient light conditions.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage	40V
V_{CEO}	Collector to Emitter Voltage	22V
V_{EBO}	Emitter to Base Voltage	3.3V
I_C	DC Collector Current	50 mA
P_T	Total Device Dissipation[2]	700 mW
T_J	Junction Temperature	200° C
T_{STG}	Storage Temperature	-65° C to +200° C

Notes:

1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device mean time between failure (MTBF) to below the design goal of 1 x 10^7 hours at T_J = 175° C assumed Activation Energy = 1.5 eV).
2. Power dissipation derating should include a Θ_{JB} (Junction-to-Back contact thermal resistance) of 150° C/W.

Total Θ_{JA} (Junction-to-Ambient) will be dependent upon the heat sinking provided in the individual application.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	45V
V_{CEO}	Collector to Emitter Voltage	27V
V_{EBO}	Emitter to Base Voltage	4.0V
I_C	DC Collector Current	100 mA
P_T	Total Device Dissipation	1.4W
T_J	Junction Temperature	300° C
$T_{STG(MAX)}$	Maximum Storage Temperature	300° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

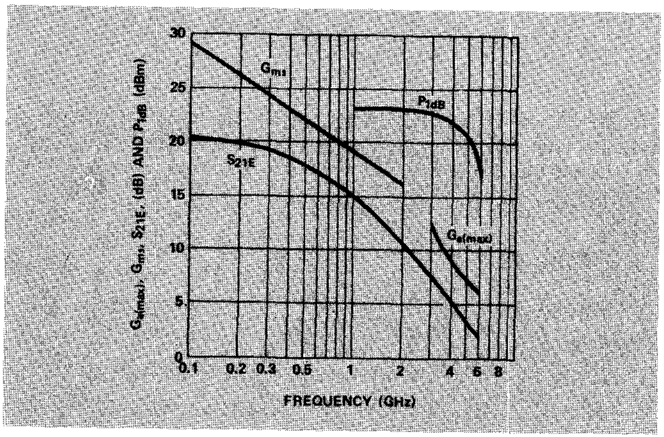


Figure 1. Typical G_a(max), Maximum Stable Gain (G_{ms}), S_{21E}, and P_{1dB} Linear Power vs. Frequency at V_{CE} = 18V, I_C = 30 mA.

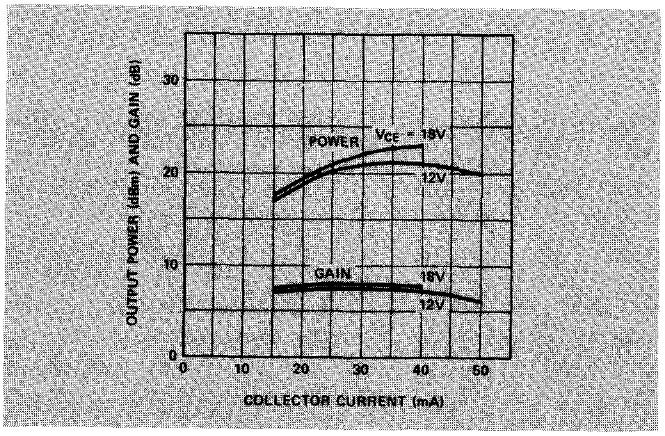


Figure 2. Typical P_{1dB} Linear Power and Associated 1 dB Compressed Gain vs. Current at V_{CE} = 12V and 18V at 4 GHz.

Typical S-Parameters* V_{CE} = 18V, I_C = 30 mA

Freq. (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	dB	Mag.	Ang.	dB	Mag.	Ang.	Mag.	Ang.
0.100	0.74	-15	20.2	10.2	171	-38	0.01	83	0.99	-5
0.200	0.73	-30	19.9	9.88	162	-33	0.02	75	0.97	-10
0.300	0.72	-44	19.5	9.42	154	-30	0.03	69	0.93	-15
0.400	0.71	-57	19.0	8.87	146	-28	0.04	63	0.89	-19
0.500	0.70	-68	18.4	8.28	140	-26	0.05	58	0.85	-22
0.600	0.69	-78	17.7	7.71	134	-25	0.06	54	0.80	-24
0.700	0.67	-87	17.1	7.16	129	-25	0.06	50	0.76	-26
0.800	0.67	-94	16.5	6.65	124	-24	0.06	47	0.73	-28
0.900	0.66	-101	15.8	6.19	120	-24	0.07	44	0.70	-29
1.000	0.65	-107	15.2	5.78	117	-23	0.07	42	0.67	-30
1.500	0.63	-128	12.6	4.25	103	-22	0.08	37	0.58	-32
2.000	0.62	-140	10.5	3.33	94	-22	0.08	35	0.53	-32
2.500	0.61	-148	8.7	2.73	87	-21	0.09	35	0.51	-33
3.000	0.61	-154	7.3	2.32	81	-21	0.09	35	0.50	-35
3.500	0.61	-158	6.1	2.02	76	-20	0.10	36	0.49	-36
4.000	0.60	-161	5.8	1.79	71	-20	0.10	37	0.49	-38
4.500	0.60	-164	4.1	1.61	66	-19	0.11	38	0.49	-40
5.000	0.60	-166	3.3	1.47	62	-19	0.11	39	0.49	-43
5.500	0.59	-168	2.6	1.35	58	-19	0.12	40	0.49	-45
6.000	0.59	-169	2.0	1.25	55	-18	0.12	40	0.49	-47

*Values do not include any parasitic bonding inductances and were generated by use of a computer model.

HEWLETT PACKARD
COMPONENTS

NEW

LINEAR POWER TRANSISTOR CHIP

HXTR-5002

Features

HIGH P_{1dB} LINEAR POWER
29 dBm Typical at 2GHz
27.5 dBm Typical at 4GHz

HIGH ASSOCIATED GAIN
12.5 dB Typical at 2GHz
7.5 dB Typical at 4GHz

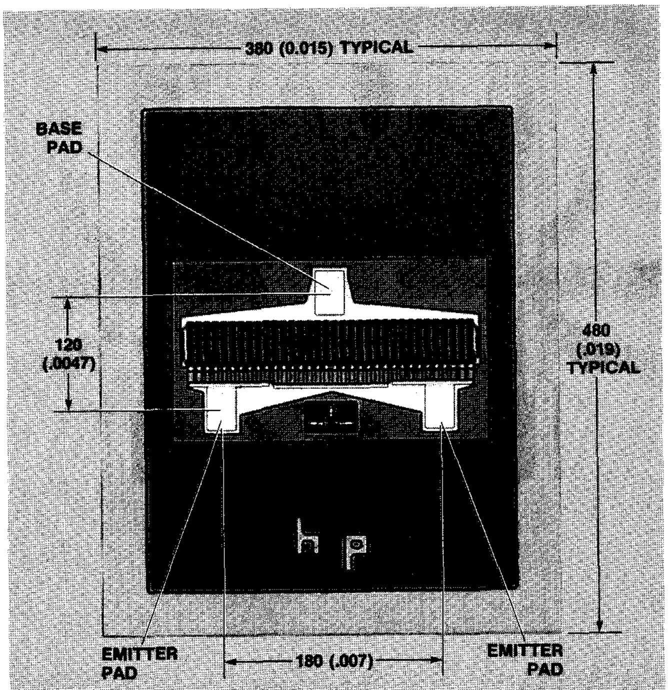
LOW DISTORTION

HIGH POWER-ADDED EFFICIENCY

Description/Applications

The HXTR-5002 is an NPN bipolar transistor chip designed for high output power and gain to 5GHz. To achieve excellent uniformity and reliability, the manufacturing process utilizes ion implantation, self-alignment techniques and Ti/Pt/Au metallization. The chip has a dielectric scratch protection over its active area and Ta_2N ballast resistors for ruggedness.

The superior power, gain and distortion performance of the HXTR-5002 commend it for use in broad and narrow band commercial and military communications, radar, and ECM hybrid applications. Programs requiring hermetically packaged devices with similar performance should employ the HXTR-5102 and the HXTR-5104, which utilize this chip.



CHIP OUTLINE
Dimensions in micrometers (inches)

Gold Bonding Pad Dimensions: ~ 38 (.0015) x 20 (.0008) Typical
Chip Thickness: 90 (.0035) Typical
Collector Back Contact: Silicon-Gold Eutectic

Electrical Specifications at T_A=25°C

Symbol	Parameters and Test Conditions		Test MIL-STD-750	Units	Min.	Typ.	Max.
BV_{CBO}	Collector-Base Breakdown Voltage at I_C=10mA		3001.1*	V	40		
BV_{CEO}	Collector-Emitter Breakdown Voltage at I_C=50mA		3011.1*	V	24		
BV_{EBO}	Emitter-Base Breakdown Voltage at I_B=100µA		3026.1*	V	3.3		
I_{EBO}	Emitter-Base Leakage Current at V_{EB}=2V		3061.1	µA			5
I_{CES}	Collector-Emitter Leakage Current at V_{CE}=32V		3041.1**	nA			200
I_{CBO}	Collector-Base Leakage Current at V_{CB}=20V		3036.1**	nA			100
h_{FE}	Forward Current Transfer Ratio at V_{CE}=18V, I_C=110mA		3076.1*		15	40	75
P_{1dB}	Power Output at 1dB Gain Compression	f = 2GHz 4GHz		dBm		29 27.5	
G_{1dB}	Associated 1dB Compressed Gain	f = 2GHz 4GHz		dB		12.5 7.5	
P_{SAT}	Saturated Power Output (8dB Gain) (3dB Gain)	f = 2GHz 4GHz		dBm		31.0 29.5	
η	Power-Added Efficiency at 1dB Compression	f = 2GHz 4GHz		%		38 23	
IMD	Third Order Intermodulation Distortion (Reference to either tone), at P_O(PEP)=.5W	f = 4GHz		dB		-30	
	Tuned for Maximum Output Power at 1dB Compression V_{CE}=18V, I_C=110mA, θ_{ja}=55°C/W						

*300µsec wide pulse measurement at ≤2% duty cycle.
**Measured under low ambient light conditions.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage	40V
V_{CEO}	Collector to Emitter Voltage	22V
V_{EBO}	Emitter to Base Voltage	3.3V
I_C	DC Collector Current	150 mA
P_T	Total Device Dissipation(2)	2.7W
T_J	Junction Temperature	200° C
T_{STG}	Storage Temperature	-65°C to +200° C

Notes:

1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device mean time between failure (MTBF) to below the design goal of 1 x 10^7 hours at T_J = 175° C (assumed Activation Energy = 1.5 eV).
2. Power dissipation derating should include a Θ_{JB} (Junction-to-Back contact thermal resistance) of 45° C/W.

   Total Θ_{JA} (Junction-to-Ambient) will be dependent upon the heat sinking provided in the individual application.

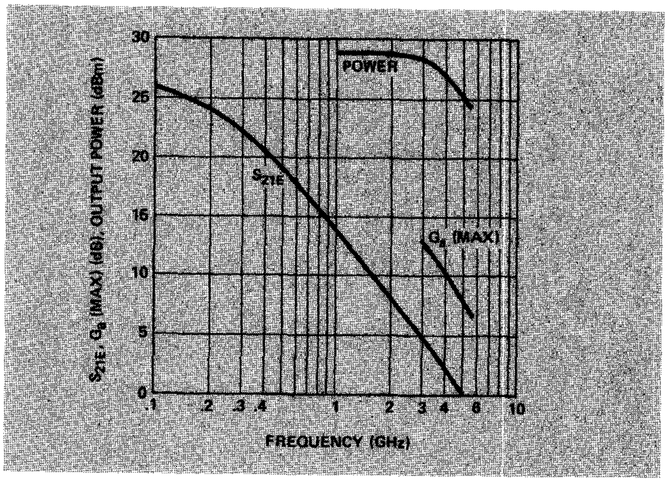


Figure 1. Typical S_{21E}, G_a(max) and P_{1dB} Linear Power vs. Frequency at V_{CE} = 18V, I_C = 110mA.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	45V
V_{CEO}	Collector to Emitter Voltage	27V
V_{EBO}	Emitter to Base Voltage	4V
I_C	DC Collector Current	250 mA
P_T	Total Device Dissipation	4W
T_J	Junction Temperature	300° C
$T_{STG(MAX)}$	Maximum Storage Temperature	300° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

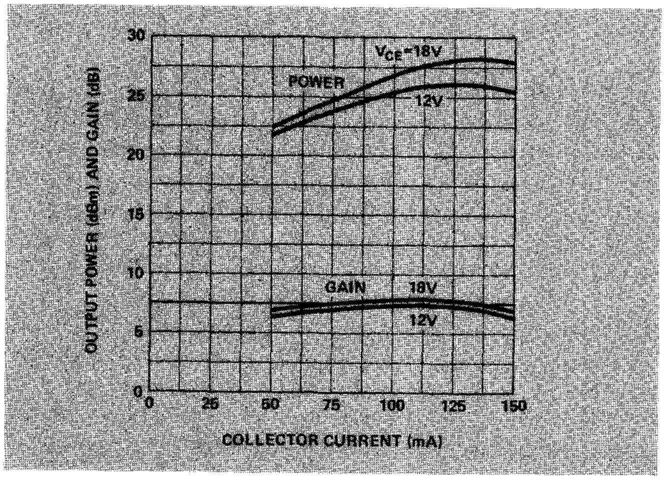


Figure 2. Typical P_{1dB} Linear Power and Associated 1dB Compressed Gain vs. Current at V_{CE} = 12 and 18V at 4GHz.

Typical S-Parameters* V_{CE} = 18V, I_C = 110mA

Freq. (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
0.100	0.55	-61	25.4	19.7	156	-31.6	0.03	68	0.93	-26
0.200	0.65	-98	24.2	16.2	133	-27.3	0.04	50	0.76	-46
0.300	0.72	-119	22.3	13.1	125	-25.6	0.05	39	0.63	-60
0.400	0.76	-132	20.6	10.7	117	-24.8	0.06	32	0.53	-71
0.500	0.79	-141	19.1	9.01	111	-24.4	0.06	27	0.45	-78
0.600	0.80	-147	17.8	7.73	106	-24.1	0.06	24	0.40	-84
0.700	0.81	-151	16.6	6.74	102	-24.0	0.06	22	0.36	-89
0.800	0.81	-155	15.5	5.97	99	-23.8	0.06	20	0.33	-93
0.900	0.82	-158	14.6	5.35	97	-23.7	0.06	19	0.31	-96
1.000	0.82	-160	13.7	4.84	94	-23.7	0.06	18	0.30	-99
1.500	0.83	-167	10.3	3.29	86	-23.4	0.07	16	0.25	-109
2.000	0.83	-170	7.9	2.49	80	-23.3	0.07	16	0.24	-114
2.500	0.83	-173	6.0	2.00	74	-23.1	0.07	17	0.24	-117
3.000	0.83	-174	4.5	1.68	69	-22.9	0.07	18	0.25	-118
3.500	0.83	-175	3.2	1.44	64	-22.6	0.07	19	0.27	-119
4.000	0.83	-176	2.1	1.27	60	-22.4	0.08	20	0.28	-120
4.500	0.83	-177	1.1	1.13	55	-22.1	0.08	21	0.30	-121
5.000	0.83	-177	0.3	1.03	51	-21.9	0.08	21	0.32	-121
5.500	0.83	-178	-0.5	0.94	47	-21.6	0.08	22	0.34	-122
6.000	0.83	-178	-1.2	0.87	43	-21.4	0.08	22	0.35	-123

* (Values do not include any parasitic bonding inductances and were generated by use of a computer model.)

HEWLETT PACKARD
COMPONENTS

NEW

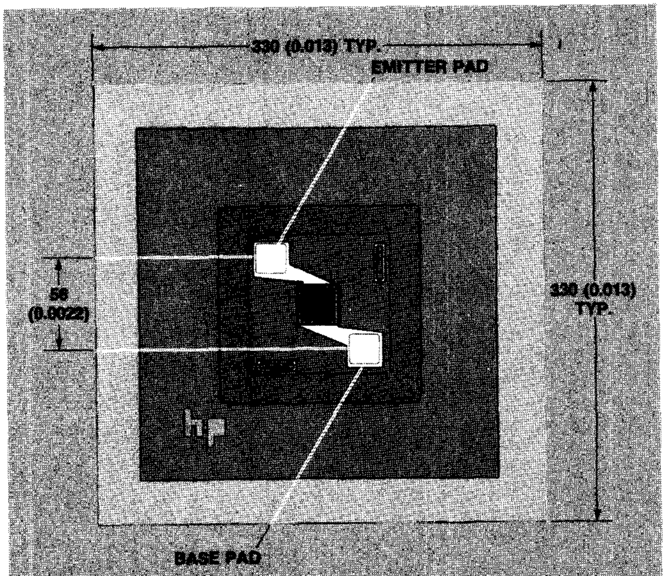
LOW NOISE TRANSISTOR CHIP

HXTR-6001

Features

LOW NOISE FIGURE
1.7 dB Typical at 2 GHz
2.7 dB Typical at 4 GHz

HIGH GAIN AT NOISE FIGURE BIAS
13.0 dB Typical at 2 GHz
9.0 dB Typical at 4 GHz



Chip Outline

Dimensions in Micrometers (Inches)

Gold Bonding Pad Dimensions:	25 (0.001) x 25 (0.001) Typical
Chip Thickness:	89 (0.0035) Typical
Collector Back Contact:	Silicon-Gold Eutectic

Description/Applications

The HXTR-6001 is an NPN bipolar transistor chip intended for use in hybrid applications requiring superior UHF and microwave low noise performance. Use of ion implantation and self-alignment techniques in its manufacture produce uniform devices requiring little or no individual circuit adjustments. The HXTR-6001 features a Ti/Pt/Au metallization system and a dielectric scratch protection over its active area to insure reliable operation.

Electrical Specifications at $T_A = 25°C$

Symbol	Parameters and Test Conditions	MIL-STD-750 Test Method	Units	Min.	Typ.	Max.
BV_{CES}	Collector-Emitter Breakdown Voltage at $I_C = 100 \mu A$	3011.1*	V	30		
I_{CEO}	Collector-Emitter Leakage Current at $V_{CE} = 10V$	3041.1**	nA			500
I_{CBO}	Collector Cutoff Current at $V_{CB} = 10V$	3036.1**	nA			100
h_{FE}	Forward Current Transfer Ratio at $V_{CE} = 10V$, $I_C = 4mA$	3076.1*	—	50	150	250
F_{MIN}	Minimum Noise Figure f=2 GHz 4 GHz	3246.1	dB		1.7 2.7	
G_a	Associated Gain f=2 GHz 4 GHz				13.0 9.0	
	Conditions for above: $V_{CE} = 10V$, $I_C = 4mA$, $\theta_{JA} = 250° C/W$					

*300µs wide pulse measurement ≤2% duty cycle.
**Measured under low ambient light conditions.

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Value
V_{CBO}	Collector to Base Voltage	25V
V_{CEO}	Collector to Emitter Voltage	16V
V_{EBO}	Emitter to Base Voltage	1.0V
I_C	DC Collector Current	10 mA
P_T	Total Device Dissipation[2]	150 mW
T_J	Junction Temperature	200° C
T_{STG}	Storage Temperature	-65° C to +200° C

Notes:

1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device mean time between failure (MTBF) to below the design goal of 1 x 10^7 hours at T_J = 175° C (assumed Activation Energy = 1.5 eV).
2. Power dissipation derating should include a Θ_{JB} (Junction-to-Back contact thermal resistance) of 150° C/W.

   Total Θ_{JA} (Junction-to-Ambient) will be dependent upon the heat sinking provided in the individual application.

Absolute Maximum Ratings*

Symbol	Parameter	Limit
V_{CBO}	Collector to Base Voltage	35V
V_{CEO}	Collector to Emitter Voltage	20V
V_{EBO}	Emitter to Base Voltage	1.5V
I_C	DC Collector Current	20 mA
P_T	Total Device Dissipation	300 mW
T_J	Junction Temperature	300° C
$T_{STG(MAX)}$	Maximum Storage Temperature	300° C

*Operation in excess of any one of these conditions may result in permanent damage to this device.

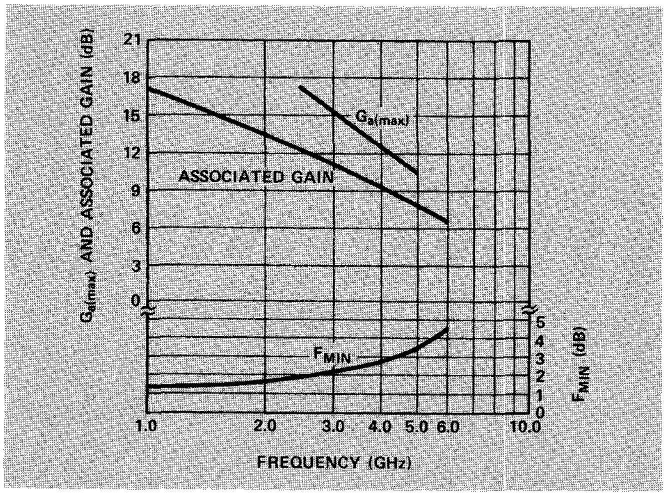


Figure 1. Typical $G_{a(max)}$, Noise Figure (F_{MIN}), and Associated Gain vs. Frequency at V_{CE} = 10V, I_C = 4mA.

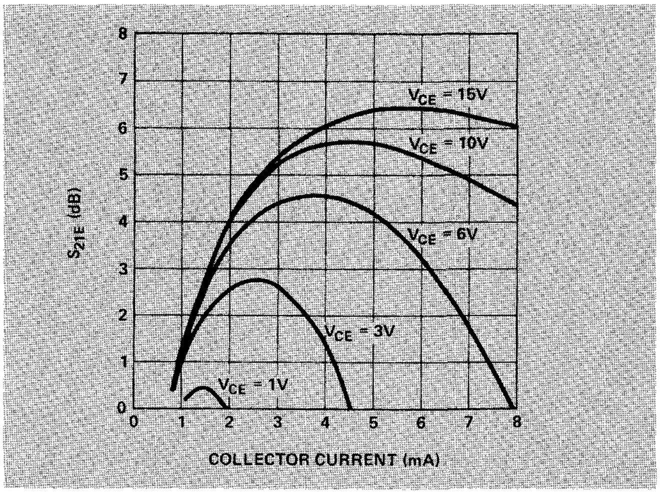


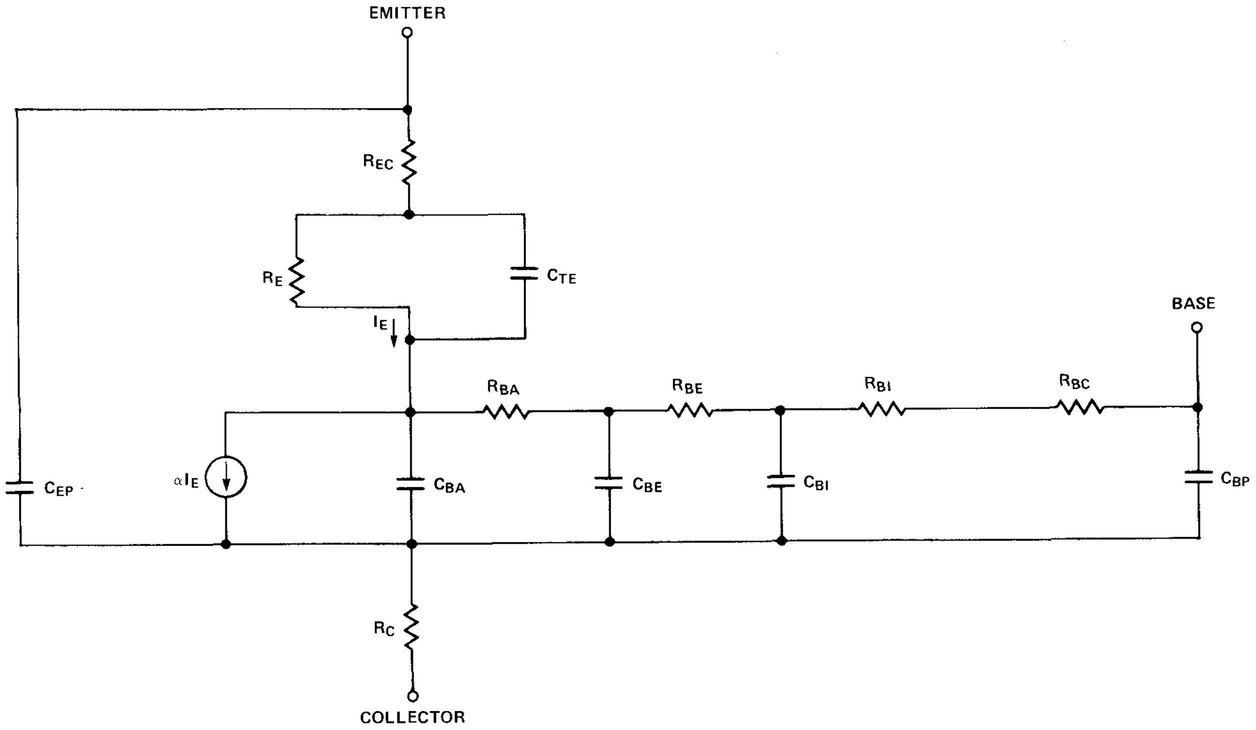
Figure 2. Typical S_{21E} vs. Current at 4 GHz.

Typical S-Parameters* V_{CE} = 10V, I_C = 4mA

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (MHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
100	0.87	-16	22.0	12.6	170	-46	0.005	82	0.99	-3
200	0.85	-30	21.7	12.1	160	-40	0.010	75	0.98	-5
300	0.82	-44	21.1	11.4	151	-36	0.015	68	0.95	-7
400	0.79	-57	20.5	10.6	144	-35	0.018	63	0.93	-9
500	0.76	-68	19.8	9.77	137	-34	0.021	58	0.91	-10
600	0.73	-78	19.1	9.00	131	-32	0.024	55	0.89	-10
700	0.70	-86	18.5	8.37	126	-32	0.025	52	0.87	-11.
800	0.68	-94	17.6	7.62	121	-31	0.027	50	0.85	-11
900	0.66	-100	17.0	7.05	118	-31	0.028	48	0.84	-11
1000	0.65	-106	16.3	6.54	114	-31	0.029	47	0.82	-11
1500	0.60	-126	13.5	4.73	102	-29	0.034	45	0.79	-12
2000	0.58	-139	11.3	3.67	93	-29	0.037	45	0.78	-13
2500	0.57	-146	9.5	2.99	87	-28	0.041	47	0.77	-14
3000	0.56	-152	8.1	2.53	82	-27	0.045	49	0.77	-15
3500	0.56	-156	6.8	2.19	77	-26	0.049	51	0.76	-16
4000	0.55	-159	5.7	1.93	72	-26	0.053	52	0.76	-18
4500	0.55	-162	4.8	1.73	68	-25	0.057	53	0.76	-19
5000	0.55	-164	3.9	1.57	65	-24	0.062	54	0.76	-21
5500	0.55	-165	3.2	1.44	61	-24	0.066	55	0.76	-23
6000	0.54	-167	2.5	1.34	57	-23	0.071	55	0.76	-24
7000	0.54	-169	1.4	1.17	51	-22	0.080	56	0.77	-28

*Values do not include any parasitic bonding inductances and were generated by use of a computer model.

BIPOLAR CHIP EQUIVALENT CIRCUIT[1]



CURRENT DEPENDENT CURRENT SOURCE

$$\alpha = \frac{\alpha_o}{1 + j\, f/f_b} \exp(-j\, 2\, \pi\, f\, \tau)$$

$$\alpha_o = \frac{H_{fe}}{1 + H_{fe}}$$

$$R_e\, \alpha = \frac{\alpha_o}{1 + (f/f_b)^2} \left[\cos(2\pi f\tau) - \frac{f}{f_b} \sin(2\pi f\tau)\right]$$

$$\mathrm{Im}\, \alpha = \frac{-\alpha_o}{1 + (f/f_b)^2} \left[\sin(2\pi f\tau) + \frac{f}{f_b} \sin(2\pi f\tau)\right]$$

NOTE: 1. This equivalent circuit is for the transistor chip only. It does not include parasitic bonding reactances. For additional information, please refer to "Low-Noise Microwave Bipolar Transistor with Sub-Half-Micrometer Emitter Width" by Tzu-Hwa Hsu and Craig P. Snapp, IEEE Transactions on Electron Devices, Vol. ED-25, No. 6, June 1978.

BIPOLAR CHIP EQUIVALENT CIRCUIT ELEMENTS

DEVICE	C_{BP} (pF)	C_{EP} (pF)	C_{BI} (pF)	C_{BE} (pF)	C_{BA} (pF)	C_{TE} (pF)	R_{EC} (Ω)	R_{BI} & R_{BC} (Ω)	R_{BE} (Ω)	R_{BA} (Ω)	R_C (Ω)	R_E (Ω)	α_o	f_b GHz	τ psec.
HXTR-6001 10V, 4 mA	0.053	0.05	0.019	0.016	0.0055	1.03	0.7	0.4	7.8	6.1	7	8.6	0.990	22.7	12.1
HXTR-2001 15V, 25 mA	0.066	0.06	0.07	0.056	0.032	4.8	0.2	0.2	3.5	4.4	5	1.0	0.990	22.7	10.8
HXTR-2001 15V, 15 mA	0.066	0.06	0.07	0.056	0.032	4.8	0.2	0.2	3.5	4.4	5	1.7	0.990	22.7	10.6
HXTR-5001 18V, 30 mA	0.065	0.06	0.07	0.053	1.034	5.1	7.2	.2	5.6	4.7	5	0.86	0.976	22.7	10.8
HXTR-5002 18V, 110 mA	0.105	0.15	0.22	0.18	0.11	17.3	3.1	0.2	1.7	1.4	3	0.24	0.976	22.7	10.9

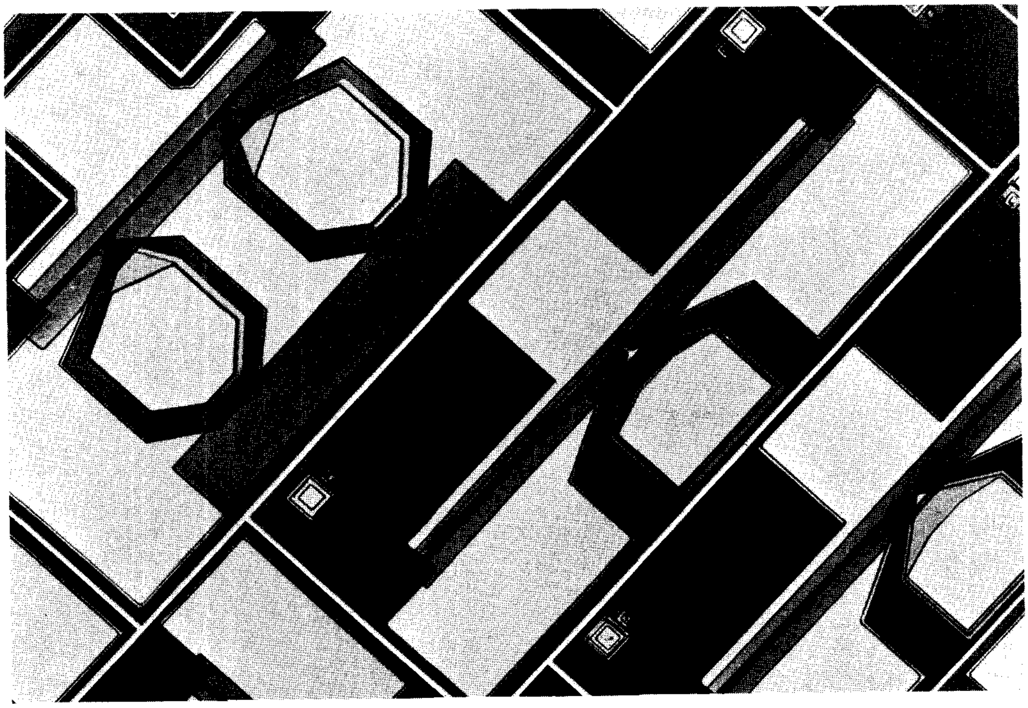
Recommended Die Attach and Bonding Procedures

Eutectic Die Attach at a stage temperature of 410 ± 10° C under an N_2 ambient. Chip should be lightly scrubbed using a tweezer and eutectic should flow within five seconds.

Thermocompression Wire Bond at a stage temperature of 310 ± 10° C, using a tip force of 30 ± 5 grams with 0.7 mil gold wire. A one mil minimum wire clearance at the passivation edge is recommended. (Ultrasonic bonding is not recommended.)

Packaging — The chip should be packaged into a clean, dry, hermetic environment.

GaAs FET Chips



GaAs Field Effect Transistor Chip Selection Guide

Features	Typical Performance at 10 GHz	Part Number HFET-	Page Number
Low Noise Figure High Associated Gain High Output Power (P_{1dB})	3.2 dB 6.9 dB 15.4 dBm	1001	207
High Linear Power High Associated 1 dB Compression Gain	19.5 dBm 6.5 dB	5001	210

HEWLETT PACKARD
COMPONENTS

NEW

GENERAL PURPOSE MICROWAVE GaAs FET CHIP

HFET -1001

Features

HIGH GAIN
13.3 dB Typical Gain at 8 GHz
11.5 dB Typical at 10 GHz

LOW NOISE FIGURE
1.5 dB Typical at 4 GHz
3.2 dB Typical at 10 GHz

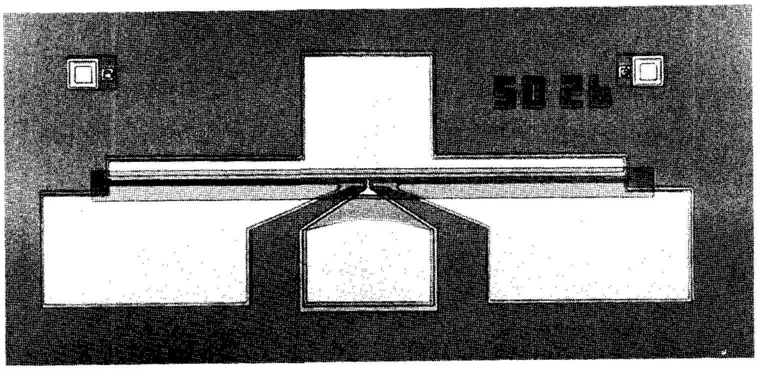
HIGH P_{1dB} LINEAR POWER
17.1 dBm Typical at 4 GHz
15.4 dBm Typical at 10 GHz

RUGGED CHIP

INTEGRAL CHANNEL PARTICLE AND SCRATCH PROTECTION

SUITABLE FOR BROADBAND APPLICATIONS

LARGE GOLD BONDING PADS



Chip Dimensions in mm (in.)
0.69 (0.027) x 0.31 (0.012) x 0.13 (0.005)
(See page 212 for bonding pad dimensions)

Description/Applications

The HFET-1001 is a gallium arsenide Schottky barrier field effect transistor chip designed for use in broadband and narrow-band applications to 12 GHz. Its rugged construction and excellent microwave performance in gain, noise figure and output power commend it for use in demanding applications such as ECM, radar and land and satellite communications.

The chip is provided with a dielectric particle and scratch protection layer over the active area. The gate width is 500 micrometers, which results in a typical linear output power of greater than 25 mW at 10 GHz and facilities matching as low as 1.5 GHz.

Electrical Specifications at $T_A = 25°C$

Symbol	Parameters and Test Conditions		Units	Min.	Typ.	Max.
I_{DSS}	Saturated Drain Current $V_{DS} = 4.0$ V, $V_{GS} = 0$ V		mA	40		120
V_{GSP}	Pinch Off Voltage $V_{DS} = 4.0$ V, $I_{DS} = 100$ μA		V	-1.5		-5.0
g_m	Transconductance $V_{DS} = 4.0$V, Δ $V_{GS} = 0$ V to -0.5 V		mmho	30	45	
$G_{a(max)}$	Maximum Available Gain $V_{DS} = 4.0$ V, $V_{GS} = 0$ V	f = 8 GHz 10 GHz	dB		13.3 11.5	
F_{min}	Noise Figure	f = 4 GHz 8 GHz 10 GHz	dB		1.5 2.6 3.2	
G_a	Associated Gain At NF Bias $V_{DS} = 3.5$V $I_{DS} = 15\%$ I_{DSS} (Typ. 12 mA)	f = 4 GHz 8 GHz 10 GHz	dB		11.8 8.5 6.9	
P_{1dB}	Power Output at 1 dB Gain Compression	f = 4 GHz 8 GHz 10 GHz	dBm		17.1 16.3 15.4	
G_{1dB}	Associated 1 dB Compressed Gain $V_{DS} = 5.0$V, $I_{DS} = 50\%$ I_{DSS} Tuned for Maximum Output Power at +5 dBm Input	f = 4 GHz 8 GHz 10 GHz	dB		12.4 10.1 9.1	

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Values
V_{DS}	Drain to Source Voltage $-5.0\ V \leq V_{GS} \leq 0.0\ V$	5V
V_{GS}[2]	Gate-to-Source Voltage $5.0\ V \geq V_{DS} \geq 0.0V$	-5V
T_{CH}[3]	Maximum Channel Temperature	175° C
T_{STG}	Storage Temperature	-65° C to +175° C

Notes:

1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device mean time between failure (MTBF) to below the design goal of 1 x 10^7 hours at T_{CH} = 150° C (assumed Activation Energy = 1.6 eV).
2. Maximum Continuous Forward Gate Current should not exceed 2.5 mA.
3. Θ_{CB} — Thermal resistance, channel to back of chip = 100° C/W.

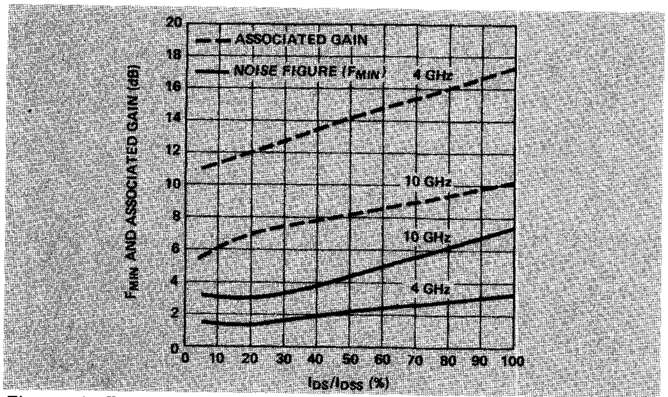


Figure 1. Typical Noise Figure and Associated Gain vs. I_{DS} as a percentage of I_{DSS} at 4 GHz and 10 GHz, V_{DS} = 3.5 V.

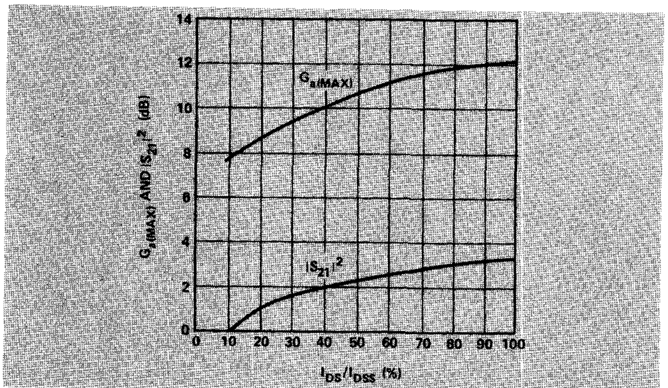


Figure 3. Typical $G_{a(max)}$ and $|S_{21}|^2$ vs. I_{DS} as a percentage of I_{DSS}. Frequency = 10 GHz, V_{DS} = 4.0 V.

Absolute Maximum Ratings[1]

Symbol	Parameter	Limits
V_{DS}	Drain to Source Voltage $-10\ V \leq V_{GS} \leq 0.0V$	11V
V_{GS}[2]	Gate to Source Voltage $10\ V \geq V_{DS} \geq 0.0\ V$	-10V
T_{CH}	Maximum Channel Temperature	300° C
$T_{STG(max)}$	Maximum Storage Temperature	300° C

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. Maximum Forward Gate Current should not exceed 3 mA.

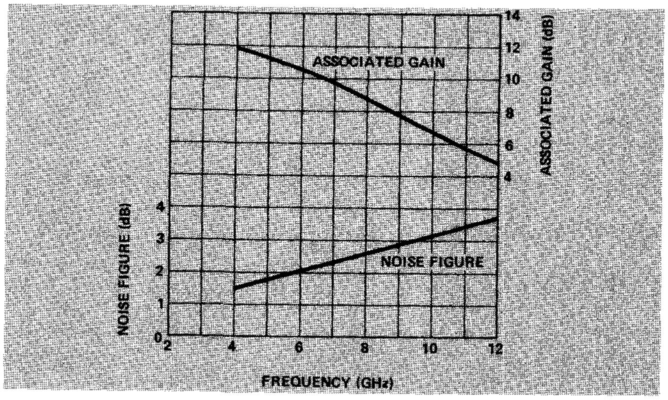


Figure 2. Typical Noise Figure and Associated Gain vs. Frequency. V_{DS} = 3.5 V, I_{DS} = 15% I_{DSS}.

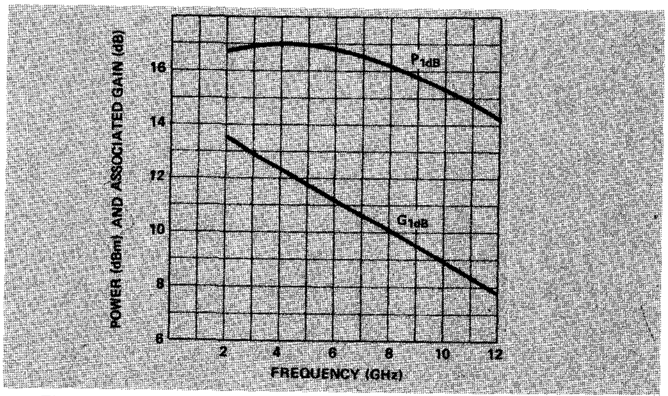


Figure 4. Typical P_{1dB} Linear Power and Associated 1 dB Compressed Gain vs. Frequency at V_{DS} = 5.0 V, I_{DS} = 50% I_{DSS}.

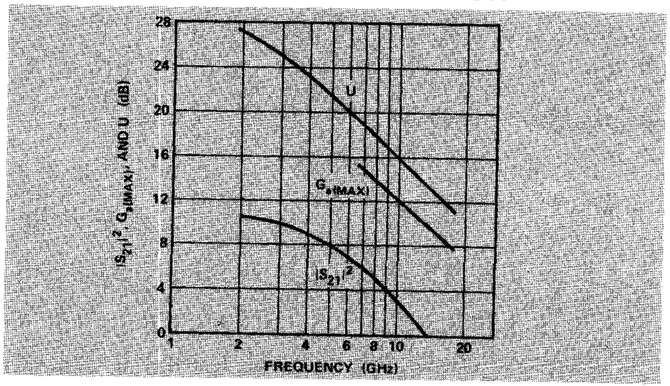


Figure 5. Mason's Gain (U), $G_{a(max)}$ and $|S_{21}|^2$ vs. Frequency, V_{DS} = 4.0 V, V_{GS} = 0.0 V.

Typical S - Parameters

HIGH GAIN BIAS $V_{DS} = 4.0V$, $V_{GS} = 0V$.

Freq. (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
2.0	0.94	-41	10.52	3.36	148	-34.42	0.02	71	0.79	-9
3.0	0.90	-62	10.04	3.18	133	-31.06	0.03	62	0.76	-17
4.0	0.85	-80	8.95	2.80	120	-30.17	0.03	57	0.76	-19
5.0	0.82	-96	7.96	2.50	107	-29.90	0.03	53	0.74	-24
6.0	0.80	-106	6.88	2.21	97	-29.37	0.03	50	0.74	-29
7.0	0.78	-117	6.24	2.05	89	-29.12	0.04	50	0.74	-33
8.0	0.77	-125	5.06	1.79	80	-30.17	0.04	49	0.74	-40
9.0	0.76	-132	4.08	1.60	72	-28.87	0.04	52	0.76	-44
10.0	0.76	-135	3.03	1.42	66	-28.87	0.04	55	0.76	-50
11.0	0.74	-139	2.61	1.35	62	-28.64	0.04	60	0.78	-52
12.0	0.73	-141	1.52	1.19	57	-28.40	0.04	64	0.79	-54

LINEAR POWER BIAS $V_{DS} = 5.0V$, $I_{DS} = 50\% \ I_{DSS}$

Freq. (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
2.0	0.93	-43	8.69	2.72	146	-33.12	0.02	69	0.77	-9
3.0	0.90	-62	7.96	2.50	131	-30.46	0.03	61	0.76	-13
4.0	0.86	-80	7.08	2.26	119	-29.07	0.04	55	0.74	-17
5.0	0.82	-94	6.20	2.04	106	-28.04	0.04	51	0.73	-21
6.0	0.77	-106	5.05	1.79	96	-27.52	0.04	47	0.72	-26
7.0	0.76	-115	4.11	1.61	88	-27.19	0.04	45	0.72	-30
8.0	0.75	-123	3.42	1.48	81	-26.98	0.05	47	0.72	-33
9.0	0.74	-128	2.61	1.35	72	-26.75	0.05	46	0.73	-38
10.0	0.72	-132	1.65	1.21	65	-26.57	0.05	48	0.73	-42
11.0	0.71	-138	1.03	1.13	61	-26.36	0.05	50	0.74	-46
12.0	0.71	-142	0.68	1.08	54	-25.89	0.05	52	0.75	-50

MINIMUM NOISE FIGURE BIAS $V_{DS} = 3.5V$, $I_{DS} = 15\% \ I_{DSS}$

Freq. (GHz)	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	MAg.	Ang.
2.0	0.95	-32	6.73	2.17	152	-28.64	0.04	72	0.72	-11
3.0	0.91	-49	6.44	2.10	139	-25.35	0.05	63	0.74	-18
4.0	0.86	-66	5.83	1.96	124	-23.48	0.07	55	0.74	-23
5.0	0.82	-81	5.20	1.82	111	-22.50	0.08	48	0.71	-28
6.0	0.79	-94	4.13	1.61	99	-22.16	0.08	42	0.70	-34
7.0	0.76	-104	3.67	1.53	91	-21.83	0.08	38	0.69	-40
8.0	0.75	-113	2.61	1.35	80	-21.41	0.09	33	0.69	-47
9.0	0.74	-120	1.66	1.21	71	-21.51	0.08	30	0.70	-54
10.0	0.74	-125	0.68	1.08	65	-21.72	0.08	30	0.71	-58
11.0	0.72	-128	0.10	1.01	60	-21.72	0.08	31	0.72	-60
12.0	0.71	-131	-0.85	0.91	55	-21.83	0.08	31	0.74	-62

HEWLETT PACKARD
COMPONENTS

NEW

MICROWAVE GaAs FET CHIP

HFET-5001

Features

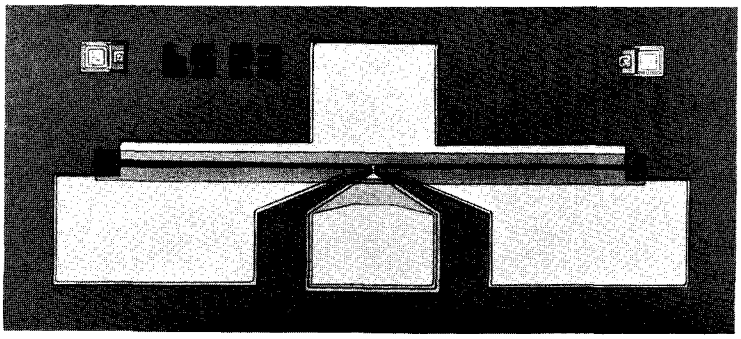
HIGH P_{1dB} LINEAR POWER
18.5 dBm Typical at 12 GHz
19.5 dBm Typical at 10 GHz
21.0 dBm Typical at 4 GHz with 11.0 dB Associated Gain

SUITABLE FOR BROADBAND APPLICATIONS

RUGGED CHIP

INTEGRAL CHANNEL PARTICLE AND SCRATCH PROTECTION

LARGE GOLD BONDING PADS



Chip Dimensions in mm (in.)
0.69 (0.027) x 0.31 (0.012) x 0.13 (0.005)
(See page 212 for bonding pad dimensions.)

Description

The HFET-5001 is a gallium arsenide Schottky barrier field effect transistor chip designed for high gain and linear power from 2 to 14 GHz. The chip is provided with a dielectric particle and scratch protection layer over the active area. The gate width is 500 micrometers resulting in a typical linear output power of greater than 100 mW at 8 GHz.

Electrical Specifications at T_A=25°C

Symbol	Parameters and Test Conditions	Units	Min.	Typ.	Max.
I_{DSS}	Saturated Drain Current V_{DS} = 4.0V, V_{GS} = 0V	mA	80		170
V_{GSP}	Pinch Off Voltage V_{DS} = 3.0V, I_{DS} = 1mA	V	−1.5		−8.0
g_m	Transconductance V_{DS} = 4.0V, ΔV_{GS} = 0V to −0.5V	mmho	25	30	
P_{1dB}	Power Output at 1 dB Gain Compression Tuning Fixed for Maximum Power Output at:				
	P_{IN} = +10 dBm f = 4 GHz	dBm		21.0	
	P_{IN} = +12 dBm f = 8 GHz			20.5	
	10 GHz			19.5	
	12 GHz			18.5	
G_{1dB}	Associated 1dB Compressed Gain f = 4 GHz	dB		11.0	
	8 GHz			8.0	
	10 GHz			6.5	
	12 GHz			5.5	
	Conditions for above: V_{DS} = 5.0V, I_{DS} = 50% I_{DSS}				

Recommended Maximum Continuous Operating Conditions[1]

Symbol	Parameter	Values
V_{DS}	Drain to Source Voltage $-8.0V \le V_{GS} \le 0.0V$	5V
V_{GS}[2]	Gate To Source Voltage $5.0V \ge V_{DS} \ge 0.0V$	-8V
T_{CH}[3]	Maximum Channel Temperature	175° C
T_{STG}	Storage Temperature	-65° C to +175° C

Notes:

1. Operation of this device in excess of any one of these conditions is likely to result in a reduction in device mean time between failure (MTBF) to below the design goal of 1 x 10^7 hours at T_{CH} = 150° C (assumed Activation Energy = 1.6 eV).
2. Maximum Continuous Forward Gate Current should not exceed 2.5 mA.
3. Θ_{CB} — Thermal resistance, channel to back of chip = 100° C/W.

Absolute Maximum Ratings[1]

Symbol	Parameter	Limits
V_{DS}	Drain to Source Voltage $-10V \le V_{GS} \le 0V$	10V
V_{GS}[2]	Gate To Source Voltage $10V \ge V_{DS} \ge 0V$	-10V
T_{CH}	Maximum Channel Temperature	300° C
$T_{STG(MAX)}$	Maximum Storage Temperature	300° C

Notes:

1. Operation in excess of any one of these conditions may result in permanent damage to this device.
2. Maximum Forward Gate Current should not exceed 3 mA.

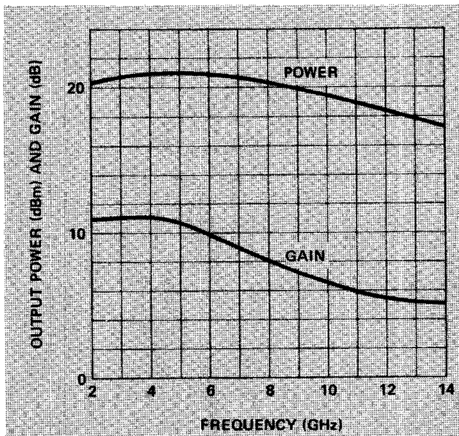


Figure 1. Typical P_{1dB} Linear Power and Associated 1 dB Compressed Gain vs. Frequency at V_{DS} = 5.0V, I_{DS} = 50% I_{DSS}.

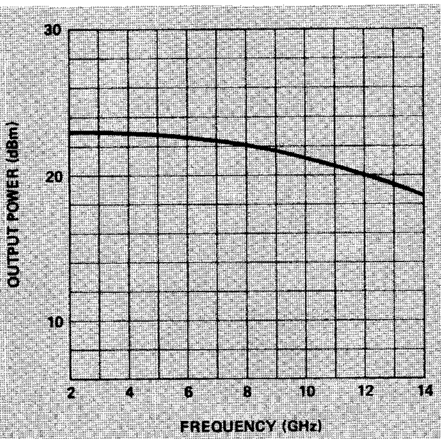


Figure 2. Typical Output Power at 3 dB Gain vs. Frequency, V_{DS} = 5.0V, I_{DS} = 50% I_{DSS}.

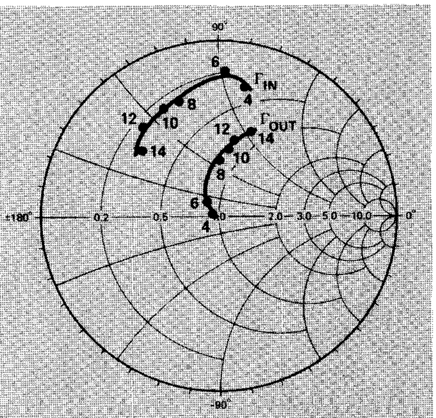


Figure 3. Typical Source (Γ_{IN}) and Load (Γ_{OUT}) Impedance for Maximum P_{1dB} Output Power (tuned with P_{IN} = +12 dBm) in the 4 to 14 GHz frequency range, V_{DS} = 5.0V, I_{DS} = 50% I_{DSS}.

Typical Small Signal S-Parameters V_{DS} = 5.0V, I_{DS} = 50% I_{DSS}

	S_{11}		S_{21}			S_{12}			S_{22}	
Freq. (GHz)	Mag.	Ang.	(dB)	Mag.	Ang.	(dB)	Mag.	Ang.	Mag.	Ang.
2.00	.97	− 32	7.72	2.43	153	−34.00	0.02	74	0.69	−10
3.00	.95	− 47	7.22	2.30	141	−30.46	0.03	67	0.68	−14
4.00	.91	− 61	6.84	2.20	130	−27.96	0.04	62	0.67	−19
5.00	.87	− 76	6.09	2.02	118	−26.02	0.05	55	0.67	−23
6.00	.84	− 87	5.37	1.86	109	−26.02	0.05	51	0.66	−28
7.00	.82	− 96	4.66	1.71	100	−26.02	0.05	49	0.65	−33
8.00	.81	−106	3.92	1.57	92	−24.44	0.06	47	0.65	−36
9.00	.78	−115	3.03	1.42	84	−24.44	0.06	45	0.66	−42
10.00	.77	−119	2.28	1.30	79	−24.44	0.06	46	0.66	−44
11.00	.77	−122	2.01	1.26	74	−24.44	0.06	48	0.66	−49
12.00	.76	−124	1.30	1.16	65	−24.44	0.06	48	0.67	−53
13.00	.75	−126	0.75	1.09	62	−24.44	0.06	49	0.69	−57
14.00	.75	−128	0.04	1.01	58	−23.10	0.07	53	0.70	−62

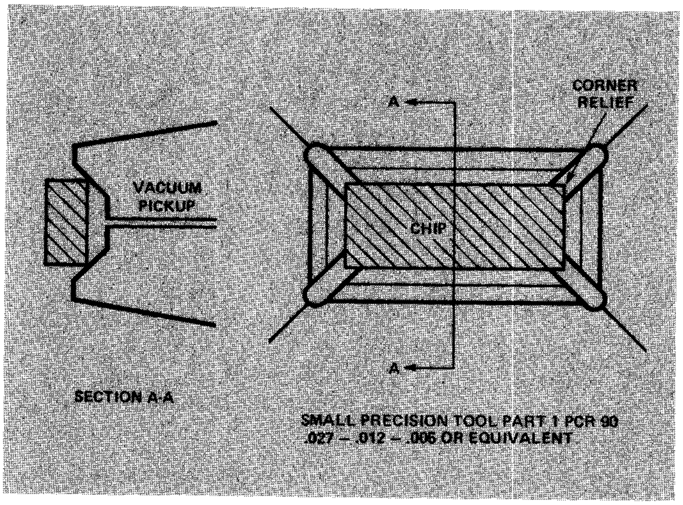
Handling And Use Precautions

1. Device voltage breakdown and permanent damage can be caused by the following:
   a. Inductive pickup from large transformers, switching power supplies, induction ovens, etc. Use shielded signal and power cables.
   b. Transients from voltmeters, multimeters, signal generators, curve tracers, etc. Avoid turning instrument power on and off, or switching between instrument ranges when bias is applied to the device.

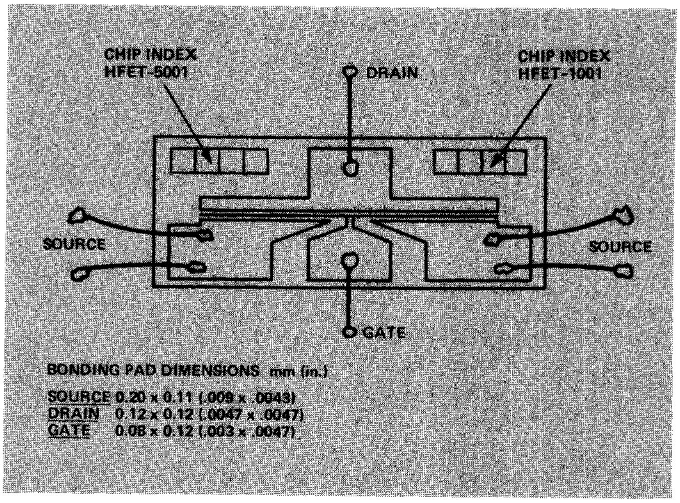
      For thermal compression and pulse bonders, insure that bonders are adequately grounded.
   c. Static Discharge—Assembly and test personnel, as well as tweezers or any other pick-up tool, should be grounded to the test or assembly station, preventing the build-up of static charge which can damage the gate area if the charge is allowed to pass through it. During the mounting procedure, insure assembly equipment is adequately grounded.

      Static discharge during handling, testing, assembly, and final seal can induce increased reverse gate leakage of a resistive nature.
2. Light Sensitivity — GaAs FETs characteristically are light sensitive and this should be borne in mind when making DC and RF measurements. Ensure that the measurement environment is the same as the use environment.
3. Moisture—The presence of excessive moisture on a FET chip surface under normal operating voltages may cause irreversible damage.
4. Application of Bias—When applying bias to the FET, first apply the gate voltage, then the drain voltage. When removing bias, remove the gate voltage last.

Die Attach And Wire Bonding



Recommended Die Attach Collet for HFET-1001, HFET-5001.



Bonding Diagram and Pad Dimensions for HFET-1001, HFET-5001.

Die Attaching

The FET chip can be die attached manually using a pair of tweezers, or automatically using a collet. In either case, provide a flow of nitrogen over the stage area. Start with a stage temperature of 300° C and raise as required. The chip should not be exposed, however, to greater than 320° C for more than 30 seconds. A 80/20 gold/tin preform of 625 x 250 x 25 micrometers (.025 x .010 x .001 in.) or standard round preform of equivalent volume is recommended. When using tweezers make sure that the chip is level to facilitate subsequent capillary wire bonding. The requirement is less critical for wedge bonding.

Gallium arsenide material is more brittle than silicon and should be handled with care. When using a collet, it is important to have a flat die attach surface. By using a minimum of downward force, the chance of breaking the chip is reduced.

Wire Bonding

Either thermal-compression or ultrasonic wire bonding of 18/25 micrometer (.0007"/.001") diameter, pure gold, stress relieved wire can be used.

For thermal-compression bonding, start with a stage temperature of 225°C and a tip temperature of 150°C. The typical bonding force should be approximately 30 grams and should not exceed 40 grams.

For ultrasonic bonding, the stage can be heated to 150°C with a bonding force of approximately 25 grams. Scrubbing frequency, amplitude and time is bonder dependent and is determined empirically.

The wire bond on the gate pad should remain well inside the pad boundaries. Additionally, mechanical contact with the transparent channel areas must be avoided to prevent gate damage.

Applications for Hybrid Devices

HEWLETT hp PACKARD
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APPLICATIONS FOR HYBRID DEVICES

Impedance Matching Techniques for Mixers and Detectors (Portion of Application Note 963)

INTRODUCTION

The use of tables for designing impedance matching filters for real loads is well known[1]. Simple complex loads can often be matched by this technique by incorporating the imaginary portion of the load into the first filter element[2]. This technique is rarely useful for matching diodes because the equivalent circuit for the diode must include several real and imaginary elements. A methodical technique for matching such complex loads to a transmission line will be described. Previous references[3] to similar procedures were empirical in nature. No tables are used, but it is necessary to know the admittance of the diode in the frequency band of interest.

This application note is applicable to both mixers and detectors. As an example, a section of the detector portion is presented here.

DETECTOR DIODE

With a small amount of dc bias, the 5082-2709 beam lead diode makes an excellent detector diode. The matching procedure will not be so successful in this application, because the admittance is farther from the center of the Smith Chart and is more dispersive. Figure 1 shows the measured admittance of the diode with 50 microamperes bias current and the equivalent circuit obtained with the computer optimization program. The circuit elements representing package parasitics were assumed to be the same for this application as for the mixer application.

Figure 2 shows the three steps in the matching procedure for the detector diode. The 8.2 ohm characteristic impedance required for the shunt resonant transmission line would be difficult to realize. By using two lines in shunt, the characteristic impedance of each is doubled to a more practicle value of 16.4 ohms. This technique also reduces parasitics by maintaining symmetry.

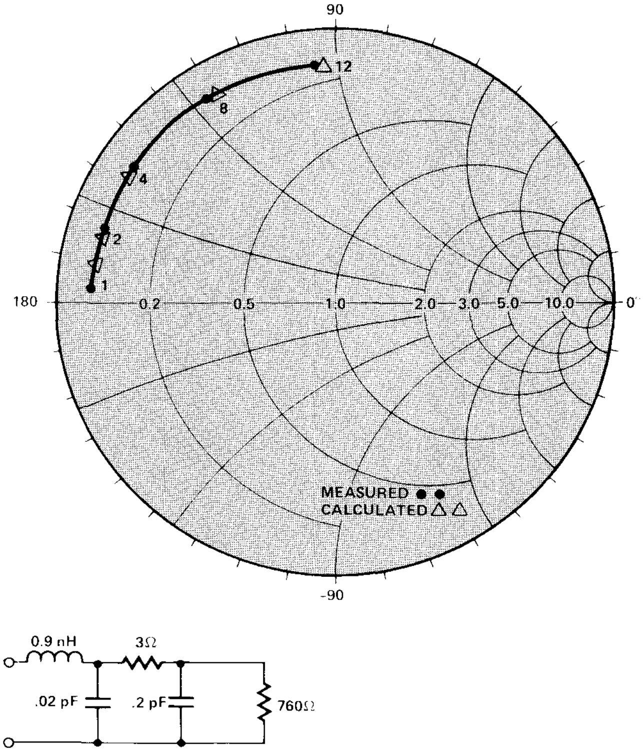


Figure 1. 5082-2709 Beam Lead Diode Admittance, 50 μA Bias.

Although the maximum VSWR of 3.6 obtained in this example is adequate for many detector applications, a smaller reflection coefficient is required in some cases in order to avoid deterioration of performance of adjacent circuits. It is possible to improve the design by using both series and shunt resonant circuits to make a double loop on the Smith Chart. However, such a complicated circuit would be difficult to realize. It is often permissible to sacrifice some sensitivity in order to improve the VSWR. In this case the technique shown in Figure 3 is suggested. Here the maximum VSWR is reduced below 1.7 by first moving the diode admittance closer to the center of the Smith Chart by adding a 300 ohm shunt resistor across the diode. The three matching elements are then added.

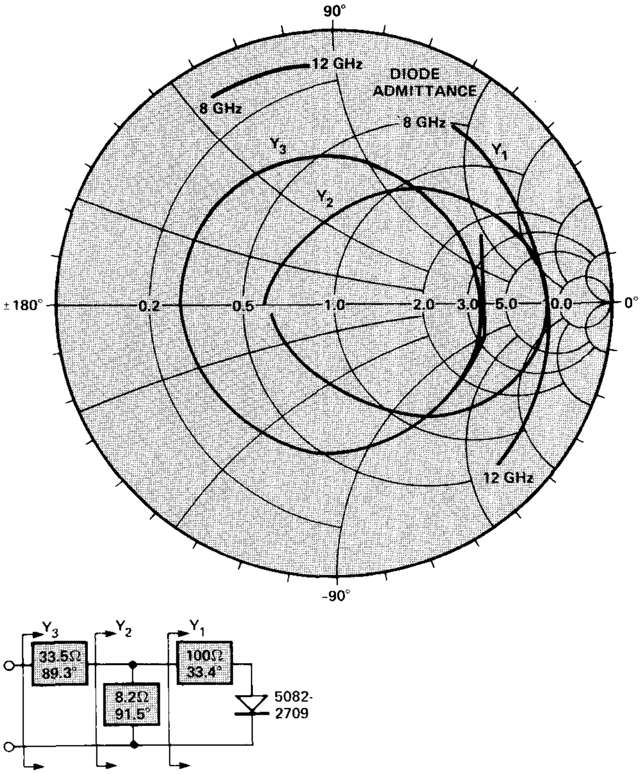


Figure 2. Matching the Detector Diode, 50 μA Bias, Admittance Coordinates.

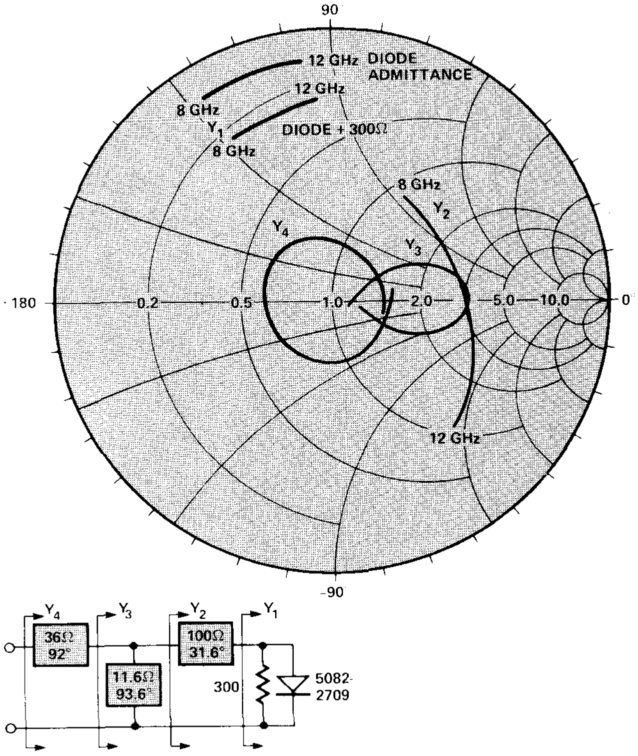


Figure 3. Resistive Matching of Detector Diode, 50 μA Bias, Admittance Coordinates.

Sensitivity may be traded for VSWR by adjusting the value of the shunt resistor. Figure 4 illustrates this tradeoff. An unmatched detector diode has a sensitivity of 1.5 millivolts per microwatt. A broadband reactive matching circuit (Figure 2) causes about 1 dB loss due to reflection. Improving the match with a shunt resistor of 1000 and 300 ohms causes more loss due to power absorbed by the resistors. However, sensitivity loss due to reflections from an unmatched diode is one or two dB worse than that due to the matching network using a 300 ohm resistor.

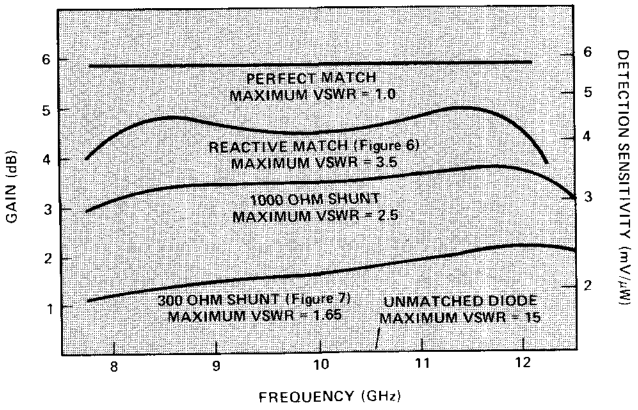


Figure 4. Gain of Detector Matching Networks.

REFERENCES

1. Weinberg, L., Network Analysis and Synthesis, McGraw-Hill, 1962.
2. Matthaei, G., Young, L., and Jones, E.M.T., Microwave Filters, Impedance-Matching Networks, and Coupling Structures, McGraw-Hill, 1964.
3. LaCombe, D., "Thick-Film Limiter-Detector Reduces Receiver Costs", Microwave System News, August, 1973, pp 37-42.

The Beam Lead Mesa PIN in Shunt Applications (Portion of AN 971)

INTRODUCTION

The low RC product, fast switching time, and other unique features of the HPND-4050 beam lead PIN diode make it well suited for switching applications in the shunt configuration. Proper choice and optimum design of circuit to minimize parasitics and loss will allow these inherent characteristics of the HPND-4050 to be exploited to the fullest and achieve maximum performance.

SWITCHING PERFORMANCE

The actual performance of the HPND-4050 as a shunt switch is illustrated in Figures 1 and 2. The points denoted by Δ are results of a computer analysis yielding the equivalent circuit shown in Figure 3. It can be observed that isolation actually increases with frequency up to X-band due to shunt capacitance before it rolls off as lead inductance dominates. Insertion loss increases steadily with frequency as a result of shunt capacitance. This data confirms the importance of low parasitics and a low RC product.

The fast switching time observed is shown in Figure 4. To switch from an isolation state with forward bias of 10 mA to a transmission (insertion loss) state with reverse bias of −10 volts, less than 1 nanosecond is required. Much less than 1 nanosecond is needed to switch from a transmission to an isolation state.

OTHER TOPICS

Practical circuits, handling, and bonding suggestions are also discussed in this application note.

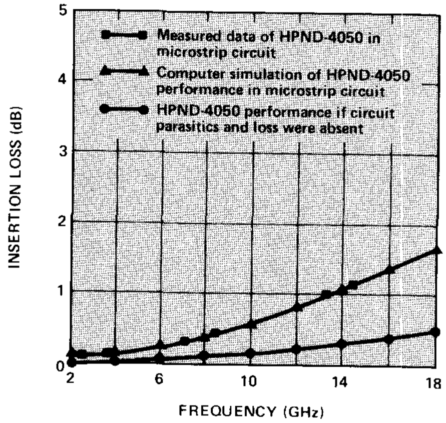


Figure 1. Insertion Loss of HPND-4050 as Shunt Switch.

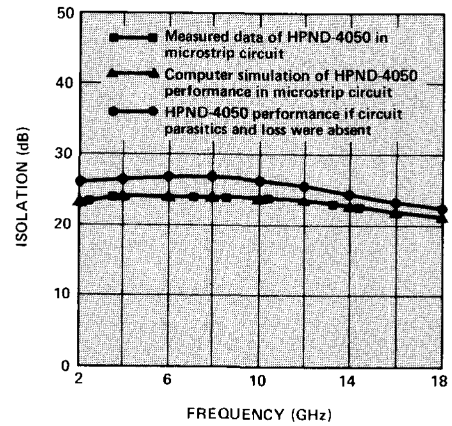
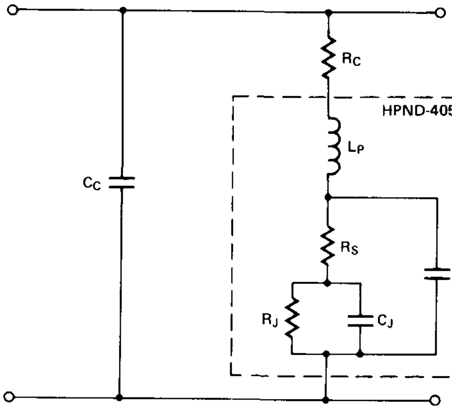


Figure 2. Isolation of HPND-4050 as Shunt Switch.



SYMBOL	PARAMETER	SWITCH "ON"	SWITCH "OFF"	UNITS
R_c	Circuit Resistance	.5	.5	Ω
C_c	Circuit Capacitance	.12	.12	pF
L_p	Package Inductance	.02	.02	nH
C_p	Package Capacitance	.02	.02	pF
R_s	Series Resistance	.5	.5	Ω
R_j	Junction Resistance	20K	.8	Ω
C_j	Junction Capacitance	.1	20	pF

Figure 3. Equivalent Circuit of HPND-4050 in Microstrip Circuit.

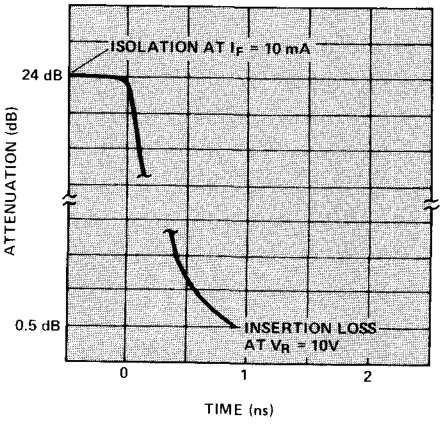
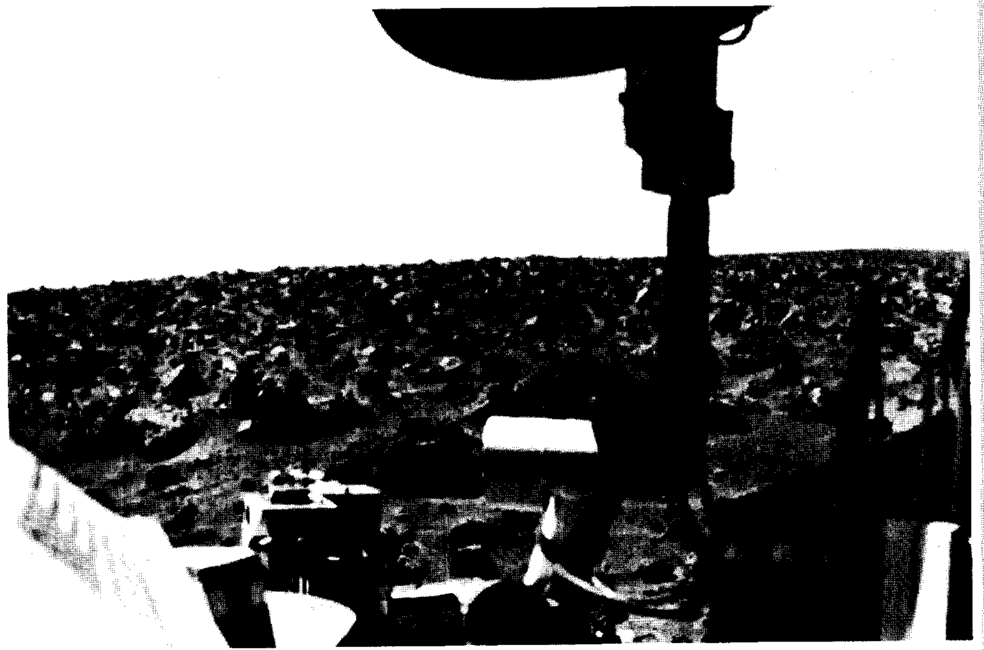


Figure 4. Beam Lead Mesa PIN Switching Time. For the beam lead mesa PIN in shunt to switch from an isolation state with forward bias of 10 mA to an insertion loss state with reverse bias of −10V less than 1 ns is required.

High Reliability Tested Products



High Reliability
PIN and Schottky Diodes Selection Guide

Commercial Part Number 5082-	Military Approved JAN/JANTX/JANTXV*	Page Number
2800	1N5711	219
2810	1N5712	221
3039	1N5719	223

*JANTXV approval does not apply to the 1N5719.

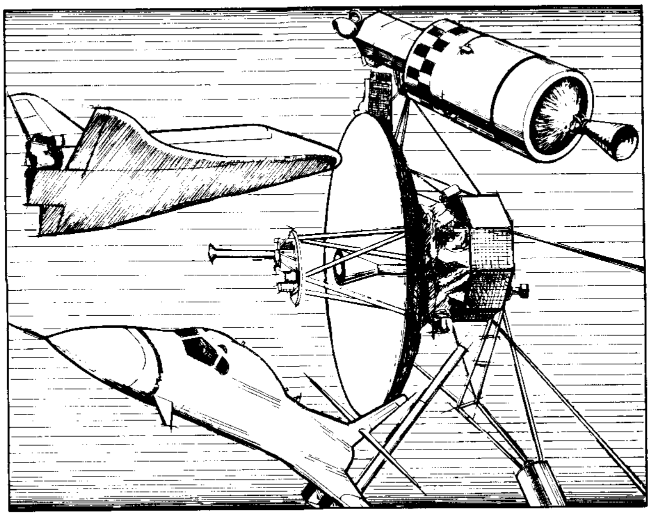
HEWLETT hp PACKARD
COMPONENTS

SCHOTTKY SWITCHING DIODE MILITARY APPROVED MIL-S-19500/444

JAN 1N5711
JANTX 1N5711
JANTXV 1N5711

Features

HIGH BREAKDOWN VOLTAGE
PICO-SECOND SWITCHING SPEED
LOW TURN-ON



Description/Applications

The JAN Series 1N5711 is an epitaxial, planar passivated Schottky Barrier Diode designed to have pico-second switching speed. These devices are well suited for high level detecting, mixing, switching, gating and converting, video detecting, frequency discriminating, sampling, and wave shaping applications that require the high reliability of a JAN/JANTX device.

Maximum Ratings at $T_{CASE}=25°C$

Operating and Storage Temperature Range .... -65°C to 200°C

Operation of these devices within the recommended temperature limits will assure a device Mean Time to Failure (MTTF) of approximately 1×10^7 hours.

Reverse Voltage (Working) .... 50 V (peak)

Power Dissipation .... 250 mW

Derate at 1.43 mW/°C for T_{CASE} = 25°C to 200°C; assumes an infinite heat sink.

Electrical Specifications at $T_A=25°C$ (Unless Otherwise Specified)

(Per Table I, Group A Testing of MIL-S-19500/444)

Specification	Symbol	Min.	Max.	Units	Test Conditions
Breakdown Voltage	V_{BR}	70	–	V	$I_R = 10\mu A$
Forward Voltage	V_{F1}	–	.41	V	$I_{F1} = 1mA$
Forward Voltage	V_{F2}	–	1.0	V	$I_{F2} = 15mA$
Reverse Leakage Current	I_R	–	200	nA	$V_R = 50V$
Reverse Leakage Current	I_R	–	200	μA	$V_R = 50V$, $T_A = +150°C$
Capacitance	$C_{T(o)}$	–	2.0	pF	$V_R = 0V$ and f = 1 MHz
Effective Minority Carrier Lifetime	τ	–	100	pS	$I_F = 5mA$ Krakauer Method [Note 1]

Note 1: Per DESC drawing C-68001

JAN 1N5711: Samples of each lot are subjected to Group A inspection for parameters listed in Table I, and to Group B and Group C tests listed below. All tests are to the conditions and limits specified by MIL-S-19500/444.

JANTX 1N5711: Devices undergo 100% screening tests as listed below to the conditions and limits specified by MIL-S-19500/444. A sample of the JANTX lot is then subjected to Group A, Group B, and Group C tests as for the JAN 1N5711 above.

JANTXV 1N5711: Devices are subject to 100% visual inspection in accordance with MIL-S-19500/444 prior to being subjected to TX screening.

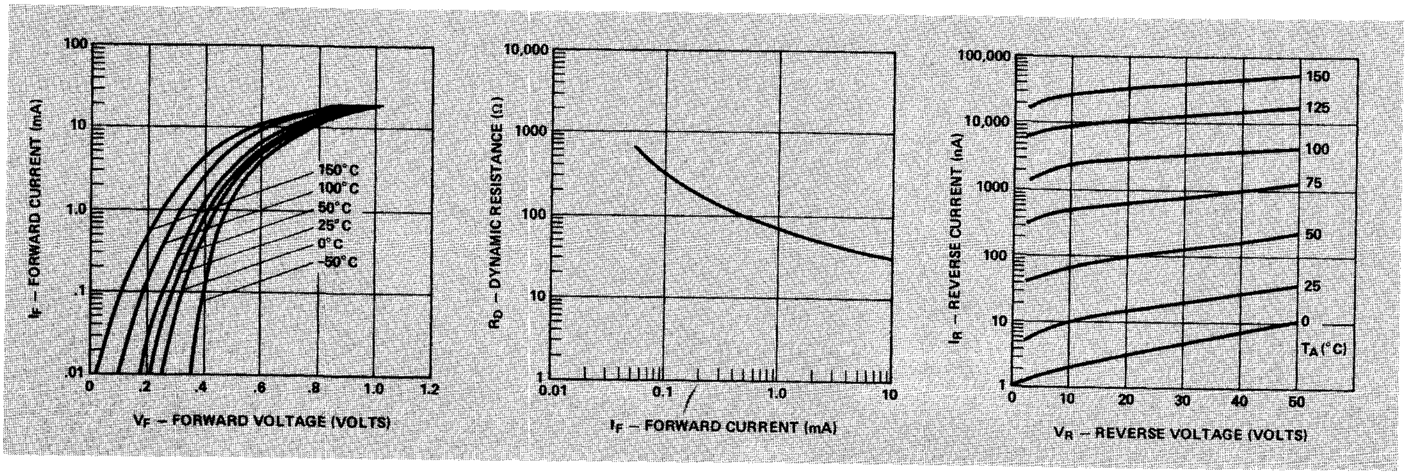
Group B Sample Acceptance Tests**	Method MIL-STD-750
Physical Dimensions	2066
Solderability	2026
Temperature Cycling	1051C
Thermal Shock (Strain)	1056A
Terminal Strength: Tension	2036A
Gross Leak Test	1071E
Moisture Resistance	1021
Mechanical Shock	2016
Vibration, Variable Frequency	2056
Constant Acceleration	2006
Terminal Strength: Lead Fatigue	2036E
Temperature Storage (200°C, 1K hrs.)	1031
Operating Life I_o = 33mAdc, V_r = 50V [pk] (f = 60Hz, T_A = 25°C, t = 1K hrs.)	1026

Group C Sample Acceptance Tests**	Method MIL-STD-750
Low Temp. Operation (−65°C)	
Forward Voltage	4011
Breakdown Voltage	4021
Salt Atmosphere	1041
Resistance to Solvents	*
Temperature Cycling	1051C
TX Screening (100%)	
High Temp. Storage (200°C, 48 hrs.)	1032
Thermal Shock	1051C
Constant Acceleration	2006
Fine Leak	1071G or H
Gross Leak	1071E
Burn-In I_o = 33mAdc, V = 50V [pk] (T_A = 25°C, f = 60Hz, t = 96hrs)	
Evaluation of Drift (I_R, V_F)	

*MIL-STD-202, Method 215

**Endpoint measurements and examinations per MIL-S-19500/444.

Typical Parameters



HEWLETT PACKARD
COMPONENTS

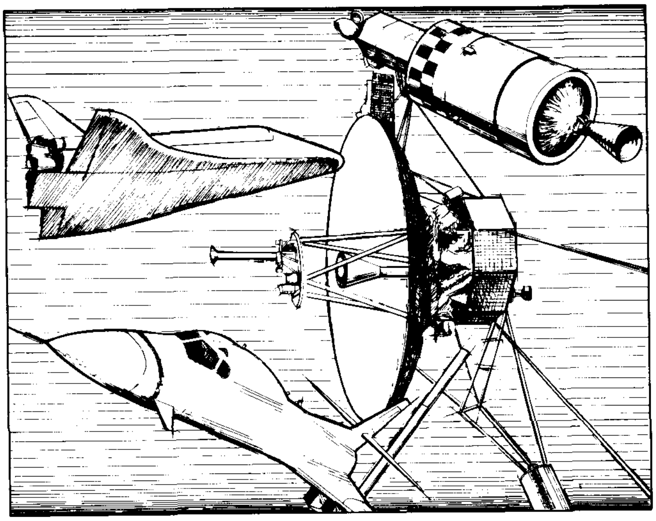
SCHOTTKY SWITCHING DIODE MILITARY APPROVED MIL-S-19500/445

JAN 1N5712
JANTX 1N5712
JANTXV 1N5712

Features

PICO-SECOND SWITCHING SPEED

LOW TURN-ON VOLTAGE



Description/Applications

The JAN Series 1N5712 is an epitaxial, planar passivated Schottky Barrier Diode designed to have pico-second switching speed. These devices are well suited for high level detecting, mixing, switching, gating, A-D converting, video detecting, frequency discriminating sampling and wave shaping applications that require the high reliability of a JAN/JANTX device.

Maximum Ratings at $T_{CASE}=25°C$

Operating and Storage Temperature
Range .... -65°C to 200°C

Operation of these devices within the recommended temperature limits will assure a device Mean Time to Failure (MTTF) of approximately 1 x 10^7 hours.

Reverse Voltage (Working) .... 16V (peak)
Power Dissipation .... 250 mW
Derate at 1.43 mW/°C for T_{CASE} = 25°C to 200°C; assumes an infinite heat sink.

Electrical Specifications at $T_A=25°C$

(Per Table I, Group A Testing of MIL-S-19500/445)

Specification	Symbol	Min.	Max.	Units	Test Conditions
Breakdown Voltage	V_{BR}	20		V	$I_R = 10\mu A$
Forward Voltage	V_{F1}		.55	V	I_{F1} = 1 mA
Forward Voltage	V_{F2}		1.0	V	I_{F2} = 35 mA
Reverse Leakage Current	I_R		150	nA	V_R = 16 V
Capacitance	$C_{T(o)}$		1.2	pF	V_R = 0V and f = 1 MHz
Effective Minority Carrier Lifetime	τ		100	pS	I_F = 5 mA Krakauer Method [Note 1]

Note 1: Per DESC drawing C-68001

JAN 1N5712: Samples of each lot are subjected to Group A inspection for parameters listed in Table I, and to Group B and Group C tests listed below. All tests are to the conditions and limits specified by MIL-S-19500/445.

JANTX 1N5712: Devices undergo 100% screening tests as listed below to the conditions and limits specified by MIL-S-19500/445. A sample of the JANTX lot is then subjected to Group A, Group B, and Group C tests as for the JAN 1N5712 above.

JANTXV 1N5712: Devices are subject to 100% visual inspection in accordance with MIL-S-19500/445 prior to being subjected to TX screening.

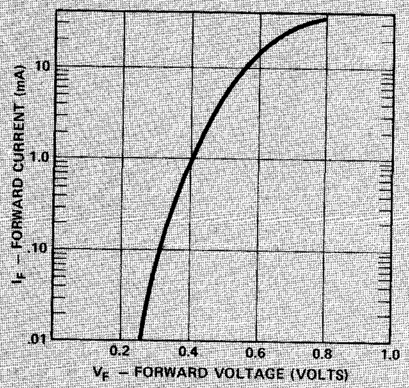
Group B Sample Acceptance Tests **	Method MIL-STD-750
Physical Dimensions	2066
Solderability	2026
Temperature Cycling	1051C
Thermal Shock (Strain)	1056A
Terminal Strength: Tension	2036A
Gross Leak Test	1071E
Moisture Resistance	1021
Mechanical Shock	2016
Vibration, Variable Frequency	2056
Constant Acceleration	2006
Terminal Strength: Lead Fatigue	2036E
Temperature Storage (200°C, 1K hrs.)	1031
Operating Life $I_o = 33$mAdc, $V_r = 16$V [pk] (f = 60Hz, $T_A = 25^\circ$C, t = 1K hrs.)	1026

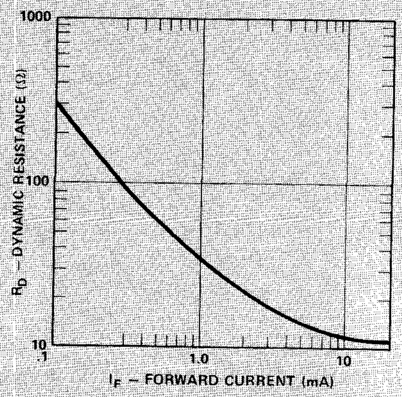
Group C Sample Acceptance Tests **	Method MIL-STD-750
Low Temp. Operation (−65°C)	
Forward Voltage	4011
Reverse Breakdown Voltage	4021
Salt Atmosphere	1041
Resistance to Solvents	*
Temperature Cycling	1051C
TX Screening (100%)	
High Temp. Storage (200°C, 48 hrs.)	1032
Thermal Shock	1051C
Constant Acceleration	2006
Fine Leak	1071G or H
Gross Leak	1071E
Burn-In $I_o = 33$mAdc, V = 16V [pk] (T_A=25°C, f=60 Hz, t=96 hrs.)	
Evaluation of Drift (I_R, V_F)	

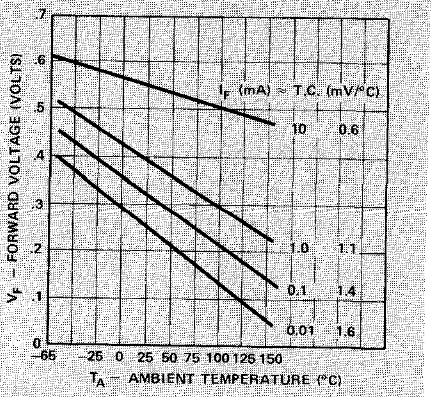
*MIL-STD-202, Method 215

**Subgroup endpoint measurements and examinations per MIL-S-19500/445.

Typical Parameters







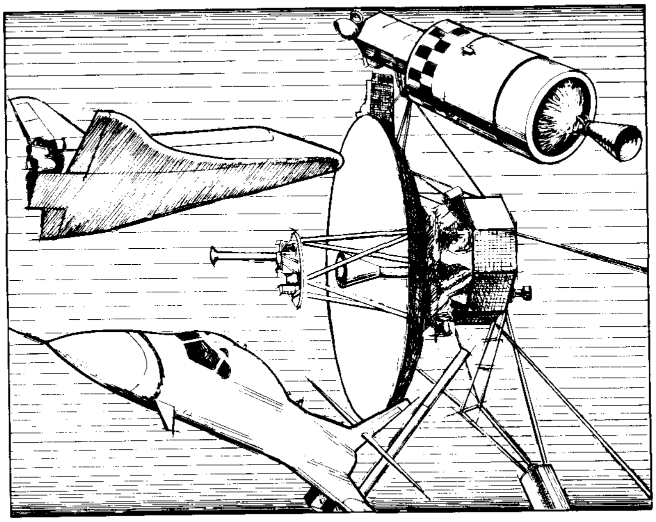
HEWLETT hp PACKARD
COMPONENTS

PIN SWITCHING DIODE MILITARY APPROVED MIL-S-19500/443

JAN 1N5719
JANTX 1N5719

Features

LARGE DYNAMIC RANGE
LOW HARMONIC DISTORTION
HIGH SERIES ISOLATION



Description/Applications

The JAN Series 1N5719 is a planar passivated silicon PIN diode designed for use in RF switching circuits. These devices are well suited for variable attenuator, AGC, modulator, limiter, and phase shifter applications that require the high reliability of a JAN/JANTX device.

Maximum Ratings at $T_{CASE} = 25°C$

Operating and Storage Temperature Range .... -65°C to +150°C

Operation of these devices within the recommended temperature limits will assure a device Mean Time to Failure (MTTF) of approximately 1×10^7 hours.

Reverse Voltage (Working)	100 V dc
Reverse Voltage (non-rep)	150 V pk
Power Dissipation [At 25°C]	250 mW

Derate at 2.0 mW/°C above $T_{CASE} = 25°C$; assumes an infinite heat sink.

Electrical Specifications at $T_A = 25°C$

(Per Table I, Group A Testing of MIL-S-19500/443)

Specification	Symbol	Min.	Max.	Units	Test Conditions
Breakdown Voltage	V_{BR}	150		V	$I_R = 10 \mu A$
Forward Voltage	V_F		1.0	V	$I_F = 100 mA$
Reverse Current	I_R		250	nA	$V_R = 100V$
Reverse Current	I_R		15	µA	$V_R = 100V$, $T_A = 150°C$
Capacitance	C_{VR}		.30	pF	$V_R = 100V$, f = 1 MHz
Series Resistance	R_S		1.25	Ω	$I_F = 100 mA$, f = 100 MHz
Effective Carrier Lifetime	τ	100		ns	$I_F = 50 mA$, $I_R = 250 mA$

JAN 1N5719: Samples of each lot are subjected to Group A inspection for parameters listed in Table I, and to Group B and Group C tests listed below. All tests are to the conditions and limits specified by MIL-S-19500/443.

JANTX 1N5719: Devices undergo 100% screening tests as listed below to the conditions and limits specified by MIL-S-19500/443. A sample of the JANTX lot is then subjected to Group A, Group B, and Group C tests as for the JAN 1N5719 above.

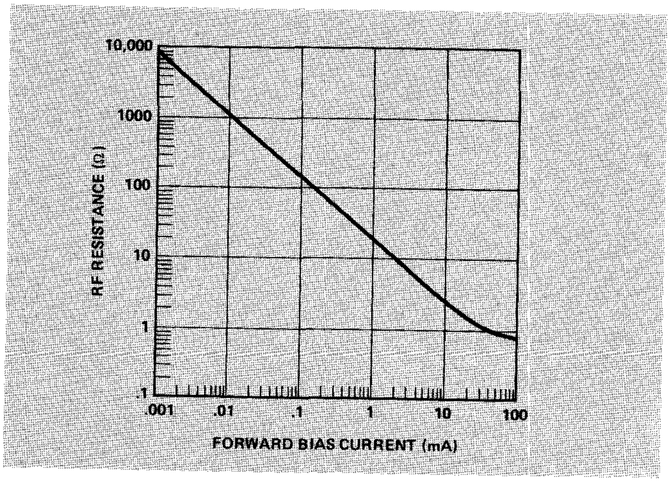
Group B Sample Acceptance Tests **	Method MIL-STD-750
Physical Dimensions	2066
Solderability	2026
Temperature Cycling	1051F
Thermal Shock (Strain)	1056A
Terminal Strength: Tension	2036A
Hermetic Seal	1071E
Moisture Resistance	1021
Mechanical Shock	2016
Vibration, Variable Frequency	2056
Constant Acceleration	2006
Terminal Strength: Lead Fatigue	2036E
Salt Atmosphere	1041
Temperature Storage ($T_A = 150°C$, t = 1k hrs.)	1031
Operating Life ($I_o = 70$mAdc, $V_R = 120$V [pk], f = 60Hz, $T_A = 25°C$, t = 1k hrs.)	1026

Group C Sample Acceptance Tests **	Method MIL-STD-750
Barometric Pressure	1001
Reverse Current	4016
Salt Atmosphere	1041
Resistance to Solvents	*
Temperature Cycling	1051F
Low Temperature Operation (−65°C)	
Forward Voltage	4011
Breakdown Voltage	4021
TX Screening (100%)	
High Temp Storage (150°C, 48 hrs.)	1032
Temperature Cycling	1051F
Constant Acceleration	2006
Fine Leak	1071 G or H
Gross Leak	1071E
Burn-in ($I_o = 70$mAdc, $V_R = 120$V [pk], $T_A = 25°C$, f = 60Hz, t = 96 hrs.)	
Evaluation of Drift (I_R, V_F)	

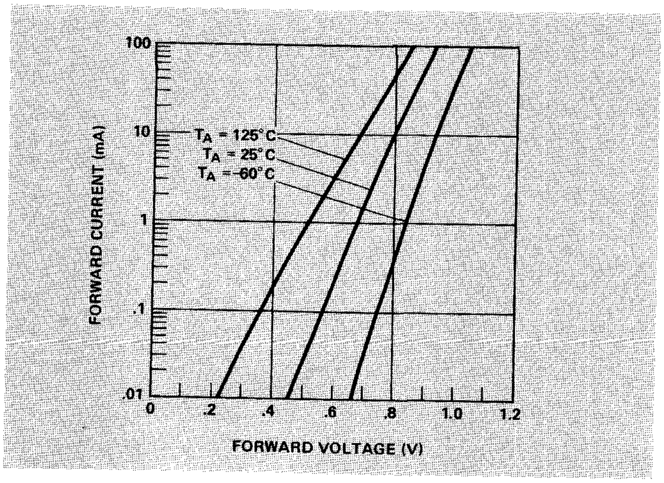
*MIL-STD-202, Method 215

**Subgroup endpoints and measurements per MIL-S-19500/443.

Typical Parameters



Typical RF Resistance vs. Forward Bias Current.



Typical Forward Current vs. Forward Voltage.

HEWLETT PACKARD

COMPONENTS

STANDARD HIGH RELIABILITY TEST PROGRAMS

Description

In addition to military qualified (JAN/JANTX) Schottky barrier and PIN diodes, Hewlett-Packard offers a line of standard high reliability test programs for most of our commercial devices. These programs are patterned after MIL-S-19500 and are designed to:

1. Eliminate the costly requirement of generating High-Rel specifications, and
2. Offer off-the-shelf delivery for many High-Rel devices.
3. Aid in writing High-Rel specifications, if required.

Three basic levels of High-Rel testing are offered on our diodes, bipolar transistors, and GaAs FETs.

1. The TX prefix indicates a part that is preconditioned and screened to a program similar to that shown in Table II. (Table V for chips and beam leads)
2. The TXB prefix identifies a part that is preconditioned and screened to TX level with a Group B quality conformance test as shown in Table IV. (Table VI for chips and beam leads)
3. The TXV and TXVB prefix indicates that an internal visual is included as part of the preconditioning and screening.

From these three basic levels, several combinations are available. Please refer to Table I as a guide.

Detailed Specification Sheets are available for all devices in the program. Standard high reliability GaAs FET products are represented following Table VI of this section. Please contact your local HP sales office for additional information.

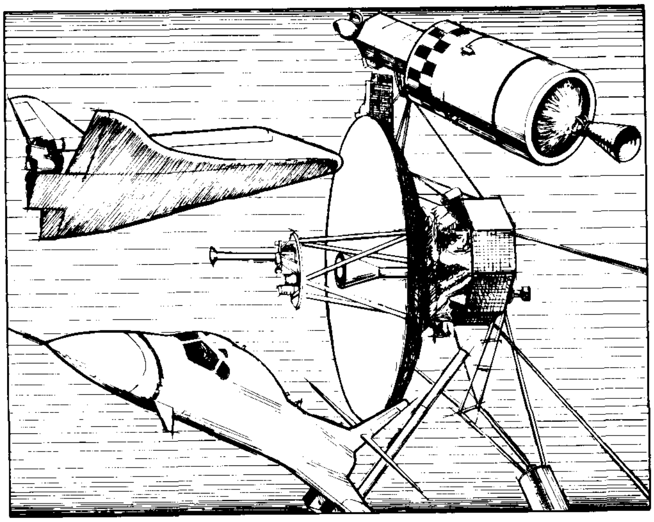


Table I. Hi-Rel Test Levels. RFQ Information, Examples:

Inspection Level	Diode with 5082 Prefix	Diode with HSCH Prefix	Diode with HPND Prefix	Transistor with HXTR Prefix
Commercial	5082-3080	HSCH-3486	HPND-4165	HXTR-2101
100% Screen	TX3080	TXS3486	TXP4165	TXT2101
100% Screen and Group B	TXB3080	TXBS3486	TXBP4165	TXBT2101
100% Screen and Visual	TXV3080	TXVS3486	TXVP4165	TXVT2101
100% Screen and Visual and Group B	TXVB3080	TXVBS3486	TXVBP4165	TXVBT2101

Table II. Typical 100% Screening Program for Packaged Devices[1]

Screening Test/Inspection	MIL-STD-750 Method (except as noted)	Conditions[2]
1. Internal Visual Inspection (TXV, TXVB options only)	2074 (Glass Body) 2072 (Other)	
2. High Temperature Life (Non-Operating)	1032	48 Hours Min. at T_{STG} (Max.)
3. Temperature Cycle	MIL-STD-883, Method 1010	10 Cycles, T_{STG} (Min.) to T_{STG} (Max.), 30 Min. per Cycle. Delete para 3.1.
4. Constant Acceleration	2006	20,000G, Y_1 Axis
5. Hermetic Seal, Fine Leak	1071	G or H
6. Hermetic Seal, Gross Leak	1071	A or C, Step 1 Only
7. Burn-In (HTRB)	1038	PIN and SRD only. 48 Hours Min., 80% V_{BR}, $T_C \geq 100°C$
8. Serialization	—	
9. Interim Electrical Test (Delta Parameters)	—	Read and Record — Note [3]
10. Burn-In	1038	96 Hours Min., 25°C
11. Final Electrical Test	—	Same as Step 9.
12. Stability Verification	—	Note [3]
13. Percent Defective Allowable	—	Note [4]
14. Radiographic Inspection (Option, must be specified)	2076	

Table III. Typical Group A Inspection for Packaged Devices[1]**. Each Lot is Submitted to Group A Inspection.**

Test/Inspection	MIL-STD-750 Method	Conditions	LTPD
Subgroup 1 Visual and Mechanical	2071	—	15
Subgroup 2 DC Electrical Tests at 25°C	—	Note [2]	5
Subgroup 3 Dynamic Electrical Tests at 25°C	—	Note [2]	5

Table IV. Typical Group B Quality Conformance Inspection for Packaged Devices[1]

Test/Inspection	MIL-STD-750 Method (except as noted)	Conditions	LTPD
Subgroup 1			
Physical Dimensions	2066	—	15
Subgroup 2 (destructive)			
Solderability	2026	—	15
Resistance to Solvents	1022	Note [5]	
Subgroup 3 (destructive)			
Temperature Cycle	MIL-STD-883, 1010	10 Cycles, T_{STG} (Max.) to T_{STG} (Min.), 30 Min. per Cycle. Delete para 3.1.	10
Thermal Shock	1056	A	
Terminal Strength, Tension	2036	A	
Hermetic Seal, Fine Leak	1071	G or H	
Hermetic Seal, Gross Leak	1071	A or C, Step 1 Only	
Moisture Resistance	1021	Omit Initial Conditioning	
Visual and Mechanical Insp.	2071	—	
Electrical Test	—	Same as Table II Step 9	
Subgroup 4			
Shock	2016	Non-Operating 1500G, 0.5ms, 5 Blows Each X_1, Y_1, Z_1 (Y_1 only for glass body)	10
Vibration, Variable Frequency	2056	—	
Constant Acceleration	2006	20,000G, X_1, Y_1, Z_1,	
Electrical Test	—	Same as Table II, Step 9	
Subgroup 5 (destructive)			
Terminal Strength, Lead Fatigue	2036	E, Note [5]	15
Subgroup 6			
High Temperature Life (Non-Operating)	1032	Same as Table II, Step 2. 340 Hours Min.	5
Electrical Test	—	Same as Table II, Step 9	
Subgroup 7			
Steady State Operation Life	1027	Same as Table II, Step 10. 340 Hours Min.	5
Electrical Test	—	Same as Table II, Step 9	

Table V. Typical 100% Screening Program for Chips and Beam Leads

Screening Test/Inspection	MIL-STD-750 Method	Conditions[2]
1. Electrical Test	—	
2. Visual Inspection	2073 (Chips) HP Spec A5956-0112-72 (Beam Leads)	

Table VI. Typical Group B Lot Acceptance Test for Chips and Beam Leads

Test/Inspection	MIL-STD-750 Method (except as noted)	Conditions[2]	LTPD
1. Assemble Samples in Carrier[6]	—	—	—
2. Electrical Test (Go/No Go)	—	—	100%
3. High Temperature Life (Non-Operating)	1032	48 Hours Min. at T_{STG} (Max.)	100%
4. Temperature Cycle	MIL-STD-883, Method 1010	10 Cycles, T_{STG} (Min.) to T_{STG} (Max.), 30 Min. per Cycle. Delete para 3.1.	100%
5. Burn-In (HTRB)	1038	PIN and SRD Only. 48 Hours Min., 80% V_{BR}, $T_C \geq 100°C$	100%
6. Serialization	—	—	—
7. Interim Electrical Test (Delta Parameters)	—	Read and Record — Note [3]	100%
8a. Burn-In	1038	168 Hours Min., 25°C	10
8b. Final Electrical Test	—	Same as Step 7	
8c. Stability Verification	—	Note [3]	

NOTES:

1. Recommended for devices in the following HP package outlines:
   Glass Body — 11, 15, 12 (delete steps 1, 5, 6 for outline 12).
   Other Coaxial Leaded Bodies — 31, 38, 40, 41, 44, 46, 49, 56, 62, 64, 65
   Stripline/Microstrip Body — C2, C4, E1, H2, H4, 60 (Delete Steps 4-6 for outlines C2, C4, E1)
2. For detailed information on test conditions please request a Hi-Rel specification sheet for the specific product required.
3. Delta Parameters. V_F and C_T are normally chosen for pulse sensitive microwave Schottky diodes. V_F and I_R are normally chosen for PIN, SRD, IMPATT and other Schottky diodes. Δ limits will depend on device type and characteristics.
4. PDA = 15% for pulse sensitive microwave Schottky diodes. PDA = 10% for PIN, SRD and other Schottky diodes.
5. Only applicable for glass body devices.
6. Chips: Outlines 15 (glass body) or 31 (ceramic coaxial lead) Beam Leads: Outline H2 or H4 (stripline).

HEWLETT hp PACKARD
COMPONENTS

HIGH RELIABILITY MICROWAVE GaAs FETs

NEW

2N6680 TXV
2N6680 TXVB
TXVF-1102
TXVBF-1102

Description

Hewlett-Packard has developed a cost-effective standard test program designed to provide stabilized Gallium Arsenide FETs for applications requiring high-reliability performance. These products are based upon the standard 2N6680 (HFET-1101) and HFET-1102. The preconditioning and screening program for the 2N6680 TXV and the TXVF-1102 is shown in Table I. The 2N6680 TXVB and the TXVBF-1102 are parts which have been preconditioned and screened per Table I and come from a lot which has passed the Group B tests detailed in Table II.

Hewlett-Packard is capable of executing alternative programs based upon individual customer's specifications.

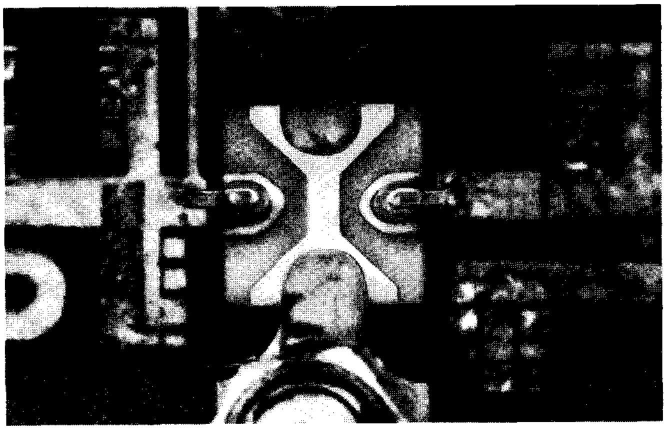
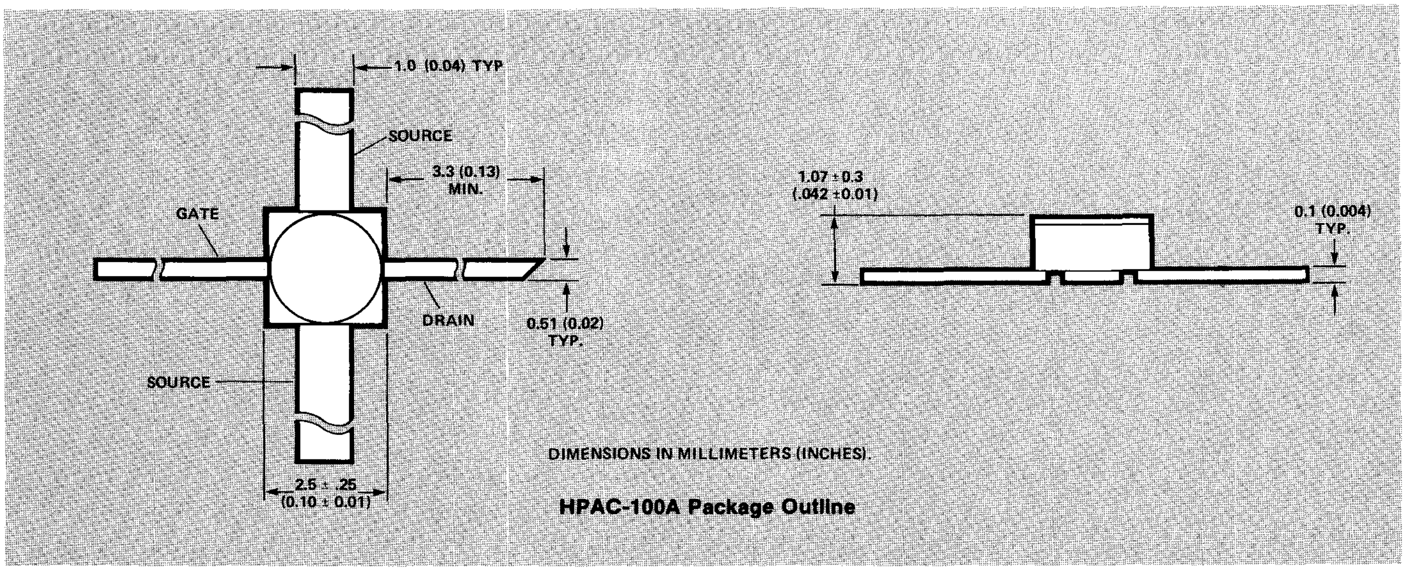


TABLE I
PRECONDITIONING AND SCREENING (100%)

	Examination or Test	**MIL-STD-750 Method**	**Step Conditions**
1.	Internal Visual	—	Per HP MSD Procedure A-5956-2150-72
2.	High Temperature Storage	1032	T_A = 125° C; t = 48 Hours Minimum
3.	Temperature Cycling	1051	Condition B, T_A = -65° C to +125° C, Ten (10) Cycles
4.	Constant Acceleration	2006	20,000G, Y_1 Axis
5.	Fine Leak	1071	Condition G or H: 60.0 psig, 4 Hours Soak in He; 5.0 x 10^{-8} cc-atm/sec.
6.	Gross Leak	1071	Condition A, C or E
7.	Pre Burn-In Electrical Test		I_{DSS}*, g_m*, V_{GSP}*, I_{GSS}
8.	Burn-In	1039	Condition B, T_A = 110° C, t = 240 Hours; T_{CH} = +125° C; V_{DS} = 5.0Vdc
9.	Post Burn-In Electrical Test		I_{DSS}*, g_m*, V_{GSP}*, I_{GSS}
10.	Burn-In Drift Evaluation Calculated from: 72 Hours to 240 Hours		$\Delta I_{DSS} = \pm 15\%$ $\Delta g_m = \pm 15\%$ $\Delta V_{GSP} = \pm 15\%$ ΔI_{GSS} = +250nAdc or +250%, whichever is greater
11.	Percent Defective Calculation		Combining Parameter Limits and Specified Drift, Allow 10.0% Max. Over Burn-in; Resubmit, Permitting Additional 5% if Lot Fails
12.	Group A Testing		
12.1	Visual Examination	2071	a) Marking: Per Data Sheet b) Package Exterior } LTPD = 10
12.2	Electrical Test*		100%. Noise; Gain

*Electrical specifications per HFET-1101/1102 data sheets (Publication numbers 5952-9836 and 5952-9857).



DIMENSIONS IN MILLIMETERS (INCHES).

HPAC-100A Package Outline

TABLE II
2N6680 TXV AND TXVBF-1102 GROUP B TESTING PER MIL-S-19500

Examination or Test	MIL-STD-750 Test Method	Environmental Conditions	LTPD
SUBGROUP 1:			20
Physical Dimensions	2066	—	
SUBGROUP 2:			10
Solderability	2026	250° C, Ten (10) sec. Max.	
Thermal Shock	1051	Condition B, Ten (10) Cycles, $T_A = -65°C$ to $+125°C$	
Hermetic Seal, Fine Leak	1071	Condition G or H, 5×10^{-8} cc-atm/sec., 60 psig, 4 Hrs.	
Hermetic Seal, Gross Leak	1071	Condition A, C or E	
Moisture Resistance	1021	Omit Initial Conditioning	
Endpoints: I_{DSS}*, g_m*, V_{GSP}*, I_{GSS}			
SUBGROUP 3:			10
Mechanical Shock	2016	1500G; 0.5msec; 5 Blows in Each of X_1, Y_1, Y_2 Axis	
Constant Acceleration	2006	20,000G; X_1, Y_1, Y_2	
Vibration Variable Frequency	2056		
Endpoints (per Subgroup 2)			
SUBGROUP 4:			20
Terminal Strength	2036	Condition E, 3.0 ozs. Max.	
SUBGROUP 5:			λ = 15
High Temperature Life	1031	$T_A = +125°C$	
Endpoints (per Subgroup 2)			
SUBGROUP 6:			λ = 15
Operating Life	1026	$T_A = +110°C$; $T_{CH} = +125°C$ $V_{DS} = +5Vdc$	
Endpoints (per Subgroup 2)			

*Electrical specifications per HFET-1101/1102 data sheets (Publication numbers 5952-9836 and 5952-9857).

HEWLETT PACKARD
COMPONENTS

NEW

HIGH RELIABILITY MICROWAVE GaAs FETs

TXVF-2201
TXVBF-2201

Description

Hewlett-Packard has developed a cost-effective standard test program designed to provide stabilized Gallium Arsenide FETs for applications requiring high-reliability performance. These products are based upon the standard HFET-2201. The preconditioning and screening program for the TXVF-2201 is shown in Table I. The TXVBF-2201 represents parts which have been preconditioned and screened per Table I and come from a lot which has passed the Group B tests detailed in Table II.

Hewlett-Packard is capable of executing alternative programs based upon individual customer's specifications.

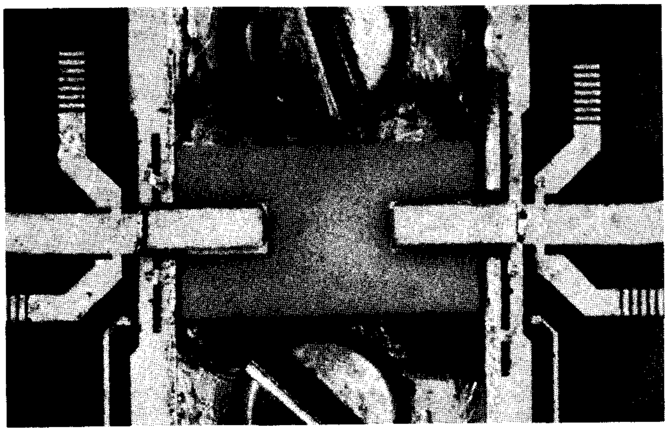
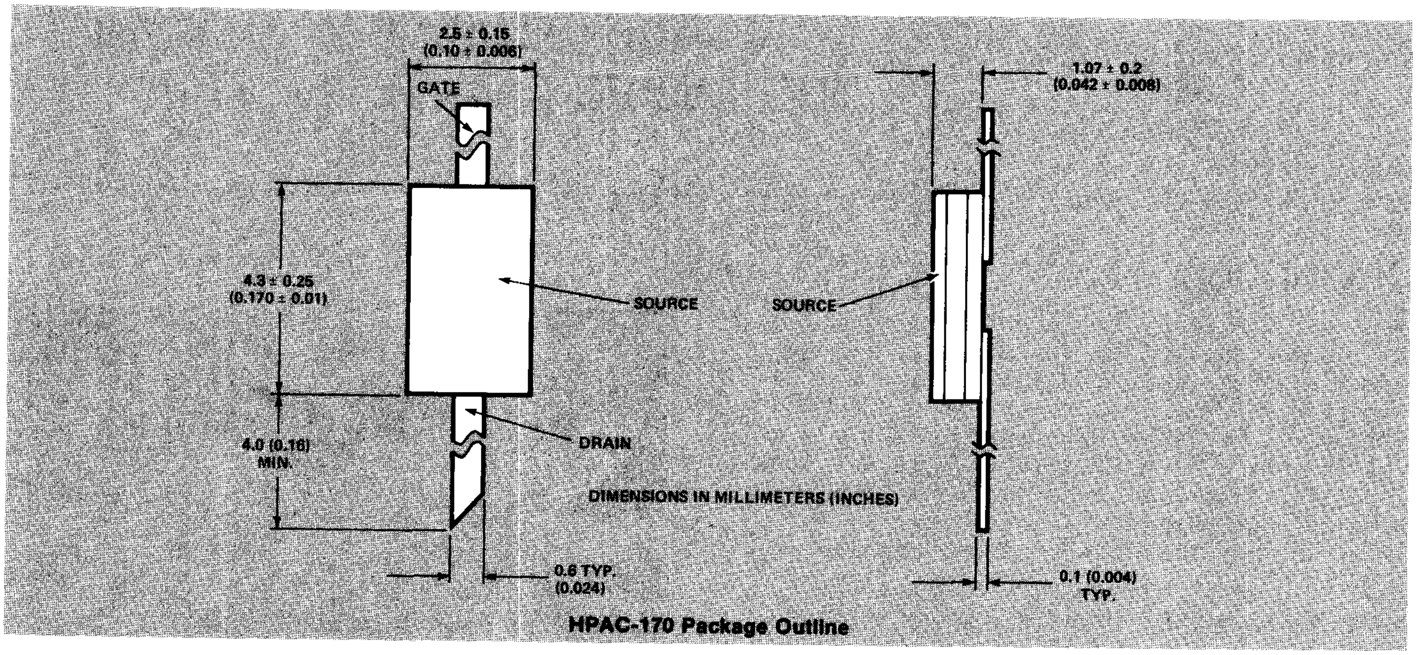


TABLE I
PRECONDITIONING AND SCREENING (100%)

	Examination or Test	MIL-STD-750 Test Method	Step Conditions
1.	Internal Visual	—	Per HP MSD Procedure A-5956-2150-72
2.	High Temperature Storage	1032	$T_A = 125°C$; $t = 48$ Hours Minimum
3.	Temperature Cycling	1051	Condition B, $T_A = -65°C$ to $+125°C$, Ten (10) Cycles
4.	Constant Acceleration	2006	20,000G, Y_1 Axis
5.	Fine Leak	1071	Condition G or H: 60.0 psig, 4 Hours Soak in He; 5×10^{-8} cc-atm/sec.
6.	Gross Leak	1071	Condition A, C or E
7.	Pre Burn-In Electrical Test		I_{DSS}*, g_m*, V_{GSP}*, I_{GSS}
8.	Burn-In	1039	Condition B, $T_A = 110°C$, $t = 240$ Hours; $T_{CH} = +125°C$; $V_{DS} = 4.0$ Vdc
9.	Post Burn-In Electrical Test		I_{DSS}*, g_m*, V_{GSP}*, I_{GSS}
10.	Burn-In Drift Evaluation Calculated from: 72 Hours to 240 Hours		$\Delta I_{DSS} = \pm 15\%$ $\Delta g_m = \pm 15\%$ $\Delta V_{GSP} = \pm 15\%$ $\Delta I_{GSS} = +250$nAdc or $+250\%$, whichever is greater
11.	Percent Defective Calculation		Combining Parameter Limits and Specified Drift, Allow 10.0% Max. Over Burn-in; Resubmit, Permitting Additional 5% if Lot Fails
12.	Group A Testing		
12.1	Visual Examination	2071	a) Marking: Per Data Sheet b) Package Exterior } LTPD = 10
12.2	Electrical Test*		100%, Noise; Gain

*Electrical specifications per HFET-2201 data sheet (Publication number 5952-9866).



HPAC-170 Package Outline

TABLE II
TXVBF-2201 GROUP B TESTING PER MIL-S-19500

Examination or Test	MIL-STD-750 Test Method	Environmental Conditions	LTPD
SUBGROUP 1:			20
Physical Dimensions	2066	—	
SUBGROUP 2:			10
Solderability	2026	250°C, Ten (10) sec. Max.	
Thermal Shock	1051	Condition B, Ten (10) Cycles, $T_A = -65°C$ to $+125°C$	
Hermetic Seal, Fine Leak	1071	Condition G or H, 5×10^{-8} cc-atm/sec., 60 psig, 4 Hours	
Hermetic Seal, Gross Leak	1071	Condition A, C or E	
Moisture Resistance	1021	Omit Initial Conditioning	
Endpoints: I_{DSS}*, g_m*, V_{GSP}*, I_{GSS}			
SUBGROUP 3:			10
Mechanical Shock	2016	1500G; 0.5msec; 5 Blows in Each of X_1, Y_1, Y_2 Axis	
Constant Acceleration	2006	20,000G; X_1, Y_1, Y_2	
Vibration Variable Frequency	2056		
Endpoints (per Subgroup 2)			
SUBGROUP 4:			20
Terminal Strength	2036	Condition E, 3.0 ozs. Max.	
SUBGROUP 5:**			$\lambda = 15$
High Temperature Life	1031	$T_A = +125°C$	
Endpoints (per Subgroup 2)			
SUBGROUP 6:**			$\lambda = 15$
Operating Life	1026	$T_A = +110°C$; $T_{CH} = +125°C$ $V_{DS} = +4.0$ Vdc	
Endpoints (per Subgroup 2)			

*Electrical specifications per HFET-2201 data sheet (Publication number 5952-9866).

**Non-destructive

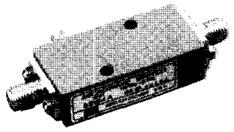
Integrated Products

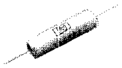
HEWLETT PACKARD
COMPONENTS

INTEGRATED PRODUCTS

SWITCHES
MODULATORS
LIMITERS
MIXERS
COMB GENERATORS

PIN DIODE SWITCHES

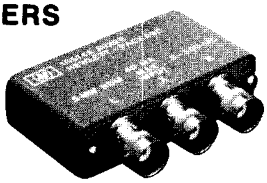


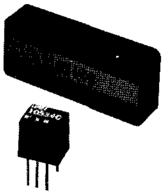


- Broadband, .1-18 GHz
- 33140 Series Optimized for Fast Switching, 5 ns
- Add-On Driver Available for 33140 Series
- 33130 Series Optimized for Low Insertion Loss
- Medium and High Isolation Units Available in Each Series
- Hermetic PIN Diode Modules

	Part Number	Min. Isolation and (Max. Insertion Loss), dB				
		1-2GHz	2-4GHz	4-8GHz	8-12GHz	12-18GHz
General Purpose	33102A 33104A	35(1.0) 65(1.0)	40(1.3) 80(1.5)	45(2.0) 80(2.1)	45(2.0) 80(2.2)	45(2.5) —
Low Loss	33132A 33134A	33(1.0) 60(1.0)	37(1.0) 80(1.4)	43(1.2) 80(1.6)	43(1.4) 80(1.8)	43(1.8) 80(2.3)
Fast Switching	33142A 33144A	30(1.0) 60(1.1)	40(1.0) 80(1.4)	45(1.5) 80(1.7)	45(1.5) 80(2.0)	45(2.5) 80(3.0)

DOUBLE BALANCED MIXERS

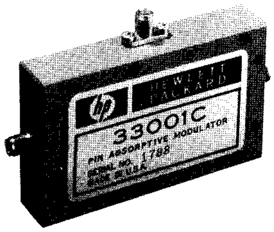




- Broadband
  10534 Series: .05-150 MHz
  10514 Series: .2-500 MHz
- Low Conversion Loss
- Low 1/f Noise, Typically Less than 100 nV per Root Hz
- High Isolation Between Ports
- Wide Range of Package Styles
  "A" Versions: BNC Jacks (Options Available)
  "B" Versions: Pins for PC Mounting
  "C" Versions: Miniature, Pins for PC Mounting
- Hermetically Sealed Schottky Diodes

Part Number	Frequency Range, MHz		Typical Conversion Loss, dB
	LO and RF	IF	
10534A 10534B 10534C	.2—35 .2—35 .05—150	DC—35 DC—35 DC—150	6.5 6.5 8.0
10514A 10514B	.5—50 .2—500	DC—50 DC—500	7.0 9.0
10514C	15—250 10—500	DC—250 DC—500	7.2 9.2

PIN ABSORPTIVE MODULATORS



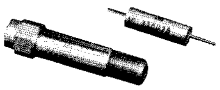
- 50Ω Match at all Attenuation Levels
- Greater than Octave Band Coverage
- 50ns Switching (10ns Available on Special Request)
- Hermetic PIN Diode Modules

Part Number	Min. Attenuation and (Max. Insertion Loss), dB					
	1-2GHz	2-4GHz	4-8GHz	8-12GHz	12-15GHz	15-18GHz
33000C 33000D	35(1.8) 65(2.0)	40(2.5) 80(3.0)	— —	— —	— —	— —
33008C 33008D	— —	— —	45(2.3) 80(2.5)	— —	— —	— —
33001C 33001D	— —	— —	— —	45(3.0) 80(3.0)	45(3.2) 80(3.5)	45(4.3) 80(4.5)

PIN DIODE LIMITERS

- Broadband, .4-12 GHz
- Low Limiting Threshold, 5mW Typical, 8-12 GHz
- Low Insertion Loss, 1.5dB Typical, 8-12 GHz
- Low Leakage, 20mW Typical, 8-12 GHz
- Hermetic PIN Diode Module
  33701A — Module
  33711A — Module with SMA Connectors

COMB GENERATORS



- 100, 250, 500 and 1000 MHz Drive Frequencies (Drive Frequencies in 50-1500 MHz Range Available on Special Request)
- Input Matched to 50Ω
- Self-biased, no External Bias Required
- Narrow Output Pulses: 130ps Pulse Width with 10V Amplitude
- Broadband Output Comb
- Hermetic Step Recovery Diode Modules

Part Number		Drive Freq., MHz	Typ. Output Power per Comb, dBm			
Comb Generator	Design Module		1-4 GHz	4-8 GHz	8-12 GHz	12-18 GHz
33002A	33002B	100	-5	-15	-25	-35
33003A	33003B	250	0	-5	-15	-30
33004A	33004B	500	+10	+5	-5	-15
33005C	33005D	1000	+10	+5	0	-5

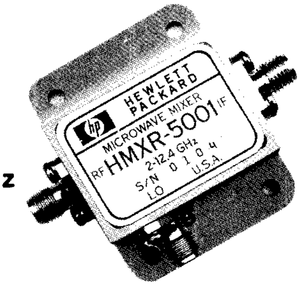
HEWLETT PACKARD
COMPONENTS

INTEGRATED PRODUCTS

MIXER
BIAS NETWORK
CATALOG

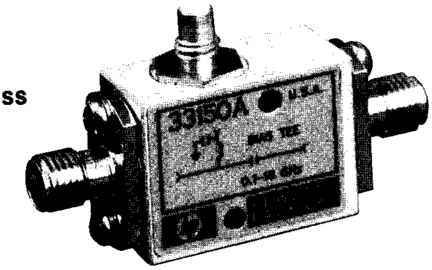
HMXR-5001 WIDEBAND DOUBLE BALANCED MIXER

- **Wideband — 2 to 12.4 GHz Usable to 18 GHz**
- **Wide IF Bandwidth 0.01 to 1.0 GHz**
- **Good Conversion Loss 7.5 dB Typical to 8 GHz 8.5 dB Typical to 12.4 GHz**
- **Excellent Isolation LO-RF: 30 dB Typical**
- **Rugged Construction**
- **Hermetically Packaged Diodes**



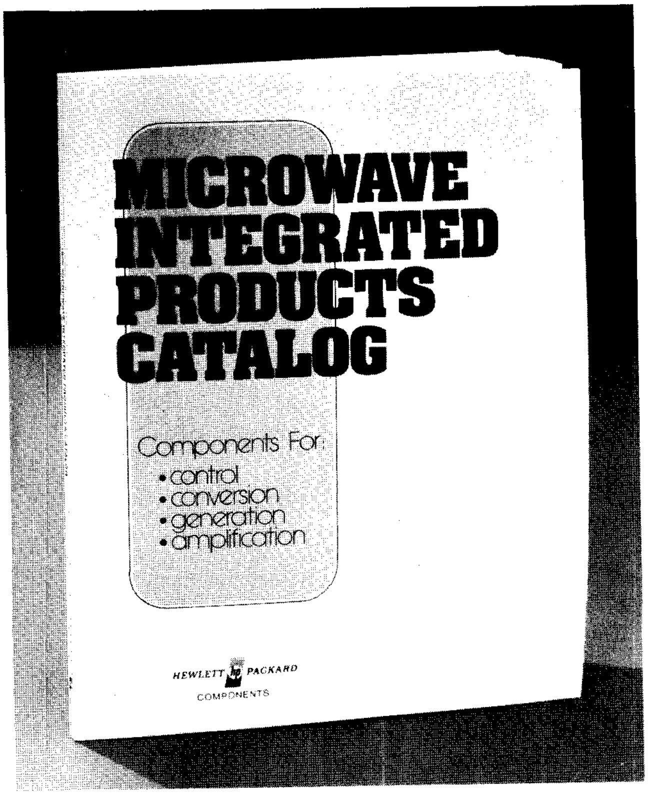
33150A MICROWAVE BIAS NETWORK 0.1-18 GHz

- **Wideband**
- **Low Insertion Loss**
- **High RF to DC Isolation**



Parameter	Frequency Range (GHz)		
	0.1-3.5	3.5-12	12-18
Maximum Insertion Loss (dB)	0.4	0.6	1.1
Maximum SWR	1.5:1	1.5:1	1.8:1
Maximum DC Bias Resistance (Ω)	4.0		

Electrical Specifications at T_{CASE} = 25° C



MICROWAVE INTEGRATED PRODUCTS CATALOG

Components For:
- control
- conversion
- generation
- amplification

HEWLETT PACKARD
COMPONENTS

Hewlett-Packard manufactures a broad line of components for the control, conversion, generation and amplification of RF and microwave signals. This designer's catalog describes our standard products and contains detailed, up-to-date specifications on our complete product lines. Special testing, screening, and electrical or mechanical modifications are available.

Integrated Production Process: Hewlett-Packard's design, manufacturing and marketing team ensures that all aspects of our production and procedures work together to bring you reliable products with known performance. They are backed by an in-house manufacturing capability that includes component fabrication, thin film circuit capabilities, MIC assembly processes, advanced assembly and test methods, and computer assisted order processing, production and shipping procedures.

For a copy of the new Microwave Integrated Products Catalog (5952-9871D) write: Inquiries Mgr., Hewlett-Packard, 1507 Page Mill Road, Palo Alto, CA 94304.

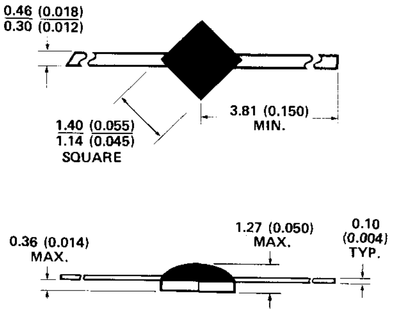
NOTES

Appendix

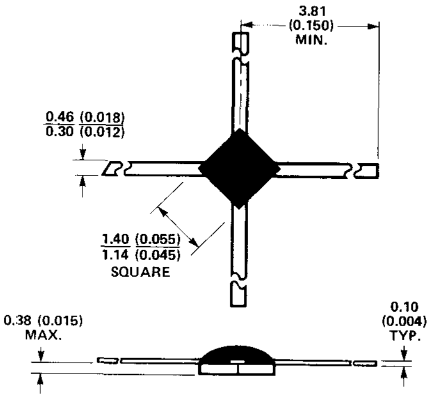
HEWLETT PACKARD COMPONENTS
An Optimum Zero Bias Schottky Detector Diode
APPLICATION BULLETIN 24
Selecting a Design Medium for the HFET-2201 GaAs Field Effect Transistor
APPLICATION NOTE 971
The HPND-4050 Beam Lead Mesa PIN in Shunt Applications
APPLICATION NOTE 967
4 GHz Transistor
HXTR-6101
APPLICATION NOTE 965
Balanced Mixer
and Applications
APPLICATION NOTE 956-6
Dependence of
Sensitivity

PACKAGE OUTLINES

All dimensions in millimeters (inches), except where noted.
For complete package specifications refer to individual product specification sheets.
Drawings are not to scale.



C2



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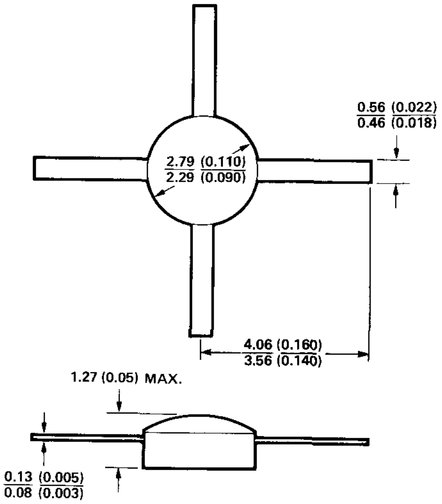
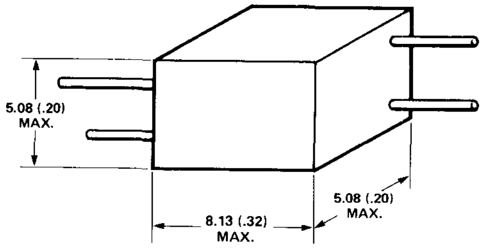
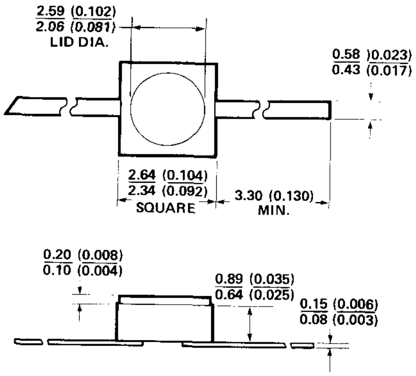


E1



LEAD LENGTH 19.05 (0.75) MIN.

G1/G2



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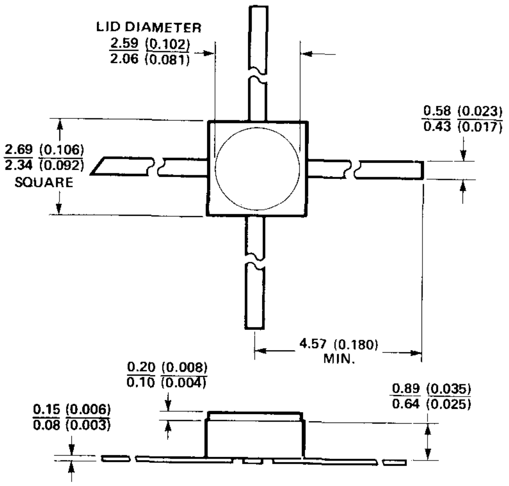

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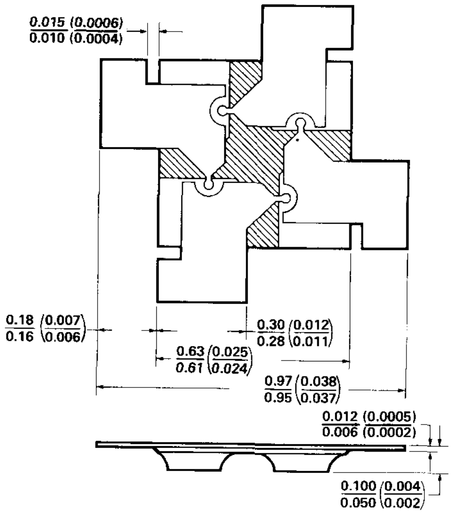
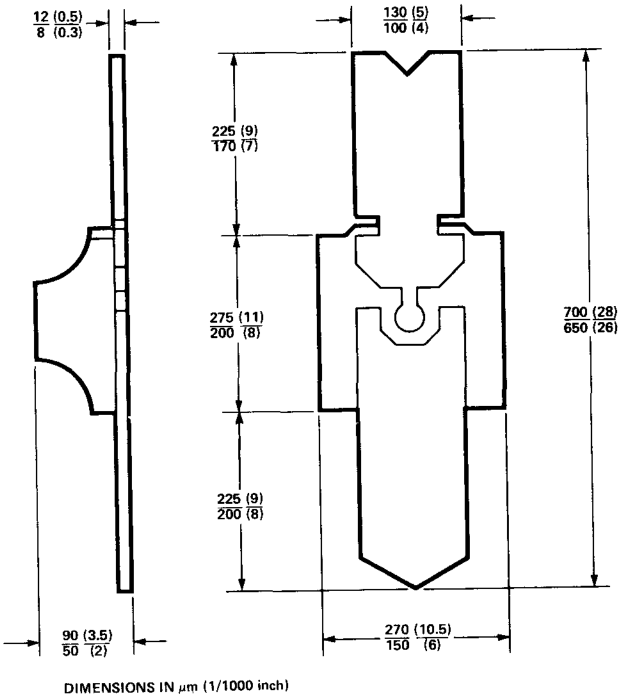
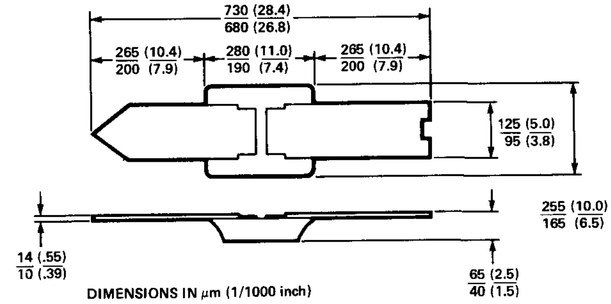


03

All dimensions in millimeters (inches), except where noted.
For complete package specifications refer to individual product specification sheets.
Drawings are not to scale.



05



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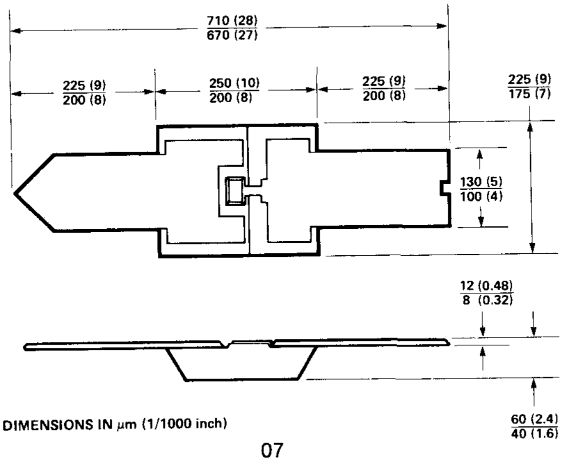

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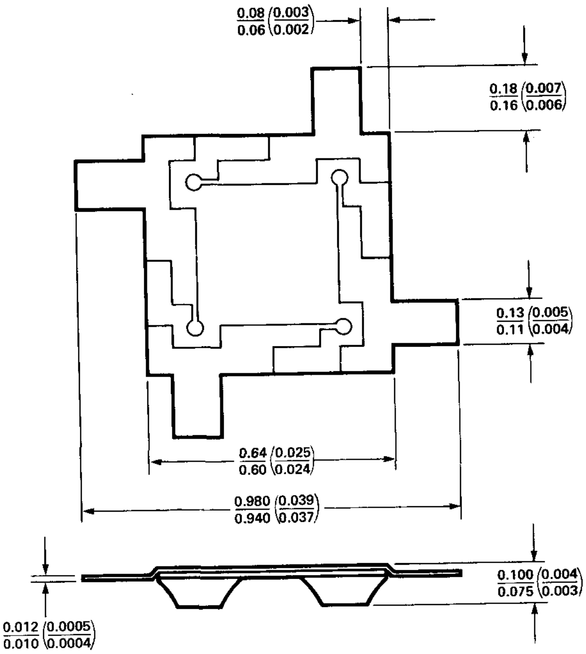

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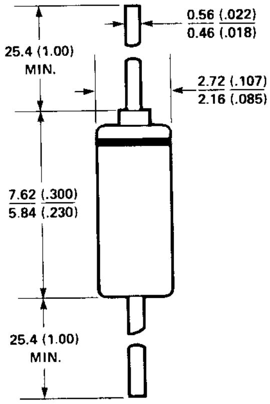

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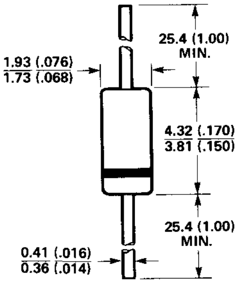

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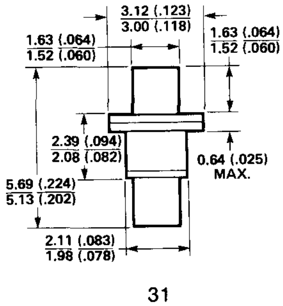

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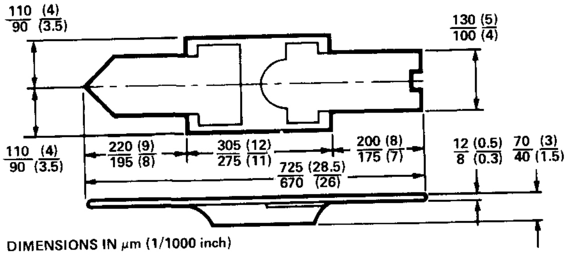

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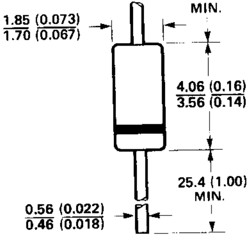

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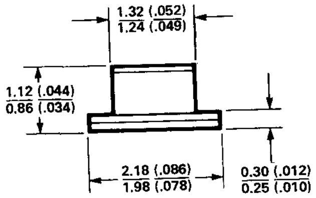

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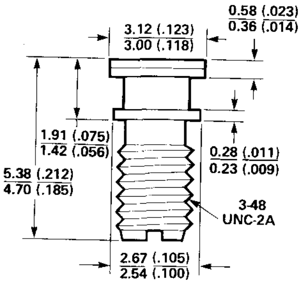
All dimensions in millimeters (inches), except where noted.
For complete package specifications refer to individual product specification sheets.
Drawings are not to scale.



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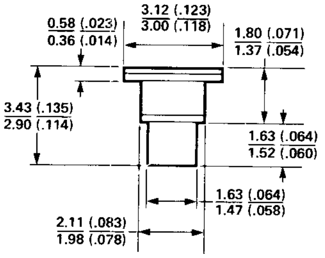

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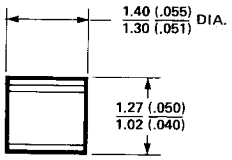

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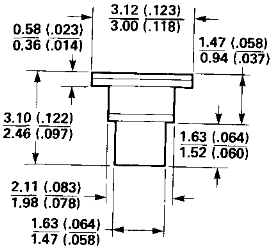

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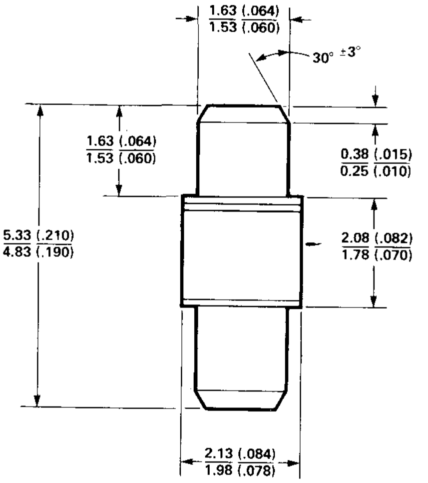

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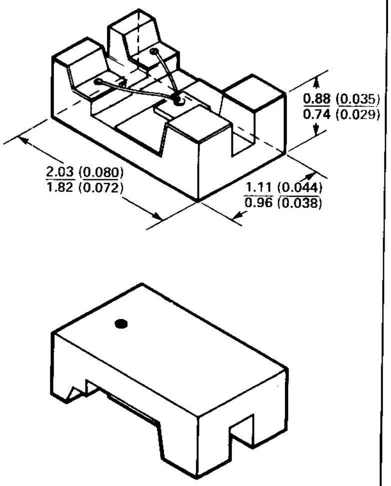

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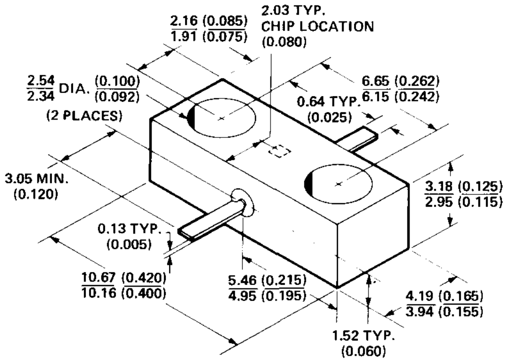

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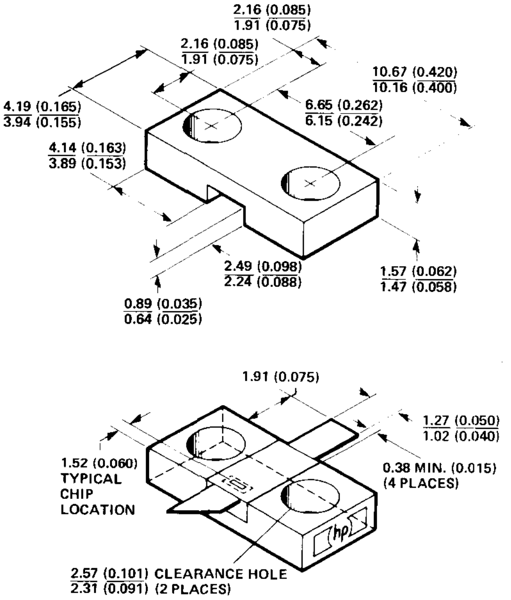

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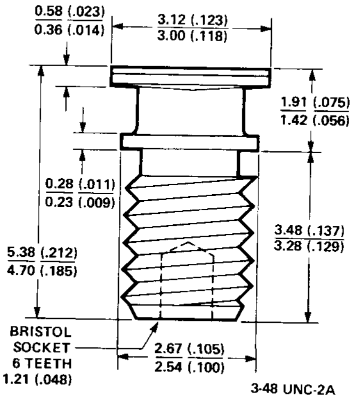

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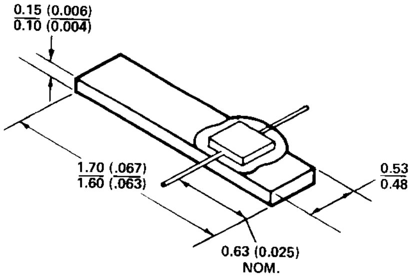

*71 MINISTRIP HAS ONLY ONE LEAD.

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All dimensions in millimeters (inches), except where noted.
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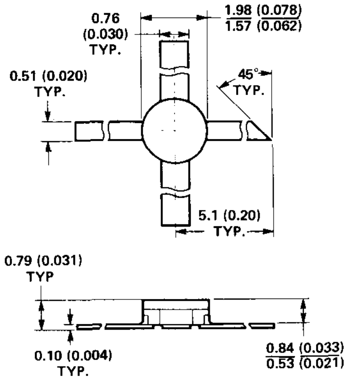
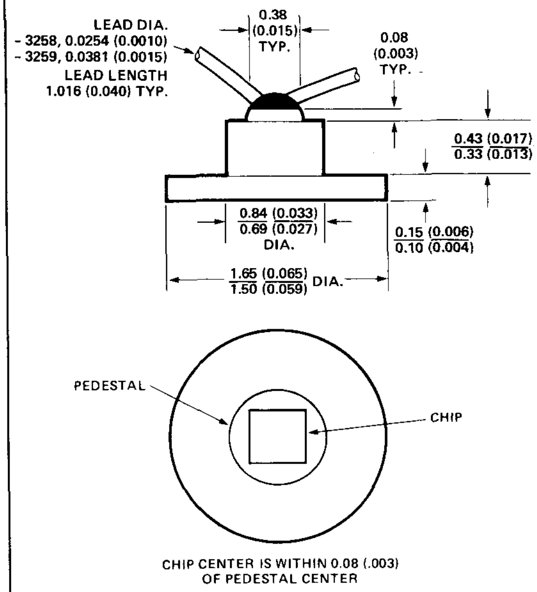


HPAC-70GT



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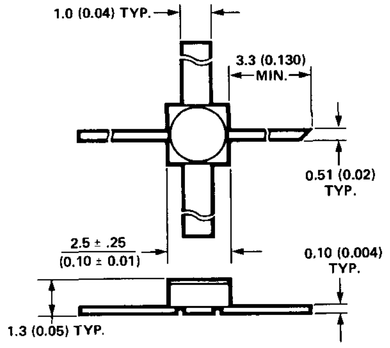

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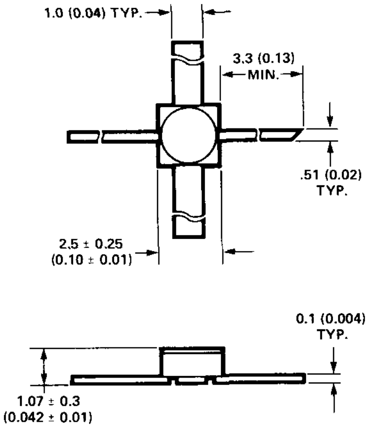

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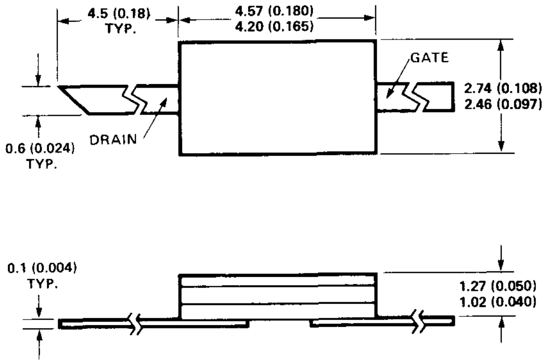

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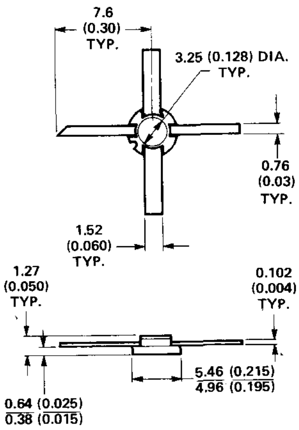
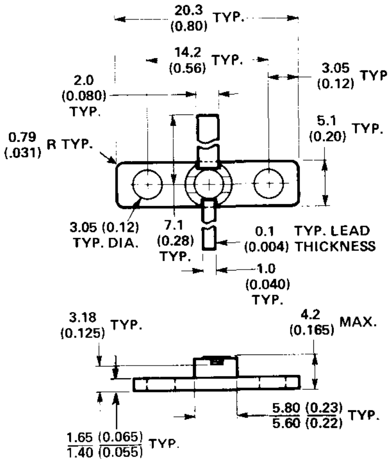


HPAC-200



HPAC-200 GB/GT

DESIGN AIDS

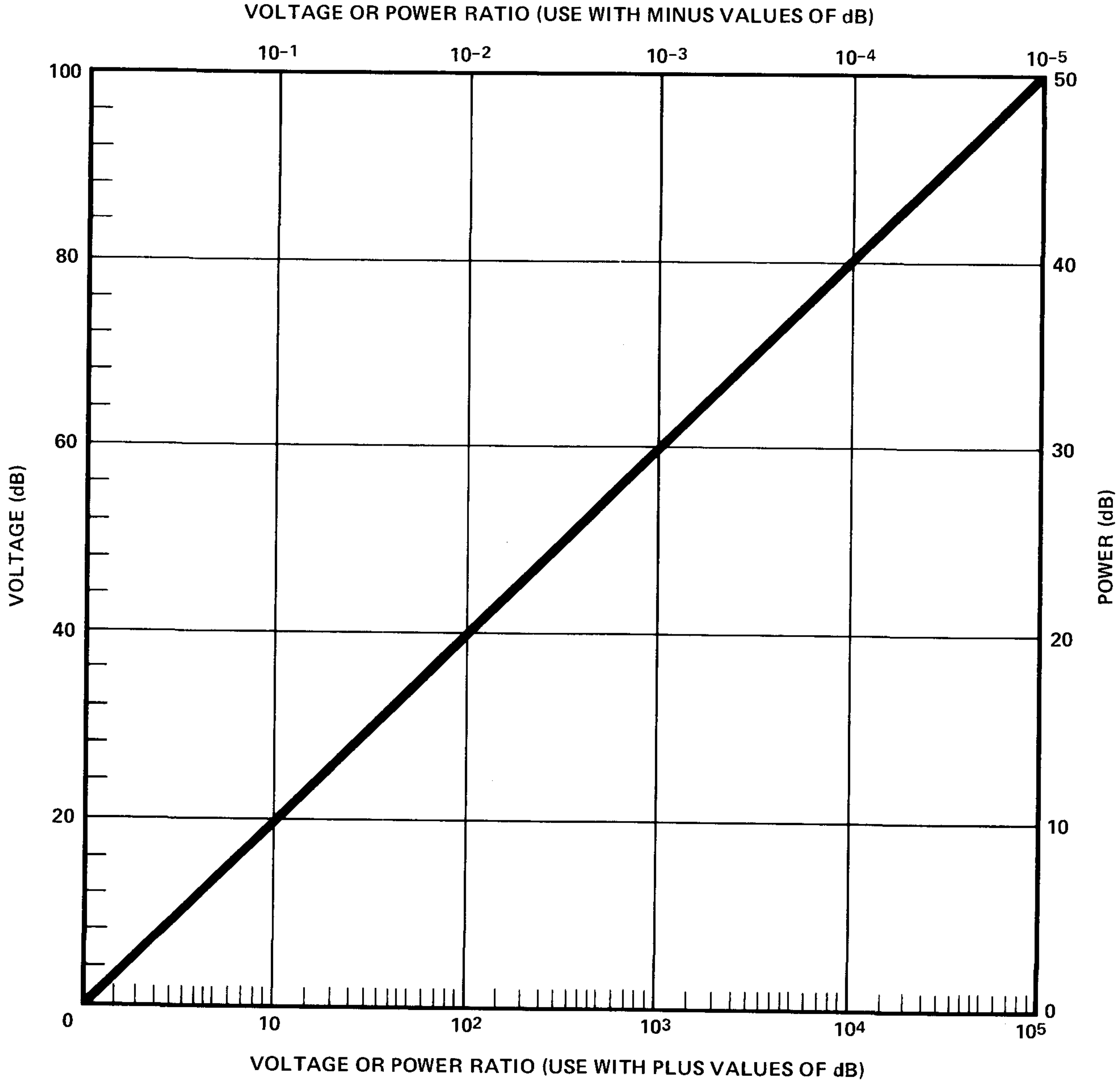
TRANSMISSION LINE EQUATIONS

Quantity	General Line Expression	Ideal Line Expression
Propagation constant	$\gamma = \alpha + j\beta = \sqrt{(R + j\omega L)(G + j\omega C)}$	$\gamma = j\omega\sqrt{LC}$
Phase constant β	Imaginary part of γ	$\beta = \omega\sqrt{LC} = \frac{2\pi}{\lambda}$
Attenuation constant α	Real part of γ	0
Characteristic impedance	$Z_o = \sqrt{\frac{R + j\omega L}{G + j\omega C}}$	$Z_o = \sqrt{\frac{L}{C}}$
Input impedance	$Z_{-\ell} = Z_o \frac{Z_r + Z_o \tanh \gamma\ell}{Z_o + Z_r \tanh \gamma\ell}$	$Z_{-\ell} = Z_o \frac{Z_r + jZ_o \tan \beta\ell}{Z_o + jZ_r \tan \beta\ell}$
Impedance of short-circuited line. $Z_r = 0$	$Z_{s.c.} = Z_o \tanh\gamma\ell$	$Z_{s.c.} = jZ_o \tan\beta\ell$
Impedance of open-circuited line. $Z_r = \infty$	$Z_{o.c.} = Z_o \coth\gamma\ell$	$Z_{o.c.} = -jZ_o \cot\beta\ell$
Impedance transformation by a line an odd number of quarter wavelengths long	$Z = Z_o \frac{Z_r + Z_o \coth\alpha\ell}{Z_o + Z_r \coth\alpha\ell}$	$Z = \frac{Z_o{}^2}{Z_r}$
Impedance transformation by a line an integral number of half wavelengths long	$Z = Z_o \frac{Z_r + Z_o \tanh\alpha\ell}{Z_o + Z_r \tanh\alpha\ell}$	$Z = Z_r$
Voltage reflection coefficient	$\rho = \frac{Z_r - Z_o}{Z_r + Z_o}$	$\rho = \frac{Z_r - Z_o}{Z_r + Z_o}$

SOME MISCELLANEOUS RELATIONS IN LOW-LOSS TRANSMISSION LINES

Equation	Explanation
$r = \frac{1 + \lvert\rho\rvert}{1 - \lvert\rho\rvert}$ $\lvert\rho\rvert = \frac{r - 1}{r + 1}$	r = SWR $\lvert\rho\rvert$ = magnitude of reflection coefficient
$\rho = \frac{R - Z_o}{R + Z_o}$ $r = \frac{R}{Z_o}$ $r = \frac{Z_o}{R}$	ρ = reflection coefficient (real) at a point in a line where impedance is real(R) $R > Z_o$ (at voltage maximum) $R < Z_o$ (at voltage minimum)
$\frac{P_r}{P_i} = \lvert\rho\rvert^2 = \left(\frac{r - 1}{r + 1}\right)^2$ $\frac{P_t}{P_i} = 1 - \lvert\rho\rvert^2 = \frac{4r}{(r + 1)^2}$	P_r = reflected power P_i = incident power P_t = transmitted power
$\frac{\alpha_r}{\alpha_m} = \frac{1 + \rho^2}{1 - \rho^2} = \frac{r^2 + 1}{2r}$	α_m = attenuation constant where r = 1, matched line. α_r = attenuation constant allowing for increased ohmic loss caused by standing waves.
$r_{max} = r_1 r_2$ $r_{min} = \frac{r_2}{r_1}; r_2 > r_1$	r_{max} = maximum SWR when r_1 and r_2 combine in worst phase. r_{min} = minimum SWR when r_1 and r_2 are in best phase.
$\lvert\rho\rvert = \frac{\lvert X\rvert}{\sqrt{X^2 + 4}}$ $r = \frac{\sqrt{X^2 + 4} + \lvert X\rvert}{\sqrt{X^2 + 4} - \lvert X\rvert}$ $\lvert X\rvert = \frac{r - 1}{\sqrt{r}}$	Relations for a normalized reactance X in series with resistance Z_o.
$\lvert\rho\rvert = \frac{\lvert B\rvert}{\sqrt{B^2 + 4}}$ $r = \frac{\sqrt{B^2 + 4} + \lvert B\rvert}{\sqrt{B^2 + 4} - \lvert B\rvert}$ $\lvert B\rvert = \frac{r - 1}{\sqrt{r}}$	Relations for a normalized susceptance B in shunt with admittance Y_o

CONVERSION OF VOLTAGE OR POWER RATIO TO DECIBELS



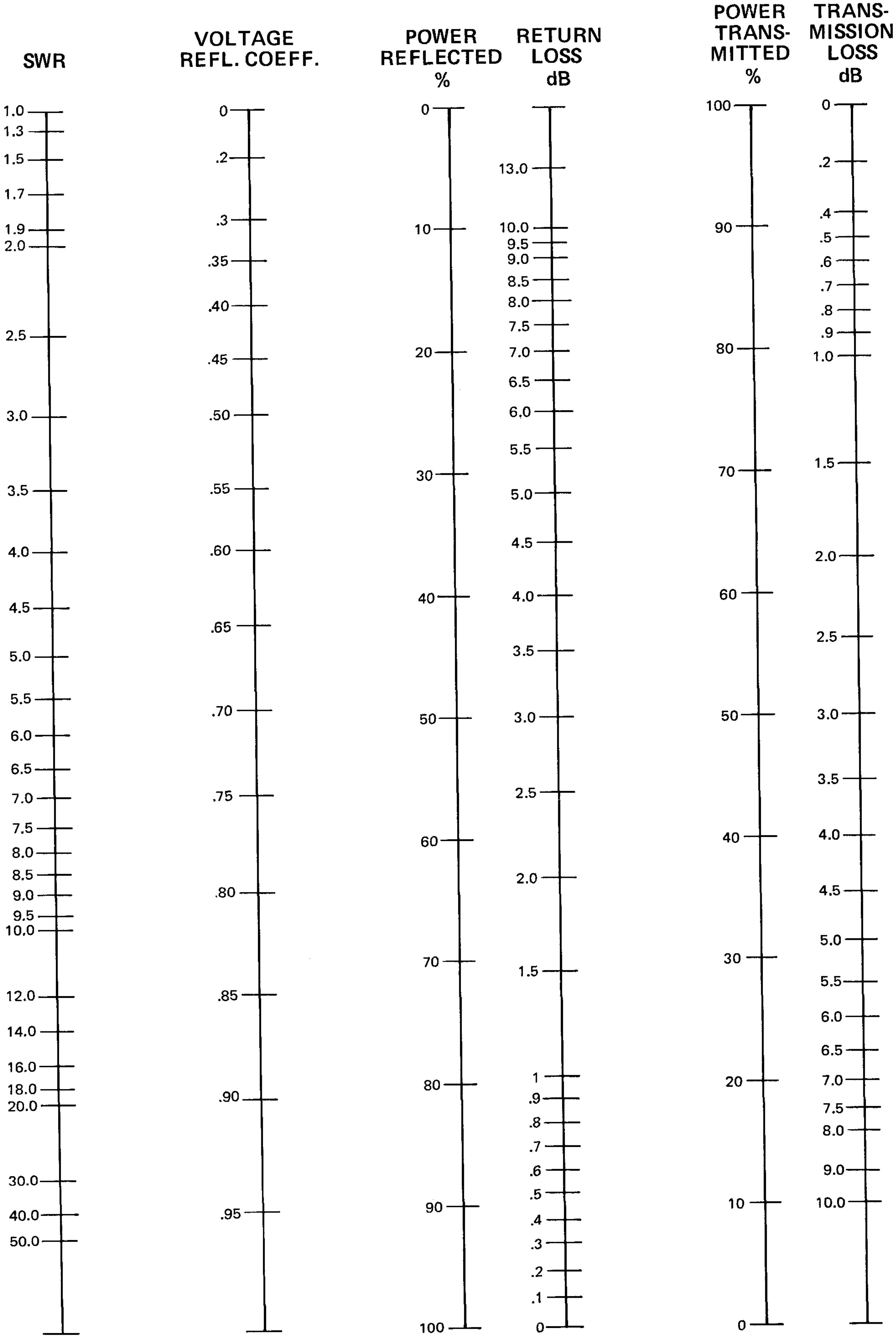
RETURN LOSS VS. STANDING WAVE RATIO
(0.0 TO 14.3 dB)

Return Loss (dB)	SWR	Return Loss (dB)	SWR	Return Loss (dB)	SWR
0.0	∞	4.8	3.710	9.6	1.990
0.1	174.4	4.9	3.639	9.7	1.973
0.2	86.72	5.0	3.569	9.8	1.957
0.3	58.00	5.1	3.503	9.9	1.941
0.4	43.44	5.2	3.440	10.0	1.925
0.5	34.78	5.3	3.379	10.1	1.910
0.6	28.98	5.4	3.320	10.2	1.894
0.7	24.84	5.5	3.263	10.3	1.880
0.8	21.73	5.6	3.209	10.4	1.865
0.9	19.32	5.7	3.156	10.5	1.851
1.0	17.40	5.8	3.106	10.6	1.837
1.1	15.81	5.9	3.057	10.7	1.824
1.2	14.50	6.0	3.010	10.8	1.810
1.3	13.39	6.1	2.964	10.9	1.798
1.4	12.43	6.2	2.920	11.0	1.785
1.5	11.61	6.3	2.877	11.1	1.772
1.6	10.89	6.4	2.836	11.2	1.760
1.7	10.25	6.5	2.796	11.3	1.748
1.8	9.684	6.6	2.757	11.4	1.737
1.9	9.178	6.7	2.720	11.5	1.725
2.0	8.723	6.8	2.684	11.6	1.714
2.1	8.311	6.9	2.649	11.7	1.703
2.2	7.936	7.0	2.615	11.8	1.692
2.3	7.598	7.1	2.582	11.9	1.681
2.4	7.285	7.2	2.549	12.0	1.671
2.5	6.997	7.3	2.518	12.1	1.661
2.6	6.731	7.4	2.488	12.2	1.651
2.7	6.485	7.5	2.458	12.3	1.641
2.8	6.257	7.6	2.430	12.4	1.631
2.9	6.045	7.7	2.402	12.5	1.622
3.0	5.847	7.8	2.375	12.6	1.612
3.1	5.662	7.9	2.348	12.7	1.603
3.2	5.489	8.0	2.323	12.8	1.594
3.3	5.327	8.1	2.298	12.9	1.586
3.4	5.175	8.2	2.273	13.0	1.577
3.5	5.030	8.3	2.250	13.1	1.568
3.6	4.894	8.4	2.227	13.2	1.560
3.7	4.765	8.5	2.204	13.3	1.552
3.8	4.645	8.6	2.182	13.4	1.544
3.9	4.529	8.7	2.161	13.5	1.536
4.0	4.420	8.8	2.140	13.6	1.528
4.1	4.315	8.9	2.120	13.7	1.520
4.2	4.216	9.0	2.100	13.8	1.513
4.3	4.122	9.1	2.081	13.9	1.506
4.4	4.033	9.2	2.061	14.0	1.498
4.5	3.947	9.3	2.043	14.1	1.491
4.6	3.864	9.4	2.025	14.2	1.484
4.7	3.786	9.5	2.008	14.3	1.478

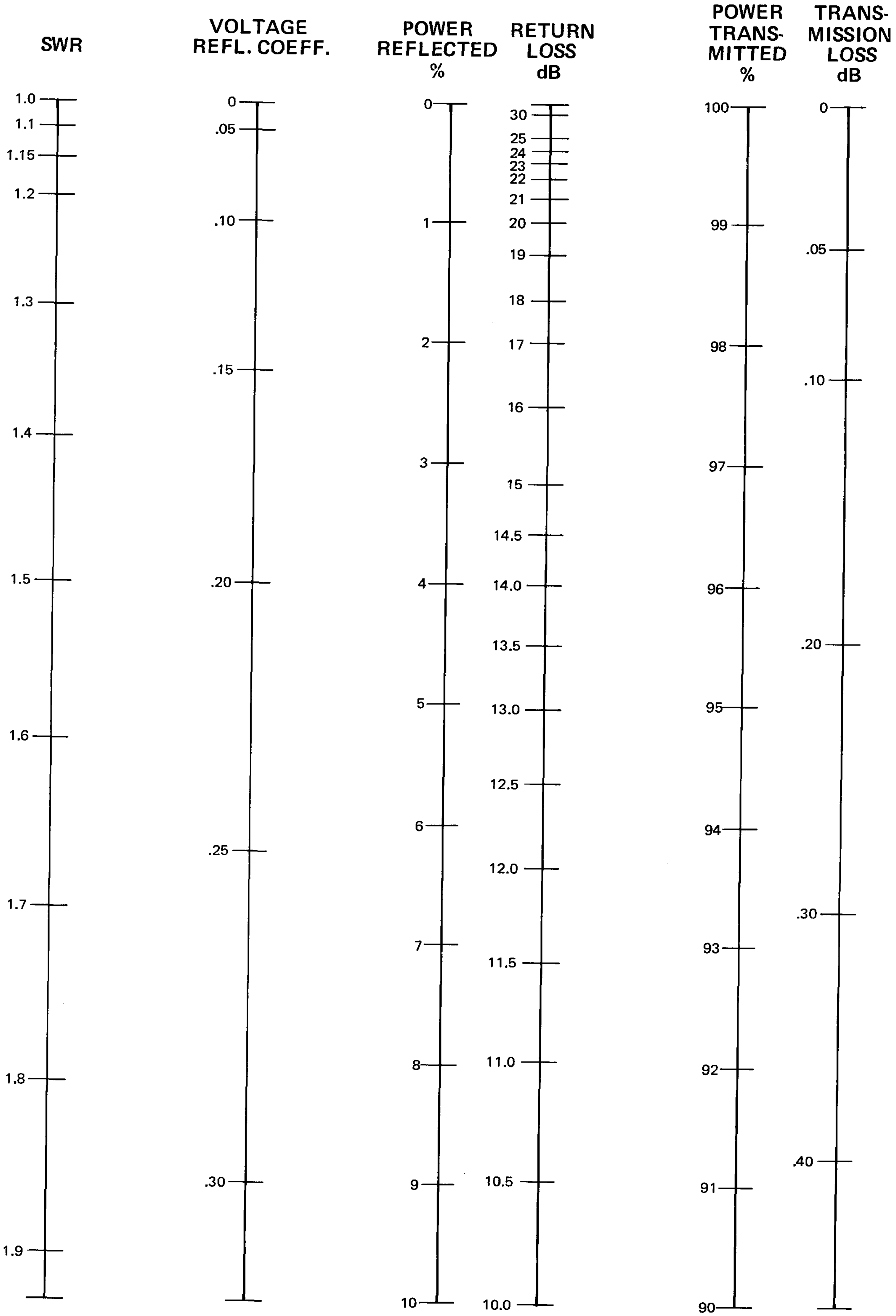
RETURN LOSS VS. STANDING WAVE RATIO
(14.4 TO 60 dB)

Return Loss (dB)	SWR	Return Loss (dB)	SWR	Return Loss (dB)	SWR
14.4	1.471	18.3	1.277	31.0	1.058
14.5	1.464	18.4	1.273	31.5	1.055
14.6	1.458	18.5	1.270	32.0	1.051
14.7	1.451	18.6	1.266	32.5	1.048
14.8	1.445	18.7	1.263	33.0	1.046
14.9	1.439	18.8	1.259	33.5	1.043
15.0	1.432	18.9	1.256	34.0	1.041
15.1	1.426	19.0	1.253	34.5	1.038
15.2	1.421	19.1	1.249	35.0	1.036
15.3	1.415	19.2	1.246	35.5	1.034
15.4	1.409	19.3	1.243	36.0	1.032
15.5	1.404	19.4	1.240	36.5	1.030
15.6	1.398	19.5	1.237	37.0	1.029
15.7	1.393	19.6	1.234	37.5	1.027
15.8	1.387	19.7	1.231	38.0	1.026
15.9	1.382	19.8	1.228	38.5	1.024
16.0	1.377	19.9	1.225	39.0	1.023
16.1	1.372	20.0	1.222	39.5	1.021
16.2	1.366	20.5	1.208	40.0	1.020
16.3	1.362	21.0	1.196	41.0	1.018
16.4	1.357	21.5	1.184	42.0	1.016
16.5	1.352	22.0	1.172	43.0	1.014
16.6	1.347	22.5	1.162	44.0	1.013
16.7	1.342	23.0	1.152	45.0	1.011
16.8	1.338	23.5	1.143	46.0	1.010
16.9	1.333	24.0	1.135	47.0	1.009
17.0	1.329	24.5	1.127	48.0	1.008
17.1	1.324	25.0	1.119	49.0	1.007
17.2	1.320	25.5	1.112	50.0	1.006
17.3	1.316	26.0	1.105	51.0	1.0056
17.4	1.312	26.5	1.099	52.0	1.0050
17.5	1.308	27.0	1.094	53.0	1.0044
17.6	1.304	27.5	1.088	54.0	1.0040
17.7	1.300	28.0	1.083	55.0	1.0036
17.8	1.296	28.5	1.078	56.0	1.0032
17.9	1.292	29.0	1.074	57.0	1.0028
18.0	1.288	29.5	1.069	58.0	1.0026
18.1	1.284	30.0	1.065	59.0	1.0022
18.2	1.280	30.5	1.061	60.0	1.0020

SWR NOMOGRAPH #1

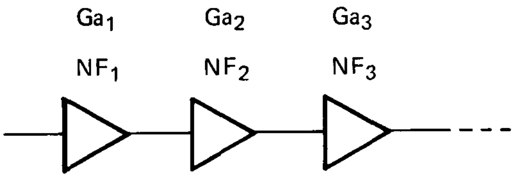


SWR NOMOGRAPH #2



USEFUL FORMULAS FOR MICROWAVE TRANSISTOR DESIGNS

Total Noise Figure of Cascaded Stage



$$F_S = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots\ldots$$

Constant Noise Circles

First define $$N_i = \frac{F_i - F_{min}}{4r_n} \cdot |1 + \Gamma_o|^2$$

The Center $$C_{Fi} = \frac{\Gamma_o}{1 + N_i}$$

The Radius $$R_{Fi} = \frac{1}{1 + N_i} \sqrt{N_i^2 + N_i (1 - |\Gamma_o|^2)}$$

F_i = the value of the noise circle

F_{min} = minimum noise figure

Γ_o = optimum source impedance for low noise

r_n = normalized noise resistance

Constant Gain Circles

$$d_i = \frac{g_i |S_{ii}|}{1 - |S_{ii}|^2 (1 - g_i)}$$

$$R_i = \frac{\sqrt{1 - g_i}\,(1 - |S_{ii}|^2)}{1 - |S_{ii}|^2 (1 - g_i)}$$

$$g_i = G_i (1 - |S_{ii}|^2) = \frac{G_i}{G_{i_{max}}}$$

d_i = the distance from the center of the Smith chart to the center of the constant gain circle along the vector S_{11}^*

R_i = the radius of the circle

g_i = the normalized gain value for the gain circle G_i

G_i = gain represented by the circle

Source Transformation

$$\Gamma_{in} = S_{11} + \frac{S_{21} S_{12} \Gamma_L}{1 - S_{22} \Gamma_L}$$

Load Transformation

$$\Gamma_{out} = S_{22} + \frac{S_{21} S_{12} \Gamma_S}{1 - S_{11} \Gamma_S}$$

ABSTRACTS OF APPLICATION NOTES

Below is a brief summary of Application Notes for diodes and transistors. Portions of many of these have been included in this catalog. Those that are included in this catalog in their entirety are also listed with the corresponding page number.

All of the Application Notes are available from your local HP Sales Office or nearest HP Components Franchised Distributor or Representative.

922 Application of PIN Diodes

Discusses how the PIN diode can be applied to a variety of RF control circuits. Such applications as attenuating, leveling, amplitude and pulse modulating, switching, and phase shifting are discussed in detail. Also examines some of the important properties of the PIN diode and how they affect its application. See page 142.

923 Hot Carrier Diode Video Detectors

Describes the characteristics of HP Schottky barrier diodes intended for use in video detector or video receiver circuits, and discusses some design features of such circuits.

Though less sensitive than the heterodyne receiver, the many advantages of the video receiver make it extremely useful. The Schottky diode can be used to advantage in applications such as beacon, missile-guidance, fuse-activating, and counter-measure receivers, and as power-leveling and signal-monitoring detectors.

Among the subjects discussed are the performance characteristics of video detector diodes—tangential sensitivity, video resistance, voltage sensitivity and figure of merit; how these characteristics affect the bandwidth of a video detector; video detector design considerations; considerations that affect dynamic range; and considerations that vary the level at which burnout can occur.

928 Ku-Band Step Recovery Multipliers

Discusses the use of step-recovery diodes in a times-eight, single-stage frequency multiplier which, at 16 GHz, has a typical maximum output of 75 mW. The note also provides design modifications, together with references, for meeting other performance requirements.

929 Fast-Switching PIN Diodes

Discusses the switching speed of the PIN diodes and the considerations which affect switching capability. For HP's 5082-3041/3042 fast-switching PIN diodes, AN 929 outlines basic drive requirements and comments on a few practical switching circuits. Considerations involved in the design of the filters required for use with the diodes are also discussed. For the 5082-3041, AN 929 provides two curves: 1) typical isolation vs. forward bias and 2) switching time vs. forward bias for peak reverse current as a parameter. See page 142.

932 Selection and Use of Microwave Diode Switches and Limiters

Helps the systems designer select the proper switching or limiting component and assists him in integrating this component into the overall design of the system. This note is a practical, user-oriented approach to problems encountered with switching and limiting microwave signals.

936 High Performance PIN Attenuator for Low-Cost AGC Applications

PIN diodes offer an economical way of achieving excellent performance in AGC circuits. Significant improvements in crossmodulation and intermodulation distortion performanace are obtained, compared to transistors. This note discusses other advantages of PIN diodes, such as low frequency operation, constant impedance levels, and low power consumption. See page 143.

942 Schottky Diodes for High Volume Low-Cost Applications

Discusses switching, sampling, mixing and other applications where the substitution of Schottky diodes will provide significant improvement over PN junction devices.

944-1 Microwave Transistor Bias Considerations

A practical discussion of the temperature dependent variables in a microwave transistor that cause RF performance degradation due to changes in quiescent point. Passive circuit networks that minimize quiescent point drift with temperature are analyzed, and the general equations for dc stability factors are given. Emphasis on practical circuit design is highlighted by typical circuit examples.

956-1 The Criterion for the Tangential Sensitivity Measurement

Discusses the meaning of Tangential Sensitivity and a recommended measurement technique. See page 114.

956-3 Flicker Noise in Schottky Diodes

Treats the subject of flicker (1/f) noise in Schottky diodes, comparing 4 different types. See page 115.

956-4 Schottky Diode Voltage Doubler

Explains how Schottky detectors can be combined to achieve higher output voltages than would be produced by a single diode.

956-5 Dynamic Range Extension of Schottky Detectors

Discusses operation of two types of detectors: the small signal type, also known as square-law detectors; and the large signal type, also known as linear or peak detectors.

Techniques for raising the compression level are presented. An example is given illustrating the effect of bias current level on an HP 5082-2751 detector. See page 116.

956-6 Temperature Dependence of Schottky Detector Voltage Sensitivity

A discussion of the effects that temperature changes have on Schottky barrier diodes. Performance improves at lower temperatures in a predictable manner. Data presented were obtained using HP 5082-2750 detector diodes. See page 117.

957-1 Broadbanding the Shunt PIN Diode SPDT Switch

Covers an impedance matching technique which improves the bandwidth of shunt PIN diode switches. See page 143.

957-2 Reducing the Insertion Loss of a Shunt PIN Diode

Examines a simple filter design which includes the shunt PIN diode capacitance into a low pass filter, thereby extending the upper frequency limit. See page 144.

957-3 Rectification Effects in PIN Attenuators

Attenuation levels of PIN diodes are changed by high incident power. Variation in attenuation may be minimized by proper choice of bias resistance. Performance of a PIN diode is limited by both carrier level and frequency because of rectification effects. This note presents the effects of frequency, power level, and bias supply for three types of HP diodes: 5082-3170, 3140 and 3141. See page 146.

959-1 Factors Affecting Silicon IMPATT Diode Reliability and Safe Operation

Treats silicon IMPATT diode reliability with heavy emphasis on how to avoid bias circuit related and tuning induced burnout.

959-2 Reliability of Silicon IMPATT Diodes

Covers the major failure mechanism in silicon IMPATT diodes with a summary of life test results on both single and double drift silicon IMPATT diodes.

961 Silicon Double-Drift IMPATT Diodes for Pulse Applications

Offers an in-depth look at the theory and applications of silicon double drift IMPATTS designed for use in pulsed oscillators and amplifiers. Major sections include device theory, circuits, performance and injection locking techniques. An appendix on pulse bias circuits is included.

962 Silicon Double-Drift IMPATT Diodes for High-Power CW Microwave Applications

Provides a thorough treatment of the theory and application of silicon double-drift IMPATTS designed for use in CW oscillators and amplifiers. Major sections include device theory, circuits, performance and injection locking techniques.

963 Impedance Matching Techniques for Mixers and Detectors

Presents a methodical technique for matching complex loads, such as Schottky diodes, to a transmission line. Direct application to broadband mixers and detectors is illustrated. See page 214.

967 A Low Noise 4 GHz Amplifier Using the HXTR-6101 Silicon Bipolar Transistor

Describes in detail the design of a single-stage, state-of-the-art low noise amplifier at 4 GHz using the HXTR-6101 silicon bipolar transistor. Both the input and output matching networks are described. See page 70.

968 IMPATT Amplifier

Discusses IMPATT amplifier design. A waveguide amplifier produced 2 watts of power with 10 dB gain at 11.2 GHz. Using a coaxial structure, similar performance was obtained at 8.4 GHz.

969 An Optimum Zero Bias Schottky Detector Diode

Describes the use of the HSCH-3171 and HSCH-3486 zero bias detector diodes. Their forward voltage characteristics are detailed, as well as discussion of voltage sensitivity including effects of junction capacitance, load resistance and reflection loss on sensitivity. Temperature characteristic curves for both devices are also included. See page 119.

NEW

970 A 6 GHz Amplifier Using the HFET-1101 GaAs FET

This application note highlights some of the design tradeoffs when using a GaAs FET. The example is an amplifier for use in the 5.9 to 6.4 GHz telecommunications band. The amplifier's performance over this band is excellent, with a minimum noise figure of 3.3 dB, a minimum associated gain of 10.9 dB, a flatness of ±0.4 dB and a 9.5 dBm minimum power output at 1 dB gain compression. The maximum input and output SWR are 2.67:1 and 1.90:1 respectively. See page 20.

971 The Beam Lead Mesa PIN in Shunt Applications

The low RC product, fast switching time, and other unique features of the HPND-4050 beam lead PIN diode make it well suited for switching applications in the shunt configuration. Switching performance, practical circuits, handling, and bonding instructions are included in the discussions in this application note. See page 216.

972 Two Telecommunications Power Amplifiers for 2 and 4 GHz Using the HXTR-5102 Silicon Bipolar Power Transistor

Describes in detail the design of two linear power amplifiers using the HXTR-5102. In each case, small signal S-parameters, and power contours are used in the characterization. See page 62.

ABSTRACTS OF APPLICATION BULLETINS

Brief summaries of Application Bulletins for diodes and transistors are given here. Those that are included in this catalog in their entirety are also listed with the corresponding page number. All of the Application Notes are available from your local HP Sales Office or nearest HP Components Franchised Distributor or Representative.

AB 5 Current Source for Diode Testing

This application bulletin describes a constant current source designed primarily for the ease of use in laboratory measurements. Easily programmable by thumb wheel switches in 10 μA steps from 10 μA to 700 mA, its accuracy exceeds most commercially available current sources.

AB 6 PIN Diode RF Resistance Measurement

The use of the HP 4815 Vector Impedance Meter, in conjunction with a tunable test fixture, provides an efficient and reliable means for measuring the RF resistance of a PIN diode.

AB 7 Mixer Distortion Measurements

Describes the measurement of distortion in a balanced mixer by the two tone method.

AB 9 Derivation, Definition and Application of Noise Measure

The associated gain at optimum noise figure bias becomes an important parameter at microwave frequencies. The noise measure of a device is a term including both noise figure and associated gain.

AB 10 Transistor Noise Measurements

The increasing acceptance of GaAs field effect and silicon bipolar transistors in low noise pre-amp applications has stressed the inportance of the techniques used in measuring noise figure. This application bulletin discusses the various techniques and possible sources of error in making a transistor noise figure measurement.

AB 13 Transistor Speed Up Using Schottky Diodes

Significant reduction in transistor switching delay time can be achieved by adding a Schottky diode and a PIN diode to the transistor switching circuit. This improvement in switching performance also extends the oscillator capability of the transistor to higher frequencies. See page 120.

AB 14 Waveform Clipping with Schottky Diodes

Consideration is given in this application bulletin to the design requirements of clipping circuits which are used to limit the transmission of signals above or below specified levels. The characteristics of Schottky diodes needed to achieve the required performance in these circuits are discussed and recommendations made. See page 121.

AB 15 Waveform Clamping with Schottky Diodes

Discussed in this application bulletin are the circuit design and diode performance requirements for a clamping circuit, which is used as a DC restorer or level shifter. Schottky diodes having the required characteristics for this type of circuit are recommended. See page 121.

AB 16 Waveform Sampling with Schottky Diodes

This application bulletin discusses the design considerations for a sampling circuit used to sample high frequency repetitive signals and reproduce them at lower frequencies for ease of monitoring. Schottky diode performance requirements important in the realization of a sampling circuit are considered. See page 122.

AB 17 Noise Parameters and Noise Circles for the HXTR-6101, -6102, -6103, -6104 and -6105 Low Noise Transistors

Noise figures as a function of source reflection coefficient (r_s) can be expressed using three parameters, F_{min}, R_n to r_o known as noise parameters. Three parameters are presented for five microwave transistors. The method of generating noise circles is given in a step-by-step fashion.

AB 18 The Performance of the HXTR-6101 at Submilliampere Bias Levels

Describes the performance of a low noise microwave transistor at bias conditions of V_{CE} ± 3V and I_C ± 1.0 mA, 0.5 mA, 0.25 mA and frequencies 1.0, 1.5, 2.0 and 3.0 GHz.

AB 19 Noise and Power Parameters for the HFET-1101

The noise parameters F_{min}, R_n to r_o are given for the HFET-1101, a general purpose microwave GaAs FET. The source and load reflection coefficients are given for maximum output power at an input power level of 5 dBm. The gain, power at 1 dB compression, and power at 3 dB compression are given for frequencies of 4, 6, 8, 10 and 12 GHz.

AB 20 Amplitude to Phase Conversion in IMPATT Amplifiers

Curves show the amplitude to phase conversion of a 5082-0610 IMPATT diode in an 11 GHz amplifier using a cavity similar to that described in AN 962.

AB 22 Equivalent Circuits for Double Drift CW IMPATT Diodes

Small signal equivalent circuits were derived for 5082-0610 and 5082-0611 IMPATT diodes in AN 962. This bulletin extends the analysis to provide both small and large signal equivalent circuits for 5082-0607, 0608, 0610, and 0611 diodes.

AB 23 Models for Double Drift CW IMPATT Diodes in a 50 Ohm Coaxial Mount

Small and large signal equivalent circuits for 5082-0607, -0608, -0610 and -0611 diodes were derived in AN 22. This bulletin provides improved models which separate the mount and package from the diode.

AB 24 Selecting a Design Medium for the HFET-2201 GaAs Field Effect Transistor

This application bulletin shows measured S-parameters on the HFET-2201 in RT/Duroid and Alumina up to 18 GHz. See page 16.

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