SIGNETICS LINEAR VOL 1 DATA BOOK

Signetics Corporation reserves the right to make changes in the products contained in this book in order to improve design or performance and to supply the best possible product.

Signetics Corporation assumes no responsibility for the use of any circuits described herein and makes no representations that they are free from patent infringement.

25% to 50% recycled paper

SECTION 1
general information

DEVICE	PKG	ORDER PART NUMBER 0°C to +70°C	-55°C to +125°C	DICE (+25°C)
501	A	NE501A		501X
	G	NE501G	SE501G	
	K	NE501K	SE501K	
510	A	NE510A	SE510A	510X
	J	NE510J	SE510J	
511	B	NE511B	SE511B	511X
	R	NE511R	SE511R	
515	A	NE515A		515X
	G	NE515G	SE515G	
	K	NE515K	SE515K	
516	A	NE516A	SE516A	516X
	G	NE516G	SE516G	
	K	NE516K	SE516K	
518	A	NE518A	SE518A	518X
	G	NE518G	SE518G	
	K	NE518K	SE518K	
526	A	NE526A	SE526A	526X
	G	NE526G	SE526G	
	K	NE526K	SE526K	
527	K	NE527K	SE527K	527X
528	B	NE528B		528X
	E	NE528E	SE528E	
	R		SE528R	
529	K	NE529K	SE529K	529X
531	G	NE531G	SE521G	531X
	T	NE531T		
	V	NE531V		
533	G	NE533G	SE533G	533X
	V	NE533V		
	T	NE533T	SE533T	
536	G		SU536G	536X
	T	NE536T	SU536T*	
537	G	NE537G	SE537G	537X
	T	NE537T	SE537T	
PA239	A	PA239A		239X
540	L	NE540L	SE540L	540X
550	A	NE550A		550X
	L	NE550L	SE550L	
555	T	NE555T	SE555T	555X
	V	NE555V		
560	B	NE560B		560X
561	B	NE561B		561X
562	B	NE562B		562X
565	A	NE565A		565X
	K	NE565K	SE565K	
566	T	NE566T	SE566T	566X
	V	NE566V		
567	T	NE567T	SE567T	567X
	V	NE567V		
592	A	NE592A		592X
	K	NE592K	SE592K	
μA709	A	μA709CA	μA709AA	709X
			μA709A	
	G	μA709CG	μA709G	
	T	μA709CT	μA709AT	
			μA709T	
	V	μA709CV		
μA710	A	μA710CA		710X
	V	μA710CV		
	T	μA710CT	μA710T	
	G	μA710CG	μA710G	
μA711	A	μA711CA		711X
	G	μA711CG	μA711G	
	K	μA711CK	μA711K	

*Temperature Range @ -55°C to 85°C

DEVICE	PKG	ORDER PART NUMBER 0°C to +70°C	-55°C to +125°C	DICE (+25°C)
μA723	L	μA723CL	μA723L	723X
	A	μA723CA		
μA733	A	μA733CA		733X
	K	μA733CK	μA733K	
	F	μA733CF	μA733F	
μA740	T	μA740CT	μA740T	740X
μA741	A	μA741CA		741X
	G	μA741CG	μA741G	
	V	μA741CV	μA741V	
	T	μA741CT	μA741T	
μA747	A	μA747CA	μA747A	747X
	K	μA747CK	μA747K	
μA748	A	μA748CA		748X
	T	μA748CT	μA748T	
	V	μA748CV		
ULN2111	A	ULN2111		2111X
5070	B	N5070B		5070X
5071	A	N5071A		5071X
5072	A	N5072A		5072X
5556	T	N5556T	S5556T	5556X
	F	N5556F	S5556F	
	V	N5556V		
5558	V	N5558V		5558X
	T	N5558T	S5558T	
	F	N5558F	S5558F	
5595	A	N5595A		5595X
	F	N5595F	S5595F	
5596	A	N5596A		5596X
	K	N5596K	S5596K	
	F	N5596F	S5596F	
7520	B	SN7520N		7520X
7521	B	SN7521N		7521X
7522	B	SN7522N		7522X
7523	B	SN7523N		7523X
7524	B	SN7524N		7524X
7525	B	SN7525N		7525X
75450	A	SN75450N		75450X
75450A	A	SN75450AN		75450AX
75451	V	SN75450P		75450X
75451A	V	SN75450AP		75450AX

DEVICE	PKG	ORDER PART NUMBER			
		0°C to +70°C	-55°C to +125°C	-20°C to +85°C	DICE (+25°C)
LM101D	F		LM101D		Note 1
LM101H	T		LM101H		Note 1
LM101F	G		LM101F		Note 1
LM101N	V		LM101N		Note 1
LM101N-14	A		LM101N-14		Note 1
LM101AH	T		LM101AH		Note 1
LM101AF	G		LM101AF		Note 1
LM101AD	F		LM101AD		Note 1
LM101AN	V		LM101AN		Note 1
LM101AN-14	A		LM101AN-14		Note 1
LM201D	F	LM201D			Note 1
LM201F	G	LM201F			Note 1
LM201H	T	LM201H			Note 1
LM201N	V	LM201N			Note 1
LM201N-14	A	LM201N-14			Note 1
LM201AH	T			LM201AH	Note 1
LM201AF	G			LM201AF	Note 1
LM201AD	F			LM201AD	Note 1
LM201AN	V			LM201AN	Note 1
LM201AN-14	A			LM201AN-14	Note 1
LM301AH	T	LM301AH			301AX
LM301AN	V	LM301AN			301AX
LM301AN-14	A	LM301AN-14			Note 1
LM301AD	F	LM301AD			Note 1
LM301AF	G	LM301AF			Note 1
LM107H	T		LM107H		Note 1
LM107F	G		LM107F		Note 1
LM107D	F		LM107D		Note 1
LM207H	T			LM207H	Note 1
LM207F	G			LM207F	Note 1
LM207D	F			LM207D	Note 1
LM307N	V	LM307N			307X
LM307H	T	LM307H			307X
LM307F	G	LM307F			307X
LM108H	T		LM108H		Note 1
LM108F	G		LM108F		Note 1
LM308H	T	LM308H			308X
LM308F	G	LM308F			308X
LM109H	DB		LM109H		Note 1
LM109K	DA		LM109K		Note 1
LM209H	DB			LM209H	Note 1
LM209K	DA			LM209K	Note 1
LM309H	DB	LM309H			309X
LM309K	DA	LM309K			309X

NOTE:
1. Most dice are available over the military temperature range.

EXPLANATION

The following table has been presented to assist the designer in selecting the optimum device for his application. For the majority of applications, the primary considerations are "Input Bias Current" and "Offset Voltage". For additional specifications refer to the appropriate device data page.

DEVICE APPLICATIONS

INPUT CURRENT (nA)		SIGNETICS NUMBER	PACKAGE TYPE
MAXIMUM	TYPICAL		
0.012	0.005	SU536	T
0.030	0.010	NE536	T
0.200	0.100	μA740	T
2.0	0.100	μA740C	T
2.0	0.8	SE537	T
2.0	0.8	LM108	T
2.0	0.8	LM108A	T
7.0	1.5	NE537	T
7.0	1.5	LM308	T
7.0	1.5	LM308A	T
10.0	2.0	SE533	T
10.0	5.0	NE533	T, V
15.0	8.0	S5556	T
30.0	15.0	N5556	T, V
75.0	30.0	LM101A	T
75.0	30.0	LM107	T
250.0	70.0	LM301A	T, V
500.0	80.0	μA748	T
500.0	80.0	μA748C	A, T, V
500.0	120.0	LM101	T
500.0	200.0	μA709	T
500.0	200.0	μA741C	A, T, V
500.0	200.0	μA741	A, T, V
500.0	200.0	SE531	T
1500.0	250.0	LM201	A, T, V
1500.0	300.0	μA709	A, T, V
1500.0	400.0	NE531	T, V
OFFSET VOLTAGE (mV)			
0.5	0.3	LM108A	T
0.5	0.3	LM308A	T
1.0	0.5	SE533	T
2.0	0.6	SE537	T
2.0	0.7	LM101	T
2.0	0.7	LM107	T
2.0	0.7	LM108	T
2.0	1.0	NE533	T, V
5.0	1.0	LM101	T
5.0	1.0	μA709	T
5.0	1.0	μA741	T
5.0	1.0	μA748	T
5.0	2.0	NE531	T
5.0	2.0	S5556	T
6.0	1.0	μA741C	A, T, V
5.0	2.0	NE531	T, V
6.0	2.0	μA748C	A, T, V
7.5	1.6	NE537	T
7.5	1.6	LM201	A, T, V
7.5	2.0	LM301	T, V
7.5	2.0	LM308	T
7.5	2.0	μA709C	A, T, V
10.0	4.0	N5556	T, V
20.0	10.00	μA740	T
50.0	20.0	SU536	T
100.0	30.0	μA740	T
100.0	50.0	NE536	T

EXPLANATION

The following tables are presented as a convenience to the designer for the purpose of comparing commercially available modular and hybrid FET input op amps with Signetics 536 FET input LIC series. Substantial cost savings, as well as size and weight reductions can now be realized. For additional specifications please refer to the appropriate device data page.

ANALOG DEVICES	MODULAR FET-OP AMPS																			HYBRID FET-OP AMPS												
Model	40		41			42			45		47		142			146		149		501			503		506	513	516	SIGNETICS	
Version	J	K	JV	KV	LV	J	K	L	J	K	A	B	A	B	C	J	K	A	B	A	B	C	J	K	J	J	J	536	Units
Input Current Max. 25°C	50	20	0.5	0.25	0.15	0.5	0.25	0.15	50	25	50	25	50	25	25	30	20	30	15	25	10	5	25	10				12	PA
Offset Drift Max.	50	20	25	10	25	75	25	75	50	15	50	15	50	25	15	7	2	25	15	75	25	25	75	25					μV/°C
CMRR Typ.	80*	80*	80	80	80	66*	66*	66*	70*	70*	86	86	66*	66*	66*	80*	80*	80*	80*	80*	80*	80*	70	70				70	dB
Gain Band Width Product	4	4	1	1	1	0.5	0.5	0.5	10	10	10	10	5	5	5	5	5	15	15	4	4	4						1	MHz
Slew Rate	6	6	3	3	3	0.2	0.2	0.2	75	75	50	50	10	10	10	10	10	100	100	3	3	3	4	4	4	30	30	6	V/μS
Output Current	5	5							20	20	20	20	20	20	20	20	20	15	15	5	5	5						30	mA
Temperature Range	C	C							I	I	I	I	I	I	I	C	C	I	I	I	I	I	C		C	C	C	-20°C +85°C	

M = -55 - +125
I = -25 - +85
C = -0 - +70

* = CMRR Over Reduced Voltage Range

* = CMRR Over Reduced Common Mode Voltage Range

SIGNETICS ■ COMPARISON TABLE

TELEDYNE PHILBRICK — MODULAR FET-OP AMPS | HYBRID FET-OP AMPS | MODULAR FET-OP AMPS

Model	QFT-2			1408	1414			1009		1003		1021	1023		1408			QFT-5	1011			1019	1025	SIGNETICS	
Version	O	A	B	10	00	10	00	01	02	00	01		00	01	00	01	02		00	01	02			536	Units
Input Current Max. 25°C	100	100	100	5	150	150	30	20	20	10	5	10	10	10	25	10	5	100	30	20	20	50	50	12	pA
Offset Drift Max.							75	50	25	4	2	50	5	2	75	25	25	300	50	25	10	25	25		µV/°C
CMRR Typ.	70	70	70	25	50	50	60	60	60	120	120	120	120	120	80	80	80	60	66	66	66	100	*	70	dB
Gain Band Width Product	1.7	1.7	1.7	80	66	66	1	1	1	1.5	1.5	2	2	2	4	4	4	1.7	12	12	12	100	50	1	MHz
Slew Rate	10	10	10	4	10	10	5	5	5	7	7	6	6	6	6	6	6	5	70	70	70	1000	650	6	V/µS (typ.)
Output Current	10	10	10	6	50	50	5	5	5	20	20	20	20	20	5	5	5	5	20	20	20	20	50	30	mV
Temperature Range	I	I	I	I	I	I	I	I	I	C	C	I	C	C	I	I	I	I	I	I	I	I		-20°C +85°C	

M - 55 + 125
I - 25 + 85
C - 0 + 70

* = Inverting Only

ZELTEX — MODULAR FET-OP AMPS | HYBRID FET-OP AMPS

Model	ZA 801			ZA 802		ZA 803	133			134		135	136	ZA 801			SIGNETICS	
Version	M1	M2	M3	M1	M2	M1	00	03	04	0	D			D1	E1	T1	536	Units
Input Current Max. 25°C	25	25	25	5	5	2	10	10	10	100	100	100	100	25	25	25	12	pA
Offset Drift Max.	50	20	5	50	20	10	50	4	10	50	100	20	25	50	50	50		µV/°C
CMRR Typ.	80	80	80	100	100	100	86	86	86	60*	60*	100	100	80	80	80	70	dB
Gain Band Width Product	4	4	4	2	2	2	1.5	1.5	1.5	1.3	1.3	5	1	4	4	4	1	MHz
Slew Rate (min.)	6	6	6	6	6		6	6	6	6	6	100	25	6	6	6	6	V/µS
Output Current	7	7	7	7	7	7	5	5	5	4	4	20	20 (+100)	7	7	7	30	mA
Temperature Range	I	I	I	I	I	I	I	C	I	I	I	I	I	I	I	I	-20°C +85°C	

* = CMRR Over Reduced C.M. Voltage Range

BURR-BROWN — MODULAR FET-OP AMPS | HYBRID FET-OP AMPS

Model	3420			3421			3308	3307	3312	3313	3310	3311	3317	3318	3348	3349	3350	3503						SIGNETICS	
Version	J	K	L	J	K	L	12C	12C	12C	12C	12C	12C	14	14	03	03	03	A	B	C	R	S	T	536	Units
Input Current Max. 25°C	10	4	1	0.5	0.1	0.2	50	20	20	50	2	2	20	50	10	10	50	25	10	1	25	10	1	12	pA
Offset Drift Max.	5	2	1	50	25	10	50	20	20	50	10	25	20	50	5	10	20	75	25	50	75	25	50		µV/°C
CMRR Typ.	90*	90*	90*	80	80	80	80*	80*	92	92	100	100	80*	80*	80	80	80	86	86	86	86	86	86	70	dB
Gain Band Width Product	1	1	1	.25	.25	.25	4	4	3	3	1	1	3	3	1	1	1	1	1	1	1	1	1	1	MHz
Slew Rate (min.)	1	1	1	0.3	0.3	0.3	6	6	6	6	6	6	6	6	3	3	3	2.5	2.5	2.5	2.5	2.5	2.5	6	V/µS (typ.)
Output Current	10	10	10	10	10	10	5	5	5	5	5	5	5	20	5	5	5	5	5	5	5	5	5	30	mA
Temperature Range	C	C	C	C	C	C	I	I	I	I	I	I	I	I	I	I	I	I	I	I	M	M	M	-20°C +85°C	

M - 55 + 125
I - 25 + 85
C - 0 + 70

* = CMRR Over Reduced C.M. Voltage Range

ANALOG DEVICES	SIGNETICS DIRECT REPLACEMENT		SIGNETICS FUNCTIONAL EQUIVALENT	
	OLD	NEW	OLD	NEW
AD710CN	N5710A	μA710CA		
AD710CH	N5710T	μA710CT		
AD710H	S5710T	μA710T		
AD711CN	N5711A	μA711CA		
AD711CH	N5711K	μA711CK		
AD711H	S5711K	μA711K		
AD741CN	N5741A	μA741CA		
AD741CH	N5741T	μA741CT		
AD741H	S5741T	μA741T		
AD301AH	N53A1T	LM301AH		
AD201AH	N52A1T	LM201AH		
AD101AH	S51A1T	LM101AH		
AD308H	N5308T	LM308H		
AD108H	S5108T	LM108H		

FAIRCHILD	SIGNETICS DIRECT REPLACEMENT		SIGNETICS FUNCTIONAL EQUIVALENT	
	OLD	NEW	OLD	NEW
U5B7709312	S5709T	μA709T		
U5B7709393	N5709T	μA709CT		
U6A7709393	N5709A	μA709CA		
U5B7710312	S5710T	μA710T		
U5B7710393	N5710T	μA710CT		
U6A7710393	N5710A	μA710CA		
U5F7711312	S5711K	μA711K		
U5E7711393	N5711K	μA711CK		
U6A7711393	N5711A	μA711CA		
U5R7723312	S5723L	μA723L		
U5R7723393	N5723L	μA723CL		
U6A7723393	N5723A	μA723CA		
U5F7733312	S5733K	μA733K		
U5F7733393	N5733K	μA733CK		
U6A7733393	N5733A	μA733CA		
U6A7733312	S5733F	μA733F		
U5B7740312	S5740T	μA740T		
U5B7740393	N5740T	μA740CT		
U5B7741312	S5741T	μA741T		
U5B7741393	N5741T	μA741CT		
U6A7741393	N5741A	μA741CA		
U9T7741393	N5741V	μA741CV		
U7A7747312	S5747A	μA747A		
U7A7747393	N5747A	μA747CA		
U5F7747312	S5747K	μA747K		
U5F7747393	N5747K	μA747CK		
U5B7748312	S5748T	μA748T		
U5B7748393	N5748T	μA748CT		
U6A7748393	N5748A	μA748CA		
U9T7748393	N5748V	μA748CV		
SN7524	N7524B	SN7425N		
SN7525	N7525B	SN7525N		

MOTOROLA	SIGNETICS DIRECT REPLACEMENT		SIGNETICS FUNCTIONAL EQUIVALENT	
	OLD	NEW	OLD	NEW
MC1456G	N5556T	N5556T		
MC1458L	N5558F	N5558F		
MC1458G	N5558T	N5558T		
MC1495L	N5595F	N5595F		
MC1496G	N5596K	N5596K		
MC1556G	S5556G	S5556G		
MC1558L	S5558F	S5558F		
MC1558G	S5558T	S5558T		
MC1595L	S5595F	S5595F		
MC1596G	S5596K	S5596K		
MC1709CP	N5709A	μA709CA		
MC1709CG	N5709T	μA709CT		
MC1709F	S5709G	μA709G		
MC1709G	S5709T	μA709T		
MC1710CP	N5710A	μA710CA		
MC1710CG	N5710T	μA710CT		
MC1710F	S5710G	μA710G		
MC1710G	S5710T	μA710T		
MC1711CP	N5711A	μA711CA		
MC1711G	N5711K	μA711CK		
MC1711G	S5711K	μA711K		
MC1741CP	N5741A	μA741CA		
MC1741CG	N5741T	μA741CT		
MC1741G	S5741T	μA741T		
MC7520P	N7520B	SN7520N		
MC7521P	N7521B	SN7521N		
MC7522P	N7522B	SN7522N		
MC7523P	N7523B	SN7523N		
MC7524P	N7524B	SN7524N		
MC7525P	N7525B	SN7525N		
MC1445G			N5733K	μA733CK
MC1460			N5723L	μA723CL
MC1460R			S5723L	μA723L
MC1461G			N5723L	μA723CL
MC1461R			N5723L	μA723CL
MC1463R			N5723L	μA723CL
MC1469R			N5723L	μA723CL
MC1519G			S5733K	μA733K
MC1536G			S5741T	μA741T
MC1545G			S5733K	μA733K
MC1545L			S5733F	μA733F
MC1546L			S5733F	μA733F
MC1560G			S5723L	μA723L
MC1560R			S5723L	μA723L
MC1561G			S5723L	μA723L
MC1561R			S5723L	μA723L
MC1563R			S5723L	μA723L
MC1569R			S5723L	μA723L
MFC4060			N5723L	μA723L

NATIONAL	SIGNETICS DIRECT REPLACEMENT		SIGNETICS FUNCTIONAL EQUIVALENT	
	OLD	NEW	OLD	NEW
LM101H	S5101T	LM101H		
LM101AH	S51A1T	LM101AH		
LM101AF	S51A1G	LM101AF		
LM101AD	S51A1A	LM101AD		
LM107H	S5107T	LM107H		
LM107F	S5107G	LM107F		
LM107D	S5107A	LM107D		
LM201D	N5201A	LM201D		
LM201H	N5201T	LM201H		
LM201N	N5201V	LM201N		
LM201AH	N51A1T	LM201AH		
LM201AF	N51A1G	LM201AF		
LM201AD	N51A1A	LM101AD		
LM207H	S5107T	LM107H		
LM207F	S5107G	LM107F		
LM207D	S5107A	LM207D		
LM301AH	N53A1T	LM301AH		
LM301AN	N53A1V	LM301AN		
LM307H	N5307T	LM307H		
LM308H	N5308T	LM308H		
LM308AH	N53A8T	LM308AH		
LM309H	N5309H	LM309H		
LM309K	N5309K	LM309K		
LM709CH	N5709A	μA709CA		
LM709F	S5709G	μA709G		
LM709H	S5709T	μA709T		
LM710CN	N5710A	μA710CA		
LM710CH	N5710T	μA710CT		
LM710F	S5710G	μA710G		
LM710H	S5710T	μA710T		
LM711CN	N5711A	μA711CA		
LM711CH	N5711K	μA711CK		
LM711H	S5711K	μA711K		
LM723CN	N5723A	μA723CA		
LM723CH	N5723L	μA723CL		
LM723H	S5723L	μA723L		
LM741CH	N5741T	μA741CT		
LM741CN	N5741V	μA741CV		
LM741H	S5741T	μA741T		
LM748CH	N5748T	μA748CT		
LM748H	S5748T	μA748T		
LM1458H	N5558T	N5558T		
LM1458N	N5558V	N5558V		
LM1558H	S5558T	S5558T		
LM7520N	N7520B	SN7520N		
LM7521N	N7521B	SN7521N		
LM7522N	N7522B	SN7522N		
LM7523N	N7523B	SN7523N		
LM7524N	N7524B	SN7524N		
LM7525N	N7525B	SN7525N		
LH740ACH	N5740T	μA740CT		
LH740AH	S5740T	μA740T		
LH101			S5741T	μA741T
LH201			N5741T	μA741CT
LH740A			S5740T	μA740T
LH700AC			N5740T	μA740CT
LM100			S5723L	μA723L
LM104			S5723L	μA723L
LM105			S5723L	μA723L
LM106			S5710T	μA710T
LM110			S5741T	μA741T
LM210			S5741T	μA741T
LM300			N5723L	μA723CL
LM304			N5723L	μA723CL
LM306			N5710T	μA710CT
LM310			N5741T	μA710CT

RAYTHEON	SIGNETICS DIRECT REPLACEMENT		SIGNETICS FUNCTIONAL EQUIVALENT	
	OLD	NEW	OLD	NEW
RL709T	N5709T	μA709CT		
RM7090	S5709G	μA709G		
RM709T	S5709T	μA709T		
SG710CN	N5710A	μA710CA		
SG710CT	N5710T	μA710CT		
SG710T	S5710T	μA710T		
RL711T	N5711K	μA711CK		
RM711T	S5711K	μA711K		
RL733T	N5733K	μA733CK		
RM733T	S5733K	μA733K		
RC741T	N5741T	μA741CT		
RM741T	S5741T	μA741T		
RL101T	N5201T	LM201H		
RM101T	S5101T	LM101H		

SILICON GENERAL	SIGNETICS DIRECT REPLACEMENT		SIGNETICS FUNCTIONAL EQUIVALENT	
	OLD	NEW	OLD	NEW
SG709CN	N5709A	μA709CA		
SG709CT	N5709T	μA709CT		
SG709T	S5709T	μA709T		
SG710CN	N5710A	μA710CA		
SG710CT	N5710T	μA710CT		
SG710T	S5710T	μA710T		
SG711CN	N5711A	μA711CA		
SG711CT	N5711K	μA711CK		
SG711T	S5711K	μA711K		
SG723CN	N5723A	μA723CA		
SG723CT	N5723L	μA723CL		
SG723T	S5723L	μA723L		
SG733CN	N5733A	μA733CA		
SG733CT	N5733K	μA733CK		
SG733T	S5733K	μA733K		
SG741CN	N5741A	μA741CA		
SG741CT	N5741T	μA741CT		
SG741T	S5741T	μA741T		
SG748CT	N5748T	μA748CT		
SG748T	S5748T	μA748T		
SG14950	N5595F	N5595F		
SG15950	S5595F	S5595F		
SG1496N	N5596F	S5596F		
SG1496T	N5596K	N5596K		
SG1596T	S5596K	S5596K		
SG201N	N5201A	LM201D		
SG201T	N5201T	LM201H		
SG101T	S5101T	LM101H		
SG7520N	N7520B	SN7520N		
SG7521N	N7521B	SN7521N		
SG7522N	N7522B	SN7522N		
SG7523N	N7523B	SN7523N		
SG7524N	N7524B	SN7524N		
SG7525N	N7525B	SN7525N		

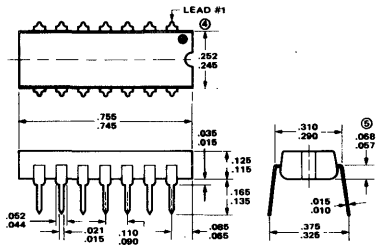
TI	SIGNETICS DIRECT REPLACEMENT		SIGNETICS FUNCTIONAL EQUIVALENT	
	OLD	NEW	OLD	NEW
SN7522N	N7522B	SN7522N		
SN7523N	N7523B	SN7523N		
SN7524N	N7524B	SN7524N		
SN7525N	N7525B	SN7525N		
SN5512L			S5733K	μA733K
SN7512L			N5733K	μA733CK
SN5514L			S5733K	μA733K
SN7514L			N5733K	μA733CK
SN52810L			S5710T	μA710T
SN72810L			N5710T	μA710CT
SN52510L			S5710T	μA710T
SN72510L			N5710T	μA710CT
SN5510L			S5733K	μA733K
SN52770L			S5740T	μA740T
SN72770L			N5740T	μA740CT
SN52771L			S5740T	μA740T
SN72771L			N5740T	μA740CT
SN72709	N5709A	μA709CA		
SN72709L	N5709T	μA709CT		
SN52709F	S5709G	μA709G		
SN52709L	S5709T	μA709T		
SN72710N	N5710A	μA710CA		
SN72710L	N5710T	μA710CT		
SN52710F	S5710G	μA710G		
SN52710L	S5710T	μA710T		
SN72711N	N5711A	μA711CA		
SN72711L	N5711K	μA711CK		
SN52711L	S5711K	μA711K		
SN72741N	N5741A	μA741CA		
SN72741L	N5741T	μA741CT		
SN72741P	N5741V	μA741CV		
SN72741L	S5741T	μA741T		
SN7520N	N7520B	SN7520N		
SN7521N	N7521B	SN7521N		
SN75450N	N75450A	SN75450N		
SN75450AN	N75450AA	SN75450AN		
SN75451N	N75451A	SN75451N		
SN75451AN	N75451AA	SN75451AN		

NOTES:

1. Signetics provides silicone dip 14 and 16 pin dual inline packages.
2. Cerdip will be available May 1, 1972.

SECTION 2
package types

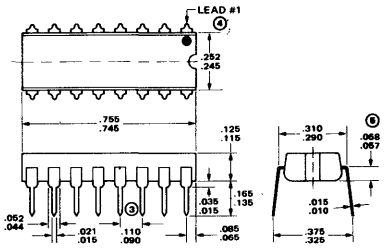
A PACKAGE



NOTES:

1. Lead Material: Alloy 42 or equivalent
2. Body Material: Silicone molded
3. Tolerances non-cumulative
4. Signetics symbol denotes Lead No. 1
5. Lead spacing shall be measured within this zone
6. Body dimensions do not include molding flash
7. Thermal resistance: $\theta J_A = .16^\circ C/mW$, $\theta J_C = .08^\circ C/mW$

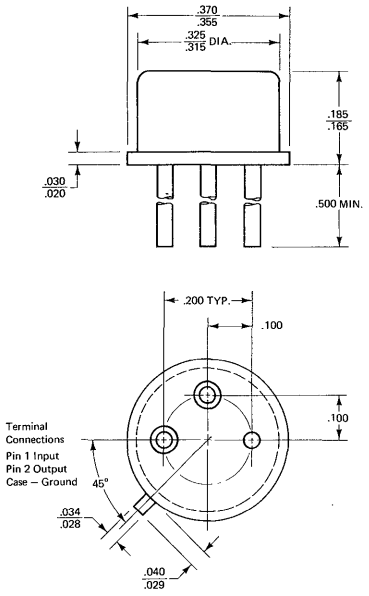
B PACKAGE



NOTES:

1. Lead Material: Alloy 42 or equivalent
2. Body Material: Silicone molded
3. Tolerances non-cumulative
4. Signetics symbol denotes Lead No. 1
5. Lead spacing shall be measured within this zone
6. Body dimensions do not include molding flash
7. Thermal resistance: $\theta J_A = .16^\circ C/mW$, $\theta J = .08^\circ C/mW$

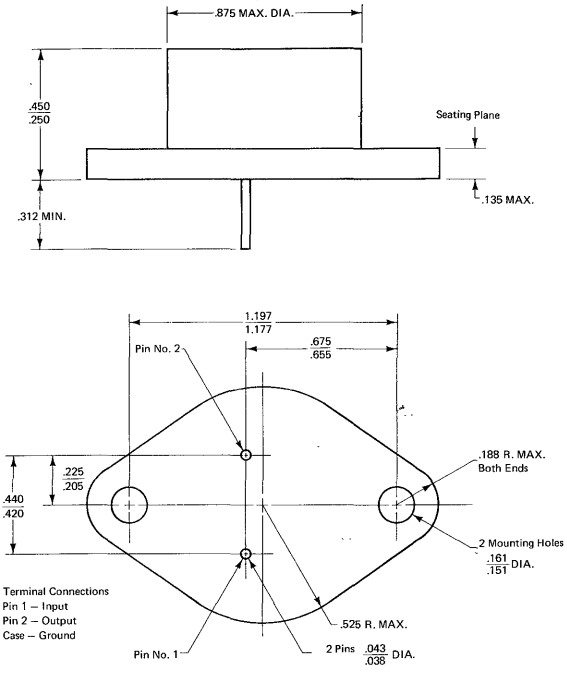
DB PACKAGE



NOTES:

1. Lead Material: Kovar Equivalent– Gold Plated
2. Body Material: Eyelet, Kovar or Equivalent– Gold Plated Glass Body
3. Lid Material: Nickel, Weld Seal

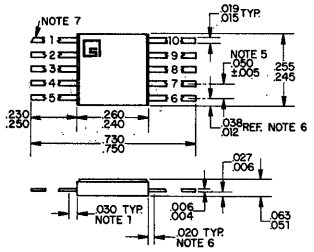
DA PACKAGE



NOTES:

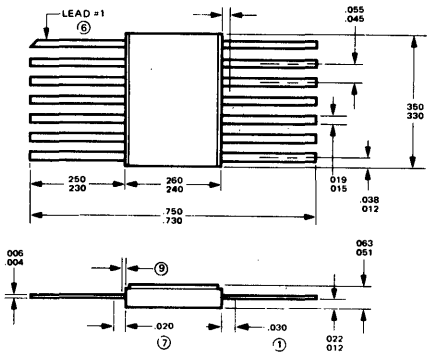
1. Lead Material No. 52 Alloy Gold Plated
2. Body Material: 1010 Steel Gold Plated
3. Lid Material: Steel Nickel Plated, Weld Seal

G PACKAGE



NOTES:
1. Recommended minimum offset before lead bend.
2. All leads weldable and solderable.
3. Thermal resistance: Θ_{J-A} = 0.3°C/mW.
4. All dimensions in inches.
5. Tolerances are non-cumulative.
6. Lead spacing dimensions apply to this area only.
7. Signetics symbol or angle cut identifies lead No. 1.

J PACKAGE



NOTES:

(1.) Recommended minimum offset before lead bend

2. Lead Material: Kovar or equivalent, gold plated
3. Body Material: Glass
4. Lid Material: Kovar, oxidized, glass seal

(5.) Tolerances non-cumulative

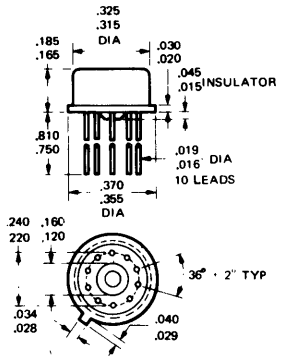
(6.) Signetics symbol or angle cut denotes Lead No. 1

(7.) Lead spacing shall be measured within this zone

8. Thermal Resistance: θJ_A = .300° C/mW, θJ_C = .140° C/mW

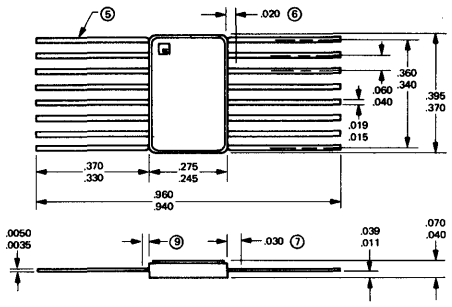
(9.) Maximum glass climb: .010

K PACKAGE



NOTES:
1. Lead Material: Kovar or Equivalent - Gold Plated
2. Body Material: Eyelet, Kovar or Equivalent - Gold Plated Glass Body
3. Lid Material: Nickel, Weld Seal

R PACKAGE



NOTES:
1. Lead Material: Kovar or equivalent, gold plated
2. Body Material: Top ring and Base - Kovar or equivalent. gold plated, glass body
3. Lid Material: Kovar or equivalent, gold plated, alloy seal

(4.) Tolerances non-cumulative

(5.) Signetics symbol denotes lead No. 1

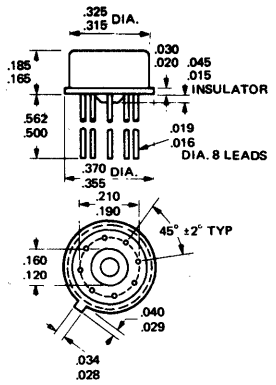
(6.) Lead spacing shall be measured within this zone

(7.) Recommended minimum offset before lead bend

8. Thermal Resistance: θJ_A = .155° C/mW, θJ_C = .070° C/mW

(9.) Maximum glass climb: .010

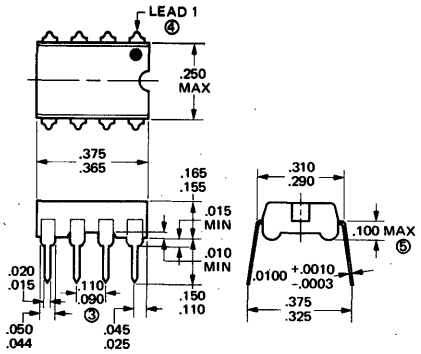
T PACKAGE



NOTES:

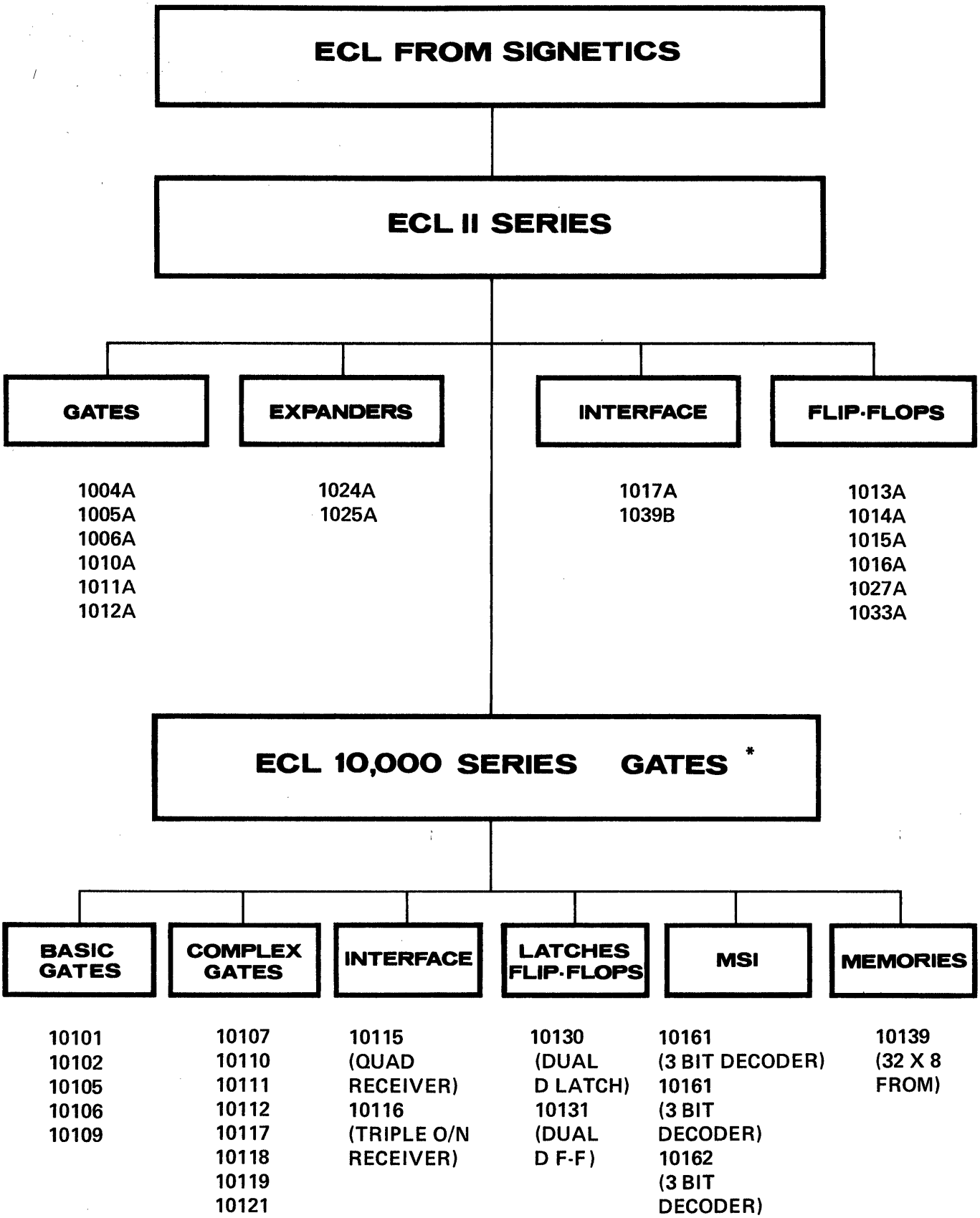
1. Lead Material: Kovar or equivalent - gold plated
2. Body Material: Eyelet, kovar or equivalent - gold plated glass body
3. Lid Material: Nickel, weld seal

V PACKAGE



NOTES:

1. Lead Material: Alloy 42 or equivalent, tinned
2. Body Material: Silicone Molded
3. Tolerances Non-Cumulative
4. Signetics Symbol Denotes Lead =1
5. Lead Spacing shall be Measured within this Zone
6. Body Dimensions do not Include Molding Flash



* TO BE ANNOUNCED

SECTION 3
operational amplifiers

DESCRIPTION

The 516 is a high gain operational amplifier with differential input and output. Features include large gain-bandwidth product, stable open-loop operation, high output voltage swing under load, high input resistance, wide common mode voltage range and high common mode rejection.

FEATURES

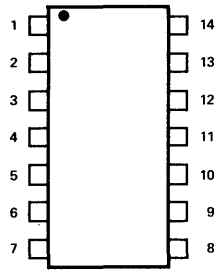
- OPEN LOOP VOLTAGE GAIN = NE516 15,000 / SE516 18,000
- OPEN LOOP GAIN STABILITY = ±20%
- OUTPUT VOLTAGE SWING = NE516 +10 Volts / SE516 +11 Volts
- DIFFERENTIAL INPUT RESISTANCE = NE516 100KΩ / SE516 400KΩ
- INPUT COMMON MODE VOLTAGE RANGE = 23 Volts
- COMMON MODE REJECTION RATIO = 100 db
- INPUT OFFSET CURRENT = NE516 100nA / SE516 300nA
- OPEN LOOP BANDWIDTH = 300 kHz

ABSOLUTE MAXIMUM RATINGS

Voltage Applied (Between Pins 1 and 6)	
NE516	34V
SE516	36V
Voltage Applied (Differential)	10V
Current Rating (Pins 1, 2, 6 and 10)	25mA
Current Rating (Other Pins)	10mA
Output Short Circuit Duration (25°C)	10sec
Storage Temperature	-65°C to +150°C
Operating Temperature	
NE516	0°C to +75°C
SE516	-55°C to +125°C
Junction Temperature	
NE516	150°C
SE516	175°C

PIN CONFIGURATION

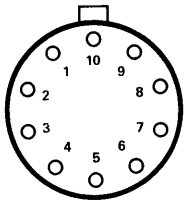
A PACKAGE
(Top View)



1. Input B
2. Com. 1A
3. NC
4. Com. 2B
5. NC
6. Output B
7. V^-
8. Output A
9. NC
10. Com 2A
11. Com. 1B
12. NC
13. Input A
14. V^+

ORDER PART NOS.
SE516A/NE516A

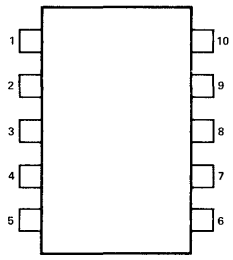
K PACKAGE



1. V^-
2. Output A
3. Com. 2A
4. Com. 1B
5. Input A
6. V^+
7. Input B
8. Com. 1A
9. Com. 2B
10. Output B

ORDER PART NOS.
SE516K/NE516K

G PACKAGE

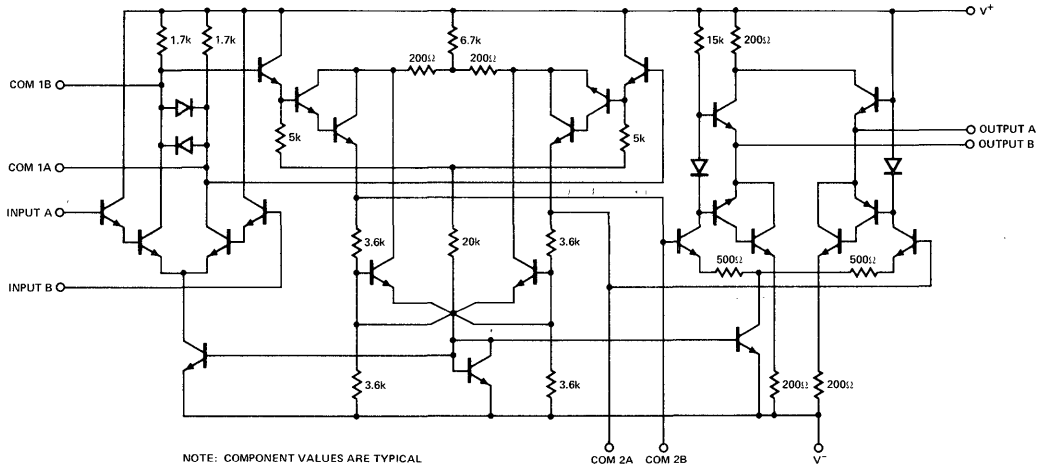


1. V^-
2. Output A
3. Com. 2A
4. Com. 1B
5. Input A
6. V^+
7. Input B
8. Com. 1A
9. Com. 2B
10. Output B

ORDER PART NOS.
SE516G/NE516G

Maximum ratings are limiting values above which serviceability may be impaired.

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (Notes: 1, 2, 3, 8) (Standard Conditions: V_E = +15V, V_K = -15V, V_A = 0V)

PARAMETERS	TEST CONDITIONS	NE516				SE516				UNITS
		MIN	TYP	MAX	TEMP.	MIN	TYP	MAX	TEMP.	
Open Loop Voltage Gain (DC)	$R_L \geq 2k\Omega$,		16,000		0°C		22,000		-55°C	V/V
	Notes 5, 7	10,000	15,000		+25°C	13,000	18,000		+25°C	V/V
		8,000	13,000		+75°C	10,000	15,000		+125°C	V/V
Open Loop Voltage Gain (AC)	$R_L \geq 2k\Omega$, f = 250 kHz, Note 7	8,000	12,000		+25°C	10,000	15,000		+25°C	V/V
Input Offset Voltage	Note 6		5.0	15	0°C		3.0	10	-55°C	mV
			5.0	15	+25°C		3.0	10	+25°C	mV
			5.0	15	+75°C		3.0	10	+125°C	mV
Input Bias Current	Note 6		1.5	4.5	0°C		0.6	2.0	-55°C	μA
			1.0	3.0	+25°C		0.3	1.0	+25°C	μA
			0.6		+75°C		0.15		+125°C	μA
Input Offset Current	Note 6						0.06		-55°C	μA
			0.1	0.6	+25°C		0.03	0.2	+25°C	μA
							0.02		+125°C	μA
Differential Input Resistance	Notes 4, 6					40	150		-55°C	kΩ
		40	100		+25°C	100	400		+25°C	kΩ
							1,000		+125°C	kΩ
Input Common Mode Range		+8.0	+10		+25°C	+8.0	+10		+25°C	V
		-12	-13			-12	-13			
Power Supply Sensitivity			50		+25°C	50			+25°C	μV/V
(Referred to Input)			50		+25°C	50			+25°C	μV/V
Balanced Output dc Level	$R_L \geq 2k\Omega$, Note 6					-2.0	+0.5	+2.5	-55°C	V
		-2.5	0	+2.5	+25°C	-1.5	0	+1.5	+25°C	V
						-2.5	-0.5	+2.0	+125°C	V
Output Voltage Swing	$R_L \geq 2k\Omega$	±8.0	±10		0°C	±10	±11		-55°C	V
		±8.0	±10		+25°C	±10	±11		+25°C	V
		±8.0	±10		+75°C	±10	±11		+125°C	V
Output Resistance	Note 6		500		+25°C		500		+25°C	Ω
Common Mode Rejection Ratio			100		+25°C		100		+25°C	dB
Power Supply Current	Note 6		5.0		0°C		5.0		-55°C	mA
			5.0	6.0	+25°C		5.0	6.0	+25°C	mA
			5.0	6.0	+75°C		5.0	6.0	+125°C	mA

Letter subscripts refer to pins on circuit schematic.

NOTES:

1. Voltage and current subscripts refer to pin numbers.
2. All measurements are referenced to an external ground. Positive current flow is defined as into the terminal indicated.
3. All specifications herein apply for interchange of voltages and currents at Pins 5 and 7.
4. Differential Input Resistance is a value computed from input bias current limits.
5. Output voltage swing = 5V peak to peak.
6. Adjust V_5 to obtain V_2 = V10.
7. Differential input, single ended output.

DESCRIPTION

The 531 is a fast slewing high performance operational amplifier which retains D.C. performance equal to the best general purpose types while providing far superior large signal A.C. performance. A unique input stage design allows the amplifier to have a large signal response nearly identical to its small signal response. The amplifier can be compensated for truly negligible overshoot with a single capacitor. In applications where fast settling and superior large signal bandwidths are required, the amplifier out performs conventional designs which have much better small signal response. Also, because the small signal response is not extended, no special precautions need be taken with circuit board layout to achieve stability. The high gain, simple compensation and excellent stability of this amplifier allow its use in a wide variety of instrumentation applications.

FEATURES

- 35V/μsec SLEW RATE AT UNITY GAIN
- PIN FOR PIN REPLACEMENT FOR μA709, μA748 OR LM101
- COMPENSATED WITH A SINGLE CAPACITOR
- SAME LOW DRIFT OFFSET NULL CIRCUITRY AS μA741
- SMALL SIGNAL BANDWIDTH 1 MHz
- LARGE SIGNAL BANDWIDTH 500KHz
- TRUE OP AMP D.C. CHARACTERISTICS MAKE THE 531 THE IDEAL ANSWER TO ALL SLEW RATE LIMITED OPERATIONAL AMPLIFIER APPLICATIONS.

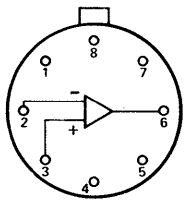
NOTES:
1. Rating applies for case temperatures to 125 °C, derate linearly at 6.5mW/°C for ambient temperatures above +75°C
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	300mW
Differential Input Voltage	±15V
Common Mode Input Voltage (Note 2)	±15V
Voltage Between Offset Null and V^-	±0.5V
Operating Temperature Range	
NE531	0°C to +70°C
SE531	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Solder, 60 sec.)	300°C
Output Short Circuit Duration (Note 3)	Indefinite

PIN CONFIGURATION

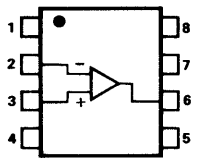
T PACKAGE
(Top View)



1. Offset Null
2. Inverting Input
3. Noninverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp.

ORDER PART NOS.
SE531T/NE531T

V PACKAGE

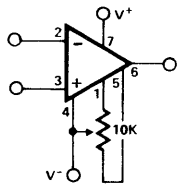


1. Offset Null
2. Inverting Input
3. Noninverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp.

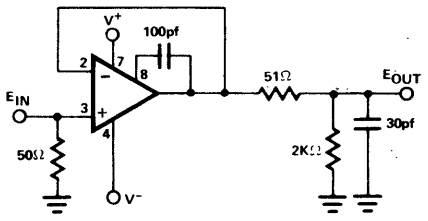
ORDER PART NO. NE531V

TEST CIRCUITS

OFFSET NULL CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT



GENERAL ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$, $T_A = 25°C$ Unless Otherwise Specified)

NE531

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10K\Omega$		2.0	6	mV
Input Offset Current			50	200	nA
Input Bias Current			0.4	1.5	μA
Input Resistance			20		MΩ
Input Voltage Range		±10			Volts
Common Mode Rejection Ratio	$R_S \leq 10K\Omega$	70	100		dB
Supply Voltage Rejection Ratio	$R_S \leq 10K\Omega$		10	150	μV/V
Large Signal Voltage Gain	$R_L \geq 2K\Omega$, $V_{OUT} = \pm 10V$	20,000	60,000		
Output Resistance			75		Ω
Supply Current			5.5	10	mA
Power Consumption			165	300	mW
Full Power Bandwidth			500		KHz
Settling Time, 1%	$A_V = +1$, $V_{IN} = \pm 10V$		1.5		μsec
Settling Time, .01%	$A_V = +1$, $V_{IN} = \pm 10V$		2.5		μsec
Large Signal Overshoot	$A_V = +1$, $V_{IN} = \pm 10V$		2		%
Small Signal Overshoot	$A_V = +1$, $V_{IN} = 400mV$		5		%
Small Signal Risetime	$A_V = +1$, $V_{IN} = 400mV$		300		nsec
The Following Apply for $0°C \leq T_A \leq +70°C$:					
Input Offset Voltage	$R_S \leq 10K\Omega$			7.5	mV
Input Offset Current	$T_A = +70°C$			200	nA
	$T_A = 0°C$			300	nA
Input Bias Current	$T_A = +70°C$			1.5	μA
	$T_A = 0°C$			2.0	μA
Large Signal Voltage Gain	$R_L \geq 2K\Omega$, $V_{OUT} = \pm 10V$	15,000			
Output Voltage Swing	$R_L \geq 2K\Omega$	±10	±13		Volts
Slew Rate	$A_V = 100$		35		V/μs
	$A_V = 10$		35		V/μs
	$A_V = 1$ (non-inverting)		30		V/μs
	$A_V = 1$ (inverting)		35		V/μs
Supply Current	$T_A = +70°C$		4.5	5.5	mA

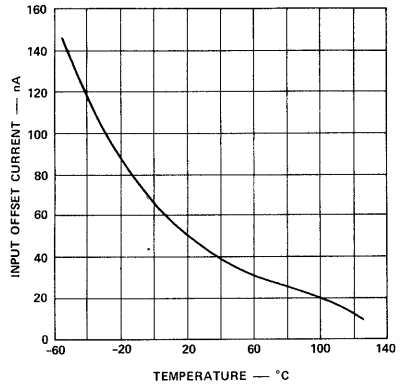
SE531

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10K\Omega$		2.0	5.0	mV
Input Offset Current			30	200	nA
Input Bias Current			300	500	nA
Input Resistance			20		MΩ
Input Voltage Range		±10			Volts
Large Signal Voltage Gain	$R_L \geq 2K\Omega$, $V_{OUT} = \pm 10V$	50,000	100,000		
Output Resistance			75		Ω
Supply Current			5.5	7.0	mA
Power Consumption			165	210	mW
Full Power Bandwidth			500		KHz
Settling Time, 1%	$A_V = +1$, $V_{IN} = \pm 10V$		1.5		μsec
Settling Time, .01%	$A_V = +1$, $V_{IN} = \pm 10V$		2.5		μsec
Large Signal Overshoot	$A_V = +1$, $V_{IN} = \pm 10V$		2		%
Small Signal Risetime	$A_V = +1$, $V_{IN} = 400mV$		300		nsec
Small Signal Overshoot	$A_V = +1$, $V_{IN} = 400mV$		5		%
Slew Rate	$A_V = 100$		35		V/μs
	$A_V = 10$		35		V/μs
	$A_V = 1$ (non-inverting)		30		V/μs
	$A_V = 1$ (inverting)		35		V/μs
The following apply for $-55°C \leq T_A \leq +125°C$:					
Input Offset Voltage	$R_S \leq 10K\Omega$			6	mV
Input Offset Current	$T_A = +125°C$			200	nA
	$T_A = -55°C$			500	nA
Input Bias Current	$T_A = +125°C$			500	nA
	$T_A = -55°C$			1.5	μA
Common Mode Rejection Ratio	$R_S \leq 10K\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10K\Omega$		10	150	μV/V
Large Signal Voltage Gain	$R_L = 2K\Omega$, $V_{OUT} = \pm 10V$	25,000			
Output Voltage Swing	$R_L = 2K\Omega$	±10	±13		V
Supply Current	T_A +125°C		4.5	5.5	mA

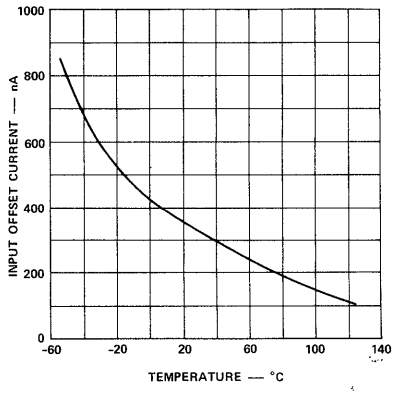
NOTES:
All AC parametric testing is performed using the conditions of the transient response test circuit, page 1.

TYPICAL PERFORMANCE CHARACTERISTICS (V_S = ±15V, T_A = +25°C unless otherwise noted)

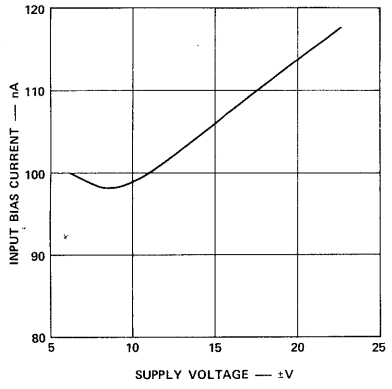
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



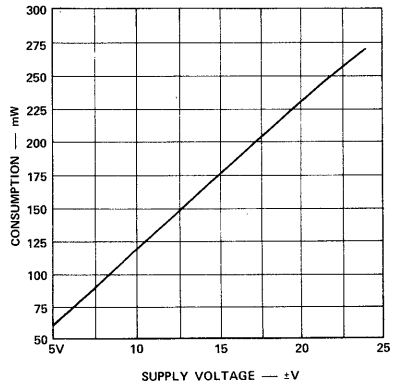
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



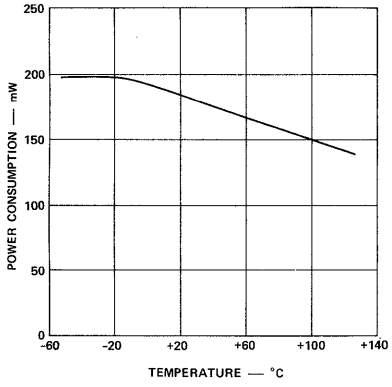
INPUT BIAS CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



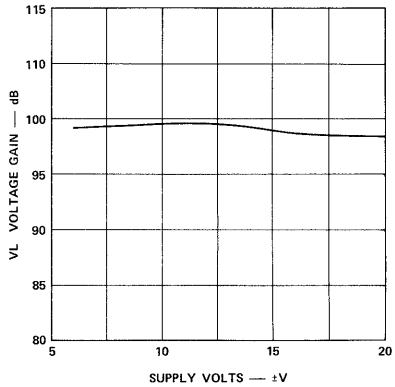
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



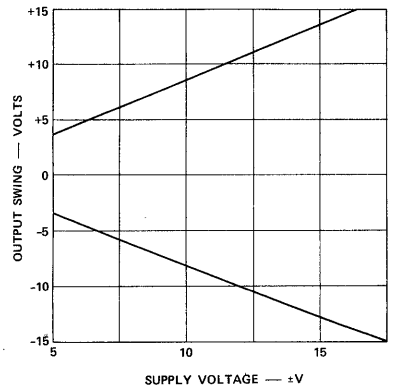
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



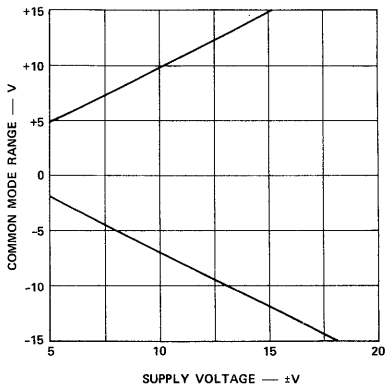
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



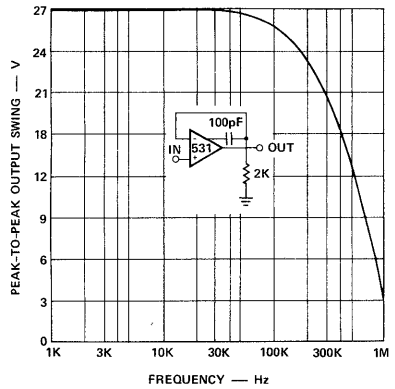
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

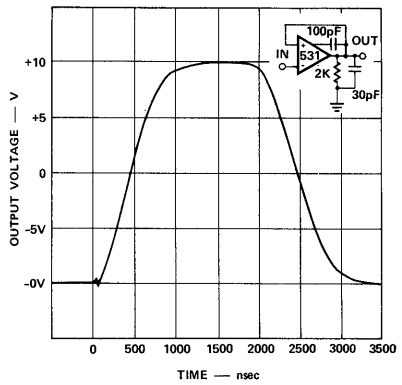


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

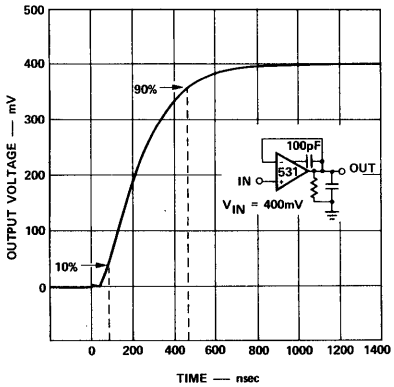


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

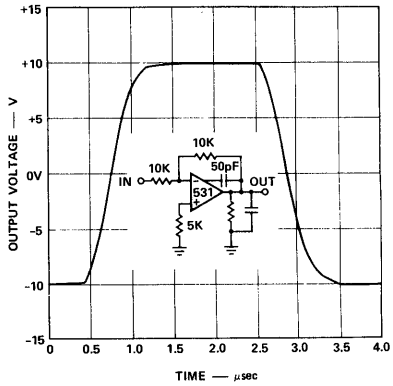
VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



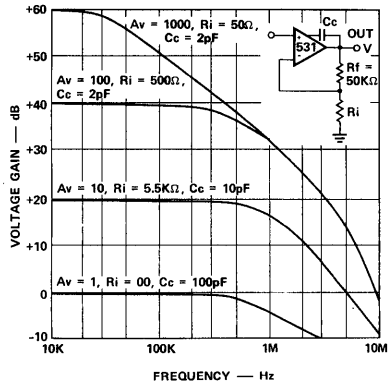
VOLTAGE FOLLOWER TRANSIENT RESPONSE



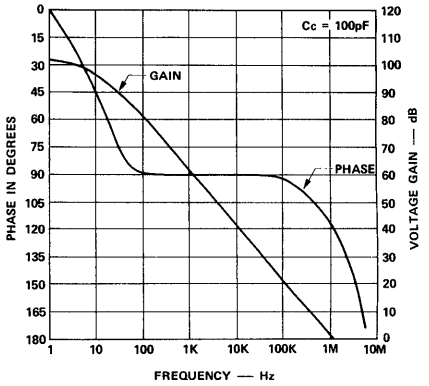
UNITY GAIN INVERTING AMPLIFIER LARGE SIGNAL RESPONSE



CLOSED LOOP NON-INVERTING VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

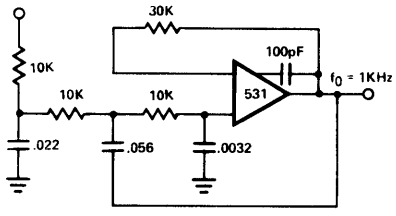


OPEN LOOP PHASE RESPONSE AND VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

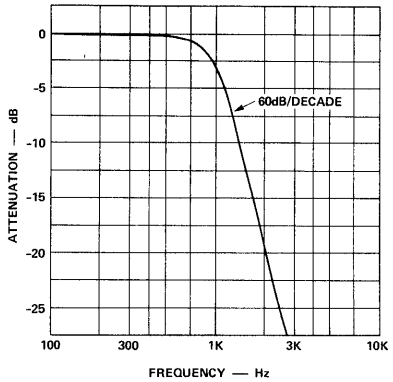


TYPICAL APPLICATIONS

3 POLE ACTIVE LOW PASS FILTER BUTTERWORTH MAXIMALLY FLAT RESPONSE*



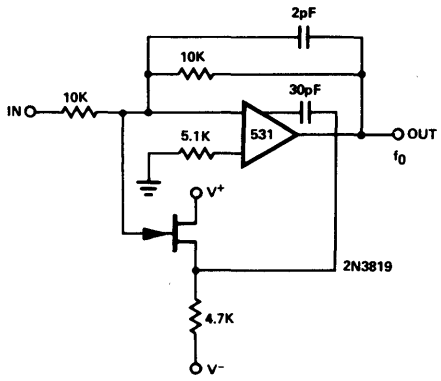
RESPONSE OF 3-POLE ACTIVE BUTTERWORTH MAXIMALLY FLAT FILTER



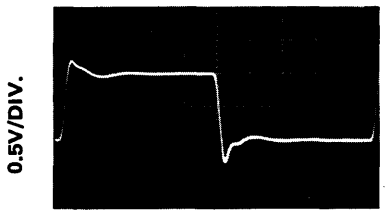
*Reference — EDN Dec. 15, 1970
Simplify 3-Pole Active Filter Design
A. Paul Brokow

TYPICAL APPLICATIONS (Cont'd.)

HIGH SPEED INVERTER (10MHz Bandwidth)

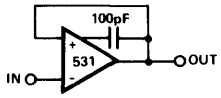


PULSE RESPONSE
HIGH SPEED INVERTER

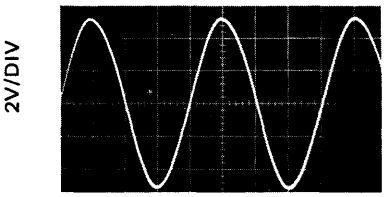


200nsec/DIV

FAST SETTLING VOLTAGE FOLLOWER



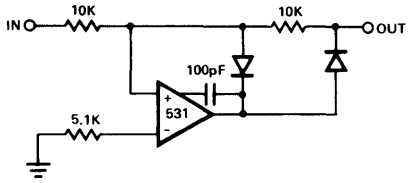
LARGE SIGNAL RESPONSE
VOLTAGE FOLLOWER



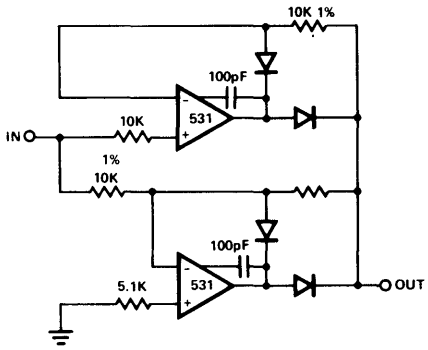
0.5μs/DIV f = 500KHz

PRECISION RECTIFIERS

(a) HALF WAVE

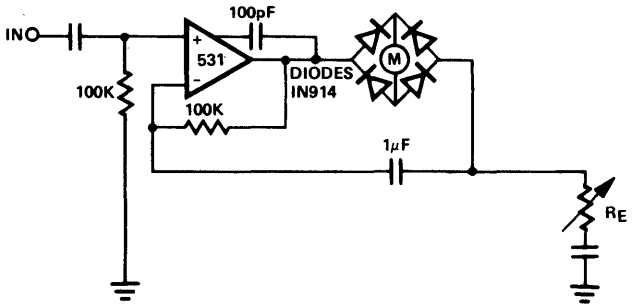


(b) FULL WAVE

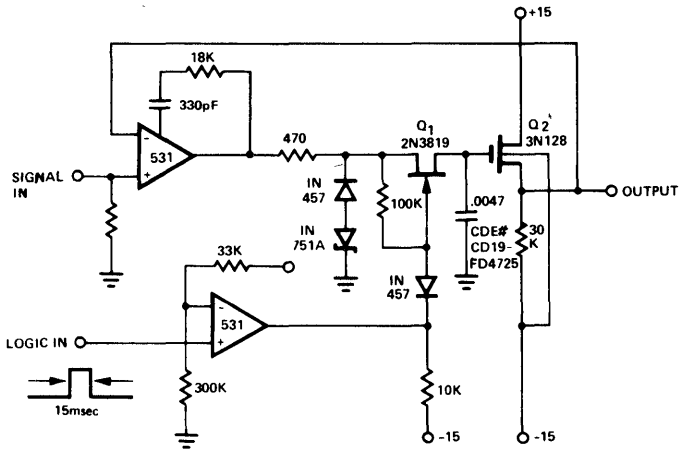


TYPICAL APPLICATIONS (Cont'd.)

AC MILLIVOLTMETER



SAMPLE AND HOLD



DESCRIPTION

The 533 is a high performance operational amplifier specifically designed for applications requiring low power consumption or reduced supply voltage. The 533 features single capacitor compensation, input and output protection and is pin compatible with the μA709, μA748, and LM101.

FEATURES

- LESS THAN 100μW POWER DISSIPATION
- LOW INPUT OFFSET VOLTAGE
- LOW INPUT BIAS AND OFFSET CURRENTS
- HIGH COMMON MODE AND POWER SUPPLY REJECTION RATIOS
- EXCELLENT TEMPERATURE STABILITY
- NO LATCH UP

ABSOLUTE MAXIMUM RATINGS

Supply Voltage		±18V
Differential Input Voltage		±5V
Input Voltage		$\pm V_S$
Operating Temperature Range	SE533	-55°C to +125°C
	NE533	0°C to 70°C
Lead Temperature (Solder, 60 sec)		300°C
Output Short Circuit Duration (Note 1)		Indefinite

1. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

PULSE RESPONSE TEST CIRCUIT

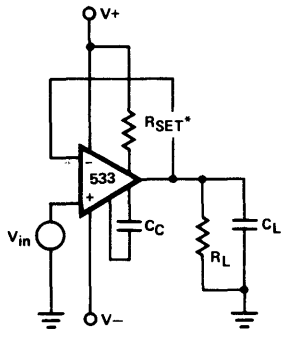
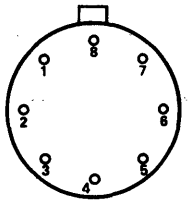


FIGURE 1

PIN CONFIGURATION

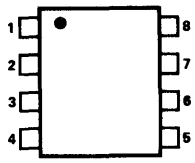
T PACKAGE
(Top View)



1. Compensation
2. Inverting Input
3. Noninverting Input
4. V^-
5. Compensation
6. Output
7. V^+
8. R_{SET}

ORDER PART NOS.
SE533T/NE533T

V PACKAGE
(Top View)



1. Compensation
2. Inverting Input
3. Noninverting Input
4. V^-
5. Compensation
6. Output
7. V^+
8. R_{SET}

ORDER PART NOS.
SE533V/NE533V

NOTE:
R_{SET} establishes internal biasing of the amplifier to allow for a wide range of supply voltages. Recommended values of R_{SET} are 3.9mΩ at V_s = ±3V or 15mΩ at V_s = ±15V. Consult graphs for intermediate values.

ELECTRICAL CHARACTERISTICS (NOTE 1)

PARAMETER	CONDITIONS	NE533			SE533			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	V_S = ±3V, and ±15, R_S = 100KΩ			3			2	mV
Input Offset Voltage	V_S = ±3V, and ±15V, R_S=100K, T_A=25°C		1	2		0.5	1	mV
Input Bias Current	V_S = ±3V, and ±15V			30			30	nA
Input Bias Current	V_S = ±3V, and ±15V, T_A = 25°C		5	10		2	10	nA
Input Offset Current	V_S = ±3V, and ±15V			10			10	nA
Input Offset Current	V_S = ±3V, and ±15V, T_A = 25°C		1	5		0.5	5	nA
Input Resistance	V_S = ±3V, and ±15V	15			15			mΩ
Input Resistance	V_S = ±3V, and ±15V, T_A = 25°C	30	60		30	60		mΩ
Input Voltage Range	V_S = ±3V	±1.50			±1.50			V
Input Voltage Range	V_S = ±15V	±10			±10			V
Large Signal Voltage Gain	V_S = ±3V, R_L ≥ 20kΩ, V_{out} = ±1.0V	10			10			V/mV
Large Signal Voltage Gain	V_S = ±3V, R_L ≥ 20kΩ, V_{out} = ±1.0V, T_A = 25°C	12	15		16	20		V/mV
Large Signal Voltage Gain	V_S = ±15V, R_L ≥ 50kΩ, V_{out} = ±10V	25			25			V/mV
Large Signal Voltage Gain	V_S = ±15V, R_L ≥ 50kΩ, V_{out} = ±10V, T_A = 25°C	40	60		50	70		V/mV
Output Short Circuit Current	V_S = ±3V, ±15V, T_A = 25°C		6			6		mA
Common Mode Rejection Ratio	V_S = ±3V, R_S ≤ 100kΩ	74			80			dB
Common Mode Rejection Ratio	V_S = ±3V, R_S ≤ 100kΩ, T_A = 25°C	84	105		90	100		dB
Common Mode Rejection Ratio	V_S = ±15V, R_S ≤ 100kΩ	84			80			dB
Common Mode Rejection Ratio	V_S = ±15V, R_S ≤ 100kΩ, T_A = 25°C	90	110		100	120		dB
Power Supply Rejection Ratio	V_S = ±3V to ±15V, R_S ≤ 100kΩ			100			50	μV/V
Power Supply Rejection Ratio	V_S = ±3V to ±15V, R_S ≤ 100kΩ, T_A=25°C T_A = 25°C		20	50		10	25	μV/V
Supply Current	V_S = ±3V V_O= OV			20			16	μA
Supply Current	V_S = ±15V V_O= OV			50			30	μA
Power Dissipation	V_S = ±3V V_O= OV			120			96	μW
Power Dissipation	V_S = ±15V V_O= OV			1.5			0.9	mW

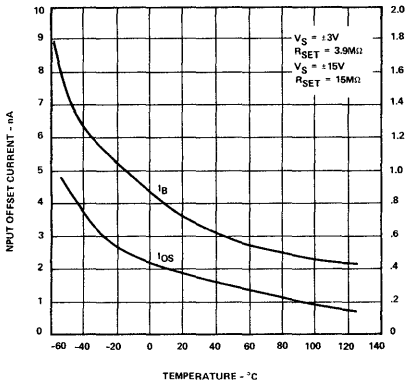
TRANSIENT RESPONSE (See Figure 1)

Rise Time	V_S = ±3V, R_L = 20k, C_L = 100pF		2			2		μsec
Overshoot	V_{in} = 10mV, C_C = 0.05μf		10			10		%
Slew Rate	T_A = 25°C		5			5		mV/μsec
Rise Time	V_S = ±15V, R_L = 50k, C_C = 100pF		1			1		μsec
Overshoot	V_{in} = 20V, C_C = 0.05μf		10			10		%
Slew Rate	T_A = 25°C		30			30		mV/μsec

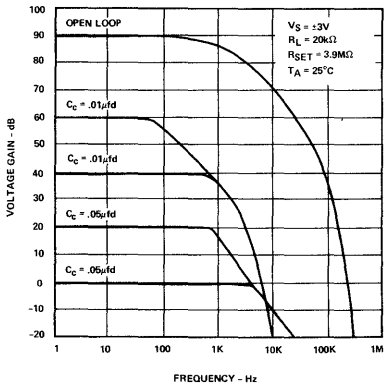
NOTE 1: Specifications apply for the full temperature range unless otherwise stated. For V_S = ±3V. R_{set} = 3.9mΩ; for V_S = ±15V. R_{set} = 15mΩ

TYPICAL CHARACTERISTIC CURVES

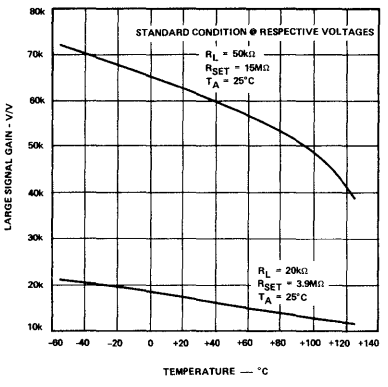
INPUT BIAS AND OFFSET CURRENTS AS FUNCTIONS OF AMBIENT TEMPERATURE



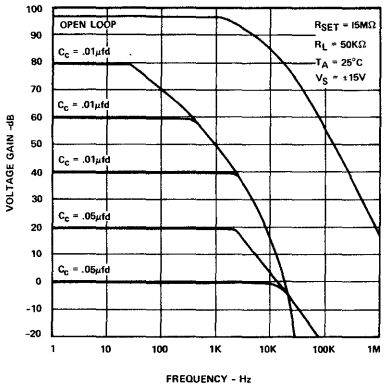
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



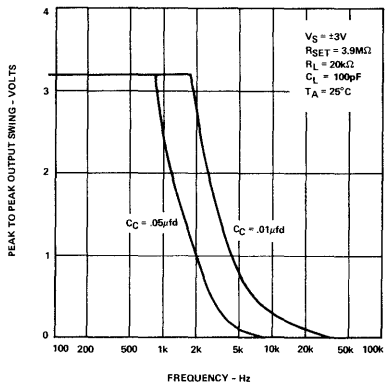
LARGE SIGNAL OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF AMBIENT TEMPERATURE



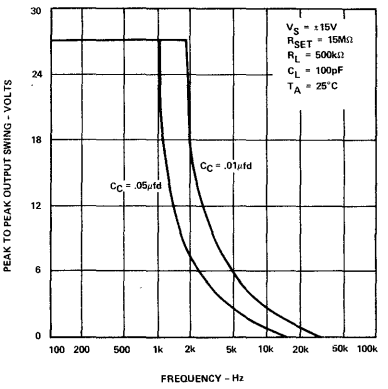
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



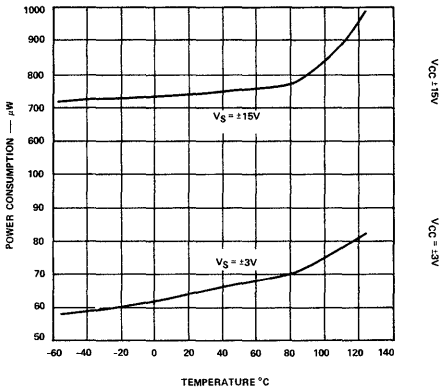
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



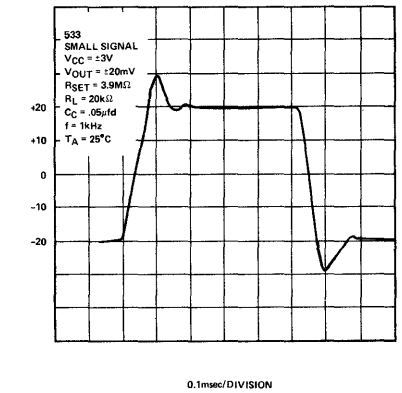
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



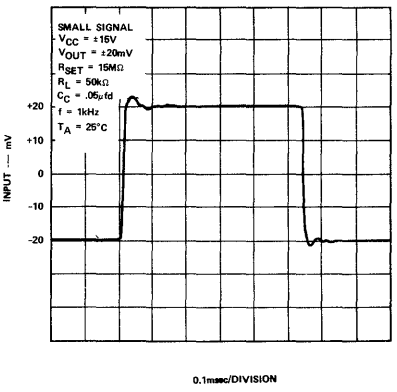
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



SMALL SIGNAL UNITY GAIN TRANSIENT RESPONSE

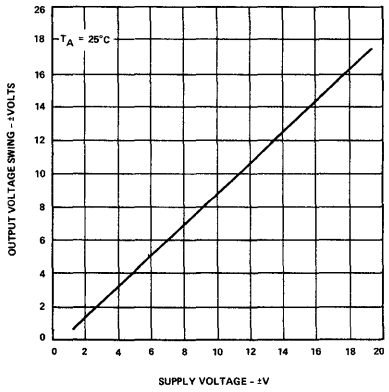


SMALL SIGNAL UNIT GAIN TRANSIENT RESPONSE

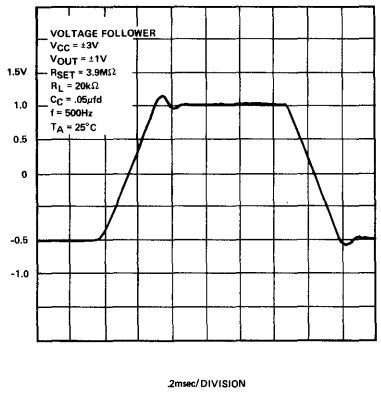


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

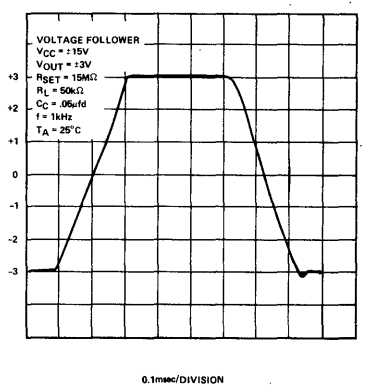
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



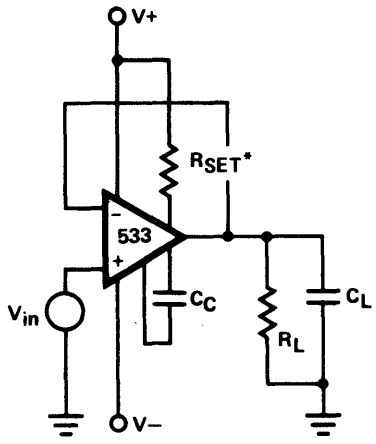
UNITY GAIN VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



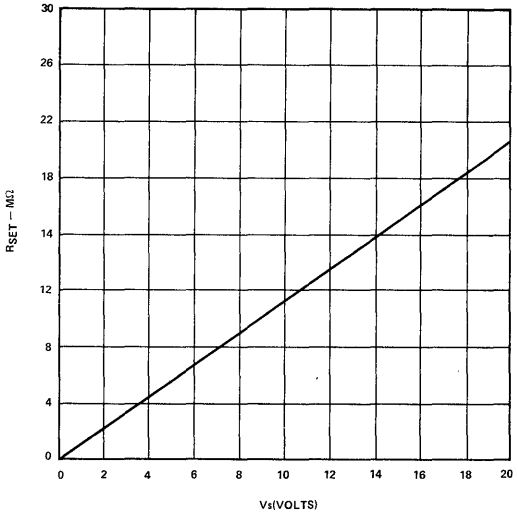
UNITY GAIN VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE



TYPICAL APPLICATIONS



RECOMMENDED VALUES OF R_{SET} FOR INTERMEDIATE SUPPLY VOLTAGES



DESCRIPTION

The 536 is a special purpose high performance operational amplifier utilizing a FET input stage for extremely high input impedance and low input current.

The device features internal compensation, standard pinout, wide differential and common mode input voltage range, high slew rate and high output drive capability.

FEATURES

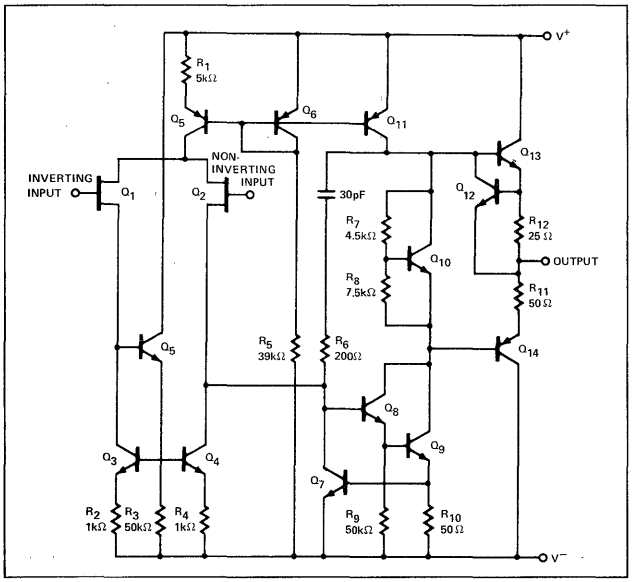
- 5pA INPUT BIAS CURRENT
- INPUT AND OUTPUT PROTECTION
- OFFSET NULL CAPABILITY
- INTERNALLY COMPENSATED
- 6V/μsec SLEW RATE
- STANDARD PINOUT
- 1 MHz UNITY GAIN BANDWIDTH

ABSOLUTE MAXIMUM RATING

Supply Voltage		±22V
Differential Input Voltage Range		±30V
Common Mode Input Voltage Range		$\pm V_S$
Power Dissipation (Note 1)		500mW
Operating Temperature Range	SU536T	−55°C to +85° C
	NE536T	0°C to +70° C
Storage Temperature Range		−65°C to +150° C
Lead Temperature (Solder, 60 sec)		300°C
Output Short Circuit Duration (Note 2)		Indefinite

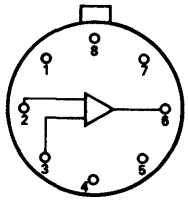
NOTES:
1. Rating applies for case temperatures to +25 °C; derate linearly at 6.5mW/ °C for ambient temperatures above 75 °C.
2. Short circuit may be to ground or either supply. Rating applies to +125 °C case temperature or +75 °C ambient temperature.

EQUIVALENT CIRCUIT



PIN CONFIGURATION

T PACKAGE
(Top View)

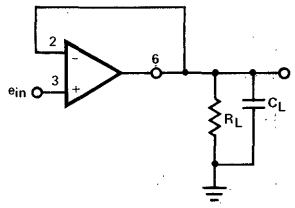


1. Offset Null
2. Inverting Input
3. Non-inverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. NC

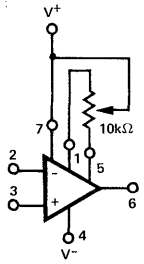
ORDER PART NOS. SE536T/NE536T

TEST CIRCUITS

VOLTAGE FOLLOWER CIRCUIT



OFFSET NULL CIRCUIT



ELECTRICAL CHARACTERISTICS (SU536: $\pm 6V \leq V_S \leq \pm 20V$; NE536: $V_S = \pm 15V$ unless otherwise noted.)

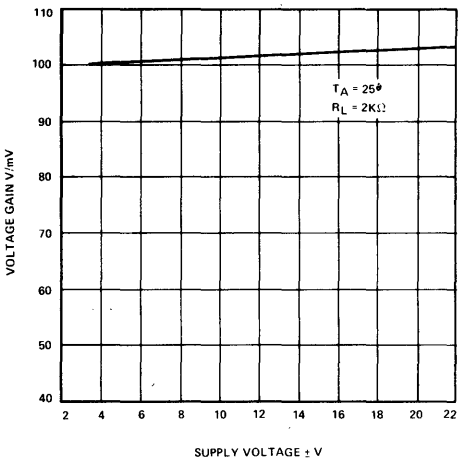
PARAMETER	TEST CONDITIONS	SU536			NE536			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISITICS								
Large Signal Voltage Gain @ +25°C	$V_S = \pm 15$ V, $V_{OUT} = \pm 10V$	50	100		50	100		V/mV
Over Temperature Range	$R_L \geq 2k\Omega$	50	100		25	100		V/mV
Input Offset Voltage @ +25°C			7.5	20		30	90	mV
Over Temperature Range			7.5	30		30		mV
vs Temperature (drift)			20			30		µV/°C
vs Common Mode Voltage (C.M.R.R.)	$V_{IN} = \pm 10V$, $R_S \leq 10k\Omega$	70	80		64	80		dB
vs Power Supply (P.S.R.R.)	Note I, $R_S \leq 10k\Omega$		50	150		100	300	µV/V
Input Current @ +25°C			5	30		30	100	pA
Over Temperature Range	Either Input		250	3000				pA
vs Temperature (drift)			Typ. Doubles Every 10°C					
Input Offset Current @ +25°C			5			5		pA
Over Temperature (drift)								
Input Impedance								
Differential Resistance	$T_A = +25°C$		10^{14}			10^{14}		Ω
Differential Capacitance	$T_A = +25°C$		6			6		pF
Input Noise (0.1Hz – 100kHz)								
Voltage Noise			20			20		µVrms
Common Mode Voltage Range	$V_S = \pm 15V$	±10	±11		±10	±11		V
OUTPUT CHARACTERISTICS								
Output Current	$V_S = \pm 15V$	5			5			mA
Open Loop Output Impedance			100			100		Ω
Output Voltage Swing	$V_S = \pm 15V$, $R_L \geq 2k\Omega$	±10	±12		±10	±10		V
	$V_S = \pm 15V$, $R_L \geq 10k\Omega$	±12	±13		±12	±13		V
Short Circuit Current	$V_S = \pm 15V$, $T_A = +25°C$		17			17		mA
FREQUENCY AND TRANSIENT RESPONSE								
Gain Bandwidth Product	$V_S = \pm 15V$, $T_A = +25°C$, $A = 100$		1			1		MHz
Unity Gain Frequency	$V_S = \pm 15V$, $T_A = +25°C$		1			1		MHz
Full Power Bandwidth	$V_S = \pm 15V$, $T_A = +25°V$		100			100		kHz
Slew Rate								
Inverter	$V_S = \pm 15V$, $T_A = +25°C$, $A = -1$		6			6		V/µs
Follower	$V_S = \pm 15V$, $T_A = +25°C$, $A = +1$		6			6		V/µs
POWER SUPPLY REQUIREMENT								
Power Supply Range		±6		±20	±6		±18	V
Quiescent Supply Current	$V_S = \pm 20V$, $V_{OUT} = 0V$, $T_A = +25°C$		4.5	5.5				mA
	$V_S = \pm 15V$, $V_{OUT} = 0V$, $T_A = +25°C$					6.0	8.0	mA
Quiescent Power Dissipation	$V_S = \pm 15V$, $V_{OUT} = 0V$, $T_A = +25°C$		180			180		mW

Parameters are tested over temperature range unless otherwise noted.

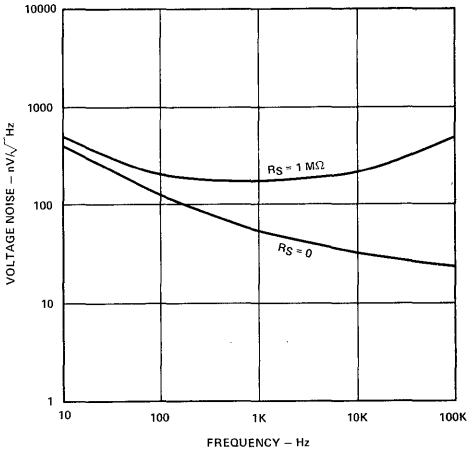
NOTE I: SU536: $V_S = \pm 6V$ to $\pm 20V$
NE536: $V_S = \pm 6V$ to $\pm 15V$

TYPICAL CHARACTERISTIC CURVES

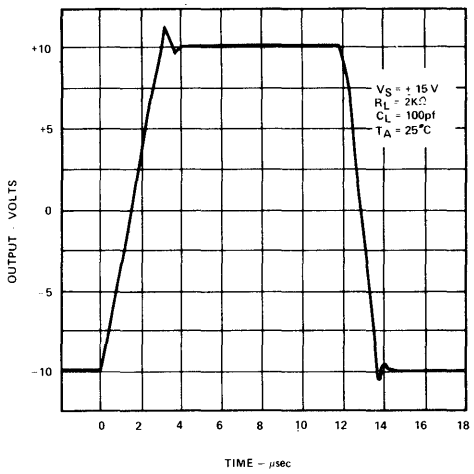
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



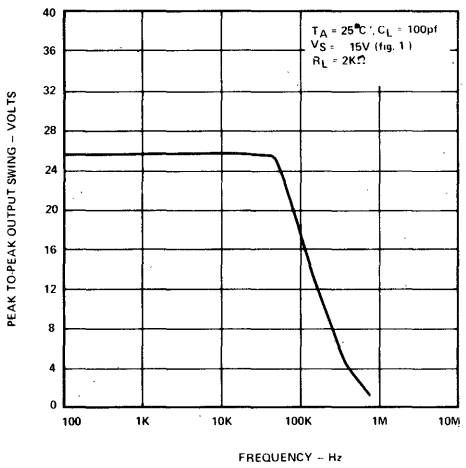
INPUT VOLTAGE NOISE AS A FUNCTION OF FREQUENCY



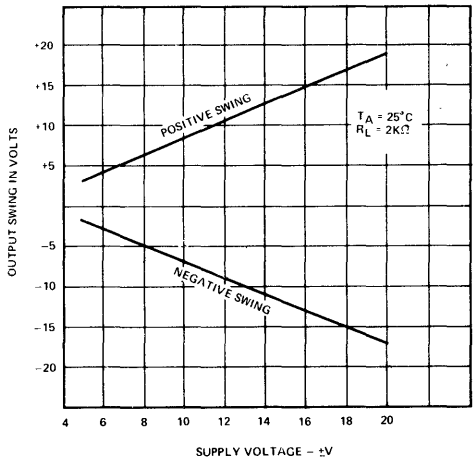
LARGE SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE



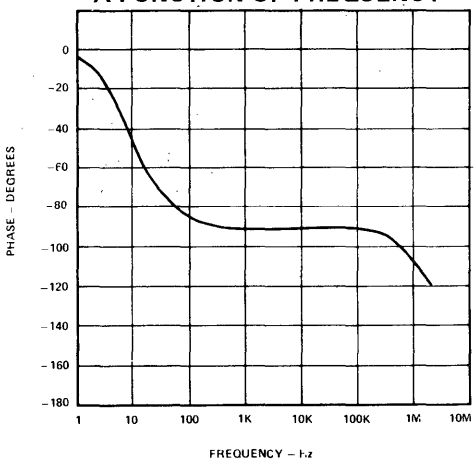
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

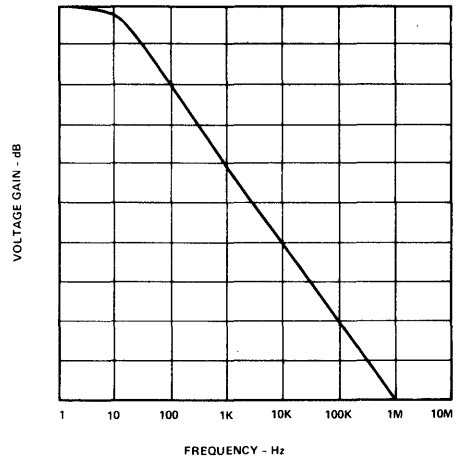


OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY

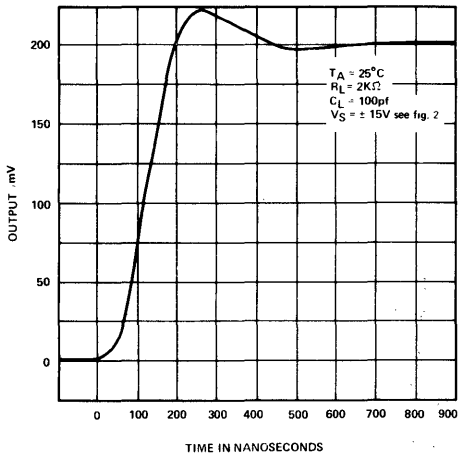


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

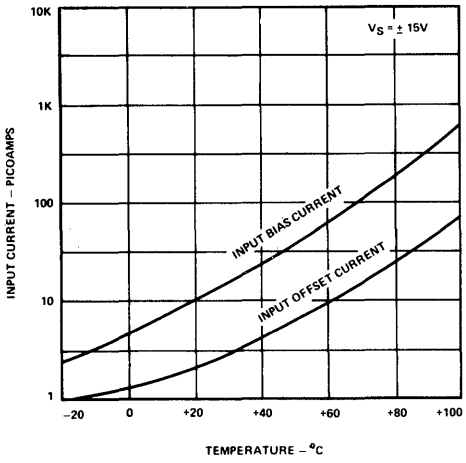
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



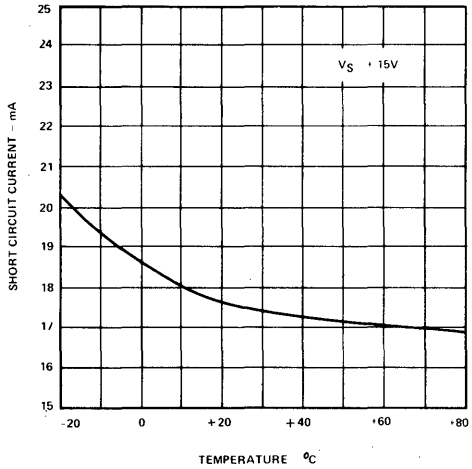
VOLTAGE FOLLOWER TRANSIENT RESPONSE



INPUT CURRENTS AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



DESCRIPTION

The 537 is a precision operational amplifier featuring very low input bias over the full temperature range, high gain, short circuit immunity, full input protection, simple compensation, excellent temperature stability, with offset voltage null capability.

FEATURES

- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH UP
- LOW INPUT BIAS AND OFFSET

ABSOLUTE MAXIMUM RATINGS

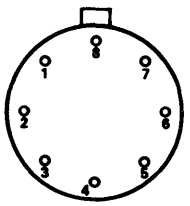
Supply Voltage	
SE537	±22V
NE537	±20V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage	±Vs
Storage Temperature	-65°C to +150°C
Operating Temperature	
SE537	-55°C to +125°C
NE537	0°C to +70°C
Lead Temperature	300°C
Output Short Circuit Duration (Note 2)	Indefinite

NOTES:

1. Rating applies for case temperature to 125°C, derate linearly at 6.5mW/°C for ambient temperature above +5°C.
2. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

PIN CONFIGURATION

T PACKAGE
(Top View)

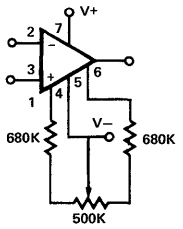


1. Freq. Comp / Offset Null
2. Inverting input
3. Noninverting input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp.

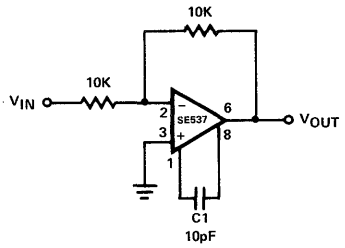
ORDER PART NOS. SE537T/NE537T

TEST CIRCUITS

VOLTAGE OFFSET
NULL CIRCUIT



TRANSIENT RESPONSE
TEST CIRCUIT

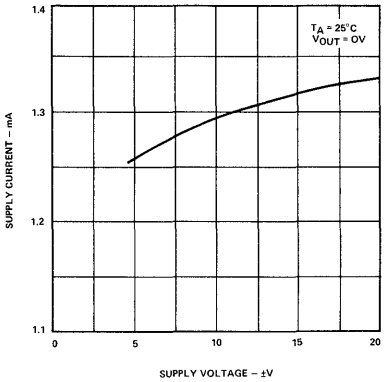


ELECTRICAL CHARACTERISTICS (V_S = ± 5V to ±20V unless otherwise specified.)

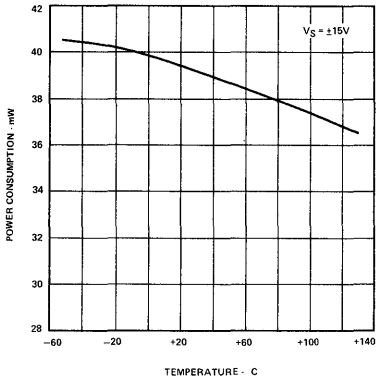
PARAMETER	CONDITIONS	NE537			SE537			
		MIN	TYP	MAX	MIN	TYP	MAX	UNIT
Input Offset Voltage	T_A = +25 °C		1.6	7.5		0.6	2.0	mV
Input Offset Voltage			2.0	10.0		1.2	3.0	mV
Input Offset Current	T_A = +25 °C		0.2	1.0		0.07	0.2	nA
Input Offset Current			0.25	1.5		0.12	0.3	nA
Input Bias Current	T_A = +25°C		1.5	7.0		0.8	2.0	nA
Input Bias Current			2.2	10.0		1.5	3.0	nA
Input Resistance		10	50		30	70		mΩ
Input Capacitance			0.5			0.5		pF
Offset Voltage Adjust Range			±15			±15		mV
Input Voltage Range	V_S = ±15V	±12	±14		±12	±14		V
Large Signal Voltage Gain	$R_L \geq$ 2k, V_{out} ±10V, V_S ±15V T_A = 25°C	25k	400k		50k	500k		
Large Signal Voltage Gain	$R_L \geq$ 2k, V_{out} ±10V, V_S ±15V	16k	250k		25k	300k		
Output Resistance			75			75		Ω
Short Circuit Current	T_A = +25 °C		25			25		mA
Supply Voltage Rejection Ratio		80	100		80	100		dB
Common Mode Rejection Ratio	V_{in} = ±12V	80	100		86	100		dB
Supply Current	T_A = +25 °C		1.25	2.0		1.20	1.50	mA
Supply Current			1.30	3.0		1.30	2.0	mA
Unity Gain Frequency	V_S = ±15V, C_C = 10pf		250			250		KHz
Slew Rate	V_O = ±5V, C_C = 10pF, R_L = 2kΩ		0.2			0.2		V/μsec
Output Voltage Swing	$R_L \geq$ 10k, V_S ±15V C_L = 100pF	±13	±13.5		±13	±13.5		V
	R ≥ 2kΩ	±10	±12.6		±10	±12.6		V
Temperature Range		-0		+75	-55		+125	°C

TYPICAL PERFORMANCE CHARACTERISTICS

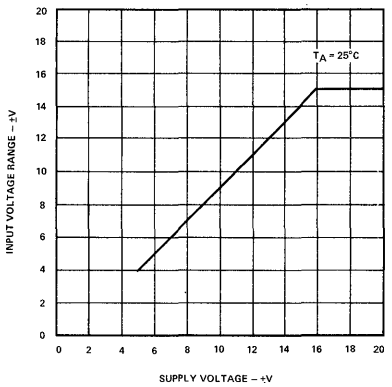
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

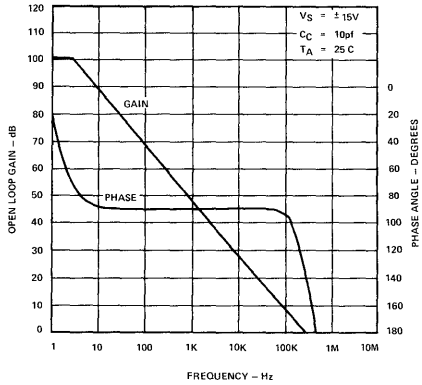


INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

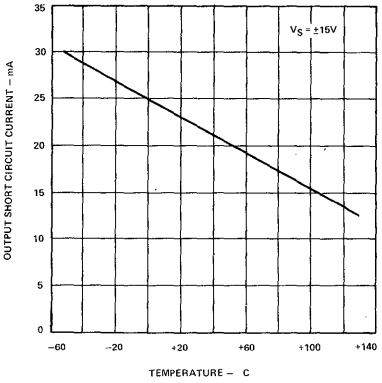


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

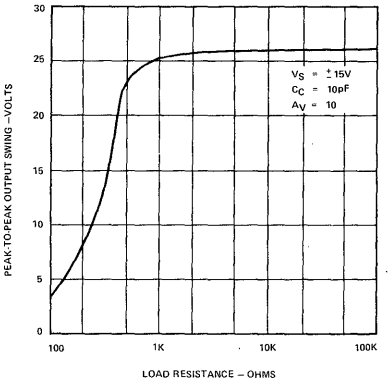
OPEN LOOP PHASE RESPONSES AND VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



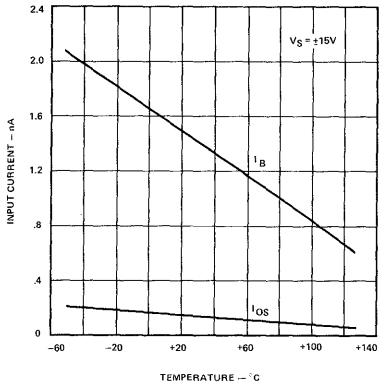
OUTPUT SHORT CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



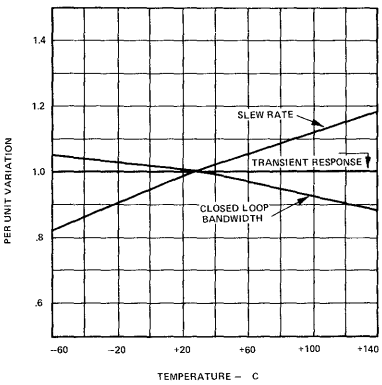
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



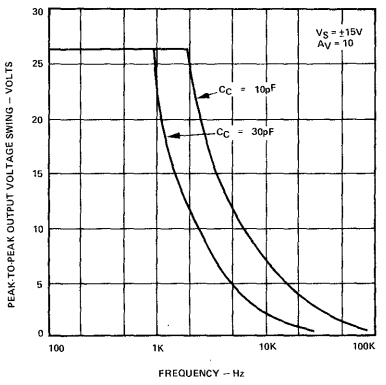
INPUT BIAS AND OFFSET CURRENTS AS FUNCTIONS OF AMBIENT TEMPERATURE



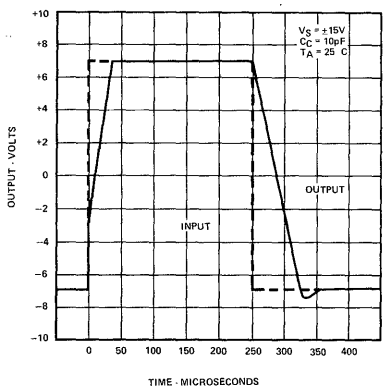
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



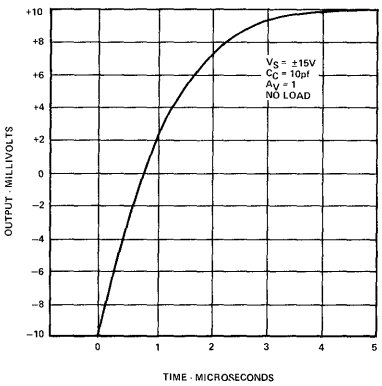
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



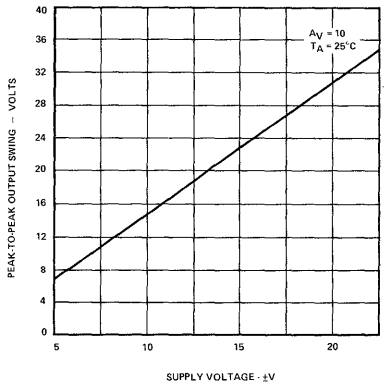
VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



SMALL SIGNAL TRANSIENT RESPONSE

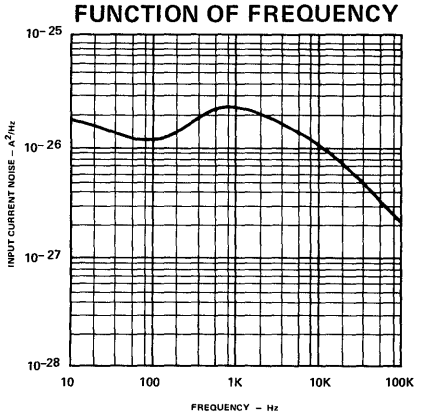


OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

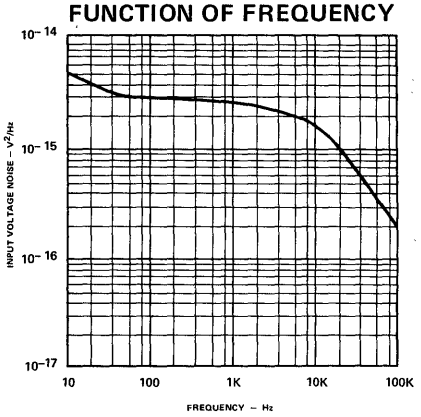


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

INPUT CURRENT NOISE AS A FUNCTION OF FREQUENCY



INPUT VOLTAGE NOISE AS A FUNCTION OF FREQUENCY



INPUT GUARD FOR LEAKAGE

Even with cleaned and coated boards, leakage currents can be comparable to the input bias current of the SE537. In addition the 537, as well as most other operational amplifiers, has its input pins adjacent to pins at the supply potential. In order to prevent leakage it is advisable to guard the input pins with a circuit board trace to ground.

PRINTED CIRCUIT LAYOUT FOR INPUT GUARDING

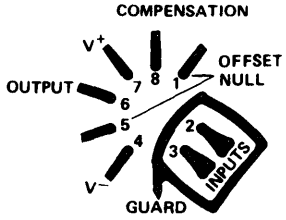


FIGURE 3a₀

INVERTING AMPLIFIER

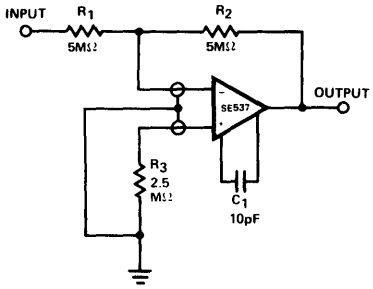


FIGURE 3b₀

NON-INVERTING AMPLIFIER

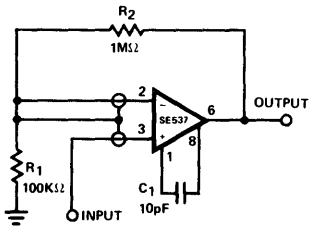
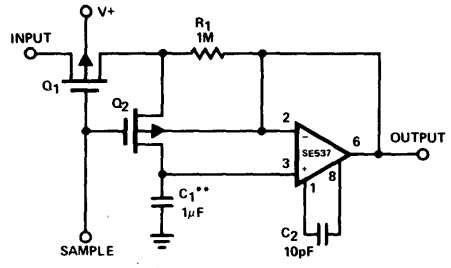


FIGURE 3c₀

TYPICAL APPLICATIONS

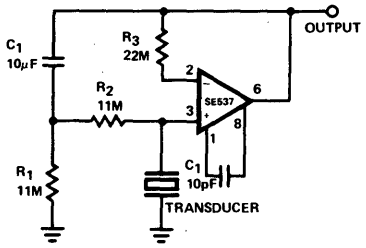
SAMPLE AND HOLD*



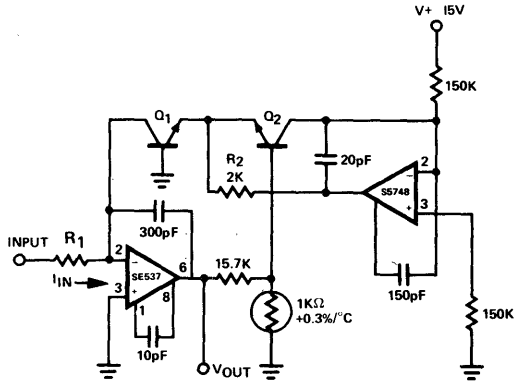
*WORST CASE DRIFT LESS THAN 2.5mV/sec

** TEFLON, POLYETHYLENE OR OR POLYCARBONATE DIELECTRIC CAPACITOR

AMPLIFIER FOR PIEZOELECTRIC TRANSDUCERS

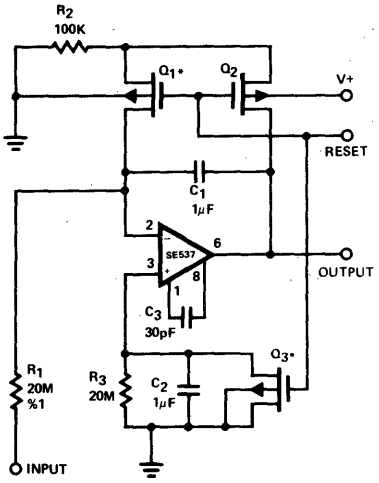


TEMPERATURE COMPENSATED LOGARITHMIC CONVERTER

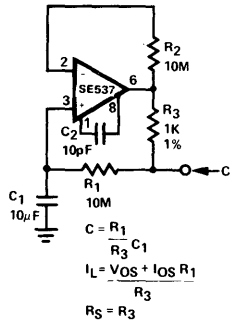


10nA< I_{IN} < 1mA
SENSITIVITY 1 V/ DECADE
"O" LEVEL 100μA

LOW DRIFT INTEGRATOR WITH RESET



CAPACITANCE MULTIPLIER

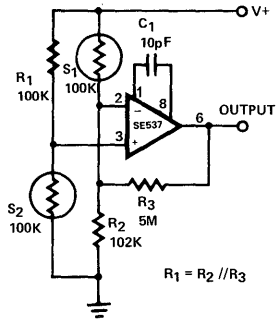


$C = \frac{R_1}{R_3} C_1$

$I_L = \frac{V_{OS} + I_{OS} R_1}{R_3}$

$R_S = R_3$

AMPLIFIER FOR BRIDGE TRANSDUCERS



$R_1 = R_2 // R_3$

DESCRIPTION

The LM101A and LM301A are high performance operational amplifiers featuring high gain, short circuit protection, simplified compensation and excellent temperature stability.

FEATURES

- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH UP

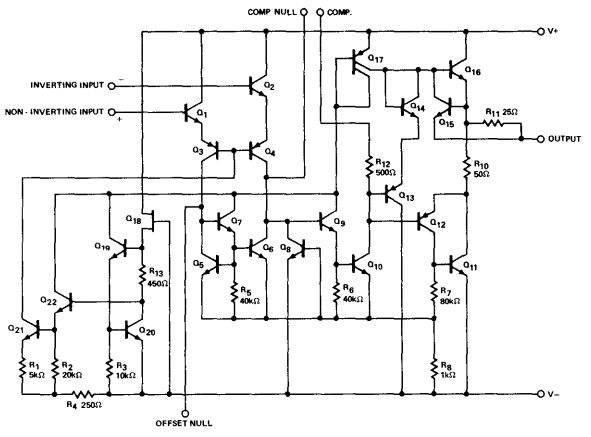
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	LM101A	±22V
	LM301A	±18V
Power Dissipation (Note 1)		500mW
Differential Input Voltage		±30V
Input Voltage (Note 2)		±15V
Output Short Circuit Duration		Indefinite
Operating Temperature Range	LM101A	-55°C to 125°C
	LM301A	0°C to 70°C
Storage Temperature Range		-65°C to 150°C
Lead Temperature (Soldering, 60 sec.)		300°C

NOTES:

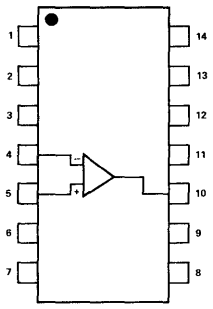
1. Absolute maximum rating holds for all packages. The maximum junction temperature is 150°C for the LM101A and 100°C for the LM301A. For operation at elevated temperatures, derate according to appropriate thermal resistances given under package information.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

EQUIVALENT CIRCUIT



PIN CONFIGURATIONS

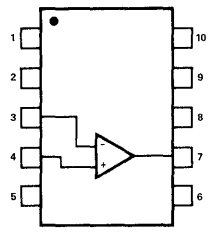
A & F PACKAGE (Top View)



1. NC
2. NC
3. Freq. Comp./Offset Null
4. Inverting Input
5. Noninverting Input
6. V^-
7. NC
8. NC
9. Offset Null
10. Output
11. V^+
12. Freq. Comp.
13. NC
14. NC

ORDER PART NOS.
LM101AD/LM301AD LM101AN-14/LM301AN-14

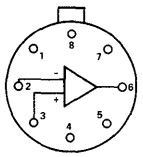
G PACKAGE



1. NC
2. Bal/Comp
3. Input
4. Input
5. V^-
6. Bal
7. Output
8. V^+
9. Comp
10. NC

ORDER PART NOS.
LM101AF/LM301AF

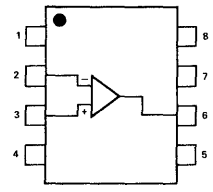
T PACKAGE



1. Freq. Comp/Offset Null
2. Inverting Input
3. Noninverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp.

ORDER PART NOS.
LM101AH/LM301AH

V PACKAGE



1. Freq. Comp./Offset Null
2. Inverting Input
3. Noninverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp.

ORDER PART NO.
LM301AN

LM101A

ELECTRICAL CHARACTERISTICS ($-55°C \leq T_A \leq 125°C$, $\pm 5V \leq V_S \leq \pm 20V$ and $C_1 = 30pF$ unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 50k\Omega$		0.7	2.0	mV
Input Offset Current	$T_A = 25°C$		1.5	10	nA
Input Bias Current	$T_A = 25°C$		30	75	nA
Input Resistance	$T_A = 25°C$	1.5	4		MΩ
Supply Current	$T_A = 25°C$, $V_S = \pm 20V$		1.8	3.0	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	50	160		V/mV
Input Offset Voltage	$R_S \leq 50k\Omega$			3.0	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15	μV/°C
Input Offset Current				20	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 125°C$ $-55°C \leq T_A \leq 25°C$		0.01 0.02	0.1 0.2	nA/°C nA/°C
Input Bias Current				100	nA
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$		1.2	2.5	mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$	25			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 ±10	±14 ±13		V V
Input Voltage Range	$V_S = \pm 20V$	±15			V
Common Mode Rejection Ratio	$R_S \leq 50k\Omega$	80	96		dB
Supply Voltage Rejection Ratio	$R_S \leq 50k\Omega$	80	96		dB

LM301A

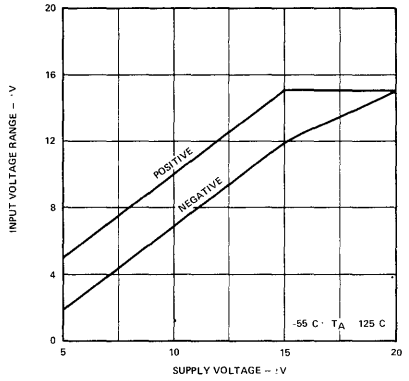
ELECTRICAL CHARACTERISTICS ($0°C \leq T_A < 70°C$, $\pm 5V$, $\leq V_S \leq \pm 15V$ and $C_1 = 30pF$ unless otherwise specified.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 50k\Omega$		2.0	7.5	mV
Input Offset Current	$T_A = 25°C$		3	50	nA
Input Bias Current	$T_A = 25°C$		70	250	nA
Input Resistance	$T_A = 25°C$	0.5	2		MΩ
Supply Current	$T_A = 25°C$, $V_S = \pm 15V$		1.8	3.0	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$ $V_{OUT} = \pm 10V$; $R_L \geq 2k\Omega$	25	160		V/mV
Input Offset Voltage	$R_S \leq 50k\Omega$			10	mV
Average Temperature Coefficient of Input Offset Voltage			6.0	30	μV/°C
Input Offset Current				70	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 70°C$ $0°C \leq T_A \leq 25°C$		0.01 0.02	0.3 0.6	nA/°C nA/°C
Input Bias Current				300	nA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$	15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$ $R_L = 2k\Omega$	±12 ±10	±14 ±13		V V
Input Voltage Range	$V_S = \pm 15V$	±12			V
Common Mode Rejection Ratio	$R_S \leq 50k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 50k\Omega$	70	96		dB

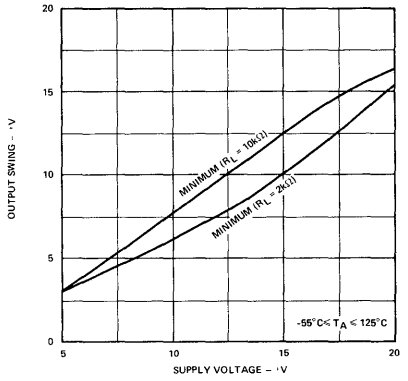
TYPICAL CHARACTERISTIC CURVES

LM101A

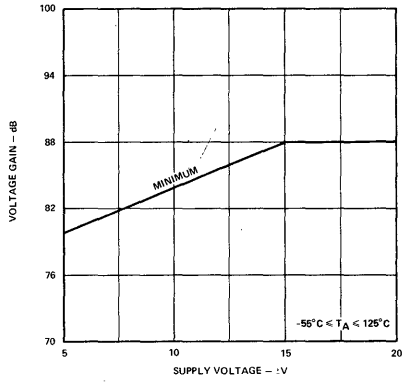
INPUT VOLTAGE RANGE VERSUS SUPPLY VOLTAGE



OUTPUT SWING VERSUS SUPPLY VOLTAGE

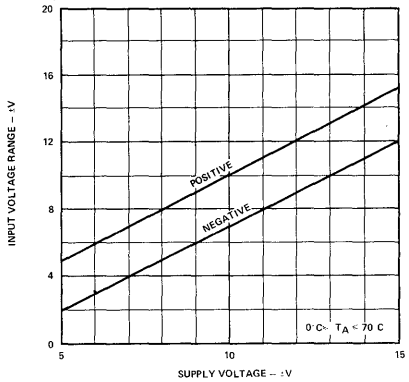


VOLTAGE GAIN VERSUS SUPPLY VOLTAGE

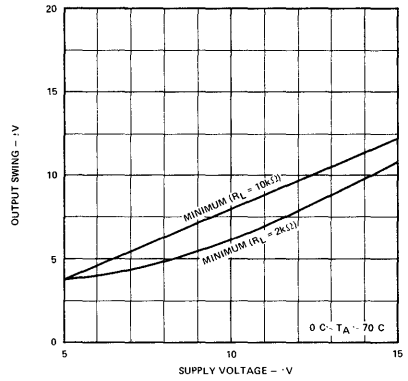


LM301A

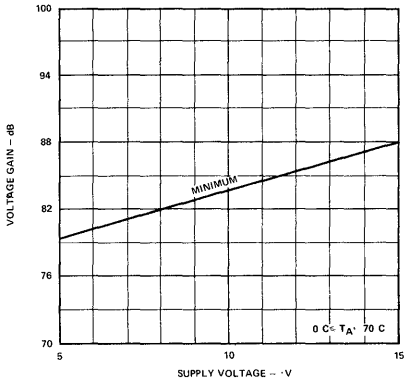
INPUT VOLTAGE RANGE VERSUS SUPPLY VOLTAGE



OUTPUT SWING VERSUS SUPPLY VOLTAGE

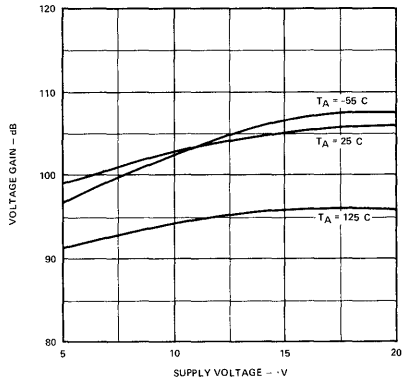


VOLTAGE GAIN VERSUS SUPPLY VOLTAGE

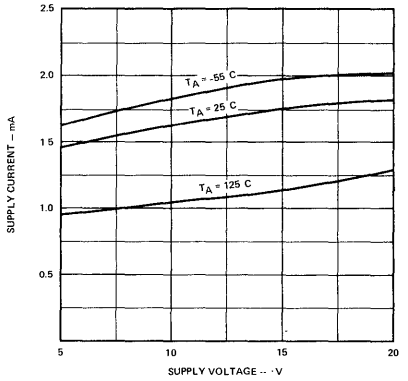


LM101A

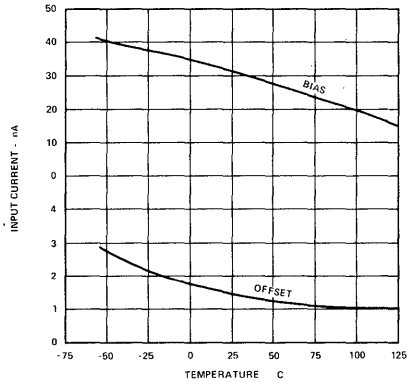
VOLTAGE GAIN



SUPPLY CURRENT



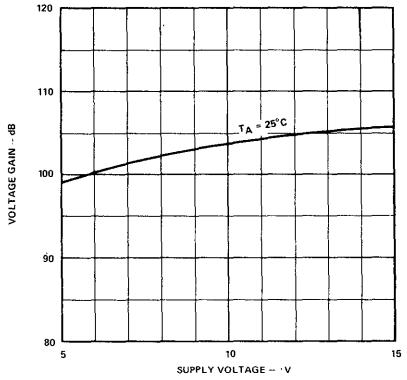
INPUT CURRENT



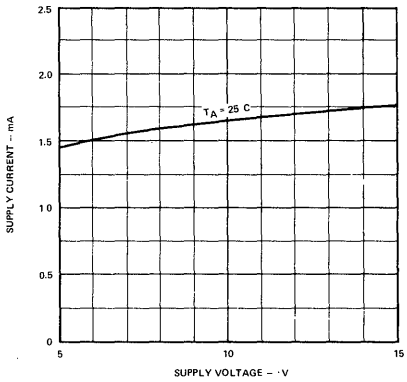
TYPICAL CHARACTERISTIC CURVES (Cont'd.)

LM301A

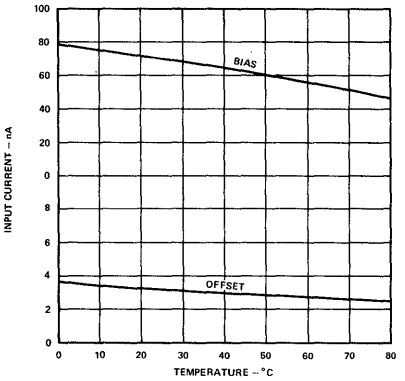
VOLTAGE GAIN



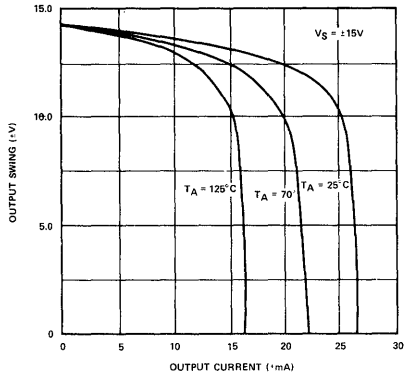
SUPPLY CURRENT



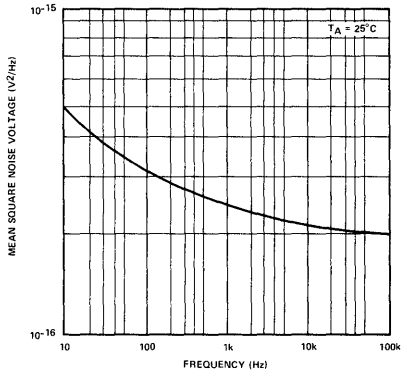
INPUT CURRENT



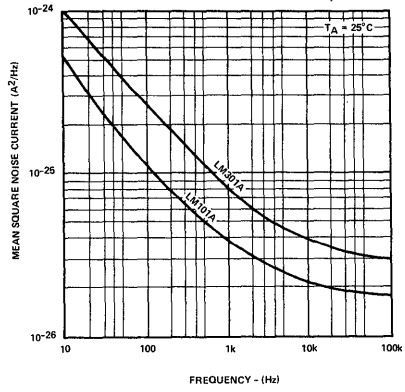
CURRENT LIMITING



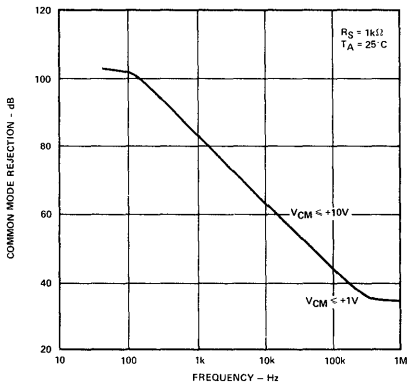
INPUT NOISE VOLTAGE



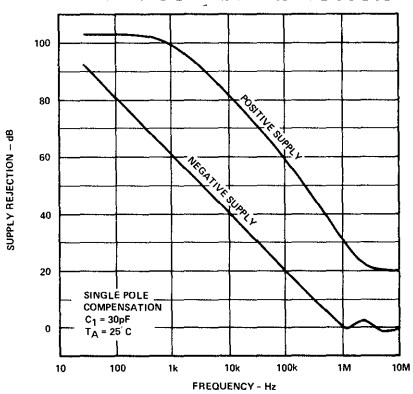
INPUT NOISE CURRENT



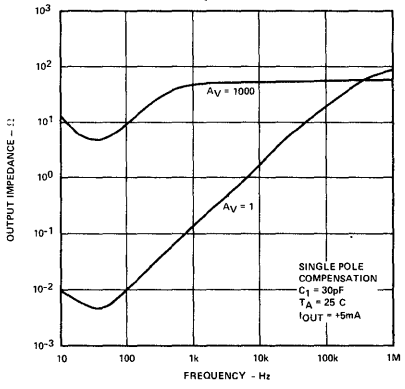
COMMON MODE REJECTION



POWER SUPPLY REJECTION



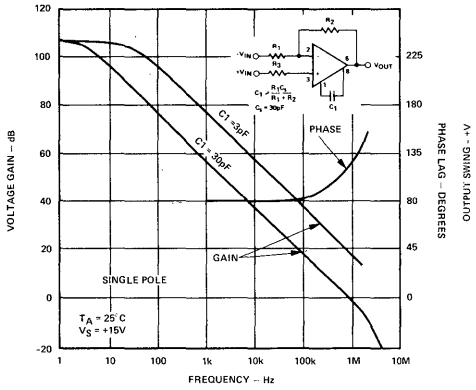
CLOSED LOOP OUTPUT IMPEDANCE



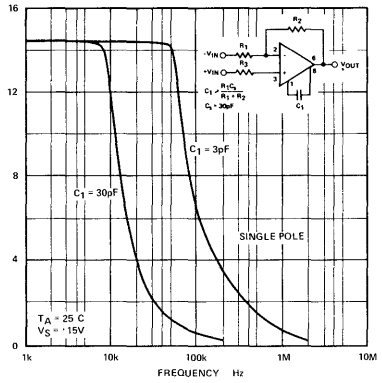
TYPICAL CHARACTERISTIC CURVES (Cont'd.)

SINGLE POLE COMPENSATION

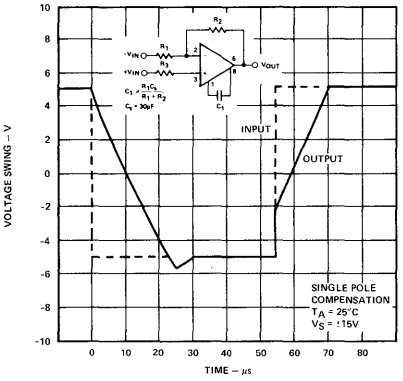
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE

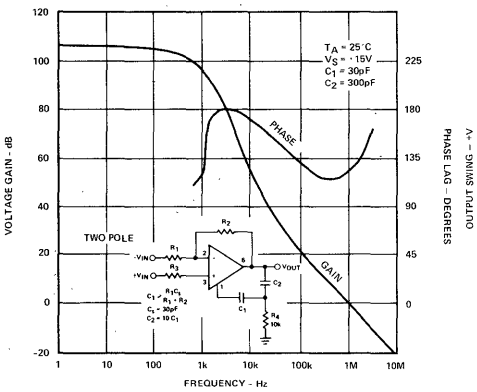


VOLTAGE FOLLOWER PULSE RESPONSE

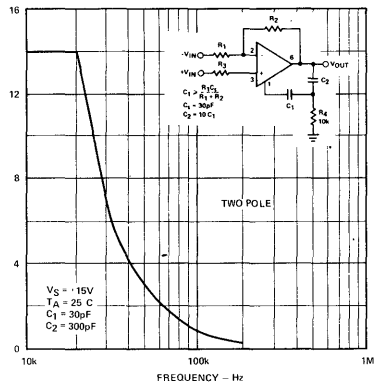


TWO POLE COMPENSATION

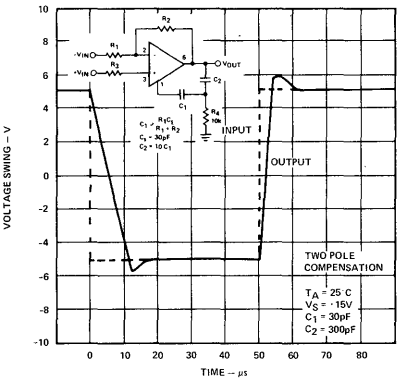
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE

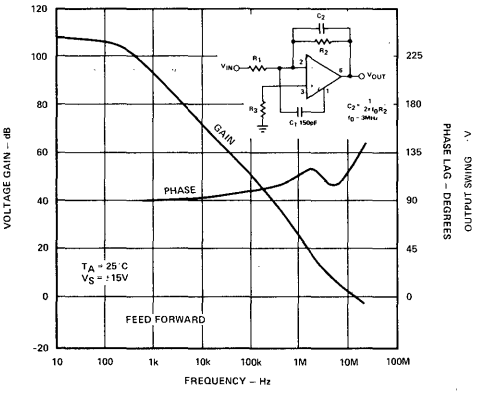


VOLTAGE FOLLOWER PULSE RESPONSE

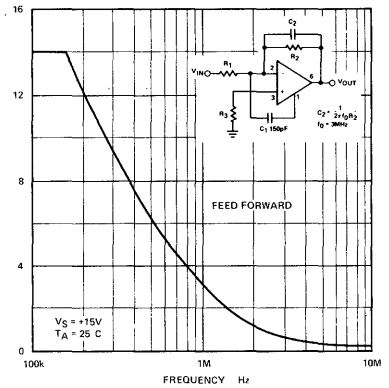


FEED FORWARD COMPENSATION

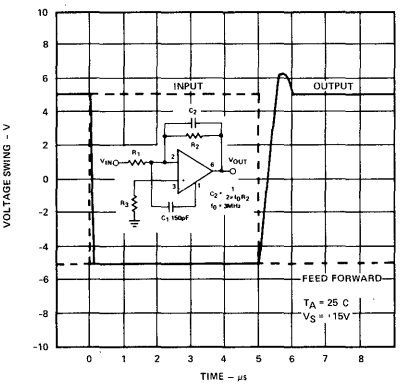
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE

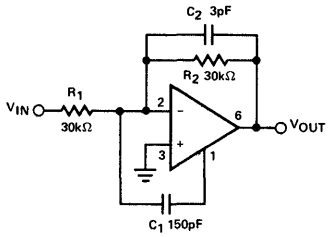


INVERTER PULSE RESPONSE



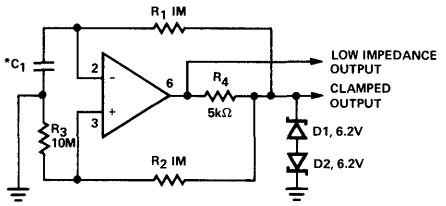
TYPICAL APPLICATIONS (Pin numbers shown refer to T or V package only)

FAST SUMMING AMPLIFIER



Power Bandwidth: 250kHz
Small Signal Bandwidth: 3.5MHz
Slew Rate: 10V/μs

LOW FREQUENCY SQUARE WAVE GENERATOR



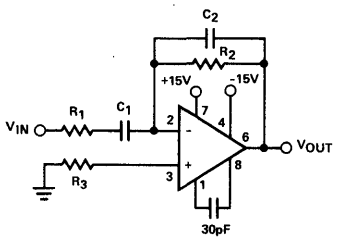
*Adjust C_1 for frequency

PRACTICAL DIFFERENTIATOR

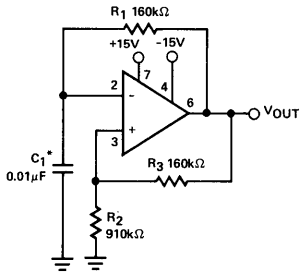
$$f_c = \frac{1}{2\pi R_2 C_1}$$

$$f_n = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi R_2 C_2}$$

$f_c < f_n < f_{unity\ gain}$

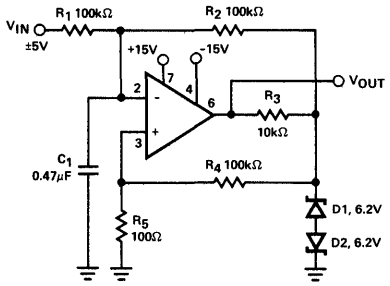


FREE-RUNNING MULTIVIBRATOR

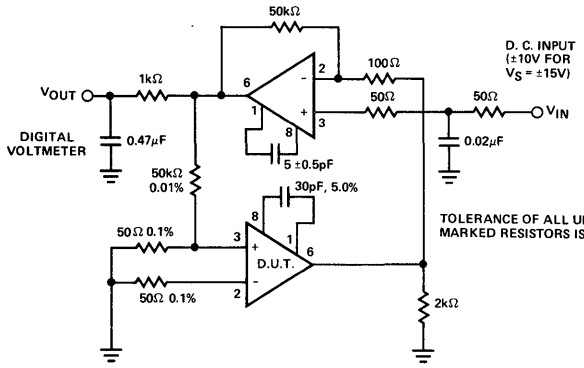


*Chosen for oscillation at 100Hz

PULSE WIDTH MODULATOR

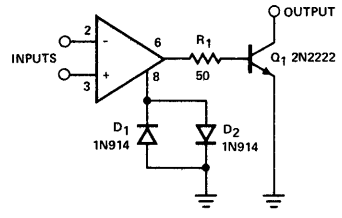


GAIN TEST CIRCUIT

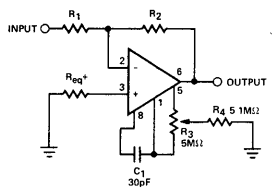


$$A_{VO} = \frac{V_{IN} \times 10^3}{V_{OUT}}$$

VOLTAGE COMPARATOR FOR DRIVING RTL LOGIC OR HIGH CURRENT DRIVER

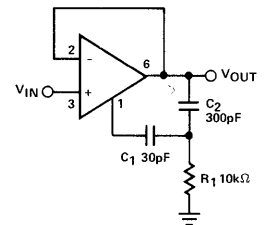


INVERTING AMPLIFIER WITH BALANCING CIRCUIT



†May be zero or equal to parallel combination of R_1 and R_2 for minimum offset.

FAST VOLTAGE FOLLOWER



Power Bandwidth: 15kHz
Slew Rate: 1V/μs

DESCRIPTION

The LM101 and LM201 are high performance operational amplifiers featuring high gain, short circuit protection, simplified compensation and excellent temperature stability.

FEATURES

- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH UP

ABSOLUTE MAXIMUM RATINGS

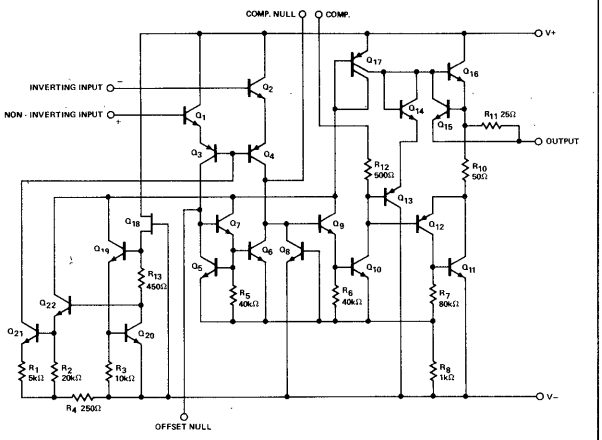
Supply Voltage		±22V
Power Dissipation (Note 1)		500mW
Differential Input Voltage		±30V
Input Voltage (Note 2)		±15V
Output Short Circuit Duration		Indefinite
Operating Temperature Range	LM101	−55°C to 125°C
	LM201	0°C to 70°C
Storage Temperature Range		−65°C to 150°C
Lead Temperature (Soldering, 60 sec.)		300°C

NOTES

1. Absolute maximum rating holds for all packages. The maximum junction temperature is 150°C for the LM101 and 100°C for the LM201. For operation at elevated temperatures, derate according to appropriate thermal resistances given under package information.

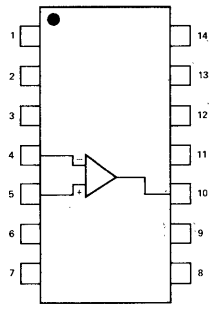
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

EQUIVALENT CIRCUIT



PIN CONFIGURATIONS

A & F PACKAGE (Top View)

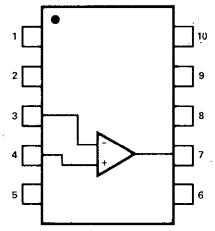


1. NC
2. NC
3. Freq. Comp./Offset Null
4. Inverting Input
5. Noninverting Input
6. V^-
7. NC
8. NC
9. Offset Null
10. Output
11. V^+
12. Freq. Comp.
13. NC
14. NC

ORDER PART NOS.

LM10IN-14, LM20IN-14 } Silicone
LM101D, LM201D } Ceramic

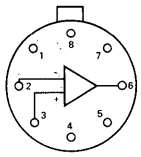
G PACKAGE



1. NC
2. Bal/Comp
3. Input
4. Input
5. V^-
6. Bal
7. Output
8. V^+
9. Comp
10. NC

ORDER PART NOS.
LM101F/LM201F

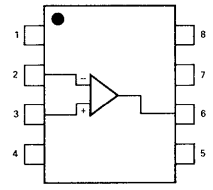
T PACKAGE



1. Freq. Comp/Offset Null
2. Inverting Input
3. Noninverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp.

ORDER PART NOS.
LM101H/LM201H

V PACKAGE



1. Freq. Comp./Offset Null
2. Inverting Input
3. Noninverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp.

ORDER PART NO. LM201N

ELECTRICAL CHARACTERISTICS

$-55°C \leq T_A \leq 125°C$, $\pm 15V \leq V_S \leq \pm 20V$ and $C_1 = 30$ pF unless otherwise specified).

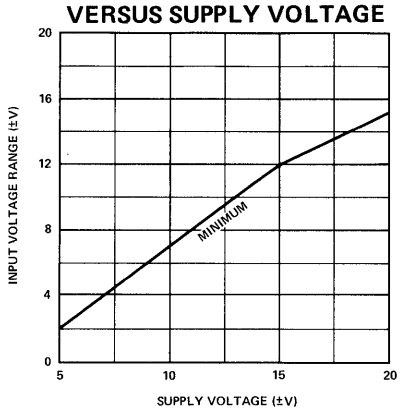
LM101 PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$T_A = 25°C$, $R_s \leq 10k\Omega$		1.0	5.0	mV
Input Offset Current	$T_A = 25°C$		40	200	nA
Input Bias Current	$T_A = 25°C$		120	500	nA
Input Resistance	$T_A = 25°C$	300	800		kΩ
Supply Current	$T_A = 25°C$, $V_s = \pm 20V$		1.8	3.0	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_s = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	50	160		V/mV
Input Offset Voltage	$R_s \leq 10k\Omega$			6.0	mV
Average Temperature Coefficient of Input Offset Voltage	$R_s \leq 50\Omega$		3.0		μV/°C
	$R_s \leq 10k\Omega$		6.0		μV/°C
Input Offset Current	$T_A = +125°C$		10	200	nA
	$T_A = -55°C$		100	500	nA
Input Bias Current	$T_A = -55°C$		0.28	1.5	μA
Supply Current	$T_A = +125°C$, $V_s = \pm 20V$		1.2	2.5	mA
Large Signal Voltage Gain	$V_s = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$	25			V/mV
Output Voltage Swing	$V_s = \pm 15V$, $R_L = 10k\Omega$	±12	±14		V
	$R_L = 2k\Omega$	±10	±13		V
Input Voltage Range	$V_s = \pm 15V$	±12			V
Common Mode Rejection Ratio	$R_s \leq 10k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_s \leq 10k\Omega$	70	90		dB

LM201 PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$T_A = 25°C$, $R_s \leq 10k\Omega$		2.0	7.5	mV
Input Offset Current	$T_A = 25°C$		100	500	nA
Input Bias Current	$T_A = 25°C$		0.25	1.5	μA
Input Resistance	$T_A = 25°C$	100	400		kΩ
Supply Current	$T_A = 25°C$, $V_s = \pm 20V$		1.8	3.0	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_s = \pm 15V$ $V_{OUT} = \pm 10V$, $R_L \geq 2k\Omega$	20	150		V/mV
Input Offset Voltage	$R_s \leq 10k\Omega$			10	mV
Average Temperature Coefficient of Input Offset Voltage	$R_s \leq 50\Omega$		6		μV/°C
	$R_s \leq 10k\Omega$		10		μV/°C
Input Offset Current	$T_A = +70°C$		50	400	nA
	$T_A = 0°C$		150	750	nA
Input Bias Current	$T_A = 0°C$		0.32	2.0	μA
Large Signal Voltage Gain	$V_s = \pm 15V$, $V_{OUT} = \pm 10V$ $R_L \geq 2k\Omega$	15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10k\Omega$	±12	±14		V
	$R_L = 2k\Omega$	±10	±13		V
Input Voltage Range	$V_s = \pm 15V$	±12			V
Common Mode Rejection Ratio	$R_s \leq 10k\Omega$	65	90		dB
Supply Voltage Rejection Ratio	$R_s \leq 10k\Omega$	70	90		dB

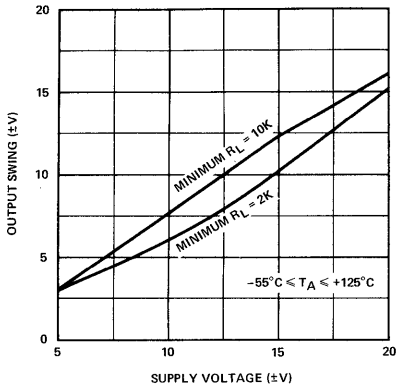
TYPICAL CHARACTERISTIC CURVES

LM101

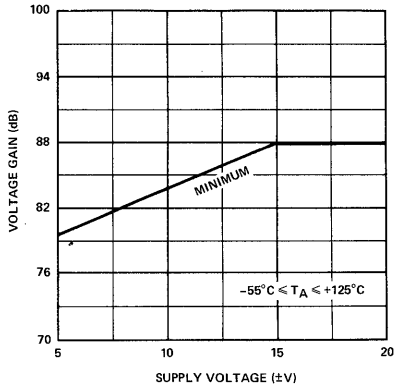
INPUT VOLTAGE RANGE VERSUS SUPPLY VOLTAGE



OUTPUT SWING VERSUS SUPPLY VOLTAGE

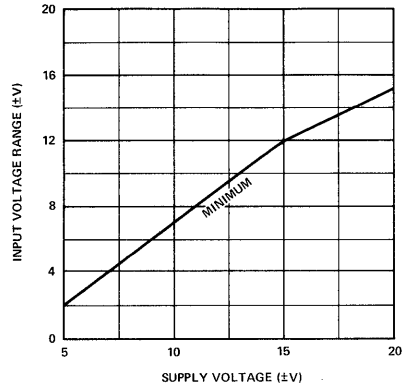


VOLTAGE GAIN VERSUS SUPPLY VOLTAGE

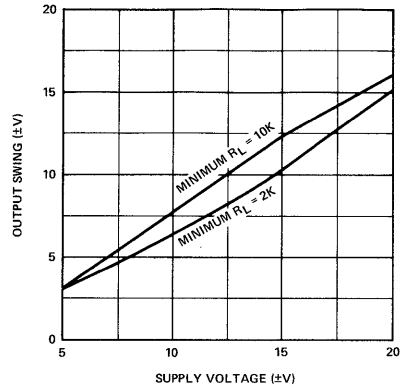


LM201

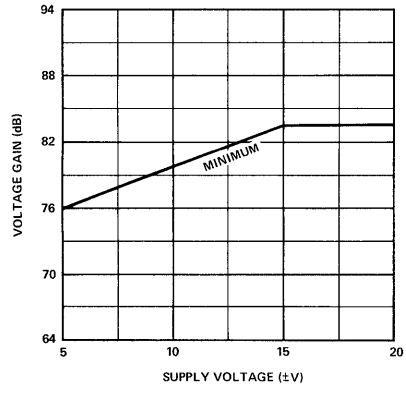
INPUT VOLTAGE RANGE VERSUS SUPPLY VOLTAGE



OUTPUT SWING VERSUS SUPPLY VOLTAGE



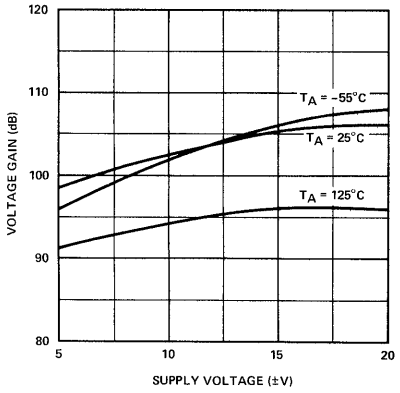
VOLTAGE GAIN VERSUS SUPPLY VOLTAGE



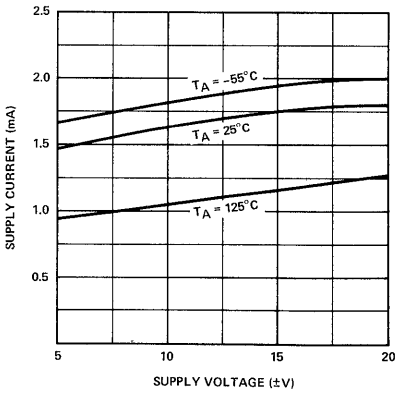
TYPICAL CHARACTERISTIC CURVES (Cont'd.)

LM101

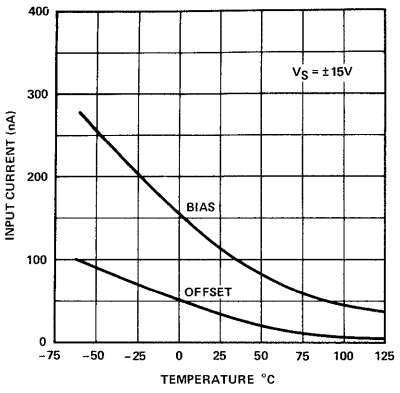
VOLTAGE GAIN



SUPPLY CURRENT

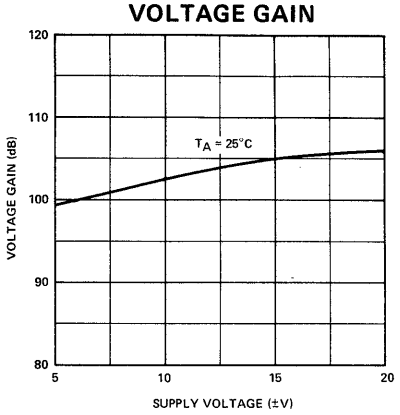


INPUT CURRENT

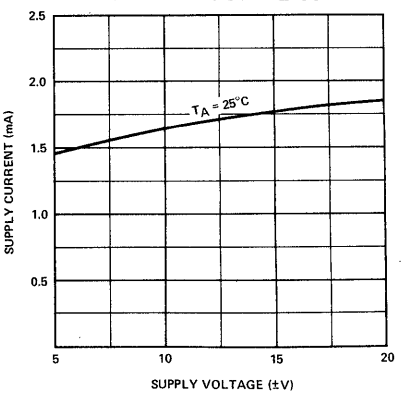


LM201

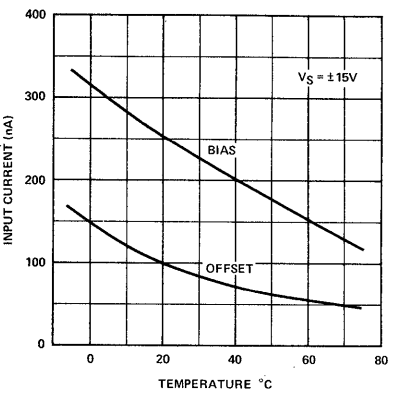
VOLTAGE GAIN



SUPPLY CURRENT



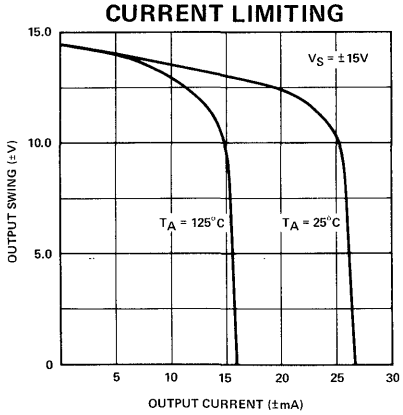
INPUT CURRENT



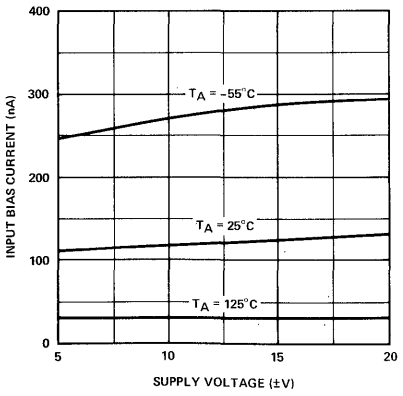
TYPICAL CHARACTERISTIC CURVES (Cont'd.)

LM101

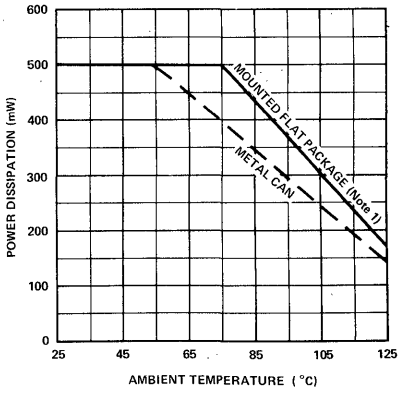
CURRENT LIMITING



INPUT CURRENT

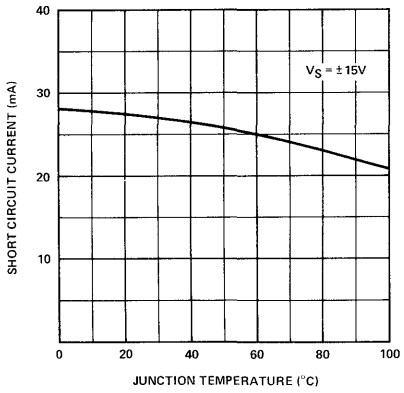


MAXIMUM POWER DISSIPATION

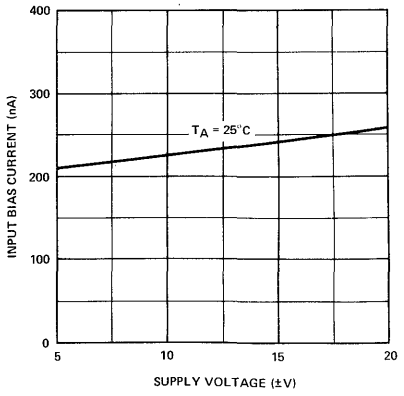


LM201

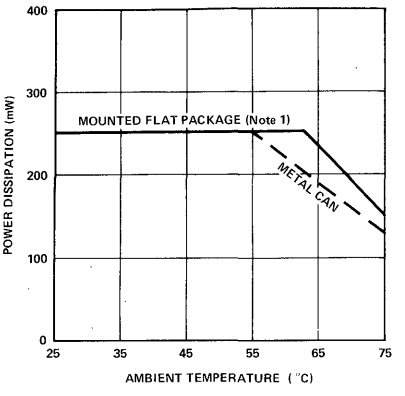
SHORT CIRCUIT CURRENT



INPUT CURRENT

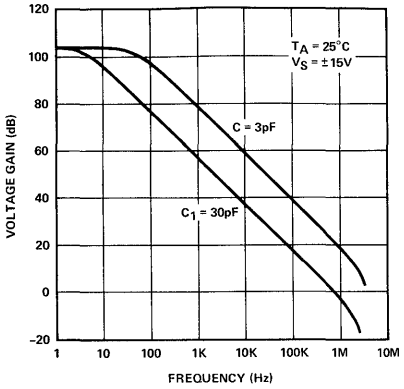


MAXIMUM POWER DISSIPATION

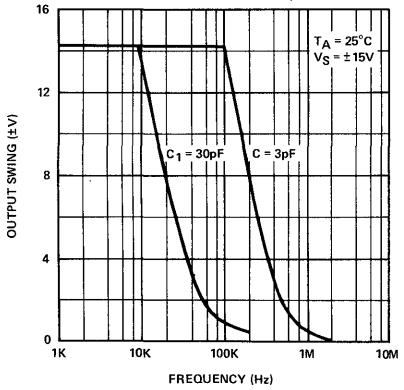


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

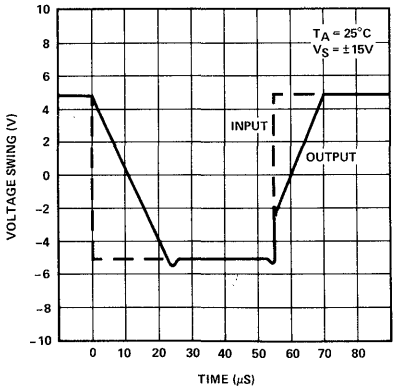
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE

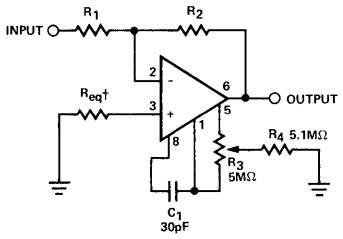


VOLTAGE FOLLOWER PULSE RESPONSE



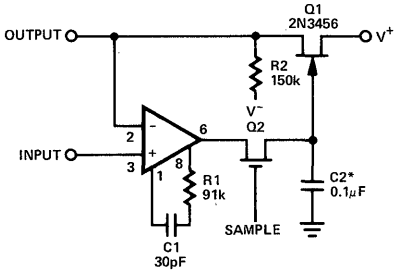
TYPICAL APPLICATIONS (Pin numbers shown refer to T or V package only)

INVERTING AMPLIFIER WITH BALANCING CIRCUIT



†May be zero or equal to parallel combination of R_1 and R_2 for minimum offset.

LOW DRIFT SAMPLE AND HOLD



*POLYCARBONATE DIELECTRIC CAPACITOR

DESCRIPTION

The LM107/307 is a general purpose internally compensated operational amplifier. Advanced processing techniques provide input currents which are an order of magnitude lower than the μA709. Standard pin out allows plug in replacement for the μA709, LM101, LM101A, and the μA741.

FEATURES

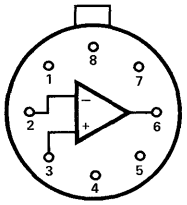
- 3mV MAX OFFSET VOLTAGE OVER TEMP
- 100 nA MAX INPUT CURRENT OVER TEMP
- 20 nA MAX INPUT OFFSET CURRENT OVER TEMP
- OFFSETS GUARANTEED OVER COMMON MODE RANGE
- INPUT/OUTPUT SHORT CIRCUIT PROTECTED

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	LM107	±22V
	LM307	±18V
Power Dissipation (Note 1)		500 mW
Differential Input Voltage		±30V
Input Voltage (Note 2)		±15V
Output Short-Circuit Duration (Note 3)		Indefinite
Operating Temperature Range	LM107	-55°C to 125°C
	LM307	0°C to 70°C
Storage Temperature Range		-65°C to 150°C
Lead Temperature (Soldering, 60 sec)		300°C

PIN CONFIGURATIONS

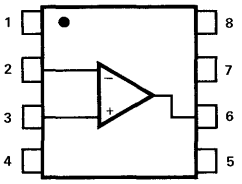
T PACKAGE
(Top View)



1. NC
2. Inverting Input
3. Noninverting Input
4. V^-
5. NC
6. Output
7. V^+
8. NC

ORDER PART NOS.
LM107H/LM307H

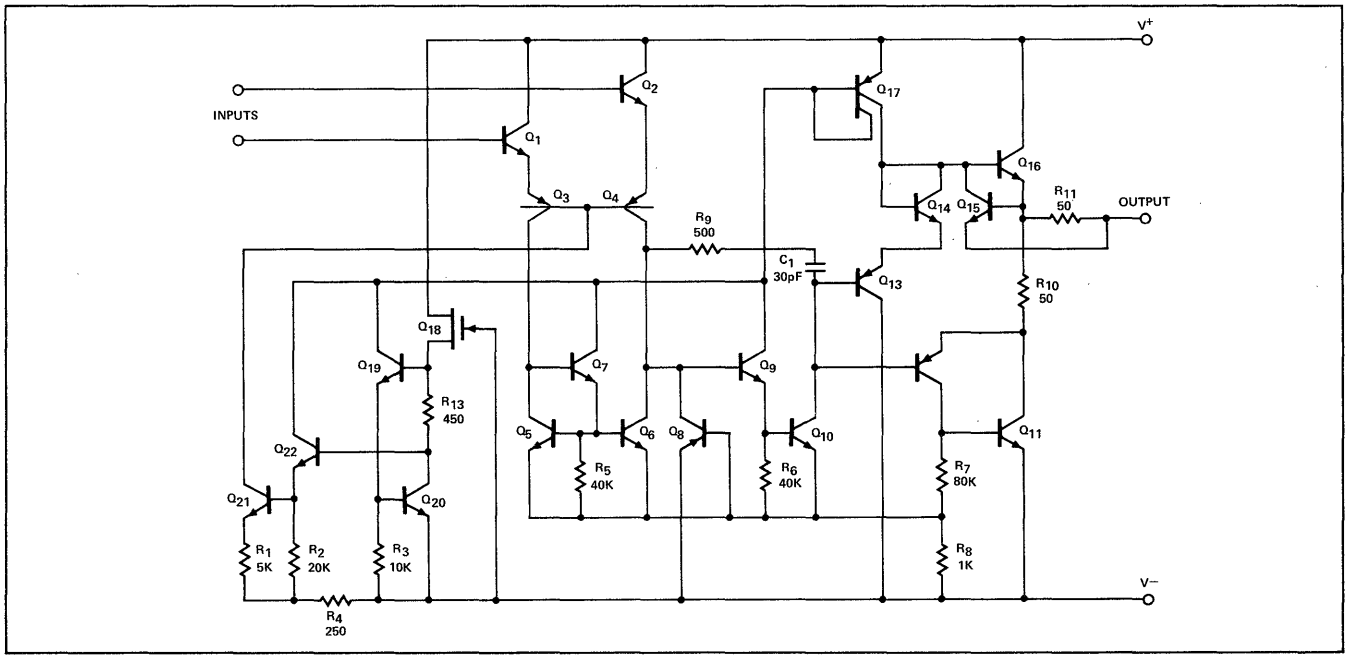
V PACKAGE



1. NC
2. Inverting Input
3. Noninverting Input
4. V^-
5. NC
6. Output
7. V^+
8. NC

ORDER PART NO. LM307N

EQUIVALENT SCHEMATIC



ELECTRICAL CHARACTERISTICS

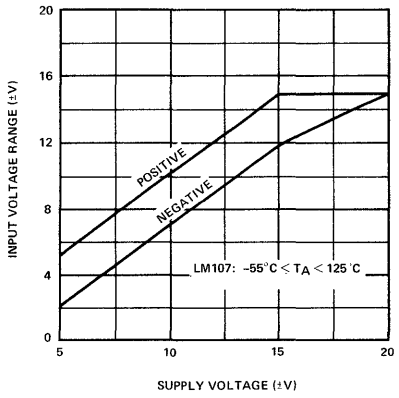
		LM107			LM307			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 10K\Omega$	–	0.7	2.0	–	–	–	mV
	$T_A = 25°C$, $R_S \leq 50K\Omega$	–	–	–	–	2.0	7.5	–
Input Offset Current	$T_A = 25°C$	–	1.5	10	–	3	50	nA
Input Bias Current	$T_A = 25°C$	–	30	75	–	70	250	nA
Input Resistance	$T_A = 25°C$	1.5	4	–	0.5	2	–	MΩ
Supply Current	$T_A = 25°C$, $V_S = \pm 20V$	–	1.8	3.0	–	–	–	mA
	$T_A = 25°C$, $V_S = \pm 15V$	–	–	–	–	1.8	3.0	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2K\Omega$	50	160	–	25	160	–	V/mV
Input Offset Voltage	$R_S \leq 10K\Omega$	–	–	3.0	–	–	–	mV
	$R_S \leq 50K\Omega$	–	–	–	–	–	10	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15	–	6.0	30	μV/°C
Input Offset Current		–	–	20	–	–	70	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 125°C$	–	0.01	0.1	–			nA/°C
	$-55°C \leq T_A \leq 25°C$	–	0.02	0.2	–			nA/°C
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 70°C$	–	–	–	–	0.01	0.3	nA/°C
	$0°C \leq T_A \leq 25°C$	–	–	–	–	0.02	0.6	nA/°C
Input Bias Current		–	–	100	–	–	300	nA
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$	–	1.2	2.5	–	–	–	mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2K\Omega$	25	–	–	15	–	–	V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10K\Omega$	±12	±14	–	±12	±14	–	V
	$R_L = 2K\Omega$	±10	±13	–	±10	±13	–	V
Input Voltage Range	$V_S = \pm 20V$	±15	–	–	–	–	–	V
	$V_S = \pm 15V$	–	–	–	±12	–	–	V
Common Mode Rejection Ratio	$R_S \leq 10K\Omega$	80	96	–	–	–	–	dB
	$R_S \leq 50K\Omega$	–	–	–	70	90	–	dB
Supply Voltage Rejection Ratio	$R_S \leq 10K\Omega$	80	96	–	–	–	–	dB
	$R_S \leq 50K\Omega$	–	–	–	70	96	–	dB

NOTES:
1. For operating at elevated temperatures, the device must be derated based on a 150°C maximum junction temperature and a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case (for T Package).
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Continuous short circuit is allowed for case temperatures to 70°C and ambient temperatures to 55°C.
4. The specifications apply for -55°C to 125°C for LM107 and 0°C to 70°C for LM307 unless otherwise specified.
5. $\pm 5V \leq V_S \leq \pm 15V$ unless otherwise specified.

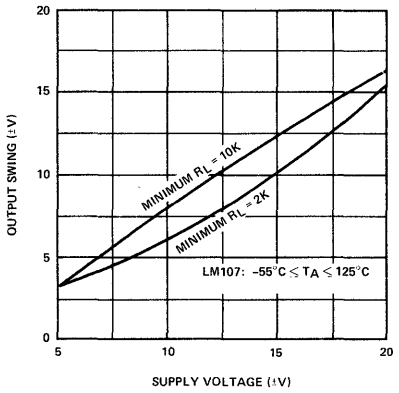
GUARANTEED PERFORMANCE CURVES

LM107

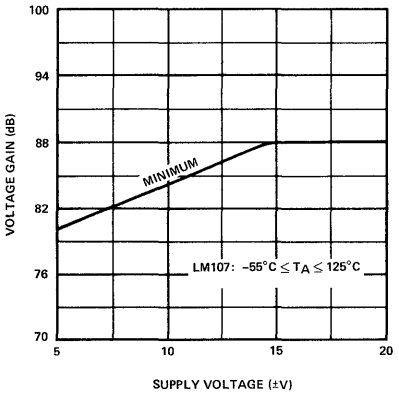
INPUT VOLTAGE RANGE



OUTPUT SWING

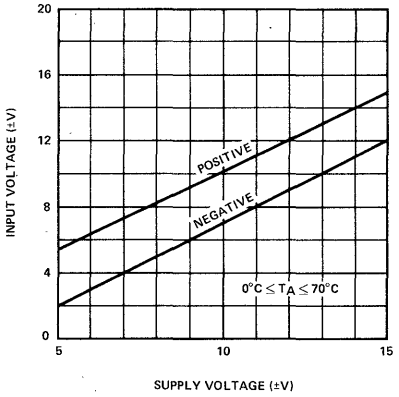


VOLTAGE GAIN

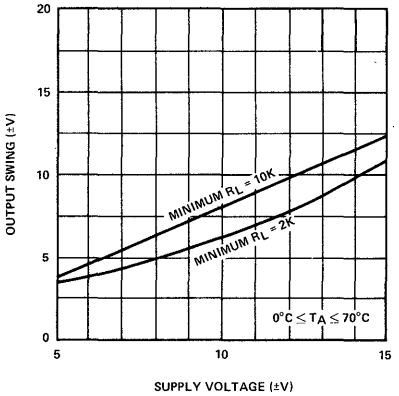


LM307

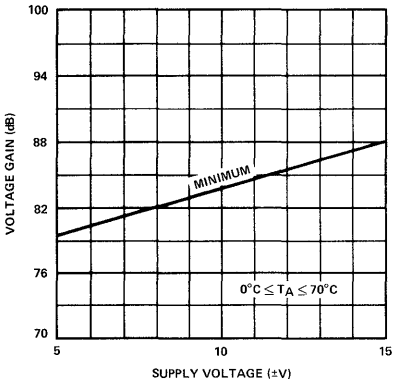
INPUT VOLTAGE RANGE



OUTPUT SWING

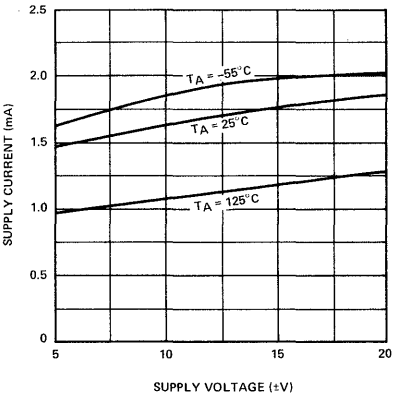


VOLTAGE GAIN

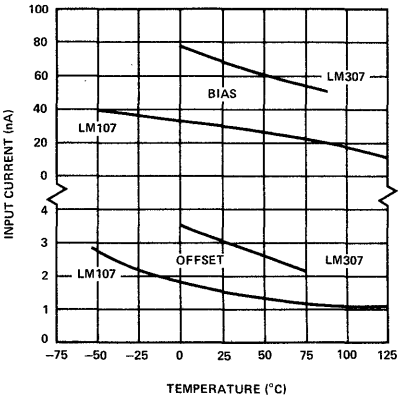


TYPICAL PERFORMANCE CURVES

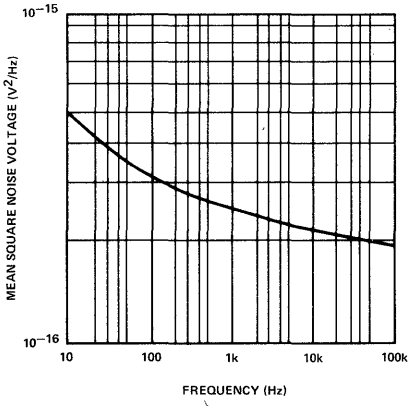
SUPPLY CURRENT



INPUT CURRENT

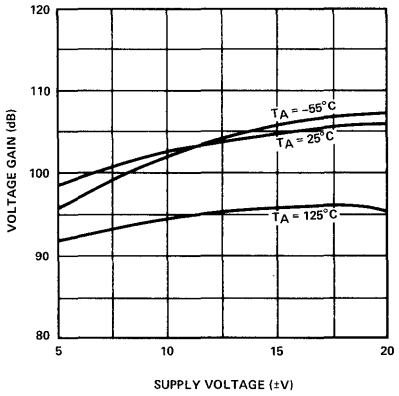


INPUT NOISE VOLTAGE

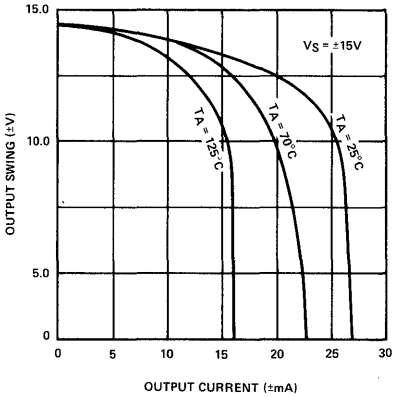


TYPICAL PERFORMANCE CURVES (cont'd)

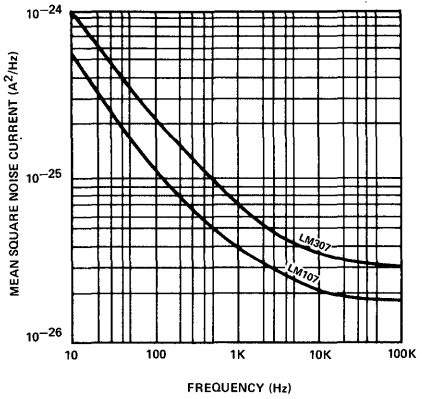
VOLTAGE GAIN



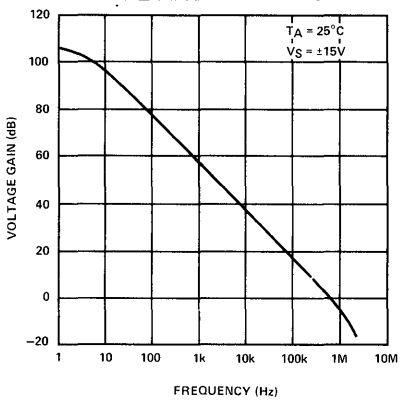
CURRENT LIMITING



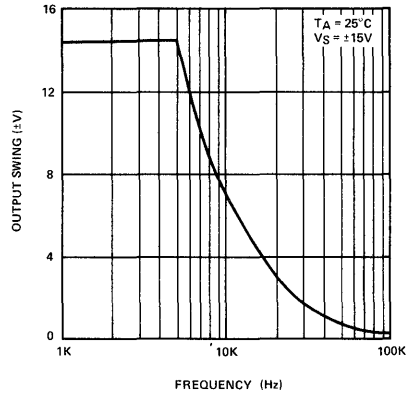
INPUT NOISE CURRENT



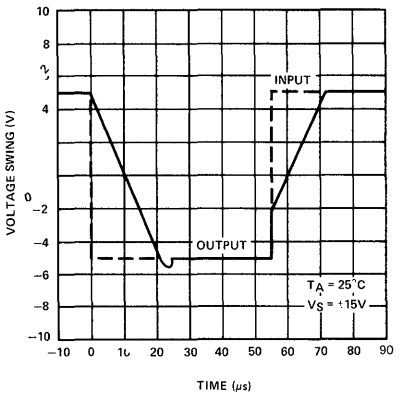
OPEN LOOP FREQUENCY RESPONSE



LARGE SIGNAL FREQUENCY RESPONSE

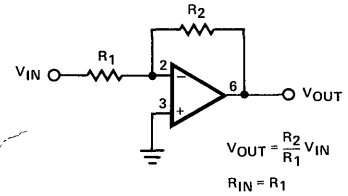


VOLTAGE FOLLOWER PULSE RESPONSE



TYPICAL APPLICATIONS

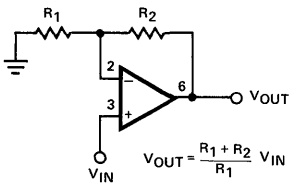
INVERTING AMPLIFIER



$V_{OUT} = \frac{R_2}{R_1} V_{IN}$

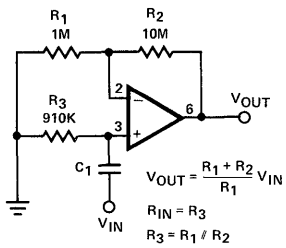
$R_{IN} = R_1$

NON-INVERTING AMPLIFIER



$V_{OUT} = \frac{R_1 + R_2}{R_1} V_{IN}$

NON-INVERTING AC AMPLIFIER



$V_{OUT} = \frac{R_1 + R_2}{R_1} V_{IN}$

$R_{IN} = R_3$

$R_3 = R_1 \,/\!/\, R_2$

DESCRIPTION

The 5556 is an internally compensated precision monolithic operational amplifier featuring extremely low offset and bias currents and offset null capability. The 5556 is short circuit protected and its high common mode and differential input voltage range provides exceptional performance when used as an integrator, summing amplifier, and voltage follower.

The 5556 features industry standard pinout and is a direct pin-for-pin replacement for the MC15556G and MC1456G.

ABSOLUTE MAXIMUM RATINGS

Power Supply Voltage

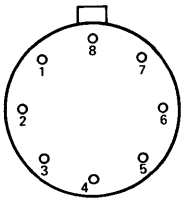
S5556	±22V
N5556	±18V
Differential Input Voltage	± V^+
Common Mode Input Voltage	± V^+
Load Current	20mA
Output Short Circuit Duration	Indefinite
Power Dissipation	680mW
Derate Above T_A = 25°C	4.6mW/°C
Operating Temperature Range	
S5556	−55°C to +125°C
N5556	0°C to +70°C
Storage Temperature Range	−65°C to +150°C

FEATURES

- LOW INPUT BIAS CURRENT - 15nA maximum
- LOW INPUT OFFSET CURRENT - 2.0nA maximum
- LOW INPUT OFFSET VOLTAGE - 4.0mV maximum
- HIGH SLEW RATE - 2.5 V/μs typical
- LARGE POWER BANDWIDTH - 40kHz typical
- LOW POWER CONSUMPTION - 45mW maximum
- OFFSET VOLTAGE NULL CAPABILITY

PIN CONFIGURATIONS (Top View)

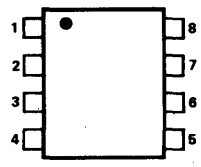
T PACKAGE



1. Offset Null
2. Inverting Input
3. Non-inverting Input
4. V^-
5. Offset Null
6. V_{OUT}
7. V^+
8. NC

Order Part Nos. S5556T/N5556T

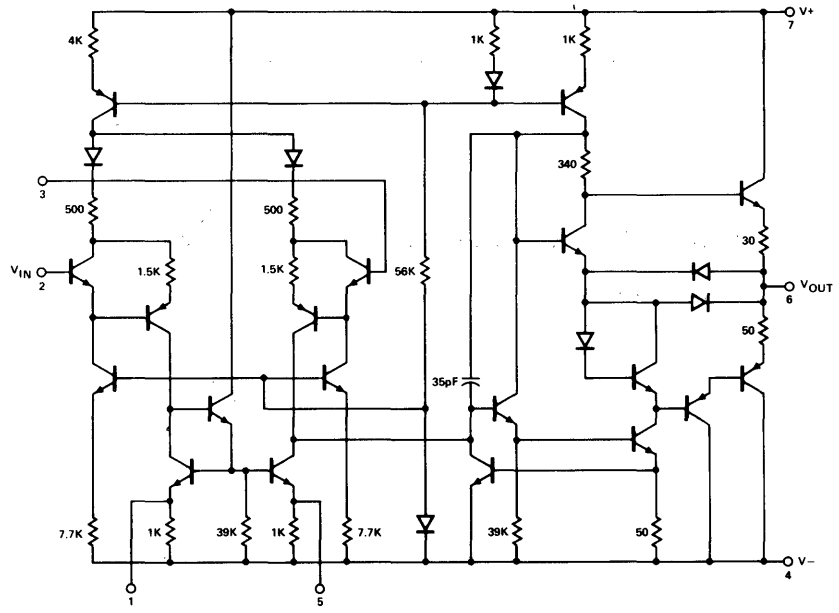
V PACKAGE



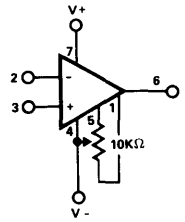
1. Offset Null
2. Inverting Input
3. Non-inverting Input
4. V^-
5. Offset Null
6. V_{OUT}
7. V^+
8. NC

Order Part Nos. S5556V/N5556V

EQUIVALENT CIRCUIT



OFFSET ADJUST CIRCUIT



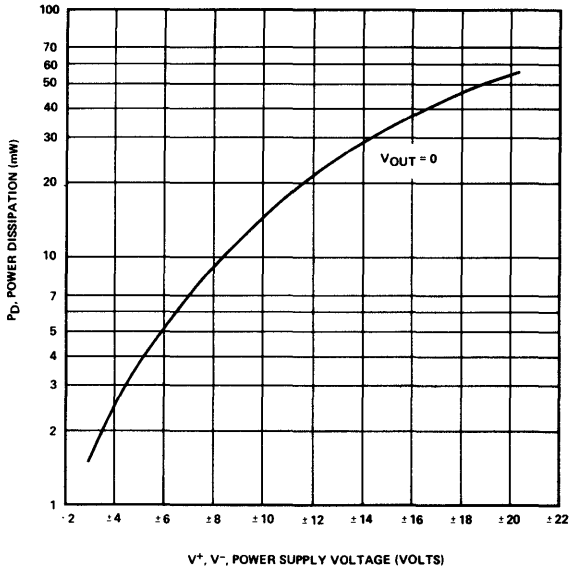
ELECTRICAL CHARACTERISTICS ($V^+ = +15V$, $V^- = -15V$, $T_A = +25°C$ Unless Otherwise Noted)

PARAMETER	SYMBOL	MIN		TYP		MAX		UNITS
		S5556	N5556	S5556	N5556	S5556	N5556	
Input Bias Current	I_B							
$T_A = 25°C$				8	15	15	30	nA
$T_A = T_{LOW}$ to T_{HIGH} (Note 1)						30	40	nA
Input Offset Current	I_{io}							
$T_A = 25°$				1.0	5.0	2.0	10	nA
$T_A = 25°C$ to T_{High}						3.0	14	nA
$T_A = T_{LOW}$ to 25°C						5.0	14	nA
Input Offset Voltage	V_{io}							
$T_A = 25°C$				2.0	5.0	4.0	10	mV
$T_A = T_{LOW}$ to T_{HIGH}						6.0	14	mV
Differential Input Impedance (Open Loop–f = 20Hz)								
Parallel Input Resistance	R_p			5.0	3.0			M
Parallel Input Capacitance	C_p			6.0	6.0			pF
Common Mode Input Impedance (f = 20Hz)	Z_{IN}			250	250			M
Common Mode Input Voltage Swing	CMV_{IN}	±12	±11	±13	±12			V
Equivalent Input Noise Voltage	E_{IN}			45	45			$nV/\sqrt{Hz}$
(Av = 100, Rs = 10KΩ, F = 1.0KHz, BW = 1.0Hz)								
Common Mode Rejection Ratio (f = 100Hz)	CMRR	80	70	110	110			dB
Open Loop Voltage Gain (V_{Out} = ±10V, R_L = 2KΩ)	AVO							
$T_A = 25°C$		100K	70K	200K	100K			V/V
$T_A = T_{LOW}$ to T_{HIGH}		40K	40K					V/V
Power Bandwidth Av = 1, R_L = 2KΩ, THD ≤ 5%, V_{OUT} = ±10V)	P_{BW}			40	40			KHz
Unity Gain Crossover Frequency (open-loop)				1.0	1.0			MHz
Phase Margin (open-loop, unity gain)				70	70			Degrees
Gain Margin				18	18			dB
Slew Rate (unity gain)	dV_{OUT}/dt			2.5	2.5			V/μsec
Output Impedance (f = 20Hz)	Z_{OUT}			1.0	1.0	2.0	2.5	KΩ
Output Voltage Swing (R_L = 2KΩ)	V_{OUT}	±12	±11	±13	±12			V
Power Supply Sensitivity								
V^- = Constant, RS ≤ 10K	S^+			50	75	100	200	MV/V
V^+ = Constant, RS ≤ 10K	S^-			50	75	100	200	MV/V
Power Supply Current	I_{D+}			1.0	1.3	1.5	3.0	mA
	I_{D-}			1.0	1.3	1.5	3.0	mA
DC Quiescent Power Dissipation (V_{OUT} = 0)	P_D			30	40	45	90	mW

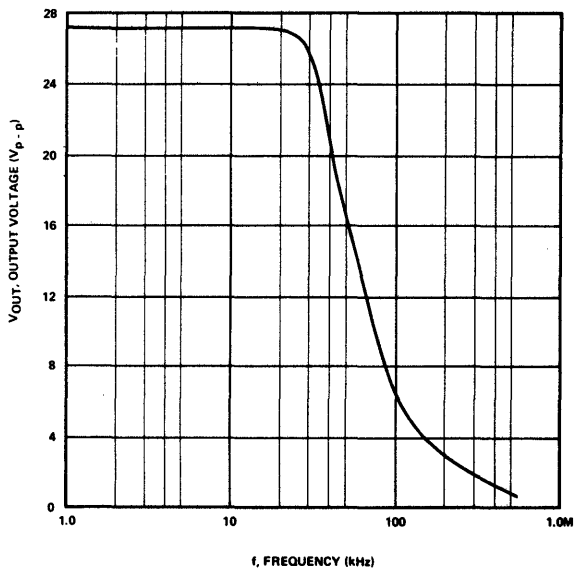
NOTE:
1. $T_{LOW} = 0°C$ for N5556, –55°C for S5556; $T_{HIGH} = 70°C$ for N5556, 125°C for S5556

TYPICAL PERFORMANCE CHARACTERISTICS

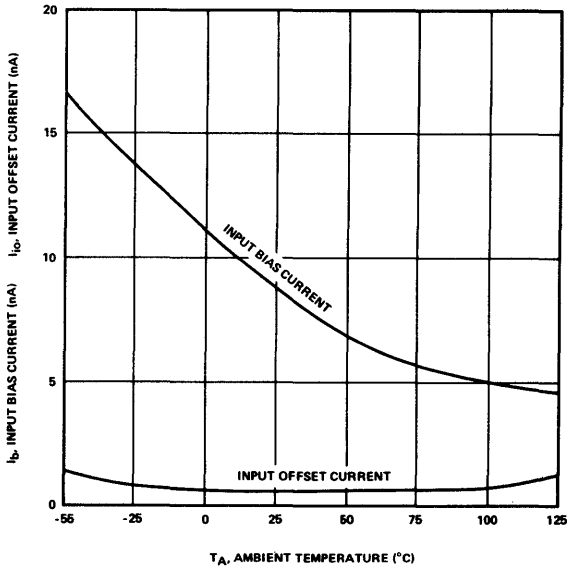
POWER DISSIPATION VERSUS POWER SUPPLY VOLTAGE



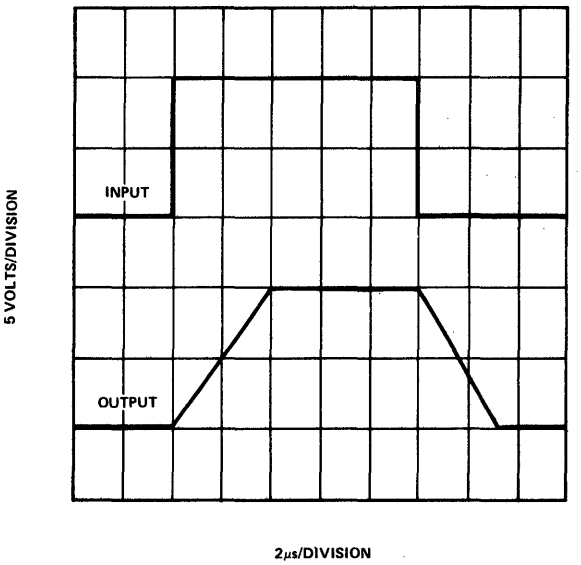
POWER BANDWIDTH



TYPICAL INPUT BIAS CURRENT AND INPUT OFFSET CURRENT VERSUS TEMPERATURE FOR S5556



VOLTAGE-FOLLOWER PULSE RESPONSE



DESCRIPTION

The 5558 consists of a pair of high performance monolithic operational amplifiers constructed on a single chip. It features internal compensation and is intended for use in a variety of analog applications. High common mode voltage range and immunity to latch-up makes the 5558 ideal for use as a voltage follower. The high gain and wide range of operating voltage achieves superior performance in integrator, summing amplifier, and general feedback applications. The device is short-circuit protected. For single amplifier performance see the 5741 data sheet. The 5558 is a pin-for-pin replacement for the MC1558G.

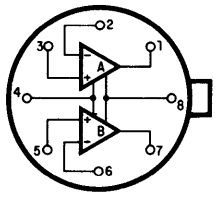
ABSOLUTE MAXIMUM RATINGS

Power Supply Voltages	
S5558	±22V
N5558	±18V
Differential Input Voltage	±30V
Common-mode Input Swing	±15V
Output Short Circuit Duration	Continuous
Power Dissipation (Note 1)	
T Package – (MO-002-AG)	680mW
Operating Temperature Range	
S5558	–55°C to +125°C
N5558	0°C to +75°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Note 1. Derate linearly at 4.6 mW/°C for ambient temperatures above +25°C

PIN CONFIGURATIONS

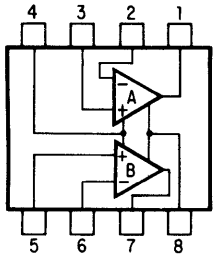
T-PACKAGE
(Top View)



1. Output A
2. Inverting Input A
3. Noninverting Input A
4. V^-
5. Noninverting Input B
6. Inverting Input B
7. Output B
8. V^+

ORDER PART NOS. S5558T/N5558T

V-PACKAGE



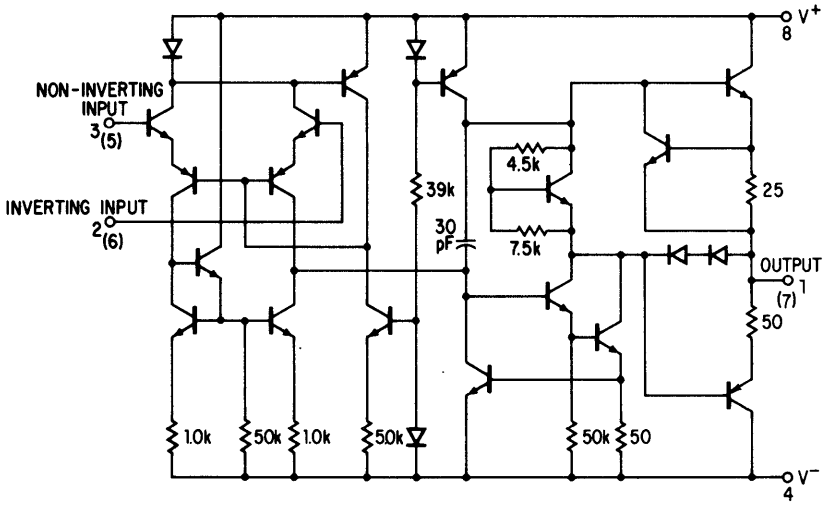
1. Output A
2. Inverting Input A
3. Noninverting Input A
4. V^-
5. Noninverting Input B
6. Inverting Input B
7. Output B
8. V^+

ORDER PART NO. N5558V

FEATURES:

- "OP AMPS" IN SPACE OF ONE 5741A ('V' PACKAGE)
- NO FREQUENCY COMPENSATION REQUIRED
- SHORT CIRCUIT PROTECTION
- LOW POWER CONSUMPTION
- LARGE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGES
- NO LATCH-UP

EQUIVALENT SCHEMATIC



The numbers without parenthesis represent the pin numbers for ½ of the dual circuit. The numbers in parenthesis represent the pin numbers for the other half.

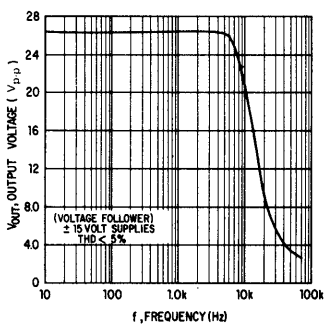
ELECTRICAL CHARACTERISTICS ($V^+ = +15$ Vdc, $V^- = -15$ Vdc, $T_A = +25°C$ unless otherwise noted)

CHARACTERISTICS	SYMBOL	MIN		TYP		MAX		UNIT
		S5558	N5558	S5558	N5558	S5558	N5558	
Input Bias Current	I_b							μAdc
$T_A = +25°C$				0.2	0.2	0.5	0.5	
$T_A = T_{low}$ to T_{high} (See Note 1)						1.5	0.8	
Input Offset Current	$\|I_{io}\|$							μAdc
$T_A = +25°C$				0.03	0.03	0.2	0.2	
$T_A = T_{low}$ to T_{high}						0.5	0.3	
Input Offset Voltage ($R_S \leq 10k\Omega$)	$\|V_{io}\|$							mVdc
$T_A = +25°C$				1.0	2.0	5.0	6.0	
$T_A = T_{low}$ to T_{high}						6.0	7.5	
Differential Input Impedance (Open-Loop, f = 20 Hz)								
Parallel Input Resistance	R_P	0.3	0.3	1.0	1.0			Megohm
Parallel Input Capacitance	C_P			6.0	6.0			pF
Common-Mode Input Impedance (f = 20 Hz)	$Z_{(in)}$			200	200			Megohms
Common-Mode Input Voltage Swing	CMV_{in}	±12	±12	±13	±13			V_{pk}
Equivalent Input Noise Voltage	e_n							nV(Hz)½
($A_V = 100$, $R_s = k\Omega$, f = 1.0 kHz, BW = 1.0 Hz)				45	45			
Common-Mode Rejection Ratio (f = 100 Hz)	CM_{rej}	70	70	90	90			dB
Open-Loop Voltage Gain, ($V_{out} = \pm 10V$, $R_L = 2.0k\Omega$)	A_{VOL}							V/V
$T_A = +25°C$		50,000	20,000	200,000	100,000			
$T_A = T_{low}$ to T_{high}		25,000	15,000					
Power Bandwidth ($A_V = 1$, $R_L = 2.0k\Omega$, THD≤5%, $V_{out} = 20V_{p-p}$)	P_{BW}			14	14			kHz
Unity Gain Crossover Frequency (open-loop)				1.1	1.1			MHz
Phase Margin (open-loop, unity gain)				65	65			degrees
Gain Margin				11	11			dB
Slew Rate (Unity Gain)	dV_{out}/dt			0.8	0.8			V/μs
Output Impedance (f = 20 Hz)	Z_{out}			300	300			ohms
Short-Circuit Output Current	I_{SC}			20	20			mAdc
Output Voltage Swing	V_{out}							V_{pk}
($R_L = 10k\Omega$)		±12	±12	±14	±14			
$R_L = 2k\Omega$ ($T_A = T_{low}$ to T_{high})		±10	±10	±13	±13			
Power Supply Sensitivity								μV/V
V^- = constant, $R_s \leq 10k\Omega$	S^+			30	30	150	150	
V^+ = constant, $R_s \leq 10k\Omega$	S^-			30	30	150	150	
Power Supply Current	I_D^+			2.3	2.3	5.0	5.6	mAdc
	I_D^-			2.3	2.3	5.0	5.6	
DC Quiescent Power Dissipation ($V_{out} = 0$)	P_D			70	70	150	170	mW
Channel Separation	e_{o1}/e_{o2}			120	120			dB

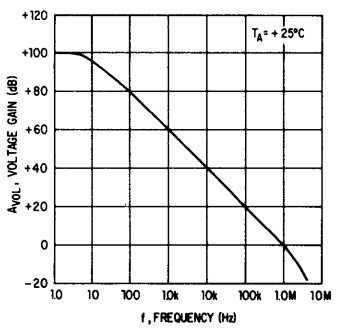
Note 1: T_{low}: 0°C for N5558, −55°C for S5558; T_{high}: +75°C for N5558, +125°C for S5558

TYPICAL CHARACTERISTIC CURVES

POWER BANDWIDTH (Large Signal Swing versus Frequency)



OPEN LOOP FREQUENCY RESPONSE



DESCRIPTION

The μA709 is a high performance monolithic operational amplifier with differential inputs. High open loop gain, high input impedance, wide input common mode and output voltage ranges plus low temperature drift enable it to be used in many applications formerly satisfied only by discrete amplifiers.

FEATURES

- **OPEN LOOP VOLTAGE GAIN =** **45,000**
- **OUTPUT VOLTAGE SWING =** **±14V**
- **INPUT COMMON MODE RANGE =** **±10V**
- **DIFFERENTIAL INPUT RESISTANCE = μA709 250kΩ**
  μA709C 400kΩ

ABSOLUTE MAXIMUM RATINGS

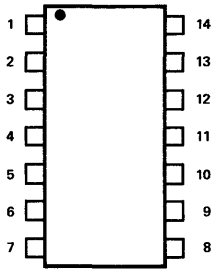
Supply Voltage	±18V
Internal Power Dissipation (Note 1)	N5709 250 mW
	S5709 300 mW
Differential Input Voltage	±5.0V
Input Voltage	±10V
Open Short-Circuit Duration (T_A = 25°C)	-25°C
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	μA709C 0°C to +75°C
	μA709 -55°C to +125°C
Lead Temperature (Soldering, 60 sec)	300°C

NOTE:

1. Rating applied for case temperatures to +125°C; derate linearly at 5.6mW/°C for ambient temperatures above +95°C.

PIN CONFIGURATIONS

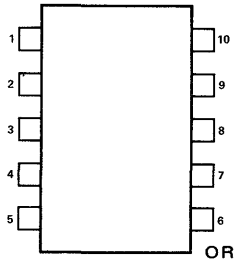
A PACKAGE
(Top View)



ORDER PART NOS.
μA790A/μA709CA

1. NC
2. NC
3. Input compensation A
4. Inverting input
5. Non-inverting input
6. V^-
7. NC
8. NC
9. Output Compensation
10. Output
11. V^+
12. Input compensation B
13. NC
14. NC

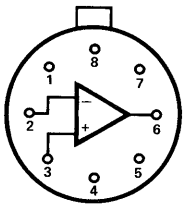
G PACKAGE



1. NC
2. Input compensation A
3. Inverting input
4. Non-inverting input
5. V^-
6. Output compensation
7. Output
8. V^+
9. Input compensation B
10. NC

ORDER PART NOS. μA709G/μA709CG

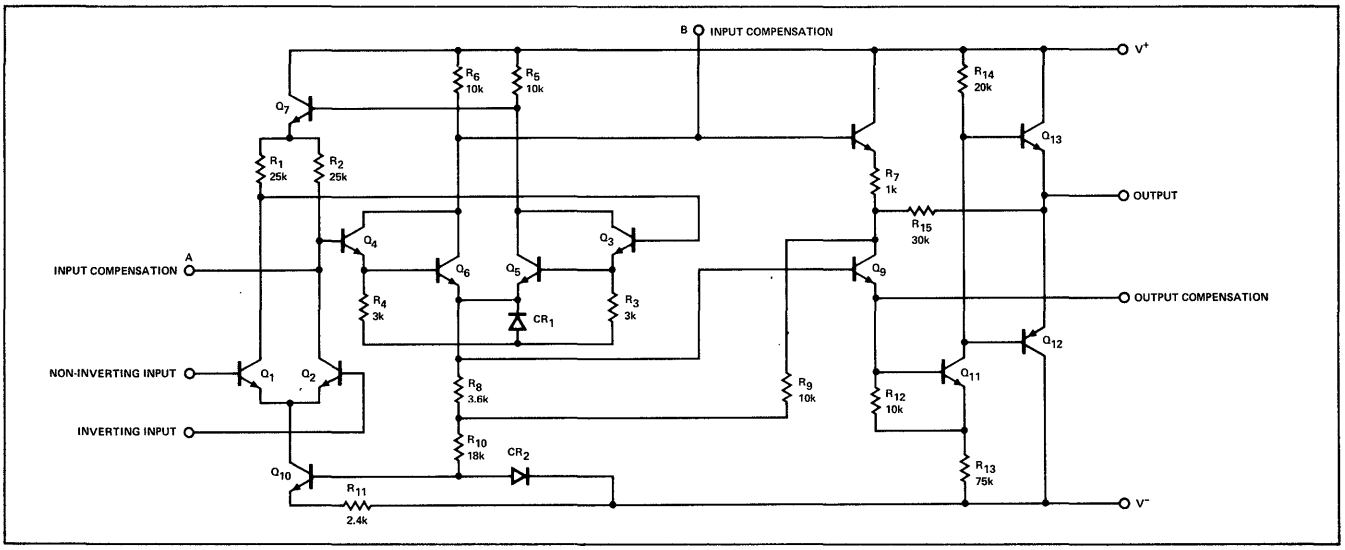
T PACKAGE



1. Input compensation A
2. Inverting input
3. Non-inverting input
4. V^-
5. Output compensation
6. Output
7. V^+
8. Input compensation B

ORDER PART NOS. μA709T/μA709CT

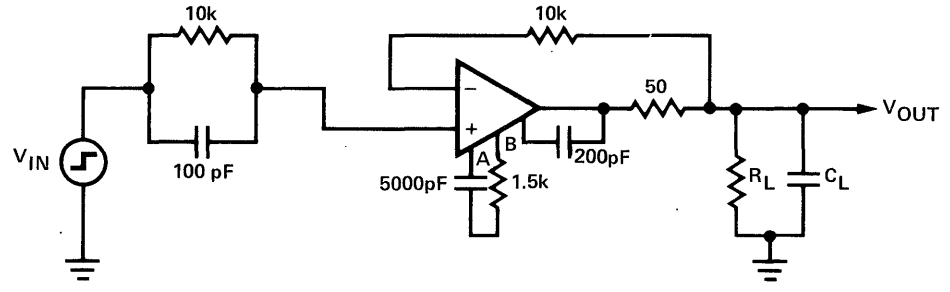
BASIC CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS ($T_A = \pm 25^\circ C$, $V_S = \pm 15V$ (709C); $\pm 9 \leq V_S \leq \pm 15$ (709) unless otherwise specified)

PARAMETER	TEST CONDITIONS	μA709			μA709C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS								
Offset Voltage @ 25°C	$R_S \leq 10K\Omega$, $+9V, \leq V_S \leq +15V$		1	5		2	7.5	mV
Over Temperature	$R_S \leq 10K\Omega$, $\pm 9V \leq \pm 15V$			6			10	mV
Offset Current @ 25°C			50	200		100	500	nA
Over Temperature	$T_A = +125^\circ C$		20	200				nA
	$T_A = -55^\circ C$		100	500				nA
	$0^\circ C \leq T_A \leq 75^\circ C$						750	nA
Bias Current @ 25°C			200	500		300	1500	nA
Over Temperature	$T_A = -55^\circ C$		0.5	1.5				μA
INPUT RESISTANCE @ 25°C		150	400		50	250		kΩ
Over Temperature		40	100		35			kΩ
INPUT VOLTAGE RANGE @ 25°C					±8.0	±10		V
Over Temperature	$V_S = \pm 15V$	±8.0	±10					V
OUTPUT CHARACTERISTICS								
Resistance @ 25°C			150			150		Ω
Voltage Swing	$R_L \geq 10K\Omega$				±12	±14		V
	$R_L \geq 2k\Omega$				±10	±13		V
Over Temperature	$V_S = \pm 15V$, $R_L \geq 10K\Omega$	±12	±14					V
	$V_S = \pm 15V$, $R_L \geq 2K\Omega$	±10	±13					V
POWER CONSUMPTION	$V_S = +15V$		80	165		80	200	mW
TRANSIENT RESPONSE (Figure 1)	$V_{in} = 10mV$, $R_L = 2K\Omega$							
Rise Time			0.3	1.0		0.3	1.0	μW
Overshoot	$C_L \leq 100$ pF		10	30		10	30	%
LARGE SIGNAL VOLTAGE GAIN @ 25°C	$R_L \geq 25K\Omega$, $V_{out} = \pm 10V$				15,000	45,000		V/V
Over Temperature	$R_L \geq 25K\Omega$, $V_{out} = \pm 10V$	25,000	45,000	70,000	12,000			V/V
COMMON MODE REJECTION RATIO @ 25°C	$R_S \leq 10K\Omega$				65	90		dB
Over Temperature	$R_S \leq 10K\Omega$	70	90					dB
SUPPLY VOLTAGE REJECTION RATIO @ 25°C	$R_S \leq 10K\Omega$					25	200	mV/V
Over Temperature	$R_S \leq 10K\Omega$	25	150					μV/V
AVERAGE TEMPERATURE Coefficient of Input	$R_S = 50\Omega$		3.0					μV/°C
Offset Voltage	$R_S \leq 10K\Omega$		6.0					μV/°C

TEST CIRCUIT



DESCRIPTION

The μA740 is a special purpose high performance operational amplifier utilizing a FET input stage for high input impedance and low input current.

The device features internal compensation, standard pinout, wide differential and common mode input voltage range, high slew rate and high output drive capability.

FEATURES

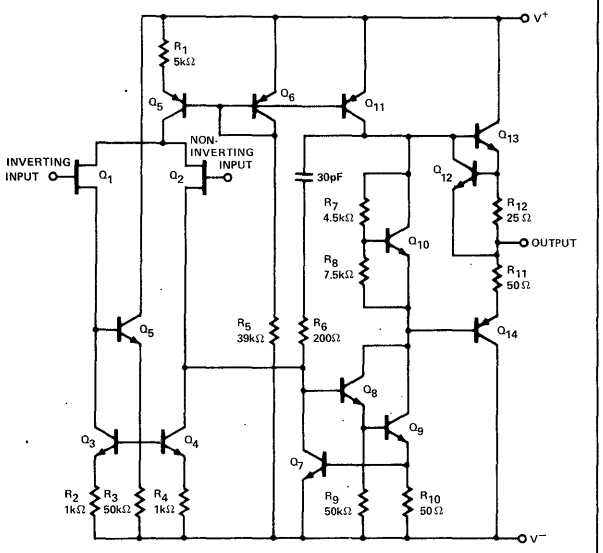
- 0.1 nA INPUT BIAS CURRENT
- INPUT AND OUTPUT PROTECTION
- OFFSET NULL CAPABILITY
- INTERNALLY COMPENSATED
- 6V/μsec SLEW RATE
- STANDARD PINOUT
- NO LATCH UP

ABSOLUTE MAXIMUM RATING

Supply Voltage	±22V
Differential Input Voltage Range	±30V
Common Mode Input Voltage Range	$\pm V_S$
Power Dissipation (Note 1)	500mW
Operating Temperature Range	0°C to +70° C
Storage Temperature Range	−65°C to +150° C
Lead Temperature (Solder, 60 sec)	300° C
Output short Circuit Duration (Note 2)	Indefinite

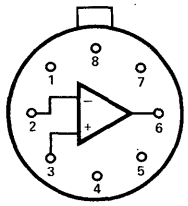
1. Rating applies for case temperatures to +25°V; derate linearly at 6.5mW/°C for ambient temperatures above 75°C.
2. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

EQUIVALENT CIRCUIT



PIN CONFIGURATION (Top View)

T PACKAGE

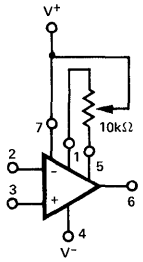


1. Offset Null
2. Inverting Input
3. Non-inverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. NC

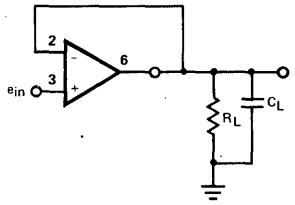
ORDER PART NOS. μA740T/μA740CT

TEST CIRCUITS

OFFSET NULL CIRCUIT



VOLTAGE FOLLOWER CIRCUIT

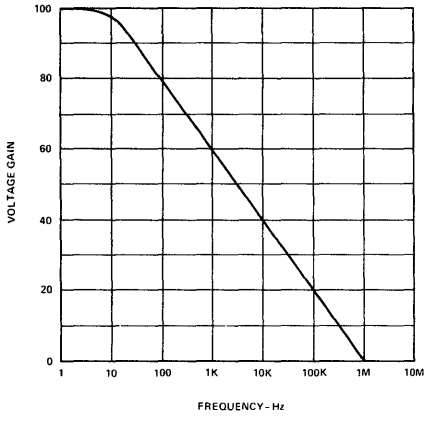


ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_C = 25°C unless otherwise specified)

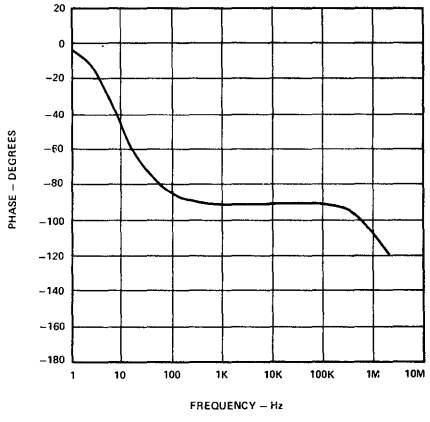
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 100$ kΩ		30		mV
Input Offset Current			60		pA
Input Current (either input)			0.1	2.0	nA
Input Resistance			1,000,000		MΩ
Large Signal Voltage Gain	$R_L \geq 2$kΩ, V_{out} = ±10V		1,000,000		
Output Resistance			75		Ω
Output Short-Circuit Current			20		mA
Supply Current			4.2	3.0	mA
Power Consumption			126	240	mW
Slew Rate			6.0		V/μs
Unity Gain Bandwidth			1.0		MHz
Transient Response (Unity Gain)	$C_L \leq 100$ pF, R_L = 2 kΩ, V_{in} = 100 mV				
Risetime			300		ns
Overshoot			10		%
The following specifications apply for 0°C ≤ T_A ≤ +70°C					
Input Voltage Range			±12		V
Common Mode Rejection Ratio			80		db
Supply Voltage Rejection Ratio			70		μV/V
Large Signal Voltage Gain			500,000		
Output Voltage Swing	$R_L \geq 10$ kΩ	±12	±14		V
	$R_L \geq 2$ kΩ	±10	±13		V
Input Offset Voltage			30		mV
Input Offset Current			60		pA
Input Current (either input)			1.1	10	nA

TYPICAL CHARACTERISTIC CURVES

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



DESCRIPTION

The μA741 is a high performance operational amplifier with high open loop gain, internal compensation, high common mode range and exceptional temperature stability. The μA741 is short-circuit protected and allows for nulling of offset voltage.

FEATURES

- INTERNAL FREQUENCY COMPENSATION
- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- EXCELLENT TEMPERATURE STABILITY
- HIGH INPUT VOLTAGE RANGE
- NO LATCH-UP

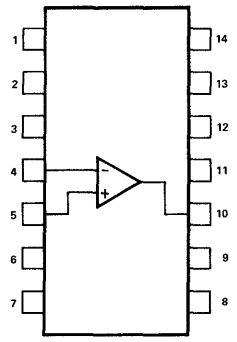
ABSOLUTE MAXIMUM RATINGS

	μA741C	μA741
Supply Voltage	±18V	±22V
Internal Power Dissipation (Note 1)	500mW	500mW
Differential Input Voltage	±30V	±30V
Input Voltage (Note 2)	±15V	±15V
Voltage between Offset Null and V^-	±0.5V	±0.5V
Operating Temperature Range	0°C to +70°C	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C
Lead Temperature (Solder, 60 sec)	300°C	300°C
Output Short Circuit Duration (Note 3)	Indefinite	Indefinite

Notes
1. Rating applies for case temperatures to 125°C; derate linearly at 6.5mW/°C for ambient temperatures above +75°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

PIN CONFIGURATIONS

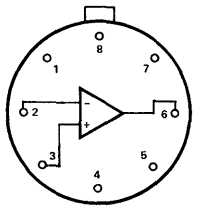
A PACKAGE
(Top View)



1. NC
2. NC
3. Offset Null
4. Inv. Input
5. Non-Inv. Input
6. V^-
7. NC
8. NC
9. Offset Null
10. Output
11. V^+
12. NC
13. NC
14. NC

ORDER PART NO. μA741CA

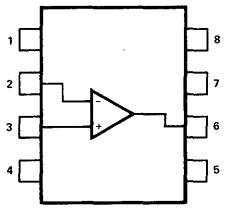
T PACKAGE



1. Offset Null
2. Inverting Input
3. Non-Inverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. NC

ORDER PART NOS. μA741T/μA741CT

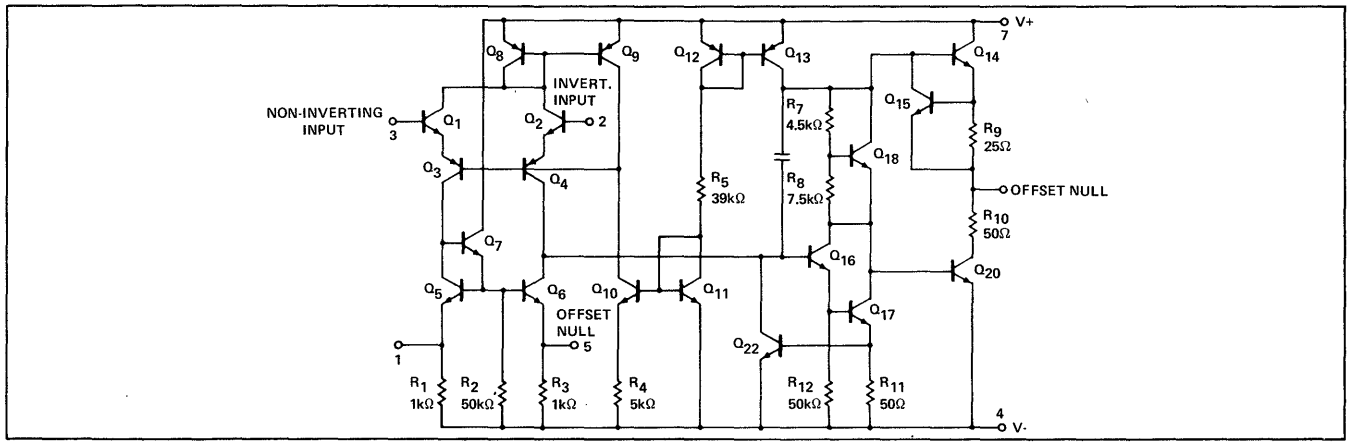
V PACKAGE



1. Offset Null
2. Inv. Input
3. Non-Inv. Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. NC

ORDER PART NO. μA741CV

EQUIVALENT CIRCUIT

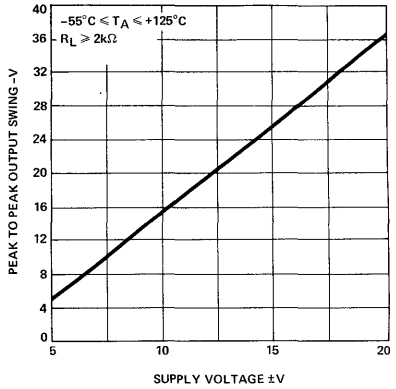


ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$, $T_A = 25°C$ unless otherwise specified)

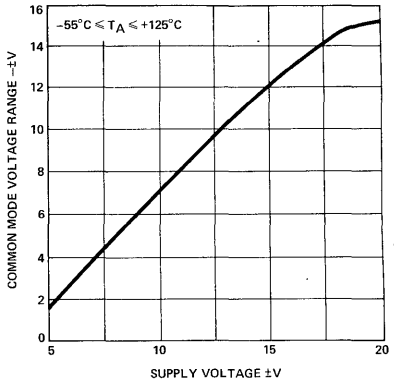
PARAMETER	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
μA741C					
Input Offset Voltage		2.0	6.0	mV	$R_S \leq 10k\Omega$
Input Offset Current		20	200	nA	
Input Bias Current		80	500	nA	
Input Resistance	0.3	2.0		MΩ	
Input Capacitance		1.4		pF	
Offset Voltage Adjustment Range		±15		mV	
Input Voltage Range	±12	±13		V	
Common Mode Rejection Ratio	70	90		dB	$R_S \leq 10k\Omega$
Supply Voltage Rejection Ratio		10	150	μV/V	$R_S \leq 10k\Omega$
Large-Signal Voltage Gain	20,000	200,000			$R_L \geq 2k\Omega$, $V_{out} = \pm 10V$
Output Voltage Swing	±12	±14		V	$R_L \geq 10k\Omega$
	±10	±13		V	$R_L \geq 2k\Omega$
Output Resistance		75		Ω	
Output Short-Circuit Current		25		mA	
Supply Current		1.4	2.8	mA	
Power Consumption		50	85	mW	
Transient Response (unity gain)					$V_{in} = 20mV$, $R_L = 2k\Omega$, $C_L \leq 100pF$
Risetime		0.3		μs	
Overshoot		5.0		%	
Slew Rate		0.5		V/μs	$R_L \geq 2k\Omega$
The following specifications apply for $0°C \leq T_A \leq +70°C$					
Input Offset Voltage			7.5	mV	
Input Offset Current			300	nA	
Input Bias Current			800	nA	
Large-Signal Voltage Gain	15,000				$R_L \geq 2k\Omega$, $V_{out} = \pm 10V$
Output Voltage Swing	±10	±13		V	$R_L \geq 2k\Omega$
μA741					
Input Offset Voltage		1.0	5.0	mV	$R_S \leq 10k\Omega$
Input Offset Current		10	200	nA	
Input Bias Current		80	500	nA	
Input Resistance	0.3	2.0		MΩ	
Input Capacitance		1.4		pF	
Offset Voltage Adjustment Range		±15		mV	
Large-Signal Voltage Gain	50,000	200,000			$R_L \geq 2k\Omega$, $V_{out} = \pm 10V$
Output Resistance		75		Ω	
Output Short Circuit Current		25		mA	
Supply Current		1.4	2.8	mA	
Power Consumption		50	85	mW	
Transient Response (unity gain)					$V_{in} = 20mV$, $R_L = 2k\Omega$, $C_L \leq 100pF$
Risetime		0.3		μs	
Overshoot		5.0		%	
Slew Rate		0.5		V/μs	$R_L \geq 2k\Omega$
The following specifications apply for $-55°C \leq T_A \leq +125°C$					
Input Offset Voltage		1.0	6.0	mV	$R_S \leq 10k\Omega$
Input Offset Current		7.0	200	nA	$T_A = +125°C$
		20	500	nA	$T_A = -55°C$
Input Bias Current		0.03	0.5	μA	$T_A = +125°C$
		0.3	1.5	μA	$T_A = -55°C$
Input Voltage Range	±12	±13		V	
Common Mode Rejection Ratio	70	90		dB	$R_S \leq 10k\Omega$
Supply Voltage Refection Ratio		10	150	μV/V	$R_S \leq 10k\Omega$
Large-Signal Voltage Gain	25,000				$R_L \geq 2k\Omega$, $V_{out} = \pm 10V$
Output Voltage Swing	±12	±14		V	$R_L \geq 10k\Omega$
	±10	±13		V	$R_L \geq 2k\Omega$
Supply Current		1.5	2.5	mA	$T_A = +125°C$
		2.0	3.3	mA	$T_A = -55°C$
Power Consumption		45	75	mW	$T_A = +125°C$
		45	100	mW	$T_A = -55°C$

TYPICAL CHARACTERISTIC CURVES

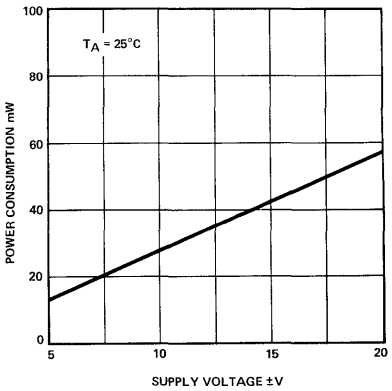
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



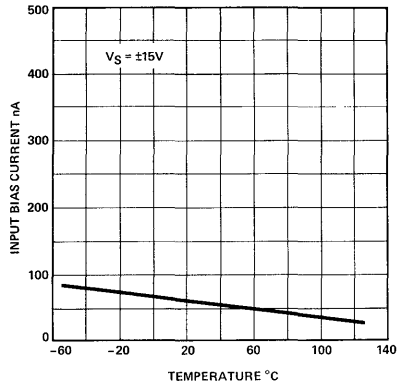
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



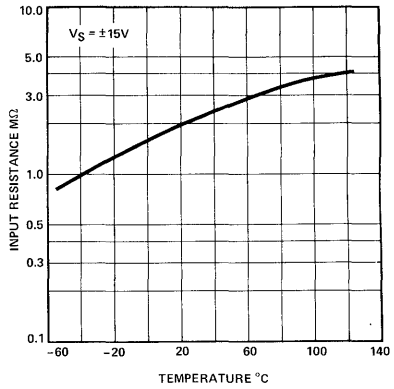
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



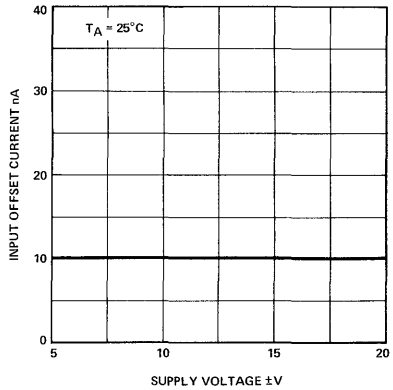
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



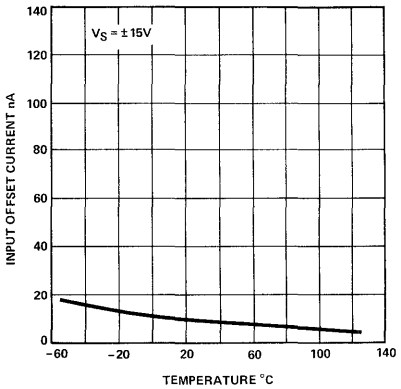
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



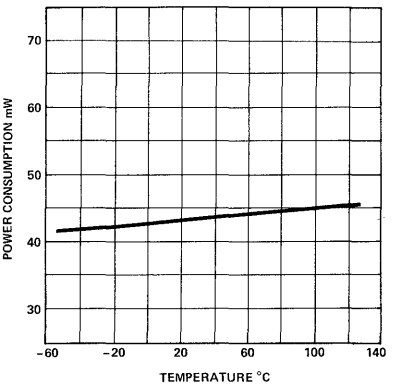
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



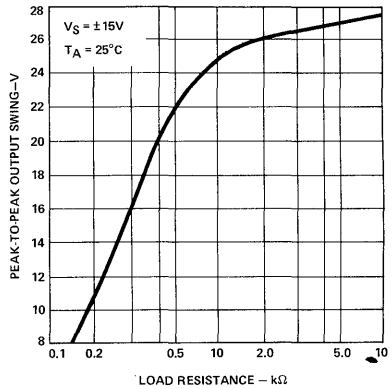
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

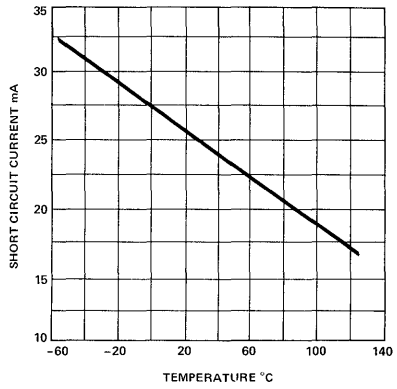


OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

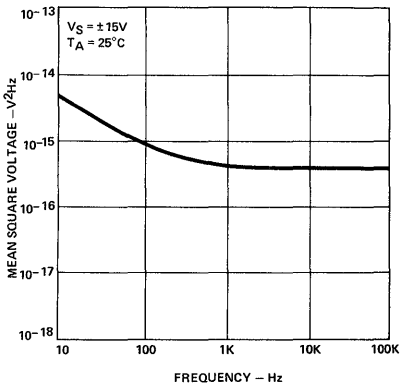


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

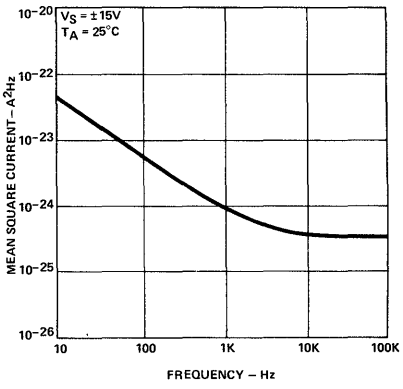
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



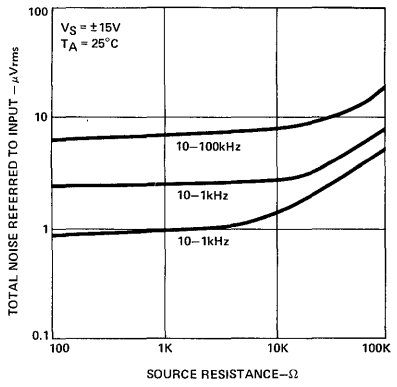
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



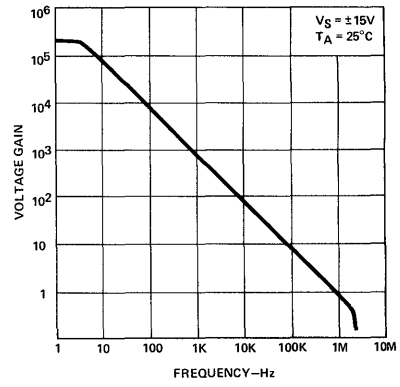
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



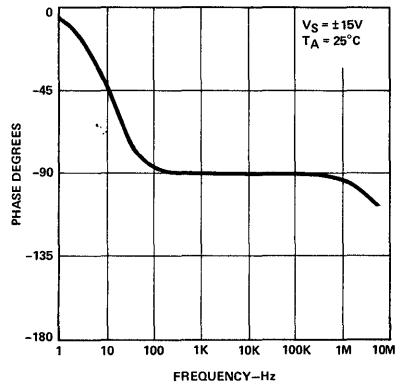
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



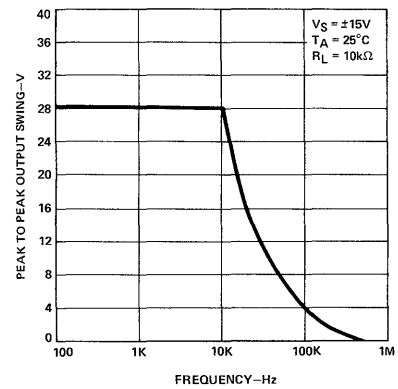
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



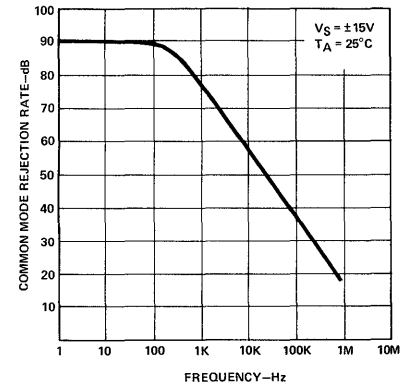
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



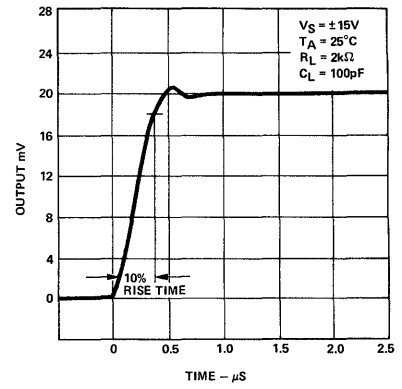
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



TRANSIENT RESPONSE



DESCRIPTION

The μA747 is a pair of high performance monolithic operational amplifiers constructed on a single silicon chip. They are intended for a wide range of analog applications where board space or weight are important. High common mode voltage range and absence of "latch-up" make the μA747 ideal for use as a voltage follower. The high gain and wide range of operating voltage provides superior performance in integrator, summing amplifier, and general feedback applications. The μA747 is short-circuit protected and requires no external components for frequency compensation. The internal 6 db/octave roll-off insures stability in closed loop applications. For single amplifier performance, see μA741 data sheet.

FEATURES

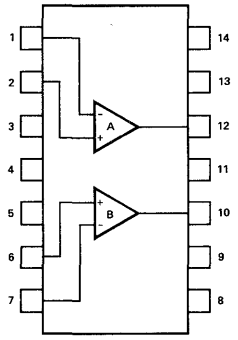
- NO FREQUENCY COMPENSATION REQUIRED
- SHORT-CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH UP

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	A747	+22V
	A747C	+18V
Internal Power Dissipation (Note 1)	Metal Can	500 mW
	DIP	670 mW
Differential Input Voltage		+30V
Input Voltage (Note 2)		+15V
Voltage between Offset Null and V^-		+0.5V
Storage Temperature Range		-65°C to +155°C
Operating Temperature Range	A747	-55°C to +125°C
	A747C	0°C to +70°C
Lead Temperature (Soldering 60 seconds)		300°C
Output Short Circuit Duration (Note 3)		Indefinite

PIN CONFIGURATION

A PACKAGE
(Top View)

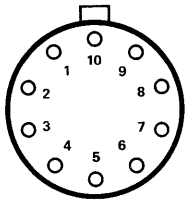


1. Inv Input A
2. Non-inv Input A
3. Offset Null A
4. V^-
5. Offset Null B
6. Non-inv Input B
7. Inv Input B
8. Offset Null B
9. V+ B
10. Output B
11. No Connect
12. Output A
13. V+ A
14. Offset Null A

ORDER PART NOS.

μA747A
μA747CA

K PACKAGE

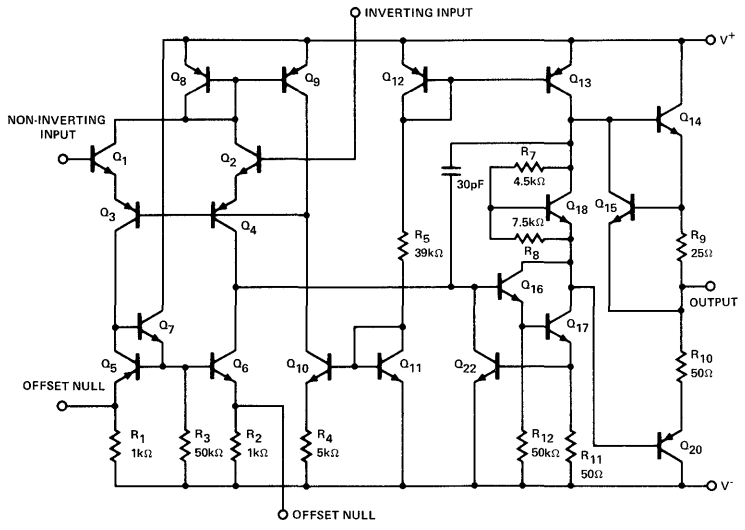


1. Output A
2. V^+ A
3. Inverting Input A
4. Non-inverting Input A
5. V^-
6. Non-inverting Input B
7. Inverting Input B
8. V^+B
9. Output B
10. NC

ORDER PART NOS.

μA747K
μA747CK

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25^\circ C$ unless otherwise specified)

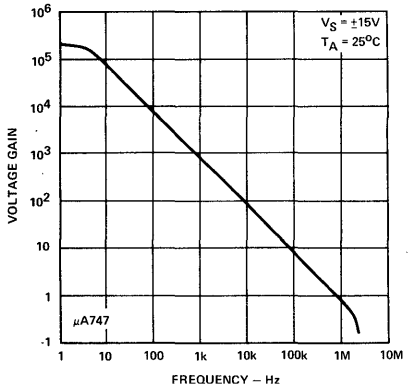
PARAMETERS	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage	$R_S \leq 10$ kΩ		1.0		mV
μA747			5.0		mV
μA747C			6.0		mV
Input Offset Current			20	200	nA
Input Bias Current			80	500	nA
Input Resistance		0.3	2.0		MΩ
Input Capacitance			1.4		pF
Offset Voltage Adjustment Range			±15		mV
Large-Signal Voltage Gain	$R_L \geq 2K\Omega, V_{out} = \pm 10V$		200,000		
μA747		50,000			
μA747C		25,000			
Output Resistance			75		Ω
Output Short-Circuit Current			25		mA
Supply Current			1.7	2.8	mA
Power Consumption			50	85	mW
Transient Response (unity gain)	$V_{in} = 20$ mV, $R_L =$ 2kΩ, $C_L \leq 100$ pF				
Risetime			0.3		μS
Overshoot			5.0		%
Slew Rate	$R_L \geq 2k\Omega$		0.5		V/μS
Channel Separation			120		dB
μA747 ONLY					
The following specifications apply for $-55^\circ C \leq T_A \leq +125^\circ C$					
Input Offset Voltage	$R_S \leq 10k\Omega$		1.0	6.0	mV
Input Offset Current	$T_A = +125^\circ C$		7.0	200	nA
	$T_A = -55^\circ C$		85	500	nA
Input Bias Current	$T_A = +125^\circ C$		0.03	0.5	μA
	$T_A = -55^\circ C$		0.3	1.5	μA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2k\Omega, V_{out} = \pm 10V$	25,000			
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		V
Supply Current	$T_A = +125^\circ C$		1.5	2.5	mA
	$T_A = -55^\circ C$		2.0	3.3	mA
Power Consumption	$T_A = +125^\circ C$		45	75	mW
	$T_A = -55^\circ C$		60	100	mW
μA747C					
The following specifications apply for $0^\circ C \leq T_A \leq +70^\circ C$					
Input Offset Voltage	$R_S \leq 10k\Omega$		1.0	7.5	mV
Input Offset Current			7.0	300	nA
Input Bias Current			0.03	0.8	μA
Input Voltage Range		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2k\Omega, V_{out} = \pm 10V$	15,000			
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		V
Supply Current			2.0	3.3	mA
Power Consumption			60	100	mW

NOTES:

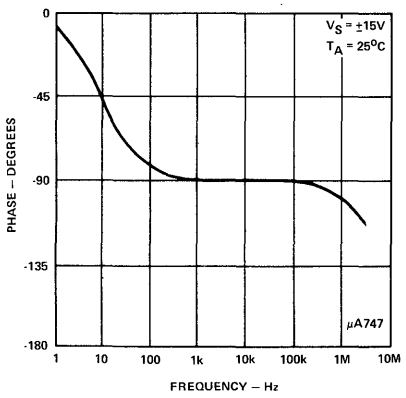
1. Rating applied to ambient temperatures up to $70^\circ C$ ambient derate linearly at 6.3 mW/$^\circ C$ for the Metal Can and 8.3 mW/$^\circ C$ for the Ceramic DIP package.
2. For supply voltages less than +15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Military rating applies to $+125^\circ C$ case temperature or $+60^\circ C$ ambient temperature for each side.

TYPICAL CHARACTERISTIC CURVES

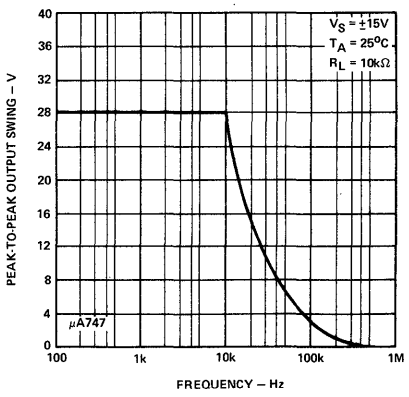
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



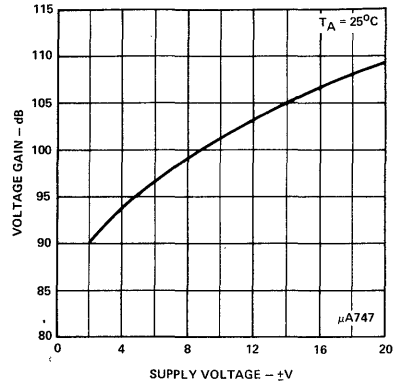
OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY



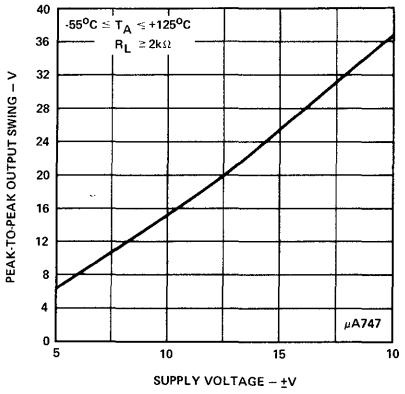
OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY



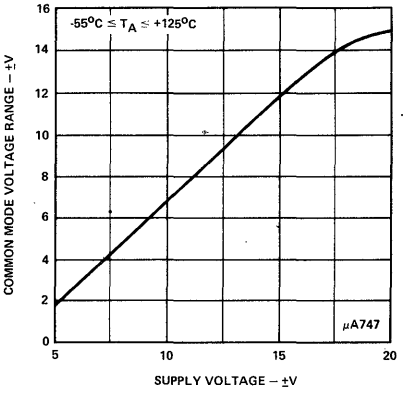
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



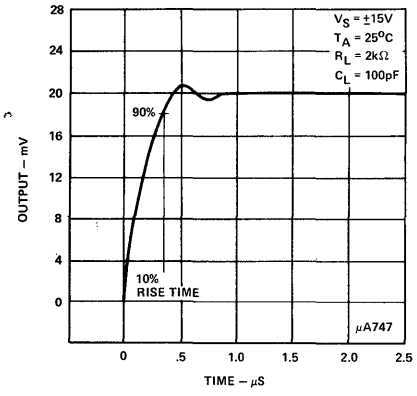
OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



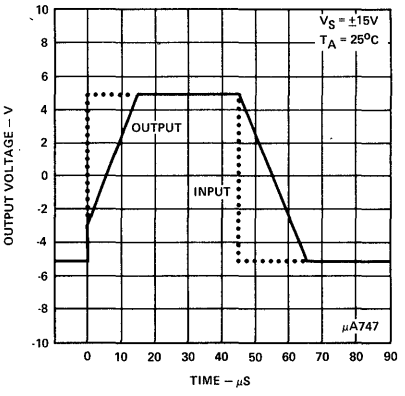
INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE



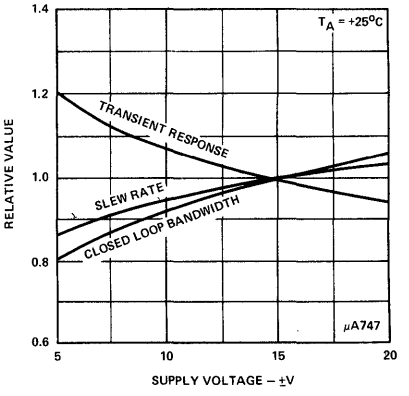
TRANSIENT RESPONSE



VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE

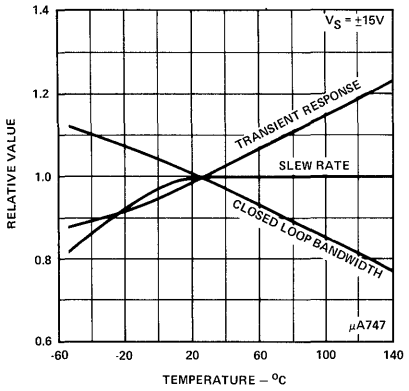


FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE

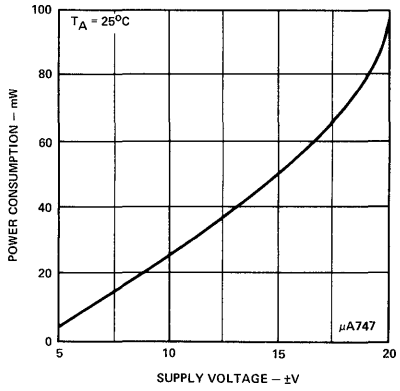


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

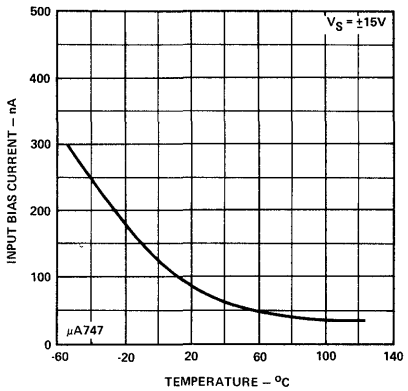
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



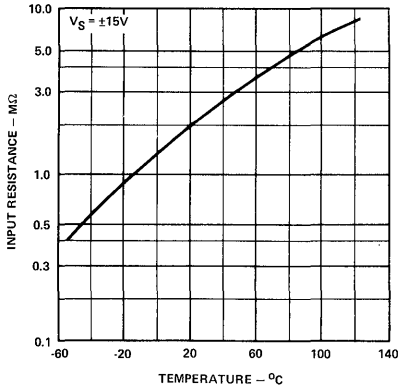
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



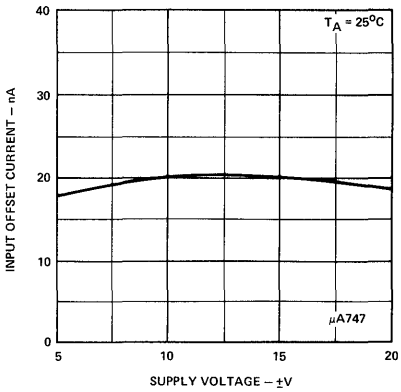
INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



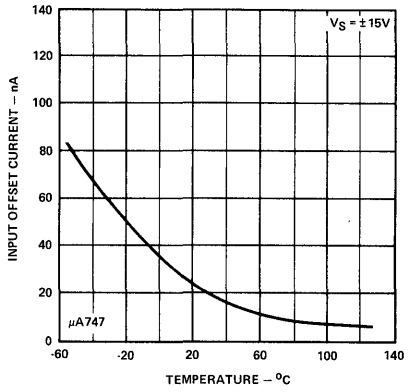
INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE



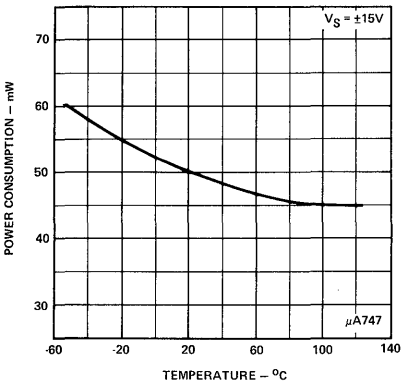
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



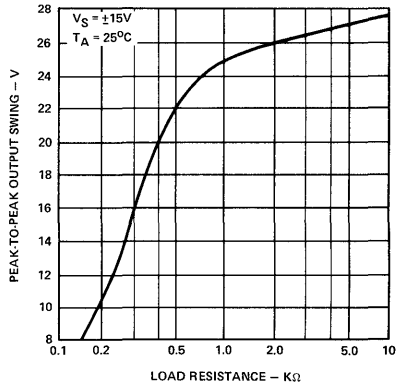
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



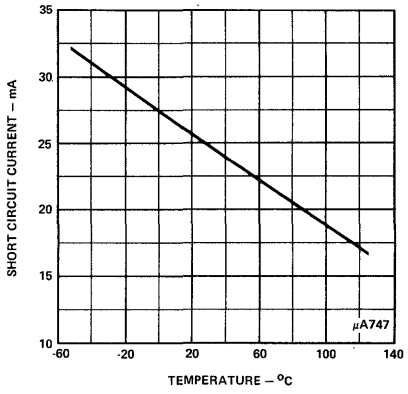
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

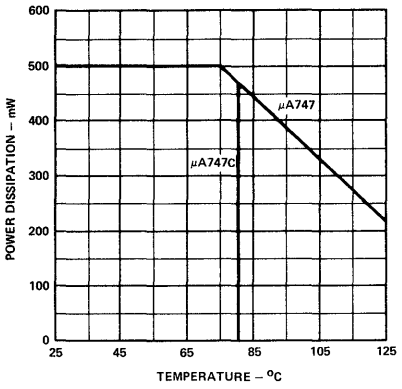


OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

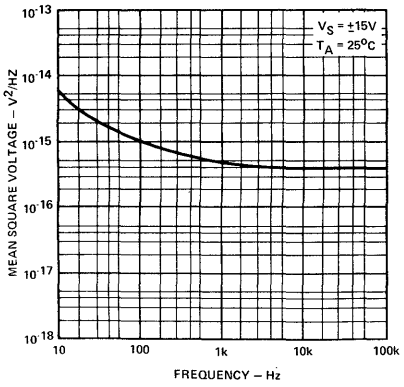


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

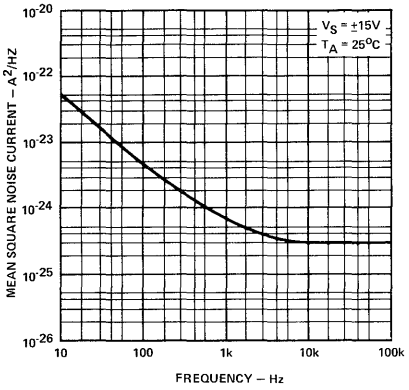
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION AMBIENT TEMPERATURE



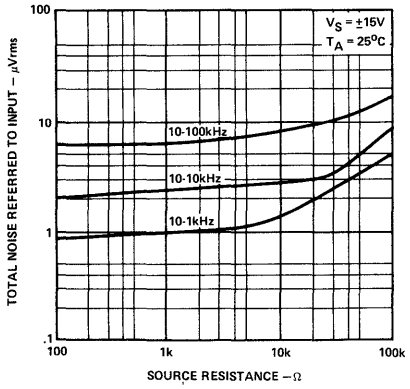
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



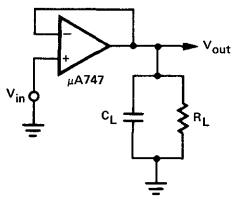
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



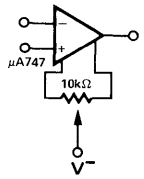
BROADBAND NOISE FOR VARIOUS BANDWIDTHS



TRANSIENT RESPONSE TEST CIRCUIT



VOLTAGE OFFSET NULL CIRCUIT



signetics

HIGH PERFORMANCE OPERATIONAL AMPLIFIER μA748

LINEAR INTEGRATED CIRCUITS

DESCRIPTION

The μA748 is a High Performance Operational Amplifier featuring high gain, short circuit immunity, offset voltage null capability, simplified compensation and excellent temperature stability.

FEATURES

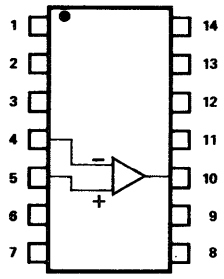
- SHORT CIRCUIT PROTECTION
- OFFSET VOLTAGE NULL CAPABILITY
- LARGE COMMON-MODE AND DIFFERENTIAL VOLTAGE RANGES
- LOW POWER CONSUMPTION
- NO LATCH UP

ABSOLUTE MAXIMUM RATINGS:

Supply Voltage	
μA748	±22V
μA748C	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
μA748	-55°C to +125°C
μA748C	0°C to +70°C
Lead Temperature	300°C
Output Short Circuit Duration (Note 3)	Indefinite

PIN CONFIGURATIONS

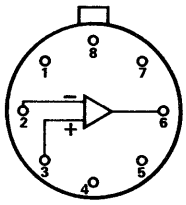
A PACKAGE
(Top View)



ORDER PART NOS.
μA748A/μA748CA

1. NC
2. NC
3. Freq. Comp. A/Offset Null
4. Inverting Input
5. Noninverting Input
6. V^-
7. NC
8. NC
9. Offset Null
10. Output
11. V^+
12. Freq. Comp. B
13. NC
14. NC

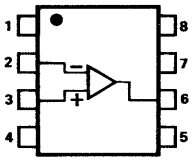
T PACKAGE



ORDER PART NOS.
μA748T/μA748CT

1. Freq. Comp. A/ Offset Null.
2. Inverting Input
3. Noninverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp. B

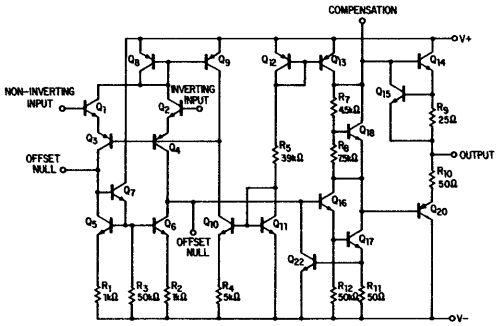
V PACKAGE



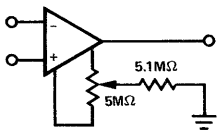
ORDER PART NO.
μA748CV

1. Freq. Comp. A/ Offset Null.
2. Inverting Input
3. Noninverting Input
4. V^-
5. Offset Null
6. Output
7. V^+
8. Freq. Comp. B

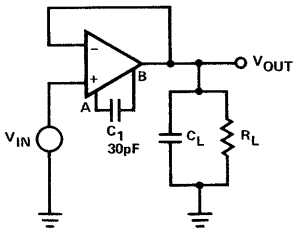
EQUIVALENT CIRCUIT



VOLTAGE OFFSET NULL CIRCUIT



TRANSIENT RESPONSE TEST CIRCUIT



NOTES:

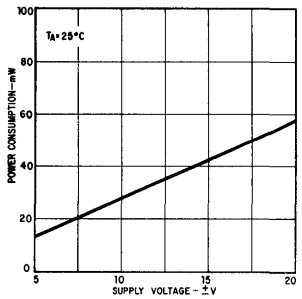
1. Rating applies for case temperatures to +70°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

ELECTRICAL CHARACTERISTICS: (V_S = ±15V, T_A = 25°C unless otherwise specified)

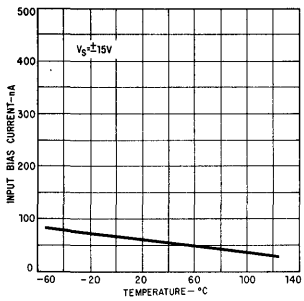
PARAMETER	CONDITIONS	μA748C			μA748			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10\ k\Omega$		2.0	6.0		1.0	5.0	mV
Input Offset Current			20	200		20	200	nA
Input Bias Current			80	500		80	500	nA
Input Resistance		0.3	2.0		0.3	2.0		MΩ
Input Capacitance			1.4			1.4		pF
Offset Voltage Adjustment Range			±15			±15		mV
Input Voltage Range		±12	±13		±12	±13		V
Large-Signal Voltage Gain	$R_L \geq 2\ k\Omega$, $V_{out} = \pm 10V$	50K	200K		50K	200K		
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		30	150		30	150	μV/V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		70	90		dB
Supply Current			1.7	2.8		1.7	2.8	mA
Power Consumption			50	85		50	85	mW
Transient Response (unity gain)	$V_{in} = 20mV$, $R_L = 2\ k\Omega$, $C_L \leq 100\ pF$							
Risetime	$C_1 = 30\ pF$		0.3			0.3		μs
Overshoot			5.0			5.0		%
Slew Rate	$R_L \geq 2\ k\Omega$ $C_1 = 30\ pF$		0.5			0.5		V/μs
The Following Specifications Apply Over the Operating Temperature Ranges								
Input Offset Voltage	$R_S \leq 10\ k\Omega$			7.5			6.0	mV
Input Offset Current	T_A max		9.0	300		7.0	200	nA
	T_A min		35	300		85	500	nA
Input Bias Current	T_A max		0.04	0.8		0.03	0.5	μA
	T_A min		0.13	0.8		0.3	1.5	μA
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		30	150		30	150	μV/V
Large-Signal Voltage Gain	$R_L \geq 2\ k\Omega$, $V_{out} = \pm 10V$	25			25			V/mV
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2\ k\Omega$	±10	±13		±10	±13		V
Supply Current	T_A max		1.6	3.3		1.5	2.5	mA
	T_A min		1.8	3.3		2.0	3.3	mA
Power Consumption	T_A max		48	100		45	75	mW
	T_A min		54	100		60	100	mW

TYPICAL CHARACTERISTIC CURVES

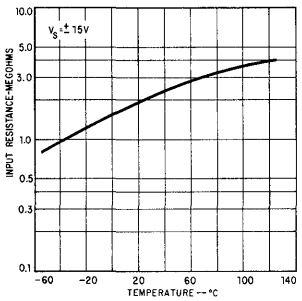
POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE



INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

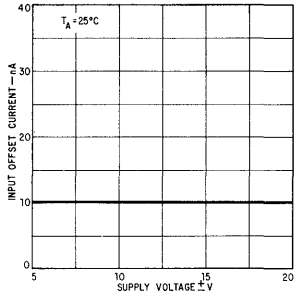


INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

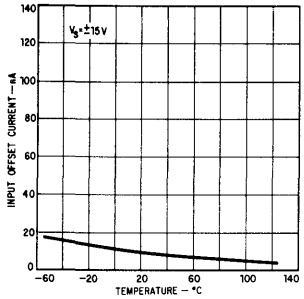


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

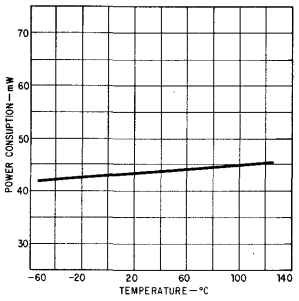
INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



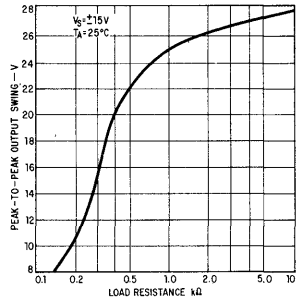
INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



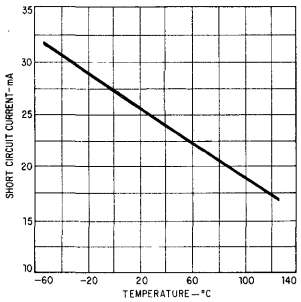
POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE



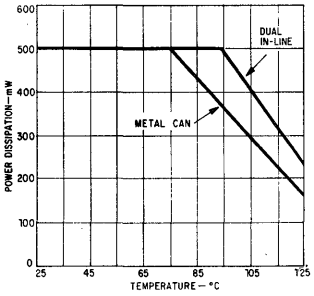
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



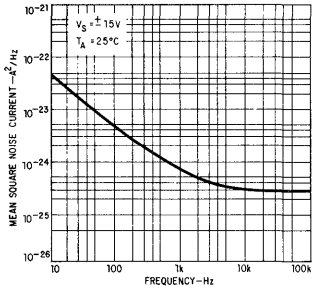
OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE



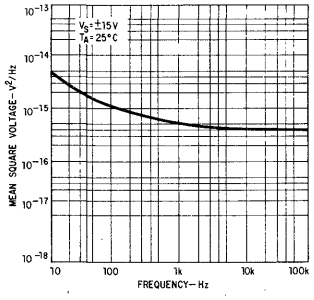
ABSOLUTE MAXIMUM POWER DISSIPATION AS A FUNCTION OF AMBIENT TEMPERATURE



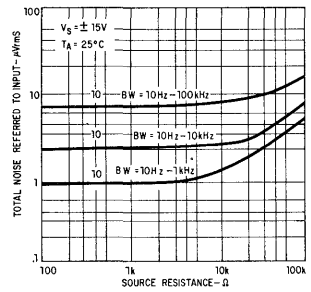
INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY



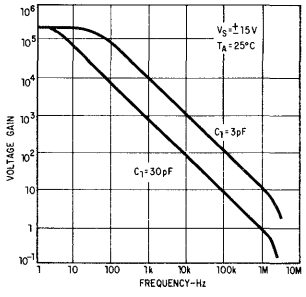
INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY



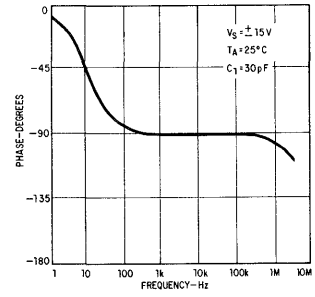
BROADBAND NOISE AS A FUNCTION OF SOURCE RESISTANCE



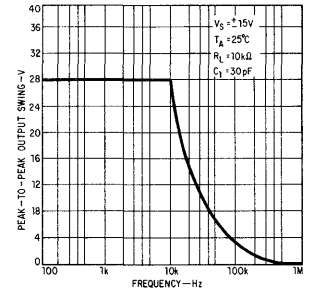
OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY

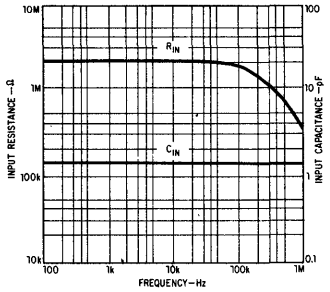


OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

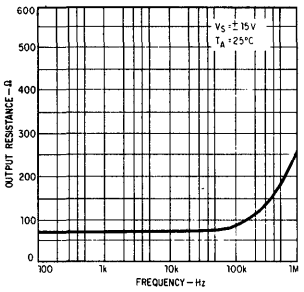


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

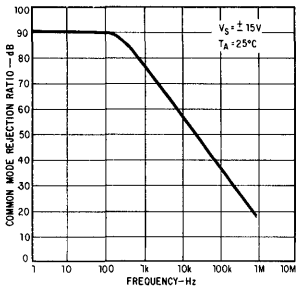
INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY



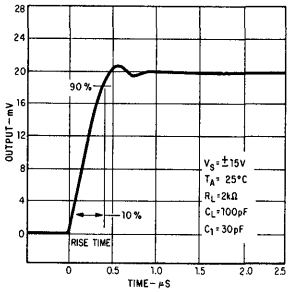
OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY



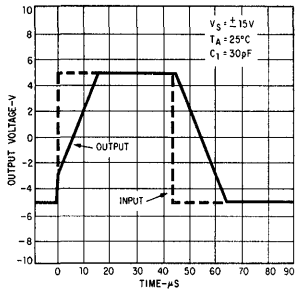
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



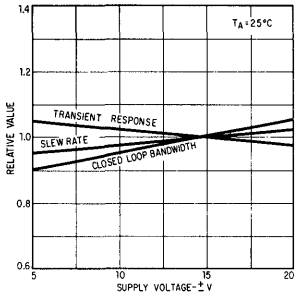
TRANSIENT RESPONSE



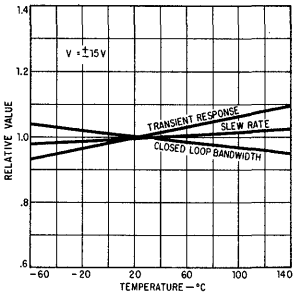
VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE



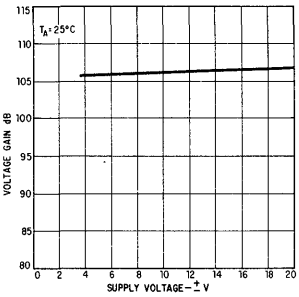
FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE



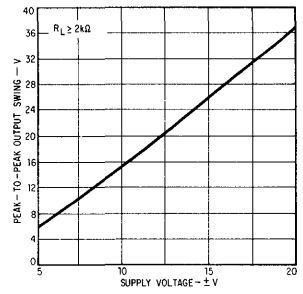
FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE



OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE



SECTION 4
voltage regulators

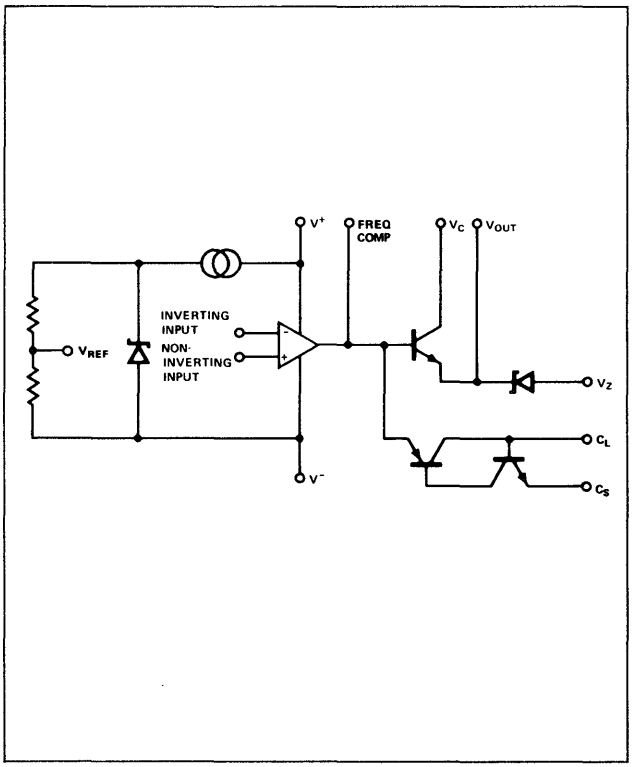
DESCRIPTION

The 550 is a precision monolithic voltage regulator capable of positive or negative supply operation as series, shunt, switching or floating regulator. Guaranteed line regulation is provided for input voltages ranging from 8.5 volts to as high as 50 volts. The output voltage can be continuously adjusted from 2 volts to 40 volts. Foldback current limiting can be accomplished through the use of one external resistor. Internal circuitry permits on and off strobing with DTL and TTL logic inputs and latched shut-down with a pulsed input.

FEATURES:

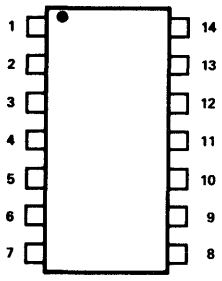
- LINE REGULATION GUARANTEED OVER INPUT VOLTAGE RANGE OF 8.5 VOLTS TO AS HIGH AS 50 VOLTS.
- OUTPUT VOLTAGE CONTINUOUSLY ADJUSTABLE FROM 2 VOLTS TO 40 VOLTS
- LOAD REGULATION 0.1% OF V_{out}
- ADJUSTABLE LIMITING OF SHORT CIRCUIT CURRENT
- FOLDBACK CURRENT LIMITING WITH ONE EXTERNAL RESISTOR
- REMOTE AND LATCHING SHUTDOWN
- OUTPUT CURRENT UP TO 150mA WITHOUT EXTERNAL POWER TRANSISTORS

BASIC CIRCUIT SCHEMATIC



PIN CONFIGURATIONS

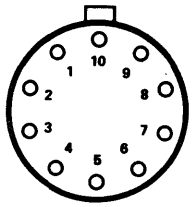
A PACKAGE
(Top View)



1. NC
2. Current Limit
3. Current Sense
4. Inverting Input
5. Noninverting Input
6. V_{REF}
7. V^-
8. NC
9. V_z
10. V_{out}
11. V_C
12. V^+
13. Frequency Compensation
14. NC

ORDER PART NO. NE550A

L PACKAGE



1. Current Sense
2. Inverting Input
3. Noninverting Input
4. V_{REF}
5. V^-
6. V_{out}
7. V_C
8. V^+
9. Frequency Compensation
10. Current Limit

ORDER PART NOS. NE550L/SE550L

ABSOLUTE MAXIMUM RATINGS:

	SE550	NE550
Voltage from V^+ to V^-	50V	40V
Input-Output Voltage Differential	45V	37V
Maximum Output Current	150mA	150mA
Current from V_Z	15mA	15mA
Internal Power Dissipation (Note 1)	800mW	800mW
Operating Temperature Range	-55°C to +125°C	-0°C to 70°C
Storage Temperature Range	-65°C to +150°C	-65°C to +150°C
Lead Temperature	300°C	300°C

NOTE:

1. Rating applies for case temperatures to 125°C; derate linearly at 6.5mW/°C for ambient temperatures above +75°C.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Notes 1 and 2)

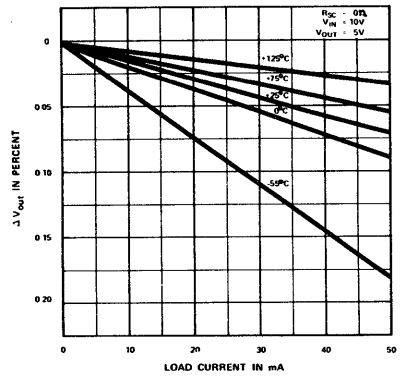
PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
NE550					
Line Regulation		.08	0.3	% V_{out}	V_{in} = 8.5 to 40V
			0.35	% V_{out}	0°C ≤ T_A ≤ 70°C, V_{in} = 12 to 40V
Load Regulation		.03	0.2	% V_{out}	I_L = 1mA to 50mA
			0.4	% V_{out}	0°C ≤ T_A ≤ 70°C, I_L = 1mA to 50mA
Ripple Rejection		75		dB	f = 50 Hz to 10 kHz, CREF = 0
		90		dB	f = 50 Hz to 10 kHz, CREF = 5μF
Average Temperature Coefficient of Output Voltage		.002	.015	%/°C	0°C ≤ T_A ≤ 70°C
Short Circuit Current Limit	50	60	70	mA	RSC = 10Ω, V_{out} = 0
Reference Voltage	1.53	1.63	1.73	V	
Output Noise Voltage		20		μV rms	BW = 100 Hz to 10 kHz, CREF = 0
		2.5		μV rms	BW = 100 Hz to 10 kHz, CREF = 5μF
Long Term Stability		0.1		%/1000 hrs.	
Standby Current Drain		1.6	3.0	mA	I_L = 0, V_{in} = 40V
Input Voltage Range	8.5		40	V	
Output Voltage Range	2.0		37	V	
Input-Output Voltage Differential	3.0		38	V	
SE550					
Line Regulation		0.05	0.1	% V_{out}	V_{in} = 12 to 40V
		0.2	0.6	% V_{out}	V_{in} = 8.5 to 50V
			0.25	% V_{out}	-55°C ≤ T_A ≤ +125°C, V_{in} = 12 to 40V
Load Regulation		0.3	.10	% V_{out}	I_L = 1mA to 50mA
			.6	% V_{out}	-55°C ≤ T_A ≤ +125°C, I_L = mA to 50mA
Ripple Rejection		75		dB	F = 50 Hz to 10 kHz, CREF = 0
		90		dB	F = 50 Hz to 10 kHz, CREF = 5μF
Average Temperature Coefficient of Output Voltage		.002	.012	%/°C	-55°C ≤ T_A ≤ +125°C
Short Circuit Limit	50	60	70	mA	RSC = 10Ω, V_{out} = 0
Reference Voltage	1.58	1.63	1.68	V	
Output Noise Voltage		20		μV rms	BW = 100 Hz to 10 kHz, CREF = 0
		2.5		μV rms	BW = 100 Hz to 10 kHz, CREF = 5μF
Long Term Stability		0.1		%/1000 hrs.	
Standby Current Drain		1.3	2.0	mA	I_L = 0, V_{in} = 50V
Input Voltage Range	8.5		50	V	
Output Voltage Range	2.0		40	V	
Input-Output Voltage Differential	3.0		45	V	

NOTES

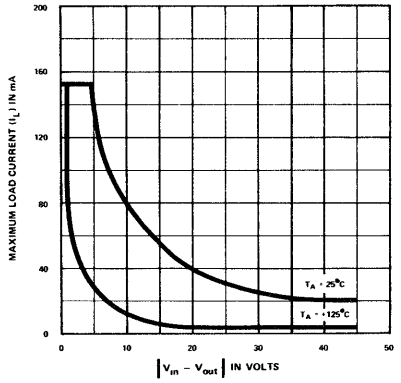
1. Unless otherwise specified, T_A = 25°C, V_{in} = V^+ = V_c = 12V, V^- = 0V, V_{out} = 5V, I_L = 1mA, R_{sc} = 0, C_1 = 100pF, and divider impedance as seen by error amplifier ≃ 2kΩ when connected as shown in Figure 1.
2. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high or varying dissipation.

TYPICAL CHARACTERISTIC CURVES

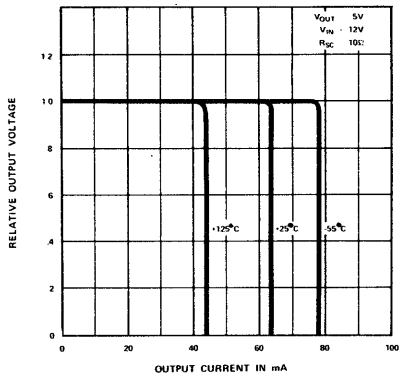
LOAD REGULATION AS A FUNCTION OF LOAD CURRENT



MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

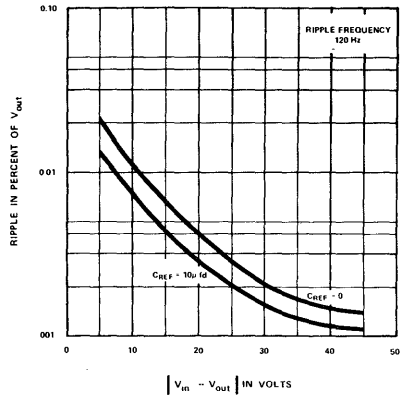


RELATIVE OUTPUT VOLTAGE AS A FUNCTION OF LIMITED OUTPUT CURRENT

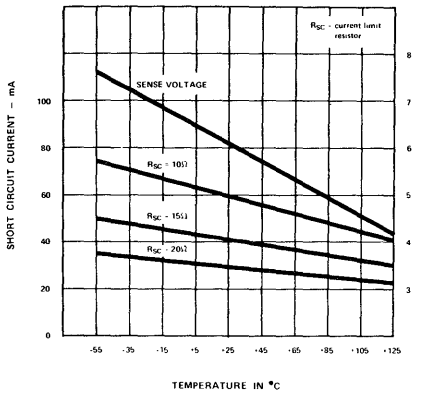


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

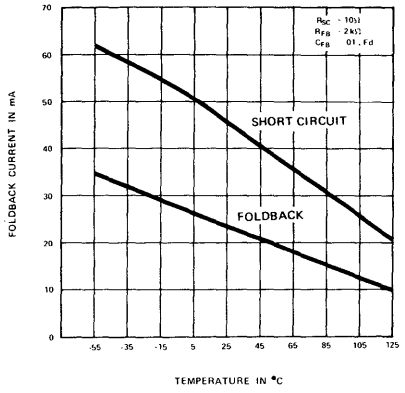
RIPPLE REJECTION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



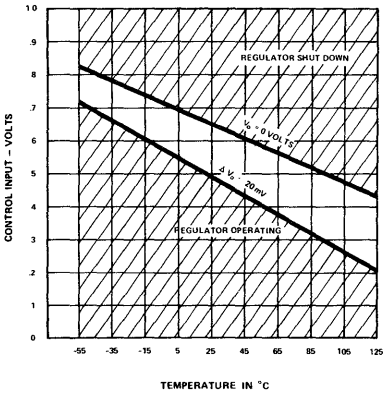
SENSE VOLTAGE AND SHORT CIRCUIT CURRENT LIMIT AS A FUNCTION OF TEMPERATURE



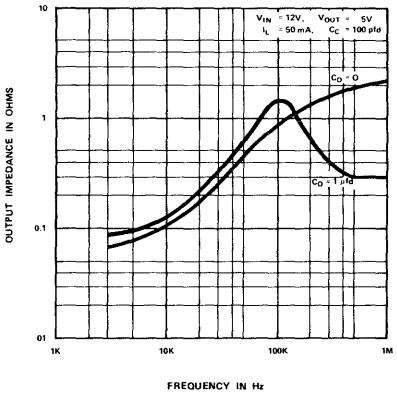
SHORT CIRCUIT FOLDBACK CURRENT AS A FUNCTION OF TEMPERATURE



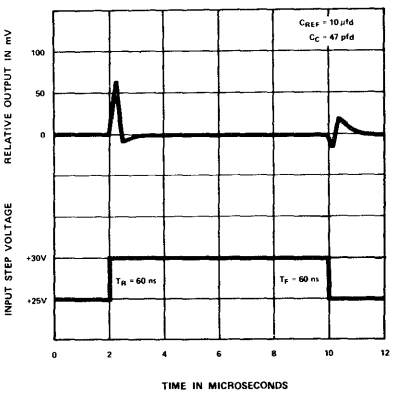
REMOTE CONTROL CHARACTERISTICS AS A FUNCTION OF TEMPERATURE



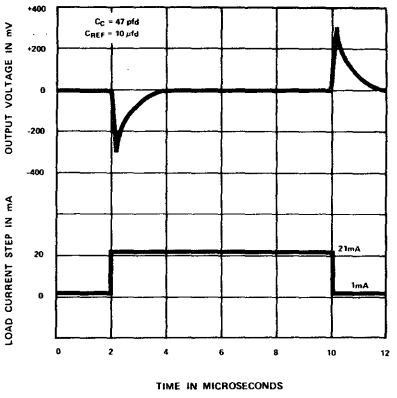
OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY



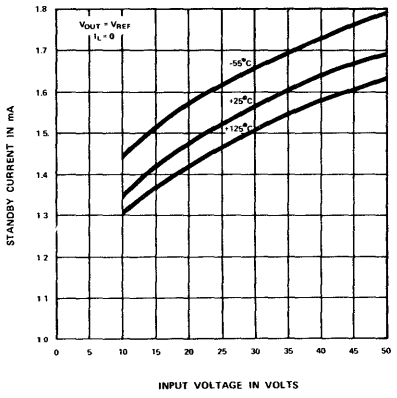
LINE TRANSIENT RESPONSE



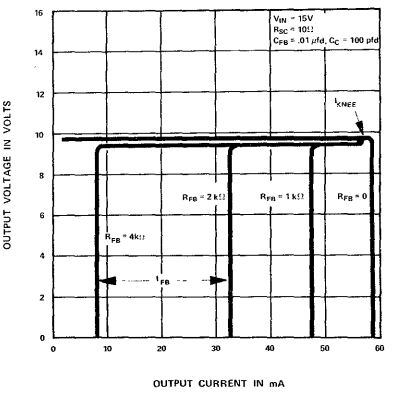
LOAD TRANSIENT RESPONSE



STANDBY CURRENT AS A FUNCTION OF INPUT VOLTAGE

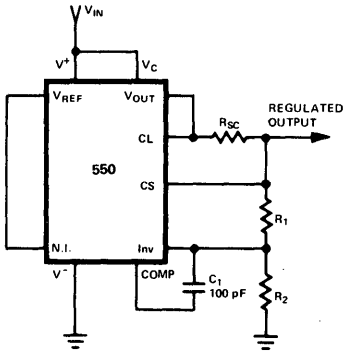


FOLDBACK CURRENT LIMITED OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



TYPICAL APPLICATIONS

BASIC POSITIVE VOLTAGE REGULATOR

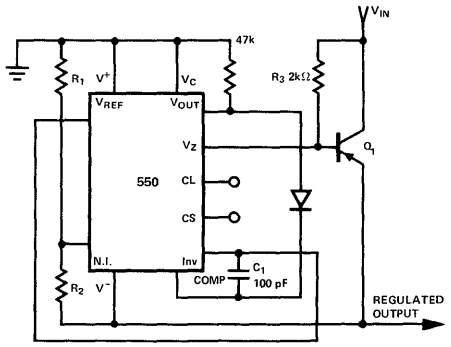


$$V_{out} = V_{REF}\ \frac{R_1 + R_2}{R_2}$$

$\frac{R_1\ R_2}{R_1 + R_2} = 2k\Omega$ for minimum temperature drift

FIGURE 1

NEGATIVE VOLTAGE REGULATOR



$$V_{out} = -V_{REF} \times \frac{R_1 + R_2}{R_2}$$

$\frac{R_1\ R_2}{R_1 + R_2} = 2k\Omega$ for minimum temperature drift

NOTE 1

FIGURE 2

POSITIVE VOLTAGE REGULATOR (External PNP Pass Transistor)

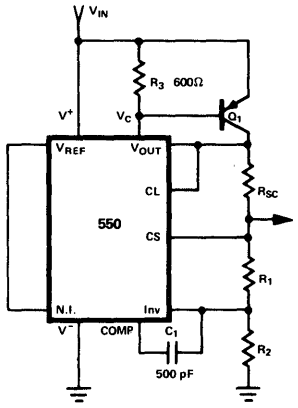


FIGURE 3

POSITIVE VOLTAGE REGULATOR (External NPN Pass Transistor)

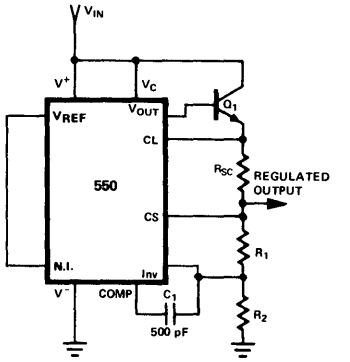
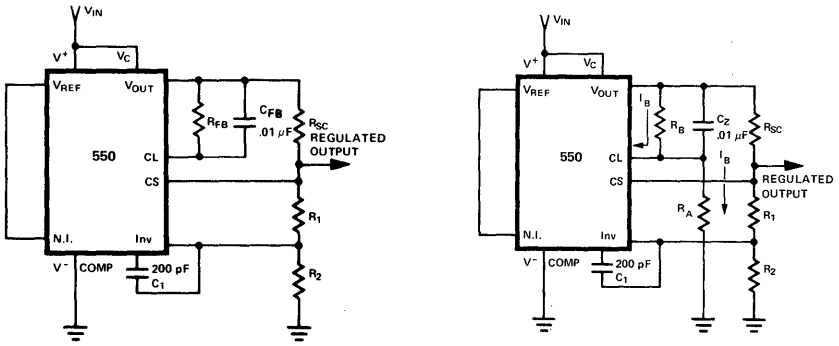


FIGURE 4.

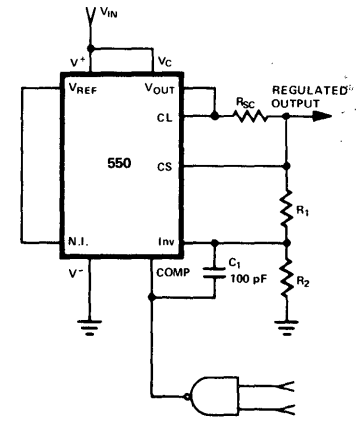
FOLDBACK CURRENT LIMITED OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT



$$I_{SC} = \frac{V_{SENSE}}{R_{SC}} \qquad R_A = \frac{I_{FL}\ R_{SC} - V_{SENSE}}{I_{BLEED}} \qquad R_B = \frac{V_{OUT} + V_{SENSE}}{I_B + I_{BIAS}}$$

FIGURE 5.

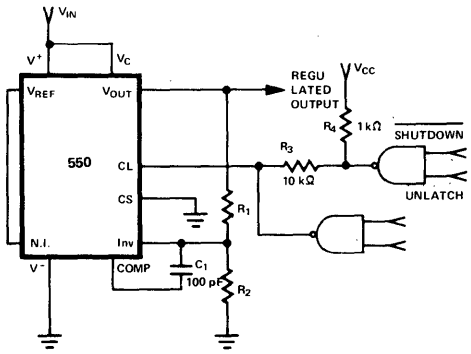
REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING



1/4 8T80, 1/6 8T90, 1/10 8T01B, etc.

FIGURE 6

REMOTE LATCHING SHUTDOWN REGULATOR

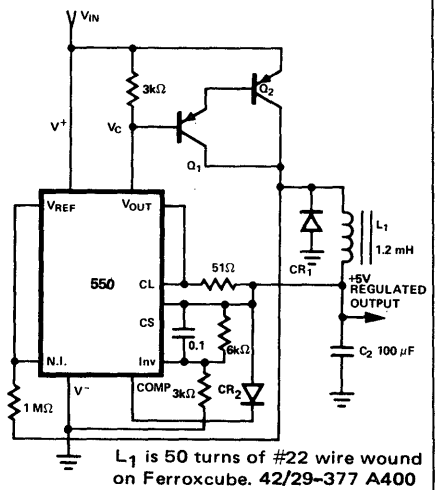


8415, 8417, 2/3 8471, 1/3 8891, 8T90, 1/2 8481, 8881, 8T90

NOTE 2

FIGURE 7

POSITIVE SWITCHING REGULATOR



L_1 is 50 turns of #22 wire wound on Ferroxcube. 42/29-377 A400

FIGURE 8

TYPICAL APPLICATIONS (Cont'd.)

POSITIVE FLOATING REGULATOR

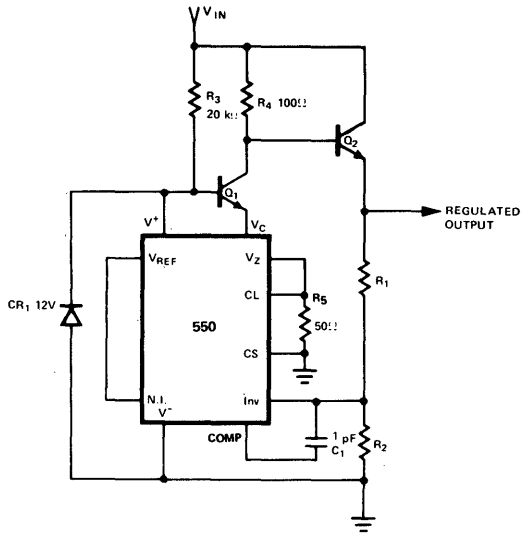


FIGURE 9

NEGATIVE FLOATING REGULATOR

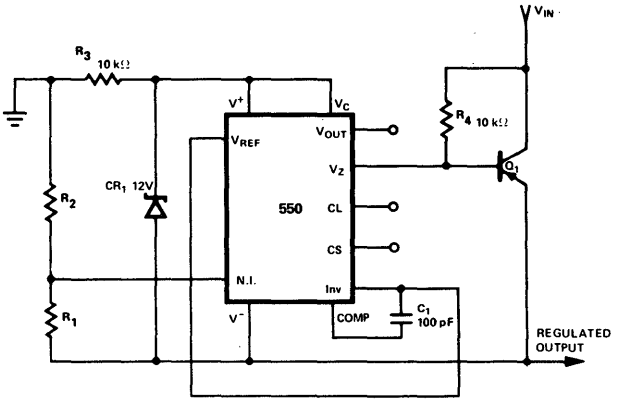
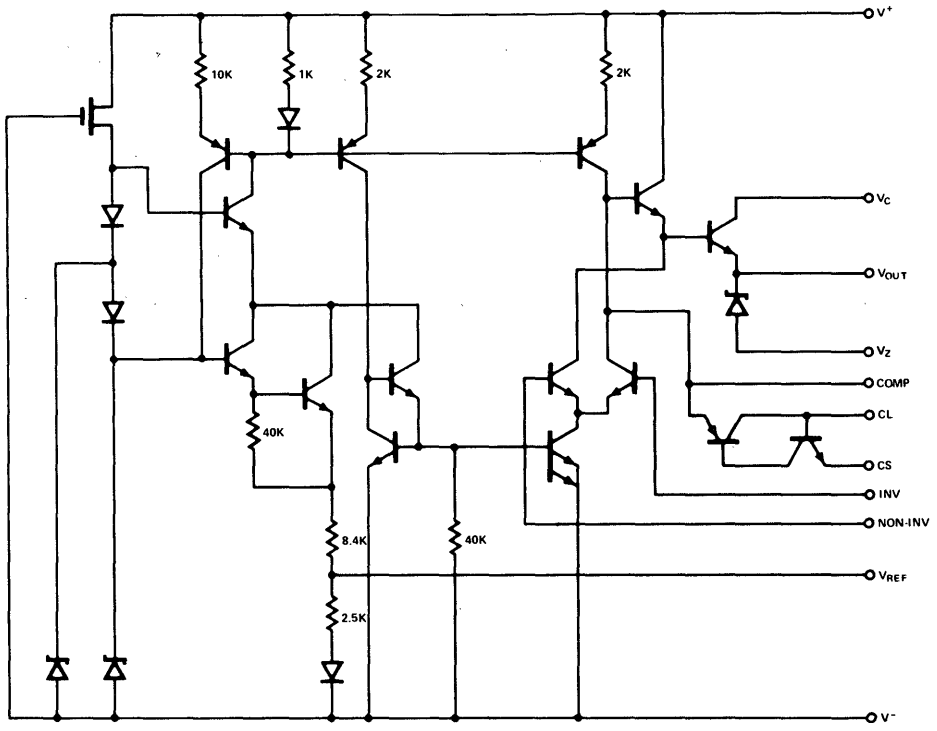


FIGURE 10

NOTES:

1. To utilize the SE550L in applications which require V_Z, an external 6.2 volt zener diode should be connected in series with V_{OUT}.
2. The "Shut-down" gate need only be pulsed to latch the regulator output to zero. R_4 may be omitted for active pull-up devices. The "Unlatch" gate must have an open collector.

EQUIVALENT CIRCUIT



DESCRIPTION

The LM109 and LM309 are complete 5 volt regulators fabricated on a single silicon chip. These regulators are designed for local "on card" regulation to eliminate many of the noise and ground loop problems associated with single-point regulation. They employ internal current limiting, thermal shutdown, and safe-area compensation which makes the circuitry essentially blow-out proof. If adequate heat sinking is provided, the devices can deliver output currents in excess of 200mA from the TO-5 package, and 1A from the TO-3 package. In addition to their use as fixed 5 volt regulators, these devices may be used with external components to obtain adjustable output levels. They may also be used as the power pass element in precision regulators.

FEATURES

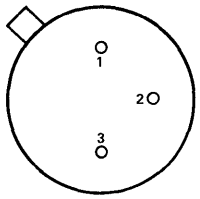
- **OUTPUT CURRENTS IN EXCESS OF 1 amp**
- **INTERNAL THERMAL OVERLOAD PROTECTION**
- **INTERNAL CURRENT LIMITING**
- **NO EXTERNAL COMPONENTS REQUIRED**

ABSOLUTE MAXIMUM RATINGS

Input Voltage	35V
Power Dissipation	Internally Limited
Operating Junction Temperature Range	
LM109	-55°C to 150°C
LM309	0°C to 125°C
Storage Temperature Range	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PIN CONFIGURATIONS

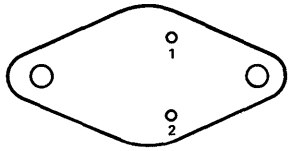
H PACKAGE
(Top View)



1. Input
2. Output
3. Ground

ORDER PART NOS. LM109H/LM309H

K PACKAGE

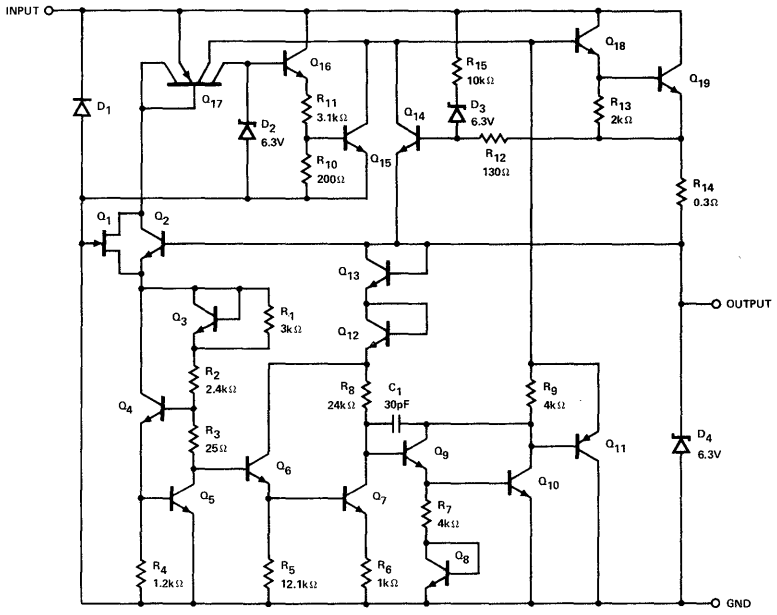


1. Input
2. Output

Case is connected to ground.

ORDER PART NOS. LM109K/LM309K

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS (Note 1)

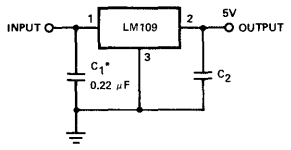
PARAMETER	CONDITIONS	LM109			LM309			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Output Voltage	$T_j = 25°C$	4.7	5.05	5.3	4.8	5.05	5.2	V
Line Regulation	$T_j = 25°C$							
	$7V \leqslant V_{IN} \leqslant 25V$		4	50		4	50	mV
Load Regulation	$T_j = 25°C$							
TO-5	$5mA \leqslant I_{OUT} \leqslant 0.5A$		20	50		20	50	mV
TO-3	$5mA \leqslant I_{OUT} \leqslant 1.5A$		50	100		50	100	mV
Output Voltage	$7V \leqslant V_{IN} \leqslant 25V$							
	$5mA \leqslant I_{OUT} \leqslant I_{max}$							
	$P < P_{max}$	4.6		5.4	4.75		5.25	V
Quiescent Current	$7V \leqslant V_{IN} \leqslant 25V$		5.2	10		5.2	10	mA
Quiescent Current Change	$7V \leqslant V_{IN} \leqslant 25V$			0.5			0.5	mA
	$5mA \leqslant I_{OUT} \leqslant I_{max}$			0.8			0.8	mA
Output Noise Voltage	$T_A = 25°C$							
	$10Hz \leqslant f \leqslant 100$ kHz		40			40		μV
Long Term Stability				10			20	mV
Thermal Resistance								
Junction to Case (Note 2)								
TO-5			15			15		°C/W
TO-3			3			3		°C/W

NOTES:

1. Unless otherwise specified, these specifications apply for $-55°C \leqslant T_j \leqslant 150°C$ for the 5109 or $0°C \leqslant T_j \leqslant 125°C$ for the 5309, V_{IN} = 10V and I_{OUT} = 0.1A for the TO-5 package or I_{OUT} = 0.5A for the TO-3 package. For the TO-5 package, I_{max} = 0.2A and P_{max} = 2.0W. For the TO-3 package, I_{max} = 1.0A and P_{max} = 20W.
2. Without a heat sink, the thermal resistance of the TO-5 package is about 150°C/W, while that of the TO-3 package is approximately 35°C/W. With a heat sink, the effective thermal resistance can only approach the values specified, depending on the efficiency of the sink.

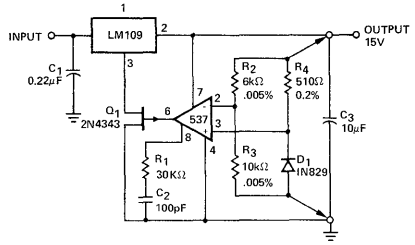
TYPICAL APPLICATIONS

FIXED 5V REGULATOR



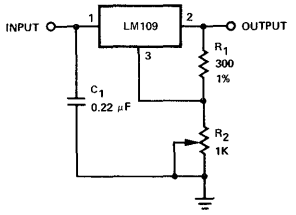
NOTES: *Required if regulator is located an appreciable distance from power supply filter.
†Although no output capacitor is needed for stability, it does improve transient response.

PRECISION VOLTAGE REGULATOR

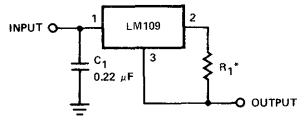


NOTES: *Regulation better than 0.01% load, line and temperature, can be obtained.
†Determines zener current. May be adjusted to minimize thermal drift.
‡Solid tantalum.

ADJUSTABLE OUTPUT REGULATOR



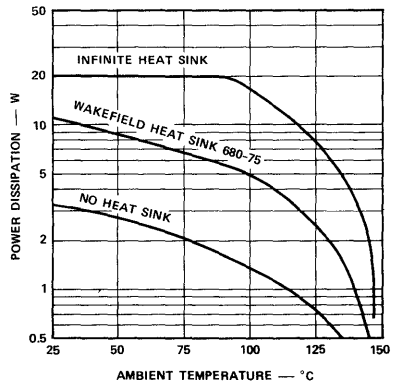
CURRENT REGULATOR



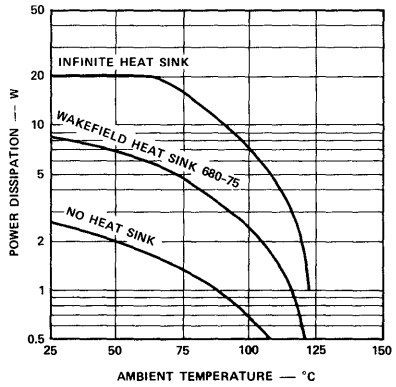
NOTES: *Determines output current.

TYPICAL CHARACTERISTIC CURVES

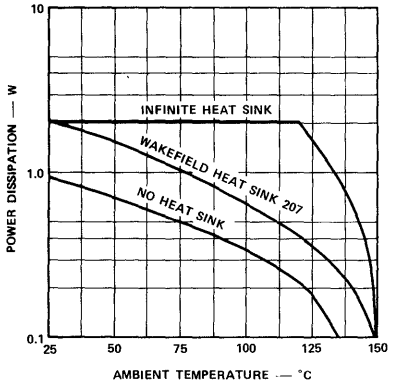
MAXIMUM AVERAGE POWER DISSIPATION LM109 (TO-3)



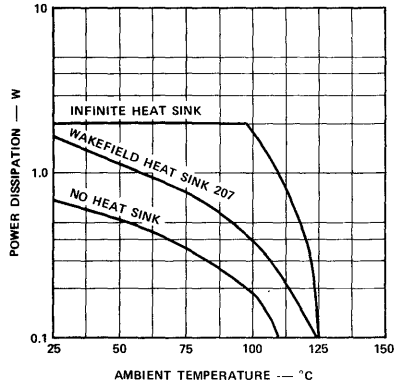
MAXIMUM AVERAGE POWER DISSIPATION LM309 (TO-3)



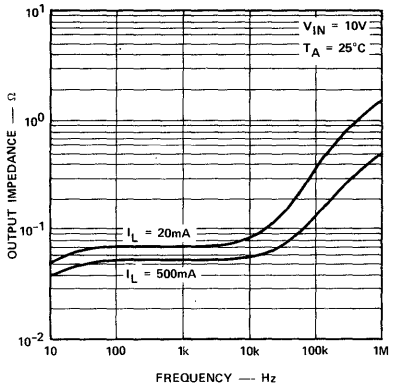
MAXIMUM AVERAGE POWER DISSIPATION LM109 (TO-5)



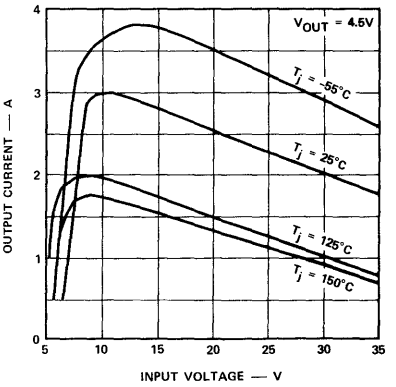
MAXIMUM AVERAGE POWER DISSIPATION LM309 (TO-5)



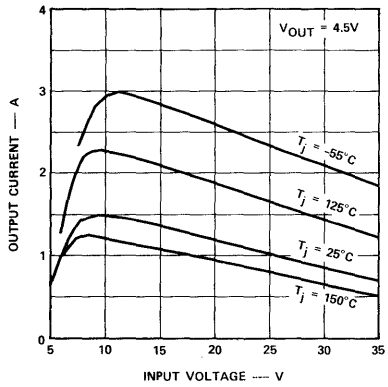
OUTPUT IMPEDANCE



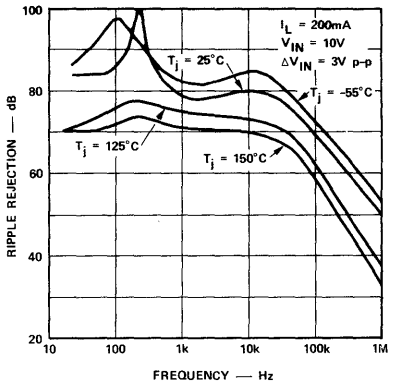
PEAK OUTPUT CURRENT K PACKAGE (TO-3)



PEAK OUTPUT CURRENT H PACKAGE (TO-5)

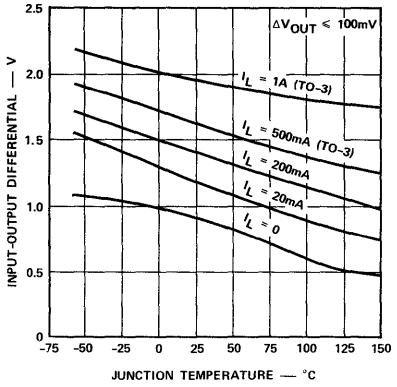


RIPPLE REJECTION

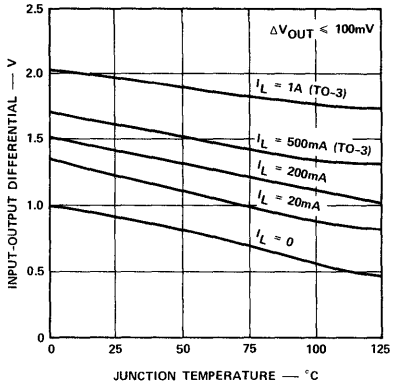


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

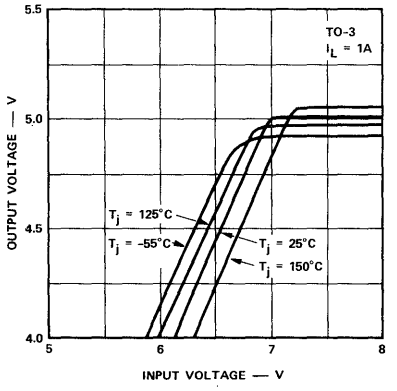
DROPOUT VOLTAGE



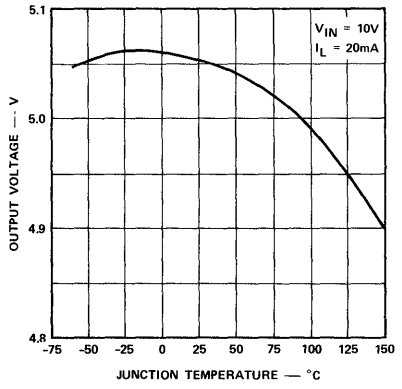
DROPOUT VOLTAGE



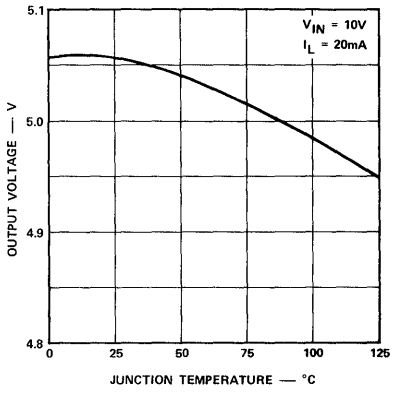
DROPOUT CHARACTERISTIC



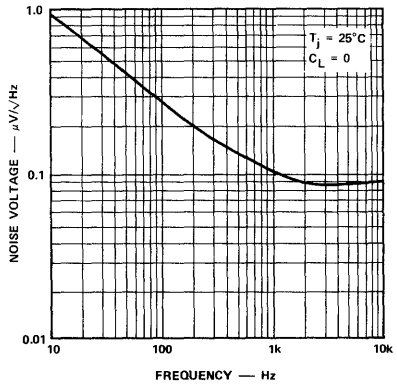
OUTPUT VOLTAGE



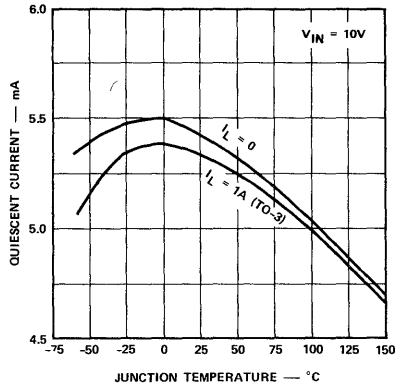
OUTPUT VOLTAGE



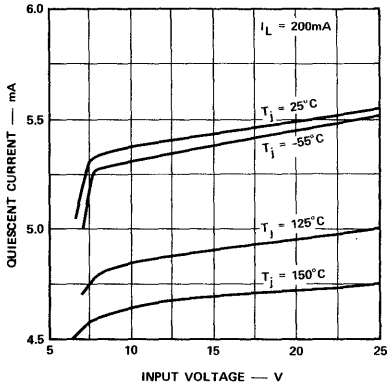
OUTPUT NOISE VOLTAGE



QUIESCENT CURRENT



QUIESCENT CURRENT



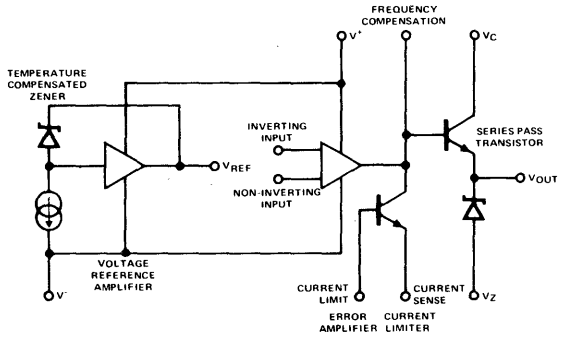
DESCRIPTION

The μA723 is a Monolithic Precision Voltage Regulator capable of operation in positive or negative supplies as a series, shunt, switching or floating regulator. The μA723 contains a temperature compensated reference amplifier, error amplifier, series pass transistor, and current limiter, with access to remote shutdown.

FEATURES

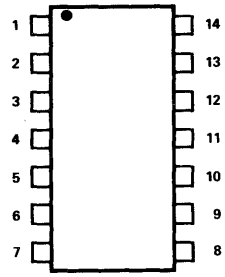
- POSITIVE OR NEGATIVE SUPPLY OPERATION
- SERIES, SHUNT, SWITCHING OR FLOATING OPERATION
- .01% LINE AND LOAD REGULATION
- OUTPUT VOLTAGE ADJUSTABLE FROM 2 TO 37 VOLTS
- OUTPUT CURRENT TO 150mA WITHOUT EXTERNAL PASS TRANSISTOR

EQUIVALENT CIRCUIT



PIN CONFIGURATION

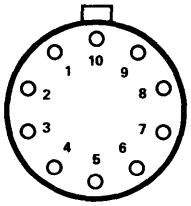
A PACKAGE
(Top View)



1. NC
2. Current Limit
3. Current Sense
4. Inverting Input
5. Noninverting Input
6. V_{REF}
7. V^-
8. NC
9. V_z
10. V_{out}
11. V_c
12. V^+
13. Frequency Compensation
14. NC

ORDER PART NOS. μA723A/μA723CA

L PACKAGE



1. Current Sense
2. Inverting Input
3. Noninverting Input
4. V_{REF}
5. V^-
6. V_{out}
7. V_c
8. V^+
9. Frequency Compensation
10. Current Limit

ORDER PART NOS. μA723L/μA723CL

ABSOLUTE MAXIMUM RATINGS

	μA723	μA723C
Pulse Voltage from V^+ to V^- (50ms)	50V	
Continuous Voltage from V^+ to V^-	40V	40V
Input-Output Voltage Differential	40V	40V
Maximum Output Current	150mA	150mA
Current from V_{REF}	15mA	
Current from V_z		25mA
Internal Power Dissipation (Note 1)	800mW	800mW
Operating Temperature Range	−55 to +125°C	0 to 70°C
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature	300°C	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified – Note 1)

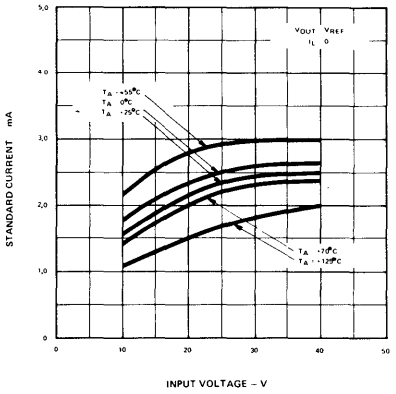
PARAMETER (See definitions)	MIN	TYP	MAX	UNITS	CONDITIONS
μA723C					
Line Regulation (Note 2)		0.01	0.1	% V_{out}	V_{in} = 12V to V_{in} = 15V
		0.1	0.5	% V_{out}	V_{in} = 12V to V_{in} = 40V
Load Regulation (Note 2)		0.03	0.2	% V_{out}	I_L = 1mA to I_L = 50mA
Ripple Rejection		74		dB	f = 50 Hz to 10 kHz, C_{REF} = 0
		86		dB	f = 50 Hz to 10 kHz, C_{REF} = 5μF
Short Circuit Current Limit		65		mA	R_{sc} = 10Ω, V_{out} = 0
Reference Voltage	6.80	7.15	7.50	V	
Output Noise Voltage		20		μV rms	BW = 100 Hz to 10 kHz, C_{REF} = 0
		2.5		μV rms	BW = 100 Hz to 10 kHz, C_{REF} = 5μF
Long Term Stability			0.1	%/1000 hrs.	
Standby Current Drain		2.3	4.0	mA	I_L = 0, V_{in} = 30V
Input Voltage Range	9.5		40	V	
Output Voltage Range	2.0		37	V	
Input-Output Voltage Differential	3.0		38	V	
The Following Specifications Apply Over the Operating Temperature Ranges					
Line Regulation			0.3	% V_{out}	
Load Regulation			0.6	% V_{out}	
Average Temperature Coefficient of Output Voltage		0.003	0.015	%/°C	V_{in} = 12V to V_{in} = 15V, I_L = 1mA to I_L = 50mA
μA723					
Line Regulation (Note 2)		0.01	0.1	%V_{out}	V_{in} = 12V to V_{in} = 15V
		0.02	0.2	%V_{out}	V_{in} = 12V to V_{in} =40V
Load Regulation (Note 2)		0.03	0.15	%V_{out}	I_L = 1mA to I_L = 50mA
Ripple Rejection		74		dB	f = 50 Hz to 10 kHz, C_{REF} = 0
		86		dB	f = 50 Hz to 10 kHz, C_{REF} = 5μF
Short Circuit Current Limit		65		mA	R_{SC} = 10Ω, V_{out} = 0
Reference Voltage	6.95	7.15	7.35	V	
Output Noise Voltage		20		μV rms	BW = 100 Hz to 10 kHz, C_{REF} = 0
		2.5		μV rms	BW = 100 Hz to 10 kHz, C_{REF} = 5μF
Long Term Stability		0.1		%/1000 hrs	
Standby Current Drain		2.3	3.5	mA	I_L = 0, V_{in} = 30V
Input Voltage Range	9.5		40	V	
Output Voltage Range	2.0		37	V	
Input-Output Voltage Differential	3.0		38	V	
The Following Specifications Apply Over the Operating Temperature Ranges					
Line Regulation			0.3	% V_{out}	
Load Regulation			0.6	% V_{out}	
Average Temperature Coefficient of Output Voltage		0.002	0.015	%/°C	V_{in} = 12V to V_{in} = 15V, I_L = 1mA to I_L = 50mA

NOTES

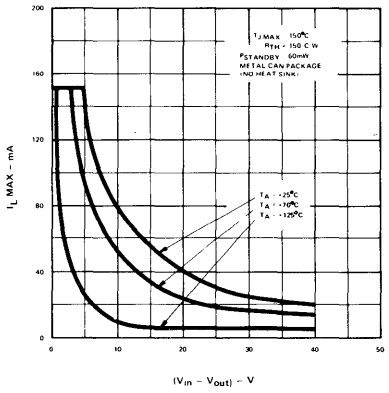
1. Unless otherwise specified, T_A = 25°C, V_{in} = V+ = V_c = 12V, V– = 0V, V_{out} = 5V, I_L = 1mA, R_{sc} = 0, C_1 = 100pF, C_{REF} = 0 and divider impedance as seen by error amplifier ≤ 10kΩ when connected as shown in Figure 3.
2. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

TYPICAL CHARACTERISTIC CURVES

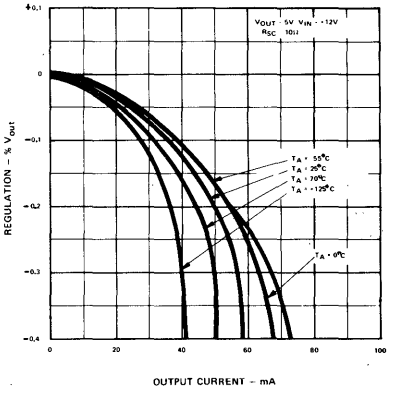
STANDBY CURRENT DRAIN AS A FUNCTION OF INPUT VOLTAGE



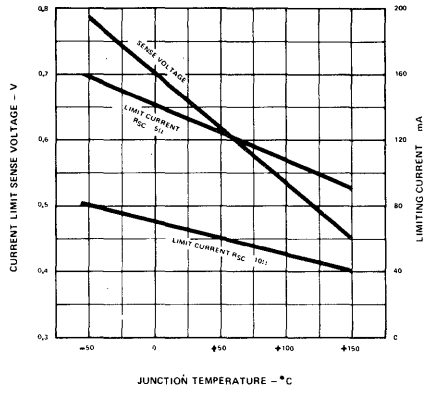
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



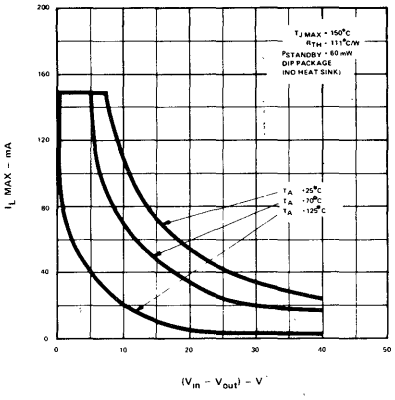
LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING



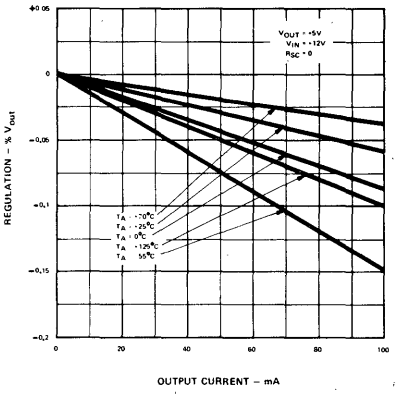
CURRENT LIMITING CHARACTERISTICS AS A FUNCTION OF JUNCTION TEMPEATURE



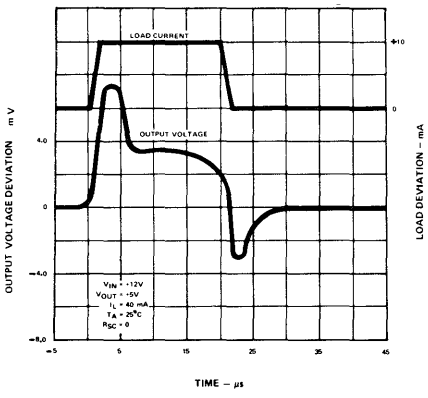
MAXIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL



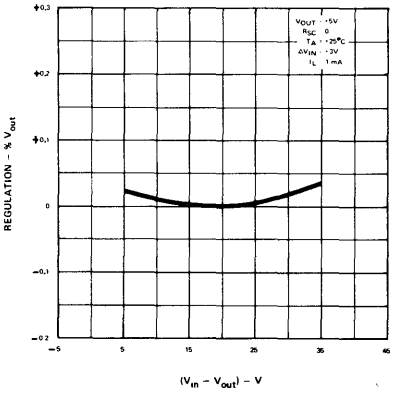
LOAD REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING



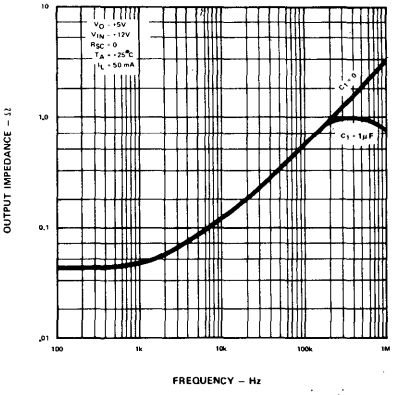
LOAD TRANSIENT RESPONSE



LINE REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

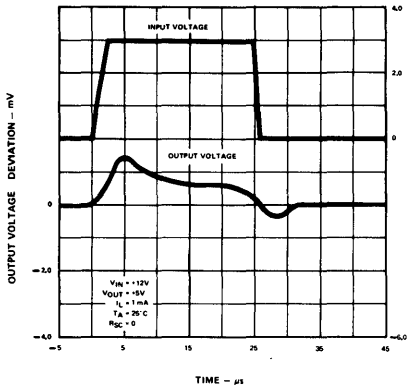


OUTPUT IMPEDANCE AS A FUNCTION OF FREQUENCY

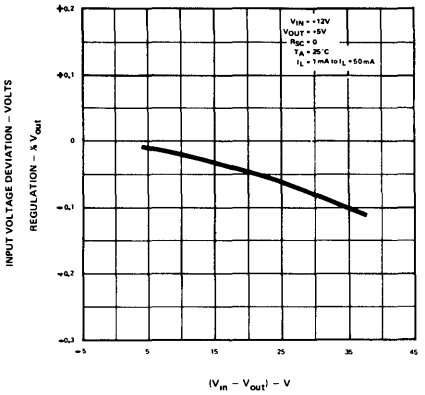


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

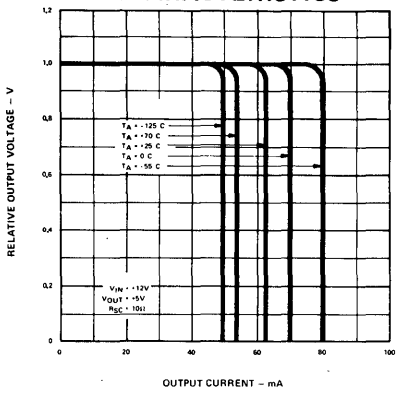
LINE TRANSIENT RESPONSE



LOAD REGULATION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

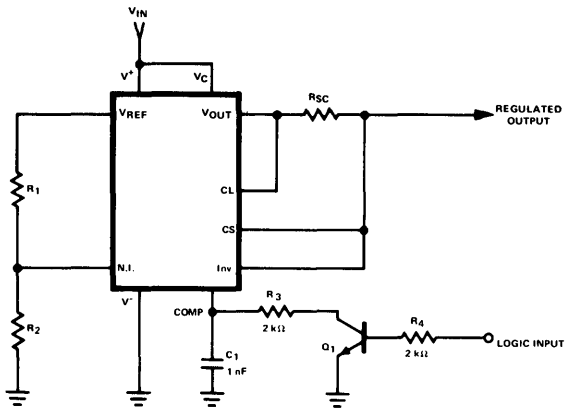


CURRENT LIMITING CHARACTERISTICS



BASIC μA723 REGULATOR APPLICATIONS

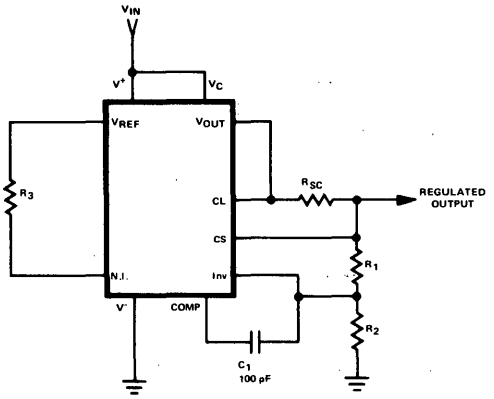
REMOTE SHUTDOWN REGULATOR WITH CURRENT LIMITING (V_{out} = 2 to 7 Volts)



$$V_{out} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2} \right]$$

FIGURE 1

HIGH VOLTAGE REGULATOR (V_{out} = 7 to 37 Volts)



$$V_{out} = \left[V_{REF} \times \frac{R_1 + R_2}{R_2} \right]$$

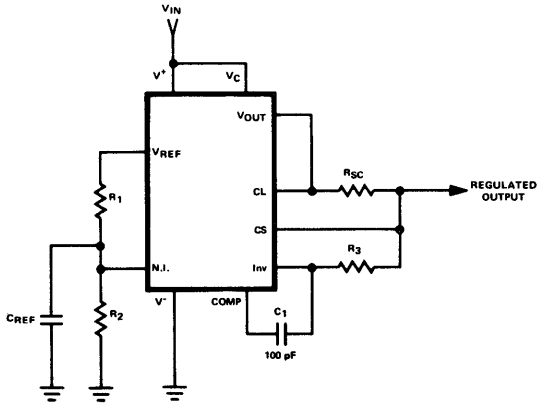
$$R_3 = \frac{R_1 R_2}{R_1 + R_2}$$ for minimum temperature drift

R_3 may be eliminated for minimum component count

FIGURE 2

BASIC μA723 REGULATOR APPLICATIONS (Cont'd.)

LOW VOLTAGE REGULATOR
(V_{out} = 2 to 7 Volts)

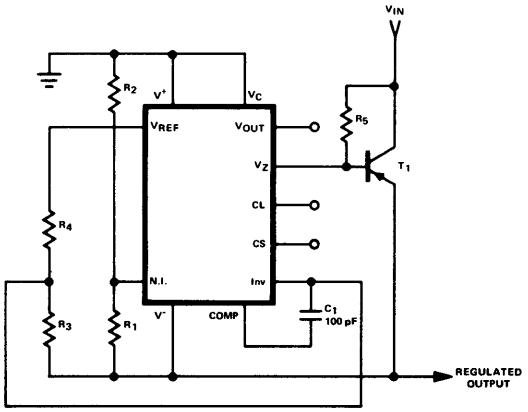


$$V_{out} = \left[V_{REF} \times \frac{R_2}{R_1 + R_2}\right]$$

$$R_3 = \frac{R_1 R_2}{R_2 + R_2} \quad \text{for minimum temperature drift}$$

FIGURE 3

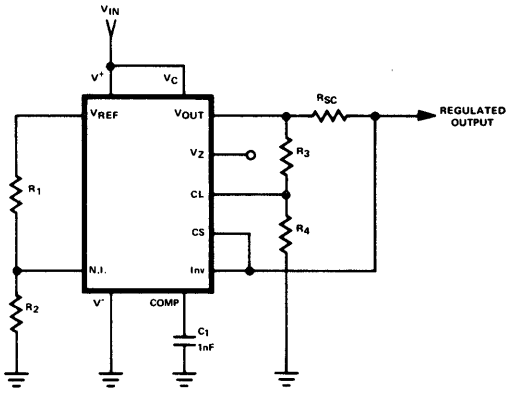
NEGATIVE VOLTAGE REGULATOR

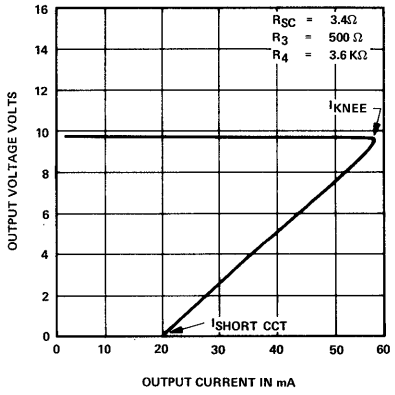


$$V_{out} = \left[\frac{V_{REF}}{2} \times \frac{R_1 + R_2}{R_1}\right] \quad ; \; R_3 = R_4$$

FIGURE 4

FOLDBACK CURRENT LIMITING REGULATOR
(V_{out} = 2 to 7 Volts)





$$I_{KNEE} = \left[\frac{V_{out} R_3}{R_{sc} R_4} + \frac{V_{SENSE}(R_3 + R_4)}{R_{sc} R_4}\right]$$

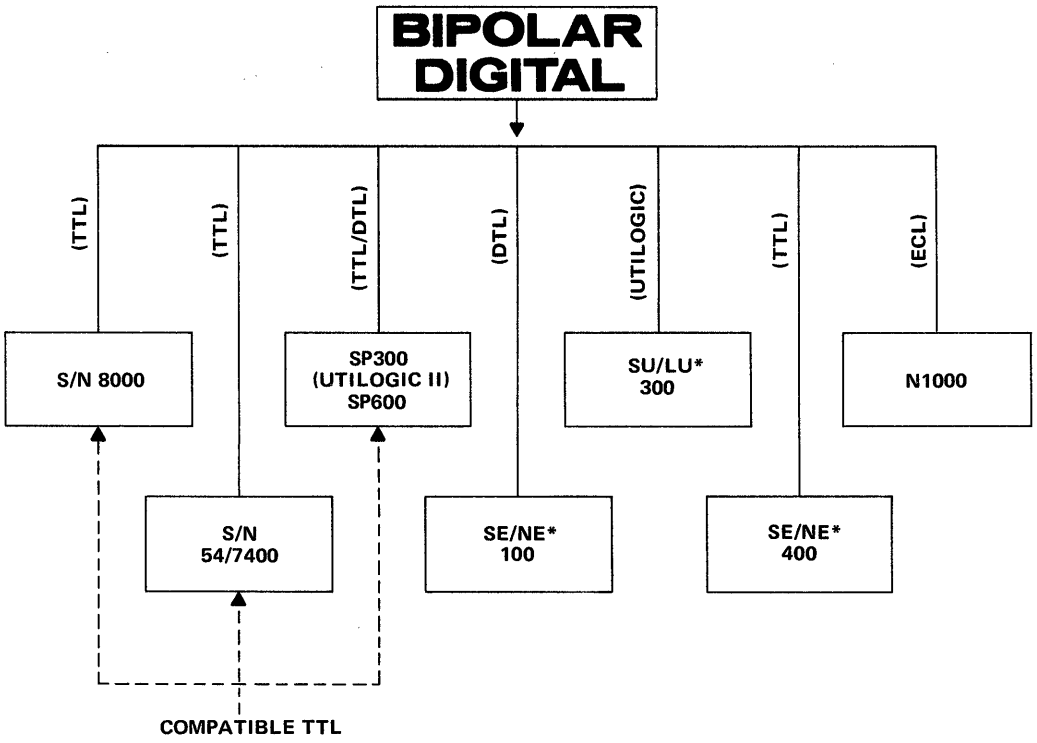
$$V_{out} = \left[V_{REF} \times \frac{R_1 + R_2}{R_2}\right]$$

$$I_{SHORT\ CKT} = \left[\frac{V_{SENSE}}{R_{sc}} \times \frac{R_3 + R_4}{R_4}\right]$$

$$\frac{R_4}{R_3} = \frac{V_{OUT}\, I_{SC}}{V_{SENSE}(I_{KVEE}\, I_{SHORTCCT})} - 1$$

$$R_{SC} = \frac{V_{SENSE}}{I_{SC}}\left[1 + \frac{R_3}{R_4}\right]$$

FIGURE 5



*NOTE: Information pertaining to these Signetics series product lines may be obtained by contacting your local sales representative.

8000 SERIES

The concept of cross-family compatibility in integrated circuits was born in 1966 when Signetics introduced Designer's Choice Logic (DCL). This family consists of the following compatible sub-families:

8100	Special purpose sub-systems.
8200	Integrated monolithic sub-systems (MSI).
8400	Offers DTL logic flexibility at lower power consumption and higher fan-out than any other DTL family.
8800	The classical high level TTL circuit design is utilized to provide low propagation delays and high noise immunity.
8H00	A higher speed version of the 8800.
8T00	A group of interface elements which includes voltage level translators, line drivers and receivers, and Display (Nixie* and Seven Segment) Drivers.

8000 series devices are available in military and commercial temperature ranges and a wide variety of package types.

SECTION 5
comparators and sense amplifiers

DESCRIPTION

The Signetics 518 is a medium-gain, high frequency differential amplifier fabricated within a monolithic silicon substrate by planar and epitaxial techniques. It is designed for voltage comparator, sense amplifier and general broadband amplifier applications. Its superior current sinking and current sourcing capabilities make it ideal for driving digital circuitry.

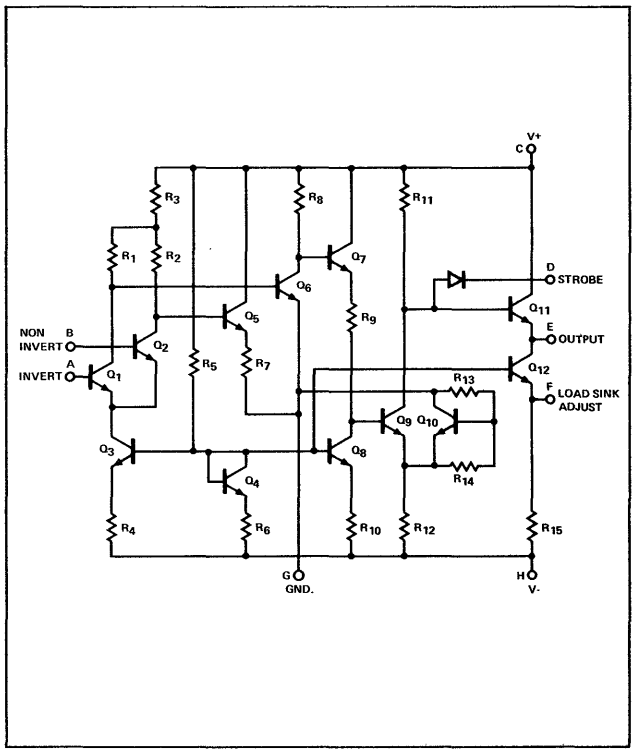
FEATURES

- **STROBE CONTROL**
- **ADJUSTABLE CURRENT SINK**
- **RESPONSE TIME = NE 60ns**
  SE 55ns
- **INPUT OFFSET VOLTAGE = 1.0mV**
- **OPEN LOOP GAIN = NE 1800**
  SE 2100
- **OUTPUT IMPEDANCE = 50Ω**
- **BANDWIDTH = 5.0mHz**

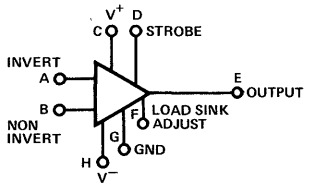
ABSOLUTE MAXIMUM RATINGS

Voltage Applied (Positive)	+8.0V
Voltage Applied (Negative)	-4.0V
Voltage Applied (Input)	±5.0V
Power Consumption	300mW
Power Supply Current Rating	-25mA
Output Source Current	20mA
Storage Temperature	-65°C to +150°C
Operating Temperature	NE 0°C to +70°C
	SE -55°C to +125°C

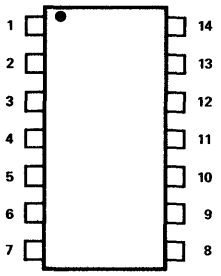
CIRCUIT SCHEMATIC



PIN CONFIGURATIONS



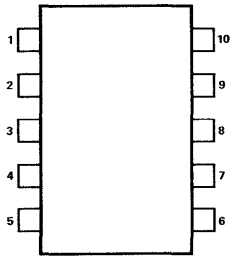
A PACKAGE
(Top View)



1. NC
2. NC
3. Ground
4. Invert
5. Non Invert
6. NC
7. V^-
8. NC
9. NC
10. Load Sink Adjust
11. Output
12. Strobe
13. NC
14. V^+

ORDER PART NOS.
SE518A/NE518A

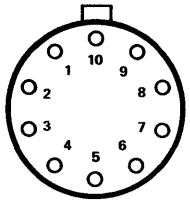
G PACKAGE



1. V^-
2. NC
3. Load Sink Adjust
4. Output
5. Strobe
6. V^+
7. Ground
8. Invert
9. Non Invert
10. NC

ORDER PART NOS. SE518G/NE518G

K PACKAGE



1. V^-
2. NC
3. Load Sink Adjust
4. Output
5. Strobe
6. V^+
7. Ground
8. Invert
9. Non Invert
10. NC

ORDER PART NOS. SE518K/NE518K

ELECTRICAL CHARACTERISTICS (Standard Conditions: V+ = +6.0V, V- = -3.0V; Note 1)

CHARACTERISTICS	TEST CONDITIONS	NE518				SE518				UNITS
		MIN	TYP.	MAX.	TEMP.	MIN.	TYP.	MAX.	TEMP.	
INPUT OFFSET VOLTAGE	V_E = 1.0V, V_B = 0V, Note 5			4.0	0°C			4.0	-55°C	mV
			1.0	3.5	+25°C		1.0	3.0	+25°C	mV
				4.0	+70°C			4.0	+125°C	mV
VARIATION OF INPUT OFFSET	Note 7			1.0	0°C			1.5	-55°C	mV
VOLTAGE WITH TEMPERATURE				1.0	+70°C			1.5	+125°C	mV
INPUT BIAS CURRENT	$V_A = V_B$ = 0V			70	0°C			70	-55°C	μA
			35	50	+25°C		28	35	+25°C	μA
INPUT OFFSET CURRENT	$V_A = V_B$ = 0V			12	0°C			12	-55°C	μA
			3	9	+25°C		2.0	6.0	+25°C	μA
TURN ON DELAY TIME	Notes 3, 4		45	60	+25°C		40	50	+25°C	ns
RISE TIME	Notes 3, 4		15	25	+25°C		12	20	+25°C	ns
TURN OFF DELAY TIME	Notes 3, 4		45	60	+25°C		40	50	+25°C	ns
FALL TIME	Notes 3, 4		30	40	+25°C		25	35	+25°C	ns
OPEN LOOP BANDWIDTH (-3dB)			5.0		+25°C		5.0		+25°C	mHz
OPEN LOOP VOLTAGE GAIN		1200			0°C	1200			-55°C	V/V
		1375	1800		+25°C	1600	2100		+25°C	V/V
		1375			+70°C	1600			+125°C	V/V
OUTPUT VOLTAGE SWING (Positive)	V_A = -0.1V,	4.6			0°C	4.6			-55°C	V
	V_B = 0V	4.8	5.0		+25°C	4.9	5.1		+25°C	V
OUTPUT VOLTAGE SWING (Negative)	V_A = +0.1V,	-1.5			0°C	-1.5			-55°C	V
	V_B = 0V	-1.2	-1.4		+25°C	-1.2	-1.4		+25°C	V
		-0.8			+70°C	-0.8			+125°C	V
OUTPUT IMPEDANCE	f ≤ 10kHz		50		+25°C		50		+25°C	Ω
OUTPUT SINK CURRENT	V_A = +0.1V, V_B = 0V Note 2 R_L = 150Ω	2.2	2.8		+25°C	2.2	2.8		+25°C	mA
OUTPUT SOURCE CURRENT	V_A = -0.1V, V_B = 0V Note 2 R_L = 150Ω	-15	-18		+25°C	-18	-20		+25°C	mA
STROBE ON CURRENT	$V_D = V_B$ = 0V, V_A = -0.1V		-4.0	-4.75	+25°C		-3.8	-4.6	+25°C	mA
STROBE LEAKAGE CURRENT	V_D = 6.0V, V_A = +0.1V, V_B=0V		1.0	10	+70°C		1.0	10	+125°C	μA
DIFFERENTIAL INPUT IMPEDANCE	f ≤ 10kHz		1400		+25°C		2000		+25°C	Ω
COMMON MODE REJECTION RATIO	Note 6		80		+25°C		80		+25°C	dB
POWER SUPPLY CURRENT	$V_A = V_B$ = 0V		19	27	+25°C		19	25	+25°C	mA

NOTES

Letter subscripts refer to pins on circuit schematic.

1. All voltages are referenced to Pin G.
2. R_L must be connected between Pins E and G. Output sink current capability may be increased up to 10mA by connecting an external resistor between Pins H and F.
3. Differential Overdrive Voltage = 10mV.
4. t_{d_1} and t_{d_2} are measured from 80% point of input pulse to 20% point of output pulse. t_r and t_f are measured from 20% to 80% of output pulse.
5. Input offset voltage may be (+) or (–), Pin A with respect to Pin B.
6. Measured at a common mode voltage of +1.0VDC.
7. Variation from room temperature value.
8. See Signetics Bulletin No. 5001 for details of acceptance tests under Signetics SURE Program.
9. Positive current flow is defined as into the terminal referenced.
10. Precautionary measures should be taken to ensure current limiting in accordance with maximum ratings should the isolation diodes become forward biased.

DESCRIPTION

The 526 is a high speed analog comparator intended for use in systems where low propagation delay and fast recovery from common mode or differential input overdrive is required. The device is specifically designed to provide a wide input common mode range while operating from power supplies commonly found in digital logic systems.

The 526 consists of a medium gain, high frequency differential amplifier and a high speed TTL gate fabricated within a single substrate by planar and epitaxial techniques. The output gate of the 526 has voltage and current capabilities compatible with DCL, DTL and TTL. The 526 output gate has a full fan-out of 10 to standard TTL loads.

The amplifier and gate may be used independently or cascaded for applications as a voltage comparator, digital line receiver or sense amplifier. The second gate input is used to provide strobe capability when operating the amplifier and gate in cascade.

FEATURES

- **PROPAGATION DELAY** — **30ns**
- **INPUT COMMON MODE RANGE** — **+4.5V, −3.5V**
- **DIFFERENTIAL OVERDRIVE RECOVERY** — **20ns**
- **OUTPUT COMPATIBLE WITH STANDARD LOGIC FORMS**
- **OPERATES FROM STANDARD ±5V SUPPLIES**

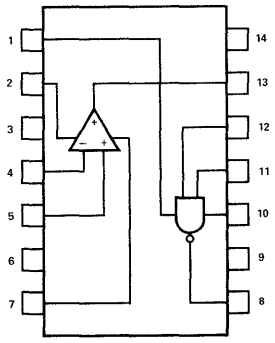
ABSOLUTE MAXIMUM RATINGS

Supply Voltage		+7.0V
Gate Input Voltage		+6.0V
Differential Input Voltage		+5.0V
Common Mode Input Voltage		+5.0V
Gate Output Current		+100 mA
Storage Temperature		-65°C to +150°C
Operating Temperature	SE526	-55°C to +125°C
	NE526	0°C to +75°C

Absolute Maximum Ratings are limiting values above which serviceability may be impaired.

PIN CONFIGURATION

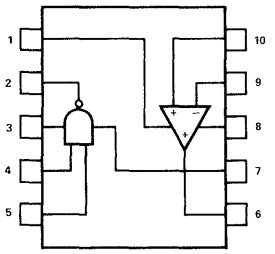
A PACKAGE



1. V_2^+
2. V_1^+
3. NC
4. V_{IN}
5. V_{IN}
6. NC
7. V^-
8. V_o
9. NC
10. Ground
11. V_{IN}
12. V_{IN}
13. e_o
14. NC

ORDER PART NOS.
SE526A/NE526A

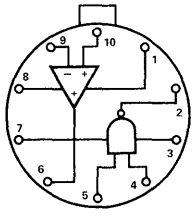
G PACKAGE



1. V_1^-
2. V_o
3. Ground
4. V_{IN}
5. V_{IN}
6. e_o
7. V_2^+
8. V_1^+
9. e_{in}
10. e_{in}

ORDER PART NOS.
SE526G/NE526G

K PACKAGE



1. V_1^-
2. V_o
3. Ground
4. V_{IN}
5. V_{IN}
6. e_o
7. V_2^+
8. V_1^+
9. e_{in}
10. e_{in}

ORDER PART NOS.
SE526K/NE526K

ELECTRICAL CHARACTERISTICS (Standard Conditions: $V_1^+ = V_2^+ = 5.0V$, $V^- = -5.0V$; Notes 1,2,3,4,13,14)

CHARACTERISTIC	SYMBOL	LIMITS				TEMPERATURE		NOTES
		MIN.	TYP.	MAX.	UNIT	SE526	NE526	
Input Offset Voltage	V_{io}		2.0	5.0	mV	−55°C	0°C	5
	V_{io}		2.0	5.0	mV	+25°C	+25°C	5
	V_{io}		2.0	5.0	mV	+125°C	+75°C	5
Input Bias Current	I_{in}		30.0	35.0	μA	−55°C	0°C	6
	I_{in}		25.0	35.0	μA	+25°C	+25°C	6
	I_{in}		22.0	35.0	μA	+125°C	+75°C	6
Input Offset Current	I_{io}		0.6	5.0	μA	−55°C	0°C	
	I_{io}		0.5	5.0	μA	+25°C	+25°C	
	I_{io}		0.4	5.0	μA	+125°C	+75°C	
Input Common Mode Range	V_{cm}	+4.2	+4.7		V	−55°C	0°C	
	V_{cm}	+4.2	+4.5		V	+25°C	+25°C	
	V_{cm}	+4.2	+4.4		V	+125°C	+75°C	
	V_{cm}	−3.2	−3.5		V	−55°C	0°C	
	V_{cm}	−3.2	−3.5		V	+25°C	+25°C	
	V_{cm}	−3.2	−3.5		V	+125°C	+75°C	
Amplifier Output Voltage	V_{ohi}	3.5			V	−55°C	0°C	
	V_{ohi}	3.5			V	+25°C	+25°C	
	V_{ohi}	3.5			V	+125°C	+75°C	
	V_{olo}			0.6	V	−55°C	0°C	
	V_{olo}			0.5	V	+25°C	+25°C	
	V_{olo}			0.4	V	+125°C	+75°C	
Amplifier Power Consumption	P_d		90	120	mV	−55°C	0°C	
	P_d		100	120	mV	+25°C	+25°C	
	P_d		110	120	mV	+125°C	+75°C	
Gate Output Voltage	$V1_o$	2.8	3.5		V	−55°C	0°C	7, 8
	$V1_o$	2.8	3.2		V	+25°C	+25°C	7, 8
	$V1_o$	2.8	3.0		V	+125°C	+75°C	7, 8
	$V0_o$		0.3	0.4	V	−55°C	0°C	7, 8
	$V0_o$		0.2	0.4	V	+25°C	+25°C	7, 8
	$V0_o$		0.3	0.4	V	+125°C	+75°C	7, 8
Gate Output Sink Current	$I0_o$	16.0			mA	+25°C	+25°C	8
Gate Output Source Current	$I1_o$	1.0			mA	+25°C	+25°C	7
Gate Input Threshold Voltage	$V1_i$	2.0			V	−55°C	0°C	9
	$V1_i$	2.0			V	+25°C	+25°C	9
	$V1_i$	2.0			V	+125°C	+75°C	9
	$V0_i$			1.0	V	−55°C	0°C	10
	$V0_i$			0.9	V	+25°C	+25°C	10
	$V0_i$			0.8	V	+125°C	+75°C	10
Gate Input Current (Input "0")	$I0_i$	−0.1	−1.2	−1.6	mA	−55°C	0°C	
	$I0_i$	−0.1	−1.4	−1.6	mA	+25°C	+25°C	
	$I0_i$	−0.1	−1.2	−1.6	mA	+125°C	+75°C	
(Input "1")	$I1_i$		5	25	μA	−55°C	0°C	
	$I1_i$		10	25	μA	+25°C	+25°C	
	$I1_i$		15	25	μA	+125°C	+75°C	
Gate Current Consumption (Output "1")	$I_{CC}1$			2.00	mA	−55°C	0°C	
	$I_{CC}1$			2.00	mA	+25°C	+25°C	
	$I_{CC}1$			2.00	mA	+125°C	+75°C	
(Output "0")	$I_{CC}0$			5.00	mA	−55°C	0°C	
	$I_{CC}0$			5.00	mA	+25°C	+25°C	
	$I_{CC}0$			5.00	mA	+125°C	+75°C	
Gate Input Latch Voltage Rating	BV_i			6.0	V	+25°C	+25°C	
Gate Output Short Circuit Current	I_{so}	−10.0		−70.0	mA	+25°C	+25°C	
Switching Times								
Gate Turn-On Delay	T_{on}		15	17	ns	+25°C	+25°C	11
Gate Turn-Off Delay	T_{off}		15	17	ns	+25°C	+25°C	11
Propagation Delay	$T_{pd}0$		30	42	ns	+25°C	+25°C	11
Propagation Delay	$T_{pd}1$		40	48	ns	+25°C	+25°C	11
Differential Overload Recovery	t_{dm}		30	40	ns	+25°C	+25°C	11, 12

Recommended Operating Supply Voltages ($V_1^+ = V_2^+ = 5.0V$, $V^- = -5.0V$

NOTES:

1. All measurements are referenced to the ground terminal.
2. Positive current is defined as into the pin referenced.
3. Pins not specifically referenced are left electrically open.
4. Precautionary measures should be taken to ensure current limiting in accordance with Absolute Maximum Ratings should the isolation diodes become forward biased.
5. Input Offset Voltage is tested at guaranteed Input Common Mode Range voltage limits and includes the worst-case variations of voltage gain and input impedance. These are the maximum values required to drive the output down to "0" or up to "1".
6. Input Bias Current is defined as the maximum current required to bias either input.
7. Output source current is supplied through a resistor to ground.
8. Output sink current is supplied through a resistor to V_2^+.
9. These limits are guaranteed by Gate Output Voltage ($V0_O$) test.
10. These limits are guaranteed by Gate Output Voltage ($V1_O$) tests.
11. Load capacitance includes test fixture and probe capacitance.
12. Differential Input Voltage = 500mV for this test.
13. Acceptance Test Subgroup A-7 provides end point parameters for linear devices processed to Signetics SURE Program. See Signetics SURE Bulletin 5001.
14. Manufacturer reserves the right to make design and process changes and improvements.

DESCRIPTION

The SE/NE 527 is a high speed analog voltage comparator which, for the first time mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed T^2L gates with a precision linear amplifier on a single monolithic chip.

The SE/NE 527 is similar in design to the Signetics SE/NE 529 voltage comparator except that it incorporates a "Emitter Follower" input stage for extremely low input currents. This opens the door to a whole new range of applications for analog voltage comparators.

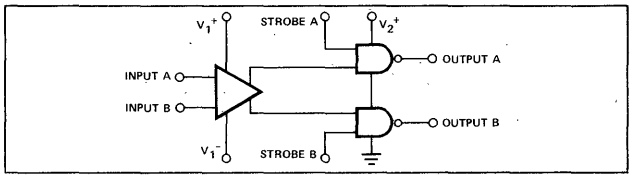
FEATURES

- 15 nsec PROPAGATION DELAY
- COMPLEMENTARY OUTPUT GATES
- TTL OR ECL COMPATIBLE OUTPUTS
- WIDE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGE

APPLICATIONS

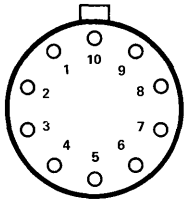
A/D CONVERSION
ECL TO TTL INTERFACE
TTL TO ECL INTERFACE
MEMORY SENSING
OPTICAL DATA COUPLING

BLOCK DIAGRAM



PIN CONFIGURATION

K PACKAGE
(Top View)



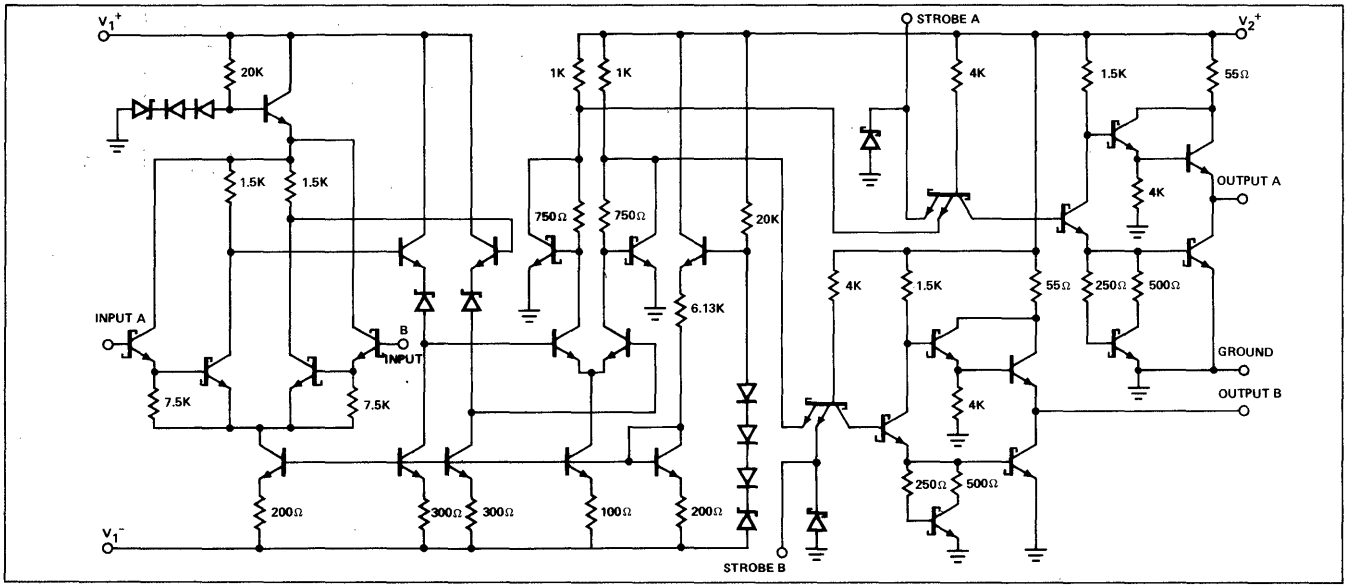
1. Input A
2. Input B
3. V_1^-
4. Strobe B
5. Output B
6. Ground
7. Output A
8. Strobe A
9. V_2^+
10. V_1^+

ORDER PART NOS. SE527K/NE527K

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (V_1^+)	+15 volts
Negative Supply Voltage (V_1^-)	-15 volts
Gate Supply Voltage (V_2^+)	+7 volts
Output Voltage	+15 volts
Differential Input Voltage	±5 volts
Input Common Mode Voltage	±6 volts
Power Dissipation	600mW
Operating Temperature Range	
NE 527	0°C to +70°C
SE 527	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 60 seconds)	+300°C

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS ($V_1^+ = +10V$, $V_1^- = -10V$, $V_2^+ = +5.0V$, $V_{in} = 0V$)

PARAMET	TEST CONDITIONS	SE 527			NE 527			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Input Offset Voltage @25°C				4			6	mV
over temperature range				6			10	mV
Input Bias Current @25°C	$V_1^+ = 10V$, $V_1^- = -10V$			2			2	μA
over temperature range	$V_{in} = 0V$			4			4	μA
Input Offset Current @25°C	$V_1^+ = 10V$, $V_1^- = -10V$			0.5			0.75	μA
over temperature range	$V_{in} = 0V$			1			1	μA
Voltage Gain	$T_A = 25°C$		5			5		V/mV
Input Resistance	$T_A = 25°C$, f = 1 kHz		500			500		KΩ
GATE CHARACTERISTICS								
Output Voltage								
"1" State	$V_2^+ = 4.75V$, $I_{source} = -1mA$	2.5	3.3		2.7	3.3		V
"0" State	$V_2^+ = 4.75V$, $I_{sink} = 10mA$			0.5			0.5	V
Strobe Inputs								
"0" Input Current	$V_2^+ = 5.25V$, $V_{strobe} = 0.5V$			-2			-2	mA
"1" Input Current @25°C	$V_2^+ = 5.25V$, $V_{strobe} = 2.7V$			50			100	μA
over temperature range				200			200	μA
"0" Input Voltage	$V_2^+ = 4.75V$			0.8			0.8	V
"1" Input Voltage	$V_2^+ = 4.75V$	2.0			2.0			V
Short Circuit Output Current	$V_2^+ = 5.25V$, $V_{out} = 0V$	-40		-100	-40		-100	mA
POWER SUPPLY REQUIREMENTS								
Supply Voltage								
V_1^+		5		10	5		10	V
V_1^-		-6		-10	-6		-10	V
V_2^+		4.5	5	5.5	4.75	5	5.25	V
Supply Current	$V_1^+ = 10V$, $V_1^- = -10V$							
	$V_2^+ = 5.25V$							
I_1^+	$T_A = 125°C$			3.25				mA
	$T_A = 25°C$			3.75				mA
	$T_A = -55°C$			4.0				mA
	$0°C \leqslant T_A \leqslant 70°C$						5	mA
I_1^-	$T_A = 125°C$			7.0				mA
	$T_A = 25°C$			7.5				mA
	$T_A = -55°C$			8.5				mA
	$0°C \leqslant T_A \leqslant 70°C$						10	mA
I_2^+	$T_A = 125°C$			15				mA
	$T_A = 25°C$			16				mA
	$T_A = -55°C$			18				mA
	$0°C \leqslant T_A \leqslant 70°C$						20	mA
TRANSIENT RESPONSE	V_{in} = 50 mV overdrive							
Propagation Delay Time								
t_{pd} (0)	$T_A = +25°C$		14			14		ns
t_{pd} (1)	$T_A = +25°C$		16			16		ns
Delay between Output A and B	$T_A = +25°C$		2			2		ns
Strobe Delay Time								
Turn On	$T_A = +25°C$		6			6		ns
Turn Off	$T_A = +25°C$		6			6		ns

Parameters are guaranteed over the temperature range unless otherwise noted.

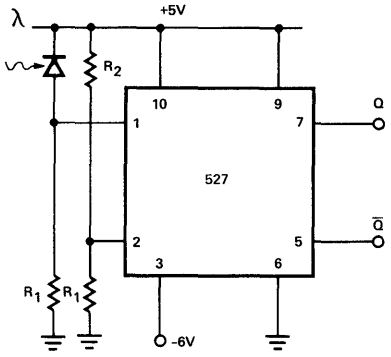
APPLICATIONS

One of the main features of the device is that supply voltages (V_1^+, V_1^-) need not be balanced, as indicated in the following diagrams. For proper operation, however, negative supply (V_1^-) should always be at least six volts more negative than the ground terminal (pin 6). Input Common Mode range should be limited to values of two volts less than the supply voltages (V_1^+ and V_1^-) up to a maximum of ±6 volts as supply voltages are increased.

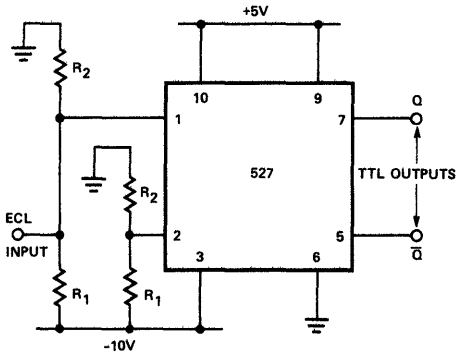
It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

TYPICAL APPLICATIONS

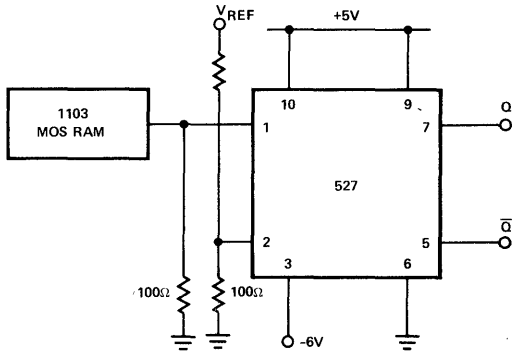
PHOTODIODE DETECTOR



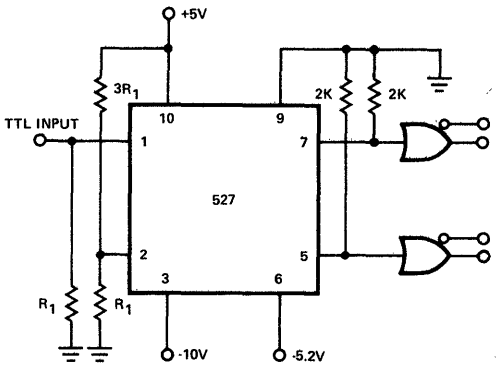
ECL TO TTL INTERFACE



MOS MEMORY SENSE AMP.

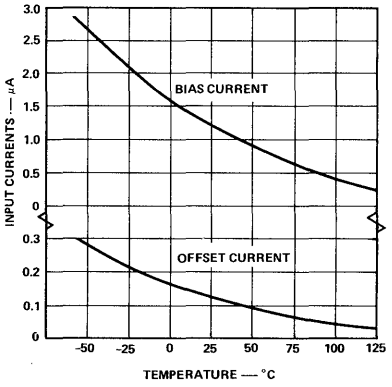


TTL TO ECL INTERFACE

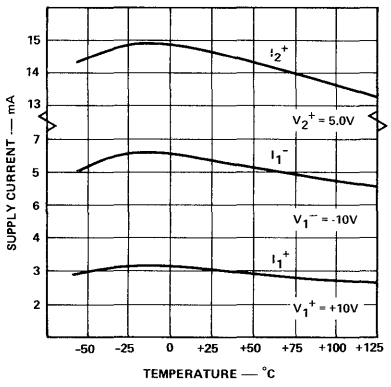


TYPICAL PERFORMANCE CURVES

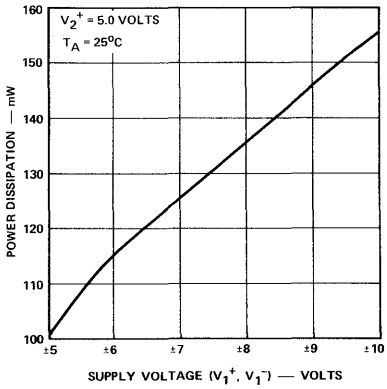
INPUT CURRENTS VS TEMPERATURE



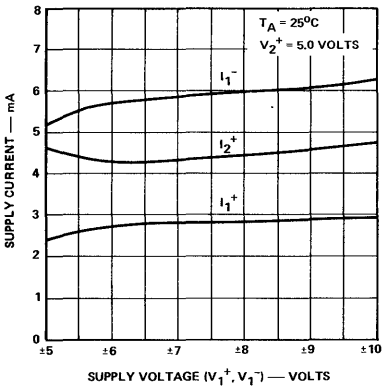
SUPPLY CURRENT VS TEMPERATURE



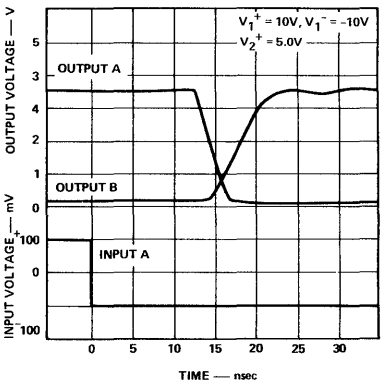
POWER DISSIPATION VS SUPPLY VOLTAGE



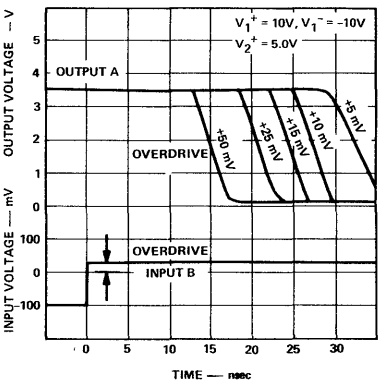
SUPPLY CURRENT VS SUPPLY VOLTAGE



OUTPUT PROPAGATION DELAYS



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



DESCRIPTION

The SE/NE 529 is a high speed analog voltage comparator which, for the first time mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed T^2L gates with a precision linear amplifier on a single monolithic chip.

FEATURES

- 10 nsec PROPAGATION DELAY
- COMPLEMENTARY OUTPUT GATES
- TTL OR ECL COMPATIBLE OUTPUTS
- WIDE COMMON MODE AND DIFFERENTIAL VOLTAGE RANGE

APPLICATIONS

A/D CONVERSION

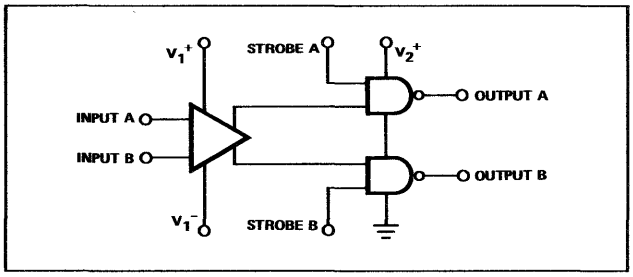
ECL TO TTL INTERFACE

TTL TO ECL INTERFACE

MEMORY SENSING

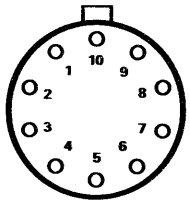
OPTICAL DATA COUPLING

BLOCK DIAGRAM



PIN CONFIGURATION

K PACKAGE
(Top View)



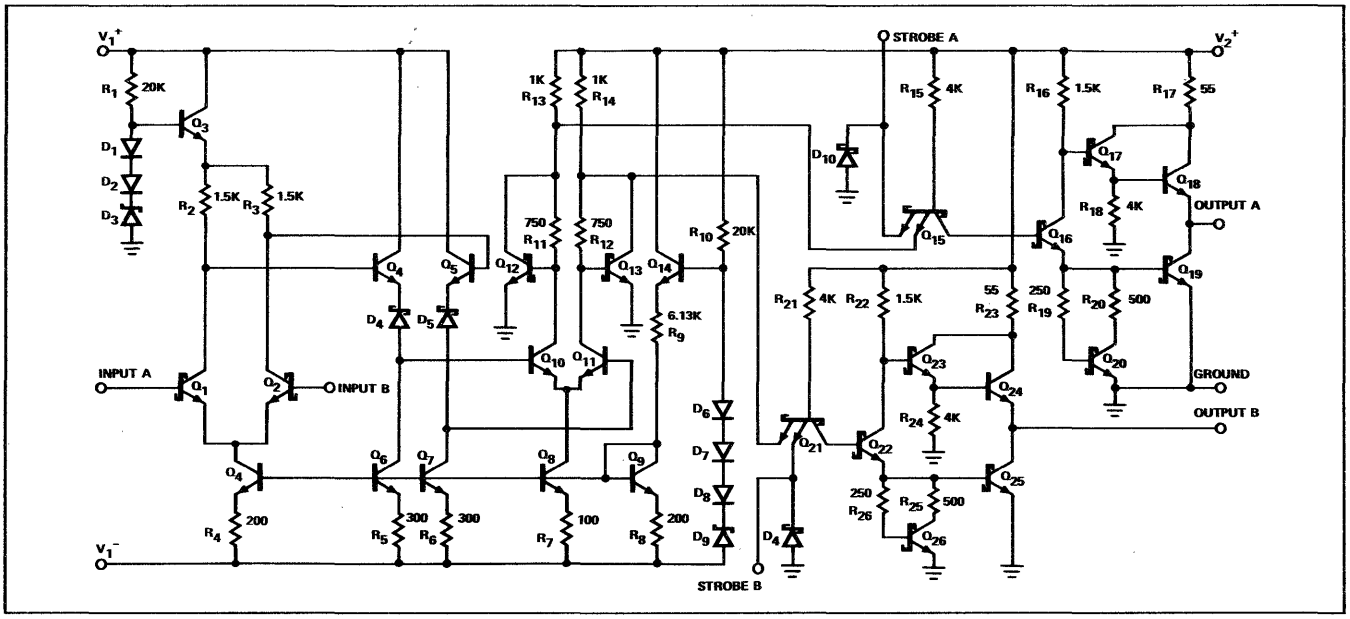
1. Input A
2. Input B
3. V_1^-
4. Strobe B
5. Output B
6. Ground
7. Output A
8. Strobe A
9. V_2^+
10. V_1^+

ORDER PART NOS. SE529K/NE529K

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (V_1^+)	+15 volts
Negative Supply Voltage (V_1^-)	-15 volts
Gate Supply Voltage (V_2^+)	+7 volts
Output Voltage	+15 volts
Differential Input Voltage	±5 volts
Input Common Mode Voltage	±6 volts
Power Dissipation	600mW
Operating Temperature Range	
NE 529	0°C to +70°C
SE 529	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 60 seconds)	+300°C

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS ($V_1^+ = +10V$, $V_2^+ = +5.0V$, $V_1^- = -10V$, $V_{in} = 0V$)

PARAMETER	TEST CONDITIONS	SE 529			NE 529			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Input Offset Voltage @25°C				4			6	mV
over temperature range				6			10	mV
Input Bias Current @25°C	$V_1^+ = 10V$, $V_1^- = -10V$		5	12		5	20	μA
over temperature range	$V_{in} = 0V$			36			50	μA
Input Offset Current @25°C	$V_1^+ = 10V$, $V_1^- = -10V$		2	3		2	5	μA
over temperature range	$V_{in} = 0V$			9			15	μA
Voltage Gain	$T_A = 25°C$		5			5		V/mV
Input Resistance	$T_A = 25°C$, f = 1 kHz		10			10		KΩ
GATE CHARACTERISTICS								
Output Voltage								
"1" State @25°C	$V_2^+ = 4.75V$, $I_{source} = -1mA$	2.5	3.3		2.7	3.3		V
"0" State @25°C	$V_2^+ = 4.75V$, $I_{sink} = 10mA$			0.5			0.5	V
Strobe Inputs								
"0" Input Current	$V_2^+ = 5.25V$, $V_{strobe} = 0.5V$			-2			-2	mA
"1" Input Current @25°C	$V_2^+ = 5.25V$, $V_{strobe} = 2.7V$			50			100	μA
over temperature range				200			200	μA
"0" Input Voltage	$V_2^+ = 4.75V$			0.8			0.8	V
"1" Input Voltage	$V_2^+ = 4.75V$	2.0			2.0			V
Short Circuit Output Current	$V_2^+ = 5.25V$, $V_{out} = 0V$	-40		-100	-40		-100	mA
POWER SUPPLY REQUIREMENTS								
Supply Voltage								
V_1^+		5		10	5		10	V
V_1^-		-6		-10	-6		-10	V
V_2^+		4.5	5	5.5	4.75	5	5.25	V
Supply Current	$V_1^+ = 10V$, $V_1^- = -10V$, $V_2^+ = 5.25V$							
I_1^+	$T_A = 125°C$			3.25				mA
	$T_A = 25°C$			3.75				mA
	$T_A = -55°C$			4.0				mA
	$0°C \leqslant T_A \leqslant 70°C$						5	mA
I_1^-	$T_A = 125°C$			7.0				mA
	$T_A = 25°C$			7.5				mA
	$T_A = -55°C$			8.5				mA
	$0°C \leqslant T_A \leqslant 70°C$						10	mA
I_2^+	$T_A = 125°C$			15				mA
	$T_A = 25°C$			16				mA
	$T_A = -55°C$			18				mA
	$0°C \leqslant T_A \leqslant 70°C$						20	mA
TRANSIENT RESPONSE	V_{in} = 50 mV overdrive							
Propagation Delay Time								
t_{pd} (0)	$T_A = +25°C$		10			10		ns
t_{pd} (1)	$T_A = +25°C$		12			12		ns
Delay between Output A and B	$T_A = +25°C$		2			2		ns
Strobe Delay Time								
Turn On	$T_A = +25°C$		6			6		ns
Turn Off	$T_A = +25°C$		6			6		ns

Parameters are guaranteed over the temperature range unless otherwise noted.

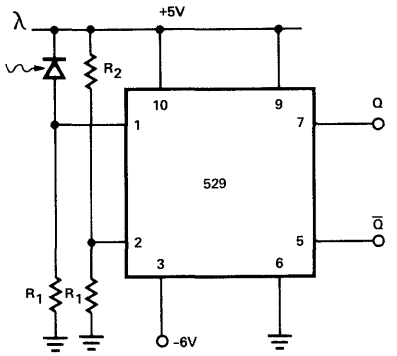
APPLICATIONS

One of the main features of the device is that supply voltages (V_1^+, V_1^-) need not be balanced, as indicated in the following diagrams. For proper operation, however, negative supply (V_1^-) should always be at least five volts more negative than the ground terminal (pin 6). Input Common Mode range should be limited to values of two volts less than the supply voltages (V_1^+ and V_1^-) up to a maximum of ±6 volts as supply voltages are increased.

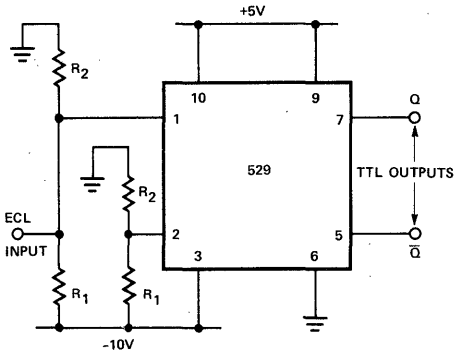
It is also important to note that Output A is in phase with Input A and Output B is in phase with Input B.

TYPICAL APPLICATIONS

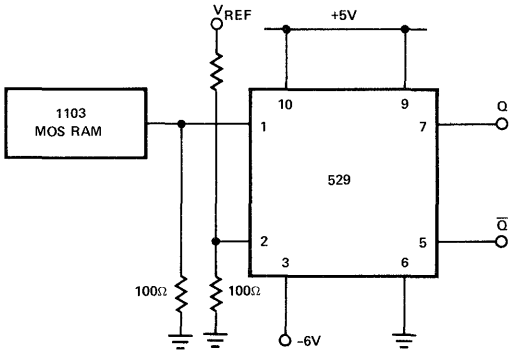
PHOTODIODE DETECTOR



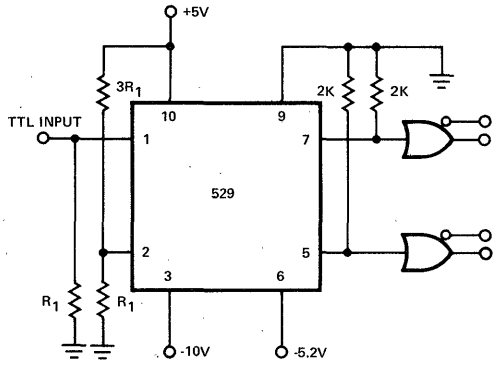
ECL TO TTL INTERFACE



MOS MEMORY SENSE AMP

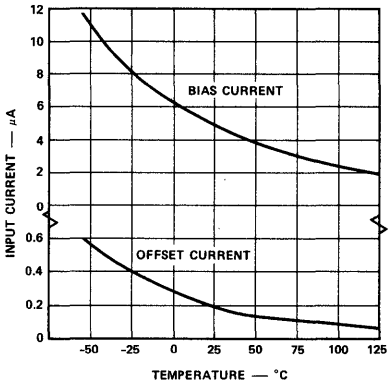


TTL TO ECL INTERFACE

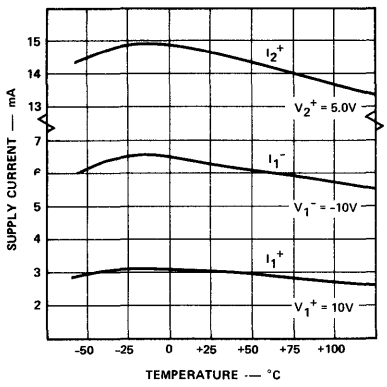


TYPICAL PERFORMANCE CURVES

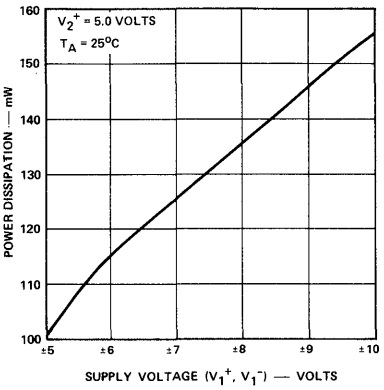
INPUT CURRENTS VS TEMPERATURE



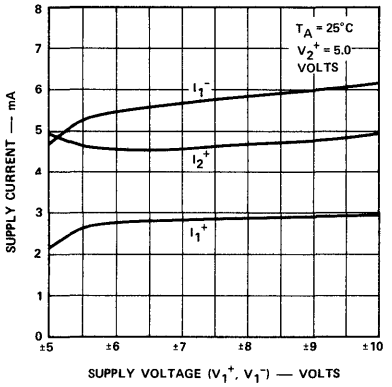
SUPPLY CURRENT VS TEMPERATURE



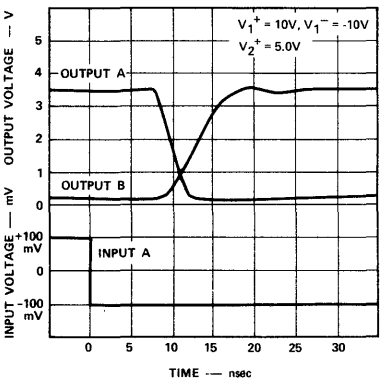
POWER DISSIPATION VS SUPPLY VOLTAGE



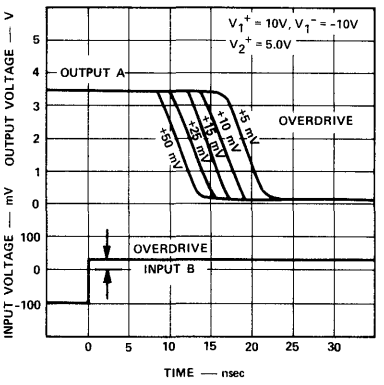
SUPPLY CURRENT VS SUPPLY VOLTAGE



OUTPUT PROPAGATION DELAYS



RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



DESCRIPTION

The μA710 is a High Speed Differential Voltage Comparator featuring low offset voltage, high sensitivity and a wide input voltage range. It is ideally suited for use as a pulse height discriminator, an analog comparator or a digital line receiver. The output structure of the μA710 is compatible with DTL, TTL and Utilogic integrated circuits.

The μA710 is specified for operation over the MIL temperature range of -55°C to +125°C. The μA710C is specified for operation over the commercial/industrial temperature range of 0°C to +75°C.

FEATURES

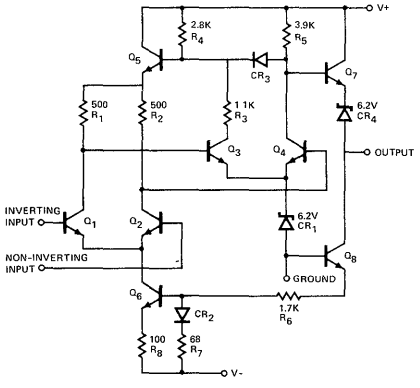
- **FAST RESPONSE – 40ns**
- **HIGH SENSITIVITY – 1.7V/mv**
- **LOW OFFSET VOLTAGE TEMPERATURE COEFFICIENT – 3.5μV/°C**
- **HIGH INPUT VOLTAGE RANGE – ±5.0V**

ABSOLUTE MAXIMUM RATINGS

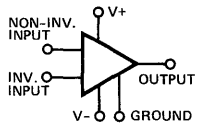
Positive Supply Voltage	+14.0V
Negative Supply Voltage	-7.0V
Peak Output Current	10mA
Differential Input Voltage	±5.0V
Input Voltage	±7.0V
Internal Power Dissipation (Note 4)	
TO-99	300mW
TO-91	200mW
Operating Temperature Range	
μA710	-55°C to +125°C
μA710C	0°C to +75°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Maximum Ratings are limiting values above which serviceability may be impaired.

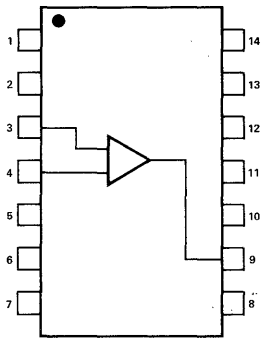
BASIC CIRCUIT SCHEMATIC



PIN CONFIGURATION



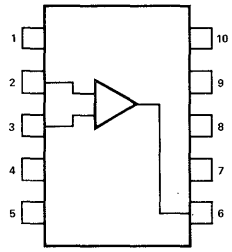
A PACKAGE
(Top View)



1. NC
2. Ground
3. Non-Inverting Input
4. Inverting Input
5. NC
6. V^-
7. NC
8. NC
9. Output
10. NC
11. V^+
12. NC
13. NC
14. NC

ORDER PART NOS. μA710A/μA710CA

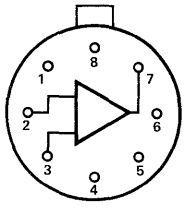
G PACKAGE



1. Ground
2. Non-Inverting Input
3. Inverting Input
4. NC
5. V^-
6. Output
7. NC
8. V^+
9. NC
10. NC

ORDER PART NOS. μA710G/μA710CG

T PACKAGE



1. Ground
2. Non-Inverting Input
3. Inverting Input
4. V^-
5. NC
6. NC
7. Output
8. V^+

ORDER PART NOS. μA710T/μA710CT

ELECTRICAL CHARACTERISTICS (Note 1)

(Standard Conditions: T_A = +25°C, V^+ = 12V, V^- = -6.0V unless otherwise specified)

PARAMETERS	TEST CONDITIONS	MIN		TYP		MAX		UNITS
		μA710	μA710C	μA710	μA710C	μA710	μA710C	
Input Offset Voltage	$R_S \leq 200\Omega$ Note 3			0.6	1.6	2.0	5.0	mV
Input Offset Current	Note 3			0.75	1.8	3.0	5.0	μA
Input Bias Current				13	16	20	25	μA
Voltage Gain		1250	1000	1700	1500			
Output Resistance				200	200			Ω
Output Sink Current	$\Delta V_{in} \geq 5mV$, $V_{out} = 0$	2.0	1.6	2.5				mA
Response Time	Note 2			40	40			ns
Except as noted, the following specifications apply over the temperature ranges of:		-55°C ≤ T_A ≤ +125°C for the S5710 0°C ≤ T_A ≤ +75°C for the N5710						
Input Offset Voltage	$R_S \leq 200\Omega$ Note 3					3.0	6.5	
Average Temperature Coefficient of Input Offset Voltage	$R_S = 50\Omega$, T_A = +25°C to +125°C			3.5		10		μV/°C
	$R_S = 50\Omega$, T_A = +25°C to -55°C			2.7		10		
	$R_S = 50\Omega$, T_A = 0°C to +75°C				5		20	
Input Offset Current	T_A = +125°C Note 3			0.25		3.0		μA
	T_A = -55°C			1.8		7.0		μA
	T_A = 0°C to +75°C						7.5	μA
Average Temperature Coefficient of Input Offset Current	T_A = +25°C to +125°C			5.0		25		nA/°C
	T_A = +25°C to -55°C			15		75		nA/°C
	T_A = +25°C to +75°C				15		50	μA/°C
	T_A = +25°C to 0°C				24		100	μA/°C
Input Bias Current	T_A = -55°C			27		45		μA
	T_A = 0°C				25		40	μA
Input Common Mode Voltage Range	V^- = -7.0V	±5.0	±5.0					V
Common Mode Rejection Ratio	$R_S \leq 200\Omega$	80	70	100	98			dB
Differential Input Voltage Range		±5.0	±5.0					
Voltage Gain		1000	800					
Positive Output Level	$\Delta V_{in} \geq 5mV$, $0 \leq I_{out} \leq 5.0mA$	2.5	2.5	3.2	3.2	4.0	4.0	V
Negative Output Level	$\Delta V_{in} \geq 5mV$	-1.0	-1.0	-0.5	-0.5	0	0	V
Output Sink Current	T_A = +125°C, $\Delta V_{in} \geq 5ma$, $V_{out} = 0$	0.5		1.7				mA
	T_A = -55°C, $\Delta V_{in} \geq 5mV$, $V_{out} = 0$	1.0		2.3				mA
	T_A = 0°C to +75°C, $\Delta V_{in} \geq 5mV$, $V_{out} = 0$		0.5					mA
Positive Supply Current	$V_{out} \leq 0$			5.2	5.2	9.0	9.0	mA
Negative Supply Current				4.6	4.6	7.0	7.0	mA
Power Consumption				90	90	150	150	mW

(Recommended Operating Supply Voltages: V^+ = 12V, V^- = -6V)

NOTES:

1. All voltages are referenced to pin F.
2. The response time specified is measured with a 100mV input step, and a 5mV overdrive.
3. Input Offset Voltage and Input Offset Current are specified for output voltage levels of:

μA710	μA710C
1.8V at -55°C	1.5V at 0°C
1.4V at +25°C	1.4V at +25°C
1.0V at +125°C	1.2V at +75°C

4. Rating applies for temperatures up to: μA710 — +125°C
   μA710C — +75°C

DESCRIPTION

The μA711 High Speed Dual Voltage Comparator features low offset voltage, high sensitivity and a wide input voltage range. It is ideal for use as a bi-directional limit detector in automatic test equipment.

Due to fast response and strobe control capabilities the μA711 performs well as a sense amplifier in core memory systems.

The μA711 is specified over the military temperature range of -55°C to +125°C. The μA711 is specified over the commercial/industrial temperature range of 0°C to +75°C.

FEATURES

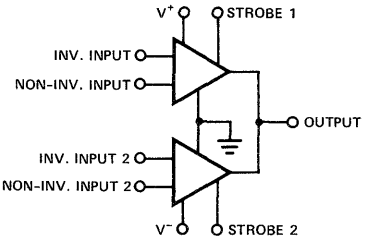
- **FAST RESPONSE – 40ns**
- **HIGH SENSITIVITY – 1.5V/mV**
- **LOW OFFSET VOLTAGE TEMPERATURE COEFFICIENT – 5μV/°C**
- **HIGH INPUT VOLTAGE RANGE – ±5.0V**

ABSOLUTE MAXIMUM RATINGS

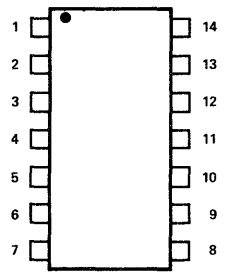
Positive Supply Voltage	+14.0V
Negative Supply Voltage	-7.0V
Peak Output Current	50mA
Differential Input Voltage	±5.0V
Input Voltage	±7.0V
Internal Power Dissipation (Note 4)	
TO-99	300mW
Operating Temperature Range	
μA711	-55°C to +125°C
μA711C	0°C to +75°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

Maximum ratings are limiting values above which serviceability may be impaired.

PIN CONFIGURATION



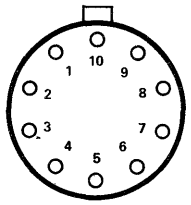
A PACKAGE
(Top View)



ORDER PART NOS.
μA711A/μA711CA

1. NC
2. Inverting Input 1
3. Non-Inverting Input 1
4. V^-
5. Non-Inverting Input 1
6. Inverting Input 2
7. NC
8. NC
9. Strobe 2
10. Output
11. V^+
12. Ground
13. Strobe 1
14. NC

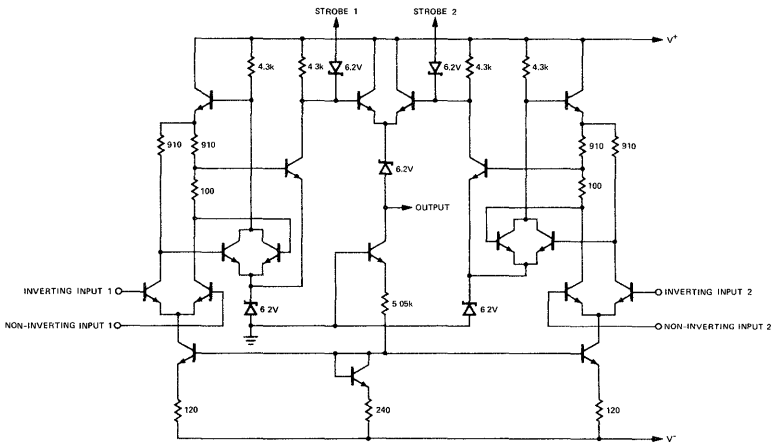
K PACKAGE



ORDER PART NOS.
μA711K/μA711CK

1. Ground
2. Strobe 1
3. Inverting Input 1
4. Non-Inverting Input 1
5. V^-
6. Non-Inverting Input 2
7. Inverting Input 2
8. Strobe 2
9. Output
10. V^+

BASIC CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS (Note 1)

(Standard Conditions: $T_A = +25°C$, $V^+ = 12.0V$, $V^- = -6.0V$ unless otherwise specified)

PARAMETERS	TEST CONDITIONS	MIN		TYP		MAX		UNITS
		μA711	711C	μA711	711C	μA711	711C	
Input Offset Voltage	$V_{out} = +1.4V$, $R_S \leq 200\Omega$, $V_{cm} = 0$			1.0	1.0	3.5	5.0	mV
	$V_{out} = +1.4V$, $R_S \leq 200\Omega$			1.0	1.0	5.0	7.5	mV
Input Offset Current	$V_{out} = +1.4V$			0.5	0.5	10.0	15.0	μA
Input Bias Current				25	25	75	100	μA
Voltage Gain		750	700	1500	1500			
Response Time	Note 2			40	40			ns
Strobe Release Time				12	12			ns
Input Common Mode Voltage Range	$V^- = -7.0V$	±5.0	±5.0					V
Differential Input Voltage Range		±5.0	±5.0					V
Output Resistance				200	200			Ω
Positive Output Level	$V_{in} \geq 10mV$			4.5	4.5	5.0	5.0	V
Loaded Positive Output Level	$V_{in} \geq 10mV$, $I_o = 5mA$	2.5	2.5	3.5	3.5			
Negative Output Level	$V_{in} \geq 10mV$	-1.0	-1.0	-0.5	-0.5	0	0	V
Strobed Output Level	$V_{strobe} < 0.3V$	-1.0	-1.0			0	0	V
Output Sink Current	$V_{in} \geq 10mV$, $V_{out} \geq 0$	0.5	0.5	0.8	0.8			mA
Strobe Current	$V_{strobe} = 100mV$			1.2	1.2	2.5	2.5	mA
Positive Supply Current	$V_{out} \leq 0$			8.6	8.6			mA
Negative Supply Current				3.9	3.9			mA
Power Consumption				130	130	200	200	mW
The following specifications apply over the temperature ranges of:		$-55°C \leq T_A \leq +125°C$ for the μA711 $0°C \leq T_A \leq +75°C$ for the μA711C						
Input Offset Voltage	$R_S \leq 200\Omega$, $V_{cm} = 0$, Note 3					4.5	6.0	mV
	$R_S \leq 200\Omega$					6.0	10.0	mV
Input Offset Current	Note 3					20	25	μA
Input Bias Current						150	150	μA
Temperature Coefficient of Input Offset Voltage				5.0	5.0			μV/°C
Voltage Gain		500	500					

Recommended Operating Supply Voltages: $V^+ = 12V$, $V^- = -6V$

NOTES:

1. All voltages are referenced to pin 1.
2. The response time specified is for a 100mV input step, with a 5mV overdrive.
3. The Input Offset Voltage and Input Offset Current are specified for a logic threshold voltage of: 1.8V at 0°C.

μA711	μA711C
1.8V at 0°C	1.5V at 0°C
1.4V at +25°C	1.4V at +25°C
1.0V at +125°C	1.2V at +75°C

4. Rating applies for temperatures up to: μA711 — +125°C
   μA711C — +75°C

DESCRIPTION

The NE528B is a monolithic four channel plated wire sense amplifier designed to read small signals, 3mV or above, and translate them to TTL logic levels. The NE528B features input channel selection by means of three TTL channel select inputs, one of which allows for total input disable. The output is TTL compatible and can be used in the "WIRED-OR" configuration.

FEATURES

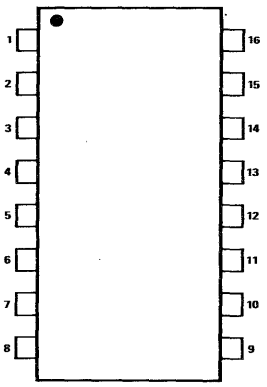
- FOUR CHANNELS IN ONE PACKAGE
- TOTAL INPUT DISABLE PROVIDED
- 16mA SINK CAPABILITY
- OUTPUT STRUCTURE ALLOWS FOR WIRED-OR, PARALLELING
- CHANNEL SELECT, STROBE AND OUTPUT TTL COMPATIBLE

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±10V
Strobe Control Voltage	+6V
Differential Input Voltage	±5V
Amplifier Input Current	2mA
Common Mode Input Voltage	+5 to -6V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	0°C to 70°C

PIN CONFIGURATION

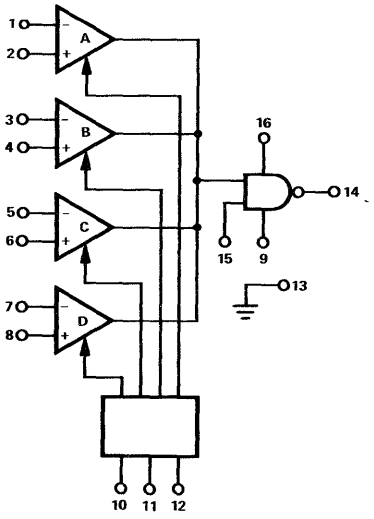
B & E PACKAGE
(Top View)



1. Input A^-
2. Input A^+
3. Input B^-
4. Input B^+
5. Input C^-
6. Input C^+
7. Input D^-
8. Input D^+
9. V^-
10. Input Enable 1
11. Input Enable 2
12. Input Enable 3
13. Ground
14. Output
15. Strobe
16. V^+

ORDER PART NOS. NE528B/NE528E

LOGIC DIAGRAM AND TRUTH TABLE



Amplifier Activated	Enable Input 1	Enable Input 2	Enable Input 3
A	0	0	1
B	1	0	1
C	1	1	1
D	0	1	1
NONE	X	X	0

x = DON'T CARE

ELECTRICAL CHARACTERISTICS (Conditions: $V^+ = 5V$, $V^- = -6V$, $T_A = 25°$ unless specified)

PARAMETERS	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Bias Current	$V^+ = 5.25V$, $V^- = -6.3V$, $V_{in} = 0$		15	50	μA
Input Offset Current	$V^+ = 5.25V$, $V^- = -6.3V$, $V_{in} = 0$		0.5	5	μA
Differential Input Threshold Voltage	Figure 1	-3		+3	mV
Output Voltage					
"1" State	$V^+ = 4.75V$	2.4			V
"0" State	$V^+ = 5.25V$			0.4	V
Enable and Strobe Inputs					
"0" Input Current	$V^+ = 5.25V$, $V^- = -6.3V$, $V_{in} = 0.4V$			-1.6	mA
"1" Input Current	$V^+ = 5.25V$, $V^- = -6.3V$, $V_{in} = 2.4V$			40	μA
"0" Input Voltage	$V^+ = 4.75V$, $V^- = -5.7V$			0.8	V
"1" Input Voltage	$V^+ = 4.75V$, $V^- = -5.7V$	2.0			V
Power Consumption	$V^+ = 5.25V$, $V^- = -6.3V$			270	mW
Positive Supply Current	$V^+ = 5.25V$, $V^- = -6.3V$			35	mA
Negative Supply Current	$V^+ = 5.25V$, $V^- = -6.3V$			15	mA
Input Resistance	f = 1 kHz		2K		Ω
Propagation Delay	Unused Inputs Grounded, Figure 2				
t_{pd} (0)			20		nsec
t_{pd} (1)			25		nsec
Output Rise Time	Figure 3		16		nsec
Output Fall Time	Figure 3		6		nsec
Strobe Delay Time	Figure 2				
Turn On			10		nsec
Turn Off			12		nsec
Channel Select Time	Figure 3		9		nsec
Total Disable to Enable Time	Figure 2		25		nsec
Enable to Total Disable Time	Figure 2		28		nsec

LOGIC DIAGRAM AND TEST TABLE ($V^+ = 5V$, $V^- = -6V$, $T_A = 25°C$)

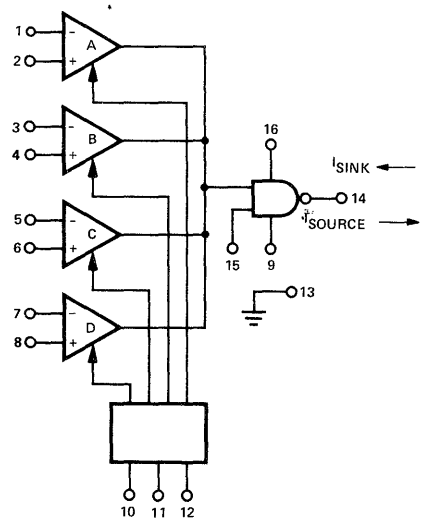
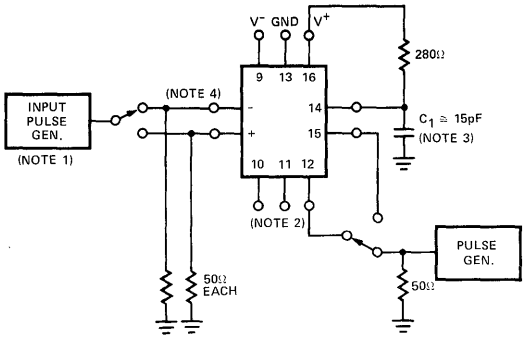
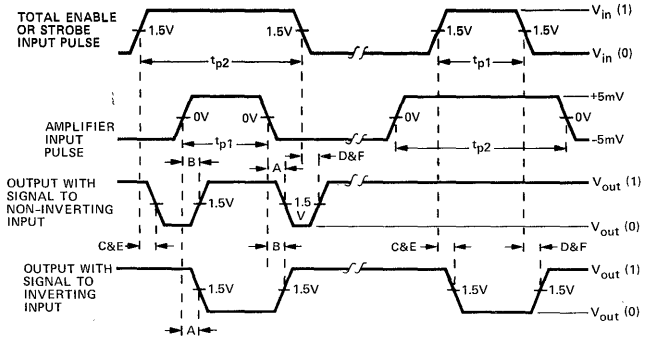


FIGURE 1

Pin 10	Pin 11	Pin 12	Pin 15	Enabled Inputs	V_{in}	V_{out}	I_{Sink}	I_{Source}
0	0	1	1	1-2	3mV	≤0.4V	16mA	
0	0	1	1	1-2	-3mV	≥2.4V		-400μA
0	0	1	1	2-1	3mV	≥2.4V		-400μA
0	0	1	1	2-1	-3mV	≤0.4V	16mA	
1	0	1	1	3-4	3mV	≤0.4V	16mA	
1	0	1	1	3-4	-3mV	≥2.4V		-400μA
1	0	1	1	4-3	3mV	≥2.4V		-400μA
1	0	1	1	4-3	-3mV	≤0.4V	16mA	
1	1	1	1	5-6	3mV	≤0.4V	16mA	
1	1	1	1	5-6	-3mV	≥2.4V		-400μA
1	1	1	1	6-5	3mV	≥2.4V		-400μA
1	1	1	1	6-5	-3mV	≤0.4V	16mA	
0	1	1	1	7-8	3mV	≤0.4V	16mA	
0	1	1	1	7-8	-3mV	≥2.4V		-400μA
0	1	1	1	8-7	3mV	≥2.4V		-400μA
0	1	1	1	8-7	-3mV	≤0.4V	16mA	
X	X	X	0	X	X	≥2.4V		-400μA
X	X	0	X	X	X	≥2.4V		-400μA

TEST FIGURE AND WAVEFORMS





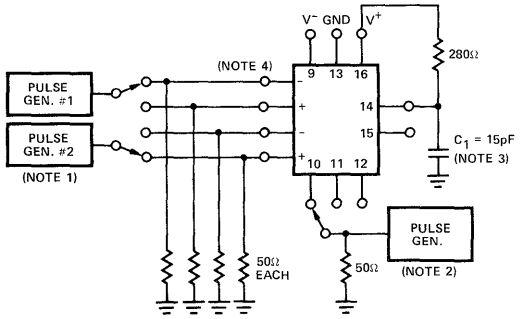
NOTES:

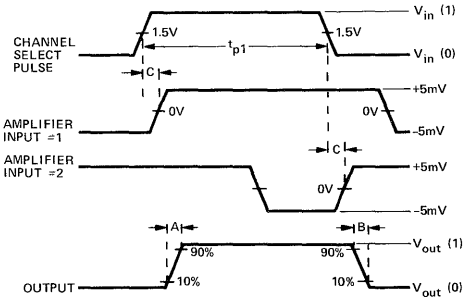
1. Pulse generators have the following characteristics: $Z_{out} = 50\Omega$, $t_r = t_f = 15\ (\pm 5)$ns, $t_{p1} = 100$ns, $t_{p2} = 300$ns, PRR = 1 MHz.
2. See channel select table on page 1.
3. C_1 includes probe and lead capacitance.
4. + and – are the input pins for the enabled channel such as (1, 2), (3, 4), (5, 6), (7, 8).

NOTES:

1. A is propagation delay t_{pd} (0)
2. B is propagation delay t_{pd} (1)
3. C is strobe delay time, t_{on}
4. D is strobe delay time, t_{off}
5. E is total disable to enable time
6. F is enable to total disable time

FIGURE 2





A is output rise time
B is output fall time
C is channel select time

NOTES:

1. Pulse generators have the following characteristics: $Z_{out} = 50\Omega$, $t_r = t_f = 15\ (\pm 5)$ns, $t_{p1} = 100$ns, PRR = 1 MHz.
2. See channel select table on page 1.
3. C_1 includes probe and lead capacitance.
4. + and – are the input pins for the enabled channel such as (1, 2), (3, 4), (5, 6), (7, 8).

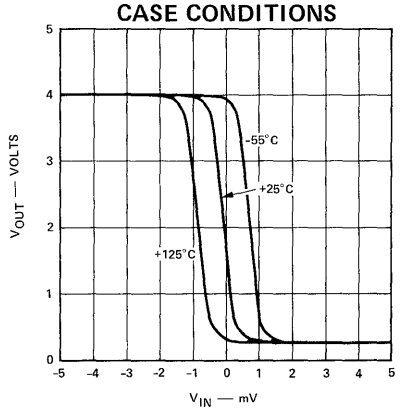
NOTES:

1. Channel select time is further defined as the minimum time between the 1.5V level of the channel select pulse and the 50% level of the input signal that allows for a full width output.
2. A is output rise time, B is output fall time, and C is channel select time.

FIGURE 3

TYPICAL CHARACTERISTIC CURVE

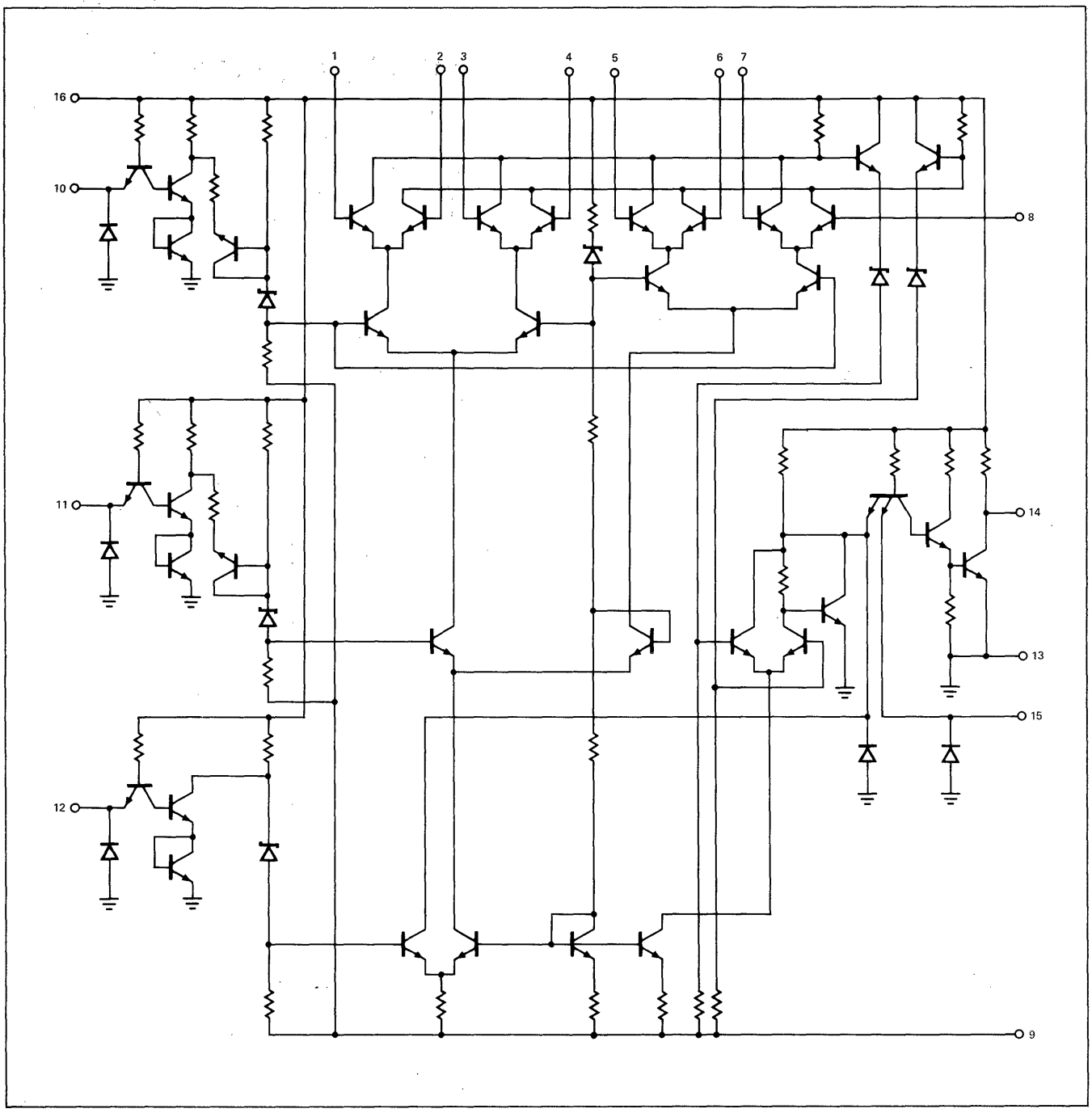
TYPICAL TRANSFER CHARACTERISTICS OVER TEMPERATURE UNDER WORST CASE CONDITIONS



CONDITIONS:

1. $V^+ = 4.75V$, $V^- = -5.70V$
2. $I_{source} = 400\mu A$ for $V_{out} > 2.4V$
3. $I_{sink} = 16mA$ for $V_{out} < 0.4V$

EQUIVALENT SCHEMATIC DIAGRAM



signetics DUAL CORE SENSE MEMORY AMPLIFIERS

LINEAR INTEGRATED CIRCUITS

SN7520
SN7521
SN7522
SN7523
SN7524
SN7525

DESCRIPTION

The 7520 Series Dual Core Memory Sense Amplifiers are designed for use in high speed core memory systems. Three separate logic configurations allow flexibility of system design.

The 7520 and 7521 can be used to perform the function of a flip-flop or a data register which responds to the sense and strobe-input conditions.

The 7522 and 7523 features an open collector stage which may be used to perform the wired-OR function.

The 7524 and 7525 features two independent sense channels with separate outputs.

FEATURES

- DUAL SENSE AMPS
- ±4mV THRESHOLD UNCERTAINTY
- DESIGN VERSATILITY
- 25ns PROPAGATION DELAY

ABSOLUTE MAXIMUM RATINGS

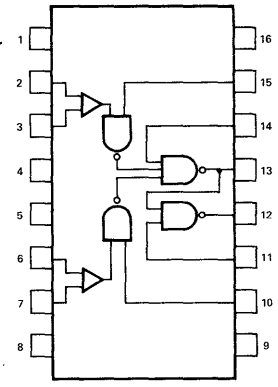
Differential Input Voltage	±5V
V_{CC}	±7V
Strobe & Gain Input Voltages	+5.5V
Storage Temperature	-65°C to +150°C
Operating Temperature	0°C to +70°C
Power Dissipation	500mW

PIN CONFIGURATIONS

B PACKAGE (Top View)

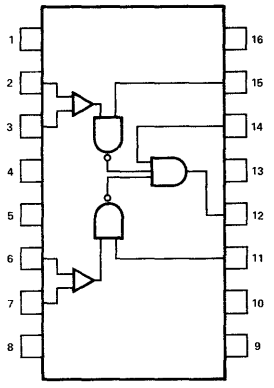
7520/21

ORDER PART NOS. SN7520N/ SN7521N



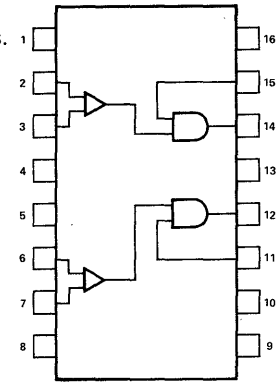
7522/23

ORDER PART NOS. SN7522N/ SN7523N



7524/25

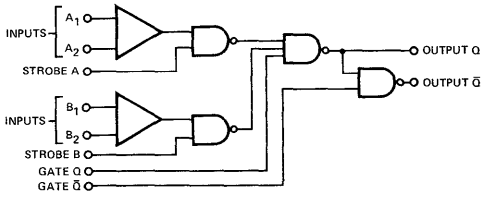
ORDER PART NOS. SN7524N/ SN7525N



*The Signetics 7520/21/22/23/24/25 does not require an external capacitor (C_{ext}) to stabilize the pre-amplifier. Pin 1 may be used as a test point, giving access to the pre-amplifier output. No degradation of performance will result if a 100pF capacitor is connected from Pin 1 to GND.

LOGIC DIAGRAMS

7520/21



Output $Q = G_Q + (S_A\ IN_A + S_B\ IN_B)\ G_Q$

Output $Q = G_Q\ (G_Q + S_A\ IN_A + S_B\ IN_B)$

where:

G_Q = Gate Q ⩾ 2V

S_A = Strobe A ⩾ 2V

IN_A = (V_{inD} at Inputs A_1 and A_2) > V_T

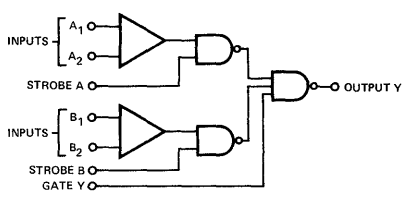
S_B = Strobe B ⩾ 2V

IN_B = (V_{inD} at Inputs B_1 and B_2) > V_T

G_Q = Gate Q ⩽ 0.8V

G_Q = Gate Q ⩾ 2V

7522/23



Output $Y = G(S_A\ IN_A + S_B\ IN_B) + G$

where:

G = Gate ⩾ 2V

S_A = Strobe A ⩾ 2V

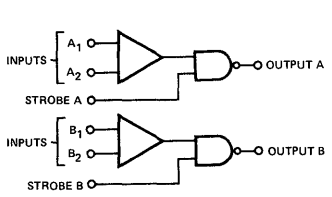
IN_A = (V_{inD} at Inputs A_1 and A_2) > V_T

S_B = Strobe B ⩾ 2V

IN_B = (V_{inD} at Inputs B_1 and B_2) > V_T

G = Gate ⩽ 0.4V

7524/25



Output $A = S_A\ IN_A$

Output $B = S_B\ IN_B$

where:

S_A = Strobe A ⩾ 2V

IN_A = (V_{inD} at Inputs A_1 and A_2) > V_T

S_B = Strobe B ⩾ 2V

IN_B = (V_{inD} at Inputs B_1 and B_2) > V_T

ELECTRICAL CHARACTERISTICS (V_{cc1} = 5V, V_{cc2} = -5V, T_A = 0°C to +70°C, unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNITS
V_T	Differential-Input Threshold Voltage (See Note 1)	V_{ref} = 15mV	7520	11	15	18	mV
			7521	8	15	22	mV
		V_{ref} = 40mV	7520	36	40	44	mV
			7521	33	40	47	mV
V_{CMF}	Common-Mode Input Firing Voltage (See Note 2)	Strobe Input: $V_{inS} = V_{in(1)}$ Common-Mode Input Pulse: $t_r = t_f \leqslant 15ns$, $t_{p(in)}$ = 50ns T_A = 25°C			±3		V
I_{in}	Differential-Input Bias Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V V_{inD} = 0mV			30	75	μA
I_{DI}	Differential-Input Offset Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V			0.5		μA
z_{inD}	Differential-Input Impedance	f = 1 kHz			2		kΩ
$V_{in(1)}$	Logical 1 Input Voltage (gate and strobe inputs)	V_{cc1} = 4.75V, V_{cc2} = -4.75V $V_{in(0)}$ = 0.8V		2			V
$V_{in(0)}$	Logical 0 Input Voltage (gate	V_{cc1} = 4.75V, V_{cc2} = -4.75V $V_{in(1)}$ = 2V				0.8	V
$I_{in(0)}$	Logical 0 Level Input Current (gate and strobe inputs)	V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(0)}$ = 0.4V				-1.6	mA
$I_{in(1)}$	Logical 1 Level Input Current (gate and strobe inputs)	V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(1)}$ = 2.4V				40	μA
		V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(1)} = V_{cc1}$				1	mA
$V_{out(1)}$	Logical 1 Output Voltage	V_{cc1} = 4.75V, V_{cc2} = -4.75V I_{load} = -400μA		2.4	3.9		V
$V_{out(0)}$	Logical 0 Output Voltage	V_{cc1} = 4.75V, V_{cc2} = -4.75V I_{sink} = 16mA			0.25	0.4	V
$I_{OS(Q)}$	Q Output Short-Circuit Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V		3.3		5	mA
$I_{OS(\overline{Q})}$	$\overline{Q}$ Output Short-Circuit Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V		2.1		3.5	mA
I_{cc1}	V_{cc1} Supply Current	T_A = 25°C			28		mA
I_{cc2}	V_{cc2} Supply Current	T_A = 25°C			-14		mA
$t_{or\ D}$	Differential-Input Overload Recovery Time (See Note 3)	V_{inD} = 2V, $t_r = t_f$ = 20ns			20		ns
$t_{or\ CM}$	Common-Mode Input Overload Recovery Time (See Note 4)	V_{inCM} = 2V, $t_r = t_f$ = 20ns			20		ns
$t_{cyc(min)}$	Minimum cycle time				200		ns

PROPAGATION DELAY TIMES			MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT				
$t_{pd(1)DQ}$, $t_{pd(0)DQ}$	$A_1 - A_2$ or $B_1 - B_2$	Q		20	40	ns
				30		ns
$t_{pd(1)D\overline{Q}}$, $t_{pd(0)D\overline{Q}}$	$A_1 - A_2$ or $B_1 - B_2$	$\overline{Q}$		25		ns
				35	55	ns
$t_{pd(1)SQ}$, $t_{pd(0)SQ}$	Strobe A or B	Q		15	30	ns
				25		ns
$t_{pd(1)S\overline{Q}}$, $t_{pd(0)S\overline{Q}}$	Strobe A or B	$\overline{Q}$		15		ns
				35	55	ns
$t_{pd(1)G_QQ}$, $t_{pd(0)G_QQ}$	Gate Q	Q		10	20	ns
				15		ns
$t_{pd(1)G_Q\overline{Q}}$, $t_{pd(0)G_Q\overline{Q}}$	Gate Q	$\overline{Q}$		15		ns
				20	30	ns
$t_{pd(1)G_Q\overline{Q}}$, $t_{pd(0)G_Q\overline{Q}}$	Gate $\overline{Q}$	$\overline{Q}$		15		ns
				10	20	ns

(SEE NOTES PAGE 128)

ELECTRICAL CHARACTERISTICS (V_{cc1} = 5V, V_{cc2} = -5V, T_A = 0°C to +70°C, unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_T	Differential Input Threshold Voltage (See Note 1)	V_{ref} = 15mV	7522	11	15	19	mV
			7523	8	15	22	mV
		V_{ref} = 40mV	7522	36	40	44	mV
			7523	33	40	47	mV
V_{CMF}	Common Mode Input Firing Voltage (See Note 2)	Strobe Input: $V_{inS} = V_{in(1)}$ Common Mode Input Pulse: $t_r = t_f \geqslant 15$ns, $t_{p(in)}$ = 50ns T_A = 25°C			±3		V
I_{in}	Differential Input Bias Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V V_{inD} = 0mV			30	75	μA
I_{DI}	Differential Input Offset Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V			0.5		μA
z_{inD}	Differential Input Impedance	f = 1 kHz			2		kΩ
$V_{in(1)}$	Logical 1 Input Voltage (gate and strobe inputs)	V_{cc1} = 4.75V, V_{cc2} = -4.75V $V_{in(0)}$ = 0.8V		2			V
$V_{in(0)}$	Logical 0 Input Voltage (gate and strobe inputs)	V_{cc1} = 4.75V, V_{cc2} = -4.75V $V_{in(1)}$ = 2V				0.8	V
$I_{in(0)}$	Logical 0 Level Input Current (gate and strobe inputs)	V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(0)}$ = 0.4V			-1	-1.6	mA
$I_{in(1)}$	Logical 1 Level Input Current (gate and strobe inputs)	V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(1)}$ = 2.4V				40	μA
		V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(1)} = V_{cc1}$				1	mA
$V_{out(1)}$	Logical 1 Output Voltage	V_{cc1} = 4.75V, V_{cc2} = -4.75V I_{load} = -400μA, V_{in} = 2V		2.4	3.9		V
$V_{out(0)}$	Logical 0 Output Voltage	V_{cc1} = 4.75V, V_{cc2} = -4.75V I_{sink} = 16mA, V_{in} = 0.8V			0.2	0.4	V
$I_{out(1)}$	Output Reverse Current	V_{cc1} = 4.75V, V_{cc2} = -4.75V V_{out} = 5.25V, V_{in} = 2V				250	μA
I_{OS}	Output Short Circuit Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V		2.1		3.5	mA
I_{cc1}	V_{cc1} Supply Current	T_A = 25°C			27		mA
I_{cc2}	V_{cc2} Supply Current	T_A = 25°C			15		mA
$t_{or D}$	Differential Input Overload Recovery Time (See Note 3)	V_{inD} = 2V, $t_r = t_f$ = 20ns			20		ns
$t_{or CM}$	Common Mode Input Overload Recovery Time (See Note 4)	V_{inCM} = ±2V, $t_r = t_f$ = 20ns			20		ns
$t_{cyc(min)}$	Minimum Cycle Time				200		ns

PROPAGATION DELAY TIMES			MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT				
$t_{pd(1)D}$	$A_1 - A_2$ or $B_1 - B_2$	Y		20		ns
$t_{pd(0)D}$				30	45	ns
$t_{pd(1)S}$	Strobe A or B	Y		15		ns
$t_{pd(0)S}$				25	40	ns
$t_{pd(1)G}$	Gate	Y		10		ns
$t_{pd(0)G}$				15	25	ns

(SEE NOTES PAGE 128)

ELECTRICAL CHARACTERISTICS (V_{cc1} = 5V, V_{cc2} = -5V, T_A = 0°C to +70°C, unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_T	Differential Input Threshold Voltage (See Note 1)	V_{ref} = 15mV	7524	11	15	19	mV
			7525	8	15	22	mV
		V_{ref} = 40mV	7524	36	40	44	mV
			7525	33	40	47	mV
		Strobe Input: $V_{inS} = V_{in(1)}$					
V_{CMF}	Common Mode Input Firing Voltage (See Note 2)	Common Mode Input Pulse: $t_r = t_f \leqslant 15ns$, $t_{p(in)}$ = 50ns T_A = 25°C			±3		V
I_{in}	Differential Input Bias Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V V_{inD} = 0mV			30	75	μA
I_{DI}	Differential Input Offset Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V			0.5		μA
z_{inD}	Differential Input Impedance	f = 1 kHz			2		kΩ
$V_{in(1)}$	Logical 1 Input Voltage (strobe inputs)	V_{cc1} = 4.75V, V_{cc2} = -4.75V $V_{in(0)}$ = 0.8V		2			V
$V_{in(0)}$	Logical 0 Input Voltage (strobe inputs)	V_{cc1} = 4.75V, V_{cc2} = -4.75V $V_{in(1)}$ = 2V				0.8	V
$I_{in(0)}$	Logical 0 Level Input Current (strobe inputs)	V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(0)}$ = 0.4V			-1	-1.6	mA
$I_{in(1)}$	Logical 1 Level Input Current (strobe inputs)	V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(1)}$ = 2.4V				40	μA
		V_{cc1} = 5.25V, V_{cc2} = -5.25V $V_{in(1)} = V_{cc1}$				1	mA
$V_{out(1)}$	Logical 1 Output Voltage	V_{cc1} = 4.75V, V_{cc2} = -4.75V I_{load} = -400μA, $V_{in(1)}$ = 2V $V_{in(0)}$ = 0.8V		2.4	3.9		V
$V_{out(0)}$	Logical 0 Output Voltage	V_{cc1} = 4.75V, V_{cc2} = -4.75V I_{sink} = 16mA, $V_{in(0)}$ = 0.8V			0.25	0.4	V
I_{OS}	Output Short Circuit Current	V_{cc1} = 5.25V, V_{cc2} = -5.25V		2.1		3.5	mA
I_{cc1}	V_{cc1} Supply Current	T_A = 25°C			25		mA
I_{cc2}	V_{cc2} Supply Current	T_A = 25°C			-15		mA
$t_{\text{or D}}$	Differential Input Overload Recovery Time (See Note 3)	V_{inD} = 2V, $t_r = t_f$ = 20ns			20		ns
$t_{\text{or CM}}$	Common Mode Input Overload Recovery Time (See Note 4)	V_{inCM} = ±2V, $t_r = t_f$ = 20ns			20		ns
$t_{cyc(min)}$	Minimum Cycle Time				200		ns

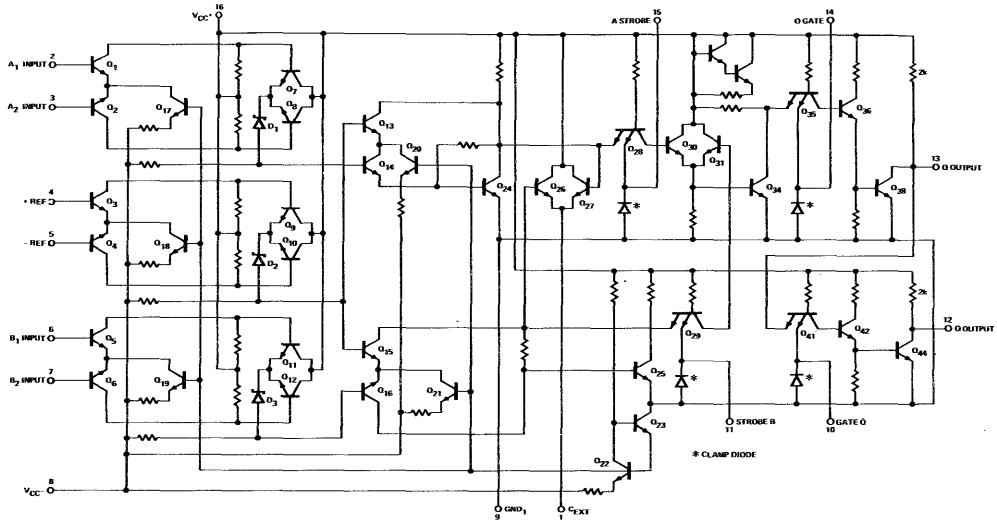
PROPAGATION DELAY TIMES			MIN	TYP	MAX	UNIT
SYMBOL	FROM INPUT	TO OUTPUT				
$t_{pd(1)D}$	$A_1 - A_2$ or $B_1 - B_2$	A or B		25	40	ns
$t_{pd(0)D}$				20		ns
$t_{pd(1)S}$	Strobe A or B	A or B		15	30	ns
$t_{pd(0)S}$				20		ns

NOTES:

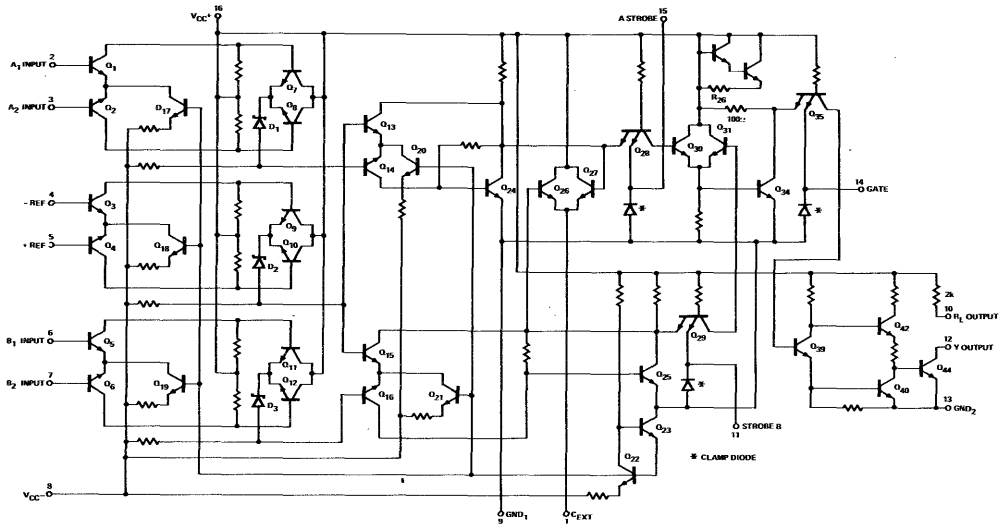
1. The differential input threshold voltage (V_T) is defined as the DC input voltage (V_{in}) required to force the output of the sense amplifier to the logic gate threshold voltage level.
2. Common mode input firing voltage is the common mode voltage that will exceed the dynamic range of the input at the specified conditions and cause the logic output to switch. The specified common mode input signal is applied with a strobe enable signal present.
3. Differential input overload recovery time is the time necessary for the device to recover from the specified differential input overload signal prior to the strobe enable signal.
4. Common mode input overload recovery time is the time necessary for the device to recover from the specified common mode input overload signal prior to the strobe enable signal.

SCHEMATIC DIAGRAMS

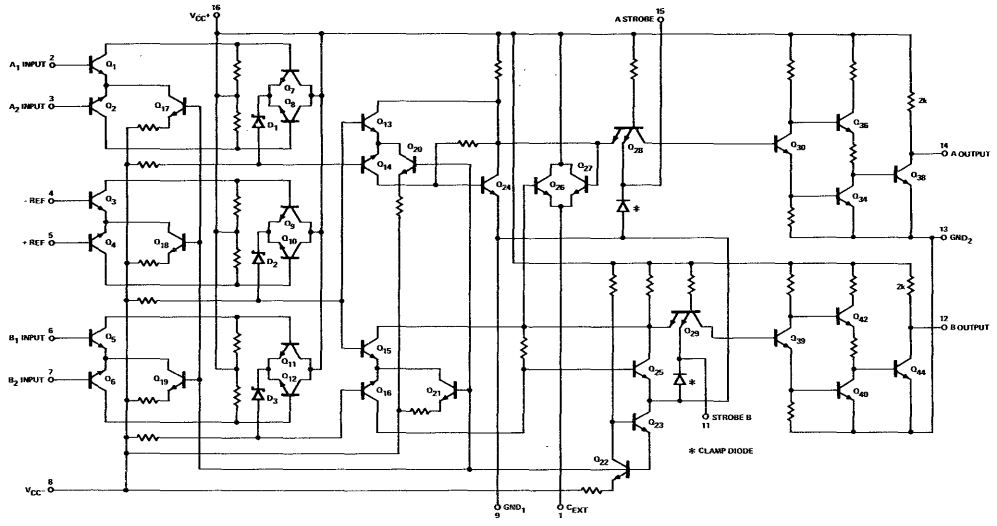
7520/21



7522/23

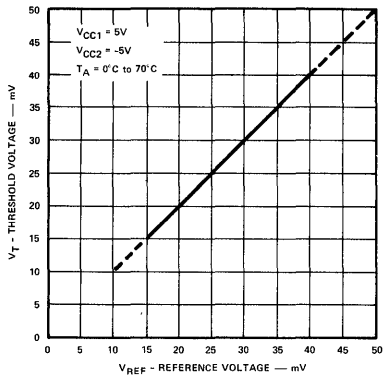


7524/25

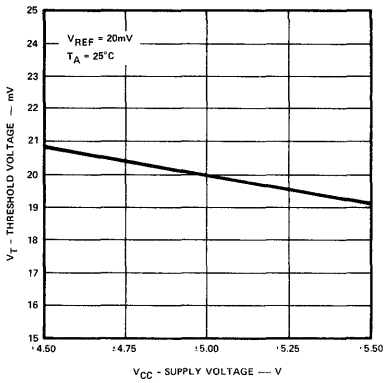


TYPICAL CHARACTERISTIC CURVES

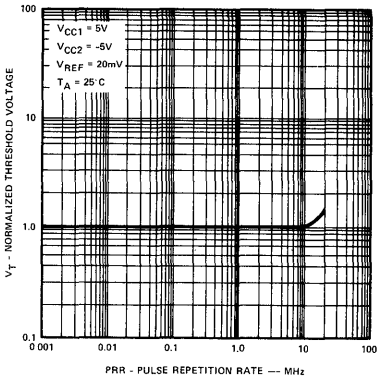
THRESHOLD VOLTAGE VERSUS REFERENCE VOLTAGE



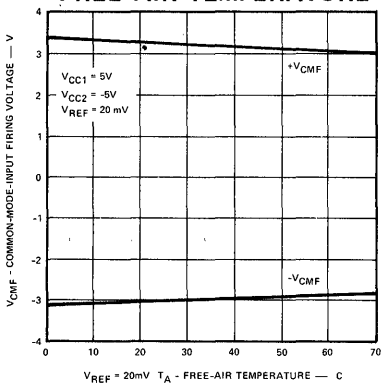
THRESHOLD VOLTAGE VERSUS SUPPLY VOLTAGE



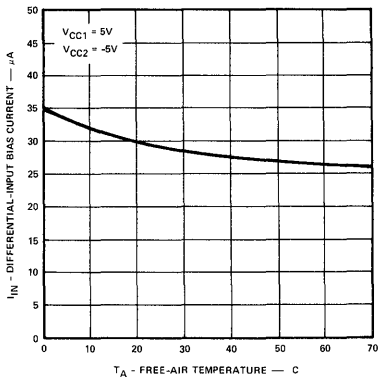
NORMALIZED THRESHOLD VOLTAGE VERSUS PULSE REPETITION RATE



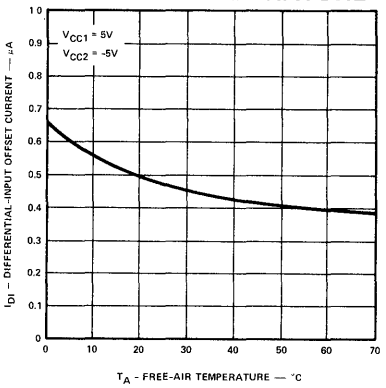
COMMON-MODE FIRING VOLTAGE VERSUS FREE-AIR TEMPERATURE



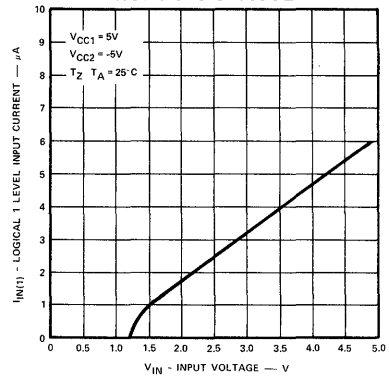
DIFFERENTIAL-INPUT BIAS CURRENT VERSUS FREE-AIR TEMPERATURE



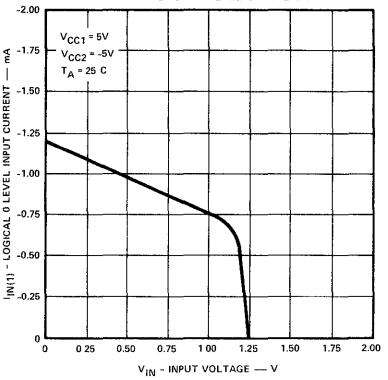
DIFFERENTIAL-INPUT OFFSET CURRENT VS FREE-AIR TEMPERATURE



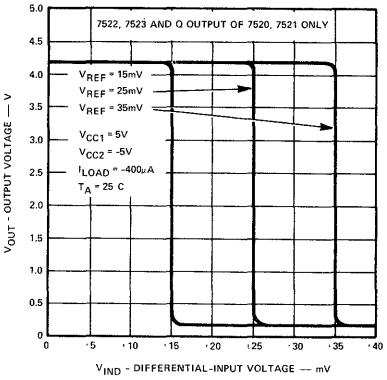
LOGICAL 1 LEVEL INPUT CURRENT VERSUS INPUT VOLTAGE



LOGICAL 0 LEVEL INPUT CURRENT VERSUS INPUT VOLTAGE

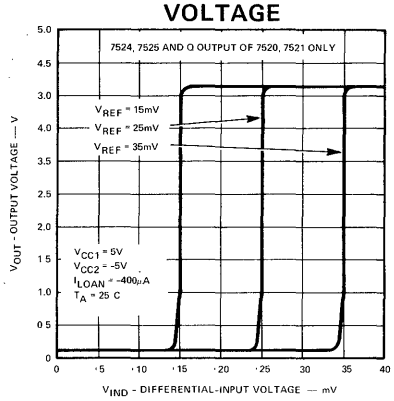


OUTPUT VOLTAGE VERSUS DIFFERENTIAL-INPUT VOLTAGE

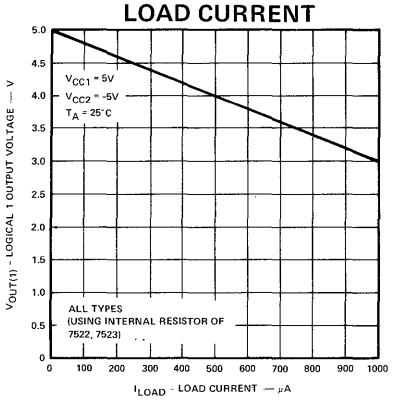


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

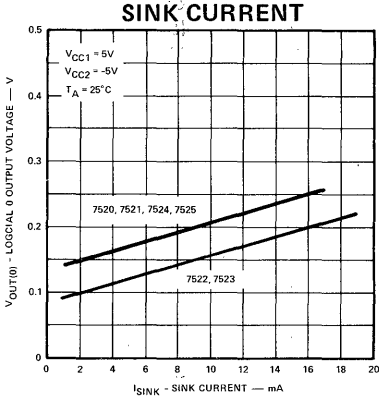
OUTPUT VOLTAGE VERSUS DIFFERENTIAL-INPUT VOLTAGE



LOGICAL 1 OUTPUT VOLTAGE VERSUS LOAD CURRENT



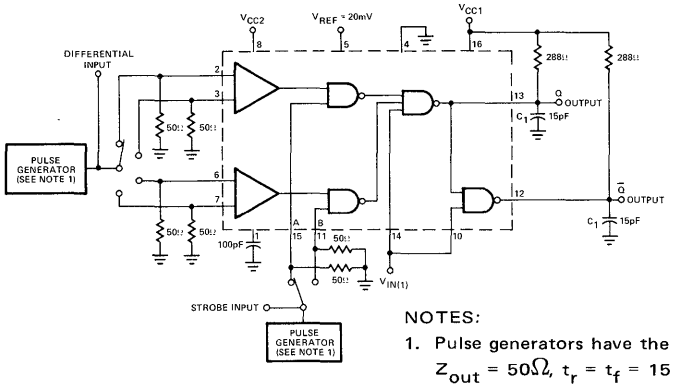
LOGICAL 0 OUTPUT VOLTAGE VERSUS SINK CURRENT



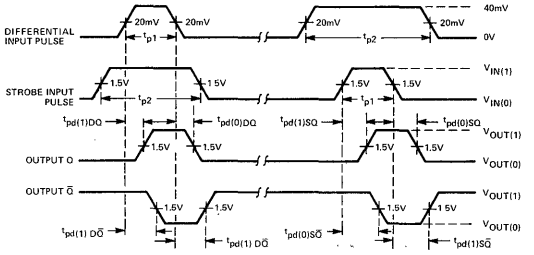
SWITCHING CHARACTERISTICS (Propagation Delay Times)

7520/21

TEST CIRCUIT – DIFFERENTIAL AND STROBE INPUTS TO OUTPUTS

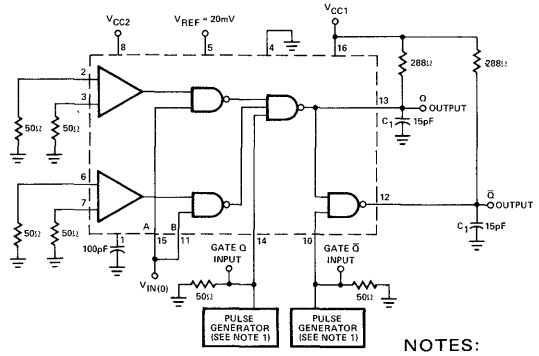


VOLTAGE WAVEFORMS – DIFFERENTIAL AND STROBE INPUTS TO OUTPUTS

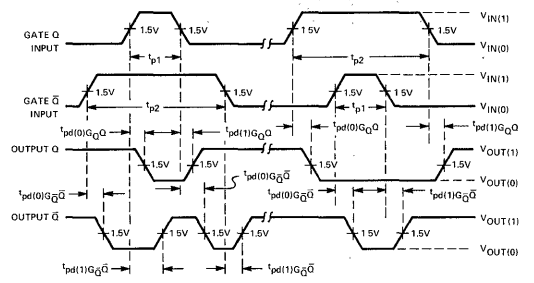


NOTES:
1. Pulse generators have the following characteristics: $Z_{out} = 50\Omega$, $t_r = t_f = 15(\pm5)$ns, $t_{p1} = 100$ns, $t_{p2} = 300$ns, and PRR = 1 MHz.
2. C_1 includes probe and jig capacitance.

TEST CIRCUIT



VOLTAGE WAVEFORMS

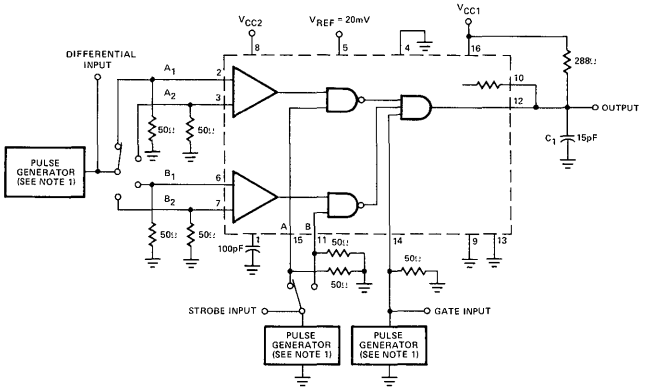


NOTES:
1. Pulse generators have the following characteristics: $Z_{OUT} = 50\Omega$, $t_r = t_f = 15(\pm5)$ns, $t_{p1} = 100$ns, $t_{p2} = 300$ns, and PRR = 1 MHz.
2. C_1 includes probe and jig capacitance.

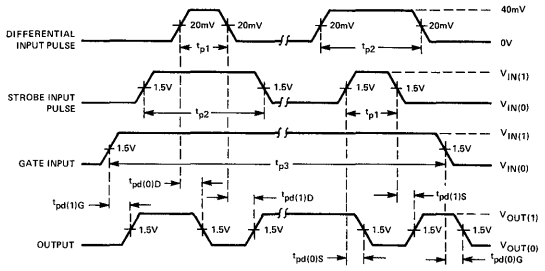
SWITCHING CHARACTERISTICS (Propagation Delay Times)(Cont'd)

7522/23

TEST CIRCUIT



VOLTAGE WAVEFORMS

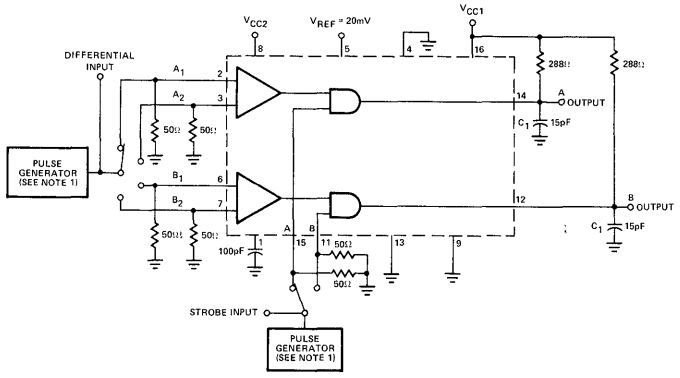


NOTES:

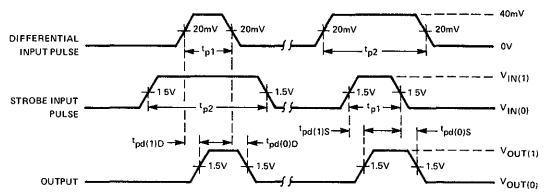
1. Pulse generators have the following characteristics:
   Z_{out} = 50Ω, t_r = t_f = 15(±5)ns, t_{p1} = 100ns,
   t_{p2} = 300ns, PRR = 1 MHz.
2. Strobe input pulse is applied to Strobe A when inputs A_1 - A_2 are being tested and to Strobe B when inputs B_1 - B_2 are being tested.
3. C_1 includes probe and jig capacitance.

7524/25

TEST CIRCUIT



VOLTAGE WAVEFORMS



NOTES:

1. Pulse generators have the following characteristics:
   Z_{out} = 50Ω, t_r = t_f = 15(±5)ns, t_{p1} = 100ns,
   t_{p2} = 300ns, PRR = 1 MHz.
2. Strobe input pulse is applied to Strobe A when inputs A_1 - A_2 are being tested and to Strobe B when inputs B_1 - B_2 are being tested.
3. C_1 includes probe and jig capacitance.

SECTION 6
communications circuits

DESCRIPTION

The Signetics NE501 is a direct-coupled broad-band amplifier fabricated within a monolithic silicon substrate by planar and epitaxial techniques. Typical applications include video amplifiers.

Application flexibility is provided by several external pin connections which adjust the amplifier characteristics to individual needs.

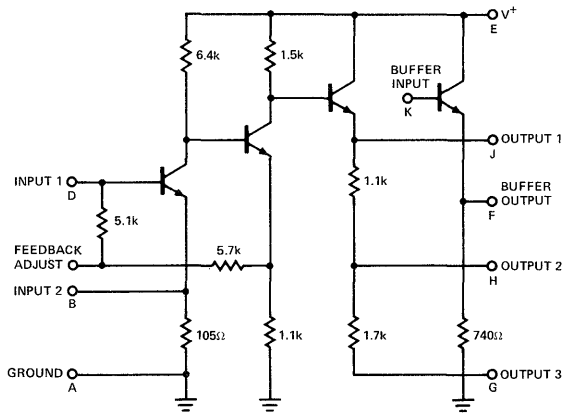
FEATURES

- ADJUSTABLE GAIN AND IMPEDANCE CHARACTERISTICS
- UNITY GAIN FREQUENCY – 150 MHz
- NOISE FIGURE – 5.0dB
- POWER DISSIPATION – 20mW

ABSOLUTE MAXIMUM RATINGS

Voltage Applied $V_{G,H,E,C}$		+8.0V
Voltage Applied V_B		±3.0V
Voltage Applied $V_{K,D}$		+4.0V
Current Rating $I_{F,J}$		±30mA
Storage Temperature		-65°C to +150°C
Operating Temperature	NE501	0°C to +70°C
	SE501	-55°C to +125°C

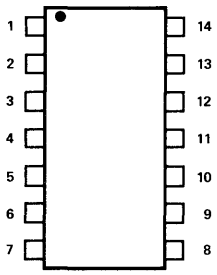
CIRCUIT SCHEMATIC



NOTE: Component values are typical.

PIN CONFIGURATIONS

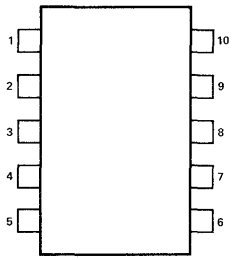
A PACKAGE
(Top View)



ORDER PART NOS.
SE501A/NE501A

1. Feedback adjust
2. Input 1
3. NC
4. NC
5. Output 3
6. Input 2
7. Ground
8. Output 2
9. V^+
10. NC
11. NC
12. Buffer output
13. Buffer input
14. Output 1

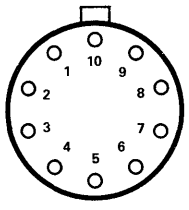
G PACKAGE



ORDER PART NOS.
SE501G/NE501G

1. Ground
2. Output 3
3. Input 2
4. Output 2
5. V^+
6. Buffer output
7. Buffer input
8. Output 1
9. Feedback adjust
10. Input 1

K PACKAGE



ORDER PART NOS.
SE501K/NE501K

1. Ground
2. Output 3
3. Input 2
4. Output 2
5. V^+
6. Buffer output
7. Buffer input
8. Output 1
9. Feedback adjust
10. Input 1

ELECTRICAL CHARACTERISTICS

PARAMETER	TEST CONDITIONS	NE501			SE501			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Voltage Gain	f = 50 kHz; Notes 1, 2, 6	22.5	24	26.5	23	24	26	dB
Bandwidth (-3dB)	Notes 1, 2, 6	11			14			MHz
Unity Gain Frequency	A_{Vo} = 0dB; Notes 2, 6	100	150		100	150		MHz
Voltage Gain Stability	f = 50 kHz; T = 0°C; Notes 2, 6	-1.0						dB
	f = 50 kHz; T = +70°C; Notes 2, 6			+0.6				dB
	f = 50 kHz; T = -55°C; Notes 2, 6				-1.0			dB
	f = 50 kHz; T = +125°C; Notes 2, 6						+0.6	dB
Output Voltage	Notes 1, 2, 6, 9	0.71	1.0		0.71	1.0		V_{RMS}
Input Impedance	Notes 1, 6; f = 50 kHz; $V_J = V_K$	470		1200	540		1100	Ω
Output Impedance	Notes 1, 2; f = 50 kHz; V_D = AC ground		12	18		12	18	Ω
Output Impedance	Notes 1, 5; f = 50 kHz; V_D = AC ground		25	65		25	50	Ω
Power Dissipation				24			21	mW
Power Dissipation	$V_K = V_J$			60			53	mW
Pulse Response								
Delay Time	Notes 2, 6, 7			15			15	ns
Rise Time	Notes 2, 6, 7		12	20		12	16	ns
Noise Figure	f = 100 kHz; BW = 100 Hz; Z_s = 500Ω		5.0	8.0				dB
	f_c = 100 kHz, BW = 100 Hz; Z_s = 500Ω, $V_J = V_K$					5.0	7.0	dB

(Notes: 3, 4, 5, 8) Standard Conditions: V_E = +6.0V, V_A = 0V, $V_G = V_B$, T = +25°C (except as noted)

NOTES:

1. Variations in this parameter depend on optional alternate connections as indicated in accompanying curves.
2. Measured at Pin F, with Pins J and K connected.
3. Pins not specifically referenced are left electrically open. All voltages are referenced to Pin A. Letter subscripts denote pins on circuit schematic.
4. Positive current flow is defined as into the terminal referenced.
5. Measured at Pin J.
6. Load Resistance = 600Ω, capacitively coupled.
7. Delay time is defined as the time interval between the 50% points of e_D and e_F. Rise time = 20% to 80% points of e_F. Input Pulse Characteristics: Amplitude = 25mV; PW = 100ns.
8. See Signetics SURE Program Bulletin No. 5001 for definition of Acceptance test Sub-Groups. Sub-Group A-7 is used for the electrical end points for Linear Products.
9. Total harmonic distortion less than 5% at e_o = 0.71 V_{RMS}.

DESCRIPTION

The SE/NE592 is a monolithic, two stage, differential input, differential output, wideband video amplifier. It offers fixed gains of 100 and 400 without external components and adjustable gains from 400 to 0 with one external resistor. The input stage has been designed so that with the addition of a few external reactive elements between the gain select terminals, the circuit can function as a high pass, low pass, or band pass filter. This feature makes the circuit ideal for use as a video or pulse amplifier in communications, magnetic memories, display and video recorder systems.

FEATURES

- **120 MHz BANDWIDTH**
- **ADJUSTABLE GAINS FROM 0 TO 400**
- **ADJUSTABLE PASS BAND**
- **NO FREQUENCY COMPENSATION REQUIRED**

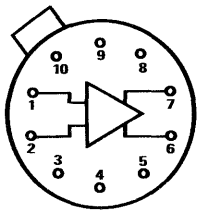
ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±8V
Differential Input Voltage	±5V
Common Mode Input Voltage	±6V
Output Current	10mA
Operating Temperature Range	
SE592K	-55°C to +125°C
NE592K	0°C to + 70°C
Storage Temperature Range	-65°C to +150°C

CONNECTION DIAGRAM

K PACKAGE

(Top View)

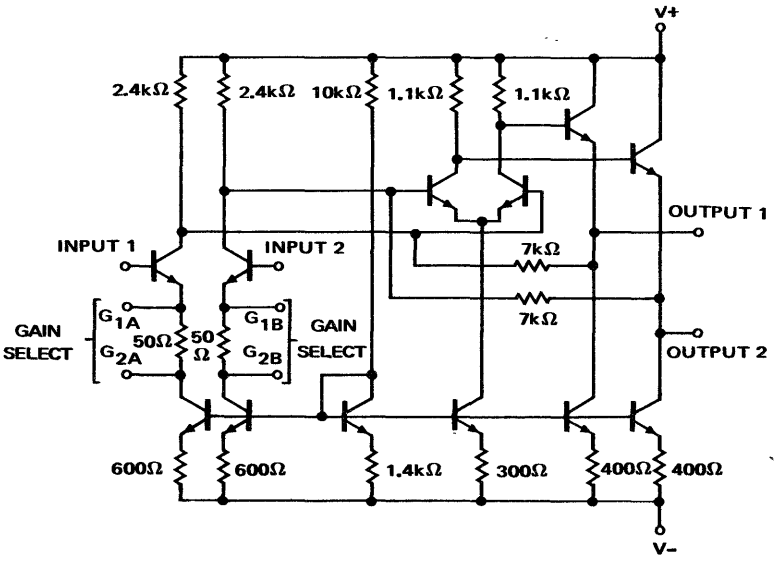


1. Input 1
2. Input 2
3. Gain Select G_{2B}
4. Gain Select G_{1B}
5. V^-
6. Output 2
7. Output 1
8. V^+
9. Gain Select G_{1A}
10. Gain Select G_{2A}

NOTE: Pin 5 connected to case.

ORDER PART NOS. SE592K/NE592K

EQUIVALENT CIRCUIT



DESCRIPTION

The 733 is a monolithic differential input, differential output, wideband video amplifier. It offers fixed gains of 10,100 or 400 without external components, and adjustable gains from 10 to 400 by the use of an external resistor. No external frequency compensation components are required for any gain option. Gain stability, wide bandwidth and low phase distortion are obtained through use of the classic series-shunt feedback from the emitter follower outputs to the inputs of the second stage. The emitter follower outputs provide low output impedance, and enable the device to drive capacitive loads. The 733 is intended for use as a high performance video and pulse amplifier in communications, magnetic memories, display and video recorder systems.

FEATURES

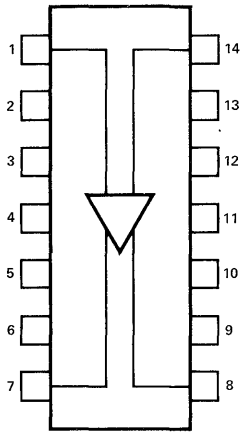
- **120 MHz BANDWIDTH**
- **250kΩ INPUT RESISTANCE**
- **SELECTABLE GAINS OF 10,100 and 400**
- **NO FREQUENCY COMPENSATION REQUIRED**

ABSOLUTE MAXIMUM RATINGS

Differential Input Voltage	±5V
Common Mode Input Voltage	±6V
V_{CC}	±8V
Output Current	10mA
Junction Temperature	+150°C
Storage Temperature Range	-65°C to +150°C
Operation Temperature Range	
μA733C	0°C to +75°C
μA733	-55°C to +75°C

PIN CONFIGURATIONS

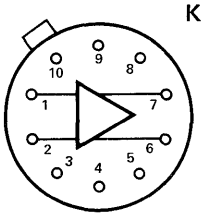
A & F PACKAGE



1. Input 2
2. NC
3. G_{2B} Gain Select
4. G_{1B} Gain Select
5. V^-
6. NC
7. Output 2
8. Output 1
9. NC
10. V^+
11. G_{1A} Gain Select
12. G_{2A} Gain Select
13. NC
14. Input 1

ORDER PART NOS.
μA733A/ μA733F/
μA733CA/ μA733CF

K PACKAGE



1. Input 1
2. Input 2
3. G_{2B} Gain Select
4. G_{1B} Gain Select
5. V^-
6. Output 2
7. Output 1
8. V^+
9. G_{1A} Gain Select
10. G_{2A} Gain Select

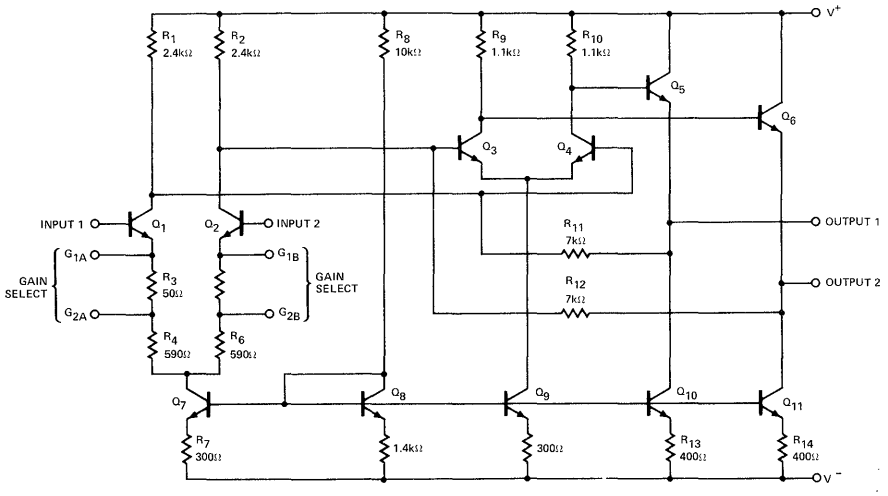
NOTE: Pin 5 connected to case.

ORDER PART NOS.
μA733K/μA733CK

Thermal Resistance (θ_{J-A}, Junction to Ambient for each package):

A Package	0.16°C/mW
F Package	0.10°C/mW
K Package	0.145°C/mW
Power Dissipation	500mW

BASIC CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS Standard Conditions (T_A = +25°C, V_S = ±V, V_{CM} = 0 unless otherwise specified)

PARAMETERS	TEST CONDITIONS		μA733C			μA733			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
Differential Voltage Gain									
Gain 1		Note 1	250	400	600	300	400	500	
Gain 2	R_l = 2kΩ, V_{out} = $3V_{p-p}$	Note 2	80	100	120	90	100	110	
Gain 3		Note 3	8.0	10	12	9.0	10	11	
Bandwidth									
Gain 1		Note 1		40			40		MHz
Gain 2		Note 2		90			90		MHz
Gain 3		Note 3		120			120		MHz
Rise Time									
Gain 1		Note 1		10.5			10.5		ns
Gain 2	V_{out} = $1V_{p-p}$	Note 2		4.5	12		4.5	10	ns
Gain 3		Note 3		2.5			2.5		ns
Propagation Delay									
Gain 1		Note 1		7.5			7.5		ns
Gain 2	V_{out} = $1V_{p-p}$	Note 2		6.0	10		6.0	10	ns
Gain 3		Note 3		3.6			3.6		ns
Input Resistance									
Gain 1		Note 1		4.0			4.0		kΩ
Gain 2		Note 2	10	30		20	30		kΩ
Gain 3		Note 3		250			250		kΩ
Input Capacitance	Gain 2	Note 2		2.0			2.0		pF
Input Offset Current				0.4	5.0		0.4	3.0	μA
Input Bias Current				9.0	30		9.0	20	μA
Input Noise Voltage	BW = 1 kHz to 10 MHz			12			12		μV_{rms}
Input Voltage Range			±1.0			±1.0			V
Common Mode Rejection Ratio									
Gain 2	V_{CM} = ±1V, f ⩽ 100 kHz		60	86		60	86		dB
Gain 2	V_{CM} = ±1V, F = 5 MHz			60			60		dB
Supply Voltage Rejection Ratio									
Gain 2	ΔV_S = ±0.5V		50	70		50	70		dB
Output Offset Voltage									
Gain 1	R_L = ∞	Note 1		0.6	1.5		0.6	1.5	V
Gain 2 and 3		Notes 2,3		0.35	1.5		0.35	1.0	V
Output Common Mode Voltage	R_L = ∞		2.4	2.9	3.4	2.4	2.9	3.4	V
Output Voltage Swing	R_L = 2k		3.0	4.0		3.0	4.0		
Output Sink Current			2.5	3.6		2.5	3.6		mA
Output Resistance				20			20		Ω
Power Supply Current	R_L = ∞			18	24		18	24	mA

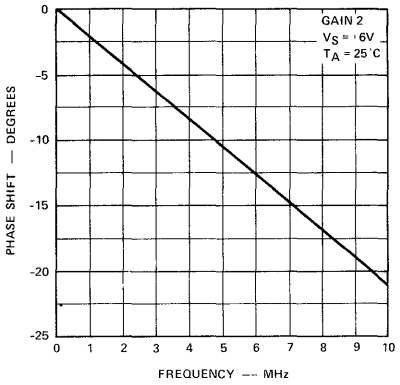
Recommended Operating Supply Voltages (V_S = ±6.0V)

NOTES
1. Gain select pins G_{1A} and G_{1B} connected together.
2. Gain select pins G_{2A} and G_{2B} connected together.
3. All gain select pins open.

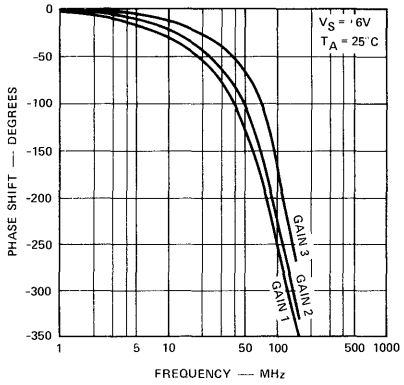
TEST CIRCUITS (T_A = 25°C unless otherwise specified)

TYPICAL CHARACTERISTIC CURVES

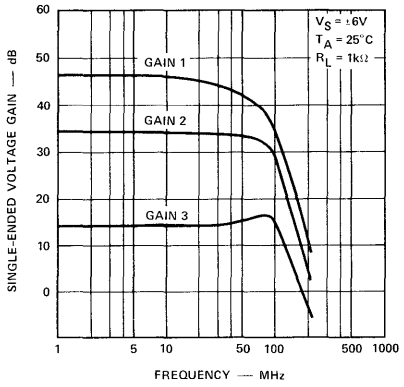
PHASE SHIFT AS A FUNCTION OF FREQUENCY



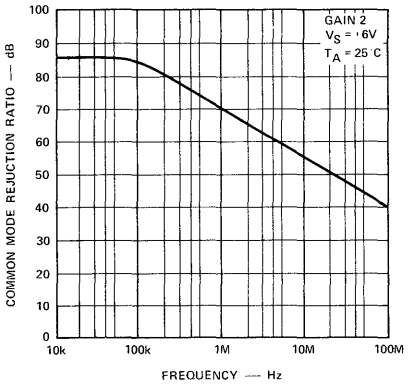
PHASE SHIFT AS A FUNCTION OF FREQUENCY



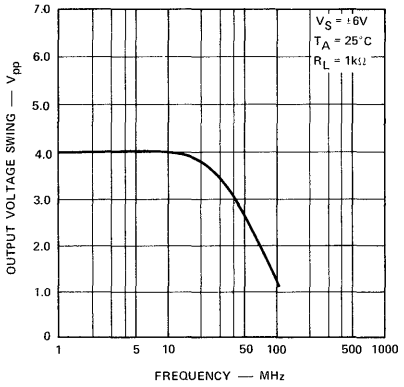
VOLTAGE GAIN AS A FUNCTION OF FREQUENCY



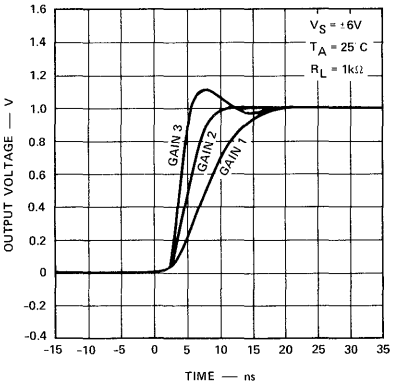
COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY



OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

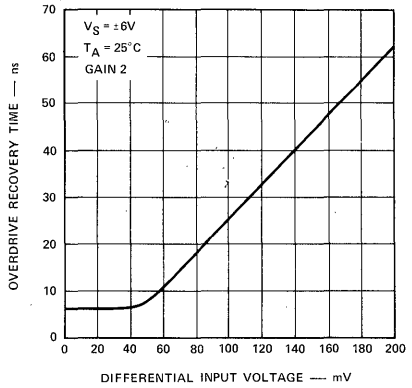


PULSE RESPONSE

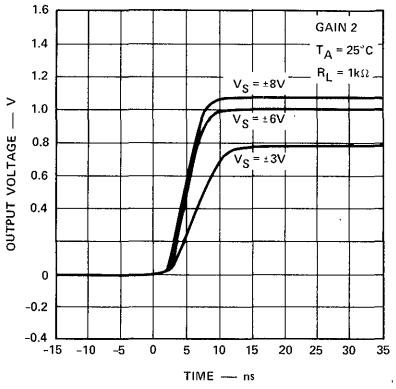


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

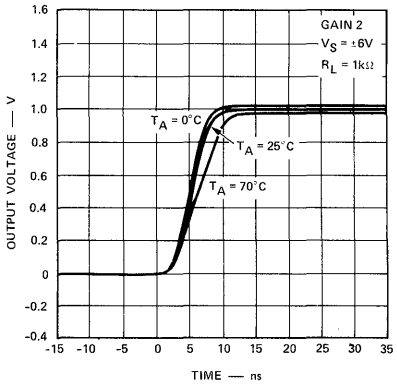
DIFFERENTIAL OVERDRIVE RECOVERY TIME



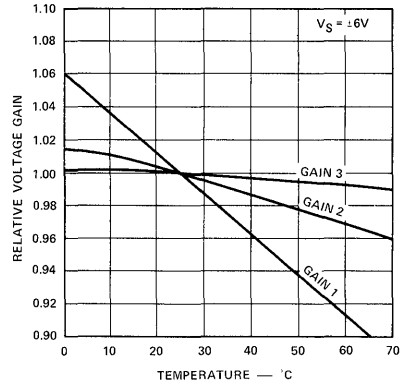
PULSE RESPONSE AS A FUNCTION OF SUPPLY VOLTAGE



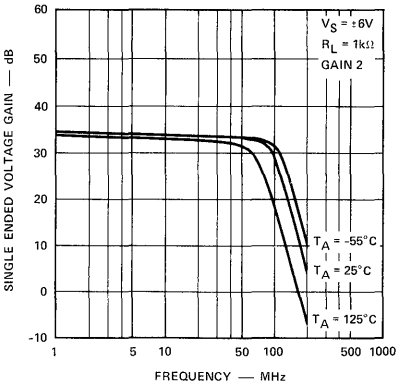
PULSE RESPONSE AS A FUNCTION OF TEMPERATURE



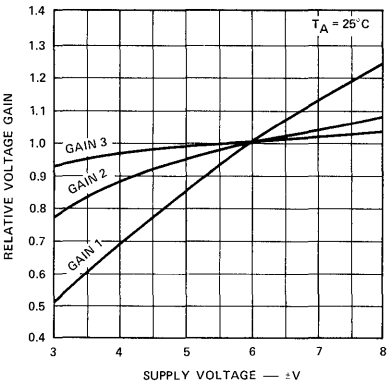
VOLTAGE GAIN AS A FUNCTION OF TEMPERATURE



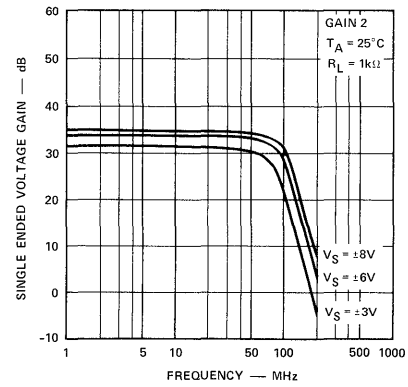
GAIN VS FREQUENCY AS A FUNCTION OF TEMPERATURE



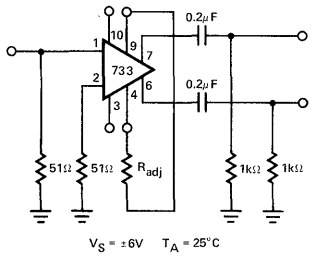
VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE



GAIN VS FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE



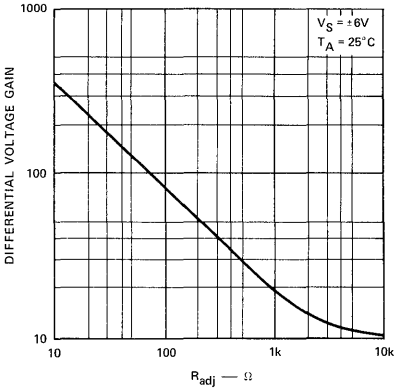
VOLTAGE GAIN ADJUST CIRCUIT



(Pin numbers apply to K Package)

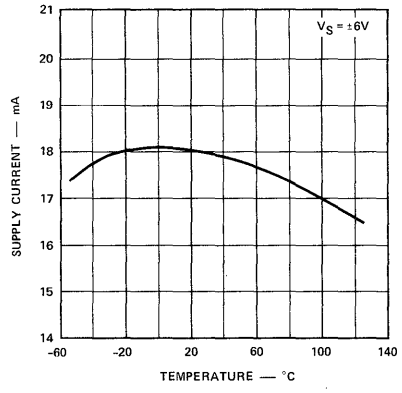
FIGURE 3

VOLTAGE GAIN AS A FUNCTION OF R_{ADJ} (FIGURE 3)

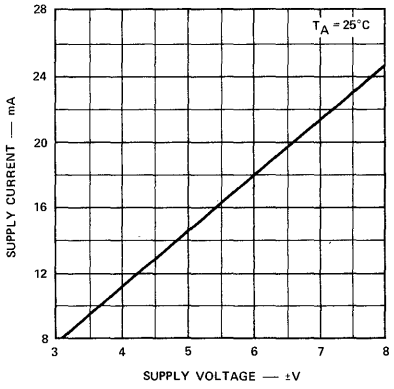


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

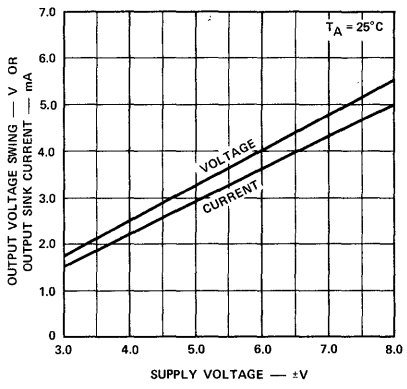
SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE



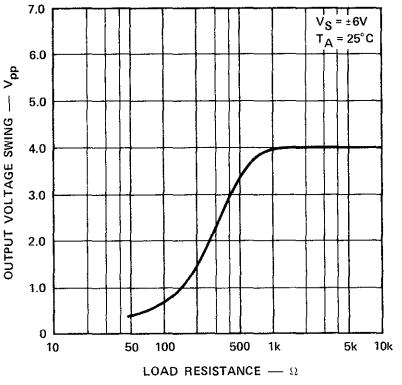
SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



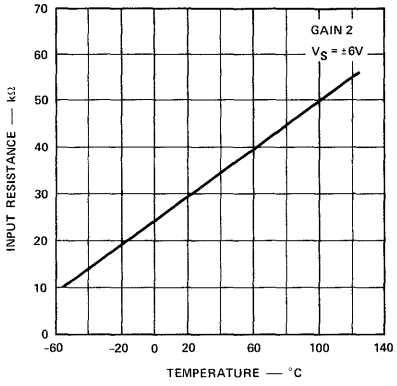
OUTPUT VOLTAGE AND CURRENT SWING AS A FUNCTION OF SUPPLY VOLTAGE



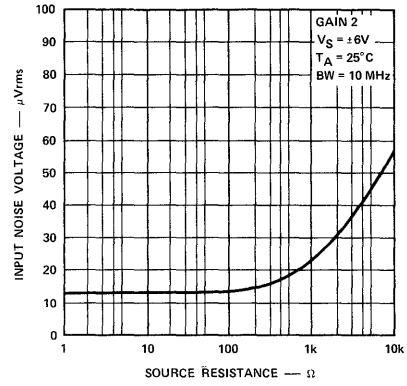
OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE



INPUT RESISTANCE AS A FUNCTION OF TEMPERATURE



INPUT NOISE VOLTAGE AS A FUNCTION OF SOURCE RESISTANCE



DESCRIPTION

The 511 is a monolithic dual high frequency differential amplifier with associated constant current source transistors and biasing diode. It is useful from DC to 100 MHz. The circuit arrangement provides for connection as two completely independent emitter coupled (differential) or cascode amplifiers. The bias diode allows stabilization of the current source currents over a large temperature range.

FEATURES

- LOW INPUT OFFSET VOLTAGE = ±2mV
- LOW INPUT OFFSET CURRENT = ±3μA
- AGC CAPABILITY
- HIGH FORWARD TRANSADMITTANCE
- LOW FEEDBACK CAPACITANCE
- SINGLE POWER SUPPLY

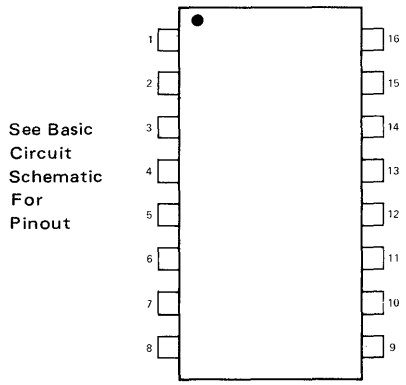
ABSOLUTE MAXIMUM RATINGS

Applied Voltage (V+)	20V
Output Collector Voltage	25V
Current (All Pins)	±15mA
Storage Temperature	-65°C to +150°C
Operating Temperature	
SE511R, SE511B	-55°C to +125°C
NE511B, NE511R	0°C to +75°C
Junction Temperature	150°C

Maximum ratings are limiting values above which serviceability may be impaired.

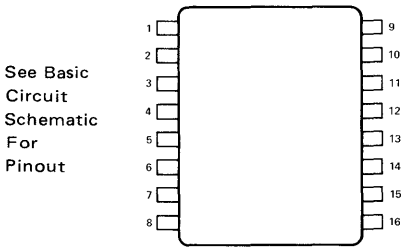
PIN CONFIGURATIONS

B PACKAGE
(Top View)



ORDER PART NOS. SE511B/NE511B

R PACKAGE

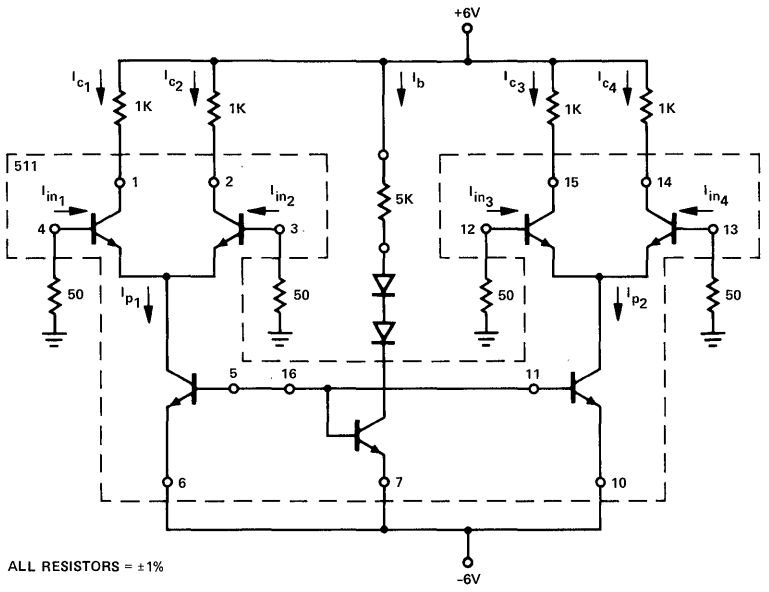


ORDER PART NOS. SE511R/NE511R

ELECTRICAL CHARACTERISTICS (Standard Test Circuit)

ACCEPTANCE TEST SUBGROUP	PARAMETERS	SYMBOL	LIMITS						UNITS	TEMPERATURE	TEST CONDITIONS
			MIN		TYP		MAX				
			SE511	NE511	SE511	NE511	SE511	NE511			
A-3	Input Offset Voltage	ΔV_{in}			0.5	0.5	2	3	mV	+25°C	
A-4		ΔV_{in}				1.0		4.0		0°C to +75°C	
A-5		ΔV_{in}			1.5		3.5			-55°C to +125°C	
A-3	Input Offset Current	ΔI_{in}			2.0	2.0	3.5	6	μA	+25°C	
A-4		ΔI_{in}				2.5		9		0°C to +75°C	
A-5		ΔI_{in}			2.5		7.5			-55°C to +125°C	
A-3	Input Bias Current	I_{in}			8.0	8.0	20	25	μA	+25°C	
A-4		I_{in}				10.0		40		0°C to +75°C	
A-5		I_{in}			16.0		40			-55°C to +125°C	
A-3	Differential Collector Current	ΔI_c			45	45	62.5	75	μA	+25°C	V_{in} = 0;
A-4	per differential pair	ΔI_c				50		100		0°C to +75°C	I_p = 2mA
A-5		ΔI_c			50		100			-55°C to +125°C	
A-3	Differential Current in the	ΔI_p			30	30	62.5	75	μA	+25°C	
A-4	Current Sources	ΔI_p				35		100		0°C to +75°C	
A-5		ΔI_p			35		100			-55°C to +125°C	
A-2	Total Current	I_{cc}			11.0	11.0	15.0	15.0	mA	+25°C	
A-3	Common Mode Rejection Ratio	CMRR	60	60	80	80			dB	+25°C	
A-3	Output Conductance	G_{22}			0.01	0.01			mmho	+25°C	
C-2	Output Capacitance	C_{ob}			2.5	2.5			pF	+25°C	
C-2	Input Capacitance	C_{ib}			10	10			pF	+25°C	

STANDARD TEST CIRCUIT



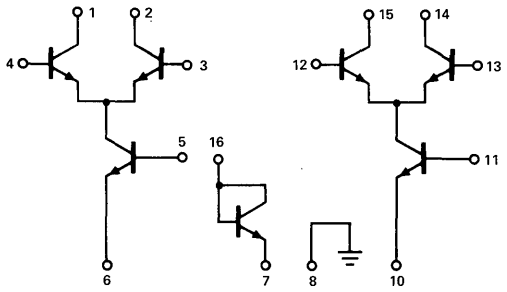
$\Delta I_{in} = I_{in_1} - I_{in_2}$ or $I_{in_3} - I_{in_4}$

$\Delta I_c = I_{c_1} - I_{c_2}$ or $I_{c_3} - I_{c_4}$

$\Delta I_p = I_{p_1} - I_{p_2}$

$I_{cc} = I_{c_1} + I_{c_2} + I_{c_3} + I_{c_4} + I_b$

BASIC CIRCUIT SCHEMATIC



DESCRIPTION

The 515 is a general purpose high-gain amplifier with differential input and output. It is fabricated within a monolithic silicon substrate by planar and epitaxial techniques. A pair of compensation points is provided to allow frequency compensation for stable closed loop operation.

This device is not internally referenced to ground and with proper input bias may be operated from a single power supply.

FEATURES

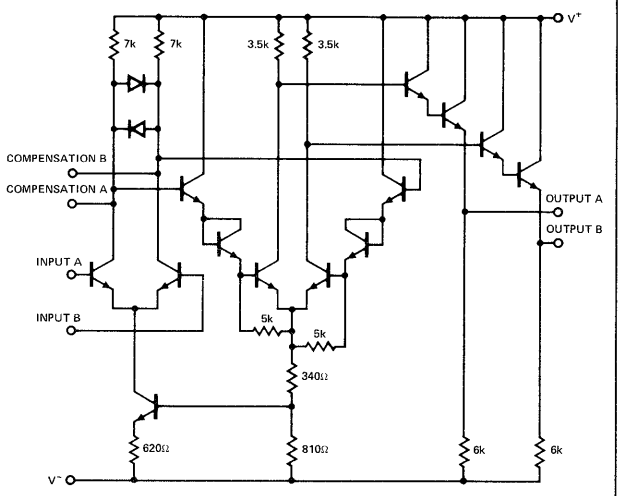
- **DIFFERENTIAL VOLTAGE GAIN (Open Loop) = 4,500**
- **INPUT OFFSET VOLTAGE = 0.5mV**
- **INPUT OFFSET VOLTAGE STABILITY = 5.0μV/°C**
- **INPUT COMMON MODE RANGE = +1.5V, -1.0V**
- **COMMON MODE REJECTION RATIO = 100dB**
- **BANDWIDTH (Open Loop) = 1.0 MHz**

ABSOLUTE MAXIMUM RATINGS

Applied Voltage (V+ to V-)	12V
Differential Input Voltage (V_5 to V_7)	±5.0V
Input Current (I_5, I_7)	±2.0mA
Output Current (I_2, I_{10})	±30mA
Storage Temperature	-65°C to +150°C
Operating Temperature	0°C to +75°C
Junction Temperature	150°C

Maximum ratings are limiting values above which serviceability may be impaired.

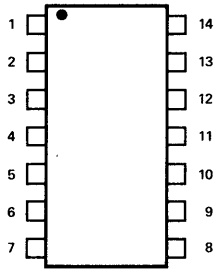
EQUIVALENT CIRCUIT



NOTE: Component values are typical.

PIN CONFIGURATIONS

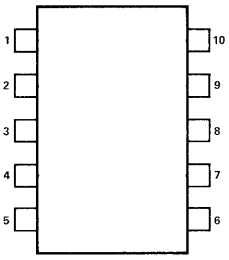
A PACKAGE
(Top View)



1. Input B
2. NC
3. NC
4. Compensation
5. NC
6. Output B
7. V^-
8. Output A
9. NC
10. NC
11. Compensation
12. NC
13. Input A
14. V^+

ORDER PART NO. NE515A

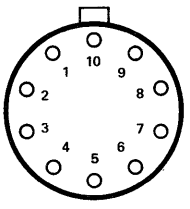
G PACKAGE



1. V^-
2. Output A
3. NC
4. Compensation
5. Input A
6. V^+
7. Input B
8. Compensation
9. NC
10. Output B

ORDER PART NOS. SE515G/NE515G

K PACKAGE



1. V^-
2. Output A
3. NC
4. Compensation
5. Input A
6. V^+
7. Input B
8. Compensation
9. NC
10. Output B

ORDER PART NOS. SE515K/NE515K

SE515 ELECTRICAL CHARACTERISTICS (Standard Conditions: V_7 = 0V, V_1 = -3.0V; Notes: 4, 5, 6, 7, 8, 9)

CHARACTERISTIC	V_6 = +4.0V	V_6 = +6.0V			UNITS	TEMP	TEST CONDITIONS
	TYP	MIN	TYP	MAX			
Open Loop Voltage Gain (dc)	2,500	3,500	4,500		V/V	+25°C	Note 2
	1,800		3,000		V/V	+125°C	
Open Loop Voltage Gain (ac)	2,000	2,500	3,500		V/V	+25°C	f = 800 kHz
Input Offset Voltage	0.5		0.5	3.0	mV	-55°C	Note 1
	0.5		0.5	2.0	mV	+25°C	
	0.5		0.5	3.0	mV	+125°C	
Input Bias Current	18		25	40	μA	-55°C	Note 1
	12		16	24	μA		
Differential Input Resistance	2.0	1.0	1.5		kΩ	-55°C	Note 10
	4.0	2.0	3.2		kΩ	+25°C	
Input Common Mode Range	±1.0		+1.5		V	+25°C	
			-1.0				
Balanced Output dc Level	-0.1		+1.2		V	-55°C	Note 1
	+0.3		+1.6	+1.8	V	+25°C	
	+0.6		+1.9		V	+125°C	
Output Voltage Swing	4.7	5.7	6.3		V	-55°C	Note 3
	4.7	5.7	6.3		V	+25°C	
	4.7	5.7	6.3		V	+125°C	
High Output Level	+2.3	+4.0	+4.3		V	-55°C	V_5 = 10mV
	+2.6	+4.3	+4.6		V	+25°C	
	+3.0	+4.7	+5.0		V	+125°C	
Low Output Level	-2.4	-1.7	-2.0		V	-55°C	V_5 = 10mV
	-2.1	-1.4	-1.7		V	+25°C	
	-1.7	-1.0	-1.3		V	+125°C	
Output Resistance	100		100		Ω	+25°C	Note 1
Common Mode Rejection Ratio	100		100		dB		
Power Supply Current				7.0	mA		Note 1
	3.5		5.5	7.0	mA		
				7.0	mA		

NOTES:

1. Adjust V_5 to obtain $V_2 = V_{10}$.
2. Output voltage swing = 1.3V peak to peak.
3. Output voltage swing is guaranteed by output voltage limit tests.
4. Voltage and current subscripts refer to pin numbers.
5. All measurements are referenced to power supply common. Positive current flow is defined as into the terminal indicated.
6. All specifications herein apply for interchange of voltages and currents at Pins 5 and 7.
7. Acceptance Test Sub-Group references apply to minimum and maximum limits only.
8. The SE515K has Pins 1, 3 and 9 connected to the case. The SE515G has Pins 3 and 9 open.
9. See Signetics SURE Program Bulletin No. 5001 for definition of Acceptance Test Sub-Groups. Sub-Group A-7 is used for electrical end points for Linear Products.
10. Differential Input Resistance is computed from input bias current.

NE515 ELECTRICAL CHARACTERISTICS (Standard Conditions: V_B = 0V, V_A = 3.0V; Notes: 4, 5, 6, 7, 8, 9)

CHARACTERISTIC	V_F = +4.0V	V_F = +6.0V			UNITS	TEMP	TEST CONDITIONS
	TYP	MIN	TYP	MAX			
Open Loop Voltage Gain (dc)	1,800	2,500	3,200		V/V	+25°C	Note 2
	1,350		2,200		V/V	+75°C	
Open Loop Voltage Gain (ac)	1,500	1,700	2,500		V/V	+25°C	f = 800 kHz
Input Offset Voltage	0.5		0.5	4.0	mV	0°C	Note 1
	0.5		0.5	3.0	mV	+25°C	
	0.5		0.5	4.0	mV	+75°C	
Input Bias Current	18		25	40	μA	0°C	Note 1
	15		20	31	μA	+25°C	
Differential Input Resistance	3.2	1.4	2.3		kΩ	0°C	Note 10
	3.5	1.7	2.6		kΩ	+25°C	
Input Common Mode Range	±1.0		+1.5		V	+25°C	
			-1.0				
Balanced Output dc Level	-0.1		+1.2		V	0°C	Note 1
	+0.3		+1.6	+1.8	V	+25°C	
	+0.6		+1.9		V	+75°C	
Output Voltage Swing	4.5	5.3	6.1		V	0°C	Note 3
	4.5	5.3	6.1		V	+25°C	
	4.5	5.3	6.1		V	+75°C	
High Output Level	+2.3	+3.9	+4.3		V	0°C	V_C = 10mV
	+2.5	+4.1	+4.5		V	+25°C	
	+2.8	+4.3	+4.8		V	+75°C	
Low Output Level	-2.2	-1.4	-1.8		V	0°C	V_C = 10mV
	-2.0	-1.2	-1.6		V	+25°C	
	-1.7	-1.0	-1.3		V	+75°C	
Output Resistance	100		100		Ω	+25°C	Note 1
Common Mode Rejection Ratio	100		100		dB	+25°C	
Power Supply Current				7.0	mA	0°C	Note 1
	3.5		5.5	7.0	mA	+25°C	
				7.0	mA	+75°C	

Letter subscripts refer to pins on circuit schematic.

NOTES:

1. Adjust V_C to obtain $V_G = V_H$.
2. Output voltage swing = 1.3V peak to peak.
3. Output voltage swing is guaranteed by output voltage limit tests.
4. Voltage and current subscripts refer to pin numbers.
5. All measurements are referenced by power supply common. Positive current flow is defined as into the terminal indicated.
6. All specifications herein apply for interchange of voltages and currents at Pins B and C.
7. Acceptance Test Sub-Group references apply to minimum and maximum limits only.
8. The NE515K has Pins 1, 3 and 9 connected to the case. The NE515G has Pins 3 and 9 open.
9. See Signetics SURE Program Bulletin No. 5001 for definition of Acceptance Test Sub-Groups. Sub-Group A-7 is used for electrical end points for Linear Products.
10. Differential Input Resistance is computed from input bias current.

DESCRIPTION

The 510 is a dual high-frequency differential amplifier with associated constant current sources and biasing elements contained within a silicon monolithic epitaxial substrate. The large number of accessable internal points provide extreme flexibility of application. The 510 is intended for RF-IF amplifier service to beyond 100 MHz. Circuit layout provides for connection as either a high-gain, common-emitter, common-base, cascode amplifier or a common-collector, common-base, differential amplifier that is useful in critical limiter applications. Automatic gain control may be applied to either circuit.

The SE510J and SE510A meet or exceed the mechanical and environmental requirements of MIL-S-19500 over the temperature range of -55°C to +125°C.

The NE510A and NE510J are intended for industrial applications over the temperature range of 0°C to +75°C.

FEATURES

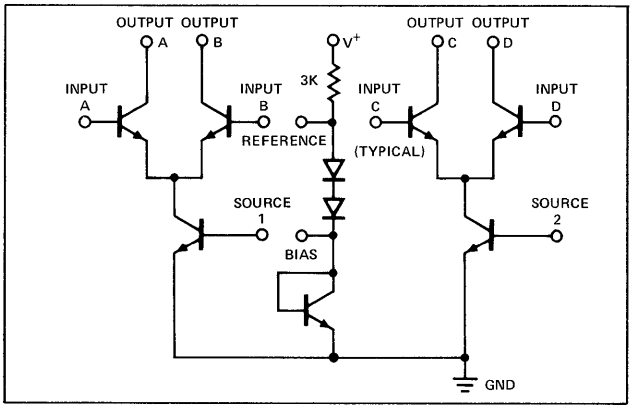
- **LOW INPUT OFFSET VOLTAGE = ±2mV**
- **LOW INPUT OFFSET CURRENT = ±3μA**
- **SINGLE POWER SUPPLY**
- **AGC CAPABILITY**
- **HIGH FORWARD TRANSADMITTANCE**
- **LOW FEEDBACK CAPACITANCE**

ABSOLUTE MAXIMUM RATINGS

Applied Voltage (V^+)	20V
Output Collector Voltage	25V
Current (Pin K)	-25mA
Current (All Other Pins)	±15mA
Storage Temperature	-65°C to +150°C
Operating Temperature	
SE510J, SE510A	-55°C to +125°C
NE510A, NE510J	0°C to +75°C
Junction Temperature	150°C

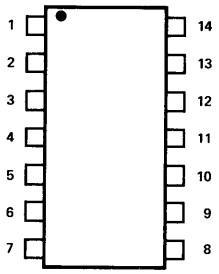
Maximum ratings are limiting values above which serviceability may be impaired.

BASIC CIRCUIT SCHEMATIC



PIN CONFIGURATIONS

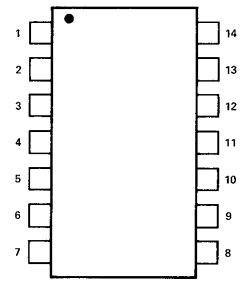
A PACKAGE
(Top View)



1. Output B
2. Output A
3. Input A
4. Input B
5. Reference
6. Source 1
7. Ground
8. Source 2
9. Bias
10. Input D
11. Input C
12. Output C
13. Output D
14. V^+

ORDER PART NOS. SE510A/NE510A

J PACKAGE



1. Input C
2. Output C
3. Output D
4. V^+
5. Output B
6. Output A
7. Input A
8. Input B
9. Reference
10. Source 1
11. Ground
12. Source 2
13. Bias
14. Input D

ORDER PART NOS. SE510J/NE510J

ELECTRICAL CHARACTERISTICS

PARAMETERS	TEMPERATURE	TEST CONDITIONS	LIMITS						UNITS
			NE510			SE510			
			MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	+25°C			0.5	3		0.5	2	mV
	0°C to +70°C			1.0	4				
	-55°C to +125°C						1.5	3.5	
Input Offset Current	+25°C			2.0	6		2.0	3.5	μA
	0°C to +70°C			2.5	9				
	-55°C to +125°C						2.5	7.5	
Input Bias Current	+25°C			8.0	25		8.0	20	μA
	0°C to +70°C			10.0	40				
	-55°C to +125°C						16.0	40	
Differential Collector Current per Differential Pair	+25°C	$V_{in} = 0$		45	75		45	62.5	μA
	0°C to +70°C			50	100				
	-55°C to +125°C						50	100	
Differential Current in the Current Sources	+25°C			30	75		30	62.5	μA
	0°C to +70°C			35	100				
	-55°C to +125°C						35	100	
Total Current	+25°C			11.0	15.0		11.0	15.0	mA
Common Mode Rejection Ratio	+25°C		60	80		60	80		dB

ELECTRICAL CHARACTERISTICS ($V^+ = +12V$, $T = 25°C$ applicable from DC to 10 MHz, unless otherwise noted)

PARAMETER	EMITTER COUPLED CONFIGURATION	CASCODE CONFIGURATION $V_{AGC} = 0V$	UNITS
Input Conductance $[R_e(Y_{11})]$	0.7	3.0	mmho
Output Conductance $[R_e(Y_{22})]$	0.01	0.01	mmho
Input Capacitance	4.5	10	pF
Output Capacitance	2.5	2.5	pF
Reverse Transfer Capacitance	0.05	0.05	pF
Forward Transconductance	25	90	mmho

signetics DUAL LOW NOISE PREAMPLIFIER PA239

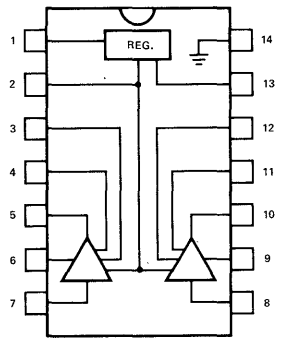
LINEAR INTEGRATED CIRCUITS

DESCRIPTION

The PA239 is a dual low noise preamplifier featuring two identically-matched 68dB gain amplifiers fed from an internal zener regulated power supply.
Operation requires only a single power supply and a minimum number of external frequency shaping components.

PIN CONFIGURATION

A PACKAGE
(Top View)



1. V+
2. Zener
3. Feedback 1
4. Roll 1
5. Out 1
6. Input Ret. 1
7. Input 1
8. Input 2
9. Input Ret. 2
10. Out 2
11. Roll 2
12. Feedback 2
13. Reg. Gnd.
14. Amp. Gnd.

ORDER PART NO.
PA239A

FEATURES

- MATCHED OPEN LOOP VOLTAGE GAIN
- LOW AUDIO NOISE
- SINGLE POWER SUPPLY
- WIDE POWER SUPPLY RANGE
- BUILT-IN POWER SUPPLY FILTER
- HIGH INPUT IMPEDANCE
- EMITTER FOLLOWER OUTPUT
- LOW DISTORTION
- SELF BIASING
- MINIMUM NUMBER OF EXTERNAL COMPONENTS
- OUTPUT CIRCUIT IS SHORT CIRCUIT PROTECTED
- HIGH CHANNEL SEPARATION
- VARIETY OF FEEDBACK OPTIONS
- NO CIRCUIT DAMAGE IF PLUGGED IN BACKWARDS
- 7.5V REGULATOR BIAS SOURCE

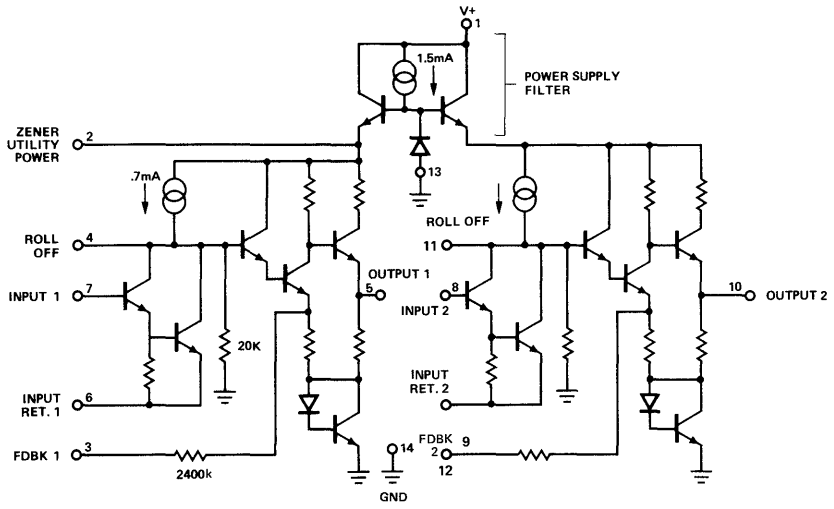
APPLICATIONS

STEREO TAPE PLAYERS/RECORDERS
DICTATING EQUIPMENT
MOVIE PROJECTORS
PHONOGRAPHS
TV REMOTE CONTROL RECEIVER
MICROPHONE AMPLIFIERS
STEREO RADIO RECEIVER SYSTEMS
VIDEO PREAMPLIFICATION
NARROW BAND AMPLIFICATION
DRIVER-PREAMP FOR LOSSY NETWORKS
SUPER GAIN CASCADED AMPLIFIERS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	16V
Temperature	
Storage	-55°C to +150°C
Operating	-30°C to +85°C

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS (25°C) (V_{CC} = 12V)

PARAMETERS	MIN	TYP	MAX	UNITS
Supply Current (V_{CC} = 12V)		16	22	mA
Voltage Gain	65	68	71	dB
Gain Balance		0.3	2	dB
Channel Separation (f = 1 kHz), Figure 1	45	90		dB
Input Resistance	100K	250K		Ω
Signal Output		1.5		Vrms
Output Resistance		100		Ω
Power Supply Rejection (f = 1 kHz), Figure 2	45	55		dB
Total Harmonic Distortion Without Feedback (0.5V rms into 3kΩ Load, 1 kHz)		0.5	0.9	%
Input dc Bias Current		0.8	3	μA
Gain to Feedback Terminal 3, 12		45		dB
Impedance at Feedback Terminal		2400		Ω
Amplifier Noise Figure (100Hz to 10 kHz, 5kΩ Rs)		1.8		dB
Equivalent Input Noise (100Hz to 10 kHz, 680Ω Rs)		0.7	1.2	μV

TEST CIRCUITS

CHANNEL SEPARATION

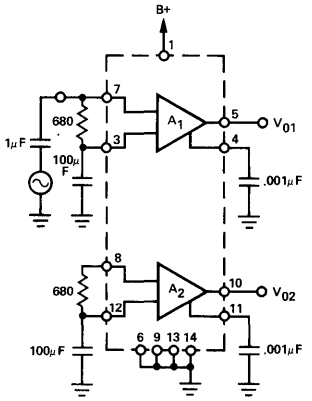


Figure 1

POWER SUPPLY REJECTION

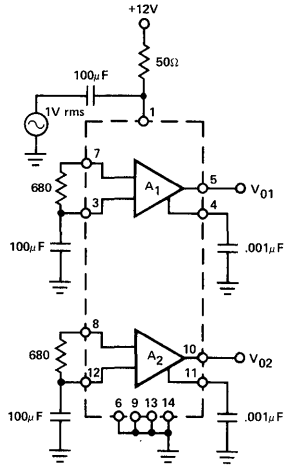


Figure 2

NOISE

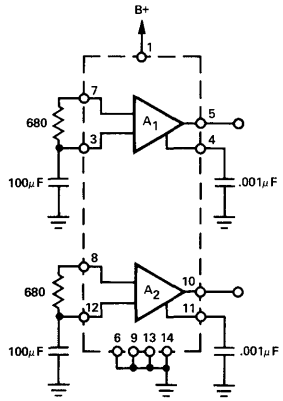


Figure 3

DESCRIPTION

The 5595 is a Monolithic Four-Quadrant Multiplier designed for uses where the output voltage is a linear product of two input voltages. The S5595F is a pin-for-pin replacement for the MC1595L and the N5595A replaces the MC1495L.

FEATURES

- **EXCELLENT LINEARITY – 1% MAX ERROR ON X-INPUT, 2% MAX ERROR ON Y-INPUT – S5595F**
- **EXCELLENT LINEARITY – 2% MAX ERROR ON X-INPUT, 4% MAX ERROR ON Y-INPUT – N5595A**
- **ADJUSTABLE SCALE FACTOR, K**
- **EXCELLENT TEMPERATURE STABILITY**
- **WIDE INPUT VOLTAGE RANGE – ±10 VOLTS**

APPLICATIONS

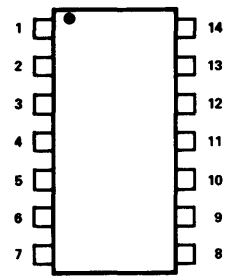
ANALOG MULTIPLICATION AND DIVISION
SQUARE ROOT OPERATION
MEAN SQUARING
PHASE DETECTION
FREQUENCY DOUBLING
BALANCED MODULATION/DEMODULATION
ELECTRONIC GAIN CONTROL

ABSOLUTE MAXIMUM RATINGS

Applied Voltage		30V
(V_2-V_1, V_{14}-V_1, V_1-V_9, V_1-V_{12}, V_1-V_4, V_1-V_8, V_{12}-V_7, V_9-V_7, V_8-V_7, V_4-V_7)		
Differential Input Signal	V_{12}-V_9	$\pm(6 + I_{13}R_X)V$
	V_4-V_8	$\pm(6 + I_3R_Y)V$

PIN CONFIGURATION

A AND F PACKAGE
(Top View)



1. V^+
2. V_{out}^+
3. Y Bias
4. +Y Input
5. Y Gain Adjust
6. Y Gain Adjust
7. V^-
8. –Y Input
9. +X Input
10. X Gain Adjust
11. X Gain Adjust
12. –X Input
13. X Bias
14. V_{out}^-

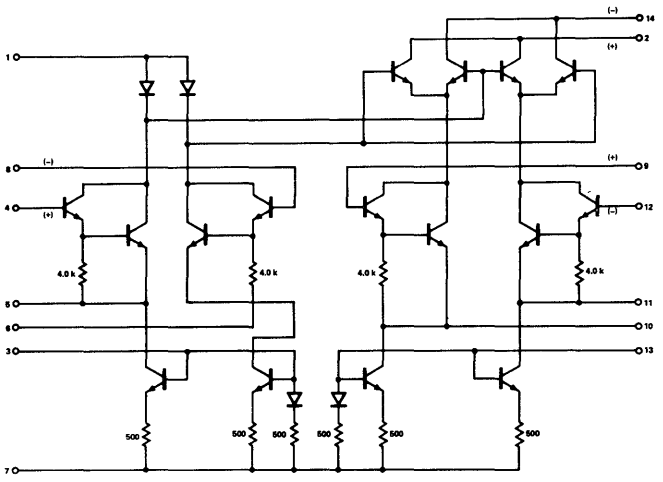
ORDER PART NOS. S5595F/N5595A

ABSOLUTE MAXIMUM RATINGS (Cont'd.)

Maximum Bias Current	I_3	10mA
	I_{13}	10mA
Power Dissipation (Note 1)		
Ceramic Package		750mW
Operating Temperature Range		
S5595F		–55°C to +125°C
N5595A		0°C to +70°C
Storage Temperature Range		–65°C to +150°C

Note 1: Derate linearly at 5mW/°C for ambient temperatures above +25°C

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS ($V^+ = +32V$, $V^- = -15V$, $T_A = 25°C$, $I_3 = I_{13} = 1$ mA, $R_X = R_Y = 15$ kΩ, $R_L = 11$ kΩ unless otherwise noted)

CHARACTERISTICS	SYMBOL	LIMITS						UNITS	TEMPERATURE	FIGURE
		MIN		TYP		MAX				
		S5595	N5595	S5595	N5595	S5595	N5595			
Linearity:										
Output Error in Percent of Full Scale:								%		1
$-10 < V_X < +10 (V_Y = \pm 10V)$	E_{RX}			0.5	1.0	1.0	2.0		+25°C	
					1.5				0°C to +70°C	
				0.75					−55°C to +125°C	
$-10 < V_Y < +10 (V_X = \pm 10V)$	E_{RY}			1.0	2.0	2.0	4.0		+25°C	
					3.0				0°C to +70°C	
				1.5					−55°C to +125°C	
Squaring Mode Error:										
Accuracy in Percent of Full Scale After Offset and Scale Factor Adjustment	E_{SQ}			0.5	0.75			%	+25°C	1
					1.0				0°C to +70°C	
				0.75					−55°C to +125°C	
Scale Factor (Adjustable)										
$K = \frac{2R_L}{I_3 R_X R_Y}$	K			0.1	0.1				+25°C	1
Input Resistance										
(f = 20 Hz)	R_{inx}			35	20			MΩ	+25°C	2
	R_{iny}			35	20					
Differential Output Resistance (f = 20 Hz)	R_o			300	300			kΩ	+25°C	3
Input Bias Current										
$I_{bx} = \frac{(I_9 + I_{12})}{2}$, $I_{by} = \frac{(I_4 + I_8)}{2}$	I_{bx}			2.0	2.0	8.0	12	μA	+25°	4
	I_{by}			2.0	2.0	8.0	12	μA		
Input Offset Current										
$\lvert I_9 - I_{12} \rvert$	$\lvert I_{iox} \rvert$			0.2	0.4	1.0	2.0	μA	+25	4
$\lvert I_4 - I_8 \rvert$	$\lvert I_{ioy} \rvert$			0.2	0.4	1.0	2.0			
Average Temperature Coefficient of Input Offset Current	$\lvert TC_{Iio} \rvert$					2.0		nA/°C	0°C to +70°C	4
					2.0				−55 to +70°C	
Output Offset Current										
$\lvert I_{14} - I_2 \rvert$	$\lvert I_{oo} \rvert$			10	20	50	100	μA	+25°C	4
Average Temperature Coefficient of Output Offset Current	$\lvert TC_{Ioo} \rvert$				20			nA/°C	0°C to +70°C	4
				20					−55°C to +125°C	
Frequency Response										
3.0 dB Bandwidth	BW_{3dB}			3.0	3.0			MHz	+25°C	5
3° Relative Phase Shift between V_X and V_Y	f_ϕ			750	750			kHz		
1% Absolute Error Due to Input-Output Phase Shift	f_θ			30	30			kHz		
Common Mode Input Swing (Either Input)	CMV	±11.5	±10.5	±13	±12			V	+25°C	6
Common Mode Gain (Either Input)	A_{CM}	−50	−40	−60	−50			dB	+25°C	6
Common Mode Quiescent Output Voltage	V_{o1}			21	21			V	+25°C	1
	V_{o2}			21	21					
Differential Output Voltage Swing Capability	V_{out}			±14	±14			V	+25°C	1
Power Supply Sensitivity	S^+			5.0	5.0			mV/V	+25°C	7
	S^-			10	10					
Power Supply Current	I_7			6.0	6.0	7.0	7.0	mA	+25°C	1
DC Power Dissipation	P_D			135	135	170	170	mW	+25°C	1

DESCRIPTION

The 5596 is a monolithic Double-Balanced Modulator/Demodulator designed for use where the output voltage is a product of an input voltage (signal) and a switched function (carrier). The S5596 will operate over the full military temperature range of -55°C to +125°C. The N5596 is intended for applications within the range of 0°C to +70°C.

FEATURES

- EXCELLENT CARRIER SUPPRESSION

  65dB typ @ 0.5 MHz

  50dB typ @ 10 MHz

- ADJUSTABLE GAIN AND SIGNAL HANDLING
- BALANCED INPUTS AND OUTPUTS
- HIGH COMMON-MODE REJECTION – 85dB typ

APPLICATIONS

SUPPRESSED CARRIER AND AMPLITUDE MODULATION
SYNCHRONOUS DETECTION
FM DETECTION
PHASE DETECTION
SAMPLING
SINGLE SIDEBAND
FREQUENCY DOUBLING

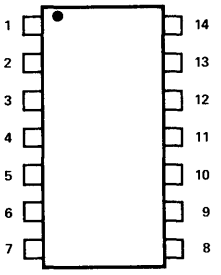
ABSOLUTE MAXIMUM RATINGS

Applied Voltage (Note 1)	30V
Differential Input Signal ($V_7 - V_8$)	±5.0V
Differential Input Signal ($V_4 - V_1$)	$\pm(5 + I_5 R_e)$V
Input Signal ($V_2 - V_1$, $V_3 - V_4$)	5.0V
Bias Current (I_5)	10mA
Power Dissipation (Pkg. Limitation)	
K-Package	680mW
Derate above 25°C	5.4mW/°C
A-Package (TO-116)	900mW
Derate above 25°C	7.2mW/°C
Operating Temperature Range	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

NOTES:
1. Voltage applied between pins 6-7, 8-1, 9-7, 9-8, 7-4, 7-1, 8-4, 6-8, 2-5, 3-5.
2. Pin number references pertain to K package pinout only.

PIN CONFIGURATIONS

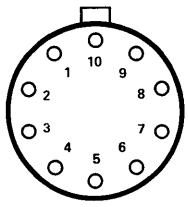
A PACKAGE
(Top View)



ORDER PART NOS.
S5596A/N5596A

1. Positive Signal Input
2. Gain Adjust
3. NC
4. Gain Adjust
5. Negative Signal Input
6. Bias
7. NC
8. Positive Output
9. Positive Carrier Input
10. Negative Carrier Input
11. NC
12. NC
13. Negative Output
14. V^-

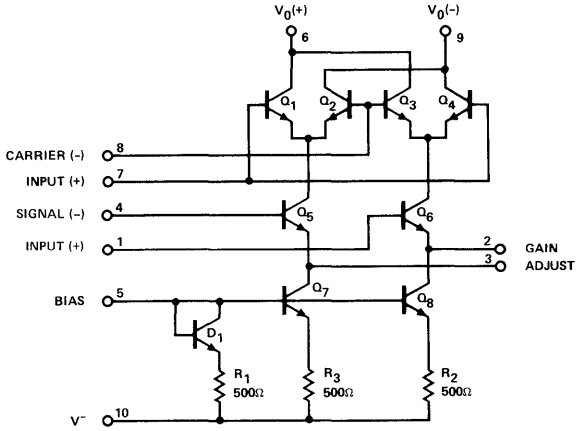
K PACKAGE



ORDER PART NOS.
S5596K/N5596K

1. Positive Signal Input
2. Gain Adjust
3. Gain Adjust
4. Negative Signal Input
5. Bias
6. Positive Output
7. Positive Carrier Input
8. Negative Carrier Input
9. Negative Output
10. V^-

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS* (All input and output characteristics are single-ended unless otherwise noted.)

PARAMETER	S5596			N5596			UNITS
	MIN	TYP	MAX	MIN	TYP	MAX	
Carrier Feedthrough							μV(rms)
V_C = 60 mV(rms) sine wave and f_C = 1.0 kHz		40			40		
offset adjusted to zero f_C = 10 MHz		140			140		
V_C = 300 mVp-p square wave:							mV(rms)
offset adjusted to zero f_C = 1.0 kHz		0.04	0.2		0.04	0.4	
offset not adjusted f_C = 1.0 kHz		20	100		20	200	
Carrier Suppressions							dB
f_S = 10 kHz, 300 mV(rms)							
f_C = 500 kHz, 60 mV(rms) sine wave	50	65		40	65		
f_C = 10 MHz, 60 mV(rms) sine wave		50			50		
Transadmittance Bandwidth (Magnitude) (R_L = 50Ω)							MHz
Carrier Input Port, V_C = 60 mV(rms) sine wave		300			300		
f_S = 1.0 kHz, 300 mV(rms) sine wave							
Signal Input Port, V_S = 300 mV(rms) sine wave		80			80		
$\|V_C\|$ = 0.5V dc							
Signal Gain	2.5	3.5		2.5	3.5		V/V
V_S = 100 mV(rms), f = 1.0 kHz; $\|V_C\|$ = 0.5V dc							
Single-Ended Input Impedance, Signal Port, f = 5.0 MHz							
Parallel Input Resistance		200			200		kΩ
Parallel Input Capacitance		2.0			2.0		pF
Single-Ended Output Impedance, f = 10 MHz							
Parallel Output Resistance		40			40		kΩ
Parallel Output Capacitance		5.0			5.0		pF
Input Bias Current							μA
$I_{bS} = \frac{I_1 + I_4}{2}$; $I_{bC} = \frac{I_7 + I_8}{2}$		12	25		12	30	
		12	25		12	30	
Input Offset Current							μA
$I_{ioS} = I_1 - I_4$; $I_{ioC} = I_7 - I_8$		0.7	5.0		0.7	7.0	
		0.7	5.0		0.7	7.0	
Average Temperature Coefficient of Input Offset Current		2.0			2.0		nA/°C
(T_A = -55°C to +125°C)							
Output Offset Current		14	50		15	80	μA
($I_6 - I_9$)							
Average Temperature Coefficient of Output Offset Current		90			90		nA/°C
(T_A = -55°C to +125°C)							
Common-Mode Input Swing, Signal Port, f_S = 1.0 kHz		5.0			5.0		Vp-p
Common-Mode Gain, Signal Port, f_S = 1.0 kHz,		-85			-85		dB
$\|V_C\|$ = 0.5V dc							
Common-Mode Quiescent Output Voltage (Pin 6 or Pin 9)		8.0			8.0		Vdc
Differential Output Voltage Swing Capability		8.0			8.0		Vp-p
Power Supply Current							mAdc
$I_6 + I_9$		2.0	3.0		2.0	4.0	
I_{10}		3.0	4.0		3.0	5.0	
DC Power Dissipation		33			33		mW

(V^+ = +12V dc, V^- = -8.0V dc, I_5 = 1.0mA dc, R_L = 3.9kΩ, R_e = 1.0kΩ, T_A = +25°C unless otherwise noted)

*Pin number references pertain to K package pinout only.

signetics

DESCRIPTION

The 75450 and 75450A are dual peripheral drivers designed for use in systems that employ TTL or DTL logic. These circuits feature two standard 7400 series gates and two uncommitted, high current, high voltage, npn output driver transistors.

ABSOLUTE MAXIMUM RATINGS

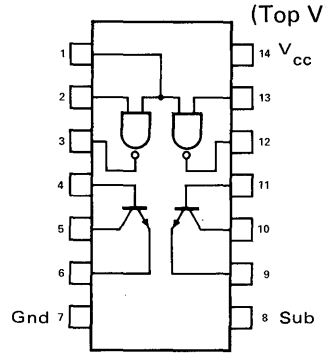
Supply Voltage	+7V
Input Voltage	+5.5V
Collector-Emitter Voltage	+30V
Continuous Collector Current	300mA
Continuous Total Power Dissipation	800mW

NOTES:

Positive Logic: $Y = \overline{AG}$ (gate only)
$C = AG$ (gate and transistor)

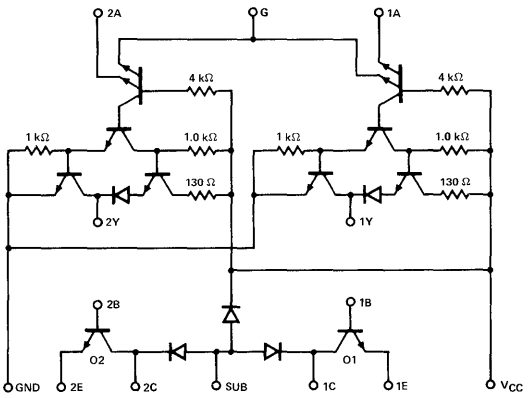
PIN CONFIGURATION

A PACKAGE
(Top View)



ORDER PART NOS.
SN75450N
SN75450AN

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS - TTL GATES (V_{CC} = 5V, T_A = 25°C)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-Level Input Voltage			2			V
V_{IL}	Low-Level Input Voltage					0.8	V
V_I	Input Clamp Voltage		V_{CC} = 4.75V, I_I = −12mA			−1.5	V
V_{OH}	High-Level Output Voltage		V_{CC} = 4.75V, V_{IL} = 0.8V, I_{OM} = −400μA	2.4	3.3		V
V_{OL}	Low-Level Output Voltage		V_{CC} = 4.75V, V_{1H} = 2V, I_{OL} = 16mA		0.22	0.4	V
I_I	Input Current at Maximum Input Voltage	Input A Input G	V_{CC} = 5.25V, V_I = 5.5V			1 2	mA
I_{IH}	High-Level Input Current	Input A Input G	V_{CC} = 5.25V, V_I = 2.4V			40 80	μA
I_{IL}	Low-Level Input Current	Input A Input G	V_{CC} = 5.25V, V_I = 0.4V			−1.6 −3.2	mA
I_{OS}	Short Circuit Output Current		V_{CC} = 5.25V	−18		−55	mA
I_{CCH}	Supply Current, High-Level Output		V_{CC} = 5.25V, V_I = 0		2	4	mA
I_{CCL}	Supply Current, Low-Level Output		V_{CC} = 5.25V, V_I = 5V		6	11	mA

ELECTRICAL CHARACTERISTICS - OUTPUT TRANSISTORS (Cont'd)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(BR)\ CBO}$ Collector-Base Breakdown Voltage	$I_C = 100\mu A$, $I_E = 0$	35			V
$V_{(BR)\ CER}$ Collector-Emitter Breakdown Voltage	$I_C = 100\mu A$, $R_{BE} = 500\Omega$	30			V
$V_{(BR)\ EBO}$ Emitter-Base Breakdown Voltage	$I_E = 100\mu A$, $I_C = 0$	5			V
h_{FE} Static Forward Current Transfer Ratio	$V_{CE} = 3V$, $I_C = 100mA$, $T_A = 25°C$	25			
	$V_{CE} = 3V$, $I_C = 300mA$, $T_A = 25°C$	30			
	$V_{CE} = 3V$, $I_C = 100mA$ $T_A = 0°C$	20			
	$V_{CE} = 3V$, $I_C = 300mA$, $T_A = 0°C$	25			
V_{BE} Base-Emitter Voltage	$I_B = 10mA$, $I_C = 100mA$		0.85	1	V
	$I_B = 30mA$, $I_C = 300mA$		1.05	1.2	V
$V_{CE\ (sat)}$ Collector-Emitter Saturation Voltage	$I_B = 10mA$, $I_C = 100mA$		0.25	0.4	V
	$I_B = 30mA$, $I_C = 300mA$		0.5	0.7	V

SWITCHING CHARACTERISTICS - TTL GATES ($V_{CC} = 5V$, $T_A = 25°C$)

PARAMETER	TEST CONDITIONS	75450			75450A			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
TTL GATES								
t_{PLH} Propagation Delay Time Low-to-High-Level Output	$C_L = 15pF$, $R_L = 400\Omega$		12	22		20		ns
t_{PHL} Propagation Delay Time, High-to-High-Level Output			8	15		8		ns
OUTPUT TRANSISTORS								
t_D Delay Time	$I_C = 200mA$, $I_{B(1)} = 20mA$		8	15		8		ns
t_r Rise Time	$I_{B(2)} = -40mA$,		12	20		12		ns
t_s Storage Time	$V_{BE(off)} = -1V$		7	15		7		ns
t_f Fall Time	$C_L = 15pF$, $R_L = 50$		6	15		6		ns
GATES AND TRANSISTORS COMBINED								
t_{PLH} Propagation Delay Time, Low-to-High-Level Output	$I_C = 200mA$, $C_L = 15pF$, $R_L = 50$		17			40		ns
t_{PHL} Propagation Delay Time, High-to-Low-Level Output			16			25		ns
t_{TLH} Transition Time, Low-to-High-Level Output			7			10		ns
t_{THL} Transition Time, High-to-Low-Level Output			9			12		ns

DESCRIPTION

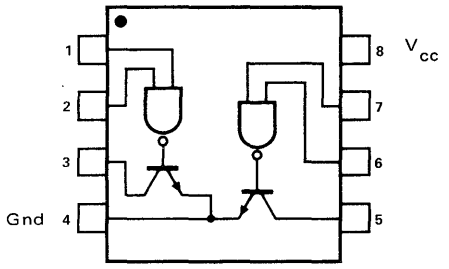
The SN75451 and SN75451A dual peripheral drivers are versatile devices designed for use in systems that employ TTL or DTL logic. These circuits are dual AND drivers (positive logic) with the gate outputs internally connected to the npn output transistors.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	+7V
Input Voltage	+5.5V
Output Voltage	+30V
Continuous Output Current	300mA
Continuous Power Dissipation	800mW
Positive Logic	Y = AB

PIN CONFIGURATION

V PACKAGE
(Top View)

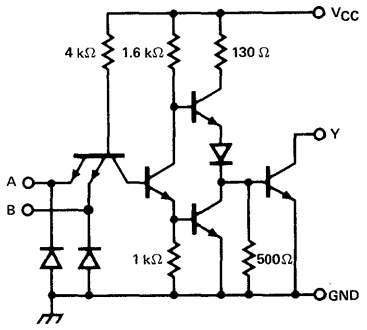


ORDER PART NO. SN75451P/SN75451AP

TRUTH TABLE

A	B	Y
L	L	L (on state)
L	H	L (on state)
H	L	L (on state)
H	H	H (off state)

EQUIVALENT CIRCUIT (Each Driver)



ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-Level Input Voltage		2			V
V_{IL}	Low-Level Input Voltage				0.8	V
V_I	Input Clamp Voltage	V_{CC} = 4.75V, I_I = −12mA			−1.5	V
I_{OH}	High-Level Output Current	V_{CC} = 4.75V, V_{IH} = 2V, V_{OH} = 30V			100	μA
V_{OL}	Low-Level Output Voltage	V_{CC} = 4.75V, V_{IL} = 0.8V, I_{OL} = 100mA		0.25	0.4	V
		V_{CC} = 4.75V, V_{IL} = 0.8V, I_{OL} = 300mA		0.5	0.7	V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.25V, V_I = 5.5V			1	mA
I_{IH}	High-Level Input Current	V_{CC} = 5.25V, V_I = 2.4V			40	μA
I_{IL}	Low-Level Input Current	V_{CC} = 5.25V, V_I = 0.4V		−1	−1.6	mA
I_{CCH}	Supply Current, High-Level Output	V_{CC} = 5.25V, V_I = 5V		7	11	mA
I_{CCL}	Supply Current, Low-Level Output	V_{CC} = 5.25V, V_T = 0		52	65	mA

SWITCHING CHARACTERISTICS (V_{CC} = 5V, T_A = 25°C)

PARAMETER	TEST CONDITIONS	75451			75451A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH} Propagation Delay Time Low-toHigh-Level Output			20	25		45		ns
t_{PHL} Propagation Delay Time High-to-Low Level Output	$I_O \approx 200mA, C_L$ = 15pF		20	30		25		ns
t_{TLH} Transition Time, Low-to-High-Level Output	$R_L = 50\Omega$		10			10		ns
t_{THL} Transition Time, High-to-Low-Level Output			10			12		ns

SECTION 7
consumer circuits

DESCRIPTION

The 540 is a monolithic, class AB power amplifier designed specifically to drive a pair of complementary output transistors. The device features low standby current yet retains a high output current drive capability with internal current limiting. A wide power bandwidth and excellent linearity make this device ideal for use as an audio power amplifier.

FEATURES

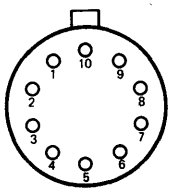
- INTERNAL CURRENT LIMITING
- LOW STANDBY CURRENT
- HIGH OUTPUT CURRENT CAPABILITY
- WIDE POWER BANDWIDTH
- LOW DISTORTION

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	± 27 Volts SE540
	± 22 Volts NE540
Operating Temperature Range	-55°C to +125°C SE540
	0°C to +70°C NE540
Storage Temperature Range	-65°C to +150°C
Output Short Circuit Duration (Not exceeding maximum dissipation.)	Indefinite

PIN CONFIGURATION

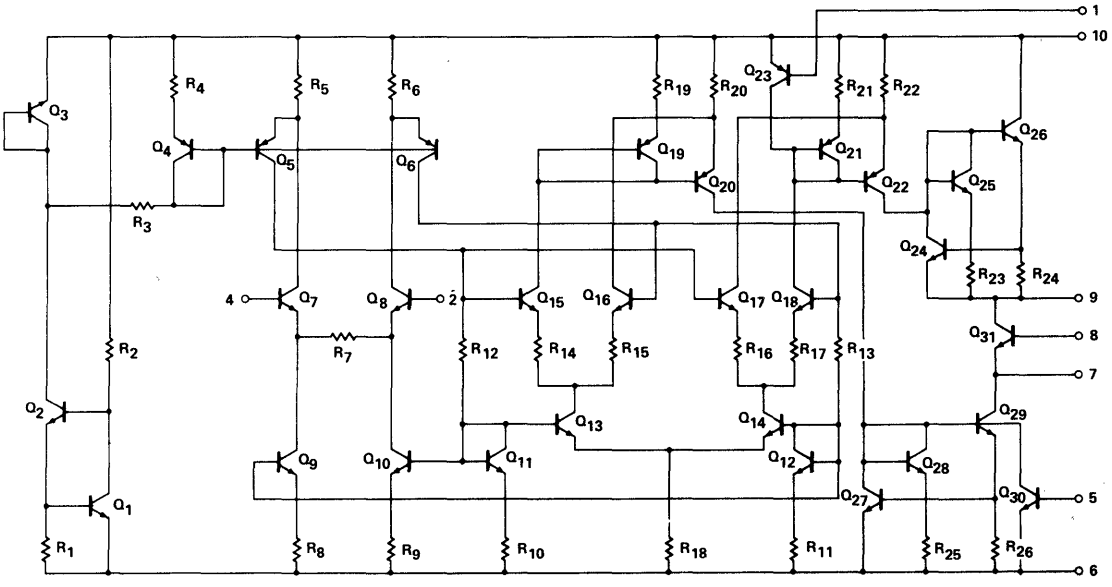
L PACKAGE
(Top View)



1. Power Limit
2. Non Inverting Input
3. NC
4. Inverting Input
5. Power Limit
6. V^-
7. Output 1 (emmitter)
8. Output 2 (base)
9. Output 3 (collector)
10. V^+

ORDER PART NOS. SE540L/NE540L

SCHEMATIC DIAGRAM

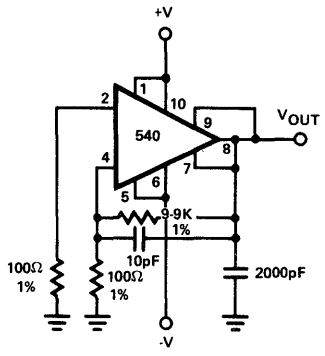


ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

PARAMETER	TEST CONDITIONS	SE 540			NE 540			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Operating Temperature Range		-55		+125	0		+70	°C
Operating Supply Voltage		±5		±25	±5		±20	Volts
Quiescent Current			13	20		13	20	mA
Input Offset Voltage			5	7		7	10	mV
Input Offset Current			0.3	0.7		0.5	1	μA
Input Bias Current			1.5	3		2	5	μA
Input Impedance	40 dB Gain		20			20		kΩ
Current Gain		80	100		70	90		dB
Gain Variation Over Temperature Range	40 dB Gain		±0.1			±0.1		dB
Frequency Response	40 dB Gain ±1 dB		500			100		kHz
Distortion	40 dB Gain Output 3 dB below maximum R_L = 600Ω		0.25	0.5		0.5	1.0	%
Equivalent Input Noise Voltage	R_S = 600Ω 50 Hz to 500 kHz		10			10		μV
Power Supply Rejection Ratio	40 dB Gain	80	90		60	80		dB
Common Mode Rejection Ratio			110			90		dB
Output Drive Current		±120	±150		±80	±100		mA
Slew Rate	V_S = ±20V V_{OUT} = ±15V		200			200		V/μs

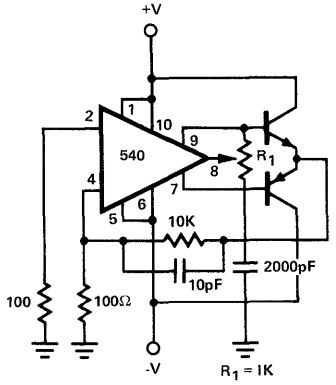
TEST CIRCUITS

OFFSET VOLTAGE MEASUREMENT



$$V_{OFFSET} = \frac{V_{OUT}}{100}$$

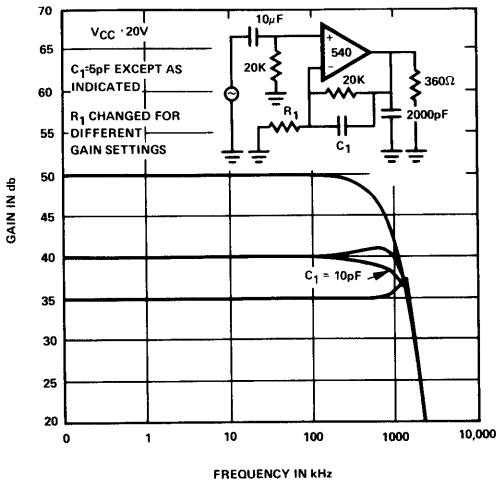
OUTPUT BIAS CONTROL



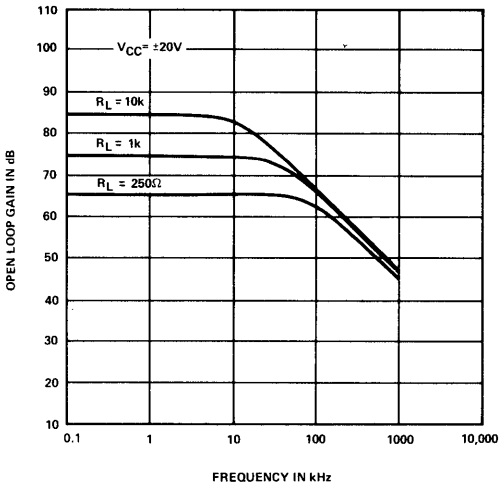
BIAS CONTROL FOR OUTPUT TRANSISTORS

TYPICAL PERFORMANCE CHARACTERISTICS

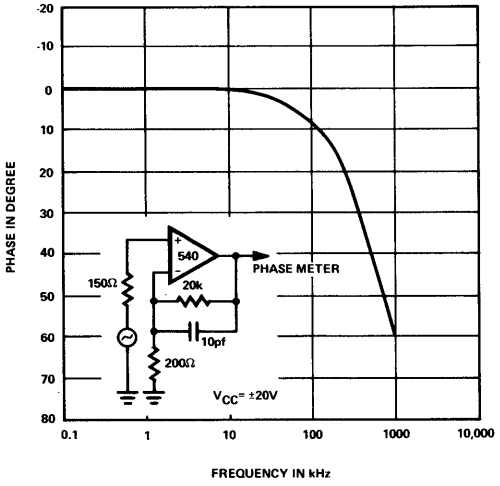
CLOSED LOOP FREQUENCY RESPONSE



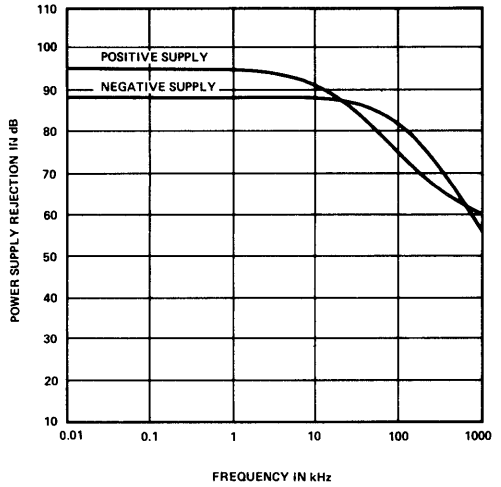
OPEN LOOP GAIN AND FREQUENCY RESPONSE



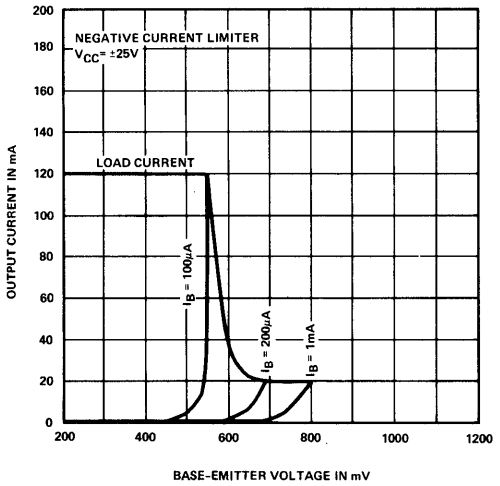
PHASE RESPONSE VERSUS FREQUENCY



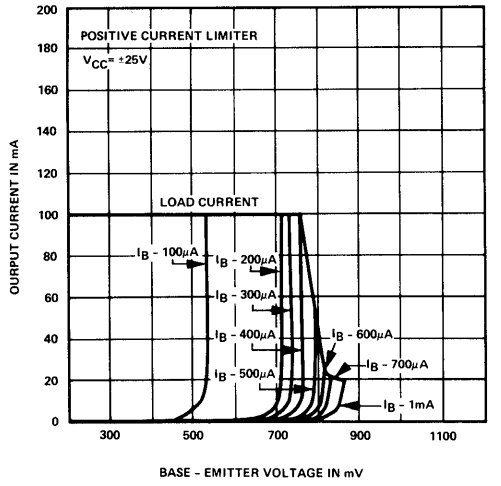
POWER SUPPLY REJECTION VERSUS FREQUENCY



OUTPUT CURRENT VERSUS I_B/V_{BE} OF CURRENT LIMITER

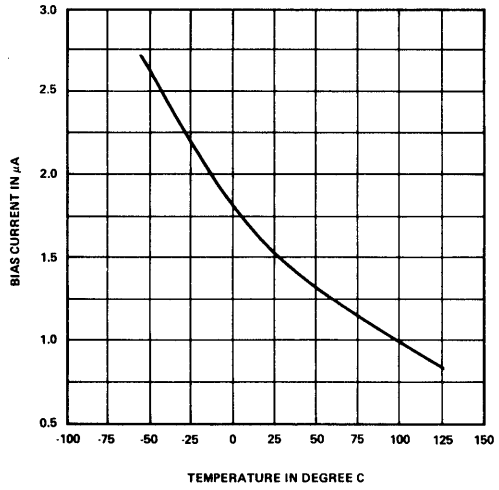


OUTPUT CURRENT VERSUS I_B/V_{BE} OF CURRENT LIMITER

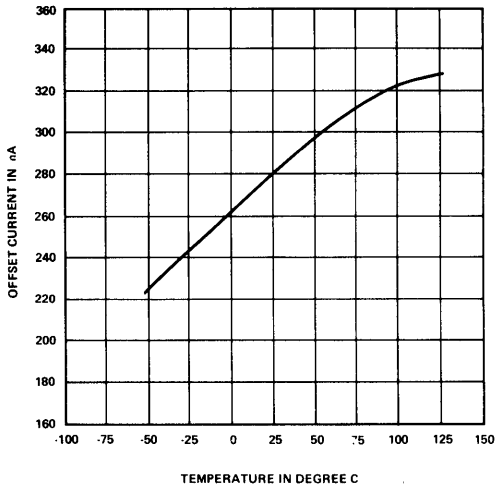


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd.)

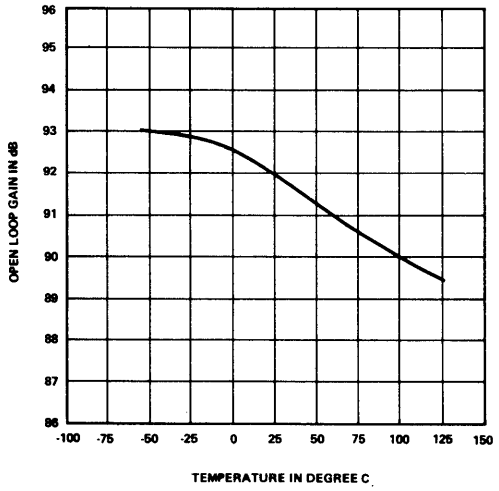
BIAS CURRENT VERSUS TEMPERATURE



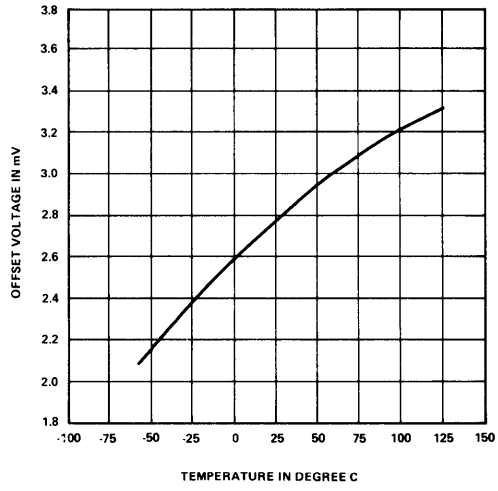
OFFSET CURRENT VERSUS TEMPERATURE



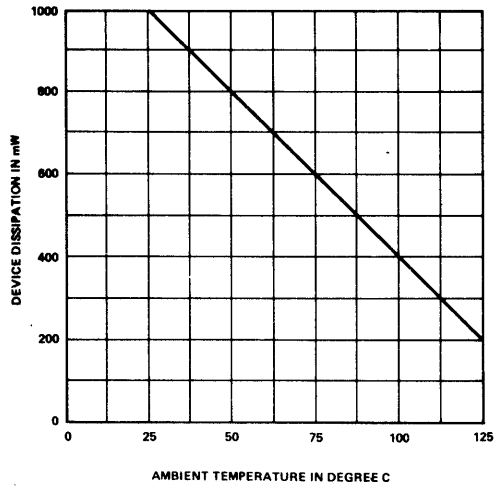
OPEN LOOP GAIN VERSUS TEMPERATURE



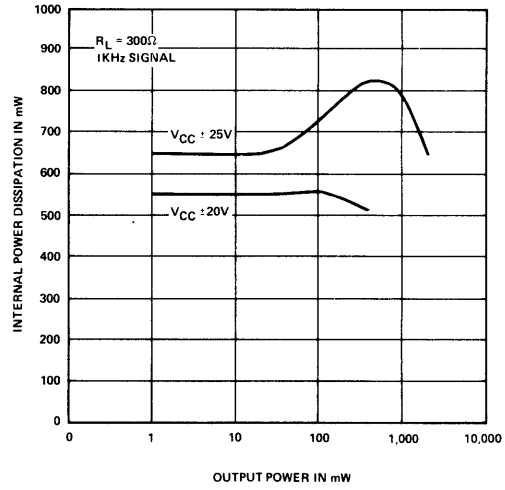
OFFSET VOLTAGE VERSUS TEMPERATURE



MAXIMUM DISSIPATION VERSUS AMBIENT TEMPERATURE

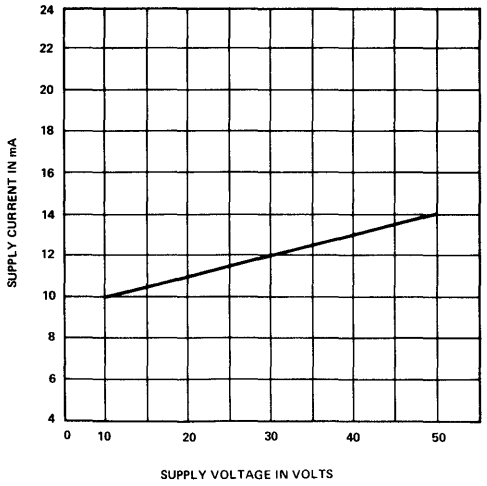


INTERNAL POWER DISSIPATION VERSUS LOAD POWER

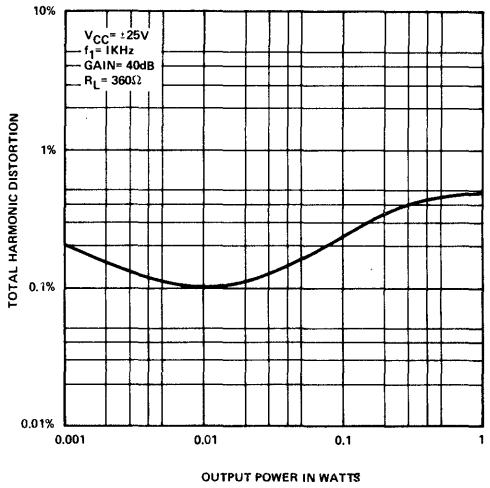


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd.)

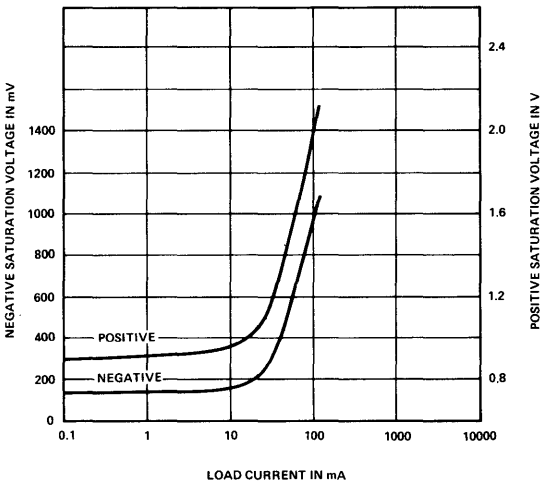
QUIESCENT CURRENT VERSUS SUPPLY VOLTAGE



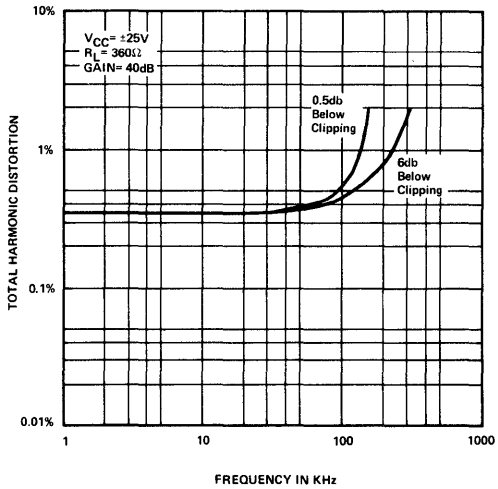
TOTAL HARMONIC DISTORTION VERSUS OUTPUT



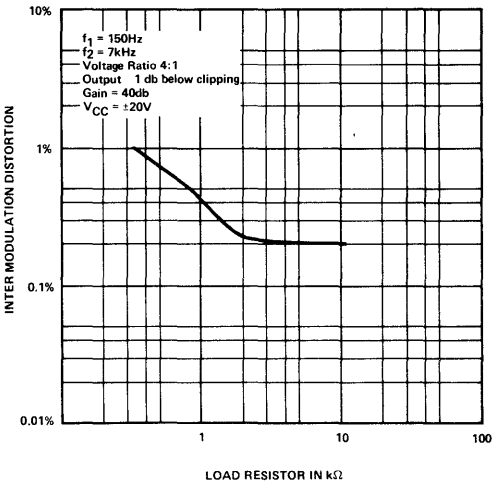
OUTPUT SATURATION VOLTAGE VERSUS LOAD



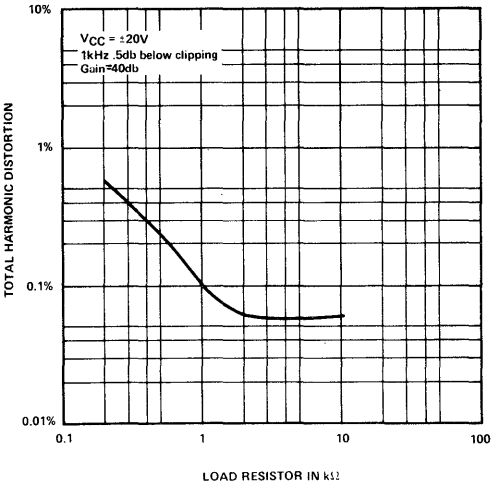
TOTAL HARMONIC DISTORTION VERSUS FREQUENCY



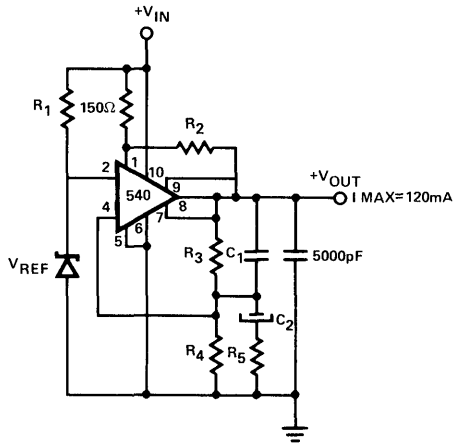
INTERMODULATION DISTORTION VERSUS LOAD

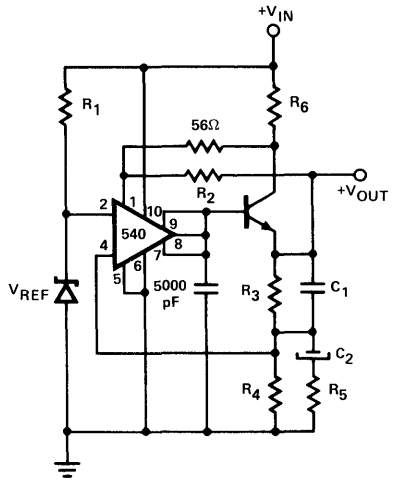


TOTAL HARMONIC DISTORTION VERSUS LOAD



POSITIVE VOLTAGE REGULATORS



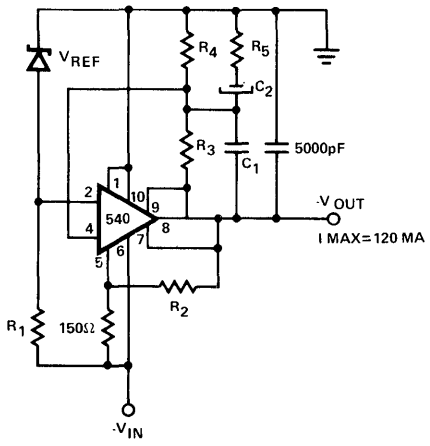


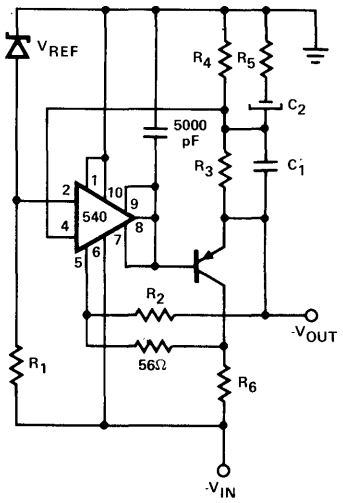
$$V_{OUT} \simeq \frac{R_3 + R_4}{R_4} \; V_{REF} \qquad R_5 \simeq \frac{R_3}{100}$$

$$R_1 \simeq \frac{V_{IN} - V_{REF}}{I_{ZENER}} \qquad C_1 \simeq \frac{0.2}{R_3} \; \mu F$$

$$R_2 \simeq \frac{2\,V_{IN} \cdot V_{OUT}}{4mA} \qquad C_2 \simeq 10\mu F$$

NEGATIVE VOLTAGE REGULATORS





$$V_{OUT} \simeq \frac{R_3 + R_4}{R_4} \; V_{REF} \qquad R_5 \simeq \frac{R_3}{100}$$

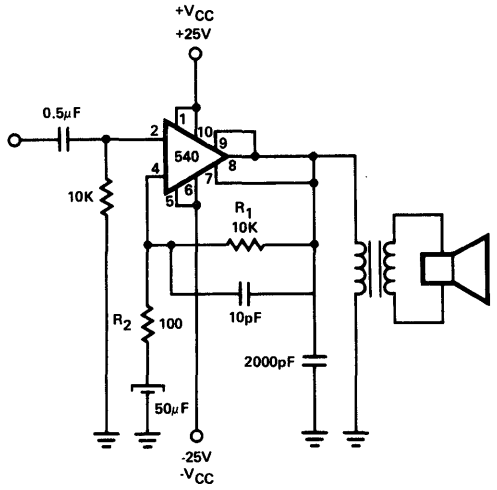
$$R_1 \simeq \frac{V_{IN} \cdot V_{REF}}{I_{ZENER}} \qquad C_1 \simeq \frac{0.2}{R_3} \; \mu F$$

$$R_2 \simeq \frac{2\,V_{IN} \cdot V_{OUT}}{4mA} \qquad C_2 \simeq 10\mu F$$

TYPICAL APPLICATIONS

POWER AMPLIFIERS

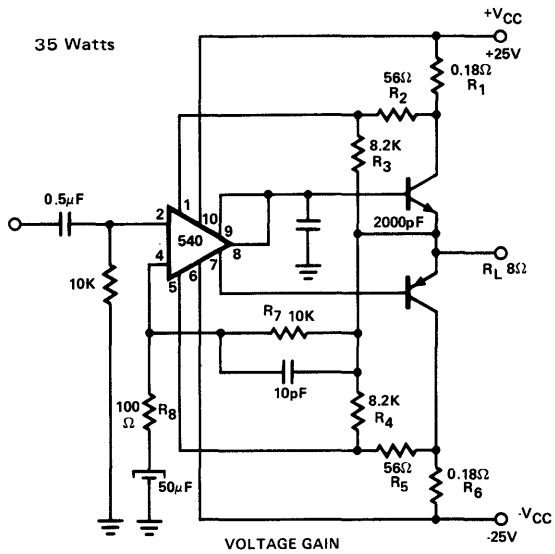
1 Watt



VOLTAGE GAIN

$A_V \simeq \frac{R_1 + R_2}{R_2}$

35 Watts



VOLTAGE GAIN

$A_V = \frac{R_7 + R_8}{R_8}$

CURRENT LIMITING

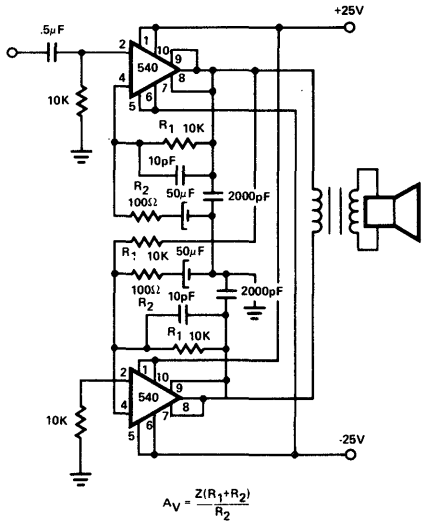
$R_1 = R_6 \simeq \frac{650mV}{I_{peak}}$

POWER LIMITING

$R_2 = R_5 \simeq 56\Omega$

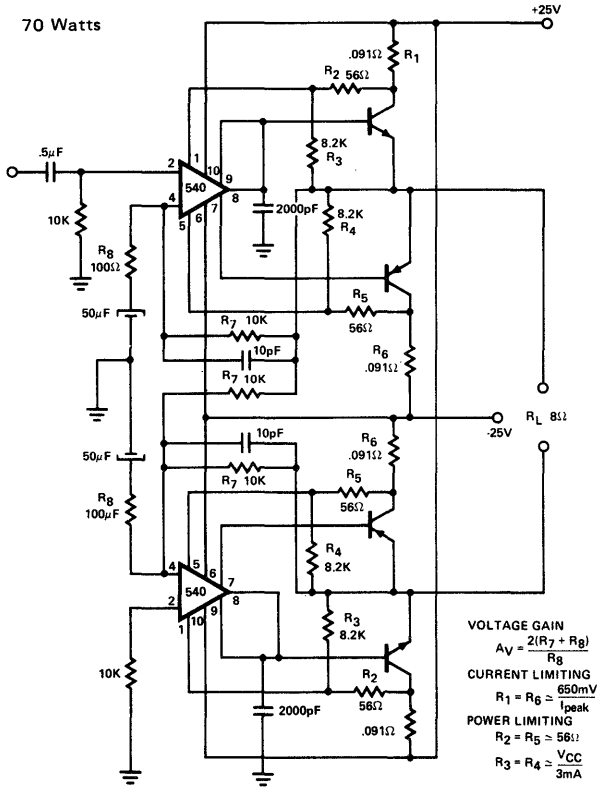
$R_3 = R_4 \simeq \frac{V_{CC}}{3mA}$

3 Watts



$A_V = \frac{Z(R_1+R_2)}{R_2}$

70 Watts



VOLTAGE GAIN

$A_V = \frac{2(R_7 + R_8)}{R_8}$

CURRENT LIMITING

$R_1 = R_6 \simeq \frac{650mV}{I_{peak}}$

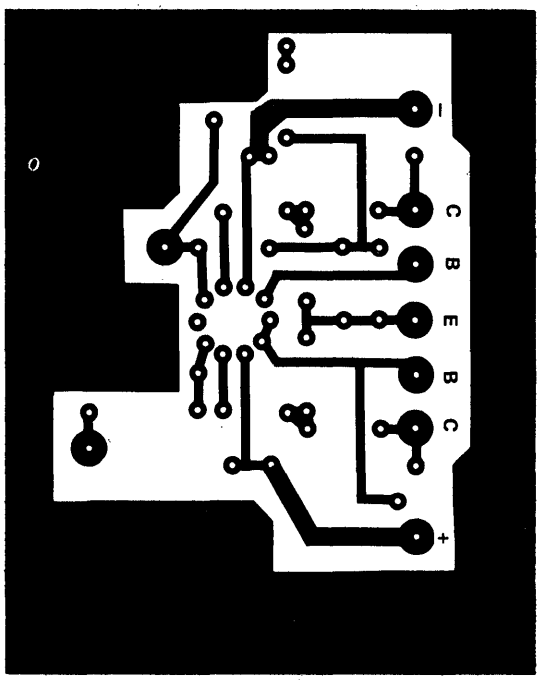
POWER LIMITING

$R_2 = R_5 \simeq 56\Omega$

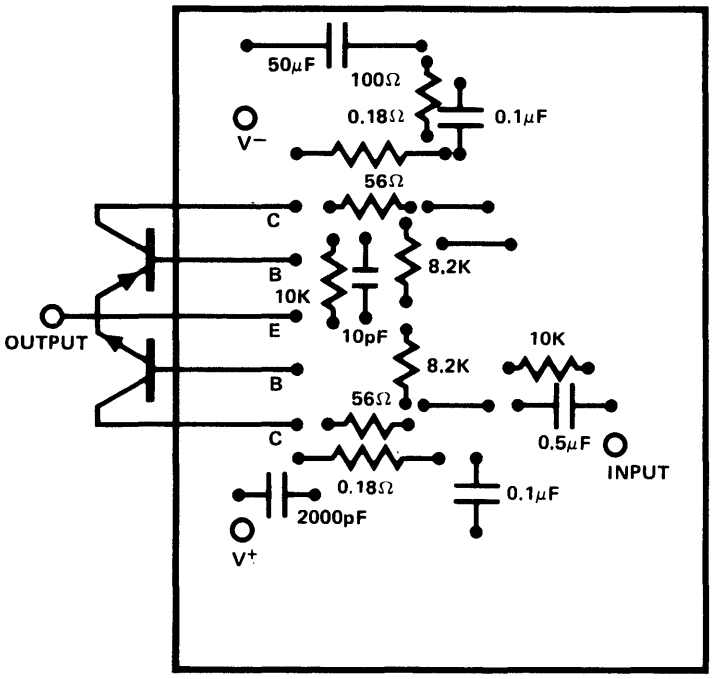
$R_3 = R_4 \simeq \frac{V_{CC}}{3mA}$

35 WATT AMPLIFIER

P.C. BOARD LAYOUT (BOTTOM VIEW)



PARTS LAYOUT (TOP VIEW)



signetics

TIMER 555

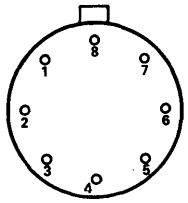
NEW PRODUCT ADVANCED INFORMATION
LINEAR INTEGRATED CIRCUITS

FEATURES

- TIMING FROM MICROSECONDS THROUGH 1 Hr.
- CAN EITHER FREE RUN OR LATCH
- ADJUSTABLE DUTY CYCLE
- TIME DELAYS CAN BE RESET
- TEMPERATURE STABILITY 0.005% PER °C
- OPERATES FROM 4 to 15 VOLTS FOR 1% CHANGE IN TIMING
- TIMING CAN BE CHANGED 10:1 WITH CONTROL VOLTAGE
- OUTPUT CAN SOURCE OR SINK 100mA

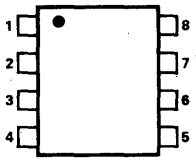
PIN CONFIGURATION

T PACKAGE
(Top View)



Order Part Nos. (SE555T/NE555T)

V PACKAGE



Order Part Nos. (SE555V/NE555V)

ELECTRICAL CHARACTERISTICS (25°unless otherwise specified)

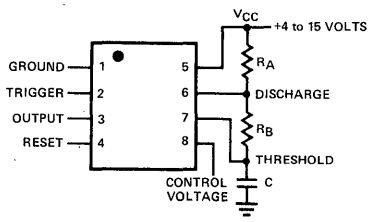
PARAMETERS	SE 555 T			NE 555 V			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Operating Temperature Range	-55		12.5	0		70	°C
Operating Supply Voltage	4.5		18	4.5		16	Volts
Operating Supply Current @5V		3			3		mA
Operating Supply Current @15V		8			8		mA
Timing Error, 10V[1]		0.5			1		%
Timing Error, 10V[2]		2			4		%
Time-Temperature Drift		30			50		ppm/°C
Time-Supply Voltage Drift		50			100		ppm/°C
Trigger Voltage		1/3			1/3		xV_{CC}
Trigger Current		0.5			0.5		μA
Reset Voltage		0.7			0.7		Volts
Reset Current		0.1			0.1		mA
FM Input Impedance		3.3			3.3		kΩ
Bias Level		2/3			2/3		xV_{CC}
Deviation Range		+30,-90			+30,-90		%
Output Voltage Drop (Low) @ 10mA		0.1			0.1		Volts
@ 100mA		1.8			1.8		Volts
@ 200mA		2.3			2.4		Volts
Output Voltage Drop (High) @ 100mA		1.5			1.6		Volts
@ 200mA		2.0			2.1		Volts
Rise Time		100			100		nSec
Fall Time		100			100		nSec

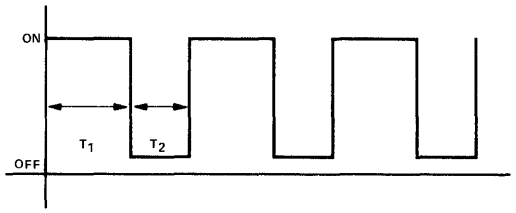
NOTES:

1. R_A, R_B = 1K Ohm to 100K Ohm, t = 100 u sec. 2. R_A, R_B = 500 Ohm to 10M Ohm, t = 10 u sec. 3. External Load to V_{CC}, 2.7KOhm.

TYPICAL CONNECTION

(Top View)





NOTES:

1. Jump 6 & 2 for free running & connect 4 to +V.
2. Ground 4 to reset timing.
3. For time delay $T = 1.1\ R_A C$ ($R_B = 0$)
4. For free running timing is as follows:
   $T_1 = 0.685\ (R_A + R_B)C$ $T_2 = 0.685 R_B C$

signetics

TELEVISION CHROMA SYSTEM

INTRODUCTION
LINEAR INTEGRATED CIRCUITS

5070
5071
5072

DESCRIPTION

The 5070, 5071, and 5072 are monolithic silicon integrated circuits that constitute a complete chroma system for color television receivers. The 5070 is a complete subcarrier regeneration system featuring a new concept of phase control applied to the oscillator circuit. The 5071 is a chroma amplifier system and the 5072 performs the demodulation function.

The 5070 utilizes the 16-lead plastic dual-in-line package; the 5071 and 5072 are supplied 14-lead plastic dual-in-line packages.

FEATURES

5070

- VOLTAGE CONTROL OSCILLATOR
- KEYED APC & ACC DETECTORS
- DC HUE CONTROL
- SHUNT REGULATOR

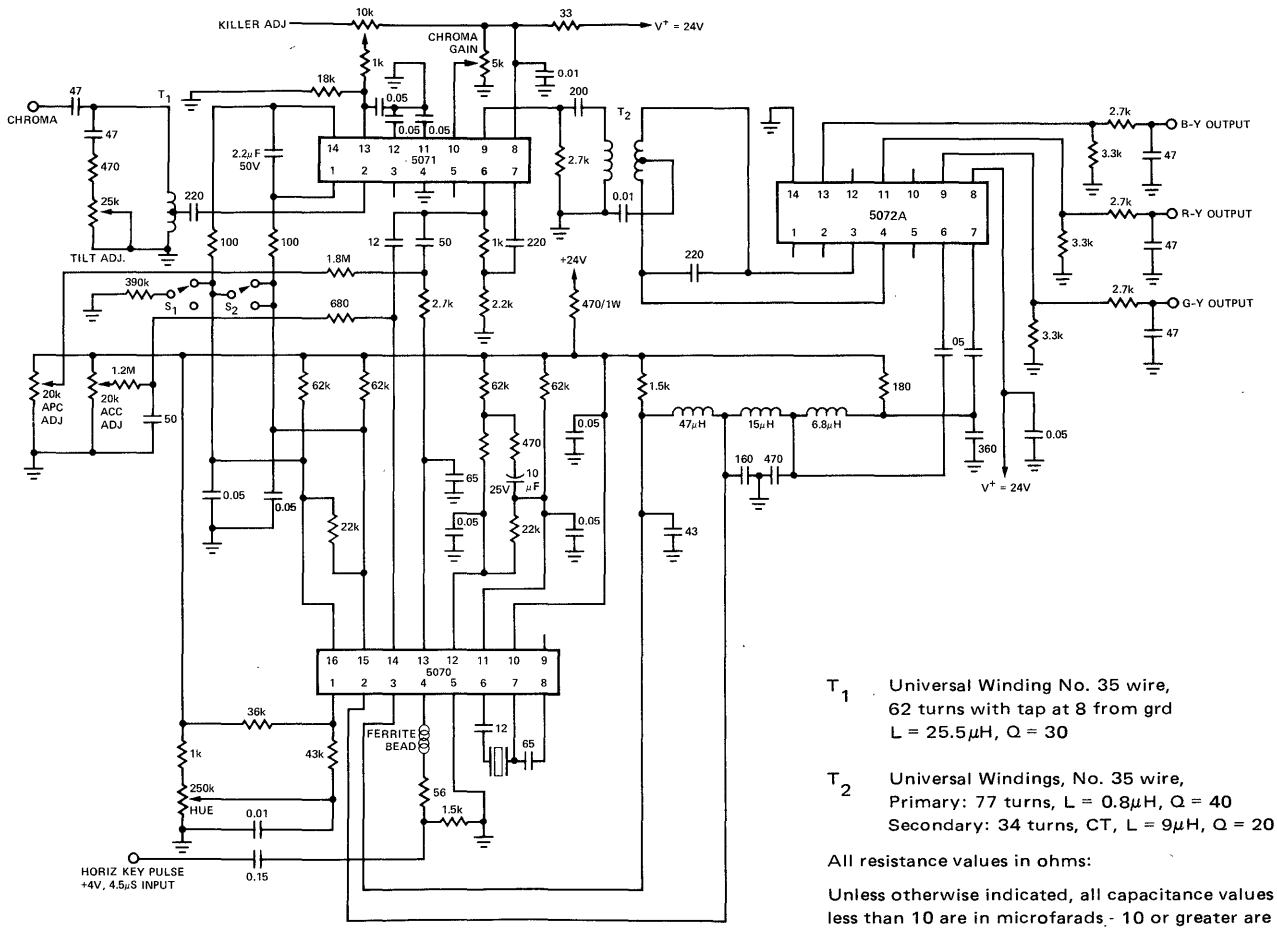
5071

- ACC CONTROLLED CHROMA AMPLIFIER
- DC CHROMA GAIN CONTROL
- COLOR KILLER
- AMPLIFIER SHORT-CIRCUIT PROTECTION

5072

- SYNCHRONOUS DETECTOR WITH COLOR DIFFERENCE MATRIX
- EMITTER-FOLLOWER OUTPUT AMPLIFIERS WITH SHORT-CIRCUIT PROTECTION

TYPICAL SCHEMATIC DIAGRAM



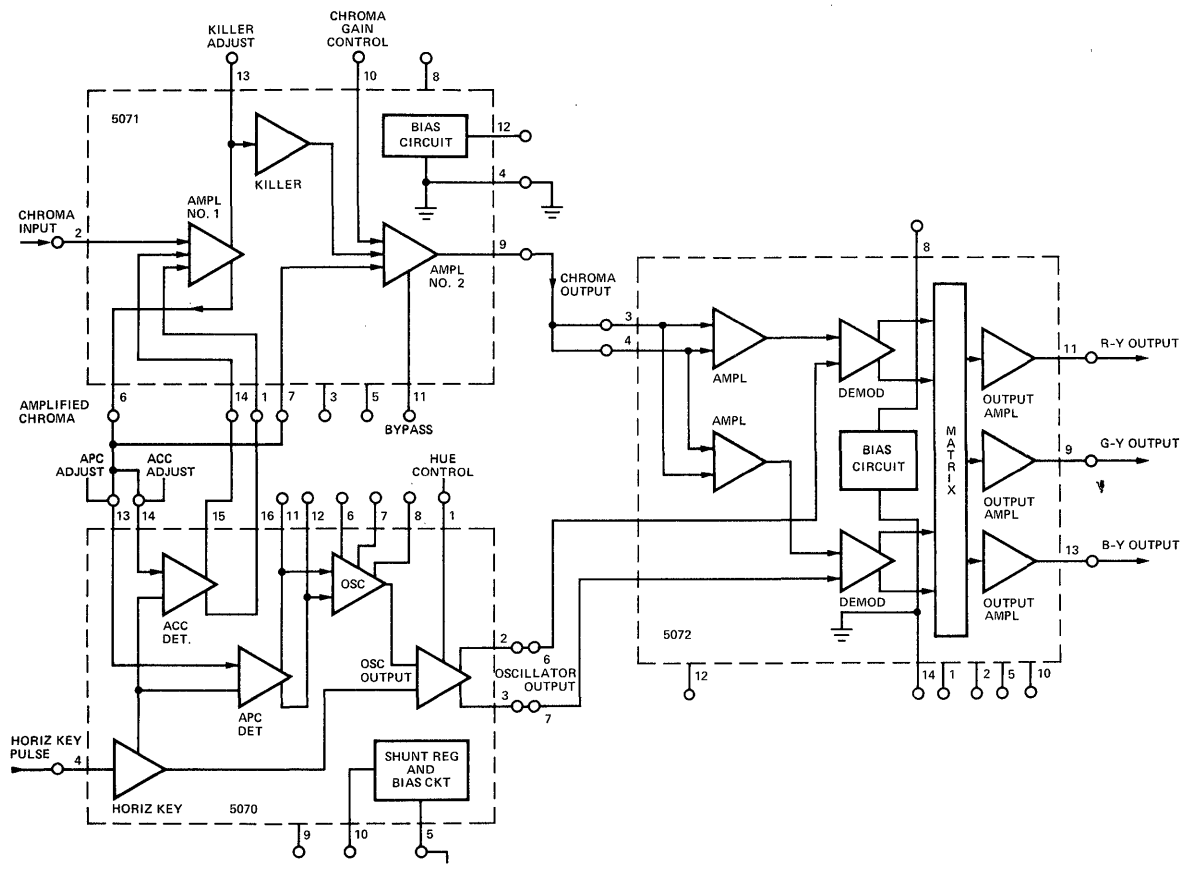
T_1 Universal Winding No. 35 wire, 62 turns with tap at 8 from grd
L = 25.5μH, Q = 30

T_2 Universal Windings, No. 35 wire,
Primary: 77 turns, L = 0.8μH, Q = 40
Secondary: 34 turns, CT, L = 9μH, Q = 20

All resistance values in ohms:

Unless otherwise indicated, all capacitance values less than 10 are in microfarads. 10 or greater are in picofarads.

TYPICAL FUNCTIONAL DIAGRAM



DESCRIPTION

The 5070 is a complete subcarrier regeneration system with automatic phase control applied to the oscillator. An amplifier chroma signal from the 5071 is applied to terminals No. 13 and No. 14, which are the automatic phase control (APC) and the automatic chroma control (ACC) inputs. APC and ACC detection is keyed by the horizontal pulse which also inhibits the oscillator output amplifier during the burst interval.

The ACC system uses a synchronous detector to develop a correction voltage at the differential output terminal Nos. 15 and 16. This control signal is applied to the input terminal Nos. 1 and 14 of the 5071. The APC system also uses a synchronous detector. The APC error voltage is internally coupled to the 3.58 MHz oscillator at balance; the phase of the signal at terminal No. 13 is in quadrature with the oscillator.

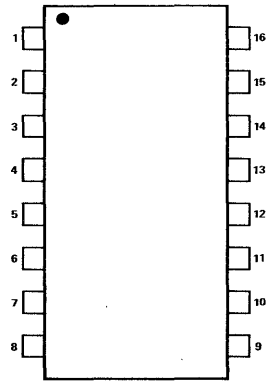
To accomplish phasing requirements, an RC phase shift network is used between the chroma input and terminal Nos. 13 and 14. The feedback loop of the oscillator is from terminal Nos. 7 and 8 back to No. 6. The same oscillator signal is available at terminal Nos. 7 and 8, but the dc output of the APC detector controls the relative signal levels at terminal Nos. 7 or 8. Because the output at terminal No. 8 is shifted in phase compared to the output at terminal No. 7, which is applied directly to the crystal circuit, control of the relative amplitudes at terminal Nos. 7 and 8 alters the phase in the feedback I_{cop}, thereby changing the frequency of the crystal oscillator. Balance adjustments of dc offsets are provided to establish an initial no-signal offset control in the ACC output, and a no-signal, on-frequency adjustment through the APC detector-amplifier circuit which controls the oscillator frequency. The oscillator output stage is differentially controlled at terminal Nos. 2 and 3 by the hue control input to terminal No. 1. The hue phase shift is accomplished by the external R, L, and C components that couple the oscillator output to the demodulator input terminals. The 5070 includes a shunt regulator to establish a 12Vdc supply.

FEATURES

- VOLTAGE CONTROLLED OSCILLATOR
- KEYED APC & ACC DETECTORS
- DC HUE CONTROL
- SHUNT REGULATOR

PIN CONFIGURATION

B PACKAGE
(Top View)



1. Tint Control
2. Oscillator Output
3. Oscillator Output
4. Gate Input
5. Ground
6. Oscillator Feedback
7. Oscillator Control
8. Oscillator Control
9. NC
10. Supply
11. APC Detector Output
12. APC Detector Output
13. APC Detector Input
14. ACC Detector Input
15. ACC Detector Output
16. ACC Detector Output

ORDER PART NO. N5070B

ABSOLUTE MAXIMUM RATINGS

(Values at $T_A = 25^\circ C$)

DC Supply Voltage and Current	See Charts
Device Dissipation:	
Up to $T_A = +70^\circ C$	530mW
Above $T_A = +70^\circ C$	Derate Linearly at 6.7 mW/°C
Ambient Temperature Range:	
Operating	-40 to +85°C
Storage	-65 to +150°C
Lead Temperature (During Soldering):	
At distance 1/32 in. (3.17 mm) from seating plane for 10s max	+265°C

Voltage (Note 1)

TERM NO.	MIN. VOLTS	MAX. VOLTS
1	0	*
2	0	+16
3	0	+16
4	-5	Note 3
6	—	—
7	—	—
8	—	—
10	0	Note 4
11	0	Note 2
12	0	Note 2
13	0	Note 2
14	0	Note 2
15	0	+16
16	0	+16

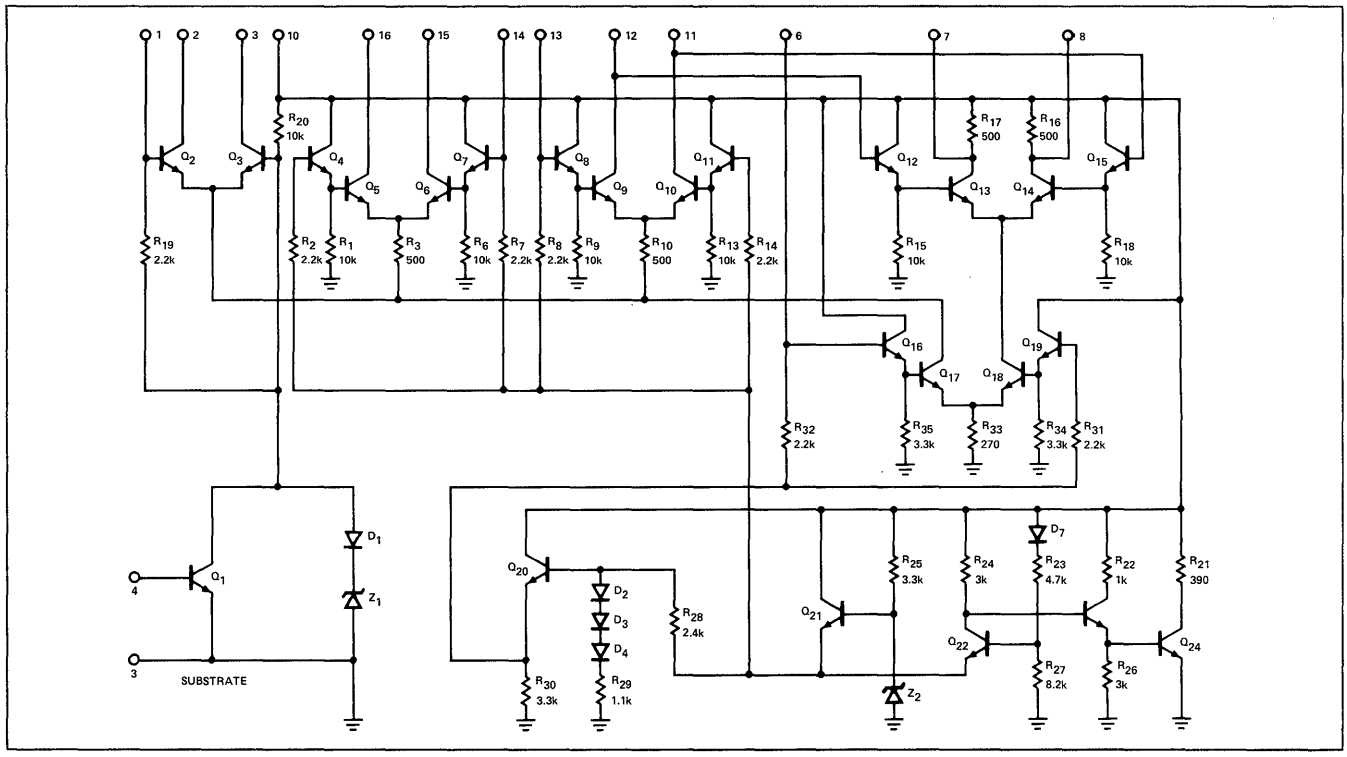
Current

TERM NO.	I_j mA	I_O mA
1	20	1
2	—	—
3	—	—
4	—	1
10	Note 4	1
11	—	—
12	—	—
13	20	1
14	20	1

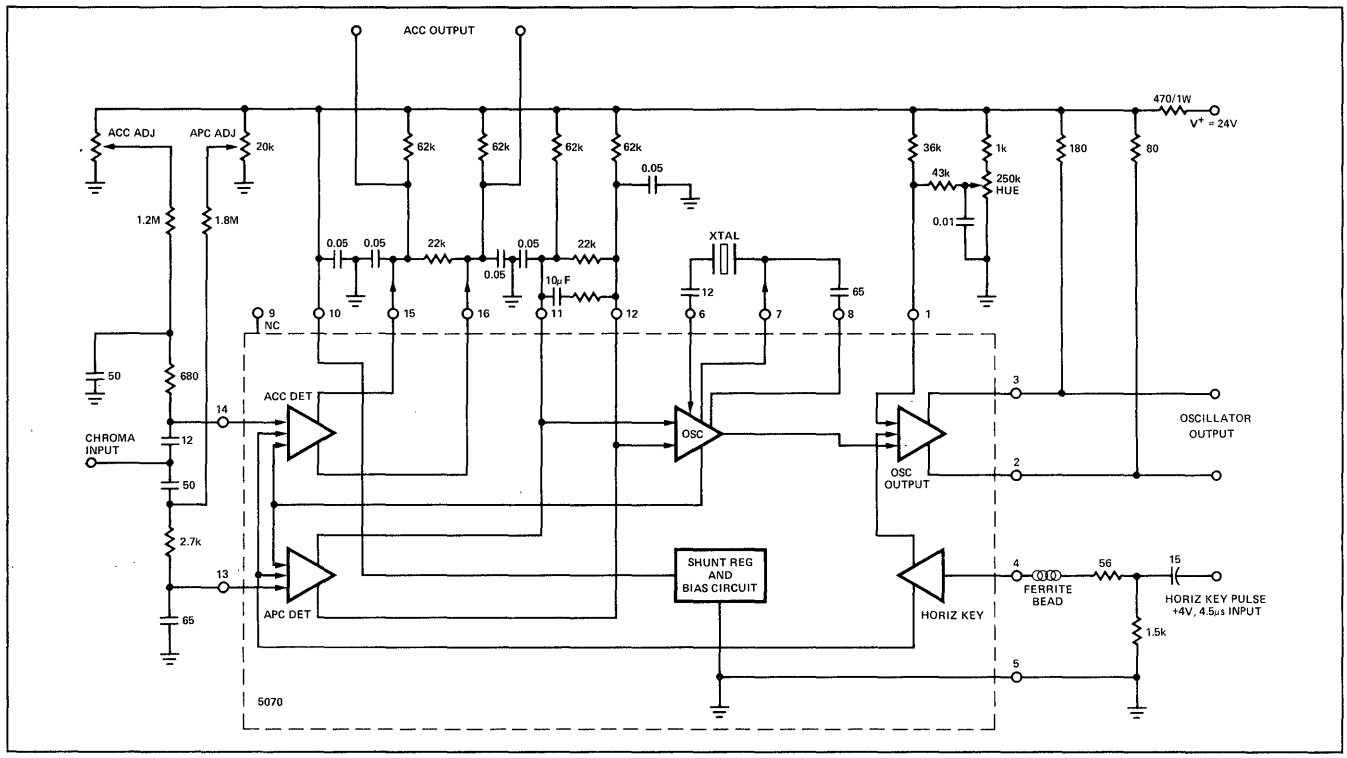
NOTES:

1. With respect to terminal No. 5 and with terminal No. 10 connected through 470Ω to +24V.
2. Regulated voltage at terminal No. 10.
3. Controlled by max. input current.
4. Limited by dissipation.

SCHEMATIC DIAGRAM



FUNCTIONAL DIAGRAM



NOTES:

1. All resistance values are in ohms
2. Unless otherwise indicated all capacitance values less than 10 are in microfarads – 10 or greater are in picofarads.

DESCRIPTION

The 5071 is a combined two-stage chroma amplifier and functional control circuit. The input signal is received from the video amplifier and applied to terminal No. 2 of the input amplifier stage. The first amplifier stage is part of the ACC system and is controlled by differential adjustment from the ACC input terminal Nos. 1 and 14. The output of the 1st amplifier is directed to terminal No. 6 from where the signal may be applied to the ACC detection system of the 5070 or an equivalent circuit. The output at terminal No. 6 is also applied to terminal No. 7 which is the input to the 2nd amplifier stage. Another output of the 1st amplifier at terminal No. 13 is directed to the killer adjustment circuit.

The dc voltage level at terminal No. 13 rises as the ACC differential voltage decreases with a reduction in the burst amplitude. At a pre-set condition determined by the killer adjustment resistor the killer circuit is activated and causes the 2nd chroma amplifier stage to be cut off. The 2nd chroma amplifier stage is also gain controlled by the adjustment or dc voltage at terminal No. 10. The output of the 2nd chroma amplifier stage is available at terminal No. 9. The typical output termination circuit that is shown, provides differential chroma drive signal to the demodulator circuit. Both amplifier outputs utilize emitter-followers with short-circuit protection.

FEATURES

- **ACC CONTROLLED CHROMA AMPLIFIER**
- **DC CHROMA GAIN CONTROL**
- **COLOR KILLER**
- **AMPLIFIER SHORT-CIRCUIT PROTECTION**

ABSOLUTE MAXIMUM RATINGS

(Values at $T_A = 25^\circ C$)

DC Supply Voltage (Terminal 8 to Terminal 14) — 30Vdc

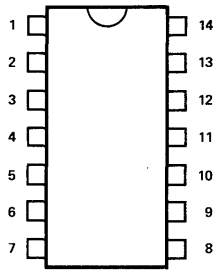
Device Dissipation:
- Up to $T_A = +70^\circ C$ — 530mW
- Above $T_A = +70^\circ C$ — Derate Linearly at 6.7 mW/°C

Ambient Temperature Range:
- Operating — -40 to +85°C
- Storage — -65 to +150°C

Lead Temperature (During Soldering):
- At distance 1/32 in (3.17 mm) from seating plane for 10s max. — +265°C

PIN CONFIGURATION

A PACKAGE
(Top View)



1. ACC Input
2. Chroma Input 1
3. Gain Preselect
4. Ground
5. NC
6. Chroma Output 1
7. Chroma Output 2
8. V+
9. Chroma Output 2
10. Chroma Level Control
11. Decouple
12. Decouple
13. Killer Adjust
14. ACC Input

ORDER PART NO. N5071A

MAXIMUM RATINGS MAXIMUM VOLTAGE & CURRENT RATINGS $T_A = 25^\circ C$

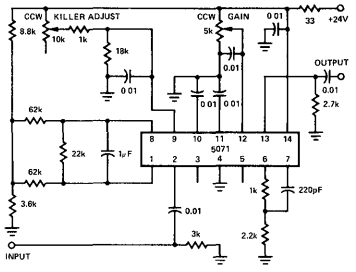
TERM NO.	Voltage (Note 1) MIN. VOLTS	MAX. VOLTS	TERM NO.	Current I_I mA	I_O mA
1	-5	+15	1	5	1.0
2	-5	+5	2	5	1.0
6	0	+24	6	1.0	20
7	-5	+5	7	5	1.0
8	0	+30	9	1.0	20
9	0	+24	12	1.0	5
10	0	+24	14	5	1.0
11	0	+24			
12	0	+20			
13	0	+20			
14	-5	+15			

NOTES:
1. With reference to terminal No. 4 and with +24V on terminal No. 8 except for the rating given for terminal No. 8.

ELECTRICAL CHARACTERISTICS (T_A = 25°C and V^+ = +24V)

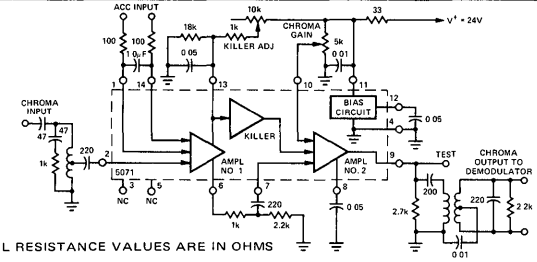
PARAMETERS	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
STATIC CHARACTERISTICS					
Voltages					
Bias Reference Terminal	S_1 Open, S_2 Open		17.3		V
Ampl No. 1 Chroma Input	S_1 Open, S_2 Open		1.75		V
Ampl No. 1 Chroma Output Balanced	S_1 Open, S_2 Open		20		V
Unbalanced	S_1 Open, S_2 Closed		13.5		V
Ampl No. 2 Chroma Input	S_1 Open, S_2 Open		1.5		V
Ampl No. 2 Chroma Output	S_1 Closed, S_2 Open		20.6		V
Supply Current	S_1 Open, S_2 Open	17		31	mA
DYNAMIC CHARACTERISTICS					
Amplifier No. 1 Voltage Gain	E_g = 30 mVrms Measure V6	14			dB
Amplifier No. 2 Voltage Gain	V_g = 10 Vrms		14		dB
Max. Chroma Output Voltage			2		Vrms
10% Chroma Gain Control Reference Voltage	E_g = 50 mVrms, adjust Chroma Gain Control to Change V_9 to 10% of Maximum Chroma Output		20.2		V
Output Voltage Killer Off	S_1 in Position 2 E_g = 50 mVrms, adjust "Killer Adjust" for an abrupt decrease in V_9			12	mV rms
Output Voltage, Chroma Off	E_g = 50 Vrms, adjust Chroms control to min. Chroma Output			12	mV rms
Bandwidth					
Amplifier No. 1			12		MHz
Amplifier No. 2			30		MHz
Ampl. No. 1 Input Impedance			2		kΩ
			4		pF
Ampl. No. 1 Output Impedance			35		Ω
Ampl. No. 2 Input Impedance			2.1		kΩ
			3.5		pF
Ampl. No. 2 Output Impedance			85		Ω

AMPLIFIER DIAGRAM



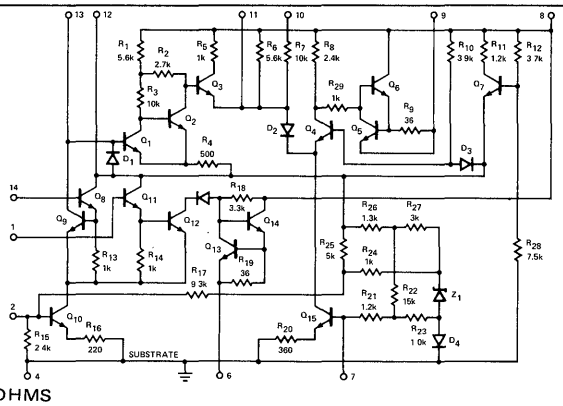
NOTE: All resistance in ohms
Unless otherwise specified, all capacitance are in microfarads.

FUNCTIONAL DIAGRAM



ALL RESISTANCE VALUES ARE IN OHMS
UNLESS OTHERWISE INDICATED, ALL CAPACITANCE VALUES LESS THAN 1.0 ARE IN MICROFARADS – 1.0 OR GREATER ARE IN PICOFARADS.

SCHEMATIC DIAGRAM



ALL RESISTANCE VALUES ARE IN OHMS

signetics

CHROMA DEMODULATOR | 5072

LINEAR INTEGRATED CIRCUITS

DESCRIPTION

The 5072 has two sets of synchronous detectors with matrix circuits to achieve the R-Y, G-Y, and B-Y color difference output signals. The chroma input signal is applied to terminal Nos. 3 and 4 while the oscillator injection signal is applied to terminal Nos. 6 and 7. The color difference signals, after matrix, have a fixed relationship of amplitude and phase nominally equal dc voltage levels. The outputs of the 5072 are suitable to driving high level color difference or R, G, B output amplifiers. Emitter-follower output stages used to drive the high level color amplifiers have short-circuit protection.

FEATURES

- **SYNCHRONOUS DETECTOR WITH COLOR DIFFERENCE MATRIX**
- **EMITTER-FOLLOWER OUTPUT AMPLIFIERS WITH SHORT-CIRCUIT PROTECTION**

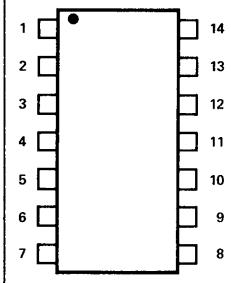
ABSOLUTE MAXIMUM RATINGS

(Values at $T_A = 25°C$)

DC Supply Voltage (Terminal 8 to Terminal 14)	27V
Reference Input Voltage	$5V_{p-p}$
Chroma Input Voltage	$5V_{p-p}$
Device Dissipation:	
Up to $T_A = +70°C$	530mW
Above $T_A = +70°C$	Derate Linearly at 6.7 mW/°C
Ambient Temperature Range:	
Operating	-40 to +85°C
Storage	-65 to +150°C
Lead Temperature (During Soldering):	
At distance 1/32 in (3.17 mm) from seating plane for 10s max.	+165°C

PIN CONFIGURATION

A PACKAGE
(Top View)



1. NC	8. V^+
2. NC	9. $E_G - E_Y$
3. Chroma (-)	10. NC
4. Chroma (+)	11. $E_R - E_Y$
5. NC	12. NC
6. Ref "B"	13. $E_B - E_Y$
7. Ref "A"	14. GND

ORDER PART NO. N5072A

MAXIMUM VOLTAGE & CURRENT RATINGS

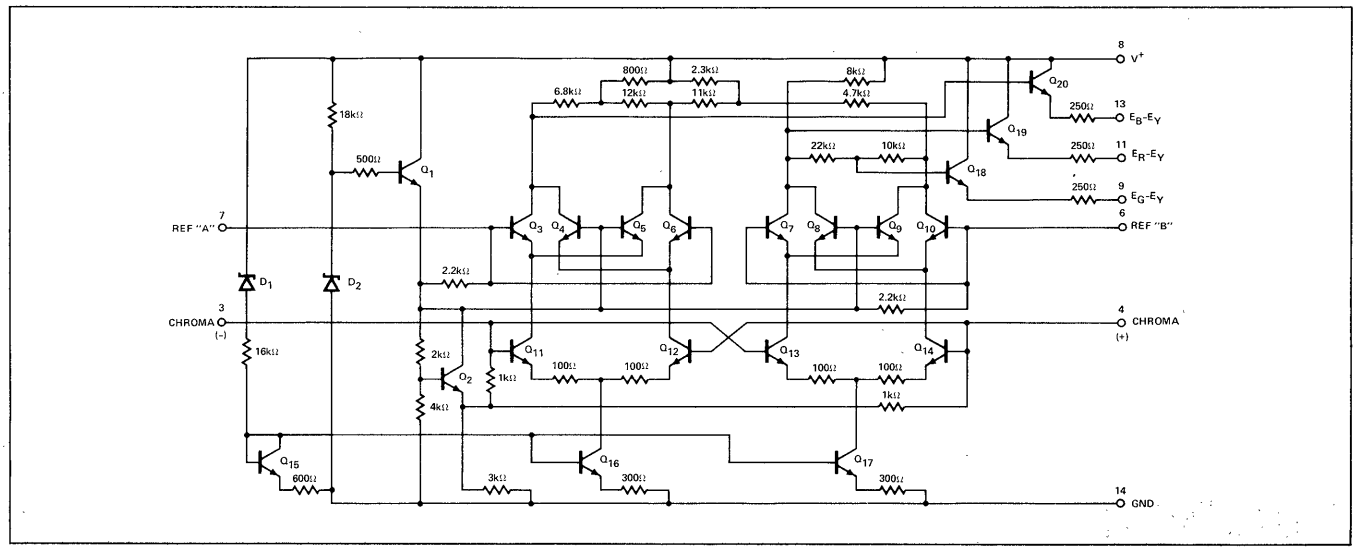
$T_A = 25°C$ **VOLTAGE (Note 1)** **CURRENT**

Terminal No.	MIN. VOLTS	MAX. VOLTS	Terminal No.	I_I mA	I_O mA
3	0	+5	3	-	-
4	0	+5	4	-	-
6	0	+12	6	-	-
7	0	+12	7	-	-
8	0	+27	8	-	-
9	0	-20	9	10	20
11	0	+20	11	10	20
13	0	+20	13	10	20

NOTE:

1. With reference to terminal No. 14 and with the voltage between terminal No. 8 and terminal No. 14 at +24 V except as given in rating for terminal No. 8.

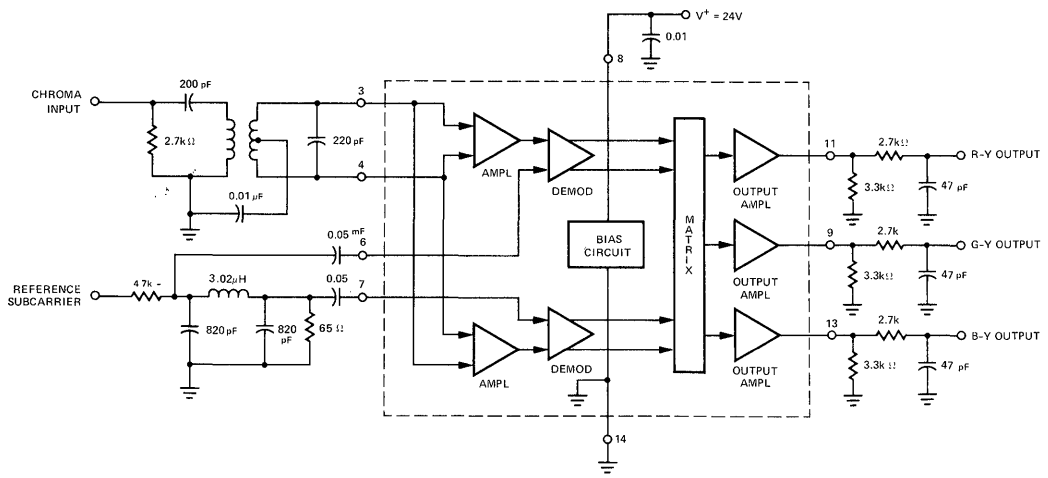
SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS (T_A = 25°C and V^+ = +24V unless otherwise specified)

PARAMETERS	TEST CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
STATIC CHARACTERISTICS					
Supply Current With Output Loads	S_1 Closed	16.5		26.5	mA
With No Output Loads	S_1 Open		9		mA
G-Y, R-Y, B-Y Outputs	S_1 Closed	13.2	14.7	15.8	V
Chroma Inputs	S_1 Open		3.3		V
Reference Subcarrier	S_1 Open		6.2		V
DYNAMIC CHARACTERISTICS					
Demodulator Unbalance	$V_3 = V_4 = 0$			0.8	
Maximum Color Difference Output Voltage	$V_3 = V_4 = 0.6$ Vp-p	8.0			Vp-p
		5.5			Vp-p
		1.2			Vp-p
Chroma Input Sensitivity	Adjust e_c for 5.0 Vp-o @ term		0.2	0.35	Vp-p
Relative R-Y Output	No. 13 (B-Y)	3.5		4.2	Vp-p
Relative G-Y Output		0.75		1.25	Vp-p
V_{DC} Difference Between any two Output Terminals	$e_c = 0$			0.6	V
Input Impedance Reference Subcarrier Inputs			1.7		kΩ
			6		pF
Input Impedance at Chroma Inputs			0.95		kΩ
			6		pF
Output Resistance			180		Ω

FUNCTIONAL DIAGRAM



DESCRIPTION

A unique method of FM detection by a new technique of linear gating is featured in the ULN2111 monolithic integrated circuit. This linear device comprises a three-stage limiter and a balanced product detector. Applications for the ULN2111 device include TV sound channels, FM receivers, automatic frequency control systems, and communication receivers.

Other applications for the ULN2111 device are in the more sophisticated circuitry in telemetry receivers, automatic control systems, and servo amplifiers.

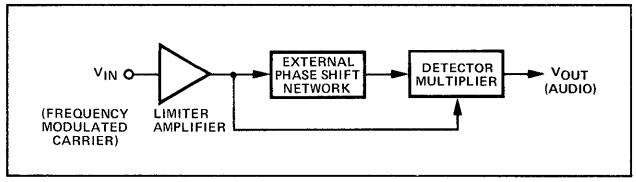
An outstanding feature of the ULN2111 is that only one, simple, low-cost, single winding coil is required for tuning. Consequently, only one screwdriver adjustment is required to tune a detector employing the ULN2111. The frequency range of the ULN2111 extends from 5 kHz to 50 MHz.

Outputs of 0.6V with a total distortion of less than 1% and a limiting threshold voltage of $400\mu V_{rms}$ are typical.

FEATURES

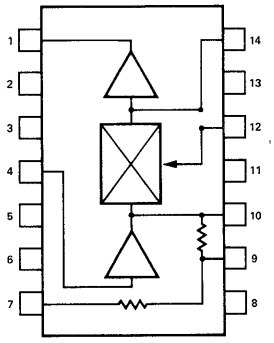
- **HIGH SENSITIVITY – INPUT LIMITING VOLTAGE AT 4.5MHz = 400μV**
- **HIGH IF VOLTAGE GAIN – 60dB**
- **SIMPLIFIED TUNING – ONE RLC PHASE SHIFT NETWORK**
- **HIGH STABILITY**
- **LOW DISTORTION – 1.0%**
- **WIDE FREQUENCY CAPABILITY – 5kHz to 50MHz**

BLOCK DIAGRAM



PIN CONFIGURATION

A PACKAGE
(Top View)



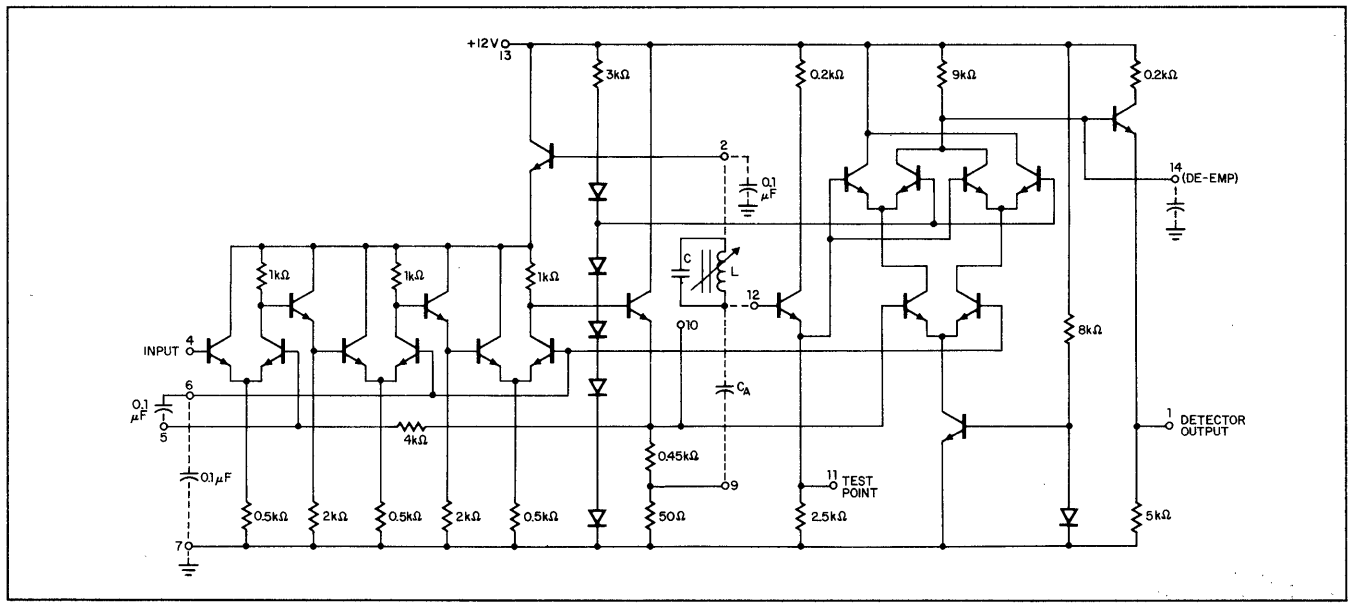
1. Audio Output
2. Detector Input Reference
3. No Connection
4. Input
5. Decoupling
6. Amplifier Input Reference
7. GND
8. No Connection
9. Amplifier Low Output
10. Amplifier High Output
11. Test Point
12. Detector Input
13. V^+
14. De-emphasis

ORDER PART NO. ULN2111A

ABSOLUTE MAXIMUM RATINGS

Input Voltage (Pin 4)	+3.5V
Output Voltage	+15V
Supply Voltage (V+)	+15V
Junction Temperature	+150°C
Storage Temperature	-65°C to +150°C
Operating Temperature	0°C to +85°C
Thermal Resistance	0.15°C/mW
$\theta_{J\text{-}A}$, Junction to Ambient	
Power Dissipation	300mW

BASIC CIRCUIT SCHEMATIC



ELECTRICAL CHARACTERISTICS: Standard Conditions: V_{CC} = +12V ±10%, T_A = 25°C

CHARACTERISTICS	SYMBOL	LIMITS				TEST CONDITIONS		TEST FIGURE	NOTES
		MIN	TYP	MAX	UNITS		Pin		
Supply Current	I_{CC}	12.0	17	22	mA		13		
Amplifier Input Reference	V_{bias}		1.45		V	Internally derived	6		
Detector Input Reference	V_{bias}		3.65		V	Internally derived	2		
Amplifier High Output Level	V_{oh}		1.45		V		10		
Amplifier Low Output Level	V_{ol}		0.145		V		9		
Detector Output Level	V_o	4.3	5.0	5.7	V		1		
Amplifier Input Resistance	R_{in}		5.0		KΩ		4		
Amplifier Input Capacitance	C_{in}		11		pF		4		
Detector Injection Input Resistance	R_{in}		70		KΩ		12		
Detector Injection Input Capacitance	C_{in}		2.7		pF		12		
Amplifier High Output Resistance	R_{out}		60		Ω		10		
Detector Output Resistance	R_{out}		200		Ω		1		
De-Emphasis Resistance	R_{de}		9		KΩ		14		
FM Detection for Television Applications:						Detector injection voltage = 60mV$_{rms}$, f_o = 4.5 MHz, F deviation = 25 kHz, Peak separation = 150 kHz, FM modulating frequency = 400 Hz, Amplifier source resistance = 50Ω.			
Amplifier Voltage Gain	V_g	55	58		dB	$V_{in} \leq 0.3mV_{rms}$, V_{cc} = 12V ±5%	10	1	
Amplifier Output Voltage	V_{oa}		1.45		V_{pp}	V_{in} = 10mV$_{rms}$	10	1	
Input Limiting Threshold	V_{th}		400	800	μV_{rms}		4	2	1
Recovered Audio Output	A_{vo}	0.5	0.6		V_{rms}		1	2	
Output Distortion	T_{hd}		1.5		%	100% FM Modulation	1	2	
AM Suppression	AMR	40	46		dB	V_{in} = 10mV$_{rms}$	1	3	2
FM Detection for 10.7 MHz Applications:						Detector injection voltage = 60mV$_{rms}$, f_o = 10.7 MHz, F deviation = 75 kHz, Peak separation = 550 kHz, FM modulating frequency = 400 Hz, Amplifier source resistance = 50Ω.			
Amplifier Voltage Gain	V_g		53		dB	$V_{in} \leq 0.3mV_{rms}$, V_{cc} = 12V ±5%.	10	1	
Amplifier Output Voltage	V_{oa}		1.45		V_{pp}	V_{in} = 10mV$_{rms}$	10	1	
Input Limiting Threshold	V_{th}		500		μV_{rms}		4	2	1
Recovered Audio Output	A_{vo}		0.45		V_{rms}		1	2	
Output Distortion	T_{hd}		1.0		%	100% FM modulation	1	2	
AM Suppression	AMR		40		dB	V_{in} = 10mV$_{rms}$	1	3	2

NOTES

1. The limiting threshold voltage is the FM input voltage V_i, expressed in rms volts, for a recovered V_{out} which is 3dB less than the recovered V_{out} at a V_i of 200mV$_{rms}$.
2. The Amplitude Modulation Rejection in decibels, often abbreviated AMR, is given by the following formula:

$$AMR = 20 \log \frac{V_{out} \text{ for 100\% FM modulated } V_i}{V_{out} \text{ for a 30\% AM } V_i}$$

USEAGE INFORMATION

1. FM DETECTION.
   a. Tuning. Apply FM modulated signal through DC decoupling network to pin 4, V_{in} = $5mV_{rms}$. Tune for maximum recovered audio at pin 1 or maximum RF voltage at pin 11.
   b. General
      (1) A DC path less than 100Ω shall be provided between pins 2 and 12. No other biasing provisions are required.

      (2) A DC path less than 300Ω should be provided between pins 4 and 6. No other biasing provisions are required.

      (3) The maximum AC load current can be increased by adding an external resistor between pins 1 and 7. The minimum value for this resistor is 800Ω, giving a maximum load current of $4mA_{rms}$.

2. EXTERNAL DECOUPLING AND MOUNTING CONSIDERATIONS.
   a. All decoupling capacitors should be ceramic type with minimum residual inductance at the operating frequency.
   b. Decoupling capacitor leads at pins 5, 6, and 12 should be as short as possible.
   c. Connections from pin 4 should be as far removed as possible from connections at pins 9, 10, and 12.
   d. The power supply pin 13 should be decoupled with a 0.1μF ceramic capacitor, keeping the leads as short as possible.
   e. When using a large internal impedance power supply (voltage dropping resistor), decouple pin 13 for the lowest audio demodulation frequency.
   f. Keep appropriate distances between the input coil and any other coil in the phase shift network for the voltage gain between these points is high (40 to 60dB).

TEST CIRCUITS

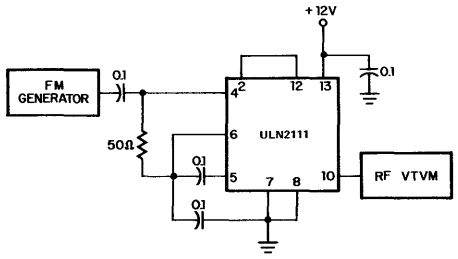


FIGURE 1

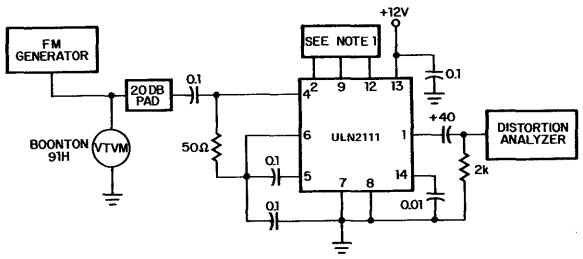


FIGURE 2

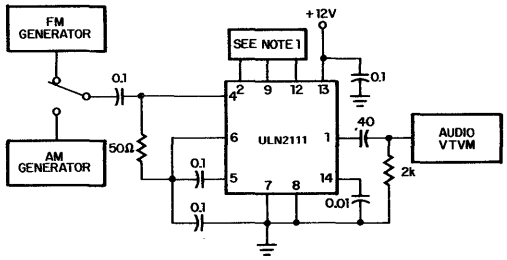


FIGURE 3

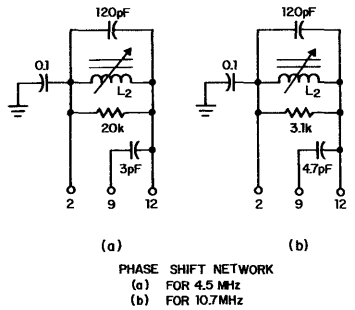
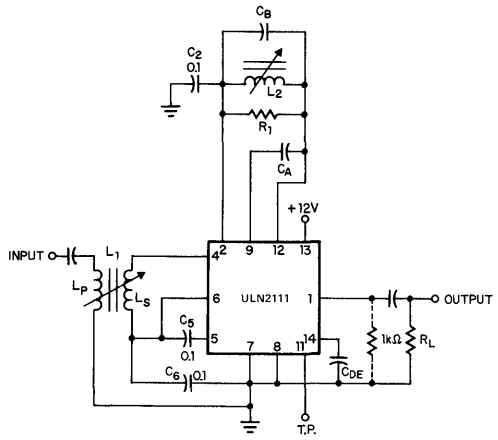


FIGURE 4

NOTES: 1. Phase shift network is specified in Figure 4. 2. All capacitors in microfarads unless otherwise noted.

APPLICATIONS

TYPICAL CIRCUIT REQUIREMENTS FOR FM DETECTION



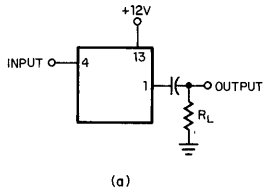
	Component Value		Notes
	TV (4.5 MHz)	FM (10.7 MHz)	
L_2 Inductance	7 - 14μH	1.5 - 3μH	1
L_2 Nom. Unloaded Q	50	50	
L_2 Nom. DC Resistance	50Ω	50Ω	
C_A	3.0pF	4.7pF	
C_B	120pF	120pF	2
R_1	20kΩ	3 1kΩ	
C_5 and C_6	30	20	
C_2	0.1μF	0.1μF	
C_{de}	0.01μF	0.01μF	

NOTES:

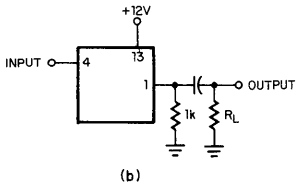
1. Suggested coil source: 1.5 - 3μH Miller 9050, 7 - 14μH Miller 9052.
2. Use NPO type capacitor.

Figure 5

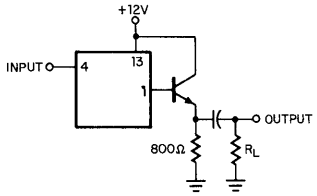
TYPICAL DRIVING CAPABILITIES at f_O = 4.5MHz



(a)



(b)

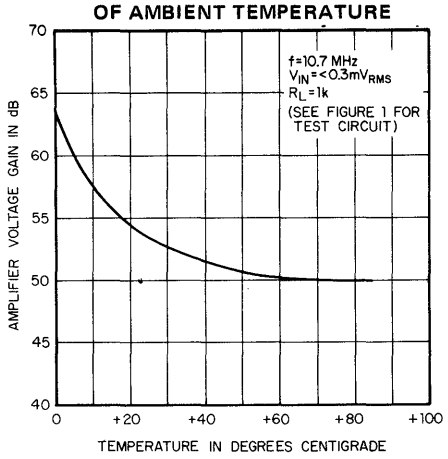


(c)

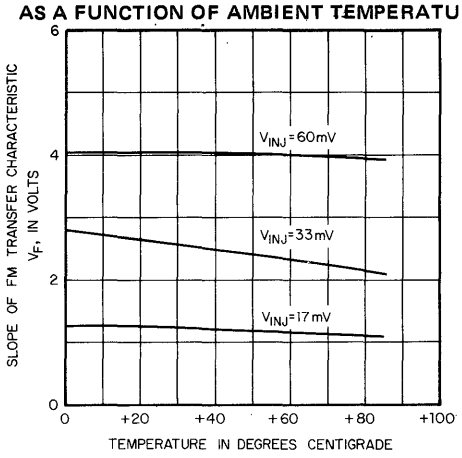
		V_o (mV_{rms})		
Figure	R_L (Ω)	Δf = 7.5 kHz	Δf = 25 kHz	Remarks
A	2000	220	650	No Clipping
B	200	130	400	No Clipping
C	200	220	650	Clipping at V_o=500mV_{rms}

Figure 6

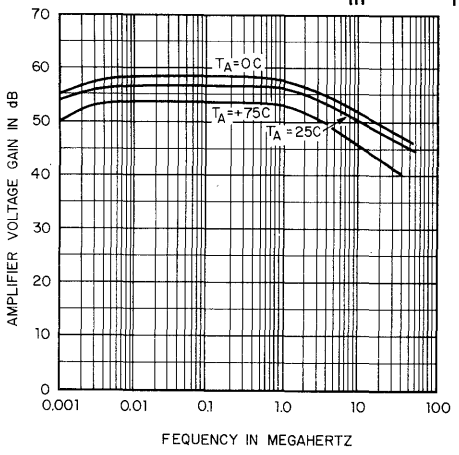
AMPLIFIER GAIN AS A FUNCTION OF AMBIENT TEMPERATURE

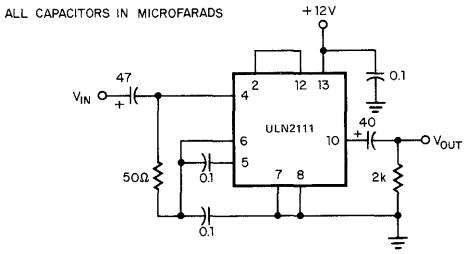


SLOPE OF FM TRANSFER CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

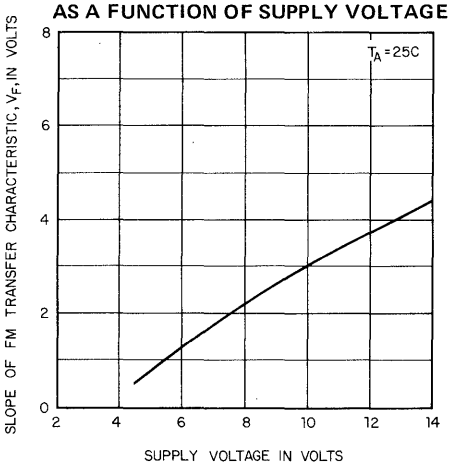


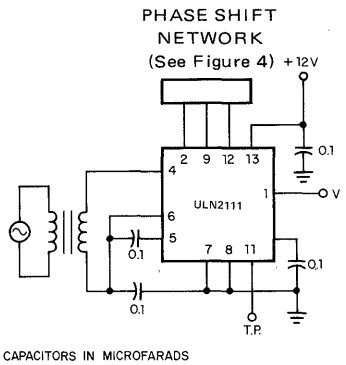
AMPLIFIER VOLTAGE GAIN AS A FUNCTION OF OPERATING FREQUENCY AT V_{in} = 0.2mV$_{ms}$





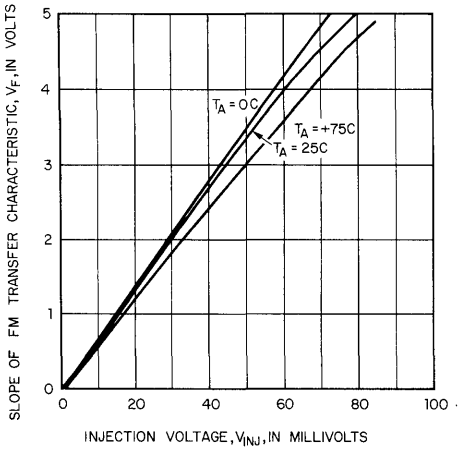
SLOPE OF FM TRANSFER CHARACTERISTIC AS A FUNCTION OF SUPPLY VOLTAGE

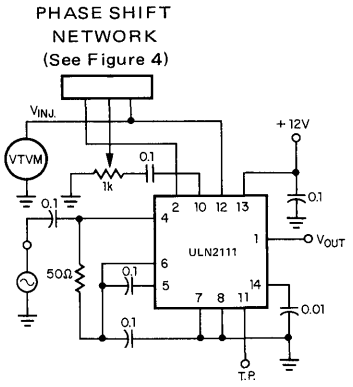




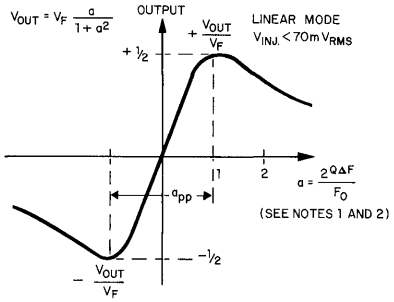
TYPICAL CHARACTERISTIC CURVES (Cont'd.)

SLOPE OF FM TRANSFER CHARACTERISTICS AS A FUNCTION OF INJECTION VOLTAGE





TRANSFER CHARACTERISTICS FOR A SIMPLE LC NETWORK



OUTPUT = ƒ (NORMALIZED DEVIATION)

(The units along the vertical axis are arbitrary units.)

Linear mode: Operation of the FM detector with no limiting after the phase shift network.

NOTES:

1. V_F defines the slope of the FM transfer characteristic, at origin:

$$V_f = \frac{dV_{out}}{da} \qquad a = 0$$

V_F is primarily a function of bias current in the detector and injection voltage.

V_F will decrease with decreasing V_{CC} or V_{INJ}.

2. a = normalized frequency deviation:

$$a = \frac{2Q\Delta F}{F_0}$$

SECTION 8
phase locked loops

DESCRIPTION

The NE560B Phase Locked Loop (PLL) is a monolithic signal conditioner, and demodulator system comprising a VCO, Phase Comparator, Amplifier and Low Pass Filter, interconnected as shown in the accompanying block diagram. The center frequency of the PLL is determined by the free running frequency (f_o) of the VCO. This VCO frequency is set by an external capacitor and can be fine tuned by an optional Potentiometer. The low pass filter, which determines the capture characteristics of the loop, is formed by the two capacitors and two resistors at the Phase Comparator output.

The PLL system has a set of self biased inputs which can be utilized in either a differential or single ended mode. The VCO output, in differential form, is available for signal conditioning frequency synchronization, multiplication and division applications. Terminals are provided for optional extended control of the tracking range, VCO frequency, and output DC level.

The monolithic signal conditioner-demodulator system is useful over a wide range of frequencies from less than 1 Hz to more than 15 MHz with an adjustable tracking range of ±1% to ±15%.

FEATURES

- FM DEMODULATION WITHOUT TUNED CIRCUITS
- NARROW BANDPASS - TO ± 1% ADJUSTABLE
- TRACKING RANGE
- EXACT FREQUENCY DUPLICATION IN HIGH
- NOISE ENVIRONMENT
- WIDE TRACKING RANGE ±15%
- HIGH LINEARITY - 1% DISTORTION MAX
- FREQUENCY MULTIPLICATION AND DIVISION
- THROUGH HARMONIC LOCKING

APPLICATIONS

TONE DECODERS

FM IF STRIPS

TELEMETRY DECODERS

DATA SYNCHRONIZERS

SIGNAL RECONSTITUTION

SIGNAL GENERATORS

MODEMS

TRACKING FILTERS

SCA RECEIVERS

FSK RECEIVERS

WIDE BAND HIGH LINEARITY DETECTORS

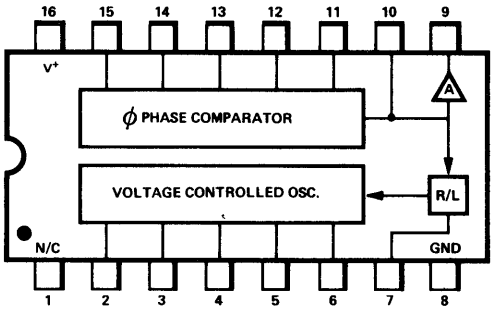
ABSOLUTE MAXIMUM RATINGS

Maximum Operating Voltage	26V
Input Voltage	1V Rms
Storage Temperature	-65°C to 150°C
Operating Temperature	0°C to 70°C
Power Dissipation	300 mw

Limiting values above which serviceability may be impaired

PIN CONFIGURATION

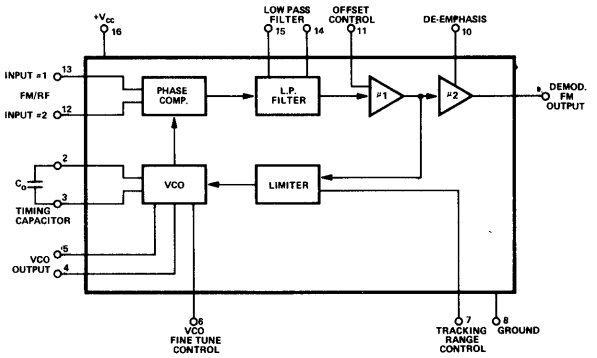
B PACKAGE
(Top View)



1. No Connection
2. VCO Timing Capacitor
3. VCO Timing Capacitor
4. VCO Output #2
5. VCO Output #1
6. Fine Tuning
7. Range Control
8. Ground (or Negative Power Supply)
9. Demodulated FM Output (an open emitter)
10. De-emphasis terminal (Audio bandshaping)
11. Offset Adjustment
12. FM/RF Input #1
13. FM/RF Input #2
14. Low Pass Loop Filter
15. Low Pass Loop Filter
16. Positive Power Supply

ORDER PART NO. NE560B

BLOCK DIAGRAM



GENERAL ELECTRICAL CHARACTERISTICS

(15KΩ Pin 9 to GND, Input Pin 12 or Pin 13 AC Ground Unused Input, Optional Controls Not Connected, V+ = 18V Unless Otherwise Specified $T_A = 25°C$)

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN	TYP	MAX	UNITS	
Lowest Practical Operating Frequency		0.1		Hz	
Maximum Operating Frequency	15	30		MHz	
Supply Current	7	9	11	Ma	
Minimum Input Signal for Lock		100		μV	
Dynamic Range		60		dB	
VCO Temp Coefficient*		±0.06	±0.12	%/°C	Measured at 2 MHz, with both inputs AC grounded
VCO Supply Voltage Regulation		±0.3	±2	%/V	Measured at 2 MHz
Input Resistance		2		KΩ	
Input Capacitance		4		Pf	
Input DC Level		+4		V	
Output DC Level	+12	+14	+16	V	
Available Output Swing		4		V_{p-p}	Measured at Pin 9
AM Rejection*	30	40		dB	See Figure 1
De-emphasis Resistance		8		KΩ	

*ACC Test Sub Group C.

ELECTRICAL CHARACTERISTICS (For FM Applications, Figure 2) (15KΩ Pin 9 to GND, Input Pin 12 or 13, AC Ground Unused Input, Optional Controls Not Connected, V+ = 18V Unless Otherwise Specified $T_A = 25°C$)

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN	TYP	MAX	UNITS	
10.7 MHz Operation **Deviation 75 kHz Source Impedance = 50Ω**					
Detection Threshold		120	300	μV	
Demodulated Output Amplitude	30	60		mV	V_{in} = 1 mv Rms Modulation Frequency 1 kHz
Distortion*		.3	1	% T.H.D.	V_{in} = 1 mv Rms Modulation Frequency 1 kHz
Signal to Noise Ratio $\frac{S+N}{N}$		35		dB	V_{in} = 1 mv Rms Modulation Frequency 1 kHz
4.5 MHz Operation **Deviation = 25 kHz, Source Impedance = 50Ω**					
Detection Threshold		120	300	μV	
Demodulated Output Amplitude	30	60		mV	V_{in} = 1 mv Rms Modulation Frequency 1 kHz
Distortion		0.3	1.0	% T.H.D.	V_{in} = 1 mv Rms Modulation Frequency 1 kHz
Signal to Noise Ratio $\frac{S+N}{N}$		35		dB	V_{in} = 1 mv Rms Modulation Frequency 1 kHz
Wide Deviation **$\Delta F/f_o$ = 5% Input = 4.5 MHz Deviation = 225 kHz @ 1 kHz Modulation Rate**					
Detection Threshold		1	5	mV	
Demodulated Output	0.2	0.5		Vrms	V_{in} = 5 mv Rms
Distortion		0.8		% T.H.D.	V_{in} = 5 mv Rms
Signal to Noise Ratio $\frac{S+N}{N}$		50		dB	V_{in} = 5 mv Rms

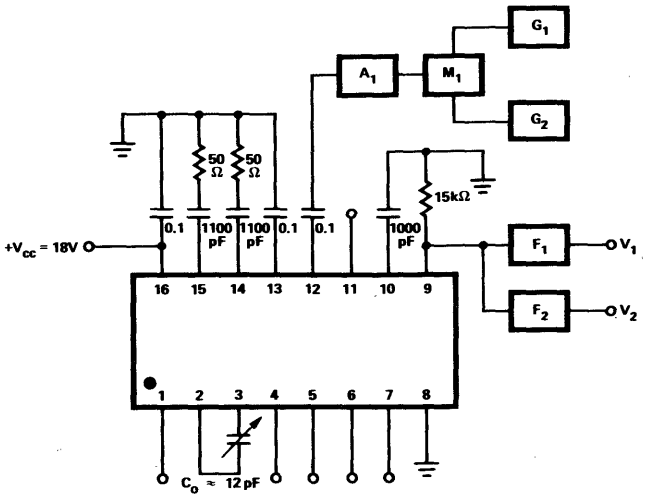
*ACC Test Sub Group C.

ELECTRICAL CHARACTERISTICS (For Tracking Filter, Figure 3) (15KΩ Pin 9 to GND, Input Pin 12 or Pin 13 AC Ground Unused Input, Optional Controls Not Connected, V+ = 18V Unless Otherwise Specified $T_A = 25°C$)

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN	TYP	MAX	UNITS	
Tracking Range	±5	±15		% of f_o	V_{in} = 5 mv Rms
Minimum Signal to Sustain Lock 0°C to 70°C		0.8		mv Rms	Input 2 MHz - See Characteristic Curves
VCO Output Impedance		1		kΩ	
VCO Output Swing	0.4	0.6		V_{p-p}	Input 2 MHz Measured with high impedance Probe with less than 10 Pf Capacitance
VCO Output DC Level		+6.5		V	
Side Band Suppression		35		dB	Input 2 MHz with ±100 kHz Side Band Separation and 3 kHz Low Pass Filter Input 1 mv Peak for Carrier Each Side Band C_1 = 0.01 μF R_1 = 0

TYPICAL TEST CIRCUITS

AM REJECTION



G_1 = FM Generator with $f_c = f_o \approx 4$ MHz, $\Delta f = 40$ kHz, $f_{mod} = 1$ kHz

G_2 = Audio Generator with $f_A = 400$ Hz

M_1 = Balanced Modulator Carrier Supplied by G_1, AM modulation provided by G_2.

A_1 = 50 Ω attenuator pad with signal level into pin 12 adjusted to 1 mV rms.

F_1 = 1 kHz Bandpass filter, Q = 20

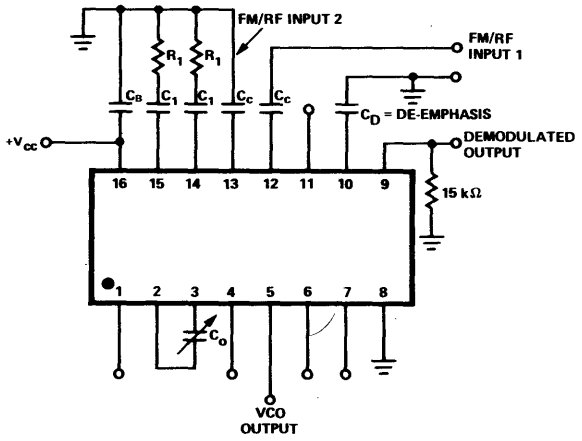
F_2 = 400 Hz Bandpass filter with Q = 50, with 1 kHz trap.

$$AMR = \frac{V_1}{V_2} \text{ in dB}$$

V_1 and V_2 are rms voltmeter readings.

Fig. 1

FM DEMODULATION

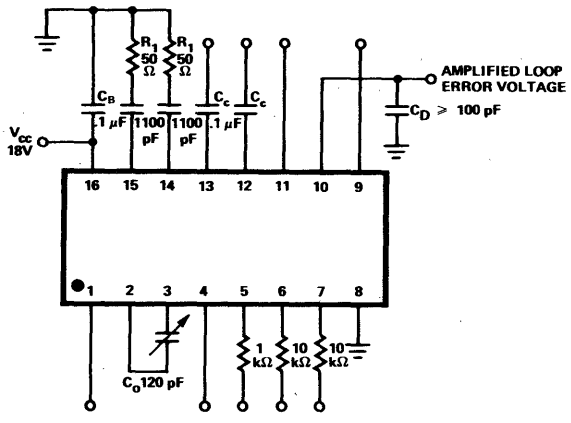


C_B = Bypass Capacitor
C_C = Coupling Capacitors
C_1 = Low Pass Filter Capacitors
C_o = Frequency Determining Capacitor

T_D = De-emphasis time constant
= (C_D) (8kΩ)

Fig. 2

TRACKING FILTER

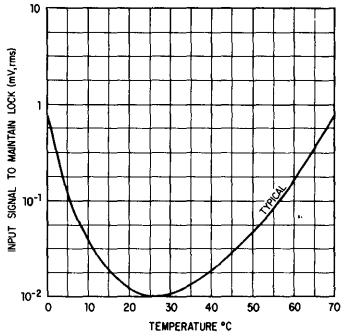


C_C = Coupling Capacitors
C_B = Bypass Capacitor
C_1 = Low Pass Filter Capacitor
C_o = VCO Frequency Set Capacitor

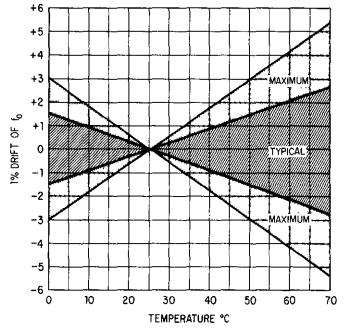
Fig. 3

TYPICAL CHARACTERISTIC CURVES

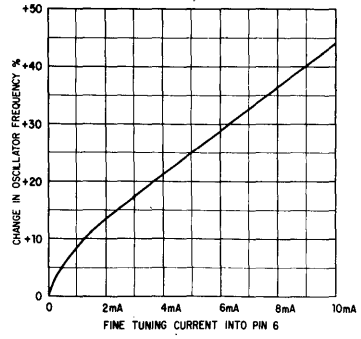
MINIMUM INPUT SIGNAL AMPLITUDE NECESSARY TO MAINTAIN LOCK AS A FUNCTION OF TEMPERATURE WITH $f_{signal} = fo_{25°C} = 2.0$ MHz



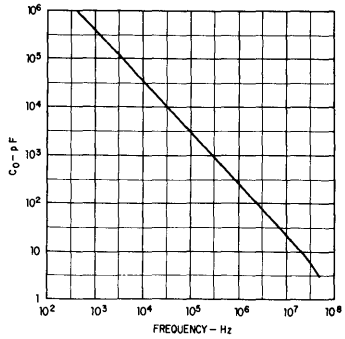
THERMAL DRIFT OF VCO FREE RUNNING FREQUENCY (f_o)



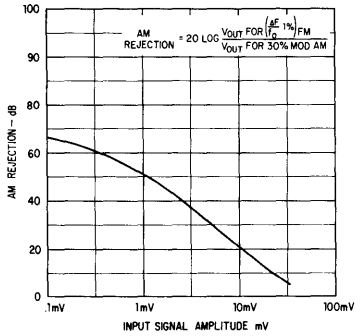
CHANGE OF FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF FINE TUNING CIRCUIT



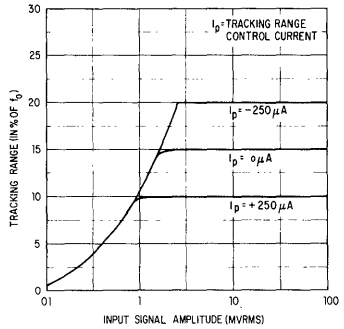
FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF VCO TIMING CAPACITANCE



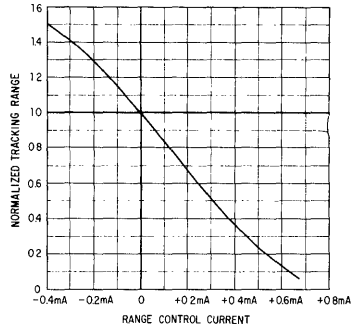
AM REJECTION AS A FUNCTION OF INPUT SIGNAL LEVEL f_o = 10 MHz



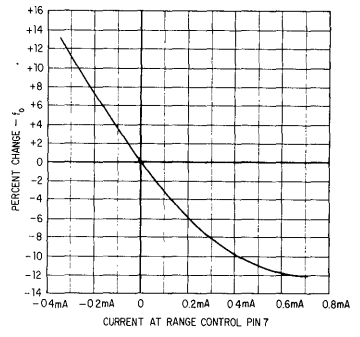
TYPICAL TRACKING RANGE AS A FUNCTION OF INPUT SIGNAL



CHANGE OF FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF RANGE CONTROL CURRENT

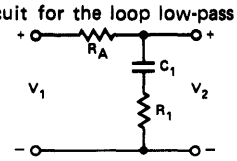


NORMALIZED TRACKING RANGE AS A FUNCTION OF RANGE CONTROL CURRENT



EXTERNAL CONTROLS

1. **Loop Low Pass Filter (Pins 14 and 15)**
   The equivalent circuit for the loop low-pass filter can be represented as:



   where RA (6K Ω) is the effective resistance seen looking into Pin #14 or Pin #15.
   The corresponding filter transfer characteristics are:

$$\frac{V_2}{V_1}(S) = (S) = \frac{1 + S R_1 C_1}{1 + S (R_1 + R_A) C_1}$$

   where S is the complex frequency variable.

2. **Loop Gain (Threshold) Control**
   The overall Phase Locked Loop gain can be reduced by connecting a feedback resistor, R_F, across the low-pass filter terminals, Pins #14 and #15. This causes the loop gain and the detection sensitivity to decrease by a factor α ($\alpha<1$)
   where:

$$\alpha = \frac{R_F}{2 R_A + R_F}$$

   Reduction of loop gain may be desirable at high input signal levels (V_{in} > 30 mV) and at high frequencies (f_o >5 MHz) where excessively high loop gain may cause instability.

3. **Tracking Range Control (Pin 7)**
   Any bias current, I_p, injected into the tracking range control, reduces the tracking range of the PLL by decreasing the output of the limiter. The variation of the tracking range and the center frequency, as a function of I_p, are shown in the characteristic curves with I_p defined positive going into the tracking range control terminal. This terminal is normally at a DC level of +0.6 Volts and presents an impedance of 600 Ω.

4. **External Fine Tuning (Pin 6)**
   Any bias current injected into the fine tuning terminal increases the frequency of oscillation, f_o, as shown in the characteristic curves. This current is defined Positive into the fine tuning terminal. This terminal is at a typical DC level of +1.3 Volts and has a dynamic impedance of 100Ω to ground.

5. **Offset Adjustment (Pin 11)**
   Application of a bias voltage to the offset adjustment terminal modifies the current in the output amplifier setting the DC level at the output. The effect on the loop is to modify the relationship between the VCO free running frequency and the lock range, allowing the VCO free running frequency to be positioned at different points throughout the lock range.

   Nominally this terminal is at +4V DC and has an input impedance of 3K Ω. The offset adjustment is optional. The characteristics specified correspond to operation of the circuit with this terminal open circuited.

6. **De-emphasis Filter (Pin 10)**
   The de-emphasis terminal is normally used when the PLL is used to demodulate Frequency Modulated Audio signals. In this application, a capacitor from this terminal to ground provides the required de-emphasis. For other applications, this terminal may be used for band shaping the output signal. The 3 dB bandwidth of the output amplifier in the system block diagram (see Figure 2 .) is related to the de-emphasis capacitor, C_D, as:

$$f_{3dB} = \frac{1}{2 \quad R_a \, C_D}$$

   where R_D is the 8000 ohm resistance seen looking into the de-emphasis terminal.
   When the PLL system is utilized for signal conditioning, and the loop error voltage is not utilized, de-emphasis terminal should be AC grounded.

DESCRIPTION

The NE561B Phase Locked Loop (PLL) is a monolithic signal conditioner, and demodulator system comprising a VCO, Phase Comparator, Amplifier and Low Pass Filter, interconnected as shown in the accompanying block diagram. The center frequency of the PLL is determined by the free running frequency (f_o) of the VCO. This VCO frequency is set by an external capacitor and can be fine tuned by an optional Potentiometer. The low pass filter, which determines the capture characteristics of the loop is formed by the two capacitors and two resistors at the Phase Comparator output.

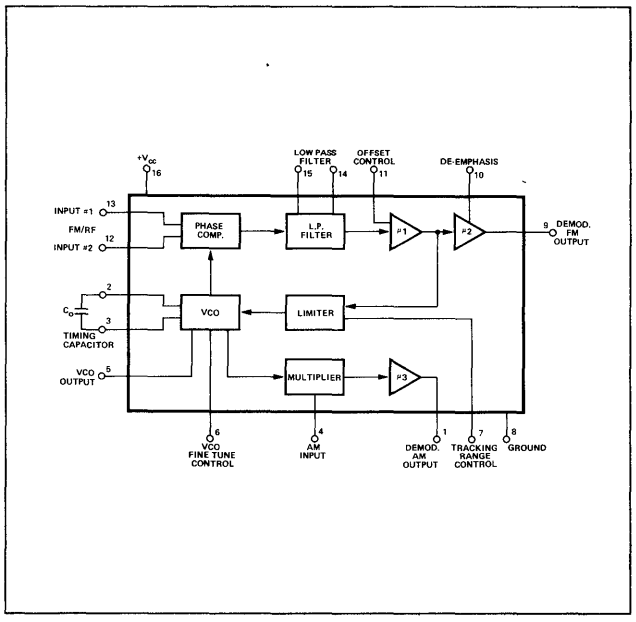
The PLL system has a set of self biased inputs which can be utilized in either a differential or single ended mode. The VCO output is available for signal conditioning, frequency synchronization, multiplication and division applications. Terminals are provided for optional external control of the tracking range, VCO frequency, and output DC level. An analog multiplier block is incorporated into the PLL system to provide frequency selective synchronous AM detection capability.

The monolithic signal conditioner-demodulator system is useful over a wide range of frequencies from less than 1 Hz to more than 15 MHz with an adjustable tracking range of ±1% to ±15%.

FEATURES

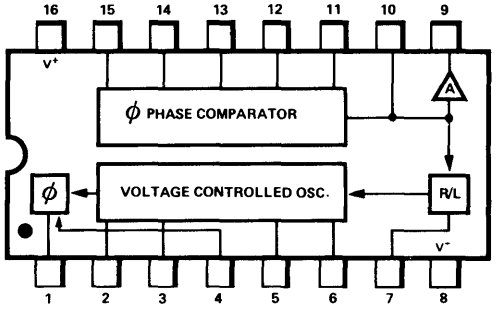
- FM DEMODULATION WITHOUT TUNED CIRCUITS
- SYNCHRONOUS AM DETECTION
- NARROW BAND PASS TO ±1%
- EXACT FREQUENCY DUPLICATION IN HIGH NOISE ENVIRONMENT
- ADJUSTABLE TRACKING RANGE
- WIDE TRACKING RANGE ±15%
- HIGH LINEARITY - 1% DISTORTION MAX
- FREQUENCY MULTIPLICATION AND DIVISION THROUGH HARMONIC LOCKING

BLOCK DIAGRAM



PIN CONFIGURATION

B PACKAGE



1. Demodulated Am Output
2. VCO Timing Capacitor
3. VCO Timing Capacitor
4. AM Input
5. VCO Output
6. Fine Tuning
7. Range Control
8. Ground (V^-)
9. Demodulated FM Output (an open emitter)
10. De-emphasis terminal (audio band shaping)
11. Offset Adjustment
12. FM/RF Input #1
13. FM/RF Input #2
14. Low Pass Loop Filter
15. Low Pass Loop Filter
16. V^+

ORDER PART NO. NE561B

ABSOLUTE MAXIMUM RATINGS

Maximum Operating Voltage	26V
Input Voltage	1V RMS
Storage Temperature	-65°C to 150°C
Operating Temperature	0°C to 70°C
Power Dissipation	300mW

Limiting values above which serviceability may be imparied

APPLICATIONS

- TONE DECODERS
- AM-FM-IF STRIPS
- TELEMETRY DECODERS
- DATA SYNCHRONIZERS
- SIGNAL RECONSTITUTION
- SIGNAL GENERATORS
- MODEMS
- TRACKING FILTERS
- SCA RECEIVERS
- FSK RECEIVERS
- WIDE BAND HIGH LINEARITY DETECTORS
- SYNCHRONOUS DETECTORS
- AM RECEIVER

GENERAL ELECTRICAL CHARACTERISTICS

(15KΩ Pin 9 to GND, Input Pin 12 or Pin 13 AC Ground Unused Input, Optional Controls Not Connected, V+ = 18V Unless Otherwise Specified $T_A = 25°C$)

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN	TYP	MAX	UNITS	
Lowest Practical Operating Frequency		0.1		Hz	
Maximum Operating Frequency	15	30		MHz	
Supply Current	8	10	12	Ma	
Minimum Input Signal for Lock		100		μV	
Dynamic Range		60		dB	
VCO Temp Coefficient*		±0.06	±0.12	%/°C	Measured at 2 MHz, with both inputs AC grounded
VCO Supply Voltage Regulation		±0.3	±2	%/V	Measured at 2 MHz
Input Resistance		2		kΩ	
Input Capacitance		4		pF	
Input DC Level		+4		V	
Output DC Level	+12	+14	+16	V	
Available Output Swing		4		V_{p-p}	Measured at Pin 9
AM Rejection*	30	40		dB	See Figure 3
De-emphasis Resistance		8		kΩ	

*ACC Test Sub Group C.

ELECTRICAL CHARACTERISTICS (For FM Applications, Figure 2) (15KΩ Pin 9 to GND, Input Pin 12 or 13,AC Ground Unused Input, Optional Controls Not Connected, V+ = 18V Unless Otherwise Specified $T_A = 25°C$)

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN	TYP	MAX	UNITS	
10.7 MHz Operation **Deviation 75 kHz Source Impedance = 50Ω**					
Detection Threshold		120	300	μV	
Demodulated Output Amplitude	30	60		mV	Vin = 1 mv Rms Modulation Frequency 1 kHz
Distortion*		.3	1	% T.H.D.	Vin = 1 mv Rms Modulation Frequency 1 kHz
Signal to Noise Ratio $\frac{S+N}{N}$		35		dB	Vin = 1 mv Rms Modulation Frequency 1 kHz
4.5 MHz Operation **Deviation = 25 kHz, Source Impedance = 50Ω**					
Detection Threshold		120	300	μV	
Demodulated Output Amplitude	30	60		mV	Vin = 1 mv Rms Modulation Frequency 1 kHz
Distortion		0.3	1.0	% T.H.D.	Vin = 1 mv Rms Modulation Frequency 1 kHz
Signal to Noise Ratio $\frac{S+N}{N}$		35		dB	Vin = 1 mv Rms Modulation Frequency 1 kHz
Wide Deviation **$\Delta F/f_o$ = 5% Input = 4.5 MHz Deviation = 225 kHz @ 1 kHz modulation rate**					
Detection Threshold		1	5	mV	
Demodulated Output	0.2	0.5		Vrms	Vin = 5 mv Rms
Distortion		0.8		% T.H.D.	Vin = 5 mv Rms
Signal to Noise Ratio $\frac{S+N}{N}$		50		dB	Vin = 5 mv Rms

*ACC Test Sub Group C.

ELECTRICAL CHARACTERISTICS (For Tracking Filter, Figure 1) (15KΩ Pin 9 to GND, Input Pin 12 or Pin 13 AC Ground Unused Input, Optional Controls Not Connected, V+ = 18V Unless Otherwise Specified $T_A = 25°C$)

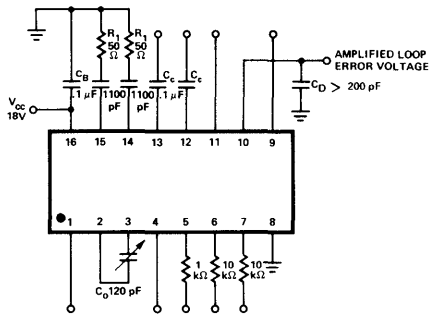
CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN	TYP	MAX	UNITS	
Tracking Range	±5	±20		% of f_o	Vin 5 mv Rms
Minimum Signal to Sustain Lock 0°C to 70°C		0.8		mv Rms	Input 2 MHz - See Characteristic Curves
VCO Output Impedance		1		kΩ	
VCO Output Swing	0.4	0.6		V_{p-p}	Input 2 MHz Measured with high impedance. Probe with less than 10 pF capacitance.
VCO Output DC Level		+6.5		V	
Side Band Suppression		35		dB	Input 2 MHz with ±100 kHz Sideband Separation and 3 kHz Low Pass Filter. Input 1 mv Peak for Carrier and each Sideband $C_1 = 0.01\ \mu F$ $R_1 = 0$

ELECTRICAL CHARACTERISTICS (For AM Synchronous Detector, Figure 4) (15KΩ Pin 9 to GND, Input Pin 12 or Pin 13 AC Ground Unused Input, Optional Controls Not Connected, V+ = 18V Unless Otherwise Specified $T_A = 25°C$)

CHARACTERISTICS	LIMITS				TEST CONDITIONS
	MIN	TYP	MAX	UNITS	
Input Impedance		3		kΩ	
Output Impedance		8		kΩ	
Output DC Level	+10	+14	+17	V	
AM Conversion Gain	3	12		dB	See Definition of Terms
Out of Band Rejection		30		dB	See Definition of Terms
Distortion		1•		% T.H.D.	

TYPICAL TEST CIRCUITS

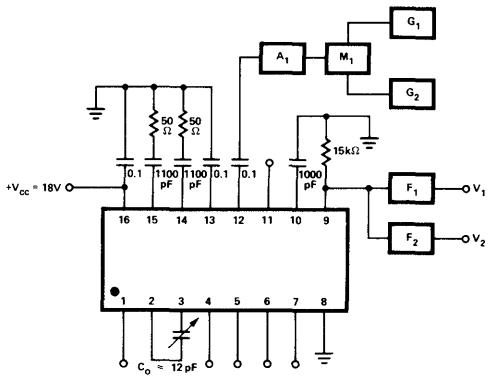
TEST CIRCUIT FOR TRACKING FILTER



C_C = Coupling Capacitors
C_B = Bypass Capacitor
C_1 = Low Pass Filter Capacitor
C_0 = VCO Frequency Set Capacitor

FIGURE 1

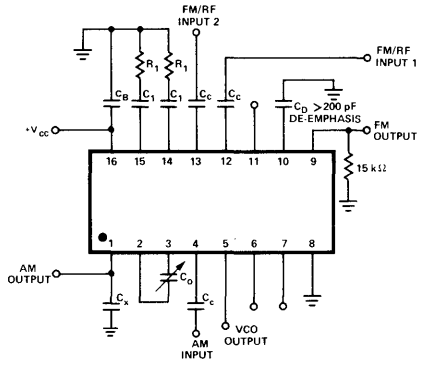
TEST CIRCUIT FOR AM REJECTION



G_1 = FM Generator with f_c = fo ≈ 4 MHz, Δf = 40 kHz, f_{mod} = 1 kHz
G_2 = Audio Generator with f_A = 400 Hz
M_1 Balanced Modulator Carrier Supplied by G_1, AM modulation provided by G_2
A_1 = 50Ω attenuator pad with signal level into pin 12 adjusted to 1 mV rms.
F_1 = 1 kHz Bandpass filter, Q = 20
F_2 = 400 Hz Bandpass filter with Q = 50, with 1 kHz trap.
AMR = $\frac{V_1}{V_2}$ in dB V_1 and V_2 are rms voltmeter readings.

FIGURE 3

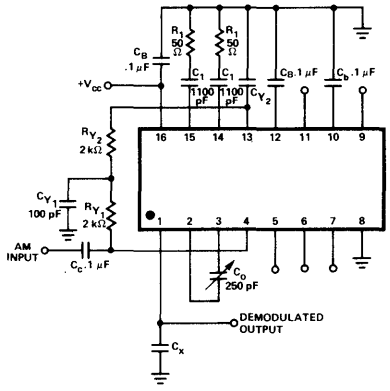
TEST CIRCUIT FOR FM DEMODULATION



C_B = Bypass Capacitor
C_C = Coupling Capacitors
C_1 = Low Pass Filter Capacitors
C_0 = Frequency Determining Capacitors
C_x = AM Post Detection Filter

FIGURE 2

TEST CIRCUIT FOR AM SYNCHRONOUS DETECTOR

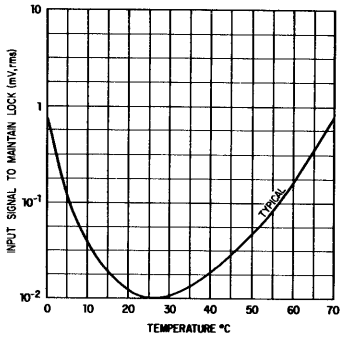


C_B = Bypass Capacitor
C_C = Coupling Capacitor
$Ry_1Cy_1 = Ry_2Cy_2 = \frac{1}{2\pi fo}$
C_x = AM Post Detection Filter

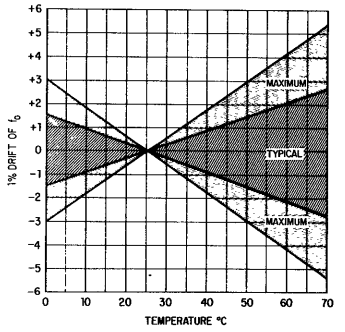
FIGURE 4

TYPICAL CHARACTERISTIC CURVES

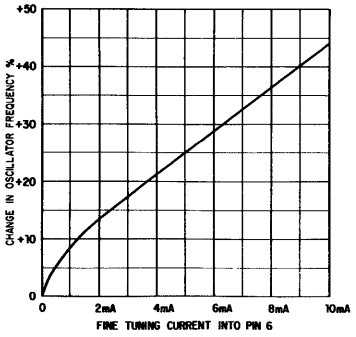
MINIMUM INPUT SIGNAL AMPLITUDE NECESSARY TO MAINTAIN LOCK AS A FUNCTION OF TEMPERATURE WITH $f_{signal} = fo_{25^oC} = 2.0$ MHz



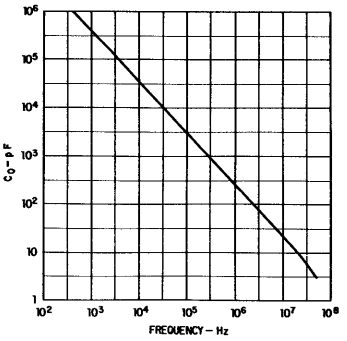
THERMAL DRIFT OF VCO FREE RUNNING FREQUENCY (f_o)



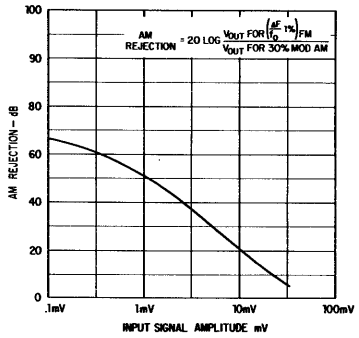
CHANGE OF FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF RANGE CONTROL CURRENT



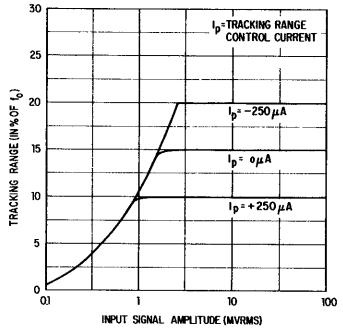
FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF VCO TIMING CAPACITANCE



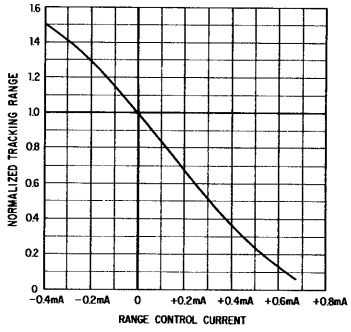
AM REJECTION AS A FUNCTION OF INPUT SIGNAL LEVEL f_o = 10 MHz



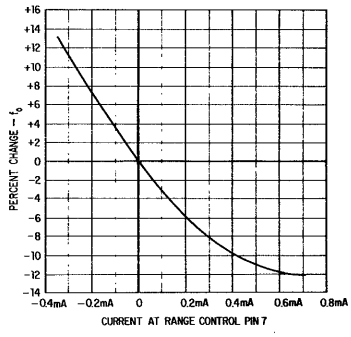
TYPICAL TRACKING RANGE AS A FUNCTION OF INPUT SIGNAL



CHANGE OF FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF FINE TUNING CIRCUIT



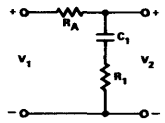
NORMALIZED TRACKING RANGE AS A FUNCTION OF RANGE CONTROL CURRENT



EXTERNAL CONTROLS

1. **Loop Low Pass Filter (Pins 14 and 15)**

The equivalent circuit for the loop low-pass filter can be represented as:



where RA (6kΩ) is the effective resistance seen looking into Pin #14 or Pin #15.

The corresponding filter transfer characteristics are:

$$\frac{V_2}{V_1}(S) = F(S) = \frac{1 + S R_1 C_1}{1 + S (R_1 + R_A) C_1}$$

where S is the complex frequency variable.

2. **Loop Gain (Threshold) Control**

The overall Phase Lock of loop gain can be reduced by connecting a feedback resistor, R_F, across the low-pass filter terminals, Pins #14 and #15. This causes the loop gain and the detection sensitivity to decrease by a factor ($\alpha < 1$), where

$$\alpha = \frac{R_F}{2R_A + R_F}$$

Reduction of loop gain may be desirable at high input signal levels (V_{in} >30 mV) and at high frequencies (f_o > 5MHz) where excessively high PLL loop gain may cause instability within the loop.

3. **Tracking Range Control (Pin 7)**

Any bias current, I_P, injected into the tracking range control, reduces the tracking range of the PLL by decreasing the output of the limiter. The variation of the tracking range and the center frequency, as a function of I_P, are shown in the characteristic curves with I_P defined positive going into the tracking range control terminal. This terminal is normally at a DC level of +0.6 Volts and presents an impedance of 600Ω.

4. **External Fine Tuning (Pin 6)**

Any bias current injected into the fine tuning terminal increases the frequency of oscillation, f_o, as shown in the characteristic curves. This current is defined Positive into the fine tuning terminal. This terminal is at a typical DC level of +1.3 Volts and has a dynamic impedance of 100Ω to ground.

5. **Offset Adjustment (Pin 11)**

Application of a bias voltage to the offset adjustment terminal modifies the current in the output amplifier setting the DC level at the output. The effect on the loop is to modify the relationship between the VCO free running frequency and the lock range, allowing the VCO free running frequency to be positioned at different points throughout the lock range.

Nominally this terminal is at +4V DC and has an input impedance of 3kΩ. The offset adjustment is optional. The characteristics specified correspond to operation of the circuit with this terminal open circuited.

6. **De-emphasis Filter (Pin 10)**

The de-emphasis terminal is normally used when the PLL is used to demodulate Frequency Modulated Audio signals. In this application, a capacitor from this terminal to ground provides the required de-emphasis. For other applications, this terminal may be used for band shaping the output signal. The 3 dB bandwidth of the output amplifier in the system block diagram (see Figure 2 .) is related to the de-emphasis capacitor, C_D, as:

$$f_{3dB} = \frac{1}{2\pi R_D C_D}$$

where R_D is the 8000 ohm resistance seen looking into the de-emphasis terminal.

When the PLL system is utilized for signal conditioning, and the loop error voltage is not utilized, de-emphasis terminal should be AC grounded.

7. **AM Post-Detection Filter (Pin 1)**

The capacitor C_x connected between Pin #1 and ground serves as a low-pass filter for synchronous AM detection with a transfer characteristic, $F_2(S)$, given as:

$$F_2(S) = \frac{1}{1 + SR_x C_x}$$

where R_x = 8kΩ is the resistance seen looking into Pin #1.

DESCRIPTION

The NE562B Phase Locked Loop (PLL) is a monolithic signal conditioner and demodulator system, comprising a VCO, phase comparator, amplifier and low pass filter, interconnected as shown in the accompanying block diagram. The center frequency of the PLL is determined by the free running frequency (f_O) of the VCO. This VCO frequency is set by an external capacitor. The low pass filter, which determines the capture characteristics of the loop, is formed by two capacitors and two resistors at the phase comparator output.

This PLL has two sets of differential inputs, one for the FM/RF input and one for the phase comparator local oscillator input. Both sets of inputs can be used in either a differential or single-ended mode. The FM/RF inputs to the comparator are self-biased. An internally regulated voltage source is provided to bias the phase comparator local oscillator inputs. The VCO output, at high level and in differential form, is available for driving logic circuits in signal conditioning and synchronization, frequency multiplication and division applications. Terminals are also provided for the optional extension of the tracking range. The monolithic signal conditioner-demodulator system is useful over a wide range of frequencies from less than 1 Hz to more than 15 MHz with an adjustable tracking range of ±1% to ±15%

FEATURES

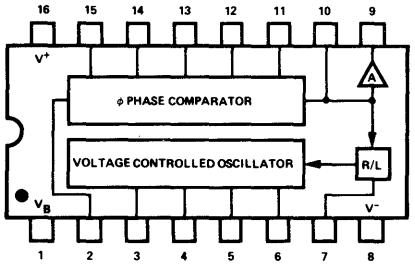
- FREQUENCY MULTIPLICATION AND DIVISION
- SIGNAL CONDITIONING AND SIDE-BAND SUPPRESSION
- FM DEMODULATION WITHOUT TUNED CIRCUITS
- NARROW BANDPASS – TO ±1%
- ADJUSTABLE TRACKING RANGE – TO ±15%
- EXACT FREQUENCY DUPLICATION IN HIGH NOISE ENVIRONMENT
- HIGH LINEARITY – 1% DISTORTION MAXIMUM AT 1% DEVIATION

APPLICATIONS

FREQUENCY SYNTHESIZERS
DATA SYNCHRONIZERS
SIGNAL CONDITIONING
TRACKING FILTERS
TELEMETRY DECODERS
MODEMS
FM IF STRIPS AND DEMODULATORS
TONE DECODERS
FSK RECEIVERS
WIDEBAND HIGH LINEARITY FM DEMODULATORS

PIN CONFIGURATION

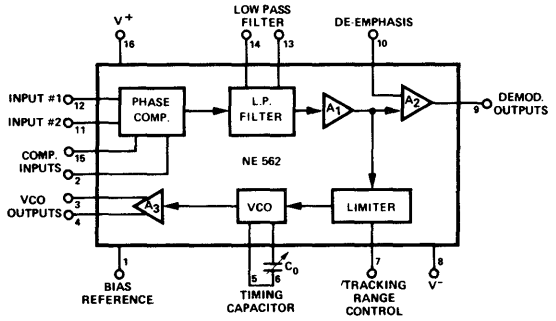
B PACKAGE
(Top View)



1. Bias Reference Voltage
2. Phase Comparator Input #1
3. VCO Output #1
4. VCO Output #2.
5. VCO Timing Capacitor
6. VCO Timing Capacitor
7. Range Control
8. Negative Power Supply (Ground)
9. Demodulated FM Output (an open emitter)
10. De-emphasis (Audio Bandshaping)
11. RF Input #1
12. RF Input #2
13. Low-Pass Loop Filter
14. Low-Pass Loop Filter
15. Phase Comparator Input #2
16. Positive Power Supply

ORDER PART NO. NE562B

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Limiting values above which serviceability may be impaired)

Maximum Operating Voltage	30V
Input Voltage	3V rms
Storage Temperature	-65°C to 150°C
Operating Temperature	0°C to 70°C
Power Dissipation	300mW

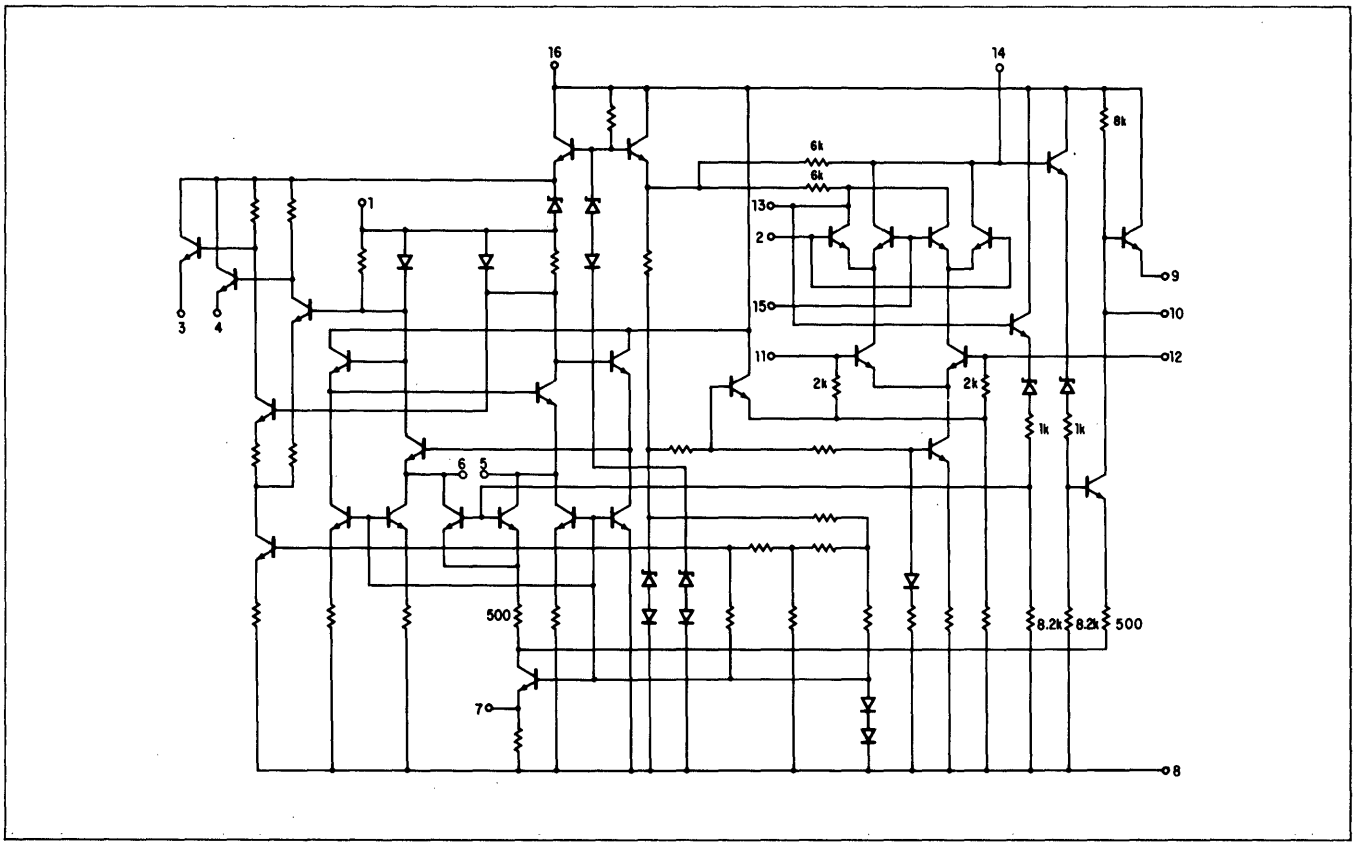
GENERAL ELECTRICAL CHARACTERISTICS

(15,000 ohms pin 9 to ground, 12,000 ohms pins 3 and 4 to ground, pins 2 and 15 to pin 1 through 1000 ohms, input to pin 11 or 12 with unused input at AC ground, range control not connected and V^+ = 18 volts unless otherwise specified. T_A = 25°C.)

CHARACTERISTICS	LIMITS			UNITS	TEST CONDITIONS
	MIN	TYP	MAX		
Lowest Practical Operating Frequency		0.1		Hz	
Maximum Operating Frequency	15	30		MHz	
Supply Current	10	12	14	mA	
Minimum Input Signal for Lock		200		μV	
Dynamic Range		80		dB	
VCO Temp Coefficient*		±0.06	±0.15	%/°C	Measured at 2 MHz
VCO Supply Voltage Regulation		±0.3	±2	%/V	Measured at 2 MHz
Input Resistance		2		kΩ	
Input Capacitance		4		pF	
Input DC Level	+12	+14	+16	V	
Output DC Level	+12	+14	+16	V	
Available Output Swing		4		$V_{p\text{-}p}$	Measured at Pin 9
AM Rejection*	30	40		dB	See Definition of Terms
De-emphasis Resistance		8		kΩ	
Bias Reference		+8		V	

*ACC Test Sub Group C.

SCHEMATIC DIAGRAM



ELECTRICAL CHARACTERISTICS FOR FM APPLICATIONS (15,000 ohms pin 9 to ground, input to pin 11 or pin 12, AC ground unused input, range control not connected and $V^+ = 18$ volts. $T_A = 25°C$.)

CHARACTERISTICS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
10.7 MHz Operation	**Deviation 75 kHz Source Impedance = 50Ω**				
Detection Threshold		200	500	μV	
Demodulated Output Amplitude	30	70		mV rms	V_{in} = 1 mV rms Modulation Frequency 1 kHz
Distortion*		0.5		% T.H.D.	V_{in} = 1 mV rms Modulation Frequency 1 kHz
Signal to Noise Ratio $\frac{S+N}{N}$		35		dB	V_{in} = 1 mV rms Modulation Frequency 1 kHz
4.5 MHz Operation	**Deviation = 25 kHz, Source Impedance = 50Ω**				
Detection Threshold		200	500	μV	
Demodulated Output Amplitude	30	60		mV rms	V_{in} = 1 mV rms Modulation Frequency 1 kHz
Distortion		0.5		% T.H.D.	V_{in} = 1 mV rms Modulation Frequency 1 kHz
Signal to Noise Ratio $\frac{S+N}{N}$		35		dB	V_{in} = 1 mV rms Modulation Frequency 1 kHz
Wide Deviation	**$\Delta F/f_o$ = 5% Input = 4.5 MHz Deviation = 225 kHz @ 1 kHz Modulation Rate**				
Detection Threshold		1	5	mV	
Demodulated Output		1		V rms	V_{in} = 5 mV rms
Distortion	0.3	0.8		% T.H.D.	V_{in} = 5 mV rms
Signal to Noise Ratio $\frac{S+N}{N}$		50		dB	V_{in} = 5 mV rms

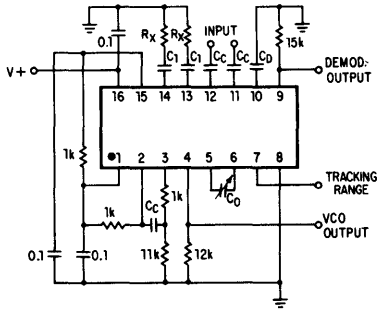
*ACC Test Sub Group C.

ELECTRICAL CHARACTERISTICS FOR SIGNAL CONDITIONER AND FREQUENCY SYNTHESIS APPLICATIONS (Input to pin 11 or pin 12, AC ground unused input, range control not connected, $V^+ = 18$ volts. $T_A = 25°C$.)

CHARACTERISTIC	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Tracking Range	±5	±15		% of f_o	200 mV p-p square wave input
Input Resistance		2		kΩ	
Input Capacitance		4		pF	
Input DC Level		4		V	
VCO Output Impedance		1.3	2.5	kΩ	
VCO Output Swing	3	4.5		V p-p	
VCO Output DC Level		12		V	
VCO Signal/Noise Ratio		60		dB	Inputs at AC ground

TEST CIRCUIT

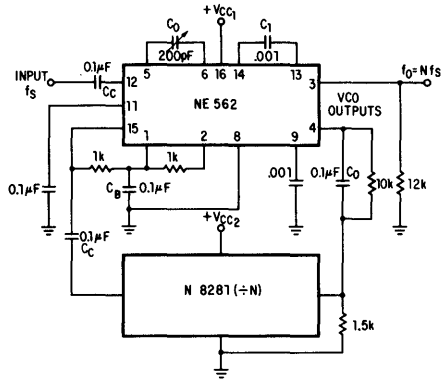
TEST CIRCUIT FOR FM DEMODULATION



C_B = Bypass Capacitor
C_C = Coupling Capacitor
C_D = .01μF for Standard FM Broadcasting
C_1 and R_X = Low Pass Filter
C_O = Frequency set Capacitor

FIGURE 1

TEST CIRCUIT FOR SIGNAL CONDITIONER AND FREQUENCY SYNTHESIS APPLICATIONS



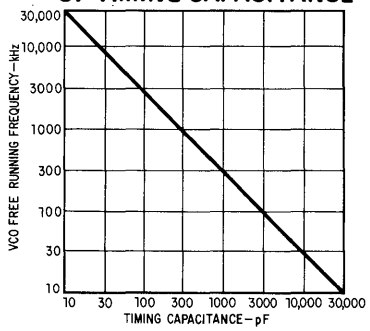
C_B = Bypass Capacitor
C_C = Coupling Capacitor
C_1 = Low Pass Filter Capacitor
C_O = Frequency Capacitor Set

Note: Fanout to divide by N counter is one.

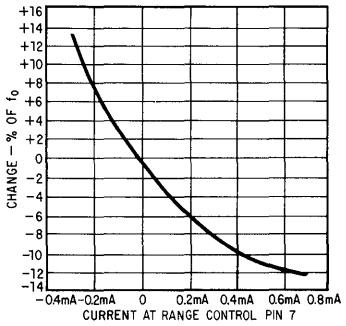
FIGURE 2

TYPICAL CHARACTERISTIC CURVES

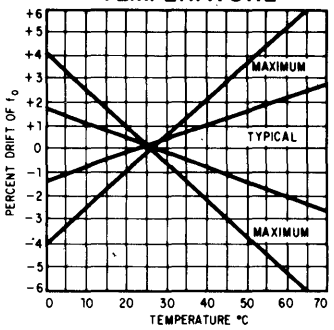
FREE RUNNING VOLTAGE CONTROLLED OSCILLATOR FREQUENCY AS A FUNCTION OF TIMING CAPACITANCE



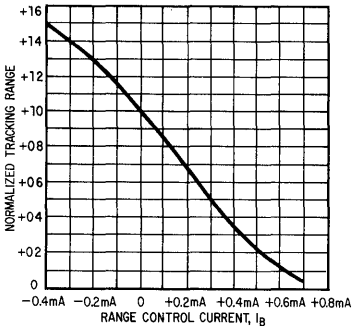
CHANGE OF FREE RUNNING OSCILLATOR FREQUENCY AS A FUNCTION OF RANGE CONTROL CURRENT



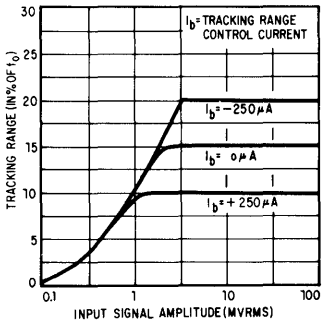
THERMAL DRIFT OF FREE RUNNING FREQUENCY AS A FUNCTION OF TEMPERATURE



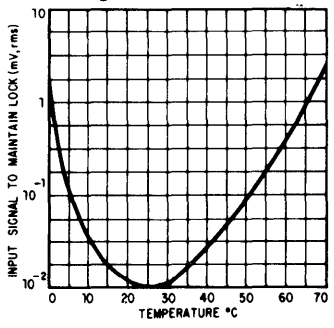
NORMALIZED TRACKING RANGE AS A FUNCTION OF RANGE CONTROL CURRENT



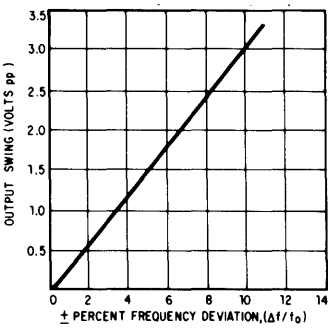
TYPICAL TRACKING RANGE AS A FUNCTION OF INPUT SIGNAL AMPLITUDE



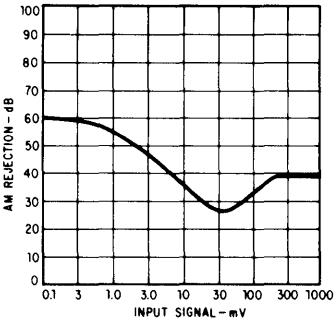
INPUT SIGNAL AMPLITUDE TO MAINTAIN LOCK AS A FUNCTION OF TEMPERATURE ($f_{signal} = f_o = 2.0$ MHz)



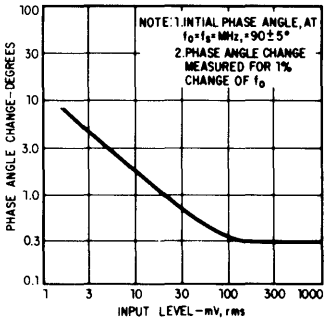
562 PHASE LOCKED LOOP DEMODULATED OUTPUT SWING AS A FUNCTION OF % FM DEVIATION



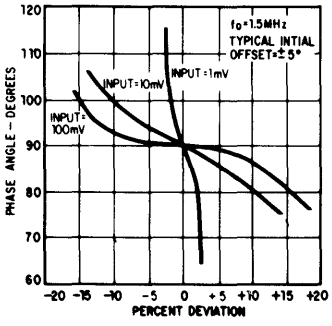
AM REJECTION AS A FUNCTION OF INPUT SIGNAL LEVEL



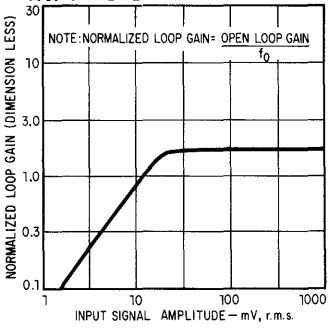
CHANGE IN PHASE ANGLE, f_o RELATIVE TO f_s, AS A FUNCTION OF INPUT SIGNAL AMPLITUDE



VCO OUTPUT PHASE AS A FUNCTION OF PERCENT FREQUENCY DEVIATION



NORMALIZED LOOP GAIN AS A FUNCTION OF INPUT SIGNAL AMPLITUDE



562 APPLICATIONS INFORMATION

1. BIAS REFERENCE

Pin 1 of the 562 is an internally regulated bias reference voltage supply which should be used as a source of bias current for the phase comparator input terminals, Pins 2 and 15. Biasing may be achieved as shown in Figure 3.

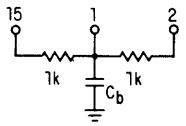


FIGURE 3

2. PHASE COMPARATOR LOOP INPUTS

Of the Signetics high frequency phase locked loops, the 562 is unique in that the loop is open between the VCO and the phase comparator. Once biasing of the comparator is accomplished, as described in Bias Reference above, loop closure can be accomplished by capacitive coupling between either one or both inputs of the phase comparator and the VCO output. A divider or counter may be enclosed in the loop at this point for frequency synthesis applications or a flip-flop may be used to ensure that the output waveform has a 50% duty cycle. If large signal swings, greater than 2 volts, are to be applied to the phase comparator inputs, a 1000 ohm current limiting buffer resistor should be used in series with the coupling capacitors.

3. VCO OUTPUT

Square wave VCO outputs of both polarities (0°C and 180°C) buffered by an amplifier are available at pins 3 and 4. For proper operation of the buffer amplifier, pins 3 and 4 must be returned to ground (or the negative supply) through resistors, typically 12,000 ohms. The value of these resistors may be reduced provided that total power dissipated in the 562 does not exceed 300 milliwatts or the total average current in each emitter does not exceed 4 mA. The output amplitude is typically 4.5 volts peak referenced at +12 volts with respect to pin 8.

4. VCO TUNING

Setting the free-running frequency of the VCO is accomplished easily with one timing capacitor connected between pins 5 and 6. For the 562 Phase Locked Loop, fine tuning of the free-running frequency may be accomplished in either or both of two ways. The first method uses a trimmer capacitor connected in parallel with the VCO timing capacitor. This is the simplest technique and requires the smallest number of extra components but at the lower frequencies may be difficult to implement. The second technique incorporates two resistors and a voltage source. The resistors are connected between each of the timing capacitor terminals and a voltage source as shown in Figure 4.

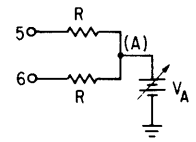


FIGURE 4

The percent change in the VCO free-running frequency, f_o, as a function of the voltage applied to point (A) is shown in the curves of Figure 5. Note that with this fine tuning technique, it is possible to *increase* the VCO free-running frequency to a value greater than possible with just a trimmer capacitor alone. A formula for the approximation of the VCO frequency as a function of the voltage at point (A), the resistance values and the starting frequency, is given below:

$$f = f_o\left[1 - \frac{V_A - 6.4}{1300R}\right]$$

The recommended resistance range of R is 20,000 to 60,000 ohms.

CHANGE IN VCO FREQUENCY AS A FUNCTION OF FINE TUNING VOLTAGE

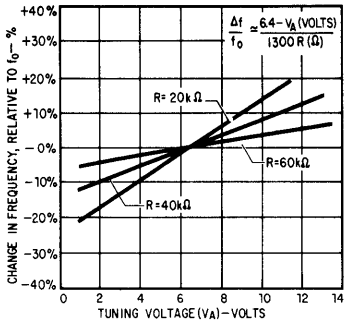


FIGURE 5

5. LOOP GAIN CHARACTERISTICS

The overall open loop gain of the 562 PLL can be expressed as: $K_0 = K_1K_2$

where:

K_0 = total open loop gain

K_1 = phase comparator and amplifier conversion gain

K_2 = VCO conversion gain

The VCO conversion gain, K_2, is the change of VCO frequency per unit of error voltage. In this particular design, it is numerically equal to the VCO frequency, i.e.,

$K_2 = f_o$ Hz/Volt

or

$K_2 = 2\pi f_o$ radians/Volt-second

The phase comparator and amplifier conversion gain, K_1, is proportional to input signal amplitude for low input levels, $V_S \leq 40$mV rms, and it is constant and equal to about 1.5 volts/radian for higher input amplitudes. Therefore, K_1 can be approximated as:

$$K_1 \cong \frac{.04\,V_S}{\sqrt{1 + \left(\frac{V_S}{40}\right)^2}}$$

where

V_S = input signal in mV rms.

562 APPLICATIONS INFORMATION (Cont'd.)

6. SIGNAL INPUT

The input structure is basically differential and may be used in this manner. Biasing is supplied to the input terminals from an internal regulated supply so signal inputs must be capacitively coupled. In most applications where the input is single-ended, the unused input should be bypassed to ground.

7. DEMODULATED OUTPUT

Pin 9 is a low impedance output terminal for the loop error voltage. It is at this point that the demodulated FM output is obtained. When used, it must be biased by a resistor to ground (or negative supply), and the resistor value may be adjusted downward provided that the output current does not exceed 5mA or the dissipation in the 562 does not exceed the absolute maximum ratings. When not used, pin 9 may be left open.

8. DE-EMPHASIS FILTER

The de-emphasis terminal, pin 10, is normally required when the PLL is used to demodulate Frequency Modulated Audio signals. In this application, a capacitor from this terminal to ground provides the required de-emphasis. For other applications it may be used to shape the output response. The 3 dB bandwidth of the output amplifier is related to the de-emphasis capacitor, C_D, as:

$$f_{3dB} = \frac{1}{2\pi R_D C_D}$$

where R_D is 8000 ohms.

When the PLL system is utilized for applications not requiring the use of the output amplifier, pin 10 should be by-passed to ground.

9. TRACKING RANGE CONTROL (Pin 7)

Any bias current, I_p, injected into the tracking range control, reduces the tracking range of the PLL by decreasing the output of the limiter. The variation of the tracking range and the center frequency, as a function of I_p, are shown in the characteristic curves with I_p defined positive going into the tracking range control terminal. This terminal is normally at a DC level of +0.6 volts and presents an impedance of 600Ω.

10. LOW-PASS FILTER

In most applications, a loop low-pass filter should be connected between pins 13 and 14 and ground. It is used to set the loop response time, controlling the capture range and the rejection of out of band information. Four filter configurations and their transfer functions are shown in Figures 6 through 9. For VCO operating frequencies below 5 MHz, configurations shown in Figures 6 and 7 may be used. At higher frequencies, configurations shown in Figures 8 and 9 should be used to ensure loop stability. R is the impedance seen looking into the low pass filter terminals, Pins 13 and 14; and, in the 562, is nominally 6000 ohms.

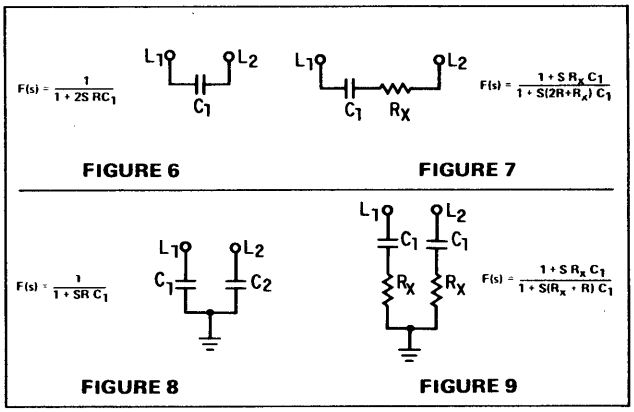


FIGURE 6 FIGURE 7

FIGURE 8 FIGURE 9

11. LOOP GAIN (Threshold) CONTROL

The overall Phase Locked Loop gain can be reduced by connecting a resistor, R_F, across the low-pass filter terminals, pins 13 and 14. This causes the loop gain and the detection sensitivity to decrease by a factor α, where:

$$\alpha = \frac{R_F}{12{,}000 + R_F}$$

Reduction of loop gain may be desirable at operating frequencies greater than 5 MHz because, at these frequencies, high loop gain may cause instability.

12. STATIC LOOP PHASE-ERROR

When the PLL is in lock, the VCO outputs have a nominal ±90°C phase shift with respect to the input signal. Due to internal offsets, this nominal angle at perfect lock condition may shift a few degrees, typically ±5°C or less.

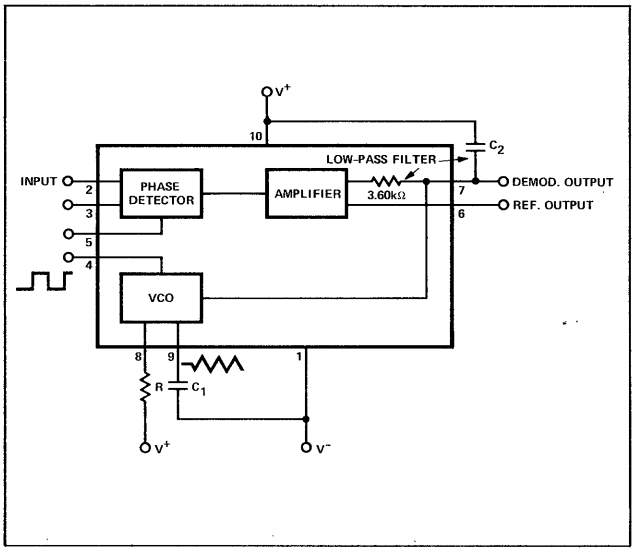
DESCRIPTION

The SE/NE565 Phase-Locked Loop (PLL) is a self-contained, adaptable filter and demodulator for the frequency range from 0.001 Hz to 500 kHz. The circuit comprises a voltage-controlled oscillator of exceptional stability and linearity, a phase comparator, an amplifier and a low-pass filter as shown in the block diagram. The center frequency of the PLL is determined by the free-running frequency of the VCO; this frequency can be adjusted externally with a resistor or a capacitor. The low-pass filter, which determines the capture characteristics of the loop, is formed by an internal resistor and an external capacitor.

FEATURES

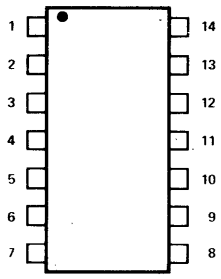
- EXTREME STABILITY OF CENTER FREQUENCY (200ppm/°C typ)
- WIDE RANGE OF OPERATING VOLTAGE (±5 to ±12 VOLTS) WITH VERY SMALL FREQUENCY DRIFT (100ppm/% typ)
- VERY HIGH LINEARITY OF DEMODULATED OUTPUT (0.2% typ)
- CENTER FREQUENCY PROGRAMMING BY MEANS OF A RESISTOR, CAPACITOR, VOLTAGE OR CURRENT
- TTL AND DTL COMPATIBLE SQUARE-WAVE OUTPUT; LOOP CAN BE OPENED TO INSERT DIGITAL FREQUENCY DIVIDER
- HIGHLY LINEAR TRIANGLE WAVE OUTPUT
- REFERENCE OUTPUT FOR CONNECTION OF COMPARATOR IN FREQUENCY DISCRIMINATOR
- BANDPASS, ADJUSTABLE FROM <±1% to >±60%
- FREQUENCY ADJUSTABLE OVER 10 TO 1 RANGE WITH SAME CAPACITOR

BLOCK DIAGRAM



PIN CONFIGURATIONS

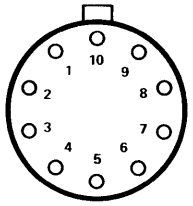
A PACKAGE
(Top View)



1. V⁻
2. Input
3. Input
4. VCO Output
5. Phase Comparator VCO Input
6. Reference Output
7. Demodulated Output
8. External R for VCO
9. External C for VCO
10. V⁺
11. NC
12. NC
13. NC
14. NC

ORDER PART NOS. SE565A/NE565A

K PACKAGE



1. V⁻
2. Input
3. Input
4. VCO Output
5. Phase Comparator VCO Input
6. Reference Output
7. Demodulated Output
8. External R for VCO
9. External C for VCO
10. V⁺

ORDER PART NOS. SE565K/NE565K

APPLICATIONS

FREQUENCY SHIFT KEYING
MODEMS
TELEMETRY RECEIVERS
TONE DECODERS
SCA RECEIVERS
WIDEBAND FM DISCRIMINATORS
DATA SYNCHRONIZERS
TRACKING FILTERS
SIGNAL RESTORATION
FREQUENCY MULTIPLICATION & DIVISION

ABSOLUTE MAXIMUM RATINGS (limiting values above which serviceability may be impaired)

Maximum Operating Voltage	26V
Storage Temperature	-65°C to 150°C
Power Dissipation	300mW

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = ±6 Volts unless otherwise noted)

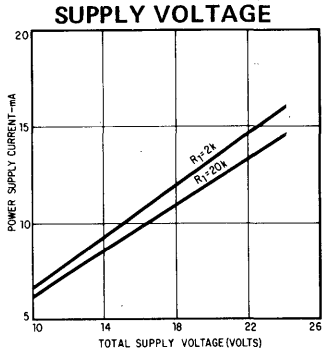
PARAMETER	TEST CONDITIONS	SE565			NE565			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
SUPPLY REQUIREMENTS								
Supply Voltage		±5		±12	±5		±12	V
Supply Current			8	12.5		8	12.5	mA
INPUT CHARACTERISTICS								
Input Impedance	$-4V \leqslant V_2, V_3 \leqslant +1V$	7	10		5	10		kΩ
Input Level Required for Tracking	f_0 = 50 kHz ±10% frequency deviation	10	1		10	1		mVrms
VCO CHARACTERISTICS								
Center Frequency								
Maximum Value	C_1 = 2.7 pF	300	500			500		kHz
Distribution	Distribution taken about $f_0 \simeq 50$ kHz R_1 = 5.0k, C_1 = 1200 pF	-10	0	+10	-30	0	+30	%
Drift with Temperature	f_0 = 50 kHz	+75	+100	+525		+200		ppm/°C
Drift with Supply Voltage	f_0 = 50 kHz V_{CC} = ±6 to ±7 Volts		0.1	1.0		0.2	1.5	%/V
Triangle Wave								
Output Voltage Level			0			0		V
Amplitude		2	2.4	3	2	2.4	3	Vp-p
Linearity			0.2			0.5		%
Square Wave								
Logical "1" Output Voltage	f_0 = 50 kHz V_{CC} = ±6 Volts	+4.9	+5.2		+4.9	+5.2		V
Logical "0" Output Voltage	f_0 = 50 kHz V_{CC} = ±6 Volts		-0.2	+0.2		-0.2	+0.2	V
Duty Cycle	f_0 = 50 kHz	45	50	55	40	50	60	%
Rise Time			20	100		20		nsec
Fall Time			50	200		50		nsec
Output Current (sink)		0.6	1		0.6	1		mA
Output Current (source)		5	10		5	10		mA
DEMODULATED OUTPUT CHARACTERISTICS								
Output Voltage Level	(pin 7) V_{CC} = ±6 Volts	4.25	4.5	4.75	4.0	4.5	5.0	V
Maximum Voltage Swing	(pin 7)		2			2		Vp-p
Output Voltage Swing	±10% frequency deviation	250	300		200	300		mVp-p
Total Harmonic Distortion			0.2	0.75		0.2	1.5	%
Output Impedance			3.6			3.6		kΩ
Offset Voltage $\lvert V_6-V_7 \rvert$	T_A = 25°C		30	100		50	200	mV
vs Temperature (drift)			50			100		μV/°C
AM Rejection		30	40			40		dB

NOTES:

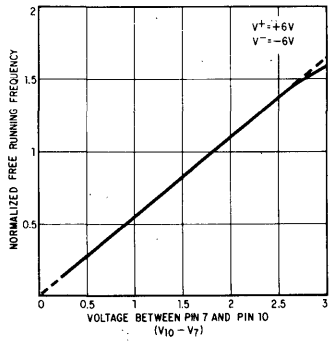
1. Both input terminals (pins 2 and 3) must receive identical dc bias. This bias may range from 0 volts to -4 volts.
2. The external resistance for frequency adjustment (R_1) must have a value between 2kΩ and 20kΩ.
3. Output voltage swings negative as input frequency increases.
4. Output not buffered.

TYPICAL PERFORMANCE CHARACTERISTICS

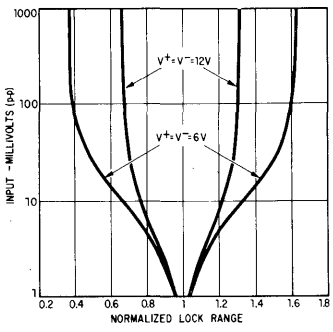
POWER SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



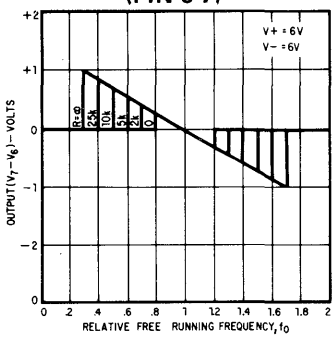
FREE-RUNNING VCO FREQ. AS A FUNCTION OF VOLTAGE BETWEEN PIN 7 & 10 (VCO CONVERSION GAIN)



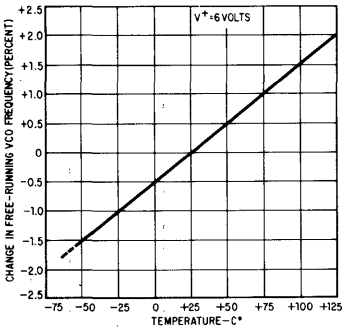
LOCK RANGE AS A FUNCTION OF INPUT VOLTAGE



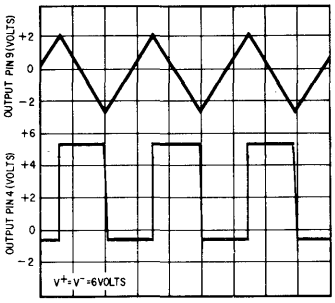
LOCK RANGE AS A FUNCTION OF GAIN SETTING RESISTANCE (PIN 6-7)



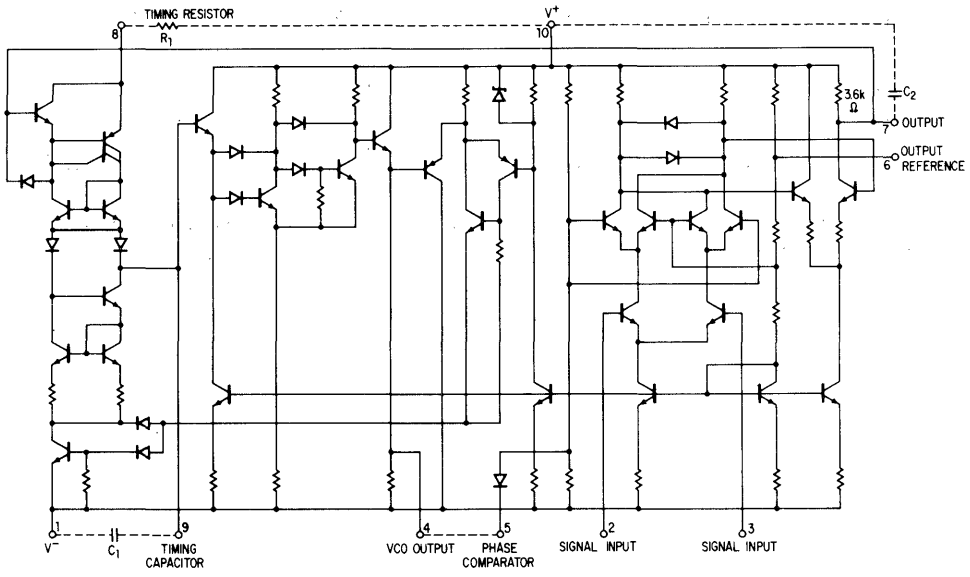
CHANGE IN FREE-RUNNING VCO FREQUENCY AS A FUNCTION OF TEMPERATURE



VCO OUTPUT WAVEFORM



SCHEMATIC DIAGRAM



DESIGN FORMULAS

Free-running frequency of VCO $f_o = \frac{1}{4R_1C_1}$ in Hz

Lock-range $f_L = \pm \frac{8f_o}{V_{cc}}$ in Hz

Capture-range $f_C \simeq \pm \frac{1}{2\pi} \sqrt{\frac{2\pi f_L}{\tau}}$

where $\tau = (3.6 \times 10^3) \times C_2$

DEFINITION OF TERMS

FREE-RUNNING FREQUENCY (f_o)

Frequency of VCO without input signal, both inputs grounded.

CAPTURE-RANGE

That range of frequencies about f_o over which the loop will acquire lock with an input signal initially starting out of lock.

LOCK-RANGE OR TRACKING-RANGE

That range of frequencies in the vicinity of f_o over which the VCO, once locked to the input signal, will remain locked.

TYPICAL APPLICATIONS

FM DEMODULATION

The 565 Phase Locked Loop is a general purpose circuit designed for highly-linear FM demodulation. During lock, the average dc level of the phase comparator output signal is directly proportional to the frequency of the input signal. As the input frequency shifts, it is this output signal which causes the VCO to shift its frequency to match that of the input. Consequently, the linearity of the phase comparator output with frequency is determined by the voltage-to-frequency transfer function of the VCO.

Because of its unique and highly linear VCO, the 565 PLL can lock to and track an input signal over a very wide range (typically ±60%) with very high linearity (typically, within 0.5%).

A typical connection diagram is shown in Figure 1. The VCO free-running frequency is given approximately by $f_o = 1/4R_1C_1$, and should be adjusted to be at the center of the input signal frequency range. C_1 can be any value, but R_1 should be within the range of 2000 to 20,000 ohms with an optimum value on the order of 4000 ohms. The source can be direct coupled if the dc resistances seen from pins 2 and 3 are equal and there is no dc voltage difference between the pins. A short between pins 4 and 5 connects the VCO to the phase comparator. Pin 6 provides a dc reference voltage that is close to the dc potential of the demodulated output (pin 7). Thus, if a resistance (R_2 in Figure 1) is connected between pins 6 and 7, the gain of the output stage can be reduced with little change in the dc voltage level at the output. This allows the lock range to be decreased with little change in the free-running frequency. In this manner the lock range can be decreased from ±60% of f_o to approximately ±20% of f_o (at ±6V).

A small capacitor (typically 0.001μF) should be connected between pins 7 and 8 to eliminate possible oscillation in the control current source.

A single-pole loop filter is formed by the capacitor C_2, connected between pin 7 and positive supply, and an internal resistance of approximately 3600 ohms.

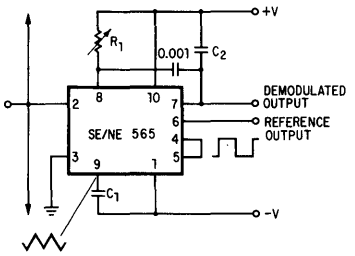


FIGURE 1

FREQUENCY SHIFT KEYING (FSK)

FSK refers to data transmission by means of carrier which is shifted between two preset frequencies. This frequency shift is usually accomplished by driving a VCO with the binary data signal so that the two resulting frequencies correspond to the "0" and "1" states (commonly called space and mark) of the binary data signal.

A simple scheme using the 565 to receive FSK signals of 1070 Hz and 1270 Hz is shown in Figure 2. As the signal appears at the input, the loop locks to the input frequency and tracks it between the two frequencies with a corresponding dc shift at the output.

The loop filter capacitor C_2 is chosen smaller than usual to eliminate overshoot on the output pulse, and a three-stage RC ladder filter is used to remove the carrier component from the output. The band edge of the ladder filter is chosen to be approximately half way between the maximum keying rate (in this case 300 baud or 150 Hz) and twice the input frequency (approximately 2200 Hz). The output signal can now be made logic compatible by connecting a voltage comparator between the output and pin 6 of the loop. The free-running frequency is adjusted with R_1 so as to result in a slightly-positive voltage at the output at f_{in} = 1070 Hz.

The input connection is typical for cases where a dc voltage is present at the source and therefore a direct connection is not desirable. Both input terminals are returned to ground with identical resistors (in this case, the values are chosen to effect a 600-ohm input impedance).

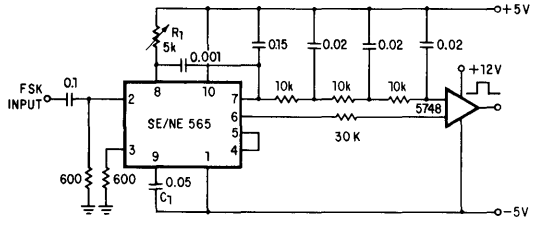


FIGURE 2

FREQUENCY MULTIPLICATION

There are two methods by which frequency multiplication can be achieved using the 565:

1. Locking to a harmonic of the input signal.
2. Inclusion of a digital frequency divider or counter in the loop between the VCO and phase comparator.

The first method is the simplest, and can be achieved by setting the free-running frequency of the VCO to a multiple of the input frequency. A limitation of this scheme is that the lock range decreases as successively higher and weaker harmonics are used for locking. If the input frequency is to be constant with little tracking required, the loop can generally be locked to any one of the first 5 harmonics. For higher orders of multiplication, or for cases where a large lock range is desired, the second scheme is more desirable. An example of this might be a case where the input signal varies over a wide frequency range and a large multiple of the input frequency is required.

A block diagram of the second scheme is shown in Figure 3. Here the loop is broken between the VCO and the phase comparator, and a frequency divider is inserted. The fundamental of the divided VCO frequency is locked to the input frequency in this case, so that the VCO is actually running at a multiple of the input frequency. The amount of multiplication is determined by the frequency divider. A typical connection scheme is shown in Figure 4. To set up the circuit, the frequency limits of the input signal must be determined. The free-running frequency of the VCO is then adjusted by means of R_1 and C_1 (as discussed under FM demodulation) so that the output frequency of the divider is midway between the input frequency limits. The filter capacitor, C_2, should be large enough to eliminate variations in the demodulated output voltage (at pin 7), in order to stabilize the VCO frequency. The output can now be taken as the VCO squarewave output, and its fundamental will be the desired multiple of the input frequency (f_1) as long as the loop is in lock.

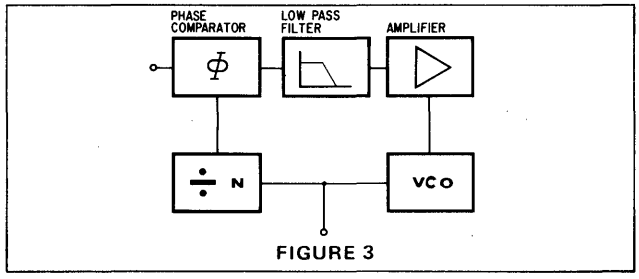


FIGURE 3

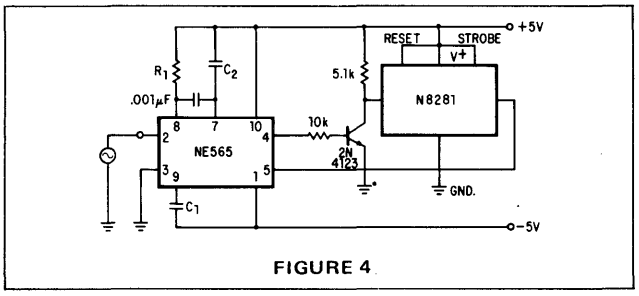


FIGURE 4

SCA (BACKGROUND MUSIC) DECODER

Some FM stations are authorized by the FCC to broadcast uninterrupted background music for commercial use. To do this a frequency modulated subcarrier of 67 kHz is used. The frequency is chosen so as not to interfere with the normal stereo or monaural program; in addition, the level of the subcarrier is only 10% of the amplitude of the combined signal.

The SCA signal can be filtered out and demodulated with the NE565 Phase Locked Loop without the use of any resonant circuits. A connection diagram is shown in Figure 5. This circuit also serves as an example of operation from a single power supply.

A resistive voltage divider is used to establish a bias voltage for the input (pins 2 and 3). The demodulated (multiplex) FM signal is fed to the input through a two-stage high-pass filter, both to effect capacitive coupling and to attenuate the strong signal of the regular channel. A total signal amplitude, between 80 mV and 300 mV, is required at the input. Its source should have an impedance of less than 10,000 ohms.

The Phase Locked Loop is tuned to 67 kHz with a 5000 ohm potentiometer; only approximate tuning is required, since the loop will seek the signal.

The demodulated output (pin 7) passes through a three-stage low-pass filter to provide de-emphasis and attenuate the high-frequency noise which often accompanies SCA transmission. Note that no capacitor is provided directly at pin 7; thus, the circuit is operating as a first-order loop. The demodulated output signal is in the order of 50 mV and the frequency response extends to 7 kHz.

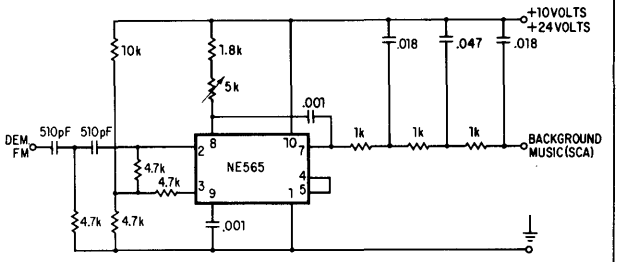


FIGURE 5

DESCRIPTION

The SE/NE 566 Function Generator is a voltage controlled oscillator of exceptional stability and linearity with buffered square wave and triangle wave outputs. The frequency of oscillation is determined by an external resistor and capacitor and the voltage applied to the control terminal. The oscillator can be programmed over a ten to one frequency range by proper selection of an external resistance and modulated over a ten to one range by the control voltage, with exceptional linearity.

FEATURES

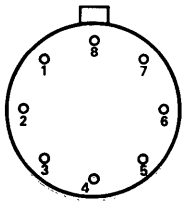
- WIDE RANGE OF OPERATING VOLTAGE (10 to 24 volts)
- VERY HIGH LINEARITY OF MODULATION
- EXTREME STABILITY OF FREQUENCY (100 ppm/°C typical)
- HIGHLY LINEAR TRIANGLE WAVE OUTPUT
- HIGH ACCURACY SQUARE WAVE OUTPUT
- FREQUENCY PROGRAMMING BY MEANS OF A RESISTOR, CAPACITOR, VOLTAGE OR CURRENT
- FREQUENCY ADJUSTABLE OVER 10 TO 1 RANGE WITH SAME CAPACITOR

APPLICATIONS

TONE GENERATORS
FREQUENCY SHIFT KEYING
FM MODULATORS
CLOCK GENERATORS
SIGNAL GENERATORS
FUNCTION GENERATORS

PIN CONFIGURATION (Top View)

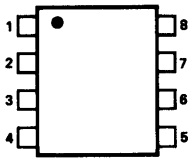
T PACKAGE



1 Ground
2 NC
3 Square Wave Output
4 Triangle Wave Output
5 Modulation Input
6 R_1
7 C_1
8 V+

ORDER PART NOS. SE566T/NE566T

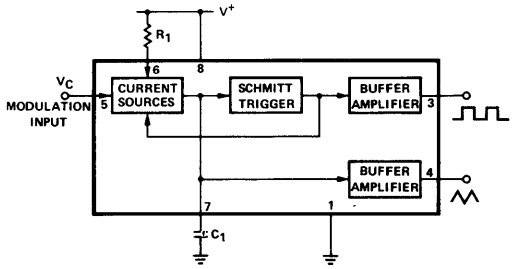
V PACKAGE



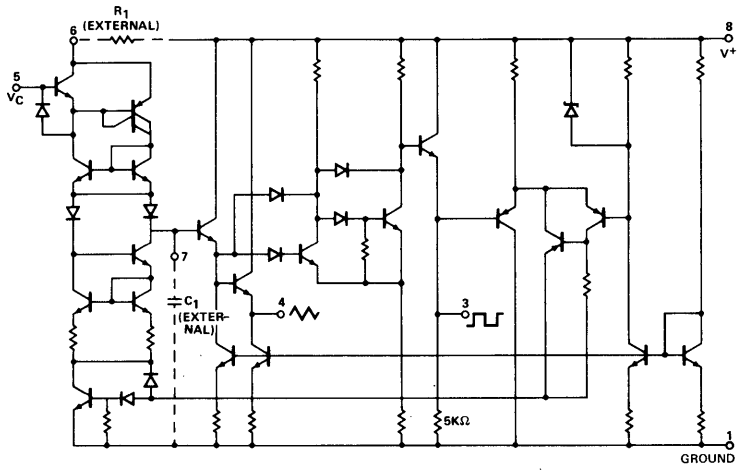
1 Ground
2 NC
3 Square Wave Output
4 Triangle Wave Output
5 Modulation Input
6 R_1
7 C_1
8 V+

ORDER PART NO. NE566V

BLOCK DIAGRAM



EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS (Limiting values above which serviceability may be impaired)

Maximum Operating Voltage	26V
Storage Temperature	−65°C to 150° C
Power Dissipation	300mW

ELECTRICAL CHARACTERISTICS (25°C, 12 Volts, unless otherwise stated)

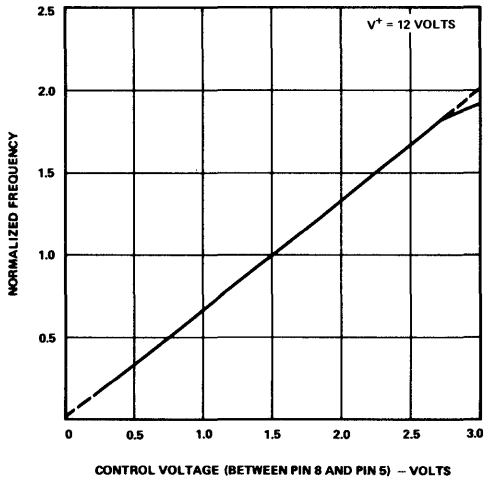
CHARACTERISTICS	SE566			NE566			UNITS
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
GENERAL							
Operating Temperature Range	-55		125	0		70	°C
Operating Supply Voltage			24			24	Volts
Operating Supply Current		7	12.5		7	12.5	mA
VCO (Note 1)							
Maximum Operating Frequency		1			1		MHz
Frequency Drift with Temperature		100			200		ppm/°C
Frequency Drift with Supply Voltage		1			2		%/volt
Control Terminal Input Impedance (Note 2)		1			1		MΩ
FM Distortion (±10% Deviation)		0.2	0.75		0.2	1.5	%
Maximum Sweep Rate		1			1		MHz
Sweep Range		10:1			10:1		
OUTPUT							
Triangle Wave Output -							
Impedance		50			50		Ω
Voltage	2	2.4		2	2.4		Volts pp
Linearity		0.2			0.5		%
Square Wave Output -							
Impedance		50			50		Ω
Voltage	5	5.4		5	5.4		Volts pp
Duty Cycle	45	50	55	40	50	60	%
Rise Time		20			20		nsec
Fall Time		50			50		nsec

NOTES:

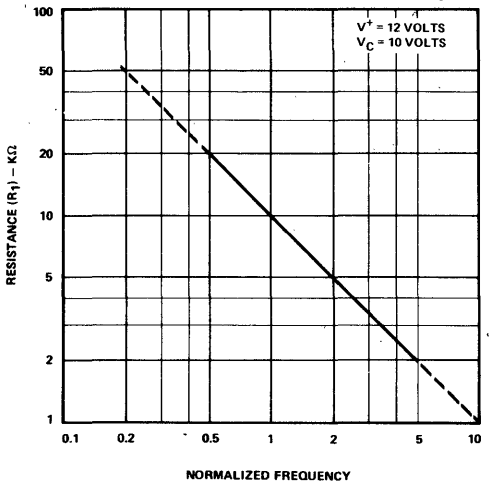
1. The external resistance for frequency adjustment (R_1) must have a value between 2KΩ and 20KΩ.
2. The bias voltage (Vc) applied to the control terminal (pin 5) should be in the range $3/4\ V^+ \leq V_C \leq V^+$.

TYPICAL PERFORMANCE CHARACTERISTICS

NORMALIZED FREQUENCY AS A FUNCTION OF CONTROL VOLTAGE

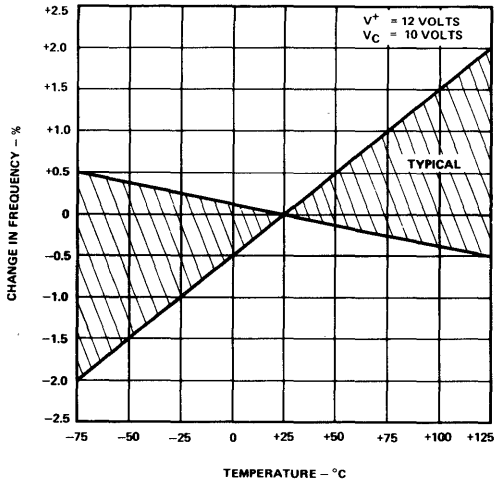


NORMALIZED FREQUENCY AS A FUNCTION OF RESISTANCE (R_1)

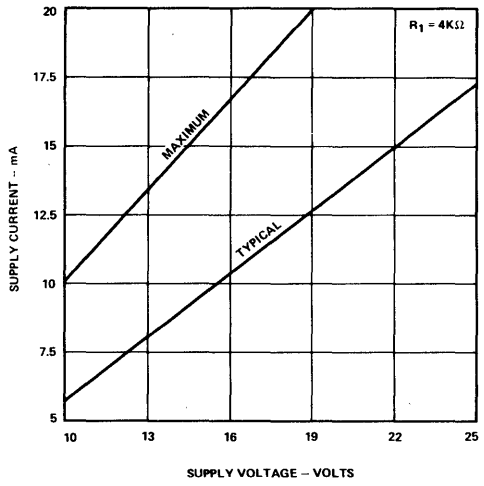


TYPICAL PERFORMANCE CHARACTERISTICS (Cont'd)

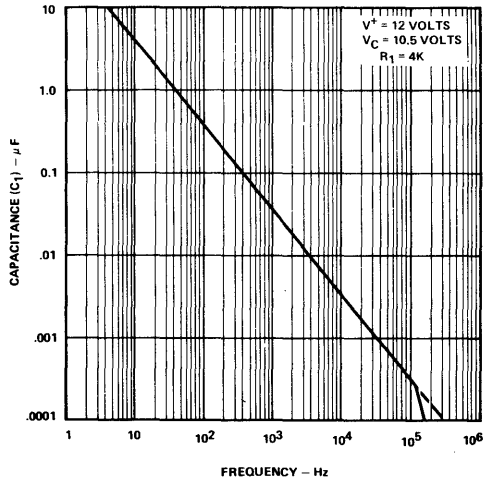
CHANGE IN FREQUENCY AS A FUNCTION OF TEMPERATURE



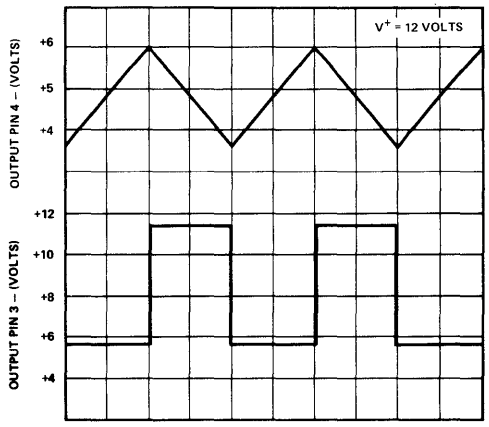
POWER SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE



FREQUENCY AS A FUNCTION OF CAPACITANCE (C_1)



VCO OUTPUT WAVEFORMS



OPERATING INSTRUCTIONS

The SE/NE 566 Function Generator is a general purpose voltage controlled oscillator designed for highly linear frequency modulation. The circuit provides simultaneous square wave and triangle wave outputs at frequencies up to 1 MHz. A typical connection diagram is shown in Figure 1. The control terminal (pin 5) must be biased externally with a voltage (V_C) in the range

$$3/4\ V^+ \leqslant V_C \leqslant V^+$$

where V_{CC} is the total supply voltage. In Figure 1, the control voltage is set by the voltage divider formed with R_2 and R_3. The modulating signal is then ac coupled with the capacitor C_2. The modulating signal can be direct coupled as well, if the appropriate dc bias voltage is applied to the control terminal. The frequency is given approximately by

$$f_o \simeq \frac{2(V^+ - V_C)}{R_1 C_1 V^+}$$

and R_1 should be in the range $2K < R_1 < 20K\Omega$.
A small capacitor (typically $0.001\mu f$) should be connected between pins 5 and 6 to eliminate possible oscillation in the control current source.

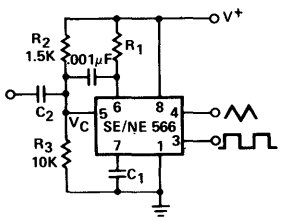


FIGURE 1

OPERATING INSTRUCTIONS (Cont'd)

If the VCO is to be used to drive standard logic circuitry, it may be desirable to use a dual supply of ±5 volts as shown in Figure 2. In this case the square wave output has the proper dc levels for logic circuitry. RTL can be driven directly from pin 3. For DTL or T^2L gates, which require a current sink of more than 1 mA, it is usually necessary to connect a 5KΩ resistor between pin 3 and negative supply. This increases the current sinking capability to 2 mA. The third type of interface shown uses a saturated transistor. between the 566 and the logic circuitry. This scheme is used primarily for T^2L circuitry which requires a fast fall time (< 50 nsec) and a large current sinking capability.

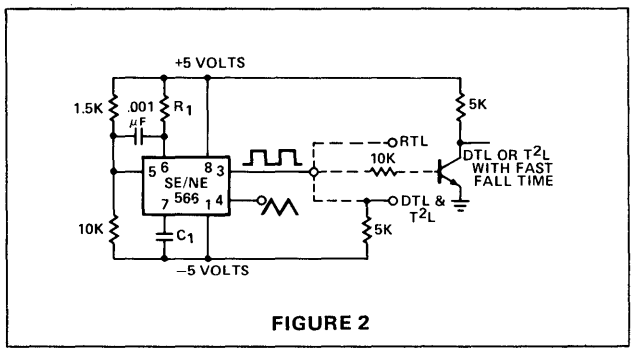


FIGURE 2

DESCRIPTION

The SE/NE 567 tone and frequency decoder is a highly stable phase-locked loop with synchronous AM lock detection and power output circuitry. Its primary function is to drive a load whenever a sustained frequency within its detection band is present at the self-biased input. The bandwidth center frequency, and output delay are independently determined by means of four external components.

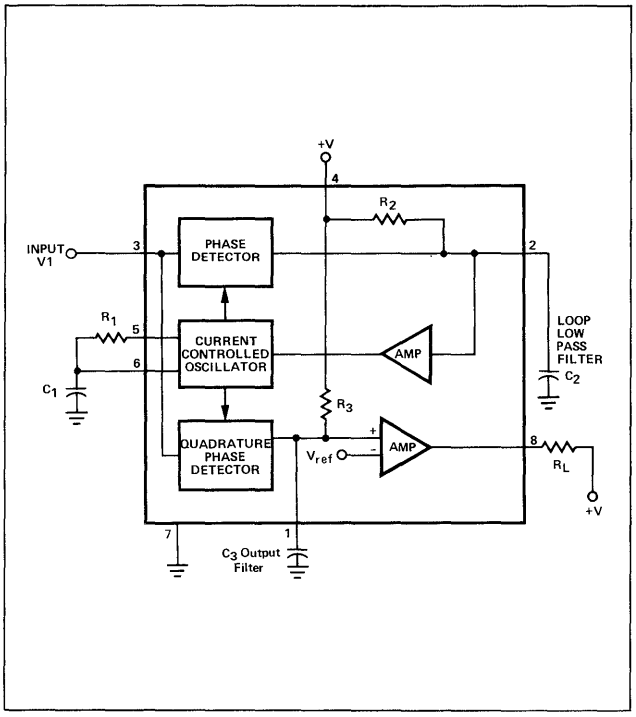
FEATURES

- WIDE FREQUENCY RANGE (.01Hz TO 500kHz)
- HIGH STABILITY OF CENTER FREQUENCY
- INDEPENDENTLY CONTROLLABLE BANDWIDTH (0 TO 14 PERCENT)
- HIGH OUT-BAND SIGNAL AND NOISE REJECTION
- LOGIC-COMPATIBLE OUTPUT WITH 100mA CURRENT SINKING CAPABILITY
- INHERENT IMMUNITY TO FALSE SIGNALS
- FREQUENCY ADJUSTMENT OVER A 20 TO 1 RANGE WITH AN EXTERNAL RESISTOR

APPLICATIONS

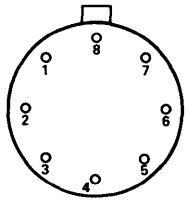
TOUCH TONE® DECODING
CARRIER CURRENT REMOTE CONTROLS
ULTRASONIC CONTROLS (REMOTE TV, ETC.)
COMMUNICATIONS PAGING
FREQUENCY MONITORING AND CONTROL
WIRELESS INTERCOM
PRECISION OSCILLATOR

BLOCK DIAGRAM



PIN CONFIGURATION

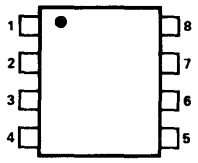
T PACKAGE
(Top View)



1. Output Filter Capacitor C_3
2. Low Pass Filter Capacitor C_2
3. Input
4. Supply Voltage +V
5. Timing Element R_1
6. Timing Elements R_1 and C_1
7. Ground
8. Output

ORDER PART NOS. SE567T/NE567T

V PACKAGE



1. Output Filter Capacitor C_3
2. Low Pass Filter Capacitor C_2
3. Input
4. Supply Voltage +V
5. Timing Element R_1
6. Timing Elements R_1 and C_1
7. Ground
8. Output

ORDER PART NO. NE567V

ABSOLUTE MAXIMUM RATINGS:

Operating Temperature	0°C to 70°C NE567 -55°C to 125°C SE567
Operating Voltage	10V
Positive Voltage at Input	0.5V above Supply Voltage (Pin 4)
Negative Voltage at Input	-10 VDC
Output Voltage (collector of output transistor)	15 VDC
Storage Temperature	-65°C to 150°C
Power Dissipation	300mW

ELECTRICAL CHARACTERISTICS (V+ = 5.0 Volts, T_A = 25°C unless noted)

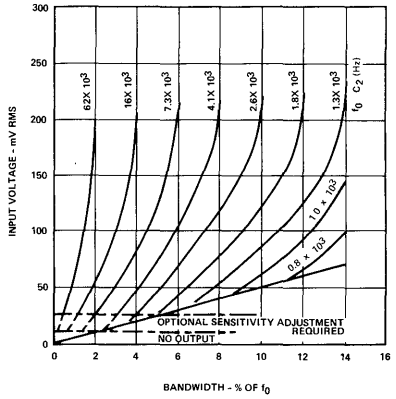
CHARACTERISTICS	SE567 MIN	SE567 TYP	SE567 MAX	NE567 MIN	NE567 TYP	NE567 MAX	UNITS	TEST CONDITIONS
CENTER FREQUENCY(NOTE 1)								
Highest Center Frequency (f_o)	100	500		100	500		kHz	
Center Frequency Stability (Note 2)		35±140 35±60			35±140 35±60		ppm/°C ppm/°C	-55 to 125°C 0 to 70°C
Center Frequency Shift with Supply Voltage		0.5	1		0.7	2	%/Volt	f_o = 100KHz
DETECTION BANDWIDTH								
Largest Detection Bandwidth	12	14	16	10	14	18	% of f_o	f_o = 100KHz
Largest Detection Bandwidth Skew		1	2		2	3	% of f_o	
Largest Detection Bandwidth - Variation with Temperature		±0.1			±0.1		%/°C	V_i = 300mVrms
Largest Detection Bandwidth - Variation with Supply Voltage		±2			±2		%/Volt	V_i = 300mVrms
INPUT								
Input Resistance		20			20		KΩ	
Smallest Detectable Input Voltage(V_i)		20	25		20	25	mV rms	I_L = 100mA, $f_i = f_o$
Largest No-Output Input Voltage	10	15		10	15		mV rms	I_L = 100mA, $f_i = f_o$
Greatest Simultaneous Outband Signal to Inband Signal Ratio		+6			+6		dB	
Minimum Input Signal to Wideband Noise Ratio		-6			-6		dB	Bn = 140KHz
OUTPUT								
Fastest On-Off Cycling Rate		f_o/20			f_o/20			
"1" Output Leakage Current		0.01	25		0.01	25	μA	
"0" Output Voltage		0.2 0.6	0.4 1.0		0.2 0.6	0.4 1.0	Volt Volt	I_L = 30mA I_L = 100mA
Output Fall Time (Note 3)		30			30		n sec	R_L = 50Ω
Output Rise Time (Note 3)		150			150		n sec	R_L = 50Ω
GENERAL								
Operating Voltage Range	4.75		9.0	4.75		9.0	Volts	
Supply Current - Quiescent		6	8		7	10	mA	
Supply Current - Activated		11	13		12	15	mA	R_L = 20KΩ
Quiescent Power Dissipation		30			35		mW	

NOTES:

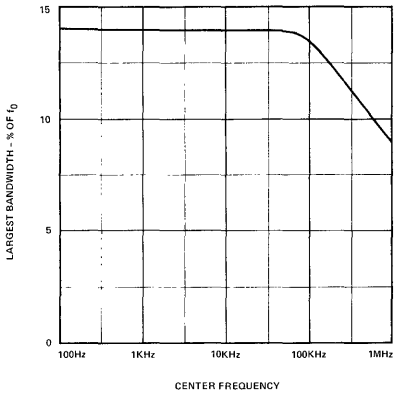
1. Frequency determining resistor R_1 should be between 1 and 20KΩ.
2. Applicable over 4.75 to 5.75 volts. See graphs for more detailed information.
3. Pin 8 to Pin 1 feedback R_L network selected to eliminate pulsing during turn-on and turn-off.

TYPICAL CHARACTERISTIC CURVES

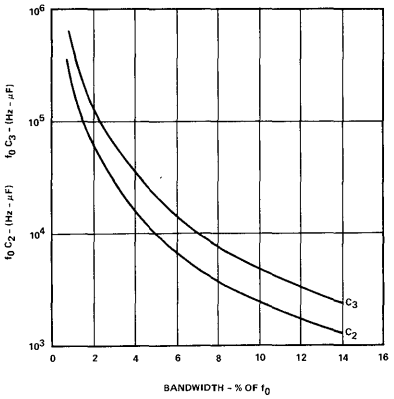
BANDWIDTH VERSUS INPUT SIGNAL AMPLITUDE



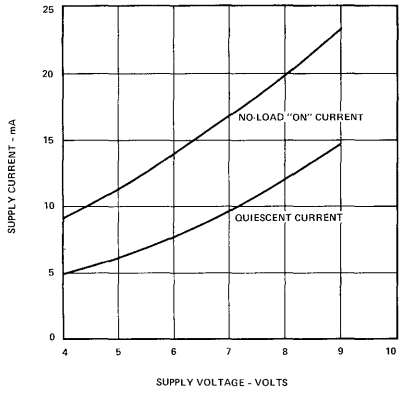
LARGEST DETECTION BANDWIDTH VERSUS OPERATING FREQUENCY



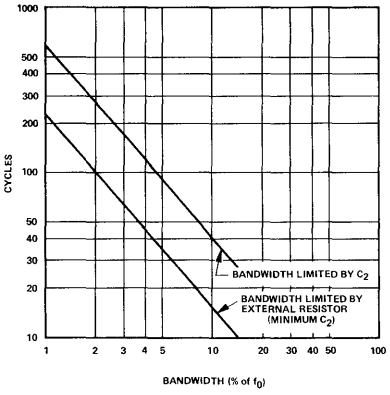
DETECTION BANDWIDTH AS A FUNCTION OF C_2 AND C_3



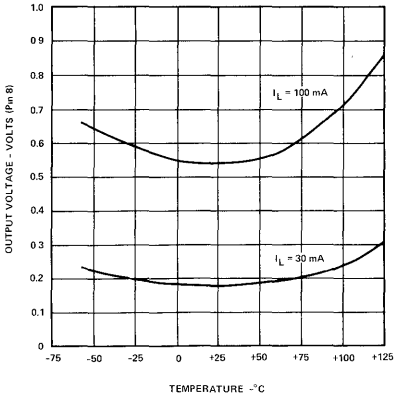
TYPICAL SUPPLY CURRENT VERSUS SUPPLY VOLTAGE



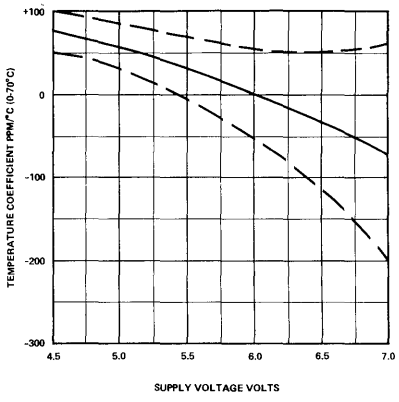
GREATEST NUMBER OF CYCLES BEFORE OUTPUT



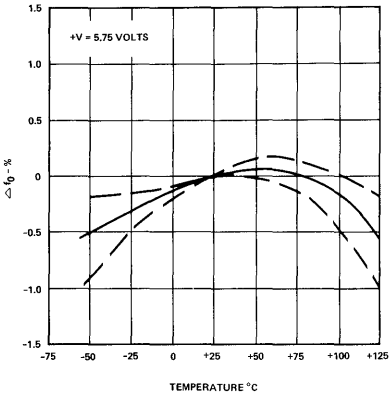
TYPICAL OUTPUT VOLTAGE VERSUS TEMPERATURE



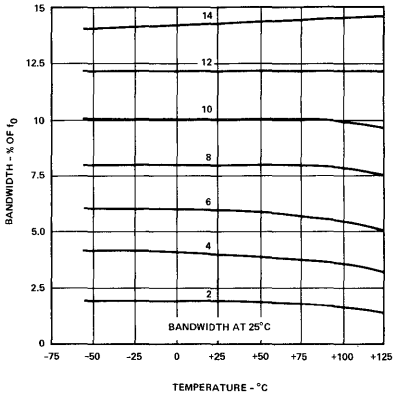
CENTER FREQUENCY COEFFICIENT TEMPERATURE (MEAN AND S.D.)



TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)

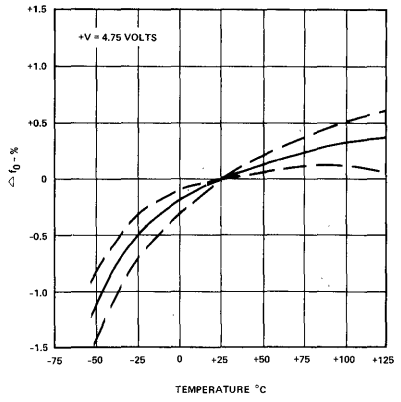


TYPICAL BANDWIDTH VARIATION WITH TEMPERATURE

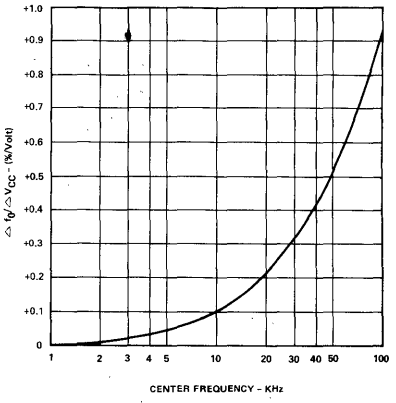


TYPICAL CHARACTERISTIC CURVES (Cont'd.)

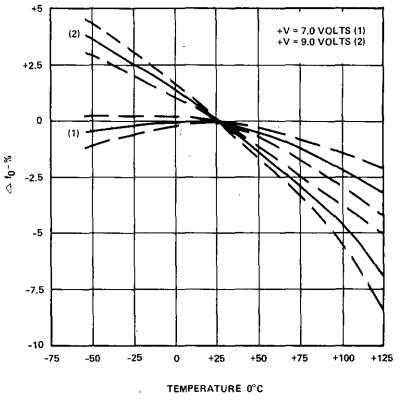
TYPICAL FREQUENCY DRIFT WITH (MEAN AND S.D.) TEMPERATURE



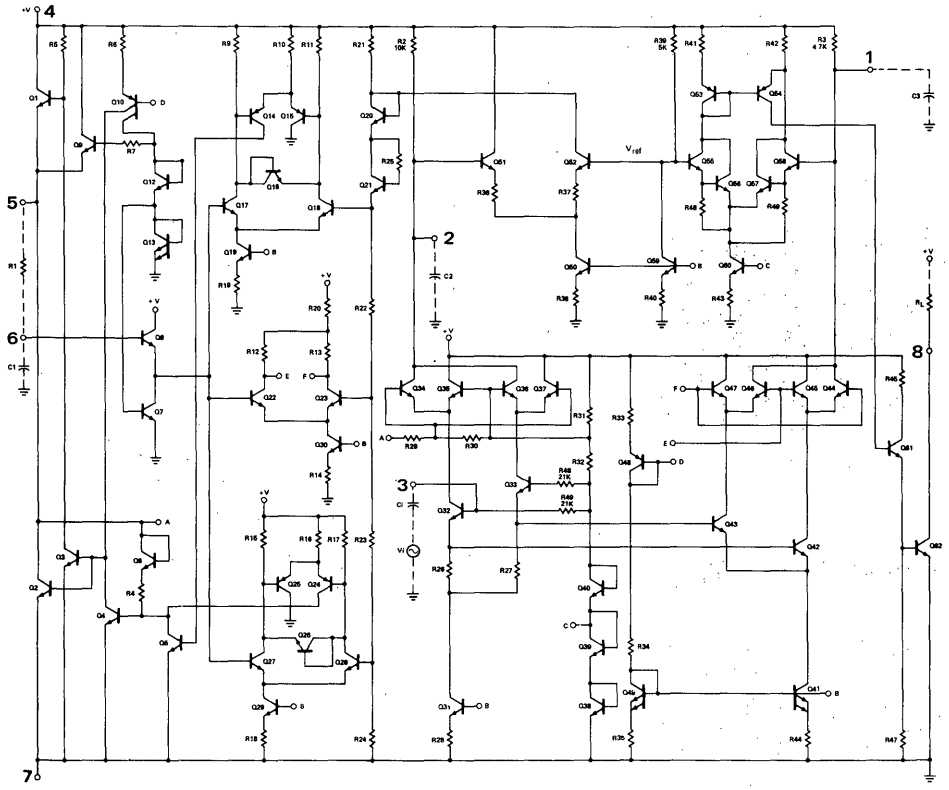
CENTER FREQUENCY SHIFT WITH SUPPLY VOLTAGE CHANGE VERSUS OPERATING FREQUENCY



TYPICAL FREQUENCY DRIFT WITH TEMPERATURE (MEAN AND S.D.)



SCHEMATIC DIAGRAM



DESIGN FORMULAS

$$f_0 \simeq \frac{1}{R_1 C_1}$$

$$BW \simeq 1070\sqrt{\frac{V_i}{f_0 C_2}} \quad \text{in \% of } f_0$$

Where

V_i = Input Voltage (Volts)
C_2 = Low-Pass Filter Capacitor (μF)

PHASE LOCKED LOOP TERMINOLOGY

CENTER FREQUENCY (f_0)

The free-running frequency of the current controlled oscillator (CCO) in the absence of an input signal.

DETECTION BANDWIDTH (BW)

The frequency range, centered about f_0, within which an input signal above the threshold voltage (typically 20mV rms) will cause a logical zero state on the output. The detection bandwidth corresponds to the loop capture range.

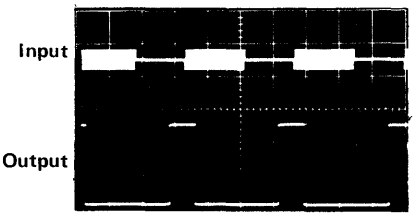
LARGEST DETECTION BANDWIDTH

The largest frequency range within which an input signal above the threshold voltage will cause a logical zero state on the output. The maximum detection bandwidth corresponds to the loop lock range.

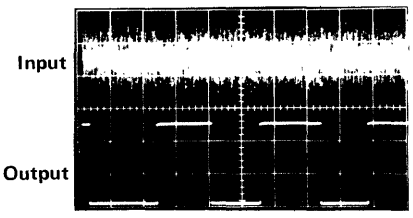
DETECTION BAND SKEW

A measure of how well the largest detection band is centered about the center frequency, f_0. The skew is defined as $(f_{max} + f_{min} - 2f_0)/f_0$ where f_{max} and f_{min} are the frequencies corresponding to the edges of the detection band. The skew can be reduced to zero if necessary by means of an optional centering adjustment.

TYPICAL RESPONSE



Response to 100mV RMS tone burst.
R_L = 100 ohms.



Response to same input tone burst with wideband noise.
$\frac{S}{N}$ = -6db R_L = 100 ohms
Noise Bandwidth = 140 Hz

OPERATING INSTRUCTIONS

Figure 1 shows a typical connection diagram for the 567. For most applications, the following three-step procedure will be sufficient for choosing the external components R_1, C_1, C_2 and C_3.

1. Select R_1 and C_1 for the desired center frequency ($f_0 \simeq 1/R_1 C_1$). For best temperature stability, R_1 should be between 2 and 20 ohm, and the R_1C_1 product should have sufficient stability, over the projected temperature range to meet the necessary requirements.
2. Select the low-pass capacitor, C_2, by referring to the Bandwidth versus Input Signal Amplitude graph. If the input amplitude variation is known, the appropriate value of f_0C_2 necessary to give the desired bandwidth may be found. Conversely, an area of operation may be selected on this graph and the input level and C_2 may be adjusted accordingly. For example, constant bandwidth operation requires that input amplitude be above 200mVrms. The bandwidth, as noted on the graph, is then controlled solely by the f_0C_2 product.
3. The value of C_3 is generally non-critical. C_3 sets the band edge of a low pass filter which attenuates frequencies outside the detection band to eliminate spurious outputs. If C_3 is too small, frequencies just outside the detection band will switch the output stage on and off at the beat frequency, or the output may pulse on and off during the turn-on transient. If C_3 is too large, turn-on and turn-off of the output stage will be delayed until the voltage on C_3 passes the threshold voltage. (Such a delay may be desirable to avoid spurious outputs due to transient frequencies.) A typical minimum value for C_3 is $2C_2$.

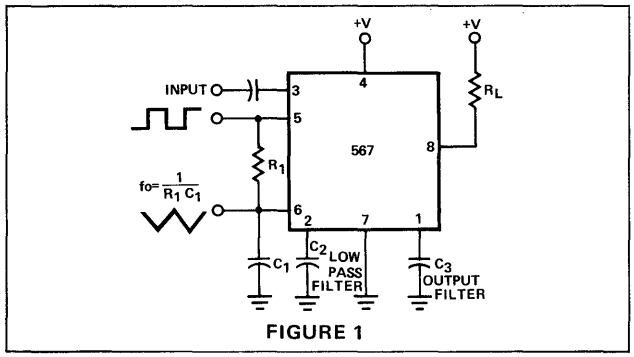


FIGURE 1

AVAILABLE OUTPUTS (Figure 2)

The primary output is the uncommitted output transistor collector, pin 8. When an in-band input signal is present, this transistor saturates; its collector voltage being less than 1.0 volt (typically 0.6V) at full output current (100mA). The voltage at pin 2 is the phase detector output, a linear function of frequency, over the range of 0.95 to 1.05 f_0, with a slope of about 20mV/% frequency deviation. The average voltage at pin 1 is, during lock, a function of the in-band input amplitude in accordance with the transfer characteristic given. Pin 5 is the controlled oscillator square wave output of magnitude $(V^+-2Vbe) \approx (V^+-1.4V)$ having a dc average of $V^+/2$. A 1KΩ load may be driven from pin 5. Pin 6 is an exponential triangle of 1 volt peak-to-peak

AVAILABLE OUTPUTS (Cont'd.)

with an average dc level of V^+ /2. Only high impedance loads may be connected to pin 6 without affecting the CCO duty cycle or temperature stability.

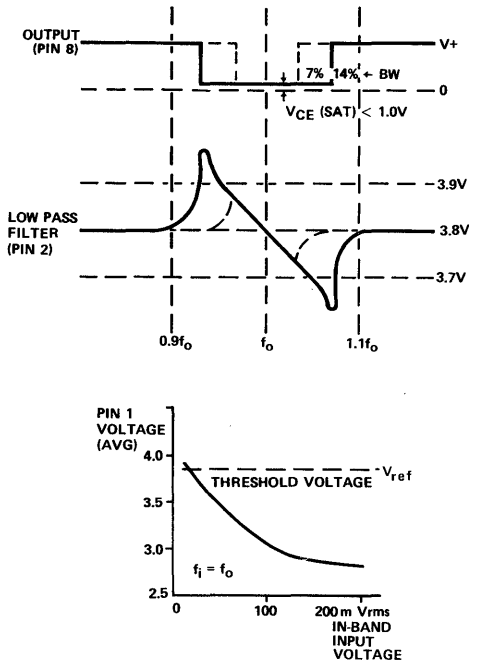


FIGURE 2

OPERATING PRECAUTIONS

A brief review of the following precautions will help the user attain the high level of performance of which the 567 is capable.

1. Operation in the high input level mode (above 200mV) will free the user from bandwidth variations due to changes in the in-band signal amplitude. The input stage is now limiting, however, so that out-band signals or high noise levels can cause an apparent bandwidth reduction as the in band signal is suppressed. Also, the limiting action will create in-band components from sub-harmonic signals, so the 567 becomes sensitive to signals at $f_o/3$, $f_o/5$, etc.

2. The 567 will lock onto signals near $(2n+1)\ f_o$, and will give an output for signals near $(4n+1)\ f_o$ where n = 0, 1, 2, etc. Thus, signals at 5 f_o and 9 f_o can cause an unwanted output. If such signals are anticipated, they should be attentuated before reaching the 567 input.

3. Maximum immunity from noise and out-band signals is afforded in the low input level (Below 200mVrms) and reduced bandwidth operating mode. However, decreased loop damping causes the worse-case lock-up time to increase, as shown by the Greatest Number of Cycles Before Output vs. Bandwidth graph.

4. Due to the high switching speeds (20ns) associated with 567 operation, care should be taken in lead routing. Lead lengths should be kept to a minimum. The power supply should be adequately bypassed close to the 567 with an 0.01μF or greater capacitor; grounding paths should be carefully chosen to avoid ground loops and unwanted voltage variations. Another factor which must be considered is the effect of load energization on the power supply. For example, an incandescent lamp typically draws 10 times rated current at turn-on. This can cause supply voltage fluctuations which could, for example, shift the detection band of narrow-band systems sufficiently to cause momentary loss of lock. The result is a low-frequency oscillation into and out of lock. Such effects can be prevented by supplying heavy load currents from a separate supply, or increasing the supply filter capacitor.

SPEED OF OPERATION

Minimum lock-up time is related to the natural frequency of the loop. The lower it is, the longer becomes the turn-on transient. Thus, maximum operating speed is obtained when C_2 is at a minimum. When the signal is first applied, the phase may be such as to initially drive the controlled oscillator away from the incoming frequency rather than toward it. Under this condition, which is of course unpredictable, the lock-up transient is at its worst and the theoretical minimum lock-up time is not achievable. We must simply wait for the transient to die out.

The following expressions give the values of C_2 and C_3 which allow highest operating speeds for various band center frequencies. The minimum rate at which digital information may be detected without information loss due to the turn-on transient or output chatter is about 10 cycles per bit, corresponding to an information transfer rate of $f_0/10$ baud.

$$C_2 = \frac{130}{f_o}\mu F$$

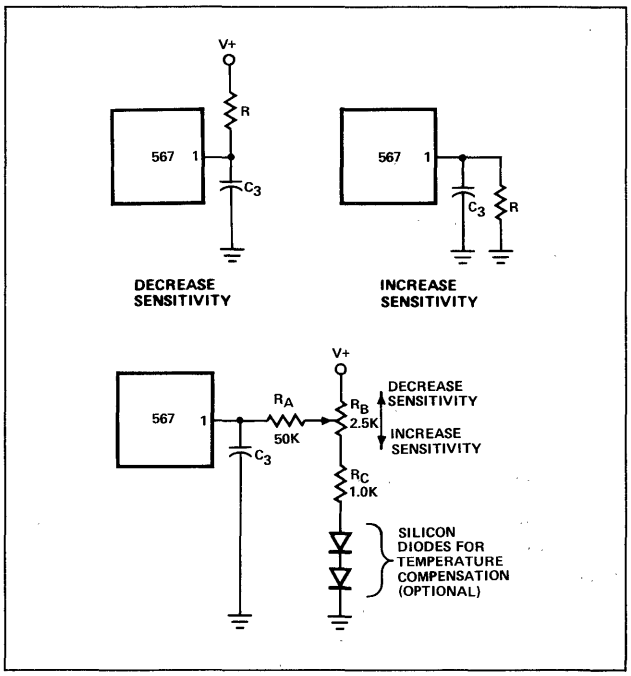
$$C_3 = \frac{260}{f_o}\mu F$$

in cases where turn-off time can be sacrificed to achieve fast turn-on, the optional sensitivity adjustment circuit can be used to move the quiescent C_3 voltage lower (closer to the threshold voltage). However, sensitivity to beat frequencies, noise and extraneous signals will be increased.

OPTIONAL CONTROLS

The 567 has been designed so that, for most applications, no external adjustments are required. Certain applications, however, will be greatly facilitated if full advantage is taken of the added control possibilities available through the use of additional external components. In the diagrams given, typical values are suggested where applicable. For best results resistors used, except where noted, should have the same temperature coefficient. Ideally, silicon diodes would be low-resistivity types, such as forward-biased low-voltage zeners or forward-biased transistor base-emitter junctions. However, ordinary low-voltage diodes should be adequate for most applications.

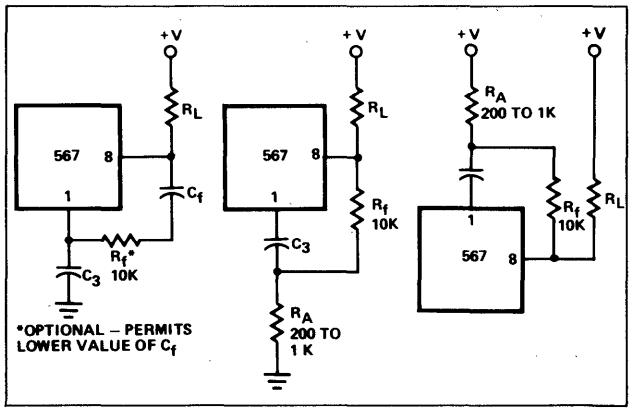
SENSITIVITY ADJUSTMENT



When operated as a very narrow band detector (less than 8 percent), both C_2 and C_3 are made quite large in order to improve noise and outband signal rejection. This will inevitably slow the response time. If, however, the output stage is biased closer to the threshold level, the turn-on time can be improved. This is accomplished by drawing additional current to terminal 1. Under this condition, the 567 will also give an output for lower-level signals (10m or lower).

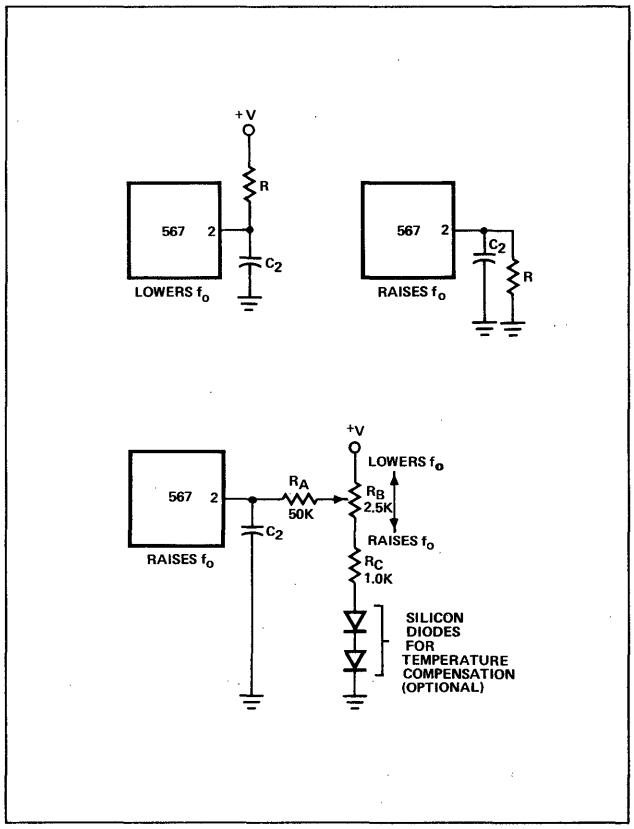
By adding current to terminal 1, the output stage is biased further away from the threshold voltage. This is most useful when, to obtain maximum operating speed, C_2 and C_3 are made very small. Normally, frequencies just outside the detection band could cause false outputs under this condition. By desensitizing the output stage, the outband beat notes do not feed through to the output stage. Since the input level must be somewhat greater when the output stage is made less sensitive, rejection of third harmonics or in-band harmonics (of lower frequency signals) is also improved.

CHATTER PREVENTION



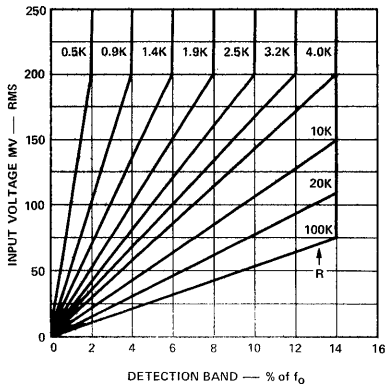
Chatter occurs in the output stage when C_3 is relatively small, so that the lock transient and the AC components at the quadrature phase detector (lock detector) output cause the output stage to move through its threshold more than once. Many loads, for example lamps and relays, will not respond to the chatter. However, logic may recognize the chatter as a series of outputs. By feeding the output stage output back to its input, (pin 1) the chatter can be eliminated. Three schemes for doing this are given above. All operate by feeding the first output step (either on or off) back to the input, pushing the input past the threshold until the transient conditions are over. It is only necessary to assure that the feedback time constant is not so large as to prevent operation at the highest anticipated speed. Although chatter can always be eliminated by making C_3 large, the feedback circuit will enable faster operation of the 567 by allowing C_3 to be kept small. Note that if the feedback time constant is made quite large, a short burst at the input frequency can be stretched into a long output pulse. This may be useful to drive, for example, stepping relays.

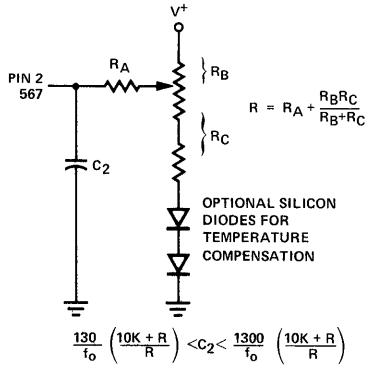
DETECTION BAND CENTERING (OR SKEW) ADJUSTMENT



When it is desired to alter the location of the detection band (corresponding to the loop capture range) within the largest detection band (lock range), the circuits shown above can be used. By moving the detection band to one edge of the range, for example, input signal variations will expand the detection band in only one direction. This may prove useful when a strong but undesirable signal is expected on one side or the other of the center frequency. Since R_B also alters the duty cycle slightly, this method may be used to obtain a precise duty cycle when the 567 is used as an oscillator.

ALTERNATE METHOD OF BANDWIDTH REDUCTION

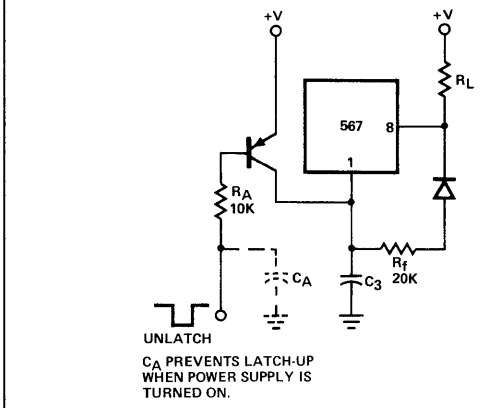


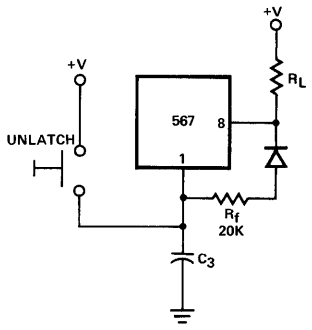


NOTE: Adjust control for symmetry of detection band edges about f_o.

Although a large value of C_2 will reduce the bandwidth, it also reduces the loop damping so as to slow the circuit response time. This may be undesirable. Bandwidth can be reduced by reducing the loop gain. This scheme will improve damping and permit faster operation under narrow-band operation. Note that the reduced impedance level at terminal 2 will require that a larger value of C_2 be used for a given filter cutoff frequency. If more than three 567s are to be used, the R_B, R_C network can be eliminated and the R_A resistors connected together. A capacitor between this junction and ground may be required to shunt high frequency components.

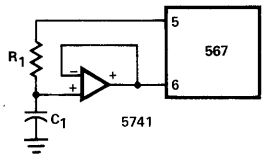
OUTPUT LATCHING





To latch the output on after a signal is received, it is necessary to provide a feedback resistor around the output stage (between pins 8 and 1). Pin 1 is pulled up to unlatch the output stage.

REDUCTION OF C_1 VALUE



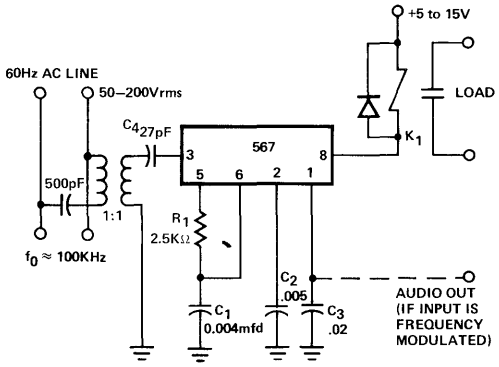
For precision, very low-frequency applications, where the value of C_1 becomes large, an overall cost savings may be achieved by inserting a voltage follower between the R_1 C_1 junction and pin 6, so as to allow a higher value of R_1 and a lower value of C_1 for a given frequency.

PROGRAMMING

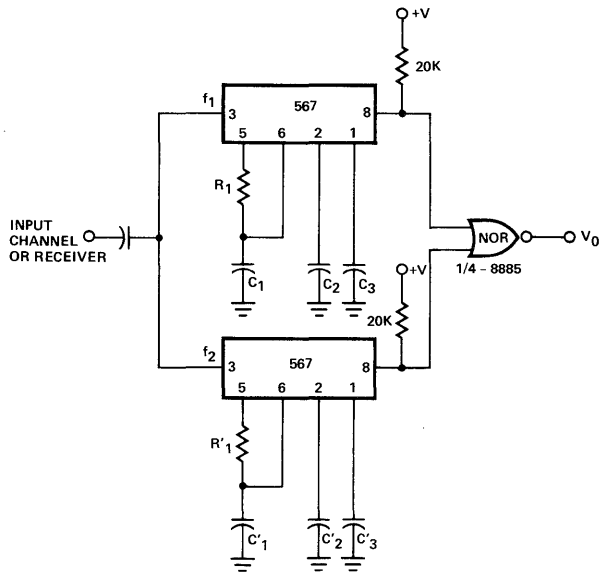
To change the center frequency, the value of R_1 can be changed with a mechanical or solid state switch, or additional C_1 capacitors may be added by grounding them through saturating npn transistors.

TYPICAL APPLICATIONS

CARRIER-CURRENT REMOTE CONTROL OR INTERCOM

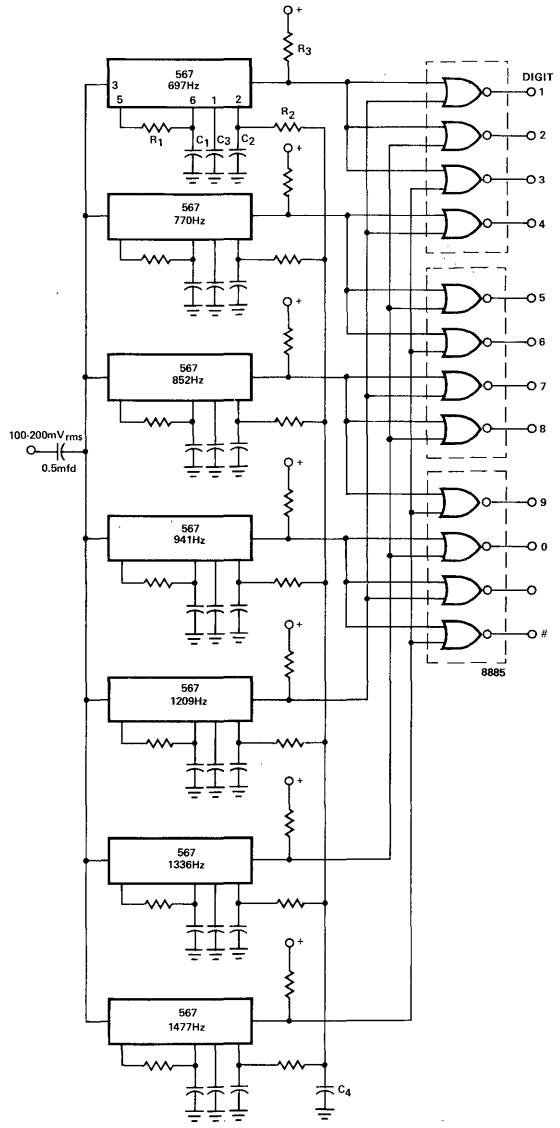


DUAL-TONE DECODER



1. Resistor and capacitor values chosen for desired frequencies and bandwidth.
2. If C_3 is made large so as to delay turn-on of the top 567, decoding of sequential (f_1, f_2) tones is possible.

TOUCH-TONE® DECODER

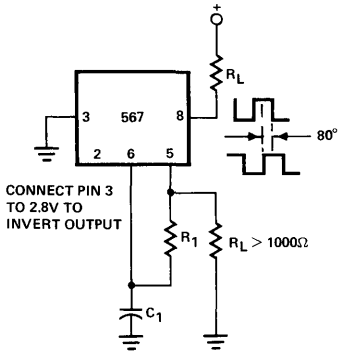


Component Values (Typical)

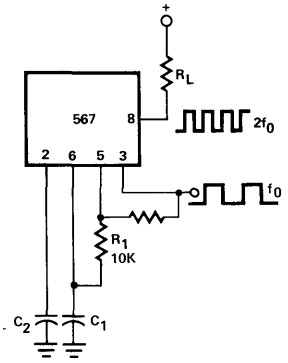
R_1	6.8 to 15K ohm
R_2	4.7K ohm
R_3	20K ohm
C_1	0.10 mfd
C_2	1.0 mfd 6V
C_3	2.2mfd 6V
C_4	250 6V

TYPICAL APPLICATIONS (Cont'd.)

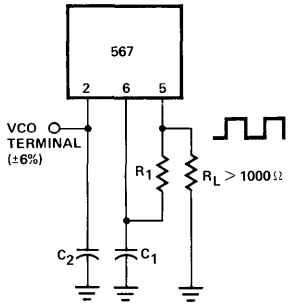
OSCILLATOR WITH QUADRATURE OUTPUT



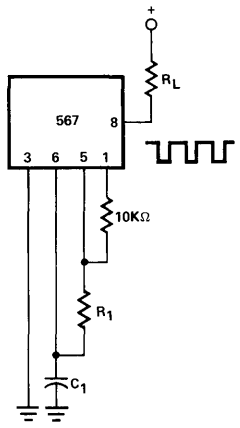
OSCILLATOR WITH DOUBLE FREQUENCY OUTPUT



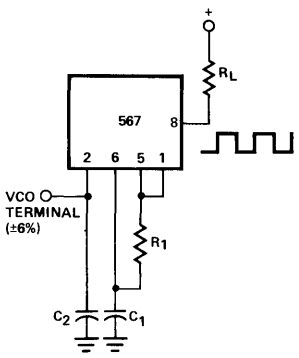
PRECISION OSCILLATOR WITH 20nsec SWITCHING



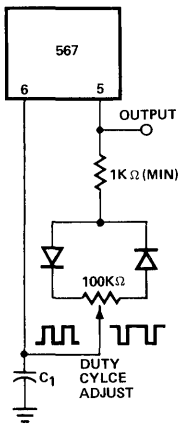
PULSE GENERATOR WITH 25% DUTY CYCLE



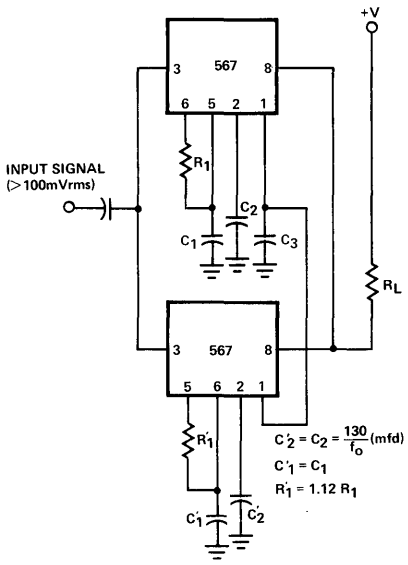
PRECISION OSCILLATOR TO SWITCH 100ma LOADS



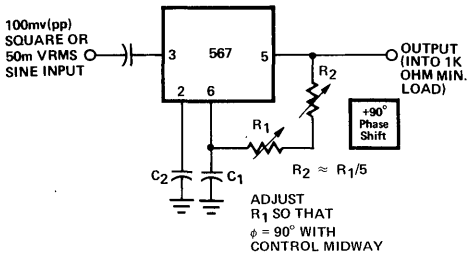
PULSE GENERATOR



24% BANDWIDTH TONE DECODER



O° TO 180° PHASE SHIFTER



SECTION 9
definition of terms

OP AMPS

AVERAGE INPUT OFFSET CURRENT t° COEFF – The change in input offset current divided by the change in ambient temperature producing it.

AVERAGE INPUT OFFSET VOLTAGE t° COEFF – The change in input offset voltage divided by the change in ambient temperature producing it.

COMMON MODE INPUT RESISTANCE – The resistance looking into both inputs tied together.

COMMON MODE REJECTION RATIO (CMRR) – The ratio of the change of input offset voltage to the input common mode voltage change producing it.

FULL POWER BANDWIDTH – The maximum frequency at which the full sinewave output might be obtained.

INPUT BIAS CURRENT – The average of the two input currents at zero output voltage. In some cases, the input current for either input independently.

INPUT CAPACITANCE – The capacitance looking into either input terminal with the other grounded.

INPUT CURRENT – The current into an input terminal.

INPUT NOISE VOLTAGE – The square root of the mean square narrow-band noise voltage referred to the input.

INPUT OFFSET CURRENT – The difference in the currents into the two input terminals with the output at zero volts.

INPUT OFFSET VOLTAGE – That voltage which must be applied between the input terminals to obtain zero output voltage. The input offset voltage may also be defined for the case where two equal resistances are inserted in series with the input leads.

INPUT RESISTANCE – The resistance looking into either input terminal with the other grounded.

INPUT VOLTAGE RANGE – The range of voltages on the input terminals for which the amplifier operates within specifications. In some cases, the input offset specifications apply over the input voltage range.

LARGE-SIGNAL VOLTAGE GAIN – The ratio of the maximum output voltage swing to the change in input voltage required to drive the output to this voltage.

OUTPUT RESISTANCE – The resistance seen looking into the output terminal with the output at null. This parameter is defined only under small signal conditions at frequencies above a few hundred cycles to eliminate the influence of drift and thermal feedback.

OUTPUT SHORT-CIRCUIT CURRENT – The maximum output current available from the amplifier with the output shorted to ground or to either supply.

OUTPUT VOLTAGE SWING – The peak output swing, referred to zero, that can be obtained.

POWER CONSUMPTION – The DC power required to operate the amplifier with the output at zero and with no load current.

POWER SUPPLY REJECTION RATIO – The ratio of the change in input offset voltage to the change in supply voltages producing it.

RISE TIME – The time required for an output voltage step to change from 10% to 90% of its final value.

SLEW RATE – The maximum rate of change of output voltage under large signal condition.

SUPPLY CURRENT – The current required from the power supply to operate the amplifier with no load and the output at zero.

TEMPERATURE STABILITY OF VOLTAGE GAIN – The maximum variation of the voltage gain over the specified temperature range.

REGULATORS

DROPOUT VOLTAGE – The input-output voltage differential at which the circuit ceases to regulate against further reductions in input voltage.

INPUT-OUTPUT VOLTAGE DIFFERENTIAL – The range of voltage difference between the supply voltage and the regulated output voltage over which the regulator will operate.

LINE REGULATOR – The percentage change in output voltage for a specified change in input voltage.

LOAD REGULATOR – The percentage change in output voltage for a specified change in load current.

MAXIMUM POWER DISSIPATION – The maximum total device dissipation for which the regulator will operate within specifications.

OUTPUT NOISE VOLTAGE – The rms output noise voltage with constant load and no input ripple.

OUTPUT VOLTAGE RANGE – The range of output voltage over which the regulator will operate.

QUIESCENT CURRENT – That part of input current to the regulator that is not delivered to the load.

REGULATORS (Cont'd.)

REFERENCE VOLTAGE – The output of the reference amplifier measured with respect to the negative supply.

RIPPLE REJECTION – The ratio of the peak-to-peak input ripple voltage to the peak-to-peak output ripple voltage.

SENSE VOLTAGE – The voltage between current sense and current limit terminals necessary to cause current limiting.

SHORT CIRCUIT CURRENT LIMIT – The output current of the regulator with the output shorted to the negative supply.

STANDBY CURRENT DRAIN – The supply current drawn by the regulator with no output load and no reference voltage load.

COMPARATORS/SENSE INTERFACE

COMMON MODE FIRING VOLTAGE – The CM input voltage that exceeds the dynamic range of the inputs with strobe enabled resulting in the output switching states.

COMMON MODE RECOVERY TIME – The time from the turn off of the CM signal to the analog input threshold of the earliest sense line pulse signal that can be processed normally. Processed normally refers to bi-polar signals greater than or less than the input threshold with a corresponding proper output.

EQUIVALENT INPUT COMMON MODE NOISE VOLTAGE – The change in input offset voltage due to common mode input noise.

LOGIC INPUT HIGH VOLTAGE – The minimum voltage allowed at a bit control gate to hold the bit off.

LOGIC INPUT LOW VOLTAGE – The maximum voltage allowed at a bit control gate to hold the bit on.

OUTPUT SINK CURRENT – The maximum negative current that can be delivered by the comparator.

PEAK OUTPUT CURRENT – The maximum current that may flow into the output load without causing damage to the comparator.

PROPAGATION DELAY – The interval between the application of an input voltage step and its arrival at either output, measured at 50% of the final value.

RESPONSE TIME – The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage overdrive.

STROBE CURRENT – The maximum current drawn by the strobe terminals when it is at the zero logic level.

STROBE DELAY – The time delay measured from strobe to output threshold with a signal present exceeding the input threshold.

STROBE RELEASE TIME – The time required for the output to rise to the logic threshold voltage after the strobe terminal has been driven from the zero to the one logic level. Appropriate input conditions are assumed.

STROBED OUTPUT LEVEL – The DC output voltage, independent of input voltage, with the voltage on the strobe terminal equal to or less than a minimum specified amount.

SWITCHING SPEED – The time required to turn on the least significant bit.

THRESHOLD UNCERTAINTY – With all sense amps sharing the same input threshold less the uncertainty as a "0". This includes unit to unit, power supply and temperature variations.

THRESHOLD VOLTAGE – The typical referred to input voltage which determines whether an input is a "1" or a "0". A signal whose magnitude is greater than the threshold level is sensed as a logic "1" and a signal whose magnitude is less as a "0".

ZERO SCALE OUTPUT CURRENT – The output current for all bits turned off.

COMMUNICATIONS CIRCUITS

ACC DETECTOR SENSITIVITY – The ratio of the incremental differential DC voltage change at the ACC Detector Output Terminals to the incremental change in peak-to-peak voltage at the ACC Detector Input Terminal for a specified burst input level, with the local oscillator locked.

APC DETECTOR SENSITIVITY – The ratio of the incremental differential DC voltage change at the APC Detector Output Terminals to the incremental change in relative phase at the APC Detector Input Terminal for a specified burst input level.

AVERAGE TEMPERATURE COEFFICIENT OF OUTPUT VOLTAGE – The percentage change in output voltage for a specified change in ambient temperature.

BANDWIDTH – The frequency at which the differential gain is 3dB below its low frequency value.

COMMUNICATIONS CIRCUITS (Cont'd)

COLOR-DIFFERENCE DEMODULATION ANGLE – A color-difference demodulation angle is defined as the instantaneous phase of the (+) Chroma input signal which produces the most positive voltage at the respective color-difference output with the phase of Reference "A" taken at 3 degrees and the phase of Reference "B" taken at 106 degrees.

(+) CHROMA INPUT – A composite chroma signal containing the burst at a phase of 180 degrees is demodulated to produce specified color-difference demodulation angles when applied to the (+) Chroma input.

(-) CHROMA INPUT – A composite chroma signal containing the burst at a phase of 0 degrees is demodulated to produce specified color-difference demodulation angles when applied to the (-) Chroma input.

DIFFERENTIAL OUTPUT VOLTAGE SWING – The peak differential output swing that can be obtained without clipping.

DIFFERENTIAL VOLTAGE GAIN – The ratio of the change in differential output voltage to the change in differential input voltage producing it.

OSCILLATOR CONTROL SENSITIVITY – The ratio of the incremental change in oscillator free running frequency to the incremental change in the differential DC voltage at the APC Detector Output Terminals.

OUTPUT COMMON MODE VOLTAGE – The average of the voltages at the two output terminals.

OUTPUT OFFSET VOLTAGE – The difference between the voltages at the two output terminals with the inputs grounded.

TOTAL HARMONIC DISTORTION – The ratio of the sum of the amplitudes of all signals harmonically related to the fundamental, and the amplitude of the fundamental signal.

MOS

Signetics offers a broad line of MOS products including Dynamic and Static Shift Registers, Random Access Memories and Read-only Memories. The 2500 series is fabricated using Signetics' advanced P-Channel SILICON-GATE PROCESS which provides compatibility with 5 volt TTL/DTL, high speed, and low power dissipation. Also available are the 2000 and 2400 series which are P-Channel metal gate devices. MOS products are available in commercial temperature ranges. All silicon gate devices are available in silicone dual in-line packages.

DYNAMIC SHIFT REGISTERS

2502
Quad 256-Bit
10MHz Typ. Data Rate
C_{CL} = 140pF max.
Power Supplies +5, -5V
40μW/bit/MHz
Multiplexed Data

2503
Dual 512-Bit
10MHz Typ. Data Rate
C_{CL} = 140pF max.
Power Supplies +5, -5V
40μW/bit/MHz
Multiplexed Data

2504
Single 1024-Bit
10MHz Typ. Data Rate
C_{CL} = 140pF max.
Power Supplies +5, -5V
40μW/bit/MHz
Multiplexed Data

2505/2524
512-Bit
5MHz Typ. Clock Rate
C_{CL} = 80pF
Power Supplies +5, -5V
100μW/bit/MHz
Recirculate Logic

2506
Dual 100-Bit
5MHz Typ. Clock Rate
C_{CL} = 40pF max.
Power Supplies +5, -5V
400μW/bit/MHz
Bare Drain Output

2507
Dual 100-Bit
5MHz Typ. Clock Rate
C_{CL} = 40pF max.
Power Supplies +5, -5V
400μW/bit/MHz
Resistor Pull-down (7.5K)

2512/2525
1024-Bit
5MHz Typ. Clock Rate
C_{CL} = 140 pF
Power Supplies +5, -5V
150μW/bit/MHz
Recirculate Logic

2515
Dual 512-Bit DSR
5MHz Clock Rate
C_{CL} = 140pF
Power Supplies +5, -5
100μW/bit/MHz
Recirculate +CS logic

2517
Dual 100-Bit
5MHz Typ. Clock Rate
C_{CL} = 40pF max.
Power Supplies +5, -5V
400μW/bit/MHz
Resistor Pull-down (20K)

STATIC SHIFT REGISTERS

2509
Dual 50 Bit
3MHz Typ. Clock Rate
Data & Clock TTL Compatible
Tri-State Outputs
Recirculate Logic
Power Supplies +5, -5, -12V

2510
Dual 100-Bit
3MHz Typ. Clock Rate
Data & Clock TTL Compatible
Tri-State Outputs
Recirculate Logic
Power Supplies +5, -5, -12V

2511
Dual 200-Bit
3MHz Typ. Clock Rate
Data & Clock TTL Compatible
Tri-State Outputs
Recirculate Logic
Power Supplies +5, -5, -12V

2518
Hex 32-Bit
2MHz Typ. Clock Rate
Data & Clock TTL Compatible
Recirculate Logic
Power Supplies +5, -12V

2519
Hex 40-Bit
2MHz Typ. Clock Rate
Data & Clock TTL Compatible
Recirculate Logic
Power Supplies +5, -12V

2521
Dual 128-Bit
3MHz Typ. Clock Rate
Data & Clock TTL Compatible
Recirculate Logic
Power Supplies +5, -12V

2522
Dual 132-Bit
3MHz Typ. Clock Rate
Data & Clock TTL Compatible
Recirculate Logic
Power Supplies +5, -12V

2000 SERIES
Static Shift Registers
C_L = 5pF
-14, -28V Power Supplies

2001
Dual 16-Bit SSR
0-1MHz

2002
Dual 25-Bit SSR
0-1MHz

2003
Dual 32-Bit SSR
0-1MHz

2004
Dual 50-Bit SSR
0-1MHz

2005
Dual 100-Bit SSR
0-1MHz

2010
Dual 100-Bit SSR
0-3MHz

RANDOM ACCESS MEMORIES

2501
256x1 Static RAM
Decoded
Access Time 1us Max.
1mW/bit Typ.
Power Supplies +5, -7, -10V or
+5, -9, -9V

2508
1024 x 1 Dynamic RAM
Decoded
Access Time 330ns
Cycle Time 500ns
3 Chip Selects
2.7mA
4 Clocks
+5, -12V
TTL Compatible Inputs
100mW

READ-ONLY MEMORIES

2513
64x8x5 Static Character Generator
Row Output
600ns Max. Access Time
ASCII Font Std.
Power Supplies +5, -5, -12V
350mW

2514
512x5 Read-Only Memory
600ns Max. Access Time
Power Supplies +5, -5, -12V
350mW

2516
64x6x8 Static Character Generator
Column Output
750ns Max. Access Time
Power Supplies +5, -5, -12V
415mW

2400 SERIES
Static Read-Only Memories
550ns Access Time
250mW
+12, -12V Power Supplies
Bare Drain or MOS Pull-Down
Resistor

2410
256x4
16-pin DIP

2420
256x4, 128x8
Single or 3-line Chip Enable
24-pin DIP

2430
256 x 8, 512 x 4
Single or 3-line Chip Enable
24-pin DIP

SECTION 10
sales offices

- **New England Regional Sales Office:** Miller Building Suite 11. 594 Marrett Road. Lexington. Massachusetts 02173
  Phone. (617) 861-0840 TWX: (710) 326-6711
- **Atlantic States Regional Sales Office:** 2460 Lemoine Ave.. Fort Lee. New Jersey 07024
  Phone: (201) 947-9870 TWX: (710) 991-9794

  Florida: 3267 San Mateo. Clearwater. 33515
  Phone: (813) 726-3469 TWX: (810) 866-0437

  Florida: 4347 Northwest 2nd Court
  Boca Raton, Florida 33432 Phone: (305) 391-8318 TWX: (510) 953-7538

  Maryland: Silver Springs
  Phone: (301) 946-6030

  Pennsylvania and Southern New Jersey. P.O. Box 431, Oakwood Drive, Medford, New Jersey 08055
  Phone: (609) 665-5071

  Virginia: 12001 Whip Road. Reston. 22070
  Phone: (301) 946-6030
- **Central Regional Sales Office:** 5105 Tollview Drive. Suite 209. Rolling Meadows. Illinois 60008
  Phone: (312) 259-8300 TWX: (910) 687-0765

  Minnesota: 7710 Computer Ave., Suite 132, Minneapolis 55435
  Phone: (612) 922-2801 TWX: (910) 576-2740

  Ohio: 3300 So. Dixie Drive, Suite 220, Dayton 45439
  Phone: (513) 294-8722

- **Northwest Regional Sales Office:** 811 E. Arques. Sunnyvale. Ca 94086
  Phone: (408) 739-7700 TWX: (910) 339-9220
  (910) 339-9283
- **Southwest Regional Sales Office:** 2061 Business Center Dr., Suite 214, Irvine, Ca. 92664
  Phone: (714) 833-8980, (213) 437-6718, TWX: (910) 595-1506

  California: P.O. Box 788. Del Mar. 92014
  Phone: (714) 453-7570

REPRESENTATIVES

ALABAMA
Huntsville 35801: Compar Corp., 904 Bob Wallace Ave.. Suite A
Phone: (205) 539-8476

ARIZONA
Scottsdale 85252: Compar Corp., Box 1607
Phone: (602) 947-4336 TWX: (910) 950-1293

CALIFORNIA
San Diego 92123: Celtec Company, Inc., 8799 Balboa Avenue
Phone: (714) 279-7961 TWX: (910) 335-1512

CANADA
Toronto 17, Ontario: Corning Glass Works of Canada, Ltd., 135 Vanderhoff Ave.
Phone. (416) 421-1500 TWX: (610) 491-2155

Montreal 265, Quebec: Corning Glass Works of Canada, 7065 Chester Ave.

COLORADO
Denver 80237: Parker Webster Company, 8213 E. Kenyon Dr.
Phone: (303) 770-1972

CONNECTICUT
Hamden 06518: Compar Corp., P.O. Box 5204
Phone: (203) 288-9276 TWX: (710) 465-1540

FLORIDA
Altamonte Springs 32701: WMM Associates Inc., 515 Tivoli Ct.
Phone: (305) 831-4645
Clearwater 33516: WMM Associates Inc., 1260A S. Highland Ave.
Phone: (813) 446-0075
Pompano Beach 33060: WMM Associates Inc., 721 South East 6th Terrace
Phone: (305) 943-3091

INDIANA
Indianapolis 46250: R. H. Newsom Associates, 6320 Woburn Dr.
Phone: (317) 849-4442

MARYLAND
Silver Springs 20904: Mechtronics Sales Inc., 11700 Old Columbia Pike, Suite L-6 Phone: (301) 622-2420

MASSACHUSETTS
Newton Highlands 02161: Compar Corp., 88 Needham Street
Phone: (617) 969-7140 TWX: (710) 335-1686

MICHIGAN
Grosse Pointe Park 48230: Greiner Associates Inc., 15324 E. Jefferson
Phone: (313) 499-0188, (313) 499-0189 TWX: (801) 221-5157

MINNESOTA
Minneapolis 55416: Compar Corp., P O Box 16095
Phone: (612) 922-7011

MISSOURI
St. Louis 63141: Compar Corp., 11734 Lackland Industrial Drive
Phone: (314) 567-3399 TWX: (910) 764-0839

SOUTHERN NEW JERSEY AND PENNSYLVANIA
Haddonfield, N.J. 08033: Compar Corp., 15 Potter Street
Phone (609) 429-1526 TWX. (710) 896-0679

NEW MEXICO
Albuquerque 87104: Compar Corp., 113 Romero St. N.W.
Phone: (505) 242-3633 TWX: (910) 989-1659

UPSTATE NEW YORK
Dewitt 13214: TriTech Electronics, Inc.,
P.O. Box C Phone: (315) 446-2881

NORTH CAROLINA
Winston-Salem 27101: Compar Corp., 1106 Burke Street
Phone: (919) 723-1002 TWX: (510) 931-3101

OHIO
Dayton 45405: Compar Corp., P.O. Box 57. Forest Park Branch
Phone: (415) 435-1301
Fairview Park 44126: Compar Corp., P.O. Box 4791
Phone: (216) 333-4120 TWX: (810) 421-8396

TEXAS
Richardson 75080: Semiconductor Sales Associates, 312 North Central Expressway. Suite 213
Phone: (214) 231-6181

WASHINGTON
Bellevue 98009: Western Technical Sales, P.O. Box 902
Phone: (206) 454-3906 TWX: (910) 443-2309

DISTRIBUTORS

ARIZONA
Phoenix 85009: Hamilton/Avnet Electronics. 1739 N. 28th Ave.
Phone: (602) 269-1391, TELEX: 667-450

CALIFORNIA
Burbank 91504: Compar Corp., 2908 Naomi Avenue
Phone: (213) 843-1772 TWX: (910) 498-2203

Burlingame 94010: Compar Corp., 820 Airport Blvd.
Phone: (415) 347-5411 TWX: (910) 374-2366

Culver City 90230: Hamilton Electro Sales, 10912 W. Washington
Phone:(213) 559-3311 TELEX: 677-100, 674-381, 674-354

El Monte 91731: G.S. Marshall, 9674 Telstar Avenue
Phone: (213) 686-1500 TWX: (910) 587-1565

Los Angeles 90022: KT/Wesco Electronics, 5650 Jillson Street
Phone: (213) 685-9525 TWX: (910) 580-1980

Mountain View 94041: Hamilton/Avnet Electronics, 340 East Middlefield Rd
Phone: (415) 961-7000 TELEX: 348-201
Palo Alto 94303: Wesco Electronics, 3973 East Bayshore Road
Phone: (415) 968-3475 TWX: (910) 379-6488
San Diego 92111: G.S. Marshall, 7990 Engineer Road, Suite 1
Phone: (714) 278-6350 TWX: (910) 587-1565
San Diego 92123: Kierulff Electronics, 8797 Balboa Avenue
Phone: (714) 278-2112 TWX: (910) 335-1182

CANADA
Downsview, Ontario: Cesco Electronics, Ltd., 24 Martin Ross Avenue
Phone: (416) 638-5250
Montreal, Quebec: Cesco Electronics, Ltd., 4050 Jean Talon West
Phone: (514) 735-5511 TWX: (610) 421-3445
Ottawa, Ontario: Cesco Electronics, Ltd., 1300 Carling Avenue
Phone: (613) 729-5118
Quebec: Cesco Electronics, Ltd., 128 St. Vallier Street
Phone: (418) 524-3518

COLORADO
Denver 80216: Hamilton/Avnet Electronics, 1400 W. 46th Avenue
Phone: (303) 433-8551 TELEX: 45872

FLORIDA
Hollywood 33021: Hamilton/Avnet Electronics, 4020 No. 29th Avenue
Phone: (305) 925-5401 TELEX: 51-4328
Orlando 32805: Hammond Electronics, 911 West Central Blvd.
Phone: (305) 241-6601 TWX: (810) 850-4121

ILLINOIS
Elmhurst 60126: Semiconductor Specialists, Inc., 195 Spangler Avenue Elmhurst Industrial Park
Phone: (312) 279-1000 TWX: (910) 254-0169
Schiller Park 60176: Hamilton/Avnet Electronics, 3901 Pace Court
Phone: (312) 678-6310 TELEX: 728-330

MARYLAND
Hanover 21076: Hamilton/Avnet Electronics, 7255 Standard Drive
Phone: (301) 796-5000 TELEX: 879-68
Rockville 20850: Pioneer Washington Electronics, Inc., 1037 Taft Street
Phone: (301) 424-3300

MASSACHUSETTS

Burlington 01803: Hamilton/Avnet Electronics
207 Cambridge Street
Phone: (617) 272-3060 TELEX: 9494-61
Needham Heights 02194: Kierulff/Schley, 14 Charles Street
Phone: (617) 449-3600 TWX: (710) 325-1179

MICHIGAN

Livonia 48150: Hamilton/Avnet Electronics, 13150 Wayne Rd.
Phone: (313) 522-4700
Detroit 48240: Semiconductor Specialists, Inc., 25127 W Six Mile Road
Phone: (313) 255-0300 TWX: (910) 254-0169

MINNESOTA

Minneapolis 55420: Semiconductor Specialists, Inc., 8030 Cedar Ave., S.
Phone (612) 854-8841

MISSOURI

Hazelwood 63042: Hamilton/Avnet Electronics, 400 Brookes Lane
Phone: (314) 731-1144 TELEX: 442348

NORTHERN NEW JERSEY

Cedar Grove 07009: Hamilton/Avnet Electronics, 220 Little Falls Road
Phone: (201) 239-0800 TELEX: 138313

SOUTHERN NEW JERSEY AND PENNSYLVANIA

Cherry Hill, N.J. 08034: Hamilton/Avnet Electronics, 1608-10 W Marlton Pike
Phone: (609) 662-9337 TELEX: 834737
Cherry Hill, N.J. 08034: Milgray-Delaware Valley, 1165 Marlkress Road
Phone: N.J. (609) 424-1300 Phila. (215) 228-2000 TWX: (710) 896-0405

NEW YORK

Buffalo 14202: Summit Distributors, Inc., 916 Main Street
Phone: (716) 884-3450 TWX: (710) 522-1692
Hauppauge, L.I. 11787: Semiconductor Concepts, Inc., Engineer Road
Phone: (516) 273-1234 TWX: (510) 227-6232
Woodbury, L. I. 11797: Harvey Radio, 60 Crossways Park West
Phone: (516) 921-8700 TWX: (510) 221-2184
New York 10011: Terminal-Hudson Electronics, 23C West 17th Street
Phone: (212) 243-5200 TWX: (710) 581-3962

OHIO

Cleveland 44105: Pioneer Standard Electronics, P.O. Box 05100
Phone: (216) 587-3600, TWX: (810) 421-8238
Kettering 45429: Arrow Electronics, 3100 Plainfield Road
Phone (513) 253-9176 TWX: (810) 459-1611

TEXAS

Dallas 75207: Hamilton/Avnet Electronics, 2403 Farrington Ave
Phone: (214) 638-2850 TELEX: 732359
Dallas 75220: Solid State Electronics Company, P O. Box 20299
Phone: (214) 352-2601
Houston 77019: Hamilton/Avnet Electronics, 1216 West Clay Street
Phone. (713) 526-4661 TELEX. 762589
Houston 77036: Universal Electronics, 5723 Savoy Street
Phone: (713) 781-0421

WASHINGTON

Seattle 98121: Hamilton/Avnet Electronics, 2320 Sixth Avenue
Phone: (206) 624-5930 TELEX: 32249

INTERNATIONAL SALES

EUROPEAN HEADQUARTERS:

Signetics International Corp., Yeoman House, 63 Croydon Rd.,
Penge, London, S.E. 20, England
Phone: (01) 6592111 TELEX: 946619

FRANCE:

Signetics S.A.R.L., 90 Rue Baudin F 92 Levallois-Perret. France
Phone: 739-85-80/739-96-40 TELEX 62014

WEST GERMANY:

Signetics GmbH, Ernsthaldenstrasse 17. D 7 Stuttgart 80. West Germany
Phone: (0711) 73-50-61 TELEX: 7255798

STOCKING DISTRIBUTORS

AUSTRALIA

Pye Industries Ltd., Technico Electronics Division. 53 Carrington Rd.
Marrickville. Sydney. N.S.W.
Phone 55-0411 TELEX: 790-21490
Pye Industries Ltd., Technico Electronics Division. 2-18 Normanby Rd.
South Melbourne. Vic
Phone. 69-60-61 TELEX 31240

WEST GERMANY

EBV Elektronik GmbH. Augustenstrasse 79. D-8 Munchen 2
Phone: (0811) 52-43-40/48 TELEX: 524535
EBV Elektronik GmbH. Mylusstrasse 54. D-6 Frankfurt/Main 1
Phone: (0611) 72-04-16/18 TELEX: 413590
EBV Elektronik GmbH. Scheurenstrasse 1. D-4 Dusseldorf
Phone: (0211) 8-48-46/47 TELEX: 8587267
"Mutron" Muller & Co. KG. Postfach 164. Bornstrasse 65. D-28 Bremen 1
Phone. (0421) 31-04-85 TELEX: 245-325
Dima-Elektronik, Karl Manger KG, Postfach 80 0744.
Robert-Leichtstrasse 43. D-7 Stuttgart-Vaihingen 80
Phone. (0711) 73-40-50/9 TELEX: 255-642
Distron GmbH, D-1 Berlin 31, Wilhelmsaue 39-41
Phone. 0311/870144 TELEX: 18-27-58
Signetics GmbH, Eulenkrugstr, 81 E, D-2 Hamburg 67
Phone: (411) 60-35-242

AUSTRIA

Ing. Ernst Steiner, Beckgasse 30, A-1130 Wien
Phone: (222) 82-10-605

SWITZERLAND

Dewald AG, Seestrasse 561. CH 8038. Zurich
Phone. (051) 45-13-00 TELEX: 52012

FRANCE

S.A. Gallec Electronique, 78. Avenue des Champs-Elysées. Paris 8e
Phone: 359-58-38/255-67-10/255-67-11
R.T.F., 73, Av. de Neuilly, 92 - Neuilly sur Seine, Paris
Phone: 722.70.40 TELEX: 65.933
Elic 38, le Bureau Barisien S.A.R.L., 8-10 Avenue du Grand Sablon.
38-La Tronche
Phone (76) 87-67-71 TELEX: 32-739

ITALY

Metroelettronica S.A.S., Viale Cirene 18. I-20135 Milano
Phone: 546-26-41 TELEX. 33-168 Metronic

UNITED KINGDOM

Quarndon Electronics Ltd., Slack Lane. Derby. Derbyshire
Phone. (0332) 3 26 51 TELEX: 37163
S.D.S. (Portsmouth) Ltd., Hilsea Industrial Estate. Portsmouth. Hampshire
Phone: 6 53 11 TELEX: 86114
Semicomps Ltd., 5 Northfield Industrial Estate. Beresford Ave., Wembley.
Middlesex Phone: (01) 903-3161 TELEX: 935243
A.M. Lock & Co. Ltd., 79 Union St., Oldham, Lancs, England
Phone: 061-624-6832

SCOTLAND

Semicomps Northern Ltd., 44. The Square. Kelso. Roxburghshire
Phone: 2366 TELEX: 72692

SWEDEN, NORWAY, FINLAND

A.B. Kuno Källman, Järntorget 7. S-413 04 Gothenburg. Sweden
Phone: 17-01-20 TELEX: 21072

DENMARK

E. Friis-Mikkelsen A/S, Krogshojvej 51. DK-2880 Bagsvaerd
Phone: (01) 986333 TELEX: 2350

THE NETHERLANDS

Mulder-Hardenberg, P.O. Box 5059, Westerhoutpark 1-A, Haarlem
Phone: (023) 3191 84 TELEX: 41431

JAPAN

Asahi Glass Co., Ltd., 1-2. Marunouchi. 2 Chome Chiyoda-ku. Tokyo
Phone: 211-0411 TELEX: 4616

SOUTH AFRICA

Indentronics Proprietary, Ltd., Sheerline House. 24 Webber Street.
Selby. Johannesburg
Phone: 834-4971/2/3 TELEX: 43-7660JH

REPRESENTATIVES

SWEDEN, NORWAY, FINLAND

A.B. Kuno Källman, Järntorget 7. S-413 04 Gothenburg. Sweden
Phone. 17-01-20 TELEX: 21072

AUSTRALIA

Corning Australia, Technical Products Division, Room 13. Barden House.
Fetherston Street. Bankstown. N.S.W. 2200
Phone: 602-9011 TELEX: 21539

ISRAEL

Rapac Electronics Ltd., P.O. Box 18053, 15 Karl Herbst St.,
Tel-Baruch, Tel-Aviv Phone: 77 71 15,6,7 TELEX: TV 528

JAPAN

Asahi Glass Co., Ltd., 1-2. Marunouchi. 2 Chome. Chiyoda-ku. Tokyo
Phone: 211-0411 TELEX: 4616

SWITZERLAND

Dewald AG, Seestrasse 561. CH 8038. Zurich
Phone (051) 45-13-00 TELEX: 52012

INDIA

Semiconductors Limited, Radia House, 6, Rampart Row,
Fort, Bombay - 1
Phone: 293667 TELEX: Transducer, Bombay

SOUTH AFRICA

Indentronics Proprietary, Ltd., Sheerline House. 24 Webber Street.
Selby. Johannesburg
Phone: 834-4971/2/3 TELEX: 43-7660JH

Signetics

811 EAST ARQUES AVENUE
SUNNYVALE, CALIFORNIA 94086
TEL: (408) 739-7700
TWX: (910) 339-9283