ALPHA & OMEGA SEMICONDUCTOR, INC.

Nov 2002

AO3404
N-Channel Enhancement Mode Field Effect Transistor

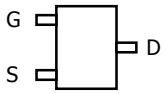
General Description

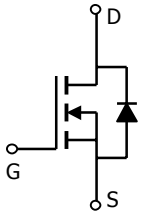
The AO3404 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge. This device may be used as a load switch or in PWM applications.

Features

V_{DS} (V) = 30V
I_D = 5.8A
$R_{DS(ON)}$ < 28mΩ (V_{GS} = 10V)
$R_{DS(ON)}$ < 42mΩ (V_{GS} = 4.5V)

TO-236
(SOT-23)
Top View





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [A]	T_A=25°C	I_D	5.8	A
	T_A=70°C		4.9	
Pulsed Drain Current [B]		I_{DM}	20	
Power Dissipation	T_A=25°C	P_D	1.4	W
	T_A=70°C		1	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	65	90	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		85	125	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	43	60	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=24V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1	1.9	3	V
$I_{D(ON)}$	On state drain current	V_{GS}=4.5V, V_{DS}=5V	20			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=5.8A		22.5	28	mΩ
		T_J=125°C		31.3	38	
		V_{GS}=4.5V, I_D=5.0A		34.5	42	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=5.8A	10	14.5		S
V_{SD}	Diode Forward Voltage	I_S=1A		0.76	1	V
I_S	Maximum Body-Diode Continuous Current				2.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		680		pF
C_{oss}	Output Capacitance			102		pF
C_{rss}	Reverse Transfer Capacitance			77		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		3		Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=5.8A		13.88		nC
Q_g(4.5V)	Total Gate Charge			6.78		nC
Q_{gs}	Gate Source Charge			1.8		nC
Q_{gd}	Gate Drain Charge			3.12		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=2.7Ω, R_{GEN}=3Ω		4.6		ns
t_r	Turn-On Rise Time			3.8		ns
$t_{D(off)}$	Turn-Off DelayTime			20.9		ns
t_f	Turn-Off Fall Time			5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=5.8A, dI/dt=100A/µs		16.1		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=5.8A, dI/dt=100A/µs		7.4		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The value in any a given application depends on the user's specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6 are obtained using 80µs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

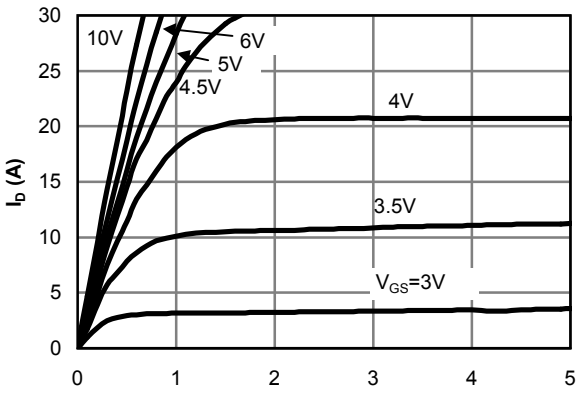


Fig 1: On-Region Characteristics

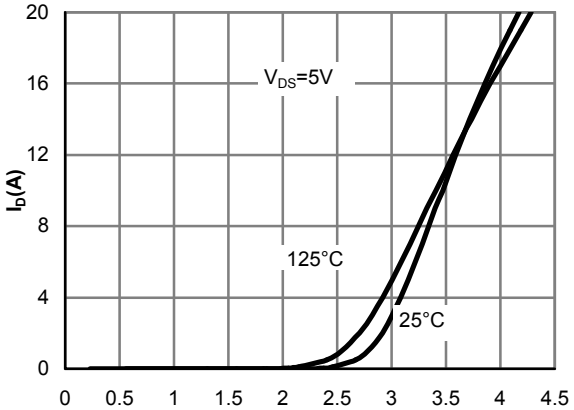


Figure 2: Transfer Characteristics

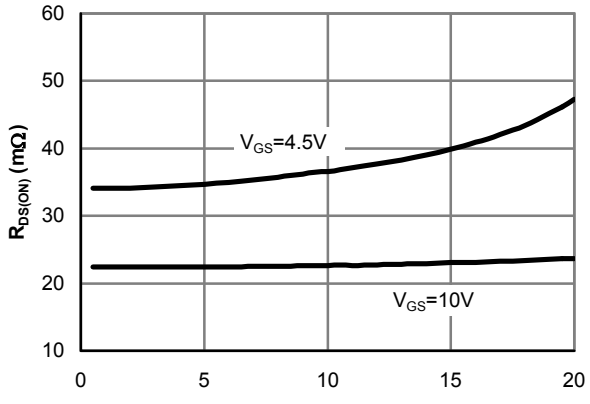


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

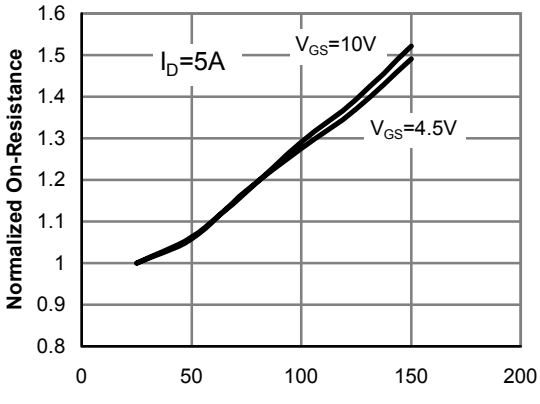


Figure 4: On-Resistance vs. Junction Temperature

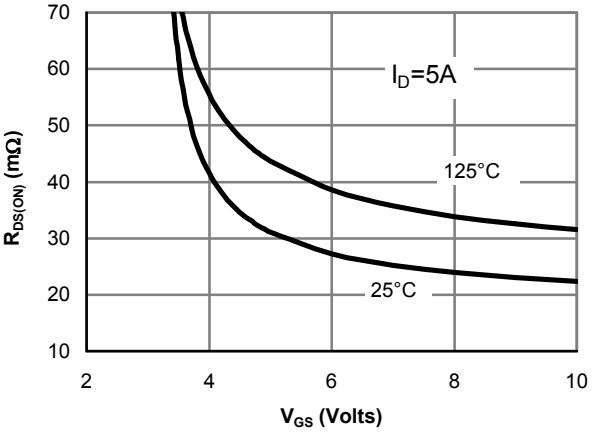


Figure 5: On-Resistance vs. Gate-Source Voltage

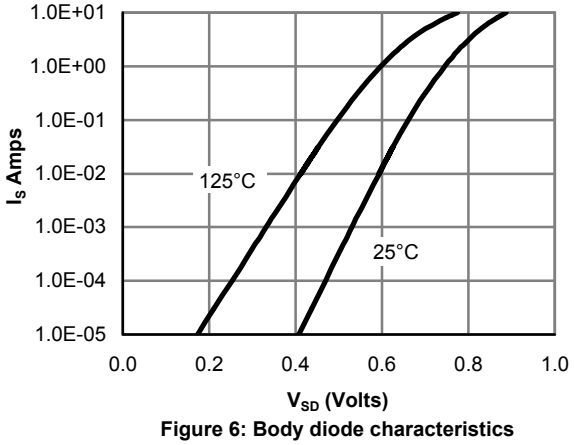


Figure 6: Body diode characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

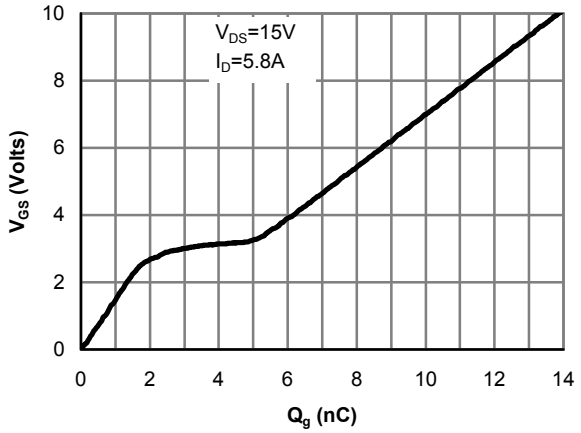


Figure 7: Gate-Charge characteristics

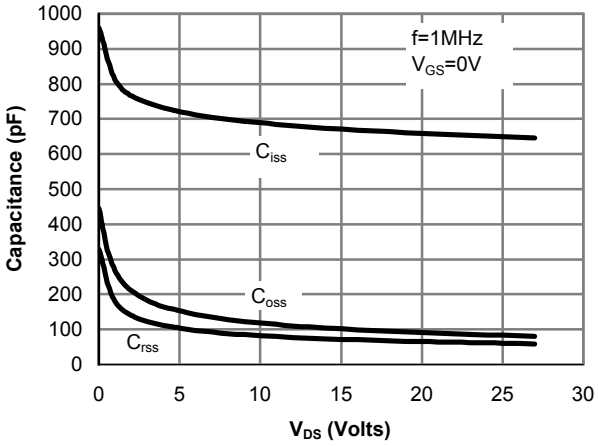


Figure 8: Capacitance Characteristics

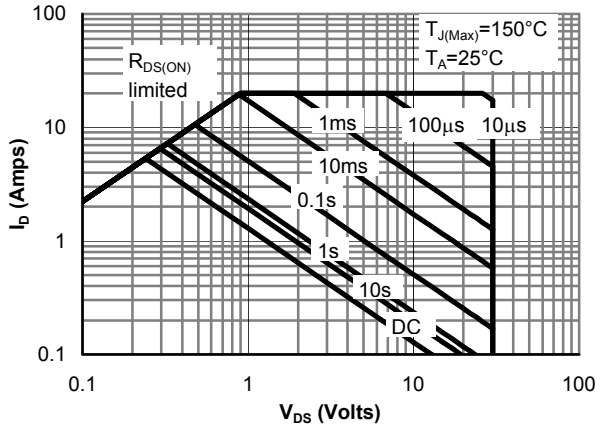


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

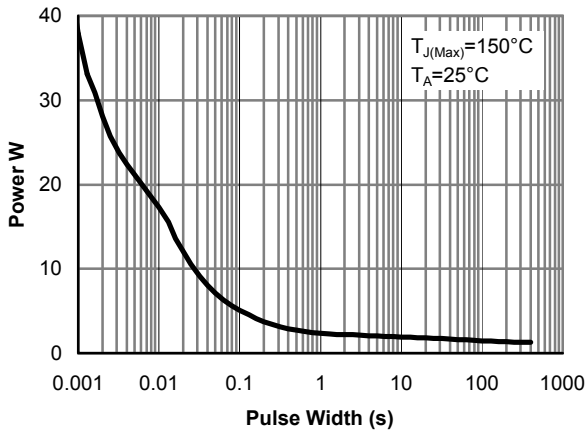


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

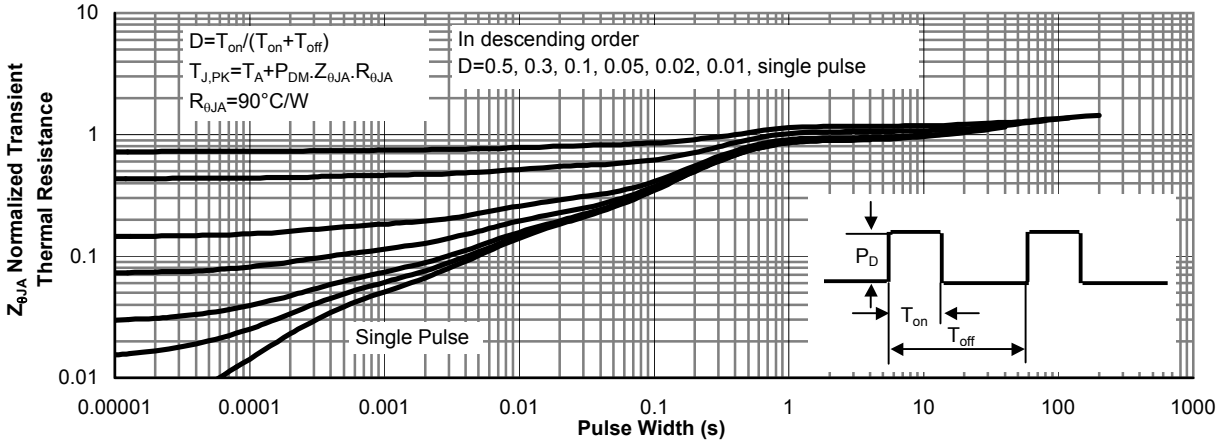


Figure 11: Normalized Maximum Transient Thermal Impedance

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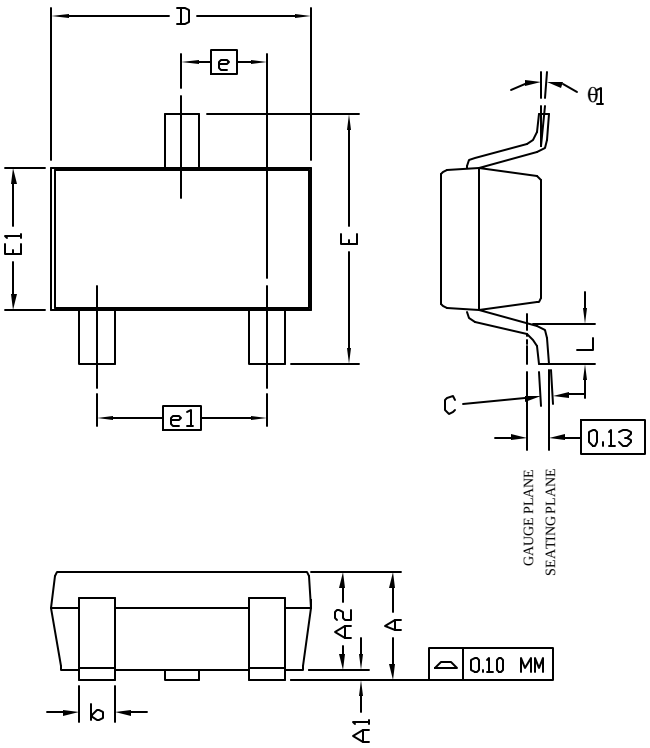
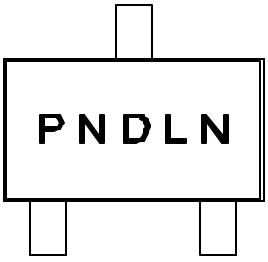
SOT-23 Package Data



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	1.00	——	1.25
A1	0.00	——	0.10
A2	1.00	1.10	1.15
b	0.35	0.40	0.50
C	0.10	0.15	0.25
D	2.80	2.90	3.04
E	2.60	2.80	2.95
E1	1.40	1.60	1.80
e	——	0.95 BSC	——
e1	——	1.90 BSC	——
L	0.40	——	0.60
θ1	1°	5°	8°

NOTE:
1. LEAD FINISH: 150 MICROINCHES (3.8 um) MIN. THICKNESS OF Tin/Lead (SOLDER) PLATED ON LEAD
2. TOLERANCE ±0.10 mm (4 mil) UNLESS OTHERWISE SPECIFIED
3. COPLANARITY : 0.10 mm
4. DIMENSION L IS MEASURED IN GAGE PLANE

PACKAGE MARKING DESCRIPTION

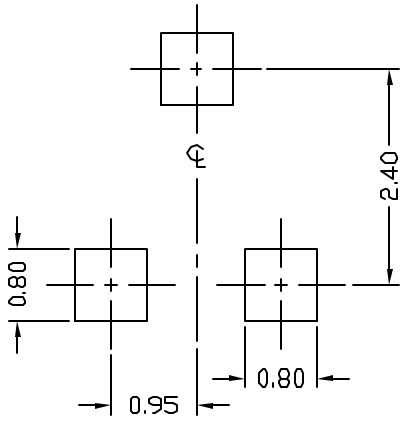


SOT-23 PART NO. CODE

PART NO.	CODE
AO3404	A0

NOTE:
P N - PART NUMBER CODE.
D - YAER AND WEEK CODE.
L N - ASSEMBLY LOT CODE, FAB AND ASSEMBLY LOCATION CODE.

RECOMMENDATION OF LAND PATTERN



Rev. A

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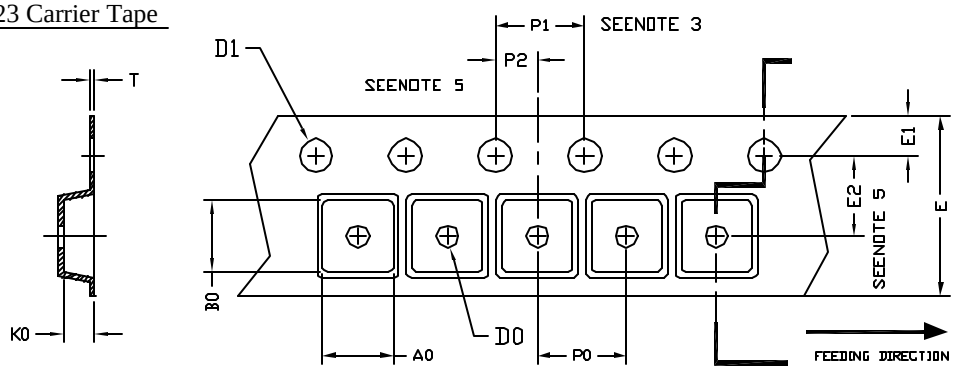
SOT-23 Tape and Reel Data

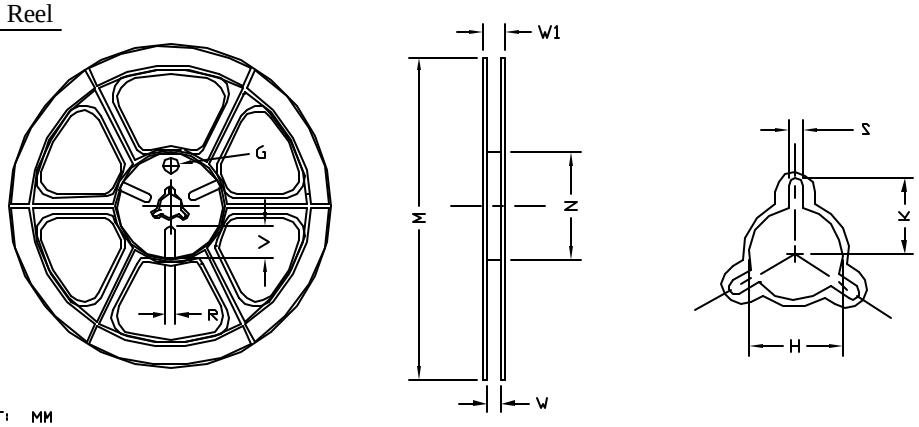
SOT-23 Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SOT-23 (8 mm)	3.15 ±0.10	3.20 ±0.10	1.40 ±0.10	1.00 MIN	1.50 +0.10	8.00 ±0.30	1.75 ±0.10	3.50 ±0.05	4.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.25 ±0.05

SOT-23 Reel



UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
8 mm	ø180	ø180.00 ±0.50	ø60.50	9.00 ±0.30	11.40 ±1.00	ø13.00 +0.50 -0.20	10.60	2.00 ±0.50	ø9.00	5.00	18.00

SOT-23 Tape

Leader / Trailer & Orientation