



AO6405

P-Channel Enhancement Mode Field Effect Transistor

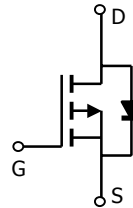
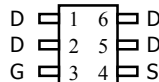
General Description

The AO6405 uses advanced trench technology to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use as a load switch or in PWM applications.

Features

- $V_{DS} (V) = -30V$
- $I_D = -5 A$
- $R_{DS(ON)} < 52m\Omega (V_{GS} = -10V)$
- $R_{DS(ON)} < 87m\Omega (V_{GS} = -4.5V)$

**TSOP6
Top View**



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^A	$T_A=25^\circ C$ $T_A=70^\circ C$	-5	A
		I_D	
Pulsed Drain Current ^B	I_{DM}	-20	
Power Dissipation ^A	$T_A=25^\circ C$ $T_A=70^\circ C$	2	W
		P_D	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ C$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	47.5	62.5	$^\circ C/W$
Maximum Junction-to-Ambient ^A		Steady-State	74	
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	37	50	$^\circ C/W$

Electrical Characteristics ($T_J=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=-250\mu\text{A}, V_{GS}=0\text{V}$	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-24\text{V}, V_{GS}=0\text{V}$ $T_J=55^\circ\text{C}$			-1 -5	μA
I_{GSS}	Gate-Body leakage current	$V_{DS}=0\text{V}, V_{GS}=\pm 20\text{V}$			± 100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu\text{A}$	-1	-1.8	-3	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-4.5\text{V}, V_{DS}=-5\text{V}$	-20			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-10\text{V}, I_D=5.0\text{A}$ $T_J=125^\circ\text{C}$		39 54	52 70	m Ω
		$V_{GS}=-4.5\text{V}, I_D=-4\text{A}$		67	87	
g_{FS}	Forward Transconductance	$V_{DS}=-5\text{V}, I_D=-5\text{A}$	6	8.6		S
V_{SD}	Diode Forward Voltage	$I_S=-1\text{A}, V_{GS}=0\text{V}$		-0.77	-1	V
I_S	Maximum Body-Diode Continuous Current				-2.8	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	$V_{GS}=0\text{V}, V_{DS}=-15\text{V}, f=1\text{MHz}$		700		pF
C_{oss}	Output Capacitance			120		pF
C_{rss}	Reverse Transfer Capacitance			75		pF
R_g	Gate resistance	$V_{GS}=0\text{V}, V_{DS}=0\text{V}, f=1\text{MHz}$		10		Ω
SWITCHING PARAMETERS						
$Q_g(10\text{V})$	Total Gate Charge (10V)	$V_{GS}=-10\text{V}, V_{DS}=-15\text{V}, I_D=-5\text{A}$		14.7		nC
$Q_g(4.5\text{V})$	Total Gate Charge (4.5V)			7.6		nC
Q_{gs}	Gate Source Charge			2		nC
Q_{gd}	Gate Drain Charge			3.8		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=-10\text{V}, V_{DS}=-15\text{V}, R_L=3\Omega,$ $R_{GEN}=3\Omega$		8.3		ns
t_r	Turn-On Rise Time			5		ns
$t_{D(off)}$	Turn-Off DelayTime			29		ns
t_f	Turn-Off Fall Time			14		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=-5\text{A}, dI/dt=100\text{A}/\mu\text{s}$		23.5		ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=-5\text{A}, dI/dt=100\text{A}/\mu\text{s}$		13.4		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The value in any a given application depends on the user's specific board design. The current rating is based on the $t \leq 10\text{s}$ thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C: The $R_{\theta JA}$ is the sum of the thermal impedance from junction to lead $R_{\theta JL}$ and lead to ambient.

D: The static characteristics in Figures 1 to 6, 12, 14 are obtained using 80 μs pulses, duty cycle 0.5% max.

E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with $T_A=25^\circ\text{C}$. The SOA curve provides a single pulse rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

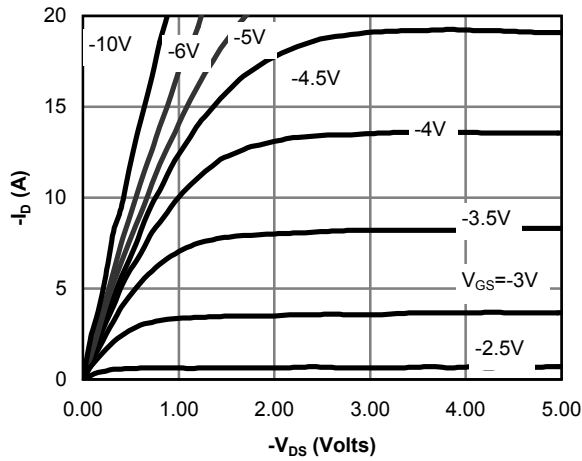


Figure 1: On-Region Characteristics

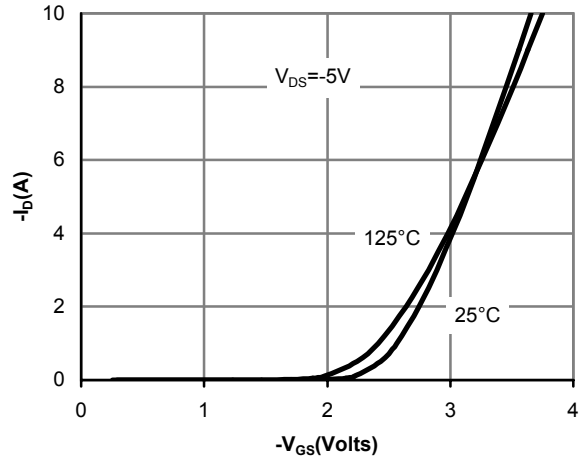


Figure 2: Transfer Characteristics

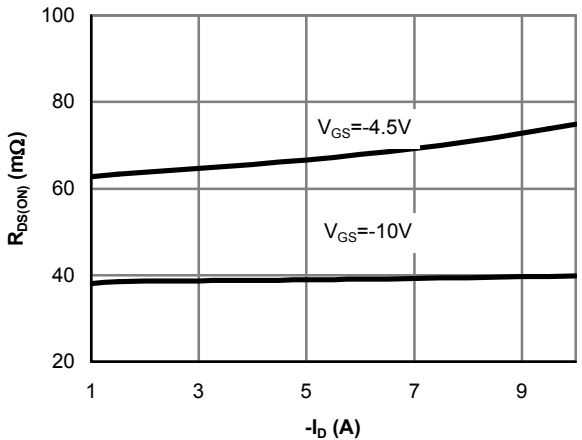


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

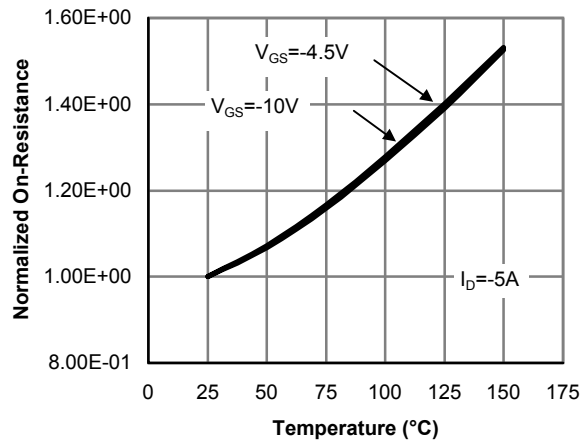


Figure 4: On-Resistance vs. Junction Temperature

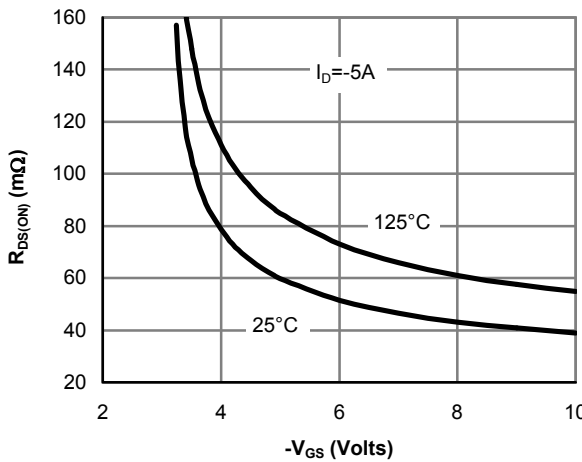


Figure 5: On-Resistance vs. Gate-Source Voltage

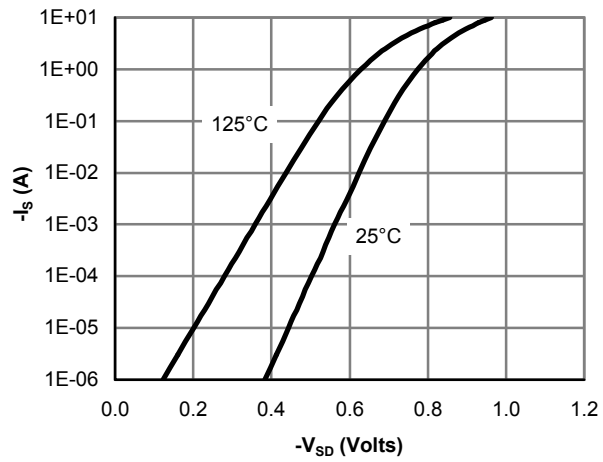


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

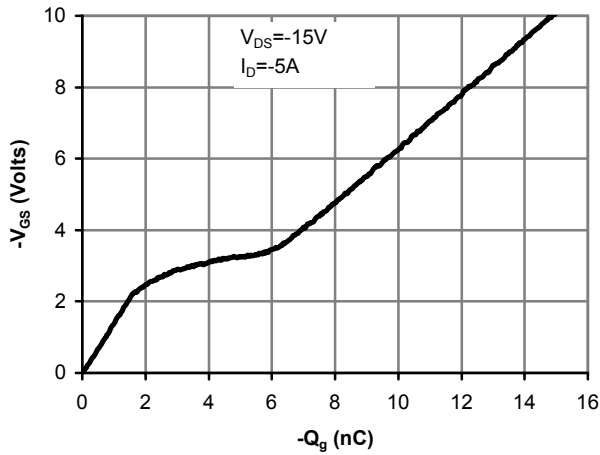


Figure 7: Gate-Charge Characteristics

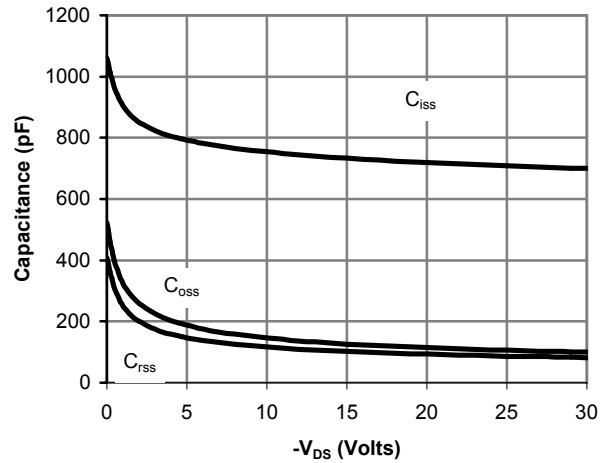


Figure 8: Capacitance Characteristics

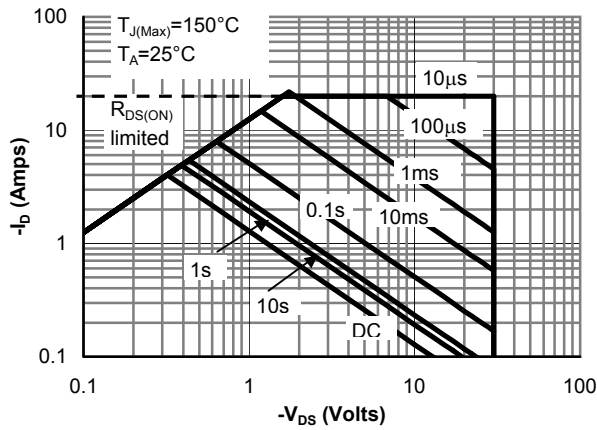


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

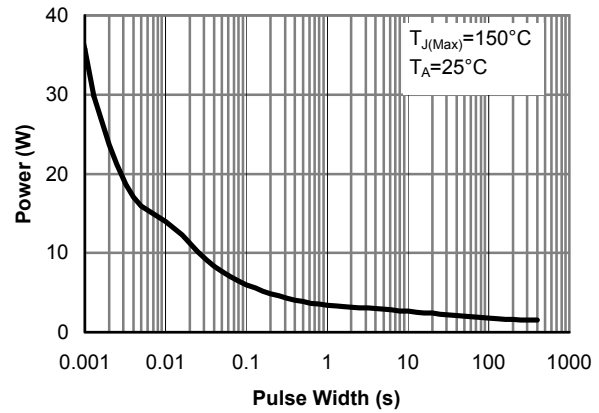


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

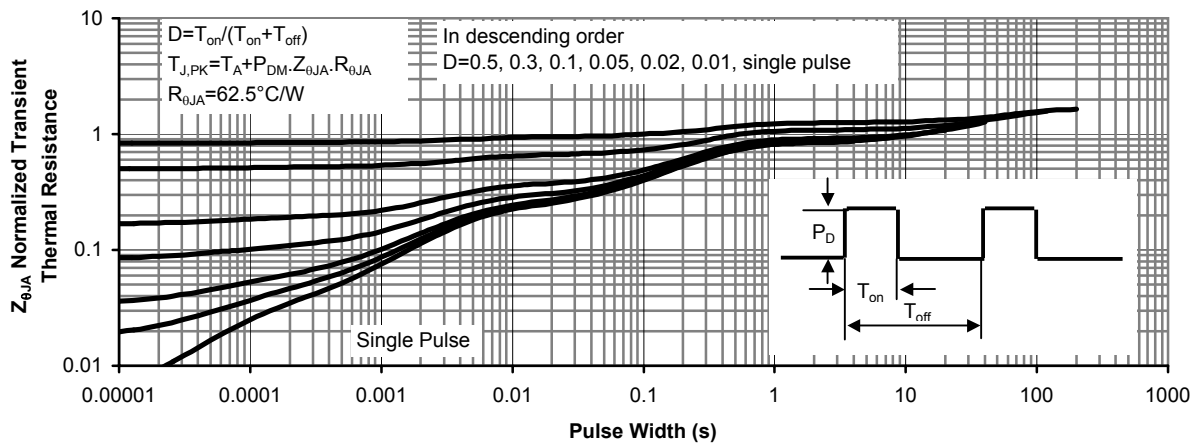
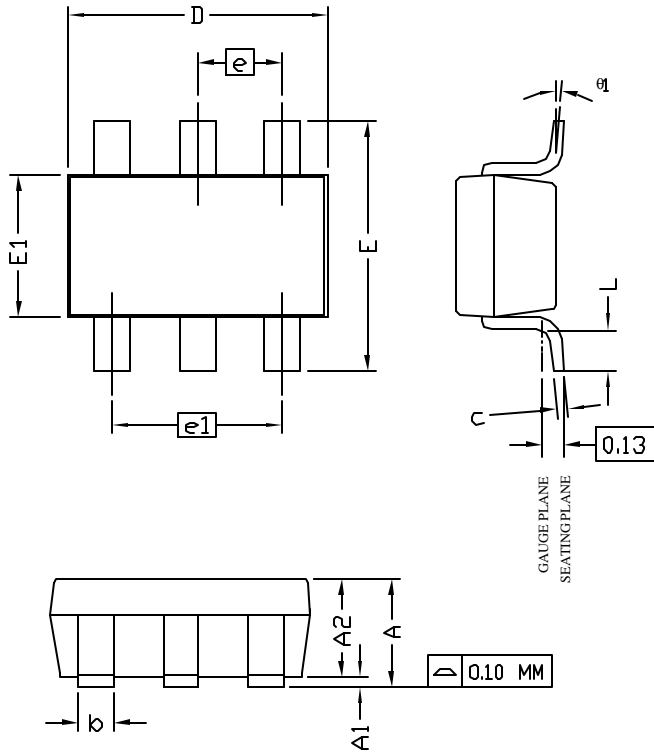


Figure 11: Normalized Maximum Transient Thermal Impedance



ALPHA & OMEGA
SEMICONDUCTOR, INC.

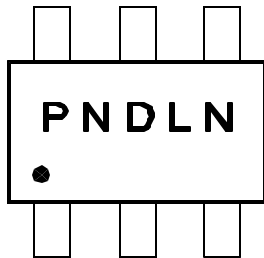
TSOP-6 Package Data



SYMBOLS	DIMENSIONS IN MILLIMETERS		
	MIN	NOM	MAX
A	1.00	—	1.25
A1	0.00	—	0.10
A2	1.00	1.10	1.15
b	0.35	0.40	0.50
c	0.10	0.13	0.20
D	2.70	2.90	3.10
E	2.60	2.80	3.00
E1	1.60	1.80	2.00
e	0.95 BSC		
e1	1.90 BSC		
L	0.37	—	—
$\theta1$	1°	5°	8°

- NOTE:
- LEAD FINISH: 150 MICRONS (3.8 μ m) MIN. THICKNESS OF Tin/Lead (SOLDER) PLATED ON LEAD
 - TOLERANCE ± 0.100 mm (4 mil) UNLESS OTHERWISE SPECIFIED
 - COPLANARITY : 0.1000 mm
 - DIMENSION L IS MEASURED IN GAGE PLANE

PACKAGE MARKING DESCRIPTION

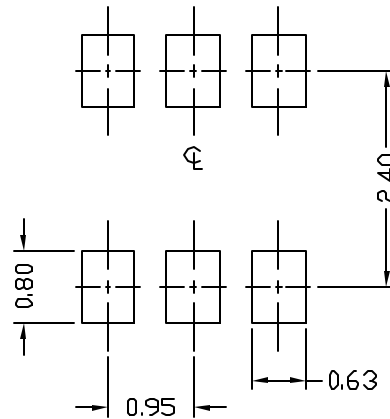


TSOP-6 PART NO. CODE

PART NO.	CODE
AO6405	D5

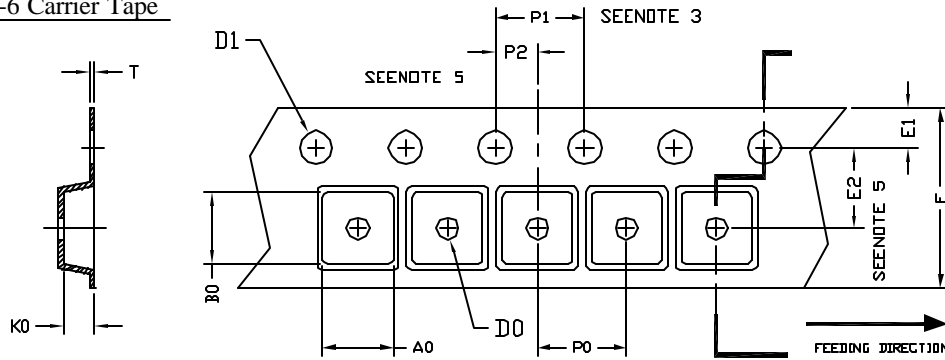
- NOTE:
- P N - PART NUMBER CODE.
 - D - YEAR AND WEEK CODE.
 - L N - ASSEMBLY LOT CODE, FAB AND ASSEMBLY LOCATION CODE.

RECOMMENDED LAND PATTERN





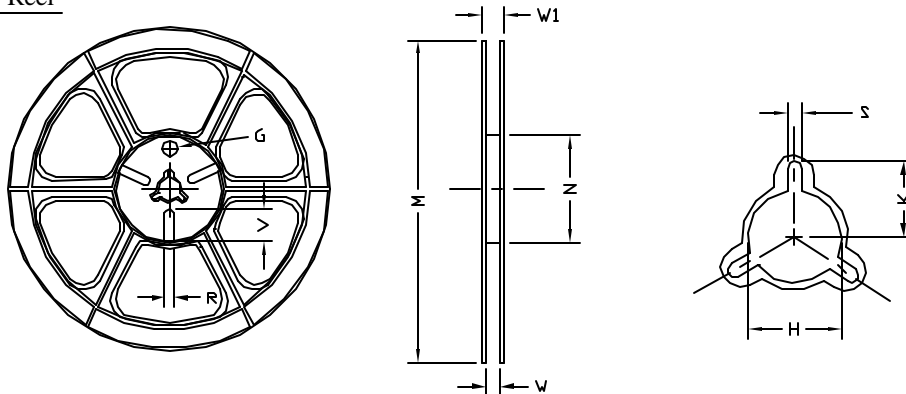
TSOP-6 Carrier Tape



UNIT: MM

PACKAGE	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SDT-23 (8 mm)	3.15 ±0.10	3.27 ±0.10	1.34 ±0.10	1.10 ±0.01	1.30 ±0.10	8.00 ±0.20	1.75 ±0.10	3.50 ±0.05	4.00 ±0.10	4.00 ±0.10	2.00 ±0.10	0.25 ±0.05

TSOP-6 Reel



UNIT: MM

TAPE SIZE	REEL SIZE	M	N	W	W1	H	K	S	G	R	V
8 mm	φ180	φ180.00 ±0.50	φ60.50	9.00 ±0.30	11.40 ±1.00	φ13.00 +0.50 -0.20	10.60	2.00 ±0.50	φ9.00	5.00	18.00

TSOP-6 Tape

Leader / Trailer
& Orientation

