



AOU402, AOU402L (Green Product)
N-Channel Enhancement Mode Field Effect Transistor

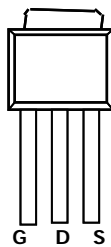
General Description

The AOU402 uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. This device is suitable for use in PWM, load switching and general purpose applications. AOU402L(Green Product) is offered in a lead-free package.

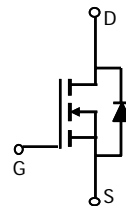
Features

- V_{DS} (V) = 60V
- I_D = 12 A
- $R_{DS(ON)} < 60 \text{ m}\Omega$ ($V_{GS} = 10\text{V}$)
- $R_{DS(ON)} < 85 \text{ m}\Omega$ ($V_{GS} = 4.5\text{V}$)

TO-251



Top View
Drain Connected to Tab



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	I_D	$T_C=25^\circ\text{C}$	A
		$T_C=100^\circ\text{C}$	
Pulsed Drain Current ^C	I_{DM}	30	
Avalanche Current ^C	I_{AR}	12	A
Repetitive avalanche energy $L=0.1\text{mH}$ ^C	E_{AR}	23	mJ
Power Dissipation ^B	P_D	$T_C=25^\circ\text{C}$	W
		$T_C=100^\circ\text{C}$	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	100	125	$^\circ\text{C/W}$
Maximum Junction-to-Case ^B	$R_{\theta JC}$	4	7.5	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =10mA, V _{GS} =0V	60			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =48V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} =±20V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1	2.4	3	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	30			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =12A T _J =125°C		47 85	60	mΩ
		V _{GS} =4.5V, I _D =6A		67	85	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =12A		14		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.74	1	V
I _S	Maximum Body-Diode Continuous Current				12	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =30V, f=1MHz		385	540	pF
C _{oss}	Output Capacitance			55		pF
C _{rss}	Reverse Transfer Capacitance			20		pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz		1.35	2	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =30V, I _D =12A		7.5	10	nC
Q _g (4.5V)	Total Gate Charge			3.8	5	nC
Q _{gs}	Gate Source Charge			1.2		nC
Q _{gd}	Gate Drain Charge			1.9		nC
t _{D(on)}	Turn-On DelayTime			4.2		ns
t _r	Turn-On Rise Time	V _{GS} =10V, V _{DS} =30V, R _L =2.5Ω, R _{GEN} =3Ω		3.4		ns
t _{D(off)}	Turn-Off DelayTime			16		ns
t _f	Turn-Off Fall Time			2		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =12A, di/dt=100A/μs		27.6	35	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =12A, di/dt=100A/μs		30		nC

- A: The value of R_{θJA} is measured with the device in a still air environment with T_A=25°C.
- B: The power dissipation P_D is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.
- C: Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175°C.
- D: The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.
- E: The static characteristics in Figures 1 to 6 are obtained using <300 μs pulses, duty cycle 0.5% max.
- F: These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C.
- G: The maximum current rating is limited by bond-wires.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

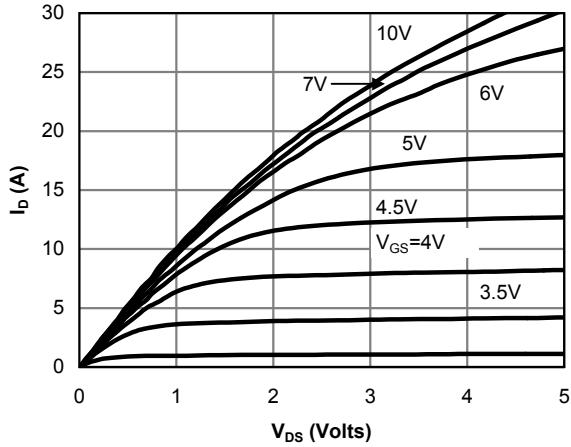


Fig 1: On-Region Characteristics

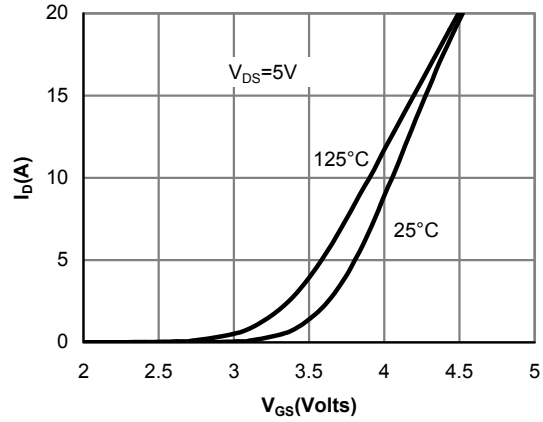


Figure 2: Transfer Characteristics

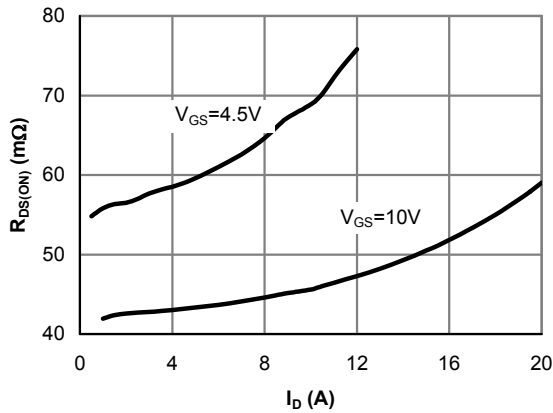


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

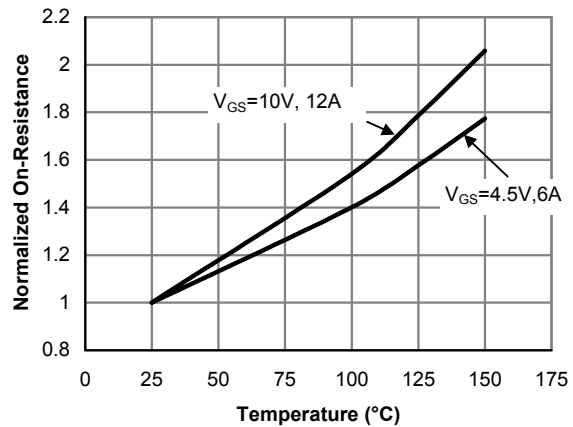


Figure 4: On-Resistance vs. Junction Temperature

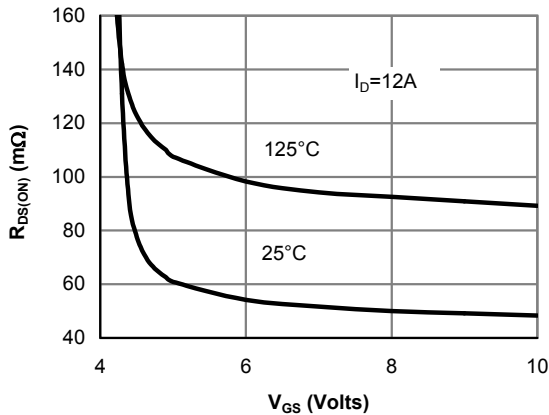


Figure 5: On-Resistance vs. Gate-Source Voltage

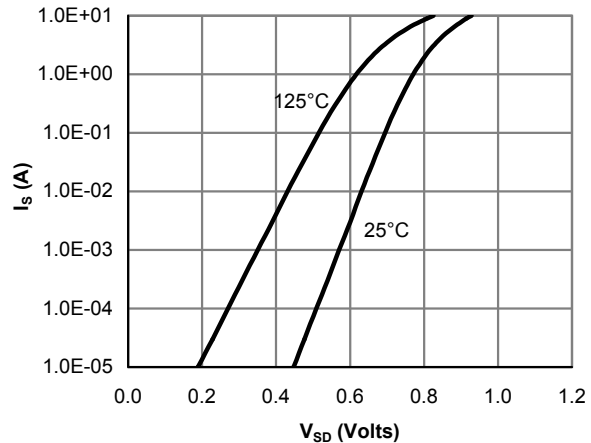


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

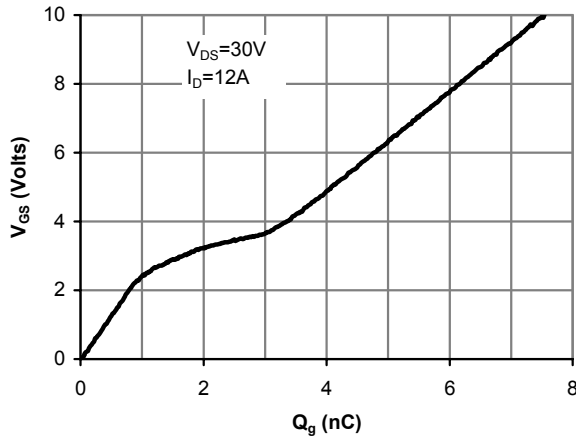


Figure 7: Gate-Charge Characteristics

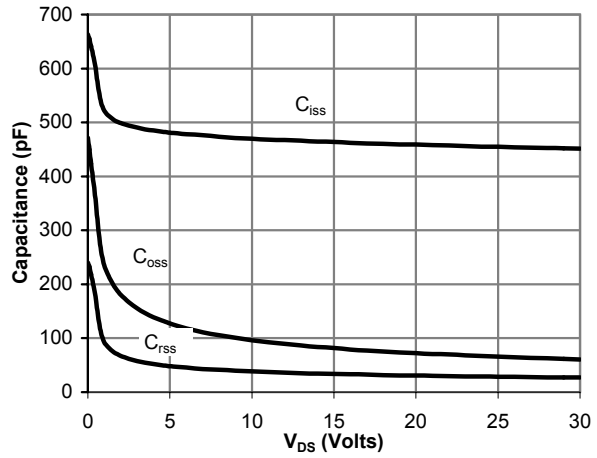


Figure 8: Capacitance Characteristics

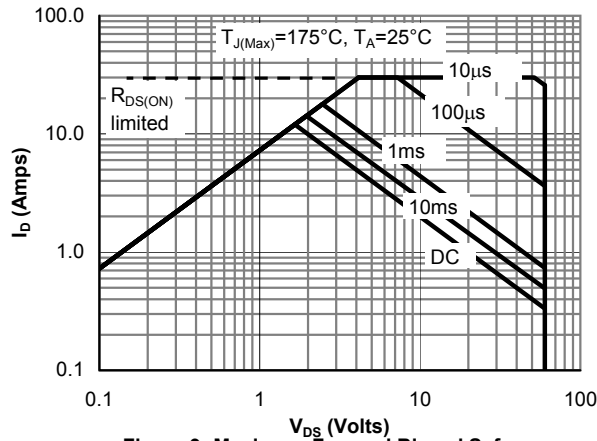


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

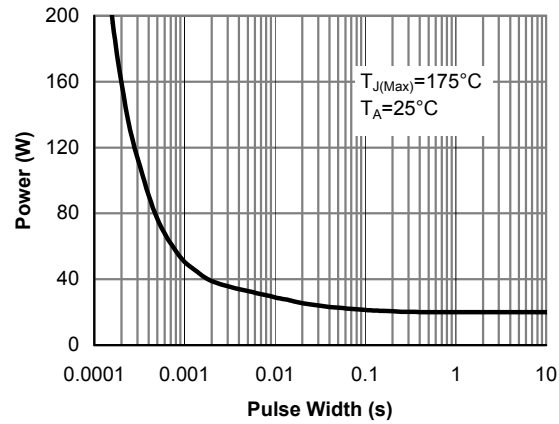


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

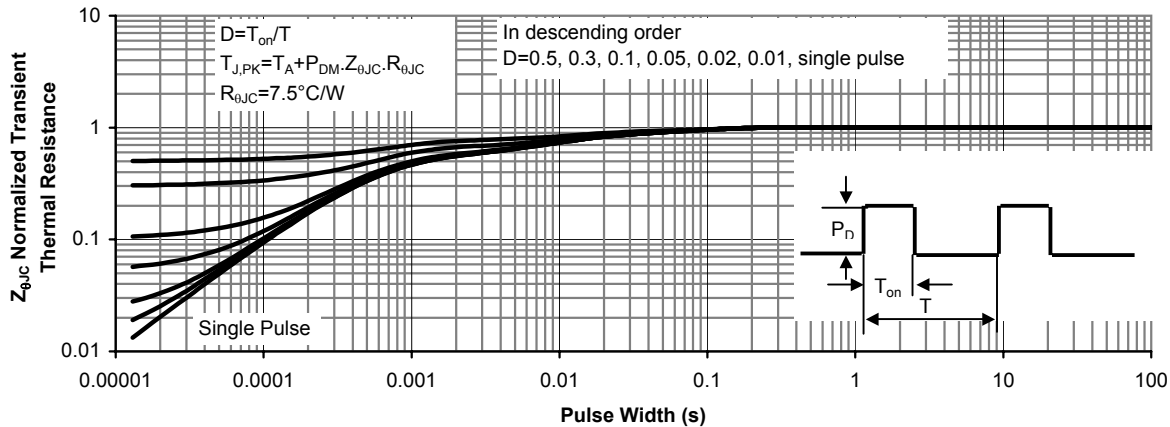


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

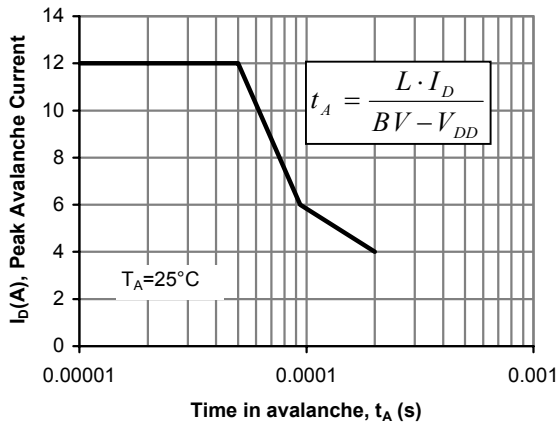


Figure 12: Single Pulse Avalanche capability

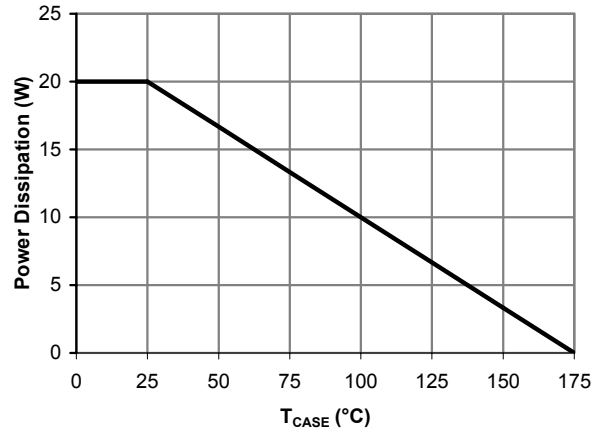


Figure 13: Power De-rating (Note B)

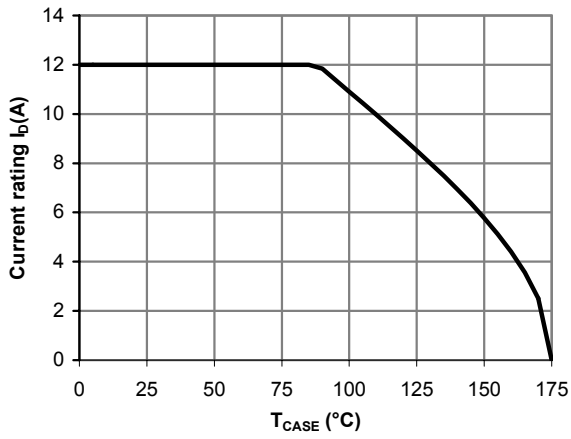
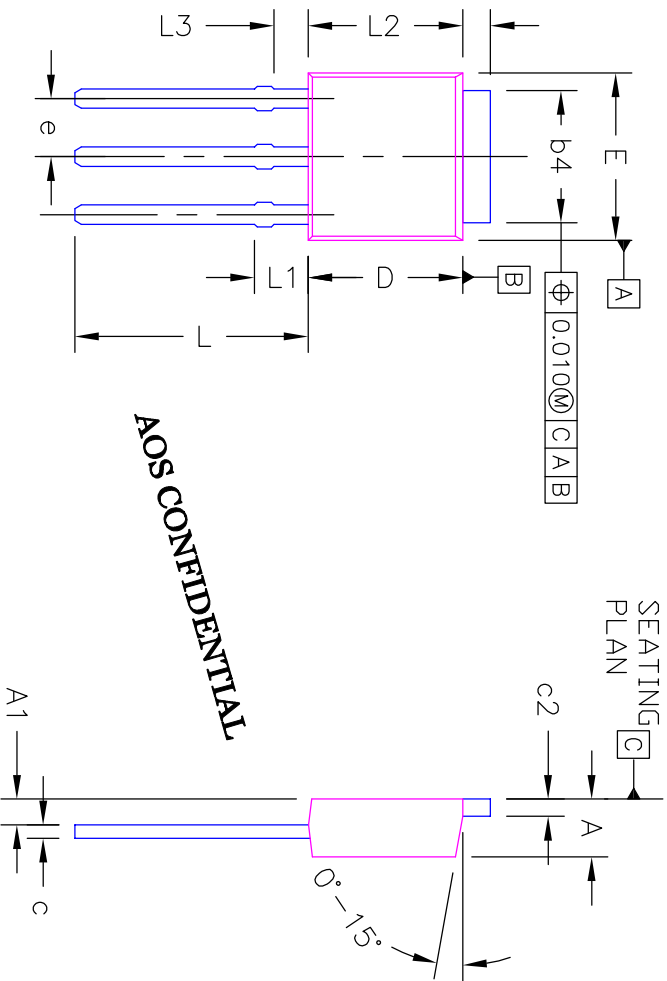
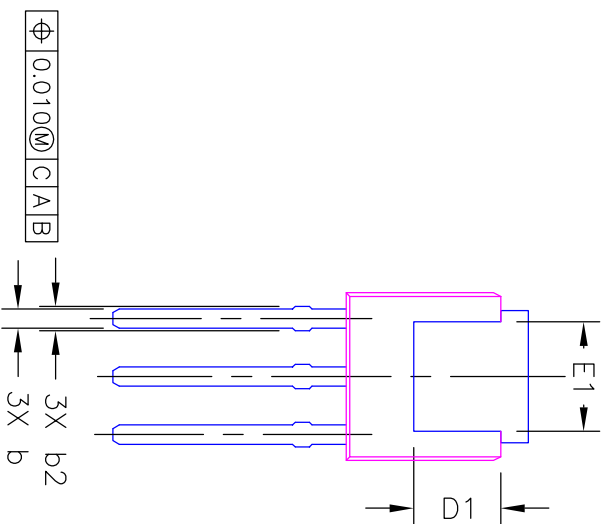


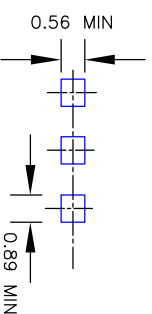
Figure 14: Current De-rating (Note B)



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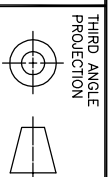
RECOMMENDATION OF HOLE PATTERN



UNIT: mm

- NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
 2. TOLERANCE 0.100 MILLIMETERS UNLESS OTHERWISE SPECIFIED.
 3. CONTROLLING DIMENSION IS MILLILITER, CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.
 4. REFER TO JEDEC TO-251D AA.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	2.24	2.29	2.39	0.088	0.090	0.094
A1	0.89	---	1.14	0.035	---	0.045
b	0.69	0.76	0.89	0.027	0.030	0.035
b2	0.89	---	1.14	0.035	---	0.045
b4	5.21	---	5.46	0.205	---	0.215
c	0.46	0.51	0.56	0.018	0.020	0.022
c2	0.48	---	0.58	0.019	---	0.023
D	5.97	6.10	6.22	0.235	0.240	0.245
D1	4.32	---	---	0.170	---	---
E	6.48	6.60	6.73	0.255	0.260	0.265
E1	4.32	---	5.33	0.170	---	0.210
e	2.29 BSC.			0.090 BSC.		
L	8.89	9.19	9.65	0.350	0.362	0.380
L1	1.91	2.11	2.29	0.075	0.083	0.090
L2	0.89	---	1.27	0.035	---	0.050
L3	1.14	1.35	1.52	0.045	0.053	0.060



Document No. PD-00016

Version rev B

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES

DECIMAL
xxx ±
xxxx ±

ANGULAR
±

INTERPRET DIM AND TOL PER ASME Y14.5M - 1994

PRINTING IS SCALED TO FIT DO NOT SCALE DRAWING

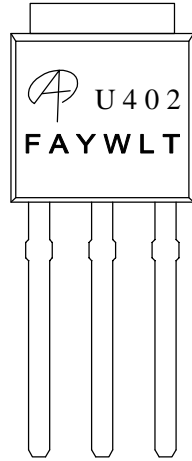
Title TO-251 PACKAGE OUTLINE



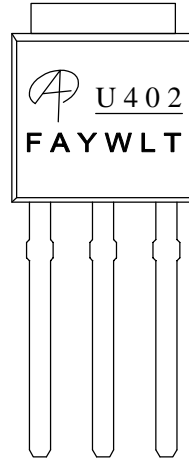
ALPHA & OMEGA
SEMICONDUCTOR, LTD.

Document No.	PD-00247
Version	rev B
Title	AOU402 Marking Description

DPAK(TO-251) PACKAGE MARKING DESCRIPTION



Standard product



Green product

NOTE:
LOGO - AOS LOGO
U402 - PART NUMBER CODE.
F&A - FOUNDRY AND ASSEMBLY LOCATION
Y - YEAR CODE
W - WEEK CODE.
L T - ASSEMBLY LOT CODE

PART NO.	DESCRIPTION	CODE
AOU402	Standard product	U402
AOU402L	Green product	<u>U402</u>