ANALOG DEVICES

AN-356
APPLICATION NOTE

ONE TECHNOLOGY WAY • P.O. BOX 9106 • NORWOOD, MASSACHUSETTS 02062-9106 • 617/329-4700

User's Guide to Applying and Measuring Operational Amplifier Specifications

by Ray Stata

SINCE THERE ARE NO established standards for operational amplifier specifications we shall discuss here the terms used by Analog Devices to define operational amplifier characteristics as well as the limitations which must be observed in applying the published data to actual circuits. Wherever possible we show the test circuits used to measure these parameters. Although these test circuits are applicable to a wide range of operational amplifiers, special amplifiers such as FET, chopper stabilized or ultra fast response amplifiers may require changes in the recommended circuit values or in some cases different test methods to measure their specifications. As a general rule the power supply for these measurements should have line and load regulation of about 0.1% and ripple should be no more than a few millivolts.

Figure 1 gives a simplified equivalent circuit for an operational amplifier showing many of the sources of error which are discussed in the text The specifications should be referenced to this diagram to predict their effect in a closed loop circuit. For a single ended amplifier you would assume that the plus or non-inverting input is grounded.

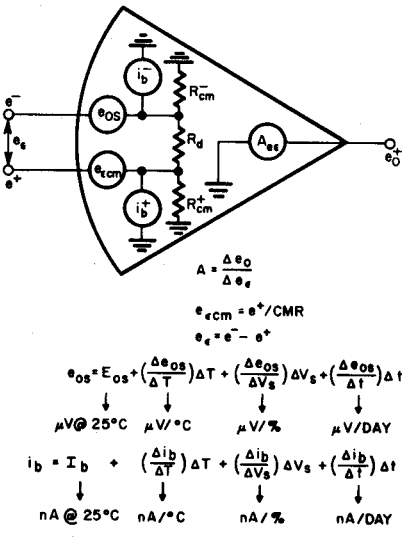


FIGURE 1. OPERATIONAL AMPLIFIER EQUIVALENT CIRCUIT

OPEN LOOP GAIN

Open loop gain, A, is defined as the ratio of output voltage to error voltage e_ϵ between inputs as shown in figure 1. Gain is usually specified only at DC (A_o), but in many applications such as AC amplifiers the frequency dependence of gain is also important. For this reason the typical open loop gain response is published for each amplifier. The open loop gain response of most amplifiers can be approximated by figure 2.

Reprinted from Analog Dialogue 1-3 1967

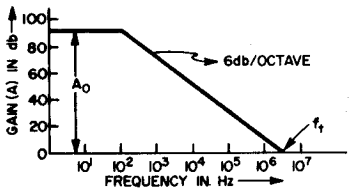


FIGURE 2. TYPICAL OPEN LOOP GAIN RESPONSE

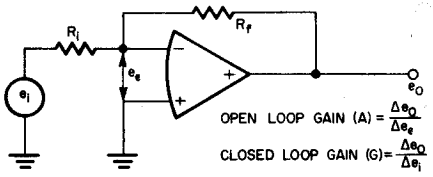


FIGURE 4. CLOSED LOOP CIRCUIT

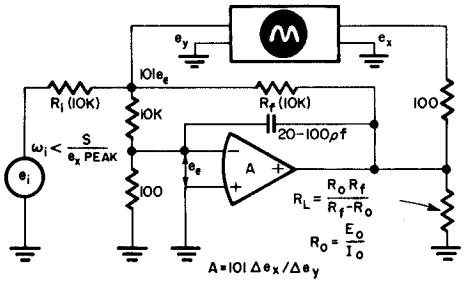


FIGURE 3. OPEN LOOP GAIN TEST CIRCUIT

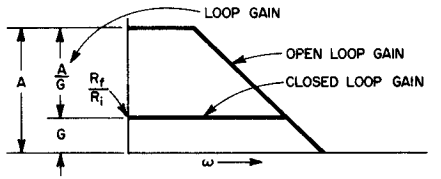


FIGURE 5. DETERMINATION OF LOOP GAIN

Open loop gain changes with load impedance (R_L), ambient temperature and supply voltage. As a rule, open loop gain will not change more than a factor of 10 between rated load and no load conditions. Most operational amplifiers have a positive gain temperature coefficient of about 0.5 to 1%/°C and gain changes with supply voltage at about 2%/%. Analog Devices specifies all open loop gains at rated load, 25°C and rated supply voltages.

A practical circuit for measuring open loop gain over a range of frequencies is shown in figure 3. The voltage divider on the negative input boosts the sensitivity of the error voltage by 100 times which makes it possible to measure gains up to one million. At low frequencies open loop gain is constant so that DC gain can be measured by a low frequency signal (about 5Hz). The voltage divider may not be necessary for low gain amplifiers (below 20,000) and it is not recommended for measuring gain at high frequencies where open loop gain is less.

At very best, noise pick up is a problem for measuring high gains and care must be taken to adequately shield the test circuit. At high frequencies the amplitude of the output voltage must be reduced to avoid exceeding the slewing rate of the amplifier. For this reason the output voltage should be adjusted, so that $e_x(\text{peak}) < \text{slew rate}/\omega_i$, where ω_i is the test frequency.

SIGNIFICANCE OF OPEN LOOP GAIN

Operational amplifiers are rarely used open loop. Instead negative feedback is used around the amplifier to improve the accuracy of the circuit. This introduces a second term, closed loop gain (G), which is defined as the gain of the circuit with feedback. The simple inverting amplifier in Figure 4 illustrates this point.

Linearity, gain stability, output impedance and gain accuracy are all improved by the amount of feedback. Figure 5 graphically illustrates the relation between open loop gain and closed loop gain.

The excess of open loop gain over closed loop gain is called loop gain. (Subtraction of dB is equivalent to arithmetic division.) The improvement of open loop performance due to feedback is directly proportional to loop gain. As a general rule for moderate accuracy, open loop gain should be 100 times greater than the closed loop gain at the frequency, or frequencies, of interest (that is loop gain = 100). For higher accuracy, loop gain should be 1000 or more. To illustrate, we recall that open loop gain stability for most operational amplifiers is about 1%/°C. With loop gain of 100, closed loop gain stability would be 100 times better or 0.01%/°C. Likewise, closed loop output impedance would be 100 times less than open loop output impedance with a loop gain of 100.

RATED OUTPUT VOLTAGE AND CURRENT

Rated output voltage, E_o, is the maximum peak output voltage which can be obtained at rated output current before clipping or excessive non-linearity occurs. This measurement is made at rated power supply voltage; at other supply voltages the output will swing to within about 4 volts of the supply voltage. Also the output voltage swing will increase somewhat at lower load current. Rated output current, I_o, is the minimum guaranteed value of current at the rated output voltage. Load impedance less than E_o/I_o can be used but E_o will decrease, distortion may increase and open loop gain will be reduced. Driving large capacitance loads at high frequencies will present a low load impedance which may then exceed the rated output current. Any convenient circuit such as figure 3 or figure 6 can be used to measure E_o and I_o.

UNITY GAIN SMALL SIGNAL RESPONSE

Unity gain small signal response, f_t, is the frequency at which the open loop gain becomes unity or zero dB (see figure 2). "Small signal" indicates that in general it is not possible to obtain large output voltage swing at high frequencies because of distortion due to slew rate limiting. Therefore in both measuring f_t and using the amplifier at high frequencies, the output voltage swing must be restricted to avoid slew rate limiting. This implies that the peak output voltage, e_o, for a sinusoidal signal at the unity gain frequency, f_t, must be less than $S/2\pi f_t$, where S is the slew rate.

For amplifiers with symmetrical response on each input, f_t may be measured by either the inverting circuit of figure 6 or the non-inverting circuit of the figure 7. Some units such as chopper stabilized amplifiers or wideband amplifiers with feed forward design have fast response only on the negative input which restricts testing and use to the inverting circuit. Remember that the closed loop unity gain response of figure 6 will be about one half the open loop unity gain response due to the loading of the feedback network. Moreover, large values of feedback resistance when coupled with stray capacitance may reduce the closed loop response and therefore the smallest possible value of R_f should be used, the limit being set by output current capability I_o.

Sometimes f_t is called unity gain-bandwidth product which implies that open loop gain at other frequencies can be predicted from this number. However, gain bandwidth product is constant only for amplifiers with 6dB/octave roll off! For fast roll off amplifiers, gain bandwidth product increases with gain and thus we publish the open loop response curve to give typical gain at each frequency.

FULL POWER RESPONSE

The large signal and small signal response characteristics of operational amplifiers differ substantially due to dynamic nonlinearities or transient saturation. An amplifier will not respond to large signal changes as fast as the small signal bandwidth characteristics would predict. The most prominent contributor to large signal response limitations is slew rate limiting in the output stages. Circuit and transistor capacitances can be charged and discharged only so fast due to the limited dynamic range of the driving circuits. Transient saturation can also occur in the input stages of the amplifier due to overloading the input stage or due to common mode voltage slew rate limiting, but this is rarely a problem as compared to saturation of the output stages.

Full power response, f_p, is the maximum frequency measured at unity closed loop gain, for which rated output voltage, $\pm E_o$, can be obtained for a sinusoidal signal at rated load without distortion due to slew rate limiting. Note that this specification does not relate to "response" in the sense of gain reduction with frequency. Instead it refers only to distortion in the output signal caused by slew rate limiting. For a sinusoidal signal, the maximum slope or rate of voltage change occurs at zero crossing and is proportional to the peak amplitude and the frequency.

Thus we see that to a first approximation slew rate, S, and full power response, f_p, are related by equation 1.

$$\left.\frac{de_o}{dt}\right|_{max} = 2\pi f_p E_o = S \qquad \text{(equation 1)}$$

As the voltage swing is reduced below rated output, E_o, the operating frequency can be proportionally increased without exceeding the slew rate, S. In the limit the operating frequency approaches the unity gain bandwidth, f_t, and the corresponding voltage signal defines the maximum peak amplitude for "small signal" unity gain response. The circuits of figure 6 or figure 7 can be used to measure full power response depending on whether inverting or non-inverting parameters are measured. Where dynamic saturation of the output stages is the primary cause for slew rate limiting either test circuit will give equivalent results. For very fast response amplifiers, load capacitance and/or capacitance from the output to the negative input will cause apparent slew rate limiting and consequent degradation of full power response. This is due to saturation of amplifier output current in charging these capacitances and therefore such capacitances must be low.

Output distortion can be measured either by a distortion meter on the output or by observing a Lissajon pattern on an oscilloscope. There is no industry wide accepted value for the distortion level which determines the full power response limitation, but a number like 1% to 3% is a reasonable figure. One subtle point here is that closed loop output distortion depends on the amount of feedback or loop gain and therefore it depends on the closed loop gain of the measurement. Full power response is generally measured at unity gain where loop gain is the highest. At higher closed loop gains output distortion will increase for the same full power response frequency.

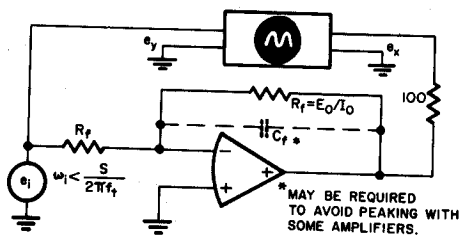


FIGURE 6. INVERTING CIRCUIT FOR MEASURING f_t, f_p, S, T

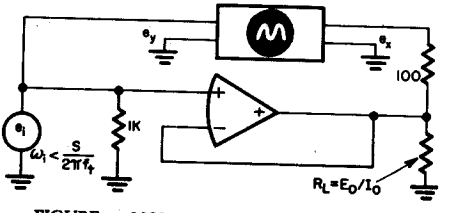


FIGURE 7. NONINVERTING CIRCUIT FOR MEASURING f_t, f_p, S, T, E_{cm}

In many applications the additional distortion which is caused by exceeding the full power response can be comfortably ignored. However, a far more serious effect, often overlooked, is that a DC offset voltage can be generated when the full power response is exceeded due to rectification of the unsymmetrical feedback waveform or due to overloading the input stage with large distortion signals at the summing junction.

These more subtle points in measuring full power response as well as the attendant side effects suggest the circuit of figure 8 as more satisfactory test circuit. By viewing the error voltage at the summing junction on an oscilloscope, distortion signals are more easily detected, signal generator distortion is eliminated from the measurement and frequency dependent DC offset can be readily observed.

SLEWING RATE

The origins of slewing rate limitations were discussed in the previous section. Slewing rate, S, usually expressed in volts/μsec defines the maximum rate of change of output voltage for a large step change.

Equation 1 suggests a convenient method to measure slewing rate by first measuring full power response, f_p, and then calculating S. Although this test method yields usable results for most amplifiers in most applications, the relationship of equation 1 does not apply under all conditions. First, slewing rate is a non-linear function of output voltage and equation 1 measures slewing rate only at zero volts output. This second order effect can usually be safely ignored in most applications. However, for certain amplifiers, particularly fast response types, the slew rate may be higher than that predictable from f_p. In these cases f_p is limited by factors other than slew rate such as DC offset errors which are generated by the rectification of large high frequency error voltages.

A more direct method to measure slewing rate is to apply low frequency square waves (about 100Hz) to the input of figure 6 or figure 7 which cause full voltage swing at the output and to observe the rise time from 10 to 90% on an oscilloscope (see figure 9). Small feedback resistors must be used to avoid degradation of slewing rate due to stray capacitance.

In applying operational amplifiers remember that repetitive input waveforms whose rise time exceeds the amplifier's slewing rate will generate voltage spikes at the summing junction. These spikes are usually unsymmetrical and are also usually clipped unsymmetrically by the input circuit of the amplifier — either or both of which effects will cause DC offsets at the output.

OVERLOAD RECOVERY

Overload recovery, τ, defines the time required for the output voltage to recover to the rated output voltage E_o from a saturated condition. For this test the circuit of figure 6 or 7 is used with an input square wave adjusted to be 50% greater than the voltage required to saturate the amplifier output. The square wave frequency should be adjusted to about 100Hz and the input-output signals should be compared on a dual trace oscilloscope as illustrated in figure 9.

In some amplifiers the overload recovery will increase for large impedances (greater than 50KΩ) in the input circuit, either the summing impedance for figure 6 or the source input for figure 7. Published specifications apply for low impedances and assume that overload recovery is not degraded by stray capacitance in the feedback network.

Normally, overloaded recovery time runs about one millisecond. For the inverting configuration an external clamp circuit can be added to improve overload recovery as illustrated in figure 10. This circuit prevents the output from saturating and therefore circumvents any delays due to overload recovery. The only constraint for proper operation is that input current (e_i/R_i) shall be approximately less than the rated output current I_o minus the load current. The clamp circuit cannot be used with the non-inverting and differential configurations.

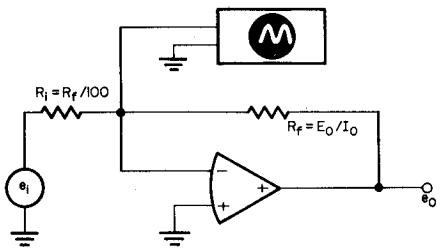


FIGURE 8. MEASURING FULL POWER RESPONSE

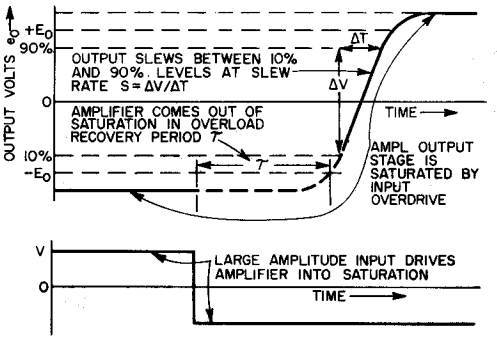


FIGURE 9. OVERLOAD RECOVERY AND SLEW RATE ILLUSTRATION

INITIAL OFFSET VOLTAGE

Offset voltage, e_{os}, is defined as the voltage required at the input from a zero source impedance to zero the output, at any temperature, supply voltage and time (see figure 1). Initial offset voltage, E_{os}, defines the offset voltage at 25°C and rated supply voltages. In most amplifiers, provisions are made to adjust initial offset to zero with an external trim potentiometer. Some amplifiers are internally trimmed to guarantee some maximum limit on initial offset (usually ±1mV) which means that in certain applications the external trim pot can be eliminated. On special order any amplifier from Analog Devices can be internally trimmed to ±1mV initial offset or less. Initial offset can be measured with the circuit of figure 11, where an appropriate fixed resistor is substituted for the external trim potentiometer. There is a warm up drift of offset voltage following the application of power supply voltage and it is recommended that you let the amplifier stabilize for at least 15 minutes before making measurements.

INITIAL BIAS CURRENT

Bias current, i_b, is defined as the current, at any temperature, supply voltage and time, required at either input from an infinite source impedance to zero the output assuming zero common mode voltage. For differential amplifiers bias current is designated by i_b- for the negative input and by i_b+ for the positive input. For single ended amplifiers, like chopper stabilized units, bias current refers to the current at the negative input only.

Initial bias current, I_b, is the bias current at either input measured at 25°C, rated supply voltages and zero common mode voltage. The designation (0,+) or (0,−) indicates that no internal compensation is used to reduce initial bias current so that the polarity is always known. The sign tells to which power supply voltage an external compensating resistor should be connected to zero the initial bias current. The designation (±) indicates that internal compensation has been used to reduce initial bias current and that the residual bias current can be of either polarity. In general compensating initial bias current has little effect on the bias current temperature coefficient. The circuit of figure 11 is used to measure initial bias current.

INITIAL DIFFERENCE CURRENT

Difference current*, i_d, is defined as the difference between the bias currents at each input from an infinite source required to zero the output assuming zero common mode voltage. The input circuitry of differential amplifiers is generally symmetrical so that bias current at each tends to be equal and tends to track with changes in temperature and supply voltage. Usually difference current is 3 to 5 times less than bias current at either input, assuming that initial bias current is not compensated. If the impedance as seen from each input terminal to ground is balanced then offset and drift errors are proportional to difference current rather than to bias current. In most applications, if the external impedances at each input are balanced then there is no particular advantage in using an amplifier where initial bias current is internally compensated. Initial difference current, I_d, the difference current measured at 25°C and rated supply voltage, can be measured by the circuit of figure 11.

*Previously called offset current.

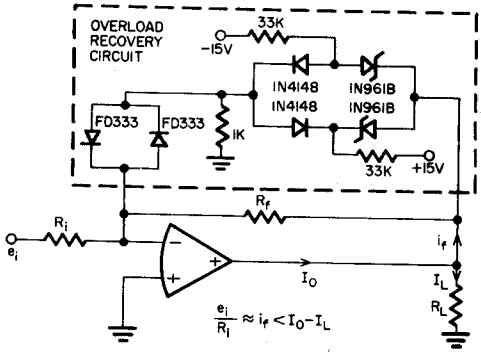


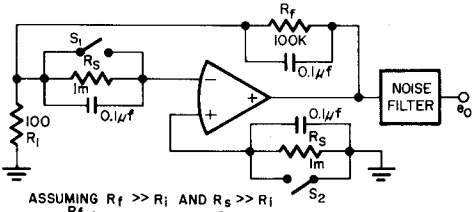
FIGURE 10. EXTERNAL CLAMP CIRCUIT FOR ±10 VOLTS

TEMPERATURE DRIFT

Offset voltage, bias current and difference current all change or "drift" from their initial values with temperature. By far this is the most important source of error in most applications. The temperature coefficients of these parameters, $\triangle e_{os}/\triangle T$, $\triangle i_b/\triangle T$ and $\triangle i_d/\triangle T$ are all defined as the average slope over a specified temperature range and are determined by subtracting the offset values at the end points of the temperature range and dividing by the temperature change. In general drift is a non-linear function of temperature and the slopes are greater at the extremes of temperature than around normal room ambient. The temperature drift coefficients are measured by the circuit of figure 11. The amplifier is used to boost its own low level input offset signal to a conveniently measurable voltage at the output. Gain is established by the ratio of R_f/R_i. The current sampling resistors, R_s, must be selected so that voltage drift is small compared to the drift due to difference current; that is $R_s \times \triangle i_d/\triangle T >> \triangle e_{os}/\triangle T$. Alternatively, voltage drift must be subtracted from the data for current drift.

One problem in using published voltage drift specifications is that this data applies only to static temperature conditions where the temperature of the module is assumed to be uniform. Voltage offset of most differential amplifiers is quite sensitive to thermal gradients, since drift performance depends on the cancellation of large offset in each transistor of the input differential pair. Therefore in environments where thermal gradients are present voltage offset may exceed that predictable from the drift coefficients. In this case where low drift over a narrow temperature range is critical, it is good practice to insulate or shield the amplifier to assure a uniform temperature. Bias current is not noticeably affected by thermal gradients and difference current, while affected, is far less sensitive to gradients than voltage offset.

Bias current and difference current for FET and varactor bridge amplifiers double each 10°C and therefore a linearized drift coefficient has little meaning except over a narrow operating temperature range.



ASSUMING $R_f >> R_i$ AND $R_S >> R_i$

$$e_o = -\frac{R_f}{R_i}[e_{os} \pm R_s(i_b^- - i_b^+)]$$

$$i_d = i_b^- - i_b^+$$

Parameter	Switch Position S1	Switch Position S2	Output Voltage
e_{os}	Closed	Closed	$e_o = -(\frac{R_f}{R_i})e_{os}$
i_b^-	Open	Closed	$e_o = -(\frac{R_f}{R_i})R_s i_b^-$
i_b^+	Closed	Open	$e_o = -(\frac{R_f}{R_i})R_s i_b^+$
i_d	Open	Open	$e_o = -(\frac{R_f}{R_i})R_s i_d$

FIGURE 11. TEST CIRCUIT FOR OFFSET VOLTAGE, BIAS CURRENT AND DIFFERENCE CURRENT

SUPPLY VOLTAGE SENSITIVITY

Offset voltage, bias current and difference current will also change when supply voltage is varied. Usually errors due to this effect are negligible compared to temperature drift. Static or DC supply voltage coefficients, $\triangle e_{os}/\triangle V_s$, $\triangle i_b/\triangle V_s$, $\triangle i_d/\triangle V_s$ are measured with the circuit in figure 11 by varying supply voltages individually by ± 1 volt.

There is a common misconception that tracking power supplies whose plus and minus voltages change by the same amounts will improve supply voltage coupling. In general tracking supplies are of no benefit since the positive supply voltage coefficient is usually much larger than the negative supply voltage coefficient. Rejection of AC noise and ripple on the power supplies is not as good as static or DC rejection, but for almost all amplifiers AC rejection will be better than 1mV/V or 60dB over a wide range of frequencies.

DRIFT VS TIME

Offset voltage, bias current and difference current change with time as components age. Static data over long time periods is difficult to obtain because of the inherent time delays involved. But it is safe to say that the published time drift for amplifiers does not accumulate linearly. For example, voltage drift for a chopper stabilized amplifier (which by the way is by far the best amplifier type for long term stability) is usually quoted as $1\mu V$/day whereas cumulative drift over 30 days will usually not exceed $5\mu V$ nor $15\mu V$ in a year.

Long term voltage drift in differential input type amplifiers depends primarily on the aging of collector resistors in the input differential pair. The aging coefficient referred to the input is about $300\mu V/\%$ change of collector resistance. It is not unlikely that carbon composition resistors will age by 1 or 2% over a year resulting in an offset voltage change of 300 to $600\mu V$. The use of metal film resistors for the collector resistors will greatly improve long term stability to the point where base to emitter voltage aging is the determining factor. With metal film resistors, offset voltage for transistor amplifiers is about $100\mu V$/year while FET amplifiers will age somewhat more.

Long term bias current stability in differential input amplifiers again depends on resistor stability when internal initial current compensation is employed. In this case, multi-megohm carbon composition resistors are used (since large value metal film resistors are not available) to supply about 90% of the base bias current. If these resistors change by 1%, the specified initial bias current will change by about 9% which can be a substantial drift. Therefore one can conclude that amplifiers without internal initial current compensation will exhibit more stable bias current. Under these conditions long term bias current stability depends primarily on the stability of the transistor or FET devices which may be better than 1%.

INPUT IMPEDANCE

Differential input impedance, R_d, is defined as the impedance between the two input terminals, measured at 25°C, assuming that the error voltage, e_ε, is nulled or very near zero volts (see figure 1). For a single ended amplifier, R_d, is the input impedance since the plus input is grounded. To a first approximation, dynamic impedance can be represented by a capacitor, C_d, in parallel with R_d.

Differential input impedance is among the most difficult parameters to measure particularly for a high gain, high impedance type amplifier. In general this measurement can only be made under laboratory conditions by an experienced engineer with special fixtures to shield against noise pick up. For this reason most companies including Analog Devices rarely measure this parameter on a production line basis. Fortunately a precise knowledge of R_d is not required, since for most circuits, so long as R_d is large compared to the external feedback impedance, its value has little bearing on closed loop performance.

The circuits of figure 12 show in principle how R_d can be measured with enough attention to reducing noise. These circuits actually measure R_d in parallel with the negative input common mode impedance. However, common mode impedance is usually 10 to 100 times greater than R_d so that the error is negligible.

Common mode impedance, R_{cm}, is defined as the impedance between each input and ground or power supply common and is specified at 25°C. (See figure 1.) For most circuits common mode impedance on the negative input, R_{cm}^-, has little significance except for the capacitance which it adds to the summing junction. However, common mode impedance on the plus input, R_{cm}^+, sets the upper limit on closed loop input impedance for the non-inverting configuration. Dynamic impedance can be represented by a capacitor, C_{cm}, in parallel with R_{cm} which usually runs from 5 to 25 pf on the plus input.

The circuit of figure 13 can be used to measure R_{cm}^+ up to about 500M ohms. Use an oscillator frequency of 1 to 5Hz

and adjust R_s for 10% reduction at the output. Then $R_{cm}+ = 9R_s$. Above this impedance it is advisable to substitute a picoameter for the resistor R_s and to measure DC bias current as a function of common mode voltage.

Common mode impedance is a non-linear function of both temperature and common mode voltage. For FET amplifiers common mode impedance is reduced by a factor of two for each 10°C temperature rise.

As a function of common mode voltage, R_{cm} is defined as average impedance for a common mode voltage change from zero to $\pm E_{cm}$, that is, maximum common mode voltage. Incremental R_{cm} about some large common mode voltage may be considerably less than the specified average R_{cm}, especially for FET input amplifiers.

MAXIMUM VOLTAGE BETWEEN INPUTS

Under most operating conditions, feedback maintains the error voltage, e_ε, between inputs very near to zero volts. However, in some applications, such as voltage comparators, or where the input voltage exceeds the level required to saturate the output, the voltage between inputs can become large. E_d defines the maximum voltage which can be applied between inputs without causing permanent damage to the amplifier. Placing parallel back to back diodes across the input terminals is one way to provide added protection for the amplifier.

MAXIMUM COMMON MODE VOLTAGE

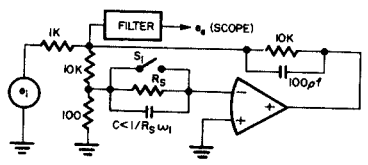
For differential input amplifiers, the voltage at both inputs can be raised above ground potential. Common mode voltage, e_{cm}, is defined as the voltage above ground at each input when both inputs are at the same voltage. E_{cm} is defined as the maximum peak common mode voltage at the input before clipping or excessive non-linearity is seen at the output. E_{cm} establishes the maximum input voltage for the voltage follower connection. (See figure 7.)

E_{cm} is measured with the circuit of figure 7 by increasing the peak input voltage (sinusoidal waveform) until distortion is seen on the scope (about 1 to 3%). The input signal frequency must be well below the full power response frequency, f_p, for the non-inverting input.

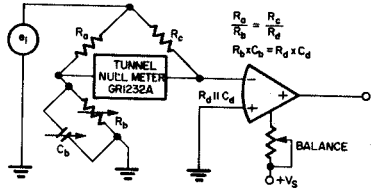
COMMON MODE REJECTION

An ideal operational amplifier responds only to the difference voltage between inputs ($e+ - e-$) and produces no output for a common mode voltage — that is when both inputs are at the same potential. However, due to slightly different gains between the plus and minus inputs, common mode input voltages are not entirely substracted at the output. If we refer the output common mode error voltage to the input (dividing by gain) and call this the input common mode error voltage, $e_{\varepsilon_{cm}}$, then common mode rejection (CMR) is defined as the ratio of common mode voltage to common mode error voltage. That is $CMR = e_{cm}/e_{\varepsilon_{cm}}$. CMR is sometimes expressed in dB in which case you take 20 times the log (base 10) of the ratio. Errors due to common mode rejection can be represented in the equivalent circuit of figure 1 by a voltage generator, $e_{\varepsilon_{cm}}$, in series with the input. Note that common mode error goes to zero when either input is grounded. Therefore the inverting configuration does not exhibit a common mode error since the plus input is grounded. Thus CMR is only a problem in the non-inverting and differential configurations where common mode voltage varies in direct proportion to the input signal. In this case $e_{\varepsilon_{cm}}$ is a basic measuring error which affects the overall circuit accuracy.

For example, if a 10 volt signal, e_i, were applied to the input of the circuit in Figure 14 common mode voltage, e_{cm}, is equal to the input voltage, e_i. This would cause a common mode voltage, $e_{\varepsilon_{cm}}$, of 2mV for an amplifier with 5,000 or 74dB CMR and thus a 0.02% measuring error.



SET e_i FOR 1 TO 5 Hz, INCREASE R_s UNTIL OPENING S_1 INCREASE e_o BY FACTOR OF 2. THEN $R_s = R_d$



BALANCE DC OUTPUT REDUCE e_i TO SMALLEST POSSIBLE VOLTAGE AND FREQUENCY

FIGURE 12. DIFFERENTIAL IMPEDANCE TEST CIRCUITS

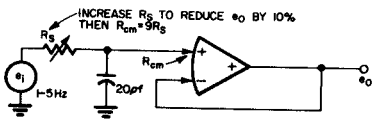


FIGURE 13. COMMON MODE IMPEDANCE TEST CIRCUIT

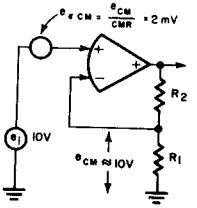


FIGURE 14. ILLUSTRATION OF COMMON MODE VOLTAGE

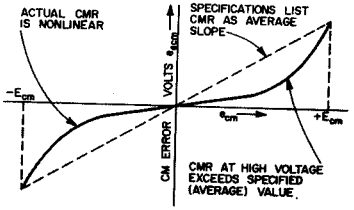


FIGURE 15. CM ERROR VS CM VOLTAGE

Precisely specifying CMR is complicated by the fact that common voltage error, $e_{\varepsilon_{cm}}$, can be a highly non-linear function of common mode voltage and it also varies with temperature. This is particularly true for FET input amplifiers. As illustrated by figure 15, CMR published by Analog Devices are average figures assuming an end point measurement at maximum common mode voltage, $\pm E_{cm}$. But the incremental CMR about some large common mode voltage may be less than the average CMR which is specified. In fact, if common mode error were a linear function of common mode voltage and if CMR were not strongly influenced by temperature then this source of error would be of little consequence. This follows since a linear CMR error can be viewed as a gain error which could be compensated for by adjusting the closed loop gain. Therefore linearity of common mode error, $e_{\varepsilon_{cm}}$, vs common mode voltage is actually more important for many applications than CMR itself.

The circuit in figure 16 provides a unique method to instrument CMR measurements as well as to measure the non-linearity of common mode errors. The oscilloscope display will duplicate the pattern of figure 15. A floated power supply allows a single ended oscilloscope to be used and almost any regulated power supply has floated outputs with sufficient isolation. Published CMR specifications apply only to DC input signals so that this measurement should be made with a signal frequency of 5Hz or less. CMR at higher frequencies, although not guaranteed by the specifications, can also be measured with this circuit. It is further assumed that the external circuit impedances of both the test circuit and the application are small compared to the common mode impedance to avoid additional common mode errors due to impedance unbalance.

INPUT NOISE

Input voltage and current noise characteristics can be in principle measured, specified and analyzed very much like offset voltage and bias current characteristics. In fact, offset voltage and bias current drift can be considered noise which occurs at very low frequencies. For this purpose in both the equivalent circuit of figure 1 and the test circuit of figure 11, replace e_{os} by e_n, an equivalent voltage noise generator, and replace i_b^- and i_b^+ by i_N^- and i_N^+, equivalent current noise generators. The primary difference in measuring and specifying noise as opposed to DC drift is that bandwidth must be considered. At low frequencies, 100Hz or less, 1/f noise prevails which means that the noise per root cycle increases inversely with frequency. At the mid band frequencies noise per root cycle is constant or "white."

To measure noise a sharp cut off bandpass filter is added to the output of the circuit of figure 11. Furthermore the impedance, gain and capacitors must be adjusted to assure that neither the amplifier nor the external feedback components limit the noise bandwidth of the measurement. For very low current noise, it becomes very difficult to make wideband measurements because of the interaction of stray capacitance and the large sampling resistor values needed to boost sensitivity.

Usually two noise measurements are taken. Low frequency noise in a bandpass of .01 to 1Hz is measured on a strip chart recorder and is specified as peak to peak with a 3σ uncertainty, meaning that 99% of the observed peak to peak exclusions will fall within the specified limits. Wideband noise in a bandpass of 5Hz to 50kHz is measured on a VTVM, preferably a true RMS type, and is specified as rms. Of course, shielding becomes very critical in these measurements to avoid power line frequency and radio frequency pick up.

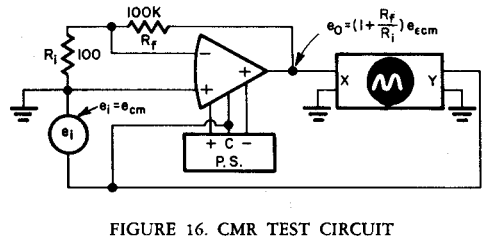


FIGURE 16. CMR TEST CIRCUIT