A DESIGNER'S GUIDE TO INSTRUMENTATION AMPLIFIERS

by
Charles Kitchin and Lew Counts

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BIBLIOGRAPHY/FURTHER READING

Jung, Walter. "IC Op-Amp Cookbook," 3rd edition. Howard W. Sams & Co., 1986. ISBN# 0-672-22453-4.

Kester, Walt. "Practical Design Techniques for Sensor Signal Conditioning," Analog Devices, Inc., 1999 Section 10. ISBN-0-916550-20-6

Brokaw, Paul. "An I.C. Amplifier Users' Guide to Decoupling, Grounding, and Making Things Go Right for a Change." Application Note AN-202, Analog Devices, 1990.

Wurcer, Scott; Jung, Walt. "Instrumentation Amplifiers Solve Unusual Design Problems," Application Note AN-245, Applications Reference Manual, Analog Devices.

Sheingold, Dan, ed. "Transducer Interface Handbook." Analog Devices, 1980, pp. 28-30.

Nash, Eamon. "Errors and Error Budget Analysis in Instrumentation Amplifier Applications," Application Note AN-539, Analog Devices.

Nash, Eamon. "A Practical Review of Common-Mode and Instrumentation Amplifiers," *Sensors Magazine*, July 1998, Article Reprint Available from Analog Devices.

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Chapter I

Basic In-Amp Theory

INTRODUCTION

The fact that some op-amps are dubbed instrumentation amplifiers (or in-amps) by their suppliers does not make them in-amps, even though they may be used in instrumentation. Likewise, an isolation amplifier is not necessarily an instrumentation amplifier. This application note will explain what an in-amp actually is, how it operates, and how and where to use it.

WHAT IS AN INSTRUMENTATION AMPLIFIER?

An instrumentation amplifier is a closed-loop gain block that has a differential input and an output that is single-ended with respect to a reference terminal. Most commonly, the impedances of the two input terminals are balanced and have high values, typically 10^9 Ω or greater. The input bias currents should also be low, typically 1 nA to 50 nA. As with op-amps, output impedance is very low, nominally only a few milli Ohms, at low frequencies.

Unlike an op-amp, which has its closed-loop gain determined by external resistors connected between its inverting input and its output, an in-amp employs an internal feedback resistor network that is isolated from its signal input terminals. With the input signal applied across the two differential inputs, gain is either preset internally or is user-set (via pins) by an internal or external gain resistor, which is also isolated from the signal inputs. Figure 1 contrasts the differences between op-amp and in-amp input characteristics.

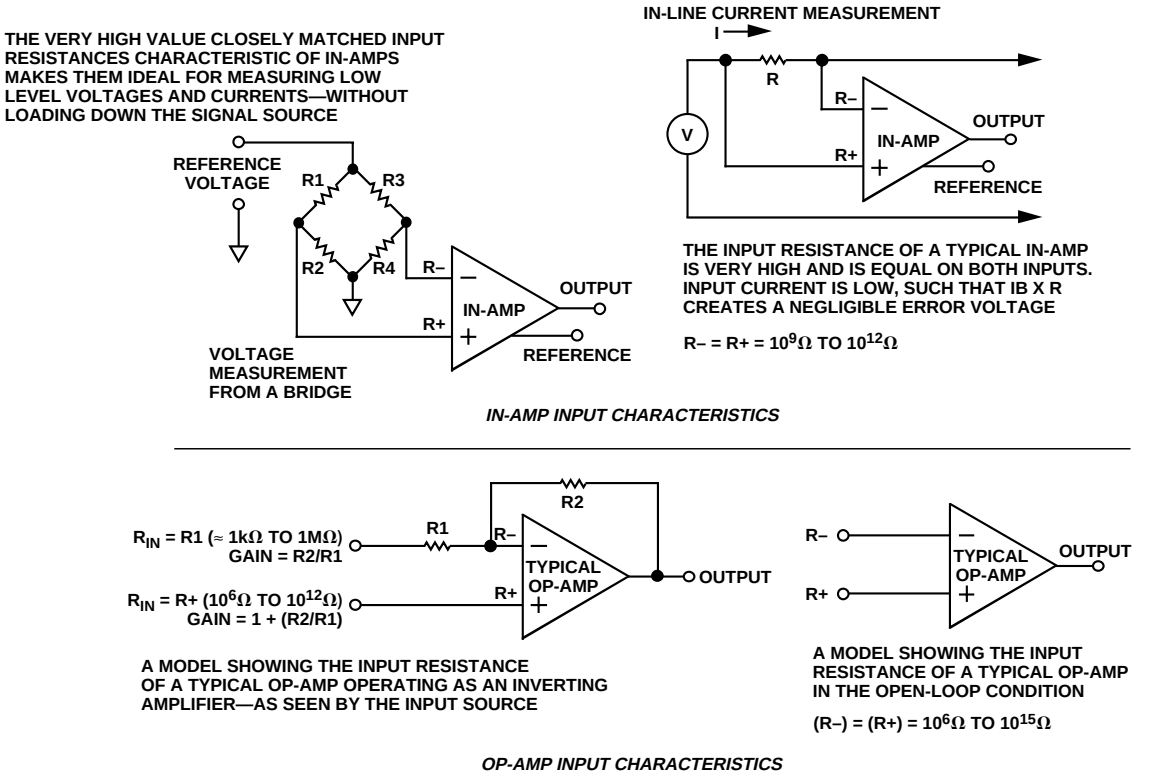


Figure 1. Op-Amp vs. In-Amp Input Characteristics

Common-mode rejection, the property of canceling out any signals that are common (the same potential on both inputs), while amplifying any signals that are differential (a potential difference between the inputs), is the most important function an instrumentation amplifier provides. Both dc and ac common-mode rejection are important in-amp specifications. Any errors due to a dc common-mode voltage (i.e., a dc voltage present at both inputs) will be reduced 80 dB to 120 dB by any decent quality modern in-amp.

However, inadequate ac CMR causes a large, time-varying error that often changes greatly with frequency and so is difficult to remove at the IA's output. Fortunately, most modern monolithic IC in-amps provide excellent ac and dc common-mode rejection.

Common-mode gain (A_{CM}) is related to common-mode rejection and is the ratio of change in output voltage to a change in common-mode input voltage. This is the net gain (or attenuation) from input to output for voltages common to both inputs. For example, an in-amp with a common-mode gain of 1/1,000 and a 10-volt common-mode voltage at its inputs will exhibit a 10 mV output change. The differential or "normal mode" gain (A_D) is the gain between input and output for voltages applied differentially (or across) the two inputs. The common-mode rejection ratio (CMRR) is simply the ratio of the differential gain, A_D, to the common-mode gain (A_{CM}). Note that in an ideal in-amp, CMRR will increase in proportion to gain.

Common-mode rejection is usually specified for a full-range common-mode voltage (CMV) change at a given frequency, and a specified imbalance of source impedance (e.g., 1 kΩ source unbalance, at 60 Hz). The term CMR is a logarithmic expression of the common-mode rejection ratio (CMRR).

That is: $CMR = 20 \log_{10} CMRR$.

In order to be effective, an in-amp needs to be able to amplify microvolt-level signals while simultaneously rejecting volts of common-mode at its inputs. It is particularly important that the in-amp is able to reject common-mode signals over the bandwidth of interest. For techniques on reducing errors due to out-of-band signals that may appear as a dc output offset, please refer to the RFI section of this guide.

This requires that instrumentation amplifiers have very high common-mode rejection over the main frequency of interest and its harmonics. Typical dc values of CMR are 70 dB to over 100 dB, with CMR usually improving at higher gains. While it is true that operational amplifiers, connected as subtractors, also provide common-mode rejection, the user must provide closely matched external resistors (to provide adequate CMRR). On the other hand, monolithic in-amps with their pretrimmed resistor networks, are far easier to apply.

WHAT OTHER PROPERTIES DEFINE A HIGH QUALITY IN-AMP?

Possessing a high common-mode rejection ratio, an instrumentation amplifier needs the following properties:

High AC (and DC) Common-Mode Rejection (CMR)

At a minimum, the in-amp's CMR should be high over the range of input frequencies that need to be rejected. This includes high CMR at power line frequencies and at the second harmonic of the power line frequency.

Low Offset Voltage and Offset Voltage Drift

As with an operational amplifier, an in-amp must have a low offset voltage. Since an instrumentation amplifier consists of two independent sections: an input stage and an output amplifier, total output offset will equal the sum of the gain, times the input offset, plus the output offset. Typical values for input and output offset drift are 1 μV/°C and 10 μV/°C, respectively. Although the initial offset voltage may be nulled with external trimming, offset voltage drift cannot be adjusted out. As with initial offset, offset drift has two components, with the input and output section of the in-amp each contributing its portion of error to the total. As gain is increased, the offset drift of the input stage becomes the dominant source of offset error.

A Matched, High Input Impedance

The impedances of the inverting and noninverting input terminals of an in-amp must be high and closely matched to one another. Values of 10^9 Ω to 10^{12} Ω are typical. Difference amplifiers, such as the AD626, have lower input impedances, but can be very effective in high common-mode voltage applications.

Low Input Bias and Offset Current Errors

Again, as with an op-amp, an instrumentation amplifier has *bias* currents that flow into, or out of, its input terminals: bipolar in-amps with their base currents and FET amplifiers with gate leakage currents. This *bias current* flowing through an imbalance in the signal source resistance will create an offset error. Note that if the input source resistance becomes infinite, as with ac (capacitive) input coupling without a resistive return to power supply ground, the input common-mode voltage will climb until the amplifier saturates. A high value resistor, (such that $I_B \times R < V_{CM}$) connected between

each input and ground, is normally used to prevent this problem. Typically, the input bias current multiplied by the resistor's value in Ohms should be less than the common-mode voltage. Input *offset current* errors are defined as the mismatch between the bias currents flowing in the two inputs. Typical values of input bias current for a bipolar in-amp range from 1 nA to 50 nA; for a FET input device, values of 1 pA to 50 pA are typical at room temperature.

Low Noise
Because it must be able to handle very low level input voltages, an in-amp must not add its own noise to that of the signal. An input noise level of 10 nV/$\sqrt{\text{Hz}}$ @ 1 kHz referred to input (RTI) or lower is desirable. Micropower in-amps are optimized for the lowest possible input stage current and so typically have higher noise levels than their higher current cousins.

Low Nonlinearity
Input offset and scale factor errors can be corrected by external trimming, but nonlinearity is an inherent performance limitation of the device and cannot be removed by external adjustment. Low nonlinearity must be designed in by the manufacturer. Nonlinearity is normally specified in percent-of-full-scale where the manufacturer measures the in-amp's error at the plus and minus full-scale voltage and at zero. A nonlinearity error of 0.01% is typical for a high quality in-amp; some even have levels as low as 0.0001%.

Simple Gain Selection
Gain selection should be easy to apply. The use of a single external gain resistor is common, but the gain resistor will affect the circuit's accuracy and gain drift with temperature. In-amps such as the AD621 provide a choice of internally preset gains that are pin selectable.

Adequate Bandwidth
An instrumentation amplifier must provide bandwidth sufficient for the particular application. Since typical unity gain small-signal bandwidths fall between 500 kHz and 4 MHz, performance at low gains is easily achieved, but at higher gains, bandwidth becomes much more of an issue. Micropower in-amps typically have lower bandwidth than comparable standard in-amps, as micropower input stages are operated at much lower current levels.

WHERE IS AN INSTRUMENTATION AMPLIFIER USED?

Data Acquisition
In-amps find their primary use amplifying signals from low output transducers in noisy environments. The amplification of pressure or temperature transducer signals is a common in-amp application. Common bridge applications include strain and weight measurement using "load cells" and temperature measurement using resistive temperature detectors or "RTDs."

Medical Instrumentation
In-amps are also widely used in medical equipment such as EKG and EEG monitors, blood pressure monitors, and defibrillators.

Monitor and Control Electronics
In-amps may be used to monitor voltages or currents in a system and then trigger alarm systems when nominal operating levels are exceeded.

Software-Programmable Applications
An in-amp may be used with a software-programmable resistor chip to allow software control of hardware systems.

Audio Applications
Again, because of their high common-mode rejection, instrumentation amplifiers are sometimes used for audio (as microphone preamps, etc.), to extract a weak signal from a noisy environment and to minimize offsets and noise due to ground loops. Refer to Table XI, (Page 51) Specialty Products Available from Analog Devices.

High-Speed Signal Conditioning
As the speed and accuracy of modern video data acquisition systems have increased, there is now a growing need for high bandwidth instrumentation amplifiers, particularly in the field of CCD imaging equipment where offset correction and input buffering are required. Double-correlated sampling techniques are often used here for offset correction of the CCD image. Two sample-and-hold amplifiers monitor the pixel and reference levels, and a dc-corrected output is provided by feeding their signals into an instrumentation amplifier.

Video Applications
High-speed in-amps may be used in many video and cable RF systems to amplify or process high frequency signals.

Power Control Applications
In-amps can be used for motor monitoring (to monitor and control motor speed, torque, etc.) by measuring the voltages, currents, and phase relationships of a three-phase ac phase motor.

IN-AMPS: AN EXTERNAL VIEW

Figure 2 shows a functional block diagram of an instrumentation amplifier.

Since an ideal instrumentation amplifier detects only the difference in voltage between its inputs, any common-mode signals (potentials that are equal on both inputs), such as noise or voltage drops in ground lines, are rejected at the input stage without being amplified.

Normally, a single resistor is used to program the in-amp for the desired gain. The user can calculate the required value of resistance for a given gain, using the gain equation listed in the in-amp's spec sheet.

The output of an instrumentation amplifier often has its own sense and reference terminals which, among their other uses, allow the in-amp to drive a load that may be in a distant location.

Figure 2 shows the input and output commons being returned to the same potential, in this case to power supply "ground." This "star" ground connection is a very effective means for minimizing ground loops in the circuit; however some residual "common-mode" ground currents will still remain. These currents flowing through R_{CM} will develop a common-mode voltage error, V_{CM}. The in-amp, by virtue of its high common-mode rejection, will amplify the differential signal while rejecting V_{CM} and any common-mode noise.

Of course, power must be supplied to the in-amp—as with op-amps, this is normally a dual supply voltage that will operate the in-amp over a specified range. Alternatively, an in-amp specified for "single supply" (rail-to-rail) operation may be used.

An instrumentation amplifier may be assembled using one or more operational amplifiers or it may be of monolithic construction. Both technologies have their virtues and limitations. In general, discrete (op-amp) in-amps offer wide flexibility at low cost and can sometimes provide performance unattainable with monolithic designs, such as very high bandwidth. In contrast, monolithic designs provide the complete in-amp function, fully specified, usually factory trimmed, and often to higher dc precision than discrete designs. Monolithic in-amps are also much smaller in size, lower in cost, and easier to apply. Discrete op-amp designs will be discussed first.

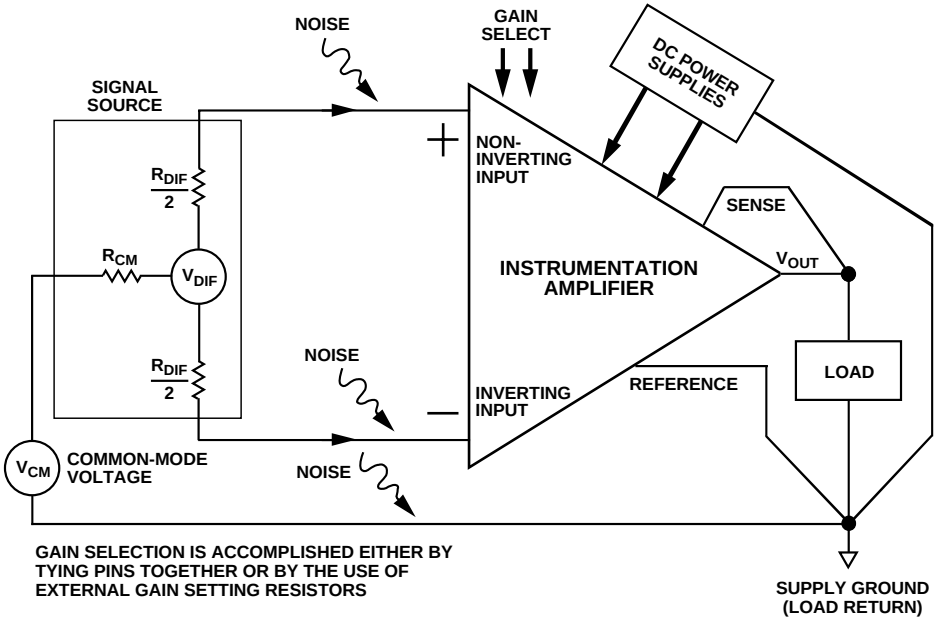


Figure 2. Basic Instrumentation Amplifier

INSIDE AN INSTRUMENTATION AMPLIFIER

A Simple Op-Amp Subtractor Provides an In-Amp Function

The simplest (but still very useful) method of implementing a differential gain block is shown in Figure 3.

If R1 = R3 and R2 = R4, then:

$$V_{OUT} = (V_{IN\#2} - V_{IN\#1})\ (R2/R1)$$

Although this circuit does provide in-amp function-amplifying differential signals while rejecting those that are common-mode—it also has some serious limitations. First, the impedances of the inverting and noninverting inputs are relatively low and unequal. In this example, the input impedance to $V_{IN\#1}$ equals 100 kΩ, while the impedance of $V_{IN\#2}$ is twice that, equaling 200 kΩ. Therefore, when voltage is applied to one input, while grounding the other, different currents will flow, depending on which input receives the applied voltage (this unbalance in the sources resistances will degrade the circuit's CMRR).

Furthermore, this circuit requires a very close ratio match between resistor pairs R1/R2 and R3/R4; otherwise, the gain from each input will be different—directly affecting common-mode rejection. For example, at a gain of 1, with all resistors of equal value, a 0.1% mismatch in just one of the resistors will degrade the CMR to a level of 66 dB (1 part in 2000). Similarly, a source resistance imbalance of 100 Ω will degrade CMR by 6 dB.

In spite of these problems, this type of "bare bones" in-amp circuit, often called a "difference amplifier or subtractor," is useful as a building block within higher performance in-amps. It is also very practical as a stand-alone functional circuit in video and other high-speed uses, or in low frequency, high CMV applications, where the input resistors divide down the input voltage as well as provide input protection for the amplifier. Some monolithic in-amps such as the Analog Devices' AD629 employ a variation of the simple subtractor in their design. This allows the in-amp to handle common-mode input voltages higher than its own supply voltage. For example, when powered from a ±15 V supply, the AD629 can amplify signals with common-mode voltages as high as ±270 V.

Improving the Simple Subtractor with Input Buffering

An obvious way to significantly improve performance is to add high input impedance buffer amplifiers ahead of the simple subtractor circuit, as shown in the three op-amp instrumentation amplifier circuit of Figure 4.

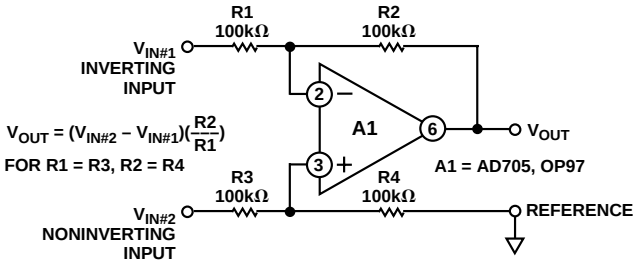


Figure 3. A One Op-Amp In-Amp Circuit Functional Diagram

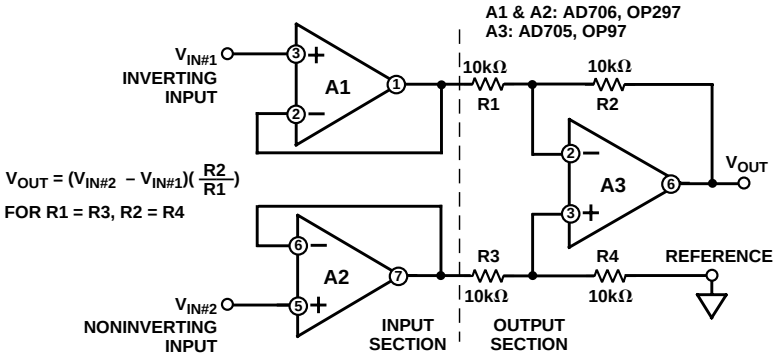


Figure 4. A Subtractor Circuit with Input Buffering

This circuit now provides matched, high impedance inputs so that the impedances of the input sources will have a minimal effect on the circuit's common-mode rejection. The use of a dual op-amp for the two input buffer amplifiers is preferred since they will better track each other over temperature and save board space. Although the resistance values are different, this circuit has the same transfer function as the circuit of Figure 3.

Figure 5 shows a further improvement: now the input buffers are operating with gain, which provides a circuit with more flexibility. If R5 = R8 and R6 = R7 and, as before R1 = R3 and R2 = R4, then:

$$V_{OUT} = (V_{IN\#2} - V_{IN\#1})\ (1 + R5/R6)\ (R2/R1)$$

While the circuit of Figure 5 does increase gain (equally) for differential signals, it also increases the gain for common-mode signals.

The Three Op-Amp In-Amp

The circuit of Figure 6 provides a final refinement and has become the most popular configuration for instrumentation amplifier design.

The "classic" three op-amp in-amp circuit is a clever modification of the buffered subtractor circuit of Figure 5. As with the previous circuit, op-amps A1 and A2 of Figure 6 buffer the input voltage. But in this configuration, a single gain resistor, R_G, is connected between the summing junctions of the two input buffers, replacing R6 and R7. The full differential input voltage will now appear across R_G (because the voltage at the summing junction of each amplifier is equal to the voltage applied to its + input). Since the amplified input voltage (at the outputs of A1 and A2) appears differentially across the three resistors, R5, R_G, and R6, the differential gain may be varied by just changing R_G.

Another advantage of this connection is that once the subtractor circuit has been set up with its ratio-matched resistors, no further resistor matching is required when changing gains. If R5 = R6 and R1 = R3 and R2 = R4, then:

$$V_{OUT} = (V_{IN\#2} - V_{IN\#1})\ (1 + 2R5/R_G)(R2/R1)$$

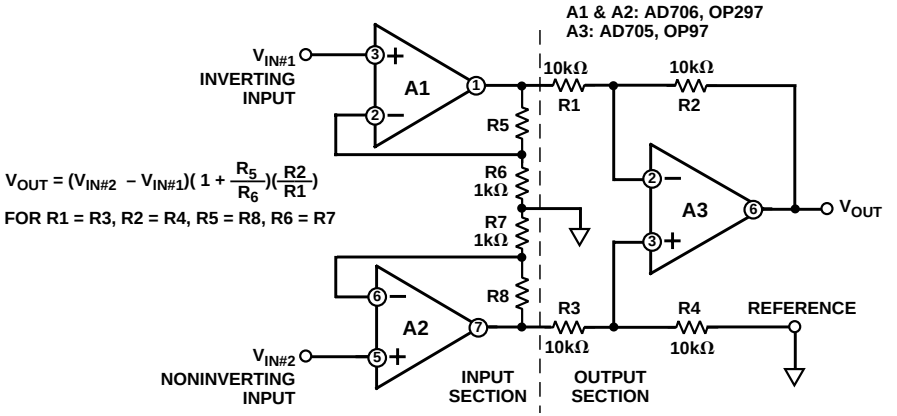


Figure 5. A Buffered Subtractor Circuit with Buffer Amplifiers Operating with Gain

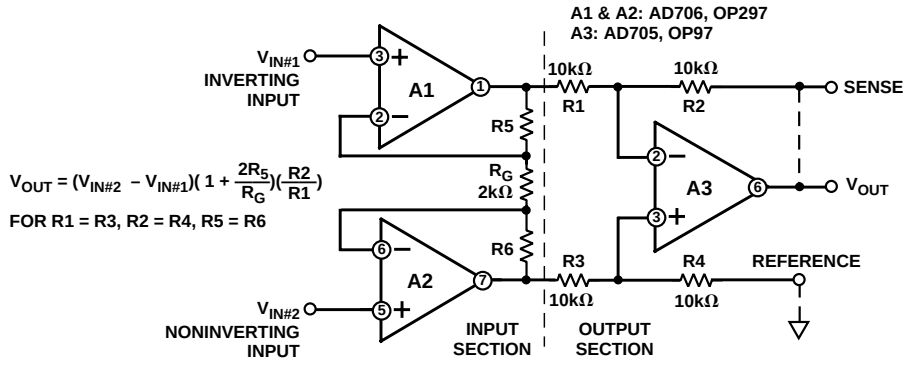


Figure 6. The "Classic" Three Op-Amp In-Amp Circuit

Since the voltage across R_G equals V_{IN}, the current through R_G will equal: (V_{IN}/R_G). Amplifiers A1 and A2 will, therefore, operate with gain and amplify the input signal. Note, however, that if a common-mode voltage is applied to the amplifier inputs, the voltages on each side of R_G will be equal and no current will flow through this resistor. Since no current flows through R_G (and, therefore, through R5 and R6), amplifiers A1 and A2 will operate as unity gain followers. Therefore, common-mode signals will be passed through the input buffers at unity gain, but differential voltages will be amplified by the factor (1 + (2 R_F/R_G)).

In theory, this means that the user may take as much gain in the front end as desired (as determined by R_G) without increasing the common-mode gain and error. That is, the differential signal will be increased by gain, but the common-mode error will not, so the ratio (Gain (V_{DIFF})/($V_{ERROR\ CM}$)) will increase. Thus, CMRR will theoretically increase in direct proportion to gain—a very useful property.

Finally, because of the symmetry of this configuration, common-mode errors in the input amplifiers, if they track, tend to be canceled out by the output stage subtractor. This includes such errors as common-mode rejection vs. frequency. These features explain the popularity of this configuration.

Three Op-Amp In-Amp Design Considerations

Three op-amp instrumentation amplifiers may be constructed using either FET or bipolar input operational amplifiers. FET input op-amps have very low bias currents and are generally well-suited for use with very high (>10^6 Ω) source impedances. FET amplifiers usually have lower CMR, higher offset voltage, and higher offset drift than bipolar amplifiers. They also may provide a higher slew rate for a given amount of power.

The sense and reference terminals (Figure 6) permit the user to change A3's feedback and ground connections. The sense pin may be externally driven for servo and other applications where the gain of A3 needs to be varied. Likewise, the reference terminal allows an external offset voltage to be applied to A3. For normal operation the sense and output terminals are tied together, as are reference and ground.

Amplifiers with bipolar input stages will tend to achieve both higher CMR and lower input offset voltage drift than FET input amplifiers. Superbeta bipolar input stages combine many of the benefits of both FET and bipolar processes, with even lower IB drift than FET devices.

A common (but frequently overlooked) pitfall for the unwary designer using a three op-amp in-amp design is the reduction of common-mode voltage range which occurs when the in-amp is operating at high gain. Figure 7 is a schematic of a three op-amp in-amp operating at a gain of 1000.

In this example, the input amplifiers, A1 and A2, are operating at a gain of 1000, while the output amplifier is providing unity gain. This means that the voltage at the output of each input amplifier will equal one-half the peak-to-peak input voltage times 1000, plus any common-mode voltage that is present on the inputs (the common-mode voltage will pass through at unity gain

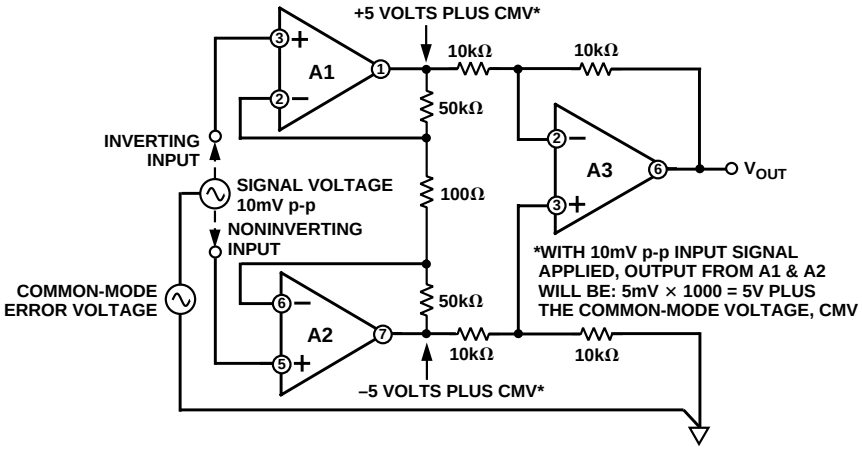


Figure 7. A Three Op-Amp In-Amp Showing Reduced CMV Range

regardless of the differential gain). Therefore, if a 10 mV differential signal is applied to the amplifier inputs, amplifier Al's output will equal +5 volts plus the common-mode voltage and A2's output will be –5 volts plus the common-mode voltage. If the amplifiers are operating from +15 volt supplies, they will usually have 7 volts or so of headroom left, thus permitting an 8-volt common-mode voltage—but not the full 12 volts of CMV which, typically, would be available at unity gain (for a 10 mV input). Higher gains, or lower supply voltages, will further reduce the common-mode voltage range.

The Basic Two Op-Amp Instrumentation Amplifier

Figure 8 is a schematic of a typical two op-amp in-amp circuit. It has the obvious advantage of requiring only two, rather than three, operational amplifiers with subsequent savings in cost and power consumption. However, the nonsymmetrical topology of the two op-amp in-amp circuit can lead to several disadvantages compared to the three op-amp design, most notably lower ac CMRR, which limits its usefulness.

The transfer function of this circuit is:

$$V_{OUT} = (V_{IN\#2} - V_{IN\#1})\ (1 + R4/R3)$$

for $R1 = R4$ and $R2 = R3$

Input resistance is high and balanced, thus permitting the signal source to have an unbalanced output impedance. The circuit's input bias currents are set by the input current requirements of the noninverting input of the two op-amps which, typically, are very low.

Disadvantages of this circuit include the inability to operate at unity gain, a decreased common-mode voltage range as circuit gain is lowered, and its usually poor ac common-mode rejection. The poor CMR is due to the unequal phase shift occurring in the two inputs, $V_{IN\#1}$ and $V_{IN\#2}$. That is, the signal must travel through amplifier A1 *before* it is subtracted from $V_{IN\#2}$ by amplifier A2. Thus, the voltage at the output of A1 is slightly delayed or phase-shifted with respect to $V_{IN\#1}$.

Minimum circuit gains of 5 are commonly used with the two op-amp in-amp circuit, as this permits an adequate dc common-mode input range and also provides sufficient bandwidth for most applications. The use of rail-to-rail (single supply) amplifiers will provide a common-mode voltage range that extends down to $-V_S$ (or "ground" in single supply operation), plus true "rail-to-rail" output voltage range (i.e., an output swing from $+V_S$ to $-V_S$).

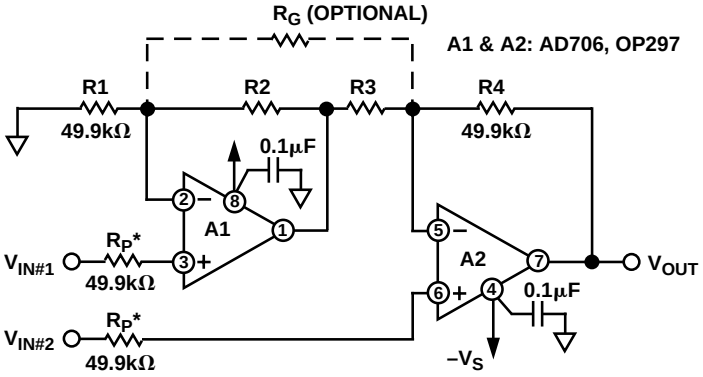


Figure 8. A Two Op-Amp In-Amp Circuit

Table I shows amplifier gain vs. circuit gain for the circuit of Figure 8 and gives practical 1% resistor values for several common circuit gains.

Table I. Operating Gains of Amplifiers A1 and A2 and Practical 1% Resistor Values for the Circuit of Figure 8

Circuit Gain	Gain of A1	Gain of A2	R2, R3 (kΩ)	R1, R4 (kΩ)
1.10	11.00	1.10	499	49.9
1.33	4.01	1.33	150	49.9
1.50	3.00	1.50	100	49.9
2.00	2.00	2.00	49.9	49.9
10.1	1.11	10.10	5.49	49.9
101.0	1.01	101.0	499	49.9
1001	1.001	1001	49.9	49.9

Two Op-Amp In-Amps—Common-Mode Design Considerations for Single Supply Operation

If the two op-amp in-amp circuit of Figure 9a is examined from the reference input, it can be seen that it is simply a cascade of two inverters. Assuming that the voltage at both of the signal inputs, V_{IN1} and V_{IN2}, is zero, the output of A1 will equal:

$$V_{O1} = -V_{REF}\,(R2/R3)$$

A positive voltage applied to V_{REF} will tend to drive the output voltage of A1 negative, which is clearly NOT possible if the amplifier is operating from a single power supply voltage ($+V_S$ and 0 V).

The gain from the output of amplifier A1 to the circuit's output, V_{OUT}, at A2, is equal to:

$$V_{OUT} = -V_{O1}\,(R4/R3)$$

The gain from V_{REF} to V_{OUT} is the product of these two gains and equals:

$$V_{OUT} = (-V_{REF}\,(R2/R3))(-R4/R3)$$

In this case, R1 = R4 and R2 = R3. Therefore, the "reference gain" is +1 as expected. Note that this is the result of two inversions, in contrast to the noninverting signal path of the reference input in a typical three op-amp IA circuit.

Just as with the three op-amp IA, the common-mode voltage range of the two op-amp IA can be limited by single supply operation and by the choice of reference voltage.

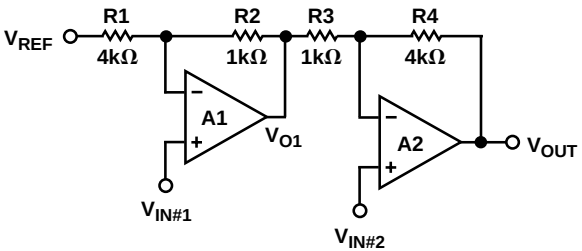


Figure 9a. The Two Op-Amp In-Amp Architecture

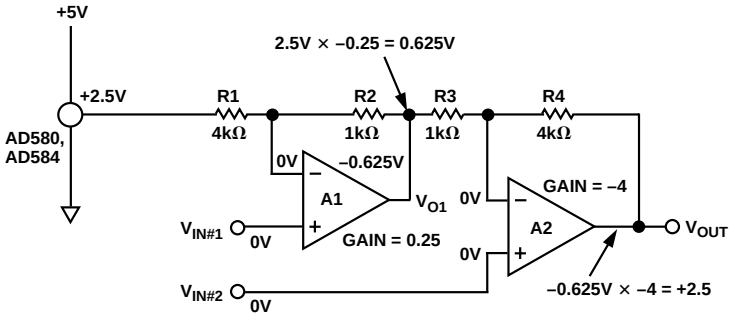


Figure 9b. Output Swing Limitations of Two Op-Amp In-Amp Using A +2.5 V Reference

Figure 9b is a schematic of a two op-amp in-amp operating from a single +5 V power supply. The reference input is tied to $V_S/2$ which, in this case, is +2.5 V. The output voltage should ideally be +2.5 V for a differential input voltage of zero volts and for any common-mode voltage within the power supply voltage range (0 V to +5 V).

As the common-mode voltage is increased from +2.5 V toward +5 V, the output voltage of A1 (V_{O1}) will equal:

$$V_{O1} = V_{CM} + ((V_{CM} - V_{REF})\ (R2/R1))$$

In this case, V_{REF} = +2.5 V and R2/R1 = 1/4. The output voltage of A1 will reach +5 V when V_{CM} = +4.5 V. Further increases in common-mode voltage obviously cannot be rejected. In practice, the input voltage range limitations of amplifiers A_1 and A_2 may limit the IA's common-mode voltage range to less than +4.5 V.

Similarly, as the common-mode voltage is reduced from +2.5 V toward zero volts, the output voltage of A_1 will "hit" zero for a V_{CM} of 0.5 V. Clearly, the output of A_1 cannot go more negative than the negative supply line (assuming no "charge pump"), which, for a single supply connection, equals zero volts. This negative or "zero in" common-mode range limitation can be overcome by proper design of the in-amp's internal level shifting, as in the AD627 monolithic two op-amp IA. However, even with good design, some positive common-mode voltage range will be "traded-off" to achieve operation at zero common-mode voltage.

Another, and perhaps more serious, limitation of the standard two amplifier IA circuit, compared to three amplifier designs, is the intrinsic difficulty of achieving high ac common-mode rejection. This limitation stems from the inherent imbalance in the common-mode signal path of the two-amplifier circuit.

Assume that a sinusoidal common-mode voltage, V_{CM}, at a frequency F_{CM}, is applied (common-mode) to inputs V_{IN1} and V_{IN2} (Figure 9b). Ideally, the amplitude of the resulting ac output voltage (the common-mode error) should be zero, independent of frequency, F_{CM}, at least over the range of normal ac power line ("mains") frequencies: 50 Hz to 400 Hz. Power lines tend to be the source of much "common-mode interference."

If the ac common-mode error is zero, amplifier A_2 and gain network R3, R4 must see zero instantaneous difference between the common-mode voltage, applied directly to V_{IN2}, and the version of the common-mode voltage that is amplified by A_1 and its associated gain network R1, R2. Any "dc" common-mode error (assuming negligible error from the amplifier's own CMRR) can be nulled by trimming the ratios of R1, R2, R3, and R4, to achieve the balance:

$$R1 \equiv R4 \text{ and } R2 \equiv R3$$

However, any phase shift (delay) introduced by amplifier A_1 will cause the phase of V_{O1} to slightly lag behind the phase of the directly applied common-mode voltage of V_{IN2}. This difference in phase will result in an instantaneous (vector) difference in V_{O1} and V_{IN2}, even if the amplitude of both voltages are at their ideal levels. This will cause a frequency-dependent common-mode error voltage at the circuit's output, V_{OUT}. Further, this ac common-mode error will increase linearly with common-mode frequency, because the phase shift through A_1 (assuming a single-pole roll-off) will increase directly with frequency. In fact, for frequencies less than 1/10th the closed-loop bandwidth (f_{T1}) of A_1, the common-mode error (referred to the input of the in-amp) can be approximated by:

$$\%\ CM\ Error = \frac{V_E/G}{V_{CM}}\left(100\%\right) = \frac{f_{CM}}{f_{TI}}\left(100\%\right)$$

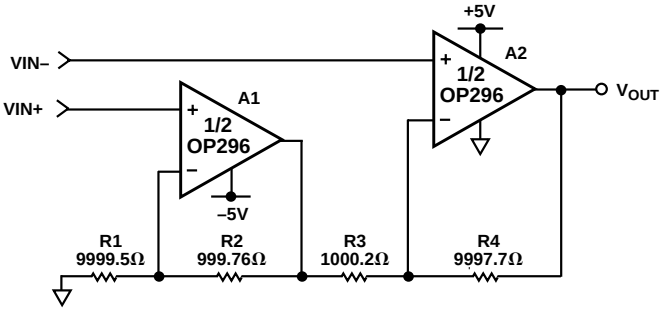


Figure 10a. "Homebrew In-Amp" Example

Where V_E is the common-mode error voltage at V_{OUT}, and G is the differential gain, in this case five.

For example, if A_1 has a closed-loop bandwidth of 100 kHz (a typical value for a micropower op-amp), when operating at the gain set by R1 and R2, and the common-mode frequency is 100 Hz, then:

$$\%\,CM\ Error = \frac{100\ Hz}{100\ kHz}\left(100\%\right) = 0.1\%$$

A common-mode error of 0.1% is equivalent to 60 dB of common-mode rejection. So, in this example, even if this circuit were trimmed to achieve 100 dB CMR at dc, this would be valid only for frequencies less than 1 Hz. At 100 Hz, the CMR could never be better than 60 dB.

The AD627 monolithic in-amp embodies an advanced version of the two op-amp IA circuit which overcomes these ac common-mode rejection limitations. As illustrated in Figure 31, the AD627 maintains over 80 dB of CMR out to 8 kHz (Gain of 1000), even though the bandwidth of amplifiers A1 and A2 is only 150 kHz.

Make vs. Buy: A Two Op-Amp In-Amp Example

The examples in Figures 10a and 10b serve as a good comparison between the errors associated with an integrated and a discrete in-amp implementation. A ±100 mV signal from a resistive bridge (common-mode voltage = +2.5 V) is to be amplified. This example compares the resulting errors from a discrete two op-amp in-amp and from the AD627. The discrete implementation uses a four-resistor precision network (1% match, 50 ppm/°C tracking).

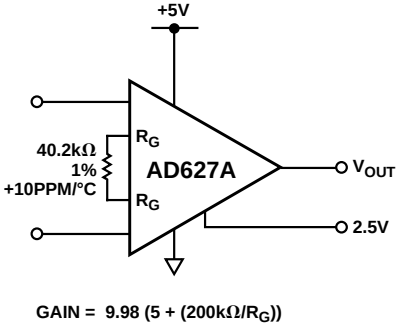


Figure 10b. AD627 Monolithic In-Amp Circuit

The errors associated with each implementation show the integrated in-amp to be more precise, both at ambient and over temperature. It should be noted that the discrete implementation is also more expensive. This is primarily due to the relatively high cost of the low drift precision resistor network.

Note that a mismatch of 0.1% between the four gain setting resistors will determine the low frequency CMR of a two op-amp in-amp. The plot in Figure 11a shows the practical results, at ambient temperature, of resistor mismatch. The CMR of the circuit in Figure 10a (Gain = 11) was measured using four resistors which had a mismatch of almost exactly 0.1% (R1 = 9999.5 Ω, R2 = 999.76 Ω, R3 = 1000.2 Ω, R4 = 9997.7 Ω).

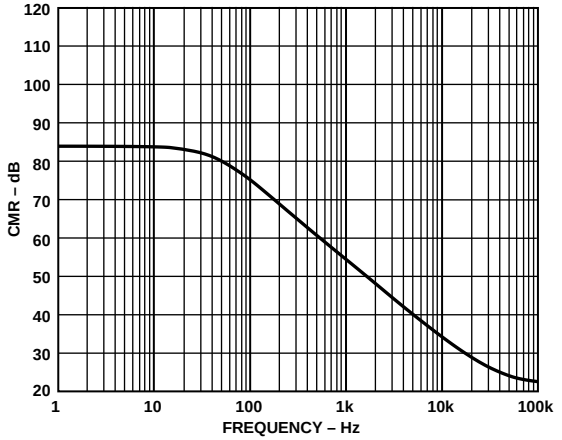


Figure 11a. CMR over Frequency of "Homebrew" In-Amp

As expected, the CMR at dc was measured at about 84 dB (calculated value is 85 dB). However, as the frequency increases, the CMR quickly degrades. For example, a 200 mV p-p common-mode voltage at 180 Hz (the third harmonic of the 60 Hz ac power line frequency) would result in an output voltage of approximately 800 μV p-p, compared to a level of 160 μV p-p at the 60 Hz fundamental. To put this in context, a 12-bit data acquisition system with an input range of 0 V to 2.5 V, has an LSB weighting of 610 μV.

By contrast, the AD627 uses precision laser trimming of internal resistors along with patented ac CMR balancing circuit to achieve a higher dc CMR and a wider bandwidth over which the CMR is flat. This is shown in Figure 11b.

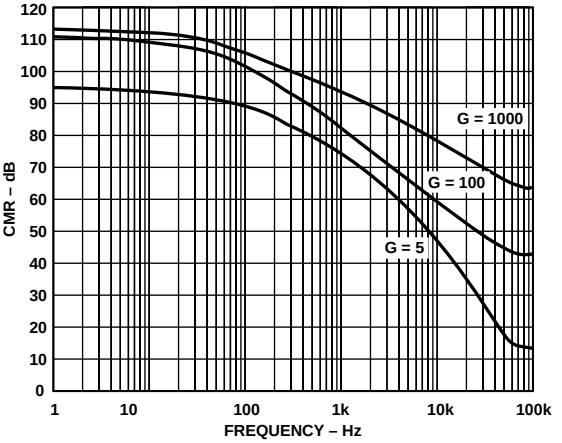


Figure 11b. CMR over Frequency of AD627 In-Amp Circuit

Chapter II

Monolithic Instrumentation Amplifiers

ADVANTAGES OVER OP-AMP IN-AMPS

To satisfy the demand for in-amps that would be easier to apply, monolithic IC instrumentation amplifiers were developed. These circuits incorporate variations in the three op-amp and two op-amp in-amp circuits previously described, while providing laser-trimmed resistors and other benefits of monolithic IC technology. Since both active and passive components are now within the same die they can be closely matched—this will ensure that the device provides a high CMR. In addition, these components will stay matched over temperature, assuring excellent performance over a wide temperature range. IC technologies such as laser wafer trimming allow monolithic integrated circuits to be "tuned-up" to very high accuracy and provide low cost, high volume manufacturing. A final advantage of monolithic devices is that they are available in very small, very low cost SOIC, or microSOIC packages designed for use in high volume production. Table II provides a quick performance summary of Analog Devices' in-amps.

Table II. Latest Generation Analog Devices In-Amps Summarized

Product	Features	Supply Current (Typ)	BW kHz (G = 1)	Input Offset Voltage (Max)	Input Offset Drift	RTI Noise nV/√Hz (G = 10)	Input Bias Current (Max)
AD620	General Purpose	0.9 mA	800	125 µV	1 µV/°C	12 Typ	2 nA
AD622	Low Cost	0.9 mA	800	125 µV	1 µV/°C	14 Typ	5 nA
AD621	Precise Gain	0.9 mA	800	250 µV (RTI)	2.5 µV/°C (RTI)	13 Typ (RTI)	2 nA
AD623	Low Cost, Single Supply	375 µA	800	200 µV	2 µV/°C	35 Typ	25 nA
AD627	Micropower	60 µA	80	250 µV	3 µV/°C	42 Typ	10 nA
AD626	High CMV	1.5 mA	100	500 µV	1 µV/°C	250 Typ	NS
AD830	Video In-Amp	15 mA	85 MHz	1500 µV	70 µV/°C	27 Typ	10 µA
AD629	High CMV Diff Amp	0.9 mA	500 kHz	1 mV	6 µV/°C	550 Typ (G = 1)	NA
AMP03	High BW, G = 1	3.5 mA	3 MHz	400 µV	NS	750 (RTO)	NS

NS: Not Specified.
NA: Not Applicable.

MONOLITHIC IN-AMP DESIGN—THE INSIDE STORY

Monolithic In-Amps Optimized for High Performance

Analog Devices introduced the first high performance monolithic instrumentation amplifier, the AD520, in 1971.

In 1992, the **AD620** was introduced and has now become the industry standard high-performance, low cost in-amp. The AD620 is a complete monolithic instrumentation amplifier offered in both 8-lead DIP and SOIC packages. The user can program any desired gain from 1 to 1000 using a single external resistor. By design, the required resistor values for gains of 10 and 100 are standard 1% metal film resistor values.

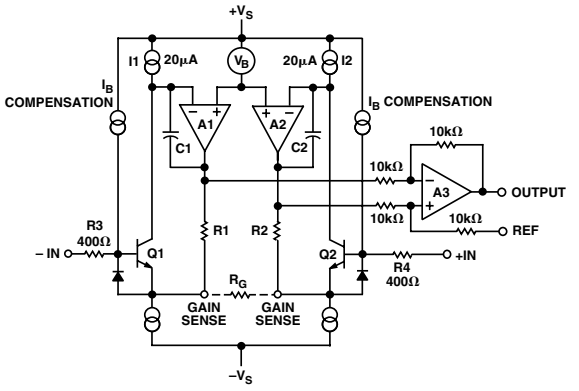


Figure 12. A Simplified Schematic of the AD620

The AD620 is a second-generation version of the classic AD524 in-amp and embodies a modification of the classic three op-amp circuit. Laser trimming of on-chip thin film resistors R1 and R2 allows the user to accurately set the gain—to 100 within ±0.5% max error, using only one external resistor. Monolithic construction and laser wafer trimming allow the tight matching and tracking of circuit components.

A preamp section comprised of Q1 and Q2 provides additional gain up front. Feedback through the Q1-A1-R1 loop and the Q2-A2-R2 loop maintains a constant collector current through the input devices Q1, Q2, thereby impressing the input voltage across the external gain setting resistor R_G. This creates a differential gain from the inputs to the A1/A2 outputs given by $G = (R1 + R2)/R_G + 1$. The unity gain subtractor A3 removes any common-mode signal, yielding a single-ended output referred to the REF pin potential.

The value of R_G also determines the transconductance of the preamp stage. As R_G is reduced for larger gains, the transconductance increases asymptotically to that of the input transistors. This has three important advantages: First, the open-loop gain is boosted for increasing programmed gain, thus reducing gain related errors.

Next, the gain bandwidth product (determined by C1, C2 and the preamp transconductance) increases with programmed gain, thus optimizing the amplifier's frequency response. Figure 13 shows the AD620's closed-loop gain vs. frequency.

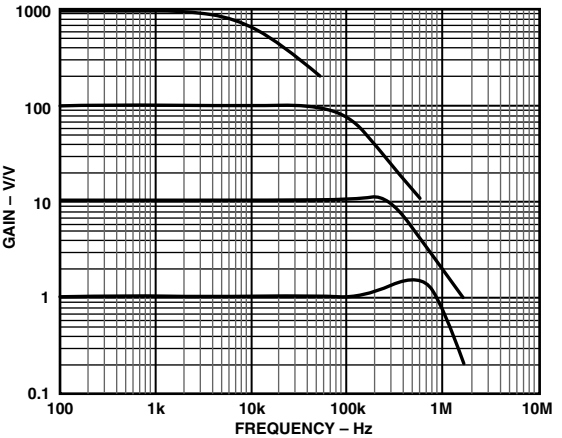


Figure 13. AD620 Closed-Loop Gain vs. Frequency

The AD620 also has superior CMR over a wide frequency range as shown by Figure 14.

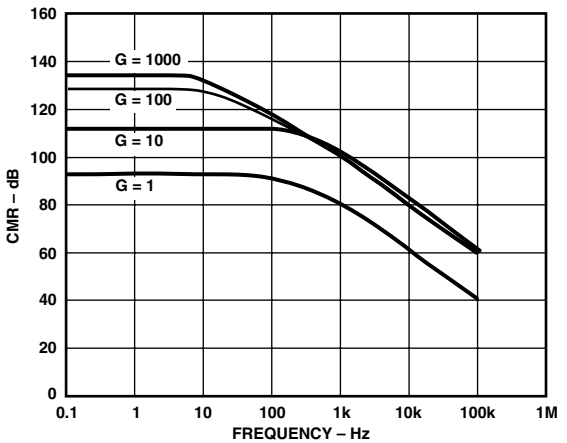


Figure 14. AD620 CMR vs. Frequency

Figures 15 and 16 show the AD620's gain nonlinearity and small signal pulse response.

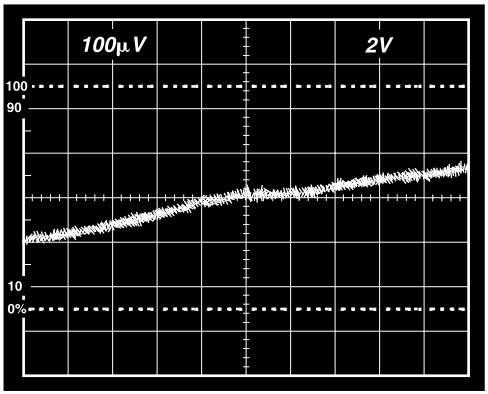


Figure 15. The AD620's Gain Nonlinearity. G = 100, R_L = 10 kΩ, Vert Scale: 100 µV = 10 ppm, Horiz Scale 2 V/Div.

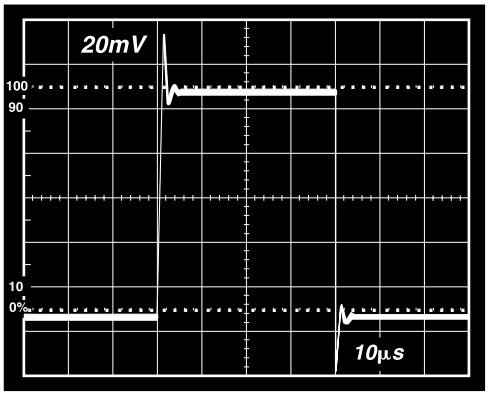


Figure 16. The Small Signal Pulse Response of the AD620. G = 10, R_L= 2 kΩ, C_L = 100 pF.

Finally, the input voltage noise is reduced to a value of 9 nV/√Hz, determined mainly by the collector current and base resistance of the input devices.

The internal gain resistors, R1 and R2 are trimmed to an absolute value of 24.7 kΩ, allowing the gain to be programmed accurately with a single external resistor. The gain equation is then:

$$G = \frac{49.4\ k\Omega}{R_G}$$

So that:

$$R_G = \frac{49.4\ k\Omega}{G - 1}$$

Where resistor R_G is in kΩ.

The value of 24.7 kΩ was chosen so that standard 1% resistor values could be used to set the most popular gains.

The AD620 was the first in a series of high performance, low cost monolithic in-amps. Table III provides a brief comparison of the basic performance of the AD620 in-amp family.

Table III. AD620 Series In-Amps

Model	Max Input Voltage Noise	Max Input Bias Current	Input Stage Operating Current (Typ)
AD620	13 nV/√Hz	2 nA	20 µA
AD621	13 nV/√Hz	2 nA	20 µA
AD622	14 nV/√Hz	5 nA	20 µA
AD623	35 nV/√Hz	25 nA*	1.5 µA
AD627	42 nV/√Hz	10 nA*	0.8 µA

*Note that the AD623 and AD627 are single supply devices. Because of this, they do not include input current compensation in their design.

The **AD622** is a low cost version of the AD620 (see AD620 simplified schematic). The AD622 uses streamlined production methods to provide most of the performance of the AD620, at lower cost.

Figures 17, 18, and 19 show the AD622's CMR vs. frequency, gain nonlinearity, and closed-loop gain vs. frequency.

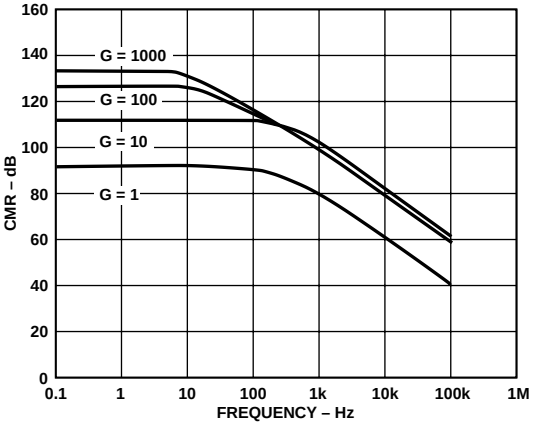


Figure 17. AD622 CMR vs. Frequency (RTI) 0 to 1 kΩ Source Imbalance

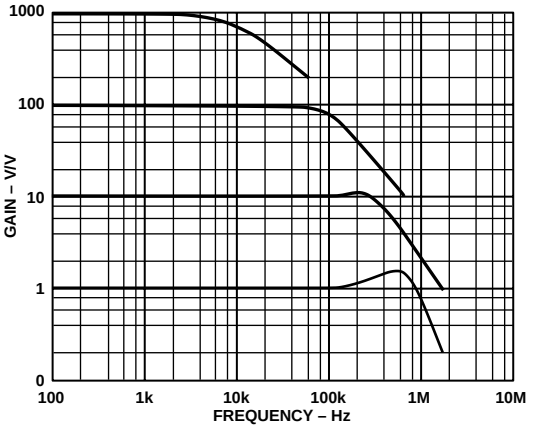


Figure 18. AD622 Closed-Loop Gain vs. Frequency

The **AD621** is also similar to the AD620, except that for gains of 10 and 100, the gain setting resistors are on the die—no external resistors are used. A single external jumper (between Pins 1 and 8) is all that is needed to select a gain of 100. For a gain of 10, leave Pin 1 and Pin 8 open. This provides excellent gain stability over temperature, as the on-chip gain resistor tracks the TC of the feedback resistor. Figure 20 is a simplified schematic of the AD621. With a max total gain error of 0.15% and ±5 ppm/°C gain drift, the AD621 has much greater built-in accuracy than the AD620.

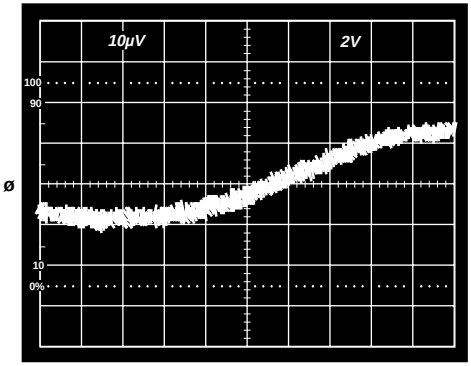


Figure 19. The AD622's Gain Nonlinearity
G = 1, R_L = 10 kΩ, Vert Scale: 20 µV = 2 ppm

The AD621 may also be operated at gains between 10 and 100 by using an external gain resistor, although gain error and gain drift over temperature will be degraded. Using external resistors, device gain is equal to:

$$G = (R1 + R2) / R_G + 1$$

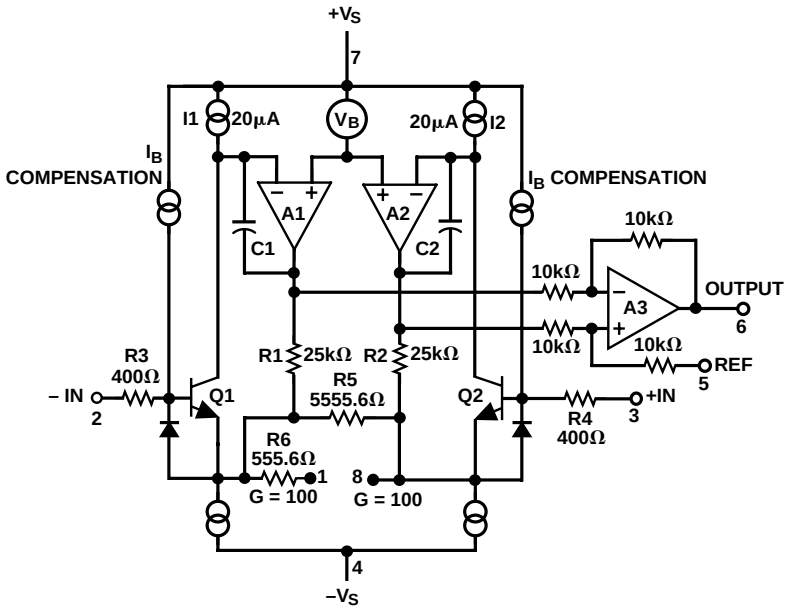


Figure 20. A Simplified Schematic of the AD621

Figures 21 and 22 show the AD621's CMR vs. frequency and closed-loop gain vs. frequency.

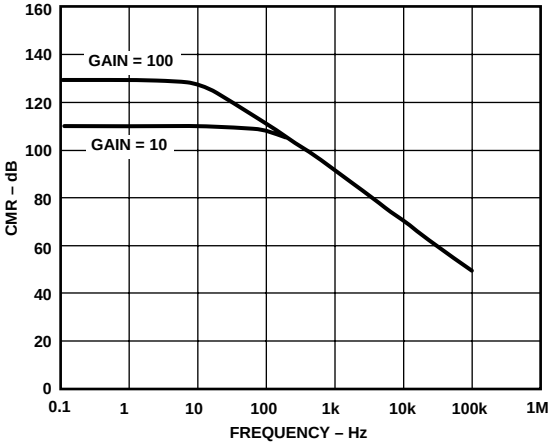


Figure 21. AD621 CMR vs. Frequency.

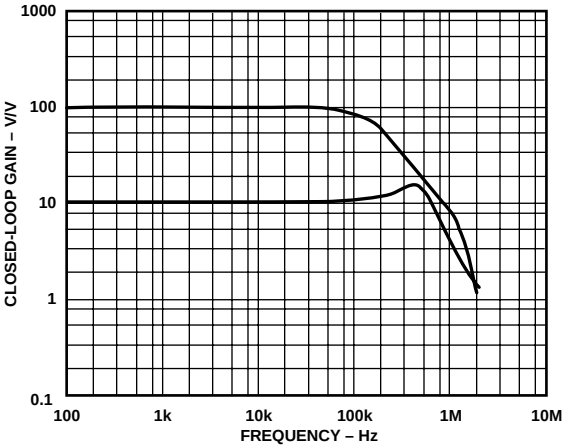


Figure 22. AD621 Closed-Loop Gain vs. Frequency

Figures 23 and 24 show the AD621's gain nonlinearity and small signal pulse response.

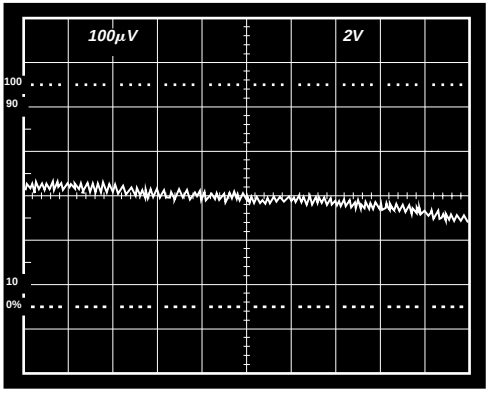


Figure 23. The AD621's Gain Nonlinearity. G = 10, R_L = 10 kΩ, Vert Scale: 100 μV/ Div = 100 ppm/Div, Horiz Scale 2 V/Div.

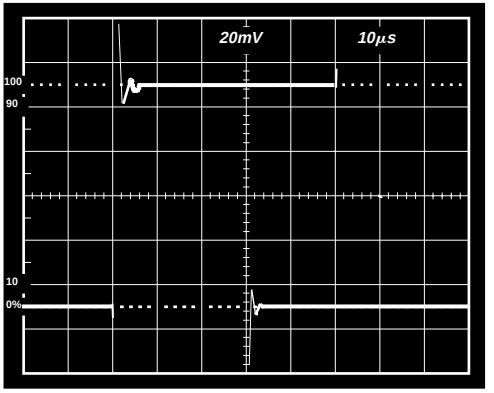


Figure 24. The Small Signal Pulse Response of the AD621. G = 10, R_L = 2 kΩ, C_L = 100 pF.

Monolithic In-Amps Optimized for Single Supply Operation

Single supply in-amps have special design problems that need to be addressed. The input stage needs to be able to amplify signals that are at ground potential (or very close to ground), and the output stage needs to be able to swing to within a few millivolts of ground or the supply rail. Low power supply current is also important. And, when operating from low power supply voltages, the in-amp needs to have an adequate gain-bandwidth product, low offset voltage drift, and good CMR vs. gain and frequency.

The **AD623** is an instrumentation amplifier based on the three op-amp in-amp circuit, modified to assure operation on either single or dual power supplies, even at common-mode voltages at or even below the negative supply rail (or below "ground" in single supply operation). Other features include: rail-to-rail output voltage swing, low supply current, microSOIC packaging, low input and output voltage offset, microvolt/dc offset level drift, high common-mode rejection, and only one external resistor to set the gain.

As shown in Figure 25, the input signal is applied to PNP transistors acting as voltage buffers and dc level-shifters. A resistor trimmed to within 0.1% of 50 kΩ in each amplifiers' (A1 and A2) feedback path assures accurate gain programmability.

The differential output is:

$$V_O = \left(1 + \frac{100\ k\Omega}{R_G}\right) + V_C$$

where R_G is in kΩ.

The differential voltage is then converted to a single-ended voltage using the output difference amplifier, which also rejects any common-mode signal at the output of the input amplifiers.

Since all the amplifiers can swing to either supply rail, as well as have their common-mode range extended to below the negative supply rail, the range over which the AD623 can operate is further enhanced.

Note that the base currents of Q1 and Q2 flow directly "out" of the input terminals, unlike dual supply input-current compensated in-amps such as the AD620. Since the inputs (i.e., the bases of Q1 and Q2) can operate at "ground" i.e., 0 V (or, more correctly, at 200 mV below ground), it was not possible to provide input current compensation for the AD623. However, the input bias current of the AD623 is still very small: only 25 nA max.

The output voltage at Pin 6 is measured with respect to the "reference" potential at Pin 5. The impedance of the reference pin is 100 kΩ. Internal ESD clamping diodes allow the input, reference, output, and gain terminals of the AD623 to safely withstand overvoltages of 0.3 V above or below the supplies. This is true for all gains, and with power on or off. This last case is particularly important since the signal source and the in-amp may be powered separately. If the overvoltage is expected to exceed this value, the current through these diodes should be limited to 10 mA, using external current limiting resistors (see Input Protection section). The value of these resistors is defined by the in-amp's noise level, the supply voltage, and the required overvoltage protection needed.

The bandwidth of the AD623 is reduced as the gain is increased, since A1 and A2 are voltage feedback op-amps. However, even at higher gains, the AD623 still has enough bandwidth for many applications.

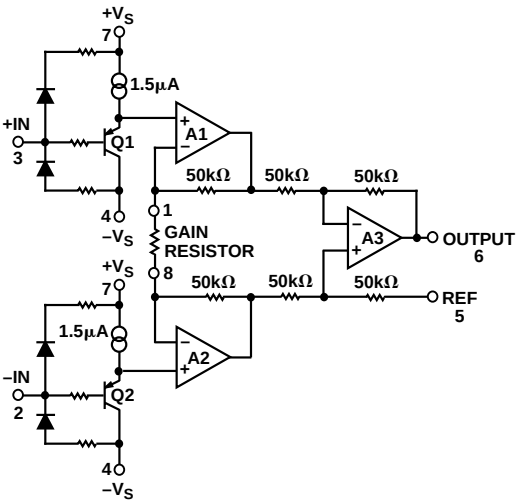


Figure 25. AD623 Simplified Schematic

The AD623's gain is resistor-programmed by R_G or, more precisely, by whatever impedance appears between Pins 1 and 8. Figure 26 shows the gain vs. frequency of the AD623. The AD623 is laser-trimmed to achieve accurate gains using 0.1% to 1% tolerance resistors.

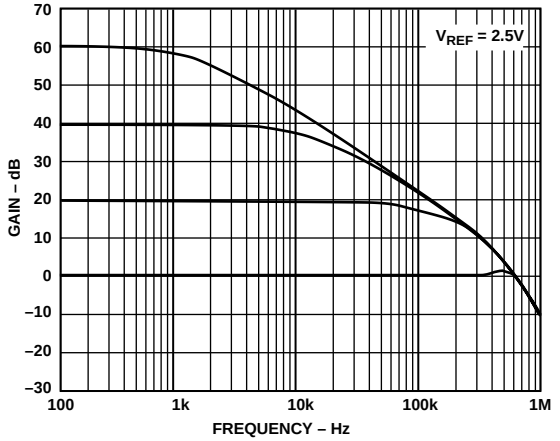


Figure 26. AD623 Closed-Loop Gain vs. Frequency

Table IV. Required Value of Gain Resistor

Desired Gain	1% Std Table Value of R_G, Ω	Calculated Gain Using 1% Resistors
2	100 k	2
5	24.9 k	5.02
10	11 k	10.09
20	5.23 k	20.12
33	3.09 k	33.36
40	2.55 k	40.21
50	2.05 k	49.78
65	1.58 k	64.29
100	1.02 k	99.04
200	499	201.4
500	200	501
1000	100	1001

Table IV shows required values of R_G for various gains. Note that for G = 1, the R_G terminals are unconnected ($R_G = \infty$). For any arbitrary gain, R_G can be calculated by using the formula:

$$R_G = 100\ k\Omega/(G - 1)$$

Figure 27 shows the AD623's CMR vs. Frequency. Note that the CMR increases with gain up to a gain of 100 and that CMR also remains high over frequency, up to 200 Hz. This ensures the attenuation of power line common-mode signals (and their harmonics).

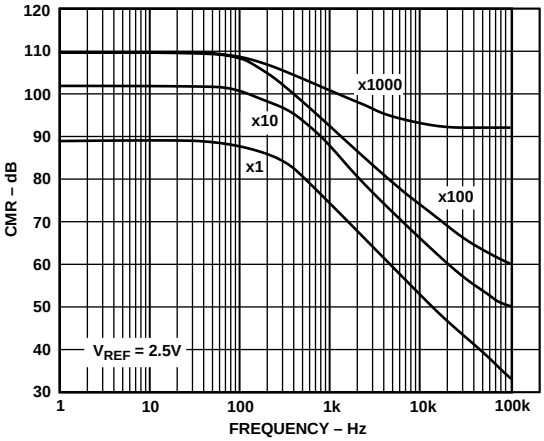


Figure 27. AD623 CMR vs. Frequency, $V_S = \pm 5$ V

The **AD627** is a single supply, micropower instrumentation amplifier that can be configured for gains between 5 and 1,000, using just a single external resistor. It provides a rail-to-rail output voltage swing, using a single +3 V to +30 V power supply. With a quiescent supply current of only 60 μA (typical), its total power consumption is less than 180 μW, operating from a +3 V supply.

Figure 28 shows the gain nonlinearity of the AD623.

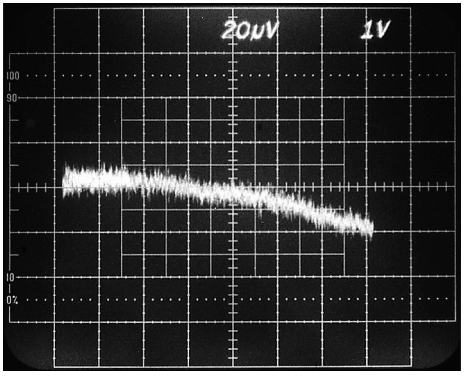


Figure 28. AD623 Gain Nonlinearity. G = –10, 50 ppm/Div

Figure 29 shows the small signal pulse response of the AD623.

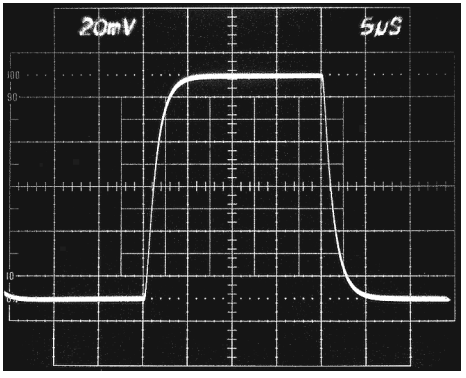


Figure 29. AD623 Small Signal Pulse Response. G = 10, R_L = 10 kΩ, C_L = 100 pF.

Figure 30 is a simplified schematic of the AD627. The AD627 is a true "instrumentation amplifier" built using two feedback loops. Its general properties are similar to those of the classic "two op-amp" instrumentation amplifier configuration, and can be regarded as such, but internally the details are somewhat different. The AD627 uses a modified "current feedback" scheme which, coupled with interstage feedforward frequency compensation, results in a much better CMRR (Common-Mode Rejection Ratio) at frequencies above dc (notably the line frequency of 50 Hz–60 Hz) than might otherwise be expected of a low power instrumentation amplifier.

As shown by Figure 30, A1 completes a feedback loop which, in conjunction with V1 and R5, forces a constant collector current in Q1. Assume that the gain-setting resistor (R_G) is not present for the moment. Resistors R2 and R1 complete the loop and force the output of A1 to be equal to the voltage on the inverting terminal with a gain of (almost exactly) 1.25. A nearly identical feedback loop completed by A2 forces a current in Q2, which is substantially identical to that in Q1, and A2 also provides the output voltage. When both loops are balanced, the gain from the noninverting terminal to V_{OUT} is equal to 5, whereas the gain from the output of A1 to V_{OUT} is equal to –4. The inverting terminal gain of A1, (1.25) times the gain of A2, (–4) makes the gain from the inverting and noninverting terminals equal.

The differential mode gain is equal to 1 + R4/R3, nominally five, and is factory trimmed to 0.01% final accuracy (AD627B typ). Adding an external gain setting resistor (R_G) increases the gain by an amount equal to (R4 + R1)/R_G. The output voltage of the AD627 is given by the following equation.

$$V_{OUT} = [V_{IN}(+) - V_{IN}(-)] \times (5 + 200\ k\Omega/R_G) + V_{REF}$$

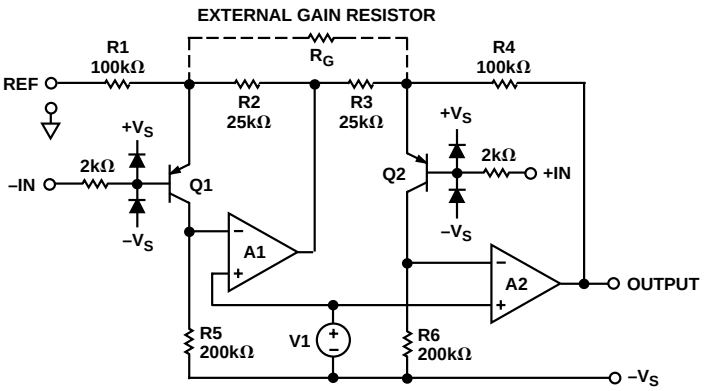


Figure 30. AD627 Simplified Schematic

Laser trims are performed on resistors R1 through R4 to ensure that their values are as close as possible to the absolute values in the gain equation. This ensures low gain error and high common-mode rejection at all practical gains.

Figure 31 shows the AD627's CMR vs. frequency.

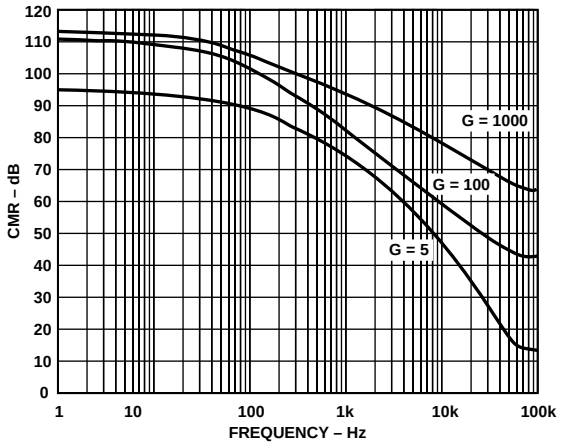


Figure 31. AD627 CMR vs. Frequency

Figures 32 and 33 show the AD627's gain vs. frequency and gain nonlinearity.

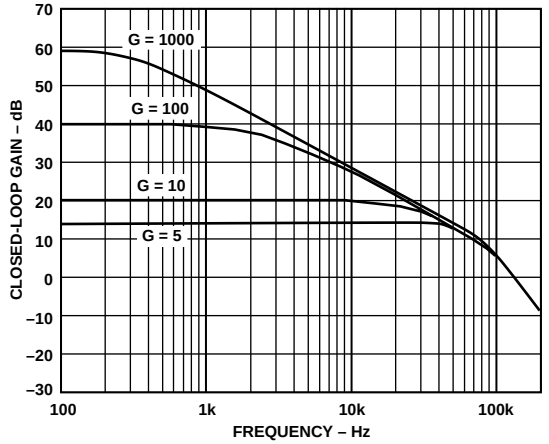


Figure 32. AD627 Closed-Loop Gain vs. Frequency

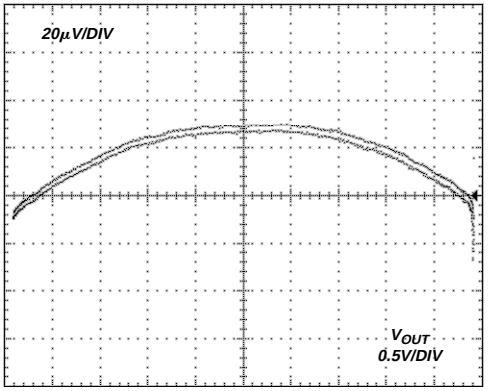


Figure 33. AD627 Gain Nonlinearity. $V_S = \pm 2.5$ V, G = 5

The AD627 also has excellent dynamic response, as shown by Figure 34.

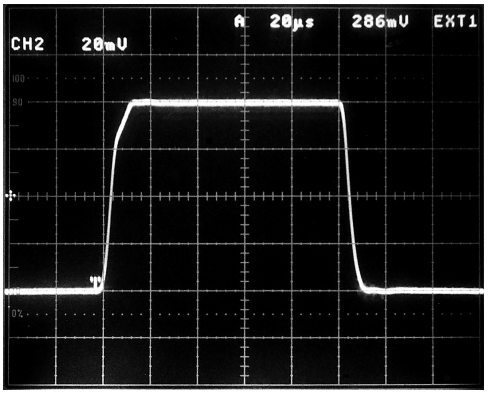


Figure 34. The Small Signal Pulse Response of the AD627. $V_S = \pm 5$ V, G = +10, R_L = 20 kΩ, C_L = 50 pF

Difference (Subtractor) Amplifier Products

The **AMP03** is a monolithic unity-gain, 3 MHz differential amplifier. Incorporating a matched thin-film resistor network, the AMP03 features stable operation over temperature without requiring expensive external matched components. The AMP03 is a basic analog building block for differential amplifier and instrumentation applications (Figure 35).

The differential amplifier topology of the AMP03 serves both to amplify the difference between two signals and to provide extremely high rejection of the common-mode input voltage. With a typical common-mode rejection of 100 dB, the AMP03 solves common problems encountered in instrumentation design. It is ideal for performing either the addition or subtraction of two input signals without using expensive externally-matched

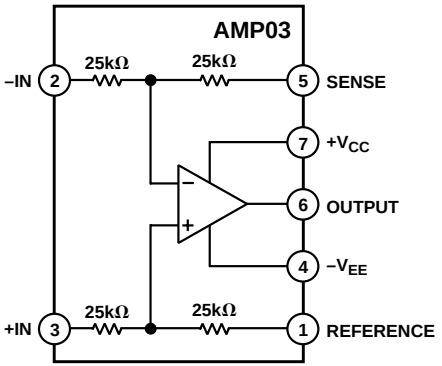


Figure 35. AMP03 Functional Block Diagram

precision resistors. Due to its high CMR over frequency, the AMP03 is an ideal general-purpose amplifier for data acquisition systems that must operate in a noisy environment. Figures 36 and 37 show the AMP03's CMR and closed-loop gain vs. frequency.

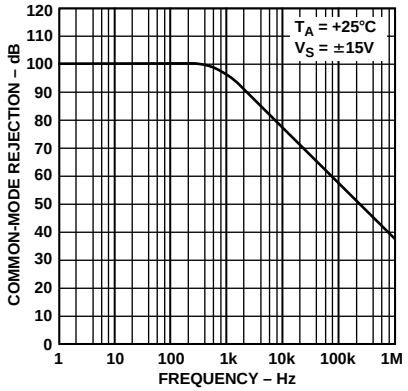


Figure 36. AMP03 CMR vs. Frequency

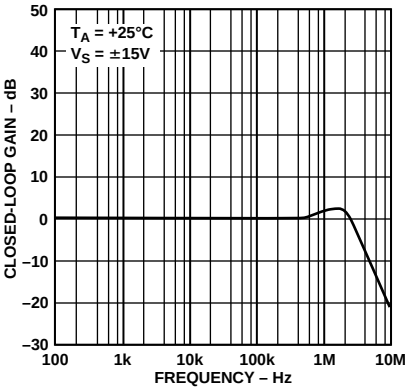


Figure 37. AMP03 Closed-Loop Gain vs. Frequency

Figure 38 shows the small signal pulse response of the AMP03.

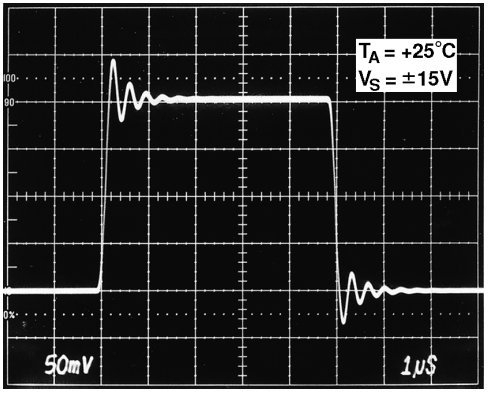


Figure 38. AMP03 Small Signal Pulse Response

The **AD626** is a single or dual supply differential amplifier consisting of a precision balanced attenuator, a very low drift preamplifier (A1), and an output buffer amplifier (A2). It has been designed so that small differential signals can be accurately amplified and filtered in the presence of large common-mode voltages (much greater than the supply voltage) without the use of any other active components.

Figure 39 shows the main elements of the AD626. The signal inputs at Pins 1 and 8 are first applied to dual resistive attenuators R1 through R4 whose purpose is to reduce the peak common-mode voltage at the input to the preamplifier—a feedback stage based on the very low drift op-amp A1. This allows the differential input voltage to be accurately amplified in the presence of large common-mode voltages—six times greater than that which can be tolerated by the actual input to A1. As a result, the input common-mode range extends to six times the quantity (V_S – 1 V). The overall common-mode error is minimized by precise laser-trimming of R3 and R4, thus giving the AD626 a common-mode rejection ratio of at least 10,000:1 (80 dB). The output of A1 is connected to the input of A2 via a 100 kΩ (R12) resistor to facilitate the low-pass filtering of the signal of interest. The AD626 is easily configured for gains of 10 or 100. For a gain of 10, Pin 7 is simply left unconnected; similarly, for a gain of 100, Pin 7 is grounded. Gains between 10 and 100 are easily set by connecting a resistor between Pin 7 and Analog GND. Because the on-chip resistors have an absolute tolerance of ±20% (although they are ratio matched to within 0.1%), at least a 20% adjustment range must be provided. The nominal value for this gain setting resistor is equal to:

$$R = \left(\frac{50,000\,\Omega}{GAIN - 10}\right) - 555\,\Omega$$

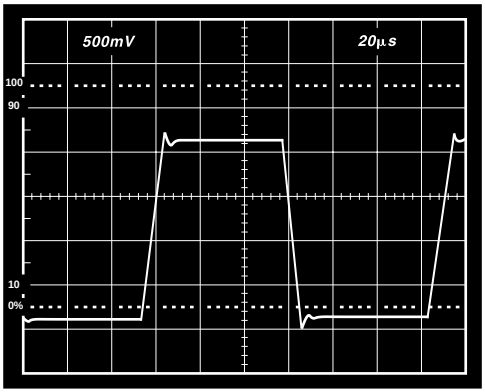


Figure 40. The Large Signal Pulse Response of the AD626. G = 10

Figure 40 shows the large signal pulse response of the AD626.

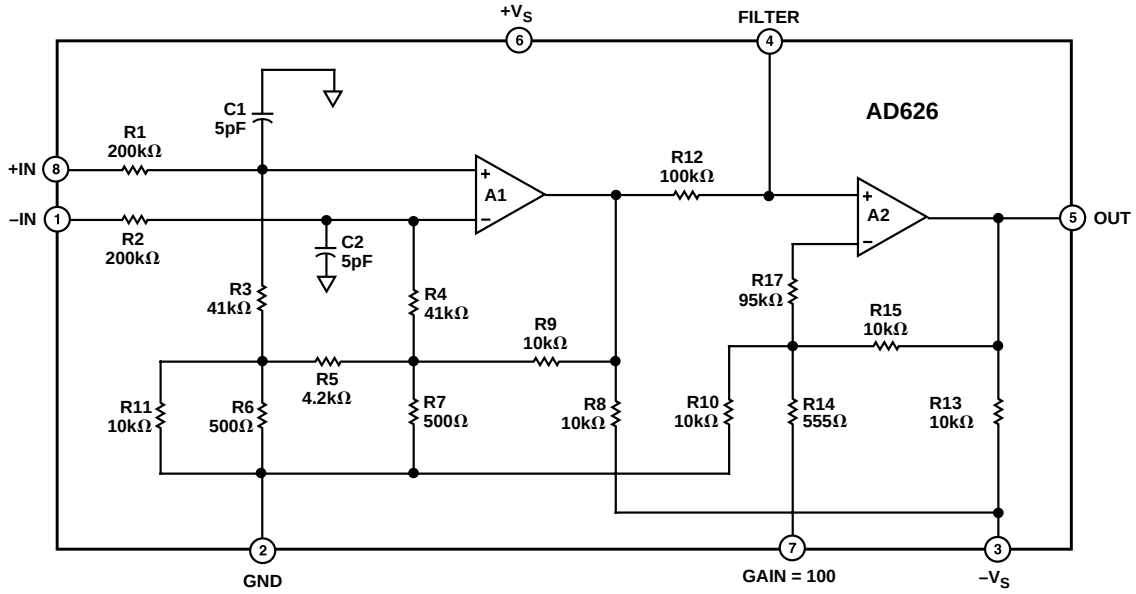


Figure 39. AD626 Simplified Schematic

The **AD629** is a unity gain difference amplifier designed for applications that require the measurement of signals with common-mode input voltages of up to ±270 V. The AD629 has excellent ac and dc specifications that keep errors low when measuring small difference voltages over a wide temperature range. Additionally, the AD629 keeps errors to a minimum by providing excellent CMR in the presence of high common-mode input voltages. Finally, it can operate from a wide power supply range of ±2.5 V to ±18 V.

The AD629 can replace costly isolation amplifiers in applications that do not require galvanic isolation. Figure 41 is the connection diagram of the AD629. Figure 42 shows the AD629's CMR vs. Frequency.

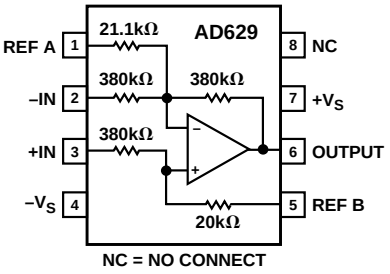


Figure 41. AD629 Connection Diagram

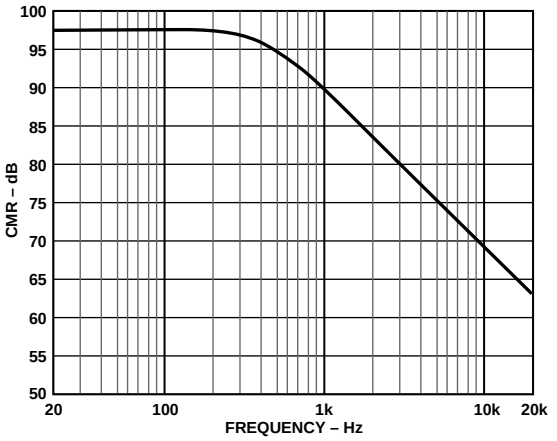


Figure 42. Common-Mode Rejection vs. Frequency

Video Speed In-Amp Products

The **AD830** is a wideband, differencing amplifier designed for general purpose signal processing from dc to 10 MHz (Figure 43). High impedance inputs ease interfacing to finite source impedances and thus preserve its excellent common-mode rejection. In many respects, such as high frequency common-mode rejection, it offers significant improvements over discrete difference amplifier designs.

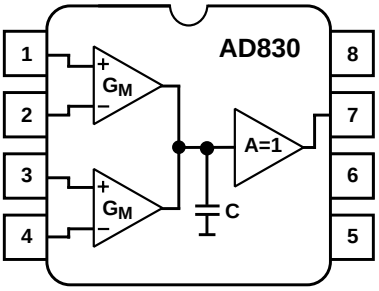


Figure 43. AD830 Connection Diagram

The AD830 uses an active feedback topology to provide inherent advantages in the handling of differential signals, differing system commons, level-shifting and low distortion, high frequency amplification.

The AD830's topology, reduced to its elemental form, is shown in Figure 44. The key feature of this topology is the use of two identical voltage-to-current converters, G_M, that make up the input and feedback signal interfaces. They are labeled with inputs V_X and V_Y, respectively. These voltage-to-current converters possess fully differential inputs, high linearity, high input impedance and wide voltage range operation.

The two G_M stage current outputs I_X and I_Y, sum together at a high impedance node that is characterized by an equivalent resistance and capacitance connected to an "ac common." A unity voltage gain stage follows the high impedance node, to provide buffering from loads.

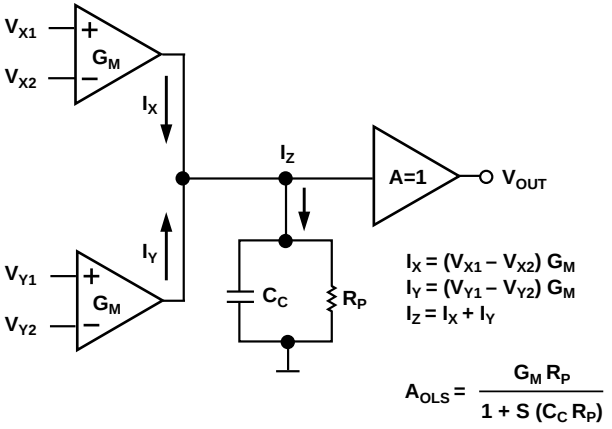


Figure 44. Topology Diagram

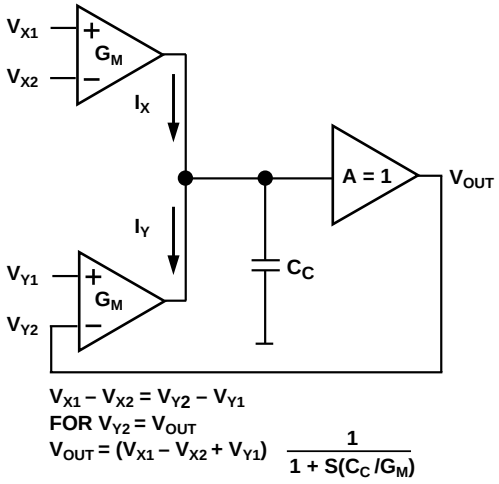


Figure 45. Closed-Loop Connection

Precise amplification is accomplished through closed-loop operation of this topology. Voltage feedback is implemented via the Y G_M stage in which the output is connected to the –Y input for negative feedback as shown in Figure 45. An input signal is applied across the X G_M stage, either differentially or single-ended, which produces a current that is summed at the high impedance node with the output current from the Y G_M stage.

Negative feedback nulls this sum to a small error current necessary to develop the output voltage at the high impedance node. The error current is usually negligible, so the null condition essentially forces the Y G_M output stage current to exactly equal the X G_M output current.

Since the two transconductances are identical, the differential voltage across the Y inputs equals the negative of the differential voltage across the X input. It is important to note that the bandwidth and general dynamic behavior is symmetrical (identical) for the noninverting and the inverting connections of the AD830.

Figures 46 and 47 show the AD830's CMR vs. frequency and normalized gain vs. frequency.

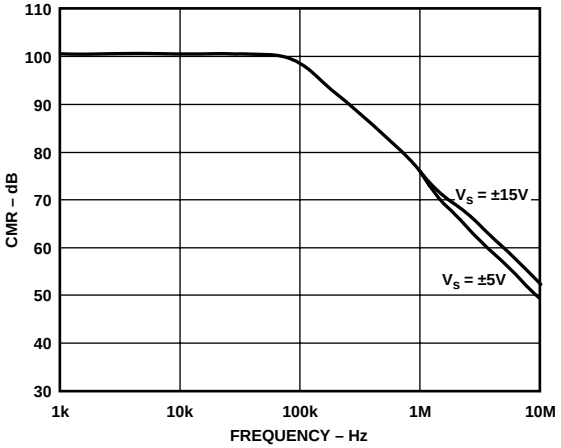


Figure 46. AD830 CMR vs. Frequency

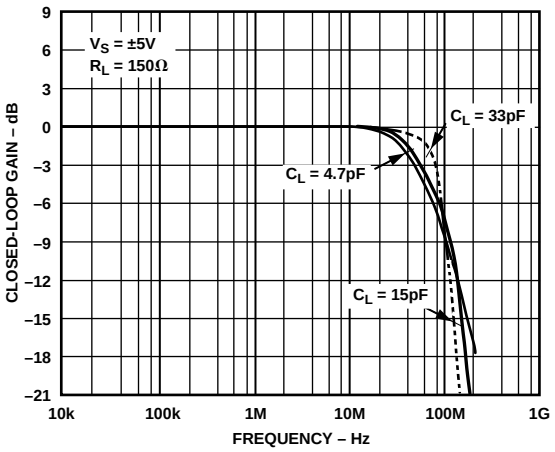


Figure 47. AD830 Closed-Loop Gain vs. Frequency

For details concerning the entire line of monolithic in-amps produced by Analog Devices, refer to Appendix B.

Chapter III

Applying In-Amps Effectively

DUAL SUPPLY OPERATION

The conventional way to power an in-amp has been from a "split" or dual polarity power supply. This has the obvious advantage of allowing both a positive and a negative input and output swing.

SINGLE SUPPLY OPERATION

Single supply operation has become an increasingly desirable characteristic of a modern in-amp. Many present-day data acquisition systems are powered from a single low voltage supply. For these systems, there are two vitally important characteristics. The first is that the in-amp's input common-mode range should extend between the positive supply and the negative supply (or ground). Second, the amplifier's output should be "rail-to-rail" as well, providing an output swing to within 100 mV or less of either supply rail or ground. In contrast, a standard dual supply in-amp can only swing to within a volt or two of either supply or ground. When operated from a 5 V single supply, these in-amps have only a volt or two of output voltage swing, while a true rail-to-rail amplifier can provide a peak-to-peak output nearly as great as the supply voltage. Another important point is that a single supply or "rail-to-rail" in-amp will still operate well (or even better) from a dual supply and it will often operate at lower power than a conventional dual supply device.

POWER SUPPLY BYPASSING, DECOUPLING AND STABILITY ISSUES

Power supply decoupling is an important detail that is often overlooked by designers. Normally, bypass capacitors (values of 0.1 μF are typical) are connected between the power supply pins of each IC and ground. While usually adequate, this practice can be ineffective or even create worse transients than no bypassing at all. It is important to consider where the circuit's currents originate, where they will return, and by what path. Once that has been established, bypass these currents around ground and other signal paths.

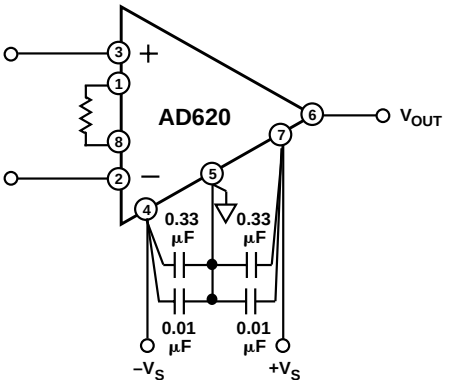


Figure 48. Recommended Method for Power Supply Bypassing

In general, most monolithic in-amps have their integrators referenced to the negative supply (such as the AD620 in-amp series) and should be decoupled with respect to the output reference terminal. This means that for each chip a bypass capacitor should be connected between each power supply pin and the point on the board where the in-amp's reference terminal is connected, as shown in Figure 48.

For a much more comprehensive discussion of these issues refer to the application note: "An I.C. Amplifier Users' Guide to Decoupling, Grounding, and Making Things Go Right for a Change," by Paul Brokaw, available free from Analog Devices.

THE IMPORTANCE OF AN INPUT GROUND RETURN

One of the most common applications problems when using in-amp circuits is failure to provide a dc return path for the in-amp's input bias currents. This usually happens when the in-amp's inputs are capacitively-coupled. Figure 49a shows just such an arrangement. Here the input bias currents quickly "charge up" capacitors C1 and C2 until the in-amp's output "rails" either to the supply or ground.

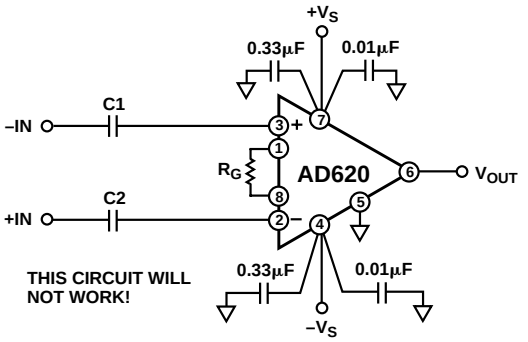


Figure 49a. An AC-Coupled In-Amp Circuit Without An Input Ground Return

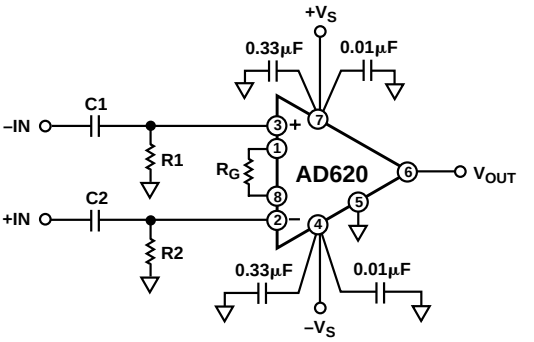


Figure 49b. A High Value Resistor Between Each Input and Ground Provides an Effective DC Return Path

The solution is to add a high value resistance (R1, R2) between each input and ground, as shown in Figure 49b. Practical values for R1 and R2 are typically 1 MΩ or less. The choice of resistor value is a trade-off: the larger the resistor, the greater the offset voltage error due to input offset currents. With lower resistance values, larger input capacitors must be used for C1 and C2 to provide the same 3 dB corner frequency ($1/2\pi R1C1$) where $R1 = R2$ and $C1 = C2$. The input bias currents can now flow freely to ground and do not build up a large input offset as before. In the vacuum tube circuits of years past, a similar effect occurred, requiring a "grid leak" resistance between the grid (input) and ground to drain off the accumulated charge (the electrons on the grid).

Figure 50 shows the recommended dc return for a transformer-coupled input.

CABLE TERMINATION

When in-amps are used at frequencies above a few hundred kilohertz, properly terminated 50 Ω or 75 Ω coaxial cable should be used for input and output connections. Normally, cable termination is simply a 50 Ω or 75 Ω resistor connected between the cable center conductor and its shield at the end of the coaxial cable. Note that a buffer amplifier may be required to drive these loads to useful levels.

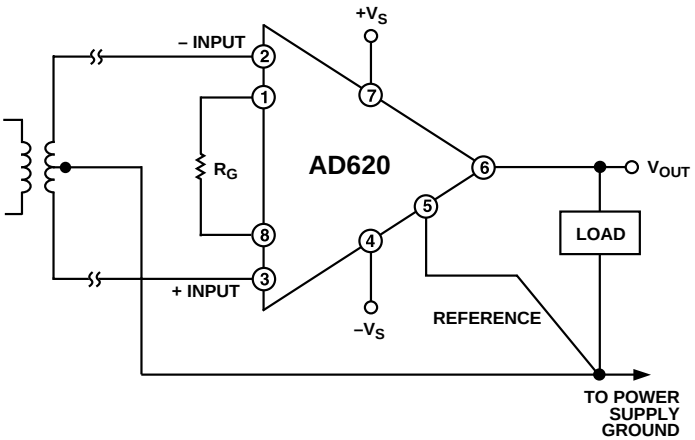


Figure 50. Recommended DC Return Path For A Transformer Coupled Input

INPUT PROTECTION BASICS FOR ADI IN-AMPS

Input Protection from ESD and DC Overload

As interface amplifiers for data acquisition systems, instrumentation amplifiers are often subjected to input overloads, i.e., voltage levels in excess of their full scale for the selected gain range or even in excess of the supply voltage. These overloads fall into two general classes: those that are steady state and those that are transient (ESD, etc.), which occur for only a fraction of a second. With three op-amp in-amp designs, when operating at low gains (10 or less), the gain resistor acts as a current-limiting element in series with their resistor inputs. At high gains, the lower value of R_G may not adequately protect the inputs from excessive currents.

Standard practice is to place current-limiting resistors in each input, but adding this protection also increases the circuit's noise level. A reasonable "balance" needs to be found between the protection provided and the increased resistor (Johnson) noise introduced. Circuits using in-amps with a relatively high noise level can tolerate more series protection without seriously increasing their total circuit noise.

Of course, the less added noise the better, but a good rule of thumb is that circuits needing this extra protection can easily tolerate resistor values that generate 30% of the total circuit noise. For example, a circuit using an in-amp with a rated noise level of 20 nV/$\sqrt{\text{Hz}}$ can tolerate an additional 6 nV/$\sqrt{\text{Hz}}$ of Johnson noise.

A "cookbook" method to translate this number into a practical resistance value follows. The Johnson noise of a 1 kΩ resistor is approximately 4 nV/$\sqrt{\text{Hz}}$. Now, this value varies as the square root of the resistance. So a 20 kΩ resistor would have $\sqrt{20}$ times as much noise as the 1 kΩ resistor, which is 17.88 nV/$\sqrt{\text{Hz}}$ (4.4721 times 4 nV/$\sqrt{\text{Hz}}$). Because *both* inputs need to be protected, two resistors are needed and their combined noise will add as the square root of the number of resistors (the root sum of squares value). In this case, the total added noise from the two 20 kΩ resistors will be 25.3 nV/$\sqrt{\text{Hz}}$ (17.88 times 1.414).

Figure 51a provides details on the input architecture of the AD620 series in-amps. As shown, the AD620 series has internal 400 Ω resistors that are in series with the input transistor junctions and their protection diodes. The AD620 series was designed to handle maximum input currents of 20 mA steady state (or dc). Their internal resistors and diodes will protect the device from input voltages 8 volts greater than either supply voltage (20 mA × 0.4 kΩ). Therefore, for ±15 volts supplies, the maximum safe input level is ±23 volts. Additional external series resistors can be added to increase this level considerably, at the expense of a higher circuit noise level.

Because the AD620 series in-amps are very low noise devices, typically 9 nV/$\sqrt{\text{Hz}}$, a single 1 kΩ resistor will add approximately 1.7 nV/$\sqrt{\text{Hz}}$ of noise. This would raise the maximum dc input level to approximately 28 volts above each supply or ±43 volts with 15 volt supplies.

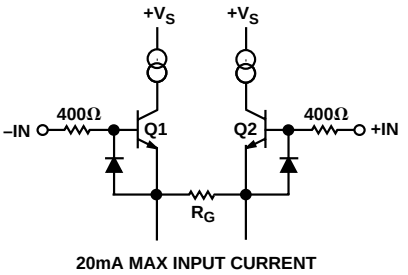


Figure 51a. AD620 Series (AD620, AD621, AD622) In-Amp Input Circuit

Figure 51b shows the input architecture for the AD627 in-amp. This two op-amp in-amp design was optimized for the lowest possible operating current consistent with good performance. Because of this, the input stage operates at lower current levels than the AD620 series and, as a consequence, is higher in noise.

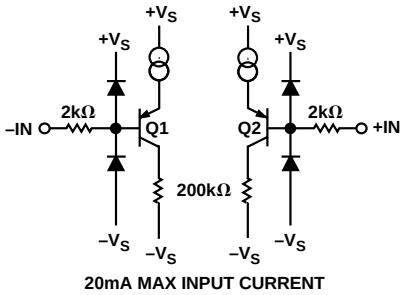


Figure 51b. AD627 In-Amp Input Circuit

Like the AD620 series, the AD627 can tolerate 20 mA transient input currents. But the AD627 has built-in 2 kΩ resistors and can handle input voltages 40 volts higher than its supply lines (20 mA times 2 kΩ). This level of protection is quite beneficial since, because of its low power, many of the AD627's applications will use a low voltage single power supply. If even more protection is needed, quite large external resistors can be added without seriously degrading the AD627's

38 nV/√Hz noise level. In this case, adding two 5 kΩ resistors will raise the circuits noise approximately 13 nV/√Hz (30 percent) but would provide an additional ±100 volts of transient overload protection.

Figure 51c shows the input architecture of the AD623 in-amp. In this design, the internal (ESD) diodes are located *before* the input resistors and as a consequence, this provides less protection than the other designs. The AD623 can tolerate 10 mA maximum input current but, in many cases, some external series resistance will be needed to keep input current below this level.

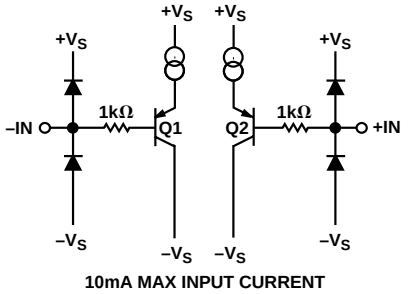


Figure 51c. AD623 In-Amp Input Circuit

Since the AD623's device noise is approximately 35 nV/√Hz, up to 5 kΩ of external resistance can be added here to provide 50 V of dc overload protection while only increasing input noise to 38 nV/√Hz total.

Table V provides recommended series protection resistor values for a 10% or 40% increase in circuit noise.

Table V. Recommended Series Protection Resistor Values

Device	In-Amp Noise (eni)	Max Input Overload Current	External Resistors Recommended* For 10% Additional Noise (Ω)	For 40% Additional Noise (kΩ)
AD620	9 nV/√Hz	20 mA	348	2.49
AD627	38 nV/√Hz	20 mA	10.0 k	45.3
AD627	35 nV/√Hz	10 mA	8.08 k	40.2

*This noise level is for two resistors, one in series with each input of the in-amp.

Adding External Protection Diodes

Device input protection may be increased with the addition of external clamping diodes as shown in Figure 52. As high current diodes are used, input protection is increased which allows the use of much lower resistance input protection resistors which, in turn, reduces the circuit's noise.

Unfortunately, most ordinary diodes (Schottky, silicon, etc.) have high leakage currents that will cause large offset errors at the in-amp's output; this leakage increases exponentially with temperature. This tends to rule out the use of external diodes in applications where the in-amp is used with high impedance sources. Specialty diodes with much lower leakage are available, but these are often difficult to find and expensive. For the vast majority of applications, limiting resistors alone provides adequate protection for ESD and longer duration input transients.

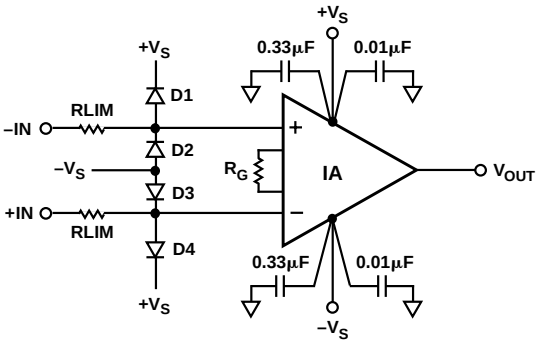


Figure 52. Using External Components to Increase Input Protection

Despite their limitations, external diodes are often required in some special applications such as electric shock defibrillators, which utilize short duration, high voltage pulses. The combination of external diodes and very large input resistors (as high as 100 kΩ) may be needed to adequately protect the in-amp.

It is a good idea to check the diodes' specifications, to ensure that their conduction begins well before the in-amp's internal protection diodes start drawing current. Although they provide excellent input protection, standard Schottky diodes can have leakage up to several mA. However, as in the example of Figure 52, fast Schottky barrier rectifiers such as the international rectifier type SD101 series can be used; these devices have 200 nA max leakage currents and 400 mW typical power dissipations.

ESD and Transient Overload Protection

Protecting in-amp inputs from high voltage transients and ESD events is all-important for a circuit's long-term reliability. Power dissipation is often a critical factor as input resistors, whether internal or external, must be able to handle most of the power of the input pulse without failing.

ESD events, while they may be very high voltage, are usually of very short duration and are normally one-time events. Since the circuit has plenty of time to cool down before the next event occurs, modest input protection is sufficient to protect the device from damage.

On the other hand, regularly occurring short duration input transients can easily overheat and burn out the input resistors or the in-amps input stage. A 1 kΩ resistor, in series with an in-amp input terminal drawing 20 mA, will dissipate 0.4 watts which can easily be handled by a standard one-half watt or greater surface mount resistor. If the input current is doubled, power consumption goes up 4×, as it increases as the square of the input current (or as the square of the applied voltage).

Although it is a simple matter to use a higher power protection resistor, this is a dangerous practice, as the power dissipation will also increase in the in-amp's input stage. This can easily lead to device failure (see the preceding section on input protection basics for input current limitations of ADI in-amps). Except for ESD events, it is always best to adopt a conservative approach and treat all transient input signals as full duration inputs.

Designs that are expected to survive such events over long periods of time, must use resistors with enough resistance to protect the in-amp's input circuitry from failure and enough power to prevent resistor burnout.

DESIGN ISSUES AFFECTING DC ACCURACY

The modern in-amp is continually being improved, providing the user with ever-increasing accuracy and versatility at a lower price. Despite these improvements in product performance, there remain some fundamental applications issues that seriously affect device accuracy. Now that low cost high resolution ADCs are in common use, system designers need to ensure that if an in-amp is used as a preamplifier ahead of the converter, that the in-amp's accuracy matches that of the ADC.

Designing For the Lowest Possible Offset Voltage Drift

Offset drift errors include not just those associated with the active device (IC in-amp or discrete in-amp design using op-amps) being used, but also include thermocouple effects in the circuit's components or wiring. The in-amp's input bias and input offset currents flowing through unbalanced source impedances also create additional offset errors. In discrete op-amp in-amp designs, these errors can increase with temperature unless precision op-amps are used.

Designing For the Lowest Possible Gain Drift

When planning for gain errors, the effects of board layout, the circuit's thermal gradients, and the characteristics of any external gain-setting resistors are often overlooked. A gain resistor's absolute tolerance, its thermal temperature coefficient, its physical position relative to other resistors in the same gain network, and even its physical orientation (vertical or horizontal), are all-important design considerations if high dc accuracy is needed.

In many ADC preamp circuits, an external user-selected resistor sets the gain of the in-amp, so the absolute tolerance of this resistor and its variation over temperature, compared to that of the IC's on-chip resistors, will affect the circuit's gain accuracy. Resistors commonly used include through-hole 1% 1/4 watt metal film types and 1% 1/8th watt chip resistors. Both types typically have a 100 ppm/°C temperature coefficient. However, some chip resistors can have TCs of 200 or even 250 ppm/°C.

Even when using a 1% 100 ppm/°C resistor, the gain accuracy of the in-amp will be degraded. The resistor's initial room temperature accuracy is only ±1% and the resistor will drift another 0.01% (100 ppm/°C) for every degree C change in temperature. The initial gain error can easily be subtracted-out in software, but to correct for the error vs. temperature, frequent recalibrations (and a temperature sensor) would be required.

If the circuit is initially calibrated, the overall gain accuracy is reduced to approximately 10 bits (0.1%) accuracy for a 10°C change. An in-amp with a standard 1% metal film gain resistor should never be used ahead of even a 12-bit converter and it would totally destroy the accuracy of a 14- or 16-bit converter.

Additional error sources associated with external resistors also affect gain accuracy. The first are variations in resistor heating caused by input signal level. Figure 53, a simple op-amp voltage amplifier, provides a practical example.

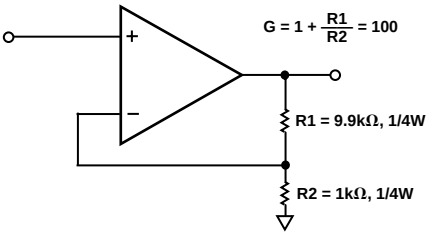


Figure 53. An Example of How Differences In Input Signal Level Can Introduce Gain Errors

Under zero signal conditions, there is no output signal and no resistor heating. When an input signal is applied, however, an (amplified) voltage appears at the op-amp output. When the amplifier is operating with gain, Resistor R1 will now be greater than R2. This means that there will be more voltage across R1 than across R2. The power dissipated in each resistor equals the square of the voltage across it divided by its resistance in ohms. The power dissipated, and therefore the internal heating of the resistor, will increase in proportion to the value of the resistor.

In the example, R1 is 9.9 kΩ and R2 1 kΩ. Consequently, R1 will dissipate 9.9 times more power than R2. This leads to a gain error that will vary with input level. The use of resistors with different temperature coefficients can also introduce gain errors.

Even when resistors with matched temperature coefficients (TC) are used, gain errors that vary with input signal level can still occur. The use of larger (i.e., higher power) resistors will reduce these effects but accurate, low TC power resistors are expensive and hard to find.

When using a discrete three op-amp in-amp, as shown in Figure 54, these errors will be reduced. In a three op-amp in-amp, there are two feedback resistors, R1 and R2, and one gain resistor, R_G. Since the in-amp uses two feedback resistors while the op-amp uses only one, each of the in-amp's resistors only needs to dissipate half the power (for the same gain). Monolithic in-amps such as the AD620 offer a further advantage by using relatively large value (25 kΩ) feedback resistors. For a given gain and output voltage, large feedback resistors will dissipate less power (i.e., $P = V^2/R_F$). Of course, a discrete in-amp can be designed to use large value, low TC resistors as well, but with added cost and complexity.

Another less serious, but still significant, error source is the so-called "thermocouple effect" sometimes referred to as "thermal EMF." This occurs when two different conductors, such as copper and metal film, are tied together. When this bimetallic junction is heated, a simple thermocouple is created. When using similar metals such as a copper-to-copper junction, a thermoelectric error voltage of up to 0.2 mV/°C may be produced. An example of these effects is shown in Figure 55.

A final error source occurs when there is a thermal gradient across the external gain resistor. Something as simple as mounting a resistor on end, in order to conserve board space, will invariably produce a temperature gradient across the resistor. Placing the resistor flat down against the PC board will cure this problem unless there is air flowing along the axis of the resistor (where the air flow cools one side of the resistor more

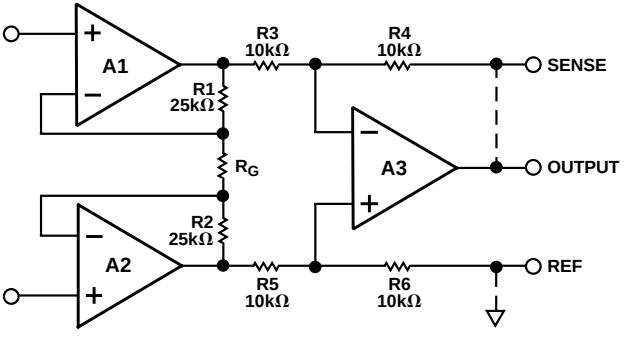
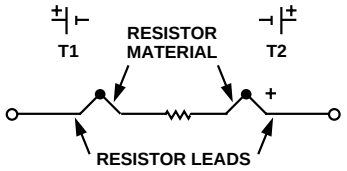


Figure 54. A Typical Discrete Three Op-Amp In-Amp Using Large Value, Low TC Feedback Resistors

than the other side). Orienting the resistor so that its axis is perpendicular to the airflow will minimize this effect.



TYPICAL RESISTOR THERMOCOUPLE EMFs	
• CARBON COMPOSITION	400μV/°C
• METAL FILM	20μV/°C
• EVENOHM OR MANGANIN WIRE-WOUND	2μV/°C
• RCD COMPONENTS HP-SERIES	0.05μV/°C

Figure 55. Thermocouple Effects Inside Discrete Resistors

Practical Solutions

As outlined, a number of dc offset and gain errors are introduced when external resistors are used with a monolithic in-amp. And discrete designs tend to have even larger errors. There are three practical solutions to this problem: use higher quality resistors, use software correction, or, better still, use an in-amp that has *all* of its gain resistors on-chip, such as the AD621.

Option 1: Use A Better Quality Gain Resistor

As a general rule, only 12- or 13-bit gain performance is possible using commonly available 1% resistors, which assumes that some type of initial calibration is performed.

A practical solution to this problem is simply to use a better quality resistor. A significant improvement can be made by using a 0.1% 1/10th watt surface mount resistor. Aside from having a 10× better initial accuracy, they typically have a TC of only 25 ppm/°C which will provide better than 13-bit accuracy over a 10°C temperature range.

If even better gain accuracy is needed, there are specialty houses that sell resistors with lower TCs, but these are usually expensive military varieties.

Option 2: Use The AD621

By far, the best overall dc performance is provided by using a monolithic in-amp such as the AD621 in which *all* the resistors are contained within the IC and gain is pin programmable. Now, all resistors have identical TCs, all are at virtually the same temperature, and any thermal gradients across the chip are very small and gain error drift is guaranteed and specified to very high standards.

At a gain of 10, the AD621 has a guaranteed maximum dc offset shift of less than 2.5 μV/°C and a maximum gain drift of ± 5 ppm/°C, which is only 0.0005 percent/°C.

RTI and RTO Errors

Another important design consideration is how circuit gain affects many in-amp error sources such as dc offset and noise. An in-amp should be regarded as a two stage amplifier with both an input and an output section. Each section has its own error sources.

Because the errors of the output section are multiplied by a fixed gain (usually two), this section is often the principle error source at low circuit gains. When the in-amp is operating at higher gains, the gain of the input stage is increased. As the gain is raised, errors contributed by the input section are multiplied, while output errors are not. So, at high gains it is the input stage errors that dominate.

Since device specifications on different data sheets often refer to different types of errors, it is *very* easy for the unwary designer to make an inaccurate comparison between products. Any (or several) of four basic error categories may be listed: input errors, outputs errors, total error RTI and total error RTO. Here follows an attempt to list, and hopefully simplify, an otherwise complicated set of definitions.

Input errors are those contributed by the amplifier's input stage alone; output errors are those due to the output section. Input-related specifications are often combined and classified together as a "referred to input" (RTI) error while all output-related specifications are considered "referred to output" (RTO) errors.

For a given gain, an in-amp's input and output errors can be calculated by using the following formulas:

$$\textit{Total Error, RTI} = \textit{Input Error} + (\textit{Output Error}/\textit{Gain})$$

$$\textit{Total Error, RTO} = (\textit{Gain} \times \textit{Input Error}) + \textit{Output Error}$$

Sometimes the spec page will list an error term as RTI or RTO for a specified gain, in other cases it is up to the user to calculate the error for the desired gain.

Offset Error

Using offset error as an example, the total voltage offset error of the AD620A in-amp when operating at a gain of ten can be calculated using the individual errors listed on its specifications page. The (typical) input offset of the AD620 (V_{OSI}), is listed as 30 μV. Its output

offset (V_{OSO}) is listed as 400 μV. Thus, the total voltage offset referred to input, RTI, is equal to:

Total RTI Error = V_{OSI} + (V_{OSO}/*G*) = 30 μ*V* + (400 μ*V*/10) = 30 μ*V* + 40 μ*V* = 70 μ*V*.

The total voltage offset referred to the output, RTO, is equal to:

Total Offset Error RTO = (*G* (V_{OSI})) + V_{OSO} = (10 (30 μ*V*)) + 400 μ*V* = 700 μ*V*.

Note that the two error numbers (RTI vs. RTO) are 10× in value and logically they should be, as, at a gain of ten, the error at the output of the in-amp should be ten times the error at its input.

Noise Errors

In-amp noise errors also need to be considered in a similar way. Since the output section of a typical three op-amp in-amp operates at unity gain, the noise contribution from the output stage is usually very small. But there are three op-amp in-amps that operate the output stage at higher gains and two op-amp in-amps regularly operate the second amplifier at gain. When either section is operated at gain, its noise is amplified along with the input signal. Both RTI and RTO noise errors are calculated the same way as offset errors except that the noise of two sections adds as the root-mean-square. That is:

$$Input\ Noise = eni, Output\ Noise = eno$$

$$Total\ Noise\ RTI = \sqrt{\left(eni\right)^2 + \left(eno/Gain\right)^2}$$

$$Total\ Noise\ RTO = \sqrt{\left(Gain\left(eni\right)\right)^2 + \left(eno\right)^2}$$

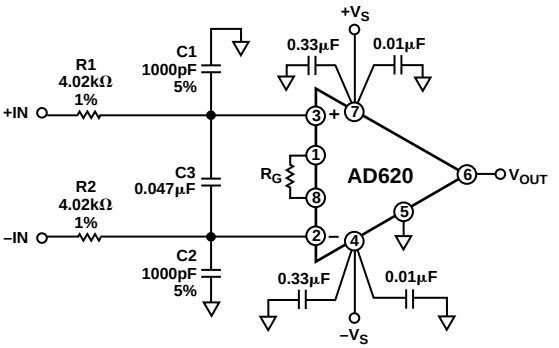
For example, the (typical) noise of the AD620A is specified as 9 nV/√Hz eni and 72 nV/√Hz eno. Therefore, the total RTI noise of the AD620A operating at a gain of 10 is equal to:

$$Total\ Noise\ RTI = \sqrt{\left(eni\right)^2 + \left(eno/Gain\right)^2} =$$

$$\sqrt{\left(9\right)^2 + \left(72/10\right)^2} = 11.5\,nV/\sqrt{Hz}$$

Reducing Errors Due to Radio Frequency Interference

In real-world applications, a potential problem is that of radio frequency interference (RFI) finding its way into the in-amp being rectified, and then appearing as a dc offset error at the in-amp's output. Common-mode signals present at the in-amp's input are normally greatly reduced by the amplifier's common-mode rejection but, at RF frequencies, most in-amps have no common-mode rejection. If the RF interference is modulated, keyed, or otherwise of an intermittent nature, this dc offset can vary over time and lead to measurement errors that are difficult to detect.



LOCATE C1–C3 AS CLOSE TO THE INPUT PINS AS POSSIBLE. USE SHORT LEADS AND A GROUND PLANE ON THE PC BOARD.

Figure 56. A Practical RFI Suppression Circuit For the AD620 In-Amp

The circuit of Figure 56 is recommended for AD620 series in-amps and provides good RFI suppression at the expense of reducing the (differential) bandwidth. In addition, this RC input network also provides additional input overload protection (see input protection section). Resistors R1 and R2 were selected to be high enough in value to isolate the circuit's input from capacitors C1–C3, but without significantly increasing the circuit's noise.

R1/R2 and C1/C2 form a bridge circuit whose output appears across the in-amp's input pins. Any mismatch between the C1/R1 and C2/R2 time constant will unbalance the bridge and reduce common-mode rejection. C3 ensures that any RF signals are common-mode (the same on both in-amp inputs) and are not applied differentially.

This low-pass network has a –3 dB BW equal to:

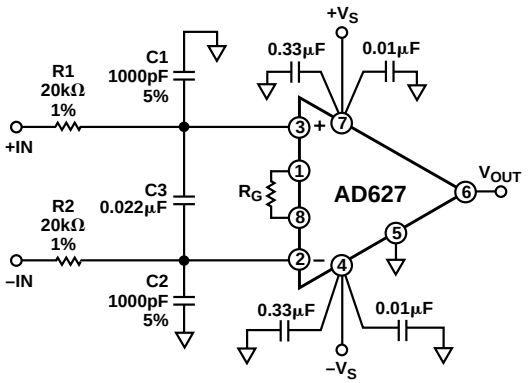
$$\frac{1}{\left(2\pi\left(R1 + R2\right)\left(C3 + C1 + C2\right)\right)}.$$

Using a C3 value of 0.047 μF as shown, the –3 dB signal BW of this circuit is approximately 400 Hz. When operating at a gain of 1000, the typical dc offset shift over a frequency range of 1 Hz to 20 MHz will be less

than 1.5 µV RTI and the circuit's RF signal rejection will be better than 71 dB. At a gain of 100, the dc offset shift is well below 1 mV RTI and RF rejection better than 70 dB.

The 3 dB signal bandwidth of this circuit may be increased to 900 Hz by reducing resistors R1 and R2 to 2.2 kΩ. The performance is similar to that using 4 kΩ resistors, except that the circuitry preceding the in-amp must drive a lower impedance load.

This circuit should be built using a PC board with a ground plane on both sides. All component leads should be made as short as possible. Resistors R1 and R2 can be common 1% metal film units, but capacitors C1 and C2 need to be ±5% tolerance devices to avoid degrading the circuit's common-mode rejection. Either the traditional 5% silver micas, miniature size micas, or the new Panasonic ±2% PPS film capacitors (Digi-key part# PS1H102G-ND) are recommended.

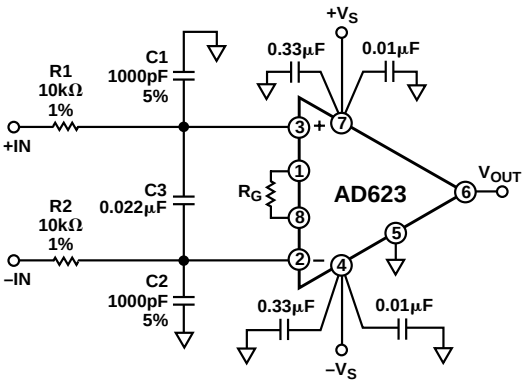


LOCATE C1–C3 AS CLOSE TO THE INPUT PINS AS POSSIBLE. USE SHORT LEADS AND A GROUND PLANE ON THE PC BOARD.

Figure 57. An RFI Suppression Circuit For the AD627 In-Amp

The circuit of Figure 57 is recommended for the AD627 micropower in-amp. Since this in-amp has higher noise (38 nV/$\sqrt{\text{Hz}}$) than the AD620 series devices, higher value input resistors can be used without seriously degrading its noise performance.

The filter bandwidth is approximately 200 Hz. At a gain of 100, maximum dc offset shift with a 1 volt p-p input applied is approximately 400 µV RTI over an input range of 1 Hz to 20 MHz. At the same gain, the circuit's RF signal rejection (RF level at output/RF applied to the input) will be better than 61 dB.



LOCATE C1–C3 AS CLOSE TO THE INPUT PINS AS POSSIBLE. USE SHORT LEADS AND A GROUND PLANE ON THE PC BOARD.

Figure 58. An RFI Suppression Circuit For the AD623 In-Amp

Figure 58 shows the recommended RFI circuit for use with the AD623 in-amp. As this device is less prone to RFI than the AD627, the input resistors can be reduced in value from 20 kΩ to 10 kΩ, to increase the circuit's signal bandwidth and lower the resistor noise contribution, and the 10 kΩ resistors still provide very effective input protection. The filter bandwidth is approximately 400 Hz. Operating at a gain of 100, the maximum dc offset shift with a 1 volt p-p input applied is less than 1 µV RTI. At the same gain, the circuit's RF signal rejection is better than 74 dB.

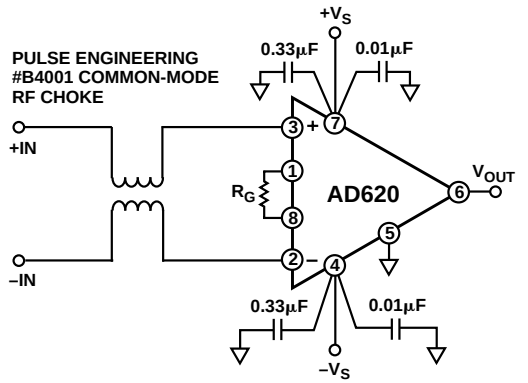


Figure 59. Using a Commercial Common-Mode RF Choke for RFI Suppression.

As an alternative to using an RC input filter, a commercial common-mode RF choke may be connected in front of the AD620 series in-amps as shown in Figure 59. A common-mode choke is a two-winding RF choke using a common core. Any RF signals that are common to both inputs will be attenuated by the choke. The common-mode choke provides a simple means for reducing RFI with a minimum of components and it provides a greater signal passband, but the effectiveness of this method depends on the quality of the particular common-mode choke being used. A choke with good internal matching is preferred. Another potential problem with using the choke is that there is no increase in input protection as is provided by the RC RFI filters.

Using the RF choke specified, at a gain of 1000, and a 1 V p-p common-mode sine wave applied to the input, the circuit of Figure 59 reduces the dc offset shift to less than 4.5 microvolts RTI.

The ac feedthrough was also greatly reduced, as shown by Table VI.

Table VI. AC CMR vs. Frequency, Using the Circuit of Figure 59

Frequency	AC CMR
100 kHz	100 dB
333 kHz	83 dB
350 kHz	79 dB
500 kHz	88 dB
1 MHz	96 dB

Because the AD627 is more susceptible to RFI than the AD620/AD621/AD622 in-amps (due to its "micropower" circuit architecture), the CM choke is not recommended for this amplifier; an RC input filter is a better choice here.

RFI Testing

Figure 60 shows a typical setup for measuring RFI rejection. To test these circuits for RFI suppression, connect the two input terminals together using very short leads. Connect a good quality sine wave generator to this input via a 50 Ω terminated cable.

Using an oscilloscope, adjust the generator for a 1 volt peak-to-peak output at the generator end of the cable. Set the in-amp to operate at high gain (such as a gain of 100). dc offset shift is simply read directly at the in-amp's output using a DVM. For measuring high frequency CMR, use an oscilloscope connected to the in-amp output by a compensated scope probe, and measure the peak-to-peak output voltage (i.e., feedthrough) vs. input frequency. When calculating CMRR vs. frequency, remember to take into account the input termination ($V_{IN}/2$) and the gain of the in-amp. The CMRR = 20 log of (($V_{IN}/2$)/(V_{OUT}/Gain)).

Miscellaneous Design Issues

Ratiometric vs. Voltage-Reference-Based Systems

Two common methods are used for ensuring that measurement accuracy does not degrade with changes in power supply voltage. The traditional approach has been to operate (or control) the entire circuit from a good quality voltage reference. More recently, many designs use an unregulated power supply to power the circuit and also use this same voltage source as a common reference for the circuit. If the individual circuit components, such as the in-amp and the ADC, are referenced via voltage dividers, etc., from a common power supply line, the individual device drifts will tend to track each other and cancel out.

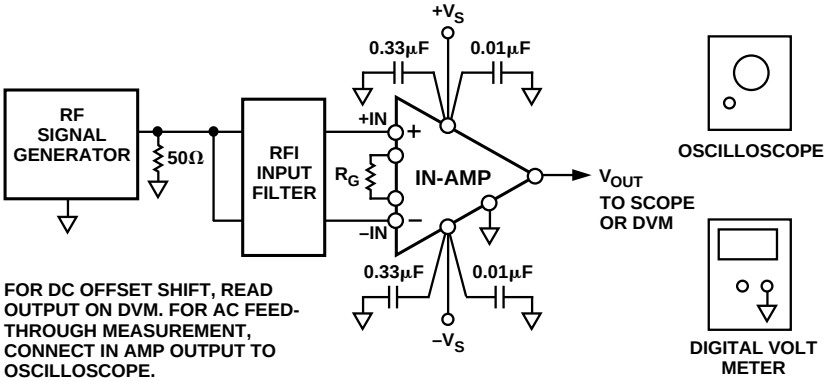


Figure 60. Typical Test Setup For Measuring An In-Amp's RFI Rejection

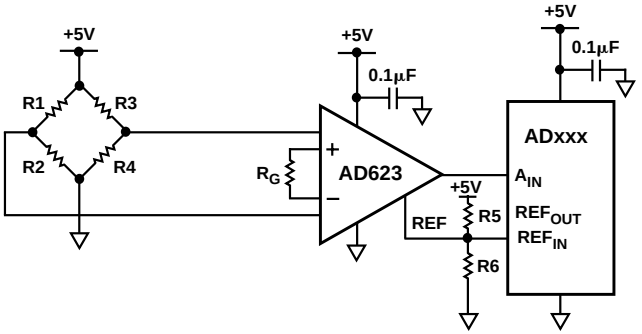


Figure 61. An In-Amp/ADC Circuit Using a Ratiometric Reference

The circuit of Figure 61 provides an example. Both the in-amp and the ADC are referenced by voltage divider R5/R6. If the supply voltage decreases by 10%, the in-amp's zero signal output voltage will go down by 10% and, at the same time, the ADC's input reference voltage also decreases by 10%.

Ratiometric circuits use fewer components, consume less power and are lower in cost than an equivalent voltage-referenced-based circuit. However, care must be taken that every device in the circuit "chain" is ratiometeric; otherwise, the net difference in drift between the regulated and ratiometric devices can produce very severe drift.

Using Low-Pass Filtering To Improve Signal-to-Noise Ratio

When trying to extract data from a noisy measurement, low-pass filtering can be used to greatly improve the signal-to-noise ratio of the measurement, by removing all signals that are not within the signal bandwidth. In some cases, bandpass filtering (reducing response both below and above the signal frequency) can be employed for an even greater improvement in measurement resolution.

The 1 Hz, 4-pole active filter of Figure 62 is an example of a very effective low-pass filter that would normally be added after the signal has been amplified by the in-amp. This filter provides high dc precision at low cost while requiring a minimum number of components.

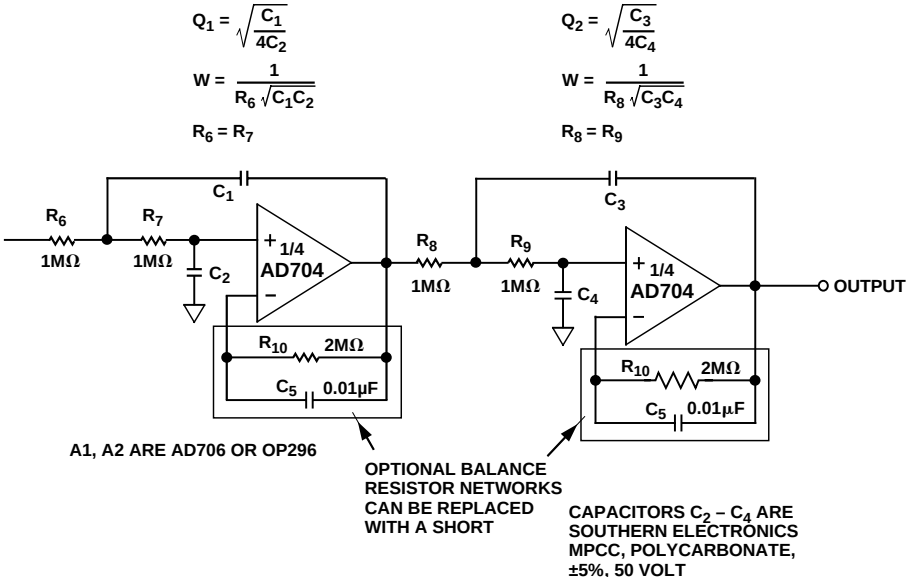


Figure 62. A 4-Pole Low-Pass Filter for Data Acquisition

Table VII. 1 Hz, 4-Pole Low-Pass Filter Recommended Component Values

Desired Low Pass Response	Section 1 Freq (Hz)	Section 1 Q	Section 2 Freq (Hz)	Section 2 Q	C1 (μF)	C2 (μF)	C3 (μF)	C4 (μF)
Bessel	1.43	0.522	1.60	0.806	0.116	0.107	0.160	0.0616
Butterworth	1.00	0.541	1.00	1.31	0.172	0.147	0.416	0.0609
0.1 dB Chebychev	0.648	0.619	0.948	2.18	0.304	0.198	0.733	0.0385
0.2 dB Chebychev	0.603	0.646	0.941	2.44	0.341	0.204	0.823	0.0347
0.5 dB Chebychev	0.540	0.705	0.932	2.94	0.416	0.209	1.00	0.0290
1.0 dB Chebychev	0.492	0.785	0.925	3.56	0.508	0.206	1.23	0.0242

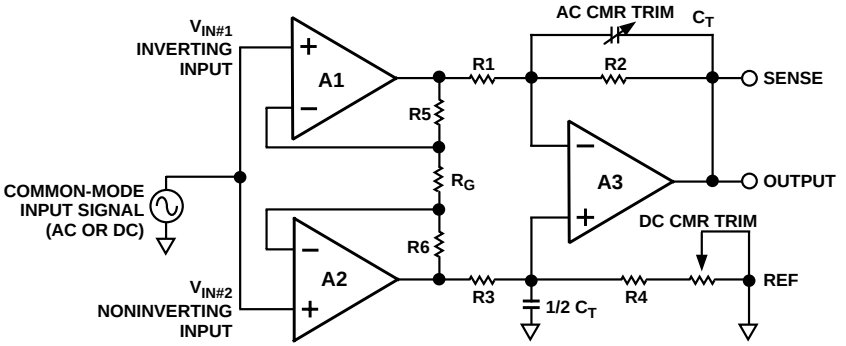


Figure 63. External DC and AC CMRR Trim Circuit for A Discrete Three Op-Amp In-Amp

Note that component values can simply be scaled to provide corner frequencies other than 1 Hz (see Table VII). If a two-pole filter is preferred, simply take the output from the first op-amp.

The low levels of current noise, input offset and input bias currents in the quad op-amp (either an AD704 or OP497) allow the use of 1 MΩ resistors without sacrificing the 1 μV/°C drift of the op-amp. Thus lower capacitor values may be used, reducing cost and space.

Furthermore, since the input bias current of these op-amps is as low as their input offset currents over most of the MIL temperature range, there rarely is a need to use the normal balancing resistor (along with its noise-reducing bypass capacitor). Note, however, that adding the optional balancing resistor will enhance performance at temperatures above 100°C.

Specified values are for a –3 dB point of 1.0 Hz. For other frequencies simply scale capacitors C1 through C4 directly; i.e., for 3 Hz Bessel response, C1 = 0.0387 μF, C2 = 0.0357 μF, C3 = 0.0533 μF, C4 = 0.0205 μF.

External CMR and Settling Time Adjustments

When a very high speed, wide bandwidth in-amp is needed, one common approach is to use several op-amps, or a combination of op-amps and a high bandwidth subtractor amplifier. These discrete designs may be readily "tuned-up" for best CMR performance by external trimming. A typical circuit is shown in Figure 63. The dc CMR should always be trimmed first, since it affects CMRR at all frequencies.

The $+V_{IN}$ and $-V_{IN}$ terminals should be tied together and a dc input voltage applied between the two inputs and ground. The voltage should be adjusted to provide a 10 volt dc input. A dc CMR trimming potentiometer is then adjusted so that the outputs are equal, and as low as possible, with both a positive and a negative dc voltage applied.

AC CMR trimming is accomplished in a similar manner, except that this time an ac input signal is applied. The input frequency used should be somewhat lower than the –3 dB bandwidth of the circuit.

The input amplitude should be set at 20 volts peak-to-peak with the inputs tied together. The ac CMR trimmer is then nulled-set to provide the lowest output possible. If the best possible settling time is needed, the ac CMR trimmer may be used, while observing the output wave form on an oscilloscope. Note that, in some cases, there will be a compromise between the best CMR and the fastest settling time.

Chapter IV:

Real-World In-Amp Applications

DATA ACQUISITION

Bridge Applications

Instrumentation amplifiers are widely used for buffering and amplifying the small voltage output from transducers that make use of the classic four resistor Wheatstone bridge.

A Classic Bridge Circuit

Figure 64 shows the AD627 configured to amplify the signal from a classic resistive bridge. This circuit will work in either dual or single supply mode. Typically the bridge will be excited by the same voltage used to power the in-amp. Connecting the bottom of the bridge to the negative supply of the in-amp (usually either 0, –5 V, –12 V or –15 V), sets up an input common-mode voltage that is optimally located midway between the supply voltages. It is also appropriate to set the voltage on the REF pin to midway between the supplies, especially if the input signal will be bipolar. However, the voltage on the REF pin can be varied to suit the application. A good example of this is when the REF pin is tied to the V_{REF} pin of an Analog-to-Digital Converter (ADC) whose input range is ($V_{REF} \pm V_{IN}$). With an available output swing on the AD627 of ($-V_S + 100$ mV) to ($+V_S - 150$ mV) the maximum programmable gain is simply this output range divided by the input range.

A Single Supply Data Acquisition System

The bridge circuit of Figure 65 is excited by a +5 V supply. The full-scale output voltage from the bridge (±10 mV) therefore has a common-mode level of 2.5 V. The AD623 removes the common-V mode component and amplifies the input signal by a factor of 100 (R_{GAIN} = 1.02 kΩ). This results in an output signal of ±1 V.

In order to prevent this signal from running into the AD623's ground rail, the voltage on the REF pin has to be raised to at least 1 V. In this example, the 2 V reference voltage from the AD7776 ADC is used to bias the AD623's output voltage to 2 V ±1 V. This corresponds to the input range of the ADC.

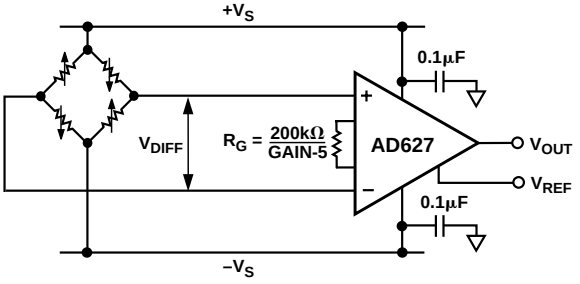


Figure 64. A Classic Bridge Circuit

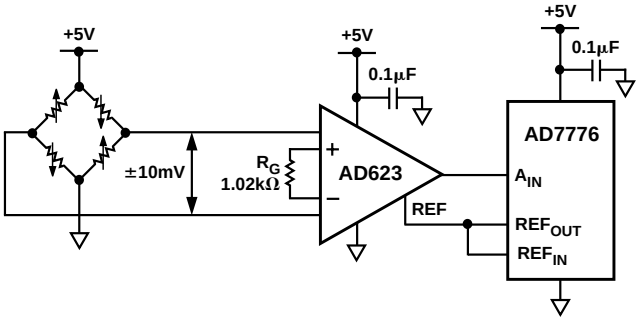


Figure 65. A Single Supply Data Acquisition System

A Low Dropout Bipolar Bridge Driver

The AD822 can be used for driving a 350 Ω Whetstone bridge. Figure 66 shows one-half of the AD822 being used to buffer the AD589, a 1.235 V low power reference. The output of +4.5 V can be used to drive an A/D converter front-end. The other half of the AD822 is configured as a unity-gain inverter and generates the other bridge input of –4.5 V.

Resistors R1 and R2 provide a constant current for bridge excitation. The AD620 low power instrumentation amplifier is used to condition the differential output voltage of the bridge. The gain of the AD620 is programmed using an external resistor, R_G, and determined by:

$$G = \frac{49.4\ k\Omega}{R_G} + 1$$

Transducer Interface Applications

Instrumentation amplifiers have long been used as preamplifiers in transducer applications. High-quality transducers typically provide a highly linear output, but at a very low level, and a characteristically high-output impedance. This requires the use of a high-gain buffer/preamplifier that will not contribute any discernible noise of its own to that of the signal. Furthermore, the high-output impedance of the typical transducer may require that the in-amp have a low input bias current.

Table VIII gives typical characteristics for some common transducer types.

Since most transducers are slow, bandwidth requirements of the in-amp are modest: a 1 MHz small signal bandwidth at unity gain is quite adequate for most applications.

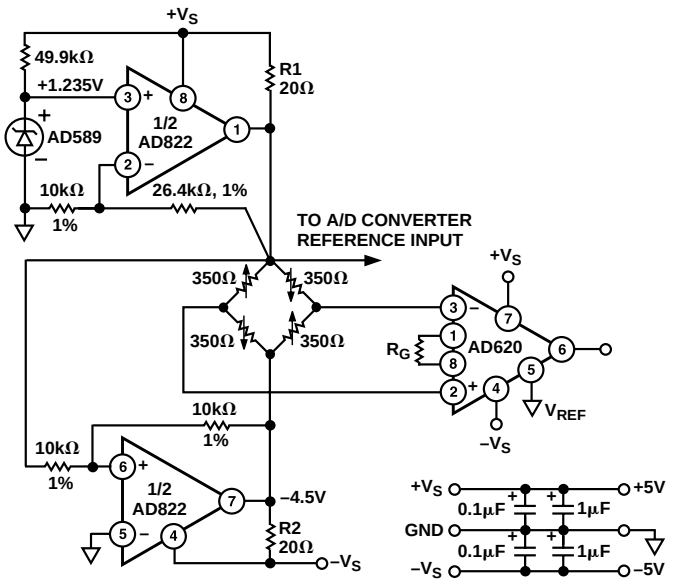


Figure 66. Low Dropout Bipolar Bridge Driver

Table VIII. Typical Transducer Characteristics

Transducer Type	Type of Output	Output Z	Recommended ADI In-Amp
Thermistor	Resistance Changes with Temperature (–TC) 4%/°C @ +25°C High Nonlinear Output Single Supply	50 Ω to 1 MΩ @ +25°C	AD627, AD629, AD620, AD621
Thermocouple	Low Source Z 10 to 100 μV/°C mV Output Level @ +25°C Single Supply	20 Ω to 2 kΩ (10 Ω typ)	AD627, AD620, AD621
Resistance Temperature Detector (RTD) (In Bridge Circuit)	Resistance Changes with Temperature (+TC) 0.1%/°C to 0.66%/°C Single or Dual Supply	20 Ω to 2 kΩ @ 0°C	AD627, AD620, AD621, AD626
Level Sensors Thermal Types Float Types	Thermistor Output (Low) Variable Resistance Outputs of mV to Several Volts Single Supply	500 Ω to 2 kΩ 100 Ω to 2 kΩ	AD626
Load Cell (Strain-Gage Bridge) (Weight Measurement)	Variable Resistance 2 mV/V of Excitation 0.1% Typical Full-Scale Change Single or Dual Supply	120 Ω to 1 kΩ	AD620, AD621
Current Sense (Shunt)	Low Value Resistor Output High Common-Mode Voltage	A Few Ohms (or Less)	AD626, AD629
EKG Monitors (Single Supply Bridge Configuration)	Low Level Differential Output Voltage 5 mV Output Typical Single or Dual Supply	500 kΩ	AD623, AD627, AD820 (Buffer)
Photodiode Sensor	Current Increases with Light Intensity. 1 pA–1 μA I_{OUTPUT} Single Supply	10^9 Ω	AD627, AD623
Hall-Effect Magnetic	5 mV/kG–120 mV/kG	1 Ω to 1 kΩ	AD627, AD623

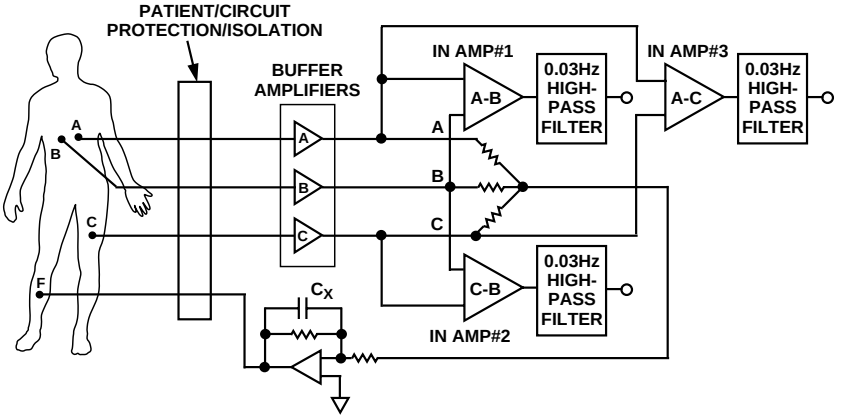


Figure 67. A Medical EKG Monitor Circuit

Medical EKG Applications

This is a challenging real-world application, as a small 5 mV signal must be extracted in the presence of much larger 60 Hz noise and large dc common-mode offset variations. Figure 67 shows a block diagram of a typical EKG monitor circuit. The value of capacitor CX is chosen to maintain stability of the right leg drive loop.

Three outputs from the patent are shown here, although several more may be used. The output buffer amplifiers should be low noise, low input bias current FET op-amps, since the patent sensors are typically very high impedance and signal levels may be quite low. A three resistor summing network is used to establish a common sense point to drive the force amplifier. The output from the force amplifier servos current through the patient until the net sum output from the three buffer amplifiers is zero.

Three in-amps are used to provide three separate outputs for monitoring the patient's condition. Suitable ADI products include the AD627 and AD623 in-amps and the AD820 op-amp for use as the buffer. Each in-amp is followed by a high-pass filter that removes the dc component from the signal. It is common practice to omit one of the in-amps and determine the third output by software (or hardware) calculation.

Proper safeguards, such as isolation, must be added to this circuit to protect the patient from possible harm.

Calculating ADC Requirements

The resolution of commercial ADCs is specified in bits. In an ADC, the available resolution equals 2^n, where n is the number of bits. For example, an 8-bit converter provides a resolution of 2^8 which equals 256. In this case, the full-scale input range of the converter divided by 256 will equal the smallest signal it can resolve. For example an 8-bit ADC with a 5 volt full-scale input range will have a limiting resolution of 19.5 mV.

In selecting an appropriate ADC to use, we need to find a device that has a resolution better than the measurement resolution but, for economy's sake, not a great deal better.

For many applications, an 8- or 10-bit converter is appropriate. The decision to use a high-resolution converter alone, or to use a gain stage ahead of a lower resolution converter, depends on which is more important: component cost or parts count and ease of assembly.

Adding amplification before the ADC will also reduce the circuit's full-scale input range but it will lower the resolution requirements (and therefore the cost) of the ADC.

For example, using an in-amp with a gain of 10 ahead of an 8- bit, 5 volt, ADC will increase circuit resolution from 19.5 mV (5 V/256) to 1.95 mV. At the same time, the full-scale input range of the circuit will be reduced to 500 mV (5 V/10).

Table IX. Typical System Resolutions Using Some Popular ADCs

Converter Type	2^n	Converter Resolution mV/Bit (5 V/2^n)	In-Amp Gain	FS Range (V p-p)	System Resolution (mV p-p)
8-Bit	256	19.5 mV	None	5	19.5
8-Bit	256	19.5 mV	2	2.5	9.75
8-Bit	256	19.5 mV	5	1	3.9
8-Bit	256	19.5 mV	10	0.5	1.95
10-Bit	1,024	4.9 mV	None	5	4.9
10-Bit	1,024	4.9 mV	2	2.5	2.45
10-Bit	1,024	4.9 mV	5	1	0.98
10-Bit	1,024	4.9 mV	10	0.5	0.49
12-Bit	4,096	1.2 mV	None	5	1.2
12-Bit	4,096	1.2 mV	2	2.5	0.6
12-Bit	4,096	1.2 mV	5	1	0.24
12-Bit	4,096	1.2 mV	10	0.5	0.12

Table IX provides input resolution and full-scale input range using an ADC with, or without, an in-amp preamplifier. Note that the system resolution specified in the figure refers to that provided by the converter together with the in-amp preamp (if used). Note that for any low level measurement, not only are low noise semiconductor devices needed, but also careful attention to component layout, grounding, power supply bypassing, and often, the use of balanced, shielded inputs.

Matching ADI In-Amps With Some Popular ADCs

Table X shows recommended ADCs for use with the latest generation of ADI in-amps.

Table X. Recommended ADCS for Use with ADI In-Amps

ADI In-Amp	**AD620**
BW	1 MHz
Noise	9 nV/√Hz
V_{OS}	125 µV
Accuracy	0.02% (12 Bits)
Supply Current	1.3 mA
Settling Time	15 µs
Recommended ADI ADC#1	**AD676/AD677**
Resolution	16-Bit
Input Range	±10 V, ±5 V
Sampling Rt	100 ksps
S/D Supply	+5 V, ±12 V
Power	360 mW
Comments	Highly Accurate Parallel/Serial Output Devices
Recommended ADI ADC#2	**AD974/AD976/AD977**
Resolution	16-Bit
Input Range	±3 V to ±10 V
Sampling Rt	100/200 ksps
S/D Supply	0 V to +4 V, 0 V to +12 V
Power	100 mW
Comments	Highly Accurate Data Acquisition System

ADI In-Amp	**AD623**
BW	800 kHz
Noise	35 nV/√Hz
V_{OS}	200 µV
Accuracy	0.1% (10 Bits)
Supply Current	575 µA
Settling Time	20 µs
Recommended ADI ADC#1	**AD7862/AD7864**
Resolution	12-Bit
Input Range	±10 V , ±2.5 V, 0 to +2.5 V
Sampling Rt	250 ksps
S/D Supply	Single +5 V
Power	60 mW
Comments	2- and 4-Channel ADCs Use in front of the AD7716 Data Acquisition System for use in bio-medical applications.
Recommended ADI ADC#2	**AD7863/AD7865**
Resolution	14-Bit
Input Range	±10 V, ±2.5 V, 0 to +2.5 V
Sampling Rt	250 ksps
S/D Supply	Single +5 V
Power	60 mW
Comments	2- and 4-Channel ADCs Recommended for providing CMRR and input scaling in 2.5 V motor control applications.
Recommended ADI ADC#3	**AD7890/AD7891/AD7892/AD7895 Series ADCs**
Resolution	12-bit
Input Range	0 to 2.5 V
Sampling Rt	600 ksps
S/D Supply	Single +5 V
Power	20-85 mW
Comments	The ADCs in this series are ideal for use with the AD623 In-Amp in low power, single supply applications. Use the AD7894 for 14-bit applications.

Device	AD627
BW	80 kHz
Noise	38 nV/$\sqrt{\text{Hz}}$
V_{OS}	200 μV
Accuracy	0.1% (10 Bits)
Supply Current	60 μA
Settling Time	135 μs
Recommended ADI ADC#1	**AD7853/AD7854/AD7858/AD7859**
Resolution	12-Bit
Input Range	0 V–5 V
Sampling Rt	100-200 ksps
S/D Supply	Single +3 V, +5 V
Power	5 mW–15 mW
Comments	Very low power, single and dual power supply ADCs. For use with the AD627 In-Amp.
Recommended ADI ADC#2	**AD7887/AD7888 or AduC812**
Resolution	12-Bit
Input Range	+2.3 V to +5 V
Sampling Rt	200 ksps
S/D Supply	Single +5 V
Power	3.6 mW (AD7888)
Comments	Use the AD7888 MicroPower ADC for the lowest possible power level. The AduC812 is a complete 5 V data acquisition system with embedded MCU.
Recommended ADI ADC#3	**AD7851 and AD7856**
Resolution	14-Bit
Input Range	Pseudo-Differential Inputs 0–V_{REF}
Sampling Rt	285 ksps–333 ksps
S/D Supply	Single +5 V
Power	60 mW
Comments	Single supply 14-bit converters with multiple unipolar inputs.

High-Speed Data Acquisition

As the speed and accuracy of modern data acquisition systems have increased, a growing need for high-bandwidth instrumentation amplifiers has developed —particularly in the field of CCD imaging equipment where offset correction and input buffering are required. Here double-correlated sampling techniques are often used for offset correction of the CCD imager. As shown in Figure 68a, two sample-and-hold amplifiers monitor the pixel and reference levels and a dc-corrected output is provided by feeding their signals into an instrumentation amplifier.

Figure 68b shows how a single multiplexed high-bandwidth in-amp can replace several slow speed nonmultiplexed buffers. The system benefits from the common-mode noise reduction, and subsequent increase in dynamic range provided by the in-amp.

Previously, the low bandwidths of commonly available instrumentation amplifiers, plus their inability to drive 50 Ω loads has restricted their use to low frequency applications—generally below 1 MHz. Some higher bandwidth amplifiers have been available, but these have been fixed-gain types with internal resistors. With these amplifiers, there was no access to the inverting and noninverting terminals of the amplifier. Using modern op-amps, employing the complementary bipolar or "CB" process, video bandwidth instrumentation amplifiers that offer both high bandwidths and impressive dc specifications may now be constructed. Common-mode rejection may be optimized by trimming or by using low cost resistor arrays.

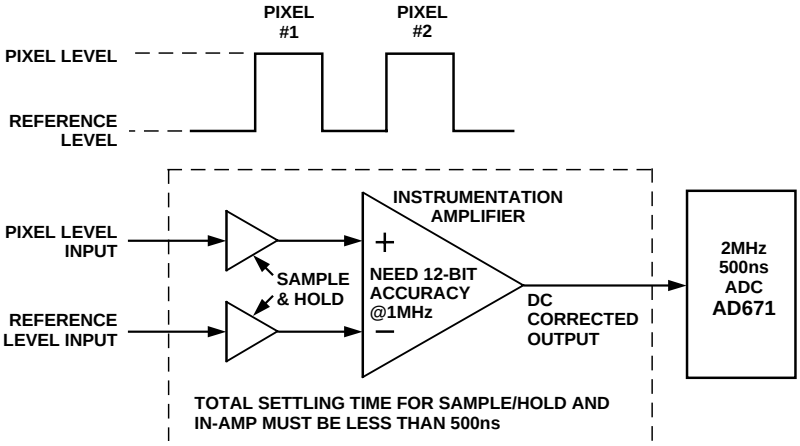


Figure 68a. In Amp Buffers ADC and Provides DC Correction

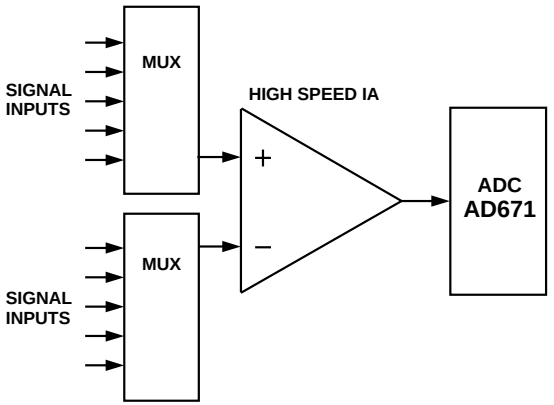


Figure 68b. Single High-Speed In-Amp and Mux Replace Several Slow Speed Buffers

The bandwidth and settling time requirements demanded of an in-amp buffering an ADC, and for the sample-and-hold function preceding it, can be quite severe. The input buffer must pass the signal along fast enough so that the signal is fully settled before the ADC takes its next sample. At least two samples per cycle are required for an ADC to unambiguously process an input signal (FS/2)—this is referred to as the "Nyquist criteria." Therefore, a 2 MHz ADC, such as the AD671, requires that the input buffer/sample hold sections preceding it provide 12-bit accuracy at a 1 MHz bandwidth. Settling time is equally important: the sampling rate of an ADC is the inverse of its sampling frequency—for the 2 MHz ADC, the sampling rate is 500 ns. This means that, for a total throughput rate of less than 1 µs, these same input buffer/sample hold sections must have a total settling time of less than 500 ns.

A High-Speed In-Amp Circuit for Data Acquisition

Figure 69 shows a discrete in-amp circuit using two AD825 op-amps and an AMP03 differential (subtractor) amplifier. This design provides both high performance and high speed at moderate gains. Circuit gain is set by resistor R_G where Gain = $1 + 2\ R_F/R_G$. Resistors R_F should be kept at around 1 kΩ to ensure maximum bandwidth. Operating at a gain of 10 (using a 222 Ω resistor for R_G) the –3 dB bandwidth of this circuit is approximately 3.4 MHz. The ac common-mode rejection ratio (gain of 10, 1 V p-p common-mode signal applied to the inputs) is 60 dB from 1 Hz to 200 kHz and 43 dB at 2 MHz. And it provides better than 46 dB CMRR from 4 MHz to 7 MHz. The RFI rejection characteristics of this amplifier are also excellent: the change in dc offset voltage vs. common-mode frequency is better than 80 dB from 1 Hz up to 15 MHz. Quiescent supply current for this circuit is 15 mA.

For lower speed applications requiring a low input current device, the AD823 FET input op-amp can be substituted for the AD825.

This circuit can be used to drive a modern, high-speed ADC such as the AD871 or AD9240, and provide very high-speed data acquisition. The AD830 can also be used for many high-speed applications.

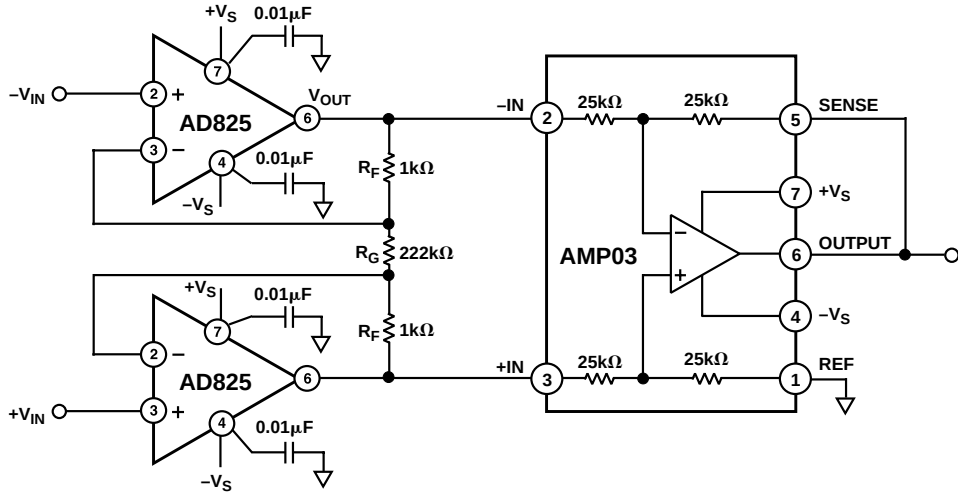


Figure 69. A High-Performance, High-Speed In-Amp Circuit

MISCELLANEOUS APPLICATIONS

An AC-Coupled Line Receiver

The AD830 is configurable as an ac-coupled differential amplifier on a single or bipolar supply voltages. All that is needed is inclusion of a few noncritical passive components as illustrated in Figure 70. A simple resistive network at the X G_M input establishes a common-mode bias. Here, the common-mode is centered at 6 volts but, in principle, can be any voltage within the common-mode limits of the AD830.

The 10 kΩ resistors to each input bias the X G_M stage with sufficiently high impedance to keep the input coupling corner frequency low, but not so large that residual bias current induced offset voltage becomes troublesome. For dual supply operation, the 10 kΩ resistors may go directly to ground. The output common is conveniently set by a Zener diode for a low impedance reference to preserve the high-frequency CMR. However, a simple resistive divider will work fine and good high-frequency CMR can be maintained by placing a compensating resistor in series with the +Y input.

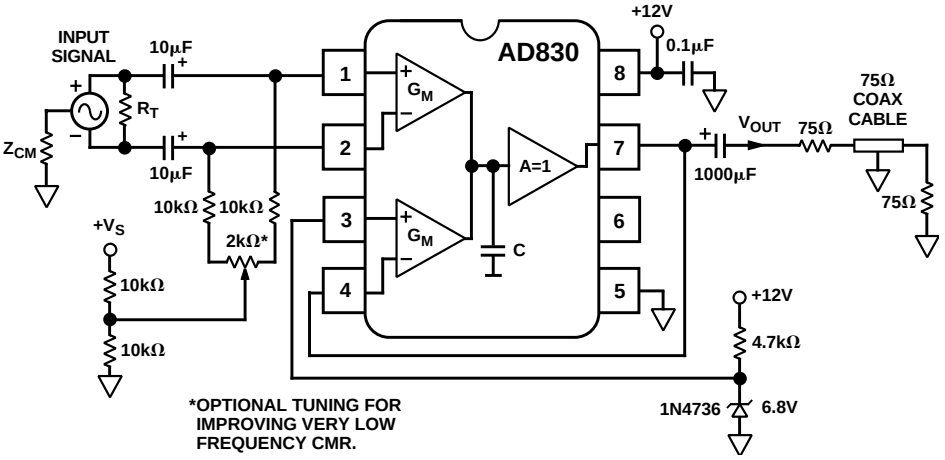


Figure 70. AC-Coupled Line Receiver

The excellent CMRR response of the circuit is shown in Figure 71. A plot of the 0.1 dB flatness from 10 Hz is shown in Figure 72. With the use of 10 μF input capacitors, the CMR is >90 dB down to a few tens of Hertz. This level of performance is almost impossible to achieve with discrete solutions.

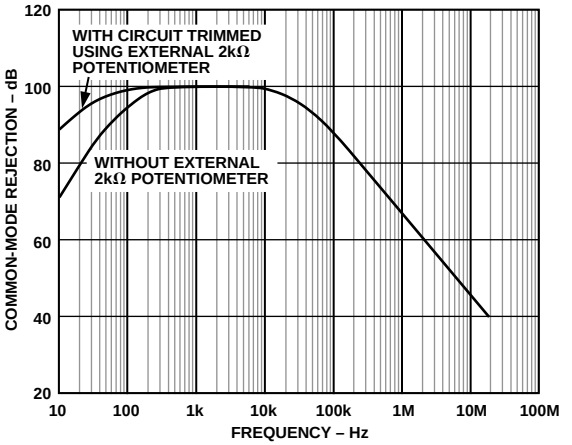


Figure 71. Common-Mode Rejection vs. Frequency for Line Receiver

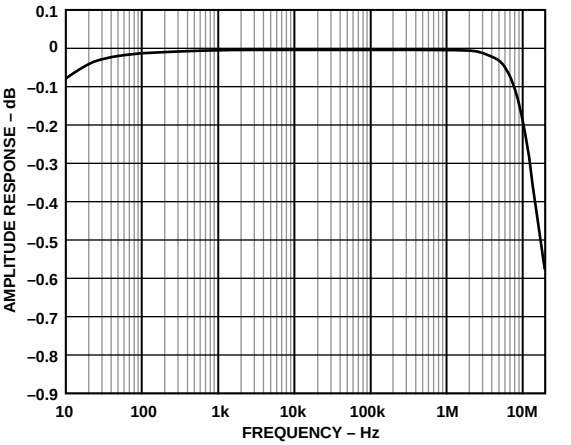


Figure 72. Amplitude Response vs. Frequency for Line Receiver

Remote Load-Sensing Technique

The circuit of Figure 73 is a unity gain instrumentation amplifier that uses its sense and reference pins to minimize any errors due to parasitic voltage drops within the circuit. If heavy output currents are expected, and there is a need to sense a load that is some distance away from the circuit, voltage drops due to trace or wire resistance can cause errors. These voltage drops are particularly troublesome with low resistance loads, such as 50 Ω.

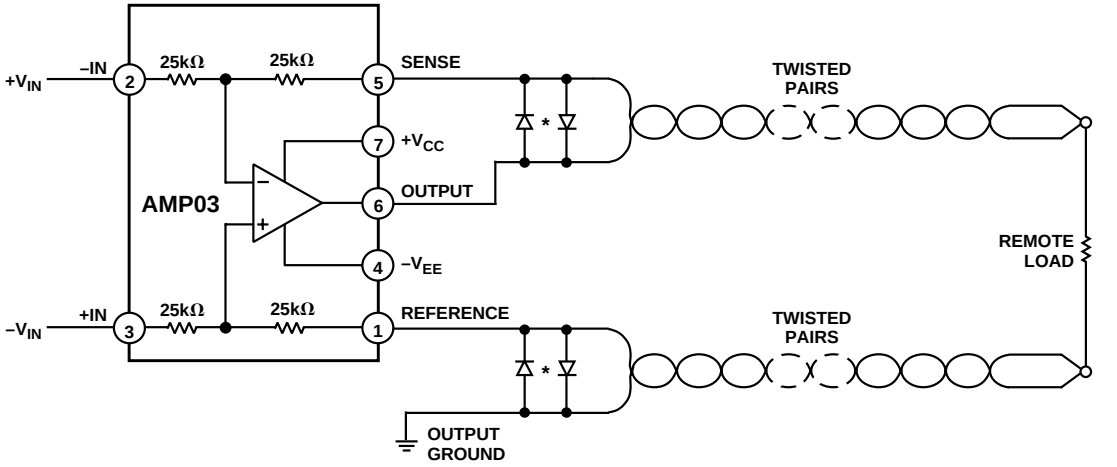


Figure 73. A Remote Load Sensing Connection

The sense terminal completes the feedback path for the instrumentation amplifier output stage and is normally connected directly to the in-amp output. Similarly, the reference terminal sets the reference voltage about which the in-amp's output will swing. This connection puts the IR drops inside the feedback loop of the in-amp and virtually eliminates any IR errors.

This circuit will provide a 3 dB bandwidth better than 3 MHz. Note that any net capacitance between the twisted pairs is isolated from the in-amp's output by 25 kΩ resistors, but any net capacitance between the twisted pairs and ground needs to be minimized to maintain stability. So, *unshielded* twisted-pair cable is recommended for this circuit. For low speed applications that require driving long lengths of *shielded* cable, the AMP01 should be substituted for the AMP03 device. The AMP01 can drive capacitance loads up to 1 μF, while the AMP03 is limited to driving a few hundred pF.

A Precision Voltage-to-Current Converter

Figure 74 is a precision voltage-to-current converter whose scale factor is easily programmed for exact decade ratios using standard 1% metal film resistor values. The AD620 operates with full accuracy on standard 5 volt power supply voltages. Note that although the quiescent current of the AD620 is only 900 μA, the addition of the AD705 will add an additional 380 μA current consumption.

A Current Sensor Interface

Figure 75 shows a novel circuit for sensing low-level currents. It makes use of the large common-mode range of the AD626. The current being measured is sensed across resistor R_S. The value of R_S should be less than 1 kΩ and should be selected so that the average differential voltage across this resistor is typically 100 mV.

To produce a full-scale output of +4 V, a gain of 40 is used, adjustable by +20% to absorb the tolerance in the

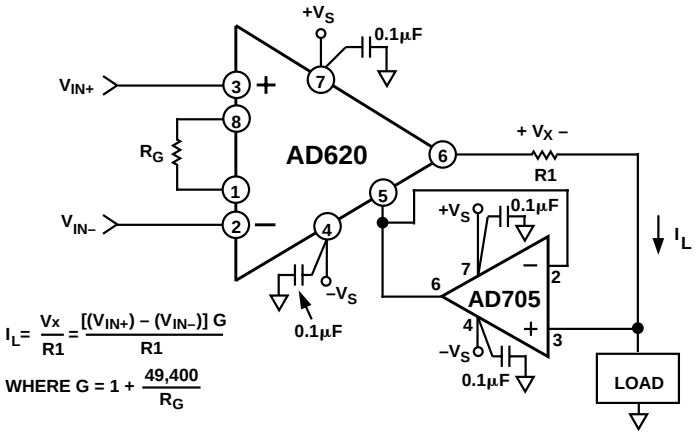


Figure 74. A Precision Voltage-to-Current Converter that Operates on ±5 Volt Supplies

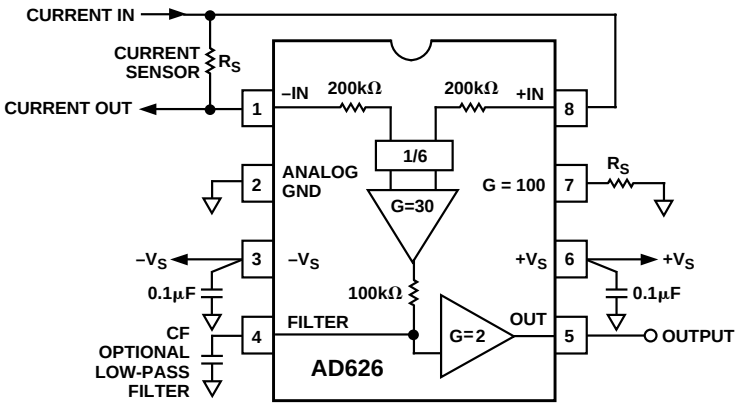


Figure 75. Current Sensor Interface

sense resistor. Note that there is sufficient headroom to allow at least a 10% overrange (to +4.4 V).

Output Buffering Low Power In-Amps

The AD627 low power in-amp is designed to drive loads of 20 kΩ or greater, but can deliver up to 20 mA to heavier loads at low output voltage swings. If more than 20 mA of output current is required, the AD627's output should be buffered with a precision op-amp such as the AD820 as shown in Figure 76. This op-amp can swing from 0 V to 4 V on its output while driving a load as small as 600 Ω. The addition of the AD820 isolates the in-amp from the load, thus greatly reducing any thermal effects.

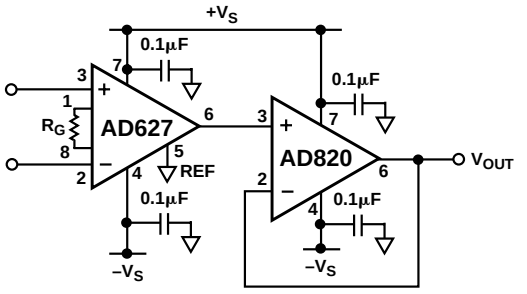


Figure 76. Output Buffer For Low Power In-Amps

A 4 mA-to-20 mA Single Supply Receiver

Figure 77 shows how a signal from a 4 mA-to-20 mA transducer can be interfaced to the ADuC812, a 12-bit ADC with an embedded microcontroller. The signal from a 4 mA-to-20 mA transducer is single-ended. This initially suggests the need for a simple shunt resistor, to convert the current to a voltage at the high-impedance analog input of the converter. However, any line resistance in the return path (to the transducer) will add a current-dependent offset error. So, the current must be sensed differentially. In this example, a 24.9 Ω shunt resistor generates a maximum differential input voltage to the AD627 of between 100 mV (for 4 mA in) and 500 mV (for 20 mA in). With no gain resistor present, the AD627 amplifies the 500 mV input voltage by a factor of 5, to 2.5 V, the full-scale input voltage of the ADC. The zero current of 4 mA corresponds to a code of 819 and the LSB size is 4.9 mV.

A Single Supply Thermocouple Amplifier

Because the common-mode input range of the AD627 extends 0.1 V below ground, it is possible to measure small differential signals with little or no common-mode component. Figure 78 shows a thermocouple application where one side of the J-type thermocouple is grounded. Over a temperature range from –200°C to

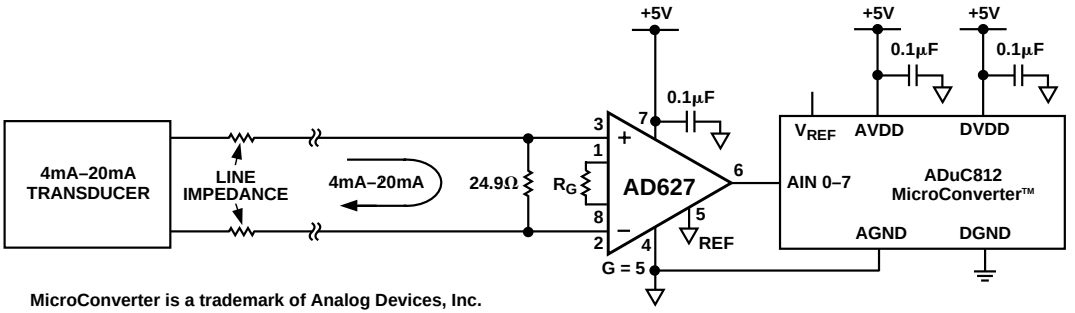


Figure 77. A 4 mA-to-20 mA Receiver Circuit

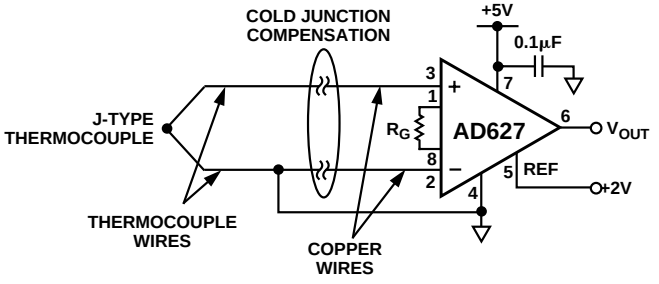


Figure 78. A Thermocouple Amplifier Using A Low Power, Single Supply In-Amp

+200°C, the J-type thermocouple delivers a voltage ranging from –7.890 mV to 10.777 mV.

A programmed gain on the AD627 of 100 (R_G = 2.1 kΩ) and a voltage on the AD627 REF pin of 2 V, results in the AD627's output voltage ranging from 1.110 V to 3.077 V relative to ground.

SPECIALTY PRODUCTS

Analog Devices sells a number of specialty products, many of which were designed for the audio market, that are useful for some in-amp applications. Table XI lists some of these products.

Table XI. Specialty Products Available from Analog Devices

Model Number	Description	BW	CMR (DC)	Supply	Features
SSM2141	Diff Line Receiver	3 MHz	100 dB	±18 V	High-CMR, Audio Subtractor
SSM2143	Diff Line Receiver	7 MHz (G = 0.5)	90 dB	±6 V to ±18 V	Low Distortion, Audio Subtractor
SSM2017	Audio Preamp	4 MHz (G = 1)	54 dB	±6 V to ±22 V	Low Noise, Low Distortion, Audio IA

Appendix A

Instrumentation Amplifier Specifications

To successfully apply any electronic component, a full understanding of its specifications is required. That is to say, the numbers contained in a spec sheet are of little value if the user does not have a clear picture of what each spec means. In this section, a typical monolithic instrumentation amplifier specification sheet will be reviewed. Some of the more important specifications will be discussed in terms of how they are measured and what errors they might contribute to the overall performance of the circuit.

Table XII shows a portion of the specification sheet for the Analog Devices AD620 instrumentation amplifier.

Table XII. AD620 Specifications

AD620—SPECIFICATIONS (Typical @ +25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted)

Model	Conditions	AD620A Min	AD620A Typ	AD620A Max	AD620B Min	AD620B Typ	AD620B Max	AD620S[1] Min	AD620S[1] Typ	AD620S[1] Max	Units
GAIN	G = 1 + (49.4 k/R_G)										
Gain Range		1		10,000	1		10,000	1		10,000	
Gain Error[2]	V_{OUT} = ±10 V										
G = 1		0.03	0.10		0.01	0.02		0.03	0.10	%	
G = 10			0.15	0.30		0.10	0.15		0.15	0.30	%
G = 100			0.15	0.30		0.10	0.15		0.15	0.30	%
G = 1000			0.40	0.70		0.35	0.50		0.40	0.70	%
Nonlinearity,	V_{OUT} = –10 V to +10 V,										
G = 1–1000	R_L = 10 kΩ		10	40		10	40		10	40	ppm
G = 1–100	R_L = 2 kΩ		10	95		10	95		10	95	ppm
Gain vs. Temperature											
	G =1			10			10			10	ppm/°C
	Gain >1[2]			–50			–50			–50	ppm/°C
VOLTAGE OFFSET	(Total RTI Error = V_{OSI} + V_{OSO}/G)										
Input Offset, V_{OSI}	V_S = ±5 V to ±15 V		30	125		15	50		30	125	µV
Over Temperature	V_S = ±5 V to ±15 V			185			85			225	µV
Average TC	V_S = ±5 V to ±15 V		0.3	1.0		0.1	0.6		0.3	1.0	µV/°C
Output Offset, V_{OSO}	V_S = ±15 V		400	1000		200	500		400	1000	µV
	V_S = ±5 V			1500			750			1500	µV
Over Temperature	V_S = ±5 V to ±15 V			2000			1000			2000	µV
Average TC	V_S = ±5 V to ±15 V		5.0	15		2.5	7.0		5.0	15	µV/°C
Offset Referred to the Input vs. Supply (PSR)	V_S = ±2.3 V to ±18 V										
G = 1		80	100		80	100		80	100		dB
G = 10		95	120		100	120		95	120		dB
G = 100		110	140		120	140		110	140		dB
G = 1000		110	140		120	140		110	140		dB
INPUT CURRENT											
Input Bias Current			0.5	2.0		0.5	1.0		0.5	2	nA
Over Temperature				2.5			1.5			4	nA
Average TC			3.0			3.0			8.0		pA/°C
Input Offset Current			0.3	1.0		0.3	0.5		0.3	1.0	nA
Over Temperature				1.5			0.75			2.0	nA
Average TC			1.5			1.5			8.0		pA/°C

Model	Conditions	AD620A Min	AD620A Typ	AD620A Max	AD620B Min	AD620B Typ	AD620B Max	AD620S[1] Min	AD620S[1] Typ	AD620S[1] Max	Units
INPUT											
Input Impedance											
Differential			10‖2			10‖2			10‖2		GΩ‖pF
Common-Mode			10‖2			10‖2			10‖2		GΩ‖pF
I Input Voltage Range[3]	V_S = ±2.3 V to ±5 V	$-V_S$ + 1.9		$+V_S$ – 1.2	$-V_S$ + 1.9		$+V_S$ – 1.2	$-V_S$ + 1.9		$+V_S$ – 1.2	V
Over Temperature		$-V_S$ + 2.1		$+V_S$ – 1.3	$-V_S$ + 2.1		$+V_S$ – 1.3	$-V_S$ + 2.1		$+V_S$ – 1.3	V
	V_S = ±5 V to ±18 V	$-V_S$ + 1.9		$+V_S$ – 1.4	$-V_S$ + 1.9		$+V_S$ – 1.4	$-V_S$ + 1.9		$+V_S$ – 1.4	V
Over Temperature		$-V_S$ + 2.1		$+V_S$ – 1.4	$-V_S$ + 2.1		$+V_S$ – 1.4	$-V_S$ + 2.3		$+V_S$ – 1.4	V
J Common-Mode Rejection											
Ratio DC to 60 Hz with											
I kΩ Source Imbalance	V_{CM} = 0 V to ±10 V										
G = 1		73	90		80	90		73	90		dB
G = 10		93	110		100	110		93	110		dB
G = 100		110	130		120	130		110	130		dB
G = 1000		110	130		120	130		110	130		dB
OUTPUT											
I Output Swing	R_L = 10 kΩ,										
	V_S = ±2.3 V to ±5 V	$-V_S$ + 1.1		$+V_S$ – 1.2	$-V_S$ + 1.1		$+V_S$ – 1.2	$-V_S$ + 1.1		$+V_S$ – 1.2	V
Over Temperature		$-V_S$ + 1.4		$+V_S$ – 1.3	$-V_S$ + 1.4		$+V_S$ – 1.3	$-V_S$ + 1.6		$+V_S$ – 1.3	V
	V_S = ±5 V to ±18 V	$-V_S$ + 1.2		$+V_S$ – 1.4	$-V_S$ + 1.2		$+V_S$ – 1.4	$-V_S$ + 1.2		$+V_S$ – 1.4	V
Over Temperature		$-V_S$ + 1.6		$+V_S$ – 1.5	$-V_S$ + 1.6		$+V_S$ – 1.5	$-V_S$ + 2.3		$+V_S$ – 1.5	V
Short Current Circuit			±18			±18			±18		mA
DYNAMIC RESPONSE											
Small Signal –3 dB Bandwidth											
G = 1			1000			1000			1000		kHz
G = 10			800			800			800		kHz
G = 100			120			120			120		kHz
G = 1000			12			12			12		kHz
Slew Rate		0.75	1.2		0.75	1.2		0.75	1.2		V/µs
K Settling Time to 0.01%	10 V Step										
G = 1–100			15			15			15		µs
G = 1000			150			150			150		µs
NOISE											
Voltage Noise, 1 kHz	$Total\ RTI\ Noise = \sqrt{(e^2_{ni}) + (e_{no}/G)^2}$										
Input, Voltage Noise, e_{ni}			9	13		9	13		9	13	nV/√Hz
Output, Voltage Noise, e_{no}			72	100		72	100		72	100	nV/√Hz
RTI, 0.1 Hz to 10 Hz											
G = 1			3.0			3.0	6.0		3.0	6.0	µV p-p
G = 10			0.55			0.55	0.8		0.55	0.8	µV p-p
G = 100–1000			0.28			0.28	0.4		0.28	0.4	µV p-p
Current Noise	f = 1 kHz		100			100			100		fA/√Hz
0.1 Hz to 10 Hz			10			10			10		pA p-p
REFERENCE INPUT											
R_{IN}			20			20			20		kΩ
I_{IN}	V_{IN+}, V_{REF} = 0		+50	+60		+50	+60		+50	+60	µA
Voltage Range		$-V_S$ + 1.6		$+V_S$ – 1.6	$-V_S$ + 1.6		$+V_S$ – 1.6	$-V_S$ + 1.6		$+V_S$ – 1.6	V
Gain to Output			1 ± 0.0001			1 ± 0.0001			1 ± 0.0001		
POWER SUPPLY											
Operating Range[4]		±2.3		±18	±2.3		±18	±2.3		±18	V
L Quiescent Current	V_S = ±2.3 V to ±18 V		0.9	1.3		0.9	1.3		0.9	1.3	mA
Over Temperature			1.1	1.6		1.1	1.6		1.1	1.6	mA
TEMPERATURE RANGE											
For Specified Performance			–40 to +85			–40 to +85			–55 to +125		°C

NOTES

[1]See Analog Devices military data sheet for 883B tested specifications.

[2]Does not include effects of external resistor R_G.

[3]One input grounded. G = 1.

[4]This is defined as the same supply range which is used to specify PSR.

Specifications subject to change without notice.

(A) Specifications (Conditions)

At the top of the spec sheet is the statement that the listed specs are typical @ $V_S = \pm 15$ V, $R_L = 2$ kΩ and $T_A = +25°C$ unless otherwise noted. This tells the user that these are the normal operating conditions under which the device is tested. Deviations from these conditions might degrade (or improve) performance. When deviations from the "normal" conditions are likely (such as a change in temperature) the significant effects are usually indicated within the specs. This statement also tells us that all numbers are typical unless noted; "typical" means that the manufacturer's characterization process has shown this number to be average, but individual devices may vary.

Specifications not discussed in detail are self-explanatory and require only a basic knowledge of electronic measurements. Those specs do not apply uniquely to instrumentation amplifiers.

Instrumentation amplifiers designed for true "rail-to-rail" operation have a few critical specifications that need to be considered. Their input voltage range should allow the in-amp to accept input signal levels that are close to the power supply or ground. Their output swing should be within 0.1 volts of the supply line or ground. In contrast, a typical dual supply in-amp can only swing within two volts or more of the supply or ground. In 5 volt single supply data acquisition systems, an extended output swing is vital as this allows the full input range of the ADC to be used, providing high resolution.

(B) Gain

These specifications relate to the transfer function of the device. The product's gain equation is normally listed at the beginning of the specifications page.

The gain equation of the AD620 is:

$$Gain = \frac{49,400\ \Omega}{R_G} + 1$$

To select an R_G for a given gain, solve the equation for R_G:

$$R_G = \frac{49,400\ \Omega}{G - 1}$$

For example, the calculated resistance for some common gains:

G = 1: $R_G = \infty$ (Open Circuit)
G = 9.998: $R_G = 5.49$ kΩ
G = 100: $R_G = 499\ \Omega$
G = 991: $R_G = 49.9\ \Omega$

Note that there will be a gain error if the standard resistance values are different from those calculated. In addition, the tolerance of the resistors used (normally 1% metal film) will also affect accuracy. And there will also be a gain drift, typically 50 ppm/°C to 100 ppm/°C, if standard resistors are used. Of course the user must provide a very clean (low leakage) circuit board to realize an accurate gain of 1, since even a 200 MΩ leakage resistance will cause a gain error of 0.2%.

Normal metal film resistors are within 1% of their stated value, which means that any two resistors could be as much as 2% different in value from one another. Thin-film resistors in monolithic integrated circuits have an absolute tolerance of only +20%, however the matching between resistors on the same chip can be excellent: typically better than 0.1% and resistors on the same chip will track each other thermally, so gain drift over temperature is greatly reduced.

(C) Gain Range

Often specified as having a gain range of 1 to 1000, or 1 to 10,000, many instrumentation amplifiers will often operate at higher gains, but the manufacturer will not promise a specific level of performance.

In practice, as the gain resistor becomes increasingly smaller, any errors due to the resistance of the metal runs and bond wires inside the IC package become significant. These errors, along with an increase in noise and drift, may make higher gains impractical.

(D) Gain Error

The number given by this specification describes maximum deviation from the gain equation. Monolithic in-amps such as the AD620 have very low factory trimmed gain errors. Although externally connected gain networks allow the user to set the gain exactly, the temperature coefficients of these external resistors and the temperature differences between individual resistors within the network, all contribute to the circuit's overall gain error.

If the data is eventually digitized and fed to an "intelligent system" (such as a microprocessor), it may be possible to correct for gain errors by measuring a known reference voltage and then multiplying by a constant.

(E) Nonlinearity

Nonlinearity is defined as the deviation from a straight line on the plot of an in-amp's output voltage versus input voltage. Figure 79 shows the transfer function of a device with exaggerated nonlinearity.

The magnitude of this error is equal to:

$$Nonlinearity = \frac{Actual\ Output - Calculated\ Output}{Rated\ Full\text{-}Scale\ Output\ Range}$$

This deviation can be specified relative to any straight line or to a specific straight line. There are two commonly used methods of specifying this ideal straight line relative to the performance of the device.

The "Best Straight Line" method of defining nonlinearity consists of measuring the peak positive and the peak negative deviation and then adjusting the gain and offset of the in-amp so that these maximum positive and negative errors are equal. For monolithic in-amps this is usually accomplished by laser trimming thin-film resistors or by other means. The "Best Straight Line" method provides impressive-looking specifications but it is much more difficult to perform. The entire output signal range needs to be examined before trimming to determine the maximum positive and negative deviations.

The "End-Point" method of specifying nonlinearity requires that any offset and/or gain calibrations are performed at the minimum and maximum extremes of the output range. Usually offset is trimmed at a very low output level while scale factor is trimmed near the maximum output level. This makes trimming much easier to implement but may result in nonlinearity errors of up to twice those attained using the "best straight line" technique. This worst case error will occur when the transfer function is "bowed" in one direction only.

Most linear devices, such as instrumentation amplifiers, are specified for best-straight-line linearity. This needs to be considered when evaluating the error budget for a particular application.

Regardless of the method used to specify nonlinearity, the errors thus created are irreducible. That is to say: these are neither fixed errors nor are they proportional to input or output voltage and, therefore, can not be reduced by external adjustment.

(F) Gain vs. Temperature

These numbers provide both maximum and typical deviations from the gain equation as a function of temperature. This error can be subtracted out in software by using a temperature reference and calibration data.

(G) Voltage Offset

Voltage offset specifications are often considered a figure of merit for instrumentation amplifiers. While any initial offset may be adjusted to zero, using hardware or software, shifts in offset voltage due to temperature variations are more difficult to correct. Intelligent systems using a microprocessor can use a temperature reference and calibration data to correct for this but there are many small-signal high-gain applications that don't have this capability.

Voltage offset and drift comprise four separate error definitions: "room temperature" (+25°C) input and output offset and offset drift over temperature referred to both input and output.

An in-amp should be regarded as a two-stage amplifier with both an input and an output section. Each section has its own error sources. Because the errors of the output section are multiplied by a fixed gain (usually two), this section is often the principle error source at low circuit gains. When the in-amp is operating at higher gains, the gain of the input stage is increased. As the gain is raised, errors contributed by the input section are multiplied, while output errors are reduced. Thus, at high gains the input stage errors dominate.

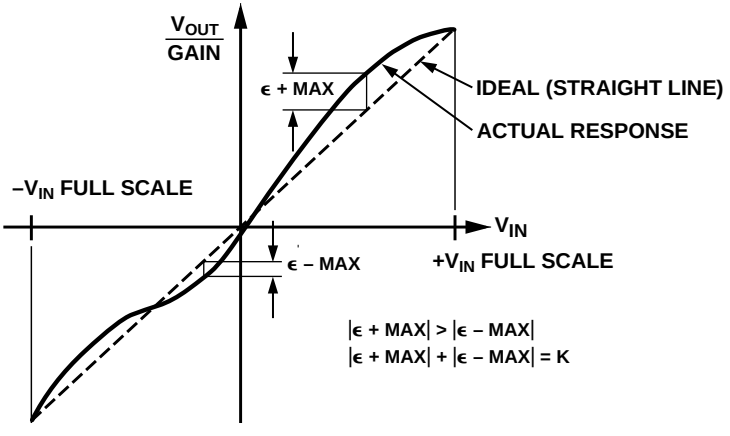


Figure 79. Transfer Function Illustrating Exaggerated Nonlinearity

Input errors are those contributed by the input stage alone; output errors are those due to the output section. Input-related specifications are often combined and classified together as "referred to input" (RTI) error while all output-related specifications are considered "referred to output" (RTO) errors. It is important to understand that although these two specifications often provide numbers that are not the same, *either* error term is correct, as each defines the total error in a different way.

For a given gain, an in-amp's input and output errors can be calculated by using the following formulas:

Total Error, RTI = Input Error + (Output Error/Gain)

Total Error, RTO = (Gain × Input Error) + Output Error

Sometimes the spec page will list an error term as RTI or RTO for a specified gain, in other cases it is up to the user to calculate the error for the desired gain.

As an example, the total voltage offset error of the AD620A in-amp when operating at a gain of ten can be calculated using the individual errors listed on its specifications page. The (typical) input offset of the AD620 (V_{OSI}), is listed as 30 μV. Its output offset (V_{OSO}) is listed as 400 μV. The total voltage offset referred to input, RTI, is equal to:

Total RTI Error = V_{OSI} + (V_{OSO}/G) = 30 μV + (400 μV/10) = 30 μV + 40 μV = 70 μV.

The total voltage offset referred to the output, RTO, is equal to:

Total Offset Error RTO = (G (V_{OSI})) + V_{OSO} = (10 (30 μV)) + 400 μV = 700 μV.

Note that the two numbers are 10× in value and logically, they should be as, at a gain of ten, the error at the output of the in-amp should be ten times the error at the input.

(H) Input Bias and Offset Currents

Input *bias* currents are those currents flowing into, or out of, the input terminals of the in-amp. In-amps using FET input stages have lower room-temperature bias currents than their bipolar cousins, but FET input currents double approximately every 11°C. Input bias currents can be considered as a source of voltage offset error (i.e., input current flowing through a source resistance causes a voltage offset). Any change in bias current is usually of more concern than the magnitude of the bias current.

Input *offset* current is the difference between the two input bias currents and this leads to offset errors in in-amps when source resistances in the two input terminals are unequal.

Although instrumentation amplifiers have differential inputs, there must be a return path for their bias currents to flow to common ("ground").

If this return path is not provided, the bases (or gates) of the input devices are left "floating" (unconnected) and the in-amp's output will rapidly drift either to common or to the supply.

Therefore, when amplifying "floating" input sources such as transformers (those without a center tap ground connection) or ungrounded thermocouples, or any ac-coupled input sources, there must still be a dc path from each input to ground. A high value resistor of 1 MΩ to 10 MΩ connected between each input and ground will normally be all that it needed to correct this condition.

(I) Key Specifications For Single Supply In-Amps

There are some specific specifications that apply to single supply (i.e., rail-to-rail) in-amp products which are of great importance to designers powering in-amps from low voltage, single supply voltages.

Input and Output Voltage Swing

A single supply in-amp needs to be able to handle input voltages that are very close to the supply and ground. In a typical dual supply in-amp the input (and output) voltage range is within only about two volts of the supply or ground. This becomes a real problem when the device is powered from a 5 V or especially so when using the new +3.3 V standard. A standard in-amp operating from a +5 V single supply line has only about 1 volt of "headroom" remaining; with a +3.3 V supply it has virtually none.

Fortunately, a decent single supply in-amp such as the AD627 will allow an output swing within 100 mV of the supply and ground. The input level is somewhat less, within 100 mV of ground and 1 V of the supply rail. In critical applications, the reference terminal of the in-amp can be moved off center to allow a symmetrical input voltage range.

Operating Voltage Range

A single supply in-amp should have the same overall operating voltage range when using either single or dual supplies. That is, a single supply in-amp, which is specified to operate with dual supply voltages from ± 1 V to ± 18 V, should also operate over a +2 V to +36 V range with a single supply. But this may not always be the case. In fact, some in-amps, such as the AD623, will operate to even lower equivalent voltage levels in single supply

mode than with a dual supply. For this reason, it is always best to check the data sheet specifications.

(J) Common-Mode Rejection

Common-Mode Rejection (CMR) is a measure of the change in output voltage when the same voltage is applied to both inputs. These specifications may be given either a full-range input voltage change or for a specified source imbalance in Ohms.

Common-Mode Rejection Ratio (CMRR) is a ratio expression while Common-Mode Rejection (CMR) is the logarithm of that ratio. Both specifications are normally referred to output (RTO). That is:

$$CMRR = \frac{Change\ in\ Output\ Voltage}{Change\ in\ Common\text{-}Mode\ Input\ Voltage}$$

While:

$$CMR = 20\ Log10\ CMRR$$

For example, a CMRR of 10,000 corresponds to a CMR of 80 dB. For most in-amps, the CMR increases with gain. This is because most designs have a front-end configuration that rejects common-mode signals while amplifying differential (i.e., signal) voltages.

Common-mode rejection is usually specified for a full-range common-mode voltage (CMV) change at a given frequency, and a specified imbalance of source impedance (e.g., 1 kΩ source unbalance, at 60 Hz).

For most in-amps, CMR increases with gain. This is very beneficial, as it allows the extraction of very weak input signals from the background noise.

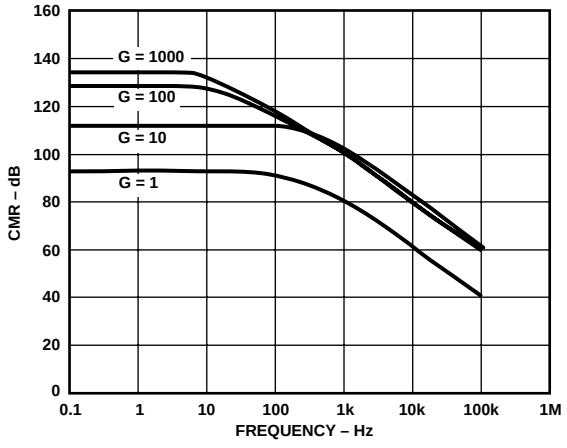


Figure 80. A Typical Graph of Common-Mode Rejection vs. Frequency

AC Common-Mode Rejection

As might be expected, an in-amp's common-mode rejection *does* vary with frequency. Usually, CMR is specified at dc or at very low input frequencies. At higher gains, an in-amp's bandwidth does decrease, lowering its gain and introducing additional phase shift in its input stage.

Since any imbalance in phase shift in the differential input stage will show up as a common-mode error, ac CMRR will usually decrease with frequency. Figure 80 shows the CMR vs. frequency of the AD620.

(K) Settling Time

Settling time is defined as that length of time required for the output voltage to approach, and remain within, a certain tolerance of its final value. It is usually specified for a fast full-scale input step and includes output slewing time. Since several factors contribute to the overall setting time, fast settling to 0.1% does not necessarily mean proportionally fast settling to 0.01%. In addition, settling time is not necessarily a function of gain. Some of the contributing factors to long settling times include slew rate limiting, underdamping (ringing) and thermal gradients (long tails).

(L) Quiescent Supply Current

This specifies the quiescent or nonsignal power supply current consumed by an in-amp within a specified operating voltage range. An in-amp's quiescent supply current is an increasingly important issue as an increasing number of real applications need to be battery powered.

With the increasing number of battery-powered applications, device power consumption has become a critical design factor. Products such as the AD627 have a very low quiescent current consumption of only 60 μA which at +5 V is only 0.3 mW. Compare this power level to that of an older, "vintage," dual supply product such as the AD526. The AD526 draws 14 mA with a ±15 V supply (30 V total) for a whopping 420 mW, 1400 times the power consumption of the AD627. The implications for battery life are dramatic.

With the introduction of products such as the AD627, very impressive overall performance is provided while consuming only microamps of supply current. Of course, some trade-offs are always necessary, so micropower in-amps tend to have lower bandwidth and higher noise than full power devices. The ability to operate rail-to-rail from a single supply voltage is an essential feature of any micropower in-amp.

Appendix B

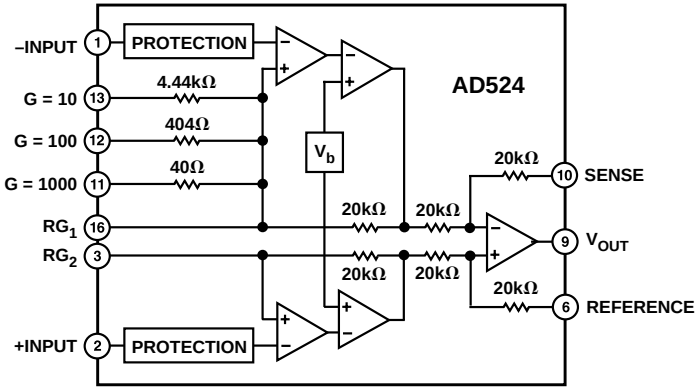
Monolithic In-Amps Available From Analog Devices

Table XIII below is useful for comparing the specifications of Analog Devices In-Amp Products. In addition, the Analog Devices Designer's Reference Manual is available on CD ROM. For the very latest update on any ADI product, check the Analog Devices Website at: http://www.analog.com.

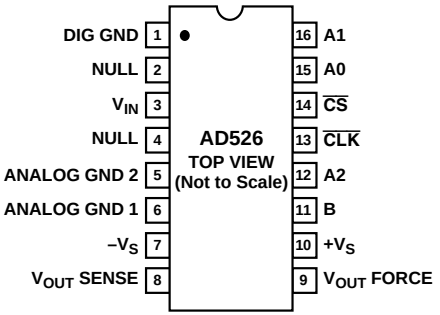
Table XIII. Specifications

Generic Part Number	Supply Current (mA) Max	Operating Voltage Range (V)	Gain Setting Method	CMR @ 60 Hz, 1k Source Imbalance, G = 10 (dB)	BW @ G = 10 (kHz) Min	Settling Time to 0.01%, G = 10 (μs) Typ	Input Voltage Offset (μV) Typ	Input Voltage Offset TC (μV/°C) Max	Input Bias Current (nA) Max	Output Offset Voltage (mV) Max	Input Voltage Noise Density (f = 1 kHz) (nV/√Hz) Max	Gain Range Min to Max	Gain Error @ G = 10 (%) Max
IN-AMPS FOR NEW DESIGNS													
Low Cost In-Amps													
AD622	1.3	±2.3 to ±18	Resistor	86	800	10	125	1	5	1.5	12 (typ)	1 to 1k	0.5
AD623	0.575	±2.5 to ±6 Dual, +3 to +12 Single	Resistor	90	100	20	200	2	25	1	35 (typ)	1 to 1k	0.35
Single Supply In-Amps													
AD623	0.575	±2.5 to ±6 Dual, +3 to +12 Single	Resistor	90	100	20	200	2	25	1	35 (typ)	1 to 1k	0.35
AD626	20.23	±2.5 to ±6	Pin	67	100	24	500	1 (typ)	ns	ns	250 (typ)	10,	0.51
AD627	0.085	Dual, +2.4 to +10 Single ±1.2 to	Resistor	(f = 100 Hz) 77	80	135	200	3	10	1	38	100 5 to	0.35
AMP04	0.9	±18 Dual, +2.2 to +36 Single ±5 to ±15 Dual, +5 to +30 Single	Resistor	55 (typ) 45 (typ)	(G = 5) 300 700	(G = 5) ns	600 900	6	40	6 3	45	1000 1 to 1k	0.75
High Accuracy In-Amps													
AD620	1.3	±2.3 to ±18	Resistor	93	800	15	125	1	2	1	13	1 to 10000	0.3
AD621	1.3	±2.3 to ±18	Pin	93	800	12	250 (Total RTI)	2.5 (Total RTI)	2	na	17 (Total RTI)	10, 100	0.15
Wide Bandwidth													
AMP03	3.5	±4.5 to ±19	na	80	3000	1 (typ)	ns	ns	ns	ns	750 (Total RTO)	1	0.008 (G = 1)
High CMV													
AD629	1	±2.5 to ±18	na	77 (G = 1)	500 (G = 1)	15 (G = 1)	1	20	na	na	550	na	0.05
VINTAGE IN-AMPS													
High Accuracy In-Amps													
AD524	5	±6 to ±18	Pin	85	400	15	250	2	50	5	7	1 to 1k	0.25
AMP01	4.8	±4.5 to ±18	Resistor	95	100	13	100	1	6	6	59	0.1 to 10000	0.8
AMP02	6	±6 to ±18	Resistor	95	300	10	200	4	20	8	18 (typ)	1 to 10000	0.4
Low Noise In-Amps													
AD624	5	±6 to ±18	Pin	90	1000 (G = 1)	15	200	2	±50	5	4	1 to 1k	±0.05 (G = 1)
AD625	5	±5 to ±18	Resistor	90	400	15	200	2	±50	5	4	1 to 1k	0.05
Software-Programmable													
AD526	14	±4.5 to ±16.5	Soft-ware	ns	350 (G = 16)	7 (G = 16)	700	10	0.15	ns	30	1, 2, 4, 8, 16	0.07 (G = 16)

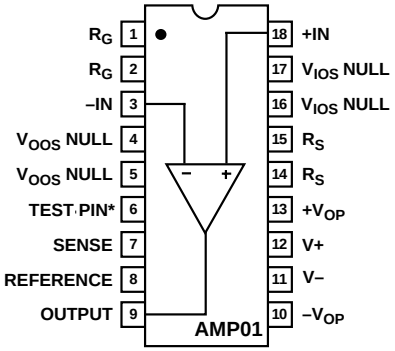
Device Pinouts for Older In-Amp Products



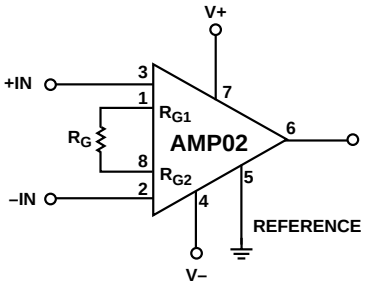
AD524



AD526



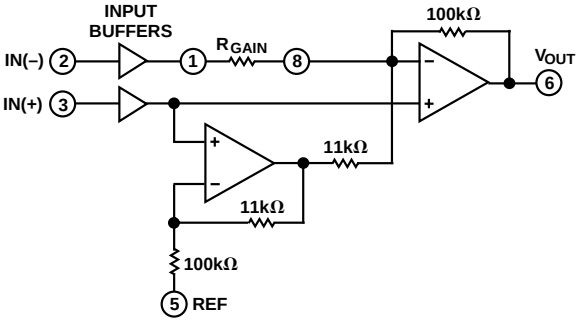
AMP01



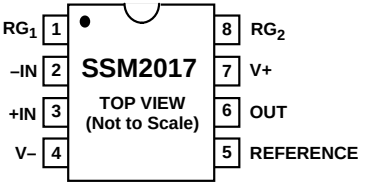
$$G = \frac{V_{OUT}}{(+IN) - (-IN)} = \left(\frac{50k\Omega}{R_G}\right) + 1$$

FOR SOL CONNECT SENSE TO OUTPUT

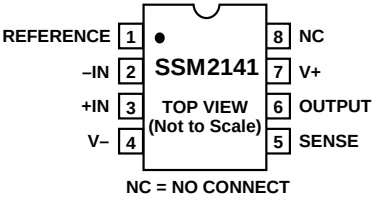
AMP02



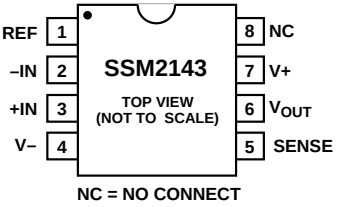
AMP04



SSM2017



SSM2141



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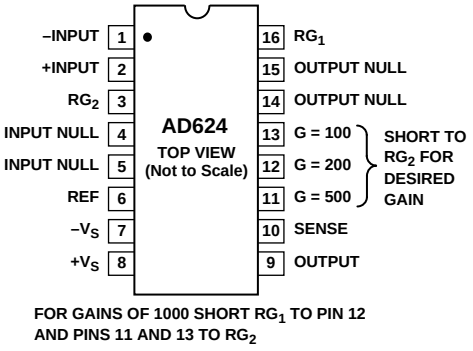

AD624

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