ADuC7026 Evaluation Board Reference Guide

MicroConverter® ADuC7026 Development System

CONTENTS:

Evaluation Board Reference Guide:

(1) EVALUATION BOARD OVERVIEW

The ADuC7026 Evaluation board has the following features :

- 2 Layer PCB (4" X 5" Form Factor)
- 9V power supply regulated to 3.3V on board
- 4 pin UART header to connect to RS232 Interface Cable
- 20-pin standard JTAG connector to connect to ULINK emulator
- Demonstration Circuit
- 32.768kHz Watch Crystal to drive the PLL clock
- ADR291 2.5V External Reference Chip
- Reset/Download/IRQ0 Push Buttons
- Power Indicator/General Purpose LEDs
- Access to all ADC inputs and DAC output from external header. All device Ports are brought out to external header pins.
- Surface mount and through hole general purpose prototype area
- External memories and latch footprint

THIS DOCUMENT REFERS TO THE MICROCONVERTER ADUC7026 EVAL BOARD REV B1

NOTES :

1. All references in this document to physical orientation of components on the board are made with respect to a component side view of the board with the prototype area appearing in the bottom of the board.

2. The board is laid out to minimize coupling between the analog and digital sections of the board. To this end, the ground plane is split with the analog section on the left hand side and a digital plane on the right hand side of the board. The regulated 3.3V power supply is routed directly to the digital section and is filtered before being routed into the analog section of the board.

(2) EVALUATION BOARD FEATURES

Power Supply:

The user should connect the 9V power supply via the 2.1mm input power socket (J5). The input connector is configured as 'CENTER NEGATIVE' i.e. GND on the center pin and +9V on the outer shield.

This 9V supply is regulated via a linear voltage regulator (U5). The 3.3V regulator output is used to drive the digital side of the board directly. The 3.3V supply is also filtered and then used to supply the analog side of the board.

When on, the LED (D3) indicates that a valid 3.3V supply is being driven from the regulator circuit. All active components are decoupled with 0.1uF at device supply pins to ground.

RS232 Interface:

The ADuC7026 (U1) P1.1 and P1.0 lines are connected to the RS232 Interface Cable via connector (J1). The Interface Cable generates the required level shifting to allow direct connection to a PC serial port. Ensure that the cable supplied is connected to the board correctly i.e. DVDD is connected to DVDD and DGND is connected to DGND.

Emulation Interface:

Non-intrusive emulation and download are possible on the ADuC7026 via JTAG by connecting a JTAG emulator to the J4 connector.

Crystal Circuit:

The board is fitted with a 32.768kHz crystal, from which the on-chip PLL circuit can generate a 41.78MHz clock.

External Reference (ADR291):

The external 2.5V reference chip (U2) has two functions. It is provided on the evaluation board to demonstrate the external reference option of the ADuC7026 but its main purpose is to generate the V_{OCM} voltage of the differential amplifier if required.

Reset/Download/IRQ0 Push Buttons:

A RESET push button is provided to allow the user to manually reset the part. When inserted the RESET pin of the ADuC7026 will be pulled to DGND. Because the RESET pin on the ADuC7026 is Schmidt triggered internally there is no need to use an external Schmidt trigger on this pin.

When inserted the IRQ0 push button switch drives P0.4/IRQ0 high. This can be used to initiate an external interrupt 0.

To enter serial download mode the user must pull the P0.0/BM pin low while reset is toggled. On the evaluation board serial download mode can be easily initiated by holding down the serial download push button (S2) while inserting and releasing the reset button (S3) as illustrated in Figure 1.

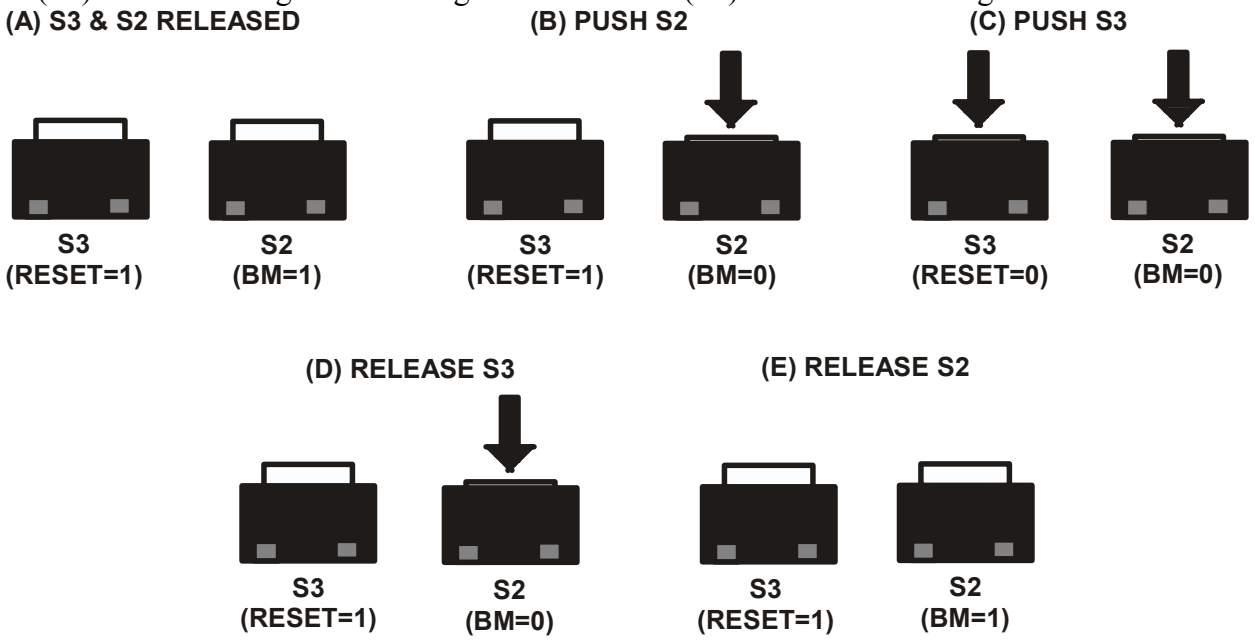

Figure 1: Entering Serial Download Mode on the Evaluation Board.

Power Indicator/General Purpose LEDs:

A power LED (D3) is used to indicate that a sufficient supply is available on the board. A general purpose LED (D2) is directly connected to P4.2 of the ADuC7026. When P4.2 is cleared the LED will be turned ON and when P4.2 is set the LED will be turned off.

Analog I/O Connections:

All analog I/O are brought out on header J3.
ADC0 and ADC1 are buffered using a AD8606 to evaluate single–ended and pseudo differential mode. A potentiometer can be connected to ADC0 buffered.
ADC3 and ADC4 can be buffered with a single-ended to differential op-amp on board, the AD8132 used to evaluate the ADC in fully differential mode.
ADC2 and ADC5 to ADC11 are not buffered. Be sure to follow the datasheet recommendation when connecting signals to these inputs.
DAC1 can be used to controlled the brightness of the green LED D1, when connected via the S1 switch.

General Purpose prototype area:

General Purpose prototype areas are provided at the bottom of the evaluation board for adding external components as required in the users application. As can be seen from the layout AV_{DD}, AGND, V_{DDIO} and DGND tracks are provided in this prototype area.

External memories and latch footprint:

Footprint for a 32k x 16 static RAM (CY7C1020CV33), a 64k x 16 Flash (AT29LV1024) and 16-bit latch is also on board. See chapter on external memory interface.

(3) DIP SWITCH LINK OPTIONS

S1-1 VREF

Function: Connects the output of the 2.5V external reference (ADR291) to the VREF pin (pin #55) of the ADuC7026.

Use: ***Slide S1-1 to the ON position*** to connect the external reference to the ADuC7026.
Slide S1-1 to the OFF position to use the internal 2.5V reference or a different external reference on VREF pin of J3 header.

S1-2 V_{OCM}

Function: Connects 1.67V to the V_{OCM} pin of the AD8132. No extra DC voltage is required on the board to use the ADC in differential mode.

Use : ***Slide S1-2 to the ON position*** to connect V_{OCM} of the differential amplifier to 1.67V, divided output of the ADR291 reference.
Slide S1-2 to the OFF position to use a different voltage for V_{OCM} by connecting a DC voltage to the V_{OCM} pin of J3 header. Note that V_{OCM} value is dependant on reference value as shown in Table 1:

V_{REF}	V_{OCM} min	V_{OCM} max
2.5V	1.25V	2.05V
2.048V	1.024V	2.276V
1.25V	0.75V	2.55V

Table 1: V_{OCM} range

S1-3 POT

Function: Connects the potentiometer output to ADC0. This input is buffered by an AD8606. This is for demonstration purposes.

Use : ***Slide S1-3 to the ON position*** to connect the potentiometer to the op-amp of ADC0 input channel.
Slide S1-3 to the OFF position to use ADC0 input on J3 header.

S1-4 ADC3

Function: Brings out ADC3 (pin #64) on J3 header.

Use: ***Slide S1-6 to the ON Position*** to connect directly ADC3 of J3 header to ADC3 pin (pin #64) of the ADuC7026.
Slide S1-6 to the OFF Position to disconnect ADC3 of J3 header from ADC3 pin (pin #64) of the ADuC7026.

S1-5 VIN-

Function: Connects -OUT of the single-ended to differential op-amp (AD8132) to ADC3. S1-5 and S1-6 must be used together, when VIN- is in the ON position, VIN+ must also be in the ON position to use the differential op-amp on channel ADC3 and ADC4.

Use: ***Slide S1-5 to the ON Position*** to connect –OUT of the AD8132 to ADC3.
Slide S1-5 to the OFF Position to use ADC3 without the AD8132.

S1-6 VIN+

Function: Connects +OUT of the single-ended to differential op-amp (AD8132) to ADC4. When VIN+ is in the ON position, VIN- must also be in the ON position to use the differential op-amp on channel ADC3 and ADC4.

Use: ***Slide S1-6 to the ON Position*** to connect +OUT of AD8132 to ADC4.
Slide S1-6 to the OFF Position to use ADC4 without the AD8132.

S1-7 ADC4

Use: ***Slide S1-6 to the ON Position*** to connect directly ADC4 of J3 header to ADC4 pin (pin #1) of the ADuC7026.
Slide S1-6 to the OFF Position to disconnect ADC4 of J3 header from ADC4 pin (pin #1) of the ADuC7026.

S1-8 LED

Function : Connects the DAC1 output to the green LED of the demo circuit, D1.

Use : ***Slide S1-7 to the ON position*** to connect the DAC1 output to D1.
Slide s1-7 to the OFF position to use DAC1 output on J3 header.

(4) EXTERNAL CONNECTORS:

J3 Analog I/O Connector

The analog I/O connector J3 provides external connections for all ADC inputs, reference inputs and DAC outputs. The pinout of the connector is shown below in Table 2.

Pin #	Pin Description
J3-1	AV_{DD}
J3-2	AGND
J3-3	V_{REF}
J3-4	DAC_{REF}
J3-5	ADC0
J3-6	ADC1
J3-7	ADC2
J3-8	ADC3
J3-9	ADC4
J3-10	ADC5
J3-11	ADC6
J3-12	ADC7
J3-13	ADC8
J3-14	ADC9
J3-15	ADC10
J3-16	ADC11
J3-17	V_{DIFF}
J3-18	V_{OCM}
J3-19	DAC0
J3-20	DAC1
J3-21	DAC2
J3-22	DAC3
J3-23	ADC_{NEG}
J3-24	AGND

Table 2: Pin functions for Analog I/O connector J3

J5 Power Supply Connections

J5 allows for the connection between the evaluation board and the 9V power supply provided in the ADuC7026 Development System.

J4 Emulation Connector

J4 provides a connection of the evaluation board to the PC via a USB cable and mIDAS Link provided in the ADuC7026 QuickStart Plus Development System only.

J1 Serial Interface Connector

J1 provides a simple connection of the evaluation board to the PC via a PC serial port cable provided with the ADuC7026 Development System.

J2 Digital I/O Connector

The digital I/O connector J2 provides external connections for all GPIOs. The pinout of the connector is shown below in Table 3, with details of the pin functions.

Pin #	Pin Description
J2-1	DGND
J2-2	**P4.5** AD13/PLAO[13]
J2-3	**P4.4** AD12/PLAO[12]
J2-4	**P4.3** AD/11PLAO[11]
J2-5	**P4.2** AD10/PLAO[10]
J2-6	**P1.0** T1/SIN/SCL0/PLAI[0]
J2-7	**P1.1** SOUT/SDA0/PLAI[1]
J2-8	**P1.2** RTS/SCL1/PLAI[2]
J2-9	**P1.3** CTS/SDA1/PLAI[3]
J2-10	**P1.4** IRQ2/RI/CLK/PLAI[4]
J2-11	**P1.5** IRQ3/DCD/MISO/PLAI[5]
J2-12	**P4.1** AD9/PLAO[9]
J2-13	**P4.0** AD8/PLAO[8]
J2-14	**P1.6** DSR/MOSI/PLAI[6]
J2-15	**P1.7** DTR/CSL/PLAO[0]
J2-16	**P2.2** $PWM0_L$/RS/PLAO[7]
J2-17	**P2.1** $PWM0_H$/WS/PLAO[6]
J2-18	**P2.7** PWM1L/$\overline{MS3}$
J2-19	**P3.7** PWM_{SYNC}/AD7/PLAI[15]
J2-20	**P3.6** PWM_{TRIP}/AD6/PLAI[14]
J2-21	**P0.7** ECLK/XCLK/SIN/PLAO[4]

Pin #	Pin Description
J2-22	**P2.0** $\overline{CONV_{START}}$/SOUT/PLAO[5]
J2-23	**P0.5** IRQ1/ADC_{BUSY}/MS0/PLAO[2]
J2-24	**P0.4** IRQ0/PWM_{TRIP}/$\overline{MS1}$/PLAO[1]
J2-25	**P3.5** $PWM2_L$/AD5/PLAI[13]
J2-26	**P3.4** $PWM2_H$/AD4/PLAI[12]
J2-27	**P2.6** $PWM1_H$/$\overline{MS2}$
J2-28	**P2.5** $PWM0_L$/$\overline{MS1}$
J2-29	**P0.3** TRST/A16/ADC_{BUSY}
J2-30	**P2.4** $PWM0_H$/$\overline{MS0}$
J2-31	**P3.3** $PWM1_L$/AD3/PLAI[11]
J2-32	**P3.2** $PWM1_H$/AD2/PLAI[10]
J2-33	**P3.1** $PWM0_L$/AD1/PLAI[9]
J2-34	**P3.0** $PWM0_H$/AD0/PLAI[8]
J2-35	**P0.2** $PWM2_L$/$\overline{BHE}$
J2-36	**P0.6** T1/MRST/AE/PLAO[3]
J2-37	**P0.0** CMP/$\overline{MS2}$/PLAI[7]
J2-38	**P4.7** AD15/PLAO[15]
J2-39	**P4.6** AD14/PLAO[14]
J2-40	**P2.3** AE
J2-41	**P0.1** $PWM2_H$/$\overline{BLE}$
J2-42	**DGND**

Table 3: Pin functions for digital I/O connector J2

(5) EXTERNAL MEMORY INTERFACE

A footprint for a 32kb x 16 SRAM and for a 64k x 16 Flash are provided on board as well as a foot print for a 16-bit D-latch since address and data are multiplexed on the external bus.

The memory footprints are for a CY7C1020CV33 and AT29LV1024.
The latch footprint is for a 74LVT16373AGG.

Note that you can use different version of the CY7C1020CV33 memory, with different access time. Wait states can be added in the XMxPAR register to allow interfacing a slower memory if required.

Connections:

Controls: $\overline{RS}$, $\overline{WS}$ and AE are the minimum control signals of any memory interface.
$\overline{MS0}$ and $\overline{MS1}$, memory select signals, are connected to the $\overline{CE}$ of respectively the SRAM and the Flash to enable the memory when necessary.
$\overline{BHE}$ and $\overline{BLE}$ allows to select the high or low byte of the 16-bit SRAM.

Data: 16 bit of data AD[15-0] are directly connected from the ADuC7026 to the memories.

Addresses: There is two ways of addressing a 16-bit memory:
1) connecting AD[15-0] to A[15-0]. It requires to enable dynamic addressing (set bit 11 in XMxPAR) to address in 16-bit mode instead of 8-bit mode.
2) connecting AD[16-1] of the ADuC702x to A[15-0] of the memory, without using dynamic addressing.

On the evaluation board, AD[15-0] are connected. In software, dynamic addressing must be enabled.
To address the 32k of the SRAM only 14-bit addresses are required. 15-bit addresses are required for the 64k Flash.

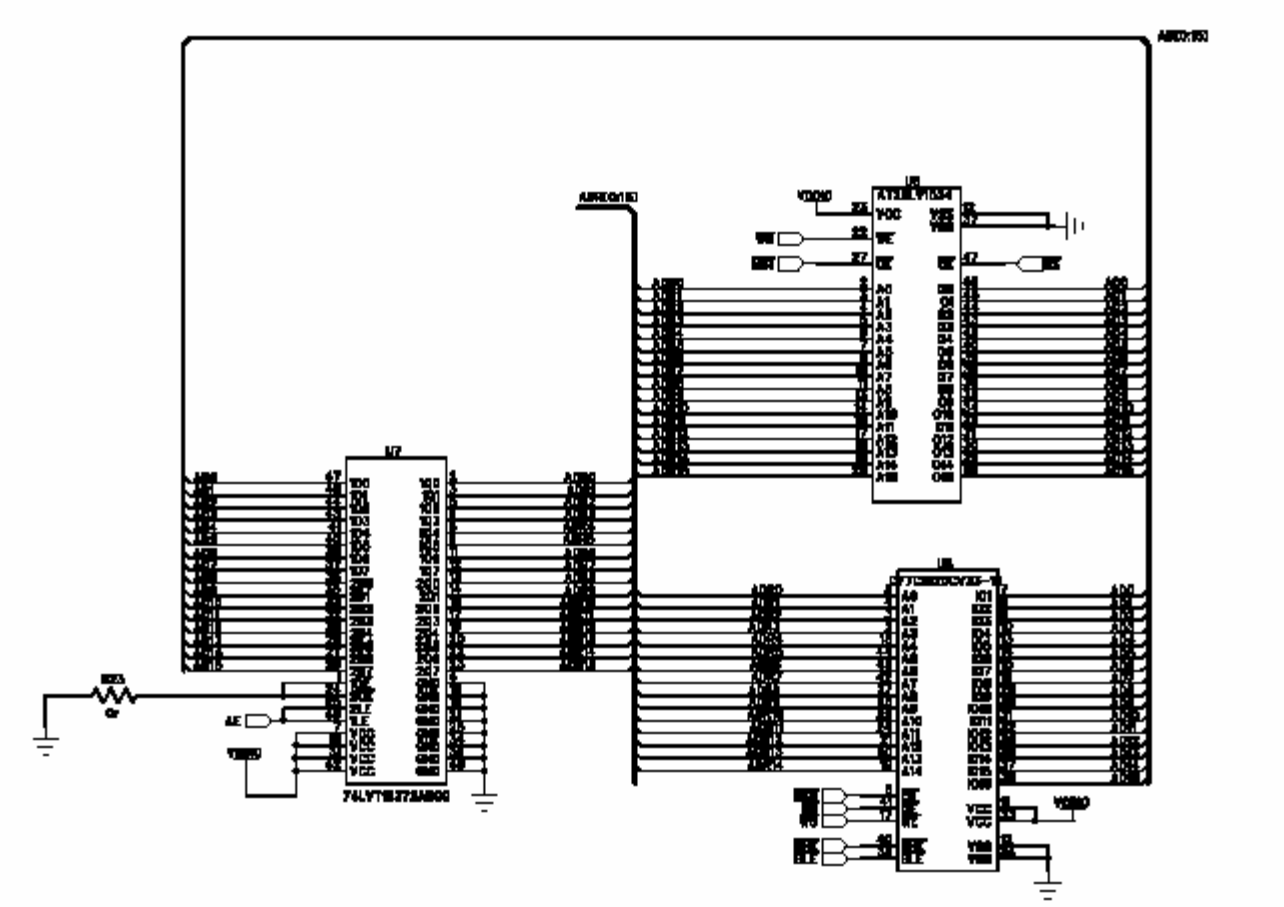

Figure 2: External Memory Connections.

Note: The footprint for the Flash is on the bottom side of the board.

(6) POTENTIOMETER DEMONSTRATION CIRCUIT

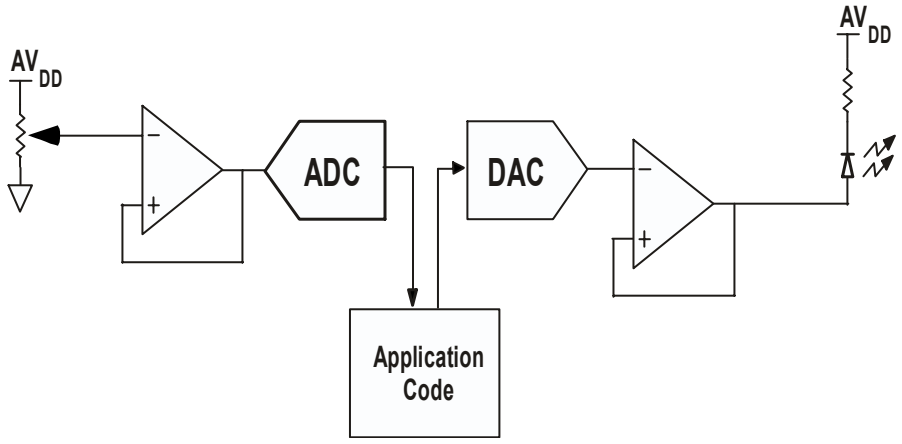

Figure 3: Circuit diagram of the RTD Circuit

Using the sample code in pot.c under the code example folder the variation in the potentiometer resistance can be seen on the output LED.
Note that the internal and external reference are 2.5V, which gives an ADC input range of 0V to 2.5V in single-ended mode. The potentiometer can give a voltage between 0V and AV_{DD} = 3.3V.

(7) SCHEMATIC

Figure 4: ADuC7026 Evaluation Board Schematic

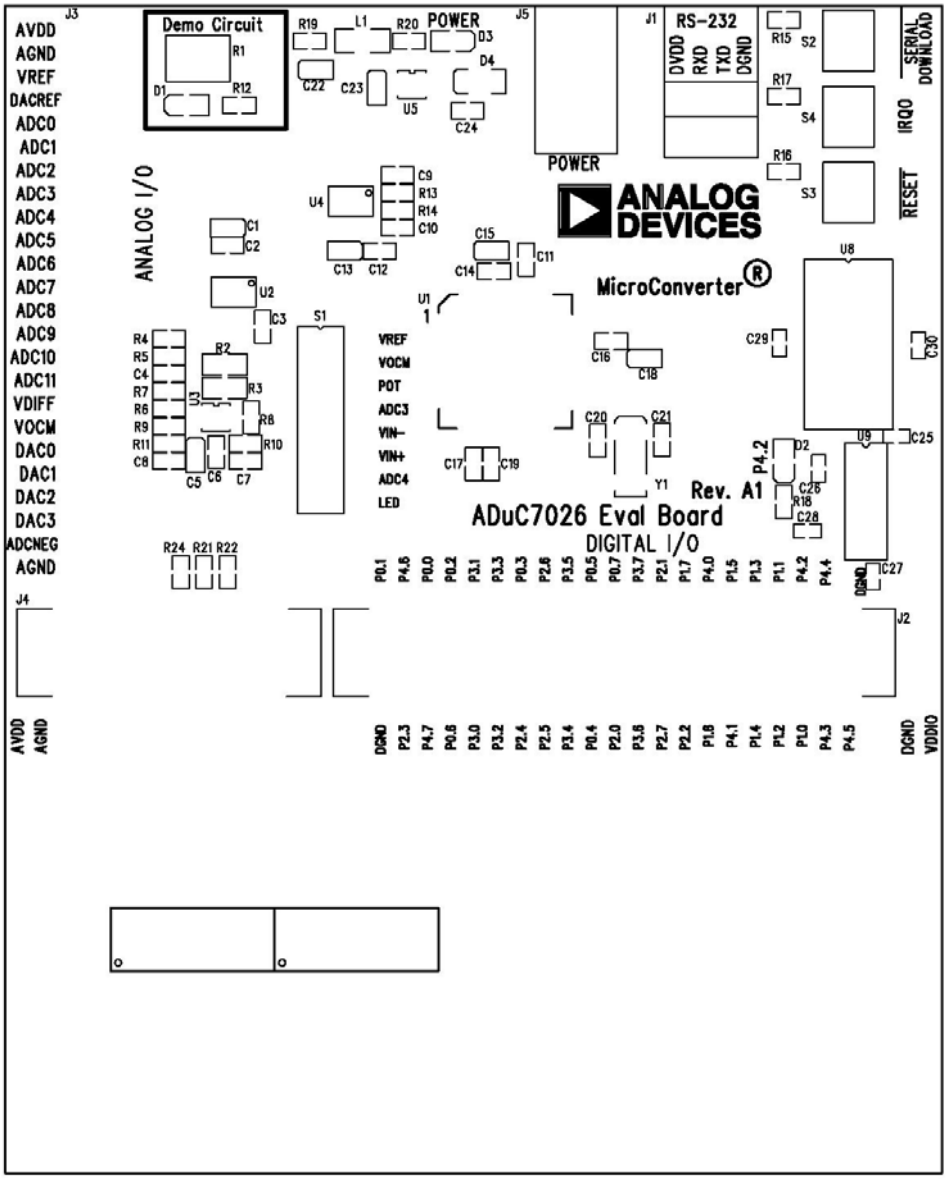

Figure 5: ADuC7026 Evaluation Board Silkscreen

(8) ADuC7026 Evaluation Board Parts List

Component	Qty	Part	Description	Order No	Order From
EVAL- ADuC7026QS QuickStart PCB	1	PCB-1	2 sided surface mount PCB		
PCB Stand-off	4	Stand-off	Stick on mounting feet	148-922	Farnell
U1	1	ADuC7026	MicroConverter (80LQFP)	ADuC7026CP	ADI
U2	1	ADR291	Bandgap reference	ADR291ER	ADI
U3	1	AD8132	Differential Op-Amp	AD8132ARM	ADI
U4	1	AD8606	Dual Op-Amp, (8 pin SOIC)	AD8606AR	ADI
U5	1	ADP3333	Fixed 3.3V Linear Voltage Regulator	ADP3333ARM3.3	ADI
U6 (**NOT POPULATED**)	0	AT29LV1024	64k x 16 Flash	AT29LV1024	
U7 (**NOT POPULATED**)	0	74LVT16373ADGG	16-bit D-latch	74LVT16373ADGG	
U8 (**NOT POPULATED**)	0	CY7C1020CV33-12	32K x 16 Static RAM	CY7C1020CV33-12	
Y1	1	32.768kHz	Watch Crystal	971-3220	Farnell
S1	1	SW\8DIP	8-way DIP switch	566-718	Farnell
S2, S3, S4	3	Push button Switch	PCB mounted push button switch	177-807	Farnell
D1, D2, D3	3	Led	1.8mm miniature led	515-620	Farnell
D4	1	PRLL4002	Diode	BAV103DITR-ND	Digikey
C1, C5, C13, C15, C18, C22, C23	7	10µF	Surface Mount Tantalum Cap, Taj-B Case	197-130	Farnell
C2-C4, C6, C12, C14, C16, C17, C24-C31	16	0.1µF	Surface Mount Ceramic Cap, 0603 Case	317-287	Farnell
C7, C8	2	22pF	Surface Mount Ceramic Cap, 0603 Case	722-005	Farnell
C9, C10	2	10nF	Surface Mount Ceramic Cap, 0603 Case	301-9561	Farnell
C11, C19	2	470nF	Surface Mount Ceramic Cap, 0603 Case	318-8851	Farnell
C20, C21	2	12pF	Surface Mount Ceramic Cap, 0603 Case	721-979	Farnell

R1	1	10K potentiometer	0.25W -4 series- 4mm square sealed	307-1741	Farnell
R2	1	100R	Surface Mount Resistor, 0603 Case	911-732	Farnell
R3	1	200R	Surface Mount Resistor, 0603 Case	321-7978	Farnell
R4	1	49R9	Surface Mount Resistor, 0805 Case	422-1825	Farnell
R5, R6, R8, R9	4	348R	Surface Mount Resistor, 0603 Case	422-2570	Farnell
R7	1	24R9	Surface Mount Resistor, 0805 Case	422-1539	Farnell
R10, R11	2	60R4	Surface Mount Resistor, 0805 Case	422-1904	Farnell
R12, R18, R20	2	270R	Surface Mount Resistor, 0603 Case	613-022	Farnell
R13, R14, R23	3	0R	Surface Mount Resistor, 0603 Case	772-227	Farnell
R15, R16, R17	3	1K	Surface Mount Resistor, 0603 Case	911-239	Farnell
R19	1	1R5	Surface Mount Resistor, 0603 Case	758-267	Farnell
R21, R22, R24	3	100k	Surface Mount Resistor, 0603 Case	911-471	Farnell
L1	1	Ferrite Bead	Surface Mount Inductor, 1206 Case	581-094	Farnell
J1	1	4-pin header	4 Pin 90º Single Row Header	TSM-104-02-T-SH	Samtec
J2	1	32-pin header	32-pin straight single row header	TSM-132-01-T-SV	Samtec
J3	1	20-pin header	20-pin straight single row header	TSM-120-01-T-SV	Samtec
J4	1	20-pin header	20-pin connector	HTST-110-01-L-DV	Samtec
J5	1		PCB mounted socket (2mm pin diameter)	KLD-SMT2-0202-A	Kycon