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APPLICATION NOTES

An-XXX

LFCSP

Lead Frame Chip Scale Package

Contents

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LFCSP- Lead Frame Chip Scale Package

1.0 SCOPE

The scope of this application note is to provide design and manufacturing guidance in the use of the Lead Frame Chip Scale Package (LFCSP). The LFCSP is compliant with JEDEC MO220 & MO229 outlines.

2.0 DESCRIPTION

LFCSP is a near Chip Scale Package (CSP), plastic encapsulated wirebond package with a copper leadframe substrate, in a leadless package format.
Perimeter input/output pads are located on the outside edges of the package. Electrical contact to the Printed Circuit Board (PCB) is made by soldering the perimeter pads and exposed paddle on the bottom surface of the package to the PCB. Heat is efficiently conducted from the package by soldering the exposed Thermal Paddle (see Figure 1) to the PCB. Stable electrical ground connections are provided through down bonds and through conductive die attach material. Wire bonding is provided using gold wires (Figure 2). Perimeter pad finish is plated as Sn/Pb solder or 100% Sn. Packaging is in Tape&Reel or Trays.

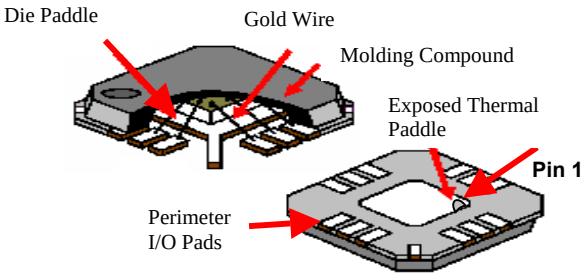


Fig.1. Isometric Cut-Away View of the LFCSP

The LFCSP is ideally suited to handheld mobile application or any application where weight and size is an issue. It allows higher density PCB application than the corresponding leaded package style

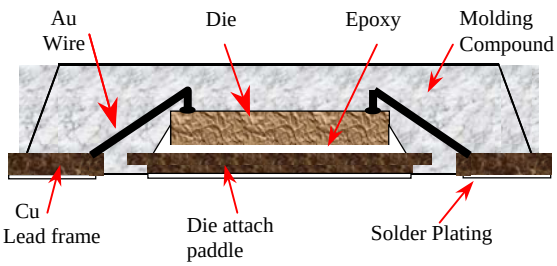


Fig.2. Cross Section of the LFCSP

The detail package outline of LFCSP is shown in Figure 3.

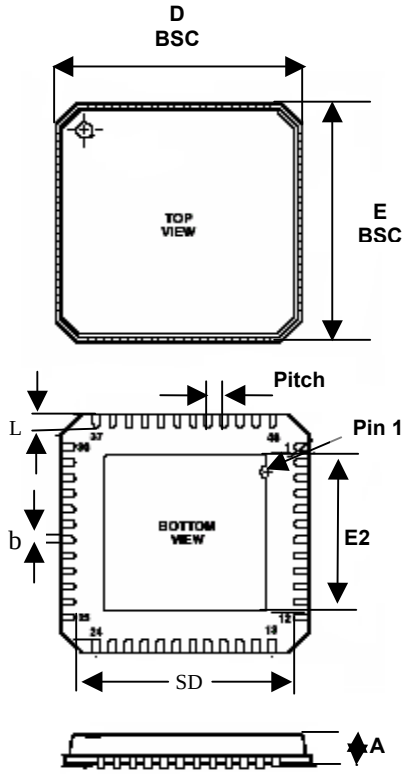


Fig.3. LFCSP Outline Drawing (JEDEC MO-220)

ADI packages are punched or sawn from a molded strip during final assembly. Half etching of the leadframe provides mold compound locking features for the perimeter pads and die paddle see Figure 4. This package is currently characterized as Moisture sensitivity (MSL) level 3 see JEDEC J-STD-20 for MSL levels.

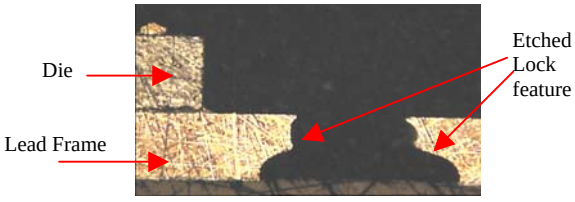


Fig.4. Leadframe locking features

2.1 Benefits over Other Standard Plastic Packages

LFCSP technology offers a number of significant benefits over standard plastic packages

- Reduction in board mounting space as die size is closer to the package size.
- Superior Electrical characteristics are obtained due to elimination of leads reducing electrical path lengths from the die to PCB.
- Lower thermal resistance because the exposed paddle is soldered to the PCB.
- The Leadframe process utilizes existing proven leadframe package technology
- Standard SMT assembly equipment can be used, no underfill required.
- High assembly yields can be realized from the self-aligning characteristic of the low mass package during solder attachment.

3.0 BOARD DESIGN CONSIDERATIONS

For optimum performance special considerations should be used to design the motherboard and to mount the package. For enhanced thermal, electrical, and board level performance, the exposed paddle on the bottom of the package is soldered to the corresponding thermal land paddle on the PCB. Thermal vias are designed into the PCB land paddle area to further improve heat dissipation.

A number of factors may have a significant effect on mounting LFCSP package on the board and the quality of solder joints. Some of these factors include: board material, board thickness, PCB perimeter pad design, thermal paddle and via design, stencil design, solder paste and solder profile.

3.1 Board Material

Standard epoxy glass substrates (FR-4) are compatible with LFCSP assembly. Use of substrate with lower coefficient of thermal expansion (CTE) can improve reliability. The CTE of a PCB can also be affected by factors such as number of metal layers, laminate materials, trace density, operating environment, site population density and mounting on the reverse side of the PCB.

3.2 Land Pattern Design Guide

The PCB land pattern for LFCSP is designed based on guidelines developed by the board assembler or by following industry standards such as IPC-SM-782. However, because of exposed thermal paddle and the package perimeter pads on the bottom side of the package, constraints should be added to IPC's methodology. The land patterns developed in the ADI Application Notes are for guideline purposes only and factor in perimeter pads and package tolerances

3.3 PCB Land Pattern

The PCB land pattern for LFCSP is defined in Figure 5.
The Tolerance analysis requires the consideration of

- Component tolerances
- PCB tolerances
- Accuracy of the equipment used for placing the component

For component tolerances, the profile tolerances usually given in the package outline drawing are converted into Maximum Material Condition (MMC) and Least Material Condition (LMC) based tolerances. The board tolerance defines the difference between the MMC and LMC of each pattern dimension. Here PCB tolerance is assumed as 0.05mm.
Equipment placement tolerance is also assumed as 0.05mm.

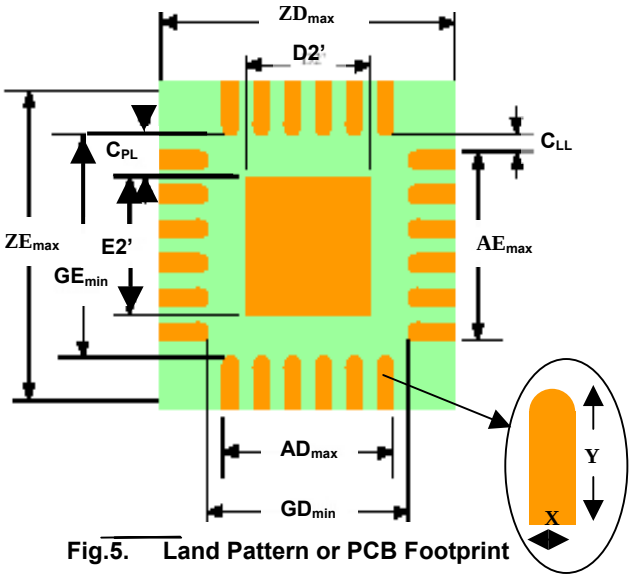
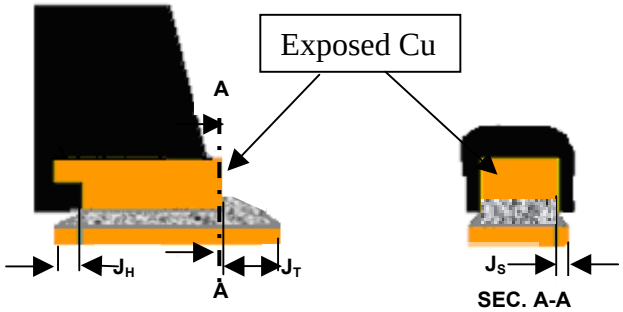


Fig.5. Land Pattern or PCB Footprint



J_T min	Minimum Toe Fillet	0.1 mm
J_H min	Minimum Heel Fillet	0.05 mm
J_S min	Minimum Side Fillet	0.0 mm

Fig.6. Toe, Heel and Side Fillets for LFCSP

The minimum values for solder joint fillets, defined in Figure 6 are used to calculate the land pattern dimensions. The values are selected recognizing that both sides and one end of the leads are embedded in the mold compound and solder fillets cannot be formed on these sides. The fourth side has the full lead thickness of Copper (Cu) exposed on the side of the package. By design this lead thickness is exposed copper since the leads are cut after plating. The cutting action on the leads is from the bottom to top of the package which results in the bottom section of the exposed copper getting covered with solder. It is generally observed that the toe fillets are formed depending on the type of solder paste used and length

of exposure of package to environmental conditions but this cannot be guaranteed. IPC/EIA J STD–001 does not require a toe fillet on the lead edge with exposed copper for bottom only terminations.
Minimum values of toe, heel, and side fillets are considered for the formation of reliable solder joints. The toe fillet will improve the solder joint reliability and provision should be made for its formation.

3.4 Land Pattern Design Calculations

The Guideline dimensions for the layout of the Land Pattern are listed in the ADI website http://wwmfg.analog.com/wwmfg/backend/globalTeams/packagingAssemblyEng/techdev/techdev.cfm click on Solder land Sizes.
Land pattern dimensions are determined initially using the following relations:

$$ZD_{max} = D_{min} + 2J_T + T_T$$

Pitch	0.5mm	0.65mm	0.8mm
X_{max} mm	0.28mm	0.37mm	0.42mm

Table1. X_{max} Values depend on Pitch

X_{max} in Table 1 is set smaller than b_{max} the max package lead width for 0.5mm pitch to avoid solder bridging.

T_T	Ts
0.31mm	0.00mm

Table2. Approximate Values for T_T, and T_S

T_T, and T_S, in Table 2 are the RMS values of toe, and side tolerances, which account for component, board, and placement tolerances. The calculations for these values are defined in more detail in IPC-SM-782.

The calculation for GD_{min} below does not account for the leads on adjacent sides of the package. In order to avoid any solder bridging between the two perpendicular leads on each corner, a minimum clearance, C_{LL}, is needed. This clearance is assumed as ≥ 0.1 mm and the value of GD_{min} is determined by using the following constraint:

$$GD_{min} \geq AD_{max} + 2C_{LL}$$

Where,

AD_{max} = (lead pitch) X (# leads on side –1) + pad width

The pad length is determined as:

$$Y = (ZD_{max} - GD_{min})/2$$

In order to ensure a robust design and to minimize any possibility of solder bridging during board assembly, a minimum metal to metal clearance of 0.2mm is required. Therefore a final adjustment to the Land Pattern is made by overlaying the nominal package outline onto the land pattern and maintaining the 0.2mm minimum metal to metal clearance, using the maximum package metal dimension.

3.5 Thermal Paddle Design

The LFCSP is designed with an exposed thermal paddle to conduct heat away from the package and into the PCB. By incorporating thermal vias into the PCB thermal paddle, heat is dissipated more effectively into the inner metal layers of the PCB.
Depending upon the package paddle size, the PCB thermal paddle size is modified, to avoid solder bridging between paddle and the perimeter pads. This is done by defining a minimum clearance between the outer edges of the thermal paddle and the inner edges of the perimeter pads as C_{PL}. This minimum clearance is fixed as 0.25mm to give the maximum size of the thermal paddle as calculated by the following relationship.

$$D2'_{TH\ max} = G_{min} - 2C_{PL}$$

The number of thermal vias incorporated into the design will depend on the power dissipation and electrical requirements of the specific application. There is a point of diminishing returns where additional thermal vias may not significantly improve the performance of the package. This is shown in Figure 7 where the effect of number of vias on Θ_{ja} is plotted for 7mm, 48 lead packages. A via diameter of 0.3mm was used for this simulation. As the via pitch decreases more vias can be incorporated for the same thermal paddle size however, the incremental performance improvement reduces.

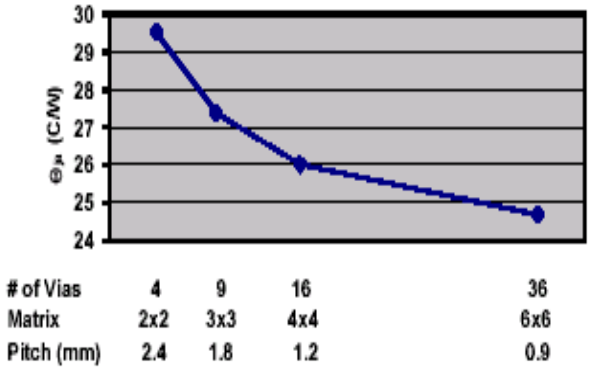


Fig.7. Effect of Number of Thermal Vias on Package Thermal Performance

It is recommended that via diameter of 0.3 to 0.33mm is used set a pitch between 1.0 and 1.2mm. A representative of these arrays is shown in Figure 8 for a 7mm x 7mm-48 lead LFCSP.

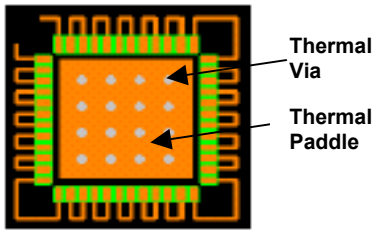


Fig.8. PCB Thermal Paddle and Via

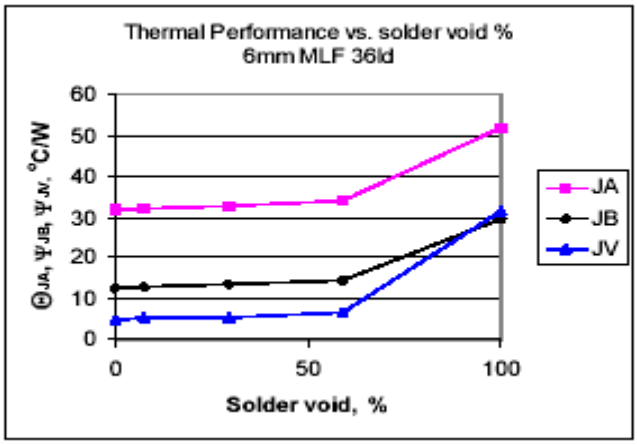


Fig.9. Effect of Voids on Thermal Performance

Thermal performance Θ_{ja} in Figure 9 is only marginally affected by small multiple voids covering up to 50% of the paddle area for LFCSP 6x6mm.

Note: Small voids do not impact the reliability of the solder joints. Large voids in the thermal paddle area should be avoided as these can affect electrical and mechanical performance.

3.6 Solder Mask Design

Two types of land pattern are used on the PCB for surface mount packages

(1) Solder Mask Defined Pads (SMD)
(2) Non Solder Mask Defined Pads (NSMD)

The copper etching process has tighter control than the solder masking process, for this reason NSMD is preferred over SMD. The solder mask opening on NSMD pads is larger than the copper pads this allows the solder to adhere to the sides of the copper pad improving reliability of the solder joints.

The difference between these two land patterns is shown in Figure 10.

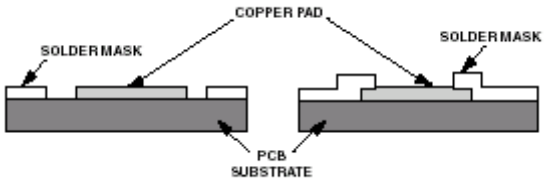


Fig.10. Cross-Sections of NSMD & SMD Pads/Land Patterns

The recommended solder mask opening should be 120 to 150 microns larger than the copper pad size to allow for solder mask registration tolerances, which are typically between 50 to 65 microns. The solder mask web must be a minimum of 75 microns in width to adhere to the PCB surface. This constraint allows each land pad to be individually masked for lead pitches of 0.5mm and higher. However, for 0.4mm pitch parts with PCB pad width of 0.25mm, not enough space is available for solder mask web in between the pads. It is recommended to use "Trench" type solder mask opening where a big opening is designed around all pads on each side of the package with no solder mask in between the pads, as shown in Figure 11. It is better to round the inner edge of the solder mask especially for corner leads to allow for enough solder mask web in the corner area.

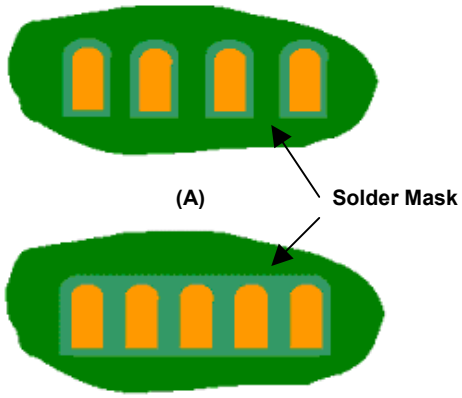


Fig.11. Solder mask for perimeter lands a) for 0.5mm and higher pitch parts, b) for 0.4mm pitch parts

Where the thermal land dimension is close to the theoretical maximum, it is recommended that the thermal paddle area should be solder mask defined in order to avoid any solder bridging between the thermal paddle and the perimeter pads. The mask opening should be 100 microns smaller than the thermal land size on all four sides.

4.0 ASSEMBLY CONSIDERATIONS

Because of the small perimeter pad surface area care should be taken to form reliable solder joints for LFCSP. This is further complicated by the large thermal paddle underneath the package and its proximity to the inner edges of the perimeter pads. Although the perimeter pad pattern design suggested above might help in eliminating some of the surface mounting problems, special considerations are needed in stencil design and paste printing for both perimeter and thermal pads. Since surface mount assembly processes vary from company to company, careful process development and characterization is recommended.

4.1 Stencil Design for Perimeter Pads

Optimum and reliable solder joints for perimeter pads should have about 50 to 75 µm standoff height and good side fillet on the outside. The first step in achieving good standoff is the solder paste stencil design for perimeter pads. The stencil aperture opening should be designed to achieve maximum paste release. This is accomplished by considering the following two ratios:

Area Ratio = Area of Aperture opening/Aperture wall area

Aspect Ratio = Aperture width / Stencil thickness

For rectangular aperture openings, as required for this package, these ratios are given as

Area Ratio = LW/2T (L+W)

Aspect Ratio = W/T

Where L and W are the aperture length and width, and

T is stencil thickness. For optimum paste release the area and aspect ratios should be greater than 0.66 and 1.5 respectively. It is recommended that the stencil aperture should be 1:1 to PCB pad sizes as both area and aspect ratio targets are easily achieved by this aperture. The stencil should be laser cut and electro-polished. Electro-polishing helps to smooth the stencil walls and results in better paste release. It is also recommended that the stencil aperture tolerances should be tightly controlled, especially for 0.4 and 0.5mm pitch devices, as these tolerances can effectively reduce the aperture size.

4.2 Stencil Design for Thermal Paddle

To effectively remove the heat from the package and to enhance electrical performance, the thermal paddle needs to be soldered (bonded) to the PCB thermal paddle, preferably with minimum voids. However, eliminating voids may not be possible because of the presence of thermal vias and the large size of the thermal paddle for larger size packages. Also, out gassing during the reflow process may cause defects (splatter, solder balling) if the solder paste coverage is too big. It is recommended that smaller multiple openings in stencil should be used instead of one big opening for printing solder paste on the thermal paddle region. This will typically result in 50 to 80% solder paste coverage. Shown in Figure 12 are some of the ways to achieve these levels of coverage.

Voids within solder joints under the exposed paddle can have an adverse effect on high speed and RF applications as well as on thermal performance. As the LFCSP package incorporates a large center paddle, controlling solder voiding within this region can be difficult. Voids within this ground plane can increase the current path of the circuit. The maximum size for a void should be less than via pitch within the plane. This assures that any one via would not be rendered ineffectual based on any void increasing the current path beyond the distance to the next available via.

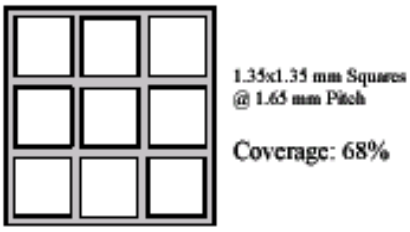


Fig.12. Thermal Paddle Stencil Design for a 7mm x7 mm LFCSP Package

Large voids in thermal paddle area should be avoided. In order to control voids in the thermal paddle area solder masking may be required for thermal vias to prevent solder wicking inside the via during reflow thus displacing the solder away from the interface between the package thermal paddle and thermal paddle land on the PCB. There are several methods employed for this purpose, such as “via tenting” (top or bottom side) using dry film solder mask, “via plugging” with liquid photo-imagible (LPI) solder mask from the bottom side, or “via encroaching”. These options are depicted in Figure 13. In case of via tenting, the solder mask diameter should be 100 microns larger than via diameter.

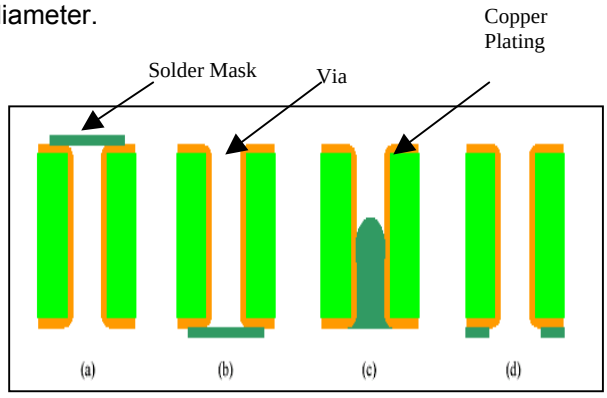


Fig.13. Solder mask options for thermal vias
(a) via tenting from top (b) via tenting from bottom
(c) via plugging bottom (d) via encroach bottom

A stencil thickness of 0.125mm is recommended for 0.4 and 0.5mm pitch parts. The stencil thickness can be increased to 0.15mm – 0.2mm for coarser pitch parts. A laser-cut, stainless steel stencil is recommended with electro-polished trapezoidal walls to improve the paste release. Since not enough space is available underneath the part after reflow, it is recommended that “No Clean”, Type 3 paste be used for mounting LFCSP. Inert Atmosphere is also recommended during reflow.

4.3 Assembly Process Sequence

Figure 14 shows the typical process flow for mounting surface mount packages to PCB.

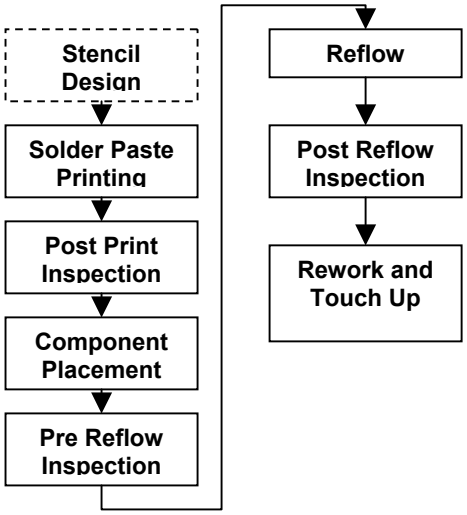


Fig.14.Typical PCB Mounting Process Flow

It is important to include post print and post reflow inspection. The volume of paste printed should be measured either by 2D or 3D techniques. The paste volume should be around 80 to 90% of stencil aperture volume to indicate good paste release. After reflow, the mounted package should be inspected for presence of voids, solder balling or defects. Cross sectioning may also be required to determine the fillet shape and size and joint standoff height.

4.4 Solder Joint Standoff Height & Fillet Formation

The solder joint standoff is a direct function of amount of paste coverage on the thermal paddle and the type of vias used for LFCSPs with exposed thermal paddle at the bottom. Board mounting studies have shown that the package standoff increases by increasing the paste coverage and by using plugged vias in the thermal paddle region as shown in Table 3 below.

	48 I/o		68 i/o	
Paste Coverage	**37%**	**67%**	**50%**	**81%**
Plugged Via	35	64	67	76
Encroached Via	16	35	32	48

Table 3. Standoff Height (µm) as a function of Via Type and Paste Coverage

The standoff height varies by the amount of solder that wets or flows into the plated through via (PTH). The encroached via provides an easy path for solder to flow into the PTH and decreases package standoff height while the plugged via impedes the flow of solder into the vias due to the plugged vias closed barrel end. In addition, the number of vias and their finished hole size will also influence the standoff height for encroached via design. The solder paste type and reactivity can affect standoff height as can PCB thickness, surface finish and reflow profile.
To achieve 50 micron thick solder joints, which help in improving the board level reliability, it is recommended that that the solder paste coverage is at least 50% for plugged vias and 75% for encroached via types.

The peripheral solder joint fillets formation is driven by multiple factors. It should be realized that only bottom surface of the leads are plated with solder and not the ends. The bare Cu on the side of the leads may oxidize if the packages are stored in uncontrolled environment. It is possible that a solder fillet will be formed depending on the solder paste (flux) used and the level of oxidation.

The fillet formation is also a function of PCB land size, printed solder volume, and the package standoff height. Since there is only limited solder available, higher standoff - controlled by paste coverage on the thermal paddle – may not leave enough solder for fillet formation. Conversely, if the standoff is too low, large convex shape fillets may form. Since center paddle coverage and via type have the greatest impact on standoff height the volume of solder necessary to create optimum fillet varies. Package standoff height and PCB pad sizes will establish the required volume.

4.5 Solder Paste Reflow

Reflow profile and peak temperature have a strong influence on void formation.

The reflow temperature should not exceed the maximum temperature the package is qualified for, according to moisture sensitivity level. The time above liquidus temperature should be around 60 seconds and the ramp rate during preheat should not exceed 3 °C/sec. Typical Pb-Free profile is shown in Figure 15 based on JEDEC J-STD-20C.

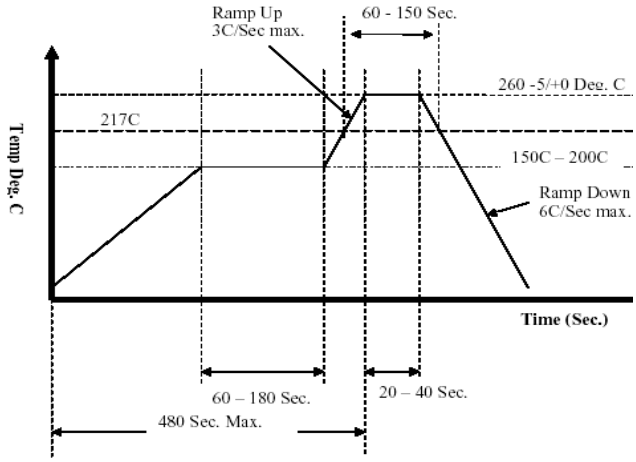


Fig.15. Pb-Free Reflow Profile

4.6 X-ray inspection

Inspection of LFCSP components mounted on PCB is achieved by using transmission of X-ray equipment in the z-plane which can detect bridging, shorts, opens and solder voids.

4.7 Visual Inspection

As the solder joints are located entirely beneath the LFCSP package, visual inspection of the joints from overhead (Z-plane) is not possible. An operator checks for misalignment of the component with the PCB lands, solder bridging or other process related failures with visual inspection equipment.

5.0 REWORK

In the event of defects occurring after component attachment, the board assembly will require rework to remove and replace the device. Since most of the soldered joint is inaccessible, correction of the defect will generally require the complete removal and replacement of the component.

Usual applications for LFCSPs involve mounting on small, thin, densely populated PCBs. These factors, coupled with the small size of the components themselves can lead to challenges in reworking defects. Because of the product dependent complexities, the following only provides a guideline and a starting point for the development of a successful rework process for these packages.

The rework process can be described in the following steps:

- Board Preparation
- Component Removal
- PCB Land Clean Up
- Application of Solder Paste
- Component Alignment & Placement
- Component Attachment
- Inspection of Rework.

5.1 Board Preparation

Prior to any rework being carried out, it is strongly recommended that the PCB assembly be baked for at least 4 hours at 125°C in order to remove any residual moisture from the assembly. Components should not exceed the conditions specified on the packaging label.

5.2 Component Removal

In order to facilitate the removal of the component from the PCB, the solder joints attaching component to the board should be reflowed. Ideally the reflow profile used for removing the component should be the same as that used for component attachment. However, the time above liquidus can be reduced as long as the reflow is complete. Removed components must not be reused.

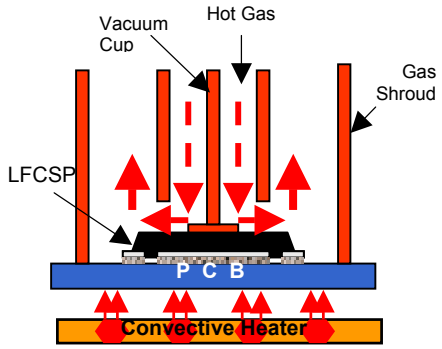


Fig.16. Solder is reflowed and the LFCSP is withdrawn before solidification

A typical component removal setup is illustrated in Figure 16. During reflow localized heating of the PCB from the bottom side using convective heaters is recommended. Reflow of the solder is achieved by directing hot gas onto the topside of the component. During the reflow of the solder joints, a vacuum cup operating within the confines of the gas shroud attaches to the topside of the component. Once the joints have reflowed, the vacuum lift-off should be automatically engaged during the transition from reflow to cool down. Given the small size of the components, the vacuum pressure should be kept below 0.5 kg/cm². This will prevent the component being lifted out before all the joints have been reflowed and avoid pad liftoff.

5.3 PCB Land Clean Up

Once the component has been removed, the site should be adequately prepared to receive the replacement device.

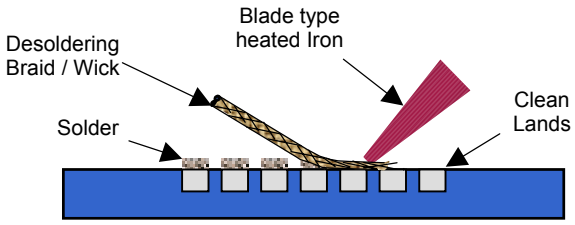


Fig.17. Desoldering the PCB lands

Cleaning the site is done in two steps:

1. Desoldering is achieved through the use of desoldering braid in conjunction with a blade type soldering Iron as shown in Figure 17. The width of the blade should match to the maximum width of the component footprint and the blade temperature should be low enough to avoid any damage to the circuit board.
2. Cleaning. The site should then be wiped clean using a lint free cloth and solvent. The solvent is usually specific to the type of paste used in the original assembly.

5.4 Application of Solder Paste

Pad geometries of the LFCSP component present a challenge in producing an even solder line thickness on reflow. A number of critical features of the print stencil should be considered. Stencil alignment accuracy and consistent solder volume transfer is critical for uniform reflow-solder processing. The stencil thickness, as well as the etched pattern geometry, determines the precise volume of solder paste deposited. Stencils are usually made of brass or stainless steel, with stainless steel being more durable. As a guide it is recommended to use a 125 microns stencil thickness for LFCSP components.

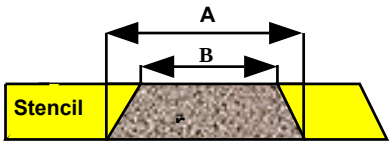


Fig.18. Stencil Aperture Geometry

Stencil apertures should be trapezoidal, as shown in Figure 18, to ensure uniform release of the solder paste and to reduce smearing, thus dimension “A” is greater than dimension “B”. The tight geometries and dense population of modern PCBs make accurate and uniform screen-printing of solder paste onto an already populated board very difficult. Thus it is recommended that the solder paste be applied directly onto the base of the component.

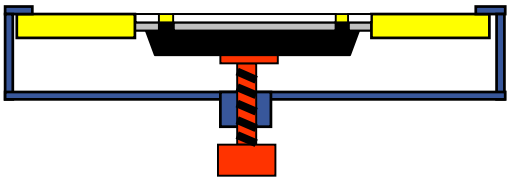


Fig. 19. LFCSP is place is clamped into stencil/jig

As shown in Figure 19 & Figure 20 the component is (a) placed into a stencil and jig specific to the particular package, (b) clamped in place, and (c) the solder is then applied using a metal squeegee blade, 125 microns thick stencil with aperture size and shape the same as the package land.

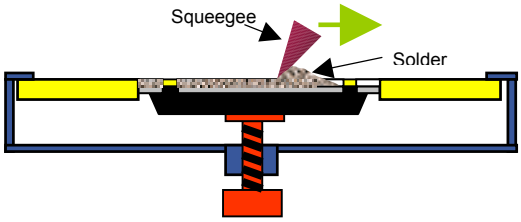


Fig. 20. Solder paste is applied through stencil to the under surface of the LFCSP

Note: The small standoff height of LFCSPs does not leave much room for cleaning therefore Type 3 (25 to 45 particle size range) no–clean solder paste should be used.

5.5 Component Alignment & Placement

The accuracy of component placement of the package is equipment or process dependent. LFCSP packages tend to have self-centering ability due to their small mass. Slightly misaligned parts (less than 50 percent off the pad center) should self-align during reflow as a result of surface tension within the liquid solder. Grossly misaligned packages (greater than 50 percent off pad center) however, are likely to result in electrical shorts as a result of solder bridges, when they are subjected to reflow.

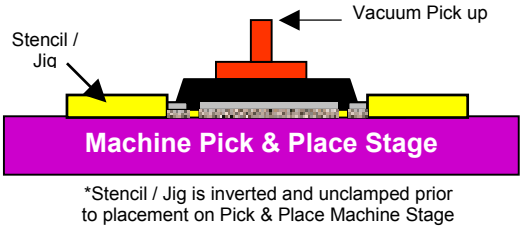


Fig.21. Stencil/Jig is placed on rework machines "Pick and Place" stage

Having screen-printed the solder paste directly on to the component, the stencil is then unclamped and both the package and stencil are placed onto the pick and place stage of the rework machine, oriented so as to provide the vacuum cup clear access to the topside of the device, as shown in Figure 21. The vacuum cup then lifts the component clear of the stencil without disturbing the solder paste, as shown in Figure 22.

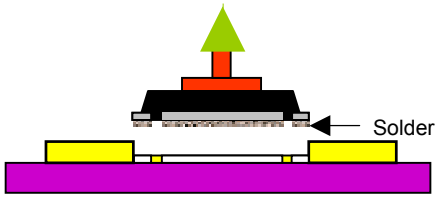


Fig.22. Vacuum cup retrieves LFCSP from Stencil without disturbing solder paste

Given that the leads on the LFCSP are located on the underside of the package, a Split-Beam optical system should be used to align the component with the solder pad array on the motherboard, see Figure 23.

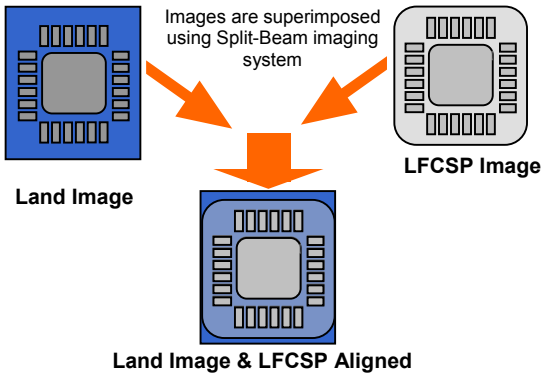


Fig.23. Image of LFCSP is superimposed onto the image of the land pattern to facilitate alignment

This type of imaging system will provide an image of the leads that can be superimposed, and by fine adjustment be overlaid onto the mating footprint on the PCB and thus align component with pad array. The alignment should be done at 50 to 100X magnification. The placement machine must have the capability of allowing fine adjustments in X, Y, and rotational axes.

5.6 Component Attachment

The reflow profile developed during original attachment or removal should be used to attach the new component, since all reflow profile parameters have already been optimized.

6.0 THERMAL PERFORMANCE

Material properties are a function of temperature and affect the reliability of the product operation. Thermal management plays an important role in the control of failure mechanisms driven by absolute temperature.
Internal resistance is the resistance at the component level. It is the resistance that exists between the junction or any other circuit element that generates heat and an outside surface of the component. External resistance is the package level resistance. The external thermal resistance is the resistance to the heat flow from the surface of the case to a reference point.

6.1 Calculation of θ_{JA} for a 7mm x 7mm LFCSP

The thermal performance of the package was calculated using ANSYS. The calculations were carried out on a 7mm x 7mm- 44 lead LFCSP, with a containing 3.81 mm square die. The model assumed that the package was attached to a 1S2P (1 Signal layer, 2 Planes) JEDEC thermal test board, constructed using JESD51-5 standard, for packages with direct thermal attachment mechanisms, with a metallized area of 76mm square. The assumed environment was that the package and test board were in a horizontal orientation. θ_{JA} was then calculated at power levels between 0.5 and 2.5 watts and at air velocities of 0, 1.0 and 2.5 m/s.

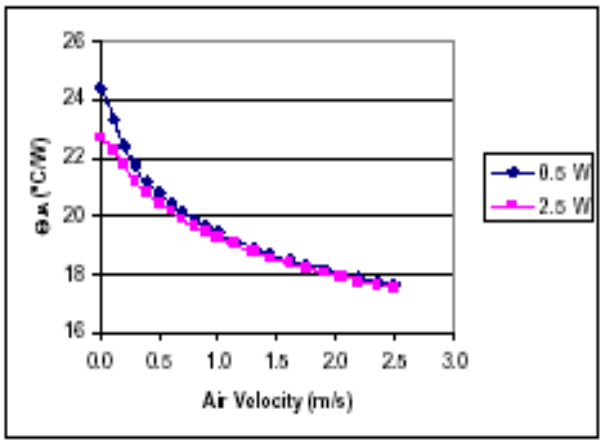


Fig. 24. Plots of θ_{JA} versus air velocity

θ_{JA} results are depicted graphically in Figure 24. In natural convection, there is a weak dependence of θ_{JA} on power. Above an air velocity of 1m/s this dependence becomes negligible. The results of the analysis imply most of the heat from the package flows into the board by way of the thermal vias and the fused leads. The metal with high thermal conductivity serves as the main heat dissipation path for the package. At 1W power, under natural convection conditions, the die temperature is approximately 25°C hotter than the ambient.

6.2 Modeling Methodology

The thermal performance of the package was calculated using a commercial finite element method software tool (ANSYS). The package leadframe patterns were generated by means of imported AUTOCAD drawings. The remainder of the package and board features was generated using parametric scripts with ANSYS.

The only geometrical approximation in the model was that the vias in the board are represented as solid cylinders. A derated thermal conductivity was used to represent via material to correct for this modification. These approximations are not expected to affect the accuracy of the model. Because of the symmetry in the package design, a one- eighth-model of the package and test board was analyzed.

7.0 ELECTRICAL CHARACTERISTICS:

Important aspects of electrical design are providing suitable paths for signals and power distribution. Lumped element electrical parameters were computed for a LFCSP. Simulations were performed using the Maxwell Q3D Extractor tool that extracts lumped element partial self and mutual inductance, bulk and mutual capacitance, partial self-resistance and SPICE models. Results were provided at high frequency for all leads and bond wires separately in partial self and mutual inductances. Self-resistances were provided at 100MHz. The package leads were laid out symmetrically as shown in Figure 25, so one quarter of the package was modeled to represent the whole package characterization. All conductors were taken to be perfect conductors in the analysis. Most leadframes are at least 150 microns thick and as the skin depth in copper at 100MHz is just a few microns, hence use of perfect conductors is reasonable.

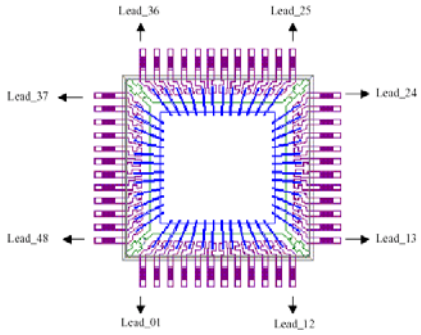


Fig.25. Package Model Top View

The package was mounted on a 15 mil thick FR-4 board. Typical bondwires were defined for each lead using the standard JEDEC4 segment bondwire model. The permittivity of the mold compound was taken as a constant with frequency and there was no loss term.

Lead	L_{11}	L_{12}	C_{11}	C_{12}
Corner	1.974	0.68	0.3300	0.1027
Centre	1.708	0.592	0.2907	0.0823
Ground plane at the same level of seating plane				
Package				
Lead count	48			
Dimension (l x w x t)	7.0x7.0x1.4 mm^3			
Lead Frame				
Material	EFTEC 64T			
Lead thickness	127µm			
Paddle size	5x5 mm^2			
Die				
Dimension (l x w x t)	4.25x4.25x0.37 mm^3			
Wire material	Gold			
Gold conductivity	4.10E+7 S/m			
Wire diameter	1.2 mm			
Wire loop height	8.0 mm			
Length	57.3 mm (Corner) 51.3 mm (Center)			

Table 4. Results for 7mm x 7mm x 1.4mm LQFP

The results from this analysis are tabulated in Table 4 and Table 5 for 7mm x 7mm- 48 lead x 1.4mm thick LFQP 7mm x 7mm- 48 lead x 0.9mm thick LFCSP.

Where,
L_{11}: Self Inductance (nH)
L_{12}: Mutual Inductance (nH) to 1st Adjacent Lead
C_{11}: Bulk Capacitance (pF)
C_{12}: Mutual Capacitance (pF) to 1st Adjacent Lead

Lead	L_{11}	L_{12}	C_{11}	C_{12}
Corner	1.135	0.211	0.280	0.048
Centre	0.909	0.143	0.268	0.043
Ground plane at the same level of seating plane				
Lead	**L_{11}**	**L_{12}**	**C_{11}**	**C_{12}**

Corner	1.149	0.213	0.263	0.063
Centre	0.920	0.149	0.239	0.056
Ground plane 15 mms below seating plane				

Package	
Lead count	48
Dimension (l x w x t)	7.0x7.0x0.9mm^3
Lead Frame	
Material	C7025
Lead thickness	127µm
Paddle size	4.75x4.75 mm^2
Die	
Dimension (l x w x t)	4.5x4.5x0.30 mm^3
Wire material	Gold
Gold conductivity	4.10E+7 S/m
Wire diameter	1.0 mm
Wire loop height	8.0 mm
Length	53.3 mm (Corner) 46.4 mm (Center)

Table 5. Results for 7mm x 7mm x 0.9mm LFCSP

The results for a 3mm x 2mm x 0.85 Lead LFCSP and 3mmx3mmx0.9mm Lead TSSOP are shown in Table 6 and Table 7.

Lead	**L_{11}**	**L_{12}**	**C_{11}**	**C_{12}**
Corner	0.487	0.056	0.168	0.040
Centre	0.418	0.039	0.183	0.035

Package	
Lead count	8
Dimension (l x w x t)	3.0x2.0x0.85 mm^3
Lead Frame	
Material	C-194
Lead thickness	203.2µm
Paddle size	1.94x0.65 mm^2
Die	
Dimension (l x w x t)	1.175x0.665x0.25 mm^3
Wire material	Gold
Gold conductivity	4.10E+7 S/m
Wire diameter	1.0 mm
Wire loop height	8.0 mm
Length	39.3 mm (Corner) 36.7 mm (Center)

Table 6. Results for 3mm x2mm x 0.85mm Lead LFCSP

Lead	**L_{11}**	**L_{12}**	**C_{11}**	**C_{12}**
Maximum	1.486	0.372	0.230	0.058
Minimum	1.275	0.329	0.242	0.052

Package	
Lead count	8
Dimension (l x w x t)	3.0x3.0x0.9 mm^3
Lead Frame	
Material	C7025
Lead thickness	127µm
Paddle size	2.4x1.7mm^2
Die	
Dimension (l x w x t)	1.6x1.0x0.25 mm^3
Wire material	Gold
Gold conductivity	4.10E+7 S/m
Wire diameter	1.0 mm
Wire loop height	7.1 mm
Length	1.23 mm (Corner) 1.03 mm (Center)

Table 7. Results for 3mm x3mm x 0.9mm Lead TSSOP

8.0 SOLDER JOINT RELIABILITY

Reliability is an important aspect in the LFCSP design and its usage for various applications. The I/O pads in the LFCSP are not as compliant as a leaded package and will fail in second level reliability sooner but are more than adequate for the use conditions outlined in this section. Conditions used for temperature cycling are 15/15/15/15 minutes ramp/dwell.

8.1 Reliability Testing

The primary failure mechanism in solder joints is fatigue caused by thermal cycling. This mechanism occurs as a result of repeated exposure to changes in temperature experienced by the solder joints in operation. When solder undergoes an increase in temperature (i.e. change in load), plastic deformation (creep) first occurs. This creep causes an increase in stress within the solder, which increases to plastic yielding (fracture) if the load increases beyond the yield strength of the solder. If the load is maintained at a stable level (or temperature), stress relaxation will occur and all stresses within the solder will completely relax. If the load is then removed and maintained at a stable level, similar stress are imposed on the solder until stress relaxation again occurs. The stress imposed on the solder by the increase and decrease in load causes fatigue damage, which is not repairable and accumulates as the solder is exposed to repeated load cycles.

8.2 Reliability of Sn63/Pb37 and Sn95.5/Ag4.0Cu0.5 Solder joints in 7mm x 7mm LFCSP

PCB layout/land sizes were based on the requirements of IPC-SM-782. Devices with SnPb and Pb-Free lead finish were assembled in a daisy chain layout to enable continuous measurement of joint resistance during temperature cycling. Temperature cycling conditions best suited are: Slow Ramp Rate i.e. slow change in temperature, to allow the solder to “creep” and; Long Dwell times to allow stress relaxation. Failures occurred due to open circuit solder joints resulting from fatigue damage. The test conditions for *Consumer, Computer*, and *Telecom* applications are shown in Table 8.

Application	Typical Operating	Cycles / Year	Typical Service	Delta T	Max Temp
Consumer	+20°C/+55°C	365	1-3 yrs	35°C	55°C
Computer	+25°C/+45°C	1460	5 yrs	20°C	45°C
Telecom	+10°C/+45°C	365	7-20 yrs	35°C	45°C

Table 8. Typical Use Categories and Conditions as Per IPC-SM-785

Resistance greater than 300 ohms was classified as OPEN. Results were then plotted on a Weibull distribution and typical Weibull characteristics determined. Using the modified Coffin Manson equation (Norris Landzberg model), comparisons were made with typical use conditions. Results for each solder type, as shown in Table 9, demonstrate the package meets and exceeds the requirements for many use categories in tin/lead and lead free solder applications.

SOLDER TYPE	LEAD MATERIAL	CYCLES TO FIRST FAIL	TYPICAL LIFE (YRS)
	Consumer		
Sn63/Pb37	Sn	18756	51
Sn63/Pb37	SnPb	28530	78
Sn95.5/Ag4.0Cu0.5	Sn	16680	46
Sn95.5/Ag4.0Cu0.5	SnPb	27919	76
	Computer		
Sn63/Pb37	Sn	98384	67
Sn63/Pb37	SnPb	149652	103
Sn95.5/Ag4.0Cu0.5	Sn	87494	60
Sn95.5/Ag4.0Cu0.5	SnPb	146450	100
	Telecom		
Sn63/Pb37	Sn	21502	59
Sn63/Pb37	SnPb	32706	90
Sn95.5/Ag4.0Cu0.5	Sn	19122	52
Sn95.5/Ag4.0Cu0.5	SnPb	32006	88

Table 9. Solder joint reliability in 7mm x 7mm LFCSP

Summary of solder joint reliability and Weibull characteristics are shown in Figure 26 and Table 10 respectively.

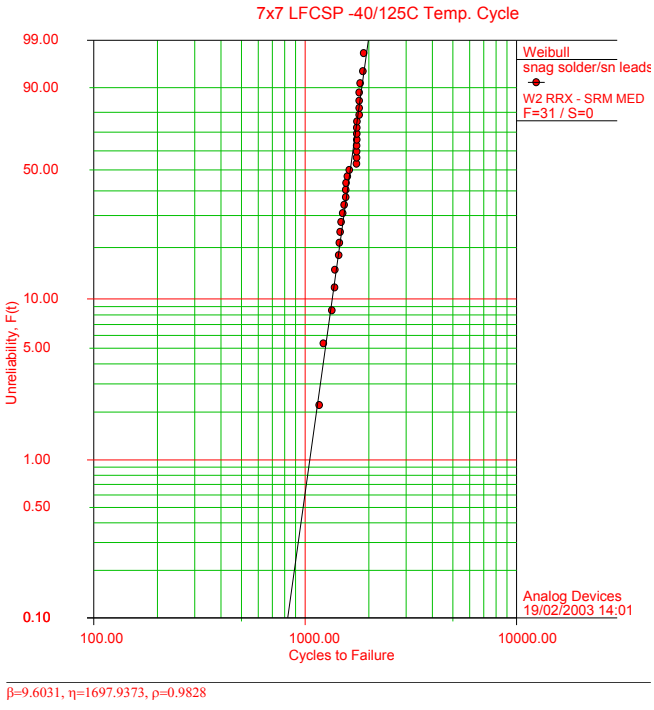


Fig. 26. Weibull Characteristics

Parameter	Description	Accelerated Test Result
β	Slope	9.6031
ρ	Correlation Coefficient	0.9828
η	Characteristic Life (63.2%)	1697 Cycles
T0.1%	Time to 0.1% Cumulative Failure	827 Cycles
T50.0%	Time to 50% Cumulative Failure	1634 Cycles

Table 10. Summary of Solder joint reliability

9.0 REFERENCES

9.1 Documents:

- Sample application note for microCSP by Analog Devices(Report AN-617)
- Application Notes for Surface Mount Assembly of Amkor's Microleadframe (MLF) Packages, September 2002
- Electrical Report from Amkor Technology: 7.0mmx7.0mmx1.4mm, 48 Lead LQFP, 3D Electrical Parasitic Parameters (Report EM-99-19), February 1999
- Electrical Report from Amkor Technology: 7.0mmx7.0mmx0.9mm 48 Lead MLP2, 3D Electrical Parasitic Parameters (Report EM-99-03), February 1999
- Electrical Report from Amkor Technology: 3.0mmx3.0mmx0.9mm 8 Lead TSSOP, 3D Electrical Parasitic Parameters (Report EM-98-57), October 1998
- Electrical Report from Amkor Technology: 3.0mmx2.0mmx0.85mm 8 Lead MLF, 3D Electrical Parasitic Parameters (Report EM-2000-011), July 2000
- Reliability Report from Analog Devices: Evaluation of Reliability of SnPb and SnAgCu Solder Joints In 7x7mm LFCSP Package, March 2003
- Thermal Report from Amkor Technology: 7 mm square body, 44 lead MicroLeadFrame Packages(TM-00-11), April 2000
- Lead Frame Chip Scale Package Rework Guidelines, Analog Devices

9.2 Websites:

- http://www.amkor.com/services/electrical/FAQ_3Dsoftware_data.pdf