

6 5 4 3 2 1

D

C

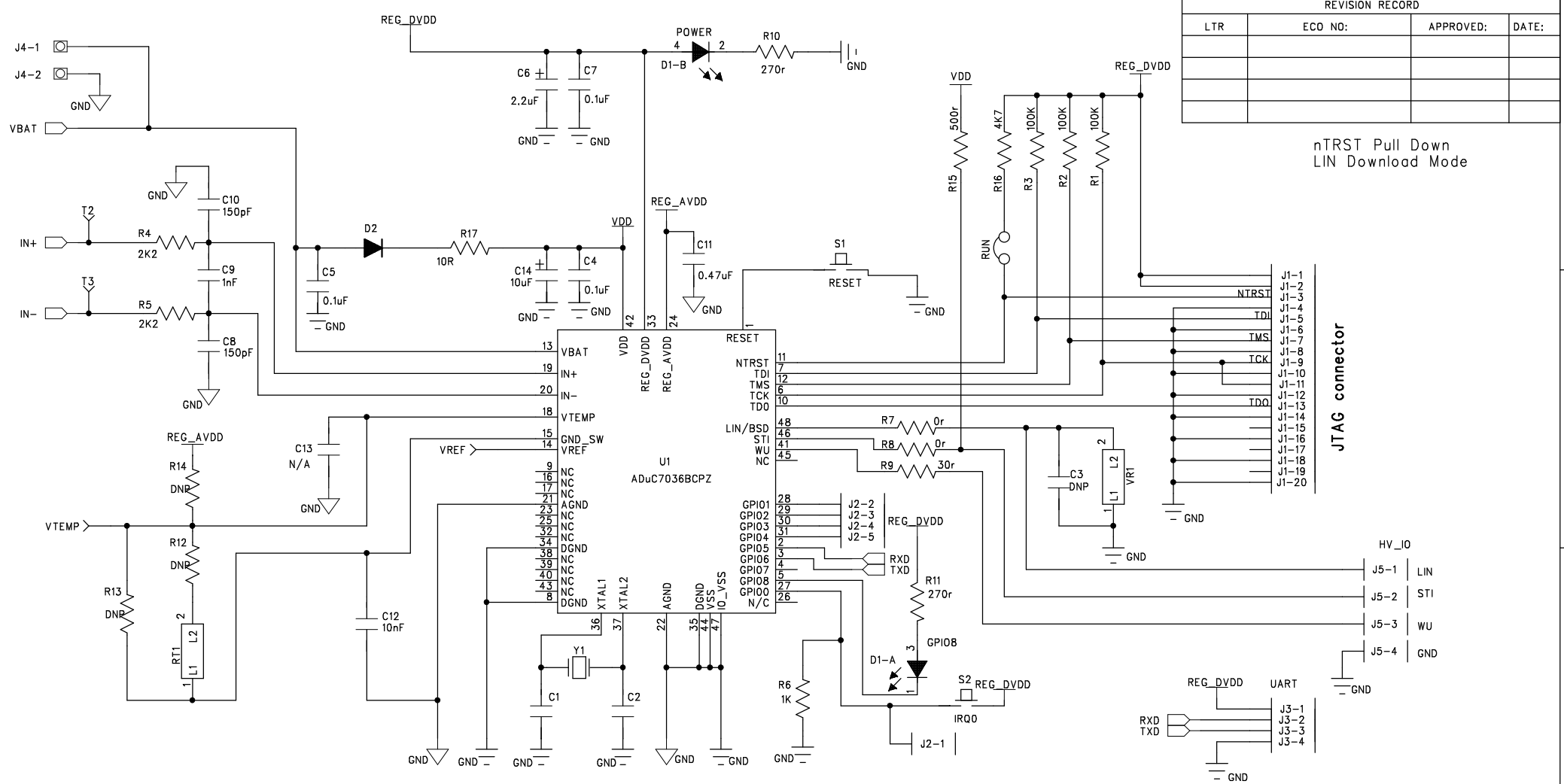
B

A

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

nTRST Pull Down
LIN Download Mode

JTAG connector



Notes

1. Prototype area to be included in board layout
2. 4 Layer PCB, Single tracking layer and 3 ground plane layers
3. Track VBAT separately to U1-VBAT and U1-VDD
4. Exposed paddle on LFCSP package is connected directly to ground plane layers
5. Overall board dimensions = 38mm X 63.5mm (approx.)
6. C12 is to be placed as close as possible to the GND_SW pin - 10nF recommended

COMPANY: **ANALOG DEVICES**

TITLE: **Battery Sensor Converter Applications Board Schematic**

DRAWN: Martin Murnane	DATED: FEB '08	CODE:	SIZE:	DRAWING NO:	REV:
CHECKED:	DATED:	EVAL-ADuC7036QSPZ			A
QUALITY CONTROL:	DATED:				
RELEASED:	DATED:	SCALE:	SHEET: 1 OF 1		