

6

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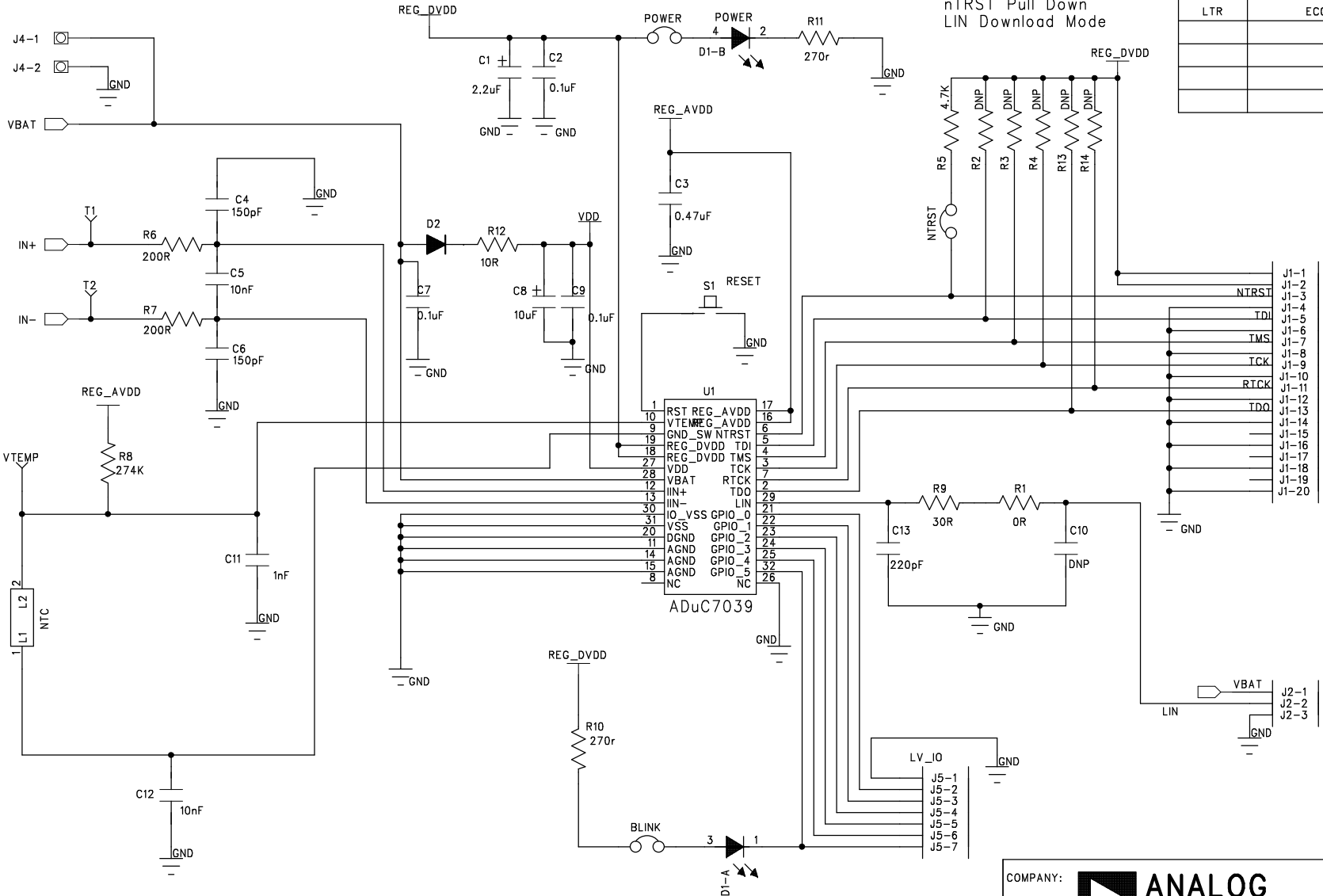
1

D

C

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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

JTAG connector

HV\_IO

### Notes

1. Prototype area to be included in board layout.
2. 4 Layer PCB, Single tracking layer and 3 ground plane layers.
3. Track VBAT separately to U1-VBAT and U1-VDD.
4. Paddle connected to ground.

COMPANY:  **ANALOG DEVICES**

TITLE: **Battery Sensor Converter Applications Board Schematic**

DRAWN: Martin Murnane	DATED: Oct '09	CODE:	SIZE:	DRAWING NO:	REV:
CHECKED:	DATED:	<b>EVAL-ADuC7039QSPZ</b>			<b>B</b>
QUALITY CONTROL:	DATED:				
RELEASED:	DATED:	SCALE:	SHEET: 1 OF 1		